Functional Safety Information

TMCS2100-Q1-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TMCS2100-Q1 (TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

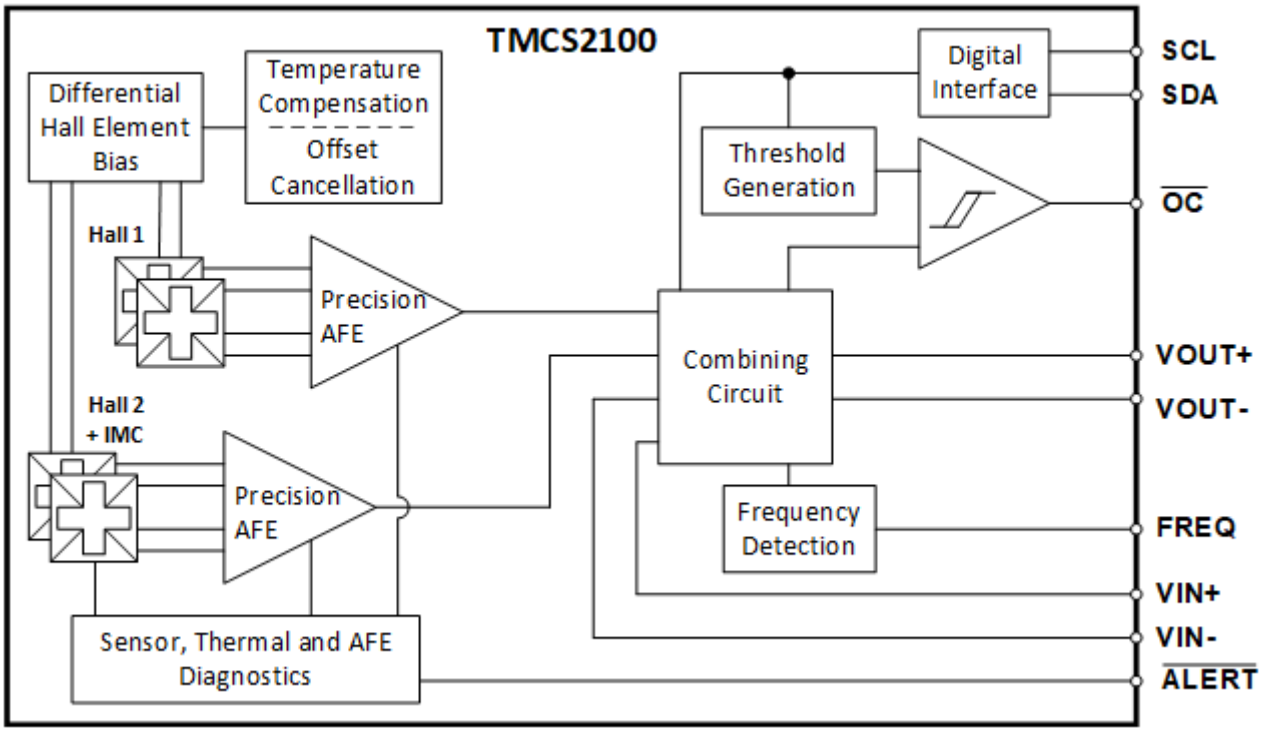

Figure 1-1. TMCS2100-Q1 Functional Block Diagram

The TMCS2100-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TMCS2100-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	3
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 140mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog and mixed ≤ 50V supply	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TMCS2100-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT± open (Hi-Z)	12
VOUT± stuck (high or low)	14
VOUT± functional, not in specification	40
SDA open (Hi-Z)	3
$\overline{\text{ALERT}}$ stuck (high or low)	4
FREQ open (Hi-Z)	22
$\overline{\text{OC}}$ false trip, failure to trip	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TMCS2100-Q1 (TSSOP package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +150°C
- V_S = 3V to 5.5V

4.1 TSSOP Pin FMA

Figure 4-1 shows the TMCS2100-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TMCS2100-Q1 datasheet.

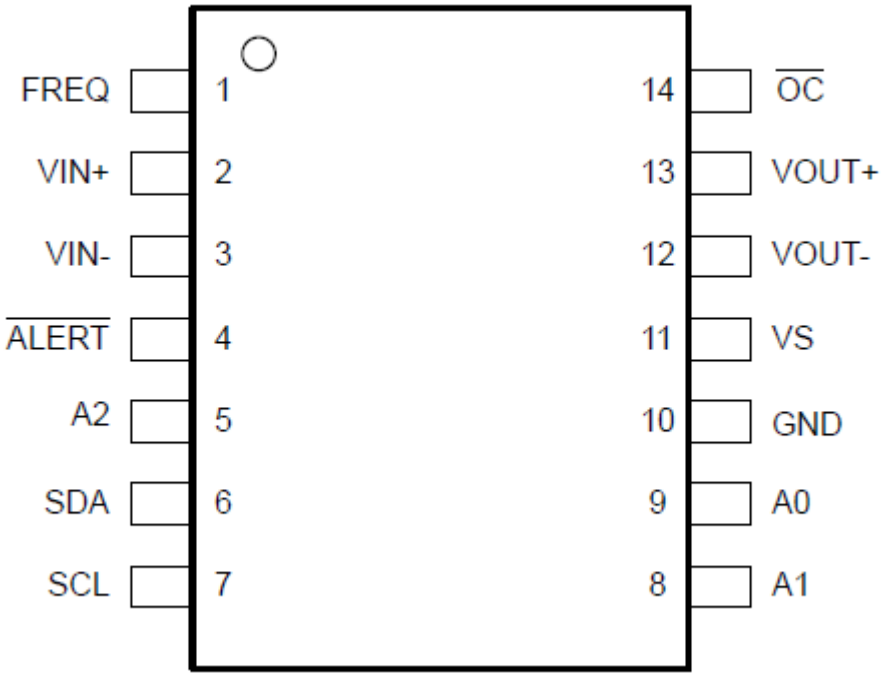

Figure 4-1. TMCS2100-Q1 Pin Diagram

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FREQ	1	Unable to provide frequency information.	B
IN+	2	Unexpected output.	B
IN-	3	Unexpected output.	B
$\overline{\text{ALERT}}$	4	Alert give false readings.	B
A2	5	Forces the device into secondary mode.	B
SDA	6	I2C communication to the device is lost.	B
SCL	7	I2C communication to the device is lost.	B
A1	8	Incorrect addresses potentially cause communication loss.	B
A0	9	Incorrect addresses potentially cause communication loss.	B
GND	10	Normal operation.	D
VS	11	Power supply is shorted to ground.	B
VOUT-	12	The output is short circuit limited.	A
VOUT+	13	The output is short circuit limited.	A
$\overline{\text{OC}}$	14	OC gives false readings.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FREQ	1	Unable to provide frequency information.	B
IN+	2	Normal operation.	D
IN-	3	Normal operation.	D
$\overline{\text{ALERT}}$	4	Alert is open; not able to read alert.	B
A2	5	Device detection as primary or secondary is unknown.	B
SDA	6	I2C communication to the device is lost.	B
SCL	7	I2C communication to the device is lost.	B
A1	8	Inability to communicate with the device due to unknown address.	B
A0	9	Inability to communicate with the device due to unknown address.	B
GND	10	Ground is floating. The output is incorrect as the output is no longer referenced to GND.	B
VS	11	No power to the device.	B
VOUT-	12	Normal operation.	D
VOUT+	13	Normal operation.	D
$\overline{\text{OC}}$	14	OC is open; inability to read OC.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FREQ	1	IN+	Unexpected output; similar to shorting IN+ to VS or GND.	B
IN+	2	IN-	Normal operation.	D
IN-	3	$\overline{\text{ALERT}}$	Unexpected output; similar to shorting IN- to VS or GND.	B
$\overline{\text{ALERT}}$	4	A2	Can change whether the device is primary or secondary.	B
A2	5	SDA	SDA can be forced high or low; affecting communication.	B
SDA	6	SCL	Communication errors.	B
SCL	7	A1	SCL can be forced high or low; affecting communication.	B
A1	8	A0	Can short power to ground, depending on the assigned address.	B
A0	9	GND	Normal operation.	D
GND	10	VS	Supply is shorted to ground.	B
VS	11	VOUT-	The output is short circuit limited.	A
VOUT-	12	VOUT+	The device becomes unstable and there are oscillations.	B
VOUT+	13	$\overline{\text{OC}}$	The output is short circuit limited.	A
$\overline{\text{OC}}$	14	FREQ	OC provides false readings.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FREQ	1	Loses frequency information.	B
IN+	2	Incorrect output.	B
IN-	3	Incorrect output.	B
$\overline{\text{ALERT}}$	4	The alert pin is stuck high; current draw is potentially too high when triggered.	B
A2	5	The device is forced into primary mode.	B
SDA	6	I2C communication to the device is lost.	B
SCL	7	I2C communication to the device is lost.	B
A1	8	Incorrect addresses potentially cause communication loss.	B
A0	9	Incorrect addresses potentially cause communication loss.	B
GND	10	Supply is shorted to ground.	B
VS	11	Normal operation.	D
VOUT-	12	The output is short circuit limited.	A
VOUT+	13	The output is short circuit limited.	A
$\overline{\text{OC}}$	14	The OC pin is stuck high; current draw is potentially too high when triggered.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 5, 2026 to August 16, 2026 (from Revision A (February 2026) to Revision B (August 2026)) **Page**

- Removed the NDA information banner....2
- Updated GPN to TMCS2100-Q1....2
- Updated pin diagram....5

Changes from August 5, 2025 to February 5, 2026 (from Revision * (August 2025) to Revision A (February 2025)) **Page**

- Added the NDA information banner....2

- Updated the values in the *Die Failure Modes and Distribution* table.....4

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