Functional Safety Information

TPS1HC120-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS1HC120-Q1 (DYC (SOT, 8) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

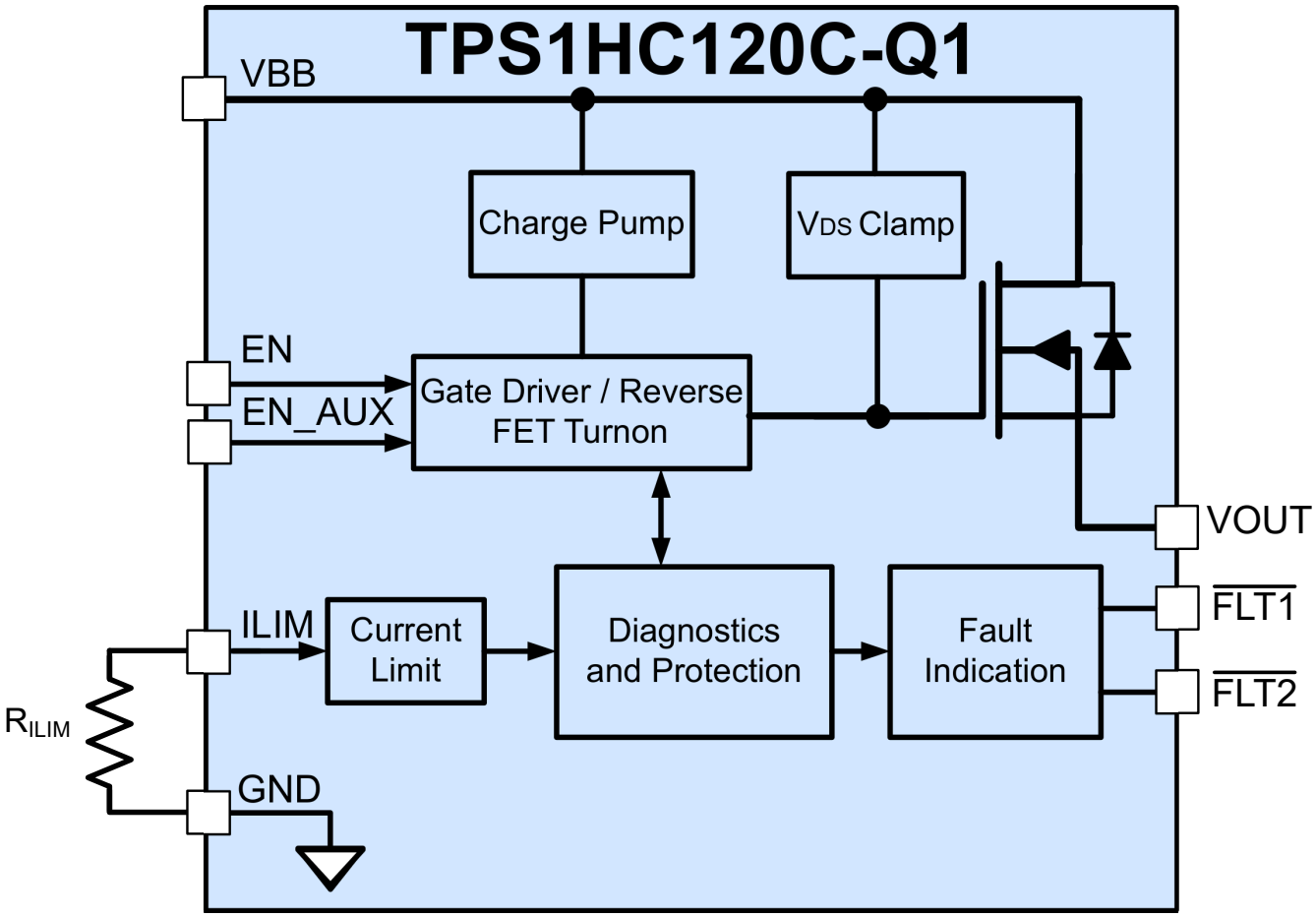

Figure 1-1. Functional Block Diagram

The TPS1HC120-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS1HC120-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	21
Die FIT rate	19
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS1HC120-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	20
VOUT stuck ON	10
VOUT functional, not within specified voltage or timing	50
Diagnostics not within specification	10
Protection function fails to trigger	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS1HC120-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS1HC120-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS1HC120-Q1 datasheet.

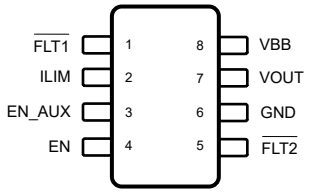

Figure 4-1. Pin Diagram (8-Pin SOT (Top View), C Version)

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device pins are connected per the recommendation in the datasheet, including pullup and pulldown resistors, as needed.
- The datasheet recommendations for operating conditions, external component selection, and PCB layout are followed.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FLT1	1	The reported current limit, short circuit, or thermal shutdown status is potentially erroneous.	B
ILIM	2	The current limit is set at 2.1A typical, as per the datasheet.	C
EN_AUX	3	No effect if EN is not also shorted to ground.	D
EN	4	The FET is turned off.	B
FLT2	5	The reported ON state open load fault status is potentially erroneous.	B
GND	6	Any GND network, connected for protection, is bypassed.	B
VOUT	7	The current limit of the device engages, and thermal protection turns off the FET.	B
VBB	8	The output stages are not powered, and the FET does not turn ON.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FLT1	1	Current limit, short circuit, or thermal shutdown condition is not reported.	B
ILIM	2	Current limit is set at 2.1A as per datasheet.	C
EN_AUX	3	No effect if EN1 is also not open circuited.	D
EN	4	The FET is turned off.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FLT2	5	ON state open load fault is not reported.	B
GND	6	The loss of ground detection engages, and the device turns OFF.	B
VOUT	7	During the ON state of the device, output is disconnected.	B
VBB	8	The device is not powered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
FLT1	1	2 (ILIM)	Current limit and fault response are not predictable.	B
ILIM	2	3 (EN_AUX)	Current limit value is not predictable.	B
EN_AUX	3	4 (EN)	No effect.	D
FLT2	5	6 (GND)	The reported ON state open load fault status is potentially erroneous.	B
GND	6	7 (VOUT)	The current limit of the device engages, and thermal protection turns off the FET.	B
VOUT	7	8 (VBB)	The output is pulled to the supply voltage.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
FLT1	1	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
ILIM	2	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
EN_AUX	3	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
EN	4	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
FLT2	5	If pin voltage exceeds the absolute maximum rating, device damage is possible due to voltage breakdown on the ESD circuit.	A
GND	6	The supply power is bypassed, and the device stays OFF.	B
VOUT	7	The output is pulled to the supply voltage.	B
VBB	8	No effect.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

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