Functional Safety Information

LM34938-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

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1 Overview

This document contains information for the LM34938-Q1 (RHA (VQFN, 40) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

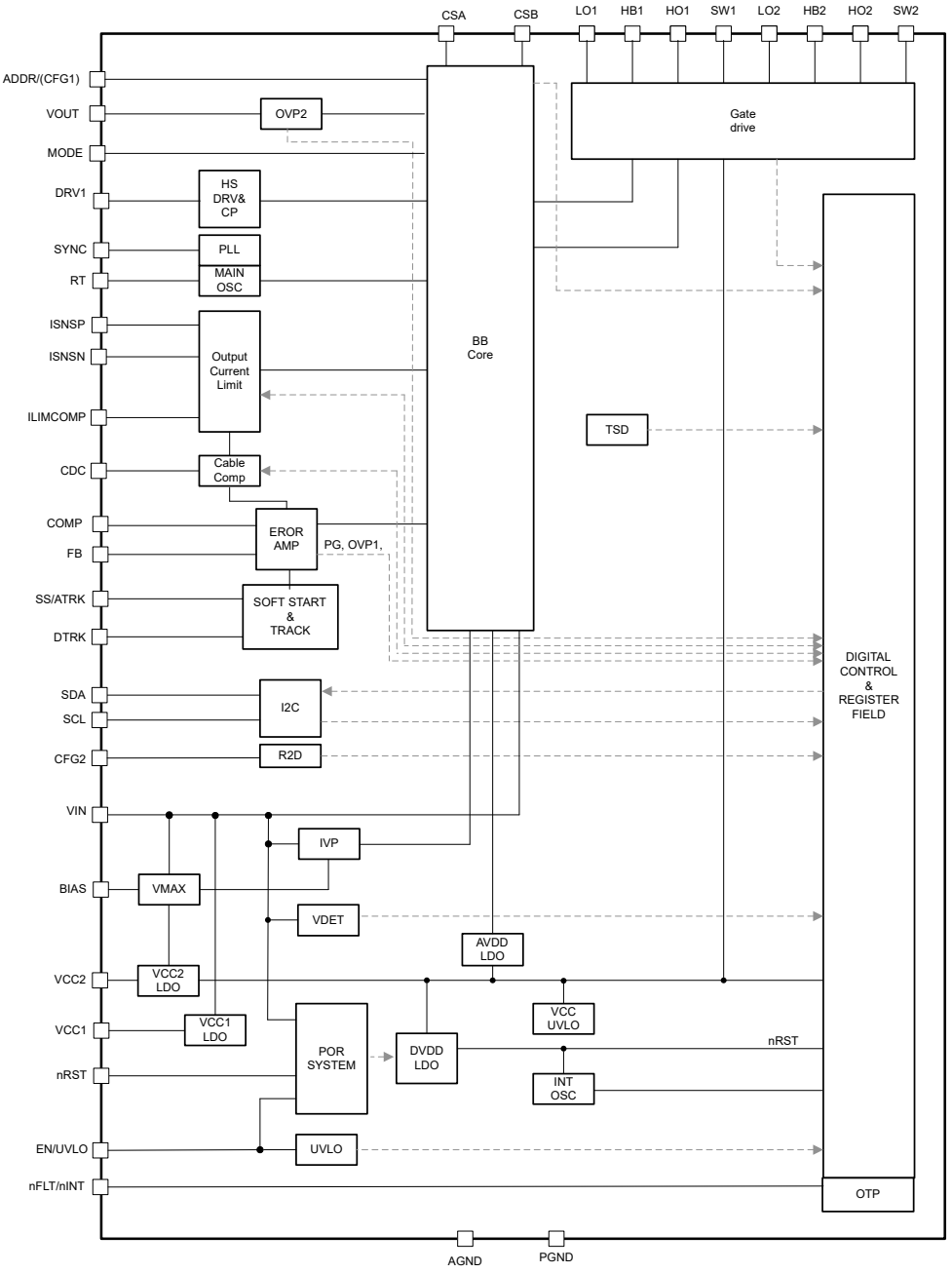

Figure 1-1. Functional Block Diagram of the LM34938-Q1

The LM34938-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LM34938-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	30
Die FIT rate	5
Package FIT rate	25

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1400mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs analog and mixed HV >50V supply	N/A	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LM34938-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
HO1 and HO2 or LO1 and LO2 gate drivers are stuck on	10
HO1 and HO2 or LO1 and LO2 gate drivers are stuck off	20
HO1 and HO2 or LO1 and LO2 gate drivers are Hi-Z	3
VCC1 and VCC2 LDO output voltage out of specification	10
DRV1 or nFLT false switching	3
VOUT voltage out of specification	30
Average current out of specifications	14
Digital control malfunctions or electrical parameters are out of specification	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM34938-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM34938-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LM34938-Q1 datasheet.

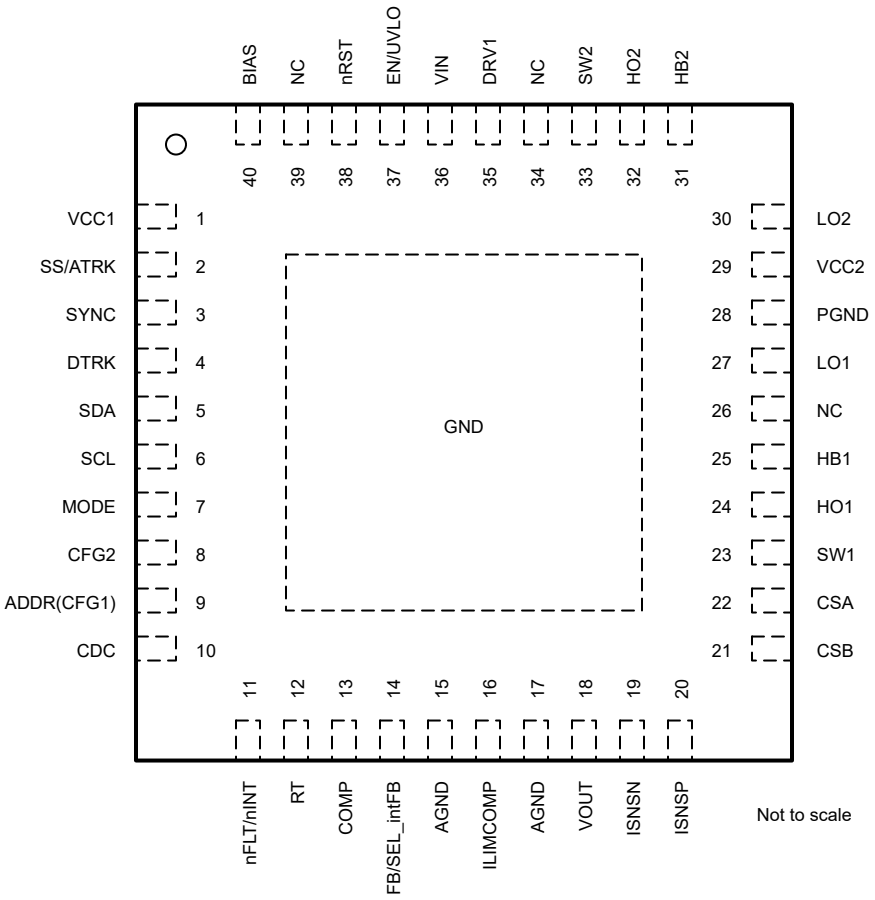

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the LM34938-Q1 datasheet.
- For the analysis, the typical application with V_I = 9V to 36V, V_O = 5V to 32V and P_O = 60W shown in the *Typical Application* section of the LM34938-Q1 datasheet is considered.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC1	1	When the VCC1 pin is disabled through logic and connected through a resistor to GND: There is no impact to the device.	D
		When the VCC1 pin is disabled through logic and connected to the VCC2 pin: The device does not start.	B
		When the VCC1 pin is enabled: VCC1 operates in current limit at 0V.	B
SS/ATRK	2	The device regulates the output voltage to 0V.	B
SYNC	3	When the SYNC pin is not used and connected to GND: There is no effect to the device.	D
		When the SYNC pin is not used and connected to the VCC2 pin: The device does not start.	B
		When the SYNC pin is configured as the clock input signal: There is no SYNC functionality.	C
		When the SYNC pin is configured as the clock output signal: There is no SYNC signal available to the other phase.	C
DTRK	4	When the DTRK pin is used: There is a loss of the functionality of DTRK, the device regulates to the internal reference.	B
		When the DTRK pin is not used and connected to GND: There is no effect to the device.	D
		When the DTRK pin is not used and connected to the VCC2 pin: The device does not start.	B
SDA	5	Communication with the device is not possible.	B
SCL	6	Communication with the device is not possible.	B
MODE	7	Power save mode is enabled.	C
		When the MODE pin is connected to the VCC2 pin: The device does not start.	B
CFG2	8	When the CFG2 pin is used at nRST rise: There is a possible configuration change from the expected configuration to configuration 1, see the *CFG2 Pin (R2D-CH2) Configuration Overview* table in the datasheet.	C
		When the CFG2 pin is used after start-up: There is no effect to the device.	D
ADDR(CFG1)	9	When the ADDR(CFG1) pin is shorted at nRST rise: I2C is enabled, the device address is set to 0x6A, and the slope compensation is set according configuration 1, see the *ADDR Pin (R2D-CH1 Configuration Overview* table in the datasheet.	C
		When the ADDR(CFG1) pin is shorted after start-up: There is no effect to the device.	D
CDC	10	When the CDC pin is configured as current monitor: There is no output signal.	B
		When the CDC pin is configured as cable drop compensation: There is no load current dependent offset on the output voltage of the converter.	B
		When the CDC pin is disabled: There is no impact to the device.	D
nFLT/nINT	11	The pin permanently indicates a fault or interrupt.	B
RT	12	The converter switches at maximum frequency (≅2.5MHz).	B
COMP	13	If the MODE pin is low: The converter does not switch.	B
		If the MODE pin is high: The inductor current goes to the negative current limit until IVP is triggered.	B
FB/SEL_intFB	14	With external feedback (FB): The output voltage rises until the device triggers overvoltage protection.	B
		When the internal FB is used, and the pin is connected to the VCC2 pin: The device does not start.	B
AGND	15	There is no effect to the device. The device operates normally.	D
ILIMCOMP	16	The pin is used: The current loop is unstable, or the average current limit is not available.	C
		The pin is connected to the VCC2 pin: The device does not switch.	B
AGND	17	There is no effect to the device. The device operates normally.	D
VOUT	18	The converter operates in peak or average current limit and the output voltage is shorted to GND.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
ISNSN	19	The differential voltage on the sense amplifier is too high. Potential damage to the pin.	A
ISNSP	20	The differential voltage on the sense amplifier is too high. Potential damage to the pin.	A
CSB	21	The differential voltage on the sense amplifier is too high. Potential damage to the pin.	A
CSA	22	The differential voltage on the sense amplifier is too high. Potential damage to the pin.	A
SW1	23	There is no output voltage. Potential damage to the device.	A
HO1	24	There is no output voltage. The buck high-side FET is off.	B
HB1	25	There is no supply for the gate driver. The device is in standby (BOOT_UV).	B
NC	26	There is no effect to the device. The device operates normally.	D
LO1	27	The operation is non-synchronous in buck-mode and partially in buck-boost mode. Potential damage to the external FET due to power dissipation.	C
PGND	28	There is no effect to the device. The device operates normally.	D
VCC2	29	The device does not start.	B
LO2	30	The boost low-side FET is always off. There is no boost operation.	C
HB2	31	There is no supply for the gate driver. The device is in standby (BOOT_UV).	B
HO2	32	The operation is non-synchronous in boost-mode and partially in buck-boost mode. Potential damage to the external FET due to power dissipation.	C
SW2	33	There is no output voltage. Potential damage to the device.	A
NC	34	There is no effect to the device. The device operates normally.	D
DRV1	35	When DRV1 is used: There is no system output.	B
		When DRV1 is not used: There is no effect to the device.	D
VIN	36	The device is in shutdown or standby.	B
EN/UVLO	37	The device is in shutdown or standby.	B
nRST	38	The device is in shutdown.	B
NC	39	There is no effect to the device. The device operates normally.	D
BIAS	40	There is no effect to the device. The efficiency of the converter is potentially reduced, or the thermal shutdown triggers.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC1	1	When the VCC1 pin is disabled: there is no impact to the device.	D
		When the VCC1 pin is enabled: VCC1 oscillates. Potential damage to the device.	A
SS/ATRK	2	There is a rapid start-up with potentially high inrush current to the converter.	C
SYNC	3	Unstable switching frequency is possible.	C
DTRK	4	Erratic operation is possible.	B
SDA	5	Communication with the device is not possible.	B
SCL	6	Communication with the device is not possible.	B
MODE	7	PSM/FPWM is undefined.	C
CFG2	8	When the open happens before nRST rise: At nRST rise, the configuration of the device is undefined.	C
		When the CFG2 pin open happens after start-up: There is no effect to the device.	D
ADDR (CFG1)	9	When the ADDR(CFG1) pin open happens before nRST rise: At nRST rise, the address and configuration of the device are undefined.	C
		When the ADDR(CFG1) pin open happens after start-up: There is no effect to the device.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
CDC	10	When the CDC pin is configured as current monitor: There is no signal to the system.	C
		When the CDC pin is configured as cable drop compensation: The maximum offset on the output is undefined and independent of the load current.	B
		When the CDC pin is disabled: There is no impact to the device.	D
nFLT/nINT	11	The pin does not indicate a fault or interrupt.	B
RT	12	The lowest switching frequency is selected and the converter is potentially unstable.	C
COMP	13	The voltage loop is unstable. Potential damage to the external components or the device.	A
FB/SEL_intFB	14	The output voltage is regulated to the overvoltage protection (OVP) level or 0V.	B
AGND	15	Increased current flow at the internal AGND/PGND connection. The operation is potentially erratic. Potential damage to the device.	A
ILIMCOMP	16	The current loop is unstable.	C
AGND	17	Increased current flow at the internal AGND/PGND connection. The operation is potentially erratic. Potential damage to the device.	A
VOUT	18	With an internal FB divider: There is no regulation of the output voltage. Potential damage to the external components or the device.	A
		With an external FB divider: There is no overvoltage protection (OVP), and no slope compensation. Potential unstable current loop.	B
ISNSN	19	If the average current function is not used, there is no effect to the device.	D
		There is no average current limit function.	B
ISNSP	20	If the average current function is not used, there is no effect to the device.	D
		There is no average current limit function.	B
CSB	21	There is erratic switching behavior. There is a loss of regulation. Potential damage to the device or external components.	A
CSA	22	There is erratic switching behavior. There is a loss of regulation. Potential damage to the device or external components.	A
SW1	23	There is a loss of operation or regulation, or the device turns off.	B
HO1	24	There is no output voltage. The buck high-side FET is off.	B
HB1	25	There is no supply for the gate driver. The device is in standby (BOOT_UV).	B
NC	26	There is no effect to the device. The device operates normally.	D
LO1	27	The operation is non-synchronous in buck-mode and partially in buck-boost mode. Potential damage to the external FET due to power dissipation.	C
PGND	28	Increased current flow at the internal AGND/PGND connection. The operation is potentially erratic. Potential damage to the device.	A
VCC2	29	The internal supply us unstable. The operation is erratic.	B
LO2	30	The boost low-side FET is always off, no boost operation.	B
HB2	31	There is no supply for the gate driver. The device is in standby (BOOT_UV).	B
HO2	32	The operation is non-synchronous in boost-mode and partially in buck-boost mode. Potential damage to the external FET due to power dissipation.	C
SW2	33	There is a loss of operation, or the device turns off.	B
NC	34	There is no effect to the device. The device operates normally.	D
DRV1	35	When the DRV1 pin is used: There is no output voltage to the load.	B
		When the DRV1 pin is not used: There is no effect to the device.	D
VIN	36	The device is not supplied. The device does not start-up.	B
EN/UVLO	37	The device turns on or off unpredictably.	B
nRST	38	The device turns on or off unpredictably.	B
NC	39	There is no effect to the device. The device operates normally.	D
BIAS	40	The efficiency of the device is potentially reduced, or there is a thermal shutdown.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VCC1	1	SS/ATRK (2)	When the VCC1 pin is enabled: There is no functionality of SS/ATRK.	C
			When the VCC1 pin is disabled and tied to GND: The output is regulated to 0V.	B
			When the VCC1 pin is disabled and tied to the VCC2 pin: There is no functionality of SS/ATRK.	C
SS/ATRK	2	SYNC (3)	When the SYNC pin is connected to GND: The device does not start-up.	B
			When the SYNC pin is connected to the VCC2 pin: There is no functionality of SS/ATRK.	C
			When the SYNC pin is driven from external signal: Erratic functionality.	B
			When the SYNC pin is configured as output: The output voltage is modulating with the SYNC signal.	B
SYNC	3	DTRK (4)	When the SYNC and DTRK pins are connected to the same signal: There is no effect to the device.	D
			When the SYNC or DTRK pins are driven from an external signal: The output voltage and frequency are modulated with the external signal.	B
			When the SYNC pin is configured as output: The output voltage of the converter is at 50% due to the DTRK functionality.	B
DTRK	4	SDA (5)	The output voltage is potentially modulated with the I2C communication, or I2C communication is not possible.	B
SDA	5	SCL (6)	I2C communication is not possible, so the device does not start-up.	B
SCL	6	MODE (7)	I2C communication is not possible, so the device does not start-up.	B
MODE	7	CFG2 (8)	When nRST rises: Configuration 1 or 16 are selected dependent on the voltage at MODE pin.	B
			The short is applied after start-up: The PFM or FPWM selection is unclear.	B
			When one pin is connected to VCC2, and the other pin is connected to GND: The device does not start.	B
CFG2	8	ADDR(CFG1) (9)	The setting of the ADDR(CFG1) pin defines if the device is operating in configuration 1 or 16, see the datasheet.	B
			When the short is applied after start-up: There is no effect to the device.	D
			When one pin is connected to the VCC2 pin, and the other pin is connected to GND: The device does not start.	B
ADDR(CFG1)	9	CDC (10)	When ADDR(CFG1) is connected to GND, see the pin to GND short table.	B/D
			When ADDR(CFG1) is connected to VCC2 and the CDC pin is configured as current monitor: The system gets a current signal indicated that is at the highest possible level independent of the real value measured.	B
			When ADDR(CFG1) is connected to VCC2 and the CDC pin is configured as cable drop compensation: The maximum offset on the output is undefined and independent of the load current.	B
			When ADDR(CFG1) is connected to VCC2 and the CDC pin is disabled (and connected to GND), see the pin to GND short table.	C/D
CDC	10	nFLT/nINT (11)	If a pullup is connected to the nFLT/nINT pin, and the CDC pin is configured as cable drop compensation: The output voltage is somewhat higher than set by the measured output current.	C
			If a pullup is connected to the nFLT/nINT pin, and the CDC pin is configured as current monitor: The system gets a current signal indication that is higher than the measured output current.	C
			If the CDC pin is disabled (and connected to GND): The nFLT/nINT permanently indicates a fault.	B
nFLT/nINT	11	RT (12)	If a pullup is connected to the nFLT/nINT pin: The switching frequency decreases.	C
			Whenever the nFLT/nINT pin is pulled low, the converter operates at maximum switching frequency and can become unstable.	B
RT	12	COMP (13)	The switching frequency is unstable. The voltage loop is potentially unstable.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
COMP	13	FB/SEL_intFB (14)	When there is an external FB divider: The operation is erratic.	B
			When there is an internal FB divider, and the pin is connected to the VCC2 pin: The operation is in current limit until OVP is triggered.	B
FB/SEL_intFB	14	AGND (15)	See pin to GND short table.	B
AGND	15	ILIMCOMP (16)	See pin to GND short table.	B/C
ILIMCOMP	16	AGND (17)	See pin to GND short table.	B/C
AGND	17	VOUT (18)	The converter operates in peak or average current limit and the output voltage is shorted to GND.	B
VOUT	18	ISNSN (19)	When the ISNSN pin is connected to GND: The device operates in peak or average current limit and the output voltage is shorted to GND.	B
			With input sensing: The differential voltage on the ISNSx pin is potentially too high.	A
			With output sensing: The average current limit (sense line shorted) is potentially inaccurate.	C
ISNSN	19	ISNSP (20)	There is no average current limit function.	B
ISNSP	20	CSB (21)	The differential voltage on the sense amplifier is too high. Potential damage to one of the pins.	A
CSB	21	CSA (22)	There is no peak current limit function.	B
CSA	22	SW1 (23)	The peak current limit (sense line shorted) is potentially inaccurate.	C
SW1	23	HO1 (24)	The device is in standby (BOOT_UV).	B
HO1	24	HB1 (25)	The device is in standby (BOOT_UV).	B
HB1	25	NC (26)	There is no effect to the device. The device operates normally.	D
NC	26	LO1 (27)	There is no effect to the device. The device operates normally.	D
LO1	27	PGND (28)	The operation is non-synchronous in buck-mode and partially in buck-boost mode. Potential damage to the external FET due to power dissipation.	C
PGND	28	VCC2 (29)	The device does not start.	B
VCC2	29	LO2 (30)	The device is in standby or shuts down. (The VCC2 pin is pulled to ground when the LO2 pin is pulled low.)	B
LO2	30	HB2 (31)	At startup the device stays in standby (BOOT_UV)	B
			After startup potential damage due to overvoltage on pin LO2.	A
HB2	31	HO2 (32)	The device is in standby (BOOT_UV).	B
HO2	32	SW2 (33)	The device is in standby (BOOT_UV).	B
SW2	33	NC (34)	There is no effect to the device. The device operates normally.	D
NC	34	DRV1 (35)	There is no effect to the device. The device operates normally.	D
DRV1	35	VIN (36)	If DRV1 is unused, there is no effect to the device. The device operates normally.	D
			If DRV1 is used, the internal MOSFET to GND gets possibly damaged.	A
VIN	36	EN/UVLO (37)	The UVLO function is lost and only VDET disables the device	C
EN/UVLO	37	nRST (38)	There is a loss of the control of the EN/UVLO pin, and the device is in standby or the device is on.	C
nRST	38	NC (39)	There is no effect to the device. The device operates normally.	D
NC	39	BIAS (40)	There is no effect to the device. The device operates normally.	D
BIAS	40	VCC1 (1)	There is no effect to the device. The efficiency of the converter is potentially reduced, or the thermal shutdown triggers.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to $V_{(VIN)}$

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VCC1	1	There is device damage due to high voltage.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to $V_{(VIN)}$ (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SS/ATRK	2	There is device damage due to high voltage.	A
SYNC	3	There is device damage due to high voltage.	A
DTRK	4	There is device damage due to high voltage.	A
SDA	5	There is device damage due to high voltage.	A
SCL	6	There is device damage due to high voltage.	A
MODE	7	There is device damage due to high voltage.	A
CFG2	8	There is device damage due to high voltage.	A
ADDR(CFG1)	9	There is device damage due to high voltage.	A
CDC	10	There is device damage due to high voltage.	A
nFLT/nINT	11	There is device damage due to high voltage.	A
RT	12	There is device damage due to high voltage.	A
COMP	13	There is device damage due to high voltage.	A
FB/SEL_intFB	14	There is device damage due to high voltage.	A
AGND	15	There is device damage due to high voltage to PGND.	A
ILIMCOMP	16	There is device damage due to high voltage.	A
AGND	17	There is device damage due to high voltage to PGND.	A
VOUT	18	The converter is bypassed.	B
ISNSN	19	With input sensing: There is no average current limit.	B
		With output sensing: The differential voltage between the ISNSP and ISNSN pins is potentially too high.	A
ISNSP	20	With input sensing: The input sensing (sense line shorted) is inaccurate.	C
		With output sensing: The differential voltage between the ISNSP and ISNSN pins is potentially too high.	A
CSB	21	The buck high-side FET is bypassed. The operation is erratic. There is potentially damage to the device due to high differential voltage between the CSA and CSB pins.	A
CSA	22	The buck high-side FET is bypassed. The operation is erratic. There is potentially damage to the device due to high differential voltage between the CSA and CSB pins.	A
SW1	23	The buck high-side FET is bypassed. The operation is erratic.	B
HO1	24	There is device damage due to high voltage.	A
HB1	25	There is device damage due to high voltage.	A
NC	26	There is no effect to the device. The device operates normally.	D
LO1	27	There is device damage due to high voltage.	A
PGND	28	There is device damage due to high voltage to AGND.	A
VCC2	29	There is device damage due to high voltage.	A
LO2	30	There is device damage due to high voltage.	A
HB2	31	There is device damage due to high voltage.	A
HO2	32	There is device damage due to high voltage.	A
SW2	33	The boost low-side FET is potentially damaged.	B
NC	34	There is no effect to the device. The device operates normally.	D
DRV1	35	The external disconnect FET is potentially damaged.	B
VIN	36	There is no effect to the device. The device operates normally.	D
EN/UVLO	37	There is no UVLO function. The nRST pin defines standby and enable.	D
nRST	38	The nRST pin is always enabled.	D
NC	39	There is no effect to the device. The device operates normally.	D
BIAS	40	When the BIAS pin is connected to the VOUT pin: VIN and VOUT are shorted.	B
		When the BIAS pin is connected to VIN: There is no effect to the device.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

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