Functional Safety Information

TPS6281x
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview 2
2 Functional Safety Failure In Time (FIT) Rates 3
3 Failure Mode Distribution (FMD) 4
4 Pin Failure Mode Analysis (Pin FMA) 5
5 Revision History 6

1 Overview

This document contains information for TPS62810, TPS62811, TPS62812, and TPS62813 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

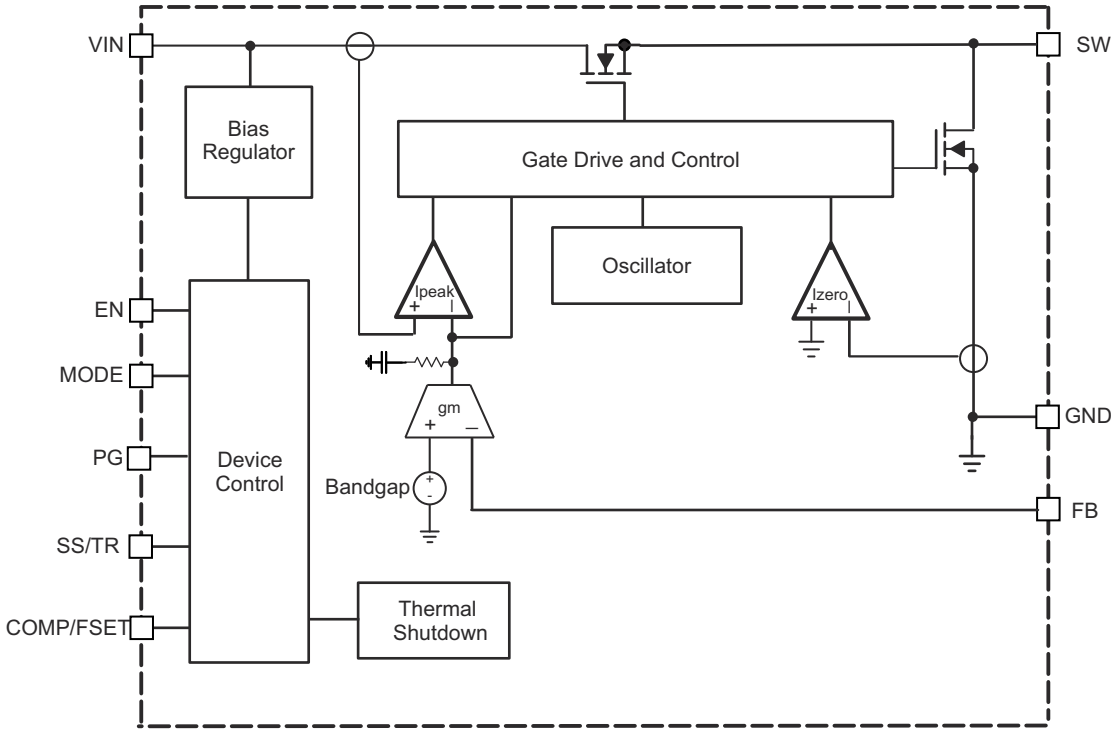

Figure 1-1. Functional Block Diagram

TPS6281x were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS6281x based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11.
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2.

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	5
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	25 FIT	55 °C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS6281x in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35
SW output not in specification – voltage or timing	45
SW power HS or LS FET stuck on	10
PG false trip or fails to trip	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS6281x. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1shows the TPS6281x pin diagram for the VQFN package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS6281x datasheet.

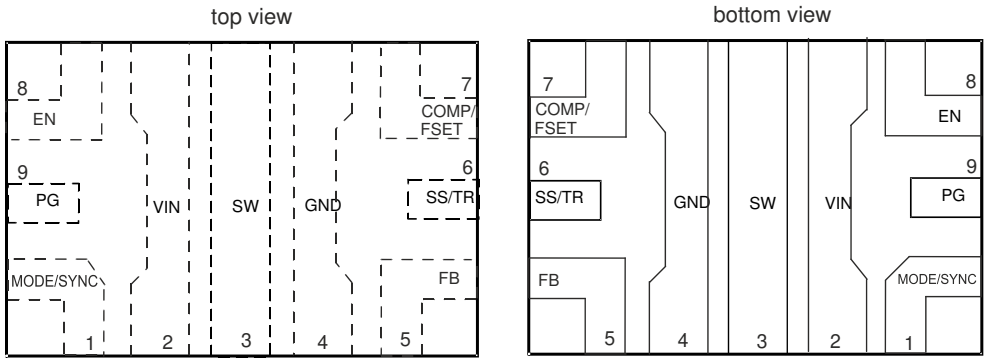

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used according to the typical application, refer to the *Simplified Schematics* section in the TPS6281x datasheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MODE/SYNC	1	The device functions as intended.	D
VIN	2	The device does not power up.	B
SW	3	The device is potentially damages.	A
GND	4	There is no effect to the device.	D
FB	5	The output voltage is regulated to V_{IN} (100% mode).	B
SS/TR	6	The device is not functional.	B
COMP/FSET	7	The device functions as intended.	D
EN	8	The device functions as intended.	D
PG	9	The device functions as intended.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MODE/SYNC	1	The operation of the device is undetermined.	B
VIN	2	The device does not power up.	B
SW	3	The device is not functional, open loop operation.	B
GND	4	The device is not functional.	B
FB	5	The output voltage behavior is undetermined; open loop operation.	B
SS/TR	6	The device functions as intended.	D
COMP/FSET	7	The device functions as intended.	D
EN	8	The operation of the device is undetermined; the device potentially power up or potentially does not power up.	B
PG	9	The device functions as intended.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
MODE/SYNC	1	PG	The device runs FPWM mode once the PG pin is high impedance.	B
FB	5	SS/TR	The operation of the device is undetermined, V_{OUT} spikes up to V_{IN}.	B
SS/TR	6	COMP/FSET	The operation of the device is undetermined.	B
EN	8	PG	The device does not power up.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
MODE/SYNC	1	The device functions as intended: Forced PWM.	D
VIN	2	The device functions as intended.	D
SW	3	The device is potentially damaged.	A
GND	4	The device does not power up.	B
FB	5	The device is potentially damaged.	A
SS/TR	6	The device functions as intended.	D
COMP/FSET	7	The device functions as intended.	D
EN	8	The device functions as intended.	D
PG	9	The device is potentially damaged.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025