

Functional Safety Information

SN74LVC1G09B-Q1

Functional Safety FIT Rate, FMD and Pin FMA



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1 Overview

This document contains information for the SN74LVC1G09B-Q1 (DBV, DCK, and X2SON packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

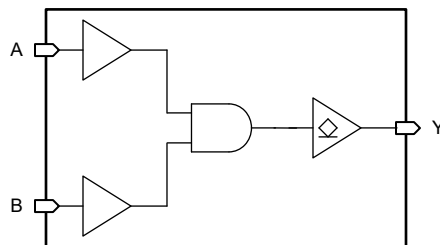


Figure 1-1. Functional Block Diagram

The SN74LVC1G09B-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DBV Package

This section provides functional safety failure in time (FIT) rates for the DBV package of the SN74LVC1G09B-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 10mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	3 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 DCK Package

This section provides functional safety failure in time (FIT) rates for the DCK package of the SN74LVC1G09B-Q1 based on two different industry-wide used reliability standards:

- [Table 2-5](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-6](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	3
Die FIT rate	2
Package FIT rate	1

The failure rate and mission profile information in [Table 2-5](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 and figure 16
- Power dissipation: 10mW
- Climate type: World-wide table 8 and figure 13
- Package factor (lambda 3): From table 17b and figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	3 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-6](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 X2SON Package

This section provides functional safety failure in time (FIT) rates for the X2SON package of the SN74LVC1G09B-Q1 based on two different industry-wide used reliability standards:

- [Table 2-5](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-6](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	3
Die FIT rate	2
Package FIT rate	1

The failure rate and mission profile information in [Table 2-5](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 and figure 16
- Power dissipation: 10mW
- Climate type: World-wide table 8 and figure 13
- Package factor (lambda 3): From table 17b and figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	3 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-6](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the SN74LVC1G09B-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck-at-fault	20
Output open (Hi-Z)	20
Output functional - out of specification timing or voltage	40
Short circuit any two pins	20

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the SN74LVC1G09B-Q1 (DBV, DCK, and X2SON packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to supply (see [Table 4-5](#))

[Table 4-2](#) through [Table 4-5](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin short-circuited to ground
- Pin open-circuited
- Pin short-circuited to an adjacent pin
- Pin short-circuited to VCC

4.1 DBV, DCK, and X2SON Package

[Figure 4-1](#) and [Figure 4-2](#) shows the SN74LVC1G09B-Q1 pin diagram for the DBV, DCK, and X2SON package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the SN74LVC1G09B-Q1 datasheet.

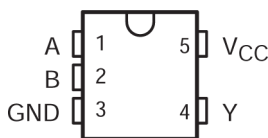


Figure 4-1. Pin Diagram (DBV or DCK) Package

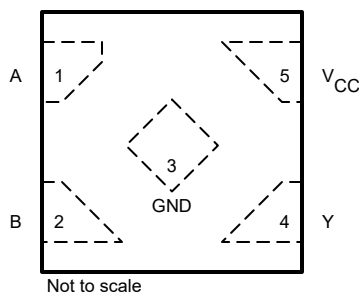


Figure 4-2. Pin Diagram (X2SON Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A	1	The functionality of the input pin is defined; such as, input is LOW – See the <i>Device Function</i> table. (For example, if the buffer input is GND, the output is always driven LOW).	B
B	2	The functionality of the input pin is defined; such as, input is LOW – See the <i>Device Function</i> table. (For example, if the buffer input is GND, the output is always driven LOW).	B
GND	3	The device operates as normal.	D
Y	4	Excessive output current can occur, or the output does not switch. (For example, if the buffer output is shorted to ground and attempts to drive to VCC).	A
VCC	5	The device is not powered because the short is external to the device. System-level damage potentially occurs in this scenario.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A	1	The pin is floating and can change the output state and cause excessive current from VCC to GND. See Implications of Slow or Floating CMOS Inputs .	A
B	2	The pin is floating and can change the output state and cause excessive current from VCC to GND. See Implications of Slow or Floating CMOS Inputs .	A
GND	3	The device is not powered.	B
Y	4	The device operates as normal.	D
VCC	5	The device is not powered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
A	1	2	Two inputs shorted together do not cause damage unless there is an external bus contention that drives the input so that $V_{IL} < \text{Input Voltage} < V_{IH}$; in which case, excessive supply current to GND potentially causes damage. System-level damage potentially occurs in this scenario.	A
B	2	3	Two inputs shorted together do not cause damage unless there is an external bus contention that drives the input so that $V_{IL} < \text{Input Voltage} < V_{IH}$; in which case, excessive supply current to GND potentially causes damage. System-level damage potentially occurs in this scenario.	A
GND	3	4	Excessive output current can occur and the output does not switch. (For example, if one output is driving to VCC and another output is driving to GND).	A
Y	4	5	Excessive output current can occur and the output does not switch. (For example, if one output is driving to VCC and another output is driving to GND).	A
VCC	5	1	Two inputs shorted together do not cause damage unless there is an external bus contention that drives the input so that $V_{IL} < \text{Input Voltage} < V_{IH}$; in which case, excessive supply current to GND potentially causes damage. System-level damage potentially occurs in this scenario.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
A	1	The functionality of the input pin is defined; such as, input is HIGH – See the <i>Device Function</i> table. (For example, if the buffer input is VCC, the output is always driven HIGH).	B
B	2	The functionality of the input pin is defined; such as, input is HIGH – See the <i>Device Function</i> table. (For example, if the buffer input is VCC, the output is always driven HIGH).	B
GND	3	The device is not powered because the short is external to the device. System-level damage potentially occurs in this scenario.	B
Y	4	Excessive output current can occur, or the output does not switch. (For example, if the buffer output is shorted to ground and attempts to drive to VCC).	A
VCC	5	The device operates as normal.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

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Last updated 10/2025