Functional Safety Information

TPS22810-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TPS22810-Q1 (6-Pin SOT-23 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

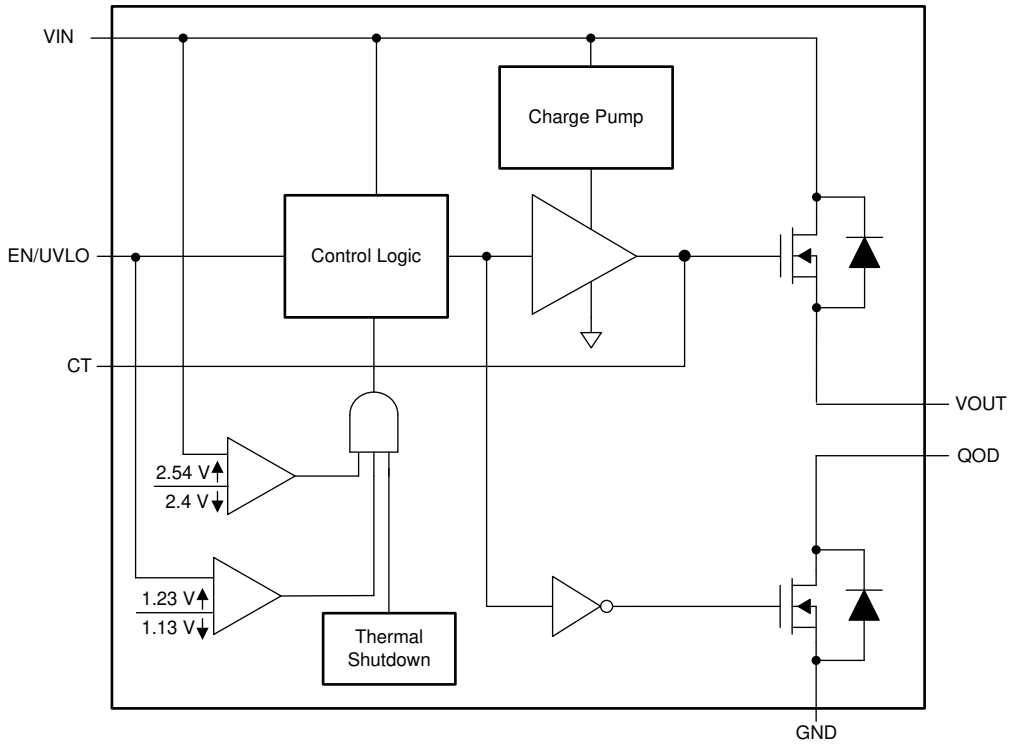


Figure 1-1. Functional Block Diagram

TPS22810-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for TPS22810-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	12
Die FIT rate	9
Package FIT rate	3

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 237mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Analog and mixed ≤50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS22810-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT stuck on	25
VOUT open or Hi-Z	25
VOUT outside specification (voltage or rise time)	35
QOD stuck on	5
QOD stuck off	5
Pin to pin short (any two pins)	5

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS22810-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-3)
- Pin open-circuited (see Table 4-4)
- Pin short-circuited to an adjacent pin (see Table 4-5)
- Pin short-circuited to supply (see Table 4-6)

Table 4-3 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS22810-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS22810-Q1 datasheet.

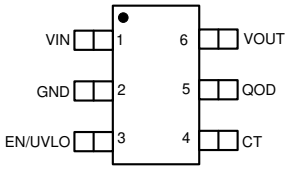


Figure 4-1. Pin Diagram

Table 4-2. Pin Descriptions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input.
2	GND	—	Device ground.
3	EN/UVLO	I	Active high switch control input and UVLO adjustment. Do not leave floating
4	CT	O	Switch slew rate control. Can be left floating
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating
6	VOUT	O	Switch output.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The absolute maximum ratings for the device are not exceeded.

Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	The power supply is shorted.	B
GND	2	This is the intended operation for the GND pin.	D
EN/UVLO	3	The device is disabled.	B
CT	4	Grounding this pin prevents the device from turning on.	B

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Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
QOD	5	If the QOD pin is left floating in the application, short to ground has no effect. If the QOD pin is connected to the VOUT pin, the device thermally cycles until the short to ground is removed, repetitive cycles can potentially damage the device.	A
VOUT	6	The device thermally cycles until the short to ground is removed, repetitive cycles can potentially damage the device.	A

Table 4-4. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	There is no power supply to the device. The device does not pass through voltage to the VOUT pin.	B
GND	2	There is no GND connection to the device. The device is not functional.	B
EN/UVLO	3	The EN/UVLO pin potentially floats high or low, the output state is unknown.	B
CT	4	The output rise time is no longer controlled; the device turns on at the fastest slew rate of the device with higher inrush current.	C
QOD	5	If the QOD pin is left floating in the application, there is no quick output discharge functionality.	B
VOUT	6	The output does not deliver the voltage to the load.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VIN	1	GND	The power supply is shorted.	B
GND	2	EN/UVLO	The device is disabled.	B
CT	4	QOD	If QOD is tied to VOUT, CT is pulled up to VIN and can potentially damage the device. If QOD is floating, no effect.	A
QOD	5	VOUT	The discharge rate after the switch becomes disabled, and is controlled with the value of the internal pull-down resistance.	D

Table 4-6. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VIN	1	The device operates normally, as expected.	D
GND	2	The power supply is shorted.	B
EN/UVLO	3	The device is enabled if the power supply is above the EN threshold (V_{ENR}).	B
CT	4	Biasing the CT pin can potentially damage the device.	A
QOD	5	Having continuous power on the QOD pin can potentially damage the device.	A
VOUT	6	The switch is bypassed, so the output cannot be turned off. If QOD is tied to VOUT, the device can be damaged.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2026	*	Initial Release

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