Functional Safety Information

TLIN829-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TLIN829-Q1 (SOIC (D, 8) and VSON (DRB, 8) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

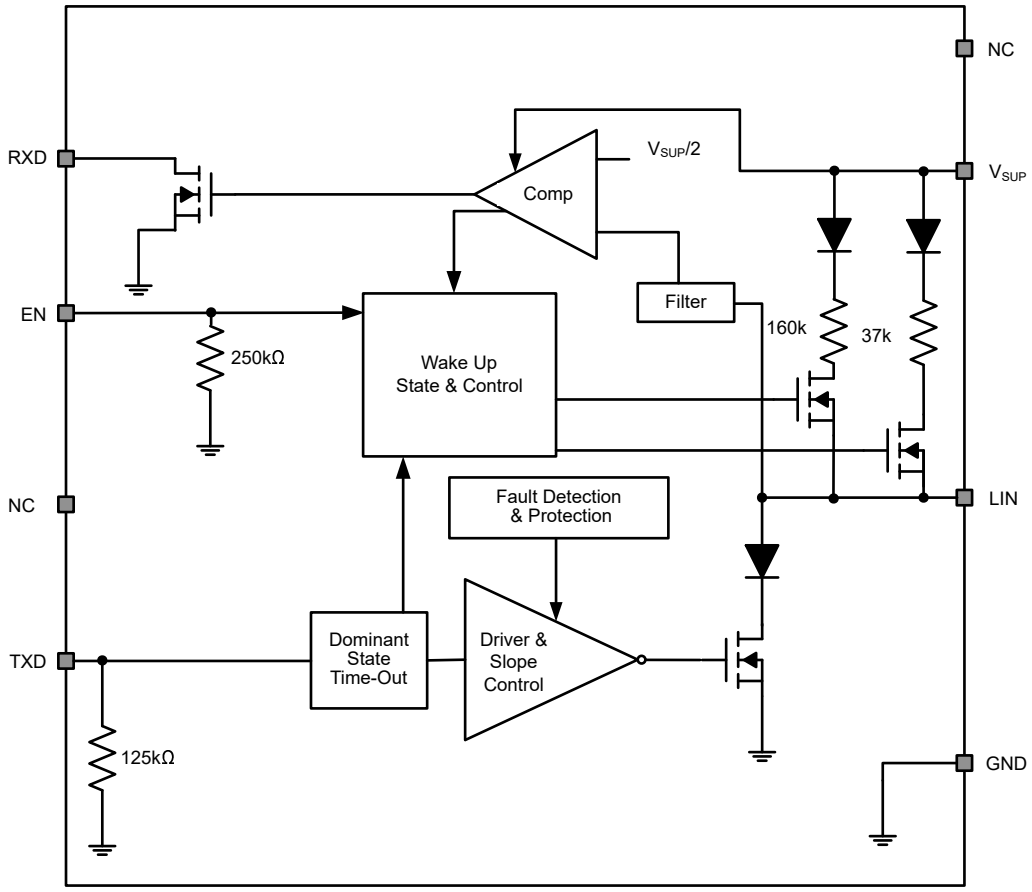


Figure 1-1. Functional Block Diagram

The TLIN829-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC (D, 8) Package

This section provides functional safety failure in time (FIT) rates for the SOIC (D, 8) package of the TLIN829-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) SOIC (D, 8)
Total component FIT rate	13
Die FIT rate	5
Package FIT rate	8

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 120mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. SOIC (D, 8) Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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2.2 VSON (DRB, 8) Package

This section provides functional safety failure in time (FIT) rates for the VSON (DRB, 8) package of the TLIN829-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	3
Package FIT rate	4

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 120mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLIN829-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
LIN transmitter failure	43
LIN receiver failure	4
High voltage I/O failure	13
Digital logic + I/O buffers failure	10
Global power management + state control failure	30

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLIN829-Q1 (SOIC (D, 8) and VSON (DRB, 8) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- All conditions are within the recommended operating conditions of the datasheet

4.1 SOIC (D, 8) Package

Figure 4-1 shows the TLIN829-Q1 pin diagram for the SOIC (D, 8) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLIN829-Q1 datasheet.

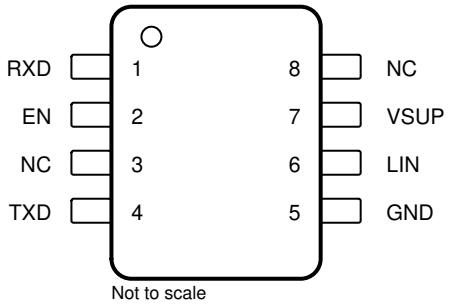


Figure 4-1. Pin Diagram (D, 8-Pin (SOIC)) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RXD	1	The RXD pin is biased dominant; communication from the LIN bus to the MCU is not possible.	B
EN	2	The device potentially only operates in standby mode after power-on. If a short occurs in normal mode, the part is forced to enter sleep mode and potentially disables LIN communication.	B
NC	3	NC is not connected and has no effect on device behavior.	D
TXD	4	The TXD pin is biased dominant; communication from the MCU to the LIN bus is not possible.	B
GND	5	None.	D
LIN	6	The LIN pin is biased dominant; LIN communication is not possible.	B
VSUP	7	The device is not powered and does not function.	B
NC	8	NC is not connected and has no effect on device behavior.	D

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RXD	1	Communication from the LIN bus to the MCU is not possible.	B
EN	2	The EN pin is biased low due to internal pulldown, so the device is in standby mode.	B
NC	3	NC is not connected and has no effect on device behavior.	D
TXD	4	Communication from the MCU to the LIN bus is not possible.	B
GND	5	The device is not powered and does not function.	B
LIN	6	LIN communication is not possible.	B
VSUP	7	The device is not powered and does not function.	B
NC	8	NC is not connected and has no effect on device behavior.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
RXD	1	EN	The device goes into sleep mode when a dominant bit is received on the LIN bus, disabling communication.	B
EN	2	NC	NC is not connected and has no effect on device behavior.	D
NC	3	TXD	NC is not connected and has no effect on device behavior.	D
GND	5	LIN	The LIN pin is biased dominant, LIN communication is not possible.	B
LIN	6	VSUP	The LIN pin is biased recessive, LIN communication is not possible.	B
VSUP	7	NC	NC is not connected and has no effect on device behavior.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VSUP Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RXD	1	There is an absolute maximum voltage violation, and the transceiver is potentially damaged.	A
EN	2	There is an absolute maximum voltage violation, and the transceiver is potentially damaged.	A
NC	3	NC is not connected and has no effect on device behavior.	D
TXD	4	There is an absolute maximum voltage violation, and the transceiver is potentially damaged.	A
GND	5	The device is not powered and does not function.	A
LIN	6	The LIN pin is biased recessive, LIN communication is not possible.	B
VSUP	7	None	D
NC	8	NC is not connected and has no effect on device behavior.	D

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4.2 VSON (DRB, 8) Package

Figure 4-2 shows the TLIN829-Q1 pin diagram for the VSON (DRB, 8) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLIN829-Q1 datasheet.

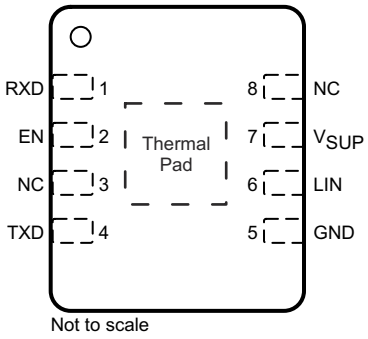


Figure 4-2. Pin Diagram (DRB Package, 8-Pin (VSON) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RXD	1	The RXD pin is biased dominant; communication from the LIN bus to the MCU is not possible.	B
EN	2	The device potentially only operates in standby mode after power-on. If a short occurs in normal mode, the part is forced to enter sleep mode and potentially disables LIN communication.	B
WAKE	3	The WAKE pin is biased to ground and a local wake up is not possible.	B
TXD	4	The TXD pin is biased dominant; communication from the MCU to the LIN bus is not possible.	B
GND	5	None	D
LIN	6	The LIN pin is biased dominant; LIN communication is not possible.	B
VSUP	7	The device is not powered and does not function.	B
INH	8	The INH pin is biased to GND and is not able to enable system power if used in this manner.	B

Note

The DRB package includes a thermal pad.

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RXD	1	Communication from the LIN bus to the MCU is not possible.	B
EN	2	The EN pin is biased low due to internal pulldown, so the device is in standby mode.	B
WAKE	3	Local wake up is not possible.	B
TXD	4	Communication from the MCU to the LIN bus is not possible.	B
GND	5	The device is not powered and does not function.	B
LIN	6	LIN communication is not possible.	B
VSUP	7	The device is not powered and does not function.	B
INH	8	The INH pin is not able to enable system power if used in this manner.	B

Note

The DRB package includes a thermal pad.

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Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
RXD	1	EN	The device goes into sleep mode when a dominant bit is received on the LIN bus, disabling communication.	B
EN	2	WAKE	The absolute maximum voltage on the EN pin is potentially exceeded causing damage to EN pin.	A
WAKE	3	TXD	The absolute maximum voltage on the WAKE pin is potentially exceeded causing damage to TXD pin.	A
GND	5	LIN	The LIN pin is biased dominant, LIN communication is not possible.	B
LIN	6	VSUP	The LIN pin is biased recessive, LIN communication is not possible.	B
VSUP	7	INH	The INH pin is biased high and is not able to turn off system power if used in this manner.	B

Note

The DRB package includes a thermal pad. When the thermal pad is soldered down, there is a possibility that the pad can short to any pin on the device. The behavior of the device in this failure condition is determined by what the thermal pad is connected to. Example: If the thermal pad is soldered to a ground plane, then the adjacent pins behave as if shorted to ground.

Table 4-9. Pin FMA for Device Pins Short-Circuited to VSUP Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
RXD	1	There is an absolute maximum voltage violation, and the transceiver is potentially damaged.	A
EN	2	There is an absolute maximum voltage violation, and the transceiver is potentially damaged.	A
WAKE	3	The WAKE pin is biased high and a local wake up is not possible.	B
TXD	4	There is an absolute maximum voltage violation, and the transceiver is potentially damaged.	A
GND	5	The device is not powered and does not function.	A
LIN	6	The LIN pin is biased recessive, LIN communication is not possible.	B
VSUP	7	None	D
INH	8	The INH pin biased high and is not able to turn off system power if used in this manner.	B

Note

The DRB package includes a thermal pad.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2026	*	Initial Release

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