Functional Safety Information

TPS1HTC100-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS1HTC100-Q1 (PWP (HTSSOP, 14) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

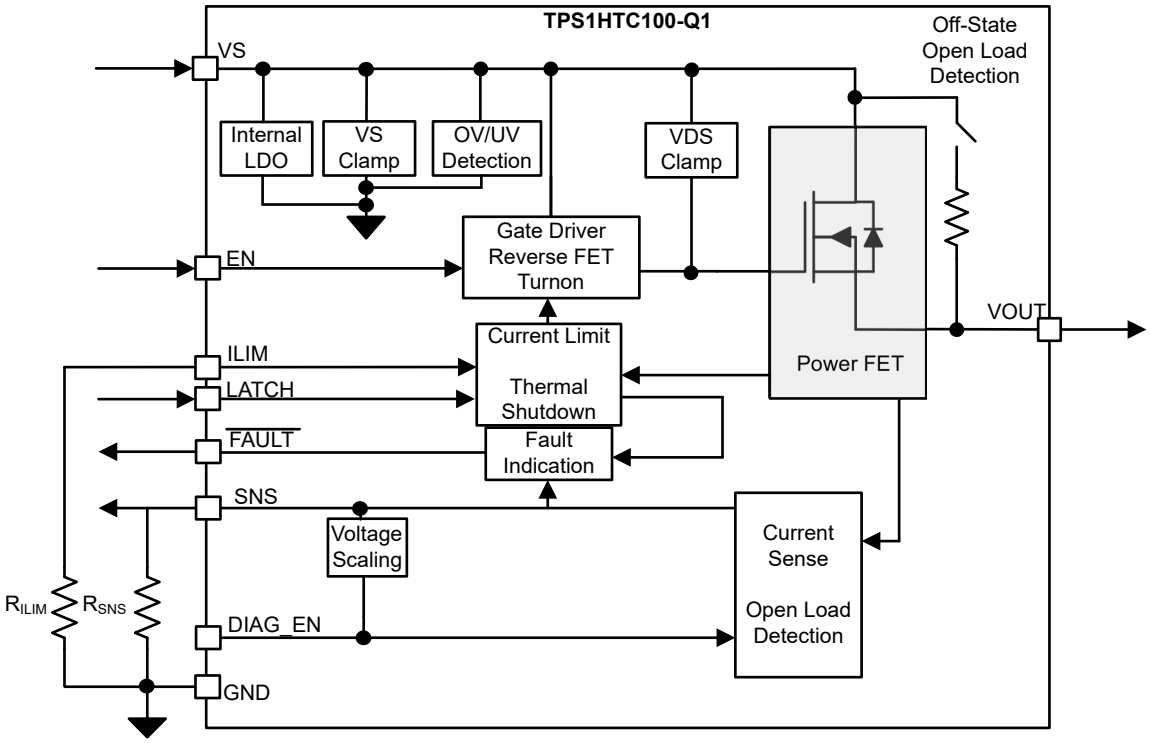


Figure 1-1. Functional Block Diagram

The TPS1HTC100-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS1HTC100-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	14
Die FIT rate	5
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS1HTC100-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT open (Hi-Z)	20
VOUT stuck on (VS)	10
VOUT functional, not in specification voltage or timing	50
Diagnostics not in specification	10
Protection function fails to trip	10

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS1HTC100-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS1HTC100-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS1HTC100-Q1 datasheet.

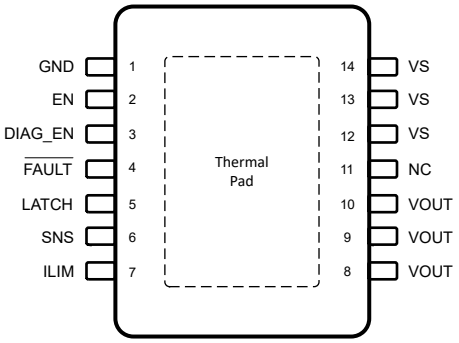


Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The user follows the datasheet recommendations for operating conditions, external components selection, and PCB layout.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The resistor diode network is bypassed if present.	B
EN	2	There is a shutdown of the output.	B
DIAG_EN	3	The diagnostics are disabled.	B
$\overline{\text{FAULT}}$	4	The reported status can be erroneous.	B
LATCH	5	The device defaults to auto-retry (automatic) mode when encountering a thermal fault.	B
SNS	6	The sense current is not valid from the SNS pin.	B
ILIM	7	The device defaults to the internal current limit.	C
NC	11	There is no effect on the device.	D
VOUT	8, 9, 10	The current limit of the device engages.	B
VS	12, 13, 14	The device has no input supply, and therefore, does not function.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Loss of ground detection engages, and the device shuts off.	B
EN	2	The output is shutdown, and the EN pin is pulled down internally.	B
DIAG_EN	3	DIAG_EN is internally pulled down. The diagnostics are disabled.	B
$\overline{\text{FAULT}}$	4	The fault signal is not reported.	B
LATCH	13	LATCH is internally pulled down. The device defaults to auto-retry mode when encountering a thermal fault.	B
SNS	10	The correct sense current cannot be read.	B
ILIM	11	The device defaults to the internal current limit.	C
NC	11	There is no effect on the device.	D
VOUT	8, 9, 10	There is no effect on the device. If configured, open load detection triggers.	B
VS	12, 13, 14	The device has no input supply, and therefore, does not function.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	EN	The channel is disabled.	B
EN	2	DIAG_EN	The EN signal effects the DIAG_EN signal and vice versa.	B
DIAG_EN	3	$\overline{\text{FAULT}}$	Fault reporting is erroneous. The diagnostics are enabled if $\overline{\text{FAULT}}$ is pulled high.	B
$\overline{\text{FAULT}}$	4	LATCH	Fault reporting is erroneous. The device is in auto-retry mode if $\overline{\text{FAULT}}$ is pulled high.	B
LATCH	5	SNS	The current sensing output is erroneous. The device is in auto-retry or latched off depending on the output of the SNS pin.	B
SNS	6	ILIM	The current limit and current sensing output are incorrect.	B
VOUT	10	NC	There is no effect on the device.	D
NC	11	VS	There is no effect on the device.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (VS)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	The supply power is bypassed, and the device does not turn on.	B
EN	2	There is a potential violation of the absolute maximum rating of pin, and a possible breakdown of the ESD cell.	A
DIAG_EN	3	There is a potential violation of the absolute maximum rating of pin, and a possible breakdown of the ESD cell.	A
$\overline{\text{FAULT}}$	4	There is a potential violation of the absolute maximum rating of pin, and a possible breakdown of the ESD cell..	A
LATCH	5	There is a potential violation of the absolute maximum rating of pin, and a possible breakdown of the ESD cell.	A
SNS	6	There is a potential violation of the absolute maximum rating of pin, and a possible breakdown of the ESD cell.	A
ILIM	7	There is a potential violation of the absolute maximum rating of pin, and a possible breakdown of the ESD cell.	A
NC	11	There is no effect on the device.	D
VOUT	8, 9, 10	The output is pulled to the supply voltage. Short-to-battery detection is triggered if configured.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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DATE	REVISION	NOTES
November 2026	*	Initial Release

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