Designing for hardware migration between MSPM0Gx51x and MSPM33C32xx

Application Note

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Abstract

The MSPMx Arm device family provides a high degree of pin-to-pin compatibility. MSPM0Gx51x and MSPM33C32xx share many packages and features which make migrating between these devices a simple process. It is possible to design a single printed circuit board (PCB) to accommodate both MSPM0Gx51x and MSPM33C32xx. This application note will discuss hardware considerations to enable seamless migration and PCB drop-in replacement between both devices.

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Chapter 1

Introduction

This document describes the process of migrating between MSPM0Gx51x and MSPM33C32xx. This document can also be used in process of planning for a single design planning to use MSPM0Gx51x and MSPM33C32xx on the same printed circuit board (PCB).

Modern microcontrollers (MCU) contain an increasing amounts of features and peripherals. This can become a challenging during migration when determining which differences impact the performance or functionality of a system. To simplify the process, this document highlights differences between MSPM0Gx51x and MSPM33C32xx family of devices so that actions can be taken to enable a smooth migration or a single PCB design. This guide focuses on differences between the MSPM0Gx51x and MSPM33C32xx devices and can be used to migrate from either device family in any direction.

This guide is most effectively used ahead of the migration or design process. Follow the steps below to address each aspect of compatibility considerations between MSPM0Gx51x and MSPM33C32xx

1. Select a target MSPM0Gx51x device and a target MSPM33C32xx device
2. Review connection and layout differences
3. Review feature level differences
4. Review pinout differences

Chapter 2

Device List

This guide will cover the design and migration process for MSPM0Gx51x and MSPM33C32xx devices that share a package. Migration of device variants not present in the table is possible, but is not covered in this guide. Start by confirming that the target MSPM0 and MSPM33 devices are present in single table below.

2.1 LQFP100 migration options

TI package code	PZ
Package family	LQFP
Pin Count	100
Pitch	0.5mm
Dimension	16mm x 16mm
Mechanical drawing	Link

Part Number	Flash (kB) / SRAM (kB)	Qualification	ADC channels	GPIO
MSPM0G1519SPZR	512 / 128	Industrial	27	94
MSPM0G1518SPZR	256 / 128	Industrial	27	94
MSPM0G3519SPZR	512 / 128	Industrial	27	94
MSPM0G3518SPZR	256 / 128	Industrial	27	94
M0G3519QPZQ1	512 / 128	Automotive	27	94
M0G3518QPZQ1	256 / 128	Automotive	27	94
MSPM33C321ASPZR	1024 / 256	Industrial	34	93

2.2 NFBGA100 migration options

TI package code	ZAW
Package family	NFBGA
Pin Count	100
Pitch	0.8mm
Dimension	9mm x 9mm
Mechanical drawing	Link

Part Number	Flash (kB) / SRAM (kB)	Qualification	ADC channels	GPIO
MSPM0G1519SZAWR	512 / 128	Industrial	27	94
MSPM0G1518SZAWR	256 / 128	Industrial	27	94
MSPM0G3519SZAWR	512 / 128	Industrial	27	94
MSPM0G3518SZAWR	256 / 128	Industrial	27	94
MSPM33C321ASZAWR	1024 / 256	Industrial	34	93

2.3 LQFP80 migration option

TI package code	PN
Package family	LQFP
Pin Count	80
Pitch	0.5mm
Dimension	14mm x 14mm
Mechanical drawing	Link

Part Number	Flash (kB) / SRAM (kB)	Qualification	ADC channels	GPIO
MSPM0G1519SPNR	512 / 128	Industrial	27	74
MSPM0G1518SPNR	256 / 128	Industrial	27	74
MSPM0G3519SPNR	512 / 128	Industrial	27	74
MSPM0G3518SPNR	256 / 128	Industrial	27	74
M0G3519QPNQ1	512 / 128	Automotive	27	74
M0G3518QPNQ1	256 / 128	Automotive	27	74
MSPM33C321ASPNR	1024 / 256	Industrial	34	73

2.4 LQFP64 migration options

TI package code	PM
Package family	LQFP
Pin Count	64
Pitch	0.5mm
Dimension	12mm x 12mm
Mechanical drawing	Link

Part Number	Flash (kB) / SRAM (kB)	Qualification	ADC channels	GPIO
MSPM0G1519SPMR	512 / 128	Industrial	27	60
MSPM0G1518SPMR	256 / 128	Industrial	27	60
MSPM0G3519SPMR	512 / 128	Industrial	27	60
MSPM0G3518SPMR	256 / 128	Industrial	27	60
M0G3519QPMQ1	512 / 128	Automotive	27	60
M0G3518QPMQ1	256 / 128	Automotive	27	60
MSPM33C321ASPMR	1024 / 256	Industrial	24	57

2.5 VQFN48 migration options

TI package code	RGZ
Package family	VQFN
Pin Count	48
Pitch	0.5mm
Dimension	12mm x 12mm
Mechanical drawing	Link

Part Number	Flash (kB) / SRAM (kB)	Qualification	ADC channels	GPIO
MSPM0G1519SRGZR	256 / 128	Industrial	19	44
MSPM0G1518SRGZR	512 / 128	Industrial	19	44
MSPM0G3519SRGZR	256 / 128	Industrial	19	44
MSPM0G3518SRGZR	512 / 128	Industrial	19	44
M0G3519QRGZRQ1	512 / 128	Automotive	19	44
M0G3518QRGZRQ1	256 / 128	Automotive	19	44
MSPM33C321ASRGZR	1024 / 256	Industrial	18	43

Chapter 3

Review of differences between MSPM0Gx51x and MSPM33C32xx

The MSPM0Gx51x family and MSPM33C32x family share many features and specification. In places where the feature-set is different it is important to understand how this may affect your application. The sections below describes similarities an application can rely on during the migration process and differences that must be assessed early in the design phase.

3.1 Schematic and PCB layout considerations

Differences with device supply pins

MSPM33C32 requires 2 VDD/VSS supply pairs in all packages, however MSPM0Gx51x only requires 1 VDD/VSS supply pair in 48 and 64 pin packages. If a single PCB is required to support both MSPM33C32x and MSPM0Gx51x it is recommended to provision 0Ω resistor connections in the locations of the additional supply pins which can be selectively populated when MSPM33C32x is installed or selectively de-populated with MSPM0Gx51x is installed. This avoids directly connecting VDD to a non-supply pin (such as a normal GPIO pin) in the case where a design is migrated from MSPM33C32x to MSPM0Gx51x.

Package family	TI package code	Device Pin	MSPM0Gx051x connection requirement	MSPM33C32xx connection requirement	Migration action
LQFP100	PZ	N/a	Same features & connections		None
NFBGA100	ZAW				
LQFP80	PN				
LQFP64	PM	Pin 8	General IO and analog input. Not recommended to be connected to VSS	Ground (VSS) connection	Ensure connection meets device specific requirement. If single PCB compatibility is required populate a 0ohm resistor to connect VSS to MSPM33C32xx or de-populate disconnect VSS from MSPM0Gx51x
		Pin 9	General purpose IO. Not recommended to be connected to VDD	VDD connection	Ensure connection meets device specific requirement. If single PCB compatibility is required populate a 0ohm resistor to connect VSS to MSPM33C32xx or de-populate disconnect VDD from MSPM0Gx51x

Package family	TI package code	Device Pin	MSPM0Gx051x connection requirement	MSPM33C32xx connection requirement	Migration action
VQFN48	RGZ	Pin 49 (PowerPad)	No connection.	VSS connection.	Ensure PowerPad is connected to low-impedance electrical ground and sufficient thermal heat sink.
		Pin 7	VSS	General purpose IO	Ensure connection meets device specific requirement. If single PCB compatibility is required populate a 0ohm resistor to connect VSS to MSPM0Gx51x or de-populate disconncec VSS from MSPM33C32xx
		Pin 30	General purpose IO	connection	Ensure connection meets device specific requirement. If single PCB compatibility is required populate a 0ohm resistor to connect VSS to MSPM33C32xx or de-populate disconnect VDD from MSPM0Gx51x

Differences with VBAT supply pins

MSPM33C32xx features a seperate low-power domain which can power a real-time clock (RTC), tamper detection pins, and a small backup memory. This power domain must be powered through an external supply pin called VBAT. MSPM0Gx51x does not include this feature. If a single PCB is required to support both MSPM33C32x and MSPM0Gx51x it is recommended to provision 0Ω resistor connections in the locations of the VBAT supply pin which can be selectively populated when MSPM33C32x is installed or selectively de-populated with MSPM0Gx51x is installed. This avoids directly connecting a supply voltage to a non-supply pin in the case where a design is migrated from MSPM33C32x to MSPM0Gx51x.

Package family	TI package code	Device Pin	MSPM0Gx051x connection requirement	MSPM33C32xx connection requirement	Migration action
LQFP100	PZ	Pin 7	General purpose IO	VBAT supply connection	Ensure connection meets device specific requirement. If single PCB compatibility is required populate a 0ohm resistor to connect VBAT to MSPM33C32xx or de-populate disconnect VBAT from MSPM0Gx51x
NFBGA100	ZAW	Pin A3			
LQFP80	PN	Pin 7			
LQFP64	PM	Pin 39			
VQFN48	RGZ	Pin 5			

Differences with VCORE capacitor

MSPM0Gx51x and MSPM33C32xx family of devices require a capacitor to be placed between the VCORE device pin and ground. MSPM0Gx51x requires a 470nF capacitor. MSPM33C32xx requires a 2.2uF capacitor. If a single PCB is required to support both MSPM0Gx51x and MSPM33C32xx ensure that the capacitor footprint selected can accommodate both capacitor values.

Package family	TI package code	Device Pin	MSPM0Gx051x connection requirement	MSPM33C32xx connection requirement	Migration action
LQFP100	PZ	Pin 100	470nF capacitor	2.2uF capacitor	Ensure correct capacitor value is populated. If single PCB compatibility is required ensure capacitor footprint can support both capacitor values
NFBGA100	ZAW	Pin A1			
LQFP80	PN	Pin 80			
LQFP64	PM	Pin 32			
VQFN48	RGZ	Pin 48			

Differences with VREF connections

To use the integrated ADC in both MSPM0Gx51x and MSPM33C321 a reference voltage must be available in the system. The reference voltage may be sourced externally or from the internal VREF generator. MSPM0Gx51x allows software to select between VDD, internal VREF, or external VREF. MSPM33C32xx does not allow software to select the reference source during runtime. The voltage reference to the MSPM33C32xx must be connected correctly at the board level in one of the ways described below:

1. ADC uses internal voltage reference (software configurable as 1.4V or 2.5V). A 1uF capacitor must be connected between VREF+ and VREF-/GND.
2. ADC uses VDD as voltage reference. VDD must be external connected to the VREF+ device pin on the PCB. A 1uF capacitor must be connected between VREF+ and VREF-/GND.
3. ADC uses external voltage reference. Use a external decoupling capacitor recommended by the external reference.

Boundary scan

MSPM33C32xx family devices support JTAG boundary scan. MSPM0Gx15x family devices do not support boundary scan. If boundary scan is not used, not modifications are required.

3.2 Feature-set difference between MSPM0Gx51x and MSPM33C32xx

Peripheral and feature comparison between MSPM0Gx51x and MSPM33C32xx

Peripheral Name	MSPM0Gx51x instance name	MSPM33C32xx instance name	Differences
CPU	M0+	M33	Feature differences. See ARM documentation
GPIO & IOMUX	GPIOA, GPIOB, GPIOC	GPIOA, GPIOB, GPIOC	No differences
Standard DMA	DMA0	DMA1	No differences
Secure DMA	-	DMA0	N/a
Math accelerator	MATHACL	-	N/a
CAN	CAN0	MCAN0	No differences
CAN	CAN1	MCAN1	No differences
UART	UART0	UC1_0	Feature differences. MSPM33C32xx does not support DALI, IrDA, or ISO7816 modes
UART	UART1	UC1_1	No differences except MSPM0Gx51x does not support LIN mode
UART	UART2	UC13_1	Feature differences. MSPM0Gx51x does not support ISO7816. MSPM33C32xx S2U0 is retained but not active in STOP and STANDBY mode
UART	UART3	UC13_0	Feature differences. MSPM0Gx51x does not support LIN, DALI, IrDA, ISO7816
UART	UART4	UC13_2	No differences except MSPM0Gx51x does not support LIN mode
UART	UART5	UC13_3	No differences except MSPM0Gx51x does not support ISO7816
UART	UART6	UC14	No differences except MSPM0Gx51x does not support ISO7816
UART	UART7	UC12	Feature differences. MSPM33C32xx S2U2 does not support LIN, DALI, IrDA. MSPM33C32xx S2U2 is retained but not active in STOP or STANDBY mode
I2C	I2C0	UC1_0 UC15_0	Feature differences. MSPM33C32xx does not support FIFO mode or digital glitch filter
I2C	I2C1	UC1_1	Feature differences. MSPM33C32xx does not support FIFO mode or digital glitch filter
I2C	I2C2	UC13_0 UC15_1	Feature differences. MSPM33C32xx does not support FIFO mode or digital glitch filter
SPI	SPI0	UC2	No differences except MSPM33C32xx does not support packing
SPI	SPI1	UC13_0	No differences except MSPM33C32xx does not support packing or multiple chip select
SPI	SPI2	UC13_1	No differences except MSPM33C32xx does not support packing or multiple chip select
	-	QSPI	N/a
Timer	TIMA0	TIMA0_0	No differences
Timer	TIMA1	TIMA0_1	No differences except MSPM33C32xx supports 4 external capture/compare units where MSPM0Gx51x supports 2 external capture compare units

Peripheral Name	MSPM0Gx51x instance name	MSPM33C32xx instance name	Differences
Timer	TIMG0	TIMG4_0	No differences except MSPM33C32xx supports shadow load and shadow capture/compare
Timer	-	TIMG4_1	N/a
Timer	TIMG6	TIMG4_2	No differences
Timer	TIMG7	TIMG4_3	No differences
Timer	TIMG8	TIMG8_0	No differences
Timer	TIMG9	TIMG8_1	No differences
Timer	TIMG12	TIMG12_0	No differences
Timer	TIMG14	-	N/a
ADC	ADC0	ADC0	Feature differences. See Technical Reference Manual.
ADC	ADC1	ADC1	Feature differences. See Technical Reference Manual.
Voltage reference	VREF	VREF	Feature differences. See the VREF comment in Schematic and PCB consideration
DAC	DAC0	-	N/a
Comparator	COMP0	COMP0	No differences except MSPM33C32xx adds low-power scan mode
Comparator	COMP1	COMP1	No differences except MSPM33C32xx adds low-power scan mode
Comparator	COMP2	-	N/a
Audio	-	I2S0	N/a
Audio	-	I2S1	N/a
RTC	RTC_B	RTC	No differences except MSPM33C32xx RTC exists in VBAT power island
Watchdog	WWDT0	WWDT	No differences.
Watchdog	WWDT1	IWDT	Feature differences. MSPM33C32xx IWDT does not support window mode, or interval timer mode
AES	AES-ADV	AES-ADV	No differences.
CRC	CRC	CRC	No differences.
SHA	-	SHA	N/a
PKA	-	PKA	N/a
Tamper	-	TAMP	N/a

3.3 Pinout considerations

MSPM0Gx51x and MSPM33C32xx have a common subset of pinout functionality. The tables in this section show which peripherals and functions have the same pinout in both MSPM0Gx51x and MSPM33C32xx. Use the tables below to make sure the chosen pinout is within the common subset of functionality between the devices.

Table 3-1. LQFP100 common functionality between MSPM0Gx51x and MSPM33C32xx

Pin Number	Device Family	Function Mapping							
Pin 1	MSPM0Gx51x	PA0	UART0_TX	I2C0_SDA	TIMA_FAL1	UART5_RX	I2C0_SDA		
	MSPM33C32xx	PA0	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL1	UC13_3_SCL_RX_SCK	UC15_0_SDA		
Pin 2	MSPM0Gx51x	PA1	UART0_RX	I2C0_SCL	TIMA0_C1	TIMG8_IDX	UART5_TX	I2C0_SCL	
	MSPM33C32xx	PA1	UC1_0_SCL_RX	UC1_0_SCL_RX	TIMA0_0_C1	TIMG8_0_IDX	UC13_3_SDA_TX_PICO	UC15_0_SCL	
Pin 3	MSPM0Gx51x	PA28	UART0_TX	I2C0_SDA	TIMA_FAL0	UART5_CTS	I2C0_SDA		
	MSPM33C32xx	PA28	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL0	UC13_3_CTS_CS0	UC15_0_SDA		
Pin 4	MSPM0Gx51x	PA29	I2C1_SCL	UART7_RTS	TIMG6_C0	UART5_RTS	I2C2_SCL		
	MSPM33C32xx	PA29	UC1_1_SCL_RX	UC12_RTS	TIMG4_2_C0	UC13_3_RTS_POCI	UC15_1_SCL		
Pin 5	MSPM0Gx51x	PA30	I2C1_SDA	UART7_CTS	TIMG6_C1	I2C2_SDA			
	MSPM33C32xx	PA30	UC1_1_SDA_TX	UC12_CTS	TIMG4_2_C1	UC15_1_SDA			
Pin 6	MSPM0Gx51x	NRST							
	MSPM33C32xx	NRST							
Pin 8	MSPM0Gx51x	VDD							
	MSPM33C32xx	VDD							
Pin 9	MSPM0Gx51x	VSS							
	MSPM33C32xx	VSS							
Pin 10	MSPM0Gx51x	PC12							
	MSPM33C32xx	PC12							
Pin 11	MSPM0Gx51x	PC15							
	MSPM33C32xx	PC15							
Pin 12	MSPM0Gx51x	PC13	SPI2_PICO						
	MSPM33C32xx	PC13	UC13_1_SDA_TX_PICO						
Pin 13	MSPM0Gx51x	PC14	SPI2_SCK						
	MSPM33C32xx	PC14	UC13_1_SCL_RX_SCK						

Table 3-1. LQFP100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 14	MSPM0Gx51x	PC28	UART5_RX							
	MSPM33C32xx	PC28	UC13_3_SCL_RX_SCK							
Pin 15	MSPM0Gx51x	PA2	TIMG8_C1	SPI0_CS0	SPI2_POCI					
	MSPM33C32xx	PA2	TIMG8_0_C1	UC2_CS0	UC13_1_RTS_POCI					
Pin 16	MSPM0Gx51x	PA3	TIMG8_C0	SPI0_CS1	I2C1_SDA	TIMA0_C1	COMP0_OUT	UART1_TX	SPI0_CS3	COMP1_OUT
	MSPM33C32xx	PA3	TIMG8_0_C0	UC2_CS1	UC1_1_SDA_TX	TIMA0_0_C1	COMP1_OUT	UC1_1_SDA_TX	UC2_CS1	COMP1_OUT
Pin 17	MSPM0Gx51x	PA4	SPI0_POCI	I2C1_SCL	TIMA0_C1N	LFCLK_IN	UART1_RX	SPI2_CS0		
	MSPM33C32xx	PA4	UC2_POCI	UC1_1_SCL_RX	TIMA0_0_C1N	LFCLK_IN	UC1_1_SCL_RX	UC13_1_CTS_CS0		
Pin 18	MSPM0Gx51x	PA5	SPI0_PICO	TIMG0_C0	TIMG6_C0					
	MSPM33C32xx	PA5	UC2_PICO	TIMG4_0_C0	TIMG4_2_C0					
Pin 19	MSPM0Gx51x	PA6	SPI0_SCK	TIMG0_C1	HFCLK_IN	TIMG6_C1	TIMA0_C2N			
	MSPM33C32xx	PA6	UC2_SCK	TIMG4_0_C1	HFCLK_IN	TIMG4_2_C1	TIMA0_0_C2N			
Pin 20	MSPM0Gx51x	PB0	UART0_TX							
	MSPM33C32xx	PB0	UC1_0_SDA_TX							
Pin 21	MSPM0Gx51x	PB1	UART0_RX							
	MSPM33C32xx	PB1	UC1_0_SCL_RX							
Pin 22	MSPM0Gx51x	PA7	COMP0_OUT	CLK_OUT	TIMA0_C2	TIMG7_C1				
	MSPM33C32xx	PA7	COMP0_OUT	CLK_OUT	TIMA0_0_C2	TIMG4_3_C1				
Pin 23	MSPM0Gx51x	PB2	I2C1_SCL	TIMA0_C3	TIMG6_C0					
	MSPM33C32xx	PB2	UC1_1_SCL_RX	TIMA0_0_C3	TIMG4_2_C0					
Pin 24	MSPM0Gx51x	PB3	I2C1_SDA	TIMA0_C3N	TIMG6_C1					
	MSPM33C32xx	PB3	UC1_1_SDA_TX	TIMA0_0_C3N	TIMG4_2_C1					
Pin 25	MSPM0Gx51x	PB4	UART1_TX	UART3_CTS	TIMA0_C2	SPI2_PICO				
	MSPM33C32xx	PB4	UC1_1_SDA_TX	UC13_0_CTS_CS0	TIMA0_0_C2	UC13_1_SDA_TX_PICO				
Pin 26	MSPM0Gx51x	PB5	UART1_RX	UART3_RTS	TIMA0_C2N	SPI2_POCI				
	MSPM33C32xx	PB5	UC1_1_SCL_RX	UC13_0_RTS_POCI	TIMA0_0_C2N	UC13_1_RTS_POCI				

Table 3-1. LQFP100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 27	MSPM0Gx51x	PA8	UART1_TX	TIMA0_C0	UART0_RTS					
	MSPM33C32xx	PA8	UC1_1_SDA_TX	TIMA0_0_C0	UC1_0_RTS					
Pin 28	MSPM0Gx51x	PA9	UART1_RX	SPI0_PICO	TIMA0_C0N	CLK_OUT	RTC_OUT	UART0_CTS		
	MSPM33C32xx	PA9	UC1_1_SCL_RX	UC2_PICO	TIMA0_0_C0N	CLK_OUT	RTC_OUT	UC1_0_CTS		
Pin 29	MSPM0Gx51x	PB28	SPI1_CS0	TIMA0_C0	UART5_RX					
	MSPM33C32xx	PB28	UC13_0_CTS_CS0	TIMA0_0_C0	UC13_3_SCL_RX_SCK					
Pin 30	MSPM0Gx51x	PB29	SPI1_POCI	TIMA0_C0N	UART5_TX	TIMG9_C0				
	MSPM33C32xx	PB29	UC13_0_RTS_POCI	TIMA0_0_C0N	UC13_3_SDA_TX_PICO	TIMG8_1_C0				
Pin 31	MSPM0Gx51x	PB30	SPI1_PICO	TIMA0_C1	UART5_CTS	TIMG9_C1				
	MSPM33C32xx	PB30	UC13_0_SDA_TX_PICO	TIMA0_0_C1	UC13_3_CTS_CS0	TIMG8_1_C1				
Pin 32	MSPM0Gx51x	PB31	SPI1_SCK	TIMG8_IDX	TIMA0_C1N	UART5_RTS	TIMG9_IDX			
	MSPM33C32xx	PB31	UC13_0_SCL_RX_SCK	TIMG8_0_IDX	TIMA0_0_C1N	UC13_3_RTS_POCI	TIMG8_1_IDX			
Pin 33	MSPM0Gx51x	PA10	UART0_TX	SPI0_POCI	I2C0_SDA	TIMA0_C2	TIMG12_C0	SPI2_SCK	I2C0_SDA	
	MSPM33C32xx	PA10	UC1_0_SDA_TX	UC2_POCI	UC1_0_SDA_TX	TIMA0_0_C2	TIMG12_0_C0	UC13_1_SCL_RX_SCK	UC15_0_SDA	
Pin 34	MSPM0Gx51x	PA11	UART0_RX	SPI0_SCK	I2C0_SCL	TIMA0_C2N	COMP0_OUT	I2C0_SCL		
	MSPM33C32xx	PA11	UC1_0_SCL_RX	UC2_SCK	UC1_0_SCL_RX	TIMA0_0_C2N	COMP0_OUT	UC15_0_SCL		
Pin 35	MSPM0Gx51x	PC16								
	MSPM33C32xx	PC16								
Pin 36	MSPM0Gx51x	PC17								
	MSPM33C32xx	PC17								
Pin 37	MSPM0Gx51x	PC29	UART5_TX							
	MSPM33C32xx	PC29	UC13_3_SDA_TX_PICO							
Pin 38	MSPM0Gx51x	PC18								
	MSPM33C32xx	PC18								
Pin 39	MSPM0Gx51x	PC19								
	MSPM33C32xx	PC19								

Table 3-1. LQFP100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping							
Pin 40	MSPM0Gx51x	PB6	UART1_TX	UART7_CTS	SPI0_CS1	TIMG6_C0			
	MSPM33C32xx	PB6	UC1_1_SDA_TX	UC12_CTS	UC2_CS1	TIMG4_2_C0			
Pin 41	MSPM0Gx51x	PB7	UART1_RX	SPI1_POCI	UART7_RTS	TIMG9_C0	TIMG6_C1		
	MSPM33C32xx	PB7	UC1_1_SCL_RX	UC13_0_RTS_POCI	UC12_RTS	TIMG8_1_C0	TIMG4_2_C1		
Pin 42	MSPM0Gx51x	PB8	UART1_CTS	SPI1_PICO	I2C2_SCL	COMP0_OUT	TIMG9_IDX	COMP1_OUT	
	MSPM33C32xx	PB8	UC1_1_CTS	UC13_0_SDA_TX_PICO	UC13_0_SCL_RX_SCK	COMP1_OUT	TIMG8_1_IDX	COMP1_OUT	
Pin 43	MSPM0Gx51x	PB9	UART1_RTS	SPI1_SCK	I2C2_SDA	TIMA0_C0N	TIMG9_C1		
	MSPM33C32xx	PB9	UC1_1_RTS	UC13_0_SCL_RX_SCK	UC13_0_SDA_TX_PICO	TIMA0_0_C0N	TIMG8_1_C1		
Pin 44	MSPM0Gx51x	PB10	TIMG0_C0	UART4_TX	TIMG6_C0				
	MSPM33C32xx	PB10	TIMG4_0_C0	UC13_2_SDA_TX_PICO	TIMG4_2_C0				
Pin 45	MSPM0Gx51x	PB11	TIMG0_C1	CLK_OUT	UART4_RX	TIMG6_C1			
	MSPM33C32xx	PB11	TIMG4_0_C1	CLK_OUT	UC13_2_SCL_RX_SCK	TIMG4_2_C1			
Pin 46	MSPM0Gx51x	PB12	UART3_TX	TIMA_FAL1	UART4_CTS				
	MSPM33C32xx	PB12	UC13_0_SDA_TX_PICO	TIMA0_0_FAL1	UC13_2_CTS_CS0				
Pin 47	MSPM0Gx51x	PB13	UART3_RX	TIMG12_C0	TIMA0_C1N	UART4_RTS			
	MSPM33C32xx	PB13	UC13_0_SCL_RX_SCK	TIMG12_0_C0	TIMA0_0_C1N	UC13_2_RTS_POCI			
Pin 48	MSPM0Gx51x	PB14	SPI1_POCI	TIMG12_C1	TIMA0_C0	TIMG8_IDX			
	MSPM33C32xx	PB14	UC13_0_RTS_POCI	TIMG12_0_C1	TIMA0_0_C0	TIMG8_0_IDX			
Pin 49	MSPM0Gx51x	PB15	UART7_TX	TIMG8_C0	TIMG7_C0				
	MSPM33C32xx	PB15	UC12_TX	TIMG8_0_C0	TIMG4_3_C0				
Pin 50	MSPM0Gx51x	PB16	UART7_RX	TIMG8_C1	TIMG7_C1				
	MSPM33C32xx	PB16	UC12_RX	TIMG8_0_C1	TIMG4_3_C1				
Pin 51	MSPM0Gx51x	PA12	UART3_CTS	FCC_IN	TIMG0_C0	SPI1_CS1	CAN0_TX	A0_8	
	MSPM33C32xx	PA12	UC13_0_CTS_CS0	FCC_IN	TIMG4_0_C0	UC13_0_CTS_CS0	CAN0_TX	A0_8	

Table 3-1. LQFP100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 52	MSPM0Gx51x	PA13	UART3_RTS	UART3_RX	TIMG0_C1	UART7_TX	CAN0_RX	A0_9	COMP0_IN2-	
	MSPM33C32xx	PA13	UC13_0_RTS_POCI	UC13_0_SCL_RX_SCK	TIMG4_0_C1	UC12_TX	CAN0_RX	A0_9	COMP0_IN2-	
Pin 53	MSPM0Gx51x	PA14	UART0_CTS	UART3_TX	CLK_OUT	UART7_RX	A0_12	COMP0_IN2+		
	MSPM33C32xx	PA14	UC1_0_CTS	UC13_0_SDA_TX_PICO	CLK_OUT	UC12_RX	A0_12	COMP0_IN2+		
Pin 54	MSPM0Gx51x	PA15	UART0_RTS	I2C1_SCL	TIMA0_C2	TIMG8_IDX	A1_0	COMP0_IN3+	COMP1_IN3+	I2C2_SCL
	MSPM33C32xx	PA15	UC1_0_RTS	UC1_1_SCL_RX	TIMA0_0_C2	TIMG8_0_IDX	A1_0	COMP0_IN3+	COMP1_IN3+	UC15_1_SCL
Pin 55	MSPM0Gx51x	PA16	SPI1_POCI	I2C1_SDA	TIMA0_C2N	FCC_IN	A1_1	I2C2_SDA		
	MSPM33C32xx	PA16	UC13_0_RTS_POCI	UC1_1_SDA_TX	TIMA0_0_C2N	FCC_IN	A1_1	UC15_1_SDA		
Pin 56	MSPM0Gx51x	PC0	TIMG8_C0	TIMA0_C2						
	MSPM33C32xx	PC0	TIMG8_0_C0	TIMA0_0_C2						
Pin 57	MSPM0Gx51x	PC1	TIMG8_C1	TIMA0_C2N						
	MSPM33C32xx	PC1	TIMG8_0_C1	TIMA0_0_C2N						
Pin 58	MSPM0Gx51x	PC20								
	MSPM33C32xx	PC20								
Pin 59	MSPM0Gx51x	PC21	CAN1_TX							
	MSPM33C32xx	PC21	CAN1_TX							
Pin 60	MSPM0Gx51x	PC22	CAN1_RX							
	MSPM33C32xx	PC22	CAN1_RX							
Pin 61	MSPM0Gx51x	PC23								
	MSPM33C32xx	PC23								
Pin 62	MSPM0Gx51x	PC24								
	MSPM33C32xx	PC24								
Pin 63	MSPM0Gx51x	VSS								
	MSPM33C32xx	VSS								
Pin 64	MSPM0Gx51x	VDD								
	MSPM33C32xx	VDD								
Pin 65	MSPM0Gx51x	PC2	I2C2_SCL	SPI1_CS0	TIMA0_C0					
	MSPM33C32xx	PC2	UC13_0_SCL_RX_SCK	UC13_0_CTS_CS0	TIMA0_0_C0					

Table 3-1. LQFP100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping							
Pin 66	MSPM0Gx51x	PC3	I2C2_SDA	TIMA0_C0N					
	MSPM33C32xx	PC3	UC13_0_SDA_TX_PICO	TIMA0_0_C0N					
Pin 67	MSPM0Gx51x	PC4	TIMA0_C1						
	MSPM33C32xx	PC4	TIMA0_0_C1						
Pin 68	MSPM0Gx51x	PC5	TIMA0_C1N						
	MSPM33C32xx	PC5	TIMA0_0_C1N						
Pin 69	MSPM0Gx51x	PA17	UART1_TX	SPI1_SCK	TIMA0_C3	TIMG7_C0	A1_2	COMP0_IN1-	
	MSPM33C32xx	PA17	UC1_1_SDA_TX	UC13_0_SCL_RX_SCK	TIMA0_0_C3	TIMG4_3_C0	A1_2	COMP0_IN1-	
Pin 70	MSPM0Gx51x	PA18	UART1_RX	SPI1_PICO	TIMA0_C3N	A1_3	COMP0_IN1+		
	MSPM33C32xx	PA18	UC1_1_SCL_RX	UC13_0_SDA_TX_PICO	TIMA0_0_C3N	A1_3	COMP0_IN1+		
Pin 71	MSPM0Gx51x	PA19	SWDIO	A0_13					
	MSPM33C32xx	PA19	SWDIO	A0_15					
Pin 72	MSPM0Gx51x	PA20	SWCLK	A0_14					
	MSPM33C32xx	PA20	SWCLK	A0_16					
Pin 73	MSPM0Gx51x	PB17	SPI0_PICO	TIMA0_C2	A1_4	COMP1_IN2-			
	MSPM33C32xx	PB17	UC2_PICO	TIMA0_0_C2	A1_4	COMP1_IN2-			
Pin 74	MSPM0Gx51x	PB18	SPI0_SCK	TIMA0_C2N	A1_5	COMP1_IN2+			
	MSPM33C32xx	PB18	UC2_SCK	TIMA0_0_C2N	A1_5	COMP1_IN2+			
Pin 75	MSPM0Gx51x	PB19	SPI0_POCI	UART0_CTS	TIMG7_C1	A1_6			
	MSPM33C32xx	PB19	UC2_POCI	UC1_0_CTS	TIMG4_3_C1	A1_6			
Pin 76	MSPM0Gx51x	PA21	UART1_CTS	TIMA0_C0	TIMG6_C0	A1_7	VREF-		
	MSPM33C32xx	PA21	UC1_1_CTS	TIMA0_0_C0	TIMG4_2_C0	A1_7	VREF-		
Pin 77	MSPM0Gx51x	PA22	UART1_RTS	TIMA0_C0N	CLK_OUT	TIMG6_C1	A0_7		
	MSPM33C32xx	PA22	UC1_1_RTS	TIMA0_0_C0N	CLK_OUT	TIMG4_2_C1	A0_7		
Pin 78	MSPM0Gx51x	PC6	UART3_TX	SPI0_CS1	TIMA0_C0				
	MSPM33C32xx	PC6	UC13_0_SDA_TX_PICO	UC2_CS1	TIMA0_0_C0				
Pin 79	MSPM0Gx51x	PC7	UART3_RX	SPI0_CS0	TIMA0_C0N				
	MSPM33C32xx	PC7	UC13_0_SCL_RX_SCK	UC2_CS0	TIMA0_0_C0N				

Table 3-1. LQFP100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 80	MSPM0Gx51x	PC8	UART3_CTS	SPI1_CS2	TIMA0_C1					
	MSPM33C32xx	PC8	UC13_0_CTS_CS0	UC13_0_CTS_CS0	TIMA0_0_C1					
Pin 81	MSPM0Gx51x	PC9	UART3_RTS	TIMA0_C1N						
	MSPM33C32xx	PC9	UC13_0_RTS_POCI	TIMA0_0_C1N						
Pin 82	MSPM0Gx51x	PB20	SPI0_CS2	TIMG12_C0	TIMA0_C1	A0_6				
	MSPM33C32xx	PB20	UC2_CS2	TIMG12_0_C0	TIMA0_0_C1	A0_6				
Pin 83	MSPM0Gx51x	PB21	TIMG8_C0	CAN1_TX	UART6_RX	A1_8				
	MSPM33C32xx	PB21	TIMG8_0_C0	CAN1_TX	UC14_SCL_RX	A1_8				
Pin 84	MSPM0Gx51x	PB22	SPI1_PICO	TIMG8_C1	CAN1_RX	UART6_TX	A1_10			
	MSPM33C32xx	PB22	UC13_0_SDA_TX_PICO	TIMG8_0_C1	CAN1_RX	UC14_SDA_TX	A1_10			
Pin 85	MSPM0Gx51x	PB23	SPI1_SCK	UART6_CTS	A1_11					
	MSPM33C32xx	PB23	UC13_0_SCL_RX_SCK	UC14_CTS	A1_11					
Pin 86	MSPM0Gx51x	PB24	SPI0_CS3	SPI0_CS1	TIMG12_C1	UART6_RTS	A0_5	COMP1_IN1+		
	MSPM33C32xx	PB24	UC2_CS3	UC2_CS3	TIMG12_0_C1	UC14_RTS	A0_5	COMP1_IN1+		
Pin 87	MSPM0Gx51x	PC10	TIMG9_C0	UART6_RX						
	MSPM33C32xx	PC10	TIMG8_1_C0	UC14_SCL_RX						
Pin 88	MSPM0Gx51x	PC11	TIMG9_C1	UART6_TX						
	MSPM33C32xx	PC11	TIMG8_1_C1	UC14_SDA_TX						
Pin 89	MSPM0Gx51x	PC25	TIMG9_IDX	UART6_CTS						
	MSPM33C32xx	PC25	TIMG8_1_IDX	UC14_CTS						
Pin 90	MSPM0Gx51x	PC26	CAN1_TX	UART6_RTS						
	MSPM33C32xx	PC26	CAN1_TX	UC14_RTS						
Pin 91	MSPM0Gx51x	PC27	CAN1_RX							
	MSPM33C32xx	PC27	CAN1_RX							
Pin 92	MSPM0Gx51x	PA23	SPI0_CS3	TIMA0_C3	UART3_CTS	TIMG0_C0	SPI1_CS1	COMP1_IN1-	VREF+	
	MSPM33C32xx	PA23	UC2_CS3	TIMA0_0_C3	UC13_0_CTS_CS0	TIMG4_0_C0	UC13_0_CTS_CS0	COMP1_IN1-	VREF+	
Pin 93	MSPM0Gx51x	PA24	SPI0_CS2	TIMA0_C3N	UART3_RTS	TIMG0_C1	A0_3			
	MSPM33C32xx	PA24	UC2_CS2	TIMA0_0_C3N	UC13_0_RTS_POCI	TIMG4_0_C1	A0_3			

Table 3-1. LQFP100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 94	MSPM0Gx51x	PA25	UART3_RX	TIMA0_C1N	A0_2					
	MSPM33C32xx	PA25	UC13_0_SCL_RX_SCK	TIMA0_0_C1N	A0_2					
Pin 95	MSPM0Gx51x	PB25	UART0_CTS	TIMA_FAL0	TIMA_FAL1	TIMA_FAL2	A0_4			
	MSPM33C32xx	PB25	UC1_0_CTS	TIMA0_0_FAL2	TIMA0_0_FAL2	TIMA0_0_FAL2	A0_4			
Pin 96	MSPM0Gx51x	PB26	UART0_RTS	TIMG6_C0	A1_13	COMP1_IN0+				
	MSPM33C32xx	PB26	UC1_0_RTS	TIMG4_2_C0	A1_13	COMP1_IN0+				
Pin 97	MSPM0Gx51x	PB27	TIMG6_C1	A1_14	COMP1_IN0-					
	MSPM33C32xx	PB27	TIMG4_2_C1	A1_14	COMP1_IN0-					
Pin 98	MSPM0Gx51x	PA26	UART3_TX	SPI1_CS0	TIMA_FAL0	CAN0_TX	TIMG7_C0	A0_1	COMP0_IN0+	
	MSPM33C32xx	PA26	UC13_0_SDA_TX_PICO	UC13_0_CTS_CS0	TIMA0_0_FAL0	CAN0_TX	TIMG4_3_C0	A0_1	COMP0_IN0+	
Pin 99	MSPM0Gx51x	PA27	TIMA_FAL2	RTC_OUT	CAN0_RX	TIMG7_C1	A0_0	COMP0_IN0-		
	MSPM33C32xx	PA27	TIMA0_0_FAL2	RTC_OUT	CAN0_RX	TIMG4_3_C1	A0_0	COMP0_IN0-		
Pin 100	MSPM0Gx51x	VCORE								
	MSPM33C32xx	VCORE								

Table 3-2. NFBGA100 common functionality between MSPM0Gx51x and MSPM33C32xx

Pin Number	Device Family	Function Mapping								
Pin A1	MSPM0Gx51x	VCORE								
	MSPM33C32xx	VCORE								
Pin A2	MSPM0Gx51x	VSS								
	MSPM33C32xx	VSS								
Pin A4	MSPM0Gx51x	VDD								
	MSPM33C32xx	VDD								
Pin A5	MSPM0Gx51x	PA2	TIMG8_C1	SPI0_CS0	SPI2_POCI					
	MSPM33C32xx	PA2	TIMG8_0_C1	UC2_CS0	UC13_1_RTS_POCI					
Pin A6	MSPM0Gx51x	PA3	TIMG8_C0	SPI0_CS1	I2C1_SDA	TIMA0_C1	COMP0_OUT	UART1_TX	SPI0_CS3	COMP1_OUT
	MSPM33C32xx	PA3	TIMG8_0_C0	UC2_CS1	UC1_1_SDA_TX	TIMA0_0_C1	COMP1_OUT	UC1_1_SDA_TX	UC2_CS1	COMP1_OUT
Pin A7	MSPM0Gx51x	PA4	SPI0_POCI	I2C1_SCL	TIMA0_C1N	LFCLK_IN	UART1_RX	SPI2_CS0		
	MSPM33C32xx	PA4	UC2_POCI	UC1_1_SCL_RX	TIMA0_0_C1N	LFCLK_IN	UC1_1_SCL_RX	UC13_1_CTS_CS0		

Table 3-2. NFBGA100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin A8	MSPM0Gx51x	PA5	SPI0_PICO	TIMG0_C0	TIMG6_C0					
	MSPM33C32xx	PA5	UC2_PICO	TIMG4_0_C0	TIMG4_2_C0					
Pin A9	MSPM0Gx51x	PA6	SPI0_SCK	TIMG0_C1	HFCLK_IN	TIMG6_C1	TIMA0_C2N			
	MSPM33C32xx	PA6	UC2_SCK	TIMG4_0_C1	HFCLK_IN	TIMG4_2_C1	TIMA0_0_C2N			
Pin A10	MSPM0Gx51x	PB31	SPI1_SCK	TIMG8_IDX	TIMA0_C1N	UART5_RTS	TIMG9_IDX			
	MSPM33C32xx	PB31	UC13_0_SCL_RX_SCK	TIMG8_0_IDX	TIMA0_0_C1N	UC13_3_RTS_POCI	TIMG8_1_IDX			
Pin B1	MSPM0Gx51x	PB26	UART0_RTS	TIMG6_C0	A1_13	COMP1_IN0+				
	MSPM33C32xx	PB26	UC1_0_RTS	TIMG4_2_C0	A1_13	COMP1_IN0+				
Pin B2	MSPM0Gx51x	PA27	TIMA_FAL2	RTC_OUT	CAN0_RX	TIMG7_C1	A0_0	COMP0_IN0-		
	MSPM33C32xx	PA27	TIMA0_0_FAL2	RTC_OUT	CAN0_RX	TIMG4_3_C1	A0_0	COMP0_IN0-		
Pin B3	MSPM0Gx51x	PA29	I2C1_SCL	UART7_RTS	TIMG6_C0	UART5_RTS	I2C2_SCL			
	MSPM33C32xx	PA29	UC1_1_SCL_RX	UC12_RTS	TIMG4_2_C0	UC13_3_RTS_POCI	UC15_1_SCL			
Pin B4	MSPM0Gx51x	NRST								
	MSPM33C32xx	NRST								
Pin B5	MSPM0Gx51x	PC15								
	MSPM33C32xx	PC15								
Pin B6	MSPM0Gx51x	PC14	SPI2_SCK							
	MSPM33C32xx	PC14	UC13_1_SCL_RX_SCK							
Pin B7	MSPM0Gx51x	PA7	COMP0_OUT	CLK_OUT	TIMA0_C2	TIMG7_C1				
	MSPM33C32xx	PA7	COMP0_OUT	CLK_OUT	TIMA0_0_C2	TIMG4_3_C1				
Pin B8	MSPM0Gx51x	PB5	UART1_RX	UART3_RTS	TIMA0_C2N	SPI2_POCI				
	MSPM33C32xx	PB5	UC1_1_SCL_RX	UC13_0_RTS_POCI	TIMA0_0_C2N	UC13_1_RTS_POCI				
Pin B9	MSPM0Gx51x	PB29	SPI1_POCI	TIMA0_C0N	UART5_TX	TIMG9_C0				
	MSPM33C32xx	PB29	UC13_0_RTS_POCI	TIMA0_0_C0N	UC13_3_SDA_TX_PICO	TIMG8_1_C0				
Pin B10	MSPM0Gx51x	PC17								
	MSPM33C32xx	PC17								
Pin C1	MSPM0Gx51x	PB25	UART0_CTS	TIMA_FAL0	TIMA_FAL1	TIMA_FAL2	A0_4			
	MSPM33C32xx	PB25	UC1_0_CTS	TIMA0_0_FAL2	TIMA0_0_FAL2	TIMA0_0_FAL2	A0_4			

Table 3-2. NFBGA100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin C2	MSPM0Gx51x	PA26	UART3_TX	SPI1_CS0	TIMA_FAL0	CAN0_TX	TIMG7_C0	A0_1	COMP0_IN0+	
	MSPM33C32xx	PA26	UC13_0_SDA_TX_PICO	UC13_0_CTS_CS0	TIMA0_0_FAL0	CAN0_TX	TIMG4_3_C0	A0_1	COMP0_IN0+	
Pin C3	MSPM0Gx51x	PA28	UART0_TX	I2C0_SDA	TIMA_FAL0	UART5_CTS	I2C0_SDA			
	MSPM33C32xx	PA28	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL0	UC13_3_CTS_CS0	UC15_0_SDA			
Pin C4	MSPM0Gx51x	PA1	UART0_RX	I2C0_SCL	TIMA0_C1	TIMG8_IDX	UART5_TX	I2C0_SCL		
	MSPM33C32xx	PA1	UC1_0_SCL_RX	UC1_0_SCL_RX	TIMA0_0_C1	TIMG8_0_IDX	UC13_3_SDA_TX_PICO	UC15_0_SCL		
Pin C5	MSPM0Gx51x	PC12								
	MSPM33C32xx	PC12								
Pin C6	MSPM0Gx51x	PB0	UART0_TX							
	MSPM33C32xx	PB0	UC1_0_SDA_TX							
Pin C7	MSPM0Gx51x	PB1	UART0_RX							
	MSPM33C32xx	PB1	UC1_0_SCL_RX							
Pin C8	MSPM0Gx51x	PB2	I2C1_SCL	TIMA0_C3	TIMG6_C0					
	MSPM33C32xx	PB2	UC1_1_SCL_RX	TIMA0_0_C3	TIMG4_2_C0					
Pin C9	MSPM0Gx51x	PA9	UART1_RX	SPI0_PICO	TIMA0_C0N	CLK_OUT	RTC_OUT	UART0_CTS		
	MSPM33C32xx	PA9	UC1_1_SCL_RX	UC2_PICO	TIMA0_0_C0N	CLK_OUT	RTC_OUT	UC1_0_CTS		
Pin C10	MSPM0Gx51x	PC18								
	MSPM33C32xx	PC18								
Pin D1	MSPM0Gx51x	PA25	UART3_RX	TIMA0_C1N	A0_2					
	MSPM33C32xx	PA25	UC13_0_SCL_RX_SCK	TIMA0_0_C1N	A0_2					
Pin D2	MSPM0Gx51x	PB27	TIMG6_C1	A1_14	COMP1_IN0-					
	MSPM33C32xx	PB27	TIMG4_2_C1	A1_14	COMP1_IN0-					
Pin D3	MSPM0Gx51x	PA0	UART0_TX	I2C0_SDA	TIMA_FAL1	UART5_RX	I2C0_SDA			
	MSPM33C32xx	PA0	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL1	UC13_3_SCL_RX_SCK	UC15_0_SDA			
Pin D4	MSPM0Gx51x	PA30	I2C1_SDA	UART7_CTS	TIMG6_C1	I2C2_SDA				
	MSPM33C32xx	PA30	UC1_1_SDA_TX	UC12_CTS	TIMG4_2_C1	UC15_1_SDA				

Table 3-2. NFBGA100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin D5	MSPM0Gx51x	PC13	SPI2_PICO							
	MSPM33C32xx	PC13	UC13_1_SDA_TX_PICO							
Pin D6	MSPM0Gx51x	PC28	UART5_RX							
	MSPM33C32xx	PC28	UC13_3_SCL_RX_SCK							
Pin D7	MSPM0Gx51x	PB30	SPI1_PICO	TIMA0_C1	UART5_CTS	TIMG9_C1				
	MSPM33C32xx	PB30	UC13_0_SDA_TX_PICO	TIMA0_0_C1	UC13_3_CTS_CS0	TIMG8_1_C1				
Pin D8	MSPM0Gx51x	PB3	I2C1_SDA	TIMA0_C3N	TIMG6_C1					
	MSPM33C32xx	PB3	UC1_1_SDA_TX	TIMA0_0_C3N	TIMG4_2_C1					
Pin D9	MSPM0Gx51x	PB4	UART1_TX	UART3_CTS	TIMA0_C2	SPI2_PICO				
	MSPM33C32xx	PB4	UC1_1_SDA_TX	UC13_0_CTS_CS0	TIMA0_0_C2	UC13_1_SDA_TX_PICO				
Pin D10	MSPM0Gx51x	PA8	UART1_TX	TIMA0_C0	UART0_RTS					
	MSPM33C32xx	PA8	UC1_1_SDA_TX	TIMA0_0_C0	UC1_0_RTS					
Pin E1	MSPM0Gx51x	PA23	SPI0_CS3	TIMA0_C3	UART3_CTS	TIMG0_C0	SPI1_CS1	COMP1_IN1-	VREF+	
	MSPM33C32xx	PA23	UC2_CS3	TIMA0_0_C3	UC13_0_CTS_CS0	TIMG4_0_C0	UC13_0_CTS_CS0	COMP1_IN1-	VREF+	
Pin E2	MSPM0Gx51x	PA24	SPI0_CS2	TIMA0_C3N	UART3_RTS	TIMG0_C1	A0_3			
	MSPM33C32xx	PA24	UC2_CS2	TIMA0_0_C3N	UC13_0_RTS_POCI	TIMG4_0_C1	A0_3			
Pin E3	MSPM0Gx51x	PC27	CAN1_RX							
	MSPM33C32xx	PC27	CAN1_RX							
Pin E4	MSPM0Gx51x	PC25	TIMG9_IDX	UART6_CTS						
	MSPM33C32xx	PC25	TIMG8_1_IDX	UC14_CTS						
Pin E5	MSPM0Gx51x	PC11	TIMG9_C1	UART6_TX						
	MSPM33C32xx	PC11	TIMG8_1_C1	UC14_SDA_TX						
Pin E6	MSPM0Gx51x	PC16								
	MSPM33C32xx	PC16								
Pin E7	MSPM0Gx51x	PA10	UART0_TX	SPI0_POCI	I2C0_SDA	TIMA0_C2	TIMG12_C0	SPI2_SCK	I2C0_SDA	
	MSPM33C32xx	PA10	UC1_0_SDA_TX	UC2_POCI	UC1_0_SDA_TX	TIMA0_0_C2	TIMG12_0_C0	UC13_1_SCL_RX_SCK	UC15_0_SDA	

Table 3-2. NFBGA100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin E8	MSPM0Gx51x	PB28	SPI1_CS0	TIMA0_C0	UART5_RX					
	MSPM33C32xx	PB28	UC13_0_CTS_CS0	TIMA0_0_C0	UC13_3_SCL_RX_SCK					
Pin E9	MSPM0Gx51x	PA11	UART0_RX	SPI0_SCK	I2C0_SCL	TIMA0_C2N	COMP0_OUT	I2C0_SCL		
	MSPM33C32xx	PA11	UC1_0_SCL_RX	UC2_SCK	UC1_0_SCL_RX	TIMA0_0_C2N	COMP0_OUT	UC15_0_SCL		
Pin E10	MSPM0Gx51x	PB6	UART1_TX	UART7_CTS	SPI0_CS1	TIMG6_C0				
	MSPM33C32xx	PB6	UC1_1_SDA_TX	UC12_CTS	UC2_CS1	TIMG4_2_C0				
Pin F1	MSPM0Gx51x	PC26	CAN1_TX	UART6_RTS						
	MSPM33C32xx	PC26	CAN1_TX	UC14_RTS						
Pin F2	MSPM0Gx51x	PB24	SPI0_CS3	SPI0_CS1	TIMG12_C1	UART6_RTS	A0_5	COMP1_IN1+		
	MSPM33C32xx	PB24	UC2_CS3	UC2_CS3	TIMG12_0_C1	UC14_RTS	A0_5	COMP1_IN1+		
Pin F3	MSPM0Gx51x	PB20	SPI0_CS2	TIMG12_C0	TIMA0_C1	A0_6				
	MSPM33C32xx	PB20	UC2_CS2	TIMG12_0_C0	TIMA0_0_C1	A0_6				
Pin F4	MSPM0Gx51x	PC9	UART3_RTS	TIMA0_C1N						
	MSPM33C32xx	PC9	UC13_0_RTS_POCI	TIMA0_0_C1N						
Pin F5	MSPM0Gx51x	PC10	TIMG9_C0	UART6_RX						
	MSPM33C32xx	PC10	TIMG8_1_C0	UC14_SCL_RX						
Pin F6	MSPM0Gx51x	PC29	UART5_TX							
	MSPM33C32xx	PC29	UC13_3_SDA_TX_PICO							
Pin F7	MSPM0Gx51x	PC19								
	MSPM33C32xx	PC19								
Pin F8	MSPM0Gx51x	PB7	UART1_RX	SPI1_POCI	UART7_RTS	TIMG9_C0	TIMG6_C1			
	MSPM33C32xx	PB7	UC1_1_SCL_RX	UC13_0_RTS_POCI	UC12_RTS	TIMG8_1_C0	TIMG4_2_C1			
Pin F9	MSPM0Gx51x	PB8	UART1_CTS	SPI1_PICO	I2C2_SCL	COMP0_OUT	TIMG9_IDX	COMP1_OUT		
	MSPM33C32xx	PB8	UC1_1_CTS	UC13_0_SDA_TX_PICO	UC13_0_SCL_RX_SCK	COMP1_OUT	TIMG8_1_IDX	COMP1_OUT		
Pin F10	MSPM0Gx51x	PB10	TIMG0_C0	UART4_TX	TIMG6_C0					
	MSPM33C32xx	PB10	TIMG4_0_C0	UC13_2_SDA_TX_PICO	TIMG4_2_C0					

Table 3-2. NFBGA100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin G1	MSPM0Gx51x	PB23	SPI1_SCK	UART6_CTS	A1_11					
	MSPM33C32xx	PB23	UC13_0_SCL_RX_SCK	UC14_CTS	A1_11					
Pin G2	MSPM0Gx51x	PB21	TIMG8_C0	CAN1_TX	UART6_RX	A1_8				
	MSPM33C32xx	PB21	TIMG8_0_C0	CAN1_TX	UC14_SCL_RX	A1_8				
Pin G3	MSPM0Gx51x	PC7	UART3_RX	SPI0_CS0	TIMA0_C0N					
	MSPM33C32xx	PC7	UC13_0_SCL_RX_SCK	UC2_CS0	TIMA0_0_C0N					
Pin G4	MSPM0Gx51x	PC8	UART3_CTS	SPI1_CS2	TIMA0_C1					
	MSPM33C32xx	PC8	UC13_0_CTS_CS0	UC13_0_CTS_CS0	TIMA0_0_C1					
Pin G5	MSPM0Gx51x	PC5	TIMA0_C1N							
	MSPM33C32xx	PC5	TIMA0_0_C1N							
Pin G6	MSPM0Gx51x	PC4	TIMA0_C1							
	MSPM33C32xx	PC4	TIMA0_0_C1							
Pin G7	MSPM0Gx51x	PB9	UART1_RTS	SPI1_SCK	I2C2_SDA	TIMA0_C0N	TIMG9_C1			
	MSPM33C32xx	PB9	UC1_1_RTS	UC13_0_SCL_RX_SCK	UC13_0_SDA_TX_PICO	TIMA0_0_C0N	TIMG8_1_C1			
Pin G8	MSPM0Gx51x	PB15	UART7_TX	TIMG8_C0	TIMG7_C0					
	MSPM33C32xx	PB15	UC12_TX	TIMG8_0_C0	TIMG4_3_C0					
Pin G9	MSPM0Gx51x	PB11	TIMG0_C1	CLK_OUT	UART4_RX	TIMG6_C1				
	MSPM33C32xx	PB11	TIMG4_0_C1	CLK_OUT	UC13_2_SCL_RX_SCK	TIMG4_2_C1				
Pin G10	MSPM0Gx51x	PB12	UART3_TX	TIMA_FAL1	UART4_CTS					
	MSPM33C32xx	PB12	UC13_0_SDA_TX_PICO	TIMA0_0_FAL1	UC13_2_CTS_CS0					
Pin H1	MSPM0Gx51x	PB22	SPI1_PICO	TIMG8_C1	CAN1_RX	UART6_TX	A1_10			
	MSPM33C32xx	PB22	UC13_0_SDA_TX_PICO	TIMG8_0_C1	CAN1_RX	UC14_SDA_TX	A1_10			
Pin H2	MSPM0Gx51x	PA22	UART1_RTS	TIMA0_C0N	CLK_OUT	TIMG6_C1	A0_7			
	MSPM33C32xx	PA22	UC1_1_RTS	TIMA0_0_C0N	CLK_OUT	TIMG4_2_C1	A0_7			
Pin H3	MSPM0Gx51x	PC6	UART3_TX	SPI0_CS1	TIMA0_C0					
	MSPM33C32xx	PC6	UC13_0_SDA_TX_PICO	UC2_CS1	TIMA0_0_C0					

Table 3-2. NFBGA100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping							
Pin H4	MSPM0Gx51x	PC3	I2C2_SDA	TIMA0_C0N					
	MSPM33C32xx	PC3	UC13_0_SDA_TX_PICO	TIMA0_0_C0N					
Pin H5	MSPM0Gx51x	PC2	I2C2_SCL	SPI1_CS0	TIMA0_C0				
	MSPM33C32xx	PC2	UC13_0_SCL_RX_SCK	UC13_0_CTS_CS0	TIMA0_0_C0				
Pin H6	MSPM0Gx51x	PC21	CAN1_TX						
	MSPM33C32xx	PC21	CAN1_TX						
Pin H7	MSPM0Gx51x	PA16	SPI1_POCI	I2C1_SDA	TIMA0_C2N	FCC_IN	A1_1	I2C2_SDA	
	MSPM33C32xx	PA16	UC13_0_RTS_POCI	UC1_1_SDA_TX	TIMA0_0_C2N	FCC_IN	A1_1	UC15_1_SDA	
Pin H8	MSPM0Gx51x	PC1	TIMG8_C1	TIMA0_C2N					
	MSPM33C32xx	PC1	TIMG8_0_C1	TIMA0_0_C2N					
Pin H9	MSPM0Gx51x	PC20							
	MSPM33C32xx	PC20							
Pin H10	MSPM0Gx51x	PB13	UART3_RX	TIMG12_C0	TIMA0_C1N	UART4_RTS			
	MSPM33C32xx	PB13	UC13_0_SCL_RX_SCK	TIMG12_0_C0	TIMA0_0_C1N	UC13_2_RTS_POCI			
Pin J1	MSPM0Gx51x	PB19	SPI0_POCI	UART0_CTS	TIMG7_C1	A1_6			
	MSPM33C32xx	PB19	UC2_POCI	UC1_0_CTS	TIMG4_3_C1	A1_6			
Pin J2	MSPM0Gx51x	PA21	UART1_CTS	TIMA0_C0	TIMG6_C0	A1_7	VREF-		
	MSPM33C32xx	PA21	UC1_1_CTS	TIMA0_0_C0	TIMG4_2_C0	A1_7	VREF-		
Pin J3	MSPM0Gx51x	PA20	SWCLK	A0_14					
	MSPM33C32xx	PA20	SWCLK	A0_16					
Pin J4	MSPM0Gx51x	PA19	SWDIO	A0_13					
	MSPM33C32xx	PA19	SWDIO	A0_15					
Pin J5	MSPM0Gx51x	PC24							
	MSPM33C32xx	PC24							
Pin J6	MSPM0Gx51x	PC23							
	MSPM33C32xx	PC23							
Pin J7	MSPM0Gx51x	PC0	TIMG8_C0	TIMA0_C2					
	MSPM33C32xx	PC0	TIMG8_0_C0	TIMA0_0_C2					

Table 3-2. NFBGA100 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin J8	MSPM0Gx51x	PB16	UART7_RX	TIMG8_C1	TIMG7_C1					
	MSPM33C32xx	PB16	UC12_RX	TIMG8_0_C1	TIMG4_3_C1					
Pin J9	MSPM0Gx51x	PB14	SPI1_POCI	TIMG12_C1	TIMA0_C0	TIMG8_IDX				
	MSPM33C32xx	PB14	UC13_0_RTS_POCI	TIMG12_0_C1	TIMA0_0_C0	TIMG8_0_IDX				
Pin J10	MSPM0Gx51x	PA12	UART3_CTS	FCC_IN	TIMG0_C0	SPI1_CS1	CAN0_TX	A0_8		
	MSPM33C32xx	PA12	UC13_0_CTS_CS0	FCC_IN	TIMG4_0_C0	UC13_0_CTS_CS0	CAN0_TX	A0_8		
Pin K1	MSPM0Gx51x	PB18	SPI0_SCK	TIMA0_C2N	A1_5	COMP1_IN2+				
	MSPM33C32xx	PB18	UC2_SCK	TIMA0_0_C2N	A1_5	COMP1_IN2+				
Pin K2	MSPM0Gx51x	PB17	SPI0_PICO	TIMA0_C2	A1_4	COMP1_IN2-				
	MSPM33C32xx	PB17	UC2_PICO	TIMA0_0_C2	A1_4	COMP1_IN2-				
Pin K3	MSPM0Gx51x	PA18	UART1_RX	SPI1_PICO	TIMA0_C3N	A1_3	COMP0_IN1+			
	MSPM33C32xx	PA18	UC1_1_SCL_RX	UC13_0_SDA_TX_PICO	TIMA0_0_C3N	A1_3	COMP0_IN1+			
Pin K4	MSPM0Gx51x	PA17	UART1_TX	SPI1_SCK	TIMA0_C3	TIMG7_C0	A1_2	COMP0_IN1-		
	MSPM33C32xx	PA17	UC1_1_SDA_TX	UC13_0_SCL_RX_SCK	TIMA0_0_C3	TIMG4_3_C0	A1_2	COMP0_IN1-		
Pin K5	MSPM0Gx51x	PC22	CAN1_RX							
	MSPM33C32xx	PC22	CAN1_RX							
Pin K6	MSPM0Gx51x	VDD								
	MSPM33C32xx	VDD								
Pin K7	MSPM0Gx51x	PA15	UART0_RTS	I2C1_SCL	TIMA0_C2	TIMG8_IDX	A1_0	COMP0_IN3+	COMP1_IN3+	I2C2_SCL
	MSPM33C32xx	PA15	UC1_0_RTS	UC1_1_SCL_RX	TIMA0_0_C2	TIMG8_0_IDX	A1_0	COMP0_IN3+	COMP1_IN3+	UC15_1_SCL
Pin K8	MSPM0Gx51x	PA14	UART0_CTS	UART3_TX	CLK_OUT	UART7_RX	A0_12	COMP0_IN2+		
	MSPM33C32xx	PA14	UC1_0_CTS	UC13_0_SDA_TX_PICO	CLK_OUT	UC12_RX	A0_12	COMP0_IN2+		
Pin K9	MSPM0Gx51x	VSS								
	MSPM33C32xx	VSS								
Pin K10	MSPM0Gx51x	PA13	UART3_RTS	UART3_RX	TIMG0_C1	UART7_TX	CAN0_RX	A0_9	COMP0_IN2-	
	MSPM33C32xx	PA13	UC13_0_RTS_POCI	UC13_0_SCL_RX_SCK	TIMG4_0_C1	UC12_TX	CAN0_RX	A0_9	COMP0_IN2-	

Table 3-3. LQFP80 common functionality between MSPM0Gx51x and MSPM33C32xx

Pin Number	Device Family	Function Mapping								
Pin 1	MSPM0Gx51x	PA0	UART0_TX	I2C0_SDA	TIMA_FAL1	UART5_RX	I2C0_SDA			
	MSPM33C32xx	PA0	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL1	UC13_3_SCL_RX_SCK	UC15_0_SDA			
Pin 2	MSPM0Gx51x	PA1	UART0_RX	I2C0_SCL	TIMA0_C1	TIMG8_IDX	UART5_TX	I2C0_SCL		
	MSPM33C32xx	PA1	UC1_0_SCL_RX	UC1_0_SCL_RX	TIMA0_0_C1	TIMG8_0_IDX	UC13_3_SDA_TX_PICO	UC15_0_SCL		
Pin 3	MSPM0Gx51x	PA28	UART0_TX	I2C0_SDA	TIMA_FAL0	UART5_CTS	I2C0_SDA			
	MSPM33C32xx	PA28	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL0	UC13_3_CTS_CS0	UC15_0_SDA			
Pin 4	MSPM0Gx51x	PA29	I2C1_SCL	UART7_RTS	TIMG6_C0	UART5_RTS	I2C2_SCL			
	MSPM33C32xx	PA29	UC1_1_SCL_RX	UC12_RTS	TIMG4_2_C0	UC13_3_RTS_POCI	UC15_1_SCL			
Pin 5	MSPM0Gx51x	PA30	I2C1_SDA	UART7_CTS	TIMG6_C1	I2C2_SDA				
	MSPM33C32xx	PA30	UC1_1_SDA_TX	UC12_CTS	TIMG4_2_C1	UC15_1_SDA				
Pin 6	MSPM0Gx51x	NRST								
	MSPM33C32xx	NRST								
Pin 8	MSPM0Gx51x	VDD								
	MSPM33C32xx	VDD								
Pin 9	MSPM0Gx51x	VSS								
	MSPM33C32xx	VSS								
Pin 10	MSPM0Gx51x	PA2	TIMG8_C1	SPI0_CS0	SPI2_POCI					
	MSPM33C32xx	PA2	TIMG8_0_C1	UC2_CS0	UC13_1_RTS_POCI					
Pin 11	MSPM0Gx51x	PA3	TIMG8_C0	SPI0_CS1	I2C1_SDA	TIMA0_C1	COMP0_OUT	UART1_TX	SPI0_CS3	COMP1_OUT
	MSPM33C32xx	PA3	TIMG8_0_C0	UC2_CS1	UC1_1_SDA_TX	TIMA0_0_C1	COMP1_OUT	UC1_1_SDA_TX	UC2_CS1	COMP1_OUT
Pin 12	MSPM0Gx51x	PA4	SPI0_POCI	I2C1_SCL	TIMA0_C1N	LFCLK_IN	UART1_RX	SPI2_CS0		
	MSPM33C32xx	PA4	UC2_POCI	UC1_1_SCL_RX	TIMA0_0_C1N	LFCLK_IN	UC1_1_SCL_RX	UC13_1_CTS_CS0		
Pin 13	MSPM0Gx51x	PA5	SPI0_PICO	TIMG0_C0	TIMG6_C0					
	MSPM33C32xx	PA5	UC2_PICO	TIMG4_0_C0	TIMG4_2_C0					
Pin 14	MSPM0Gx51x	PA6	SPI0_SCK	TIMG0_C1	HFCLK_IN	TIMG6_C1	TIMA0_C2N			
	MSPM33C32xx	PA6	UC2_SCK	TIMG4_0_C1	HFCLK_IN	TIMG4_2_C1	TIMA0_0_C2N			

Table 3-3. LQFP80 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 15	MSPM0Gx51x	PB0	UART0_TX							
	MSPM33C32xx	PB0	UC1_0_SDA_TX							
Pin 16	MSPM0Gx51x	PB1	UART0_RX							
	MSPM33C32xx	PB1	UC1_0_SCL_RX							
Pin 17	MSPM0Gx51x	PA7	COMP0_OUT	CLK_OUT	TIMA0_C2	TIMG7_C1				
	MSPM33C32xx	PA7	COMP0_OUT	CLK_OUT	TIMA0_0_C2	TIMG4_3_C1				
Pin 18	MSPM0Gx51x	PB2	I2C1_SCL	TIMA0_C3	TIMG6_C0					
	MSPM33C32xx	PB2	UC1_1_SCL_RX	TIMA0_0_C3	TIMG4_2_C0					
Pin 19	MSPM0Gx51x	PB3	I2C1_SDA	TIMA0_C3N	TIMG6_C1					
	MSPM33C32xx	PB3	UC1_1_SDA_TX	TIMA0_0_C3N	TIMG4_2_C1					
Pin 20	MSPM0Gx51x	PB4	UART1_TX	UART3_CTS	TIMA0_C2	SPI2_PICO				
	MSPM33C32xx	PB4	UC1_1_SDA_TX	UC13_0_CTS_CS0	TIMA0_0_C2	UC13_1_SDA_TX_PICO				
Pin 21	MSPM0Gx51x	PB5	UART1_RX	UART3_RTS	TIMA0_C2N	SPI2_POCI				
	MSPM33C32xx	PB5	UC1_1_SCL_RX	UC13_0_RTS_POCI	TIMA0_0_C2N	UC13_1_RTS_POCI				
Pin 22	MSPM0Gx51x	PA8	UART1_TX	TIMA0_C0	UART0_RTS					
	MSPM33C32xx	PA8	UC1_1_SDA_TX	TIMA0_0_C0	UC1_0_RTS					
Pin 23	MSPM0Gx51x	PA9	UART1_RX	SPI0_PICO	TIMA0_C0N	CLK_OUT	RTC_OUT	UART0_CTS		
	MSPM33C32xx	PA9	UC1_1_SCL_RX	UC2_PICO	TIMA0_0_C0N	CLK_OUT	RTC_OUT	UC1_0_CTS		
Pin 24	MSPM0Gx51x	PB28	SPI1_CS0	TIMA0_C0	UART5_RX					
	MSPM33C32xx	PB28	UC13_0_CTS_CS0	TIMA0_0_C0	UC13_3_SCL_RX_SCK					
Pin 25	MSPM0Gx51x	PB29	SPI1_POCI	TIMA0_C0N	UART5_TX	TIMG9_C0				
	MSPM33C32xx	PB29	UC13_0_RTS_POCI	TIMA0_0_C0N	UC13_3_SDA_TX_PICO	TIMG8_1_C0				
Pin 26	MSPM0Gx51x	PB30	SPI1_PICO	TIMA0_C1	UART5_CTS	TIMG9_C1				
	MSPM33C32xx	PB30	UC13_0_SDA_TX_PICO	TIMA0_0_C1	UC13_3_CTS_CS0	TIMG8_1_C1				

Table 3-3. LQFP80 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping							
Pin 27	MSPM0Gx51x	PB31	SPI1_SCK	TIMG8_IDX	TIMA0_C1N	UART5_RTS	TIMG9_IDX		
	MSPM33C32xx	PB31	UC13_0_SCL_RX_SCK	TIMG8_0_IDX	TIMA0_0_C1N	UC13_3_RTS_POCI	TIMG8_1_IDX		
Pin 28	MSPM0Gx51x	PA10	UART0_TX	SPI0_POCI	I2C0_SDA	TIMA0_C2	TIMG12_C0	SPI2_SCK	I2C0_SDA
	MSPM33C32xx	PA10	UC1_0_SDA_TX	UC2_POCI	UC1_0_SDA_TX	TIMA0_0_C2	TIMG12_0_C0	UC13_1_SCL_RX_SCK	UC15_0_SDA
Pin 29	MSPM0Gx51x	PA11	UART0_RX	SPI0_SCK	I2C0_SCL	TIMA0_C2N	COMP0_OUT	I2C0_SCL	
	MSPM33C32xx	PA11	UC1_0_SCL_RX	UC2_SCK	UC1_0_SCL_RX	TIMA0_0_C2N	COMP0_OUT	UC15_0_SCL	
Pin 30	MSPM0Gx51x	PB6	UART1_TX	UART7_CTS	SPI0_CS1	TIMG6_C0			
	MSPM33C32xx	PB6	UC1_1_SDA_TX	UC12_CTS	UC2_CS1	TIMG4_2_C0			
Pin 31	MSPM0Gx51x	PB7	UART1_RX	SPI1_POCI	UART7_RTS	TIMG9_C0	TIMG6_C1		
	MSPM33C32xx	PB7	UC1_1_SCL_RX	UC13_0_RTS_POCI	UC12_RTS	TIMG8_1_C0	TIMG4_2_C1		
Pin 32	MSPM0Gx51x	PB8	UART1_CTS	SPI1_PICO	I2C2_SCL	COMP0_OUT	TIMG9_IDX	COMP1_OUT	
	MSPM33C32xx	PB8	UC1_1_CTS	UC13_0_SDA_TX_PICO	UC13_0_SCL_RX_SCK	COMP1_OUT	TIMG8_1_IDX	COMP1_OUT	
Pin 33	MSPM0Gx51x	PB9	UART1_RTS	SPI1_SCK	I2C2_SDA	TIMA0_C0N	TIMG9_C1		
	MSPM33C32xx	PB9	UC1_1_RTS	UC13_0_SCL_RX_SCK	UC13_0_SDA_TX_PICO	TIMA0_0_C0N	TIMG8_1_C1		
Pin 34	MSPM0Gx51x	PB10	TIMG0_C0	UART4_TX	TIMG6_C0				
	MSPM33C32xx	PB10	TIMG4_0_C0	UC13_2_SDA_TX_PICO	TIMG4_2_C0				
Pin 35	MSPM0Gx51x	PB11	TIMG0_C1	CLK_OUT	UART4_RX	TIMG6_C1			
	MSPM33C32xx	PB11	TIMG4_0_C1	CLK_OUT	UC13_2_SCL_RX_SCK	TIMG4_2_C1			
Pin 36	MSPM0Gx51x	PB12	UART3_TX	TIMA_FAL1	UART4_CTS				
	MSPM33C32xx	PB12	UC13_0_SDA_TX_PICO	TIMA0_0_FAL1	UC13_2_CTS_CS0				
Pin 37	MSPM0Gx51x	PB13	UART3_RX	TIMG12_C0	TIMA0_C1N	UART4_RTS			
	MSPM33C32xx	PB13	UC13_0_SCL_RX_SCK	TIMG12_0_C0	TIMA0_0_C1N	UC13_2_RTS_POCI			
Pin 38	MSPM0Gx51x	PB14	SPI1_POCI	TIMG12_C1	TIMA0_C0	TIMG8_IDX			
	MSPM33C32xx	PB14	UC13_0_RTS_POCI	TIMG12_0_C1	TIMA0_0_C0	TIMG8_0_IDX			

Table 3-3. LQFP80 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 39	MSPM0Gx51x	PB15	UART7_TX	TIMG8_C0	TIMG7_C0					
	MSPM33C32xx	PB15	UC12_TX	TIMG8_0_C0	TIMG4_3_C0					
Pin 40	MSPM0Gx51x	PB16	UART7_RX	TIMG8_C1	TIMG7_C1					
	MSPM33C32xx	PB16	UC12_RX	TIMG8_0_C1	TIMG4_3_C1					
Pin 41	MSPM0Gx51x	PA12	UART3_CTS	FCC_IN	TIMG0_C0	SPI1_CS1	CAN0_TX	A0_8		
	MSPM33C32xx	PA12	UC13_0_CTS_CS0	FCC_IN	TIMG4_0_C0	UC13_0_CTS_CS0	CAN0_TX	A0_8		
Pin 42	MSPM0Gx51x	PA13	UART3_RTS	UART3_RX	TIMG0_C1	UART7_TX	CAN0_RX	A0_9	COMP0_IN2-	
	MSPM33C32xx	PA13	UC13_0_RTS_POCI	UC13_0_SCL_RX_SCK	TIMG4_0_C1	UC12_TX	CAN0_RX	A0_9	COMP0_IN2-	
Pin 43	MSPM0Gx51x	PA14	UART0_CTS	UART3_TX	CLK_OUT	UART7_RX	A0_12	COMP0_IN2+		
	MSPM33C32xx	PA14	UC1_0_CTS	UC13_0_SDA_TX_PICO	CLK_OUT	UC12_RX	A0_12	COMP0_IN2+		
Pin 44	MSPM0Gx51x	PA15	UART0_RTS	I2C1_SCL	TIMA0_C2	TIMG8_IDX	A1_0	COMP0_IN3+	COMP1_IN3+	I2C2_SCL
	MSPM33C32xx	PA15	UC1_0_RTS	UC1_1_SCL_RX	TIMA0_0_C2	TIMG8_0_IDX	A1_0	COMP0_IN3+	COMP1_IN3+	UC15_1_SCL
Pin 45	MSPM0Gx51x	PA16	SPI1_POCI	I2C1_SDA	TIMA0_C2N	FCC_IN	A1_1	I2C2_SDA		
	MSPM33C32xx	PA16	UC13_0_RTS_POCI	UC1_1_SDA_TX	TIMA0_0_C2N	FCC_IN	A1_1	UC15_1_SDA		
Pin 46	MSPM0Gx51x	PC0	TIMG8_C0	TIMA0_C2						
	MSPM33C32xx	PC0	TIMG8_0_C0	TIMA0_0_C2						
Pin 47	MSPM0Gx51x	PC1	TIMG8_C1	TIMA0_C2N						
	MSPM33C32xx	PC1	TIMG8_0_C1	TIMA0_0_C2N						
Pin 48	MSPM0Gx51x	VSS								
	MSPM33C32xx	VSS								
Pin 49	MSPM0Gx51x	VDD								
	MSPM33C32xx	VDD								
Pin 50	MSPM0Gx51x	PC2	I2C2_SCL	SPI1_CS0	TIMA0_C0					
	MSPM33C32xx	PC2	UC13_0_SCL_RX_SCK	UC13_0_CTS_CS0	TIMA0_0_C0					
Pin 51	MSPM0Gx51x	PC3	I2C2_SDA	TIMA0_C0N						
	MSPM33C32xx	PC3	UC13_0_SDA_TX_PICO	TIMA0_0_C0N						

Table 3-3. LQFP80 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 52	MSPM0Gx51x	PC4	TIMA0_C1							
	MSPM33C32xx	PC4	TIMA0_0_C1							
Pin 53	MSPM0Gx51x	PC5	TIMA0_C1N							
	MSPM33C32xx	PC5	TIMA0_0_C1N							
Pin 54	MSPM0Gx51x	PA17	UART1_TX	SPI1_SCK	TIMA0_C3	TIMG7_C0	A1_2	COMP0_IN1-		
	MSPM33C32xx	PA17	UC1_1_SDA_TX	UC13_0_SCL_RX_SCK	TIMA0_0_C3	TIMG4_3_C0	A1_2	COMP0_IN1-		
Pin 55	MSPM0Gx51x	PA18	UART1_RX	SPI1_PICO	TIMA0_C3N	A1_3	COMP0_IN1+			
	MSPM33C32xx	PA18	UC1_1_SCL_RX	UC13_0_SDA_TX_PICO	TIMA0_0_C3N	A1_3	COMP0_IN1+			
Pin 56	MSPM0Gx51x	PA19	SWDIO	A0_13						
	MSPM33C32xx	PA19	SWDIO	A0_15						
Pin 57	MSPM0Gx51x	PA20	SWCLK	A0_14						
	MSPM33C32xx	PA20	SWCLK	A0_16						
Pin 58	MSPM0Gx51x	PB17	SPI0_PICO	TIMA0_C2	A1_4	COMP1_IN2-				
	MSPM33C32xx	PB17	UC2_PICO	TIMA0_0_C2	A1_4	COMP1_IN2-				
Pin 59	MSPM0Gx51x	PB18	SPI0_SCK	TIMA0_C2N	A1_5	COMP1_IN2+				
	MSPM33C32xx	PB18	UC2_SCK	TIMA0_0_C2N	A1_5	COMP1_IN2+				
Pin 60	MSPM0Gx51x	PB19	SPI0_POCI	UART0_CTS	TIMG7_C1	A1_6				
	MSPM33C32xx	PB19	UC2_POCI	UC1_0_CTS	TIMG4_3_C1	A1_6				
Pin 61	MSPM0Gx51x	PA21	UART1_CTS	TIMA0_C0	TIMG6_C0	A1_7	VREF-			
	MSPM33C32xx	PA21	UC1_1_CTS	TIMA0_0_C0	TIMG4_2_C0	A1_7	VREF-			
Pin 62	MSPM0Gx51x	PA22	UART1_RTS	TIMA0_C0N	CLK_OUT	TIMG6_C1	A0_7			
	MSPM33C32xx	PA22	UC1_1_RTS	TIMA0_0_C0N	CLK_OUT	TIMG4_2_C1	A0_7			
Pin 63	MSPM0Gx51x	PC6	UART3_TX	SPI0_CS1	TIMA0_C0					
	MSPM33C32xx	PC6	UC13_0_SDA_TX_PICO	UC2_CS1	TIMA0_0_C0					
Pin 64	MSPM0Gx51x	PC7	UART3_RX	SPI0_CS0	TIMA0_C0N					
	MSPM33C32xx	PC7	UC13_0_SCL_RX_SCK	UC2_CS0	TIMA0_0_C0N					
Pin 65	MSPM0Gx51x	PC8	UART3_CTS	SPI1_CS2	TIMA0_C1					
	MSPM33C32xx	PC8	UC13_0_CTS_CS0	UC13_0_CTS_CS0	TIMA0_0_C1					

Table 3-3. LQFP80 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 66	MSPM0Gx51x	PC9	UART3_RTS	TIMA0_C1N						
	MSPM33C32xx	PC9	UC13_0_RTS_POCI	TIMA0_0_C1N						
Pin 67	MSPM0Gx51x	PB20	SPI0_CS2	TIMG12_C0	TIMA0_C1	A0_6				
	MSPM33C32xx	PB20	UC2_CS2	TIMG12_0_C0	TIMA0_0_C1	A0_6				
Pin 68	MSPM0Gx51x	PB21	TIMG8_C0	CAN1_TX	UART6_RX	A1_8				
	MSPM33C32xx	PB21	TIMG8_0_C0	CAN1_TX	UC14_SCL_RX	A1_8				
Pin 69	MSPM0Gx51x	PB22	SPI1_PICO	TIMG8_C1	CAN1_RX	UART6_TX	A1_10			
	MSPM33C32xx	PB22	UC13_0_SDA_TX_PICO	TIMG8_0_C1	CAN1_RX	UC14_SDA_TX	A1_10			
Pin 70	MSPM0Gx51x	PB23	SPI1_SCK	UART6_CTS	A1_11					
	MSPM33C32xx	PB23	UC13_0_SCL_RX_SCK	UC14_CTS	A1_11					
Pin 71	MSPM0Gx51x	PB24	SPI0_CS3	SPI0_CS1	TIMG12_C1	UART6_RTS	A0_5	COMP1_IN1+		
	MSPM33C32xx	PB24	UC2_CS3	UC2_CS3	TIMG12_0_C1	UC14_RTS	A0_5	COMP1_IN1+		
Pin 72	MSPM0Gx51x	PA23	SPI0_CS3	TIMA0_C3	UART3_CTS	TIMG0_C0	SPI1_CS1	COMP1_IN1-	VREF+	
	MSPM33C32xx	PA23	UC2_CS3	TIMA0_0_C3	UC13_0_CTS_CS0	TIMG4_0_C0	UC13_0_CTS_CS0	COMP1_IN1-	VREF+	
Pin 73	MSPM0Gx51x	PA24	SPI0_CS2	TIMA0_C3N	UART3_RTS	TIMG0_C1	A0_3			
	MSPM33C32xx	PA24	UC2_CS2	TIMA0_0_C3N	UC13_0_RTS_POCI	TIMG4_0_C1	A0_3			
Pin 74	MSPM0Gx51x	PA25	UART3_RX	TIMA0_C1N	A0_2					
	MSPM33C32xx	PA25	UC13_0_SCL_RX_SCK	TIMA0_0_C1N	A0_2					
Pin 75	MSPM0Gx51x	PB25	UART0_CTS	TIMA_FAL0	TIMA_FAL1	TIMA_FAL2	A0_4			
	MSPM33C32xx	PB25	UC1_0_CTS	TIMA0_0_FAL2	TIMA0_0_FAL2	TIMA0_0_FAL2	A0_4			
Pin 76	MSPM0Gx51x	PB26	UART0_RTS	TIMG6_C0	A1_13	COMP1_IN0+				
	MSPM33C32xx	PB26	UC1_0_RTS	TIMG4_2_C0	A1_13	COMP1_IN0+				
Pin 77	MSPM0Gx51x	PB27	TIMG6_C1	A1_14	COMP1_IN0-					
	MSPM33C32xx	PB27	TIMG4_2_C1	A1_14	COMP1_IN0-					
Pin 78	MSPM0Gx51x	PA26	UART3_TX	SPI1_CS0	TIMA_FAL0	CAN0_TX	TIMG7_C0	A0_1	COMP0_IN0+	
	MSPM33C32xx	PA26	UC13_0_SDA_TX_PICO	UC13_0_CTS_CS0	TIMA0_0_FAL0	CAN0_TX	TIMG4_3_C0	A0_1	COMP0_IN0+	

Table 3-3. LQFP80 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 79	MSPM0Gx51x	PA27	TIMA_FAL2	RTC_OUT	CAN0_RX	TIMG7_C1	A0_0	COMP0_IN0-		
	MSPM33C32xx	PA27	TIMA0_0_FAL2	RTC_OUT	CAN0_RX	TIMG4_3_C1	A0_0	COMP0_IN0-		
Pin 80	MSPM0Gx51x	VCORE								
	MSPM33C32xx	VCORE								

Table 3-4. LQFP64 common functionality between MSPM0Gx51x and MSPM33C32xx

Pin Number	Device Family	Function Mapping								
Pin 1	MSPM0Gx51x	PB13	UART3_RX	TIMG12_C0	TIMA0_C1N	UART4_RTS				
	MSPM33C32xx	PB13	UC13_0_SCL_RX_SCK	TIMG12_0_C0	TIMA0_0_C1N	UC13_2_RTS_POCI				
Pin 2	MSPM0Gx51x	PB14	SPI1_POCI	TIMG12_C1	TIMA0_C0	TIMG8_IDX				
	MSPM33C32xx	PB14	UC13_0_RTS_POCI	TIMG12_0_C1	TIMA0_0_C0	TIMG8_0_IDX				
Pin 3	MSPM0Gx51x	PB15	UART7_TX	TIMG8_C0	TIMG7_C0					
	MSPM33C32xx	PB15	UC12_TX	TIMG8_0_C0	TIMG4_3_C0					
Pin 4	MSPM0Gx51x	PB16	UART7_RX	TIMG8_C1	TIMG7_C1					
	MSPM33C32xx	PB16	UC12_RX	TIMG8_0_C1	TIMG4_3_C1					
Pin 5	MSPM0Gx51x	PA12	UART3_CTS	FCC_IN	TIMG0_C0	SPI1_CS1	CAN0_TX	A0_8		
	MSPM33C32xx	PA12	UC13_0_CTS_CS0	FCC_IN	TIMG4_0_C0	UC13_0_CTS_CS0	CAN0_TX	A0_8		
Pin 6	MSPM0Gx51x	PA13	UART3_RTS	UART3_RX	TIMG0_C1	UART7_TX	CAN0_RX	A0_9	COMP0_IN2-	
	MSPM33C32xx	PA13	UC13_0_RTS_POCI	UC13_0_SCL_RX_SCK	TIMG4_0_C1	UC12_TX	CAN0_RX	A0_9	COMP0_IN2-	
Pin 7	MSPM0Gx51x	PA14	UART0_CTS	UART3_TX	CLK_OUT	UART7_RX	A0_12	COMP0_IN2+		
	MSPM33C32xx	PA14	UC1_0_CTS	UC13_0_SDA_TX_PICO	CLK_OUT	UC12_RX	A0_12	COMP0_IN2+		
Pin 10	MSPM0Gx51x	PA17	UART1_TX	SPI1_SCK	TIMA0_C3	TIMG7_C0	A1_2	COMP0_IN1-		
	MSPM33C32xx	PA17	UC1_1_SDA_TX	UC13_0_SCL_RX_SCK	TIMA0_0_C3	TIMG4_3_C0	A1_2	COMP0_IN1-		
Pin 11	MSPM0Gx51x	PA18	UART1_RX	SPI1_PICO	TIMA0_C3N	A1_3	COMP0_IN1+			
	MSPM33C32xx	PA18	UC1_1_SCL_RX	UC13_0_SDA_TX_PICO	TIMA0_0_C3N	A1_3	COMP0_IN1+			
Pin 12	MSPM0Gx51x	PA19	SWDIO	A0_13						
	MSPM33C32xx	PA19	SWDIO	A0_15						

Table 3-4. LQFP64 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 13	MSPM0Gx51x	PA20	SWCLK	A0_14						
	MSPM33C32xx	PA20	SWCLK	A0_16						
Pin 14	MSPM0Gx51x	PB17	SPI0_PICO	TIMA0_C2	A1_4	COMP1_IN2-				
	MSPM33C32xx	PB17	UC2_PICO	TIMA0_0_C2	A1_4	COMP1_IN2-				
Pin 15	MSPM0Gx51x	PB18	SPI0_SCK	TIMA0_C2N	A1_5	COMP1_IN2+				
	MSPM33C32xx	PB18	UC2_SCK	TIMA0_0_C2N	A1_5	COMP1_IN2+				
Pin 16	MSPM0Gx51x	PB19	SPI0_POCI	UART0_CTS	TIMG7_C1	A1_6				
	MSPM33C32xx	PB19	UC2_POCI	UC1_0_CTS	TIMG4_3_C1	A1_6				
Pin 17	MSPM0Gx51x	PA21	UART1_CTS	TIMA0_C0	TIMG6_C0	A1_7	VREF-			
	MSPM33C32xx	PA21	UC1_1_CTS	TIMA0_0_C0	TIMG4_2_C0	A1_7	VREF-			
Pin 18	MSPM0Gx51x	PA22	UART1_RTS	TIMA0_C0N	CLK_OUT	TIMG6_C1	A0_7			
	MSPM33C32xx	PA22	UC1_1_RTS	TIMA0_0_C0N	CLK_OUT	TIMG4_2_C1	A0_7			
Pin 19	MSPM0Gx51x	PB20	SPI0_CS2	TIMG12_C0	TIMA0_C1	A0_6				
	MSPM33C32xx	PB20	UC2_CS2	TIMG12_0_C0	TIMA0_0_C1	A0_6				
Pin 20	MSPM0Gx51x	PB21	TIMG8_C0	CAN1_TX	UART6_RX	A1_8				
	MSPM33C32xx	PB21	TIMG8_0_C0	CAN1_TX	UC14_SCL_RX	A1_8				
Pin 21	MSPM0Gx51x	PB22	SPI1_PICO	TIMG8_C1	CAN1_RX	UART6_TX	A1_10			
	MSPM33C32xx	PB22	UC13_0_SDA_TX_PICO	TIMG8_0_C1	CAN1_RX	UC14_SDA_TX	A1_10			
Pin 22	MSPM0Gx51x	PB23	SPI1_SCK	UART6_CTS	A1_11					
	MSPM33C32xx	PB23	UC13_0_SCL_RX_SCK	UC14_CTS	A1_11					
Pin 23	MSPM0Gx51x	PB24	SPI0_CS3	SPI0_CS1	TIMG12_C1	UART6_RTS	A0_5	COMP1_IN1+		
	MSPM33C32xx	PB24	UC2_CS3	UC2_CS3	TIMG12_0_C1	UC14_RTS	A0_5	COMP1_IN1+		
Pin 24	MSPM0Gx51x	PA23	SPI0_CS3	TIMA0_C3	UART3_CTS	TIMG0_C0	SPI1_CS1	COMP1_IN1-	VREF+	
	MSPM33C32xx	PA23	UC2_CS3	TIMA0_0_C3	UC13_0_CTS_CS0	TIMG4_0_C0	UC13_0_CTS_CS0	COMP1_IN1-	VREF+	
Pin 25	MSPM0Gx51x	PA24	SPI0_CS2	TIMA0_C3N	UART3_RTS	TIMG0_C1	A0_3			
	MSPM33C32xx	PA24	UC2_CS2	TIMA0_0_C3N	UC13_0_RTS_POCI	TIMG4_0_C1	A0_3			
Pin 26	MSPM0Gx51x	PA25	UART3_RX	TIMA0_C1N	A0_2					
	MSPM33C32xx	PA25	UC13_0_SCL_RX_SCK	TIMA0_0_C1N	A0_2					

Table 3-4. LQFP64 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 27	MSPM0Gx51x	PB25	UART0_CTS	TIMA_FAL0	TIMA_FAL1	TIMA_FAL2	A0_4			
	MSPM33C32xx	PB25	UC1_0_CTS	TIMA0_0_FAL2	TIMA0_0_FAL2	TIMA0_0_FAL2	A0_4			
Pin 28	MSPM0Gx51x	PB26	UART0_RTS	TIMG6_C0	A1_13	COMP1_IN0+				
	MSPM33C32xx	PB26	UC1_0_RTS	TIMG4_2_C0	A1_13	COMP1_IN0+				
Pin 29	MSPM0Gx51x	PB27	TIMG6_C1	A1_14	COMP1_IN0-					
	MSPM33C32xx	PB27	TIMG4_2_C1	A1_14	COMP1_IN0-					
Pin 30	MSPM0Gx51x	PA26	UART3_TX	SPI1_CS0	TIMA_FAL0	CAN0_TX	TIMG7_C0	A0_1	COMP0_IN0+	
	MSPM33C32xx	PA26	UC13_0_SDA_TX_PICO	UC13_0_CTS_CS0	TIMA0_0_FAL0	CAN0_TX	TIMG4_3_C0	A0_1	COMP0_IN0+	
Pin 31	MSPM0Gx51x	PA27	TIMA_FAL2	RTC_OUT	CAN0_RX	TIMG7_C1	A0_0	COMP0_IN0-		
	MSPM33C32xx	PA27	TIMA0_0_FAL2	RTC_OUT	CAN0_RX	TIMG4_3_C1	A0_0	COMP0_IN0-		
Pin 32	MSPM0Gx51x	VCORE								
	MSPM33C32xx	VCORE								
Pin 33	MSPM0Gx51x	PA0	UART0_TX	I2C0_SDA	TIMA_FAL1	UART5_RX	I2C0_SDA			
	MSPM33C32xx	PA0	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL1	UC13_3_SCL_RX_SCK	UC15_0_SDA			
Pin 34	MSPM0Gx51x	PA1	UART0_RX	I2C0_SCL	TIMA0_C1	TIMG8_IDX	UART5_TX	I2C0_SCL		
	MSPM33C32xx	PA1	UC1_0_SCL_RX	UC1_0_SCL_RX	TIMA0_0_C1	TIMG8_0_IDX	UC13_3_SDA_TX_PICO	UC15_0_SCL		
Pin 35	MSPM0Gx51x	PA28	UART0_TX	I2C0_SDA	TIMA_FAL0	UART5_CTS	I2C0_SDA			
	MSPM33C32xx	PA28	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL0	UC13_3_CTS_CS0	UC15_0_SDA			
Pin 36	MSPM0Gx51x	PA29	I2C1_SCL	UART7_RTS	TIMG6_C0	UART5_RTS	I2C2_SCL			
	MSPM33C32xx	PA29	UC1_1_SCL_RX	UC12_RTS	TIMG4_2_C0	UC13_3_RTS_POCI	UC15_1_SCL			
Pin 37	MSPM0Gx51x	PA30	I2C1_SDA	UART7_CTS	TIMG6_C1	I2C2_SDA				
	MSPM33C32xx	PA30	UC1_1_SDA_TX	UC12_CTS	TIMG4_2_C1	UC15_1_SDA				
Pin 38	MSPM0Gx51x	NRST								
	MSPM33C32xx	NRST								
Pin 40	MSPM0Gx51x	VDD								
	MSPM33C32xx	VDD								
Pin 41	MSPM0Gx51x	VSS								
	MSPM33C32xx	VSS								

Table 3-4. LQFP64 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 42	MSPM0Gx51x	PA2	TIMG8_C1	SPI0_CS0	SPI2_POCI					
	MSPM33C32xx	PA2	TIMG8_0_C1	UC2_CS0	UC13_1_RTS_POCI					
Pin 43	MSPM0Gx51x	PA3	TIMG8_C0	SPI0_CS1	I2C1_SDA	TIMA0_C1	COMP0_OUT	UART1_TX	SPI0_CS3	COMP1_OUT
	MSPM33C32xx	PA3	TIMG8_0_C0	UC2_CS1	UC1_1_SDA_TX	TIMA0_0_C1	COMP1_OUT	UC1_1_SDA_TX	UC2_CS1	COMP1_OUT
Pin 44	MSPM0Gx51x	PA4	SPI0_POCI	I2C1_SCL	TIMA0_C1N	LFCLK_IN	UART1_RX	SPI2_CS0		
	MSPM33C32xx	PA4	UC2_POCI	UC1_1_SCL_RX	TIMA0_0_C1N	LFCLK_IN	UC1_1_SCL_RX	UC13_1_CTS_CS0		
Pin 45	MSPM0Gx51x	PA5	SPI0_PICO	TIMG0_C0	TIMG6_C0					
	MSPM33C32xx	PA5	UC2_PICO	TIMG4_0_C0	TIMG4_2_C0					
Pin 46	MSPM0Gx51x	PA6	SPI0_SCK	TIMG0_C1	HFCLK_IN	TIMG6_C1	TIMA0_C2N			
	MSPM33C32xx	PA6	UC2_SCK	TIMG4_0_C1	HFCLK_IN	TIMG4_2_C1	TIMA0_0_C2N			
Pin 47	MSPM0Gx51x	PB0	UART0_TX							
	MSPM33C32xx	PB0	UC1_0_SDA_TX							
Pin 48	MSPM0Gx51x	PB1	UART0_RX							
	MSPM33C32xx	PB1	UC1_0_SCL_RX							
Pin 49	MSPM0Gx51x	PA7	COMP0_OUT	CLK_OUT	TIMA0_C2	TIMG7_C1				
	MSPM33C32xx	PA7	COMP0_OUT	CLK_OUT	TIMA0_0_C2	TIMG4_3_C1				
Pin 50	MSPM0Gx51x	PB2	I2C1_SCL	TIMA0_C3	TIMG6_C0					
	MSPM33C32xx	PB2	UC1_1_SCL_RX	TIMA0_0_C3	TIMG4_2_C0					
Pin 51	MSPM0Gx51x	PB3	I2C1_SDA	TIMA0_C3N	TIMG6_C1					
	MSPM33C32xx	PB3	UC1_1_SDA_TX	TIMA0_0_C3N	TIMG4_2_C1					
Pin 52	MSPM0Gx51x	PB4	UART1_TX	UART3_CTS	TIMA0_C2	SPI2_PICO				
	MSPM33C32xx	PB4	UC1_1_SDA_TX	UC13_0_CTS_CS0	TIMA0_0_C2	UC13_1_SDA_TX_PICO				
Pin 53	MSPM0Gx51x	PB5	UART1_RX	UART3_RTS	TIMA0_C2N	SPI2_POCI				
	MSPM33C32xx	PB5	UC1_1_SCL_RX	UC13_0_RTS_POCI	TIMA0_0_C2N	UC13_1_RTS_POCI				
Pin 54	MSPM0Gx51x	PA8	UART1_TX	TIMA0_C0	UART0_RTS					
	MSPM33C32xx	PA8	UC1_1_SDA_TX	TIMA0_0_C0	UC1_0_RTS					

Table 3-4. LQFP64 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping							
Pin 55	MSPM0Gx51x	PA9	UART1_RX	SPI0_PICO	TIMA0_C0N	CLK_OUT	RTC_OUT	UART0_CTS	
	MSPM33C32xx	PA9	UC1_1_SCL_RX	UC2_PICO	TIMA0_0_C0N	CLK_OUT	RTC_OUT	UC1_0_CTS	
Pin 56	MSPM0Gx51x	PA10	UART0_TX	SPI0_POCI	I2C0_SDA	TIMA0_C2	TIMG12_C0	SPI2_SCK	I2C0_SDA
	MSPM33C32xx	PA10	UC1_0_SDA_TX	UC2_POCI	UC1_0_SDA_TX	TIMA0_0_C2	TIMG12_0_C0	UC13_1_SCL_RX_SCK	UC15_0_SDA
Pin 57	MSPM0Gx51x	PA11	UART0_RX	SPI0_SCK	I2C0_SCL	TIMA0_C2N	COMP0_OUT	I2C0_SCL	
	MSPM33C32xx	PA11	UC1_0_SCL_RX	UC2_SCK	UC1_0_SCL_RX	TIMA0_0_C2N	COMP0_OUT	UC15_0_SCL	
Pin 58	MSPM0Gx51x	PB6	UART1_TX	UART7_CTS	SPI0_CS1	TIMG6_C0			
	MSPM33C32xx	PB6	UC1_1_SDA_TX	UC12_CTS	UC2_CS1	TIMG4_2_C0			
Pin 59	MSPM0Gx51x	PB7	UART1_RX	SPI1_POCI	UART7_RTS	TIMG9_C0	TIMG6_C1		
	MSPM33C32xx	PB7	UC1_1_SCL_RX	UC13_0_RTS_POCI	UC12_RTS	TIMG8_1_C0	TIMG4_2_C1		
Pin 60	MSPM0Gx51x	PB8	UART1_CTS	SPI1_PICO	I2C2_SCL	COMP0_OUT	TIMG9_IDX	COMP1_OUT	
	MSPM33C32xx	PB8	UC1_1_CTS	UC13_0_SDA_TX_PICO	UC13_0_SCL_RX_SCK	COMP1_OUT	TIMG8_1_IDX	COMP1_OUT	
Pin 61	MSPM0Gx51x	PB9	UART1_RTS	SPI1_SCK	I2C2_SDA	TIMA0_C0N	TIMG9_C1		
	MSPM33C32xx	PB9	UC1_1_RTS	UC13_0_SCL_RX_SCK	UC13_0_SDA_TX_PICO	TIMA0_0_C0N	TIMG8_1_C1		
Pin 62	MSPM0Gx51x	PB10	TIMG0_C0	UART4_TX	TIMG6_C0				
	MSPM33C32xx	PB10	TIMG4_0_C0	UC13_2_SDA_TX_PICO	TIMG4_2_C0				
Pin 63	MSPM0Gx51x	PB11	TIMG0_C1	CLK_OUT	UART4_RX	TIMG6_C1			
	MSPM33C32xx	PB11	TIMG4_0_C1	CLK_OUT	UC13_2_SCL_RX_SCK	TIMG4_2_C1			
Pin 64	MSPM0Gx51x	PB12	UART3_TX	TIMA_FAL1	UART4_CTS				
	MSPM33C32xx	PB12	UC13_0_SDA_TX_PICO	TIMA0_0_FAL1	UC13_2_CTS_CS0				

Table 3-5. VQFN48 common functionality between MSPM0Gx51x and MSPM33C32xx

Pin Number	Device Family	Function Mapping							
Pin 1	MSPM0Gx51x	PA0	UART0_TX	I2C0_SDA	TIMA_FAL1	UART5_RX	I2C0_SDA		
	MSPM33C32xx	PA0	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL1	UC13_3_SCL_RX_SCK	UC15_0_SDA		

Table 3-5. VQFN48 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 2	MSPM0Gx51x	PA1	UART0_RX	I2C0_SCL	TIMA0_C1	TIMG8_IDX	UART5_TX	I2C0_SCL		
	MSPM33C32xx	PA1	UC1_0_SCL_RX	UC1_0_SCL_RX	TIMA0_0_C1	TIMG8_0_IDX	UC13_3_SDA_TX_PICO	UC15_0_SCL		
Pin 3	MSPM0Gx51x	PA28	UART0_TX	I2C0_SDA	TIMA_FAL0	UART5_CTS	I2C0_SDA			
	MSPM33C32xx	PA28	UC1_0_SDA_TX	UC1_0_SDA_TX	TIMA0_0_FAL0	UC13_3_CTS_CS0	UC15_0_SDA			
Pin 4	MSPM0Gx51x	NRST								
	MSPM33C32xx	NRST								
Pin 6	MSPM0Gx51x	VDD								
	MSPM33C32xx	VDD								
Pin 8	MSPM0Gx51x	PA2	TIMG8_C1	SPI0_CS0	SPI2_POCI					
	MSPM33C32xx	PA2	TIMG8_0_C1	UC2_CS0	UC13_1_RTS_POCI					
Pin 9	MSPM0Gx51x	PA3	TIMG8_C0	SPI0_CS1	I2C1_SDA	TIMA0_C1	COMP0_OUT	UART1_TX	SPI0_CS3	COMP1_OUT
	MSPM33C32xx	PA3	TIMG8_0_C0	UC2_CS1	UC1_1_SDA_TX	TIMA0_0_C1	COMP1_OUT	UC1_1_SDA_TX	UC2_CS1	COMP1_OUT
Pin 10	MSPM0Gx51x	PA4	SPI0_POCI	I2C1_SCL	TIMA0_C1N	LFCLK_IN	UART1_RX	SPI2_CS0		
	MSPM33C32xx	PA4	UC2_POCI	UC1_1_SCL_RX	TIMA0_0_C1N	LFCLK_IN	UC1_1_SCL_RX	UC13_1_CTS_CS0		
Pin 11	MSPM0Gx51x	PA5	SPI0_PICO	TIMG0_C0	TIMG6_C0					
	MSPM33C32xx	PA5	UC2_PICO	TIMG4_0_C0	TIMG4_2_C0					
Pin 12	MSPM0Gx51x	PA6	SPI0_SCK	TIMG0_C1	HFCLK_IN	TIMG6_C1	TIMA0_C2N			
	MSPM33C32xx	PA6	UC2_SCK	TIMG4_0_C1	HFCLK_IN	TIMG4_2_C1	TIMA0_0_C2N			
Pin 13	MSPM0Gx51x	PA7	COMP0_OUT	CLK_OUT	TIMA0_C2	TIMG7_C1				
	MSPM33C32xx	PA7	COMP0_OUT	CLK_OUT	TIMA0_0_C2	TIMG4_3_C1				
Pin 14	MSPM0Gx51x	PB2	I2C1_SCL	TIMA0_C3	TIMG6_C0					
	MSPM33C32xx	PB2	UC1_1_SCL_RX	TIMA0_0_C3	TIMG4_2_C0					
Pin 15	MSPM0Gx51x	PB3	I2C1_SDA	TIMA0_C3N	TIMG6_C1					
	MSPM33C32xx	PB3	UC1_1_SDA_TX	TIMA0_0_C3N	TIMG4_2_C1					
Pin 16	MSPM0Gx51x	PA8	UART1_TX	TIMA0_C0	UART0_RTS					
	MSPM33C32xx	PA8	UC1_1_SDA_TX	TIMA0_0_C0	UC1_0_RTS					

Table 3-5. VQFN48 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 17	MSPM0Gx51x	PA9	UART1_RX	SPI0_PICO	TIMA0_C0N	CLK_OUT	RTC_OUT	UART0_CTS		
	MSPM33C32xx	PA9	UC1_1_SCL_RX	UC2_PICO	TIMA0_0_C0N	CLK_OUT	RTC_OUT	UC1_0_CTS		
Pin 18	MSPM0Gx51x	PA10	UART0_TX	SPI0_POCI	I2C0_SDA	TIMA0_C2	TIMG12_C0	SPI2_SCK	I2C0_SDA	
	MSPM33C32xx	PA10	UC1_0_SDA_TX	UC2_POCI	UC1_0_SDA_TX	TIMA0_0_C2	TIMG12_0_C0	UC13_1_SCL_RX_SCK	UC15_0_SDA	
Pin 19	MSPM0Gx51x	PA11	UART0_RX	SPI0_SCK	I2C0_SCL	TIMA0_C2N	COMP0_OUT	I2C0_SCL		
	MSPM33C32xx	PA11	UC1_0_SCL_RX	UC2_SCK	UC1_0_SCL_RX	TIMA0_0_C2N	COMP0_OUT	UC15_0_SCL		
Pin 20	MSPM0Gx51x	PB6	UART1_TX	UART7_CTS	SPI0_CS1	TIMG6_C0				
	MSPM33C32xx	PB6	UC1_1_SDA_TX	UC12_CTS	UC2_CS1	TIMG4_2_C0				
Pin 21	MSPM0Gx51x	PB7	UART1_RX	SPI1_POCI	UART7_RTS	TIMG9_C0	TIMG6_C1			
	MSPM33C32xx	PB7	UC1_1_SCL_RX	UC13_0_RTS_POCI	UC12_RTS	TIMG8_1_C0	TIMG4_2_C1			
Pin 22	MSPM0Gx51x	PB8	UART1_CTS	SPI1_PICO	I2C2_SCL	COMP0_OUT	TIMG9_IDX	COMP1_OUT		
	MSPM33C32xx	PB8	UC1_1_CTS	UC13_0_SDA_TX_PICO	UC13_0_SCL_RX_SCK	COMP1_OUT	TIMG8_1_IDX	COMP1_OUT		
Pin 23	MSPM0Gx51x	PB9	UART1_RTS	SPI1_SCK	I2C2_SDA	TIMA0_C0N	TIMG9_C1			
	MSPM33C32xx	PB9	UC1_1_RTS	UC13_0_SCL_RX_SCK	UC13_0_SDA_TX_PICO	TIMA0_0_C0N	TIMG8_1_C1			
Pin 24	MSPM0Gx51x	PB14	SPI1_POCI	TIMG12_C1	TIMA0_C0	TIMG8_IDX				
	MSPM33C32xx	PB14	UC13_0_RTS_POCI	TIMG12_0_C1	TIMA0_0_C0	TIMG8_0_IDX				
Pin 25	MSPM0Gx51x	PB15	UART7_TX	TIMG8_C0	TIMG7_C0					
	MSPM33C32xx	PB15	UC12_TX	TIMG8_0_C0	TIMG4_3_C0					
Pin 26	MSPM0Gx51x	PB16	UART7_RX	TIMG8_C1	TIMG7_C1					
	MSPM33C32xx	PB16	UC12_RX	TIMG8_0_C1	TIMG4_3_C1					
Pin 27	MSPM0Gx51x	PA12	UART3_CTS	FCC_IN	TIMG0_C0	SPI1_CS1	CAN0_TX	A0_8		
	MSPM33C32xx	PA12	UC13_0_CTS_CS0	FCC_IN	TIMG4_0_C0	UC13_0_CTS_CS0	CAN0_TX	A0_8		
Pin 28	MSPM0Gx51x	PA13	UART3_RTS	UART3_RX	TIMG0_C1	UART7_TX	CAN0_RX	A0_9	COMP0_IN2-	
	MSPM33C32xx	PA13	UC13_0_RTS_POCI	UC13_0_SCL_RX_SCK	TIMG4_0_C1	UC12_TX	CAN0_RX	A0_9	COMP0_IN2-	

Table 3-5. VQFN48 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 29	MSPM0Gx51x	PA14	UART0_CTS	UART3_TX	CLK_OUT	UART7_RX	A0_12	COMP0_IN2+		
	MSPM33C32xx	PA14	UC1_0_CTS	UC13_0_SDA_TX_PICO	CLK_OUT	UC12_RX	A0_12	COMP0_IN2+		
Pin 30	MSPM0Gx51x	PA15	UART0_RTS	I2C1_SCL	TIMA0_C2	TIMG8_IDX	A1_0	COMP0_IN3+	COMP1_IN3+	I2C2_SCL
	MSPM33C32xx	PA15	UC1_0_RTS	UC1_1_SCL_RX	TIMA0_0_C2	TIMG8_0_IDX	A1_0	COMP0_IN3+	COMP1_IN3+	UC15_1_SCL
Pin 32	MSPM0Gx51x	PA17	UART1_TX	SPI1_SCK	TIMA0_C3	TIMG7_C0	A1_2	COMP0_IN1-		
	MSPM33C32xx	PA17	UC1_1_SDA_TX	UC13_0_SCL_RX_SCK	TIMA0_0_C3	TIMG4_3_C0	A1_2	COMP0_IN1-		
Pin 33	MSPM0Gx51x	PA18	UART1_RX	SPI1_PICO	TIMA0_C3N	A1_3	COMP0_IN1+			
	MSPM33C32xx	PA18	UC1_1_SCL_RX	UC13_0_SDA_TX_PICO	TIMA0_0_C3N	A1_3	COMP0_IN1+			
Pin 34	MSPM0Gx51x	PA19	SWDIO	A0_13						
	MSPM33C32xx	PA19	SWDIO	A0_15						
Pin 35	MSPM0Gx51x	PA20	SWCLK	A0_14						
	MSPM33C32xx	PA20	SWCLK	A0_16						
Pin 36	MSPM0Gx51x	PB17	SPI0_PICO	TIMA0_C2	A1_4	COMP1_IN2-				
	MSPM33C32xx	PB17	UC2_PICO	TIMA0_0_C2	A1_4	COMP1_IN2-				
Pin 37	MSPM0Gx51x	PB18	SPI0_SCK	TIMA0_C2N	A1_5	COMP1_IN2+				
	MSPM33C32xx	PB18	UC2_SCK	TIMA0_0_C2N	A1_5	COMP1_IN2+				
Pin 38	MSPM0Gx51x	PB19	SPI0_POCI	UART0_CTS	TIMG7_C1	A1_6				
	MSPM33C32xx	PB19	UC2_POCI	UC1_0_CTS	TIMG4_3_C1	A1_6				
Pin 39	MSPM0Gx51x	PA21	UART1_CTS	TIMA0_C0	TIMG6_C0	A1_7	VREF-			
	MSPM33C32xx	PA21	UC1_1_CTS	TIMA0_0_C0	TIMG4_2_C0	A1_7	VREF-			
Pin 40	MSPM0Gx51x	PA22	UART1_RTS	TIMA0_C0N	CLK_OUT	TIMG6_C1	A0_7			
	MSPM33C32xx	PA22	UC1_1_RTS	TIMA0_0_C0N	CLK_OUT	TIMG4_2_C1	A0_7			
Pin 41	MSPM0Gx51x	PB20	SPI0_CS2	TIMG12_C0	TIMA0_C1	A0_6				
	MSPM33C32xx	PB20	UC2_CS2	TIMG12_0_C0	TIMA0_0_C1	A0_6				
Pin 42	MSPM0Gx51x	PB24	SPI0_CS3	SPI0_CS1	TIMG12_C1	UART6_RTS	A0_5	COMP1_IN1+		
	MSPM33C32xx	PB24	UC2_CS3	UC2_CS3	TIMG12_0_C1	UC14_RTS	A0_5	COMP1_IN1+		
Pin 43	MSPM0Gx51x	PA23	SPI0_CS3	TIMA0_C3	UART3_CTS	TIMG0_C0	SPI1_CS1	COMP1_IN1-	VREF+	
	MSPM33C32xx	PA23	UC2_CS3	TIMA0_0_C3	UC13_0_CTS_CS0	TIMG4_0_C0	UC13_0_CTS_CS0	COMP1_IN1-	VREF+	

Table 3-5. VQFN48 common functionality between MSPM0Gx51x and MSPM33C32xx (continued)

Pin Number	Device Family	Function Mapping								
Pin 44	MSPM0Gx51x	PA24	SPI0_CS2	TIMA0_C3N	UART3_RTS	TIMG0_C1	A0_3			
	MSPM33C32xx	PA24	UC2_CS2	TIMA0_0_C3N	UC13_0_RTS_POCI	TIMG4_0_C1	A0_3			
Pin 45	MSPM0Gx51x	PA25	UART3_RX	TIMA0_C1N	A0_2					
	MSPM33C32xx	PA25	UC13_0_SCL_RX_SCK	TIMA0_0_C1N	A0_2					
Pin 46	MSPM0Gx51x	PA26	UART3_TX	SPI1_CS0	TIMA_FAL0	CAN0_TX	TIMG7_C0	A0_1	COMP0_IN0+	
	MSPM33C32xx	PA26	UC13_0_SDA_TX_PICO	UC13_0_CTS_CS0	TIMA0_0_FAL0	CAN0_TX	TIMG4_3_C0	A0_1	COMP0_IN0+	
Pin 47	MSPM0Gx51x	PA27	TIMA_FAL2	RTC_OUT	CAN0_RX	TIMG7_C1	A0_0	COMP0_IN0-		
	MSPM33C32xx	PA27	TIMA0_0_FAL2	RTC_OUT	CAN0_RX	TIMG4_3_C1	A0_0	COMP0_IN0-		
Pin 48	MSPM0Gx51x	VCORE								
	MSPM33C32xx	VCORE								

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