Errata

AM13E230x Silicon Revisions A, 0 Errata

Abstract

This document describes the known exceptions to the functional specifications (advisories). This document may also contain usage notes. Usage notes describe situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness.

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1 Usage Notes and Advisories Matrices

Table 1-1 lists all advisories, modules affected, and the applicable silicon revisions.

Table 1-1. Advisories Matrix

MODULE IDENTIFIER	DESCRIPTION	SILICON REVISIONS AFFECTED	
		0	A
ADC_ERR_01	Degraded performance with ADCCLK fractional divider	YES	YES
AES_ERR_01	AES saved context ready interrupt not generating as expected	YES	YES
DEBUGSS_ERR_01	Debug disable in NONMAIN can be re-enabled using the password	YES	YES
DMA_ERR_01	DMA/CPU arbitration issue for ADCx, ADCxRESULT, and SYSCTL registers	YES	YES
KEYSTORE_ERR_01	STATUS.STAT value can be 0 or 1 without key access	YES	YES
LFOSC_ERR_01	Synchronous wakeup sources for STANDBY0 mode are not functioning as expected	YES	NO
MTB_ERR_01	MTB_BASE register value gets read improperly	YES	YES
PGA_ERR_01	ADC Assisted chopping function does not work for ADCB and ADCC	YES	YES
RST_ERR_01	NRST pulse <1ms can result in a device hang	YES	YES
SYSPLL_ERR_01	SYSPLL frequency may not lock to correct frequency when enabled	YES	YES
TIMER_ERR_01	TIMER re-enable may be missed if done close to zero event	YES	YES
TIMER_ERR_02	Writing 0 to CLKEN bit does not disable counter	YES	YES
TIMER_ERR_03	Initial repeat counter has 1 less period than next repeats module	YES	YES
UNICOMMI2C_ERR_01	I2C controller BUSY status polling issue	YES	YES
UNICOMMI2C_ERR_02	RXDONE interrupt is triggered twice when I2C controller ACKOEN bit is enabled	YES	YES
UNICOMMSPI_ERR_01	Controller Side Busy status delayed due to clock domain crossing	YES	YES
UNICOMMSPI_ERR_02	Data package size setting(DSS) must be the same on the controller and periperhal.	YES	YES
UNICOMMUART_ERR_01	IDLE period detection issue with glitch in IDLELINE mode	YES	YES
UNICOMMUART_ERR_02	Data will be missed with glitches during break field and/or sync field in LIN Mode	YES	YES
UNICOMMUART_ERR_03	LIN Mode Capture Registers CLKDIV Restriction	YES	YES
UNICOMMUART_ERR_04	CTL0.TXE bit setting to 0 in middle of frame makes current transmission error	YES	YES
UNICOMMUART_ERR_05	CTS interrupt gets toggled on both falling and rising edges of CTS line	YES	YES
UNICOMMUART_ERR_06	LCRH.SENDIDLE access missed in between fclk and new IDLELINE frame not produced	YES	YES
XTAL_ERR_01	External crystal interference from negative voltage on other analog input pins	YES	NO

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2 Nomenclature, Package Symbolization, and Revision Identification

2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *your device*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, *your device*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

2.2 Devices Supported

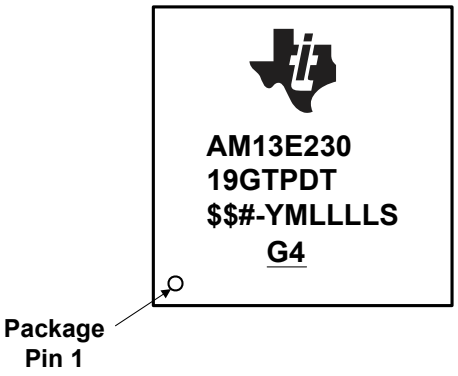
This document supports the following devices:

- AM13E23019
- AM13E23018
- AM13E23017

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2.3 Package Symbolization and Revision Identification

Figure 2-1, Figure 2-2, Figure 2-3, Figure 2-4, Figure 2-5 and Figure 2-6 and *Table y* describe package symbolization and device revision codes.



19GTPDT or 19GT2PDT

BLANK = 250MHz, 2 = 200 MHz

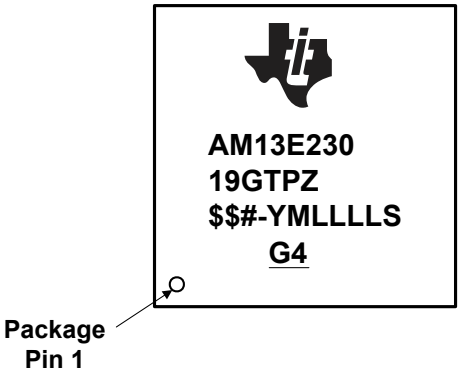
G = STM32G4 Pin Compatible, H = STM32H5 Pin Compatible

YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 2-1. Package Symbolization for PDT package



19GTPZ or 19GT2PZ

BLANK = 250MHz, 2 = 200 MHz

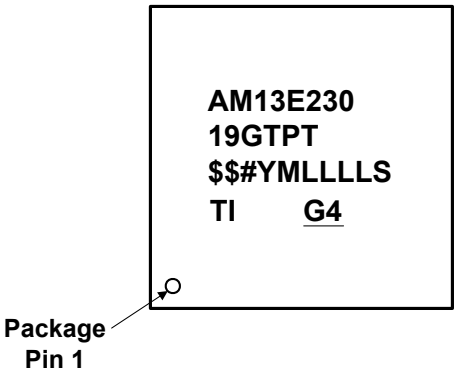
G = STM32G4 Pin Compatible, H = STM32H5 Pin Compatible

YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 2-2. Package Symbolization for PZ package



19GTPT or 19GT2PT

BLANK = 250MHz, 2 = 200 MHz

G = STM32G4 Pin Compatible, H = STM32H5 Pin Compatible

YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
 # = Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 2-3. Package Symbolization for PT package

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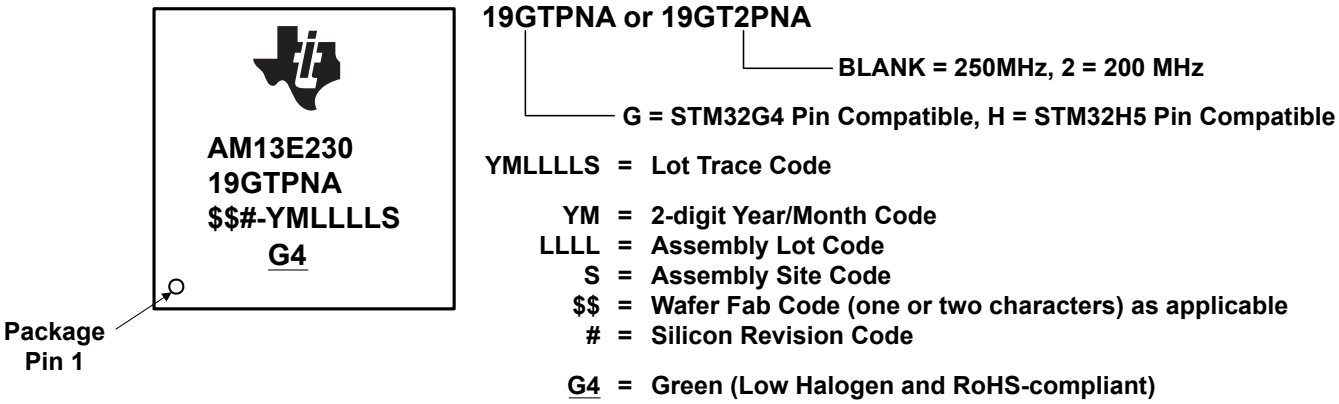


Figure 2-4. Package Symbolization for PNA package

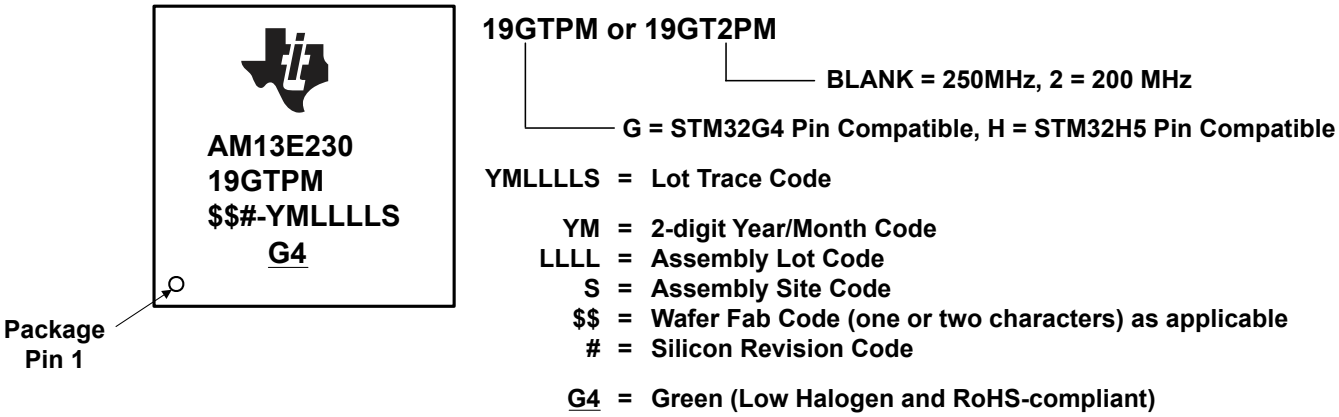


Figure 2-5. Package Symbolization for PM package

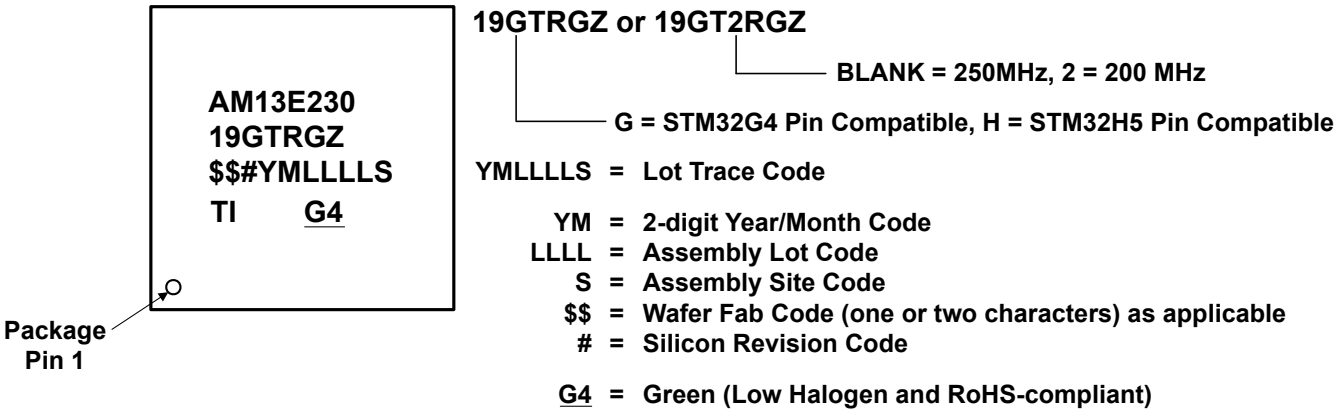


Figure 2-6. Package Symbolization for RGZ package

Table 2-1. Revision Identification

DEVICE REVISION CODE	SILICON REVISION	USERID.MAJORREVAddress: 0x60111008	COMMENTS
Blank	0	0	This silicon revision is available as TMX.
A	A	1	This silicon is available as TMS.

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3 Silicon Advisories

The following advisories are known design exceptions to functional specifications. Advisories are listed in alphabetical order.

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Advisory - ADC_ERR_01	***Degraded ADC performance with ADCCLK fractional divider***
Revisions Affected	0, A
Details	Using fractional SYSCLK-to-ADCCLK dividers (controlled by the ADCCTL2.PRESCALE field) has been shown to cause degradation in ADC performance on this device. See
Workarounds	Use even PRESCALE clock divider values. Even PRESCALE values result in integer clock dividers which do not impact the ADC performance.

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Advisory - AES_ERR_01	***AES saved context ready interrupt does not function as expected***
Revisions Affected	0,A
Details	Saved Context Ready interrupt is not generated correctly. The interrupt is generated if an access (read or write) is made to any AES register.
Workarounds	Use polling based mechanism to check the status bit for Saved Context Ready in CTRL register instead of interrupt.

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Advisory - DEBUGSS_ERR_01

Debug disable in NONMAIN can be re-enabled using the password

Revisions Affected

0, A

Details

If debug is disabled in NONMAIN configuration (DEBUGACCESS = 0x5566), the device can still be accessed using the password that is programmed (default password if not explicitly programmed).

Workarounds

Use one of the below options:

1. Set the DEBUGACCESS to Debug Enabled with Password option (DEBUGACCESS = 0xCCDD) and provide a unique password in the PWDDEBUGLOCK field. For higher security, it is recommended to have device-unique passwords that are cryptographically random. This would allow debug access with the right 128-bit password but can still allow some debug commands and access to the CFG-AP and SEC-AP.
2. Disable the physical SW Debug Port entirely by disabling SWDP_MODE. This fully prevents any debug access or requests to the device, but may affect Failure Analysis and return flows.

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Advisory - DMA_ERR_01 ***DMA/CPU arbitration issue for ADCx, ADCxRESULT, and SYSCTL registers***

Revisions Affected

0, A

Details

If access to any of the listed register spaces occurs on the same cycle by the CPU and DMA, the current bus owner misses the access. Note for ADC and ADCRESULT this only applies if the access is to the same ADC instance. For example if both CPU and DMA access ADCA, then this erratum applies. If CPU is accessing ADCA and DMA is accessing ADCB, then no interaction exists.

Workarounds

Avoid conflicts either in peripheral assignment, or by using the CPU to check the status of the DMA before performing accesses to the common peripheral region.

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Advisory - KEYSTORE_ERR_01 ***STATUS.STAT value can be 0 or 1 without key access***

Revisions Affected

0, A

Details

STATUS.STAT has a reset value of 1 and turns to 0 under these conditions:

1. After reset, debugger access via the register window returns 0x00.
2. After reset, the first CPU read returns 0x01, while subsequent CPU reads return 0x00.
3. After reset, first reading any other KEYSTORE register and then reading STATUS.STAT return 0x00.

Workarounds

STATUS.STAT=0x0 means "No Error" . For checking if a slot is valid or not (Whether key is present), check STATUS.VALID.

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Advisory - LFOSC_ERR_01	***Synchronous wakeup sources for STANDBY0 mode are not functioning as expected***
Revisions Affected	0
Details	The LFOSC does not turn on when the device enters STANDBY mode (both STANDBY0 and STANDBY1). The LFCLK is not available in the system. Effects of LFCLK absence in STANDBY0/1 Power Modes: • Gates all PD0 peripherals in STANDBY0 modes. • The Windowed Watchdog Timer (WWDT) halts and cannot provide an interrupt/NMI to WAKE the device from STANDBY0 modes. • Debug WAKE is also non-functional in STANDBY0/1 modes. NRST cannot assert a POR or BOOTRST in STANDBY0/1 modes. • PMU does not enter into sample and hold mode, contributing to higher currents in both STANDBY0/1 modes. GPIO (asynchronous)/BOR threshold based WAKE is functional in STANDBY0/1 modes.
Workarounds	Either use GPIO or BOR threshold-based WAKE sources in STANDBY0/1 modes or use STOP mode, which can enable all synchronous/asynchronous based wakeup sources.

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Advisory - MTB_ERR_01 *MTB_BASE register value gets read improperly*

Revisions Affected

0, A

Details

When Reading the MTB_BASE register the MTB_SRAM base location will be right shifted by a bit. For example, if the MTB_SRAM shows 0x80806000 the actual MTB_SRAM base location is 0x40403000.

Workarounds

When reading the MTB_BASE register to find the MTB_SRAM base location right shift the read value by one bit. Please use the code below to workaround the issue: `uint32_t mtb_base = (*(uint32_t *)(0xE004300C) >> 1);`. This workaround is already implemented for both TI and IAR toolchains.

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Advisory - PGA_ERR_01 *ADC assisted chopping function does not work for ADCB and ADCC*

Revisions Affected

0, A

Details

PGA has chopping logic that allows internal swapping of the input to the PGA for offset correction. This is controlled via the MUXSEL register, bits 14-13 PGA_CHOP. Following are options for this register:

- 00 - Chopping Disabled
- 10 - Chopping Enabled, ADC SOC will automatically change the state of the CHOP_EXTCTRL bit in PGACTL register
- 11 - Chopping Enabled, CHOP_EXTCTRL bit is manually controlled via device SW.

For ADCB and ADCC the option "10b" is not functional.

Workarounds

Either do not use the chopping feature (00b), or use external chopping control(11b) for ADCB or ADCC.

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Advisory - RST_ERR_01	***NRST pulse <1ms can result in a device hang***
Revisions Affected	0, A
Details	Pulses on NRST for less than 1ms can result in the device being held in reset state until the next power cycle.
Workarounds	Confirm external circuitry on NRST holds the pin active for 1ms or greater when issuing a device reset. This does not apply to a cold boot/power up initiated reset, only for resets initiated by driving the NRST pin low.

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Advisory - SYSPLL_ERR_01 *SYSPLL frequency may not lock to correct frequency when enabled*

Revisions Affected

0, A

Details

When setting the SYSPLLEN bit to 1 in SYSCTL HSCLKEN register, the SYSPLL will run the phase locked loop search. The search can potentially fail where the frequency will not be set to the correct value, instead the resultant frequency will be drastically different than the configured frequency.

Workarounds

Frequency Verification Process

Monitor the SYSPLL frequency output using the Frequency Clock Counter (FCC) whenever the SYSPLLEN bit is set to 1. Once the correct frequency is established, it will remain stable until the SYSPLL is disabled and re-enabled (SYSPLLEN bit toggled from 0 to 1). If an incorrect frequency is detected, disable and re-enable the SYSPLL to perform another verification

Workaround 1: FCC Ratio Check(example exists in AM13E230x SDK)

Use LFCLK as the FCC trigger source to count both SYSPLL output and input clock frequency. Execute the FCC and verify the measured ratio of the FCC check value between output and input clock to the expected ratio.

Example calculation:

- SYSPLL = 200MHz ; HFCLK = 8MHz ; LFCLK = 32.768kHz
- Expect clock ratio = 200MHz/8MHz = 25.0
- Measured FCC count (SYSPLL) = 200,000,000/32,768 = 6103
- Measured FCC count (HFCLK) = 8,000,000/32,768 =244
- Measured clock ratio = 6103/244 = 25.012

FCC Ratio Tolerance: The FCC ratio method eliminates combined clock accuracy errors and depends only on FCC uncertainty (2 counted clock cycles) and calculation rounding error. This allows for much tighter tolerance ranges compared to FCC count check method, for example +/- 0.3%.

Timing considerations:

- Clock synchronization time: 5-6 LFCLK cycles
- FCC trigger time: 1-32 LFCLK cycles (user-configurable)
- Total time per complete FCC ratio check: 2*(sync time + trigger time)

FCC Ratio Check Flow:

1. Configure FCC for SYSPLL output clock (SYSPLL0 or SYSPLL2X)
2. Start FCC and wait for FCC done (Add Timeout Protection, refer to FCC Count Check)
3. Read FCC check count back
4. Configure FCC for SYSPLL input clock (SYSOSC or HFCLK)
5. Start FCC and wait for FCC done (Add Timeout Protection, refer to FCC Count Check)
6. Read FCC check count back
7. Calculate the FCC check ratio and compared to the expected ratio range
8. If the FCC ratio falls outside the expected range, disable and re-enable the SYSPLL (set SYSPLLEN to 0, then 1) and repeat the FCC ratio verification.

Workaround 2: FCC Count Check

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Advisory - SYSPLL_ERR_01
(continued)

SYSPLL frequency may not lock to correct frequency when enabled

Use LFCLK as the FCC trigger source to count the SYSPLL output clock frequency. Execute the FCC and verify the measured value against the configured SYSPLL frequency using LFCLK as reference.

Example calculation:

- SYSPLLCLK0 = 200MHz
- LFCLK = 32.768kHz
- Measured FCC Count = 200,000,000/32,768 = 6104

FCC Count Tolerance: The real FCC count will vary depending on the combined clock accuracies (SYSPLLCLK0 and LFCLK). Recommend to add +/- 5~10% to allowed FCC check range.

- FCC count upper limit = 6104*1.05 = 6409
- FCC count lower limit = 6104*0.95 = 5798

Timing considerations:

- Clock synchronization time: 5-6 LFCLK cycles
- FCC trigger time: 1-32 LFCLK cycles (user-configurable)

Register Configuration:

- FCC Settings: SYSCTL.GENCLKCFG.FCCTRIGSRC = 1;
- SYSCTL.GENCLKCFG.FCCLVLTRIG = 0;
- SYSCTL.GENCLKCFG.FCCTRIGCNT = 0
- Start FCC: SYSCTL.FCCCMD = 0x0E000001U
- Check FCC Done Status: SYSCTL.CLKSTATUS.FCCDONE
- Read FCC Count: SYSCTL.FCC

Timeout Protection:

Implement a software-based timeout during FCC Done status monitoring to prevent longer wait time under the condition the unlocked SYSPLL frequency is less than FCC trigger clock frequency (LFCLK).

```
fccTimeOutCounter = 0;
while (DL_SYSCTL_isFCCDone() == 0) {
delay_cycles(977); /* 1x LFCLK cycle = 32MHz/32.768kHz */
fccTimeOutCounter++;
if(fccTimeOutCounter > 65) break;
/* Timeout set to approximately 2ms (user-customizable) */
}
```

FCC Check Restart: If the FCC measurement falls outside the expected range, disable and re-enable the SYSPLL (set SYSPLLEN to 0, then 1) and repeat the FCC verification.

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Advisory - TIMER_ERR_01 ***TIMER re-enable may be missed if done close to zero event***

Revisions Affected

0, A

Details

When using a TIMER in one shot mode, TIMER re-enable may be missed if performed close to the zero event. The HW update to the timer enable bit will take a single functional clock cycle. For example, if the timer's clock source is 32.768kHz and clock divider of 3, then it will take ~100us to have the enable bit set to 0 properly.

Workarounds

Wait 1 functional clock cycle before re-enabling the timer OR the timer can be disabled first before re-enabling. Disable the counter with CTRCTL.EN = 0, then re-enable with CTRCTL.EN = 1

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Advisory - TIMER_ERR_02	***Writing 0 to CLKEN bit does not disable counter***
Revisions Affected	0, A
Details	Writing 0 to the Counter Clock Control Register(CCLKCTL) Clock Enable bit(CLKEN) does not stop the timer.
Workarounds	Stop the timer by writing 0 to the Counter Control(CTRCTL) Enable(EN) bit

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Advisory - TIMER_ERR_03 ***Initial repeat counter has 1 less period than next repeats module***

Revisions Affected

0, A

Details

When using the timer repeat counter mode, the first repeat will have 1 less count than the subsequent repeats because the following repeat counters will include the transition between 0 and the load value. For example if the TIMx.RCLD = 0x3 then 3 observable zero events would appear on the first repeat counter and 4 observable zero events would appear on the following repeat counter sequences.

Workarounds

Set the initial RCLD value to 1 more than the expected RCLD, then in the ISR for the Repeat Counter Zero Event (REPC), set the RCLD to the intended RCLD value. For example, if intending to have 4 repeats, set the initial RCLD value to RCLD = 0x5, then in the timer ISR for the REPC interrupt, set RCLD = 0x4. Now all timer repeats will have the same number of zero/load events.

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Advisory - UNICOMMI2CC_ERR_01 ***I2C Controller BUSY Status Polling Issue***

Revisions Affected

0,A

Details

When initiating an I2C controller transfer by setting the BUSRTRUN/FRAME_START bit, the BUSY status flag requires approximately 2-3 I2C functional clock cycles to assert. If polling the BUSY bit immediately after setting BUSRTRUN/FRAME_START, the status might be checked by the application before it's properly set. This issue is more pronounced with higher CLKDIV values (resulting in slower I2C functional clock) or under higher compiler optimization levels.

Workarounds

Add a software delay before polling BUSY status. The recommended delay should be: Software delay = 3 x I2C functional clock = 3 x clock_divider x (CPU_CLK / selected clock source frequency) For example, with a clock_divider of 2, a clock source of 4 MHz(MFCLK), and CPU_CLK of 80 MHz: Software delay = 3 x 2 x (80 MHz / 4 MHz)= 120 CPU cycles

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Advisory - UNICOMMI2CC_ERR_02 ***RXDONE interrupt is triggered twice when I2C controller ACKOEN bit is enabled***

Revisions Affected

0, A

Details

When I2C controller CTR.ACKONE bit is enable, software controls the sending of ACK/NACK by writing CTR.ACK bit 0 or 1. This can be done in the RXDONE interrupt before the stop condition. After writing the CTR.ACK bit, there will be valid ACK/NACK signal on I2C bus, and an additional RXDONE interrupt will be triggered in the subsequent I2C stop status.

Workarounds

Disable the RXDONE interrupt before writing CTR.ACK bit, and manually enable it before next transmission.

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Advisory - UNICOMMSPI_ERR_01

Controller side busy status delayed due to clock domain crossing

Revisions Affected

0, A

Details

The SPI busy status bit does not accurately reflect the TXFIFO data state in real time. Because the busy flag is set within the SPI's own clock domain, there is propagation delay between loading data into the TXFIFO and the busy bit transitioning high. This delay becomes significant when the SPI source clock (CLKSEL) is slow for example, when using LFCLK or when CLKDIV is set to a value greater than /1. In these cases, the delay is long enough that the busy bit still reads low for a period after data has been loaded into the TXFIFO, even though a transfer is about to begin.

Workarounds

Software can introduce a delay equal to or greater than the clock domain ratio, or can check for TXFIFO empty STATUS bit for equivalent functionality.

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Advisory - UNICOMMSPI_ER R_02	***Data package size setting(DSS) must be the same on the controller and peripheral.***
Revisions Affected	0, A
Details	If data sent with different DSS settings on the controller and peripheral an error occurs inside the RXFIFO on subsequent SCLK pulses.
Workarounds	Different DSS settings between controller and peripheral are not supported. Confirm that the DSS on controller side and peripheral side are the same.

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Advisory - UNICOMMUART_ERR_01	***IDLE period detection issue with glitch in IDLELINE mode***
Revisions Affected	0, A
Details	A glitch during the idle period can corrupt the receiver's idle detection, causing the Rx side to drop the subsequent address byte. This failure mode is timing-dependent: only glitches inserted at a specific time relative to the idle period trigger the issue. Not every glitch within the idle period causes corruption.
Workarounds	External glitch filter/low pass filter. No internal mitigation exists to filter out high frequency noise.

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Advisory - UNICOMMUART_ERR_02	***Data will be missed with glitches during break field and/or sync field in LIN Mode***
Revisions Affected	0, A
Details	Break Field Scenario (High-Pulse Glitch): During the Break Field period, a negative edge will reset the counter to zero, cause break field detection failure and result in data loss. Sync Field Scenario: A glitch during Sync Field will trigger false LINC0/LINC1 interrupts, reset the counter on Rx-line negative edges, cause sync field validation failure and result in data loss.
Workarounds	External glitch filter/low pass filter. No internal mitigation exists to filter out high frequency noise.

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Advisory - UNICOMMUART_ERR_03 ***LIN mode capture registers CLKDIV restriction***

Revisions Affected

0, A

Details

When CLKDIV value is other than '0', writing into LINC0 or LINC1 does not have any effect.

Workarounds

To properly configure LIN registers:

1. Set CLKDIV to '0'
2. Update the LINC0 or LINC1 register configurations with desired values
3. Restore CLKDIV to the desired clock divider for UNICOMM UART module

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Advisory - UNICOMMUART_ERR_04 ***CTL0.TXE bit setting to 0 in middle of frame makes current transmission error***

Revisions Affected

0, A

Details

Start transmitting packet and then in middle of transfer, set the CTL0.TXE bit to 0, the current packet won't complete and the TX line will be pulled low, which shows the busy behavior as BUSY. The TX line will be released only when CTL0.TXE = 1, and till then BUSY remains 1.

Workarounds

User must poll for BUSY STATUS to go low and CTL0.TXE = 0, so as to avoid this issue.

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Advisory - UNICOMMUART_ERR_05	***CTS interrupt gets toggled on both falling and rising edges of CTS line***
Revisions Affected	0, A
Details	CTS interrupt gets toggled on both RISE edge as well as FALL edge of CTS line. Ideally, it should just toggle on the FALL edge of CTS line.
Workarounds	Instead of RIS bit, user can monitor STAT.CTS bit's toggle to 1, since this toggling of STAT.CTS = 1 indicates that falling of CTS line has been encountered.

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Advisory - UNICOMMUART_ERR_06	*LCRH.SENDIDLE access missed in between fclk and new IDLELINE frame not produced*
Revisions Affected	0, A
Details	If LCRH.SENDIDLE is toggled from 0 to 1 and then back from 1 to 0, or toggle from 1 to 0 and then back from 0 to 1 in between two fclk edges, the toggle will be missed and no new IDLELINE frame is sent.
Workarounds	After toggling LCRH.SENDIDLE, wait at least one fclk period before the next toggle.

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Advisory - XTAL_ERR_01	***External crystal interference from negative voltage on other analog input pins***
Revisions Affected	0
Details	External crystal oscillator fails to start or flatlines if negative voltage <-1V applied to any analog input pin.
Workarounds	Avoid applying out of specification negative voltage to any analog input pin. External diode clamps can be used for mitigation.

4 Trademarks

All trademarks are the property of their respective owners.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 30, 2026 to November 13, 2026 (from Revision * (March 2026) to Revision A (November 2026)) **Page**

- Update of errata for RTM. All errata except LFOSC_ERR_01 are new. LFOSC_ERR_01 Added additional column to show revisions effected....2
- New Erratum....7
- New Erratum....8
- New Erratum....9
- New Erratum....10
- Renamed Advisory-001 to Advisory-LFOSC-01....12
- New Erratum....13
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