Errata

AWRL6888 Device Silicon Errata Silicon Revisions ES1.0

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1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (AWRL6888)

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / mmWave sensor devices. Each of the Radar devices has one of the two prefixes: XALx or AWRLx (for example: **AWRL6888DBGAPD**). These prefixes represent evolutionary stages of product development from engineering prototypes (XAL) through fully qualified production devices (AWRL).

Device development evolutionary flow:

XAL —	Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
AWRL —	Production version of the silicon die that is fully qualified.

XAL devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

Figure 3-1 shows an example of the AWRL6888 Radar Device's package symbolization.

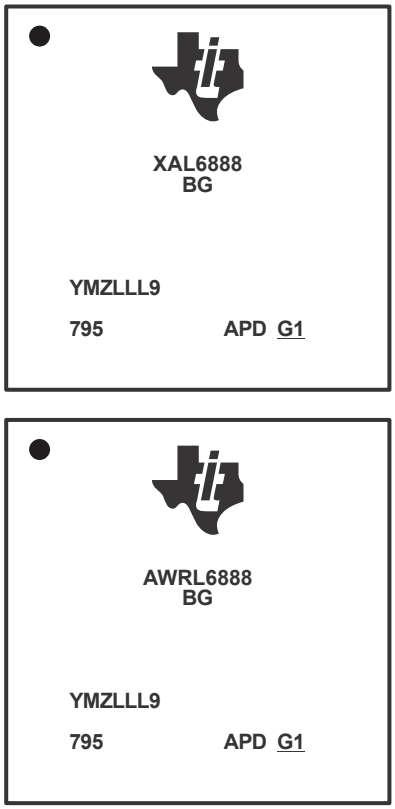

Figure 3-1. Example of Device Part Markings

This identifying number contains the following information:

- **Line 1:** TI Logo
- **Line 1:** Device Number
- **Line 2:** Safety Level and Security Grade
  - Q = Non-Functional Safety
  - B = ASIL-B capable
  - G = General
  - S = Secure
- **Line 3:** Lot Trace Code
  - YM = Year/Month Code
  - Z- Assembly Site Code
  - LLL = Assembly Lot
  - 9= Primary Site Code
- **Line 4:**
  - 795 = Device Identifier
  - APD = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Advisory to Silicon Variant / Revision Map

Table 4-1. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	AWRL6888
		ES1.0
Analog / Millimeter Wave		
ANA #51	Continuous Wave Streaming CZ mode: Sudden jump in RX output codes every 20.97152 msec	x
ANA #57	SNR degradation at 60GHz in the presence of strong near range reflector	x
ANA #65	Emission at 1.6GHz with default APLL frequency	x
Digital Subsystem		
DIG #17	HWA CFAR CA engine is not working if dynamic clock gating is enabled	x
DIG #18	Warm-Reset assertion during Spread-Spectrum enabled in ADPLL leads to a failure of phase-lock of ADPLL in the next lock attempt, which makes the device-hang	x

5 Known Design Exceptions to Functional Specifications

ANA #51 *Continuous Wave Streaming CZ mode: Sudden jump in RX output codes every 20.97152 msec*

Revision(s) Affected

AWRL6888ES1.0

Details

On Continuous Wave Streaming CZ mode, the Rx data shows a sudden jump in output codes every 20.97152 milliseconds.

This is not an issue in the Radar Functional mode when chirps are used. However, this issue will be seen when testing Rx chain in lab using continuous stream mode.

Workaround

In order to use Continuous stream (CW) mode for testing, it is recommended to start data capturing from the first sample itself to make sure the glitch occurs at deterministic samples. Please follow the below sequence to achieve this:

- Configure the LVDS (Low Voltage Differential Signaling)
- Arm the DCA1000 (Data capture card)
- Enable the continuous stream mode.

The glitch will not be seen with this sequence. For example, if the user analyzes first 20ms of data or between 21 and 41ms.

ANA #57 *SNR degradation at 60GHz in the presence of strong near range reflector*

Revision(s) Affected

AWRL6888ES1.0

Details

There is a non-linearity of the synthesizer when crossing 60GHz which causes increased noise floor at RX output in the presence of a strong near range reflector.

Workaround

Chirps with large RF bandwidth (> 1.5GHz) have negligible noise floor impact. For lower bandwidth chirps, avoid 60GHz.

ANA #65	***Emission at 1.6GHz with default APLL frequency***
Revisions Affected	AWRL6888ES1.0
Details	Configurations using frame duty cycle > 25% can have reduced margin for CISPR25 class5 emission compliance at 1.6GHz when using default APLL frequency.
Workaround	The APLL frequency shift option should be used for >25% frame duty cycle. APLL frequency shift can be enabled by setting apllFreqShiftEn configuration value to 1. Refer mmWave demo tuning guide for more details.

DIG #17	***HWA CFAR CA engine is not working if dynamic clock gating is enabled***
Revision(s) Affected	AWRL6888ES1.0
Details	Dynamic clock gating feature is added in IP for power savings. Idea is to enable clock to the FFT/CFAR-CA/CFAR-OS engine only when the respective engine is needed to be active based on the mode of operation. However, when CFAR CA engine is enabled and dynamic clock gating is set, the clock to one of the logic in the engine gets gated. Due to this, the data transfer to the logic internal to the CFAR-CA engine gets hampered. Hence, we do not get any valid data in the output of the CFAR CA engine.
Workaround	Disable the dynamic clock gating feature when CFAR CA mode of operation is enabled.

DIG #18 ***Warm-Reset assertion during Spread-Spectrum enabled in ADPLL leads to a failure of phaselock of ADPLL in the next lock attempt, which makes the device-hang***

Revisions Affected

AWRL6888ES1.0

Details

If Spread Spectrum is enabled on the 1-2 GHz VCO in ADPLL, a warm-reset of the device may cause the ADPLL to sporadically fail to achieve phase-lock, resulting in the processor hanging indefinitely in a while loop.

Workarounds

- **Workaround #1 : Disable SSC in ADPLL**

  The user needs to ensure Spread-Spectrum is completely disabled before asserting the device warm-reset. Table 5-1 lists the sequence to completely disable SSC.

Table 5-1. SSC Disable Sequence

S.No	Step	Register/Bitfield	Operation	Value
1	Disable the Spread-Spectrum	ADPLL_HSDIV_CTRL:PLL_CLKCTRL.ENSSC	wr	0
2	Wait for acknowledgement to become 0 from the ADPLL	ADPLL_HSDIV_CTRL:PLL_STATUS.SSCACK	rd	0

- **Workaround #2 : Re-enable ADPLL**

  Instead of waiting for the phaselock indefinitely, the user needs to wait for a maximum of 1ms for the phaselock to assert. If the phaselock signal is not asserted, then disable the ADPLL using the disable sequence and re-enable the ADPLL back. Table 5-2 lists the sequence to disable ADPLL.

Table 5-2. ADPLL Disable Sequence:

S.No	Step	Register/Bitfield	Operation	Value
1	Switch GCMs to crystal		wr	0
2	Disable DCO LDO	ADPLL_HSDIV_CTRL:PLL_CLKCTRL.CLKDCOLDOEN	wr	0
3	Switch off DCO LDO	ADPLL_HSDIV_CTRL:PLL_CLKCTRL.CLKDCOLDOPWDNZ	wr	0
4	Make the PLL go to IDLE state	ADPLL_HSDIV_CTRL:PLL_CLKCTRL.IDLE	wr	1
5	Reset the digital FSM in PLL	ADPLL_HSDIV_CTRL:PLL_CLKCTRL.TINTZ	wr	0

- **Workaround #3 : Issuing nReset to device**

  An external watchdog timer shall be implemented to detect device hang conditions and assert nReset to the radar device through the PMIC or host interface, initiating a cold boot. This work-around utilizes the fact that ADPLL will always be locked everytime after the cold boot.

6 Trademarks

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Revision History

DATE	REVISION	NOTES
September 2026	*	1.0

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Last updated 10/2025