

# MAX202 5-V Dual RS-232 Line Driver and Receiver With $\pm 15$ -kV ESD Protection

## 1 Features

- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- ESD protection for RS-232 bus pins:  $\pm 15$ kV human-body model
- Operates at 5V  $V_{CC}$  supply
- Operates up to 120kbit/s
- Two drivers and two receivers
- Latch-up performance exceeds 100mA Per JESD 78, class II

## 2 Applications

- [Battery-powered systems](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

## 3 Description

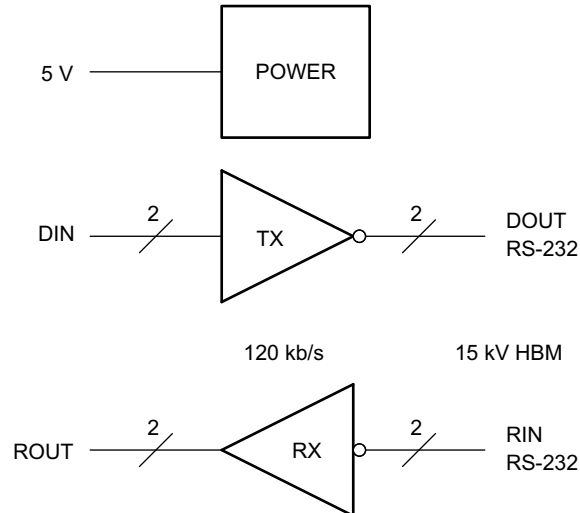
The MAX202 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5V supply. The device operates at data signaling rates up to 120kbit/s and a maximum of 30V/ $\mu$ s driver output slew rate.

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| MAX202      | SOIC (D) (16)          | 9.9mm $\times$ 6mm          |
|             | SOIC WIDE (DW) (16)    | 10.4mm $\times$ 10.3mm      |
|             | TSSOP (PW) (16)        | 5 mm $\times$ 6.4mm         |

(1) For more Information, see [Section 10](#).

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



Copyright © 2016, Texas Instruments Incorporated

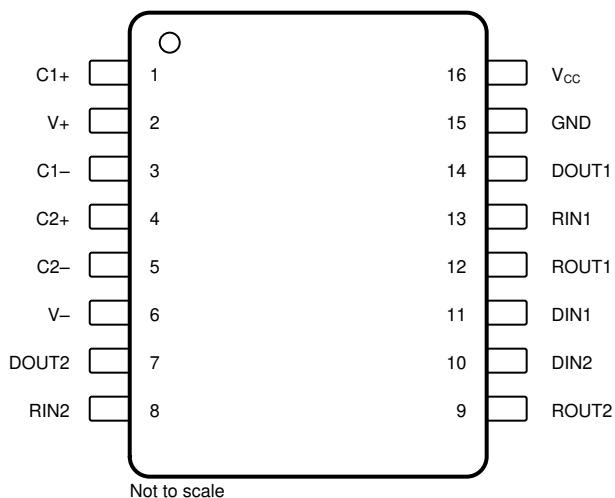
### Block Diagram



## Table of Contents

|                                                |          |                                                                  |           |
|------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                        | <b>1</b> | 6.3 Feature Description.....                                     | <b>8</b>  |
| <b>2 Applications</b> .....                    | <b>1</b> | 6.4 Device Functional Modes.....                                 | <b>8</b>  |
| <b>3 Description</b> .....                     | <b>1</b> | <b>7 Application and Implementation</b> .....                    | <b>10</b> |
| <b>4 Pin Configuration and Functions</b> ..... | <b>3</b> | 7.1 Application Information.....                                 | <b>10</b> |
| <b>5 Specifications</b> .....                  | <b>4</b> | 7.2 Typical Application.....                                     | <b>10</b> |
| 5.1 Absolute Maximum Ratings.....              | <b>4</b> | 7.3 Power Supply Recommendations.....                            | <b>12</b> |
| 5.2 ESD Ratings.....                           | <b>4</b> | 7.4 Layout.....                                                  | <b>13</b> |
| 5.3 Recommended Operating Conditions.....      | <b>4</b> | <b>8 Device and Documentation Support</b> .....                  | <b>14</b> |
| 5.4 Thermal Information.....                   | <b>4</b> | 8.1 Receiving Notification of Documentation Updates....          | <b>14</b> |
| 5.5 Electrical Characteristics.....            | <b>5</b> | 8.2 Support Resources.....                                       | <b>14</b> |
| 5.6 Switching Characteristics.....             | <b>5</b> | 8.3 Trademarks.....                                              | <b>14</b> |
| 5.7 Typical Characteristics.....               | <b>6</b> | 8.4 Electrostatic Discharge Caution.....                         | <b>14</b> |
| <b>Parameter Measurement Information</b> ..... | <b>7</b> | 8.5 Glossary.....                                                | <b>14</b> |
| <b>6 Detailed Description</b> .....            | <b>8</b> | <b>9 Revision History</b> .....                                  | <b>14</b> |
| 6.1 Overview.....                              | <b>8</b> | <b>10 Mechanical, Packaging, and Orderable Information</b> ..... | <b>14</b> |
| 6.2 Functional Block Diagram.....              | <b>8</b> |                                                                  |           |

## 4 Pin Configuration and Functions



**Figure 4-1. D, DW, or PW Package, 16-Pin SOIC or TSSOP  
(Top View)**

**Table 4-1. Pin Functions**

| PIN |                 | TYPE | DESCRIPTION                                            |
|-----|-----------------|------|--------------------------------------------------------|
| NO. | NAME            |      |                                                        |
| 1   | C1+             | —    | Positive lead of C1 capacitor                          |
| 2   | V+              | O    | Positive charge pump output for storage capacitor only |
| 3   | C1–             | —    | Negative lead of C1 capacitor                          |
| 4   | C2+             | —    | Positive lead of C2 capacitor                          |
| 5   | C2–             | —    | Negative lead of C2 capacitor                          |
| 6   | V–              | O    | Negative charge pump output for storage capacitor only |
| 7   | DOUT2           | O    | RS-232 line data output (to remote RS-232 system)      |
| 8   | RIN2            | I    | RS-232 line data input (from remote RS-232 system)     |
| 9   | ROUT2           | O    | Logic data output (to UART)                            |
| 10  | DIN2            | I    | Logic data input (from UART)                           |
| 11  | DIN1            | I    | Logic data input (from UART)                           |
| 12  | ROUT1           | O    | Logic data output (to UART)                            |
| 13  | RIN1            | I    | RS-232 line data input (from remote RS-232 system)     |
| 14  | DOUT1           | O    | RS-232 line data output (to remote RS-232 system)      |
| 15  | GND             | —    | Ground                                                 |
| 16  | V <sub>CC</sub> | —    | Supply voltage, connect to external 5V power supply    |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                    |           | MIN            | MAX            | UNIT |
|----------------------------------------------------|-----------|----------------|----------------|------|
| Supply voltage, $V_{CC}$ <sup>(2)</sup>            |           | -0.3           | 6              | V    |
| Positive charge pump voltage, $V_+$ <sup>(2)</sup> |           | $V_{CC} - 0.3$ | 14             | V    |
| Negative charge pump voltage, $V_-$ <sup>(2)</sup> |           | -14            | 0.3            | V    |
| Input voltage, $V_I$                               | Drivers   | -0.3           | $V_+ + 0.3$    | V    |
|                                                    | Receivers |                | $\pm 30$       |      |
| Output voltage, $V_O$                              | Drivers   | $V_- - 0.3$    | $V_+ + 0.3$    | V    |
|                                                    | Receivers | -0.3           | $V_{CC} + 0.3$ |      |
| Short-circuit duration, $D_{OUT}$                  |           | Continuous     |                |      |
| Operating junction temperature, $T_J$              |           |                | 150            | °C   |
| Storage temperature, $T_{stg}$                     |           | -65            | 150            | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 5.2 ESD Ratings

|                                     |                                                                                |                       | VALUE       | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-----------------------|-------------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | Pins 7, 8, 13, and 14 | $\pm 15000$ | V    |
|                                     |                                                                                | All other pins        | $\pm 2000$  |      |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> |                       | $\pm 1500$  |      |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>; see [Figure 7-1](#)

|                |                                              | MIN     | NOM | MAX | UNIT |
|----------------|----------------------------------------------|---------|-----|-----|------|
| Supply voltage |                                              | 4.5     | 5   | 5.5 | V    |
| $V_{IH}$       | Driver high-level input voltage ( $D_{IN}$ ) | 2       |     |     | V    |
| $V_{IL}$       | Driver low-level input voltage ( $D_{IN}$ )  |         |     | 0.8 | V    |
| $V_I$          | Driver input voltage ( $D_{IN}$ )            | 0       |     | 5.5 | V    |
|                | Receiver input voltage                       | -30     |     | 30  |      |
| $T_A$          | Operating free-air temperature               | MAX202C |     | 70  | °C   |
|                |                                              | MAX202I | -40 | 85  |      |

- (1) Test conditions are  $C1-C4 = 0.1\mu F$  at  $V_{CC} = 5V \pm 0.5V$ .

### 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | D (SOIC) | DW (SOIC) | PW (TSSOP) | UNIT |
|-------------------------------|----------------------------------------------|----------|-----------|------------|------|
|                               |                                              | 16 PINS  | 16 PINS   | 16 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 84.6     | 71.7      | 107.5      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 43.5     | 37.6      | 38.4       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 43.2     | 36.8      | 53.7       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 10.4     | 13.       | 3.2        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 42.8     | 36.4      | 53.1       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [Figure 7-1](#))<sup>(1)</sup>

| PARAMETER                                                                | TEST CONDITIONS                                                                    | MIN | TYP <sup>(2)</sup>    | MAX  | UNIT |
|--------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----|-----------------------|------|------|
| I <sub>CC</sub> Supply current                                           | No load, V <sub>CC</sub> = 5V                                                      |     | 8                     | 15   | mA   |
| <b>DRIVER SECTION</b>                                                    |                                                                                    |     |                       |      |      |
| V <sub>OH</sub> High-level output voltage                                | D <sub>OUT</sub> at R <sub>L</sub> = 3kΩ to GND, D <sub>IN</sub> = GND             | 5   | 9                     |      | V    |
| V <sub>OL</sub> Low-level output voltage                                 | D <sub>OUT</sub> at R <sub>L</sub> = 3kΩ to GND, D <sub>IN</sub> = V <sub>CC</sub> | –5  | –9                    |      | V    |
| I <sub>IH</sub> High-level input current                                 | V <sub>I</sub> = V <sub>CC</sub>                                                   |     | 0                     | 200  | μA   |
| I <sub>IL</sub> Low-level input current                                  | V <sub>I</sub> at 0V                                                               |     | 0                     | –200 | μA   |
| I <sub>OS</sub> <sup>(3)</sup> Short-circuit output current              | V <sub>CC</sub> = 5.5V, V <sub>O</sub> = 0V                                        |     | ±10                   | ±60  | mA   |
| r <sub>O</sub> Output resistance                                         | V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0V, V <sub>O</sub> = ±2V   | 300 |                       |      | Ω    |
| <b>RECEIVER SECTION</b>                                                  |                                                                                    |     |                       |      |      |
| V <sub>OH</sub> High-level output voltage                                | I <sub>OH</sub> = –1mA                                                             | 3.5 | V <sub>CC</sub> – 0.4 |      | V    |
| V <sub>OL</sub> Low-level output voltage                                 | I <sub>OL</sub> = 1.6mA                                                            |     |                       | 0.4  | V    |
| V <sub>IT+</sub> Positive-going input threshold voltage                  | V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C                                        |     | 1.7                   | 2.4  | V    |
| V <sub>IT–</sub> Negative-going input threshold voltage                  | V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C                                        | 0.8 | 1.2                   |      | V    |
| V <sub>hys</sub> Input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> ) |                                                                                    | 0.2 | 0.5                   | 1    | V    |
| r <sub>i</sub> Input resistance                                          | V <sub>I</sub> = ±3V to ±25V                                                       | 3   | 5                     | 7    | kΩ   |

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 5V ± 0.5V.

(2) All typical values are at V<sub>CC</sub> = 5V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

## 5.6 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted; see [Figure 7-1](#))<sup>(1)</sup>

| PARAMETER                                                                | TEST CONDITIONS                                                                                                                | MIN | TYP <sup>(2)</sup> | MAX | UNIT   |
|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-----|--------------------|-----|--------|
| <b>DRIVER SECTION</b>                                                    |                                                                                                                                |     |                    |     |        |
| Maximum data rate                                                        | C <sub>L</sub> = 50pF to 1000pF, R <sub>L</sub> = 3kΩ to 7kΩ<br>one D <sub>OUT</sub> switching, see <a href="#">Figure 6-1</a> | 120 |                    |     | kbit/s |
| t <sub>PLH(D)</sub> Propagation delay time,<br>low- to high-level output | C <sub>L</sub> = 2500pF, R <sub>L</sub> = 3kΩ, all drivers loaded,<br>see <a href="#">Figure 6-1</a>                           |     | 2                  |     | μs     |
| t <sub>PHL(D)</sub> Propagation delay time,<br>high- to low-level output | C <sub>L</sub> = 2500pF, R <sub>L</sub> = 3kΩ, all drivers loaded,<br>see <a href="#">Figure 6-1</a>                           |     | 2                  |     | μs     |
| t <sub>sk(p)</sub> Pulse skew <sup>(3)</sup>                             | C <sub>L</sub> = 150 to 2500pF, R <sub>L</sub> = 3kΩ to 7 kΩ,<br>see <a href="#">Figure 6-2</a>                                |     | 300                |     | ns     |
| SR(tr) Slew rate, transition region                                      | C <sub>L</sub> = 50 to 1000pF, R <sub>L</sub> = 3kΩ to 7 kΩ,<br>V <sub>CC</sub> = 5V, see <a href="#">Figure 6-1</a>           | 3   | 6                  | 30  | V/μs   |
| <b>RECEIVER SECTION (SEE <a href="#">Figure 6-3</a>)</b>                 |                                                                                                                                |     |                    |     |        |
| t <sub>PLH(R)</sub> Propagation delay time,<br>low- to high-level output | C <sub>L</sub> = 150pF                                                                                                         |     | 0.5                | 10  | μs     |
| t <sub>PHL(R)</sub> Propagation delay time,<br>high- to low-level output | C <sub>L</sub> = 150pF                                                                                                         |     | 0.5                | 10  | μs     |
| t <sub>sk(p)</sub> Pulse skew <sup>(3)</sup>                             | C <sub>L</sub> = 150pF                                                                                                         |     | 300                |     | ns     |

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 5V ± 0.5V.

(2) All typical values are at V<sub>CC</sub> = 5V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## 5.7 Typical Characteristics

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

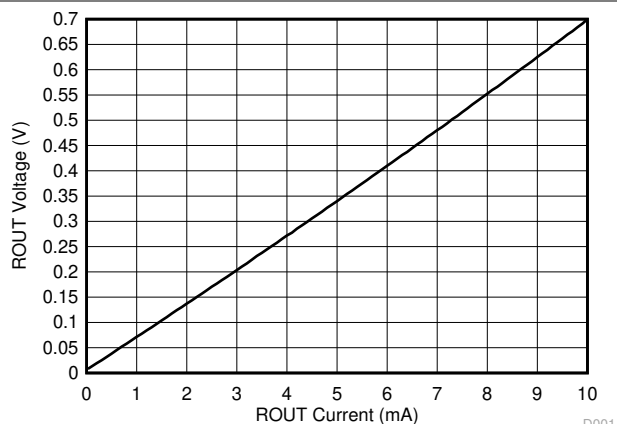


Figure 5-1. Receiver VOL vs Output Current

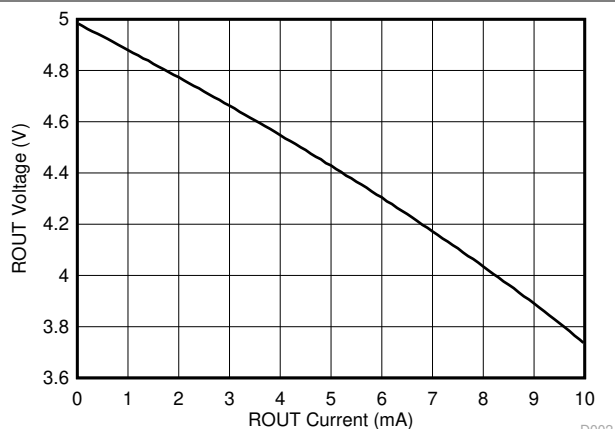


Figure 5-2. Receiver VOH vs Output Current

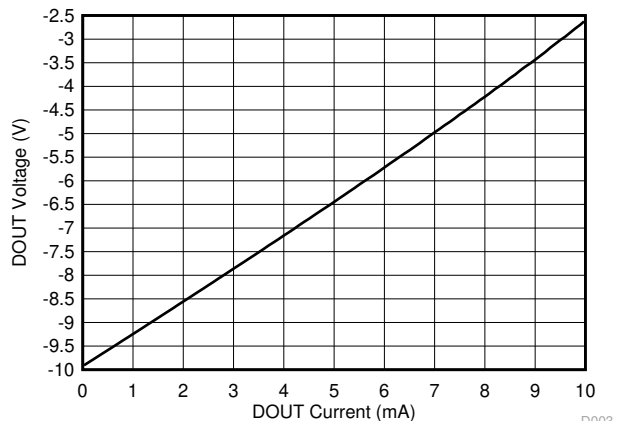


Figure 5-3. Driver VOL vs Output Current

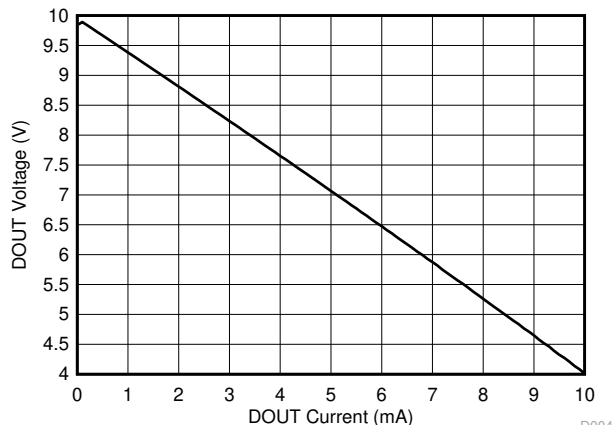


Figure 5-4. Driver VOH vs Output Current

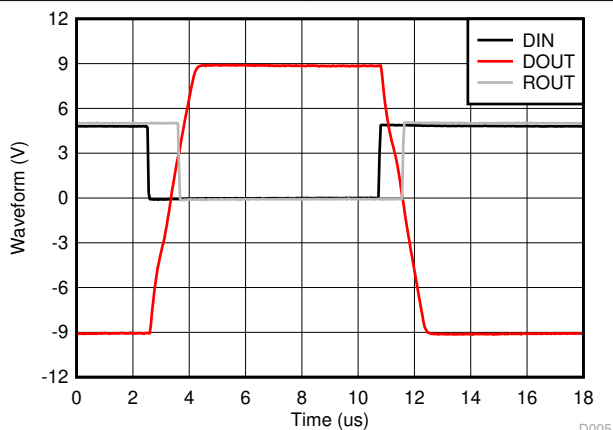
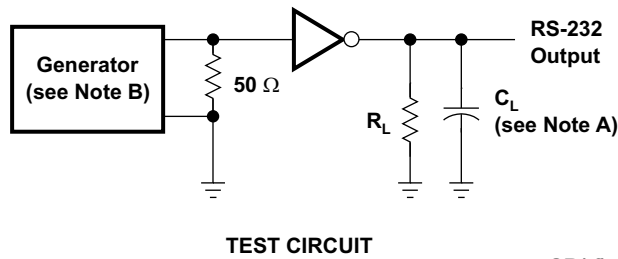
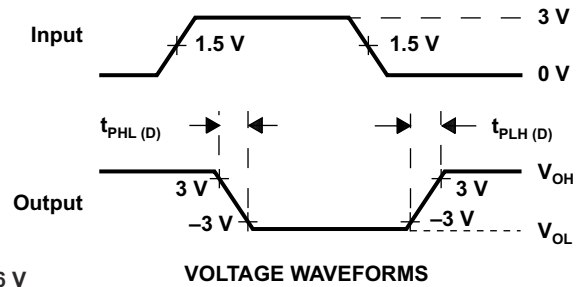


Figure 5-5. Driver and Receiver Loopback Waveforms

## Parameter Measurement Information

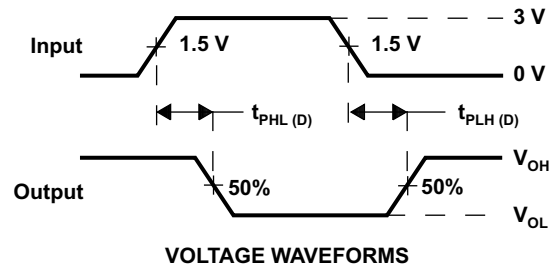
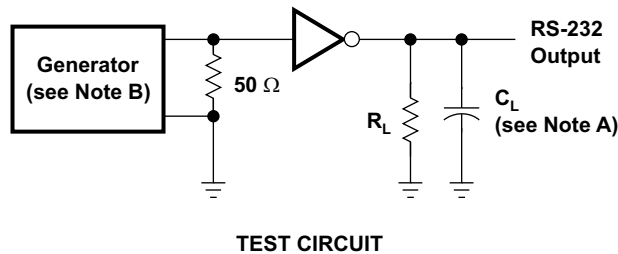


$$SR(tf) = \frac{6\text{ V}}{t_{PHL(D)} \text{ or } t_{PLH(D)}}$$



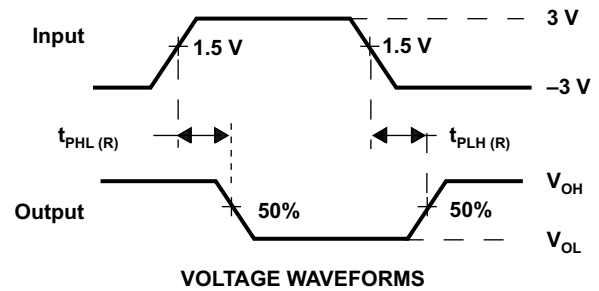
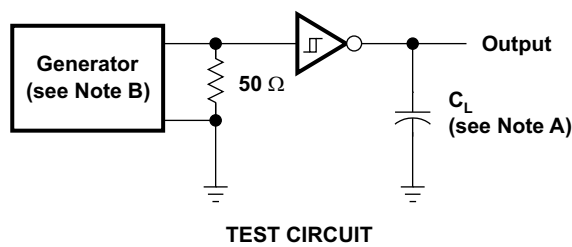
- A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: PRR = 120kbit/s,  $Z_O = 50\Omega$ , 50% duty cycle,  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ .

**Figure 6-1. Driver Slew Rate**



- A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: PRR = 120kbit/s,  $Z_O = 50\Omega$ , 50% duty cycle,  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ .

**Figure 6-2. Driver Pulse Skew**



- A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $Z_O = 50\Omega$ , 50% duty cycle,  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ .

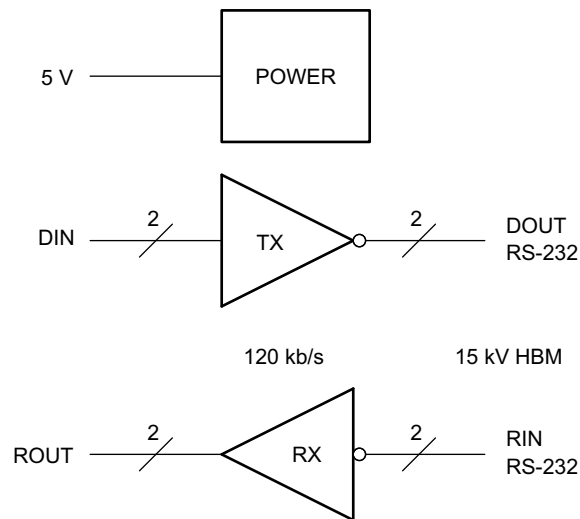
**Figure 6-3. Receiver Propagation Delay Times**

## 6 Detailed Description

### 6.1 Overview

The MAX202 is a dual driver and receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5V supply. Each receiver converts TIA/EIA-232-F inputs to 5V TTL/CMOS levels. These receivers have shorted and open fail safe. The receiver can accept up to  $\pm 30\text{V}$  inputs and decode inputs as low as  $\pm 3\text{V}$ . Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. Outputs are protected against shorts to ground.

### 6.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

### 6.3 Feature Description

#### 6.3.1 Power

The power block increases and inverts the 5V supply for the RS-232 driver using a charge pump that requires four 0.1 $\mu\text{F}$  external capacitors.

#### 6.3.2 RS-232 Driver

Two drivers interface standard logic levels to RS-232 levels. The driver inputs do not have internal pullup resistors. Do not float the driver inputs.

#### 6.3.3 RS-232 Receiver

Two Schmitt trigger receivers interface RS-232 levels to standard logic levels. Each receiver has an internal 5-k $\Omega$  load to ground. An open input results in a high output on ROUT.

### 6.4 Device Functional Modes

#### 6.4.1 $V_{CC}$ Powered by 5V

The device is in normal operation when powered by 5V.

#### 6.4.2 $V_{CC}$ Unpowered

When MAX202 is unpowered, it can be safely connected to an active remote RS-232 device.

### 6.4.3 Truth Tables

Table 6-1 and Table 6-2 list the function for each driver and receiver (respectively).

**Table 6-1. Function Table for Each Driver**

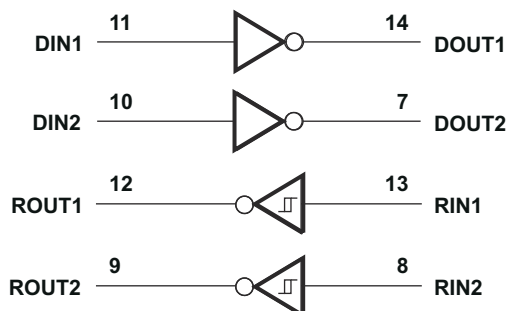
| INPUT<br>DIN <sup>(1)</sup> | OUTPUT<br>DOUT |
|-----------------------------|----------------|
| L                           | H              |
| H                           | L              |

(1) H = high level, L = low level

**Table 6-2. Function Table for Each Receiver**

| INPUT<br>RIN <sup>(1)</sup> | OUTPUT<br>ROUT |
|-----------------------------|----------------|
| L                           | H              |
| H                           | L              |
| Open                        | H              |

(1) H = high level, L = low level,  
Open = input disconnected or connected driver off



**Figure 6-1. Logic Diagram (Positive Logic)**

## 7 Application and Implementation

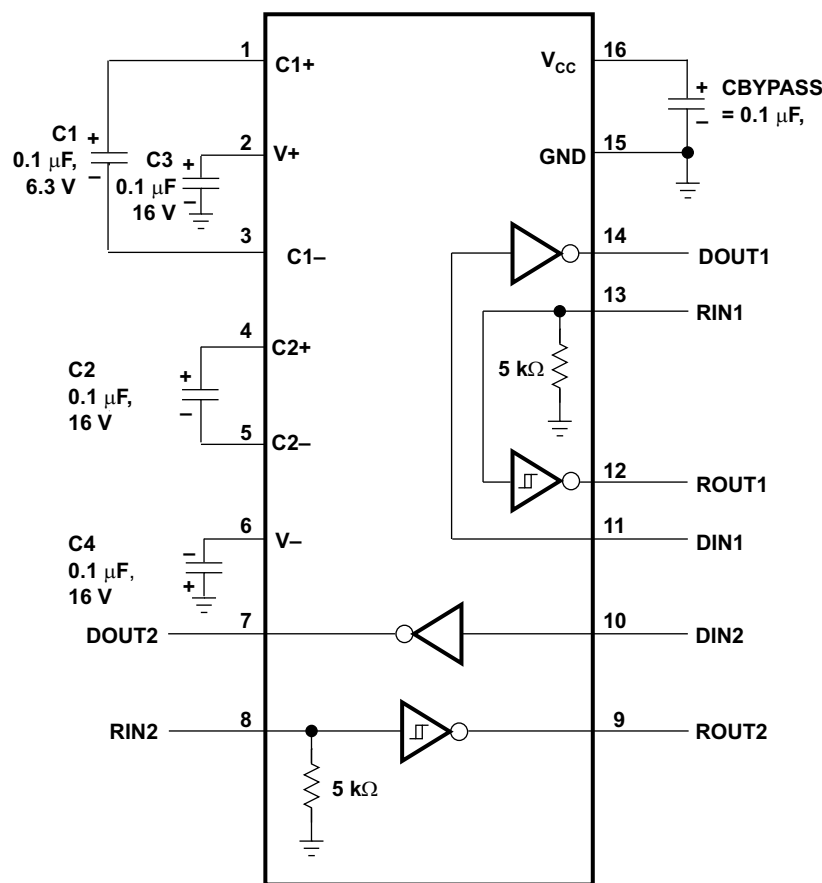
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

For proper operation, add capacitors as shown in Figure 7-1. Pins 9 through 12 connect to UART or general purpose logic lines. RS-232 lines on pins 7, 8, 13, and 14 connect to a connector or cable.

### 7.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

- A. C3 can be connected to  $V_{CC}$  or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

**Figure 7-1. Typical Operating Circuit and Capacitor Values**

#### 7.2.1 Design Requirements

- $V_{CC}$  minimum is 4.5V and maximum is 5.5V.
- Maximum recommended bit rate is 120kbps.

## 7.2.2 Detailed Design Procedure

### 7.2.2.1 Capacitor Selection

The capacitor type used for C1 through C4 is not critical for proper operation. The MAX202 requires 0.1µF capacitors. Capacitors up to 10µF can be used without harm. Ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V–.

Bypass V<sub>CC</sub> to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V<sub>CC</sub> to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

### 7.2.2.2 ESD Protection

MAX202 devices have standard ESD protection structures incorporated on all pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15kV when powered down.

### 7.2.2.3 ESD Test Conditions

Stringent ESD testing is performed by TI based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

### 7.2.2.4 Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 7-2. Figure 7-3 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-kΩ resistor.

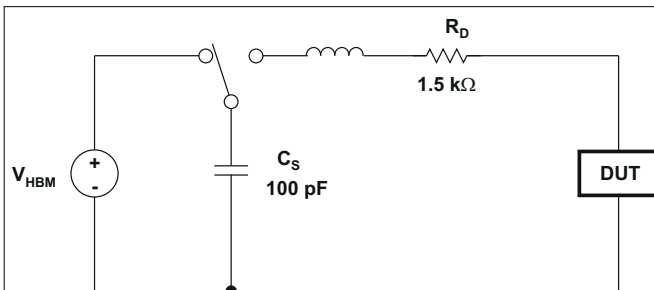


Figure 7-2. HBM ESD Test Circuit

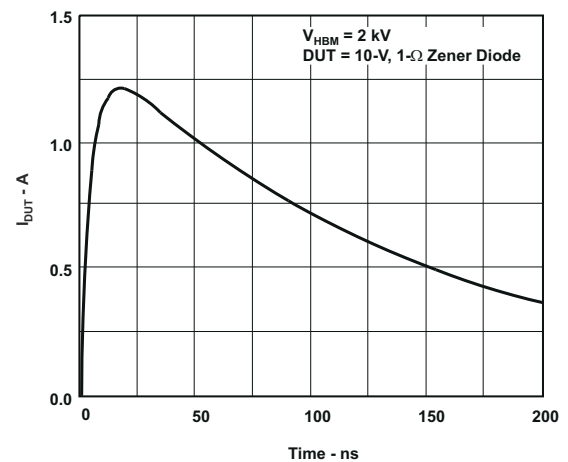
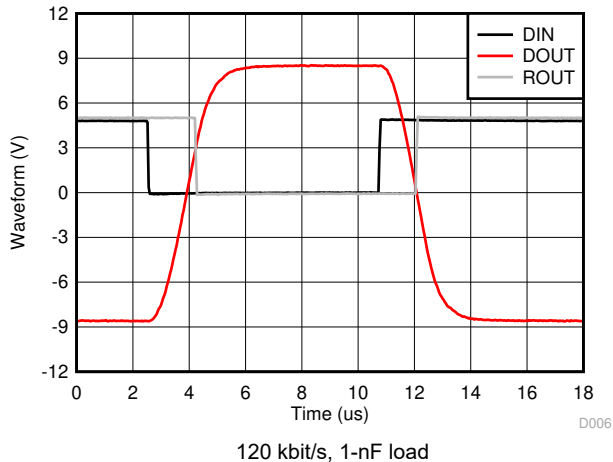


Figure 7-3. Typical HBM Current Waveform

### 7.2.3 Application Curve



**Figure 7-4. Driver and Receiver Loopback Signal**

### 7.3 Power Supply Recommendations

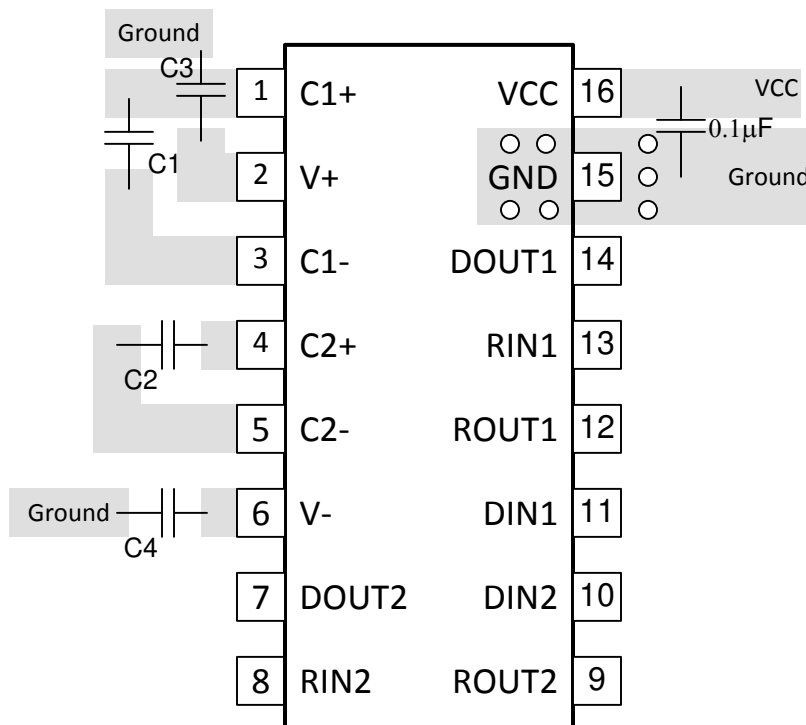
The  $V_{CC}$  voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins.  $V_{CC}$  must be between 4.5 V and 5.5 V.

## 7.4 Layout

### 7.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. For best ESD performance, make the impedance from MAX202 ground pin to the ground plane of the circuit board as low as possible. Use wide metal and multiple vias on both sides of ground pin.

### 7.4.2 Layout Example



**Figure 7-5. MAX202 Circuit Board Layout**

## 8 Device and Documentation Support

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (September 2016) to Revision G (February 2024) | Page |
|------------------------------------------------------------------------|------|
| • Changed the <i>Package Information</i> table.....                    | 1    |
| • Changed values in the <i>Thermal Information</i> table.....          | 4    |

| Changes from Revision E (April 2007) to Revision F (September 2016)                                                                                                                                                                                                                                                                                 | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1    |
| • Removed the <i>Ordering Information</i> table; see POA at the end of the data sheet.....                                                                                                                                                                                                                                                          | 1    |
| • Changed values in the <i>Thermal Information</i> table to align with JEDEC standards.....                                                                                                                                                                                                                                                         | 4    |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MAX202CD</a>   | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | MAX202C             |
| <a href="#">MAX202CDR</a>  | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | MAX202C             |
| <a href="#">MAX202CDW</a>  | Obsolete      | Production           | SOIC (DW)   16  | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | MAX202C             |
| <a href="#">MAX202CDWR</a> | Obsolete      | Production           | SOIC (DW)   16  | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | MAX202C             |
| <a href="#">MAX202CPW</a>  | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | MA202C              |
| <a href="#">MAX202CPWR</a> | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | MA202C              |
| <a href="#">MAX202ID</a>   | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | MAX202I             |
| <a href="#">MAX202IDR</a>  | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | MAX202I             |
| MAX202IDR.A                | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | MAX202I             |
| MAX202IDRE4                | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | MAX202I             |
| <a href="#">MAX202IDW</a>  | Obsolete      | Production           | SOIC (DW)   16  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | MAX202I             |
| <a href="#">MAX202IDWR</a> | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | MAX202I             |
| MAX202IDWR.A               | Active        | Production           | SOIC (DW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | MAX202I             |
| <a href="#">MAX202IPW</a>  | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | MB202I              |
| <a href="#">MAX202IPWR</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | MB202I              |
| MAX202IPWR.A               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | MB202I              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

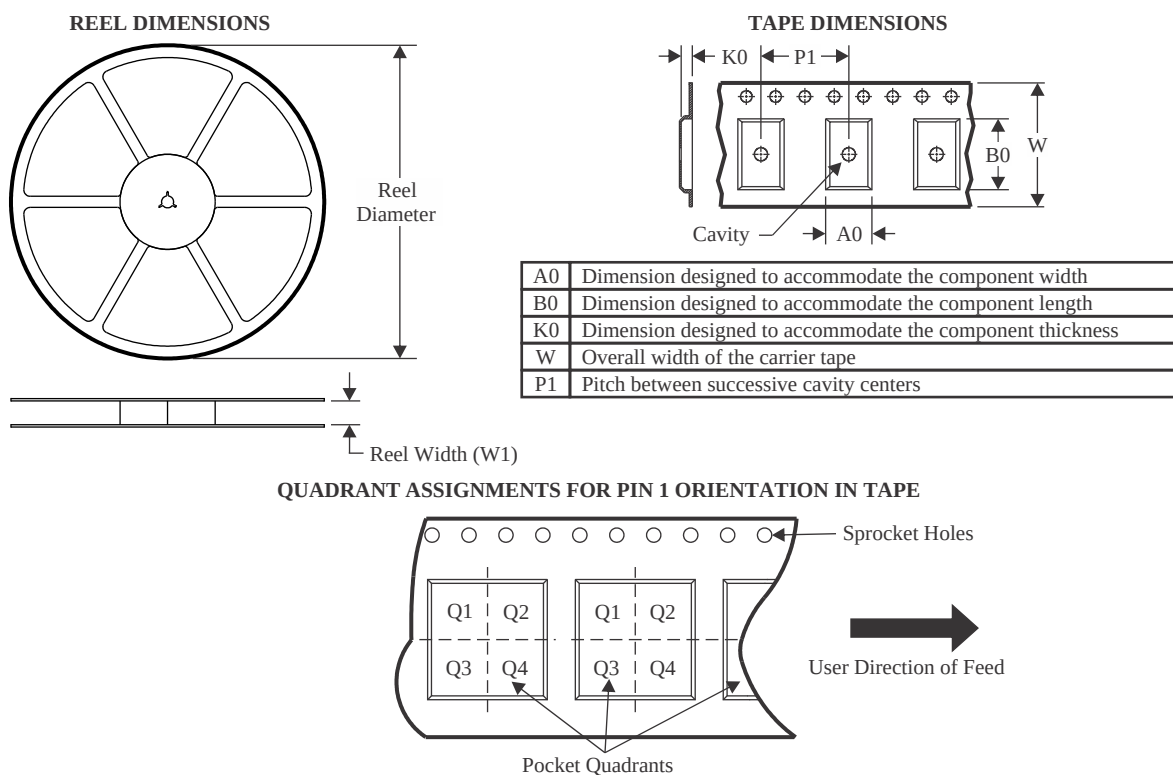
**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

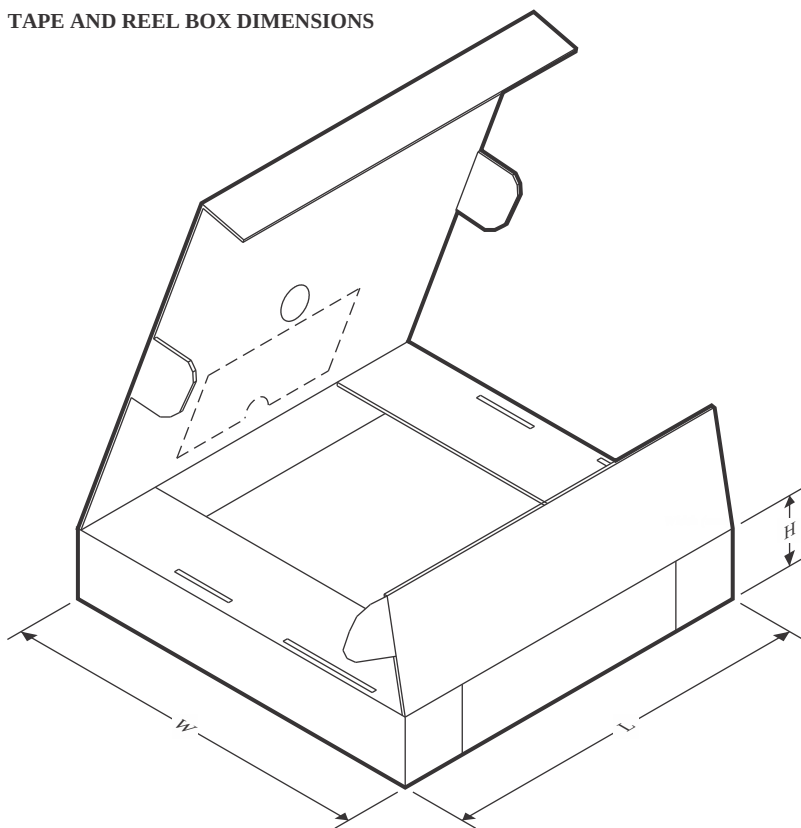
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MAX202IDR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| MAX202IDR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| MAX202IDWR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| MAX202IPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| MAX202IPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

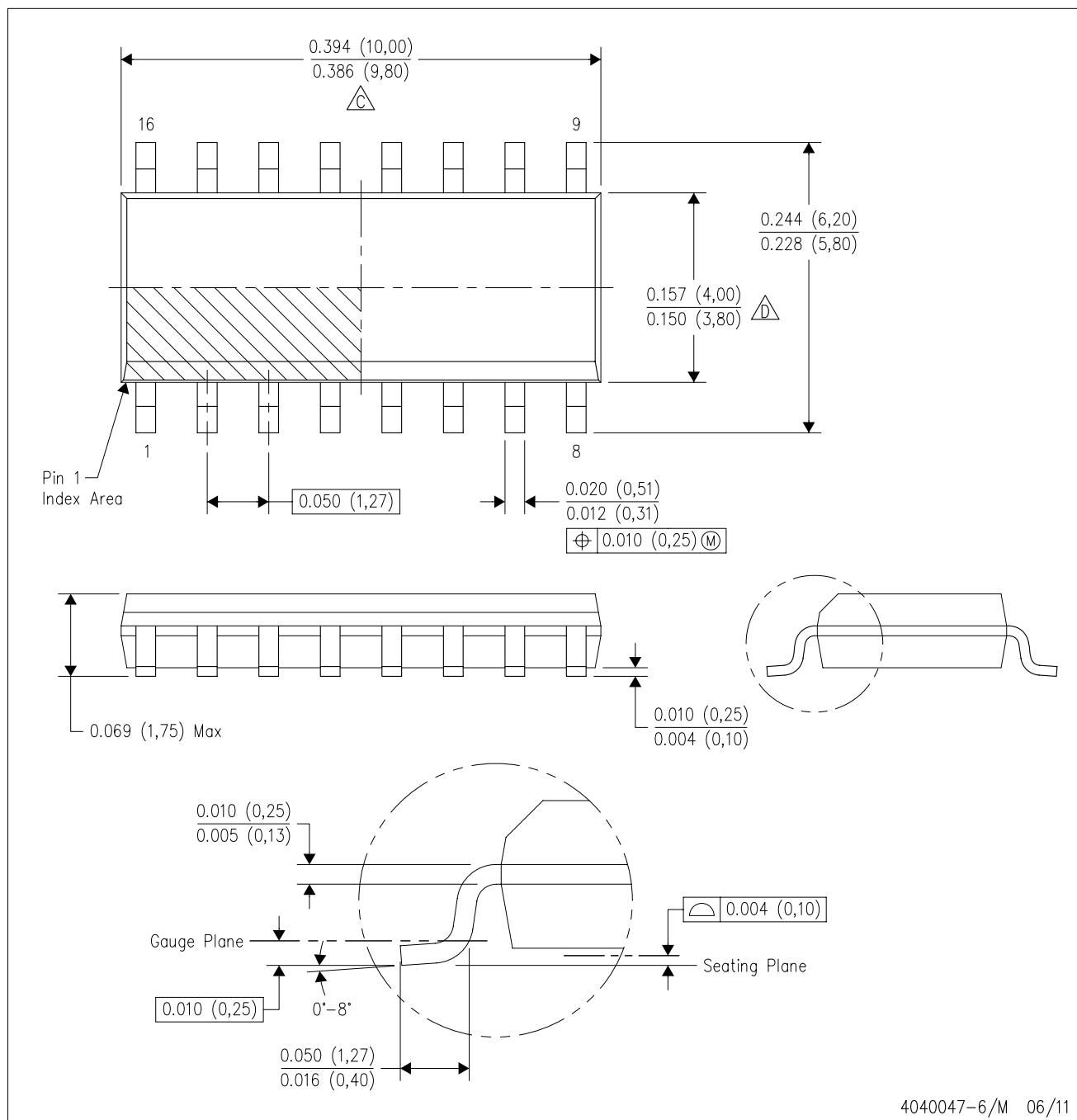


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MAX202IDR  | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| MAX202IDR  | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| MAX202IDWR | SOIC         | DW              | 16   | 2000 | 350.0       | 350.0      | 43.0        |
| MAX202IPWR | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| MAX202IPWR | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## GENERIC PACKAGE VIEW

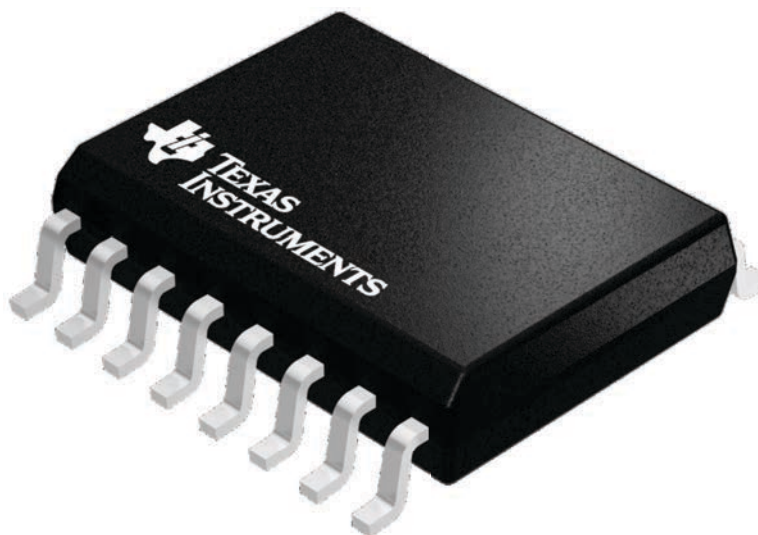
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



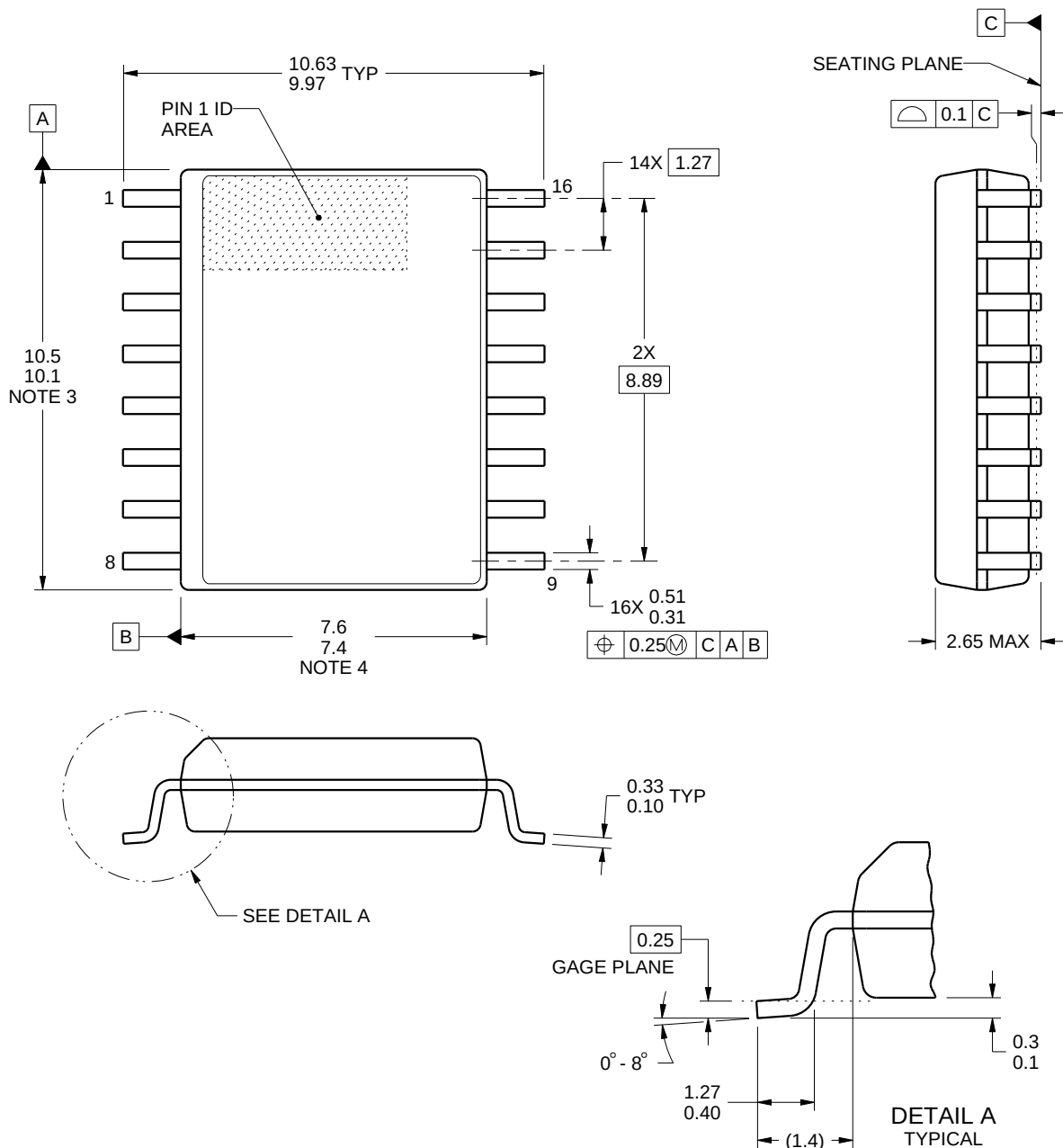
4224780/A



## PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

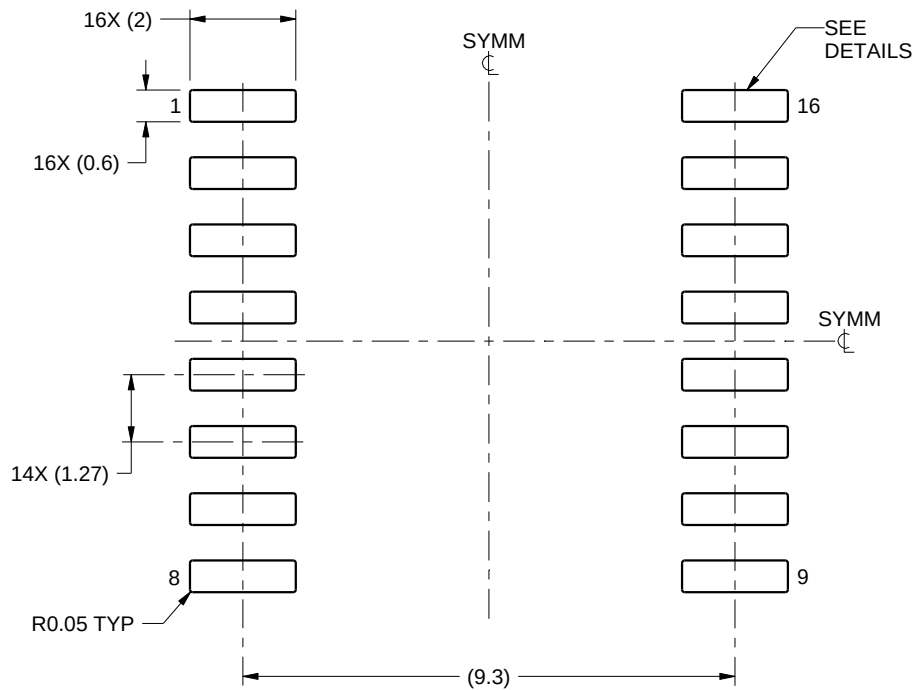
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

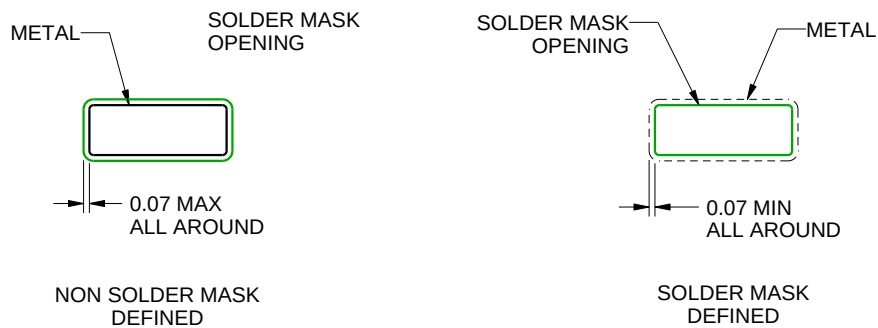
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

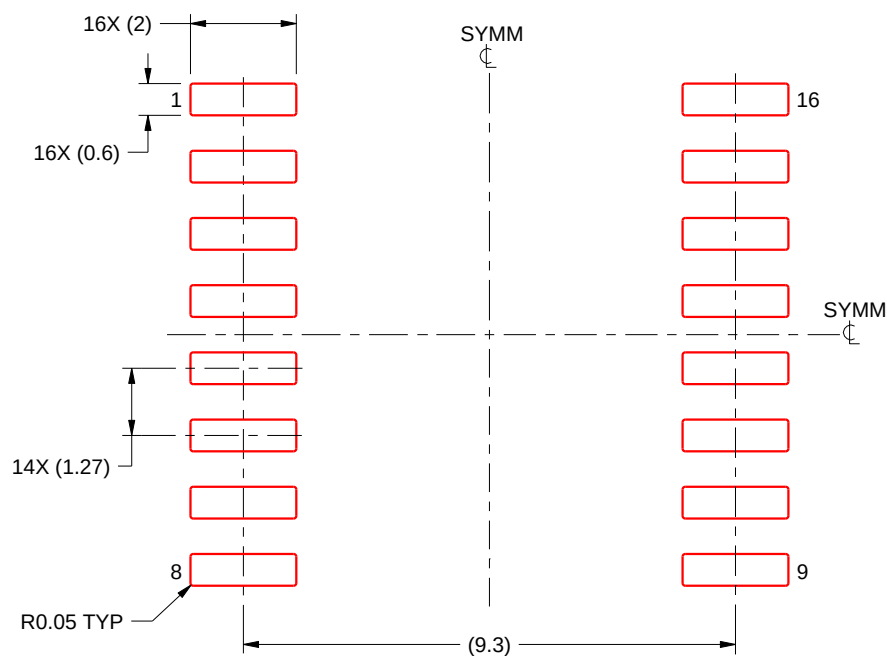
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC

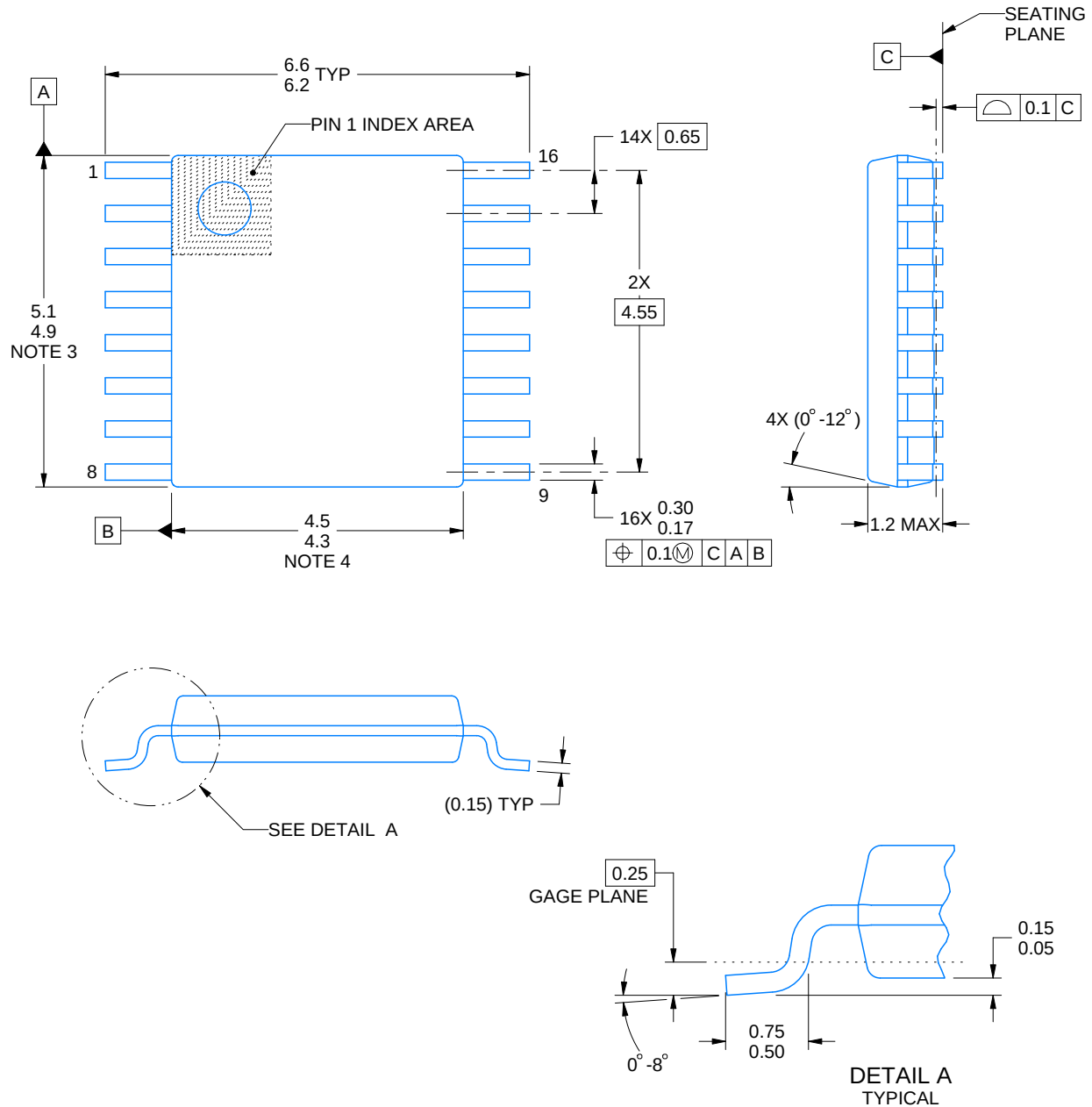
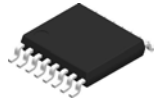


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220204/B 12/2023

## NOTES:

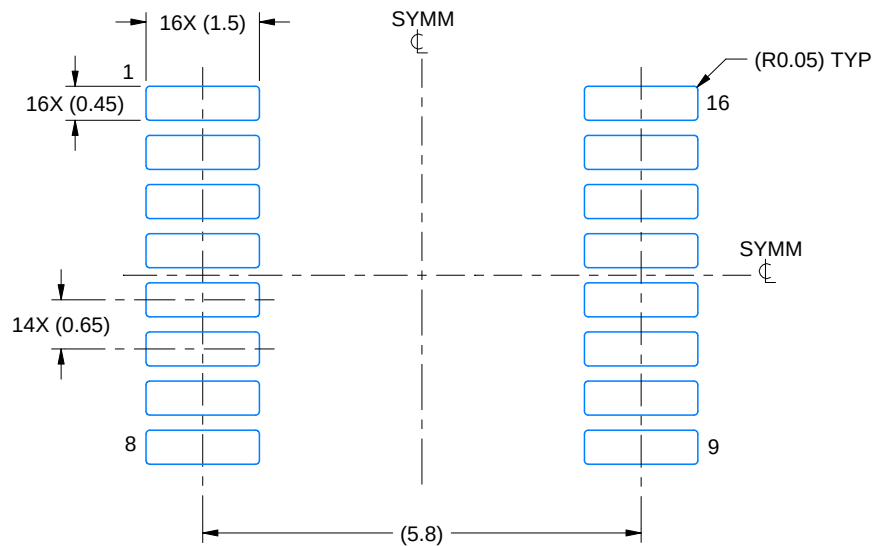
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

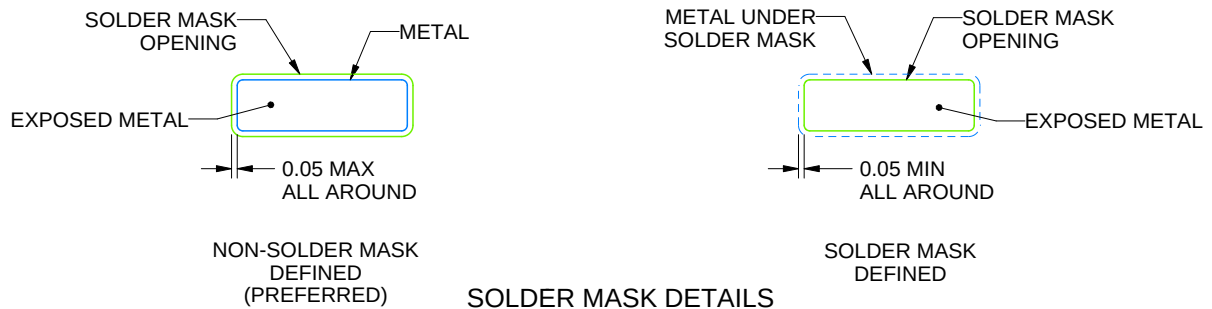
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

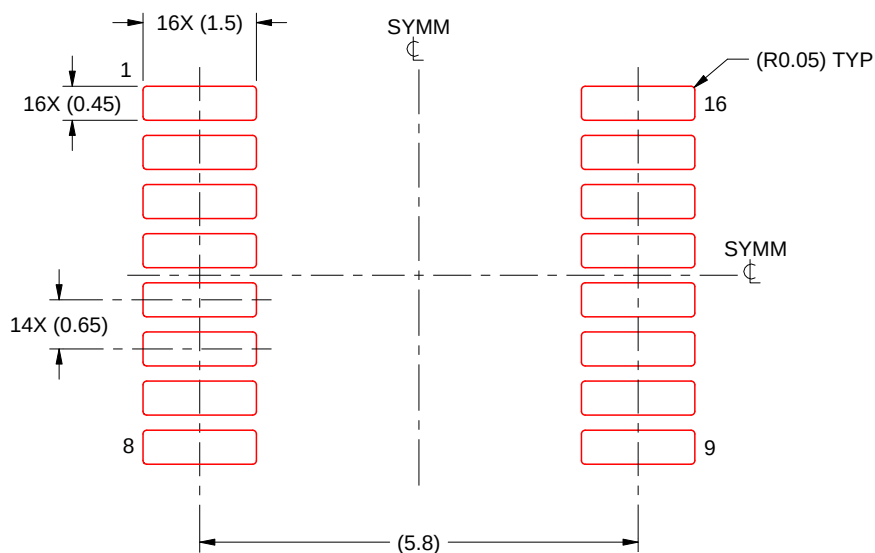
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**PW0016A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025