SN55LVTA4-SEP Radiation Tolerant Quad Channel High-Speed Differential Line Driver

1 Features

- VID V62/25605-01XE
- Total ionizing dose characterized at 30krad (Si)
  - Total ionizing dose radiation lot acceptance testing (TID RLAT) for every wafer lot to 30krad (Si)
- Single-event effects (SEE) characterized:
  - Single event latch-up (SEL) immune to linear energy transfer (LET) = 50MeV-cm2 /mg
  - Single event transient (SET) characterized to 50MeV-cm^2/mg.
- Meet or exceed the requirements of ANSI TIA/EIA-644 standard
- Low-voltage differential signaling with typical output voltage of 350mV and 100Ω load
- Typical output voltage rise and fall times of 500ps (400Mbps)
- Typical propagation delay times of 1.7ns
- Operate from a single 3.3V supply
- Power dissipation 25mW typical per driver at 200MHz
- Driver at high impedance when disabled or with V_{CC} = 0
- Bus-terminal ESD protection exceeds 8kV
- Low-voltage TTL (LVTTL) logic input levels
- Cold sparing for space and high reliability applications requiring redundancy
- Space enhanced plastic (SEP)
  - Controlled baseline
  - Gold wire, NiPdAu lead finish
  - One assembly and test site, one fabrication site
  - Extended product life cycle
  - Military (–55°C to 125°C) temperature range
  - Product traceability
  - Meets NASA ASTM E595 outgassing specification

2 Applications

- Low Earth orbit (LEO) satellite systems
- Command & data handling (C&DH)
- Communications payload
- Optical imaging payload
- Radar imaging payload

3 Description

The SN55LVTA4-SEP is a differential line driver that implements the electrical characteristics of low-voltage differential signaling (LVDS) with a 3.3V supply. This driver delivers a minimum differential output voltage magnitude of 247mV into a 100Ω load when enabled.

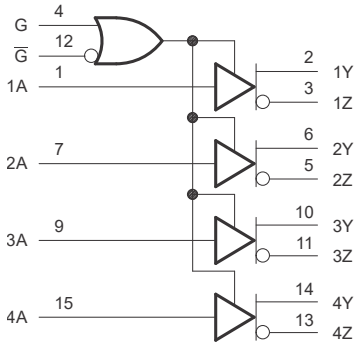
The intended application of this device and signaling technique is both point-to-point and multi-drop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100Ω. The transmission media can be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN55LVTA4-SEP is characterized for operation from –55°C to 125°C.

Package Information

PART NUMBER	PACAKAGE(1)	PACKAGE SIZE(2)
SN55LVTA4-SEP	D (SOIC, 16)	9.9mm × 6mm

(1) For more information, see Section 16.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



SN55LVTA4-SEP Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

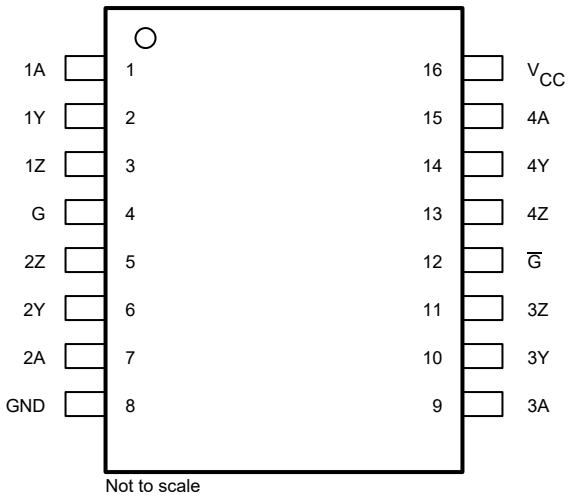


Figure 4-1. D Package, 16-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	LVTTL input signal, 300kΩ internal pull down
1Y	2	O	Differential (LVDS) non-inverting output
1Z	3	O	Differential (LVDS) inverting output
G	4	I	Enable (HI = ENABLE) (must not be left floating)
2Z	5	O	Differential (LVDS) inverting output
2Y	6	O	Differential (LVDS) non-inverting output
2A	7	I	LVTTL input signal, 300kΩ internal pull down
GND	8	G	Ground
3A	9	I	LVTTL input signal, 300kΩ internal pull down
3Y	10	O	Differential (LVDS) non-inverting output
3Z	11	O	Differential (LVDS) inverting output
$\overline{G}$	12	I	Enable (LO = ENABLE) (must not be left floating)
4Z	13	O	Differential (LVDS) inverting output
4Y	14	O	Differential (LVDS) non-inverting output
4A	15	I	LVTTL input signal, 300kΩ internal pull down
V_{CC}	16	P	Supply voltage

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P= Power, G=Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.5	4	V
Input voltage	V_I	–0.5	V_{CC} + 0.5	V
Lead temperature	1.6 mm (1/16 inch) from case for 10 seconds		260	°C
Junction temperature, T_J		-55	140	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±8,000	V
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except bus terminals and GND	±4,000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
T_A	Operating ambient temperature		–55		125	°C
TPCB	PCB temperature	1mm away from the device	–55		128	°C
T_J	Junction temperature		–55		135	°C

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver								
V_{OD}	Driver differential output voltage	R_L = 100 Ω			247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage between logic states	R_L = 100Ω			–50		50	mV
$V_{OC(SS)}$	Steady statte common-mode output voltage	R_L = 100Ω			1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 100Ω			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	R_L = 100Ω				50		mV
I_O(OFF)	Output current with power off	V_{CC} = 0 , V_O = 2.4V			–4		4	µA
I_{OZ}	High impedance state output current	V_O = 0 or 2.4V, G = 0.8V and $\overline{G}$ = 2V			–1		1	µA
I_{OS}	Short-circuit output current, Y or Z	V_O = 0V				-4	-24	mA
I_{OS}	Short-circuit output current, Y & Z	V_{OD} = 0V			-12		12	mA
Input								
V_{IH}	High level input voltage (G, $\overline{G}$, A)	V_{CC} = 3V to 3.6V			2			V
V_{IL}	Low level input voltage (G, $\overline{G}$, A)	V_{CC} = 3V to 3.6V					0.8	V
I_{IH}	High level input current ($\overline{G}$)	V_{IH} = 3.6V, V_{CC} = 0V or 3.6V				4	20	µA
I_{IL}	Low level input current ($\overline{G}$)	V_{IL} = 0V, V_{CC} = 0V or 3.6V				0.1	10	µA
I_{IH}	High level input current (G)	V_{IH} = 3.6V, V_{CC} = 0V or 3.6V				4	20	µA
I_{IL}	Low level input current (G)	V_{IL} = 0V, V_{CC} = 0V or 3.6V				0.1	10	µA
I_{IH}	High level input current (A)	V_{IH} = 3.6V, V_{CC} = 0V or 3.6V				4	20	µA
I_{IL}	Low level input current (A)	V_{IL} = 0V, V_{CC} = 0V or 3.6V				0.1	10	µA
C_I	Input Capacitance (G, $\overline{G}$, A) to ground	V_{CC} = 0V to 3.6V				5		pF
Supply								
I_{CC}	Supply current	V_I = V_{CC} or GND, No load, enabled	-55°C < T_A < 125°C			9	20	mA
		V_I = V_{CC} or GND, R_L = 100Ω, enabled	-55°C < T_A < 125°C			25	35	mA
I_{CC}	Supply current (quiescent)	V_I = V_{CC} or GND, No load, disabled	-55°C < T_A < 125°C			0.25	1	mA

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r	Differential output rise time (20% to 80%)	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 200MHz clock pattern, input V_{IL}=0.8V V_{IH}=V	V_{CC} = 3V to 3.6V	0.4	0.5	1	ns
t_f	Differential output fall time (80% to 20%)		V_{CC} = 3V to 3.6V	0.4	0.5	1	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 200MHz clock pattern, input V_{IL}=0.8V V_{IH}=2V	V_{CC} = 3V to 3.6V	0.5	1.7	4.5	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 200MHz clock pattern, input V_{IL}=0.8V V_{IH}=2V	V_{CC} = 3V to 3.6V	1	1.4	4	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 200MHz clock pattern, input V_{IL}=0.8V V_{IH}=2V	V_{CC} = 3V to 3.6V		0.3	0.6	ns
$t_{SK(O)}$	Chanel to channel output skew, $\|t_{PHL}$ to $t_{PHL}\|$ or $\|t_{PLH}$ to $t_{PLH}\|$	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 200MHz clock pattern, input V_{IL}=0.8V V_{IH}=2V	V_{CC} = 3V to 3.6V		0.3	0.6	ns
$F_{(max)}$	Maximum operating frequency	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 200MHz clock pattern, input V_{IL}=0.8V V_{IH}=2V	V_{CC} = 3V to 3.6V	200			MHz
t_{PHZ}	Disable time, 1.4V input to 50% output	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 1MHz clock pattern on enable, input V_{IL}=0.8V V_{IH}=2V	V_{CC} = 3V to 3.6V		8.1	17	ns
t_{PLZ}	Disable time, 1.4V input to 50% output	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 1MHz clock pattern on enable, input V_{IL}=0.8V V_{IH}=2V			7.3	15	ns
t_{PZH}	Enable time, 1.4V input to 50% output	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 1MHz clock pattern on enable, input V_{IL}=0.8V V_{IH}=2V			5.4	15	ns
t_{PZL}	Enable time, 1.4V input to 50% output	R_L = 100Ω, C_L= 10pF input t_r,t_f= 1ns, 1MHz clock pattern on enable, input V_{IL}=0.8V V_{IH}=2V			2.5	15	ns

5.7 Typical Characteristics

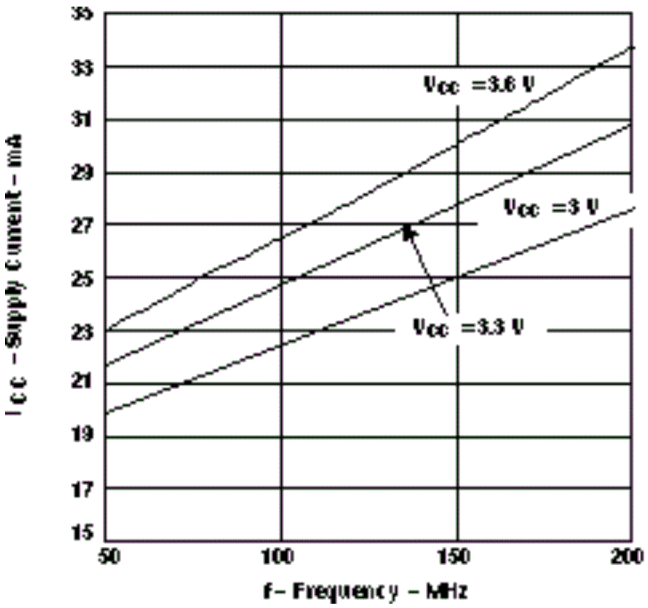


Figure 5-1. Supply Current vs Frequency

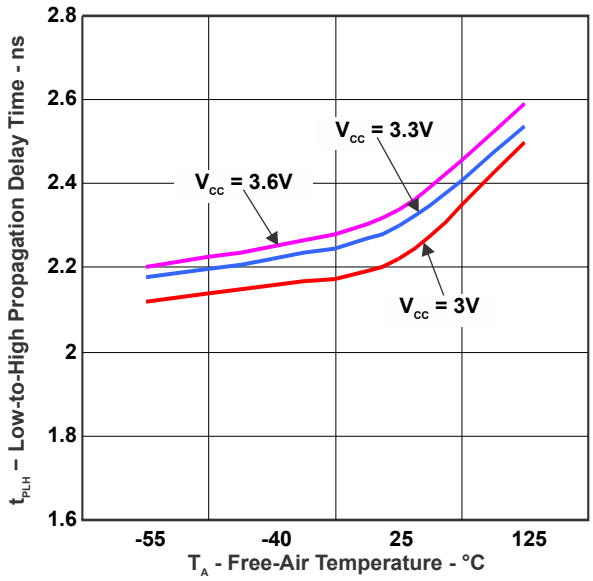


Figure 5-2. Low-to-High Propagation Delay Time vs Free-Air Temperature

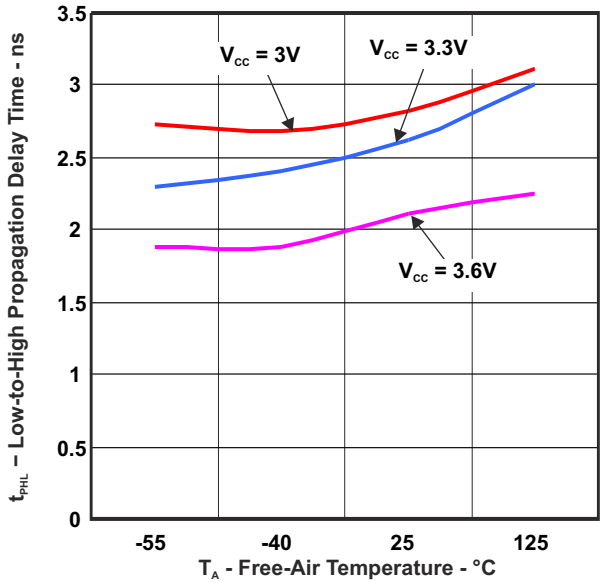


Figure 5-3. High-to-Low Propagation Delay Time vs Free-Air Temperature

6 Parameter Measurement Information

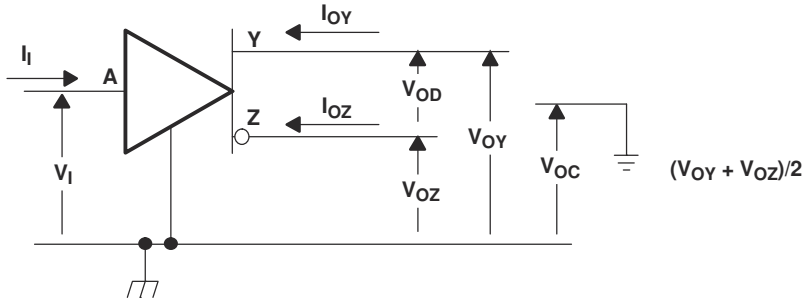
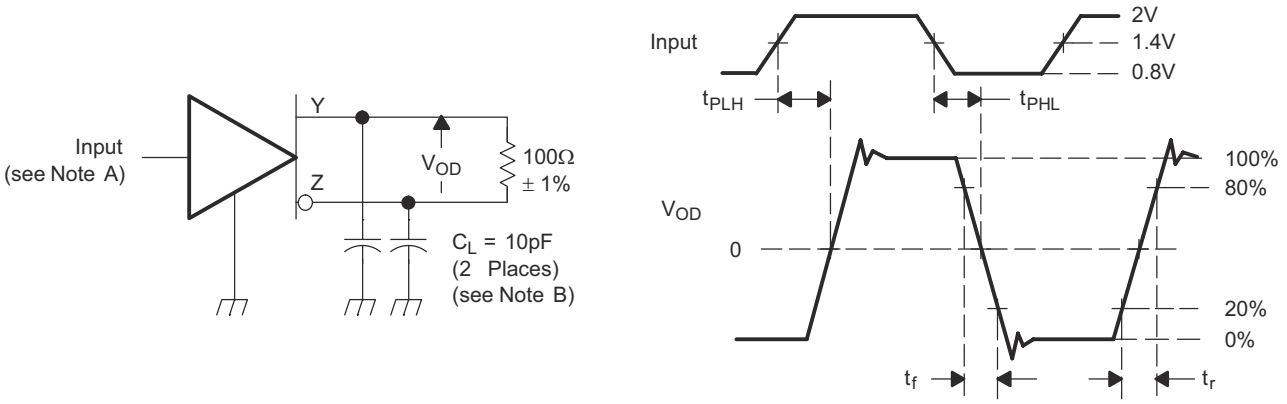


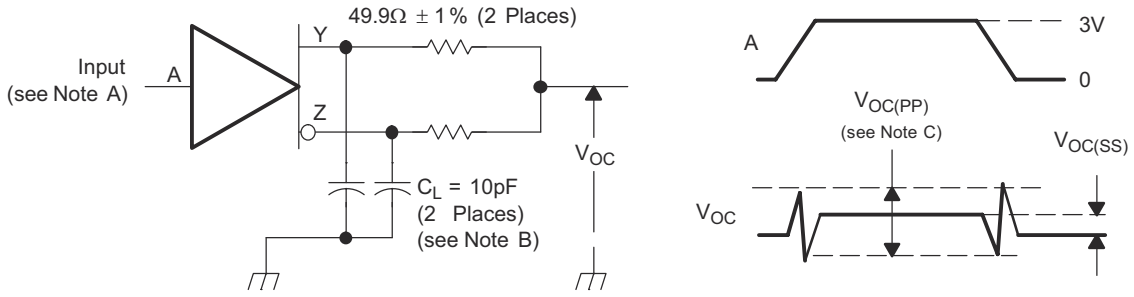
Figure 6-1. Voltage and Current Definitions



A. All input pulses are supplied by a generator having the following characteristics: tr or tf 3 1ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 10 ± 0.2ns

B. C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.

Figure 6-2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

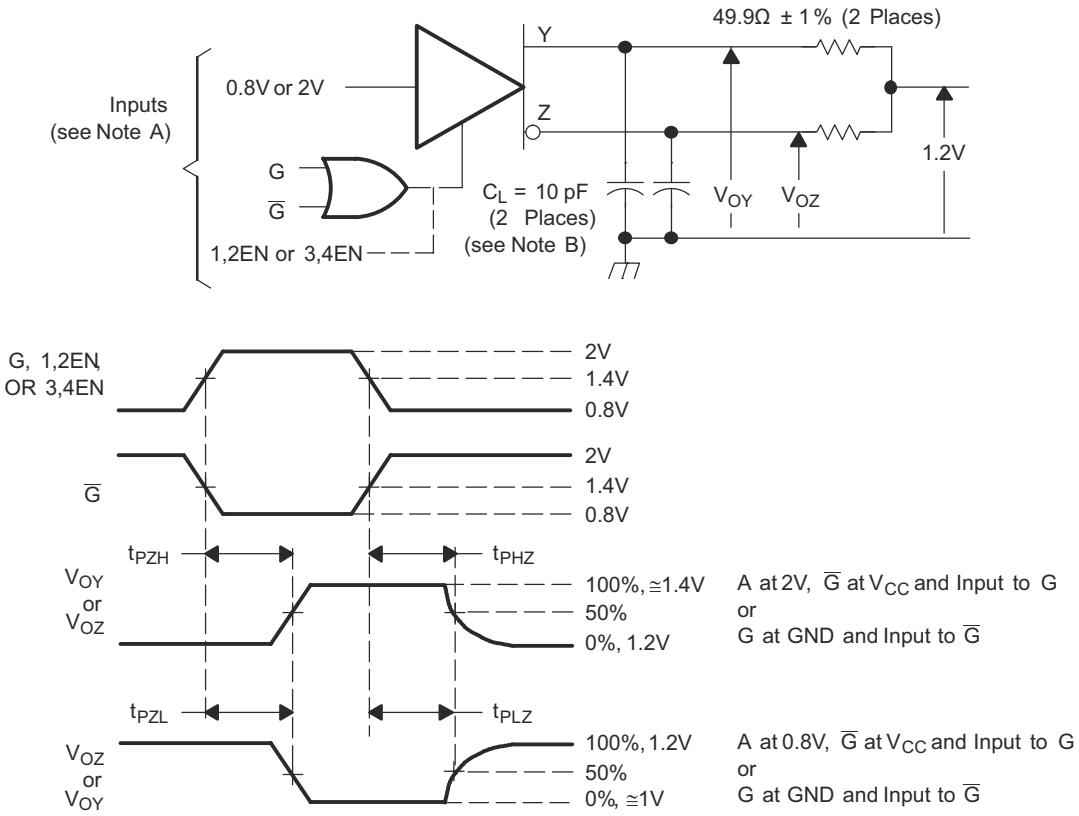


A. All input pulses are supplied by a generator having the following characteristics: tr or tf 3 1ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 10 ± 0.2ns

B. C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.

C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3dB bandwidth of at least 300MHz

Figure 6-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



A. All input pulses are supplied by a generator having the following characteristics: tr or tf < 1ns, pulse repetition rate (PRR) = 0.5Mpps, pulse width = 500 ± 10ns

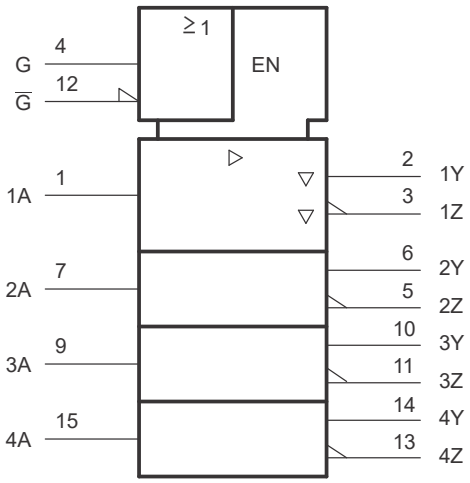
B. C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T

Figure 6-4. Enable/Disable-Time Circuit and Definitions

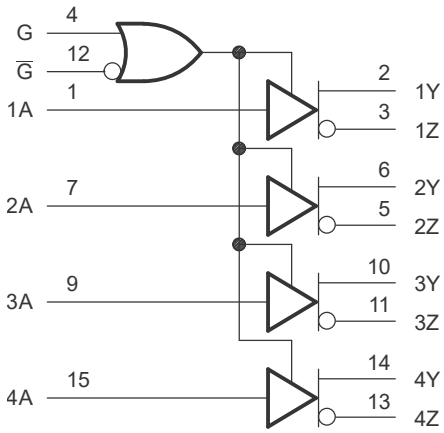
7 Detailed Description

7.1 Overview

7.2 Functional Block Diagram



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



7.3 Feature Description

7.3.1 Unused Enable Pins

Unused enable pins should be tied to V_{CC} or GND as appropriate.

7.3.2 Driver Disabled Output

When the driver is disabled, or when power is removed from the device, the driver outputs are high-impedance.

7.3.3 Driver Equivalent Schematics

The driver input is represented by a CMOS inverter stage with a 7V Zener diode. The input stage is high-impedance, and includes an internal pulldown to ground. If the driver input is left open, the driver input provides a low-level signal to the rest of the driver circuitry, resulting in a low-level signal at the driver output pins. The Zener diode provides ESD protection. The driver output stage is a differential pair, one half of which is shown in Figure 7-1. Like the input stage, the driver output includes Zener diodes for ESD protection. The schematic shows an output stage that includes a set of current sources (nominally 3.5mA) that are connected to the output load circuit based upon the input stage signal. To the first order, the output stage acts a constant-current source.

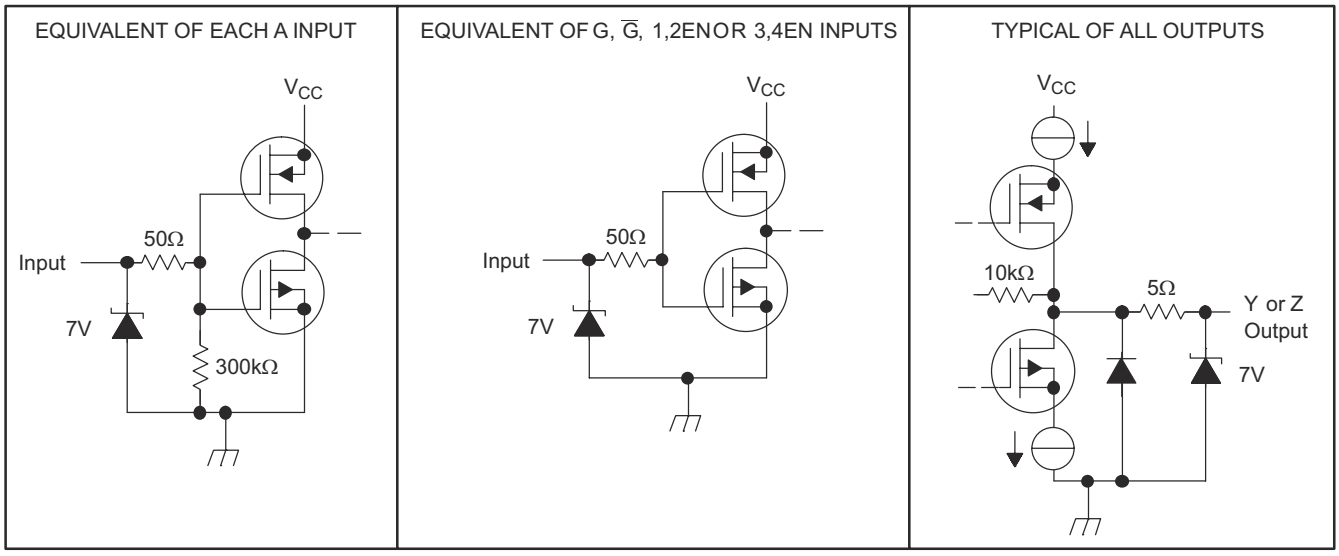


Figure 7-1. Equivalent Input and Output Schematic Diagrams

7.4 Device Functional Modes

Table 7-1. SN55LVTA4-SEP Functional Table (1)

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

8 Application and Implementation

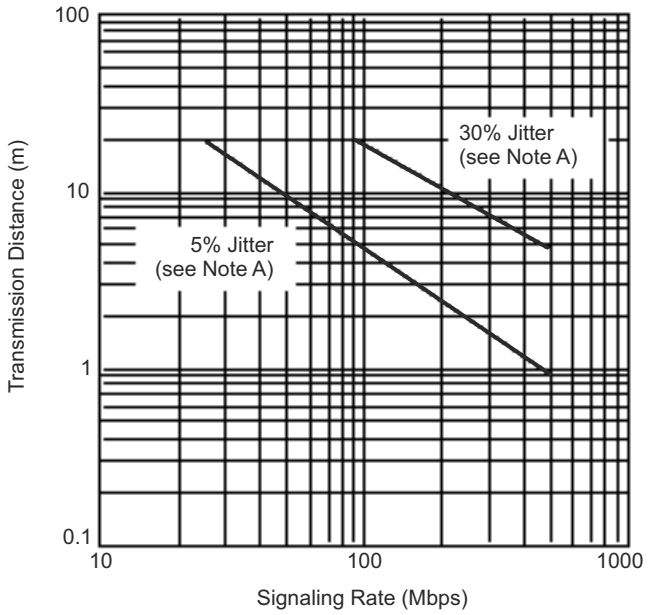
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

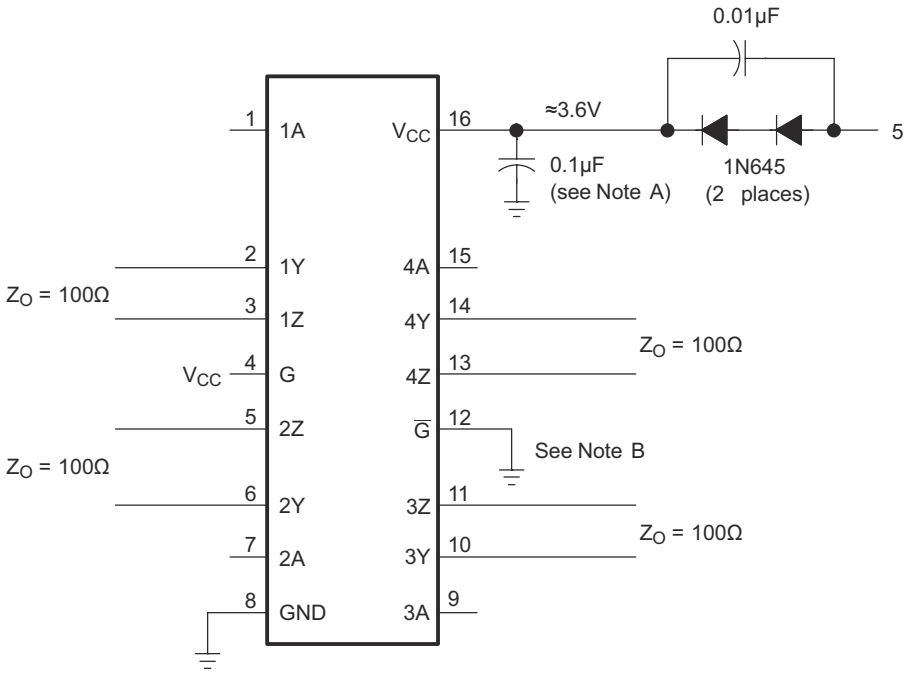
8.1.1 Typical Application

The SN55LVTA4-SEP is generally used as a building block for high-speed point-to-point data transmission where ground differences are less than 1V. The SN55LVTA4-SEP can inter-operate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.



A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudo-random data pattern.

Figure 8-1. Typical Transmission Distance Versus Signaling Rate



A. Place a 0.1µF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor shall be located as close as possible to the device terminals.

B. Unused enable inputs shall be tied to V_{CC} or GND, as appropriate.

Figure 8-2. Operation With 5V Supply

8.1.1.1 Detailed Design Procedure

8.1.1.1.1 Interconnecting Media

The physical communication channel between the driver and the receiver can be any balanced paired metal conductors meeting the requirements of the LVDS standard. This media can be a twisted pair, twinax, flat ribbon cable, or PCB traces. The nominal characteristic impedance of the interconnect is between typical 100Ω with a variation of no more than 10% (90Ω to 110Ω).

8.1.1.2 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6V
Driver Input Voltage	0.8 to 3.3V
Driver Signaling Rate	DC to 400Mbps
Interconnect Characteristic Impedance	100Ω
Termination Resistance	100Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6V
Receiver Input Voltage	0 to 2.4V
Receiver Signaling Rate	DC to 400Mbps
Ground shift between driver and receiver	±1V

8.1.1.3 Application Curve

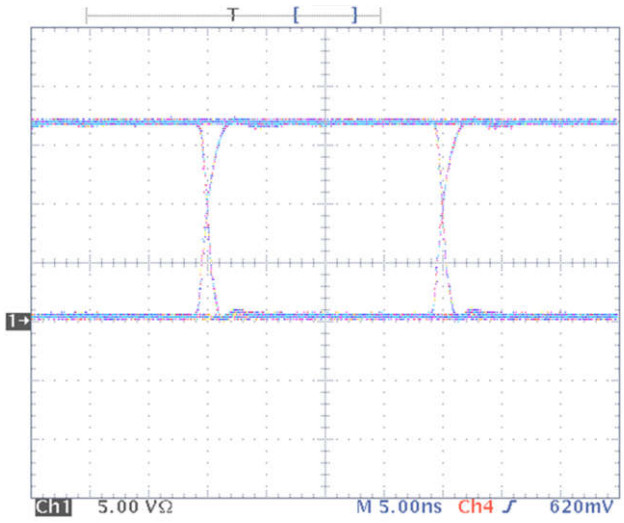


Figure 8-3. Typical Driver Output Eye Pattern in Point-to-Point System

8.1.2 Cold Sparing

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, V_{CC} must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

8.1.3 Power Supply Recommendations

8.1.3.1 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, bypass capacitors create low-impedance paths between power and ground at particular frequency depending on the value. At low frequencies, a voltage regulator offers low-impedance paths between the terminal and ground. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10µF to 1000µF) at the board-level do a good job up into the kHz range. Due to the size and length of the leads, large capacitors tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one can resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because the lead inductance is about 1nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula, equations Equation 1 to Equation 2. A conservative rise time of 200ps and a worst-case change in supply current of 1A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200mV; however, this figure varies depending on the noise budget available in your design.

$$C_{chip} = \left(\frac{\Delta I_{Maximum\ Step\ Change\ Supply\ Current}}{\Delta V_{Maximum\ Power\ Supply\ Noise}}\right) \times T_{Rise\ Time} \quad (1)$$

$$C_{LVDS} = \left(\frac{1A}{0.2V}\right) \times 200\ ps = 0.001\ \mu F \quad (2)$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10µF) and the value of capacitance found above (0.001µF). The smallest value of capacitance shall be as close as possible to the chip.

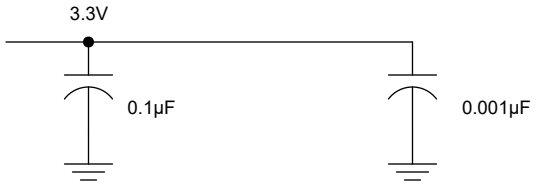


Figure 8-4. Recommended LVDS Bypass Capacitor Layout

8.1.4 Layout

8.1.4.1 Layout Guidelines

8.1.4.1.1 Microstrip vs. Stripline Topologies

As per the LVDS Application and Data Handbook, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 8-5.

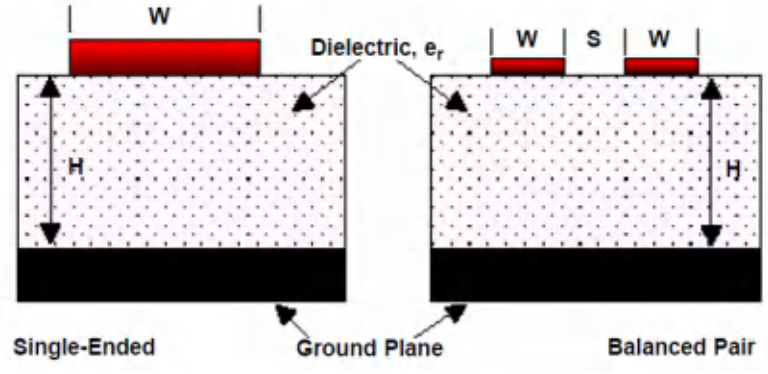


Figure 8-5. Microstrip Topology

Also, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances.

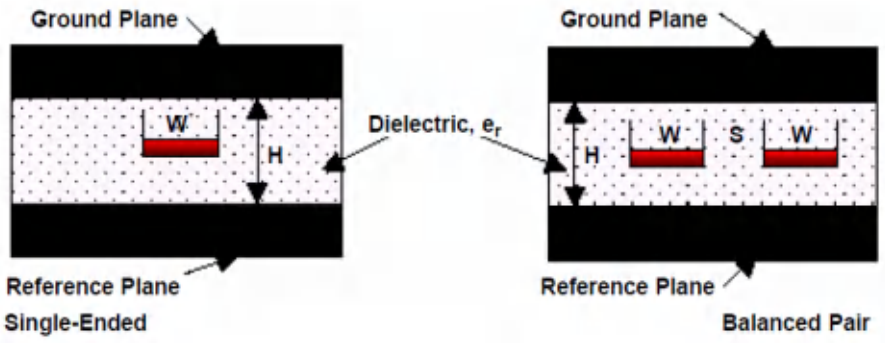


Figure 8-6. Stripline Topology

8.1.4.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15g or 1/2oz start, plated to 30g or 1oz
- All exposed circuitry should be solder-plated (60/40) to 7.62µm or 0.0003in (minimum).
- Copper plating should be 25.4µm or 0.001in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

8.1.4.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, the user should decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, a good practice is to have at least two separate signal planes as shown in Figure 8-7.

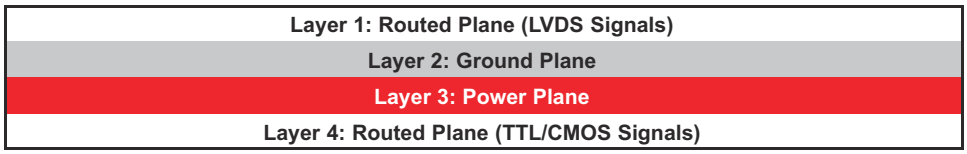


Figure 8-7. Four-Layer PCB Board

Note

The separation between layers 2 and 3 should be 127µm (0.005in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 8-8.

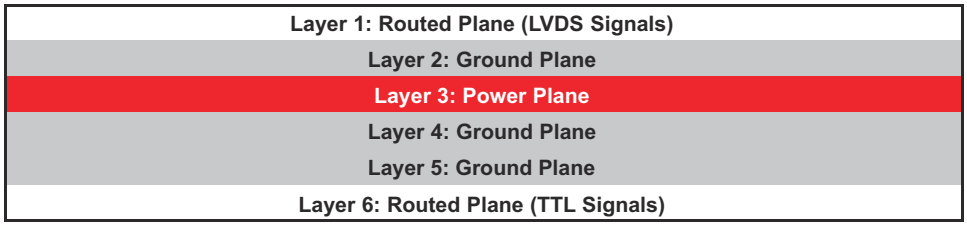


Figure 8-8. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

8.1.4.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to make sure the pairs are balanced; thus, minimizing problems with skew and signal reflection.

For two adjacent single-ended traces, one should use the 3W rule, which stipulates that the distance between two traces should be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

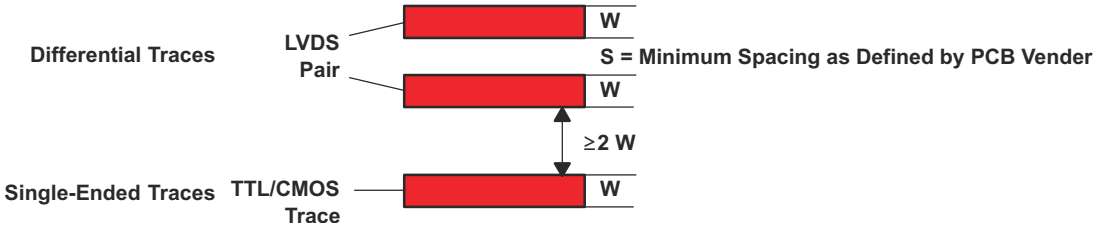


Figure 8-9. 3-W Rule for Single-Ended and Differential Traces (Top View)

The user should exercise caution when using auto-routers, because auto-routers do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

8.1.4.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

8.1.4.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 8-10.

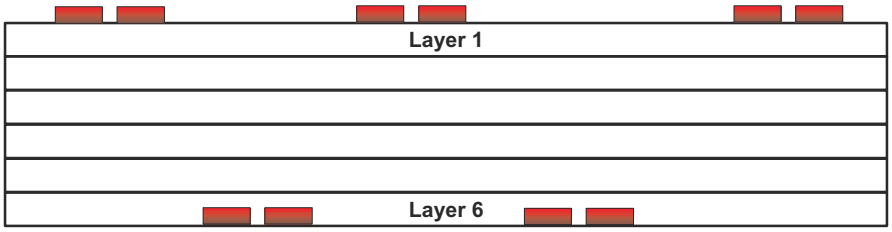


Figure 8-10. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. For continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 8-11. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 0.5pF to 1pF in FR4.

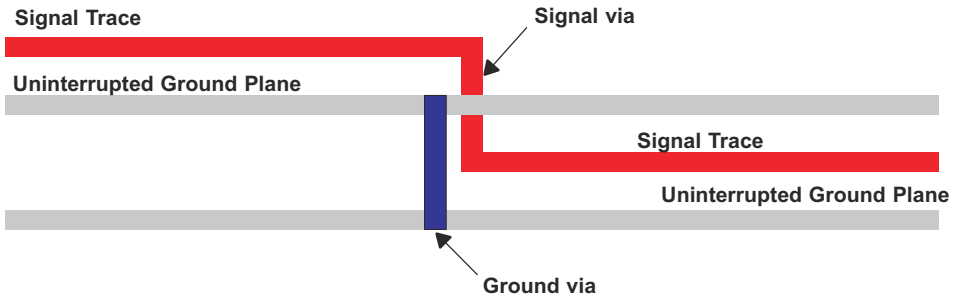


Figure 8-11. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Related Documentation

IBIS modeling is available for this device. Contact the local TI sales office or see the TI website for more information.

For more application guidelines, see the following documents:

- Texas Instruments, *Low-Voltage Differential Signaling Design Notes*
- Texas Instruments, *Interface Circuits for TIA/EIA-644* (LVDS)
- Texas Instruments, *Reducing EMI With LVDS*
- Texas Instruments, *Slew Rate Control of LVDS Circuits*
- Texas Instruments, *Using an LVDS Receiver With RS-422 Data*

10 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

15 Revision History

Changes from Revision * (April 2025) to Revision A (June 2025)	Page
• Changed the document from Advanced Information to *Production* data	1
• Added the VID number to the *Features*	1
• Changed SET from: 43MeV-cm2 /mg to: 50MeV-cm^2/mg in the *Features*	1
• Changed the typical value of C_I 3pF to 5pF in the *Electrical Characteristics*	5

16 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN55LVTA4MDTSEP	Active	Preproduction	SOIC (D) | 16	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	
SN55LVTA4MDTSEP	Active	Production	SOIC (D) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	LVTA4SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

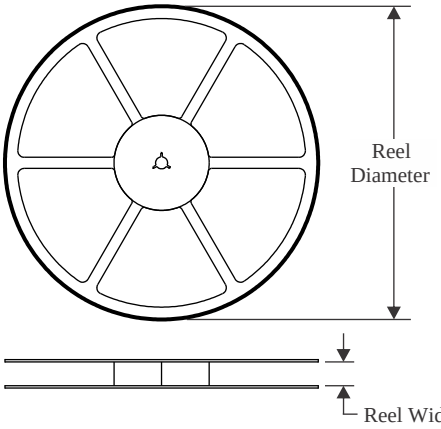
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

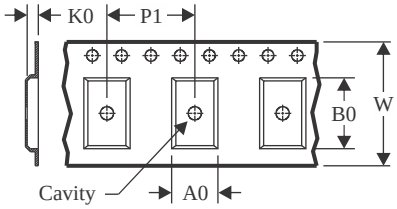
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

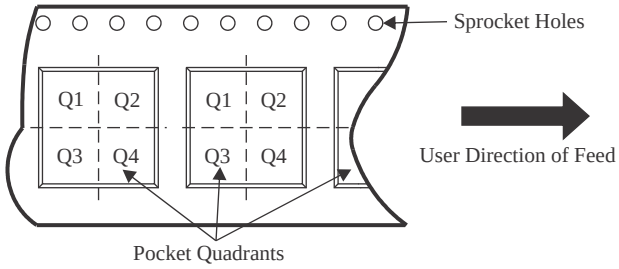


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

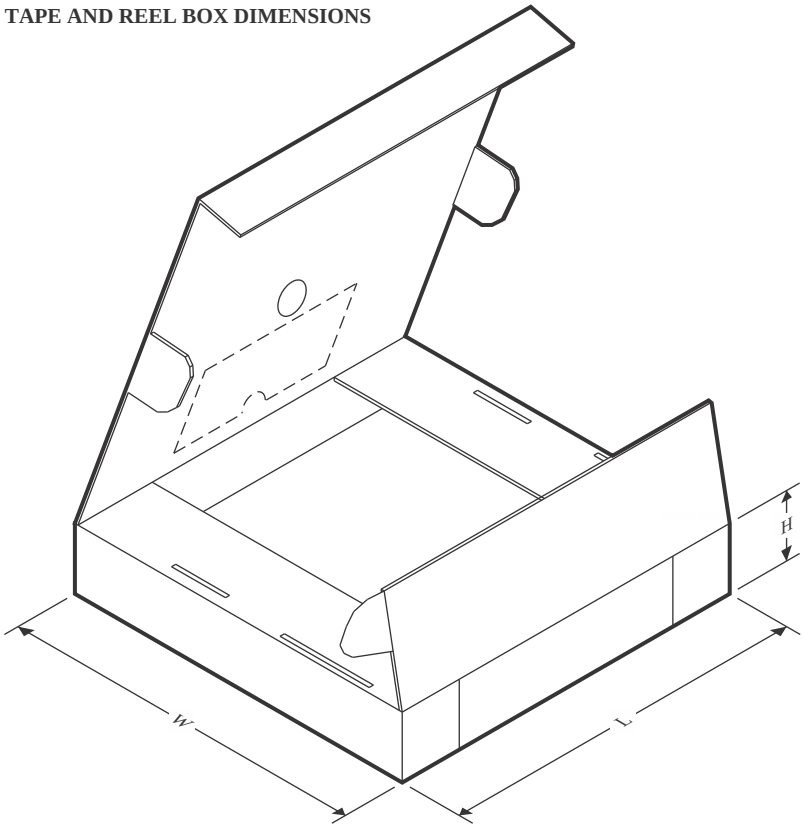
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55LVTA4MDTSEP	SOIC	D	16	250	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

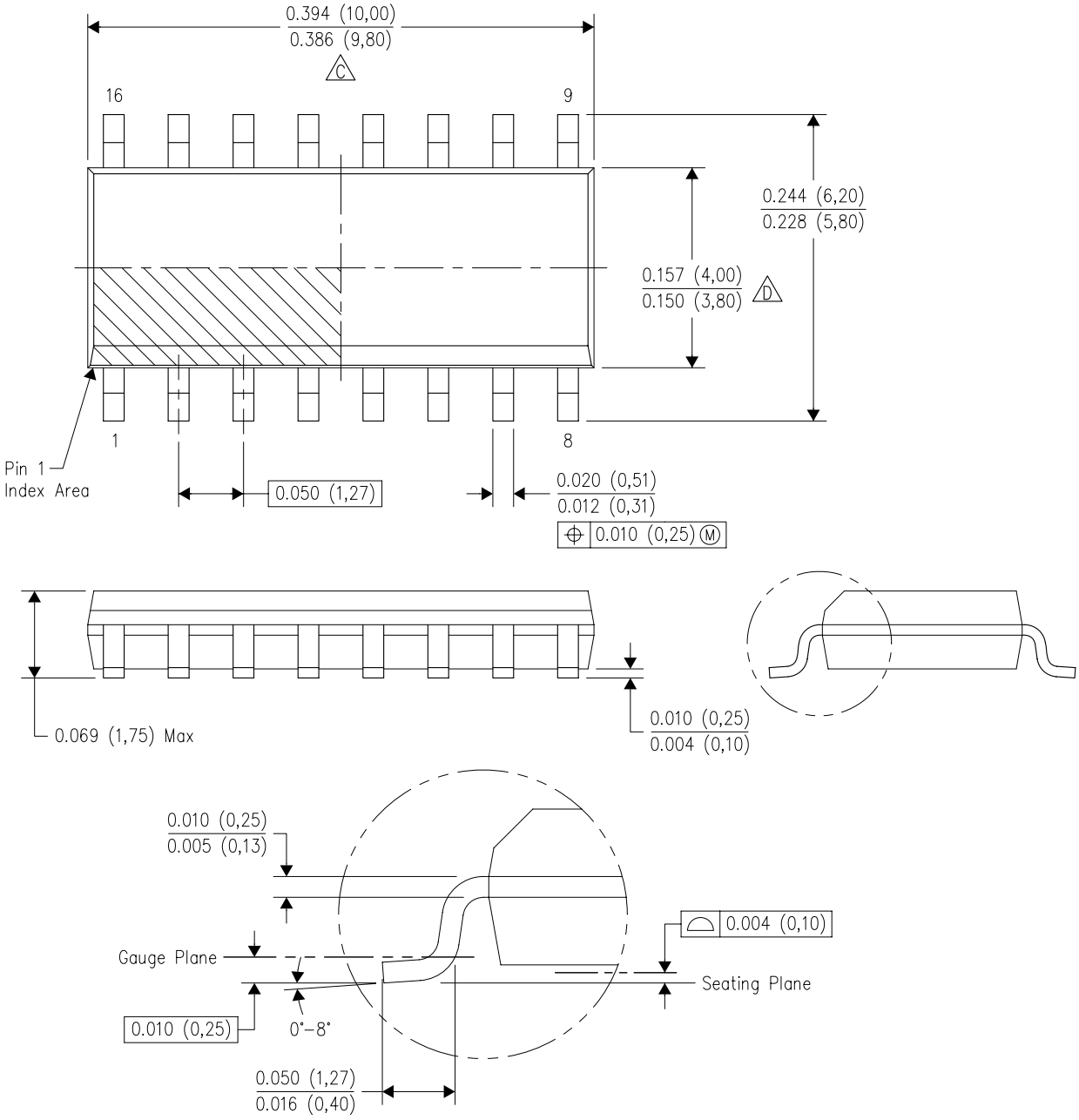
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55LVTA4MDTSEP	SOIC	D	16	250	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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Last updated 10/2025