TLIN821-Q1 Automotive Fault-Protected LIN Transceiver with Inhibit and Wake

1 Features

- AEC-Q100 Qualified for automotive applications
- Compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO 17987–4 electrical physical layer (EPL) specification
- Compliant to SAE J2602-1 LIN Network for Vehicle Applications
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Wide input operational voltage range:
  - V_{SUP} range from 5.5V to 28V
- LIN transmit data rate up to 20kbps
- LIN receive data rate up to 100kbps
- Operating modes: Normal, Standby and Sleep
- Low-power mode wake-up support with source recognition:
  - Remote wake-up over the LIN bus
  - Local wake-up via the WAKE pin
  - Local wake-up via EN
- Integrated 37kΩ LIN pull-up resistor
- Control of system-level power using the INH pin
- Power-up and down glitch-free operation on LIN bus and RXD output
- Protection features:
  - ±40V LIN bus fault tolerant
  - Undervoltage protection on V_{SUP}
  - TXD dominant state time-out, thermal shutdown
  - Unpowered node or ground disconnection fail-safe at system level
- Junction temperatures from -40°C to 150°C
- 8-pin SOIC and leadless VSON-8 package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Automotive infotainment and cluster
- Hybrid electric vehicles and PowerTrain™ systems
- Industrial transportation

3 Description

The TLIN821-Q1 is a local interconnect network (LIN) physical layer transceiver. LIN is a low-speed universal asynchronous receiver transmitter (UART) communication protocol, that supports automotive in-vehicle networking.

The TLIN821-Q1 transmitter supports data rates up to 20kbps. The transceiver controls the state of the LIN bus through the TXD pin and reports the state of the bus on its open-drain RXD output pin. The device has a current-limited wave-shaping driver to reduce electromagnetic emissions (EME).

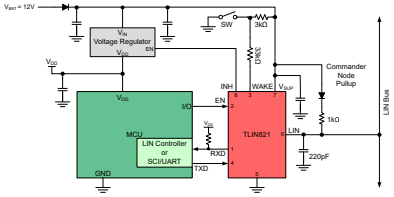
The TLIN821-Q1 is designed to support 12V applications with a wide input voltage operating range. The device supports low-power sleep mode, as well as wake-up from low-power mode through wake over LIN, the WAKE pin, or the EN pin. The device allows system-level reductions in battery current consumption, by selectively enabling the various power supplies that can be present on a node through the device INH output pin.

The device integrates a resistor for LIN responder node applications, ESD protection, and fault protection which allow a reduced amount of external components in the applications. The device prevents back-feed current through LIN to the supply input due to a ground shift or supply voltage disconnection.

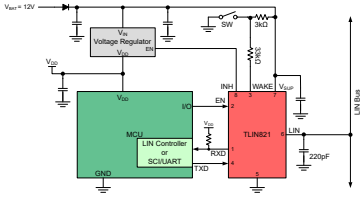
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLIN821-Q1	SOIC (D, 8)	4.9mm × 6mm
	VSON (DRB, 8)	3mm × 3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Commander Node Schematic



Simplified Responder Node Schematic

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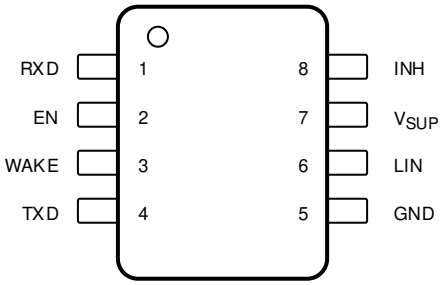
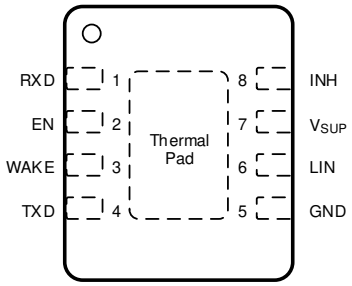
4 Pin Configuration and Functions



Not to scale

Figure 4-1. D Package, 8-Pin (SOIC) Top View



Not to scale

Figure 4-2. DRB Package, 8-Pin (VSON) Top View

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	2	Digital	Sleep mode control input, integrated pull-down
GND	5	GND	Ground connection
INH	8	High Voltage	Inhibit output to control system voltage regulators and supplies, high voltage
LIN	6	Bus IO	LIN bus input/output line
RXD	1	Digital	LIN receive data output, open-drain
Thermal Pad	—		Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief
TXD	4	Digital	LIN transmit data input, integrated pulled down - active low after a local wake-up event
V_{SUP}	7	Supply	High-voltage supply from the battery
WAKE	3	High Voltage	Local wake-up input, high voltage

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted[(1)(2)]

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO 17987)	–0.3	40	V
V_{LIN}	LIN Bus input voltage (ISO 17987)	–40	40	V
V_{WAKE}	WAKE pin input voltage	–0.3	40 and $V_I \leq V_{SUP}+0.3$	V
V_{INH}	INH pin output voltage	–0.3	40 and $V_O \leq V_{SUP}+0.3$	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_O	Digital pin output current		8	mA
$I_{O(INH)}$	Inhibit output current		6	mA
$I_{O(WAKE)}$	WAKE output current due to ground shift $V_{WAKE} \leq (V_{GND} – 0.3V)$		3	mA
T_J	Junction Temp	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM) classification level 3A: LIN with respect to ground		±6000	V
		Human body model (HBM) classification level 3A: WAKE, VSUP with respect to ground		±4000	V
		Human body model (HBM) classification level 2: RXD, EN, TXD, INH per AEC Q100-002[(1)]		±2000	V
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply Voltage	5.5		28	V
V_{LIN}	LIN Bus input voltage	0		28	V
V_{LOGIC}	Logic Pin Voltage	0		5.25	V
T_J	Operating virtual junction temperature range	-40		150	°C
T_{SDR}	Thermal shutdown rising	160			°C
T_{SDF}	Thermal shutdown falling			150	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

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5.4 Thermal Information

THERMAL METRIC[1]		TLIN821-Q1		UNIT
		SOIC (D)	VSON (DRB)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.2	72.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.2	82.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.3	45.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	23.4	10.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.6	41.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	28.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Power Supply Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current						
V_{SUP}	Supply voltage	Device is operational beyond the LIN defined nominal supply voltage range	5.5		28	V
I_{SUP}	Supply current Bus dominant	Normal mode EN = High, R_{LIN} ≥ 500Ω, C_{LIN} ≤ 10nF, INH = WAKE = V_{SUP}, V_{SUP} = 12V		1.2	3	mA
		Standby mode EN = 0V, R_{LIN} ≥ 500Ω, C_{LIN} ≤ 10nF, INH =WAKE = V_{SUP}, V_{SUP} = 12V		0.7	1.2	mA
	Supply current Bus recessive	Normal mode EN = High, INH = WAKE = V_{SUP}, V_{SUP} = 12V		300	700	µA
		Standby mode EN = 0V, INH = WAKE = V_{SUP}, V_{SUP} = 12V		20	55	µA
	Supply current Sleep mode	V_{SUP} = 12V, EN = 0V, LIN = WAKE = V_{SUP}, TXD and RXD floating		9	18	µA
		5.5V < V_{SUP} ≤ 28V, T_J = 150℃ EN = 0V, LIN = WAKE = V_{SUP}, TXD and RXD floating			22	µA
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp up		4.65	4.9	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp down	4.1	4.35		V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.3		V

5.6 Electrical Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD Output Terminal						
V_{OL}	Low-level voltage	Based upon external pull-up to V_{CC}[4]			0.6	V
I_{OL}	Low-level output current, open drain	LIN = 0V, RXD = 0.4V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{LOGIC}[4]	–5		5	µA
TXD Input Terminal						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2			V
V_{HYS}	Input voltage hysteresis		30		500	mV
I_{LKG}	Low-level input leakage current	TXD = 0V	–5		5	µA
$I_{TXD(WAKE)}$	Local wake-up source recognition TXD	Standby mode after a local wake-up event LIN = V_{SUP}, WAKE = 0V or V_{SUP}, TXD = 1V	1.3		8	mA

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5.6 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{TXD}	Internal pull-down resistor		140	500	1200	kΩ
EN Input Terminal						
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{IH}	High-level input voltage		2		5.25	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low-level input current	EN = 0V	–5		5	µA
R_{EN}	Internal pull-down resistor		140	500	1200	kΩ
LIN Terminal (Referenced to V_{SUP})						
V_{OH}	LIN recessive high-level output voltage(1)(2)(3)	TXD = V_{CC}, I_O = 0mA 7V ≤ V_{SUP} ≤ 28V	0.80			V_{SUP}
V_{OH}	LIN recessive high-level output voltage(1)(2)(3)	TXD = V_{CC}, I_O = 0mA 5.5V ≤ V_{SUP} ≤ 7V	3			V
V_{OL}	LIN dominant low-level output voltage(1)(2)(3)	TXD = 0V 7V ≤ V_{SUP} ≤ 28V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage(1)(2)(3)	TXD = 0V 5.5V ≤ V_{SUP} ≤ 7V			1.2	V
V_{BUSdom}	Low-level input voltage(3)	LIN dominant (including LIN dominant for wake up)			0.4	V_{SUP}
V_{BUSrec}	High-level input voltage(3)	Lin recessive	0.6			V_{SUP}
V_{IH}	LIN recessive high-level input voltage(1)(2)	7V ≤ V_{SUP} ≤ 18V	0.47		0.6	V_{SUP}
V_{IL}	LIN dominant low-level input voltge(1)(2)	7V ≤ V_{SUP} ≤ 18V	0.4		0.53	V_{SUP}
$V_{SUP_NON_OP}$	V_{SUP} where impact of recessive LIN bus < 5%(3)	TXD & RXD open 5.5V ≤ V_{LIN} ≤ 40V	–0.3		40	V
V_{BUS_CNT}	Receiver center threshold(3)	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom})/2	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO 17987)	V_{HYS} = V_{BUSrec} - V_{BUSdom}			0.175	V_{SUP}
V_{HYS}	Hysteresis voltage (SAE J2602)	V_{HYS} = V_{IH} - V_{IL}	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN termination pull-up path	I_{SERIAL_DIODE} = 10µA	0.4	0.7	1.0	V
$I_{BUS(LIM)}$	Limiting current ISO 17987 Param 12	TXD = 0V, V_{LIN} = 18V, V_{SUP} = 18V	40	90	200	mA
$I_{BUS_PAS_dom}$	Receiver leakage current, dominant	Driver off/recessive, LIN = 0V V_{SUP} = 12V	–1			mA
$I_{BUS_PAS_rec1}$	Receiver leakage current, recessive	Driver off/recessive, LIN ≥ V_{SUP} 5.5V ≤ V_{SUP} ≤ 28V			20	µA
$I_{BUS_PAS_rec2}$	Receiver leakage current, recessive	Driver off/recessive, LIN = V_{SUP}	–5		5	µA
$I_{BUS_NO_GND}$	Leakage current, loss of ground	GND_{Device} = V_{SUP} = 18V R_{Meas} = 1kΩ 0V < V_{LIN} < 18V	–1		1	mA
$I_{leak\ gnd(dom)}$	Leakage current, loss of ground(5)	V_{SUP} = 8V, GND = open, V_{SUP} = 18V, GND = open $R_{Commander}$ = 1kΩ, C_L = 1nF $R_{Responder}$ = 20kΩ, C_L = 1nF LIN = dominant	–1		1	mA
$I_{leak\ gnd(rec)}$	Leakage current, loss of ground(5)	V_{SUP} = 8V, GND = open, V_{SUP} = 18V, GND = open $R_{Commander}$ = 1kΩ, C_L = 1nF $R_{Responder}$ = 20kΩ, C_L = 1nF LIN = recessive	–100		100	µA
$I_{BUS_NO_BAT}$	Leakage current, loss of supply	V_{SUP} = GND 0V ≤ V_{LIN} ≤ 18V			5	µA
I_{RSLEEP}	Pull-up current source to V_{SUP} sleep mode	V_{SUP} = 14V, LIN = GND	–20		–1.5	µA
R_{PU_SLP}	Internal pull-up resistor to V_{SUP} during sleep mode	EN = 0V	1000	1700	2500	kΩ
R_{PU}	Internal pull-up resistor to V_{SUP}	Normal and standby modes	27.66	37	48	kΩ
C_{LIN}	Capacitance of the LIN pin	V_{SUP} = 14V			25	pF
INH Output Terminal						

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5.6 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_H	High-level voltage drop of INH with respect to V_{SUP}	I_{INH} = –0.5mA		0.5	1	V
$I_{LKG(INH)}$	Leakage current sleep mode	INH = 0 V	–0.5		0.5	µA
WAKE Input Terminal						
V_{IH}	High-level input voltage	Standby and sleep mode	2.6			V
V_{IL}	Low-level input voltage				1.8	V
I_{IH}	High-level input leakage current[7]	WAKE = V_{SUP}			2.5	µA
I_{IH}		WAKE = 4V	–3			µA
I_{IL}	Low-level input leakage current[7]	WAKE = 1V			3	µA
R_{WAKE}	Pull-up/pull-down resistance[7]			600		kΩ
t_{WAKE}	WAKE hold time	Wake up time from sleep mode	5		50	µs
Duty Cycle Characteristics						
D1	Duty cycle 1[3] ISO 17987 Param 27/SAE J2602 Responder/ Commander	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7V to 18V, t_{BIT} = 50µs/52µs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT})	0.396			
$D1_{LB}$	Duty cycle 1[1][2][3][6] ISO 17987 Low Battery Param 88/SAE J2602 Responder/Commander	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 5.5V to 7V, t_{BIT} = 50µs/52µs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT})	0.396			
D2	Duty cycle 2[3] ISO 17987 Param 28/SAE J2602 Responder/ Commander	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7.6V to 18V, t_{BIT} = 50µs/52µs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT})			0.581	
$D2_{LB}$	Duty cycle 2[1][2][3][6] ISO 17987 Low Battery Param 89/SAE J2602 Responder/Commander	$TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 6.1V to 7.6V, t_{BIT} = 50µs/52µs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT})			0.581	
D3	Duty cycle 3[3] ISO 17987 Param 29/SAE J2602 Responder/ Commander	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7V to 18V, t_{BIT} = 96µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT})	0.417			
$D3_{LB}$	Duty cycle 3[1][2][3][6] ISO 17987 Low Battery Param 90/SAE J2602 Responder/Commander	$TH_{REC(MAX)}$ = 0.665 x V_{SUP} $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 5.5V to 7V, t_{BIT} = 96µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT})	0.417			
D4	Duty cycle 4[3] ISO 17987 Param 30/SAE J2602 Responder/ Commander	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7.6V to 18V, t_{BIT} = 96µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT})			0.59	
$D4_{LB}$	Duty cycle 4[1][2][3][6] ISO 17987 Low Battery Param 91/SAE J2602 Responder/Commander	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1V to 7.6V, t_{BIT} = 96µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT})			0.59	
$T_{r\text{-}d\ max}$	Transmitter propagation delay timings for the duty cycle[1][2][6] Recessive to dominant	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7V ≤ V_{SUP} ≤ 18V, t_{BIT} = 52µs $t_{REC(MAX)_D1}$ - $t_{DOM(MIN)_D1}$			10.8	µs
$T_{d\text{-}r\ max}$	Transmitter propagation delay timings for the duty cycle[1][2][6] Dominant to recessive	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.284 x V_{SUP} 7.6V ≤ V_{SUP} ≤ 18V, t_{BIT} = 52µs $t_{DOM(MAX)_D2}$ - $t_{REC(MIN)_D2}$			8.4	µs
$T_{r\text{-}d\ max}$	Transmitter propagation delay timings for the duty cycle[1][2][6] Recessive to dominant	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7V ≤ V_{SUP} ≤ 18V, t_{BIT} = 96µs $t_{REC(MAX)_D3}$ - $t_{DOM(MIN)_D3}$			15.9	µs
$T_{d\text{-}r\ max}$	Transmitter propagation delay timings for the duty cycle[1][2][6] Dominant to recessive	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7.6V ≤ V_{SUP} ≤ 18V, t_{BIT} = 96µs $t_{DOM(MAX)_D4}$ - $t_{REC(MIN)_D4}$			17.28	µs

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5.6 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{r\text{-}d\ max_low}$	Low battery transmitter propagation delay timings for the duty cycle[(1)(2)(6)] Recessive to dominant	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} 5.5V ≤ V_{SUP} ≤ 7V, t_{BIT} = 52µs $t_{REC(MAX)_low}$ - $t_{DOM(MIN)_low}$			10.8	µs
$T_{d\text{-}r\ max_low}$	Low battery transmitter propagation delay timings for the duty cycle[(1)(2)(6)] Dominant to recessive	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} 6.1V ≤ V_{SUP} ≤ 7.6V, t_{BIT} = 52µs $t_{DOM(MAX)_low}$ - $t_{REC(MIN)_low}$			8.4	µs

(1) SAE 2602 commander node load conditions: 5.5nF/4kΩ and 899pF/20kΩ; t_{BIT} = 52µs and 96µs
(2) SAE 2602 responder node load conditions: 5.5nF/875Ω and 899pF/900Ω; t_{BIT} = 52µs and 96µs
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1nF/1kΩ; 6.8nF/660Ω; 10nF/500Ω; t_{BIT} = 50µs and 96µs
(4) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage.
(5) $I_{leak\ gnd}$ = (V_{BAT} - V_{LIN})/R_{Load}
(6) Specified by design
(7) To minimize system-level current consumption, the WAKE pin will automatically configure itself based upon the applied voltage to either an internal pull-up or pull-down current source. A high-level input results in an internal pull-up and a low-level input results in an internal pull-down.

5.7 AC Switching Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31	5.5V ≤ VSUP, R_{RXD} = 2.4kΩ, C_{RXD} = 20pF			6	µs
t_{rx_pdr}	Receiver rising propagation delay time ISO 17987 Param 31				6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time ISO 17987 Param 32	Rising edge with respect to falling edge t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4kΩ, C_{RXD} = 20pF	–2		2	µs
t_{LINBUS}	Minimum dominant time on LIN bus for wake-up		25	65	150	µs
t_{CLEAR}	Time to clear false wake-up prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)		8	25	50	µs
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through EN pin	2		15	µs
t_{NOMINT}	Normal mode initialization time[(1)]	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby to normal mode.			15	µs
t_{PWR}	Power-up time	Time it takes for valid data on RXD upon power-up			1.5	ms
t_{TXD_DTO}	Dominant state time out		20	50	80	ms

(1) The transition time from sleep mode to normal mode includes both t_{MODE_CHANGE} and t_{NOMINT}.

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5.8 Typical Characteristics

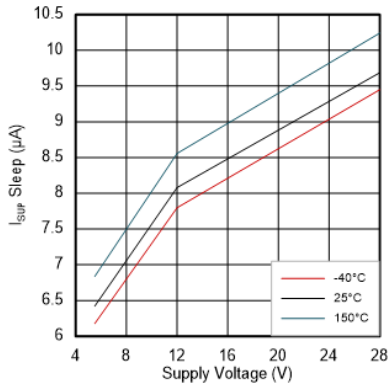

Figure 5-1. Sleep Mode I_{SUP} vs V_{SUP} and Temperature

6 Parameter Measurement Information

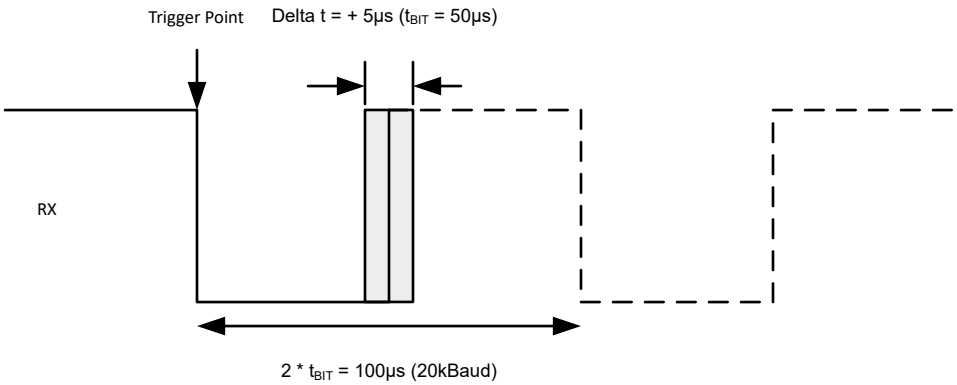

Figure 6-1. RX Response: Operating Voltage Range

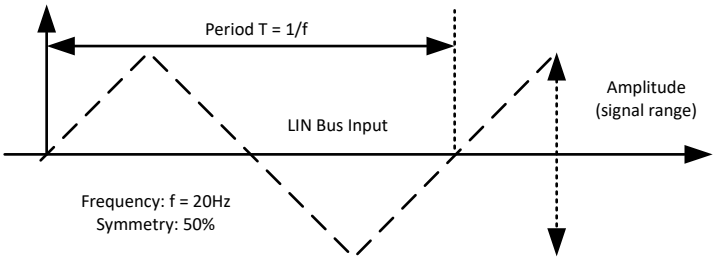

Figure 6-2. LIN Bus Input Signal

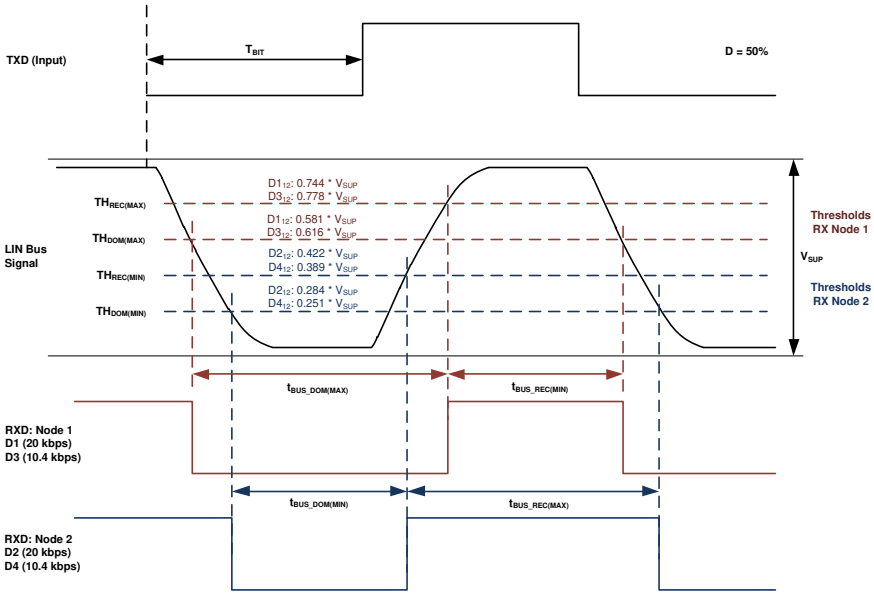

Figure 6-3. Definition of Bus Timing Parameters

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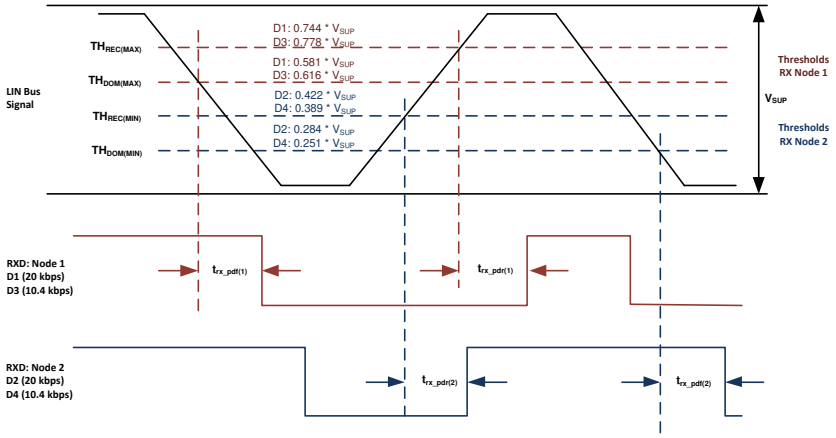

Figure 6-4. Propagation Delay

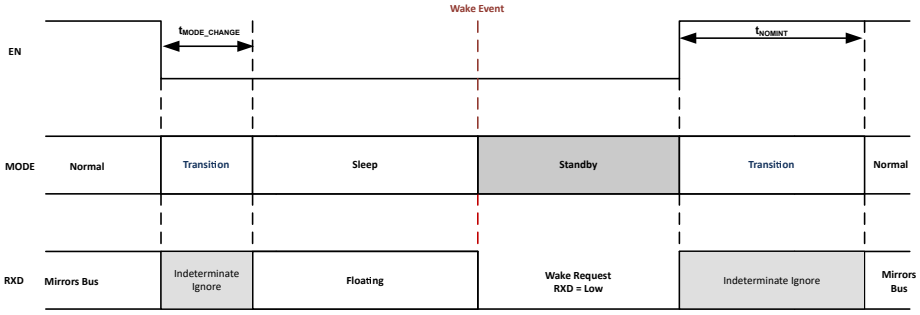

Figure 6-5. Mode Transitions

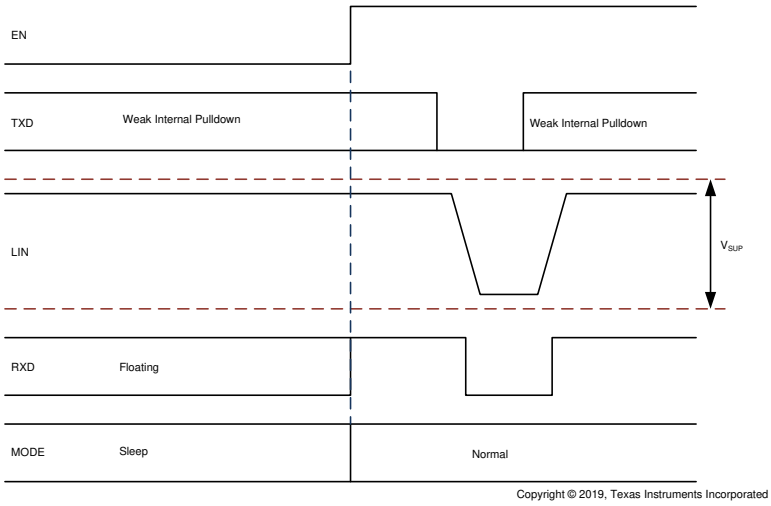

Figure 6-6. Wake-up Through EN

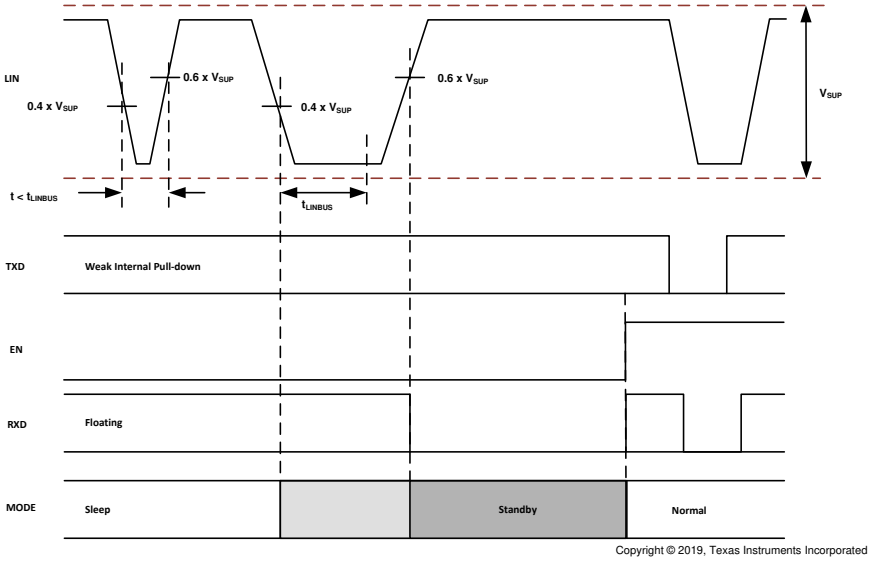

Figure 6-7. Wake-up Through LIN

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7 Detailed Description

7.1 Overview

The TLIN821-Q1 is a local interconnect network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602-1, SAE J2602-2, ISO 17987–4, and ISO 17987–7 standards. LIN is a low-speed universal asynchronous receiver transmitter (UART) communication protocol focused on automotive in-vehicle networking.

The device transmitter supports data rates from 2.4kbps to 20kbps and the receiver supports data rates up to 100kbps for end-of-line programming. The device controls the state of the LIN bus through the TXD pin and reports the state of the bus through its open-drain RXD output pin. The LIN protocol data stream on the TXD input is converted by the device into a LIN bus signal using an optimized electromagnetic emissions current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic-level signals that are sent to the microcontroller through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the transceivers internal pull-up resistor (37kΩ) and a series diode. No external pull-up components are required for responder node applications. Commander node applications require an external pull-up resistor (1kΩ) as well as a series diode per the LIN specification.

The device is designed to support 12V applications with a wide input voltage operating range and also supports low-power sleep mode. The device supports wake-up from low-power mode via wake over LIN, the WAKE pin, or the EN pin. The device allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a node through the INH output pin.

The TLIN821-Q1 integrates ESD protection and fault protection which allow for a reduction in the required external components in the applications. In the event of a ground shift or supply voltage disconnection, the device prevents back-feed current through LIN to the supply input.

The TLIN821-Q1 also include undervoltage detection, temperature shutdown protection, and loss-of-ground protection. In the event of a fault condition, the transmitter is immediately switched off and remains off until the fault condition is removed.

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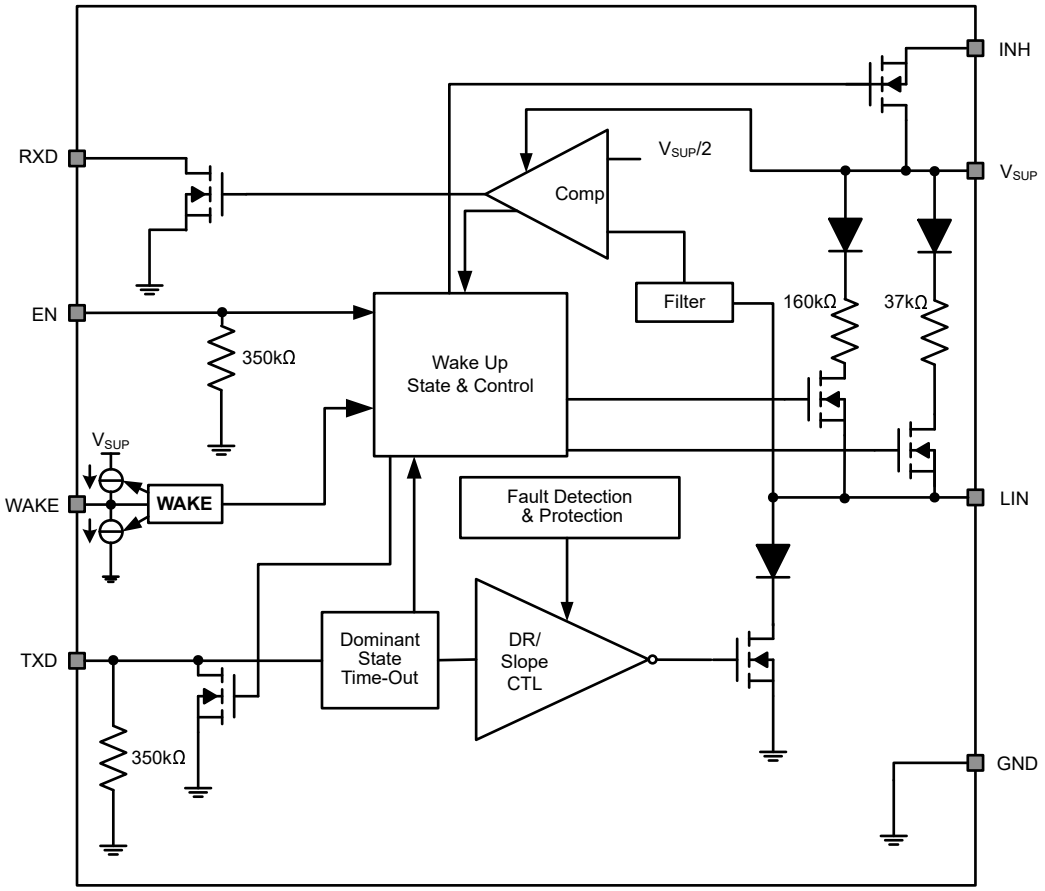
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 LIN

This high voltage input/output pin is the single-wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 40V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

7.3.1.1 LIN Transmitter Characteristics

The LIN transmitter has thresholds and AC switching parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for LIN responder node applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for in a commander node application per the LIN specification.

7.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates, > 100kbps, than supported by LIN or SAEJ2602 specifications. This allows the TLIN821-Q1 to be used for high-speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

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7.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1kΩ) and a series diode to V_{SUP} must be added when the device is used for commander node applications as per the LIN specification.

Figure 7-1 shows a commander node configuration and how the voltage levels are defined

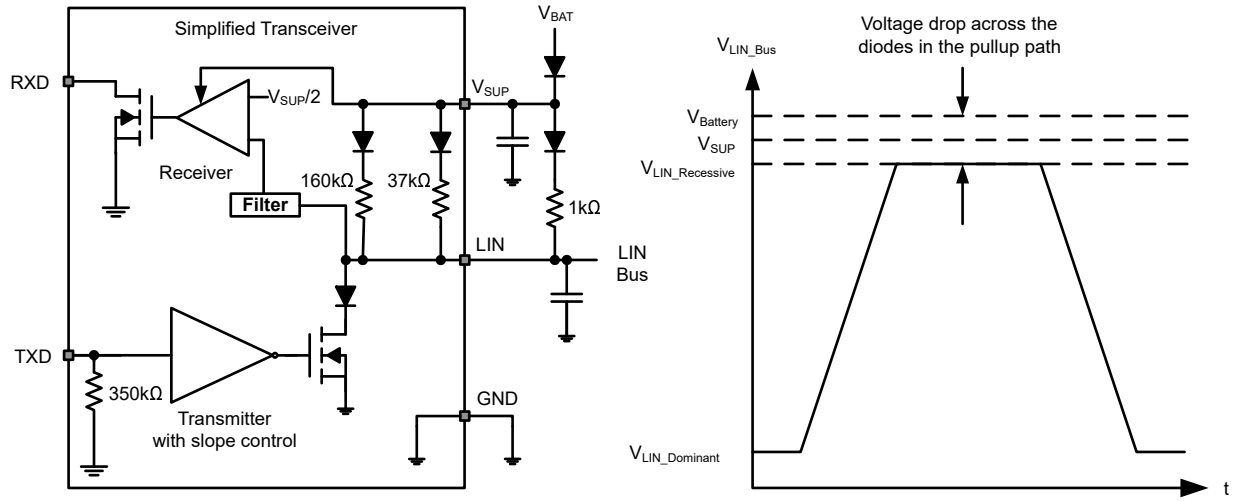

Figure 7-1. Commander Node Configuration with Voltage Levels

7.3.2 TXD

TXD is the interface to the MCU LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground) and when TXD is high the LIN output is recessive (near V_{SUP}), see Figure 7-1.

The TXD input structure is compatible with 3.3V and 5V microcontrollers and integrates a weak pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timer-out timer. When a change of state on the WAKE pin initiates a local wake-up event, the TXD pin is pulled hard to ground indicating a local wake-up event. The hard pull to ground is released upon the rising edge on the EN pin. If an external pull-up resistor is added to the TXD pin to the microcontollers IO voltage then TXD is pulled high to indicate a remote wake-up event.

7.3.3 RXD

RXD is the interface to the MCUs LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. Allowing the device to be used with 3.3V and 5V microcontrollers. If the microcontrollers RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontrollers IO supply voltage is required. In standby mode, the RXD pin is driven low to indicate a wake-up request.

7.3.4 V_{SUP}

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode, see Figure 7-1. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

7.3.5 GND

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for

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LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

7.3.6 EN

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake-up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats.

7.3.7 WAKE

The WAKE pin is a high-voltage input used for the local wake-up (LWU) function. This function is explained further in Section 7.4.4.1 section. The pin is defaulted to bidirectional edge trigger, meaning it recognizes a local wake-up (LWU) on a rising or falling edge of WAKE pin transition.

7.3.8 INH

The TLIN821-Q1 inhibit, INH, output pin can be used to control the enable of system power-management devices allowing for a significant reduction in battery quiescent current consumption while the application is in sleep mode. The INH pin has two states: driven high and high impedance. When the INH pin is driven high, the terminal shows V_{SUP} minus a diode voltage drop. In the high impedance state, the output is left floating. The INH pin is high in the normal and standby modes and is low when in sleep mode. A 100kΩ load can be added to the INH output to ensure a fast transition time from the driven high state to the low state and to also force the pin low when left floating.

The INH terminal must be considered a high-voltage logic terminal and not a power output. Thus, must be used to drive the EN terminal of the systems power-management device and not used as a switch for the power-management supply. This terminal is not reverse battery protected, and must not be connected outside the system module.

7.3.9 Local Faults

The TLIN821-Q1 has several protection features that are described as follows.

7.3.10 TXD Dominant Time-Out (DTO)

While the LIN driver is in active mode a TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit, t_{TXD_DTO}, expires the LIN driver is disabled releasing the bus line to the recessive level. This keeps the bus free for communication between other nodes on the network. The LIN driver is re-activated on the next dominant to recessive transition on the TXD terminal, thus clearing the dominant time-out. During this fault, the transceiver remains in normal mode, the integrated LIN bus pull-up termination remains on, and the LIN receiver and RXD terminal remain active reflecting the LIN bus data.

The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. If EN pin is high at power-up, the TLIN821-Q1 enters normal mode. With the internal TXD connected low, the DTO timer starts. To avoid a t_{TXD_DTO} fault, a recessive signal must be put onto the TXD pin before the t_{TXD_DTO} timer expires, or the device must be into sleep mode by connecting EN pin low.

7.3.11 Bus Stuck Dominant System Fault: False Wake-Up Lockout

The TLIN821-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus clears the bus stuck dominant fault, preventing excessive current use, see Figure 7-2 and Figure 7-3.

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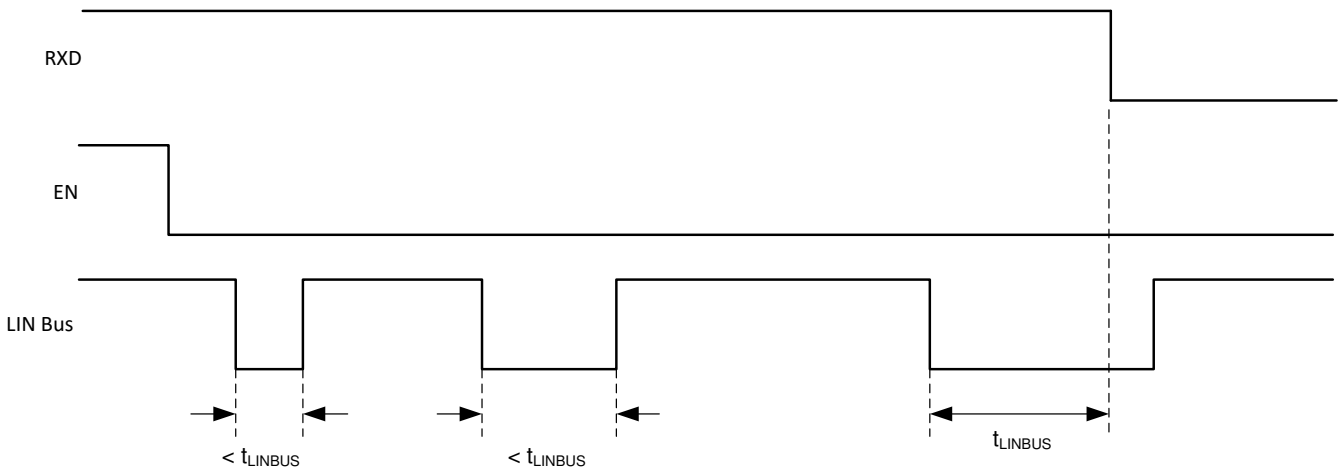

Figure 7-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake-up

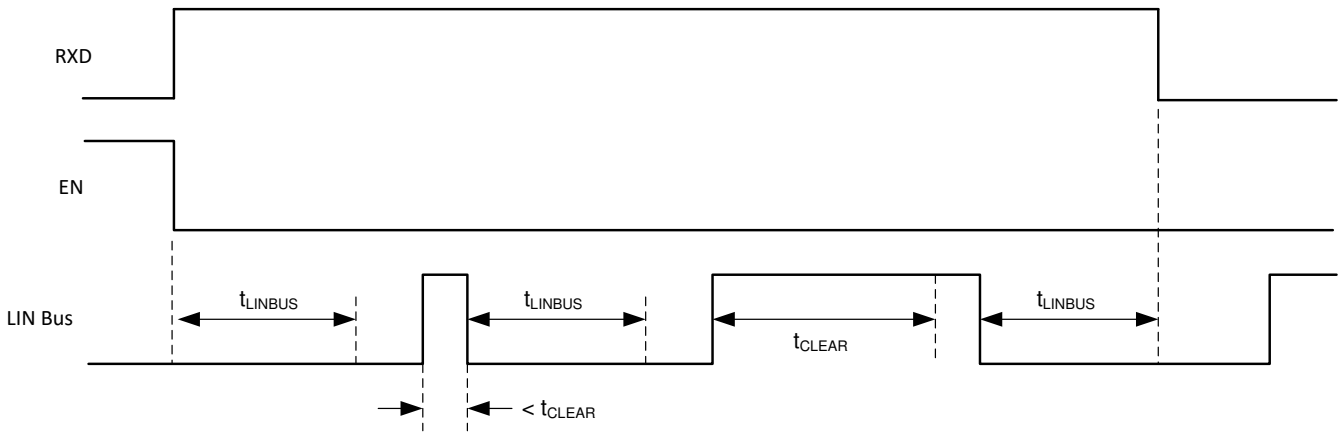

Figure 7-3. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wake-up

7.3.12 Thermal Shutdown

The TLIN821-Q1 transmitter is protected by limiting the current. If the junction temperature, T_J, of the device exceeds the thermal shutdown threshold, $T_J > T_{SDR}$, the device puts the LIN transmitter into the recessive state. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled. During this fault, the transceiver remains in normal mode, the integrated LIN bus pull-up termination remains on, the LIN receiver and RXD terminal remain active reflecting the LIN bus data.

7.3.13 Under Voltage on V_{SUP}

The device contains a power on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

7.3.14 Unpowered Device

In automotive applications, some LIN nodes in a system can be unpowered, ignition supplied, while others in the network remains powered by the battery. The device has low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down.

7.4 Device Functional Modes

The TLIN821-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections describe these modes and how the device transitions between the different modes. Figure 7-4 graphically shows the relationship while Table 7-1 shows the state of pins.

Table 7-1. Operating Modes

MODE	EN	TXD	RXD	INH	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Weak pull-down	Floating	Floating	Weak current pull-up	Off	
Standby	Low	weak pull-down if LIN bus wake-up; Strong pull-down if a local wake-up event (WAKE pin)	Low	High	37kΩ	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	High: recessive state Low: dominant state	LIN Bus Data	High	37kΩ	On	LIN transmission up to 20kbps

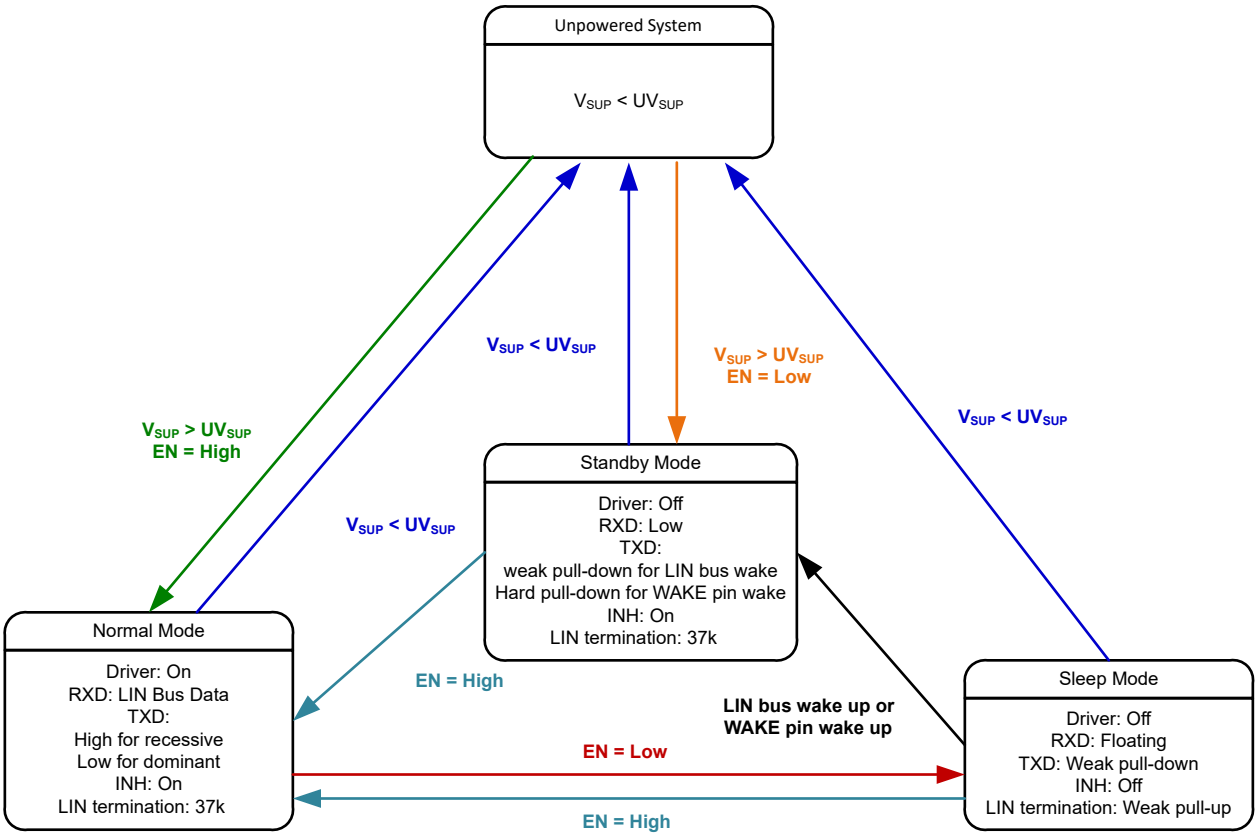

Figure 7-4. Operating State Diagram

7.4.1 Normal Mode

The EN pin controls the mode of the device. If the EN pin is high at power-up, the device powers-up in normal mode. If the EN is low at power-up, the device powers-up in standby mode. In normal mode, the receiver and transmitter are fully operational. The LIN transmitter transmits data from the LIN controller to the LIN bus up to the LIN specified maximum data rate of 20kbps. The LIN receiver detects the data stream on the LIN bus up to data rates of 100kbps, and outputs the data on RXD output for the LIN controller. Upon an EN pin transition from low to high, the TLIN821-Q1 transitions from sleep mode to normal mode in $t \geq t_{NOMINT}$.

7.4.2 Sleep Mode

Sleep mode is the lowest power mode of the TLIN821-Q1, and is only entered from normal mode when the EN pin transitions from high to low for $t > t_{MODE_CHANGE}$. In sleep mode, the LIN driver and receiver are switched off, the LIN bus is weakly pulled up, an the transceiver cannot send or receive data. The INH pin is switched to a floating output in sleep mode causing any system power elements controlled by the INH pin to be switched off thus reducing the system power consumption. While the device is in sleep mode, the following conditions exist:

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- The LIN bus driver is disabled and the internal LIN bus termination is switched off to minimize power loss if LIN is short circuited to ground.
- A weak current pull-up is active to prevent false wake-up events when an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input, WAKE pin and LIN wake-up receiver are active.

The TLIN821-Q1 supports three methods for wake-up from sleep mode:

- Wake-up over the LIN bus via the LIN wake-up receiver.
- Local wake-up via the WAKE pin.
- Local wake-up via the EN pin. The EN pin must be set high for $t > t_{NOMINT}$ for the device to wake-up.

7.4.3 Standby Mode

Standby mode is entered when a wake-up event occurs through LIN bus or the WAKE pin while the device is in sleep mode. In standby mode, the LIN bus responder termination circuit, 37kΩ, is on. When a wake-up event occurs and the TLIN821-Q1 enters standby mode the RXD pin is driven low signaling the wake-up event to the LIN controller.

The device exits standby mode and transitions to normal mode when the EN pin is set high for longer than t_{MODE_CHANGE}. The normal LIN transmitter and receiver are fully operational, and bi-directional communication is possible.

7.4.4 Wake-Up Events

There are three ways to wake-up the TLIN821-Q1 from sleep mode:

1. Remote wake-up initiated by the falling edge of a recessive-to-dominant state transition on the LIN bus where the dominant state is be held than t_{LINBUS} filter time. After the t_{LINBUS} filter time has been met, a rising edge on the LIN bus going from dominant-to-recessive initiates a remote wake-up event. The pattern and t_{LINBUS} filter time used for the LIN wake-up prevents noise and bus stuck dominant faults from causing false wake requests.
2. A local wake-up event due to the EN pin being set high for $t > t_{MODE_CHANGE}$.
3. A local wake-up event due to a change in voltage level on the WAKE pin for $t > t_{WAKE}$.

7.4.4.1 Local Wake-Up (LWU) using the WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage input which can be used for local wake-up (LWU) requests through a voltage transition. An LWU event is triggered on either a low-to-high or high-to-low transition since it has bi-directional input thresholds. The WAKE pin can be used with a switch to V_{SUP} or to ground. If the terminal is unused, pull it to V_{SUP} or ground to avoid unwanted parasitic wake-up events. When an LWU event takes place, the TXD pin is pulled hard to GND letting the LIN controller know that the wake-up event is due to the WAKE pin, and not a wake over LIN event.

The LWU circuitry is active in standby mode and sleep mode. If a valid LWU event occurs in standby mode, the device remains in standby mode and drive the RXD output low. If a valid LWU event occurs in sleep mode, the device transitions to standby mode and drive the RXD output low. The LWU circuitry is not active in normal mode. To minimize system level current consumption, the internal bias voltages of the terminal follows the state on the terminal with a delay of $t_{WAKE(MIN)}$. A constant high level on WAKE has an internal pull-up to V_{SUP}, and a constant low level on WAKE has an internal pull-down to GND.

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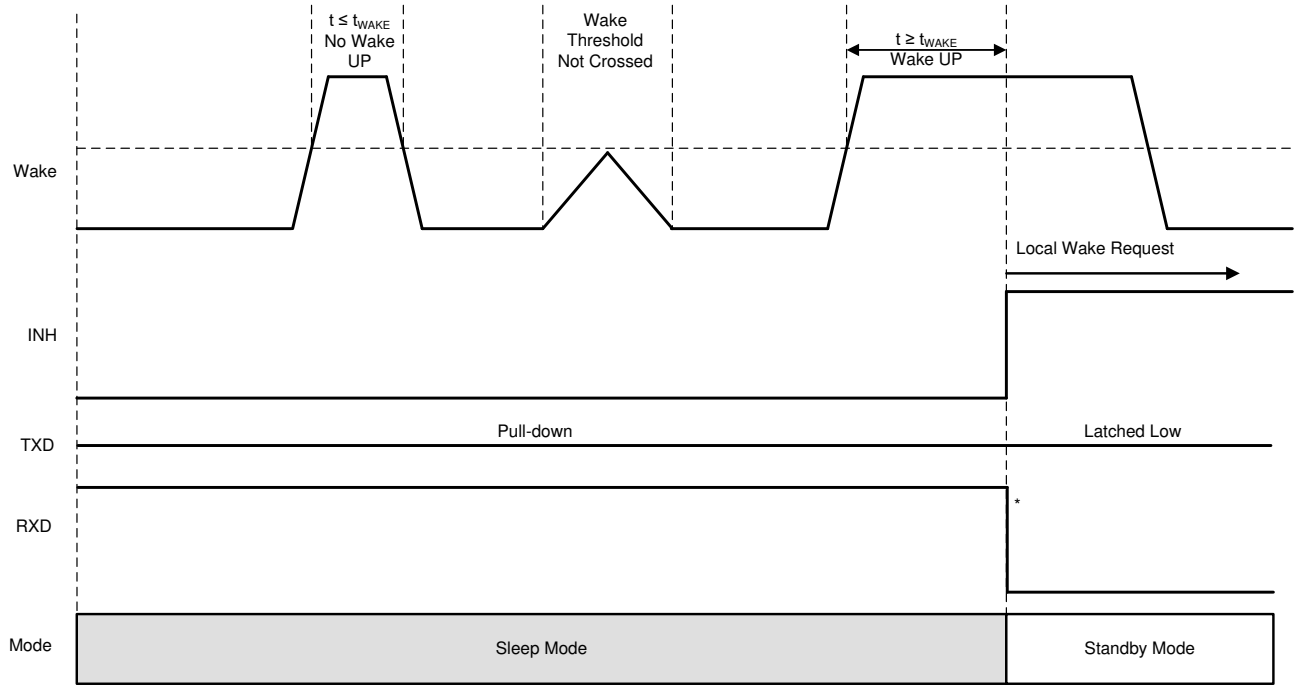

Figure 7-5. Local Wake-up – Rising Edge

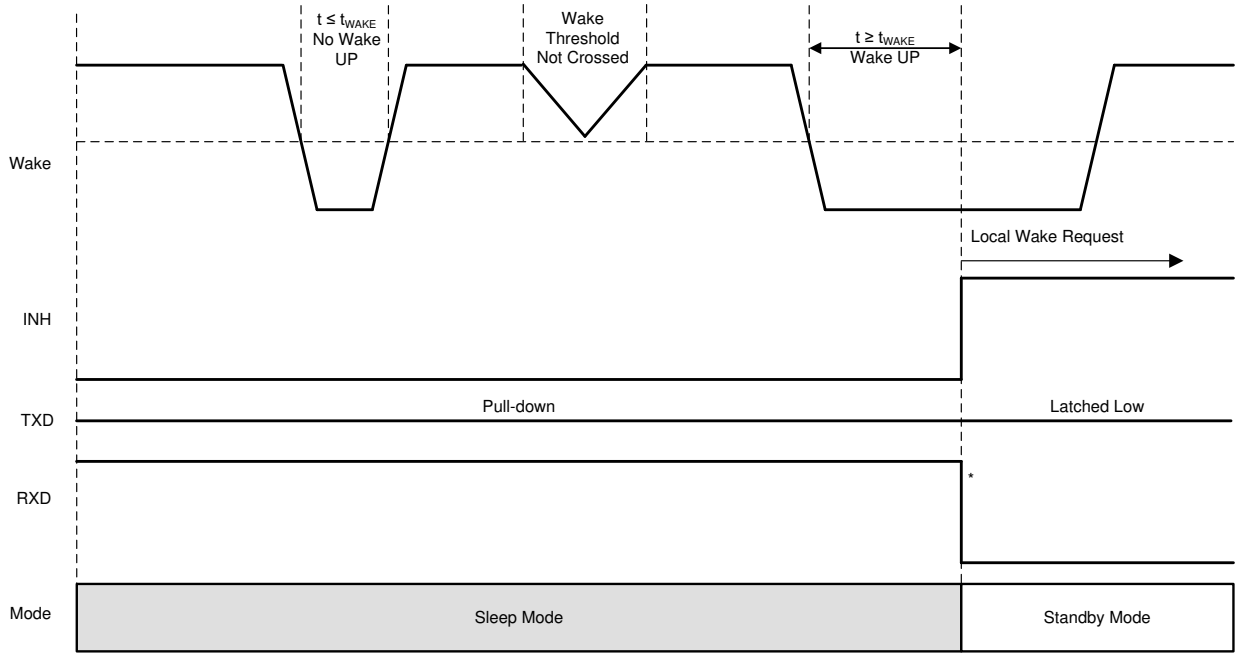

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Figure 7-6. Local Wake-up – Falling Edge

7.4.4.2 Wake-Up Request (RXD)

When the TLIN821-Q1 encounters a wake-up event from the WAKE pin or the LIN bus, the RXD output is driven low until EN is asserted high. The device enters normal mode. Once the device enters normal mode, the wake-up event is cleared, and the RXD output is released. The RXD output is fully operation and reflects the receiver output from the LIN bus.

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8 Application Information Disclaimer

Note

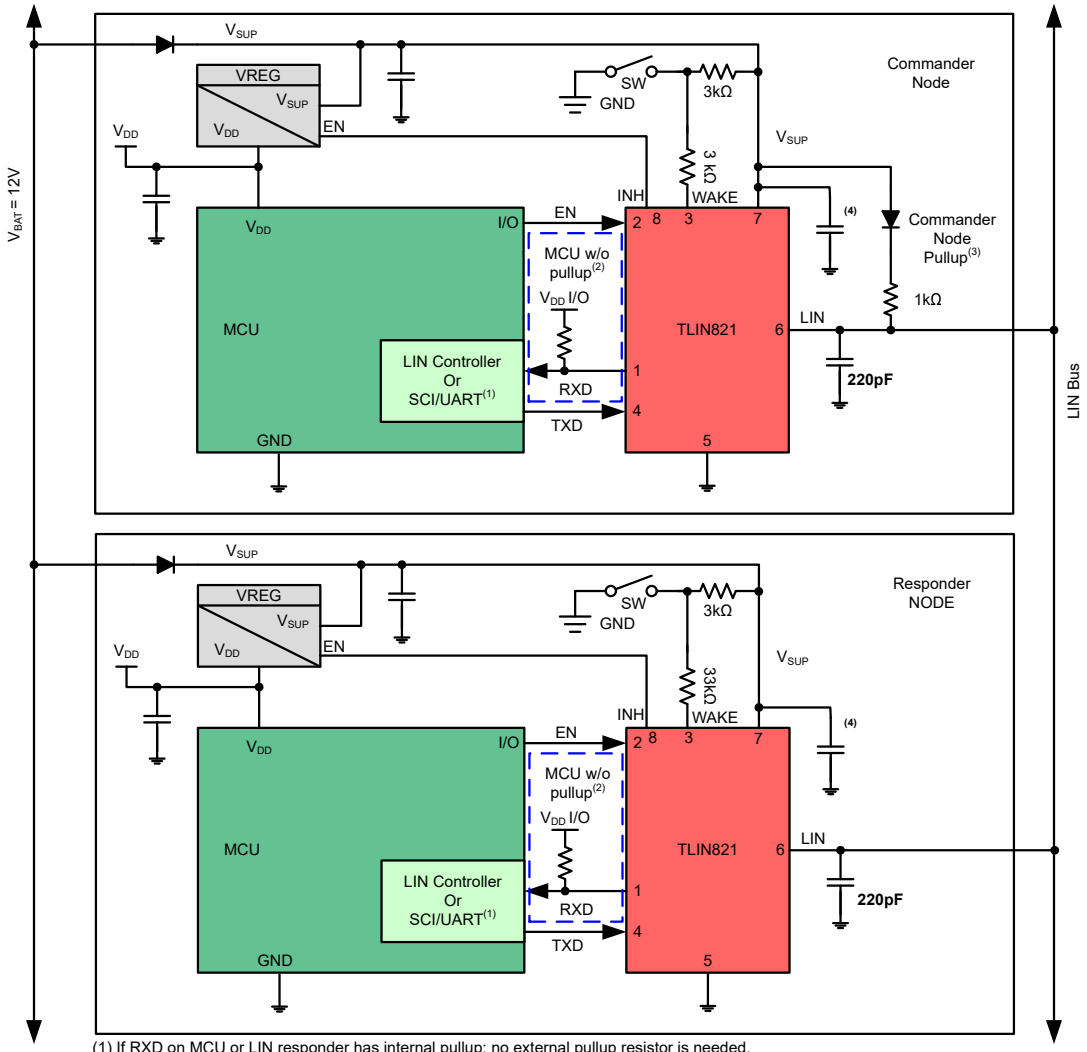
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLIN821-Q1 can be used in both a responder node application and a commander node application in a LIN network.

8.2 Typical Application

The device integrates a 37kΩ pull-up resistor and series diode for responder node applications. For commander node applications, an external 1kΩ pull-up resistor with series blocking diode can be used. Figure 8-1 shows the device being used in both commander node and responder node applications.



(1) If RXD on MCU or LIN responder has internal pullup; no external pullup resistor is needed.
(2) If RXD on MCU or LIN responder does not have an internal pullup requires external pullup resistor.
(3) Commander node applications require and external 1kΩ pullup resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100nF, 1µF and ≥10µF

Figure 8-1. Typical LIN Bus

8.2.1 Design Requirements

The RXD output structure is an open-drain output stage which allows the TLIN821-Q1 to be used with 3.3V and 5V controllers. If the RXD pin of the controller does not have an integrated pull-up, an external pull-up resistor to the controllers IO voltage is required. The external pull-up resistor value must be from 1kΩ to 10kΩ. The V_{SUP} pin of the device must be decoupled with a 100nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

8.2.2 Detailed Design Procedures

8.2.2.1 Normal Mode Application Note

When using the TLIN821-Q1 in systems which are monitoring the RXD pin for a wake-up request, be very cautious during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software must not look for an edge on the RXD pin indicating a wake-up request until t_{MODE_CHANGE} has been met. This is shown in Figure 6-5

8.2.2.2 TXD Dominant State Time-Out Application Note

The maximum dominant TXD time allowed by the TXD dominant state time-out limits the minimum possible data rate of the device. The LIN protocol has different constraints for commander node and responder node applications thus there are different maximum consecutive dominant bits for each application case thus different minimum data rates.

8.2.2.3 Standby Mode Application Note

If the TLIN821-Q1 detects an under voltage on V_{SUP} the RXD pin transitions low signaling to the controller that the TLIN821-Q1 is in standby mode. Return the transceiver to sleep mode for the lowest power state.

8.2.3 Application Curves

Figure 8-2 and Figure 8-3 show the propagation delay from the TXD pin to the LIN pin for the dominant to recessive and recessive to dominant edges. The device is configured in commander mode with external pull-up resistor (1kΩ) and 680pF bus capacitance.

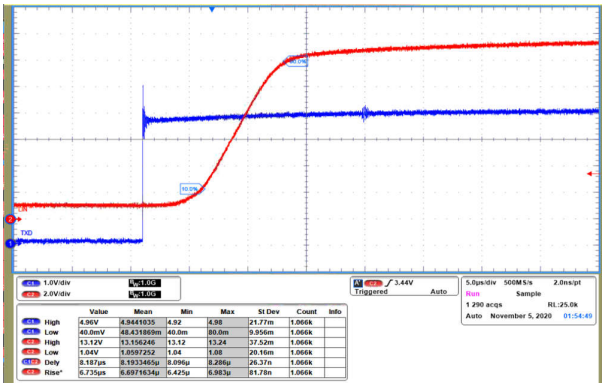


Figure 8-2. Dominant to Recessive Propagation Delay

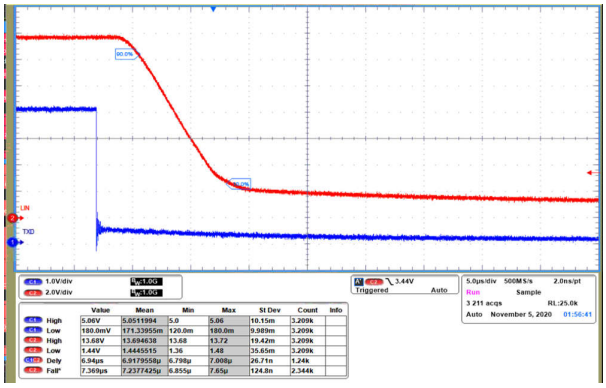


Figure 8-3. Recessive to Dominant Propagation Delay

8.3 Power Supply Recommendations

The TLIN821-Q1 is designed to operate directly from a car battery, or any other DC supply ranging from 5.5V to 28V. The V_{SUP} pin of the device must be decoupled with a 100nF capacitor by placing it close to the V_{SUP} supply pin. The system must include additional decoupling on the V_{SUP} line as needed per the application requirements.

8.4 Layout

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high frequency layout

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techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

8.4.1 Layout Guidelines

- **Pin 1(RXD):** The RXD pin is an open-drain output and requires and external pull-up resistor in the range of 1kΩ and 10kΩ to function properly. If the controller paired with the transceiver does not have an integrated pull-up, place an external resistor between RXD and the supply voltage for the controller.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in low-power sleep mode. If this feature is not used, connect the pin to the supply voltage for the controller through a series resistor using a pull-up value between 1kΩ and 10kΩ. Additionally, a series resistor can be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (WAKE):** SW1 is oriented in a low-side configuration which is used to implement a local WAKE event. The series resistor R5 is needed for protection against over current conditions as it limits the current into the WAKE pin when the ECU has lost its ground connection. The pull-up resistor R4 is required to provide sufficient current during stimulation of a WAKE event. In this layout example R4 is set to 3kΩ and R5 is set to 33kΩ.
- **Pin 4 (TXD):** The TXD pin is the transmit input signal to the device from the controller. A series resistor can be placed to limit the input current to the device due to an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to help filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin must be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** The LIN pin connects to the TLIN821-Q1 to the LIN bus. For responder node applications, a 220pF capacitor to ground is implemented. For commander node applications, an additional series resistor and blocking diode must be placed between the LIN pin and the V_{SUP} pin, see Typical LIN Bus.
- **Pin 7 (V_{SUP}):** This is the supply pin for the device. A 100nF capacitor must be placed close to the V_{SUP} supply pin for local power supply decoupling.
- **Pin 8 (INH):**The INH pin is used for system power-management. A 100kΩ load can be added to the INH output to make sure a fast transition time from the driven high state to the low state, and to force the pin low when left floating.

Note

Make all ground and power connections as short as possible and use at least two vias to minimize the total loop inductance.

8.4.2 Layout Example

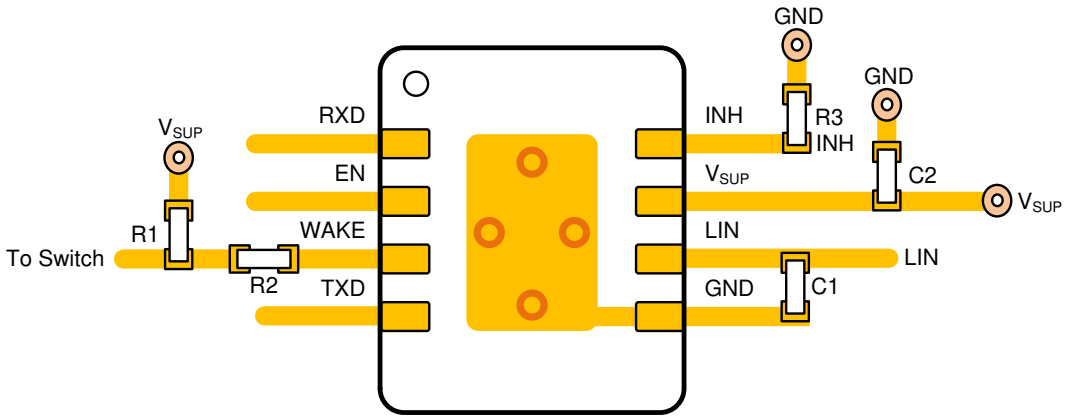

Figure 8-4. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2026) to Revision A (October 2026) — **Page**

- Updated datasheet status from *Advanced Information* to *Production Data* 1
- Removed junction temperature specification while in sleep/standby mode 4
- Removed *ESD Ratings - IEC Specification* 4
- Added *Typical Characteristics* 9
- Added D1 - D4 threshold information in *Parameter Measurement Information* 10
- Updated internal pullup resistor value on visual diagrams to 350kΩ from 500kΩ 14
- Updated threshold name in state diagram in *Device Functional Modes* to UV_{SUP} from V_{SUP_UNDER} 17
- Corrected supply voltage in *Power Supply Recommendations* to 28V from -18V 22

DATE	REVISION	NOTES
March 2026	*	Initial release.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTLIN821DRBRQ1	Active	Preproduction	SON (DRB) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTLIN821DRQ1	Active	Preproduction	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLIN821DRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL821

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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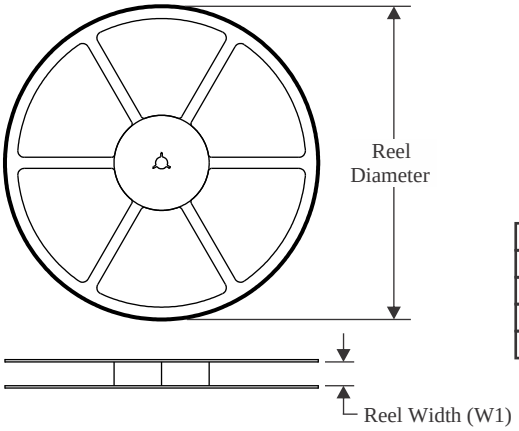
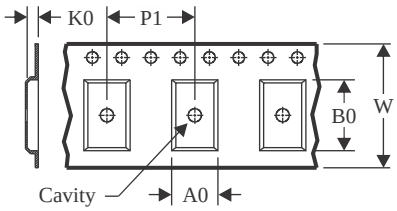
TAPE AND REEL INFORMATION

REEL DIMENSIONS

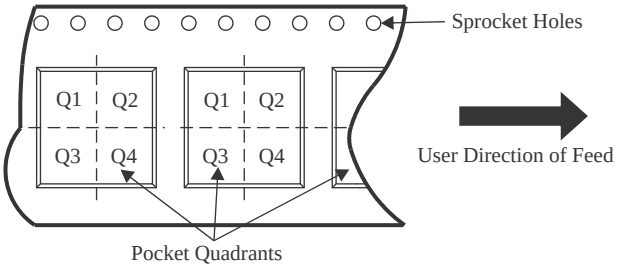


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

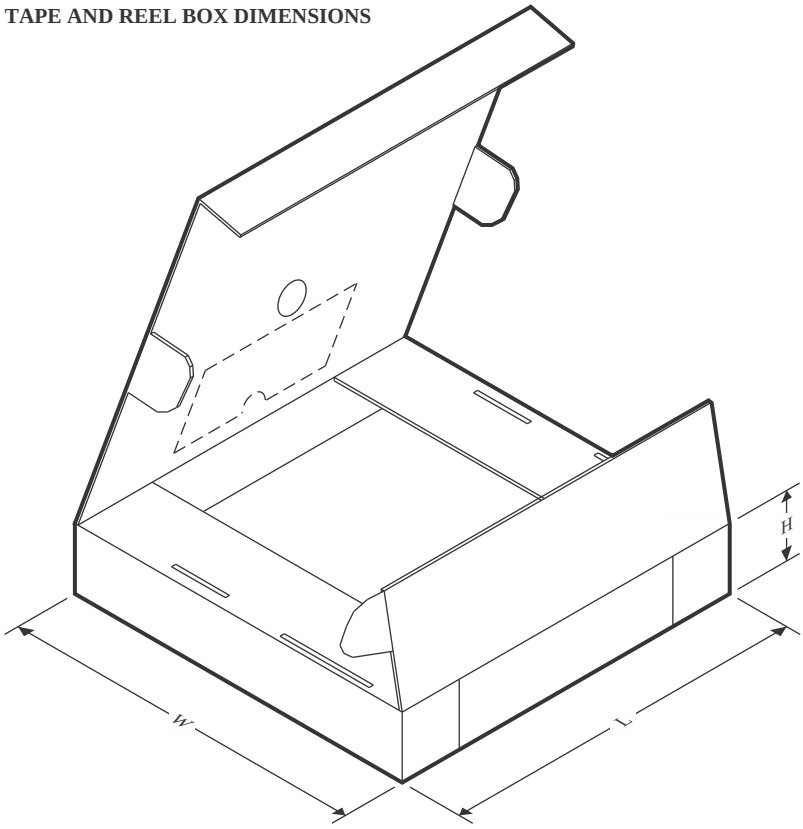
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN821DRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN821DRQ1	SOIC	D	8	2500	340.5	338.1	20.6

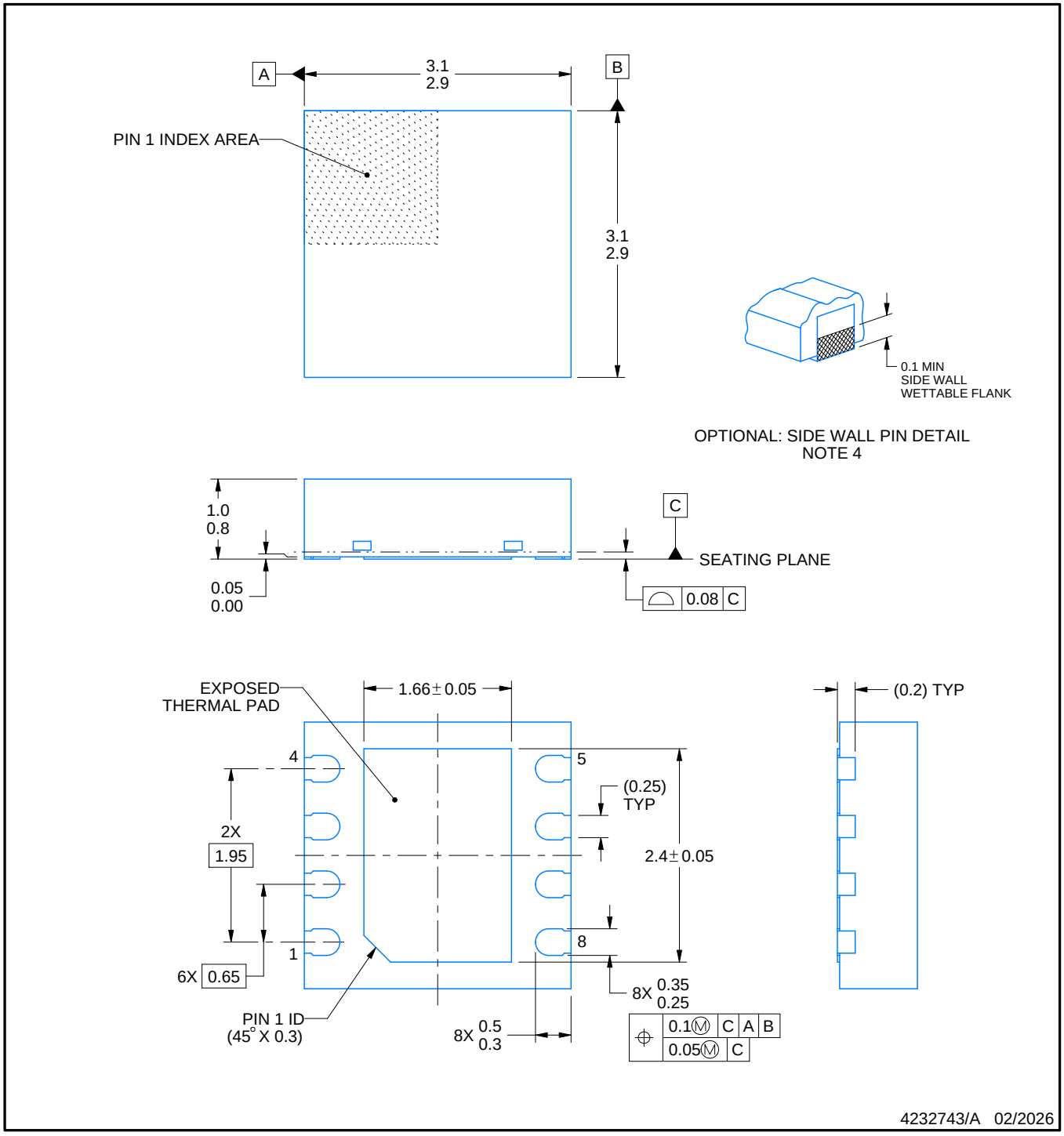
GENERIC PACKAGE VIEW

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

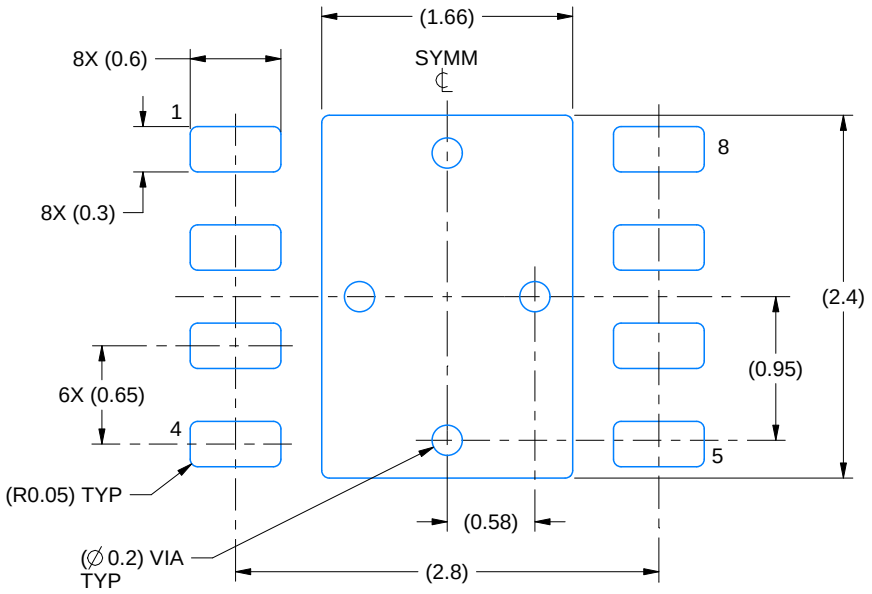
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

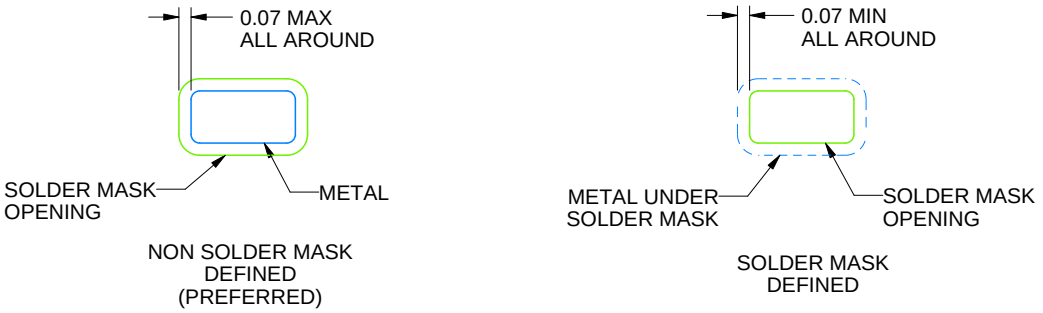


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:20X

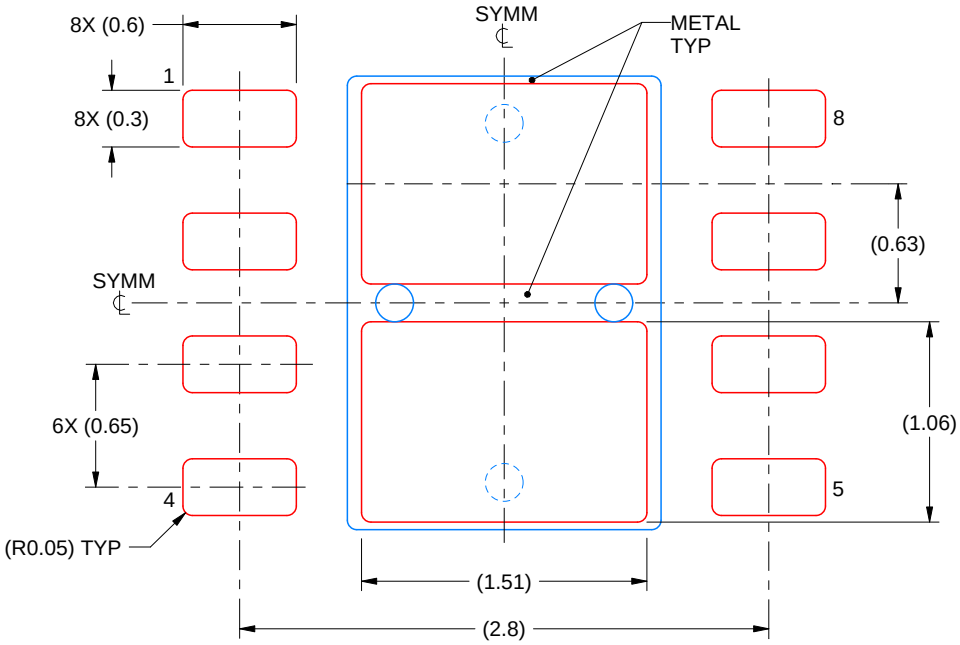


SOLDER MASK DETAILS

4232743/A 02/2026

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



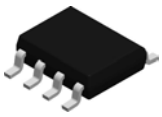
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4232743/A 02/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

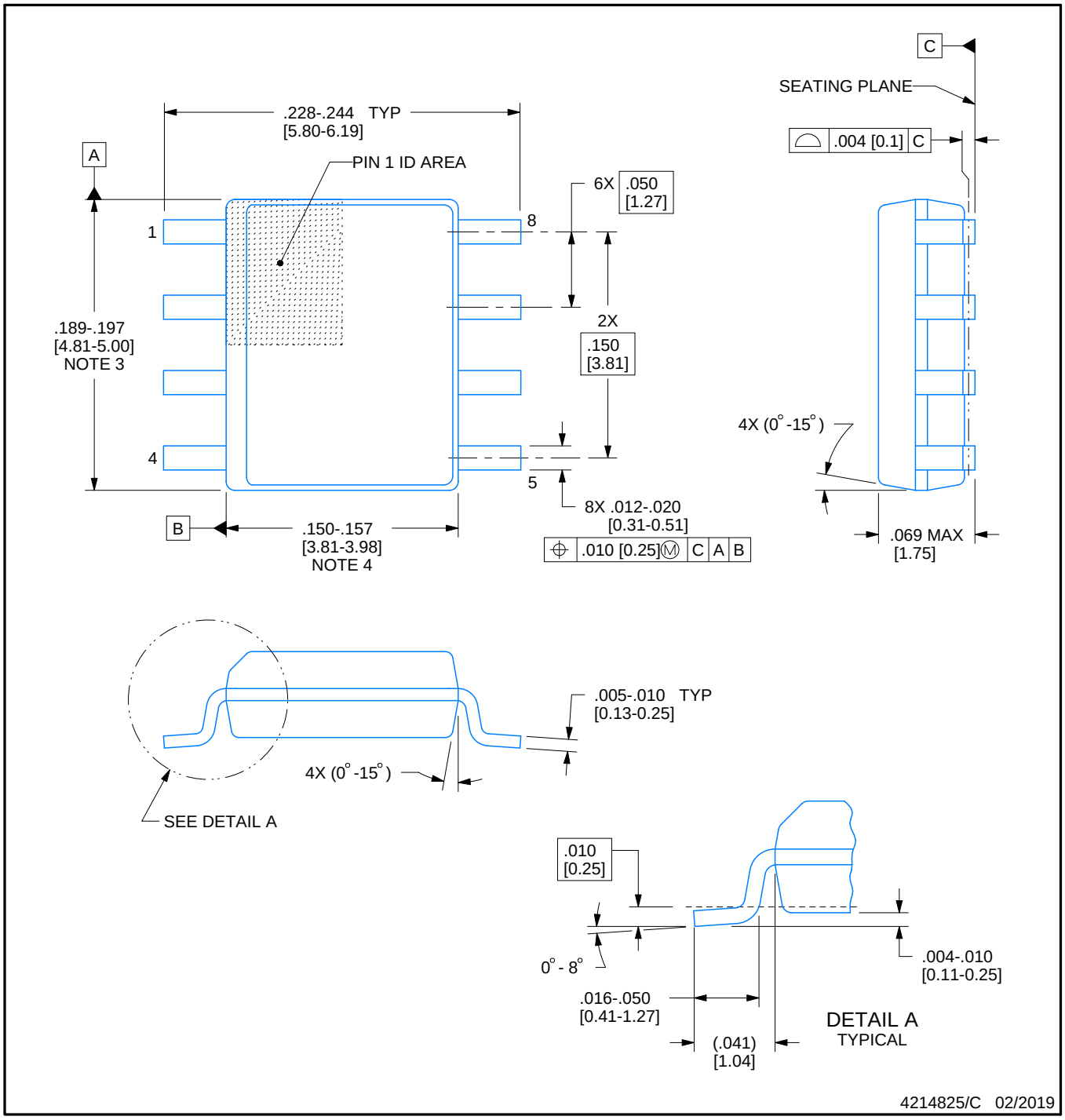


PACKAGE OUTLINE

D0008A

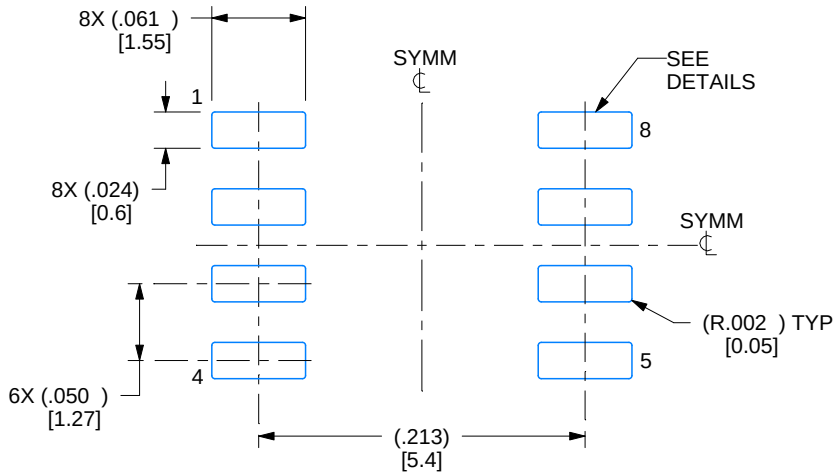
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

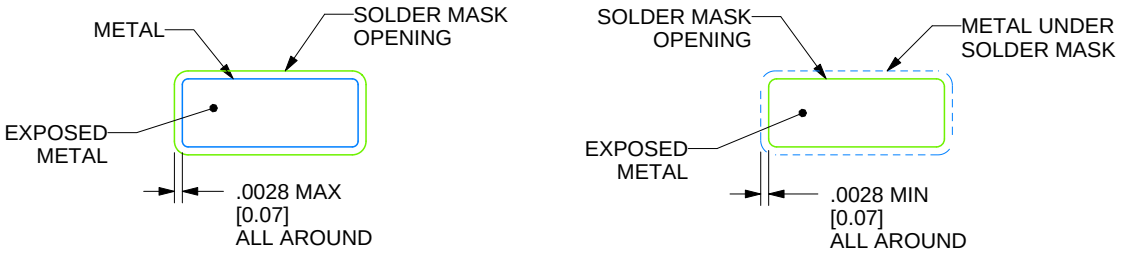


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

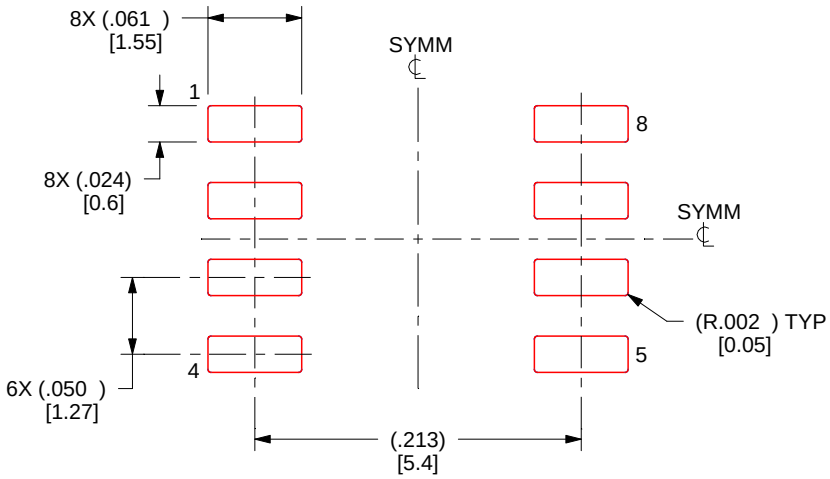


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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