MCF8315D Sensorless Field Oriented Control (FOC) Integrated FET BLDC Driver

1 Features

- Three-phase BLDC motor driver with integrated sensorless motor control algorithm
  - Code-free Field Oriented Control (FOC)
  - Speed, current, power and voltage control
  - Forward and reverse windmilling support
  - Configurable power and speed limit
  - Lead angle adjustment for high efficiency
  - Improved acoustic performance with soft-start, soft-stop and dead time compensation
  - Offline motor parameter measurement with Motor Parameter Extraction Tool (MPET)
  - Analog, PWM, freq. or I^2C based speed input
  - Configurable motor start-up and stop options
  - Flux weakening for high speed operation
  - Anti-voltage surge (AVS) protection
  - Variable monitoring through DACOUT pins
- 4.5 to 35V operating voltage (40V abs max)
- High output current capability: 4A peak
- Low MOSFET on-state resistance
  - RGF: $R_{DS(ON)}$(H+L) at T_J=25°C: 240mΩ(typ.)
  - RRY: $R_{DS(ON)}$(H+L) at T_J=25°C: 250mΩ(typ.)
  - PWP: $R_{DS(ON)}$(H+L) at T_J=25°C: 265mΩ(typ.)
- Low power sleep mode: Refer Table 6-8
  - 5µA (maximum) at V_{VM} = 24V, T_A = 25°C
- Speed loop accuracy: 3% with internal clock and 1% with external clock reference
- Configurable EEPROM with R/W security to store device configuration
- Does not require external current sense resistors; uses built-in current sensing
- Built-in 3.3V, 20mA LDO regulator
- Built-in 3.3V/5V, 170mA buck regulator
- Dedicated DRVOFF pin to disable (Hi-Z) outputs
- Spread spectrum, PWM dithering and slew rate for EMI reduction
- Suite of integrated protection features
  - Supply under voltage lockout (UVLO)
  - Supply over voltage protection (OVP)
  - Motor lock detection
  - Configurable current limit
  - Thermal warning and shutdown (OTW/TSD)
  - Fault condition indication pin (nFAULT)
  - Optional fault diagnostics over I^2C interface

2 Applications

- Brushless-DC (BLDC) Motor Modules
- Washer and Dishwashers Pumps
- Air Purifiers and Humidifier Fans
- Small Home Appliances
- Residential and Living Fans

3 Description

The MCF8315D provides a single-chip, code-free sensorless FOC device for customers driving speed-controlled 12 to 24V brushless-DC motors (BLDC) or Permanent Magnet Synchronous motor (PMSM) up to 4A peak current. The MCF8315D integrates three ½-bridges with 40V absolute maximum capability and a very low $R_{DS(ON)}$ of 240/250/265mΩ (high-side + low-side FETs). MCF8315D integrates power management circuits including a voltage-adjustable buck regulator (3.3V/5V,170mA) and LDO (3.3V, 20mA) that can be used to power external circuits.

The FOC algorithm configuration can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once the device has been configured. The device receives a speed command through a PWM input, analog voltage, variable frequency square wave, or I^2C command. There are a large number of protection features integrated into the MCF8315D, is intended to protect the device, motor, and system against fault events.

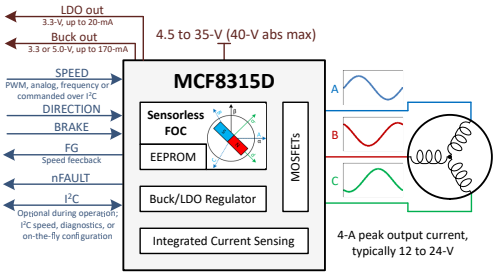
Device Information [1]

PART NUMBER	PACKAGE	PACKAGE SIZE [2]
MCF8315DVPWPR	HTSSOP (24)	7.80mm x 6.40mm
MCF8315DULVPWPR [3]	HTSSOP (24)	7.80mm x 6.40mm
MCF8315DVRGFR [3]	VQFN (40)	7.00mm x 5.00mm
MCF8315DULVRGFR [3]	VQFN (40)	7.00mm x 5.00mm
MCF8315DVRRYR [3]	WQFN (32)	6.00mm x 4.00mm
MCF8315DULVRRYR [3]	WQFN (32)	6.00mm x 4.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) Device available for preview only

Documentation for reference:

- Refer MCF8315D EVM User's Guide
- Refer to the MCF8315D EVM GUI



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....7
5.1 Absolute Maximum Ratings....7
5.2 ESD Ratings....7
5.3 Recommended Operating Conditions....7
5.4 Thermal Information....8
5.5 Electrical Characteristics....8
5.6 Characteristics of the SDA and SCL bus for Standard and Fast mode....14
6 Detailed Description....16
6.1 Overview....16
6.2 Functional Block Diagram....17
6.3 Feature Description....20
6.4 Device Functional Modes....88
6.5 External Interface....89
6.6 EEPROM access and I^2C interface....91
7 EEPROM (Non-Volatile) Register Map....98
7.1 Algorithm_Configuration Registers....98
7.2 Fault_Configuration Registers....129
7.3 Hardware_Configuration Registers....139
7.4 Internal_Algorithm_Configuration Registers....153
8 RAM (Volatile) Register Map....158
8.1 Fault_Status Registers....158
8.2 System_Status Registers....163
8.3 Device_Control Registers....167
8.4 Algorithm_Control Registers....168
8.5 Algorithm_Variables Registers....180
9 Application and Implementation....218
9.1 Application Information....218
9.2 Typical Applications....218
9.3 Power Supply Recommendations....224
9.4 Layout....225
10 Device and Documentation Support....228
10.1 Support Resources....228
10.2 Trademarks....228
10.3 Electrostatic Discharge Caution....228
10.4 Glossary....228
11 Revision History....228
12 Mechanical, Packaging, and Orderable Information....228

Copyright © 2025 Texas Instruments Incorporated

4 Pin Configuration and Functions

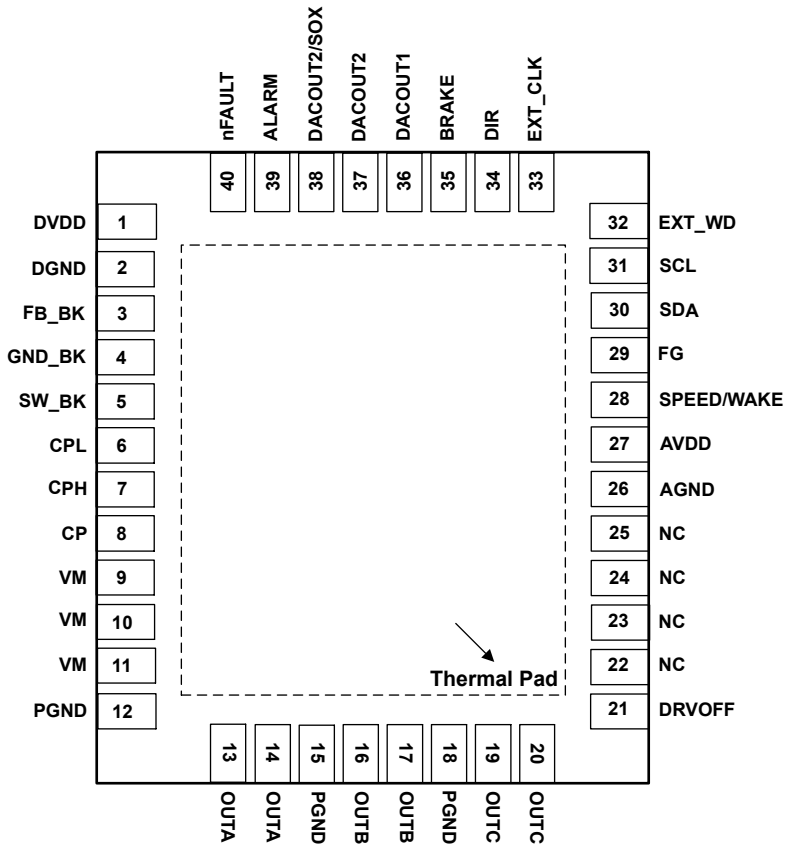


Figure 4-1. MCF8315D, 40-Pin VQFN With Exposed Thermal Pad, Top View

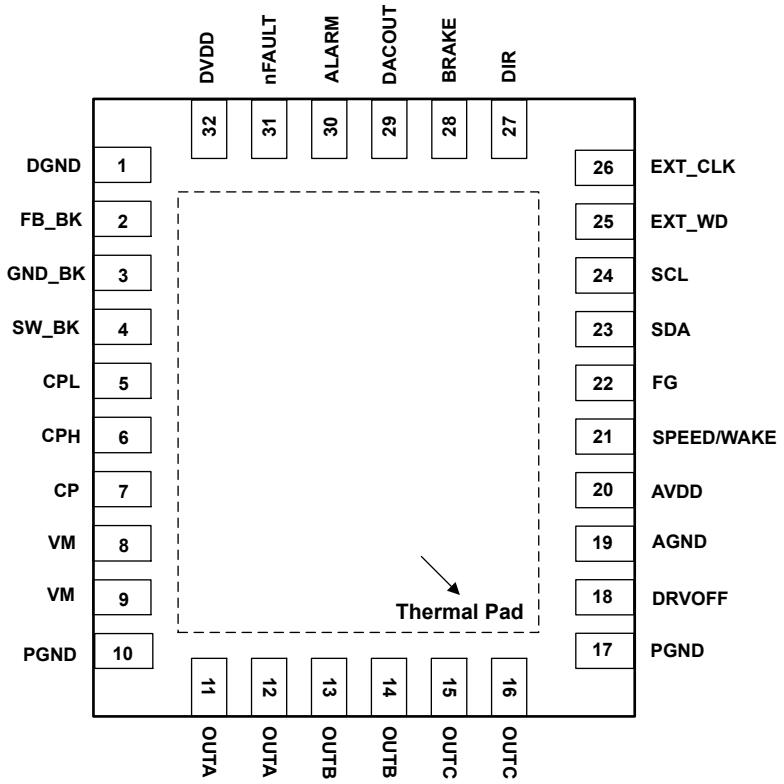


Figure 4-2. MCF8315D, 32-Pin WQFN With Exposed Thermal Pad, Top View

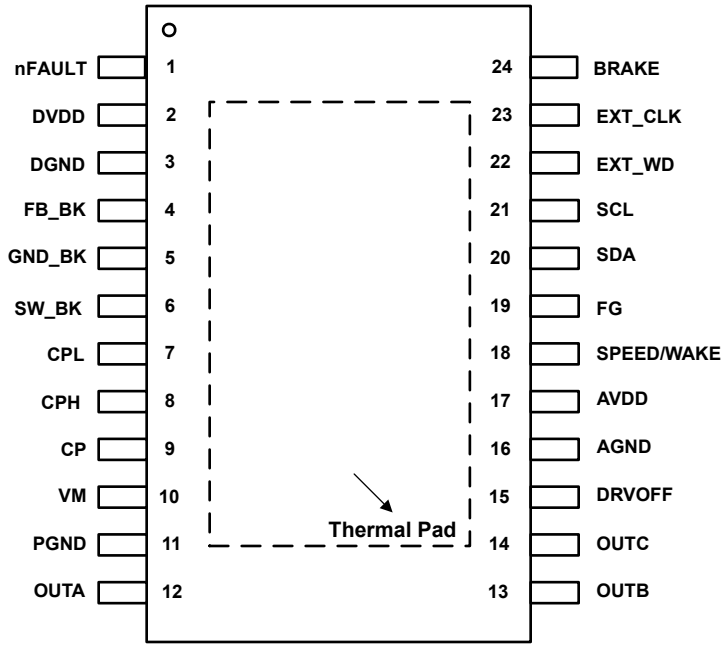


Figure 4-3. MCF8315D, 24-Pin HTSSOP With Exposed Thermal Pad, Top View

Copyright © 2025 Texas Instruments Incorporated

Table 4-1. Pin Functions

PIN	40-pin package	32-pin package	24-pin package	TYPE[1]	DESCRIPTION
NAME	MCF8315D	MCF8315D	MCF8315D		
AGND	26	19	16	GND	Device analog ground. Refer Section 9.4.1 for connection recommendation.
ALARM	39	30	-	O	Alarm signal: push-pull output. Pulled logic high during fault condition, if enabled. If ALARM pin is not used, leave the pin floating.
AVDD	27	20	17	PWR O	3.3V internal regulator output. Connect a X7R, 1µF, 10V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 20mA for external circuits.
BRAKE	35	28	24	I	High → Brake the motor Low → Normal motor operation If BRAKE pin is not used, connect to AGND directly. If BRAKE pin is used to brake the motor, use an (optional) external 10kΩ pull-down resistor (to AGND) for better noise rejection.
CP	8	7	9	PWR	Charge pump output. Connect a X7R, 1µF, 16V ceramic capacitor between the CP and VM pins.
CPH	7	6	8	PWR	Charge pump switching node. Connect a X7R, 47nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
CPL	6	5	7	PWR	
DACOUT1	36	29	-	O	DAC output DACOUT1
DACOUT2	37	-	-	O	DAC output DACOUT2
DACOUT2 /SOX	38	-	-	O	Multi-purpose pin: DAC output when configured as DACOUT2 CSA output when configured as SOX
DGND	2	1	3	GND	Device digital ground. Refer Section 9.4.1 for connection recommendation.
DIR	34	27	-	I	Direction of motor spinning; When low, phase driving sequence is OUT A → OUT C → OUT B When high, phase driving sequence is OUT A → OUT B → OUT C If DIR pin is not used, connect to AGND or AVDD directly (depending on phase driving sequence needed). If DIR pin is used for changing motor spin direction, use an (optional) external 10kΩ pulldown resistor (to AGND) for better noise rejection.
DRVOFF	21	18	15	I	Coast (Hi-Z) all six MOSFETs as long as DRVOFF is high. If DRVOFF pin is not used, connect to AGND directly. If DRVOFF pin is to be used for instantly coasting (Hi-Z) the MOSFETs, use an external 10kΩ pull-down resistor (to AGND) for better noise rejection.
DVDD	1	32	2	PWR	1.5V internal regulator output. Connect a X7R, 1µF, 6.3V ceramic capacitor between the DVDD and DGND pins.
EXT_CLK	33	26	23	I	External clock reference input in external clock reference mode.
EXT_WD	32	25	22	I	External watchdog input.
FB_BK	3	2	4	PWR I/O	Feedback for buck regulator output control. Connect to buck regulator output after the inductor/resistor.
FG	29	22	19	O	Motor speed indicator : open-drain output that requires an external pull-up resistor to 1.8V to 5.0V. An optional internal pull-up resistor to AVDD is enabled by setting PULLUP_ENABLE to 1b; no external pull-up resistor should be used when internal pull-up resistor is enabled.
GND_BK	4	3	5	GND	Buck regulator ground. Refer Section 9.4.1 for connection recommendation.
NC	22, 23, 24, 25	-	-	-	No connection. Leave these pins floating or connect to Thermal pad for better heat dissipation.

Copyright © 2025 Texas Instruments Incorporated

Table 4-1. Pin Functions (continued)

PIN	40-pin package	32-pin package	24-pin package	TYPE[1]	DESCRIPTION
NAME	MCF8315D	MCF8315D	MCF8315D		
nFAULT	40	31	1	O	Fault indicator. Pulled logic-low during fault condition; open-drain output that requires an external pull-up resistor to 1.8V to 5.0V. An optional internal pull-up resistor to AVDD is enabled by setting PULLUP_ENABLE to 1b; no external pull-up resistor should be used when internal pull-up resistor is enabled.
OUTA	13, 14	11, 12	12	PWR O	Half-bridge output A
OUTB	16, 17	13, 14	13	PWR O	Half-bridge output B
OUTC	19, 20	15, 16	14	PWR O	Half-bridge output C
PGND	12, 15, 18	10, 17	11	GND	Device power ground. Refer Section 9.4.1 for connection recommendation.
SCL	31	24	21	I	I^2C clock input
SDA	30	23	20	I/O	I^2C data line
SPEED/ WAKE	28	21	18	I	Device speed input; supports analog, PWM or frequency based speed input. The speed pin input can be configured through SPEED_MODE.
SW_BK	5	4	6	PWR	Buck switch node. Connect this pin to an inductor or resistor.
VM	9, 10, 11	8, 9	10	PWR I	Device and motor power supply. Connect to motor supply voltage; bypass to PGND with one 0.1µF capacitor plus one bulk capacitor. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
Thermal pad				GND	Must be connected to AGND.

(1) I = input, O = output, GND = ground, PWR = power, NC = no connect

Copyright © 2025 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	40	V
Voltage difference between ground pins (GND_BK, DGND, PGND, AGND)	–0.3	0.3	V
Charge pump voltage (CPH, CP)	–0.3	V_{VM} + 6	V
Charge pump negative switching pin voltage (CPL)	–0.3	V_{VM} +0.3	V
Switching regulator pin voltage (FB_BK)	–0.3	6	V
Switching node pin voltage (SW_BK)	–0.3	V_{VM} +0.3	V
Analog regulators pin voltage (AVDD)	–0.3	4	V
Analog regulators pin voltage (DVDD)	–0.3	1.7	V
Logic pin input voltage (BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SCL, SDA, SPEED)	–0.3	6	V
Open drain pin output voltage (nFAULT, FG)	–0.3	6	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_{VM} + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	35	V
I_{OUT} (1)	Peak output winding current (RGF, RRY)	OUTA, OUTB, OUTC			4	A
	Peak output winding current (PWP)				3.5	
V_{IN_LOGIC}	Logic input voltage	BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD, SPEED, SDA, SCL	–0.1		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT, FG	–0.1		5.5	V
I_{OD}	Open drain output current capability	nFAULT, FG			5	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

Copyright © 2025 Texas Instruments Incorporated

5.4 Thermal Information

THERMAL METRIC[1]		MCF8315D			UNIT
		RGF (VQFN)	RRY (WQFN)	PWP	
		40 Pins	32 Pins	24 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28	30.7	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.7	18.6	23.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.9	9.6	10.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	1.6	3.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.9	9.6	10	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	3.4	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6 V, V_{SPEED} = 0, T_A = 25 °C		3	5	µA
		V_{SPEED} = 0, T_A = 125 °C		3.5	7	µA
I_{VMS}	VM standby mode current	V_{VM} ≥ 12 V, Standby Mode, DRVOFF = High, T_A = 25 °C, L_{BK} = 47 uH, C_{BK} = 22 µF		8	16	mA
		V_{VM} ≥ 12 V, Standby Mode, DRVOFF = High, T_A = 25 °C, R_{BK} = 22 Ω, C_{BK} = 22 µF		25	29	mA
		V_{VM} ≥ 12 V, Standby Mode, DRVOFF = High, L_{BK} = 47 uH, C_{BK} = 22 µF		8	16.5	mA
		V_{VM} ≥ 12 V, Standby Mode, DRVOFF = High, R_{BK} = 22 Ω, C_{BK} = 22 µF		25	29	mA
I_{VM}	VM operating mode current	V_{VM} ≥ 12 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), T_A = 25 °C, L_{BK} = 47 uH, C_{BK} = 22 µF, No Motor Connected		11	18	mA
		V_{VM} ≥ 12 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), T_A = 25 °C, R_{BK} = 22 Ω, C_{BK} = 22 µF, No Motor Connected		27	31.5	mA
		V_{VM} ≥ 12 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), L_{BK} = 47 uH, C_{BK} = 22 µF, No Motor Connected		11	18	mA
		V_{VM} ≥ 12 V, V_{SPEED} > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), R_{BK} = 22 Ω, C_{BK} = 22 µF, No Motor Connected		28	32	mA
V_{AVDD}	Analog regulator voltage	0 mA ≤ I_{AVDD} ≤ 20 mA	3.125	3.3	3.465	V
I_{AVDD}	External analog regulator load				20	mA
V_{DVDD}	Digital regulator voltage		1.4	1.55	1.65	V
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM	4.0	4.7	5.5	V

Copyright © 2025 Texas Instruments Incorporated

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK REGULATOR						
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 170 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 170 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 170 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 170 mA, BUCK_SEL = 11b	5.2	5.7	5.8	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b, 11b), 0 mA ≤ I_{BK} ≤ 170 mA		V_{VM}– I_{BK}*(R_{LBK} +2) [1]		V
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 20 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 20 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 20 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 20 mA, BUCK_SEL = 11b	5.2	5.7	5.8	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b, 11b), 0 mA ≤ I_{BK} ≤ 20 mA		V_{VM}– I_{BK}*(R_{LBK} +2)[1]		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 10 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 10 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 10 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 10 mA, BUCK_SEL = 11b	5.2	5.7	5.8	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b, 11b), 0 mA ≤ I_{BK} ≤ 10 mA		V_{VM}– I_{BK}*(R_{BK} +2)		V
V_{BK_RIP}	Buck regulator ripple voltage	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 170 mA, Buck regulator with inductor, L_{BK} = 47 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 20 mA, Buck regulator with inductor, L_{BK} = 22 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 10 mA, Buck regulator with resistor; R_{BK} = 22 Ω, C_{BK} = 22 µF	–100		100	mV
I_{BK}	External buck regulator load	L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			170	mA
		L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			170 – I_{AVDD}	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			20	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			20 – I_{AVDD}	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			10	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			10 – I_{AVDD}	mA

Copyright © 2025 Texas Instruments Incorporated

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW_BK}	Buck regulator switching frequency	Regulation Mode	20		535	kHz
		Linear Mode	20		535	kHz
V_{BK_UVLO}	Buck regulator undervoltage lockout	V_{BK} rising, BUCK_SEL = 00b	2.7	2.8	2.95	V
		V_{BK} falling, BUCK_SEL = 00b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 01b	4.3	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 01b	4.1	4.2	4.42	V
		V_{BK} rising, BUCK_SEL = 10b	2.7	2.8	2.95	V
		V_{BK} falling, BUCK_SEL = 10b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 11b	4.3	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 11b	4.1	4.2	4.42	V
$V_{BK\_UVLO\_HYS}$	Buck regulator undervoltage lockout hysteresis	Rising to falling threshold, BUCK_SEL = 00b	90	200	400	mV
		Rising to falling threshold, BUCK_SEL = 01b	70	200	400	mV
		Rising to falling threshold, BUCK_SEL = 10b	90	200	400	mV
		Rising to falling threshold, BUCK_SEL =11b	70	200	400	mV
I_{BK_CL}	Buck regulator current limit threshold	BUCK_CL = 0b	360	600	910	mA
		BUCK_CL = 1b	80	150	250	mA
I_{BK_OCP}	Buck regulator over current protection trip point		2	3	4	A
t_{BK_RETRY}	Over current protection retry time		0.7	1	1.3	ms
DRIVER OUTPUTS						
$R_{DS(ON)}$ (RGF)	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		240	260	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		250	270	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 150°C		360	400	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 150°C		370	415	mΩ
$R_{DS(ON)}$ (RRY)	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		250	270	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		260	280	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		375	415	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		385	425	mΩ
$R_{DS(ON)}$ (PWP)	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		265	280	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		275	290	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 150°C		390	430	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 150°C		400	440	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, SLEW_RATE = 10b	80	125	210	V/µs
		V_{VM} = 24 V, SLEW_RATE = 11b	130	200	315	V/µs
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	V_{VM} = 24 V, SLEW_RATE = 10b	80	125	235	V/µs
		V_{VM} = 24 V, SLEW_RATE = 11b	130	200	345	V/µs
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24 V, SR = 125 V/µs		650	850	ns
		V_{VM} = 24 V, SR = 200 V/µs		500	550	ns
SPEED INPUT - PWM MODE						
f_{PWM}	PWM input frequency		0.01		100	kHz

Copyright © 2025 Texas Instruments Incorporated

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Res_{PWM}	PWM input resolution	f_{PWM} = 0.01 to 0.35 kHz	11	12	13	bits
		f_{PWM} = 0.35 to 2 kHz	11	13	14	bits
		f_{PWM} = 2 to 3.5 kHz	11	11.5	12	bits
		f_{PWM} = 3.5 to 7 kHz	12	13	13.5	bits
		f_{PWM} = 7 to 14 kHz	11	12	12.5	bits
		f_{PWM} = 14 to 29.2 kHz	10	11.5	12	bits
		f_{PWM} = 29.3 to 60 kHz	9	10.5	11	bits
		f_{PWM} = 60 to 100 kHz	8	9	10	bits
SPEED INPUT - ANALOG MODE						
V_{ANA_FS}	Analog full-speed voltage		2.95	3	3.05	V
V_{ANA_RES}	Analog voltage resolution			732		µV
SPEED INPUT - FREQUENCY MODE						
f_{PWM_FREQ}	PWM input frequency range	Duty cycle = 50%	3		32767	Hz
SLEEP MODE						
V_{EN_SL}	Analog voltage to enter sleep mode	SPEED_MODE = 00b (analog mode)			40	mV
V_{EX_SL}	Analog voltage to exit sleep mode	SPEED_MODE = 00b (analog mode)	2.2			V
t_{DET_ANA}	Time needed to detect wake up signal on SPEED pin	SPEED_MODE= 00b (analog mode) $V_{SPEED} > V_{EX\_SL}$	0.5	1	1.5	µs
t_{WAKE}	Wakeup time from sleep state	$V_{SPEED} > V_{EX\_SL}$ to DVDD voltage available, SPEED_MODE = 00b (analog mode)		3	5	ms
$t_{EX\_SL\_DR\_ANA}$	Time taken to drive motor after wake-up from sleep state (MCF8315D)	SPEED_MODE = 00b (analog mode), DVDD voltage available to first output PWM pulse, ISD detection disabled			30	ms
$t_{EX\_SL\_DR\_ANA}$	Time taken to drive motor after wake-up from sleep state (MCF8315DUL)	SPEED_MODE = 00b (analog mode), DVDD voltage available to first output PWM pulse, ISD detection disabled			180	ms
t_{DET_PWM}	Time needed to detect wake up signal on SPEED pin	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} > V_{IH}$	0.5	1	1.5	µs
t_{WAKE_PWM}	Wakeup time from sleep state	$V_{SPEED} > V_{IH}$ to DVDD voltage available, SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode)		3	5	ms
$t_{EX\_SL\_DR\_PWM}$	Time taken to drive motor after wake-up from sleep state (MCF8315D)	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), DVDD voltage available to first output PWM pulse, ISD detection disabled			30	ms
$t_{EX\_SL\_DR\_PWM}$	Time taken to drive motor after wake-up from sleep state (MCF8315DUL)	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), DVDD voltage available to first output PWM pulse, ISD detection disabled			180	ms
$t_{DET\_SL\_ANA}$	Time needed to detect sleep command, analog mode	SPEED_MODE = 00b (analog mode) $V_{SPEED} < V_{EN\_SL}$, SLEEP_ENTRY_TIME = 00b	0.035	0.05	0.065	ms
		SPEED_MODE = 00b (analog mode) $V_{SPEED} < V_{EN\_SL}$, SLEEP_ENTRY_TIME = 00b or 01b	0.14	0.2	0.26	ms
		SPEED_MODE = 00b (analog mode) $V_{SPEED} < V_{EN\_SL}$, SLEEP_ENTRY_TIME = 10b	14	20	26	ms
		SPEED_MODE = 00b (analog mode) $V_{SPEED} < V_{EN\_SL}$, SLEEP_ENTRY_TIME = 11b	140	200	260	ms

Copyright © 2025 Texas Instruments Incorporated

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DET\_SL\_PWM}$	Time needed to detect sleep command, PWM or frequency mode	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} < V_{IL}$, SLEEP_ENTRY_TIME = 00b	0.035	0.05	0.065	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} < V_{IL}$, SLEEP_ENTRY_TIME = 01b	0.14	0.2	0.26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} < V_{IL}$, SLEEP_ENTRY_TIME = 10b	14	20	26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED} < V_{IL}$, SLEEP_ENTRY_TIME = 11b	140	200	260	ms
t_{EN_SL}	Time needed to stop driving motor after detecting sleep command	SPEED < V_{EN_SL} (analog mode) or $V_{SPEED} < V_{IL}$ (PWM mode or Frequency mode) or VSPEED < V_{IL} and DIGITAL_SPEED_CTRL = 0b (I2C mode)		1	2	ms
STANDBY MODE						
$t_{EX\_SB\_DR\_ANA}$	Time taken to drive motor after exiting standby mode, analog mode	SPEED_MODE = 00b (analog mode), $V_{SPEED} > V_{EX\_SB}$, ISD detection disabled			6	ms
$t_{EX\_SB\_DR\_PWM}$	Time taken to drive motor after exiting standby mode, PWM mode	SPEED_MODE = 01b (PWM mode) $V_{SPEED} > V_{IH}$, ISD detection disabled			6	ms
$t_{DET\_SB\_ANA}$	Time needed to detect standby command, analog mode	SPEED_MODE = 00b (analog mode), $V_{SPEED} < V_{EN\_SB}$	0.5	1	2	ms
$t_{DET\_SB\_PWM}$	Time needed to detect standby command, PWM or frequency mode	SPEED_MODE = 01b (PWM mode) or SPEED_MODE = 11b (Freq mode), $V_{SPEED} < V_{IL}$, SLEEP_ENTRY_TIME = 00b	0.035	0.05	0.065	ms
		SPEED_MODE = 01b (PWM mode) or SPEED_MODE = 11b (Freq mode), $V_{SPEED} < V_{IL}$, SLEEP_ENTRY_TIME = 01b	0.14	0.2	0.26	ms
		SPEED_MODE = 01b (PWM mode) or SPEED_MODE = 11b (Freq mode), $V_{SPEED} < V_{IL}$, SLEEP_ENTRY_TIME = 10b	14	20	26	ms
		SPEED_MODE = 01b (PWM mode) or SPEED_MODE = 11b (Freq mode), $V_{SPEED} < V_{IL}$, SLEEP_ENTRY_TIME = 11b	140	200	260	ms
$t_{DET\_SB\_DIG}$	Time needed to detect standby mode, I^2C mode	SPEED_MODE = 10b (I^2C mode), DIGITAL_SPEED_CTRL = 0b		1	2	ms
t_{EN_SB}	Time needed to stop driving motor after detecting standby command	All reference input modes		1	2	ms
LOGIC-LEVEL INPUTS (BRAKE, DIR, EXT_CLK, EXT_WD, SPEED)						
V_{IL}	Input logic low voltage	AVDD = 3 to 3.6 V			0.25*AVDD	V
V_{IH}	Input logic high voltage	AVDD = 3 to 3.6 V	0.65*AVDD			V
V_{HYS}	Input hysteresis		50	500	800	mV
I_{IL}	Input logic low current	AVDD = 3 to 3.6 V	-0.15		0.15	µA

Copyright © 2025 Texas Instruments Incorporated

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic high current	AVDD = 3 to 3.6 V	-0.3		0	µA
R_{PD_SPEED}	Input pulldown resistance	SPEED pin To GND	0.6	1	1.4	MΩ
OPEN-DRAIN OUTPUTS (nFAULT, FG)						
V_{OL}	Output logic low voltage	I_{OD} = -5 mA			0.4	V
I_{OZ}	Output logic high current	V_{OD} = 3.3 V	0		0.5	µA
I^2C Serial Interface						
V_{I2C_L}	Input logic low voltage		-0.5		0.3*AVDD	V
V_{I2C_H}	Input logic high voltage		0.7*AVDD		5.5	V
V_{I2C_HYS}	Hysteresis		0.05*AVDD			V
V_{I2C_OL}	Output logic low voltage	Open-drain at 2mA sink current	0		0.4	V
I_{I2C_OL}	Output logic low current	V_{I2C_OL} = 0.6V			6	mA
I_{I2C_IL}	Input current on SDA and SCL		-10[2]		10[2]	µA
C_i	Capacitance for SDA and SCL				10	pF
t_{of}	Output fall time from V_{I2C_H}(min) to V_{I2C_L}(max)	Standard Mode			250[3]	ns
		Fast Mode			250[3]	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Fast Mode	0		50[4]	ns
OSCILLATOR						
f_{OSCREF}	External clock reference	EXT_CLK_CONFIG = 000b		8		kHz
		EXT_CLK_CONFIG = 001b		16		kHz
		EXT_CLK_CONFIG = 010b		32		kHz
		EXT_CLK_CONFIG = 011b		64		kHz
		EXT_CLK_CONFIG = 100b		128		kHz
		EXT_CLK_CONFIG = 101b		256		kHz
		EXT_CLK_CONFIG = 110b		512		kHz
		EXT_CLK_CONFIG = 111b		1024		kHz
EEPROM						
EE_{Prog}	Programming voltage		1.35	1.5	1.65	V
EE_{RET}	Retention	T_A = 25 ℃		100		Years
		T_J = -40 to 150 ℃	10			Years
EE_{END}	Endurance	T_J = -40 to 150 ℃	1000			Cycles
		T_J = -40 to 85 ℃	20000			Cycles
PROTECTION CIRCUITS						
V_{UVLO}	Supply under voltage lockout (UVLO)	VM rising	4.3	4.4	4.51	V
		VM falling	4.1	4.2	4.32	V
V_{UVLO_HYS}	Supply under voltage lockout hysteresis	Rising to falling threshold	90	200	350	mV
t_{UVLO}	Supply under voltage deglitch time		3	5	7	µs
V_{OVP}	Supply over voltage protection (OVP) threshold	Supply rising, OVP_EN = 1, OVP_SEL = 0	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	31.8	33	34.3	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	19	21	22	V

Copyright © 2025 Texas Instruments Incorporated

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP_HYS}	Supply over voltage protection hysteresis	Rising to falling threshold, OVP_SEL = 1	0.9	1	1.15	V
		Rising to falling threshold, OVP_SEL = 0	0.7	0.8	0.9	V
t_{OVP}	Supply over voltage deglitch time		2.5	5	7	µs
V_{CPUV}	Charge pump under voltage lockout (above VM)	Supply rising	2.25	2.5	2.75	V
		Supply falling	2.2	2.4	2.6	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	65	100	150	mV
V_{AVDD_UV}	Analog regulator (AVDD) under voltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.48	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator under voltage lockout hysteresis	Rising to falling threshold	180	200	240	mV
I_{OCP}	Over current protection trip point	OCP_LVL = 0b	5.5	9	12	A
		OCP_LVL = 1b	9	13	18	A
t_{OCP}	Over current protection deglitch time	OCP_DEG = 00b	0.02	0.2	0.4	µs
		OCP_DEG = 01b	0.2	0.6	1.2	µs
		OCP_DEG = 10b	0.5	1.2	1.8	µs
		OCP_DEG = 11b	0.9	1.6	2.5	µs
t_{RETRY}	Over current protection retry time		425	500	575	ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	135	145	155	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	15	20	30	°C
T_{TSD_BUCK}	Thermal shutdown temperature (Buck)	Die temperature (T_J)	170	180	190	°C
$T_{TSD\_BUCK\_HYS}$	Thermal shutdown hysteresis (Buck)	Die temperature (T_J)	15	20	30	°C
T_{TSD}	Thermal shutdown temperature (FET)	Die temperature (T_J)	165	175	185	°C
T_{TSD_HYS}	Thermal shutdown hysteresis (FET)	Die temperature (T_J)	15	20	30	°C

(1) R_{LBK} is resistance of inductor L_{BK}.
(2) If AVDD is switched off, I/O pins must not obstruct the SDA and SCL lines.
(3) The maximum tf for the SDA and SCL bus lines (300 ns) is longer than the specified maximum tof for the output stages (250 ns). This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
(4) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

5.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Standard-mode						
f_{SCL}	SCL clock frequency		0		100	kHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4			µs
t_{LOW}	LOW period of the SCL clock		4.7			µs
t_{HIGH}	HIGH period of the SCL clock		4			µs
t_{SU_STA}	Set-up time for a repeated START condition		4.7			µs
t_{HD_DAT}	Data hold time (2)	I2C bus devices	0 (3)		(4)	µs
t_{SU_DAT}	Data set-up time		250			ns
t_r	Rise time for both SDA and SCL signals				1000	ns
t_f	Fall time of both SDA and SCL signals (3) (6) (7) (8)				300	ns
t_{SU_STO}	Set-up time for STOP condition		4			µs

Copyright © 2025 Texas Instruments Incorporated

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{BUF}	Bus free time between STOP and START condition		4.7			µs
C_b	Capacitive load for each bus line (9)				400	pF
t_{VD_DAT}	Data valid time (10)				3.45 (4)	µs
t_{VD_ACK}	Data valid acknowledge time (11)				3.45 (4)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V
Fast-mode						
f_{SCL}	SCL clock frequency		0		400	KHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU_STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD_DAT}	Data hold time (2)		0 (3)		(4)	µs
t_{SU_DAT}	Data set-up time		100 (5)			ns
t_r	Rise time for both SDA and SCL signals		20		300	ns
t_f	Fall time of both SDA and SCL signals (3) (6) (7) (8)		20 x (AVDD/ 5.5V)		300	ns
t_{SU_STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between STOP and START condition		1.3			µs
C_b	Capacitive load for each bus line (9)				400	pF
t_{VD_DAT}	Data valid time (10)				0.9 (4)	µs
t_{VD_ACK}	Data valid acknowledge time (11)				0.9 (4)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V

(1) All values referred to $V_{IH(min)}$ ($0.3V_{DD}$) and $V_{IL(max)}$ levels
(2) t_{HD_DAT} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(4) The maximum t_{HD_DAT} could be 3.45 µs and .9 µs for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_DAT} or t_{VD_ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
(5) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement t_{SU_DAT} 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU\_DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
(6) If mixed with HS-mode devices, faster fall times according to Table 10 are allowed.
(7) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(8) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
(9) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
(10) t_{VD_DAT} = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
(11) t_{VD_ACK} = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, dependging on which one is worse).

Copyright © 2025 Texas Instruments Incorporated

6 Detailed Description

6.1 Overview

The MCF8315D provides a single-chip, code-free sensorless FOC solution for customers driving speed-controlled 12 to 24V brushless-DC motors requiring up to 4A peak phase currents.

The MCF8315D integrates three ½-bridges with 40V absolute maximum capability and a low $R_{DS(ON)}$ of 240mΩ(RGF)/250mΩ(RRY)/265mΩ(PWP) (high-side + low-side) to enable high power drive capability. Current is sensed using an integrated current sensing circuit which eliminates the need for external sense resistors. Power management features of an adjustable buck regulator and LDO generate the necessary voltage rails for the device and can also be used to power external circuits.

MCF8315D implements sensorless FOC, so an external microcontroller is not required to spin the brushless DC motor. The algorithm is implemented in a fixed-function state machine, so no coding is needed. The algorithm is highly configurable through register settings ranging from motor start-up behavior to closed-loop operation. Register settings can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. The device receives a speed command through a PWM input, analog voltage, frequency input, or I^2C command.

In-built protection features include power-supply under voltage lockout (UVLO), charge-pump under voltage lockout (CPUV), over current protection (OCP), AVDD under voltage lockout (AVDD_UV), buck regulator UVLO, motor lock detection and over temperature warning and shutdown (OTW and TSD). Fault events are indicated by the nFAULT pin with detailed fault information available in the registers.

The MCF8315D device is available in three packages:

1. RGF: 40-pin, 7x5mm, 0.5mm pin pitch VQFN with a height of 1mm
2. RRY: 32-pin, 6x4mm, 0.5mm pin pitch WQFN with a height of 0.8mm
3. PWP: 24-pin, 7.8x6.4mm, 0.65mm pin pitch HTSSOP with a height of 1.2mm

Copyright © 2025 Texas Instruments Incorporated

6.2 Functional Block Diagram

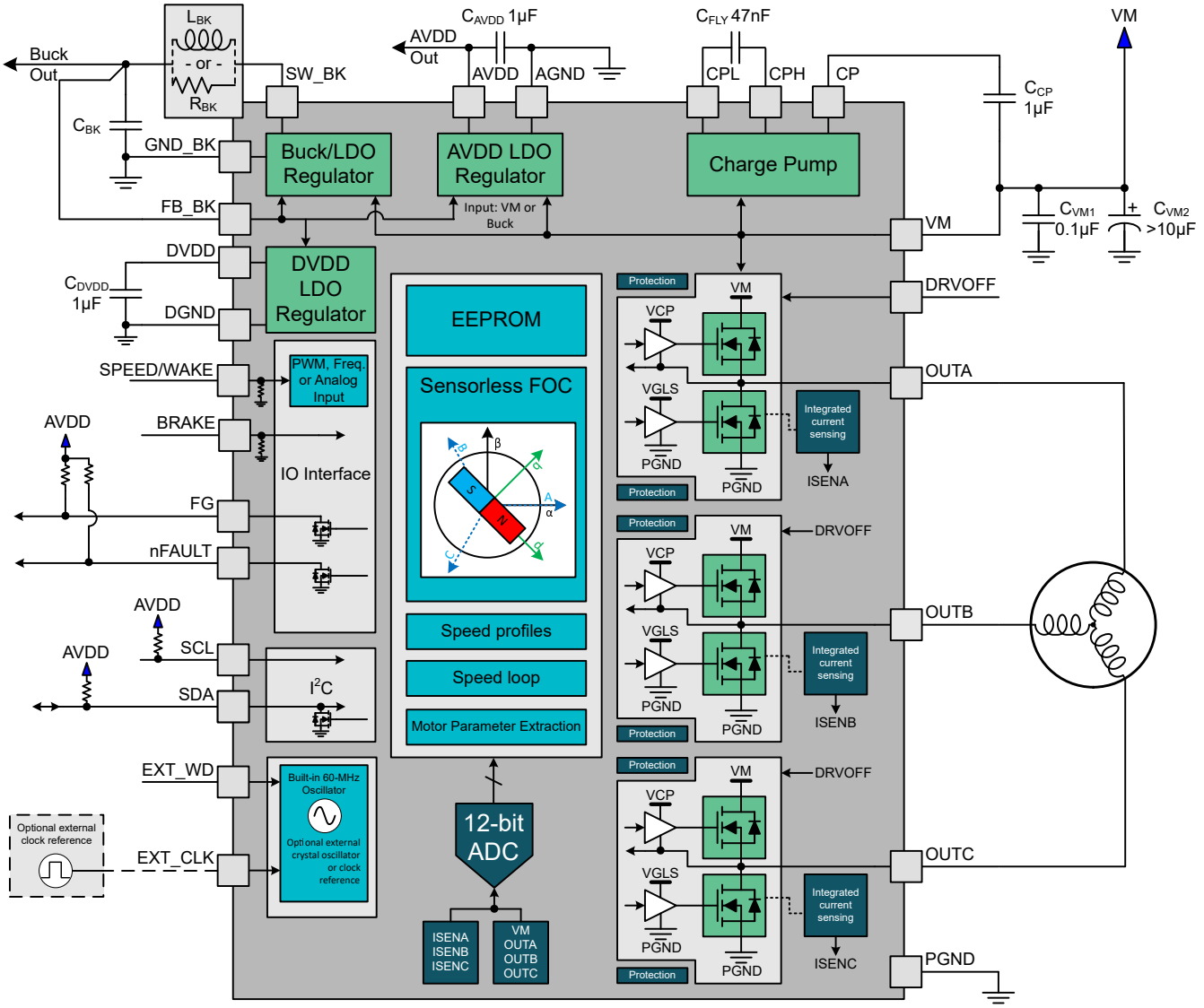


Figure 6-1. MCF8315D (PWP) Functional Block Diagram

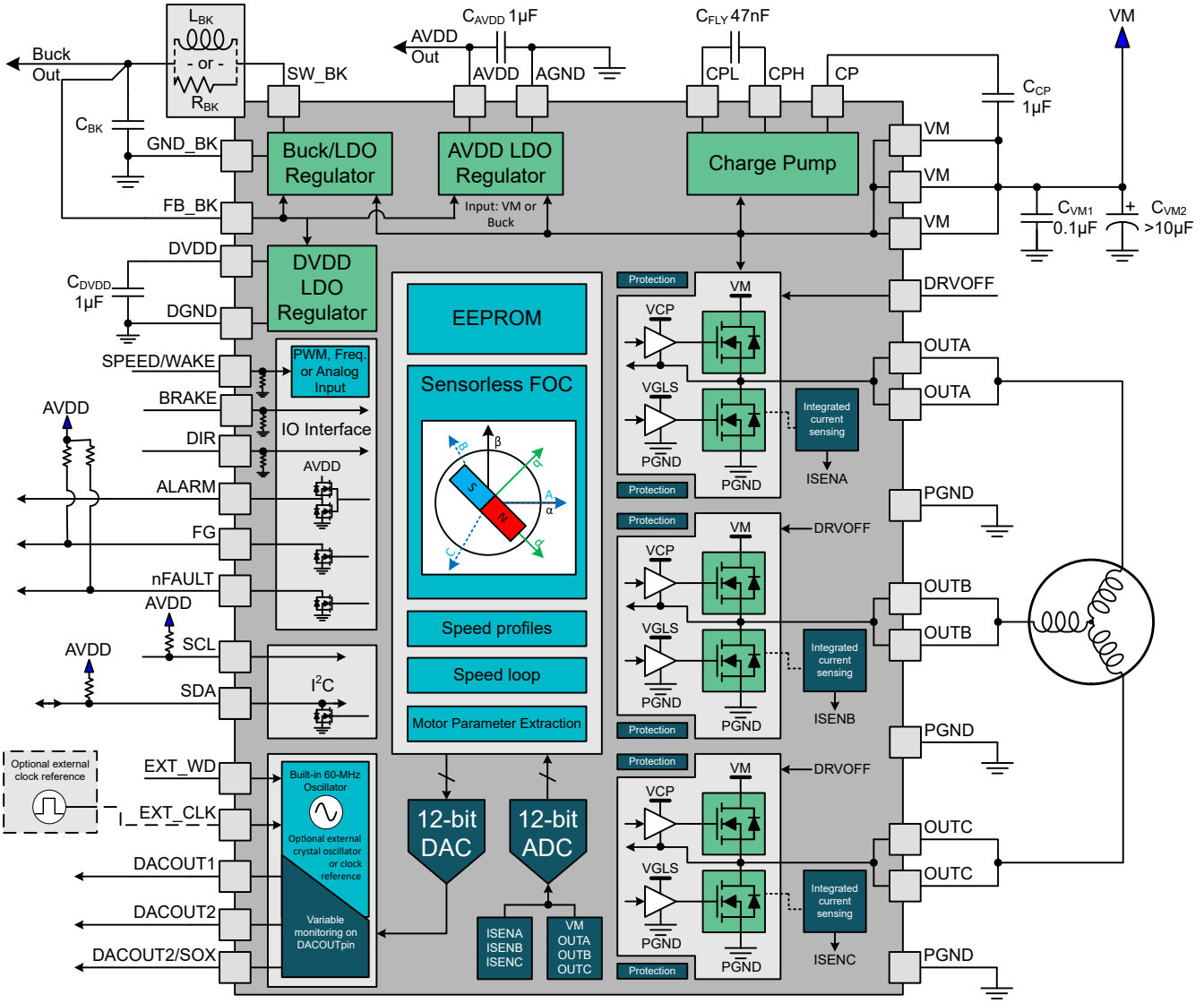


Figure 6-2. MCF8315D (RGF) Functional Block Diagram

Copyright © 2025 Texas Instruments Incorporated

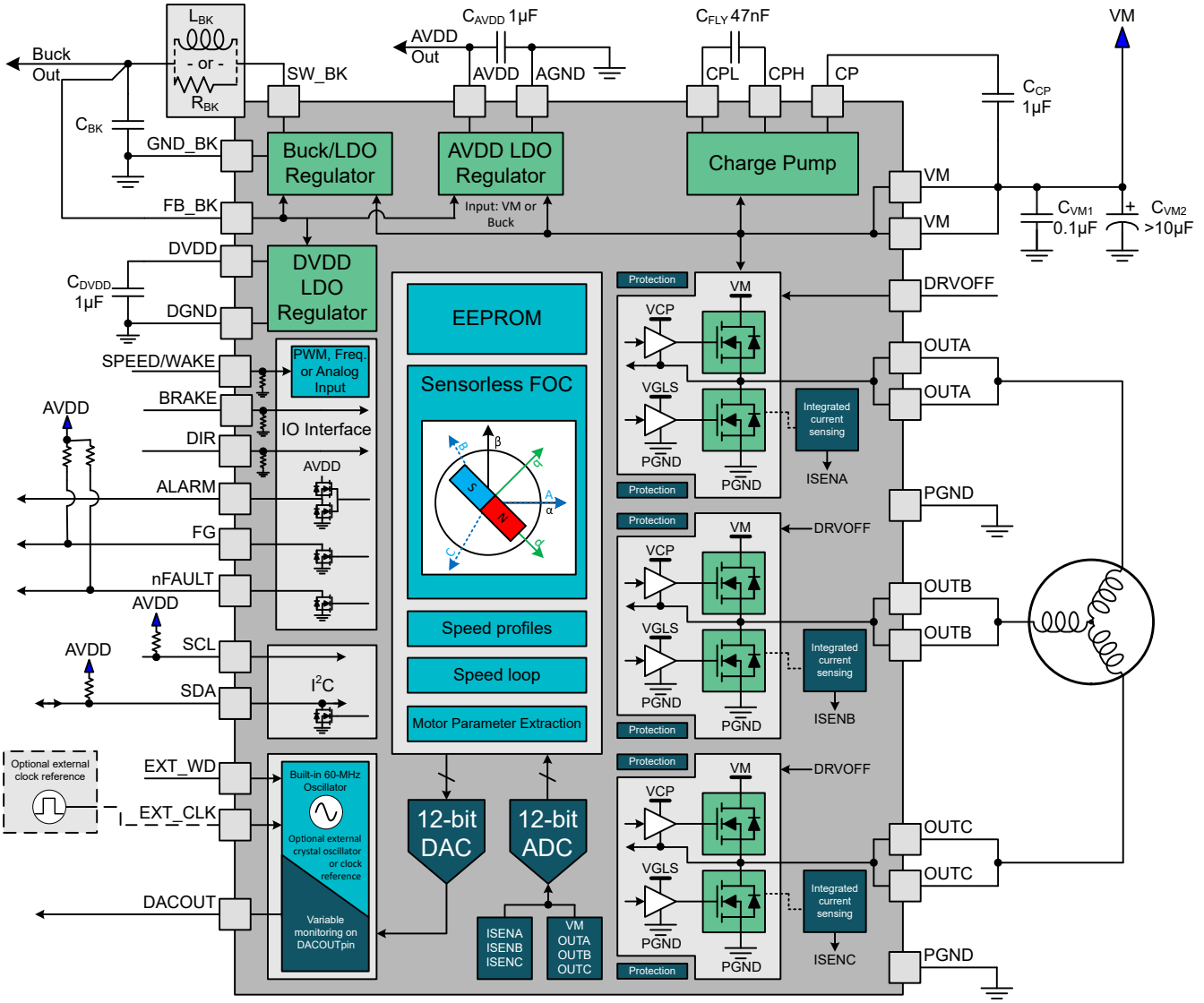


Figure 6-3. MCF8315D (RRY) Functional Block Diagram

6.3 Feature Description

6.3.1 Output Stage

The MCF8315D consists of integrated 240mΩ/250mΩ/265mΩ (combined high-side and low-side FETs' on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs.

6.3.2 Device Interface

The MCF8315D supports I^2C interface to provide end application design with adequate flexibility. MCF8315D allows controlling the motor operation and system through BRAKE, DRVOFF, DIR, EXT_CLK, EXT_WD and SPEED/WAKE pins. MCF8315D also provides different signals for monitoring system variables, speed, fault and phase current feedback through DACOUT1, DACOUT2, FG, nFAULT and SOX pins.

6.3.2.1 Interface - Control and Monitoring

Motor Control Signals

- SPEED/WAKE pin is used to control the motor speed and to wake up MCF8315D from sleep. SPEED pin can be configured to accept PWM, frequency or analog input signals. It is also used to enter and exit from sleep and standby mode (see Table 6-8).
- When BRAKE pin is driven 'High', MCF8315D enters brake state. Brake state can be configured to either low side brake (see Low-Side Braking) or align brake (see Section 6.3.22) through BRAKE_PIN_MODE. MCF8315D decreases output speed to value defined by BRAKE_SPEED_THRESHOLD before entering brake state. As long as BRAKE is driven 'High', MCF8315D stays in brake state. Brake pin input can be overwritten by configuring BRAKE_INPUT over the I^2C interface.
- The DIR pin decides the direction of motor spin; when driven 'High', the sequence is OUT A → OUT B → OUT C, and when driven 'Low', the sequence is OUT A → OUT C → OUT B. DIR pin input can be overwritten by configuring DIR_INPUT over the I^2C interface.
- When DRVOFF pin is driven 'High', MCF8315D stops driving the motor by turning OFF (Hi-Z) all MOSFETs (coast state) - this could be accompanied by faults like no motor or abnormal BEMF. When DRVOFF is driven 'Low', MCF8315D returns to normal state of operation, as if it was restarting the motor (see DRVOFF Functionality). DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active. Entry and exit from sleep or standby condition is controlled by SPEED pin.

External Oscillator and Watchdog Signals

- EXT_CLK pin can be used to provide an external clock reference (see External Clock Source).
- EXT_WD pin can be used to provide an external watchdog signal (see External Watchdog).

Output Signals

- DACOUT1 outputs internal variable defined by address in register DACOUT1_VAR_ADDR. DACOUT1 is refreshed every 100µs (see DAC outputs).
- DACOUT2 outputs internal variable defined by address in register DACOUT2_VAR_ADDR. DACOUT2 is refreshed every 100µs (see DAC outputs).
- FG pin provides pulses which are proportional to motor speed (see FG Configuration).
- nFAULT (active low) pin provides fault status in device or motor operation.
- ALARM pin, when enabled using ALARM_PIN_EN, provides fault status in device or motor operation as an active high signal. When ALARM pin is enabled, report only faults are reported only on ALARM pin (as logic high) and not reported on nFAULT pin (as logic low). When ALARM pin is enabled, actionable faults are reported on ALARM pin (as logic high) as well as on nFAULT pin (as logic low). When ALARM pin is disabled, it is in Hi-Z state and all faults (actionable and report only) are reported on nFAULT as logic low. ALARM pin should be left floating when unused/disabled.
- SOX pin provides the output of one of the current sense amplifiers.

Copyright © 2025 Texas Instruments Incorporated

Note

1. Internal pull-up resistor (to AVDD) for both FG and nFAULT pins can be enabled by configuring PULLUP_ENABLE to 1b. Any change to this bit needs to be written to EEPROM followed by a power recycle to take effect. When PULLUP_ENABLE is set to 1b, no external pull-up resistor should be provided.
2. DIR and BRAKE pins each have an internal pull-down resistor of 100kΩ. When these pins are used, an additional pull-down resistor of 10kΩ may be added externally for additional noise immunity.
3. SPEED pin has an internal pull-down resistor of 1MΩ. In analog speed input mode, a suitable R-C filter can be added externally for reducing noise. In PWM speed input mode, SPEED_PIN_GLITCH_FILTER can be appropriately configured for glitch rejection.

6.3.2.2 I²C Interface

The MCF8315D supports an I²C serial communication interface that allows an external controller to send and receive data. This I²C interface lets the external controller to configure the EEPROM and read detailed fault and motor state information. The pull-down strength of the I²C pins can be configured using SLEW_RATE_I2C_PINS. The I²C bus is a two-wire interface using the SCL and SDA pins which are described as follows :

- The SCL pin is the clock signal input.
- The SDA pin is the data input and output.

6.3.3 Step-Down Mixed-Mode Buck Regulator

The MCF8315D has an integrated mixed-mode buck regulator to supply regulated 3.3V or 5V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4V or 5.7V for supporting the extra headroom for an external LDO for generating a 3.3V or 5V supplies. The output voltage of the buck is set by BUCK_SEL.

The buck regulator has a low quiescent current of ~1-2mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

Table 6-1. Recommended settings for Buck Regulator

Buck Mode	Buck output voltage	AVDD power sequencing	Max output current from AVDD (I_{AVDD_MAX})	Max output current from Buck (I_{BK_MAX})	Buck current limit
Inductor - 47µH	3.3V or 4V	Not supported (BUCK_PS_DIS = 1b)	20mA	170mA	600mA (BUCK_CL = 0b)
Inductor - 47µH	5V or 5.7V	Supported (BUCK_PS_DIS = 0b)	20mA	170mA - I_{AVDD}	600mA (BUCK_CL = 0b)
Inductor - 22µH	3.3V or 4V	Not supported (BUCK_PS_DIS = 1b)	20mA	20mA	150mA (BUCK_CL = 1b)
Inductor - 22µH	5V or 5.7V	Supported (BUCK_PS_DIS = 0b)	20mA	20mA - I_{AVDD}	150mA (BUCK_CL = 1b)
Resistor - 22Ω	3.3V or 4V	Not supported (BUCK_PS_DIS = 1b)	20mA	10mA	150mA (BUCK_CL = 1b)
Resistor - 22Ω	5V or 5.7V	Supported (BUCK_PS_DIS = 0b)	20mA	10mA - I_{AVDD}	150mA (BUCK_CL = 1b)

6.3.3.1 Buck in Inductor Mode

The buck regulator in MCF8315D is primarily designed to support low inductance of 47µH and 22µH. A 47µH inductor allows the buck regulator to operate up to 170mA load current support, whereas applications requiring current up to 20mA can use a 22µH inductor which reduces component size.

Copyright © 2025 Texas Instruments Incorporated

Figure 6-4 shows the connection of buck regulator in inductor mode.

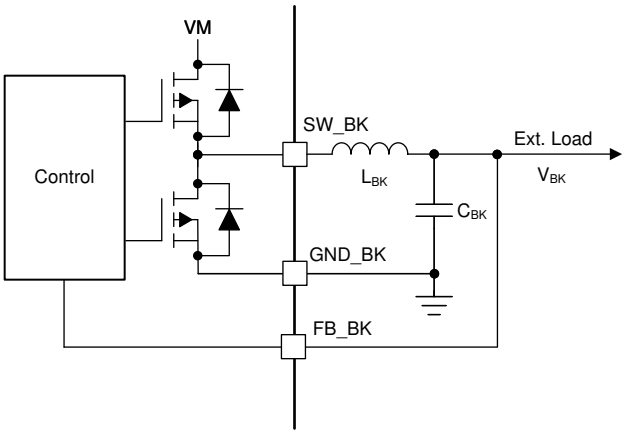


Figure 6-4. Buck (Inductor Mode)

6.3.3.2 Buck in Resistor mode

If the external load requirement is less than 10mA, the inductor can be replaced with a resistor. In resistor mode the power is dissipated across the external resistor and the efficiency is lower than buck in inductor mode.

Figure 6-5 shows the connection of buck in resistor mode.

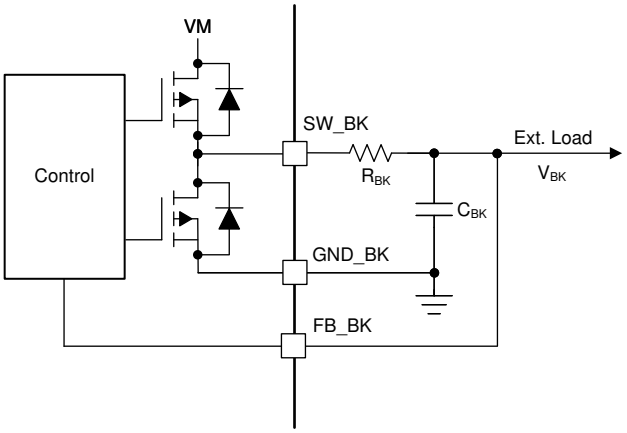


Figure 6-5. Buck (Resistor Mode)

6.3.3.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to supply an external LDO to generate standard 3.3V or 5V output rail with higher accuracies. The buck output voltage should be configured to 4V or 5.7V to provide extra headroom to support the external LDO for generating 3.3V or 5V rail as shown in Figure 6-6. This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

Copyright © 2025 Texas Instruments Incorporated

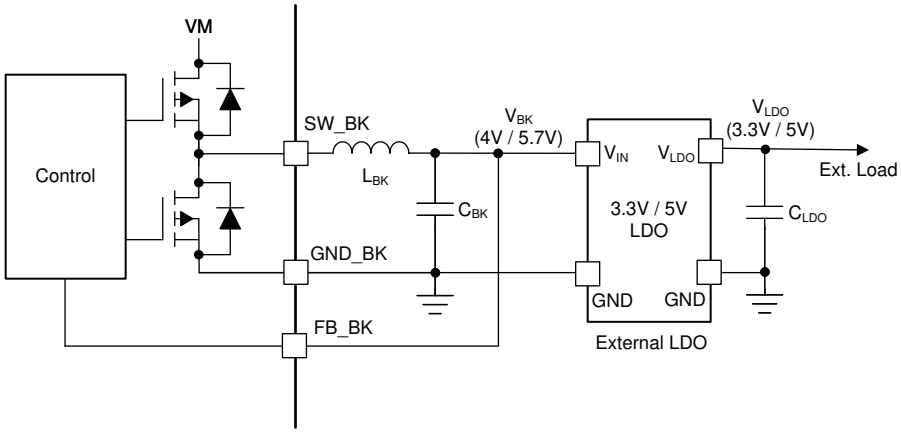


Figure 6-6. Buck Regulator with External LDO

6.3.3.4 AVDD Power Sequencing from Buck Regulator

The AVDD LDO has an option of using the power supply from mixed mode buck regulator to reduce the device power dissipation. The power sequencing mode allows on-the-fly changeover of AVDD LDO input from DC mains (VM) to buck output (V_{BK}) as shown in Figure 6-7. This sequencing can be configured through the BUCK_PS_DIS bit . Power sequencing is supported only when buck output voltage is set to 5V or 5.7V.

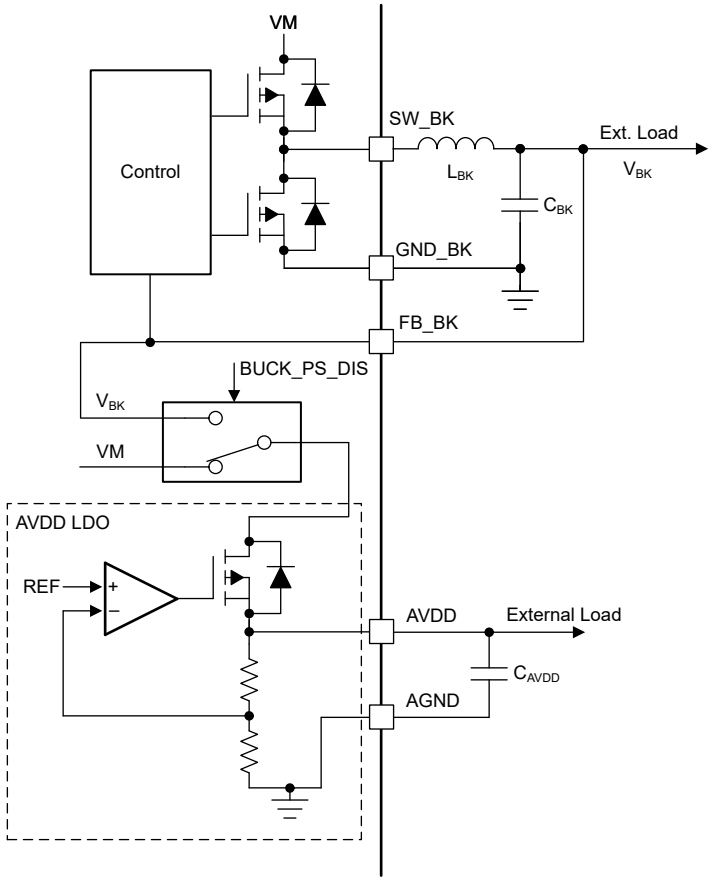


Figure 6-7. AVDD Power Sequencing from Mixed Mode Buck Regulator

Copyright © 2025 Texas Instruments Incorporated

6.3.3.5 Mixed Mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage (V_{BK_REF}) which is internally generated depending on the buck output voltage setting (BUCK_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ($V_{BK} < V_{BK\_REF}$) or low ($V_{BK} > V_{BK\_REF}$), the high-side power FET of the buck turns on and off respectively. An independent current control loop monitors the current in high-side power FET (I_{BK}) and turns off the high-side FET when the current becomes higher than the buck current limit (I_{BK_CL} set by BUCK_CL) - this implements a current limit control for the buck regulator. Figure 6-8 shows the architecture of the buck and various control/protection loops.

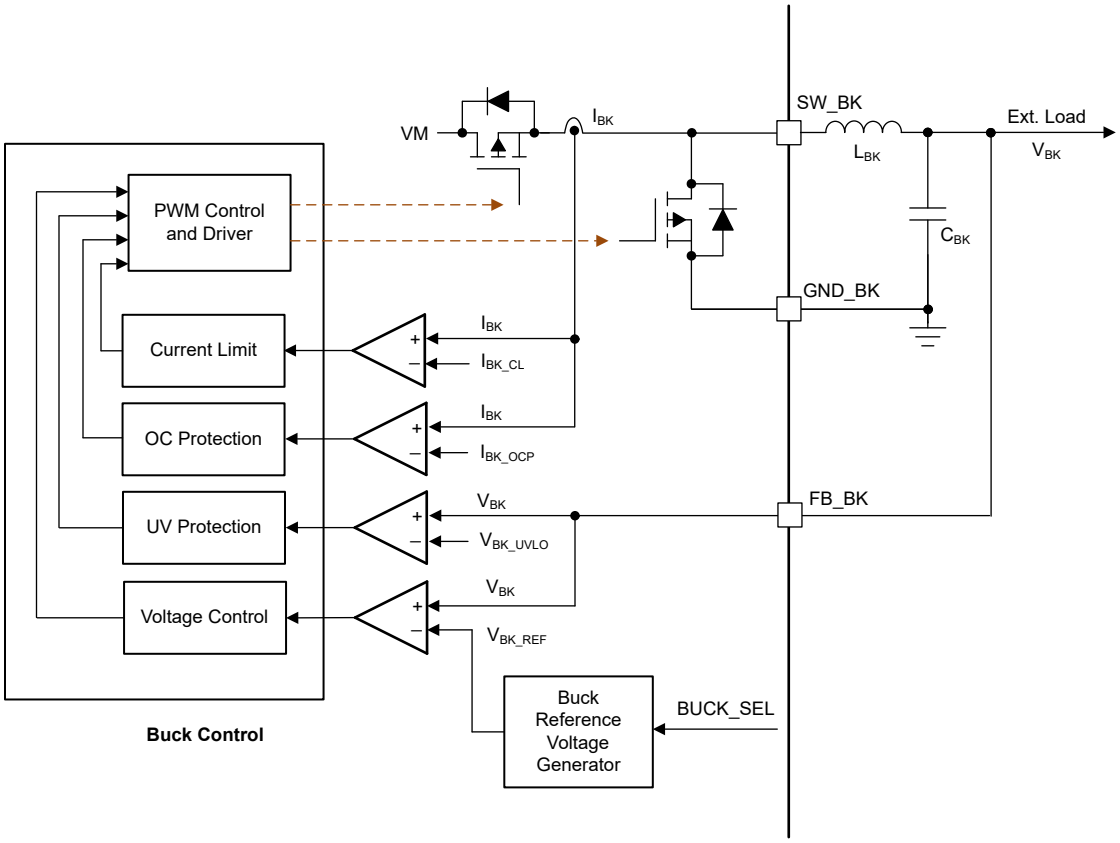


Figure 6-8. Buck Operation and Control Loops

6.3.4 AVDD Linear Voltage Regulator

A 3.3V linear regulator is integrated into MCF8315D and is available for use by external circuitry. This AVDD LDO regulator is used for powering up the internal circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other external circuitry supporting up to 20mA. The output of the AVDD regulator should be bypassed near the AVDD pin with an X5R or X7R, 1-µF, 6.3V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3V.

Copyright © 2025 Texas Instruments Incorporated

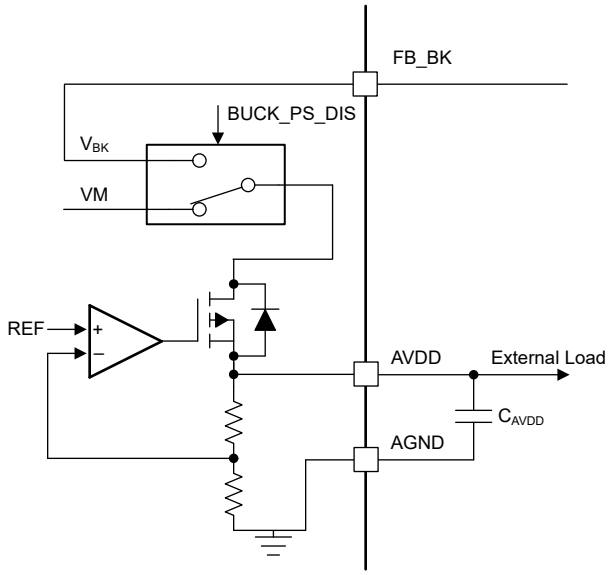


Figure 6-9. AVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply (BUCK_PS_DIS = 1b)

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{VM} of 24V, drawing 20mA out of AVDD results in power dissipation as shown in Equation 2.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (2)$$

Use Equation 3 to calculate the power dissipated in the device by the AVDD linear regulator with buck output as supply (BUCK_PS_DIS = 0b)

$$P = (V_{FB\_BK} - V_{AVDD}) \times I_{AVDD} \quad (3)$$

6.3.5 Charge Pump

Since the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to turn-on the high-side FETs. The MCF8315D integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors (C_{CP}, C_{FLY}) for operation. See Figure 6-10 and Section 4 for details on these capacitors (value, connection, and so forth).

Copyright © 2025 Texas Instruments Incorporated

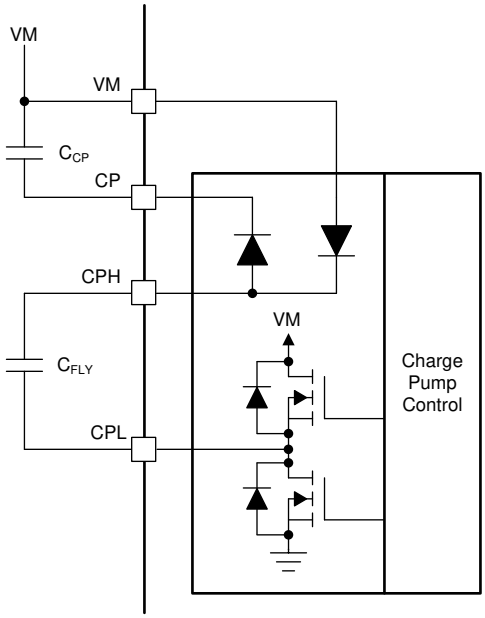


Figure 6-10. Charge Pump

6.3.6 Slew Rate Control

An adjustable gate-drive current control is provided for the output stage MOSFETs to achieve configurable slew rate for EMI mitigation. The MOSFET VDS slew rate is a critical factor for optimizing conducted and radiated emissions, total energy and duration of diode recovery spikes and switching voltage transients related to parasitic elements of the PCB. This slew rate is predominantly determined by the control of the internal MOSFET gate current as shown in Figure 6-11.

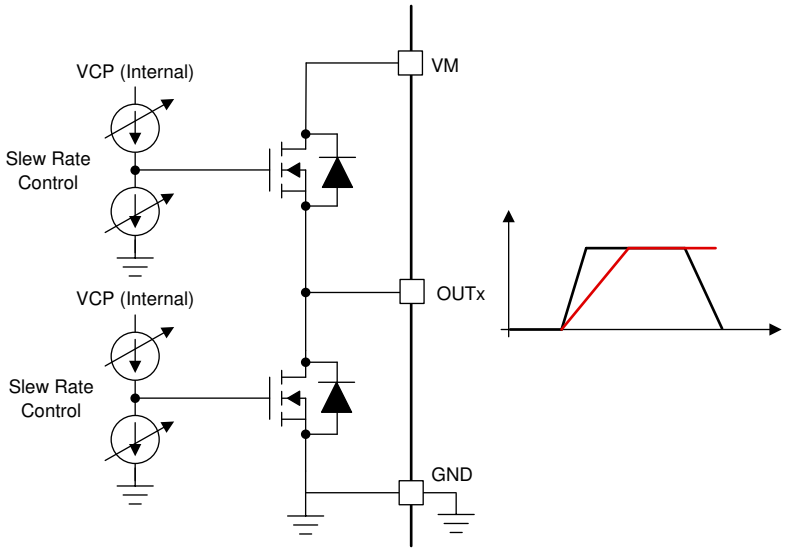


Figure 6-11. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted through SLEW_RATE. The slew rate can be configured as either 125V/µs or 200V/µs. The slew rate is calculated by the rise-time and fall-time of the voltage on the OUTx pin as shown in Figure 6-12.

Copyright © 2025 Texas Instruments Incorporated

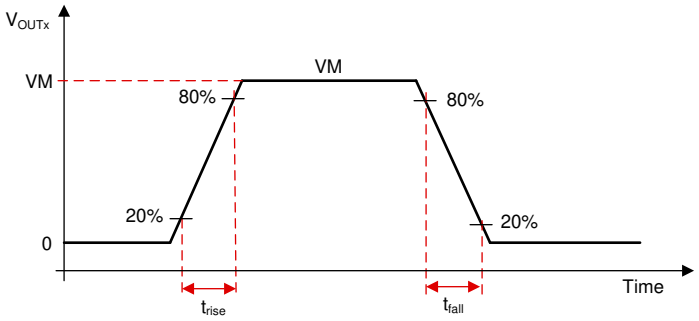


Figure 6-12. Slew Rate Timings

6.3.7 Cross Conduction (Dead Time)

The device is fully protected against any cross conduction of MOSFETs - during the switching of high-side and low-side MOSFETs, MCF8315D avoids shoot-through events by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that VGS of high-side MOSFET has dropped below turn-off level before switching on the low-side MOSFET of same half-bridge (or vice-versa) as shown in Figure 6-13and Figure 6-14. The VGS of the high-side and low-side MOSFETs (VGS_HS and VGS_LS) shown in Figure 6-14 are internal signals.

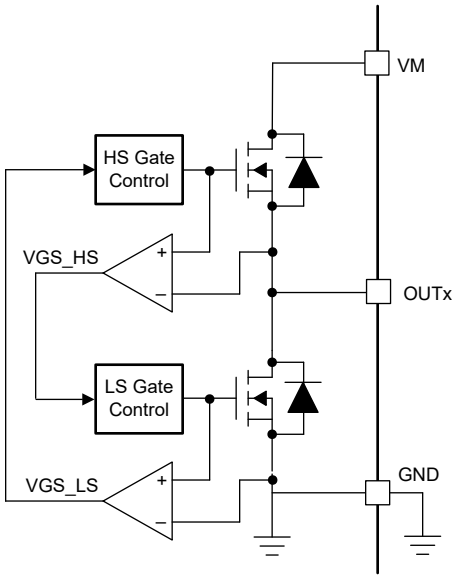


Figure 6-13. Cross Conduction Protection

Copyright © 2025 Texas Instruments Incorporated

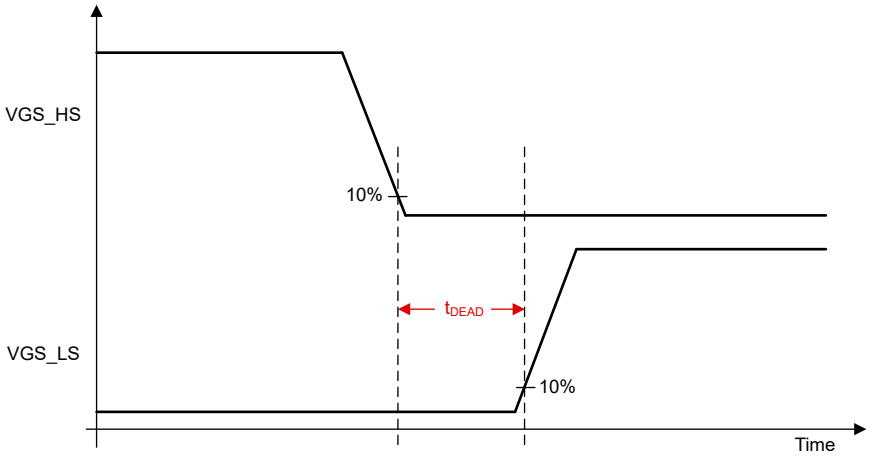


Figure 6-14. Dead Time

Copyright © 2025 Texas Instruments Incorporated

6.3.8 Motor Control Input Sources

The MCF8315D provides four ways of controlling the motor :

1. SPEED Control: In speed control mode, the speed of the motor is controlled using a closed loop PI control according to the input reference.
2. POWER Control: In power control mode, the DC input power of the inverter power stage is controlled using a closed loop PI control according to the input reference.
3. CURRENT Control: In current control mode, the torque generating current (iq) is controlled using a closed loop PI control according to the input reference.
4. VOLTAGE Control: In voltage control mode, the voltage applied to the motor is controlled according to the input reference.

The MCF8315D provides four sources of the reference input for motor control as listed below. The reference input source is configured by SPEED_MODE.

- PWM input on SPEED/WAKE pin by varying duty cycle of input signal
- Frequency input on SPEED/WAKE pin by varying frequency of input signal
- Analog input on SPEED/WAKE pin by varying amplitude of input signal
- Over I^2C by configuring DIGITAL_SPEED_CTRL register

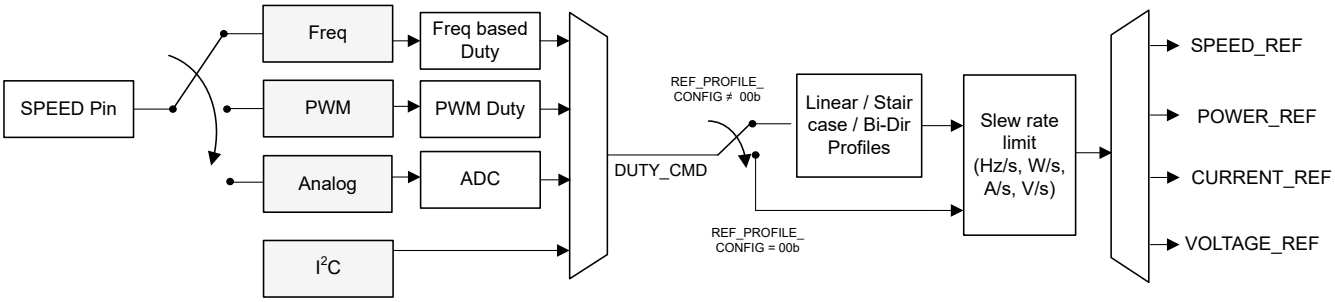


Figure 6-15. Multiplexing the Reference Input Command

The signal path from REF (SPEED/WAKE) pin input (or I^2C based speed input) to output reference (SPEED_REF or POWER_REF or CURRENT_REF or VOLTAGE_REF) shown in Figure 6-15.

6.3.8.1 Analog-Mode Motor Control

Analog input based motor control can be configured by setting SPEED_MODE to 00b. In this mode, the duty command (DUTY_CMD) varies with the analog voltage input on the SPEED pin (V_{SPEED}). When $0 \le V_{SPEED} \le V_{EN\_SB}$, DUTY_CMD is set to zero. When $V_{EX\_SB} \le V_{SPEED} \le V_{ANA\_FS}$, DUTY_CMD varies linearly with V_{SPEED} as shown in Figure 6-16. V_{EX_SB} and V_{EN_SB} are the standby entry and exit thresholds - refer Section 6.4.1.2 for more information on V_{EX_SB} and V_{EN_SB}. When $V_{SPEED} > V_{ANA\_FS}$, DUTY_CMD is clamped to 100%.

Copyright © 2025 Texas Instruments Incorporated

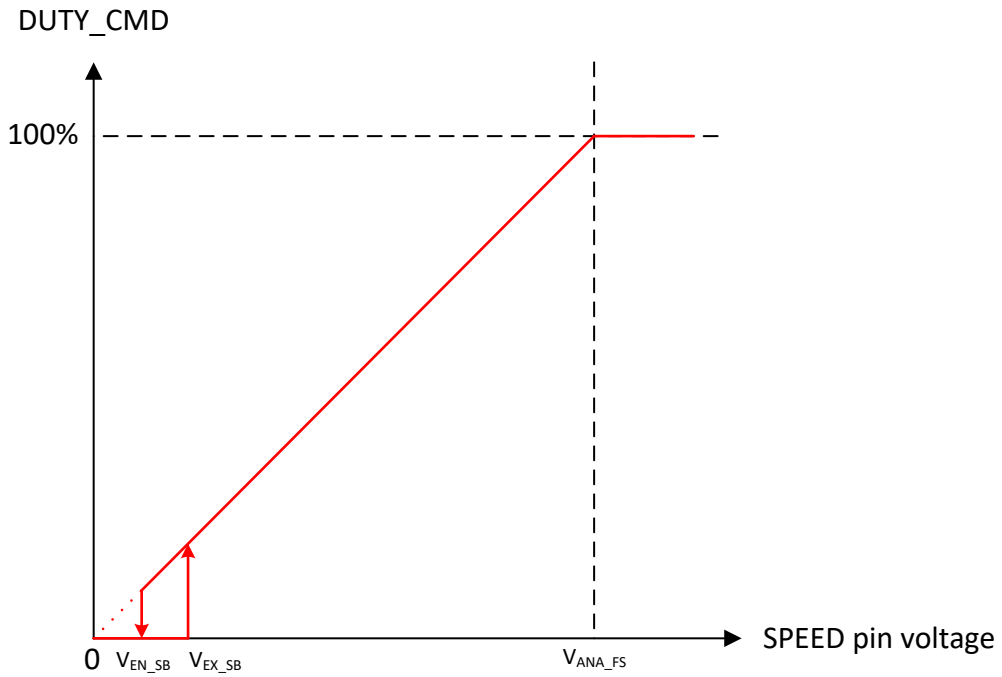


Figure 6-16. Analog-Mode Motor Control

6.3.8.2 PWM-Mode Motor Control

PWM based motor control can be configured by setting SPEED_MODE to 01b. In this mode, the PWM duty cycle applied to the SPEED pin can be varied from 0 to 100% and duty command (DUTY_CMD) varies linearly with the applied PWM duty cycle. When 0 ≤ $Duty_{SPEED}$ ≤ $Duty_{EN\_SB}$, DUTY_CMD is set to zero. When $Duty_{EX\_SB}$ ≤ $Duty_{SPEED}$ ≤ 100%, DUTY_CMD varies linearly with $Duty_{SPEED}$ as shown in Figure 6-17. $Duty_{EX\_SB}$ and $Duty_{EN\_SB}$ are the standby entry and exit thresholds - refer Section 6.4.1.2 for more information on $Duty_{EX\_SB}$ and $Duty_{EN\_SB}$. The frequency of the PWM input signal applied to the SPEED pin is defined as f_{PWM} and the range for this frequency can be configured through SPEED_RANGE_SEL.

Note

1. f_{PWM} is the frequency of the PWM signal the device can accept at SPEED pin to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phases. The PWM output frequency can be configured through PWM_FREQ_OUT (see Section 6.3.17).
2. SLEEP_ENTRY_TIME should be set longer than the off time in PWM signal (V_{SPEED} < V_{IL}) at lowest duty input. For example, if f_{PWM} is 10 kHz and lowest duty input is 2%, SLEEP_ENTRY_TIME should be more than 98 µs to ensure there is no unintended sleep/standby entry.

Copyright © 2025 Texas Instruments Incorporated

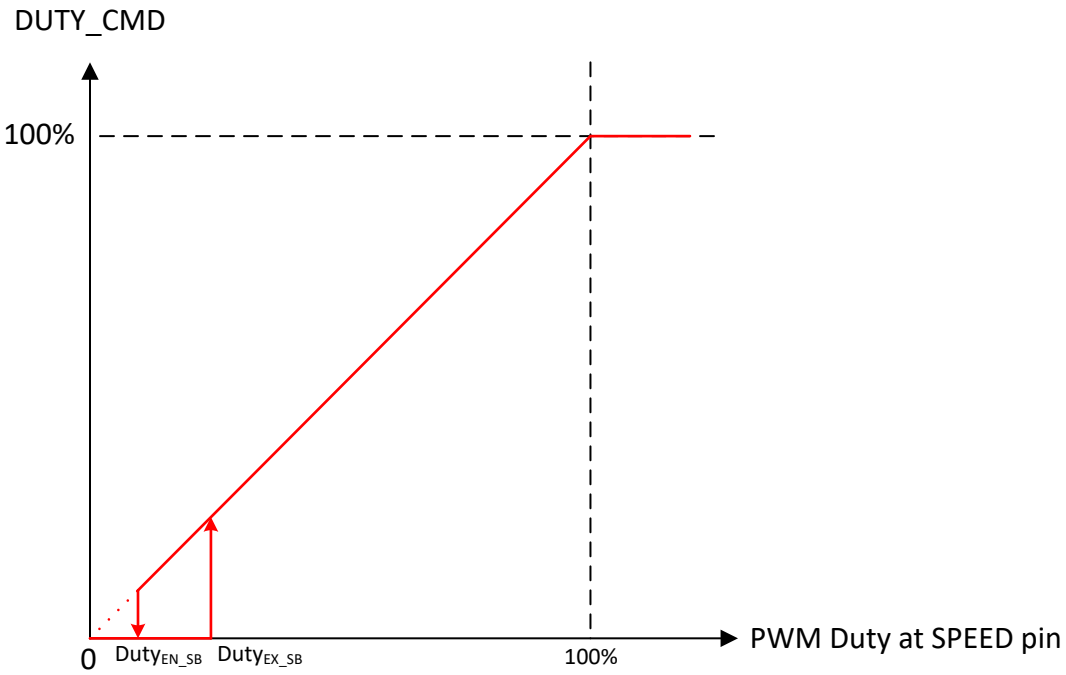


Figure 6-17. PWM-Mode Motor Control

6.3.8.3 I^{2}C-based Motor Control

I^{2}C based serial interface can be used for motor control by setting SPEED_MODE to 10b. In this mode, the control command can be written directly into DIGITAL_SPEED_CTRL register. The SPEED pin can be used to control the sleep entry and exit - if SPEED pin input is set to a value lower than V_{EN_SL} after DIGITAL_SPEED_CTRL register has been set to 0b for a time longer than SLEEP_ENTRY_TIME, MCF8315D enters sleep state. When SPEED pin > V_{EX_SL}, MCF8315D exits sleep state and motor is controlled through DIGITAL_SPEED_CTRL register. If 0 ≤ DIGITAL_SPEED_CTRL register ≤ DIGITAL_SPEED_CTRL$_{EN_SB}$ and SPEED pin > V_{EX_SL}, MCF8315D is in standby state. The relationship between DUTY_CMD and DIGITAL_SPEED_CTRL register is shown in Figure 6-18. Refer Section 6.4.1.2 for more information on DIGITAL_SPEED_CTRL$_{EN_SB\ EX_SB}$ and DIGITAL_SPEED_CTRL$_{EN_SB\ EN_SB}$.

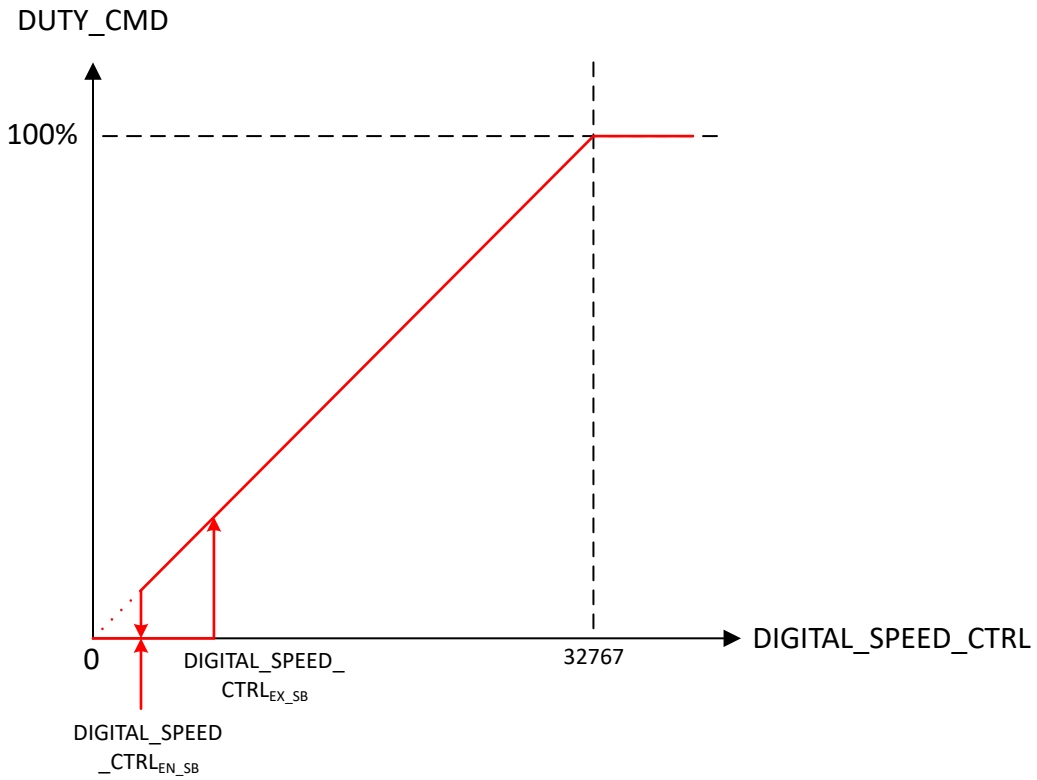


Figure 6-18. I2C Mode Speed Control

6.3.8.4 Frequency-Mode Motor Control

Frequency based motor control is configured by setting SPEED_MODE to 11b. In this mode, duty command varies linearly as a function of the frequency of the square wave input at SPEED/WAKE pin. When 0 ≤ $Freq_{SPEED}$ ≤ $Freq_{EN\_SB}$, DUTY_CMD is set to zero. When $Freq_{EX\_SB}$ ≤ $Freq_{SPEED}$ ≤ INPUT_MAXIMUM_FREQ, DUTY_CMD varies linearly with $Freq_{SPEED}$ as shown in Figure 6-19. $Freq_{EX\_SB}$ and $Freq_{EN\_SB}$ are the standby entry and exit thresholds - refer Section 6.4.1.2 for more information on $Freq_{EX\_SB}$ and $Freq_{EN\_SB}$. Input frequency greater than INPUT_MAXIMUM_FREQ clamps the DUTY_CMD to 100%.

Copyright © 2025 Texas Instruments Incorporated

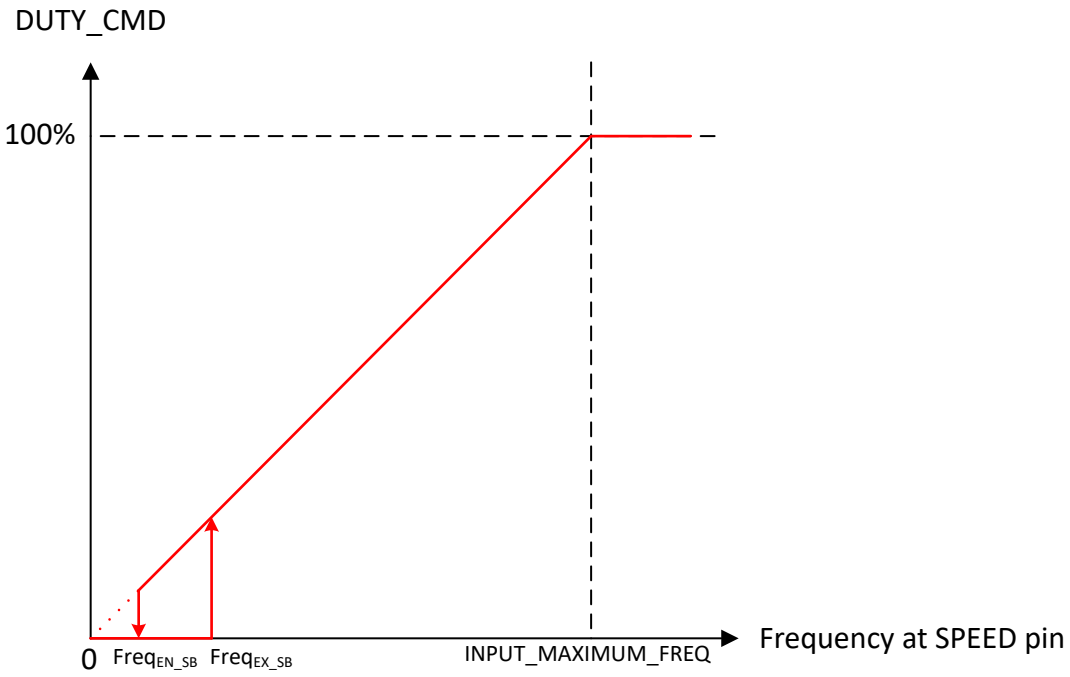


Figure 6-19. Frequency Mode Speed Control

6.3.8.5 Input Reference Profiles

MCF8315D supports three different kinds of input reference profiles (linear, step, forward-reverse) to enable a variety of end-user applications. The different profiles can be configured through REF_PROFILE_CONFIG and the input reference can be a speed, power, current or voltage command as configured by INPUT_REFERENCE_MODE.

In speed reference mode, the profiler output REF_X corresponds to percentage of MAX_SPEED as shown in Equation 4. In power reference mode, the profiler output REF_X corresponds to percentage of MAX_POWER as shown in Equation 5. In current reference mode, the profiler output REF_X corresponds to percentage of ILIMIT as shown in Equation 6. In voltage reference mode, REF_X corresponds to the modulation index applied to the motor.

$$\text{SPEED\_REF (Hz)} = (\text{REF\_X}/255) \times \text{MAX\_SPEED (Hz)} \quad (4)$$

$$\text{POWER\_REF (W)} = (\text{REF\_X}/255) \times \text{MAX\_POWER (W)} \quad (5)$$

$$\text{CURRENT\_REF (A)} = (\text{REF\_X}/255) \times \text{ILIMIT (A)} \quad (6)$$

When REF_PROFILE_CONFIG is set to 00b, the input reference is set by the duty command (DUTY_CMD) as explained in Section 6.3.8.5.5.

6.3.8.5.1 Linear Control Profiles

Note

For all three profiles (linear, step, forward/reverse),

- When MCF8315D is configured as a sleep device, a zero input reference (0V in analog mode, 0% duty in PWM mode, DIGITAL_SPEED_CTRL = 0b in I^2C mode or 0Hz in frequency mode) will stop the motor.
- When MCF8315D is configured as a standby device, a zero input reference will result in motor operating at reference level (speed, power, current or voltage) set by REF_OFF1.

Copyright © 2025 Texas Instruments Incorporated

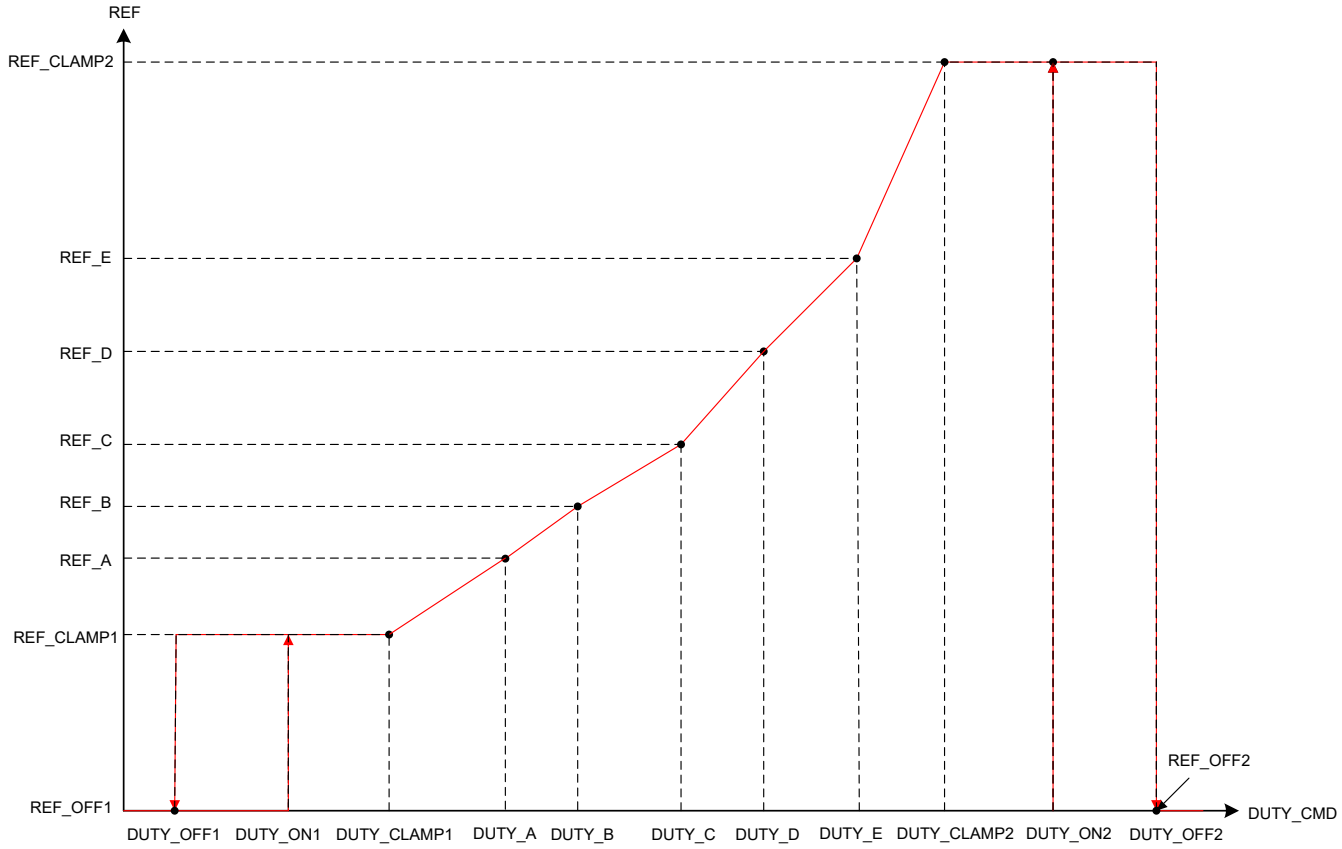


Figure 6-20. Linear Control Profiles

Linear control profiles can be configured by setting REF_PROFILE_CONFIG to 01b. Linear profiles feature input control references which change linearly between REF_CLAMP1 and REF_CLAMP2 with different slopes which can be set by configuring DUTY_x and REF_x combination.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.
- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 6-20.
- DUTY_CLAMP1 configures the duty command till which reference will be constant with a value REF_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. The reference changes from REF_CLAMP1 to REF_A linearly between DUTY_CLAMP1 and DUTY_A. DUTY_A to DUTY_E has to be in the same order as shown in Figure 6-20.
- DUTY_B configures the duty command for reference REF_B. The reference changes linearly between DUTY_A and DUTY_B.
- DUTY_C configures the duty command for reference REF_C. The reference changes linearly between DUTY_B and DUTY_C.
- DUTY_D configures the duty command for reference REF_D. The reference changes linearly between DUTY_C and DUTY_D.
- DUTY_E configures the duty command for reference REF_E. The reference changes linearly between DUTY_D and DUTY_E.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2 . The reference changes linearly between DUTY_E and DUTY_CLAMP2. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.

Copyright © 2025 Texas Instruments Incorporated

- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 6-20.
- DUTY_OFF2 configures the duty command above which the reference will change from REF_CLAMP2 to REF_OFF2.

6.3.8.5.2 Staircase Control Profiles

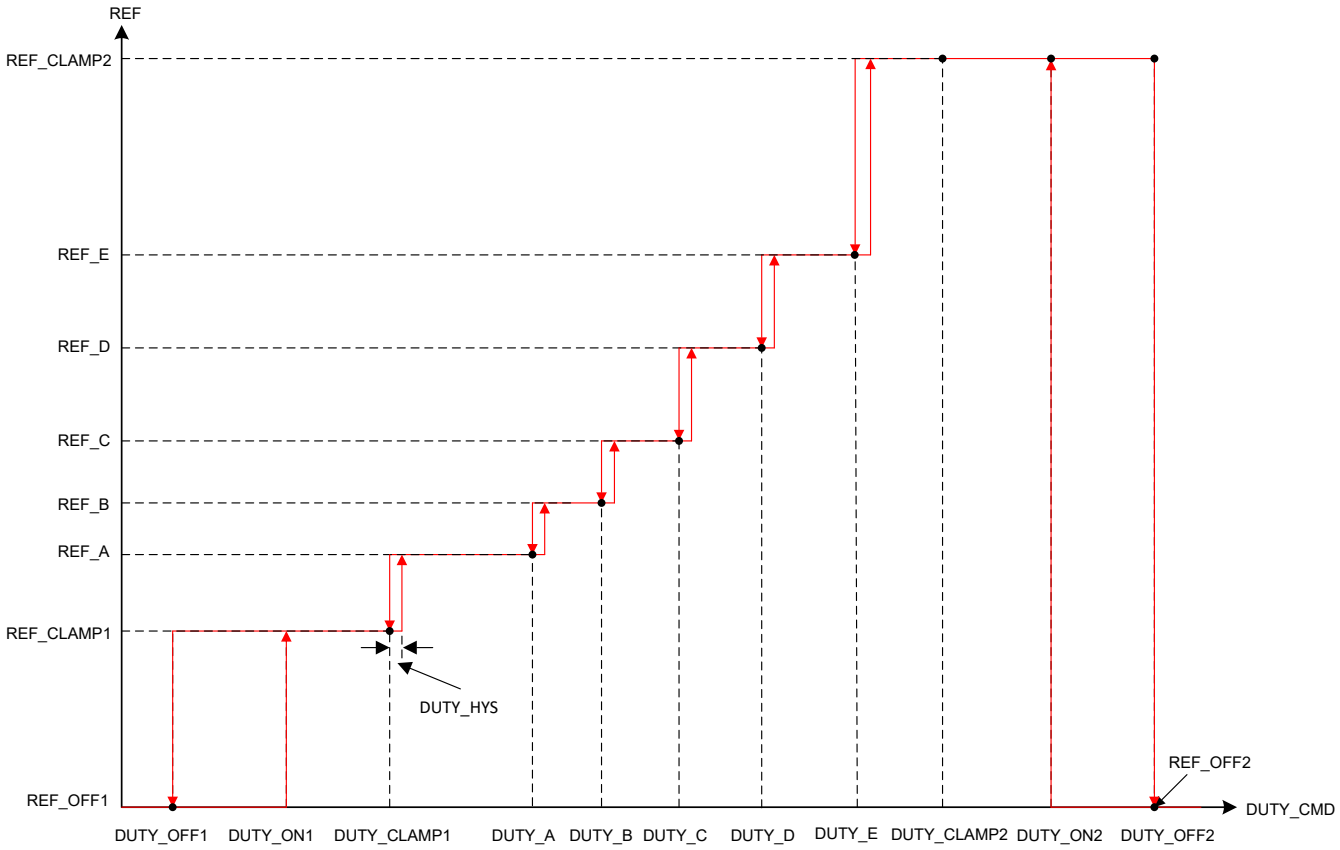


Figure 6-21. Staircase Control Profiles

Staircase control profiles can be configured by setting REF_PROFILE_CONFIG to 10b. Staircase profiles feature input control reference changes in steps between REF_CLAMP1 and REF_CLAMP2, by configuring DUTY_x and REF_x.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.
- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 6-21.
- DUTY_CLAMP1 configures the duty command till which reference will be constant. REF_CLAMP1 configures this constant reference between DUTY_OFF1 and DUTY_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. There is a step change in reference from REF_CLAMP1 to REF_A at DUTY_CLAMP1. DUTY_A to DUTY_E has to be in the same order as shown in Figure 6-21.
- DUTY_B configures the duty command for reference REF_B. There is a step change in reference from REF_A to REF_B at DUTY_A.
- DUTY_C configures the duty command for reference REF_C. There is a step change in reference from REF_B to REF_C at DUTY_B.
- DUTY_D configures the duty command for reference REF_D. There is a step change in reference from REF_C to REF_D at DUTY_C.

Copyright © 2025 Texas Instruments Incorporated

- DUTY_E configures the duty command for reference REF_E. There is a step change in reference from REF_D to REF_E at DUTY_D.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2. There is a step change in reference from REF_E to REF_CLAMP2 at DUTY_E. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.
- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 6-21.
- DUTY_OFF2 configures the duty command above which the reference will change from REF_CLAMP2 to REF_OFF2.
- DUTY_HYS configures the hysteresis during every step change at DUTY_CLAMP1, DUTY_A to DUTY_E.

6.3.8.5.3 Forward-Reverse Profiles

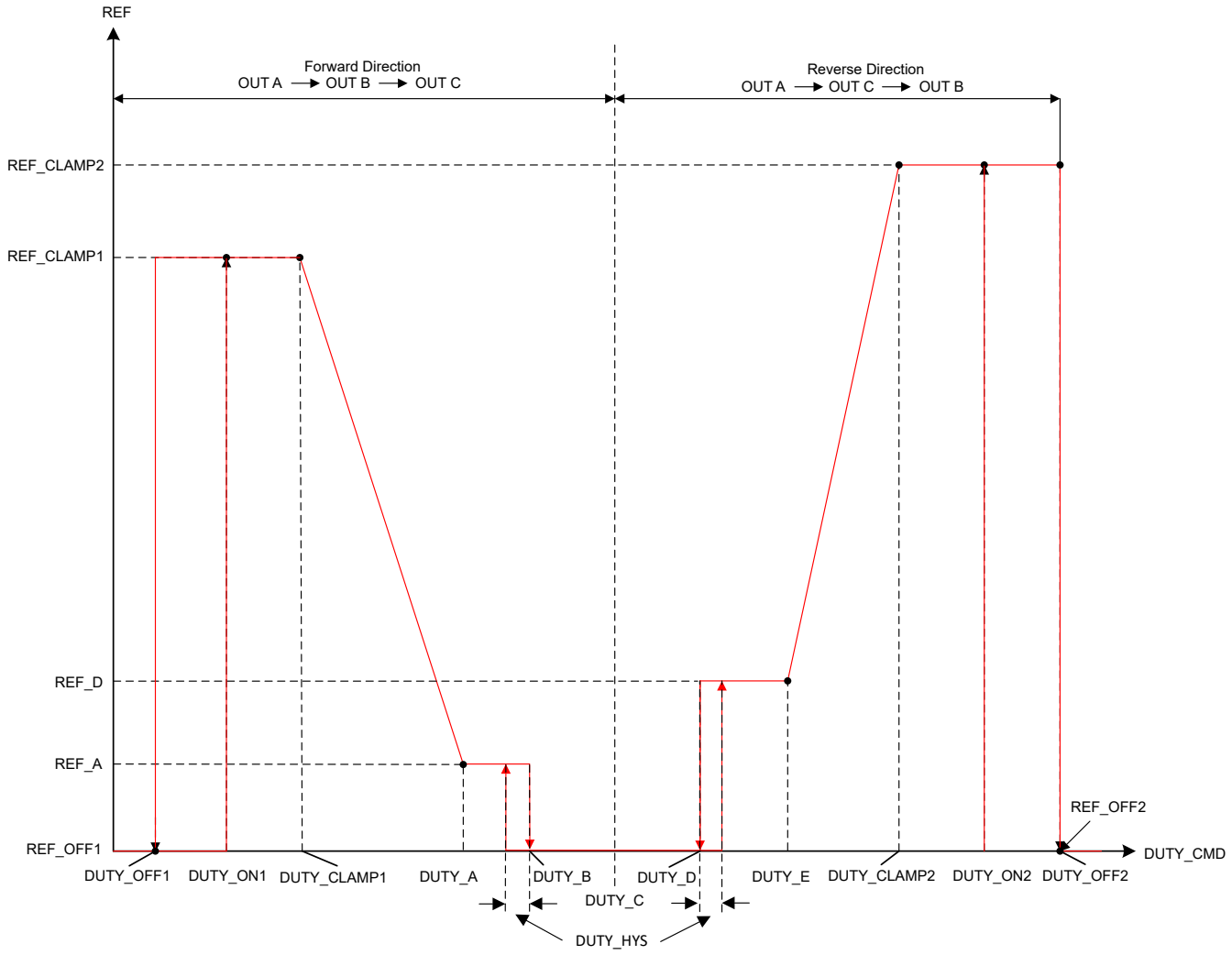


Figure 6-22. Forward Reverse Control Profiles

Forward-Reverse control profiles can be configured by setting REF_PROFILE_CONFIG to 11b. Forward-Reverse profiles feature direction change through adjusting the duty command. DUTY_C configures duty command at which the direction will be changed. The Forward-Reverse speed profile can be used to eliminate the separate signal used to control the motor direction.

Copyright © 2025 Texas Instruments Incorporated

Note

The direction change functionality through DIR pin and DIR_INPUT bits are disabled in forward reverse profile mode.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.
- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 6-22.
- DUTY_CLAMP1 configures the duty command till which reference will be constant. REF_CLAMP1 configures this constant reference between DUTY_OFF1 and DUTY_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. The reference changes linearly between DUTY_CLAMP1 and DUTY_A. DUTY_A to DUTY_E has to be in the same order as shown in Figure 6-22.
- DUTY_B configures the duty command above which MCF8315D will be in off state. The reference remains constant at REF_A between DUTY_A and DUTY_B.
- DUTY_C configures the duty command at which the direction is changed
- DUTY_D configures the duty command above which the MCF8315D will be in running state in the reverse direction. REF_D configures constant reference between DUTY_D and DUTY_E.
- DUTY_E configures the duty command above which reference changes linearly between DUTY_E and DUTY_CLAMP2.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.
- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 6-22.
- DUTY_OFF2 configures the duty command above which the reference changes in the reverse direction from REF_CLAMP2 to REF_OFF2.
- DUTY_HYS configures the hysteresis during step change at DUTY_B and DUTY_D.

6.3.8.5.4 Multi-Reference Mode Operation

Note

The multi-reference (mixed) mode operation is available only when REF_PROFILE_CONFIG is set 01b (linear profile) or 10b (staircase profile).

MCF8315D provides the option of multi-reference mode operation when VOLTAGE_MODE_CONFIG is set to 01b or 10b. When VOLTAGE_MODE_CONFIG is set to 01b, MCF8315D operates in speed, current or power reference mode till DUTY_CMD reaches DUTY_C and then switches to voltage reference mode from DUTY_C till 100% duty command as shown in Figure 6-23.

Copyright © 2025 Texas Instruments Incorporated

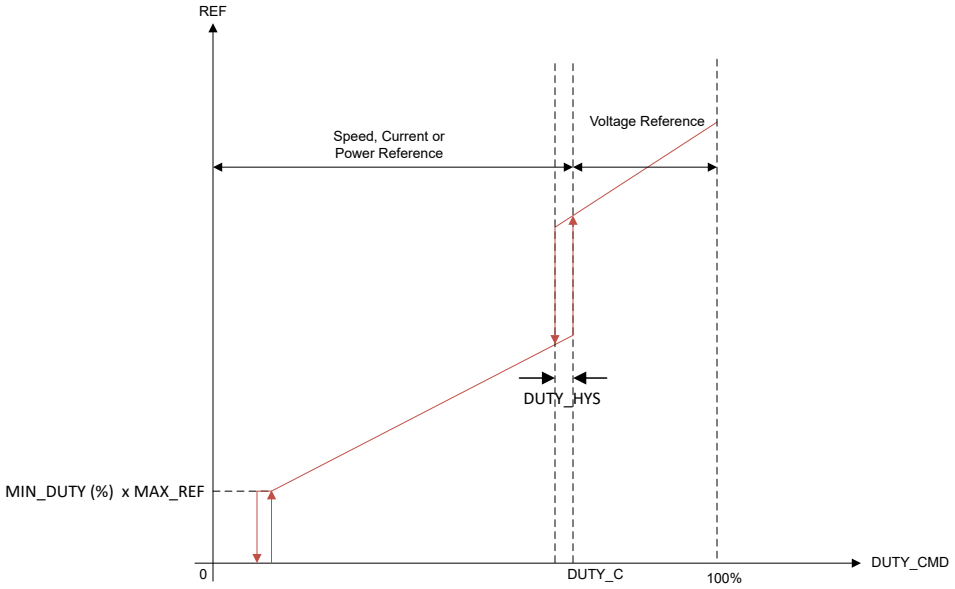


Figure 6-23. Multi-Reference Mode Operation (when VOLTAGE_MODE_CONFIG = 01b)

Conversely, MCF8315D operates in voltage reference mode till DUTY_C and then switches to speed, current or power reference from DUTY_C till 100% duty command when VOLTAGE_MODE_CONFIG is set to 10b as shown in Figure 6-24.

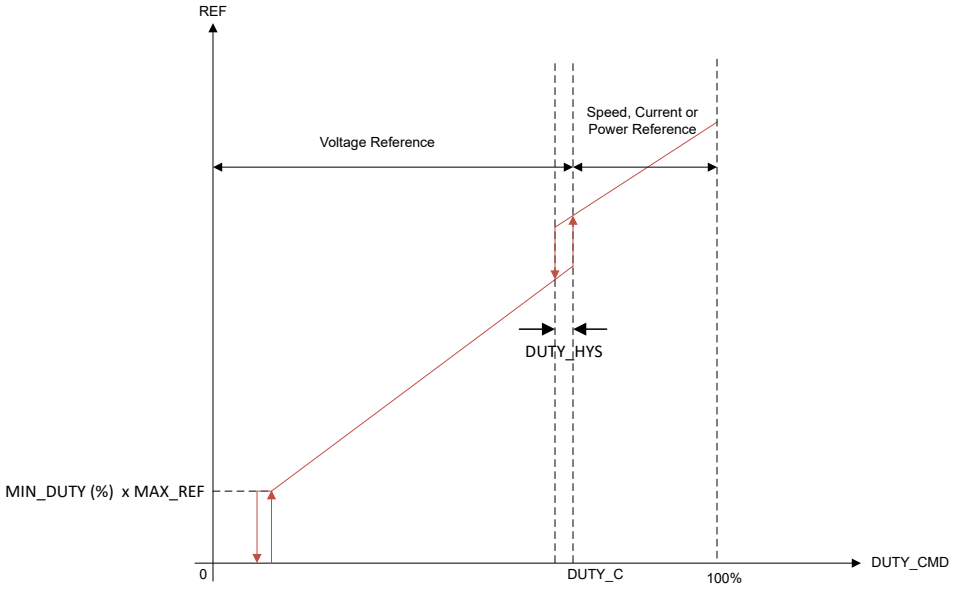


Figure 6-24. Multi-Reference Mode Operation (when VOLTAGE_MODE_CONFIG = 10b)

6.3.8.5.5 Input Reference Transfer Function without Profiler

The input reference can be a speed, power, current or voltage command as configured by INPUT_REFERENCE_MODE.

Copyright © 2025 Texas Instruments Incorporated

Note

- In this mode, if MIN_DUTY < REF_CLAMP1, the minimum reference is set by REF_CLAMP1 and not MIN_DUTY. For example, if MIN_DUTY is set to 1% and REF_CLAMP1 set to 5%, the minimum reference is REF_CLAMP1 x MAX_REFERENCE. MAX_REFERENCE can be MAX_SPEED, MAX_POWER, ILIMIT or 100% depending on input reference mode.
- Set MIN_DUTY > REF_CLAMP1 for using MIN_DUTY to set the minimum reference.

Speed Reference Transfer Function

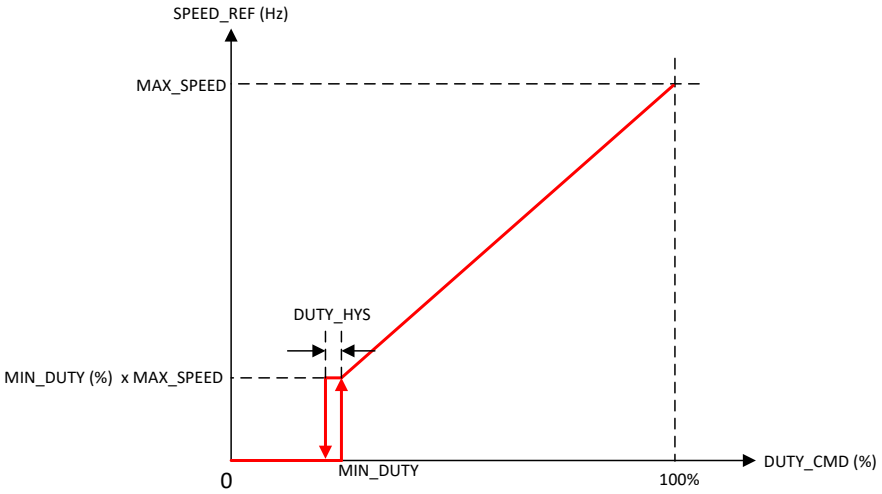


Figure 6-25. Speed Reference Transfer Function

Figure 6-25 shows the relationship between DUTY_CMD and SPEED_REF. MAX_SPEED sets the SPEED_REF at DUTY_CMD of 100%. MIN_DUTY sets the minimum SPEED_REF (MIN_DUTY x MAX_SPEED). If MAX_SPEED is set to 0-Hz, SPEED_REF is clamped to zero (irrespective of DUTY_CMD) and motor is in stopped state.

Power Reference Transfer Function

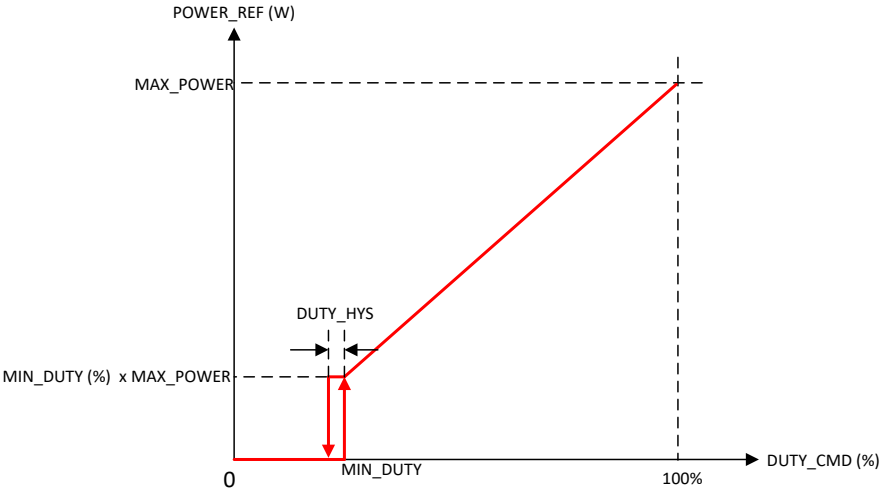


Figure 6-26. Power Reference Transfer Function

Figure 6-26 shows the relationship between DUTY_CMD and POWER_REF. MAX_POWER sets the POWER_REF at DUTY_CMD of 100%. MIN_DUTY sets the minimum POWER_REF (MIN_DUTY x

Copyright © 2025 Texas Instruments Incorporated

MAX_POWER). If MAX_POWER is set to 0-W, POWER_REF is clamped to zero (irrespective of DUTY_CMD) and motor is in stopped state.

Voltage Reference Transfer Function

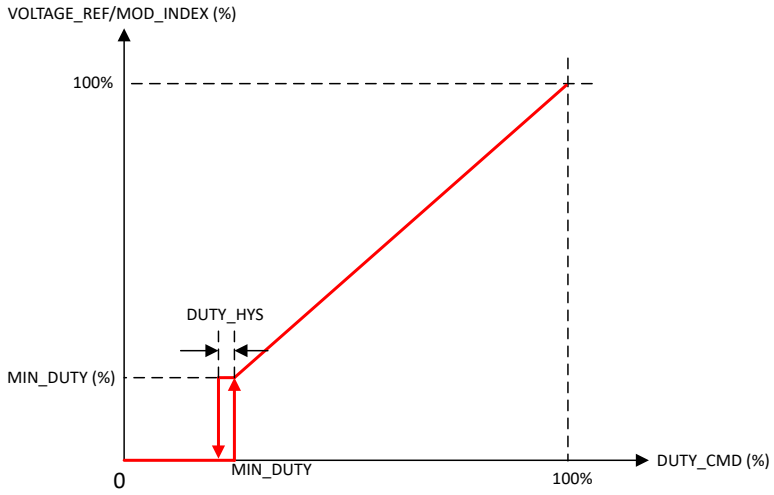


Figure 6-27. Voltage Reference Transfer Function

In voltage reference mode, the phase voltage applied to motor is proportional to the DUTY_CMD (from MIN_DUTY to 100%) as shown in Figure 6-27. For DUTY_CMD less than MIN_DUTY, the applied voltage to motor is clamped to zero.

Current Input Transfer Function

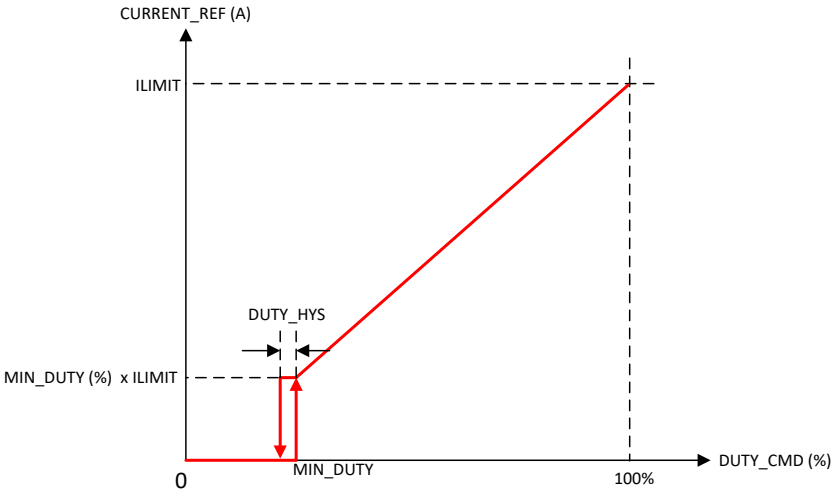


Figure 6-28. Current Reference Transfer Function

Figure 6-28 shows the relationship between DUTY_CMD and CURRENT_REF. ILIMIT sets the CURRENT_REF at DUTY_CMD of 100%. MIN_DUTY sets the minimum CURRENT_REF (MIN_DUTY x ILIMIT).

6.3.9 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when MCF8315D begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCF8315D includes a number of features to allow for reliable motor start-up under all of these conditions. Figure 6-29 shows the motor start-up flow for each of the three initial motor states.

Copyright © 2025 Texas Instruments Incorporated

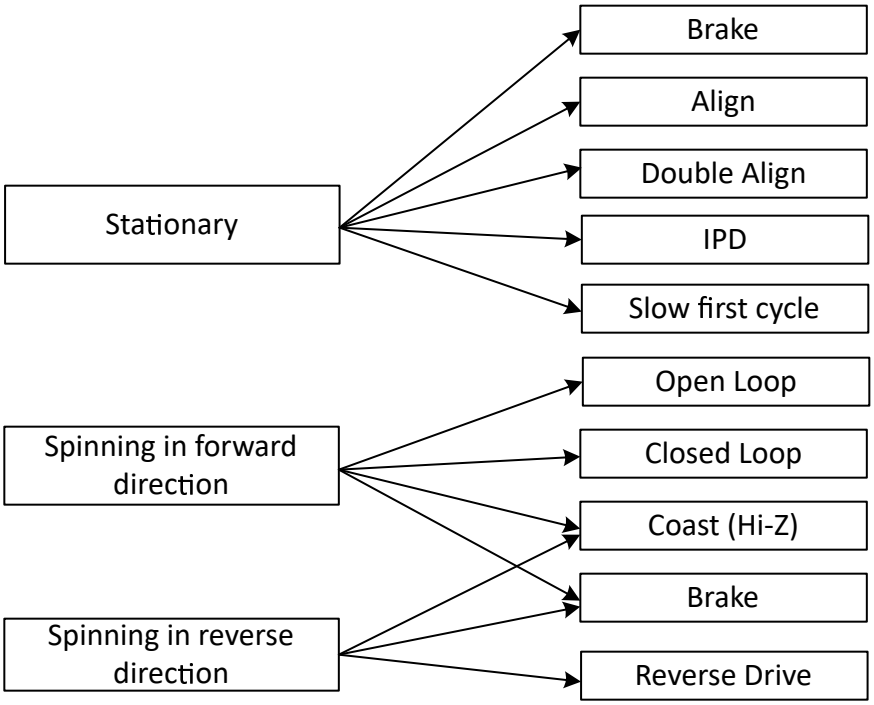


Figure 6-29. Starting the motor under different initial conditions

Note

"Forward" means "spinning in the same direction as the commanded direction", and "Reverse" means "spinning in the opposite direction as the commanded direction".

6.3.9.1 Case 1 – Motor is Stationary

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCF8315D provides various options to initialize the commutation logic to the motor position and reliably start the motor.

- The align and double align techniques force the motor into alignment by applying a voltage across particular motor phases to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The slow first cycle method starts the motor by applying a low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

MCF8315D also provides a configurable brake option to ensure the motor is stationary before initiating one of the above start-up methods. Device enters open loop acceleration after going through the configured start-up method.

6.3.9.2 Case 2 – Motor is Spinning in the Forward Direction

If the motor is spinning forward (same direction as the commanded direction) with sufficient speed (BEMF), the MCF8315D resynchronizes with the spinning motor and continues commutation by going directly to closed loop operation. If the motor speed is too low for closed loop operation, MCF8315D enters open loop operation to accelerate the motor till it reaches sufficient speed to enter closed loop operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. This resynchronization feature can be enabled or disabled through RESYNC_EN. If resynchronization is disabled, the MCF8315D can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

Copyright © 2025 Texas Instruments Incorporated

6.3.9.3 Case 3 – Motor is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction (the opposite direction as the commanded direction), the MCF8315D provides several methods to change the direction and drive the motor to the target speed reference in the commanded direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero speed.

If reverse drive is not enabled, then the MCF8315D can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

Note

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

Copyright © 2025 Texas Instruments Incorporated

6.3.10 Motor Start Sequence (MSS)

Figure 6-30 shows the motor-start sequence implemented in the MCF8315D device.

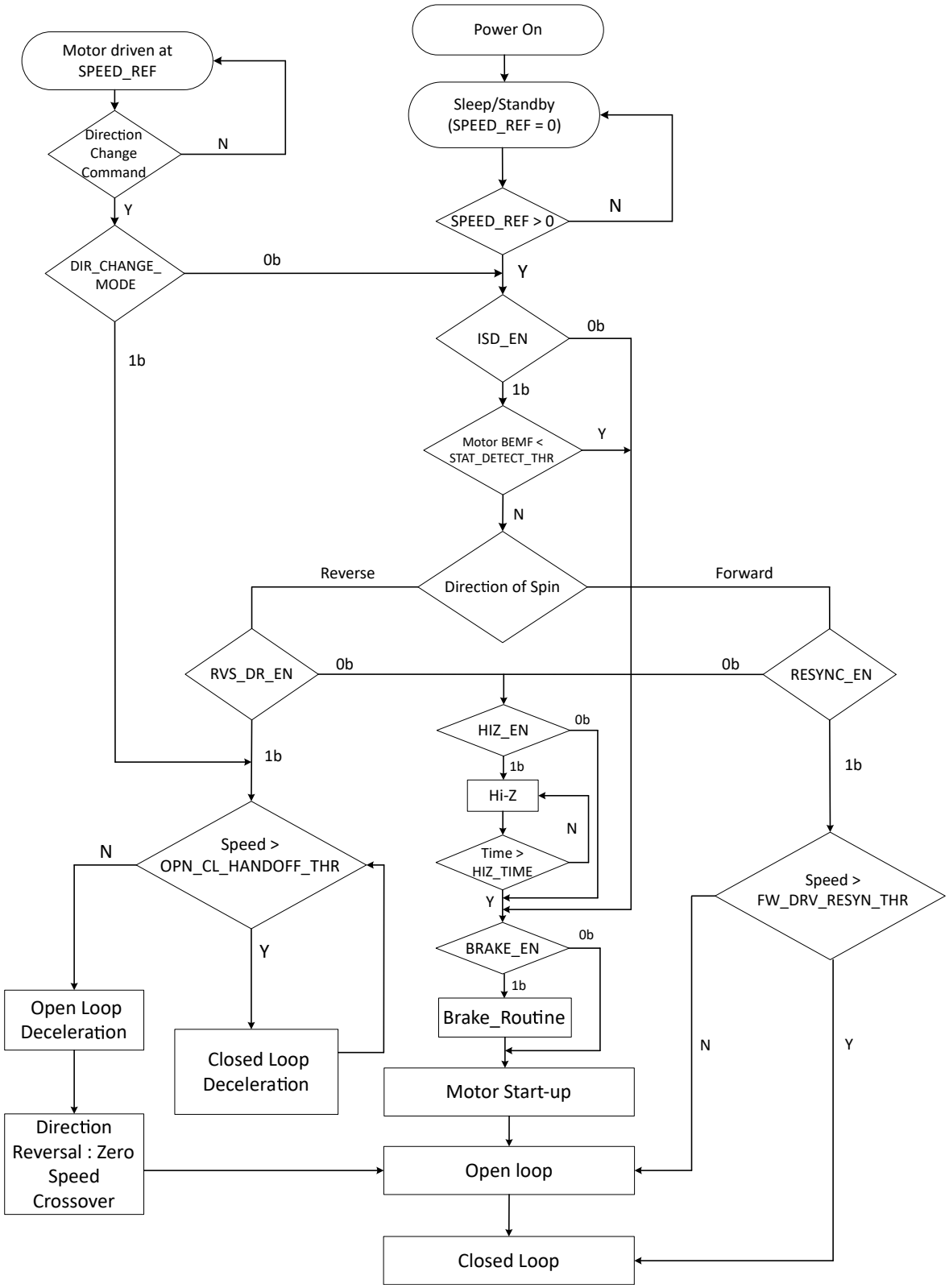


Figure 6-30. Motor Start Sequence

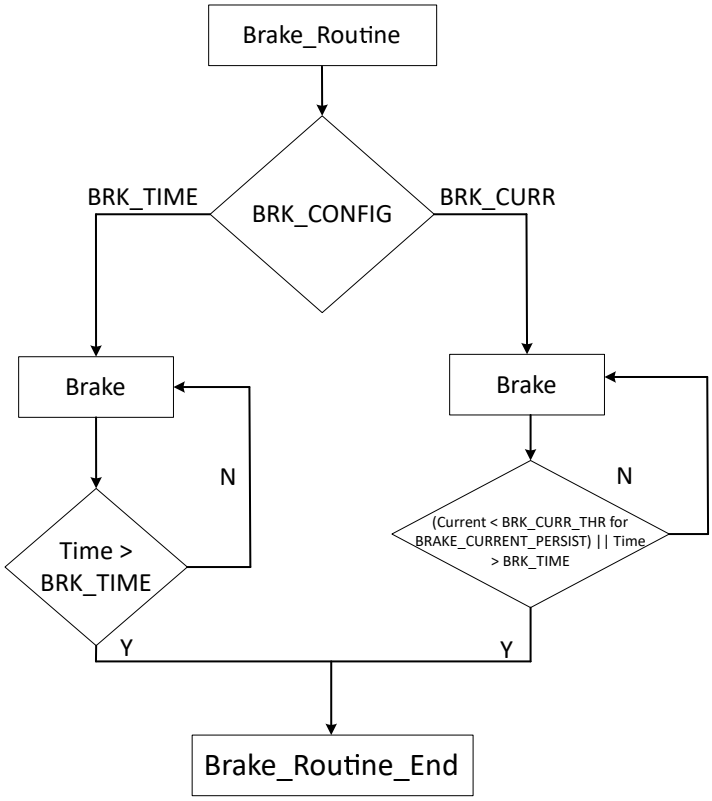


Figure 6-31. Brake Routine

Power-On State	This is the initial state of the Motor Start Sequence (MSS) when MCF8315D is powered on. In this state, MCF8315D configures the peripherals, initializes the algorithm parameters from EEPROM and prepares for driving the motor.
Sleep/Standby	In this state, SPEED_REF is set to zero and MCF8315D is either in sleep or standby mode depending on DEV_MODE and SPEED/WAKE pin voltage.
SPEED_REF > 0 Judgement	When SPEED_REF is set to greater than zero, MCF8315D exits the sleep/ standby state and proceeds to ISD_EN judgement. As long as SPEED_REF is set to zero, MCF8315D stays in sleep/standby state.
Direction Change Command Judgement	When a direction change command is received, MCF8315D proceeds to DIR_CHANGE_MODE judgement.
DIR_CHANGE_MODE Judgement	If DIR_CHANGE_MODE is set to 0b, MCF8315D initiates direction change by proceeding to ISD_EN judgement. Instead, if DIR_CHANGE_MODE is set to 1b, MCF8315D initiates direction change by proceeding to Speed > OPN_CL_HANDOFF_THR judgement.
ISD_EN Judgement	MCF8315D checks to see if the initial speed detect (ISD) function is enabled (ISD_EN = 1b). If ISD is enabled, MSS proceeds to the BEMF < STAT_DETECT_THR judgement. Instead, if ISD is disabled, the MSS proceeds directly to the BRAKE_EN judgement.
BEMF < STAT_DETECT_THR Judgement	ISD determines the initial condition (speed, angle, direction of spin) of the motor (see Section 6.3.10.1). If motor is deemed to be stationary (BEMF < STAT_DETECT_THR), the MSS proceeds to BRAKE_EN judgement. If the motor is not stationary, MSS proceeds to verify the direction of spin.
Direction of spin Judgement	The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the

Copyright © 2025 Texas Instruments Incorporated

	MCF8315D proceeds to the RESYNC_EN judgement. If the motor is spinning in the reverse direction, the MSS proceeds to the RVS_DR_EN judgement.
RESYNC_EN Judgement	If RESYNC_EN is set to 1b, MCF8315D proceeds to Speed > Open to Closed Loop Handoff (Resync) judgement. If RESYNC_EN is set to 0b, MSS proceeds to HIZ_EN judgement.
Speed > FW_DRV_RESYN_THR Judgement	If motor speed > FW_DRV_RESYN_THR, MCF8315D uses the speed and position information from the ISD to transition to the closed loop state (see Section 6.3.10.2) directly. If motor speed < FW_DRV_RESYN_THR, MCF8315D transitions to open loop state.
RVS_DR_EN Judgement	The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1b). If it is enabled, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled (RVS_DR_EN = 0b), the MSS advances to the HIZ_EN judgement.
Speed > OPN_CL_HANDOFF_THR Judgement	The MSS checks to see if the reverse speed is high enough for MCF8315D to decelerate in closed loop. Till the speed (in reverse direction) is above OL_CL_HANDOFF_THR, MSS stays in closed loop deceleration. If speed is below OPN_CL_HANDOFF_THR, then the MSS transitions to open loop deceleration.
Reverse Closed Loop, Open Loop Deceleration and Zero Speed Crossover	The MCF8315D resynchronizes in the reverse direction, decelerates the motor in closed loop till motor speed falls below the handoff threshold. (see *Reverse Drive*). When motor speed in reverse direction is too low, the MCF8315D switches to open-loop, decelerates the motor in open-loop, crosses zero speed, and accelerates in the forward direction in open-loop before entering closed loop operation after motor speed is sufficiently high.
HIZ_EN Judgement	The MSS checks to determine whether the coast (Hi-Z) function is enabled (HIZ_EN = 1b). If the coast function is enabled (HIZ_EN = 1b), the MSS advances to the coast routine. If the coast function is disabled (HIZ_EN = 0b), the MSS advances to the BRAKE_EN judgement.
Coast (Hi-Z) Routine	The device coasts the motor by turning OFF all six MOSFETs for a certain time configured by HIZ_TIME.
BRAKE_EN Judgement	The MSS checks to determine whether the brake function is enabled (BRAKE_EN = 1b). If the brake function is enabled (BRAKE_EN = 1b), the MSS advances to the brake routine. If the brake function is disabled (BRAKE_EN = 0b), the MSS advances to the motor start-up state (see Section 6.3.10.4).
Brake Routine	MCF8315D implements either a time based brake (duration configured by BRK_TIME) or a current based brake (brake applied till phase currents < BRK_CURR_THR for BRAKE_CURRENT_PERSIST) based on BRK_CONFIG. Current based brake has a timeout to ensure brake state ends in case phase currents do not drop below BRK_CURR_THR within BRK_TIME. Time based brake can be applied either using high-side or low-side MOSFETs based on BRK_MODE configuration. Current based brake is applied using low-side MOSFETs only.
Closed Loop State	In this state, the MCF8315D drives the motor with sensorless FOC based on rotor angle estimation.

6.3.10.1 Initial Speed Detect (ISD)

The ISD function is used to identify the initial condition of the motor and is enabled by setting ISD_EN to 1b. The initial speed, position and direction is determined by sensing the three phase voltages. ISD can be disabled by setting ISD_EN to 0b. If the function is disabled (ISD_EN set to 0b), the MCF8315D does not perform the initial speed detect function and proceeds to check if the brake routine (BRAKE_EN) is enabled.

Copyright © 2025 Texas Instruments Incorporated

6.3.10.2 Motor Resynchronization

The motor resynchronization function works when the ISD and resynchronization functions are both enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the commanded direction). The speed and position information measured during ISD are used to initialize the drive state of the MCF8315D , which can transition directly into closed loop (or open loop if motor speed is not sufficient for closed loop operation) state without needing to stop the motor. In the MCF8315D , motor resynchronization can be enabled/disabled through RESYNC_EN bit. If motor resynchronization is disabled, the device proceeds to check if the motor coast (Hi-Z) routine is enabled.

6.3.10.3 Reverse Drive

The MCF8315D uses the reverse drive function to change the direction of the motor rotation when ISD_EN and RVS_DR_EN are both set to 1b and the ISD determines the motor spin direction to be opposite to that of the commanded direction. Reverse drive includes synchronizing with the motor speed in the reverse direction, reverse decelerating the motor through zero speed, changing direction, and accelerating in open loop in forward (or commanded) direction until the device transitions into closed loop in forward direction (see Figure 6-32). MCF8315D provides the option of using the forward direction parameters or a separate set of reverse drive parameters by configuring REV_DRV_CONFIG.

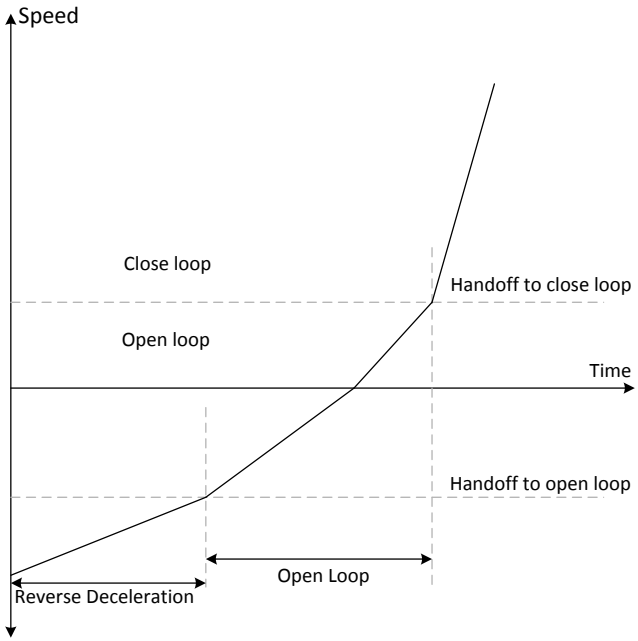


Figure 6-32. Reverse Drive Function

6.3.10.3.1 Reverse Drive Tuning

MCF8315D provides the option of tuning the open to closed loop handoff threshold, open loop acceleration (and deceleration) rates and open loop current limit in reverse drive to values different to those used in forward drive operation; the reverse drive specific parameters can be used by setting REV_DRV_CONFIG to 1b. If REV_DRV_CONFIG is set to 0b, MCF8315D uses the equivalent parameters configured for forward drive operation during the reverse drive operation too.

The speed at which motor would enter the open loop in reverse direction can be configured using REV_DRV_HANDOFF_THR. For a smooth transition without jerks or loss of synchronism, user can configure an appropriate current limit when the motor is spinning in open loop during speed reversal using REV_DRV_OPEN_LOOP_CURRENT. The open loop acceleration rates for the forward direction during speed reversal are defined using REV_DRV_OPEN_LOOP_ACCEL_A1 and REV_DRV_OPEN_LOOP_ACCEL_A2. The reverse drive open loop deceleration rate, when the motor is decelerating in the opposite direction

Copyright © 2025 Texas Instruments Incorporated

to zero speed, can be configured as a percentage of reverse drive open loop acceleration using REV_DRV_OPEN_LOOP_DEC.

6.3.10.4 Motor Start-up

There are different options available for motor start-up from a stationary position and these options can be configured by MTR_STARTUP. In align and double align mode, the motor is aligned to a known position by injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle.

6.3.10.4.1 Align

Align is enabled by configuring MTR_STARTUP to 00b. The MCF8315D aligns the motor by injecting a DC current through a particular phase pattern for a certain time configured by ALIGN_TIME. The phase pattern during align is generated based on ALIGN_ANGLE. In the MCF8315D, the current limit during align is configured through ALIGN_OR_SLOW_CURRENT_ILIMIT.

A fast change in the phase current may result in a sudden change in the driving torque and this could result in acoustic noise. To avoid this, the MCF8315D ramps up the current from 0 to the current limit at a configurable ramp rate set by ALIGN_SLOW_RAMP_RATE. At the end of align routine, the motor will be aligned at the known position.

6.3.10.4.2 Double Align

Double align is enabled by configuring MTR_STARTUP to 01b. Single align is not reliable when the initial position of the rotor is 180° out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In order to improve the reliability of align based start-up, the MCF8315D provides the option of double align start-up. In double align start-up, MCF8315D uses a phase pattern for the second align that is 90° ahead of the first align phase pattern. In double align, relevant parameters like align time, current limit, ramp rate are the same as in the case of single align - two different phase patterns are applied in succession with the same parameters to ensure that the motor will be aligned to a known position irrespective of initial rotor position.

6.3.10.4.3 Initial Position Detection (IPD)

Initial Position Detection (IPD) can be enabled by configuring MTR_STARTUP to 10b. In IPD, inductive sense method is used to determine the initial position of the motor using the spatial variation in the motor inductance.

Align or double align may result in the motor spinning in the reverse direction before starting open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. IPD does not wait for the motor to align with the commutation and therefore can allow for a faster motor start-up sequence. IPD works well when the inductance of the motor varies as a function of position. IPD works by pulsing current in to the motor and hence can generate acoustics which must be taken into account when determining the best start-up method for a particular application.

6.3.10.4.3.1 IPD Operation

IPD operates by sequentially applying six different phase patterns according to the following sequence: BC-> CB-> AB-> BA-> CA-> AC (see Figure 6-33). When the current reaches the threshold configured by IPD_CURR_THR, the MCF8315D stops driving the particular phase pattern and measures the time taken to reach the current threshold from when the particular phase pattern was applied. Thus, the time taken to reach IPD_CURR_THR is measured for all six phase patterns - this time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

Copyright © 2025 Texas Instruments Incorporated

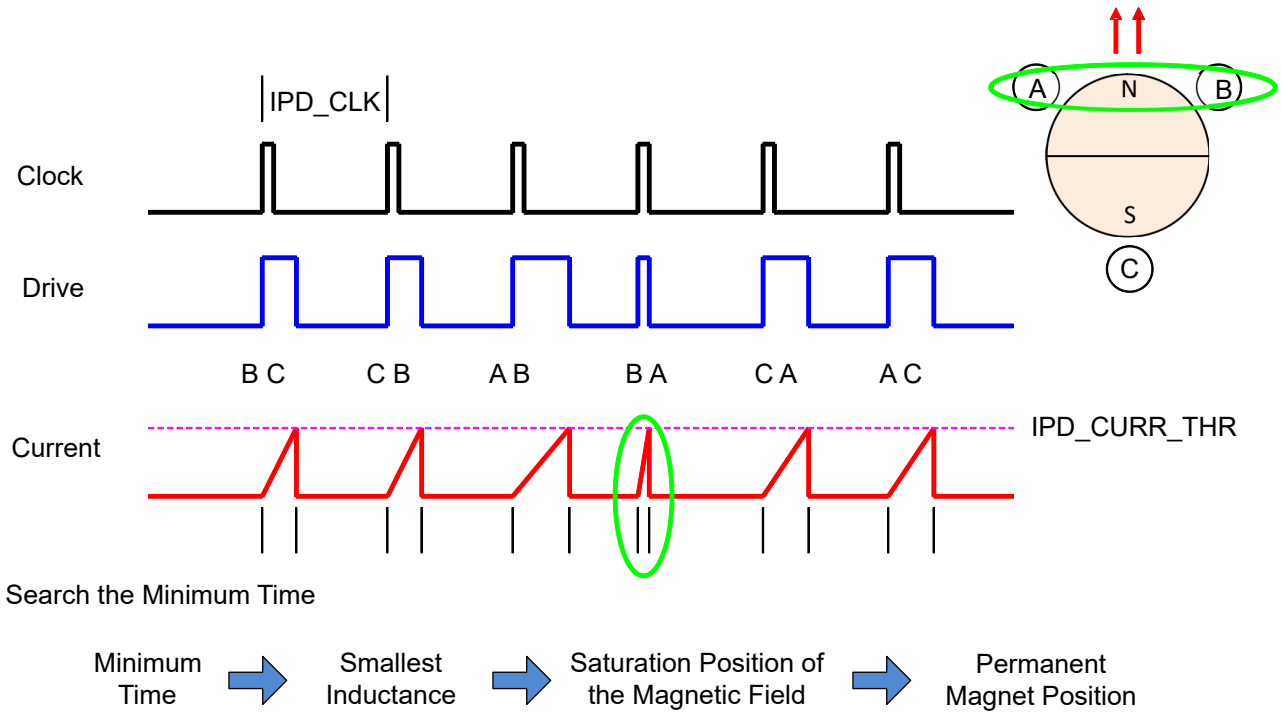


Figure 6-33. IPD Function

6.3.10.4.3.2 IPD Release Mode

Two modes are available for configuring the way the MCF8315D stops driving the motor when the current threshold is reached. The recirculate (or brake) mode is selected if IPD_RLS_MODE = 0b. In this configuration, the low-side (LSC) MOSFET remains ON to allow the current to recirculate between the MOSFET (LSC) and body diode (LSA) (see Figure 6-34). Hi-Z mode is selected if IPD_RLS_MODE = 1b. In Hi-Z mode, both the high-side (HSA) and low-side (LSC) MOSFETs are turned OFF and the current recirculates through the body diodes back to the power supply (see Figure 6-35).

In the Hi-Z mode, the phase current has a faster settle-down time, but that can result in a voltage increase on V_M. The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between V_M and PGND to absorb the energy. If the voltage surge cannot be contained or if it is unacceptable for the application, recirculate mode must be used. When using the recirculate mode, select the IPD_CLK_FREQ appropriately to give the current in the motor windings enough time to decay to 0-A before the next IPD phase pattern is applied.

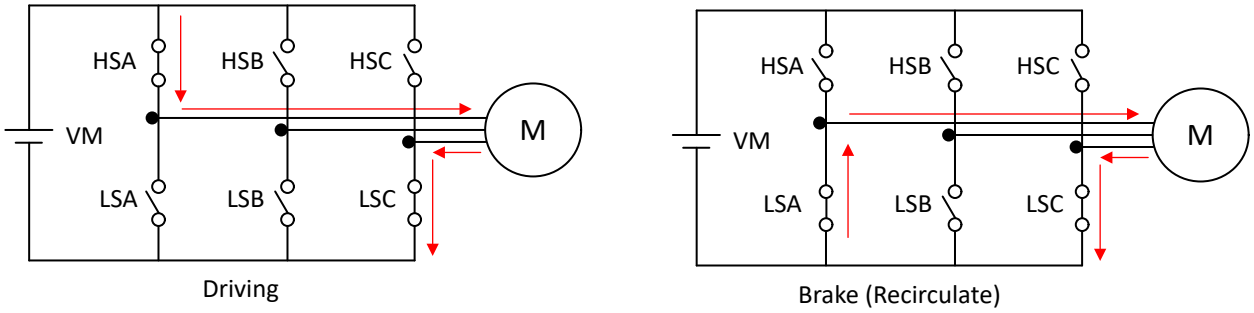


Figure 6-34. IPD Release Mode - Brake (0b)

Copyright © 2025 Texas Instruments Incorporated

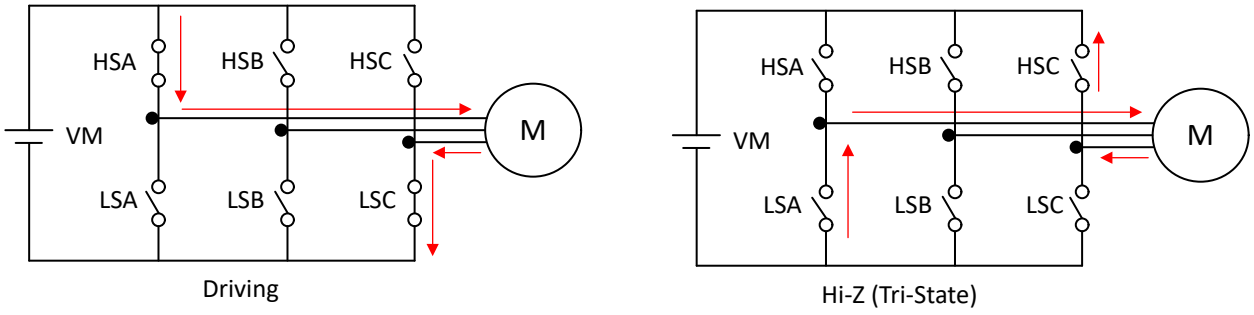


Figure 6-35. IPD Release Mode - Tristate (1b)

6.3.10.4.3.3 IPD Advance Angle

After the initial position is detected, the MCF8315D begins driving the motor in open loop at an angle specified by IPD_ADV_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD_ADV_ANGLE to allow for smooth acceleration in the application (see Figure 6-36).

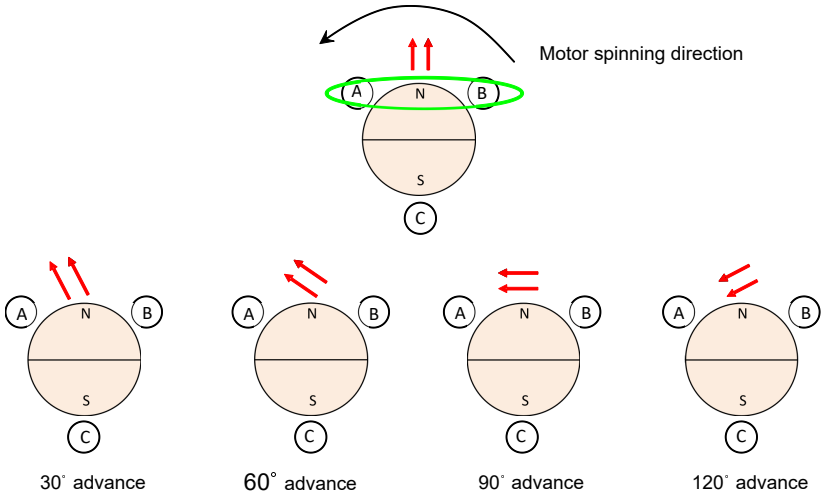


Figure 6-36. IPD Advance Angle

6.3.10.4.4 Slow First Cycle Startup

Slow First Cycle start-up is enabled by configuring MTR_STARTUP to 11b. In slow first cycle start-up, the MCF8315D starts motor commutation at a frequency defined by SLOW_FIRST_CYCLE_FREQ. The frequency configured is used only for first cycle, and then the motor commutation follows acceleration profile configured by open loop acceleration coefficients A1 and A2. The slow first cycle frequency has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

6.3.10.4.5 Open Loop

Upon completing the motor position initialization with either align, double align, IPD or slow first cycle, the MCF8315D begins to accelerate the motor in open loop. In MCF8315D, the current limit in open loop is set by OL_ILIMIT and the speed is increased using this current. In open loop, the control PI loops for I_q and I_d actively control the currents. The angle during open loop is provided from the ramp generator as shown in Figure 6-37.

Copyright © 2025 Texas Instruments Incorporated

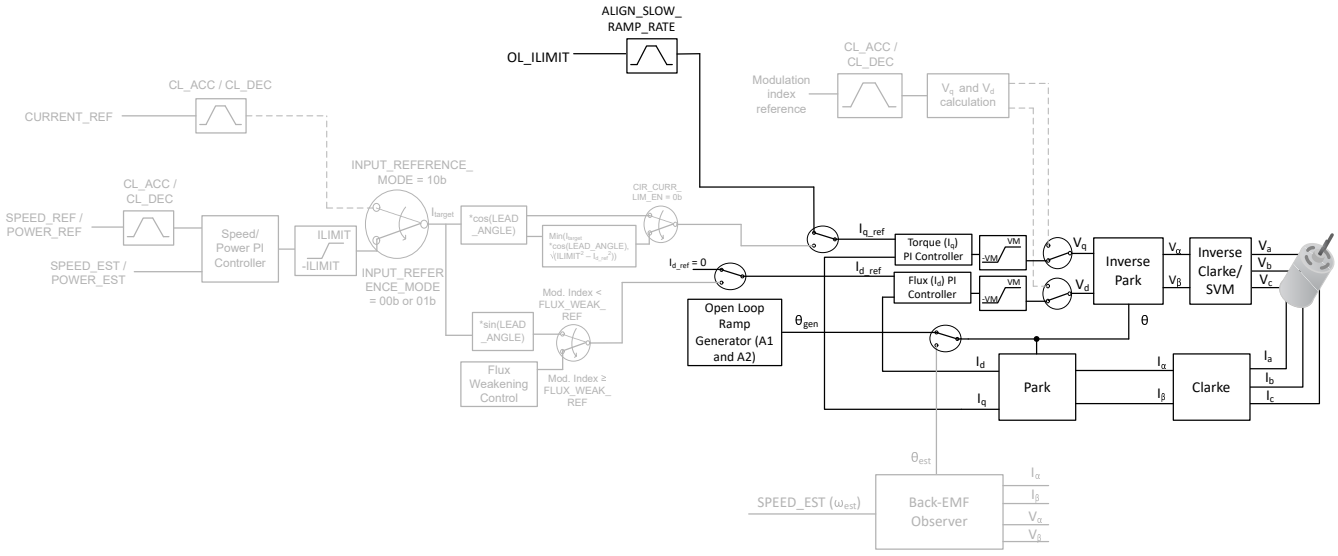


Figure 6-37. Open Loop

The function of the open-loop operation is to drive the motor to a speed at which the motor generates sufficient BEMF to allow the back-EMF observer to accurately detect the position of the rotor. The motor is accelerated in open loop and speed at any given time is determined by Equation 7. In MCF8315D, open loop acceleration coefficients, A1 and A2 are configured through OL_ACC_A1 and OL_ACC_A2 respectively.

$$\text{Speed}(t) = A1 * t + 0.5 * A2 * t^2 \quad (7)$$

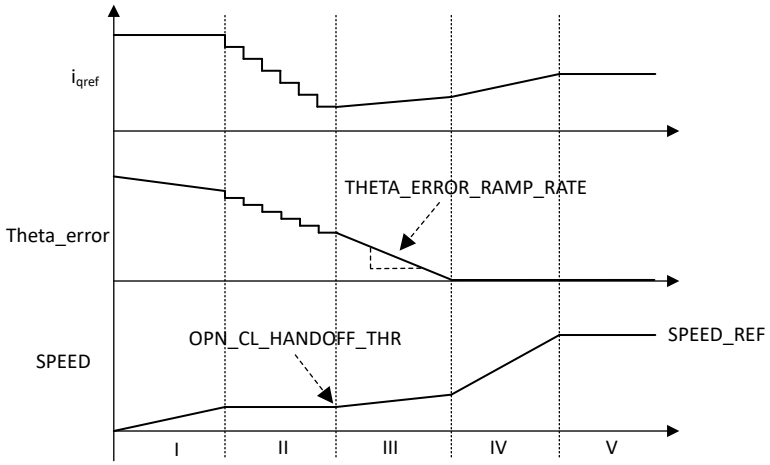
6.3.10.4.6 Transition from Open to Closed Loop

Once the motor has reached a sufficient speed for the back-EMF observer to estimate the angle and speed of the motor, the MCF8315D transitions into closed loop state. This handoff speed is automatically determined based on the measured back-EMF and motor speed. Users also have an option to manually set the handoff speed by configuring OPN_CL_HANDOFF_THR and setting AUTO_HANDOFF_EN to 0b. In order to have smooth transition and avoid speed transients, the theta error (Θ_{gen} - Θ_{est}) is decreased linearly after transition. The ramp rate of theta error reduction can be configured using THETA_ERROR_RAMP_RATE. If the current limit set during the open loop is high and if it is not reduced before transition to closed loop, the motor speed may momentarily rise to higher values than SPEED_REF after transition into closed loop. In order to avoid such speed variations, configure the IQ_RAMP_EN to 1b, so that i_{q_ref} decreases prior to transition into closed loop. However if the final speed reference (SPEED_REF) is more than two times the open loop to closed loop hand off speed (OPN_CL_HANDOFF_THR), then i_{q_ref} is not decreased independent of the IQ_RAMP_EN setting, to enable faster motor acceleration.

After hand off to closed loop at a sufficient speed, there could be still some theta error, as the estimators may not be fully aligned. A slow acceleration can be used after the open loop to closed loop transition, ensuring that the theta error reduces to zero. The slow acceleration can be configured using CL_SLOW_ACC.

Figure 6-38 shows the control sequence in open to closed loop transition. The current i_{q_ref} reduces to a lower value in current decay region, if IQ_RAMP_EN is set to 1b. If IQ_RAMP_EN is set to 0b, then the current decay region will not be present in the transition sequence.

Copyright © 2025 Texas Instruments Incorporated



I. Open Loop Acceleration, II. Current Decay, III. Closed loop slow acceleration
IV. Closed loop acceleration, V. Closed loop steady state

Figure 6-38. Control Sequence in Open to Closed Loop Transition

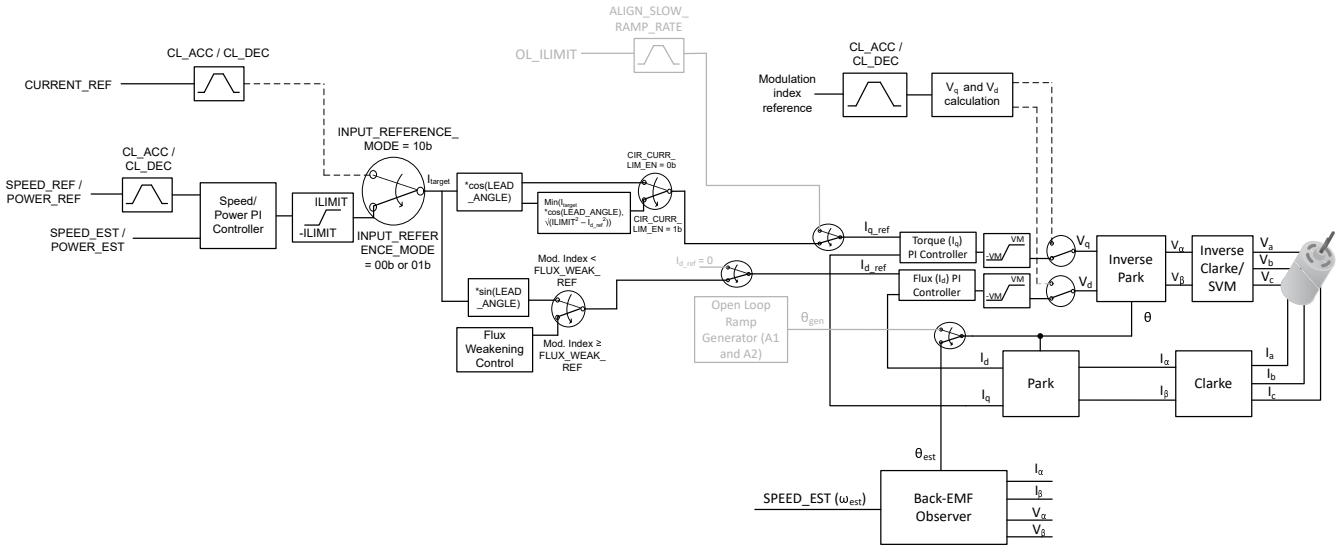


Figure 6-39. Open to Closed Loop Transition Control Block Diagram

Copyright © 2025 Texas Instruments Incorporated

6.3.11 Closed Loop Operation

The MCF8315D drives the motor using Field Oriented Control (FOC) as shown in Figure 6-40. In closed loop operation, the motor angle (Θ_{est}) and speed (SPEED_EST) are estimated using the back-EMF observer. The speed, power or current regulation is achieved using PI control loops.

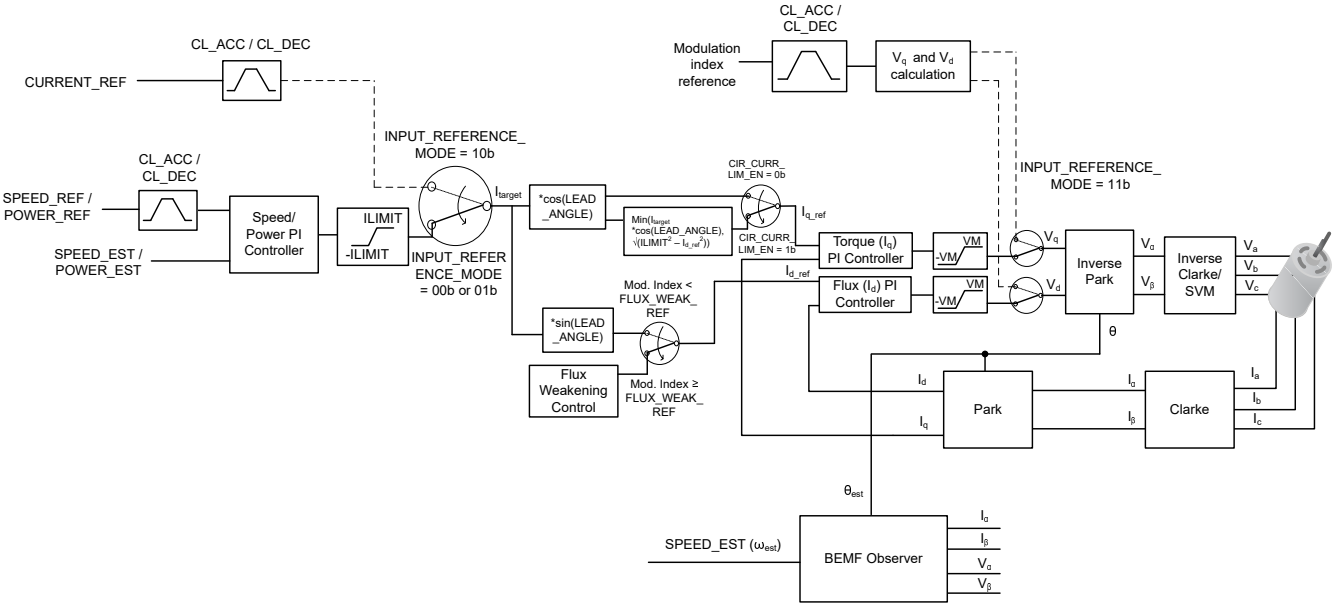


Figure 6-40. Closed Loop FOC Control

6.3.11.1 Closed Loop Acceleration/Deceleration Slew Rate

During closed loop acceleration/deceleration, MCF8315D provides the option of configuring the slew rate of the reference input. This allows for a linear change in reference input (speed or power or current or modulation index) even when there is a step change in reference input (from Analog, PWM, Frequency or I^2C) as seen in Figure 6-41. This slew rate can be configured so as to prevent sudden changes in the torque applied to the motor which could result in acoustic noise. The closed loop acceleration/deceleration slew rate parameter, CL_ACC/CL_DEC, sets the slew rate of the reference during acceleration and deceleration respectively.

Copyright © 2025 Texas Instruments Incorporated

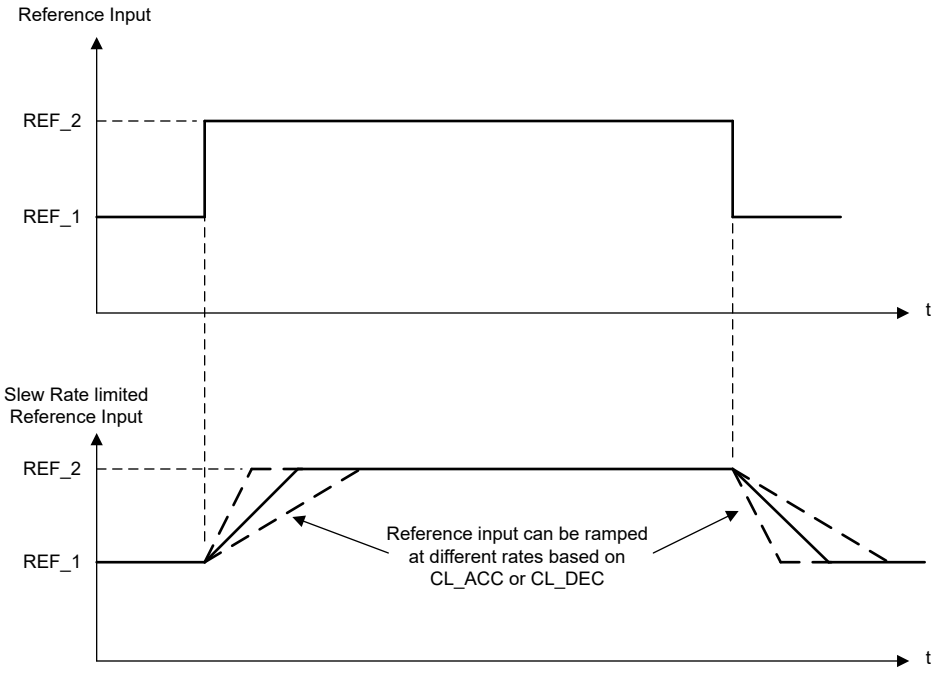


Figure 6-41. Closed Loop Acceleration/Deceleration Slew Rate

6.3.11.2 Speed PI Control

The integrated speed control loop helps maintain a constant speed over varying operating conditions. The K_p and K_i coefficients are configured through SPD_LOOP_KP and SPD_LOOP_KI. The output of the speed loop is used to generate the current reference for torque control (I_{q_ref}). The output of the speed loop is limited to implement a current limit. The current limit is set by configuring ILIMIT. When output of the speed loop saturates, the integrator is disabled to prevent integral wind-up.

SPEED_REF_SLEW is derived from the duty command input, speed profiles and closed loop acceleration/ deceleration rates configured by the user and SPEED_EST is the estimated speed from the back-EMF observer.

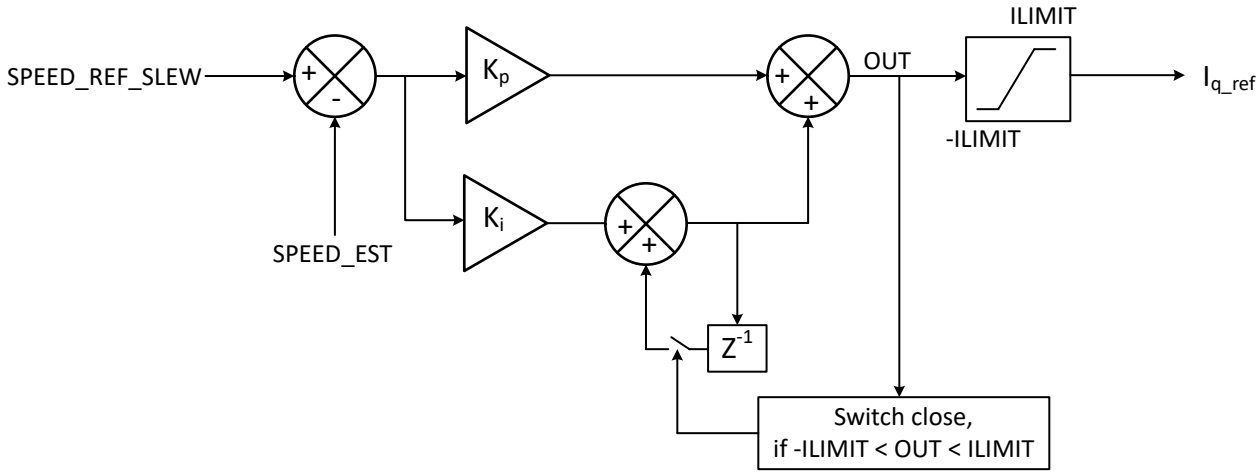


Figure 6-42. Speed PI Control

6.3.11.3 Current PI Control

The MCF8315D has two PI controllers, one each for I_d and I_q to control flux and torque separately. K_p and K_i coefficients are the same for both PI controllers and are configured through CURR_LOOP_KP and CURR_LOOP_KI. The outputs of the current control loops are used to generate voltage signals V_d and V_q to be

Copyright © 2025 Texas Instruments Incorporated

applied to the motor. The outputs of the current loops are clamped to supply voltage V_M. I_d current PI loop is executed first and output of I_d current PI loop V_d is checked for saturation. When the output of the current loop saturates, the integration is disabled to prevent integral wind-up.

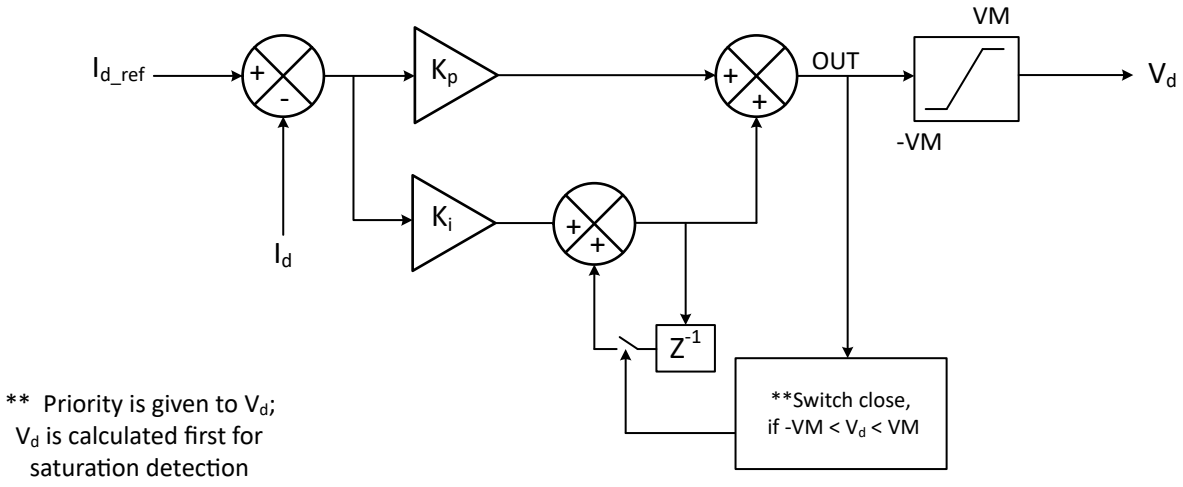


Figure 6-43. I_d Current PI Control

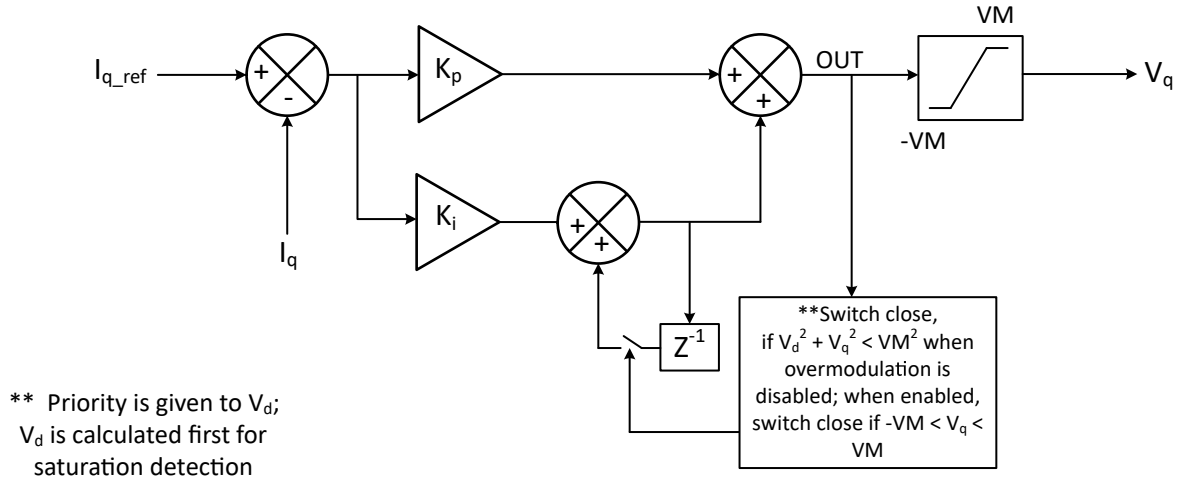


Figure 6-44. I_q Current PI Control

6.3.11.4 Power Control Mode

MCF8315D provides an option of regulating the (input DC) power instead of motor speed for a closed loop power control. Input power regulation (instead of motor speed) mode is selected by setting INPUT_REFERENCE_MODE to 01b. The maximum power that MCF8315D can draw from the DC input supply is set by MAX_POWER. The K_p and K_i coefficients for power loop are configured through SPD_LOOP_KP and SPD_LOOP_KI.

$$POWER\ REF(W) = DUTY\ CMD \times Maximum\ Power\ (W) \quad (8)$$

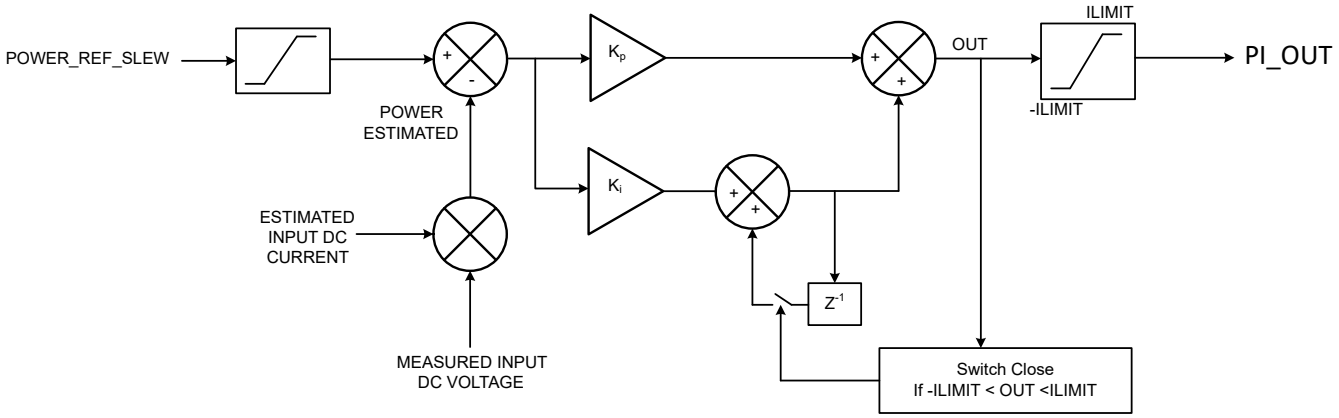


Figure 6-45. Closed Loop Power Control

6.3.11.5 Current (Torque) Control Mode

MCF8315D provides the option of controlling the motor q- and d-axis currents directly by setting INPUT_REFERENCE_MODE to 10b. In this mode, the q- and d-axis current references, I_{q_ref} and I_{d_ref} is directly set by the duty cycle input, DUTY CMD, ILIMIT and LEAD_ANGLE instead of the speed PI loop output as shown in Figure 6-40. Thus, this mode enables torque control through setting ILIMIT and hence can be used for torque mode operation.

6.3.11.6 Modulation Index Control

MCF8315D provides voltage control mode, selected by setting INPUT_REFERENCE_MODE to 11b. The closed loop speed control, power control and current control (i_q and i_d) are disabled in this mode. The applied V_q and V_d are controlled directly using the user defined modulation index reference voltage (VOLTAGE REF) and the lead angle setting. The VOLTAGE REF varies from MIN_DUTY to 100%.

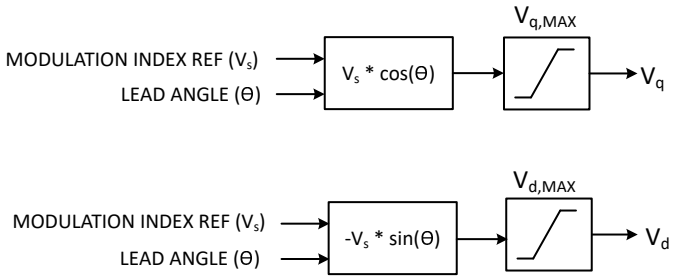


Figure 6-46. Open Loop Voltage Control

Note

MCF8315D does not support recirculation stop mode during modulation index control mode.

6.3.11.7 Overmodulation

MCF8315D provides an overmodulation option to operate the motor at a higher speed at the same VM voltage by increasing the applied fundamental phase voltage by suitably modifying the applied PWM pattern - the higher fundamental phase voltage is accompanied by an increase in higher order harmonics. This feature can be enabled by setting OVERMODULATION_ENABLE to 1b.

6.3.11.8 Motor Speed Limit

MCF8315D provides the option of limiting the motor speed to a user configured limit. When SPEED_LIMIT_ENABLE is set to 1b, irrespective of the input reference mode (current, power or voltage) and operating conditions like (VM, load), MCF8315D limits the motor speed to MAX_SPEED by restricting the input DC power, motor phase current or voltage (depending on input reference mode). When speed limit is active

Copyright © 2025 Texas Instruments Incorporated

(motor speed limited at MAX_SPEED), the acceleration/deceleration rate is set by CL_SLOW_ACC instead of CL_ACC/CL_DEC to minimize chattering around the MAX_SPEED value. When the speed limit condition becomes inactive (motor speed < MAX_SPEED), acceleration/deceleration rate reverts to CL_ACC/CL_DEC.

6.3.11.9 Input DC Power Limit

MCF8315D provides the option of limiting the power that the motor driver can draw from the input DC source (VM). When BUS_POWER_LIMIT_ENABLE is set to 1b, irrespective of the input reference mode (speed, current or voltage) and operating conditions like (VM, load), MCF8315D limits the input DC power to MAX_POWER by restricting the motor speed, current or voltage (depending on input reference mode). When power limit is active (input DC power limited at MAX_POWER), the acceleration/deceleration rate is set by CL_SLOW_ACC instead of CL_ACC/CL_DEC to minimize chattering around the MAX_POWER value. When the power limit condition becomes inactive (input DC power < MAX_POWER), acceleration/deceleration rate reverts to CL_ACC/CL_DEC.

6.3.12 Flux Weakening Control

PMSM motors can be operated not only in the constant torque region below the base speed (rated speed) but also in the constant power region above the base speed, but the base speed can be varied according to current and voltage limitation. MCF8315D provides a flux weakening control, to increase the motor speed beyond the rated speed. The flux weakening can be enabled by setting FLUX_WEAK_EN to 1b. The flux weakening control uses a PI control loop as shown in , to create the I_{d_ref}. Kp and Ki coefficients for flux weakening loop are configured through FLUX_WEAK_KP and FLUX_WEAK_KI.

User can configure the modulation index reference, V_{s_ref} (shown in Figure 6-47) below that the flux weakening is not active and I_{d_FW} is set to zero. The configuration is available in the bits FLUX_WEAK_REF.

$$V_{s\_ref} = \sqrt{V_{q\_ref}^2 + V_{d\_ref}^2} \quad (9)$$

Copyright © 2025 Texas Instruments Incorporated

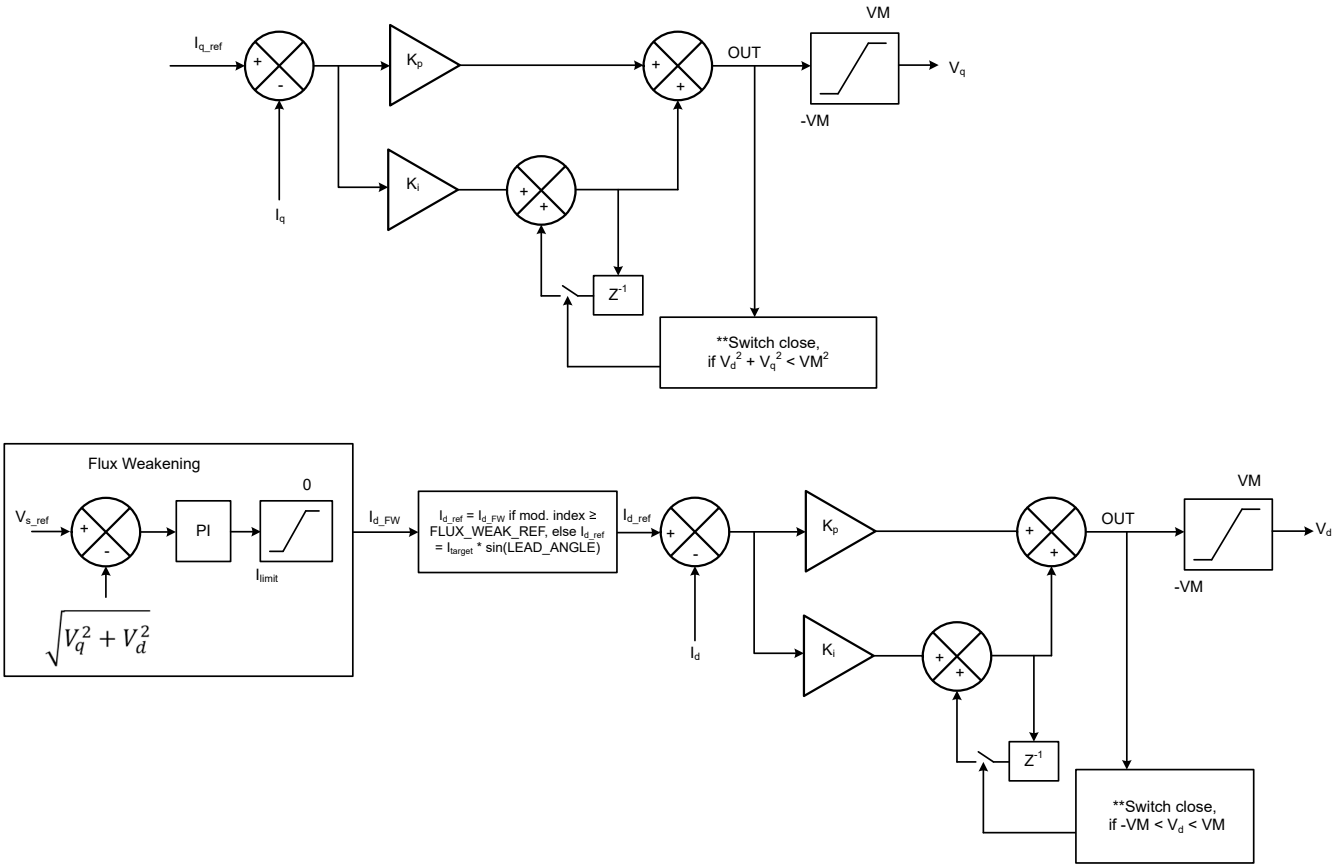


Figure 6-47. Flux Weakening Control

6.3.13 Motor Parameters

The MCF8315D uses the motor resistance, motor inductance and motor back-EMF constant to estimate motor position when operating in closed loop. The MCF8315D has the capability of measuring these motor parameters in the offline state (see Motor Parameter Extraction Tool (MPET)). Offline measurement of parameters, when enabled, takes place before normal motor operation. The user can also disable the offline measurement and configure motor parameters through EEPROM. This feature of offline motor parameter measurement is useful to account for motor to motor variation during manufacturing.

6.3.13.1 Motor Resistance

For a wye-connected motor, the motor phase resistance refers to the resistance from the phase output to the center tap, R_{PH} (denoted as R_{PH} in Figure 6-48). For a delta-connected motor, the motor phase resistance refers to the equivalent phase to center tap in the wye configuration in Figure 6-48.

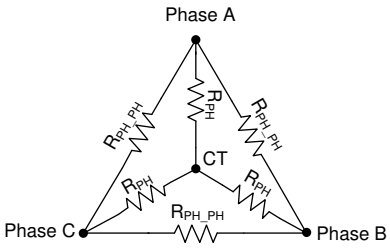


Figure 6-48. Motor Resistance

For both the delta-connected and the wye-connected motor, the easy way to get the equivalent R_{PH} is to measure the resistance between two phase terminals (R_{PH_PH}), and then divide this value by two, R_{PH} = ½

Copyright © 2025 Texas Instruments Incorporated

R_{PH_PH}. In wye-connected motor, if user has access to center tap (CT), R_{PH} can also be measured between center tap (CT) and phase terminal.

Configure the motor resistance (R_{PH}) to a nearest value from Table 6-2.

Table 6-2. Motor Resistance Look-Up Table

MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	0.145	0x80	0.465	0xC0	2.1
0x01	0.006	0x41	0.150	0x81	0.470	0xC1	2.2
0x02	0.007	0x42	0.155	0x82	0.475	0xC2	2.3
0x03	0.008	0x43	0.160	0x83	0.480	0xC3	2.4
0x04	0.009	0x44	0.165	0x84	0.485	0xC4	2.5
0x05	0.010	0x45	0.170	0x85	0.490	0xC5	2.6
0x06	0.011	0x46	0.175	0x86	0.495	0xC6	2.7
0x07	0.012	0x47	0.180	0x87	0.50	0xC7	2.8
0x08	0.013	0x48	0.185	0x88	0.51	0xC8	2.9
0x09	0.014	0x49	0.190	0x89	0.52	0xC9	3.0
0x0A	0.015	0x4A	0.195	0x8A	0.53	0xCA	3.2
0x0B	0.016	0x4B	0.200	0x8B	0.54	0xCB	3.4
0x0C	0.017	0x4C	0.205	0x8C	0.55	0xCC	3.6
0x0D	0.018	0x4D	0.210	0x8D	0.56	0xCD	3.8
0x0E	0.019	0x4E	0.215	0x8E	0.57	0xCE	4.0
0x0F	0.020	0x4F	0.220	0x8F	0.58	0xCF	4.2
0x10	0.022	0x50	0.225	0x90	0.59	0xD0	4.4
0x11	0.024	0x51	0.230	0x91	0.60	0xD1	4.6
0x12	0.026	0x52	0.235	0x92	0.61	0xD2	4.8
0x13	0.028	0x53	0.240	0x93	0.62	0xD3	5.0
0x14	0.030	0x54	0.245	0x94	0.63	0xD4	5.2
0x15	0.032	0x55	0.250	0x95	0.64	0xD5	5.4
0x16	0.034	0x56	0.255	0x96	0.65	0xD6	5.6
0x17	0.036	0x57	0.260	0x97	0.66	0xD7	5.8
0x18	0.038	0x58	0.265	0x98	0.67	0xD8	6.0
0x19	0.040	0x59	0.270	0x99	0.68	0xD9	6.2
0x1A	0.042	0x5A	0.275	0x9A	0.69	0xDA	6.4
0x1B	0.044	0x5B	0.280	0x9B	0.70	0xDB	6.6
0x1C	0.046	0x5C	0.285	0x9C	0.72	0xDC	6.8
0x1D	0.048	0x5D	0.290	0x9D	0.74	0xDD	7.0
0x1E	0.050	0x5E	0.295	0x9E	0.76	0xDE	7.2
0x1F	0.052	0x5F	0.300	0x9F	0.78	0xDF	7.4
0x20	0.054	0x60	0.305	0xA0	0.80	0xE0	7.6
0x21	0.056	0x61	0.310	0xA1	0.82	0xE1	7.8
0x22	0.058	0x62	0.315	0xA2	0.84	0xE2	8.0
0x23	0.060	0x63	0.320	0xA3	0.86	0xE3	8.2
0x24	0.062	0x64	0.325	0xA4	0.88	0xE4	8.4

Copyright © 2025 Texas Instruments Incorporated

Table 6-2. Motor Resistance Look-Up Table (continued)

MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)
0x25	0.064	0x65	0.330	0xA5	0.90	0xE5	8.6
0x26	0.066	0x66	0.335	0xA6	0.92	0xE6	8.8
0x27	0.068	0x67	0.340	0xA7	0.94	0xE7	9
0x28	0.070	0x68	0.345	0xA8	0.96	0xE8	9.2
0x29	0.072	0x69	0.350	0xA9	0.98	0xE9	9.4
0x2A	0.074	0x6A	0.355	0xAA	1.00	0xEA	9.6
0x2B	0.076	0x6B	0.360	0xAB	1.05	0xEB	9.8
0x2C	0.078	0x6C	0.365	0xAC	1.10	0xEC	10.0
0x2D	0.080	0x6D	0.370	0xAD	1.15	0xED	10.5
0x2E	0.082	0x6E	0.375	0xAE	1.20	0xEE	11.0
0x2F	0.084	0x6F	0.380	0xAF	1.25	0xEF	11.5
0x30	0.086	0x70	0.385	0xB0	1.30	0xF0	12.0
0x31	0.088	0x71	0.390	0xB1	1.35	0xF1	12.5
0x32	0.090	0x72	0.395	0xB2	1.40	0xF2	13.0
0x33	0.092	0x73	0.400	0xB3	1.45	0xF3	13.5
0x34	0.094	0x74	0.405	0xB4	1.50	0xF4	14.0
0x35	0.096	0x75	0.410	0xB5	1.55	0xF5	14.5
0x36	0.098	0x76	0.415	0xB6	1.60	0xF6	15.0
0x37	0.100	0x77	0.420	0xB7	1.65	0xF7	15.5
0x38	0.105	0x78	0.425	0xB8	1.70	0xF8	16.0
0x39	0.110	0x79	0.430	0xB9	1.75	0xF9	16.5
0x3A	0.115	0x7A	0.435	0xBA	1.80	0xFA	17.0
0x3B	0.120	0x7B	0.440	0xBB	1.85	0xFB	17.5
0x3C	0.125	0x7C	0.445	0xBC	1.90	0xFC	18.0
0x3D	0.130	0x7D	0.450	0xBD	1.95	0xFD	18.5
0x3E	0.135	0x7E	0.455	0xBE	2.00	0xFE	19.0
0x3F	0.140	0x7F	0.460	0xBF	2.05	0xFF	20.0

6.3.13.2 Motor Inductance

For a wye-connected motor, the motor phase inductance refers to the inductance from the phase output to the center tap, L_{PH} (denoted as L_{PH} in Figure 6-49). For a delta-connected motor, the motor phase inductance refers to the equivalent phase to center tap in the wye configuration in Figure 6-49.

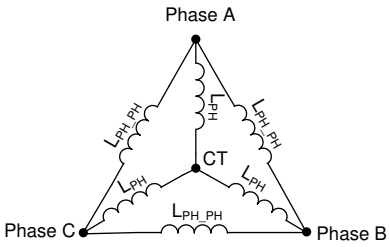


Figure 6-49. Motor Inductance

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent L_{PH} is to measure the inductance between two phase terminals (L_{PH_PH}), and then divide this value by two, L_{PH} = ½ L_{PH_PH}. In wye-connected motor, if user has access to center tap (CT), L_{PH} can also be measured between center tap (CT) and phase terminal.

Copyright © 2025 Texas Instruments Incorporated

Configure the motor inductance (L_{PH}) to a nearest value from Table 6-3.

Copyright © 2025 Texas Instruments Incorporated

Table 6-3. Motor Inductance Look-Up Table

MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	0.145	0x80	0.465	0xC0	2.1
0x01	0.006	0x41	0.150	0x81	0.470	0xC1	2.2
0x02	0.007	0x42	0.155	0x82	0.475	0xC2	2.3
0x03	0.008	0x43	0.160	0x83	0.480	0xC3	2.4
0x04	0.009	0x44	0.165	0x84	0.485	0xC4	2.5
0x05	0.010	0x45	0.170	0x85	0.490	0xC5	2.6
0x06	0.011	0x46	0.175	0x86	0.495	0xC6	2.7
0x07	0.012	0x47	0.180	0x87	0.50	0xC7	2.8
0x08	0.013	0x48	0.185	0x88	0.51	0xC8	2.9
0x09	0.014	0x49	0.190	0x89	0.52	0xC9	3.0
0x0A	0.015	0x4A	0.195	0x8A	0.53	0xCA	3.2
0x0B	0.016	0x4B	0.200	0x8B	0.54	0xCB	3.4
0x0C	0.017	0x4C	0.205	0x8C	0.55	0xCC	3.6
0x0D	0.018	0x4D	0.210	0x8D	0.56	0xCD	3.8
0x0E	0.019	0x4E	0.215	0x8E	0.57	0xCE	4.0
0x0F	0.020	0x4F	0.220	0x8F	0.58	0xCF	4.2
0x10	0.022	0x50	0.225	0x90	0.59	0xD0	4.4
0x11	0.024	0x51	0.230	0x91	0.60	0xD1	4.6
0x12	0.026	0x52	0.235	0x92	0.61	0xD2	4.8
0x13	0.028	0x53	0.240	0x93	0.62	0xD3	5.0
0x14	0.030	0x54	0.245	0x94	0.63	0xD4	5.2
0x15	0.032	0x55	0.250	0x95	0.64	0xD5	5.4
0x16	0.034	0x56	0.255	0x96	0.65	0xD6	5.6
0x17	0.036	0x57	0.260	0x97	0.66	0xD7	5.8
0x18	0.038	0x58	0.265	0x98	0.67	0xD8	6.0
0x19	0.040	0x59	0.270	0x99	0.68	0xD9	6.2
0x1A	0.042	0x5A	0.275	0x9A	0.69	0xDA	6.4
0x1B	0.044	0x5B	0.280	0x9B	0.70	0xDB	6.6
0x1C	0.046	0x5C	0.285	0x9C	0.72	0xDC	6.8
0x1D	0.048	0x5D	0.290	0x9D	0.74	0xDD	7.0
0x1E	0.050	0x5E	0.295	0x9E	0.76	0xDE	7.2
0x1F	0.052	0x5F	0.300	0x9F	0.78	0xDF	7.4
0x20	0.054	0x60	0.305	0xA0	0.80	0xE0	7.6
0x21	0.056	0x61	0.310	0xA1	0.82	0xE1	7.8
0x22	0.058	0x62	0.315	0xA2	0.84	0xE2	8.0
0x23	0.060	0x63	0.320	0xA3	0.86	0xE3	8.2
0x24	0.062	0x64	0.325	0xA4	0.88	0xE4	8.4
0x25	0.064	0x65	0.330	0xA5	0.90	0xE5	8.6
0x26	0.066	0x66	0.335	0xA6	0.92	0xE6	8.8
0x27	0.068	0x67	0.340	0xA7	0.94	0xE7	9
0x28	0.070	0x68	0.345	0xA8	0.96	0xE8	9.2

Copyright © 2025 Texas Instruments Incorporated

Table 6-3. Motor Inductance Look-Up Table (continued)

MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)
0x29	0.072	0x69	0.350	0xA9	0.98	0xE9	9.4
0x2A	0.074	0x6A	0.355	0xAA	1.00	0xEA	9.6
0x2B	0.076	0x6B	0.360	0xAB	1.05	0xEB	9.8
0x2C	0.078	0x6C	0.365	0xAC	1.10	0xEC	10.0
0x2D	0.080	0x6D	0.370	0xAD	1.15	0xED	10.5
0x2E	0.082	0x6E	0.375	0xAE	1.20	0xEE	11.0
0x2F	0.084	0x6F	0.380	0xAF	1.25	0xEF	11.5
0x30	0.086	0x70	0.385	0xB0	1.30	0xF0	12.0
0x31	0.088	0x71	0.390	0xB1	1.35	0xF1	12.5
0x32	0.090	0x72	0.395	0xB2	1.40	0xF2	13.0
0x33	0.092	0x73	0.400	0xB3	1.45	0xF3	13.5
0x34	0.094	0x74	0.405	0xB4	1.50	0xF4	14.0
0x35	0.096	0x75	0.410	0xB5	1.55	0xF5	14.5
0x36	0.098	0x76	0.415	0xB6	1.60	0xF6	15.0
0x37	0.100	0x77	0.420	0xB7	1.65	0xF7	15.5
0x38	0.105	0x78	0.425	0xB8	1.70	0xF8	16.0
0x39	0.110	0x79	0.430	0xB9	1.75	0xF9	16.5
0x3A	0.115	0x7A	0.435	0xBA	1.80	0xFA	17.0
0x3B	0.120	0x7B	0.440	0xBB	1.85	0xFB	17.5
0x3C	0.125	0x7C	0.445	0xBC	1.90	0xFC	18.0
0x3D	0.130	0x7D	0.450	0xBD	1.95	0xFD	18.5
0x3E	0.135	0x7E	0.455	0xBE	2.00	0xFE	19.0
0x3F	0.140	0x7F	0.460	0xBF	2.05	0xFF	20.0

6.3.13.3 Motor Back-EMF constant

The back-EMF constant describes the motor phase-to-neutral back-EMF voltage as a function of the motor speed. For a wye-connected motor, the motor BEMF constant refers to the BEMF as a function of time from the phase output to the center tap, Kt_{PH_N} (denoted as Kt_{PH_N} in Figure 6-50). For a delta-connected motor, the motor BEMF constant refers to the equivalent phase to center tap in the wye configuration in Figure 6-50.

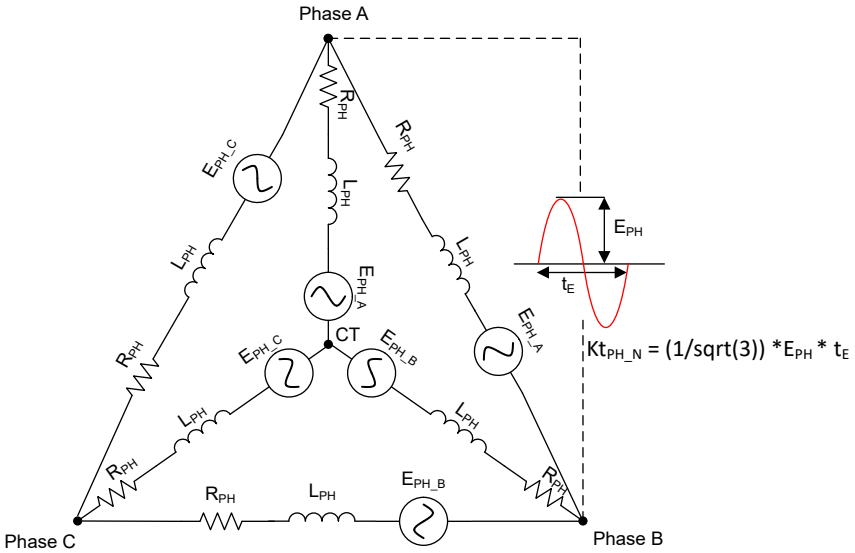


Figure 6-50. Motor back-EMF constant

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent Kt_{PH_N} is to measure the peak value of BEMF on scope for one electrical cycle between two phase terminals (E_{PH}), and then multiply by time duration of one electrical cycle and in order to convert from phase-to-phase to phase-to-neutral divide by sqrt(3) as shown in Equation 10 .

$$Kt_{PH\_N} = {}^{1}/_{\sqrt{3}} \times E_{PH} \times t_E \quad (10)$$

Configure the motor BEMF constant (Kt_{PH_N}) to a nearest value from Table 6-4.

Table 6-4. Motor BEMF constant Look-Up Table

MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	14.5	0x80	46.5	0xC0	210
0x01	0.6	0x41	15.0	0x81	47.0	0xC1	220
0x02	0.7	0x42	15.5	0x82	47.5	0xC2	230
0x03	0.8	0x43	16.0	0x83	48.0	0xC3	240
0x04	0.9	0x44	16.5	0x84	48.5	0xC4	250
0x05	1.0	0x45	17.0	0x85	49.0	0xC5	260
0x06	1.1	0x46	17.5	0x86	49.5	0xC6	270
0x07	1.2	0x47	18.0	0x87	50.0	0xC7	280
0x08	1.3	0x48	18.5	0x88	51	0xC8	290
0x09	1.4	0x49	19.0	0x89	52	0xC9	300
0x0A	1.5	0x4A	19.5	0x8A	53	0xCA	320
0x0B	1.6	0x4B	20.0	0x8B	54	0xCB	340
0x0C	1.7	0x4C	20.5	0x8C	55	0xCC	360
0x0D	1.8	0x4D	21.0	0x8D	56	0xCD	380
0x0E	1.9	0x4E	21.5	0x8E	57	0xCE	400
0x0F	2.0	0x4F	22.0	0x8F	58	0xCF	420

Copyright © 2025 Texas Instruments Incorporated

Table 6-4. Motor BEMF constant Look-Up Table (continued)

MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)
0x10	2.2	0x50	22.5	0x90	59	0xD0	440
0x11	2.4	0x51	23.0	0x91	60	0xD1	460
0x12	2.6	0x52	23.5	0x92	61	0xD2	480
0x13	2.8	0x53	24.0	0x93	62	0xD3	500
0x14	3.0	0x54	24.5	0x94	63	0xD4	520
0x15	3.2	0x55	25.0	0x95	64	0xD5	540
0x16	3.4	0x56	25.5	0x96	65	0xD6	560
0x17	3.6	0x57	26.0	0x97	66	0xD7	580
0x18	3.8	0x58	26.5	0x98	67	0xD8	600
0x19	4.0	0x59	27.0	0x99	68	0xD9	620
0x1A	4.2	0x5A	27.5	0x9A	69	0xDA	640
0x1B	4.4	0x5B	28.0	0x9B	70	0xDB	660
0x1C	4.6	0x5C	28.5	0x9C	72	0xDC	680
0x1D	4.8	0x5D	29.0	0x9D	74	0xDD	700
0x1E	5.0	0x5E	29.5	0x9E	76	0xDE	720
0x1F	5.2	0x5F	30.0	0x9F	78	0xDF	740
0x20	5.4	0x60	30.5	0xA0	80	0xE0	760
0x21	5.6	0x61	31.0	0xA1	82	0xE1	780
0x22	5.8	0x62	31.5	0xA2	84	0xE2	800
0x23	6.0	0x63	32.0	0xA3	86	0xE3	820
0x24	6.2	0x64	32.5	0xA4	88	0xE4	840
0x25	6.4	0x65	33.0	0xA5	90	0xE5	860
0x26	6.6	0x66	33.5	0xA6	92	0xE6	880
0x27	6.8	0x67	34.0	0xA7	94	0xE7	900
0x28	7.0	0x68	34.5	0xA8	96	0xE8	920
0x29	7.2	0x69	35.0	0xA9	98	0xE9	940
0x2A	7.4	0x6A	35.5	0xAA	100	0xEA	960
0x2B	7.6	0x6B	36.0	0xAB	105	0xEB	980
0x2C	7.8	0x6C	36.5	0xAC	110	0xEC	1000
0x2D	8.0	0x6D	37.0	0xAD	115	0xED	1050
0x2E	8.2	0x6E	37.5	0xAE	120	0xEE	1100
0x2F	8.4	0x6F	38.0	0xAF	125	0xEF	1150
0x30	8.6	0x70	38.5	0xB0	130	0xF0	1200
0x31	8.8	0x71	39.0	0xB1	135	0xF1	1250
0x32	9.0	0x72	39.5	0xB2	140	0xF2	1300
0x33	9.2	0x73	40.0	0xB3	145	0xF3	1350
0x34	9.4	0x74	40.5	0xB4	150	0xF4	1400
0x35	9.6	0x75	41.0	0xB5	155	0xF5	1450
0x36	9.8	0x76	41.5	0xB6	160	0xF6	1500
0x37	10.0	0x77	42.0	0xB7	165	0xF7	1550
0x38	10.5	0x78	42.5	0xB8	170	0xF8	1600
0x39	11.0	0x79	43.0	0xB9	175	0xF9	1650
0x3A	11.5	0x7A	43.5	0xBA	180	0xFA	1700
0x3B	12.0	0x7B	44.0	0xBB	185	0xFB	1750

Copyright © 2025 Texas Instruments Incorporated

Table 6-4. Motor BEMF constant Look-Up Table (continued)

MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)
0x3C	12.5	0x7C	44.5	0xBC	190	0xFC	1800
0x3D	13.0	0x7D	45.0	0xBD	195	0xFD	1850
0x3E	13.5	0x7E	45.5	0xBE	200	0xFE	1900
0x3F	14.0	0x7F	46.0	0xBF	205	0xFF	2000

6.3.14 Motor Parameter Extraction Tool (MPET)

The MCF8315D uses motor winding resistance, motor winding inductance and Back-EMF constant to estimate motor position in closed loop operation. The MCF8315D has capability of automatically measuring motor parameters in offline state, rather than having the user enter the values themselves. The MPET routine measures motor winding resistance, inductance, back EMF constant and mechanical load inertia and frictional coefficients. Offline measurement of parameters takes place before normal motor operation. TI recommends to estimate the motor parameters before motor startup to minimize the impact caused due to possible parameter variations.

Figure 6-51 shows the sequence of operation in the MPET routine. The MPET routine is entered when either the MPET_CMD bit is set to 1b or a non-zero target speed is set. The MPET routine consists of four steps namely, IPD, Open Loop Acceleration, Current Ramp Down and Coasting. Each one of these steps are executed if the condition shown below the step evaluates to TRUE; if the condition evaluates to FALSE, the algorithm bypasses that particular step and moves on to the next step in the sequence. Once all the 4 steps are completed (or bypassed), the algorithm exits the MPET routine. If target speed is set to a non-zero value, the algorithm begins the start-up and acceleration sequence (to target speed reference) once MPET routine is exited.

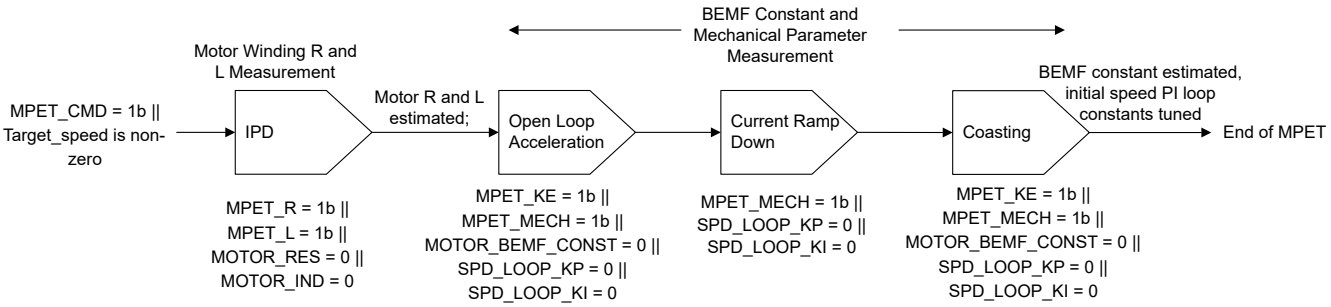


Figure 6-51. MPET Sequence

TI proprietary MPET routine includes following sequence of operation.

- **IPD**: The MPET routine starts with IPD, if the user enables motor winding resistance or inductance measurement by setting MPET_R = 1b and MPET_L = 1b or if the user defines MOTOR_RES = 0 or MOTOR_IND = 0. The IPD during MPET is configured using the normal motor operation IPD configuration parameters. The IPD current limit and the repeat number is configured using IPD_CURR_THR and IPD_REPEAT. The IPD timer over flow or the IPD current decay time more than three times the current ramp up time can result in MPET_IPD_FAULT.
- **Open loop Acceleration**:

  After IPD, the MPET routine runs align and then open loop acceleration if the back-EMF constant or mechanical parameter measurement are enabled by setting MPET_KE = 1b and MPET_MECH = 1b. The MPET routine incorporates the sequences for mechanical parameter measurement, if the speed loop PI constants are defined as zero, even if MPET_MECH = 0b. This routine uses normal motor operation open loop configuration parameters. The speed slew rate is set by OL_ACC_A1 and OL_ACC_A2, current reference is set by OL_ILIMIT and speed reference is set by OPN_CL_HANDOFF_THR.

Copyright © 2025 Texas Instruments Incorporated

- **Current Ramp Down**: After open loop acceleration, if the mechanical parameter measurement is enabled, then the MPET routine optimizes the motor current to lower value sufficient to support the load. If mechanical parameter measurement is disabled (MPET_MECH = 0b, or non-zero speed loop PI parameters) then the MPET will not have the current ramp down sequence.
- **Coasting**: MPET routine completes the sequence by allowing the motor to coast by enabling Hi-Z. The motor back EMF and indicative values of mechanical parameters are measured during the motor coasting period. If the motor back EMF is lower than the threshold defined in STAT_DETECT_THR, the MPET_BEMF_FAULT is generated.

Note

User can exit the MPET routine at any time by writing 0b to MPET_CMD bit and by making target speed as zero.

Selecting the parameters from EEPROM or MPET

The MPET estimated values are available in the MTR_PARAMS Register. Setting the MPET_WRITE_SHADOW bit to 1, writes the MPET estimated values to the shadow/RAM registers and the user-configured (from EEPROM) values in MOTOR_RES, MOTOR_IND, MOTOR_BEMF_CONST, CURR_LOOP_KP, CURR_LOOP_KI, SPD_LOOP_KP and SPD_LOOP_KI shadow/RAM registers will be overwritten by the estimated values from MPET. If any of the shadow/RAM registers are initialized to zero (from EEPROM registers), the MPET estimated values are used for those registers independent of the MPET_WRITE_SHADOW setting. The MPET calculates the current loop KP and KI by using the measured resistance and inductance. The MPET does an estimation of the mechanical parameters including the inertia and frictional coefficient at the shaft (includes both motor and shaft coupled load). These values are used to set an initial values speed loop KP and KI. The estimated speed loop KP and KI setting can be used as an initial setting only and TI recommends to tune these parameters on application by the user based on the performance requirement.

6.3.15 Anti-Voltage Surge (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive and mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the V_M voltage surges. The AVS feature works to prevent this voltage surge on V_M and can be enabled by setting AVS_EN to 1b. AVS can be disabled by setting AVS_EN to 0b. When AVS is disabled, the deceleration rate is configured through CL_DEC.

6.3.16 Active Braking

Decelerating the motor quickly requires the motor mechanical energy to be extracted from the rotor in a fast and controlled manner. However, the supply voltage (VM) increases if the motor mechanical energy is returned to the power supply during the deceleration process. MCF8315D is capable of decelerating the motor quickly without pumping energy back into the supply voltage by using a novel technique called active braking. ACTIVE_BRAKE_EN should be set to 1b to enable active braking and prevent DC bus voltage (VM) spike during fast motor deceleration. Active braking can also be used during reverse drive (see Reverse Drive) or motor stop (see Active Spin-Down) to reduce the motor speed quickly without DC bus voltage (VM) spike.

The maximum limit on the current sourced from the DC bus (i_{dc_ref}) during active braking can be configured using ACTIVE_BRAKE_CURRENT_LIMIT. The D-axis current reference (i_{d_ref}) is generated from the error between DC bus current limit (i_{dc_ref}) and the estimated DC bus current (i_{dc}) using a PI controller as shown in Figure 6-52. The gain constants of PI controller can be configured using ACTIVE_BRAKE_KP and ACTIVE_BRAKE_KI. During active braking, the DC bus current limit (i_{dc_ref}) starts from zero and linearly increases to ACTIVE_BRAKE_CURRENT_LIMIT with current slew rate as defined by ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE.

Copyright © 2025 Texas Instruments Incorporated

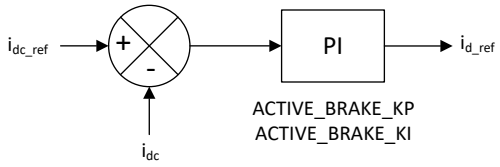


Figure 6-52. Active Braking Current Control Loop for i_{d_ref}

ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY sets the minimum difference between the initial and target speed above which active braking will be entered. For example, consider ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY is set to 10%; if the initial speed is 100% and target speed is set to 95%, MCF8315D uses AVS instead of active braking to reach 95% speed since the difference in commanded speed change (5%) is less than ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY (10%).

ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT sets the difference between the current and target speed below which active braking will be exited. For example, consider ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT is set to 5%; if the initial motor speed is 100% and target speed is set to 10%, MCF8315D uses active braking to reduce the motor speed to 15%; upon reaching 15% speed, MCF8315D exits active braking and uses AVS to decelerate the motor speed to 10%.

ACTIVE_BRAKE_MOD_INDEX_LIMIT sets the modulation index below which active braking will be used. For example, consider ACTIVE_BRAKE_MOD_INDEX_LIMIT is set to 50%, ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY is set to 5%, ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT is set to 2.5%. If the initial motor speed is at 70% (corresponding modulation index is 90%) and target speed is 40% (corresponding modulation index is 60%), MCF8315D uses AVS to decelerate the motor till target speed of 40% since the modulation index (60%) corresponding to final speed is higher than ACTIVE_BRAKE_MOD_INDEX_LIMIT of 50%. In the same case, if final speed command is 10% (corresponding modulation index is 30%), MCF8315D uses AVS till 30% speed (corresponding modulation index is 50%), switches to active braking from 30% to 15% speed (final speed of 10% + ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT of 5%) and uses AVS again from 15% to 10% speed to complete the active braking. TI recommends starting active braking tuning with ACTIVE_BRAKE_MOD_INDEX_LIMIT set to 100%; if there is a DC bus voltage (VM) spike observed during active braking, reduce ACTIVE_BRAKE_MOD_INDEX_LIMIT in steps so as to eliminate this voltage spike. If ACTIVE_BRAKE_MOD_INDEX_LIMIT is set to 0%, MCF8315D decelerates in AVS (even when ACTIVE_BRAKE_EN is set to 1b) in the forward direction; in reverse direction (during direction change), ACTIVE_BRAKE_MOD_INDEX_LIMIT is not applicable and therefore MCF8315D decelerates in active braking.

Note

1. ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY, ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT and ACTIVE_BRAKE_MOD_INDEX_LIMIT are applicable only during deceleration in forward direction and not used during direction change.
2. ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY should be set higher than ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT for active braking operation.
3. During active (or closed loop) braking, I_{q_ref} is clamped to -ILIMIT. This (I_{q_ref} being clamped to -ILIMIT) may result in the speed PI loop getting saturated and SPEED_LOOP_SATURATION bit getting set to 1b during deceleration. This bit is automatically set to 0b once the deceleration is completed and the speed PI loop is out of saturation. Hence, speed loop saturation fault should be ignored during deceleration.
4. Active braking is available only in speed control mode.
5. Active braking is not available (even when ACTIVE_BRAKE_EN = 1b) when (bus) power limit feature (BUS_POWER_LIMIT_ENABLE = 1b) is enabled.

6.3.17 Output PWM Switching Frequency

MCF8315D provides the option to configure the output PWM switching frequency of the MOSFETs through PWM_FREQ_OUT. PWM_FREQ_OUT has range of 10-60 kHz. In order to select optimal output PWM switching

Copyright © 2025 Texas Instruments Incorporated

frequency, user has to make tradeoff between the current ripple and the switching losses. Generally, motors having lower L/R ratio require higher PWM switching frequency to reduce current ripple.

6.3.18 PWM Dithering

MCF8315D provides the option of PWM dithering to reduce the EMI generated by MOSFET switching - when enabled, the PWM switching frequency is varied continuously (within a user configured frequency range) around the PWM_FREQ_OUT setting to spread the EMI energy across the frequency spectrum and reduce the EMI peak values. The user configured frequency range for PWM dithering is set by PWM_DITHER_DEPTH; setting PWM_DITHER_DEPTH to 0x0 disables PWM dithering. PWM_DITHER_DEPTH provides ±5%, ±7.5% and ±10% frequency spread options. When PWM_FREQ_OUT is set to 25kHz and PWM_DITHER_DEPTH is set to ±10%, the PWM switching frequency applied to the MOSFETs continuously varies between 22.5kHz (25kHz-10%) and 27.5kHz (25kHz+10%), thereby reducing the EMI peaks at multiples of 25kHz. PWM dithering is available in two modes - random or triangular (configured by PWM_DITHER_MODE). In random dithering, the PWM switching frequency is continuously varied randomly within the range set by PWM_FREQ_OUT and PWM_DITHER_DEPTH. In triangular dithering, the PWM switching frequency is varied at user configured slew rate (configured by PWM_DITHER_STEP) as shown in Figure 6-53.

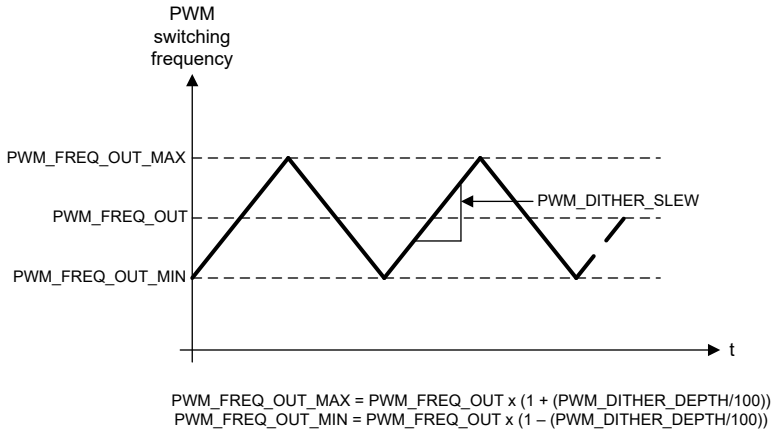


Figure 6-53. Triangular PWM Dithering

The PWM switching frequency slew rate (PWM_DITHER_SLEW in Figure 6-53) is set as shown in Equation 11.

$$\text{PWM\_DITHER\_SLEW (kHz/s)} = \text{PWM\_DITHER\_STEP} * \text{SLEW\_SCALING FACTOR} \quad (11)$$

SLEW_SCALING FACTOR varies with PWM switching frequency as listed in Table 6-5.

Table 6-5. SLEW_SCALING FACTOR vs PWM switching frequency

PWM switching frequency (kHz)	SLEW_SCALING FACTOR
10	1
15	2.25
20	2
25	3.125
30	4.5
35	3.0625
40	4
45	5.0625
50	6.25
55	7.5625
60	9

Copyright © 2025 Texas Instruments Incorporated

6.3.19 PWM Modulation Schemes

The MCF8315D supports two different modulation schemes, namely, continuous and discontinuous space vector PWM modulation schemes. In continuous PWM modulation, all the three phases switch all the time as per the defined switching frequency. In discontinuous PWM modulation, one of the phases is clamped to ground for 120° electrical period, and the other two phases are pulse width modulated. The modulation scheme is configured using PWM_MODE. Figure 6-54 shows the modulated average phase voltages for different modulation schemes.

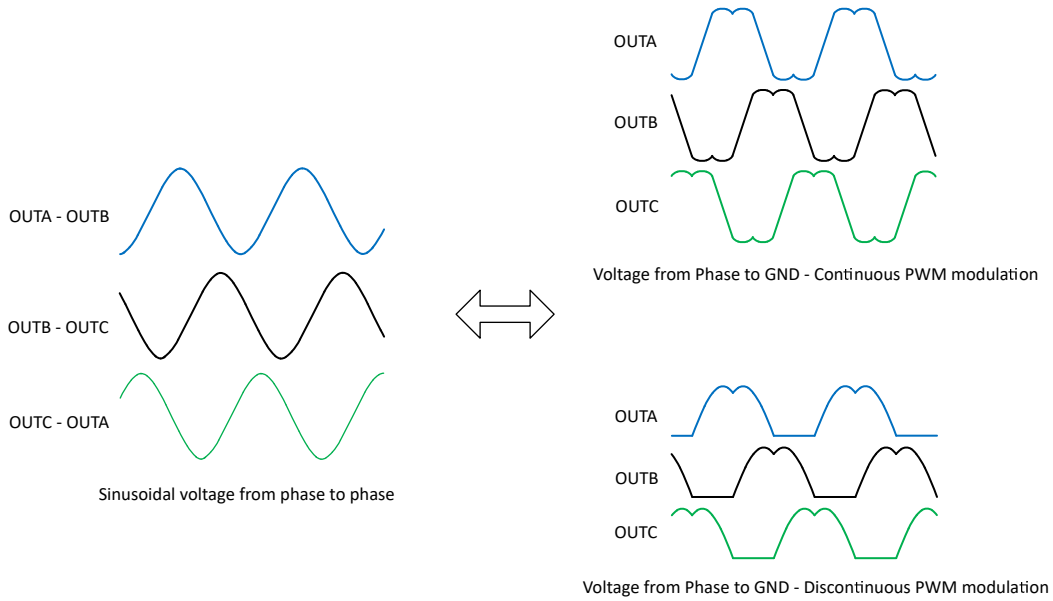


Figure 6-54. Continuous and Discontinuous PWM Modulation Phase Voltages

Continuous modulation helps in reducing current ripple for motors having low inductance but it results in higher switching losses because all three phases are switching. Discontinuous modulation has lower switching losses due to only two phases switching at a time, but higher current ripple.

6.3.20 Dead Time Compensation

Dead time is inserted between the switching instants of high-side and low-side MOSFETs in a half-bridge leg to avoid shoot-through condition. Due to dead time insertion, the expected voltage and applied voltage at the phase node differ based on the phase current direction. The phase node voltage distortion introduces undesired distortion in the phase current causing audible noise. MCF8315D integrates a proprietary dead time compensation technique to remove this phase current distortion and greatly reduce the audible noise, thereby significantly improving the acoustic performance of the FOC in MCF8315D. This dead time compensation can be enabled or disabled by configuring DEADTIME_COMP_EN. Even when DEADTIME_COMP_EN is set to 1b (compensation enabled), dead time compensation is disabled when motor electrical frequency exceeds 108Hz and re-enabled when motor electrical frequency drops below 102Hz.

6.3.21 Motor Stop Options

The MCF8315D provides different options for stopping the motor which can be configured by MTR_STOP.

6.3.21.1 Coast (Hi-Z) Mode

Coast (Hi-Z) mode is configured by setting MTR_STOP to 000b. When motor stop command is received, the MCF8315D will transition into a high impedance (Hi-Z) state by turning off all MOSFETs. When the MCF8315D transitions from driving the motor into a Hi-Z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the body diodes in the MOSFET output stage (see example Figure 6-55).

Copyright © 2025 Texas Instruments Incorporated

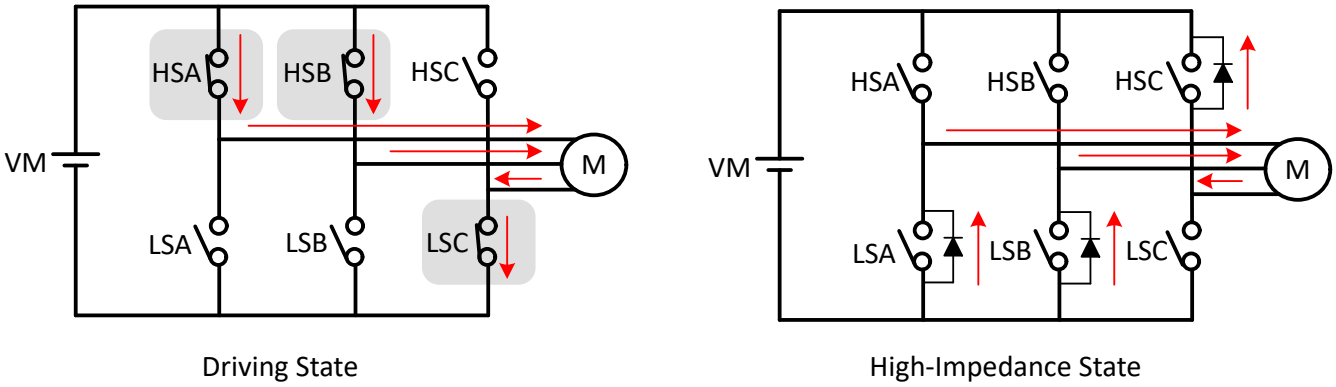


Figure 6-55. Coast (Hi-Z) Mode

In this example, current is applied to the motor through the high-side phase-A MOSFET (HSA), high-side phase-B MOSFET(HSB) and returned through the low-side phase-C MOSFET (LSC). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs LSA, LSB and HSC.

6.3.21.2 Recirculation Mode

Recirculation mode is configured by setting MTR_STOP to 001b. In order to prevent the inductive energy from returning to DC input supply during motor stop, the MCF8315D allows current to circulate within the MOSFETs by selectively turning OFF some of the active (ON) MOSFETs for a certain time (auto calculated recirculation time to allow the inductive current to decay to zero) before transitioning into Hi-Z by turning OFF the remaining MOSFETs.

Depending on the phase voltage pattern at the time of receiving the stop command, either low-side (see Figure 6-56) or high-side recirculation (see Figure 6-57) will be used to stop the motor without sending the inductive energy back to the DC input supply.

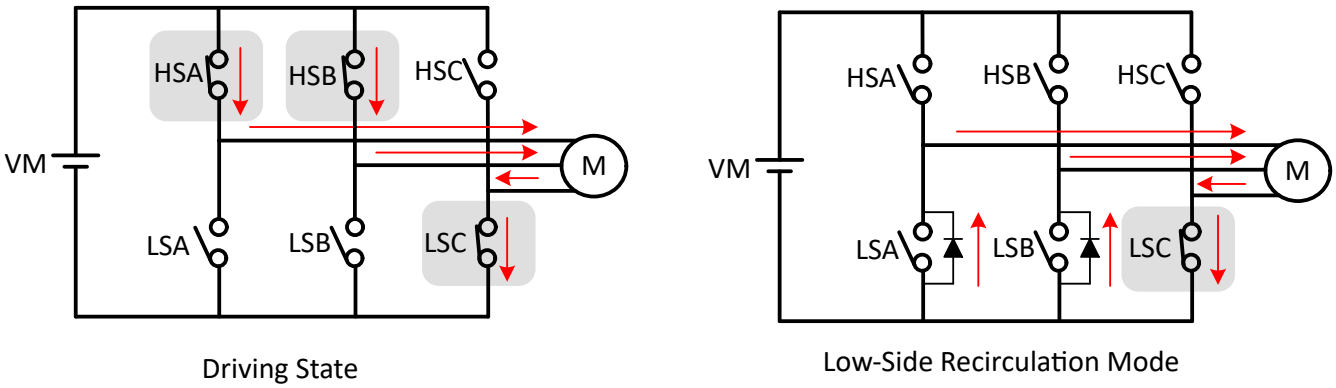


Figure 6-56. Low-Side Recirculation

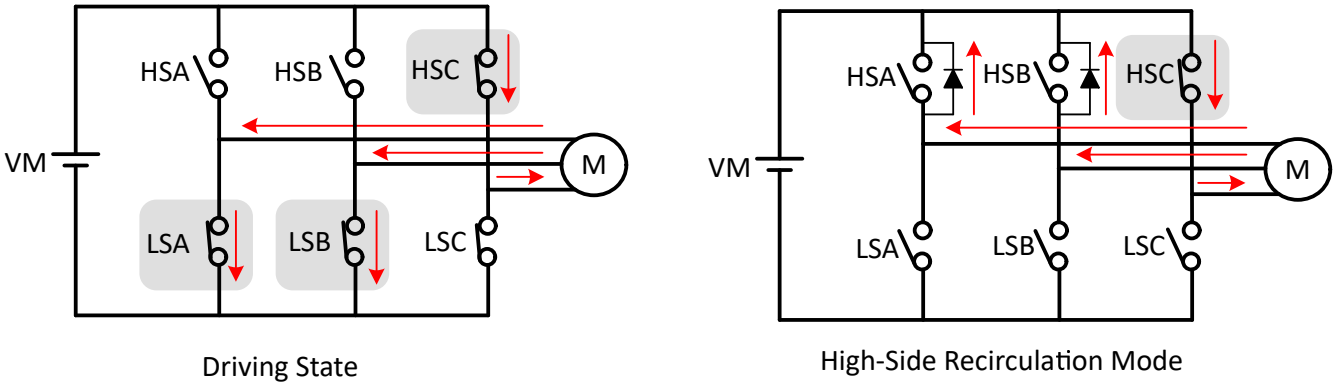


Figure 6-57. High-Side Recirculation

Note

Recirculation stop will not be available when the motor is in open loop state or active braking state or during flux weakening or when lead angle is non-zero; in such cases, the motor stop mode is set by LOW_SPEED_RECIRC_BRAKE_EN.

6.3.21.3 Low-Side Braking

Low-side braking mode is configured by setting MTR_STOP to 010b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all low-side MOSFETs ON (see example Figure 6-58) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below BRAKE_SPEED_THRESHOLD prior to receiving stop command, then the MCF8315D transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCF8315D transitions into the Hi-Z state by turning OFF all MOSFETs.

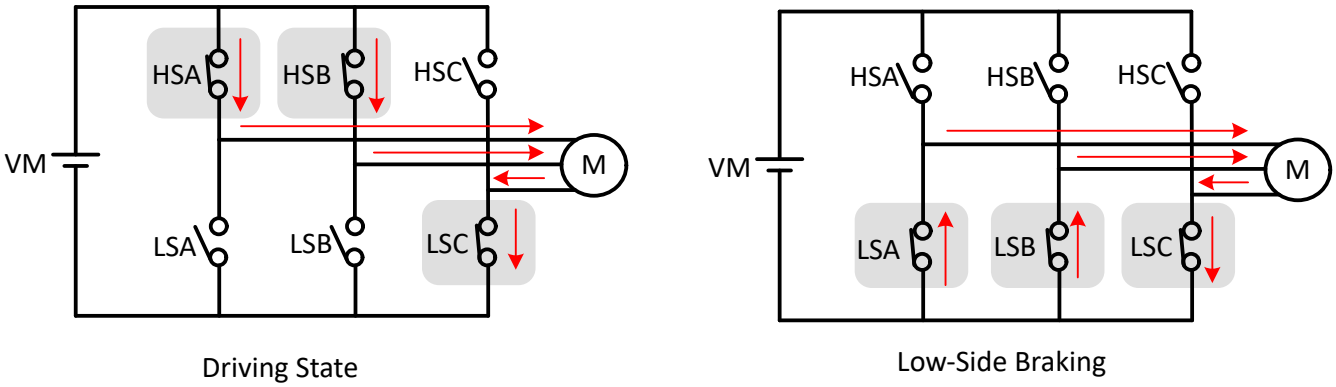


Figure 6-58. Low-Side Braking

The MCF8315D can also enter low-side braking through BRAKE pin input. When BRAKE pin is pulled to HIGH state, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all low-side MOSFETs ON. In this case, MCF8315D stays in low-side brake state till BRAKE pin changes to LOW state.

6.3.21.4 High-Side Braking

High-side braking mode is configured by setting MTR_STOP to 011b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all high-side MOSFETs ON (see example Figure 6-59) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below BRAKE_SPEED_THRESHOLD prior to receiving stop command, then the MCF8315D transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCF8315D transitions into Hi-Z state by turning OFF all MOSFETs.

Copyright © 2025 Texas Instruments Incorporated

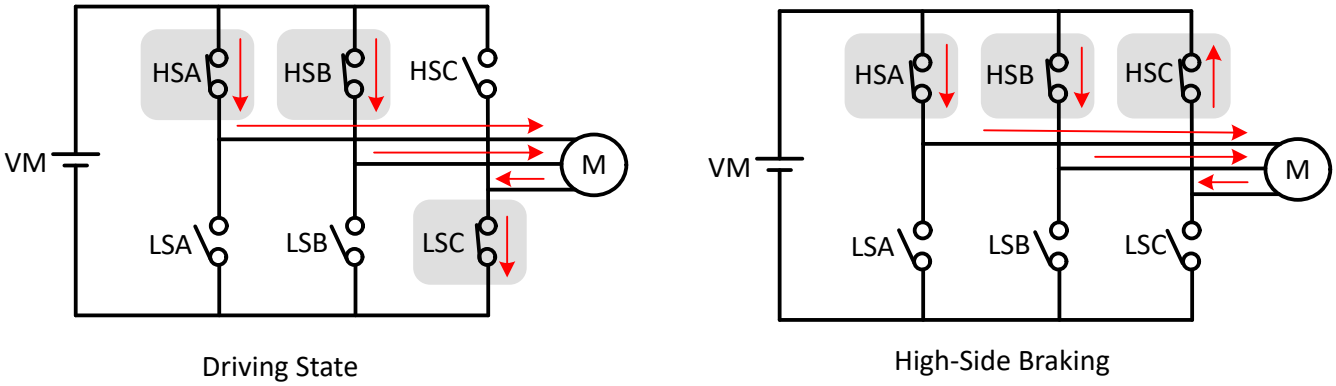


Figure 6-59. High-Side Braking

6.3.21.5 Active Spin-Down

Active spin down mode is configured by setting MTR_STOP to 100b. When a motor stop command is received, the MCF8315D reduces SPEED_REF to ACT_SPIN_THR and then transitions to Hi-Z state by turning all MOSFETs OFF. The advantage of this mode is that by reducing SPEED_REF, the motor is decelerated to lower speed thereby reducing the phase currents before entering Hi-Z. Now, when the motor transitions into Hi-Z state, the energy transfer to the power supply is reduced. The threshold ACT_SPIN_THR needs to configured high enough for MCF8315D to not lose synchronization with the motor.

6.3.22 Align Braking

Note

Align braking is available only when BRAKE_PIN_MODE is set to 1b.

Align braking is used to stop the motor at a user configured angle when a brake command is received either through a logic High signal on the BRAKE pin or by setting BRAKE_INPUT to 01b. In this mode, on receiving the brake command, MCF8315D reduces the motor speed to a value defined by BRAKE_SPEED_THRSHOLD before bringing the motor to an "aligned stop" by continuously injecting a DC current through a particular phase pattern. The phase pattern during align brake is generated based on the angle at which align needs to be performed - this angle can be configured either as the last commutation angle when BRAKE_SPEED_THRESHOLD is reached (ALIGN_BRAKE_ANGLE_SEL = 0b) or set directly using ALIGN_ANGLE (when ALIGN_BRAKE_ANGLE_SEL = 1b). The current limit during align braking is configured through ALIGN_OR_SLOW_CURRENT_ILIMIT.

6.3.23 FG Configuration

The MCF8315D provides information about the motor speed through the Frequency Generate (FG) pin. In MCF8315D, the FG pin output is configured through FG_CONFIG. When FG_CONFIG is configured to 0b, the FG output is active as long as the MCF8315D is driving the motor. When FG_CONFIG is configured to 1b, the MCF8315D provides an FG output until the motor back-EMF falls below FG_BEMF_THR.

6.3.23.1 FG Output Frequency

The FG output frequency can be configured by FG_DIV. Many applications require the FG output to provide a pulse for every mechanical rotation of the motor. Different FG_DIV configurations can accomplish this for 2-pole up to 30-pole motors. FG_DIV = 0000b provides an FG pulse every 120° (electrical) for backward compatibility with legacy 3-Hall sensored solutions.

Figure 6-60 shows the FG output when MCF8315D has been configured to provide FG pulses every 120° (elec.), once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.

Copyright © 2025 Texas Instruments Incorporated

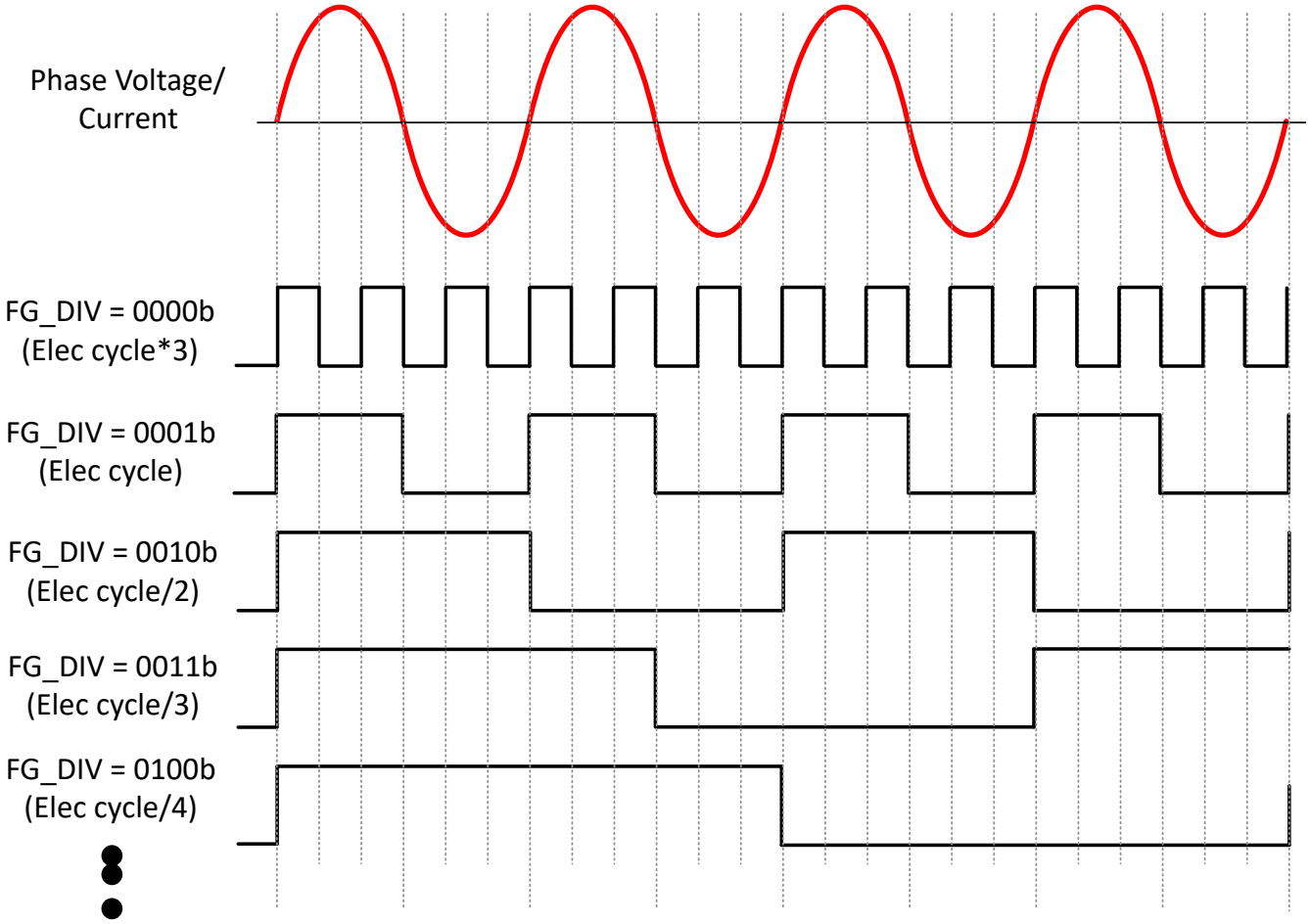


Figure 6-60. FG Frequency Divider

6.3.23.2 FG during Open and Closed Loop States

During closed loop operation, the driving speed (FG output frequency) and the actual motor speed are synchronized. During open-loop operation, however, FG may not reflect the actual motor speed.

The MCF8315D provides three options for controlling the FG output during open loop, as shown in Figure 6-61. The selection of these options is configured through FG_SEL.

If FG_SEL is set to,

- 00b: When in open loop, the FG output is based on the driving frequency.
- 01b: When in open loop, the FG output will be driven high.
- 10b: The FG output will reflect the driving frequency during open loop operation in the first motor start-up cycle after power-on, sleep/standby; FG will be held high during open loop operation in subsequent start-up cycles.

Copyright © 2025 Texas Instruments Incorporated

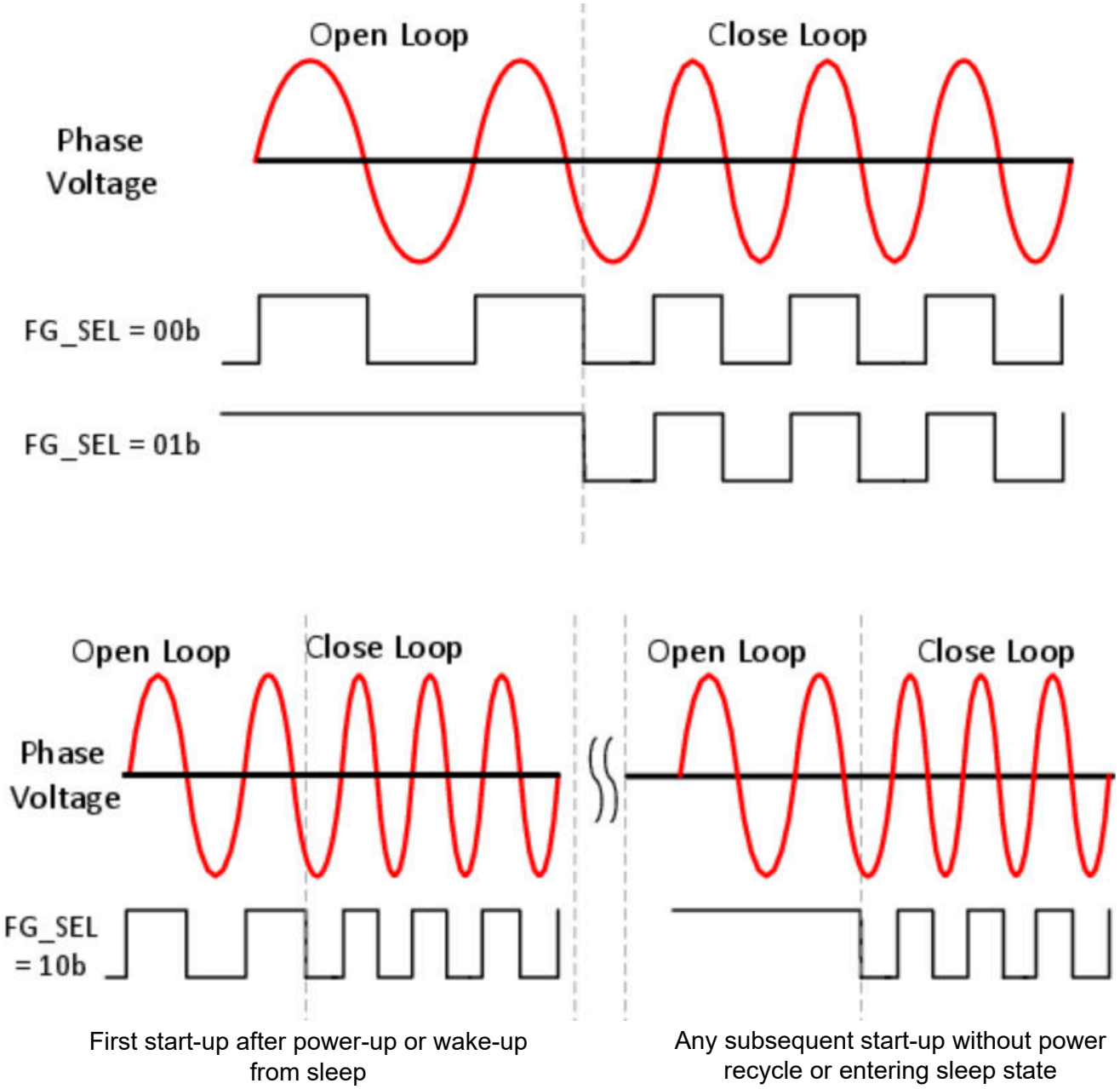


Figure 6-61. FG Behavior During Open Loop

6.3.23.3 FG during Fault and Idle States

MCF8315D provides the option of configuring FG output during fault and idle (motor stopped due to zero speed command) states. FG output during fault state is configured by FG_FAULT_CONFIG and FG output during idle state is configured by FG_IDLE_CONFIG - FG can be configured as a low or high signal during fault and can also be configured as a low or high signal during idle state. This allows the use of FG signal to uniquely determine the motor operating condition (fault, idle, spinning). For example, FG output during fault can be configured as a low signal and FG output during idle state can be configured as a high signal and FG during motor spinning can be configured to be at mechanical speed - a low FG output indicates MCF8315D encountered a fault condition, a high FG output indicates motor is in idle state and a FG signal at 50% duty indicates motor spinning at a speed equal to FG frequency.

Copyright © 2025 Texas Instruments Incorporated

Note

Motor is considered to be in stationary/idle state when back-EMF sensed at OUTx is less than STAT_DETECT_THR. STAT_DETECT_THR should be set sufficiently high to avoid spurious FG toggles due to noise in OUTx pins when motor is in stationary/idle state.

6.3.24 Protections

The MCF8315D is protected from a host of fault events including motor lock, VM undervoltage, AVDD undervoltage, buck undervoltage, charge pump undervoltage, overtemperature and overcurrent events. Table 6-6 summarizes the response, recovery modes, power stage status, reporting mechanism for different faults.

Note

1. Actionable faults (latched or retry) are always reported on nFAULT pin (as logic low).
2. Actionable faults (latched or retry) are reported on ALARM pin (as logic high) when ALARM_PIN_EN is set to 1b.
3. Report only faults are reported on nFAULT (as logic low) only when ALARM_PIN_EN is set to 0b. When ALARM_PIN_EN is set to 1b, report only faults are reported only on ALARM pin (as logic high) while nFAULT stays high (external or internal pull-up).
4. Priority order for multi-fault scenarios is latched > slower retry time fault > faster retry time fault > report only fault. For example, if a latched and retry fault happen simultaneously, the device stays latched in fault mode until user issues clear fault command by writing 1b to CLR_FLT. If two retry faults with different retry times happen simultaneously, the device retries only after the longer (slower) retry time lapses.
5. Recovery refers only to state of FETs (Hi-Z or active) after the fault condition is removed. Automatic indicates that the device automatically recovers (and FETs are active) when retry time lapses after the fault condition is removed. Latched indicates that the device waits for clearing of fault condition (by writing 1b to CLR_FLT bit) to make the FETs active again.
6. Actionable (latched or retry) faults can take up to 200-ms after fault response (FETs in Hi-Z) to be reported on nFAULT pin (as logic low), ALARM pin (as logic high) and fault status registers.
7. Latched faults can take up to 200-ms after CLR_FLT command is issued (over I^2C) to be cleared.
8. The fault state is latched when the cumulative number of automatic retry attempts (AUTO_RETRY_TIMES ≠ 000b) for all faults configured in automatic retry mode is reached. In this case, it is necessary to write 1b to CLR_FLT_RETRY_COUNT bit when writing 1b to CLR_FLT bit in ALGO_CTRL1 register to reset the retry counter to zero while clearing the latched fault state.

Table 6-6. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	DIGITAL	RECOVERY
VM undervoltage	$V_{VM} < V_{UVLO}$ (falling)	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO}$ (rising)
AVDD undervoltage	$V_{AVDD} < V_{AVDD\_UV}$ (falling)	—	—	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_UV}$ (rising)
Buck undervoltage (BUCK_UV)	$V_{FB\_BK} < V_{BK\_UV}$ (falling)	—	—	Active/Hi-Z	Active/Disabled	Automatic: $V_{FB\_BK} > V_{BK\_UV}$ (rising)
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPUV}$ (falling)	—	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$ (rising)
Over Voltage Protection (OVP)	$V_{VM} > V_{OVP}$ (rising)	OVP_EN = 0b	None	Active	Active	No action
		OVP_EN = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$ (falling)
Over Current Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		OCP_MODE = 01b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{RETRY}

Copyright © 2025 Texas Instruments Incorporated

Table 6-6. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	DIGITAL	RECOVERY
Buck Overcurrent Protection (BUCK_OCP)	$I_{BK} > I_{BK\_OCP}$	—	—	Hi-Z	Disabled	Automatic
Motor Lock (MTR_LCK)	Motor lock: Abnormal Speed; No Motor Lock; Abnormal BEMF	MTR_LCK_MODE = 000b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 001b	nFAULT and CONTROLLER_FAULT_STATUS register	Low- side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 010b	nFAULT and CONTROLLER_FAULT_STATUS register	High- side brake	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 011b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 100b	nFAULT and CONTROLLER_FAULT_STATUS register	Low- side brake	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 101b	nFAULT and CONTROLLER_FAULT_STATUS register	High- side brake	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 110b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		MTR_LCK_MODE = 111b	None	Active	Active	No action
Hardware Lock-Detection Current Limit (HW_LOCK_LIMIT)	V_{SOX} > HW_LOCK_ILIMIT	HW_LOCK_ILIMIT_MODE = 000b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 001b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 010b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 011b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MODE = 100b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MODE = 101b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MODE= 110b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		HW_LOCK_ILIMIT_MODE = 111b	None	Active	Active	No action

Copyright © 2025 Texas Instruments Incorporated

Table 6-6. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	DIGITAL	RECOVERY
Software Lock-Detection Current Limit (LOCK_LIMIT)	V_{SOX} > LOCK_ILIMIT	LOCK_ILIMIT_MODE = 000b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 001b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 010b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 011b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 100b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 101b	nFAULT and CONTROLLER_FAULT_STATUS register	High-side brake	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE= 110b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		LOCK_ILIMIT_MODE = 111b	None	Active	Active	No action
IPD Timeout Fault (IPD_T1_FAULT and IPD_T2_FAULT)	IPD TIME > 500ms (approx.), during IPD current ramp up or ramp down	IPD_TIMEOUT_FAULT_EN = 0b	—	Active	Active	No action
		IPD_TIMEOUT_FAULT_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
IPD Frequency Fault (IPD_FREQ_FAULT)	IPD pulse before the current decay in previous IPD pulse	IPD_FREQ_FAULT_EN = 0b	—	Active	Active	No action
		IPD_FREQ_FAULT_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Retry: t_{LCK_RETRY}
MPET IPD Fault (MPET_IPD_FAULT)	Same as IPD Timeout Fault during MPET R, L measurement	—	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
MPET Back-EMF Fault (MPET_BEMF_FAULT)	Motor Back EMF < STAT_DETECT_THR during MPET Ke and mechanical parameters measurement	—	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
Maximum VM (overvoltage) fault	V_{VM} > MAX_VM_MOTOR, if MAX_VM_MOTOR ≠ 000b	MAX_VM_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		MAX_VM_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Automatic: (V_{VM} < MAX_VM_MOTOR - VOLTAGE_HYSTERESIS)V
Minimum VM (undervoltage) fault	V_{VM} < MIN_VM_MOTOR, if MIN_VM_MOTOR ≠ 000b	MIN_VM_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
		MIN_VM_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Automatic: (V_{VM} > MIN_VM_MOTOR + VOLTAGE_HYSTERESIS)V
External Watchdog	Watchdog tickle does not arrive before configured time interval when EXT_WDT_EN =1b. Refer Section 6.5.5	EXT_WDT_FAULT_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		EXT_WDT_FAULT_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT

Copyright © 2025 Texas Instruments Incorporated

Table 6-6. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	FETs	DIGITAL	RECOVERY
Current Loop Saturation	Indication of current loop saturation due to lower V_{VM}	SATURATION_FLAGS_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed may not reach speed reference	Active	Automatic: motor will reach reference operating point upon exiting saturation
Speed Loop Saturation	Indication of speed loop saturation due to lower V_{VM}, lower ILIMIT setting etc.,	SATURATION_FLAGS_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed may not reach speed reference	Active	Automatic: motor will reach reference operating point upon exiting saturation
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	—	Active	Active	No action
		OTW_REP = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS register	Active	Active	No action
FET thermal shutdown (TSD_FET)	$T_J > T_{TSD\_FET}$	—	nFAULT and GATE_DRIVER_FAULT_STATUS register	Hi-Z	Active	Automatic: $T_J < T_{TSD\_FET} - T_{TSD\_FET\_HYS}$

6.3.24.1 VM Supply Undervoltage Lockout

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all the integrated FETs, driver charge-pump and digital logic are disabled as shown in Figure 6-62. MCF8315D goes into reset state whenever VM UVLO event occurs.

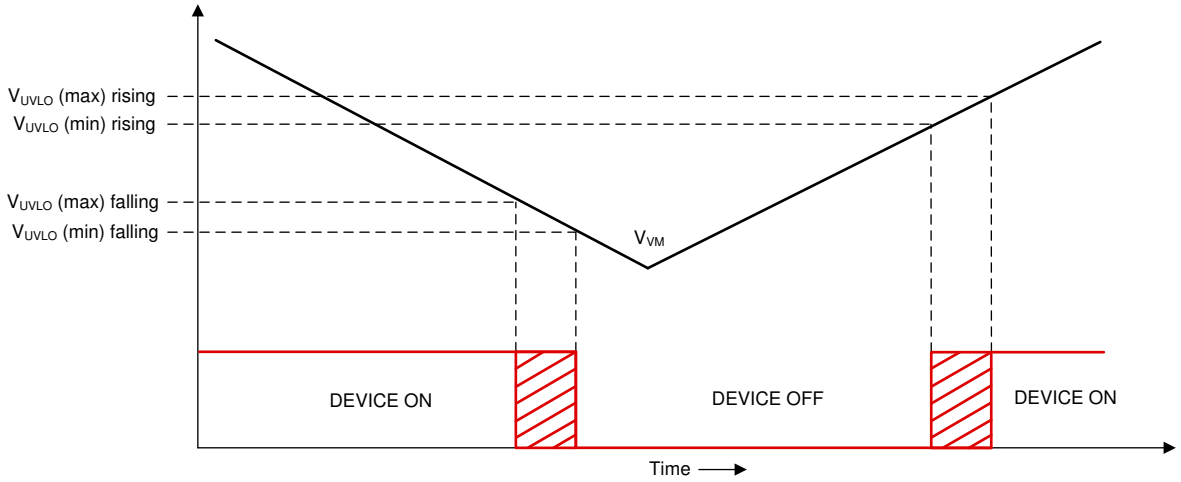


Figure 6-62. VM Supply Undervoltage Lockout

6.3.24.2 AVDD Undervoltage Lockout (AVDD_UV)

If at any time the voltage on the AVDD pin falls lower than the V_{AVDD_UV} threshold, all the integrated FETs, driver charge-pump and digital logic controller are disabled. Since internal circuitry in MCF8315D is powered through the AVDD regulator, MCF8315D goes into reset state whenever AVDD UV event occurs.

6.3.24.3 BUCK Under Voltage Lockout (BUCK_UV)

If at any time the voltage on the FB_BK pin falls lower than the V_{BK_UVLO} threshold, a buck UV fault is recognized - MCF8315D continues to attempt regulating the FB_BK voltage to set value. Since internal circuitry in MCF8315D is powered through the buck regulator, MCF8315D may go into reset state if FB_BK voltage drops low enough to trigger UV on the internal circuits.

6.3.24.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT and VCP_UV bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The VCP_UV bit stays set until cleared through the CLR_FLT bit.

6.3.24.5 Overvoltage Protection (OVP)

If at any time input supply voltage on the VM pins rises higher than V_{OVP}, all the integrated FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT and OVP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR_FLT bit. Setting the OVP_EN to 0b disables this protection feature.

The OVP threshold can be set to 22-V or 34-V based on the OVP_SEL bit.

Copyright © 2025 Texas Instruments Incorporated

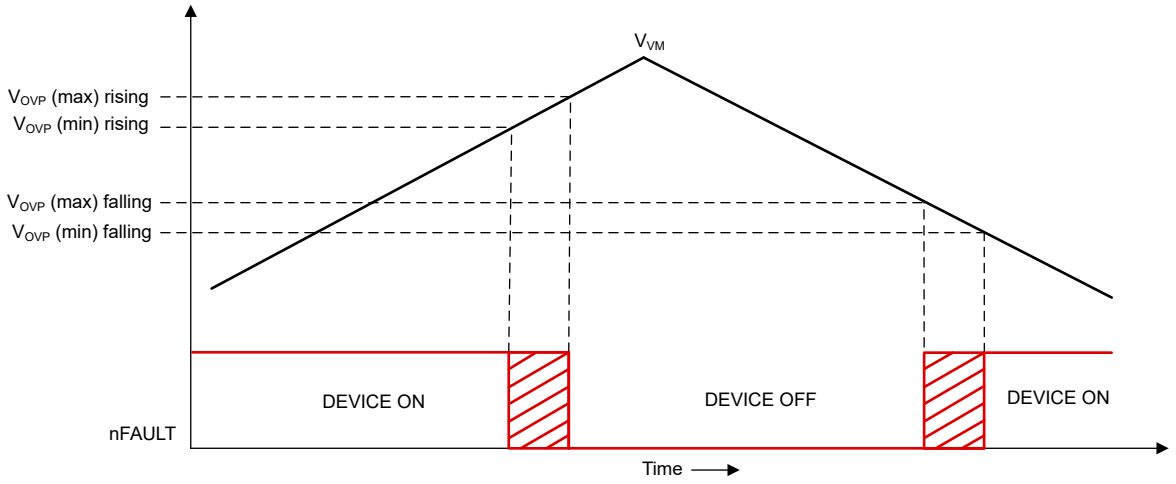


Figure 6-63. Over Voltage Protection

6.3.24.6 Overcurrent Protection (OCP)

MOSFET overcurrent event is sensed by monitoring the current flowing through the FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the deglitch time t_{OCP}, an OCP event is recognized and action is taken according to OCP_MODE. The I_{OCP} threshold is set through the OCP_LVL, t_{OCP} is set through OCP_DEG and the OCP_MODE can be configured in two different modes: latched shutdown and automatic retry.

6.3.24.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

When an OCP event happens in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the status registers. Normal operation resumes (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear fault command is issued through the CLR_FLT bit.

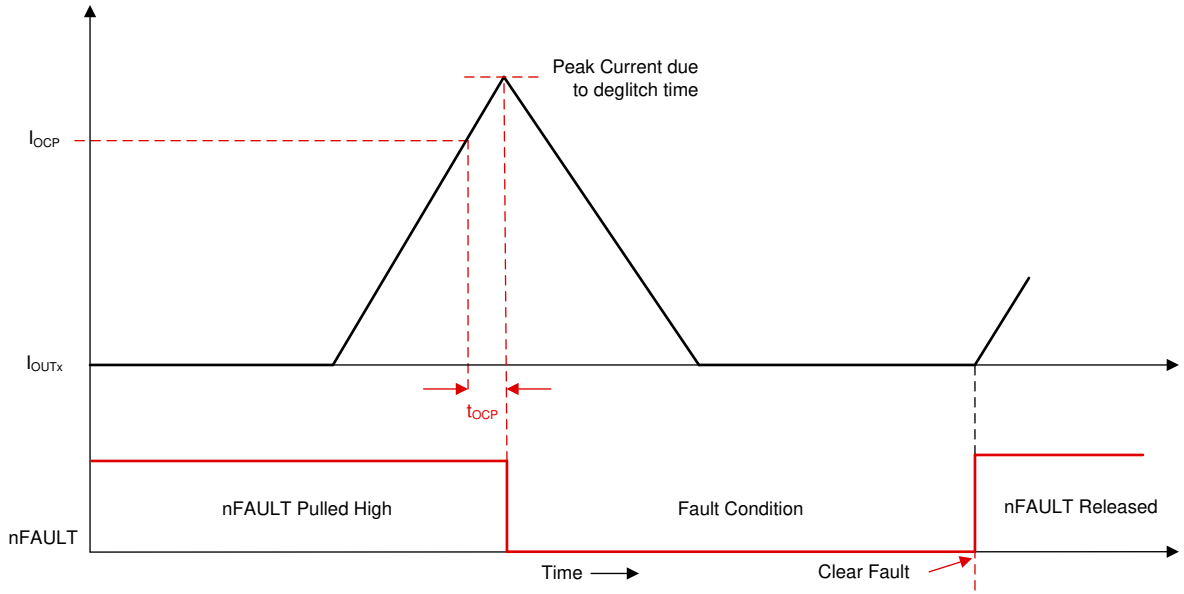


Figure 6-64. Overcurrent Protection - Latched Shutdown Mode

6.3.24.6.2 OCP Automatic Retry (OCP_MODE = 01b)

When an OCP event happens in this mode, all the FETs are disabled and the nFAULT pin is driven low. The DRIVER_FAULT, OCP and corresponding FET's OCP bits are set to 1b in the fault status registers.

Copyright © 2025 Texas Instruments Incorporated

Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} (TRETRY) time elapses. The DRIVER_FAULT bit is reset to 0b after the t_{RETRY} period expires. The OCP and corresponding FET's OCP bits are set to 1b until cleared through the CLR_FLT bit.

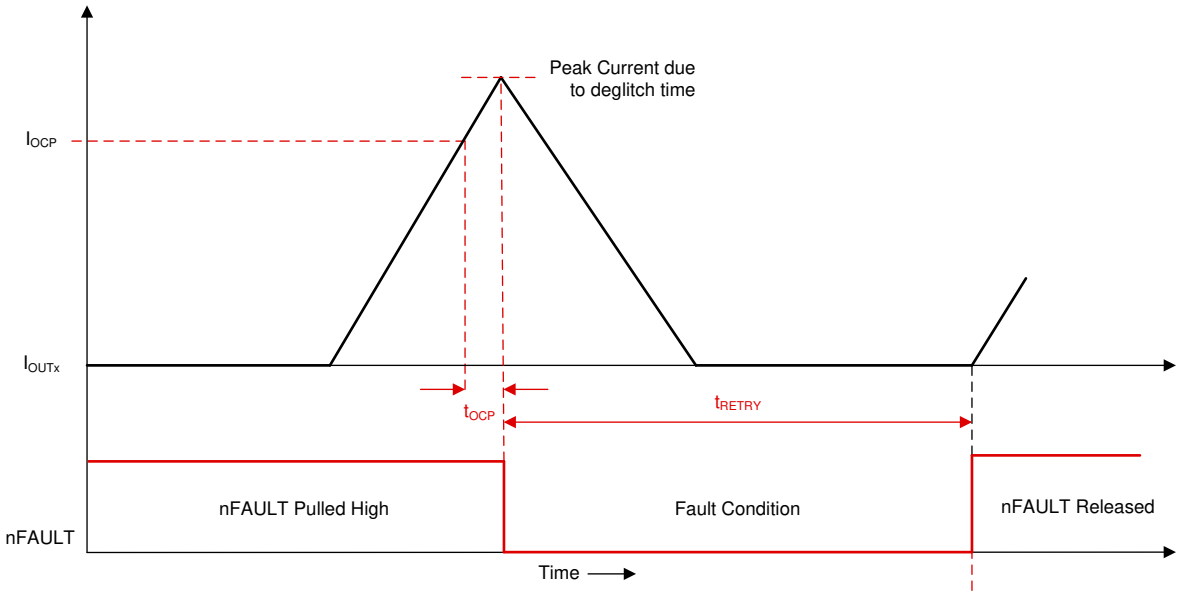


Figure 6-65. Overcurrent Protection - Automatic Retry Mode

6.3.24.7 Buck Overcurrent Protection

The buck overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current through the high-side MOSFET exceeds the I_{BK_OCP} threshold for a time longer than the deglitch time (t_{OCP}), a buck OCP event is recognized and the buck regulator MOSFETs are disabled (Hi-Z). MCF8315D goes into reset state whenever buck OCP event occurs, since the internal circuitry in MCF8315D is powered from the buck regulator output.

6.3.24.8 Hardware Lock Detection Current Limit (HW_LOCK_ILIMIT)

The hardware lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The MCF8315D continuously motor phase currents are using comparators. If at any time, any phase current exceeds HW_LOCK_ILIMIT threshold for a time longer than $t_{HW\_LOCK\_ILIMIT}$, a HW_LOCK_ILIMIT event is recognized and action is taken according to the HW_LOCK_ILIMIT_MODE. The current threshold is set by HW_LOCK_ILIMIT and the deglitch time, $t_{HW\_LCK\_ILIMIT}$ is set by HW_LOCK_ILIMIT_DEG. HW_LOCK_ILIMIT_MODE can be set in four different modes: HW_LOCK_ILIMIT latched shutdown, HW_LOCK_ILIMIT automatic retry, HW_LOCK_ILIMIT report only, and HW_LOCK_ILIMIT disabled.

6.3.24.8.1 HW_LOCK_ILIMIT Latched Shutdown

When a HW_LOCK_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW_LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFETs during HW_LOCK_ILIMIT:

- HW_LOCK_ILIMIT_MODE = 000b: All MOSFETs are turned OFF.
- HW_LOCK_ILIMIT_MODE = 001b: All low-side MOSFETs are turned ON.
- HW_LOCK_ILIMIT_MODE = 010b: All high-side MOSFETs are turned ON.

The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the HW_LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

Copyright © 2025 Texas Instruments Incorporated

6.3.24.8.2 HW_LOCK_ILIMIT Automatic Recovery

When a HW_LOCK_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW_LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFET during HW_LOCK_ILIMIT:

- HW_LOCK_ILIMIT_MODE = 011b: All MOSFETs are turned OFF.
- HW_LOCK_ILIMIT_MODE = 100b: All low-side MOSFETs are turned ON
- HW_LOCK_ILIMIT_MODE = 101b: All high-side MOSFETs are turned ON

The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are reset to 0b after the t_{LCK_RETRY} period expires.

6.3.24.8.3 HW_LOCK_ILIMIT Report Only

No protective action is taken when a HW_ LOCK_ILIMIT event happens in this mode (HW_LOCK_ILIMIT_MODE = 110b). The hardware lock detection current limit event is reported by setting the CONTROLLER_FAULT and HW_LOCK_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the HW_LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

6.3.24.8.4 HW_LOCK_ILIMIT Disabled

No action is taken when a HW_LOCK_ILIMIT event happens in this mode (HW_LOCK_ILIMIT_MODE = 111b).

6.3.24.9 Lock Detection Current Limit (LOCK_ILIMIT)

The lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The MCF8315D continuously monitors the motor phase currents through the ADC. If at any time, any phase current exceeds LOCK_ILIMIT for a time longer than t_{LCK_ILIMIT}, a LOCK_ILIMIT event is recognized and action is taken according to LOCK_ILIMIT_MODE. The current threshold is set by LOCK_ILIMIT and the deglitch time, t_{LCK_ILIMIT} is set by LOCK_ILIMIT_DEG. LOCK_ILIMIT_MODE can be set in four different modes: LOCK_ILIMIT latched shutdown, LOCK_ILIMIT automatic retry, LOCK_ILIMIT report only and LOCK_ILIMIT disabled.

6.3.24.9.1 LOCK_ILIMIT Latched Shutdown

When a LOCK_ILIMIT event happens in this mode, the status of MOSFETs will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFETs during LOCK_ILIMIT:

- LOCK_ILIMIT_MODE = 000b: All MOSFETs are turned OFF.
- LOCK_ILIMIT_MODE = 001b: All low-side MOSFETs are turned ON.
- LOCK_ILIMIT_MODE = 010b: All high-side MOSFETs are turned ON.

The CONTROLLER_FAULT and LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

6.3.24.9.2 LOCK_ILIMIT Automatic Recovery

When a LOCK_ILIMIT event happens in this mode, the status of MOSFETs will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFETs during LOCK_ILIMIT:

- LOCK_ILIMIT_MODE = 011b: All MOSFETs are turned OFF.
- LOCK_ILIMIT_MODE = 100b: All low-side MOSFETs are turned ON
- LOCK_ILIMIT_MODE = 101b: All high-side MOSFETs are turned ON

The CONTROLLER_FAULT and LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT and LOCK_ILIMIT bits are reset to 0b after the t_{LCK_RETRY} period expires.

Copyright © 2025 Texas Instruments Incorporated

6.3.24.9.3 LOCK_ILIMIT Report Only

No protective action is taken when a LOCK_ILIMIT event happens in this mode (LOCK_ILIMIT_MODE = 110b). The lock detection current limit event is reported by setting the CONTROLLER_FAULT and LOCK_ILIMIT bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

6.3.24.9.4 LOCK_ILIMIT Disabled

No action is taken when a LOCK_ILIMIT event happens in this mode (LOCK_ILIMIT_MODE = 111b).

6.3.24.10 Motor Lock Detection

The MCF8315D provides different lock detect mechanisms to determine if the motor is in a locked state. Multiple detection mechanisms work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCF8315D can also identify and take action if there is no motor connected to the system. Each of the lock detect mechanisms and the no-motor detection can be disabled by their respective register bits (LOCK1/2/3_EN).

6.3.24.10.1 Lock 1: Abnormal Speed (ABN_SPEED)

MCF8315D monitors the speed continuously and at any time the speed exceeds LOCK_ABN_SPEED, an ABN_SPEED lock event is recognized and action is taken according to the MTR_LCK_MODE. The threshold is set through the LOCK_ABN_SPEED register. ABN_SPEED lock can be enabled/disabled by LOCK1_EN.

6.3.24.10.2 Lock 2: Abnormal BEMF (ABN_BEMF)

MCF8315D estimates back-EMF in order to run motor optimally in closed loop. This estimated back-EMF is compared against the expected back-EMF calculated using the estimated speed and the BEMF constant. Whenever motor is stalled the estimated back-EMF is inaccurate due to lower back-EMF at low speed. When the difference between estimated and expected back-EMF exceeds ABNORMAL_BEMF_THR for ABNORMAL_BEMF_PERSISTENT_TIME, an abnormal BEMF fault is triggered and action is taken according to the MTR_LCK_MODE.

ABN_BEMF lock can be enabled/disabled by LOCK2_EN.

6.3.24.10.3 Lock3: No-Motor Fault (NO_MTR)

The MCF8315D continuously monitors phase currents on all three phases; if any phase current stays below NO_MTR_THR for 500ms, a NO_MTR event is recognized. The response to the NO_MTR event is configured through MTR_LCK_MODE. NO_MTR lock can be enabled/disabled by LOCK3_EN.

Note

- No motor fault is disabled when motor speed is < 2Hz.
- No motor fault is unavailable (even when enabled) during motor start-up (IPD or align or double align) state - it is available (when enabled) in open and closed loop states
- No motor fault detection during closed loop can be disabled by setting NO_MTR_FLT_ CLOSEDLOOP _DIS to 1b.

6.3.24.11 Motor Lock (MTR_LCK)

The MCF8315D continuously checks for different motor lock conditions (see Motor Lock Detection) during motor operation. When one of the enabled lock condition happens, a MTR_LCK event is recognized and action is taken according to the MTR_LCK_MODE.

All locks can be enabled or disabled individually and retry times can be configured through LCK_RETRY. MTR_LCK_MODE bit can operate in four different modes: MTR_LCK latched shutdown, MTR_LCK automatic retry, MTR_LCK report only and MTR_LCK disabled.

Copyright © 2025 Texas Instruments Incorporated

6.3.24.11.1 MTR_LCK Latched Shutdown

When a MTR_LCK event happens in this mode, the status of MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 000b: All MOSFETs are turned OFF.
- MTR_LCK_MODE = 001b: All low-side MOSFETs are turned ON.
- MTR_LCK_MODE = 010b: All high-side MOSFETs are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

6.3.24.11.2 MTR_LCK Automatic Recovery

When a MTR_LCK event happens in this mode, the status of MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 011b: All MOSFETs are turned OFF.
- MTR_LCK_MODE = 100b: All low-side MOSFETs are turned ON.
- MTR_LCK_MODE = 101b: All high-side MOSFETs are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are reset to 0b after the t_{LCK_RETRY} period expires.

6.3.24.11.3 MTR_LCK Report Only

No protective action is taken when a MTR_LCK event happens in this mode (MTR_LCK_MODE = 110b). The motor lock event is reported by setting the CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits to 1b in the fault status registers. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

6.3.24.11.4 MTR_LCK Disabled

No action is taken when a MTR_LCK event happens in this mode (MTR_LCK_MODE = 111b).

6.3.24.12 EEPROM Fault

MCF8315D provides an EEPROM fault detection feature to prevent device operation when there is EEPROM data mismatch due to an interrupted EEPROM write (UVLO during EEPROM write), EEPROM aging etc., MCF8315D implements a CRC and parity check whenever an EEPROM read command is issued - if there is a CRC or parity mismatch, an EEPROM fault is recognized and action taken according to EEP_FAULT_MODE. If EEP_FAULT_MODE is set to 0b, nFAULT is pulled low, the FETs are in Hi-Z and the CONTROLLER_FAULT and EEPROM_ERR_STATUS bits are set to 1b until the fault condition is cleared by writing 1b to CLR_FLT. If EEP_FAULT_MODE is set to 1b, this fault is reported on nFAULT pin and CONTROLLER_FAULT, EEPROM_ERR_STATUS bits are set to 1b but the device operation (FETs) continues normally. The fault reporting can be cleared (nFAULT pin is released, CONTROLLER_FAULT, EEPROM_ERR_STATUS set to 0b) by writing 1b to CLR_FLT.

Note

- An EEPROM read command is internally issued by the device at every power-up/wake-up to load the configurations from EEPROM into the shadow/RAM registers.
- A successful EEPROM write can fix EEPROM data mismatch. When an EEPROM write is successfully completed, MCF8315D automatically updates the internal CRC for the new EEPROM values - this updated CRC will be used during subsequent EEPROM read commands to check for EEPROM data mismatch.
- An EEPROM write can happen even when the device is in fault state.

Copyright © 2025 Texas Instruments Incorporated

6.3.24.13 I²C CRC Fault

MCF8315D provides I²C CRC fault detection feature to detect errors in an I²C transaction. MCF8315D implements a CRC check on the entire I²C packet when I²C CRC is enabled - if there is a CRC mismatch, an I²C CRC fault is recognized and action taken according to CRC_ERR_MODE. If CRC_ERR_MODE is set to 0b, nFAULT is pulled low, the FETs are in Hi-Z and the CONTROLLER_FAULT and I2C_CRC_FAULT_STATUS bits are set to 1b until the fault condition is cleared by writing 1b to CLR_FLT. If EEP_FAULT_MODE is set to 1b, this fault is reported on nFAULT pin and CONTROLLER_FAULT, I2C_CRC_FAULT_STATUS bits are set to 1b but the device operation (FETs) continues normally. The fault reporting can be cleared (nFAULT pin is released, CONTROLLER_FAULT, I2C_CRC_FAULT_STATUS set to 0b) by writing 1b to CLR_FLT.

6.3.24.14 Minimum VM (Undervoltage) Protection

MCF8315D provides a configurable VM undervoltage protection. The VM level at which MCF8315D triggers the undervoltage fault is set by MIN_VM_MOTOR and the fault response to VM undervoltage is set by MIN_VM_MODE. If MIN_VM_MODE is set to 0b, VM undervoltage fault (at MIN_VM_MOTOR) is latched and the FETs are in Hi-Z until the fault condition is cleared by writing 1b to CLR_FLT bit. If MIN_VM_MODE is set to 1b, VM undervoltage fault (at MIN_VM_MOTOR) automatically clears and the device starts motor operation once VM > (MIN_VM_MOTOR + VOLTAGE_HYSTERESIS).

6.3.24.15 Maximum VM (Overvoltage) Protection

MCF8315D provides a configurable VM overvoltage protection. The VM level at which MCF8315D triggers the overvoltage fault is set by MAX_VM_MOTOR and the fault response to VM overvoltage is set by MAX_VM_MODE. If MAX_VM_MODE is set to 0b, VM overvoltage fault (at MAX_VM_MOTOR) is latched and the FETs are in Hi-Z until the fault condition is cleared by writing 1b to CLR_FLT bit. If MAX_VM_MODE is set to 1b, VM overvoltage fault (at MAX_VM_MOTOR) automatically clears and the device starts motor operation once VM < (MAX_VM_MOTOR - VOLTAGE_HYSTERESIS).

6.3.24.16 MPET Faults

An error during resistance and inductance measurement is reported using MPET_IPD_FAULT. The MPET_IPD_FAULT gets triggered when the IPD timer overflows due to unsuccessful attempt to ramp up the current to the threshold value, same as explained in Section 6.3.24.17. The fault typically gets triggered when there is no motor connected to MCF8315D or when the MPET IPD current threshold is set high for motors with high resistance.

An error during BEMF constant measurement is reported using MPET_BEMF_FAULT. This fault gets triggered when the measured back EMF is less than the threshold set in STAT_DETECT_THR. One example of such fault scenario can be the motor stall while running in open loop due to incorrect open loop configuration used.

6.3.24.17 IPD Faults

The MCF8315D uses 12-bit timers to estimate the time during the current ramp up and ramp down during IPD, when the motor start-up is configured as IPD (MTR_STARTUP is set to 10b). During IPD, the algorithm checks for a successful current ramp-up to IPD_CURR_THR, starting with an IPD clock of 10MHz; if unsuccessful (timer overflow before current reaches IPD_CURR_THR), IPD is repeated with lower frequency clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD_CURR_THR) with all the four clock frequencies, then the IPD_T1_FAULT gets triggered. Similarly the algorithm checks for a successful current decay to zero during IPD current ramp down using all the mentioned IPD clock frequencies. If the IPD timer overflows (current does not ramp down to zero) in all the four attempts, then the IPD_T2_FAULT gets triggered. The user can enable IPD timeout (IPD timer overflow) by setting IPD_TIMEOUT_FAULT_EN to 1b.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCF8315D can generate a fault called IPD_FREQ_FAULT during such a scenario by setting IPD_FREQ_FAULT_EN to 1b. The IPD_FREQ_FAULT maybe triggered if the IPD frequency is too high for the IPD current limit and the IPD release mode or if the motor inductance is too high for the IPD frequency, IPD current limit and IPD release mode.

Copyright © 2025 Texas Instruments Incorporated

On the occurrence of any IPD fault, MCF8315D stops the IPD based start-up process and FETs are in Hi-Z. MCF8315D automatically retries IPD based start-up after t_{LCK_RETRY} elapses.

6.3.24.18 FET Thermal Warning (OTW)

If the FET temperature exceeds the FET thermal warning limit (T_{OTW}), nFAULT is pulled low and the OT and OTW bits in the gate driver status register are set to 1b. The reporting of OTW (on nFAULT and status bits) can be enabled by setting OTW_REP to 1b. The device performs no additional action and continues to function. The nFAULT pin is pulled low and OTW bit remains set until cleared through the CLR_FLT bit and the die temperature is lower than thermal warning limit. (T_{OTW} - T_{OTW_HYS}).

6.3.24.19 FET Thermal Shutdown (TSD_FET)

If the FET temperature exceeds the FET thermal shutdown limit (T_{TSD_FET}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the DRIVER_FAULT, OT and OTS bit in the status register are set to 1b. Normal operation resumes (driver operation and the nFAULT pin is released) when the die temperature decreases below the hysteresis point of the thermal shutdown limit (T_{TSD_FET} - $T_{TSD\_FET\_HYS}$). The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

Note

If die temperature increases to T_{TSD_BUCK}, MCF8315D will undergo a reset and all fault status bits in this case will be reset to 0b.

Copyright © 2025 Texas Instruments Incorporated

6.4 Device Functional Modes

6.4.1 Functional Modes

6.4.1.1 Sleep Mode

In sleep mode, the MOSFETs, sense amplifiers, buck regulator, charge pump, AVDD LDO regulator and the I^2C bus are disabled. The device can be configured to enter sleep (instead of standby) mode by configuring DEV_MODE to 1b. SPEED pin and I^2C speed command determine entry and exit from sleep state as described in Table 6-8.

6.4.1.2 Standby Mode

The device can be configured to operate as a standby device by setting DEV_MODE to 0b. In standby mode, the charge pump, AVDD LDO, buck regulator and I^2C bus are active while the motor is in stopped state waiting for a suitable non-zero speed command. SPEED pin (analog, PWM or frequency based speed input) or I^2C speed command (I^2C based speed input) determines entry and exit from standby state as described in Table 6-8.

The thresholds for entering and exiting standby mode in different input modes are as follows,

Table 6-7. Standby Mode Entry/Exit Thresholds

Input Source (SPEED_MODE)	Standby entry/exit thresholds	REF_PROFILE_CONFIG = 00b	REF_PROFILE_CONFIG ≠ 00b
Analog (00b)	V_{EN_SB}	1% x V_{ANA_FS}	1% x V_{ANA_FS}
	V_{EX_SB}	5% x V_{ANA_FS}	5% x V_{ANA_FS}
PWM (01b)	$Duty_{EX\_SB/EN\_SB}$	Maximum of (1%, DUTY_HYS)	0%
I^2C (10b)	$DIGITAL\_SPEED\_CTRL_{EX\_SB/EN\_SB}$	Maximum of (1%, DUTY_HYS) x 32767	0
Frequency (11b)	$Freq_{EX\_SB/EN\_SB}$	Maximum of (1%, DUTY_HYS) x INPUT_MAXIMUM_FREQ (subject to minimum of 3Hz)	< 3Hz

Table 6-8. Conditions to Enter or Exit Sleep/Standby Modes

SPEED COMMAND MODE	ENTER STANDBY CONDITION	EXIT FROM STANDBY CONDITION	ENTER SLEEP CONDITION	EXIT FROM SLEEP CONDITION
Analog	$V_{SPEED} < V_{EN\_SB}$	$V_{SPEED} > V_{EX\_SB}$	$V_{SPEED} < V_{EN\_SL}$ for $t_{DET\_SL\_ANA}$	$V_{SPEED} > V_{EX\_SL}$ for t_{DET_ANA}
PWM	$Duty_{SPEED} < Duty_{EN\_SB}$	$Duty_{SPEED} > Duty_{EX\_SB}$	$V_{SPEED} < V_{IL}$ for $t_{DET\_SL\_PWM}$	$V_{SPEED} > V_{IH}$ for t_{DET_PWM}
I^2C	DIGITAL_SPEED_CTRL < $DIGITAL\_SPEED\_CTRL_{EN\_SB}$	DIGITAL_SPEED_CTRL > $DIGITAL\_SPEED\_CTRL_{EX\_SB}$	DIGITAL_SPEED_CTRL is set to 0b for SLEEP_ENTRY_TIME and $V_{SPEED} < V_{IL}$	$V_{SPEED} > V_{IH}$ for t_{DET_PWM}
Frequency	$Freq_{SPEED} < Freq_{EN\_SB}$	$Freq_{SPEED} > Freq_{EX\_SB}$	$V_{SPEED} < V_{IL}$ for $t_{DET\_SL\_PWM}$	$V_{SPEED} > V_{IH}$ for t_{DET_PWM}

Note

V_{SPEED} : SPEED pin input voltage, $Duty_{SPEED}$: SPEED pin input PWM duty, $Freq_{SPEED}$: SPEED pin input frequency

6.4.1.3 Fault Reset (CLR_FLT)

In the case of latched faults, the device goes into a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR_FLT to 1b.

Copyright © 2025 Texas Instruments Incorporated

6.5 External Interface

6.5.1 DRVOFF Functionality

When DRVOFF pin is driven high, all six MOSFETs are put in Hi-Z state, irrespective of speed command. If motor speed command is non-zero when DRVOFF is driven high, device may encounter a fault like no motor or abnormal BEMF. Whenever DRVOFF is driven high, it should be held high for a minimum of 10s for safe operation.

6.5.2 DAC outputs

MCF8315D has two 12-bit DACs which output analog voltage equivalent of digital variables on the DACOUT1 and DACOUT2 pins. The maximum DAC output voltage is 3-V. Signals available on DACOUT pins are useful in tracking internal variables in real-time and can be used for tuning speed controller or motor acceleration time. The address for variables to be tracked on DACOUT1 and DACOUT2 are configured using DACOUT1_VAR_ADDR and DACOUT2_VAR_ADDR respectively. DACOUT1 is available on pin 36 and DACOUT2 can be configured on pin 38 by setting DAC_SOx_SEL to 00b. DACOUT2 is also available on pin 37. DAC_ENABLE should be configured to 1b for pins 36, 37 to function as DAC outputs.

6.5.3 Current Sense Output

MCF8315D can provide the built-in current sense amplifiers' output on the SOX pin. SOX output is available on pin 38 and can be configured by DAC_SOx_SEL.

6.5.4 Oscillator Source

MCF8315D has a built-in oscillator that is used as the clock source for all digital peripherals and timing measurements. Default configuration for MCF8315D is to use the internal oscillator and it is sufficient to drive the motor without need for any external crystal or clock sources.

In case MCF8315D does not meet accuracy requirements of timing measurement or speed loop, then MCF8315D has an option to support an external clock reference.

In order to improve EMI performance, MCF8315D provides the option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SPREAD_SPECTRUM_MODULATION_DIS.

6.5.4.1 External Clock Source

Speed loop accuracy of MCF8315D over the operating temperature range can be improved by providing a more accurate clock reference on EXT_CLK pin as shown in Figure 6-66. EXT_CLK will be used to calibrate the internal clock oscillator - this will help match the accuracy of the internal clock oscillator to that of the external clock. External clock source can be selected by setting EXT_CLK_EN to 1b. The external clock source frequency can be configured through EXT_CLK_CONFIG.

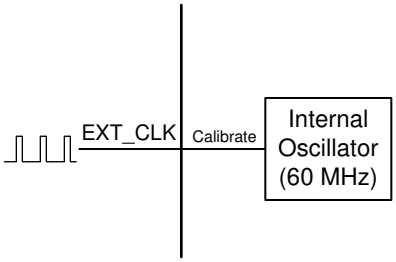


Figure 6-66. External Clock Reference

Note

External clock is optional and can be used when higher clock accuracy is needed. MCF8315D will always power up using the internal oscillator in all modes.

Copyright © 2025 Texas Instruments Incorporated

6.5.5 External Watchdog

MCF8315D provides an external watchdog feature - EXT_WDT_EN bit should be set to 1b to enable the external watchdog. When this feature is enabled, the device waits for a tickle (low to high transition in EXT_WD pin, WATCHDOG_TICKLE set to 1b in I^2C mode) from the external watchdog input for a configured time interval; if the time interval between two consecutive tickles is higher than the configured time, a watchdog fault is triggered. The watchdog fault response can be configured using EXT_WDT_FAULT_MODE either as a report only fault or as a latched fault with MOSFETs in Hi-Z state. The latched fault can be cleared by writing 1b to CLR_FLT. When a watchdog timeout occurs, WATCHDOG_FAULT bit is set to 1b. In case, the next tickle arrives before the configured time interval elapses, the watchdog timer is reset and it begins to wait for the next tickle. This can be used to continuously monitor the health of an external MCU (which is the external watchdog input) and put the MCF8315D MOSFETs in Hi-Z, in case the external MCU is in a fault/hang state.

The external watchdog input is selected using EXT_WDT_INPUT_MODE and can either be the EXT_WD pin or the I^2C interface. The time interval between two tickles to trigger a watchdog fault is configured by EXT_WDT_CONFIG; there are 4 time settings - 100, 200, 500 and 1000ms for the EXT_WD pin based watchdog and 4 time settings - 1, 2, 5 and 10s for the I^2C based watchdog.

Note

Watchdog should be disabled by setting EXT_WDT_EN to 0b before changing EXT_WDT_CONFIG configuration.

Copyright © 2025 Texas Instruments Incorporated

6.6 EEPROM access and I²C interface

6.6.1 EEPROM Access

MCF8315D has 1024 bits (16 rows of 64 bits each) of EEPROM, which are used to store the motor configuration parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit write and read operations are supported. EEPROM can be written and read using the I²C serial interface but erase cannot be performed using I²C serial interface. The shadow/RAM registers corresponding to the EEPROM are located at addresses 0x000080-0x0000AE.

Note

MCF8315D allows EEPROM write and read operations only when the motor is not spinning.

6.6.1.1 EEPROM Write

Note

- EEPROM write should be issued only when device is in idle or fault state (motor not driven by device). VM should be ≥ 6V throughout the EEPROM write process to ensure that all power rails (AVDD, FB_BK and DVDD) stay within datasheet specifications and EEPROM write is never interrupted due to any UVLO condition.
- TI does not recommend writing to EEPROM during every power-up/wake-up due to aging/write cycle limitations on number of EEPROM writes (20000 write cycles at T_J = 85°C). Repetitive register settings change can be done at shadow/RAM registers (0x000080-0x0000AE); only default configurations need to be written to EEPROM (at first power-up)

In MCF8315D, EEPROM write procedure is as follows,

1. Write register 0x000080 (ISD_CONFIG) with ISD and reverse drive configuration like resync enable, reverse drive enable, stationary detect threshold, reverse drive handoff threshold etc.
2. Write register 0x000082 (REV_DRIVE_CONFIG) with reverse drive and active brake configuration like reverse drive open loop acceleration, active brake current limit, Kp, Ki values etc.
3. Write register 0x000084 (MOTOR_STARTUP1) with motor start-up configuration like start-up method, IPD parameters, align parameters etc.
4. Write register 0x000086 (MOTOR_STARTUP2) with motor start-up configuration like open loop acceleration, open loop current limit, first cycle frequency etc.
5. Write register 0x000088 (CLOSED_LOOP1) with motor control configuration like closed loop acceleration, overmodulation enable, PWM frequency, FG signal parameters etc.
6. Write register 0x00008A (CLOSED_LOOP2) with motor control configuration like motor winding resistance and inductance, motor stop options, brake speed threshold etc.
7. Write register 0x00008C (CLOSED_LOOP3) with motor control configuration like motor BEMF constant, current loop Kp, Ki etc.
8. Write register 0x00008E (CLOSED_LOOP4) with motor control configuration like speed loop Kp, Ki and maximum speed.
9. Write register 0x000090 (FAULT_CONFIG1) with fault control configuration software and hardware current limits, lock current limit and actions, retry times etc.
10. Write register 0x000092 (FAULT_CONFIG2) with fault control configuration like hardware current limit actions, OV, UV limits and actions, abnormal speed level, no motor threshold etc.
11. Write registers 0x000094 – 0x00009E (SPEED_PROFILES1-6) with speed profile configuration like profile type, duty cycle, speed clamp level, duty cycle clamp level etc.
12. Write register 0x0000A0 (INT_ALGO_1) with miscellaneous configuration like ISD run time and timeout, MPET parameters etc.
13. Write register 0x0000A2 (INT_ALGO_2) with miscellaneous configuration like additional MPET parameters, IPD high resolution enable, active brake current slew rate, closed loop slow acceleration etc.
14. Write registers 0x0000A4 (PIN_CONFIG1) with pin configuration for speed input mode (analog or PWM), BRAKE pin mode etc.

Copyright © 2025 Texas Instruments Incorporated

15. Write registers 0x0000A6 and 0x0000A8 (DEVICE_CONFIG1 and DEVICE_CONFIG2) with device configuration like DAC/SOX, I²C target address, dynamic CSA gain enable, dynamic voltage gain enable, clock source select, speed range select etc.
16. Write register 0x0000AA (PERI_CONFIG1) with peripheral configuration like dead time, bus current limit, DIR input, SSM enable etc.
17. Write registers 0x0000AC and 0x0000AE (GD_CONFIG1 and GD_CONFIG2) with gate driver configuration like slew rate, CSA gain, OCP level, mode, OVP enable, level, buck voltage level, buck current limit etc.
18. Write 0x8A500000 into register 0x0000EA to write the shadow/RAM register (0x000080-0x0000AE) values into the EEPROM.
19. Wait for 750ms for the EEPROM write operation to complete.
20. After 750ms, read 0x0000EA register to ensure it has been reset to 0x0. This confirms that the EEPROM write process has been completed successfully.

Steps 1-17 can be selectively executed based on registers/parameters that need to be modified. After all shadow/RAM registers have been updated with the required values, steps 18-20 should be executed to write the contents of the shadow/RAM registers into the EEPROM.

6.6.1.2 EEPROM Read

In MCF8315D, EEPROM read procedure is as follows,

1. Write 0x40000000 into register 0x0000EA to read the EEPROM data into the shadow/RAM registers (0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow/RAM register values, one or two registers at a time, using the I²C read command as explained in Section 6.6.2. Shadow/RAM register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation (since each address is a 16-bit location).

6.6.1.3 EEPROM Security

MCF8315D provides configurable read and write protection to EEPROM registers. The level of protection can be configured using EEPROM_LOCK_MODE as per following list,

- 00b : EEPROM read and write are allowed without a passcode
- 01b : EEPROM read and write need a valid passcode
- 10b : EEPROM read needs a valid passcode; EEPROM write is locked permanently
- 11b : EEPROM read and write are locked permanently

Passcode is a 15-bit field in the EEPROM denoted by EEPROM_LOCK_KEY in the DEVICE_CONFIG1 register. EEPROM_LOCK_KEY is write accessible (when EEPROM_LOCK_MODE is set to 00b or 01b) but not read accessible.

When passcode based read/write protection is enabled (EEPROM_LOCK_MODE set to 01b or 10b), user has to write the passcode set in EEPROM_LOCK_KEY to USER_EEPROM_KEY bitfield in 0xF8 register after every power-up/wake-up before sending the first EEPROM read/write transaction over I²C. One valid passcode write after power-up/wake-up is sufficient for all subsequent EEPROM read/write transactions as long as there is no power reset, sleep mode entry, digital reset or incorrect passcode write. If an invalid passcode is written, the subsequent EEPROM read/write transactions are rejected - MCF8315D does not respond to the read/write requests. The read/write protection is applicable to EEPROM as well as the corresponding shadow/RAM locations. The EEPROM_LOCK_MODE as well as the passcode are part of the EEPROM registers and hence same level of read/write protection applies to these bit fields as configured by EEPROM_LOCK_MODE.

6.6.2 I²C Serial Interface

MCF8315D interfaces with an external MCU over an I²C serial interface. MCF8315D is an I²C target to be interfaced with a controller. External MCU can use this interface to read/write from/to any non-reserved register in MCF8315D.

Copyright © 2025 Texas Instruments Incorporated

Note

For reliable communication, a 100-µs delay should be used between every byte transferred over the I²C bus.

6.6.2.1 I²C Data Word

The I²C data word format is shown in Table 6-9.

Table 6-9. I²C Data Word Format

TARGET_ID	R/W	CONTROL WORD	DATA	CRC-8
A6 - A0	W0	CW23 - CW0	D15 / D31/ D63 - D0	C7 - C0

Target ID and R/W Bit: The first byte includes the 7-bit I²C target ID, followed by the read/write command bit. Every packet in MCF8315D the communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

24-bit Control Word: The Target Address is followed by a 24-bit control bit. The control word format is shown in Table 6-10.

Table 6-10. 24-bit Control Word Format

OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR
CW23	CW22	CW21- CW20	CW19 - CW16	CW15 - CW12	CW11 - CW0

Each field in the control word is explained in detail below.

OP_R/W – Read/Write: R/W bit gives information on whether this is a read (1b) operation or write (0b) operation. For write operation, MCF8315D will expect data bytes to be sent after the 24-bit control word. For read operation, MCF8315D will expect an I²C read request with repeated start or normal start after the 24-bit control word.

CRC_EN – Cyclic Redundancy Check(CRC) Enable: MCF8315D supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

DLEN – Data Length: DLEN field determines the length of the data that will be sent by external MCU to MCF8315D. MCF8315D protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

Table 6-11. Data Length Configuration

DLEN Value	Data Length
00b	16-bit
01b	32-bit
10b	64-bit
11b	Reserved

MEM_SEC – Memory Section: Each memory location in MCF8315D is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

MEM_PAGE – Memory Page: Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

MEM_ADDR – Memory Address: Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCF8315D using all three fields – Memory Section, Memory Page, Memory Address. For memory locations 0x000000-0x000800, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x800 for 0x000800). All relevant memory locations (EEPROM and RAM variables) have MEM_SEC and MEM_PAGE values both corresponding to 0x0. All other MEM_SEC, MEM_PAGE values are reserved and not for external use.

Copyright © 2025 Texas Instruments Incorporated

Data Bytes: For a write operation to MCF8315D, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section. In case of mismatch between number of data bytes and DLEN, the write operation is discarded.

CRC Byte: If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Refer to Section 6.6.2.6 for detailed information on CRC byte calculation.

6.6.2.2 I²C Write Transaction

MCF8315D write transaction over I²C involves the following sequence (see Figure 6-67).

1. I²C start condition.
2. Start is followed by the I²C target ID byte, made up of 7-bit target ID along with the R/W bit set to 0b. ACK in yellow box indicates that MCF8315D has processed the received target ID which has matched with it's I²C target ID and therefore will proceed with this transaction. If target ID received does not match with the I²C ID of MCF8315D, then the transaction is ignored. and no ACK is sent by MCF8315D.
3. The target ID byte is followed by the 24-bit control word sent one byte at a time. Bit 23 in the control word is 0b as it is a write transaction. ACK in blue boxes correspond to acknowledgements sent by MCF8315D to the controller that the previous byte (of control word) has been received and next byte can be sent.
4. The 24-bit control word is then followed by the data bytes. The number of data bytes sent by the controller depends on the DLEN field in the control word.
   a. While sending data bytes, the LSB byte is sent first. Refer to Section 6.6.2.4 for more details.
   b. 16-bit/32-bit write – The data sent is written to the address mentioned in control word.
   c. 64-bit Write – 64-bit is treated as two successive 32-bit writes. The address mentioned in control word is taken as Addr_1. Addr_2 is internally calculated by MCF8315D by incrementing Addr_1 by 0x2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first) are written to Addr_1 and the next 4 bytes are written to Addr_2.
   d. ACK in blue boxes (after every data byte) correspond to the acknowledgement sent by MCF8315D to the controller that the previous data byte has been received and next data byte can be sent.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes). MCF8315D will send an ACK on receiving the CRC byte.
6. I²C Stop condition from the controller to terminate the transaction.

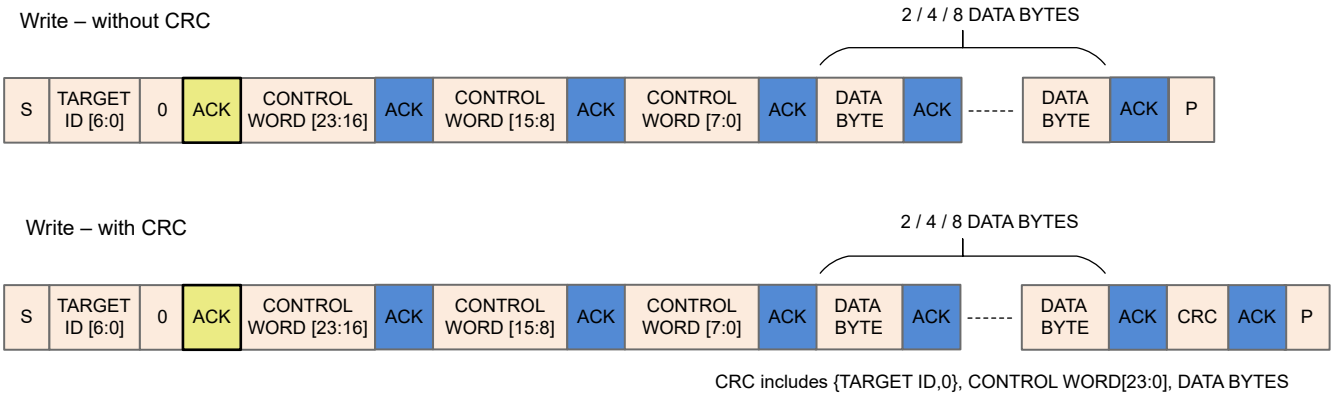


Figure 6-67. I²C Write Transaction Sequence

6.6.2.3 I²C Read Transaction

MCF8315D read transaction over I²C involves the following sequence (see Figure 6-68).

1. I²C Start condition from the controller to initiate the transaction.
2. Start is followed by the I²C target ID byte, made up of 7-bit target ID along with the R/W bit set to 0b. ACK (in yellow box) indicates that MCF8315D has processed the received target ID which has matched with it's I²C target ID and therefore will proceed with this transaction. If target ID received does not match with the I²C ID of MCF8315D, then the transaction is ignored and no ACK is sent by MCF8315D.

Copyright © 2025 Texas Instruments Incorporated

3. The target ID byte is followed by the 24-bit control word sent one byte at a time. Bit 23 in the control word is set to 1b as it is a read transaction. ACK (in blue boxes) correspond to acknowledgements sent by MCF8315D to the controller that the previous byte (of control word) has been received and next byte can be sent.
4. The control word is followed by a Repeated Start (RS, start without a preceding stop) or normal Start (P followed by S) to initiate the data (to be read back) transfer from MCF8315D to I^{2}C controller. RS or S is followed by the 7-bit target ID along with R/W bit set to 1b to initiate the read transaction. MCF8315D sends an ACK (in grey box after RS) to the controller to acknowledge the receipt of read transaction request.
5. Post acknowledgement of read transaction request, MCF8315D sends the data bytes on SDA one byte at a time. The number of data bytes sent by MCF8315D depends on the DLEN field in the control word.
   a. While sending data bytes, the LSB byte is sent first. Refer the examples in Section 6.6.2.4 for more details.
   b. 16-bit/32-bit Read – The data from the address mentioned in control word is sent back to the controller.
   c. 64-bit Read – 64-bit is treated as two successive 32-bit reads. The address mentioned in control word is taken as Addr_1. Addr_2 is internally calculated by MCF8315D by incrementing Addr_1 by 0x2. A total of 8 data bytes are sent by MCF8315D. The first 4 bytes (sent in LSB first) are read from Addr_1 and the next 4 bytes are read from Addr_2.
   d. ACK in orange boxes correspond to acknowledgements sent by the controller to MCF8315D that the previous byte has been received and next byte can be sent.
6. If CRC is enabled in the control word, then MCF8315D sends an additional CRC byte at the end. Controller has to read the CRC byte and then send the last ACK (in orange). CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).
7. I^{2}C Stop condition from the controller to terminate the transaction.

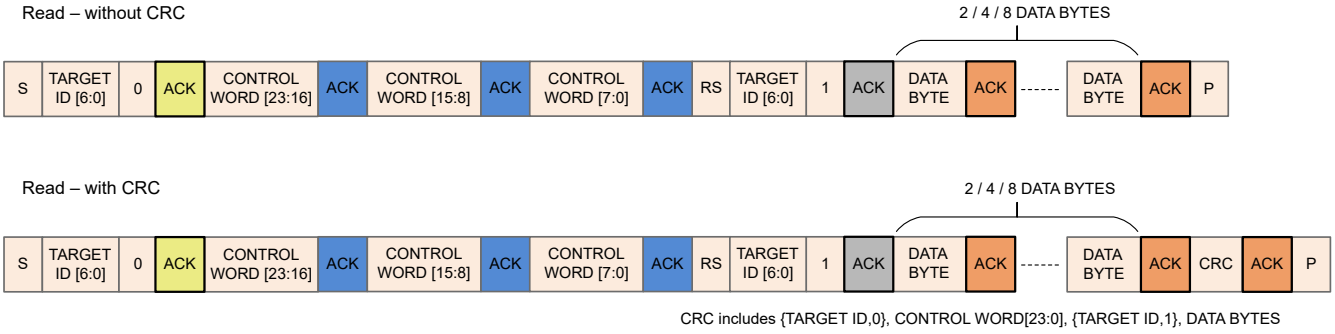


Figure 6-68. I^{2}C Read Transaction Sequence

6.6.2.4 I^{2}C Communication Protocol Packet Examples

All values used in this example section are in hex format. I^{2}C target ID used in the examples is 0x60.

Example for 32-bit Write Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 6-12. Example for 32-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes				CRC
Target ID	I^{2}C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x60	0x0	0x0	0x1	0x1	0x0	0x0	0x0	0x80	0xCD	0xAB	0x34	0x12	0x45
0xC0		0x50				0x00		0x80	0xCD	0xAB	0x34	0x12	0x45

Example for 64-bit Write Operation: Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 6-13. Example for 64-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes	CRC
Target ID	I²C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0 - DB7	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	[D7-D0] x 8	C7-C0
0x60	0x0	0x0	0x1	0x2	0x0	0x0	0x0	0x80	0x67452301EFCDAB89	0x45
0xC0		0x60				0x00		0x80	0x67452301EFCDAB89	0x45

Example for 32-bit Read Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

Table 6-14. Example for 32-bit Read Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Start Byte		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Target ID	I²C Write	R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	Target ID	I²C Read	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	A6-A0	W0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x60	0x0	0x1	0x1	0x1	0x0	0x0	0x0	0x80	0x60	0x1	0xCD	0xAB	0x34	0x12	0x56
0xC0		0xD0				0x00		0x80	0xC1		0xCD	0xAB	0x34	0x12	0x56

6.6.2.5 I²C Clock Stretching

The I²C peripheral in MCF8315D implements clock stretching under certain conditions when there are pending I²C interrupts waiting to be processed. During clock stretching, MCF8315D pulls SCL low and the I²C bus is unavailable for use by other devices. The following is a list of conditions under which clock stretching can occur:

1. **Start interrupt pending**: There are two scenarios when a start interrupt can result in clock stretching,
   a. When target ID is a match, I²C peripheral in MCF8315D raises a start interrupt request. Until this start interrupt request is processed, clock is stretched. Upon processing this request, clock is released and an ACK (marked in yellow or grey in Figure 6-67 and Figure 6-68) is sent to the controller for continuing with the transaction.
   b. If Start (followed by target ID match) for a new transaction is received when a receive interrupt from previous transaction is yet to be processed, clock is stretched until both the receive interrupt and start interrupt are processed in chronological order. This process ensures that previous transaction is executed correctly before initiating the next transaction.
2. **Receive interrupt pending**: When a receive interrupt is waiting to be processed and the receive register is full which occurs when two successive bytes (data or control) have been received by MCF8315D (separated by one ACK shown as blue boxes in Figure 6-67 and Figure 6-68) without the receive interrupt generated by the first byte being processed. Upon receive of second byte, clock is stretched until receive interrupt generated by the first byte is processed.
3. **Transmit buffer is empty**: In case of a transmit interrupt pending (to send data back to controller), if the transmit buffer is waiting to be populated with data to be read back to the controller, clock stretching is done until the transmit buffer is populated with requested data. After the buffer is populated, clock is released and data is sent to controller.

Note

I²C clock stretching is timed out after 5 ms by MCF8315D to allow I²C bus access for other devices on the same bus.

Copyright © 2025 Texas Instruments Incorporated

6.6.2.6 CRC Byte Calculation

An 8-bit CCIT polynomial ($x^8 + x^2 + x + 1$) and CRC initial value 0xFF is used for CRC computation.

CRC Calculation in Write Operation: When the external MCU writes to MCF8315D, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCF8315D will compute CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

CRC Calculation in Read Operation: When the external MCU reads from MCF8315D, if the CRC is enabled, MCF8315D sends the CRC byte at the end of the data. The CRC computation in read operation involves the start byte, control words sent by external MCU along with data bytes sent by MCF8315D. Input data for CRC calculation by external MCU to verify the data sent by MCF8315D are listed below :

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

Copyright © 2025 Texas Instruments Incorporated

7 EEPROM (Non-Volatile) Register Map

7.1 Algorithm_Configuration Registers

Table 7-1 lists the memory-mapped registers for the Algorithm_Configuration registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. ALGORITHM_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
80h	ISD_CONFIG	ISD Configuration	Section 7.1.1
82h	REV_DRIVE_CONFIG	Reverse Drive Configuration	Section 7.1.2
84h	MOTOR_STARTUP1	Motor Startup Configuration1	Section 7.1.3
86h	MOTOR_STARTUP2	Motor Startup Configuration2	Section 7.1.4
88h	CLOSED_LOOP1	Close Loop Configuration1	Section 7.1.5
8Ah	CLOSED_LOOP2	Close Loop Configuration2	Section 7.1.6
8Ch	CLOSED_LOOP3	Close Loop Configuration3	Section 7.1.7
8Eh	CLOSED_LOOP4	Close Loop Configuration4	Section 7.1.8
94h	REF_PROFILES1	Reference Profile Configuration1	Section 7.1.9
96h	REF_PROFILES2	Reference Profile Configuration2	Section 7.1.10
98h	REF_PROFILES3	Reference Profile Configuration3	Section 7.1.11
9Ah	REF_PROFILES4	Reference Profile Configuration4	Section 7.1.12
9Ch	REF_PROFILES5	Reference Profile Configuration5	Section 7.1.13
9Eh	REF_PROFILES6	Reference Profile Configuration6	Section 7.1.14

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2025 Texas Instruments Incorporated

7.1.1 ISD_CONFIG Register (Offset = 80h) [Reset = 00000000h]

ISD_CONFIG is shown in Figure 7-1 and described in Table 7-3.

Return to the Summary Table.

Register to configure initial speed detect settings

Figure 7-1. ISD_CONFIG Register

31	30	29	28	27	26	25	24
PARITY	ISD_EN	BRAKE_EN	HIZ_EN	RVS_DR_EN	RESYNC_EN	FW_DRV_RESYN_THR	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
FW_DRV_RESYN_THR		BRK_MODE	BRK_CONFIG	BRK_CURR_THR			BRK_TIME
R/W-0h		R/W-0h	R/W-0h	R/W-0h			R/W-0h
15	14	13	12	11	10	9	8
BRK_TIME			HIZ_TIME				STAT_DETECT_THR
R/W-0h			R/W-0h				R/W-0h
7	6	5	4	3	2	1	0
STAT_DETECT_THR		REV_DRV_HANDOFF_THR				REV_DRV_OPEN_LOOP_CURRENT	
R/W-0h		R/W-0h				R/W-0h	

Table 7-3. ISD_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	ISD_EN	R/W	0h	ISD enable 0h = Disable 1h = Enable
29	BRAKE_EN	R/W	0h	ISD brake enable 0h = Disable 1h = Enable
28	HIZ_EN	R/W	0h	ISD Hi-Z enable 0h = Disable 1h = Enable
27	RVS_DR_EN	R/W	0h	Reverse drive enable 0h = Disable 1h = Enable
26	RESYNC_EN	R/W	0h	Resynchronization enable 0h = Disable 1h = Enable

Copyright © 2025 Texas Instruments Incorporated

Table 7-3. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-22	FW_DRV_RESYN_THR	R/W	0h	Minimum speed threshold to resynchronize to close loop (% of MAX_SPEED) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 35% 7h = 40% 8h = 45% 9h = 50% Ah = Not Applicable Bh = Not Applicable Ch = Not Applicable Dh = Not Applicable Eh = Not Applicable Fh = Not Applicable
21	BRK_MODE	R/W	0h	Brake mode 0h = All three high side FETs turned ON 1h = All three low side FETs turned ON
20	BRK_CONFIG	R/W	0h	Brake configuration 0h = Brake time is used to come out of Brake state 1h = Brake current threshold and Brake time is used to come out of Brake state
19-17	BRK_CURR_THR	R/W	0h	Brake current threshold 0h = 0.062 A 1h = 0.125 A 2h = 0.187 A 3h = 0.312 A 4h = 0.625 A 5h = 1.25 A 6h = Not Applicable 7h = Not Applicable

Copyright © 2025 Texas Instruments Incorporated

Table 7-3. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-13	BRK_TIME	R/W	0h	Brake time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
12-9	HIZ_TIME	R/W	0h	Hi-Z time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
8-6	STAT_DETECT_THR	R/W	0h	BEMF threshold to detect if motor is stationary 0h = 50 mV 1h = 75 mV 2h = 100 mV 3h = 250 mV 4h = 500 mV 5h = 750 mV 6h = 1000 mV 7h = 1500 mV

Copyright © 2025 Texas Instruments Incorporated

Table 7-3. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-2	REV_DRV_HANDOFF_THR	R/W	0h	Speed threshold used to transition to open loop during reverse drive (% of MAX_SPEED) 0h = 2.5% 1h = 5% 2h = 7.5% 3h = 10% 4h = 12.5% 5h = 15% 6h = 20% 7h = 25% 8h = 30% 9h = 40% Ah = 50% Bh = Not Applicable Ch = Not Applicable Dh = Not Applicable Eh = Not Applicable Fh = Not Applicable
1-0	REV_DRV_OPEN_LOOP_CURRENT	R/W	0h	Open loop current limit during reverse drive 0h = 0.937 A 1h = 1.562 A 2h = 2.187 A 3h = 3.125 A

Copyright © 2025 Texas Instruments Incorporated

7.1.2 REV_DRIVE_CONFIG Register (Offset = 82h) [Reset = 00000000h]

REV_DRIVE_CONFIG is shown in Figure 7-2 and described in Table 7-4.

Return to the Summary Table.

Register to configure reverse drive settings

Figure 7-2. REV_DRIVE_CONFIG Register

31	30	29	28	27	26	25	24
PARITY	REV_DRV_OPEN_LOOP_ACCEL_A1				REV_DRV_OPEN_LOOP_ACCEL_A2		
R/W-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
REV_DRV_OPEN_LOOP_ACCEL_A2	ACTIVE_BRAKE_CURRENT_LIMIT			ACTIVE_BRAKE_KP			
R/W-0h	R/W-0h			R/W-0h			
15	14	13	12	11	10	9	8
ACTIVE_BRAKE_KP						ACTIVE_BRAKE_KI	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
ACTIVE_BRAKE_KI							
R/W-0h							

Table 7-4. REV_DRIVE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	REV_DRV_OPEN_LOOP_ACCEL_A1	R/W	0h	Open loop acceleration coefficient A1 during reverse drive 0h = 0.1 Hz/s 1h = 0.5 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s

Copyright © 2025 Texas Instruments Incorporated

Table 7-4. REV_DRIVE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	REV_DRV_OPEN_LOOP_ACCEL_A2	R/W	0h	Open loop acceleration coefficient A2 during reverse drive 0h = 0.0 Hz/s2 1h = 0.5 Hz/s2 2h = 1 Hz/s2 3h = 2.5 Hz/s2 4h = 5 Hz/s2 5h = 10 Hz/s2 6h = 25 Hz/s2 7h = 50 Hz/s2 8h = 75 Hz/s2 9h = 100 Hz/s2 Ah = 250 Hz/s2 Bh = 500 Hz/s2 Ch = 750 Hz/s2 Dh = 1000 Hz/s2 Eh = 5000 Hz/s2 Fh = 10000 Hz/s2
22-20	ACTIVE_BRAKE_CURRENT_LIMIT	R/W	0h	Bus current limit during active braking 0h = 0.312 A 1h = 0.625 A 2h = 1.25 A 3h = 1.875 A 4h = 2.5 A 5h = 3.125 A 6h = 3.75 A 7h = Not Applicable
19-10	ACTIVE_BRAKE_KP	R/W	0h	10-bit value for active braking loop Kp. Kp = ACTIVE_BRAKE_KP / 2^7
9-0	ACTIVE_BRAKE_KI	R/W	0h	10-bit value for active braking loop Ki. Ki = ACTIVE_BRAKE_KI / 2^9

Copyright © 2025 Texas Instruments Incorporated

7.1.3 MOTOR_STARTUP1 Register (Offset = 84h) [Reset = 00000000h]

MOTOR_STARTUP1 is shown in Figure 7-3 and described in Table 7-5.

Return to the Summary Table.

Register to configure motor startup settings1

Figure 7-3. MOTOR_STARTUP1 Register

31	30	29	28	27	26	25	24
PARITY	MTR_STARTUP		ALIGN_SLOW_RAMP_RATE				ALIGN_TIME
R/W-0h	R/W-0h		R/W-0h				R/W-0h
23	22	21	20	19	18	17	16
ALIGN_TIME			ALIGN_OR_SLOW_CURRENT_ILIMIT				IPD_CLK_FREQ
R/W-0h			R/W-0h				R/W-0h
15	14	13	12	11	10	9	8
IPD_CLK_FREQ		IPD_CURR_THR					IPD_RLS_MODE
R/W-0h		R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
IPD_ADV_ANGLE		IPD_REPEAT		RESERVED	IQ_RAMP_EN	ACTIVE_BRAKE_EN	REV_DRV_CONFIG
R/W-0h		R/W-0h		R-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-5. MOTOR_STARTUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	MTR_STARTUP	R/W	0h	Motor start-up method 0h = Align 1h = Double Align 2h = IPD 3h = Slow first cycle
28-25	ALIGN_SLOW_RAMP_RATE	R/W	0h	Align, slow first cycle and open loop current ramp rate 0h = 0.1 A/s 1h = 1 A/s 2h = 5 A/s 3h = 10 A/s 4h = 15 A/s 5h = 25 A/s 6h = 50 A/s 7h = 100 A/s 8h = 150 A/s 9h = 200 A/s Ah = 250 A/s Bh = 500 A/s Ch = 1000 A/s Dh = 2000 A/s Eh = 5000 A/s Fh = No Limit A/s

Copyright © 2025 Texas Instruments Incorporated

Table 7-5. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-21	ALIGN_TIME	R/W	0h	Align time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 1.5 s Ah = 2 s Bh = 3 s Ch = 4 s Dh = 5 s Eh = 7.5 s Fh = 10 s
20-17	ALIGN_OR_SLOW_CURRENT_ILIMIT	R/W	0h	Align or slow first cycle current limit 0h = 0.078 A 1h = 0.156 A 2h = 0.312 A 3h = 0.625 A 4h = 0.937 A 5h = 1.25 A 6h = 1.562 A 7h = 1.875 A 8h = 2.187 A 9h = 2.5 A Ah = 2.812 A Bh = 3.125 A Ch = 3.437 A Dh = 3.75 A Eh = Not Applicable Fh = Not Applicable
16-14	IPD_CLK_FREQ	R/W	0h	IPD clock frequency 0h = 50 Hz 1h = 100 Hz 2h = 250 Hz 3h = 500 Hz 4h = 1000 Hz 5h = 2000 Hz 6h = 5000 Hz 7h = 10000 Hz

Copyright © 2025 Texas Instruments Incorporated

Table 7-5. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-9	IPD_CURR_THR	R/W	0h	IPD current threshold 0h = 0.156 A 1h = 0.312 A 2h = 0.468 A 3h = 0.625 A 4h = 0.781 A 5h = 0.937 A 6h = 1.25 A 7h = 1.562 A 8h = 1.875 A 9h = 2.291 A Ah = 2.5 A Bh = 2.916 A Ch = 3.125 A Dh = 3.333 A Eh = 3.75 A Fh = Not Applicable 10h = Not Applicable 11h = Not Applicable 12h = Not Applicable 13h = Not Applicable 14h = Not Applicable 15h = Not Applicable 16h = Not Applicable 17h = Not Applicable 18h = Not Applicable 19h = Not Applicable 1Ah = Not Applicable 1Bh = Not Applicable 1Ch = Not Applicable 1Dh = Not Applicable 1Eh = Not Applicable 1Fh = Not Applicable
8	IPD_RLS_MODE	R/W	0h	IPD release mode 0h = Brake 1h = Tristate
7-6	IPD_ADV_ANGLE	R/W	0h	IPD advance angle 0h = 0° 1h = 30° 2h = 60° 3h = 90°

Copyright © 2025 Texas Instruments Incorporated

Table 7-5. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	IPD_REPEAT	R/W	0h	Number of times IPD is executed 0h = 1 time 1h = 2 times 2h = 3 times 3h = 4 times
3	RESERVED	R	0h	Reserved
2	IQ_RAMP_EN	R/W	0h	Iq reference ramp down during transition from open loop to closed loop 0h = Disable Iq ramp down 1h = Enable Iq ramp down
1	ACTIVE_BRAKE_EN	R/W	0h	Enable active braking 0h = Disable Active Brake 1h = Enable Active Brake
0	REV_DRV_CONFIG	R/W	0h	Choose between forward and reverse drive setting for reverse drive 0h = Open loop current, A1, A2 based on forward drive 1h = Open loop current, A1, A2 based on reverse drive

Copyright © 2025 Texas Instruments Incorporated

7.1.4 MOTOR_STARTUP2 Register (Offset = 86h) [Reset = 00000000h]

MOTOR_STARTUP2 is shown in Figure 7-4 and described in Table 7-6.

Return to the Summary Table.

Register to configure motor startup settings2

Figure 7-4. MOTOR_STARTUP2 Register

31	30	29	28	27	26	25	24
PARITY	OL_ILIMIT				OL_ACC_A1		
R/W-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
OL_ACC_A1	OL_ACC_A2				AUTO_HANDOFF_EN	OPN_CL_HANDOFF_THR	
R/W-0h	R/W-0h				R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
OPN_CL_HANDOFF_THR				ALIGN_ANGLE			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
SLOW_FIRST_CYC_FREQ				FIRST_CYCLE_FREQ_SEL	THETA_ERROR_RAMP_RATE		
R/W-0h				R/W-0h	R/W-0h		

Table 7-6. MOTOR_STARTUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	OL_ILIMIT	R/W	0h	Open loop current limit 0h = 0.078 A 1h = 0.156 A 2h = 0.312 A 3h = 0.625 A 4h = 0.937 A 5h = 1.25 A 6h = 1.562 A 7h = 1.875 A 8h = 2.187 A 9h = 2.5 A Ah = 2.812 A Bh = 3.125 A Ch = 3.437 A Dh = 3.75 A Eh = Not Applicable Fh = Not Applicable

Copyright © 2025 Texas Instruments Incorporated

Table 7-6. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	OL_ACC_A1	R/W	0h	Open loop acceleration coefficient A1 0h = 0.1 Hz/s 1h = 0.5 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s
22-19	OL_ACC_A2	R/W	0h	Open loop acceleration coefficient A2 0h = 0.0 Hz/s2 1h = 0.5 Hz/s2 2h = 1 Hz/s2 3h = 2.5 Hz/s2 4h = 5 Hz/s2 5h = 10 Hz/s2 6h = 25 Hz/s2 7h = 50 Hz/s2 8h = 75 Hz/s2 9h = 100 Hz/s2 Ah = 250 Hz/s2 Bh = 500 Hz/s2 Ch = 750 Hz/s2 Dh = 1000 Hz/s2 Eh = 5000 Hz/s2 Fh = 10000 Hz/s2
18	AUTO_HANDOFF_EN	R/W	0h	Auto handoff enable 0h = Disable Auto Handoff (and use OPN_CL_HANDOFF_THR) 1h = Enable Auto Handoff

Copyright © 2025 Texas Instruments Incorporated

Table 7-6. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-13	OPN_CL_HANDOFF_THR	R/W	0h	Open to closed loop handoff threshold (% of MAX_SPEED) 0h = 1% 1h = 2% 2h = 3% 3h = 4% 4h = 5% 5h = 6% 6h = 7% 7h = 8% 8h = 9% 9h = 10% Ah = 11% Bh = 12% Ch = 13% Dh = 14% Eh = 15% Fh = 16% 10h = 17% 11h = 18% 12h = 19% 13h = 20% 14h = 22.5% 15h = 25% 16h = 27.5% 17h = 30% 18h = 32.5% 19h = 35% 1Ah = 37.5% 1Bh = 40% 1Ch = 42.5% 1Dh = 45% 1Eh = 47.5% 1Fh = 50%

Copyright © 2025 Texas Instruments Incorporated

Table 7-6. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	ALIGN_ANGLE	R/W	0h	Align angle 0h = 0° 1h = 10° 2h = 20° 3h = 30° 4h = 45° 5h = 60° 6h = 70° 7h = 80° 8h = 90° 9h = 110° Ah = 120° Bh = 135° Ch = 150° Dh = 160° Eh = 170° Fh = 180° 10h = 190° 11h = 210° 12h = 225° 13h = 240° 14h = 250° 15h = 260° 16h = 270° 17h = 280° 18h = 290° 19h = 315° 1Ah = 330° 1Bh = 340° 1Ch = 350° 1Dh = Not Applicable 1Eh = Not Applicable 1Fh = Not Applicable

Copyright © 2025 Texas Instruments Incorporated

Table 7-6. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	SLOW_FIRST_CYC_FREQ	R/W	0h	Frequency of first cycle in open loop start-up (% of MAX_SPEED) 0h = 0.1% 1h = 0.3% 2h = 0.5% 3h = 0.7% 4h = 1.0% 5h = 1.5% 6h = 2.0% 7h = 2.5% 8h = 3.0% 9h = 4.0% Ah = 5.0% Bh = 7.5% Ch = 10.0% Dh = 15% Eh = 20% Fh = 25%
3	FIRST_CYCLE_FREQ_SEL	R/W	0h	First cycle frequency in open loop for align, double align and IPD start-up 0h = 0 Hz 1h = Defined by SLOW_FIRST_CYC_FREQ
2-0	THETA_ERROR_RAMP_RATE	R/W	0h	Ramp rate for reducing difference between estimated theta and open loop theta 0h = 0.01 deg/ms 1h = 0.05 deg/ms 2h = 0.1 deg/ms 3h = 0.15 deg/ms 4h = 0.2 deg/ms 5h = 0.5 deg/ms 6h = 1 deg/ms 7h = 2 deg/ms

Copyright © 2025 Texas Instruments Incorporated

7.1.5 CLOSED_LOOP1 Register (Offset = 88h) [Reset = 00000000h]

CLOSED_LOOP1 is shown in Figure 7-5 and described in Table 7-7.

Return to the Summary Table.

Register to configure close loop settings1

Figure 7-5. CLOSED_LOOP1 Register

31	30	29	28	27	26	25	24
PARITY	OVERMODULATION_ENABLE	CL_ACC					RESERVED
R/W-0h	R/W-0h	R/W-0h					R-0h
23	22	21	20	19	18	17	16
CL_DEC					PWM_FREQ_OUT		
R/W-0h					R/W-0h		
15	14	13	12	11	10	9	8
PWM_FREQ_OUT	PWM_MODE	FG_SEL		FG_DIV			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
FG_CONFIG	FG_BEMF_THR			AVS_EN	DEADTIME_COMP_EN	RESERVED	LOW_SPEED_RECIRC_BRAKE_EN
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R-0h	R/W-0h

Table 7-7. CLOSED_LOOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	OVERMODULATION_ENABLE	R/W	0h	Enable overmodulation 0h = Disable overmodulation 1h = Enable overmodulation

Copyright © 2025 Texas Instruments Incorporated

Table 7-7. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29-25	CL_ACC	R/W	0h	Closed loop acceleration (Speed mode: Hz/s Power mode: deciWatts/s Torque mode: centiA/s duty cycle mode: milliUnit/s) deciWatt: 0.1W centiA: 0.01A milliUnit: 0.001% 0h = 0.5 1h = 1 2h = 2.5 3h = 5 4h = 7.5 5h = 10 6h = 20 7h = 40 8h = 60 9h = 80 Ah = 100 Bh = 200 Ch = 300 Dh = 400 Eh = 500 Fh = 600 10h = 700 11h = 800 12h = 900 13h = 1000 14h = 2000 15h = 4000 16h = 6000 17h = 8000 18h = 10000 19h = 20000 1Ah = 30000 1Bh = 40000 1Ch = 50000 1Dh = 60000 1Eh = 70000 1Fh = No limit
24	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

Table 7-7. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-19	CL_DEC	R/W	0h	Closed loop deceleration (Speed mode: Hz/s Power mode: deciWatts/s Torque mode: centiA/s duty cycle mode: milliUnit/s) If AVS is enabled in speed or power mode, the current is clamped to 0 only if negative iqRef is set by outer PI (speed/power) loop deciWatt: 0.1W centiA: 0.01A milliUnit: 0.001% 0h = 0.5 1h = 1 2h = 2.5 3h = 5 4h = 7.5 5h = 10 6h = 20 7h = 40 8h = 60 9h = 80 Ah = 100 Bh = 200 Ch = 300 Dh = 400 Eh = 500 Fh = 600 10h = 700 11h = 800 12h = 900 13h = 1000 14h = 2000 15h = 4000 16h = 6000 17h = 8000 18h = 10000 19h = 20000 1Ah = 30000 1Bh = 40000 1Ch = 50000 1Dh = 60000 1Eh = 70000 1Fh = No limit

Copyright © 2025 Texas Instruments Incorporated

Table 7-7. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	PWM_FREQ_OUT	R/W	0h	PWM output frequency 0h = 10 kHz 1h = 15 kHz 2h = 20 kHz 3h = 25 kHz 4h = 30 kHz 5h = 35 kHz 6h = 40 kHz 7h = 45 kHz 8h = 50 kHz 9h = 55 kHz Ah = 60 kHz Bh = Not Applicable Ch = Not Applicable Dh = Not Applicable Eh = Not Applicable Fh = Not Applicable
14	PWM_MODE	R/W	0h	PWM modulation 0h = Continuous Space Vector Modulation 1h = Discontinuous Space Vector Modulation
13-12	FG_SEL	R/W	0h	FG select 0h = Output FG in ISD, open loop and closed loop 1h = Output FG in only closed loop 2h = Output FG in open loop for the first try. 3h = Not Applicable
11-8	FG_DIV	R/W	0h	FG division factor 0h = 3x electrical speed 1h = Divide by 1 (2-pole motor mechanical speed) 2h = Divide by 2 (4-pole motor mechanical speed) 3h = Divide by 3 (6-pole motor mechanical speed) 4h = Divide by 4 (8-pole motor mechanical speed) ... Fh = Divide by 15 (30-pole motor mechanical speed)
7	FG_CONFIG	R/W	0h	FG output configuration. BEMF threshold defined by FG_BEMF_THR 0h = FG active as long as motor is driven 1h = FG active till BEMF drops below BEMF threshold

Copyright © 2025 Texas Instruments Incorporated

Table 7-7. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	FG_BEMF_THR	R/W	0h	FG output BEMF threshold 0h = +/- 1mV 1h = +/- 2mV 2h = +/- 5mV 3h = +/- 10mV 4h = +/- 20mV 5h = +/- 30mV 6h = Not Applicable 7h = Not Applicable
3	AVS_EN	R/W	0h	AVS enable 0h = Disable 1h = Enable
2	DEADTIME_COMP_EN	R/W	0h	Deadtime compensation enable 0h = Disable 1h = Enable
1	RESERVED	R	0h	Reserved
0	LOW_SPEED_RECIRC_BRAKE_EN	R/W	0h	Stop mode applied when stop mode is recirculation brake and motor in align or open loop state 0h = Hi-z 1h = Low Side Brake

Copyright © 2025 Texas Instruments Incorporated

7.1.6 CLOSED_LOOP2 Register (Offset = 8Ah) [Reset = 00000000h]

CLOSED_LOOP2 is shown in Figure 7-6 and described in Table 7-8.

Return to the Summary Table.

Register to configure close loop settings2

Figure 7-6. CLOSED_LOOP2 Register

31	30	29	28	27	26	25	24
PARITY	MTR_STOP			MTR_STOP_BRK_TIME			
R/W-0h	R/W-0h			R/W-0h			
23	22	21	20	19	18	17	16
ACT_SPIN_THR				BRAKE_SPEED_THRESHOLD			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
MOTOR_RES							
R/W-0h							
7	6	5	4	3	2	1	0
MOTOR_IND							
R/W-0h							

Table 7-8. CLOSED_LOOP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	MTR_STOP	R/W	0h	Motor stop mode 0h = Hi-z 1h = Recirculation Stop 2h = Low side braking 3h = High side braking 4h = Active spin down 5h = Not Applicable 6h = Not Applicable 7h = Not Applicable

Copyright © 2025 Texas Instruments Incorporated

Table 7-8. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-24	MTR_STOP_BRK_TIME	R/W	0h	Brake time during motor stop 0h = 1 ms 1h = 1 ms 2h = 1 ms 3h = 1 ms 4h = 1 ms 5h = 5 ms 6h = 10 ms 7h = 50 ms 8h = 100 ms 9h = 250 ms Ah = 500 ms Bh = 1000 ms Ch = 2500 ms Dh = 5000 ms Eh = 10000 ms Fh = 15000 ms
23-20	ACT_SPIN_THR	R/W	0h	Speed threshold for active spin down (% of MAX_SPEED) 0h = 100 % 1h = 90 % 2h = 80 % 3h = 70 % 4h = 60% 5h = 50 % 6h = 45 % 7h = 40 % 8h = 35 % 9h = 30 % Ah = 25 % Bh = 20 % Ch = 15 % Dh = 10 % Eh = 5 % Fh = 2.5 %

Copyright © 2025 Texas Instruments Incorporated

Table 7-8. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	BRAKE_SPEED_THRESHOLD	R/W	0h	Speed threshold for BRAKE pin and Motor stop (Low side Braking or High Side Braking or Align Braking) (% of MAX_SPEED) 0h = 100 % 1h = 90 % 2h = 80 % 3h = 70 % 4h = 60% 5h = 50 % 6h = 45 % 7h = 40 % 8h = 35 % 9h = 30 % Ah = 25 % Bh = 20 % Ch = 15 % Dh = 10 % Eh = 5 % Fh = 2.5 %
15-8	MOTOR_RES	R/W	0h	8-bit values for motor phase resistance. See Table 6-2 for values of phase resistance
7-0	MOTOR_IND	R/W	0h	8-bit values for motor phase inductance. See Table 6-3 for values of phase inductance

Copyright © 2025 Texas Instruments Incorporated

7.1.7 CLOSED_LOOP3 Register (Offset = 8Ch) [Reset = 00000000h]

CLOSED_LOOP3 is shown in Figure 7-7 and described in Table 7-9.

Return to the Summary Table.

Register to configure close loop settings3

Figure 7-7. CLOSED_LOOP3 Register

31	30	29	28	27	26	25	24
PARITY	MOTOR_BEMF_CONST						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
MOTOR_BEMF_CONST	CURR_LOOP_KP						
R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
CURR_LOOP_KP				CURR_LOOP_KI			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
CURR_LOOP_KI						SPD_LOOP_KP	
R/W-0h						R/W-0h	

Table 7-9. CLOSED_LOOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	MOTOR_BEMF_CONST	R/W	0h	8-bit values for motor BEMF Constant. See Table 6-4 for values of BEMF constant
22-13	CURR_LOOP_KP	R/W	0h	10-bit value for current Iq and Id loop Kp. Kp = 8LSB of CURR_LOOP_KP / 10^2MSB of CURR_LOOP_KP. Set to 0 for auto calculation of current Kp and Ki
12-3	CURR_LOOP_KI	R/W	0h	10-bit value for current Iq and Id loop Ki. Ki = 1000 * 8LSB of CURR_LOOP_KI / 10^2MSB of CURR_LOOP_KI. Set to 0 for auto calculation of current Kp and Ki
2-0	SPD_LOOP_KP	R/W	0h	3 MSB bits for speed loop Kp. Kp = 0.01 * 8LSB of SPD_LOOP_KP / 10^2MSB of SPD_LOOP_KP

Copyright © 2025 Texas Instruments Incorporated

7.1.8 CLOSED_LOOP4 Register (Offset = 8Eh) [Reset = 00000000h]

CLOSED_LOOP4 is shown in Figure 7-8 and described in Table 7-10.

Return to the Summary Table.

Register to configure close loop settings4

Figure 7-8. CLOSED_LOOP4 Register

31	30	29	28	27	26	25	24
PARITY	SPD_LOOP_KP						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
SPD_LOOP_KI							
R/W-0h							
15	14	13	12	11	10	9	8
SPD_LOOP_KI	MAX_SPEED						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
MAX_SPEED							
R/W-0h							

Table 7-10. CLOSED_LOOP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-24	SPD_LOOP_KP	R/W	0h	7 LSB bits for speed loop Kp. Kp = 0.01 * 8LSB of SPD_LOOP_KP / 10^2MSB of SPD_LOOP_KP
23-14	SPD_LOOP_KI	R/W	0h	10 bit value for speed loop Ki. Ki = 0.1 * 8LSB of SPD_LOOP_KI / 10^2MSB of SPD_LOOP_KI
13-0	MAX_SPEED	R/W	0h	14-bit value for setting maximum motor speed in electrical Hz. Maximum motor electrical speed (Hz): {MAX_SPEED/6} For example: if MAX_SPEED is 0x2710, then maximum motor speed (Hz) = 10000(0x2710)/6 = 1666 Hz

Copyright © 2025 Texas Instruments Incorporated

7.1.9 REF_PROFILES1 Register (Offset = 94h) [Reset = 00000000h]

REF_PROFILES1 is shown in Figure 7-9 and described in Table 7-11.

Return to the Summary Table.

Register to configure Reference profile1

Figure 7-9. REF_PROFILES1 Register

31	30	29	28	27	26	25	24
PARITY	REF_PROFILE_CONFIG		DUTY_ON1				
R/W-0h	R/W-0h		R/W-0h				
23	22	21	20	19	18	17	16
DUTY_ON1			DUTY_OFF1				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
DUTY_OFF1			DUTY_CLAMP1				
R/W-0h			R/W-0h				
7	6	5	4	3	2	1	0
DUTY_CLAMP1			DUTY_A				
R/W-0h			R/W-0h				

Table 7-11. REF_PROFILES1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	REF_PROFILE_CONFIG	R/W	0h	Configuration for reference profiles 0h = Reference/Equation 1h = Linear Profile 2h = Staircase Profile 3h = Forward-Reverse Profile
28-21	DUTY_ON1	R/W	0h	Turn-on duty cycle (%) = {(DUTY_ON1/256)*100}
20-13	DUTY_OFF1	R/W	0h	Turn-off duty cycle (%) = {(DUTY_OFF1/256)*100}
12-5	DUTY_CLAMP1	R/W	0h	Duty cycle for clamping speed (%) = {(DUTY_CLAMP1/256)*100}
4-0	DUTY_A	R/W	0h	5 MSB bits for duty cycle A

Copyright © 2025 Texas Instruments Incorporated

7.1.10 REF_PROFILES2 Register (Offset = 96h) [Reset = 00000000h]

REF_PROFILES2 is shown in Figure 7-10 and described in Table 7-12.

Return to the Summary Table.

Register to configure Reference profile2

Figure 7-10. REF_PROFILES2 Register

31	30	29	28	27	26	25	24
PARITY	DUTY_A			DUTY_B			
R/W-0h	R/W-0h			R/W-0h			
23	22	21	20	19	18	17	16
DUTY_B				DUTY_C			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
DUTY_C				DUTY_D			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
DUTY_D				DUTY_E			
R/W-0h				R/W-0h			

Table 7-12. REF_PROFILES2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	DUTY_A	R/W	0h	3 LSB bits for duty cycle A Duty cycle A (%) = {(DUTY_A/256)*100}
27-20	DUTY_B	R/W	0h	Duty cycle B (%) = {(DUTY_B/256)*100}
19-12	DUTY_C	R/W	0h	Duty cycle C (%) = {(DUTY_C/256)*100}
11-4	DUTY_D	R/W	0h	Duty cycle D (%) = {(DUTY_D/256)*100}
3-0	DUTY_E	R/W	0h	4 MSB bits for Duty cycle E

Copyright © 2025 Texas Instruments Incorporated

7.1.11 REF_PROFILES3 Register (Offset = 98h) [Reset = 00000000h]

REF_PROFILES3 is shown in Figure 7-11 and described in Table 7-13.

Return to the Summary Table.

Register to configure Reference profile3

Figure 7-11. REF_PROFILES3 Register

31	30	29	28	27	26	25	24
PARITY	DUTY_E				DUTY_ON2		
R/W-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
DUTY_ON2					DUTY_OFF2		
R/W-0h					R/W-0h		
15	14	13	12	11	10	9	8
DUTY_OFF2					DUTY_CLAMP2		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
DUTY_CLAMP2					DUTY_HYS		RESERVED
R/W-0h					R/W-0h		R-0h

Table 7-13. REF_PROFILES3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	DUTY_E	R/W	0h	4 LSB bits for Duty cycle E Duty cycle E (%) = {(DUTY_E/256)*100}
26-19	DUTY_ON2	R/W	0h	Turn-on duty cycle (%) = {(DUTY_ON2/256)*100}
18-11	DUTY_OFF2	R/W	0h	Turn-off duty cycle (%) = {(DUTY_OFF2/256)*100}
10-3	DUTY_CLAMP2	R/W	0h	Duty cycle for clamping speed (%) = {(DUTY_CLAMP1/256)*100}
2-1	DUTY_HYS	R/W	0h	Duty hysteresis for speed reference mode 0h = 0% 1h = 1% 2h = 2% 3h = 3%
0	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

7.1.12 REF_PROFILES4 Register (Offset = 9Ah) [Reset = 00000000h]

REF_PROFILES4 is shown in Figure 7-12 and described in Table 7-14.

Return to the Summary Table.

Register to configure Reference profile4

Figure 7-12. REF_PROFILES4 Register

31	30	29	28	27	26	25	24
PARITY	REF_OFF1						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
REF_OFF1	REF_CLAMP1						
R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
REF_CLAMP1	REF_A						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
REF_A	REF_B						
R/W-0h	R/W-0h						

Table 7-14. REF_PROFILES4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	REF_OFF1	R/W	0h	Turn off reference (% of Maximum Reference) = {(REF_OFF1/256)*100}
22-15	REF_CLAMP1	R/W	0h	Clamp Ref 1 (% of Maximum Reference) = {(REF_CLAMP1/256)*100}
14-7	REF_A	R/W	0h	Ref A (% of Maximum Reference) = {(REF_A/256)*100}
6-0	REF_B	R/W	0h	7 MSB of REF_B configuration

Copyright © 2025 Texas Instruments Incorporated

7.1.13 REF_PROFILES5 Register (Offset = 9Ch) [Reset = 00000000h]

REF_PROFILES5 is shown in Figure 7-13 and described in Table 7-15.

Return to the Summary Table.

Register to configure Reference profile5

Figure 7-13. REF_PROFILES5 Register

31	30	29	28	27	26	25	24
PARITY	REF_B	REF_C					
R/W-0h	R/W-0h	R/W-0h					
23	22	21	20	19	18	17	16
REF_C		REF_D					
R/W-0h		R/W-0h					
15	14	13	12	11	10	9	8
REF_D		REF_E					
R/W-0h		R/W-0h					
7	6	5	4	3	2	1	0
REF_E		MIN_DUTY		VOLTAGE_MODE_CONFIG		DUTY_COMMAND_FILTER	RESERVED
R/W-0h		R/W-0h		R/W-0h		R/W-0h	R-0h

Table 7-15. REF_PROFILES5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	REF_B	R/W	0h	1 LSB of REF_B configuration. Ref B(% of Maximum Reference) = {(REF_B/256)*100}
29-22	REF_C	R/W	0h	Ref C (% of Maximum Reference) = {(REF_C/256)*100}
21-14	REF_D	R/W	0h	Ref D (% of Maximum Reference) = {(REF_D/256)*100}
13-6	REF_E	R/W	0h	Ref E(% of Maximum Reference) = {(REF_E/256)*100}
5-4	MIN_DUTY	R/W	0h	Minimum input duty to start driving the motor 0h = 1 % 1h = 3 % 2h = 5 % 3h = 10 %
3-2	VOLTAGE_MODE_CONFIG	R/W	0h	Voltage mode configuration for reference profiles 0h = User defined reference modes throughout the duty range 1h = Voltage mode if input duty > DUTY_C + DUTY_HYST; configured reference mode if input duty < DUTY_C - DUTY_HYST 2h = configured reference mode if input duty > DUTY_C + DUTY_HYST; voltage mode if input duty < DUTY_C - DUTY_HYST 3h = Not Applicable
1	DUTY_COMMAND_FILTER	R/W	0h	Speed pin input filter 0h = Filter on Speed pin is disabled 1h = Filter on Speed pin is enabled (0.4%)
0	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

7.1.14 REF_PROFILES6 Register (Offset = 9Eh) [Reset = 00000000h]

REF_PROFILES6 is shown in Figure 7-14 and described in Table 7-16.

Return to the Summary Table.

Register to configure Reference profile6

Figure 7-14. REF_PROFILES6 Register

31	30	29	28	27	26	25	24
PARITY	REF_OFF2						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
REF_OFF2	REF_CLAMP2						
R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
REF_CLAMP2	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-16. REF_PROFILES6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	REF_OFF2	R/W	0h	Turn off Ref (% of Maximum Reference)) = {(REF_OFF2/256)*100}
22-15	REF_CLAMP2	R/W	0h	Clamp Ref 2 (% of Maximum Reference) = {(REF_CLAMP2/256)*100}
14-0	RESERVED	R	0h	Reserved

7.2 Fault_Configuration Registers

Table 7-17 lists the memory-mapped registers for the Fault_Configuration registers. All register offset addresses not listed in Table 7-17 should be considered as reserved locations and the register contents should not be modified.

Table 7-17. FAULT_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
90h	FAULT_CONFIG1	Fault Configuration1	Section 7.2.1
92h	FAULT_CONFIG2	Fault Configuration2	Section 7.2.2

Complex bit access types are encoded to fit into small table cells. Table 7-18 shows the codes that are used for access types in this section.

Table 7-18. Fault_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		

Copyright © 2025 Texas Instruments Incorporated

Table 7-18. Fault_Configuration Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

Copyright © 2025 Texas Instruments Incorporated

7.2.1 FAULT_CONFIG1 Register (Offset = 90h) [Reset = 00000000h]

FAULT_CONFIG1 is shown in Figure 7-15 and described in Table 7-19.

Return to the Summary Table.

Register to configure fault settings1

Figure 7-15. FAULT_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	ILIMIT				HW_LOCK_ILIMIT		
R/W-0h	R/W-0h				R/W-0h		
23	22	21	20	19	18	17	16
HW_LOCK_ILIMIT	LOCK_ILIMIT				EEP_FAULT_MODE	LOCK_ILIMIT_MODE	
R/W-0h	R/W-0h				R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
LOCK_ILIMIT_MODE	LOCK_ILIMIT_DEG				LCK_RETRY		
R/W-0h	R/W-0h				R/W-0h		
7	6	5	4	3	2	1	0
LCK_RETRY	CRC_ERR_MODE	MTR_LCK_MODE			IPD_TIMEOUT_FAULT_EN	IPD_FREQ_FAULT_EN	SATURATION_FLAGS_EN
R/W-0h	R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h

Table 7-19. FAULT_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	ILIMIT	R/W	0h	Current limit for Iq axis (torque) current reference in closed loop 0h = 0.078 A 1h = 0.156 A 2h = 0.312 A 3h = 0.625 A 4h = 0.937 A 5h = 1.250 A 6h = 1.562 A 7h = 1.875 A 8h = 2.187 A 9h = 2.5 A Ah = 2.812 A Bh = 3.125 A Ch = 3.437 A Dh = 3.75 A Eh = Not Applicable Fh = Not Applicable

Copyright © 2025 Texas Instruments Incorporated

Table 7-19. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-23	HW_LOCK_ILIMIT	R/W	0h	Comparator based lock detection current threshold 0h = 0.078 A 1h = 0.156 A 2h = 0.312 A 3h = 0.625 A 4h = 0.937 A 5h = 1.250 A 6h = 1.562 A 7h = 1.875 A 8h = 2.187 A 9h = 2.5 A Ah = 2.812 A Bh = 3.125 A Ch = 3.437 A Dh = 3.75 A Eh = Not Applicable Fh = Not Applicable
22-19	LOCK_ILIMIT	R/W	0h	ADC based lock detection current threshold 0h = 0.078 A 1h = 0.156 A 2h = 0.312 A 3h = 0.625 A 4h = 0.937 A 5h = 1.250 A 6h = 1.562 A 7h = 1.875 A 8h = 2.187 A 9h = 2.5 A Ah = 2.812 A Bh = 3.125 A Ch = 3.437 A Dh = 3.75 A Eh = Not Applicable Fh = Not Applicable
18	EEP_FAULT_MODE	R/W	0h	Fault response type for EEPROM fault 0h = Latched Fault 1h = Report only fault

Copyright © 2025 Texas Instruments Incorporated

Table 7-19. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-15	LOCK_ILIMIT_MODE	R/W	0h	Lock current limit mode 0h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 2h = Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON) 3h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active 4h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high side brake mode (All high side FETs are turned ON); nFAULT active 6h = Ilimit lock detection current limit is in report only but no action is taken; nFAULT active 7h = ILIMIT LOCK is disabled
14-11	LOCK_ILIMIT_DEG	R/W	0h	Lock current limit detection deglitch time 0h = No deglitch 1h = 0.1 ms 2h = 0.2 ms 3h = 0.5 ms 4h = 1 ms 5h = 2.5 ms 6h = 5 ms 7h = 7.5 ms 8h = 10 ms 9h = 25 ms Ah = 50 ms Bh = 75 ms Ch = 100 ms Dh = 200 ms Eh = 500 ms Fh = 1000 ms

Copyright © 2025 Texas Instruments Incorporated

Table 7-19. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-7	LCK_RETRY	R/W	0h	Lock detection retry time 0h = 300 ms 1h = 500 ms 2h = 1 s 3h = 2 s 4h = 3 s 5h = 4 s 6h = 5 s 7h = 6 s 8h = 7 s 9h = 8 s Ah = 9 s Bh = 10 s Ch = 11 s Dh = 12 s Eh = 13 s Fh = 14 s
6	CRC_ERR_MODE	R/W	0h	CRC (in I2C communication) error mode 0h = CRC error on I2C causes latched fault; nFAULT active; Gate driver is tristated 1h = CRC error on I2C causes report only but no action is taken; nFAULT is active
5-3	MTR_LCK_MODE	R/W	0h	Motor lock mode 0h = Motor lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 2h = Motor lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON) 3h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active 4h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high side brake mode (All high side FETs are turned ON); nFAULT active 6h = Motor lock detection current limit is in report only but no action is taken; nFAULT active 7h = MTR LOCK is disabled

Copyright © 2025 Texas Instruments Incorporated

Table 7-19. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	IPD_TIMEOUT_FAULT_EN	R/W	0h	IPD timeout fault enable 0h = Disable 1h = Enable
1	IPD_FREQ_FAULT_EN	R/W	0h	IPD frequency fault enable 0h = Disable 1h = Enable
0	SATURATION_FLAGS_EN	R/W	0h	Enable indication of current loop and speed loop saturation 0h = Disable 1h = Enable

Copyright © 2025 Texas Instruments Incorporated

7.2.2 FAULT_CONFIG2 Register (Offset = 92h) [Reset = 00000000h]

FAULT_CONFIG2 is shown in Figure 7-16 and described in Table 7-20.

Return to the Summary Table.

Register to configure fault settings2

Figure 7-16. FAULT_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	LOCK1_EN	LOCK2_EN	LOCK3_EN	LOCK_ABN_SPEED			ABNORMAL_BEMF_THR
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
23	22	21	20	19	18	17	16
ABNORMAL_BEMF_THR		NO_MTR_THR			HW_LOCK_ILIMIT_MODE		
R/W-0h		R/W-0h			R/W-0h		
15	14	13	12	11	10	9	8
HW_LOCK_ILIMIT_DEG			VOLTAGE_HYSTERESIS		MIN_VM_MOTOR		
R/W-0h			R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
MIN_VM_MODE	MAX_VM_MOTOR			MAX_VM_MODE	AUTO_RETRY_TIMES		
R/W-0h	R/W-0h			R/W-0h	R/W-0h		

Table 7-20. FAULT_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	LOCK1_EN	R/W	0h	Lock 1 (Abnormal Speed) Enable 0h = Disable 1h = Enable
29	LOCK2_EN	R/W	0h	Lock 2 (Abnormal BEMF) Enable 0h = Disable 1h = Enable
28	LOCK3_EN	R/W	0h	Lock 3 (No Motor) Enable 0h = Disable 1h = Enable
27-25	LOCK_ABN_SPEED	R/W	0h	Abnormal speed lock threshold (% of MAX_SPEED) 0h = 130% 1h = 140% 2h = 150% 3h = 160% 4h = 170% 5h = 180% 6h = 190% 7h = 200%

Copyright © 2025 Texas Instruments Incorporated

Table 7-20. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24-22	ABNORMAL_BEMF_THR	R/W	0h	Abnormal BEMF lock threshold (% of expected BEMF) 0h = 40% 1h = 45% 2h = 50% 3h = 55% 4h = 60% 5h = 65% 6h = 67.5% 7h = 70%
21-19	NO_MTR_THR	R/W	0h	No motor lock threshold 0h = 0.023 A 1h = 0.046 A 2h = 0.062A 3h = 0.078 A 4h = 0.156 A 5h = 0.312 A 6h = 0.468 A 7h = 0.625 A
18-16	HW_LOCK_ILIMIT_MODE	R/W	0h	Hardware lock current limit mode 0h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is tristated 1h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in low side brake mode (All low side FETs are turned ON) 2h = Hardware Ilimit lock detection causes latched fault; nFAULT active; Gate driver is in high side brake mode (All high side FETs are turned ON) 3h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFAULT active 4h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in low side brake mode (All low side FETs are turned ON); nFAULT active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in high side brake mode (All high side FETs are turned ON); nFAULT active 6h = Hardware Ilimit lock detection current limit is in report only but no action is taken; nFAULT active 7h = HARDWARE ILIMIT LOCK is disabled

Copyright © 2025 Texas Instruments Incorporated

Table 7-20. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	HW_LOCK_ILIMIT_DEG	R/W	0h	Hardware lock current limit detection deglitch time 0h = No deglitch 1h = 1 µs 2h = 2 µs 3h = 3 µs 4h = 4 µs 5h = 5 µs 6h = 6 µs 7h = 7 µs
12-11	VOLTAGE_HYSTERESIS	R/W	0h	Hysteresis for controller overvoltage and undervoltage faults. Fault triggered at threshold, cleared at threshold ± hysteresis (+ for UV, - for OV). 0h = 0.5V 1h = 1V 2h = 2V 3h = 3V
10-8	MIN_VM_MOTOR	R/W	0h	Controller under voltage fault threshold - minimum DC bus voltage for running motor 0h = No Limit 1h = 6 V 2h = 7 V 3h = 8 V 4h = 10 V 5h = 14 V 6h = 16 V 7h = 18 V
7	MIN_VM_MODE	R/W	0h	DC bus (controller) undervoltage fault recovery mode 0h = Latch on Undervoltage 1h = Automatic clear if voltage in bounds
6-4	MAX_VM_MOTOR	R/W	0h	Controller over voltage fault threshold - maximum DC bus voltage for running motor 0h = No Limit 1h = 18 V 2h = 20 V 3h = 22 V 4h = 28 V 5h = 30 V 6h = 32 V 7h = 34 V
3	MAX_VM_MODE	R/W	0h	DC bus (controller) overvoltage fault recovery mode 0h = Latch on Overvoltage 1h = Automatic clear if voltage in bounds

Copyright © 2025 Texas Instruments Incorporated

Table 7-20. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	AUTO_RETRY_TIMES	R/W	0h	Number of automatic retry attempts 0h = No Limit 1h = 2 2h = 3 3h = 5 4h = 7 5h = 10 6h = 15 7h = 20

7.3 Hardware_Configuration Registers

Table 7-21 lists the memory-mapped registers for the Hardware_Configuration registers. All register offset addresses not listed in Table 7-21 should be considered as reserved locations and the register contents should not be modified.

Table 7-21. HARDWARE_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
A4h	PIN_CONFIG	Hardware Pin Configuration	Section 7.3.1
A6h	DEVICE_CONFIG1	Device configuration1	Section 7.3.2
A8h	DEVICE_CONFIG2	Device configuration2	Section 7.3.3
AAh	PERI_CONFIG1	Peripheral Configuration1	Section 7.3.4
ACh	GD_CONFIG1	Gate Driver Configuration1	Section 7.3.5
AEh	GD_CONFIG2	Gate Driver Configuration2	Section 7.3.6

Complex bit access types are encoded to fit into small table cells. Table 7-22 shows the codes that are used for access types in this section.

Table 7-22. Hardware_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2025 Texas Instruments Incorporated

7.3.1 PIN_CONFIG Register (Offset = A4h) [Reset = 00000000h]

PIN_CONFIG is shown in Figure 7-17 and described in Table 7-23.

Return to the Summary Table.

Register to configure hardware pins

Figure 7-17. PIN_CONFIG Register

31	30	29	28	27	26	25	24
PARITY	PWM_DITHER_STEP		VDC_FILTER		LEAD_ANGLE		
R/W-0h	R/W-0h		R/W-0h		R/W-0h		
23	22	21	20	19	18	17	16
LEAD_ANGLE		MAX_POWER					
R/W-0h		R/W-0h					
15	14	13	12	11	10	9	8
MAX_POWER					FG_IDLE_CONFIG		FG_FAULT_CONFIG
R/W-0h					R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
FG_FAULT_CONFIG	ALARM_PIN_EN	BRAKE_PIN_MODE	ALIGN_BRAKE_ANGLE_SEL	BRAKE_INPUT		SPEED_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

Table 7-23. PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	PWM_DITHER_STEP	R/W	0h	PWM dither slew rate 0h = 1 1h = 2 2h = 5 3h = 10
28-27	VDC_FILTER	R/W	0h	Vdc(VM) filter coefficient 0h = Disable 1h = Enable with default filter cut-off frequency 2h = Enable with filter cut-off frequency 100Hz 3h = Enable with filter cut-off frequency 1000Hz

Copyright © 2025 Texas Instruments Incorporated

Table 7-23. PIN_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-22	LEAD_ANGLE	R/W	0h	Lead angle. In voltage mode, positive value indicates the applied voltage is leading the BEMF, negative value indicates applied voltage is lagging the BEMF. In other modes, positive means negative id reference, negative means positive id reference 0h = 0 deg 1h = 3 deg 2h = 6 deg 3h = 9 deg 4h = 12 deg 5h = 15 deg 6h = 18 deg 7h = 21 deg 8h = 24 deg 9h = 27 deg Ah = 30 deg Bh = 33 deg Ch = 36 deg Dh = 39 deg Eh = 42 deg Fh = 45 deg 10h = -48 deg 11h = -45 deg 12h = -42 deg 13h = -39 deg 14h = -36 deg 15h = -33 deg 16h = -30 deg 17h = -27 deg 18h = -24 deg 19h = -21 deg 1Ah = -18 deg 1Bh = -15 deg 1Ch = -12 deg 1Dh = -9 deg 1Eh = -6 deg 1Fh = -3 deg
21-11	MAX_POWER	R/W	0h	Maximum power for power loop or power limit. Max power in Watts = (MAX_POWER / 2^{11}) * 100
10-9	FG_IDLE_CONFIG	R/W	0h	FG configuration during motor stopped/idle state 0h = FG continues and end state depends on FG_CONFIG and last state before motor stops 1h = FG is pulled High 2h = FG is pulled Low 3h = FG is pulled High

Copyright © 2025 Texas Instruments Incorporated

Table 7-23. PIN_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-7	FG_FAULT_CONFIG	R/W	0h	FG configuration during fault state. BEMF threshold defined by FG_BEMF_THR if FG_CONFIG 1 0h = Use last FG signal when motor was driven 1h = FG is pulled High 2h = FG is pulled Low 3h = FG active till BEMF drops below BEMF threshold
6	ALARM_PIN_EN	R/W	0h	Enable Alarm pin 0h = Disable 1h = Enable
5	BRAKE_PIN_MODE	R/W	0h	Brake pin mode 0h = Low side Brake 1h = Align Brake
4	ALIGN_BRAKE_ANGLE_SEL	R/W	0h	Select align brake angle 0h = Use last commutation angle before entering align braking 1h = Use ALIGN_ANGLE configuration for align braking
3-2	BRAKE_INPUT	R/W	0h	Brake pin override 0h = Hardware Pin BRAKE 1h = Override pin and brake / align according to BRAKE_PIN_MODE 2h = Override pin and do not brake / align 3h = Hardware Pin BRAKE
1-0	SPEED_MODE	R/W	0h	Configure motor control input source 0h = Controlled by analog voltage on SPEED pin 1h = Controlled by duty cycle (PWM) on SPEED pin 2h = Controlled by DIGITAL_SPEED_CTRL value (I2C) 3h = Controlled by frequency on SPEED pin

Copyright © 2025 Texas Instruments Incorporated

7.3.2 DEVICE_CONFIG1 Register (Offset = A6h) [Reset = 00000000h]

DEVICE_CONFIG1 is shown in Figure 7-18 and described in Table 7-24.

Return to the Summary Table.

Register to configure device

Figure 7-18. DEVICE_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED	DAC_SOx_SEL		PWM_DITHER_MODE	I2C_TARGET_ADDR		
R/W-0h	R-0h	R/W-0h		R/W-0h	R/W-0h		
23	22	21	20	19	18	17	16
I2C_TARGET_ADDR				EEPROM_LOCK_KEY			
R/W-0h				W-0h			
15	14	13	12	11	10	9	8
EEPROM_LOCK_KEY							
W-0h							
7	6	5	4	3	2	1	0
EEPROM_LOCK_KEY			SLEW_RATE_I2C_PINS		PULLUP_ENABLE	BUS_VOLT	
W-0h			R/W-0h		R/W-0h	R/W-0h	

Table 7-24. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	RESERVED	R	0h	Reserved
29-28	DAC_SOx_SEL	R/W	0h	Select between DACOUT2 and SOx channels 0h = DACOUT2 1h = SOA 2h = SOB 3h = SOC
27	PWM_DITHER_MODE	R/W	0h	PWM dither mode 0h = Triangular Mode 1h = Random Mode
26-20	I2C_TARGET_ADDR	R/W	0h	I2C target address
19-5	EEPROM_LOCK_KEY	W	0h	EEPROM lock/unlock key when EEPROM R/W protection is enabled. This bitfield will always read 0 when read.
4-3	SLEW_RATE_I2C_PINS	R/W	0h	Slew rate control for I2C pins 0h = 4.8 mA 1h = 3.9 mA 2h = 1.86 mA 3h = 30.8 mA
2	PULLUP_ENABLE	R/W	0h	Internal pull-up enable for nFAULT and FG pins 0h = Disable 1h = Enable

Copyright © 2025 Texas Instruments Incorporated

Table 7-24. DEVICE_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	BUS_VOLT	R/W	0h	Maximum DC bus voltage configuration 0h = 15 V 1h = 30 V 2h = 40 V 3h = Not Applicable

Copyright © 2025 Texas Instruments Incorporated

7.3.3 DEVICE_CONFIG2 Register (Offset = A8h) [Reset = 00000000h]

DEVICE_CONFIG2 is shown in Figure 7-19 and described in Table 7-25.

Return to the Summary Table.

Register to configure device

Figure 7-19. DEVICE_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	INPUT_MAXIMUM_FREQ						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
INPUT_MAXIMUM_FREQ							
R/W-0h							
15	14	13	12	11	10	9	8
SLEEP_ENTRY_TIME		DYNAMIC_CSA_GAIN_EN	DYNAMIC_VOLTAGE_GAIN_EN	DEV_MODE	PWM_DITHER_DEPTH		EXT_CLK_EN
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
7	6	5	4	3	2	1	0
EXT_CLK_CONFIG			EXT_WDT_EN	EXT_WDT_CONFIG		EXT_WDT_INPUT_MODE	EXT_WDT_FAULT_MODE
R/W-0h			R/W-0h	R/W-0h		R/W-0h	R/W-0h

Table 7-25. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-16	INPUT_MAXIMUM_FREQ	R/W	0h	Input frequency on speed pin for input reference mode as "controlled by frequency of SPEED pin" that corresponds to 100% duty cycle. Duty cycle = Input frequency / INPUT_MAXIMUM_FREQ
15-14	SLEEP_ENTRY_TIME	R/W	0h	Device enters sleep mode when input source (SPEED_MODE) is held at or below the sleep entry threshold for SLEEP_ENTRY_TIME 0h = Sleep Entry when SPEED pin remains low for 50 µs 1h = Sleep Entry when SPEED pin remains low for 200 µs 2h = Sleep Entry when SPEED pin remains low for 20 ms 3h = Sleep Entry when SPEED pin remains low for 200 ms
13	DYNAMIC_CSA_GAIN_EN	R/W	0h	Adjust CSA gain automatically for optimal current resolution at all current levels 0h = Disable 1h = Enable
12	DYNAMIC_VOLTAGE_GAIN_EN	R/W	0h	Adjust voltage gain automatically for optimal voltage resolution at all voltage levels 0h = Disable 1h = Enable
11	DEV_MODE	R/W	0h	Device mode select 0h = Standby Mode 1h = Sleep Mode

Copyright © 2025 Texas Instruments Incorporated

Table 7-25. DEVICE_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-9	PWM_DITHER_DEPTH	R/W	0h	PWM dither depth 0h = PWM dither disabled 1h = 5% 2h = 7.5% 3h = 10%
8	EXT_CLK_EN	R/W	0h	Enable external clock mode 0h = Disable 1h = Enable
7-5	EXT_CLK_CONFIG	R/W	0h	External clock frequency configuration 0h = 8 kHz 1h = 16 kHz 2h = 32 kHz 3h = 64 kHz 4h = 128 kHz 5h = 256 kHz 6h = 512 kHz 7h = 1024 kHz
4	EXT_WDT_EN	R/W	0h	Enable external watchdog 0h = Disable 1h = Enable
3-2	EXT_WDT_CONFIG	R/W	0h	Time between watchdog tickles (GPIO/I2C) 0h = 100ms/1s 1h = 200ms/2s 2h = 500ms/5s 3h = 1000ms/10s
1	EXT_WDT_INPUT_MODE	R/W	0h	External watchdog input source 0h = Watchdog tickle over I2C 1h = Watchdog tickle over GPIO
0	EXT_WDT_FAULT_MODE	R/W	0h	External watchdog fault mode 0h = Report only 1h = Latch with MOSFETs in Hi-Z

Copyright © 2025 Texas Instruments Incorporated

7.3.4 PERI_CONFIG1 Register (Offset = AAh) [Reset = 00000000h]

PERI_CONFIG1 is shown in Figure 7-20 and described in Table 7-26.

Return to the Summary Table.

Register to peripheral1

Figure 7-20. PERI_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	SPREAD_SPECTRUM_MODULATION_DIS	RESERVED	NO_MTR_FLT_CLOSEDLOOP_DIS	ABNORMAL_BEMF_PERSISTENT_TIME		FLUX_WEAK_REF	
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
INPUT_REFERENCE_WINDOW		BUS_POWER_LIMIT_ENABLE	DIR_INPUT		DIR_CHANGE_MODE	SPEED_LIMIT_ENABLE	ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY
R/W-0h		R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY			ACTIVE_BRAKE_MOD_INDEX_LIMIT			SPEED_RANGE_SEL	INPUT_REFERENCE_MODE
R/W-0h			R/W-0h			R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
INPUT_REFERENCE_MODE	EEPROM_LOCK_MODE		RESERVED				
R/W-0h	R/W-0h		R-0h				

Table 7-26. PERI_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	SPREAD_SPECTRUM_MODULATION_DIS	R/W	0h	Disable Spread Spectrum Modulation (SSM) 0h = SSM is Enabled 1h = SSM is Disabled
29	RESERVED	R	0h	Reserved
28	NO_MTR_FLT_CLOSEDLOOP_DIS	R/W	0h	Disable No Motor fault in closed loop 0h = Enable no motor fault in closed loop if LOCK2_EN is set to 0x1 1h = Disable No Motor fault in closed loop
27-26	ABNORMAL_BEMF_PERSISTENT_TIME	R/W	0h	Deglitch time for Abnormal BEMF fault detection 0h = 2 electrical cycles 1h = 500 ms 2h = 1000 ms 3h = 2000 ms
25-24	FLUX_WEAK_REF	R/W	0h	Reference for flux weakening controller 0h = 70% 1h = 80% 2h = 90% 3h = 95%

Copyright © 2025 Texas Instruments Incorporated

Table 7-26. PERI_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-22	INPUT_REFERENCE_WINDOW	R/W	0h	Disables all control loops when output reaches within the window 0h = Reference window disabled 1h = Reference window of 5% 2h = Reference window of 10% 3h = Reference window of 15%
21	BUS_POWER_LIMIT_ENABLE	R/W	0h	Enable bus power limit. Limits input DC bus power to MAX_POWER in all input reference modes except power mode 0h = Disable power limit 1h = Enable power limit
20-19	DIR_INPUT	R/W	0h	DIR pin override 0h = Hardware Pin DIR 1h = Override DIR pin with clockwise rotation OUTA-OUTB-OUTC 2h = Override DIR pin with counter clockwise rotation OUTA-OUTC-OUTB 3h = Hardware Pin DIR
18	DIR_CHANGE_MODE	R/W	0h	Response to change of DIR pin status 0h = Follow motor stop options and ISD routine on detecting DIR change 1h = Change the direction through Reverse Drive while continuously driving the motor
17	SPEED_LIMIT_ENABLE	R/W	0h	Enable motor speed limit. Limits motor speed to MAX_SPEED in all input reference modes except speed mode 0h = Disable speed limit 1h = Enable speed limit
16-13	ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY	R/W	0h	Difference between final speed and present speed below which active braking will be applied 0h = Not Applicable 1h = 5% 2h = 10% 3h = 15% 4h = 20% 5h = 25% 6h = 30% 7h = 35% 8h = 40% 9h = 45% Ah = 50% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%

Copyright © 2025 Texas Instruments Incorporated

Table 7-26. PERI_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	ACTIVE_BRAKE_MOD_INDEX_LIMIT	R/W	0h	Modulation index limit below which active braking will be applied 0h = 0% 1h = 40% 2h = 50% 3h = 60% 4h = 70% 5h = 80% 6h = 90% 7h = 100%
9	SPEED_RANGE_SEL	R/W	0h	Frequency range selection for PWM duty mode reference input 0h = 325Hz to 100kHz 1h = 10Hz to 325Hz
8-7	INPUT_REFERENCE_MODE	R/W	0h	Input reference mode used for close loop operation 0h = Control speed (Input is speed reference, scaled to MAX_SPEED) 1h = Control power (Input is power reference, scaled to MAX_POWER) 2h = Control Torque (Input is current reference, scaled to ILIMIT) 3h = Control Modulation Index (Input is modulation index scaled to 100%)
6-5	EEPROM_LOCK_MODE	R/W	0h	EEPROM lock mode 0h = EEPROM read and write allowed without a passcode 1h = EEPROM read and write need a valid passcode 2h = EEPROM read needs a valid passcode, write is locked permanently 3h = EEPROM read and write is locked permanently
4-0	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

7.3.5 GD_CONFIG1 Register (Offset = ACh) [Reset = 00000000h]

GD_CONFIG1 is shown in Figure 7-21 and described in Table 7-27.

Return to the Summary Table.

Register to configure gated driver settings1

Figure 7-21. GD_CONFIG1 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED		RESERVED	SLEW_RATE		RESERVED	
R/W-0h	R-0h		R-0h	R/W-0h		R-0h	
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	OVP_SEL	OVP_EN	RESERVED	OTW_REP
R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	RESERVED	OCP_DEG		RESERVED	OCP_LVL	OCP_MODE	
R-0h	R-0h	R/W-0h		R-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CSA_GAIN	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h	

Table 7-27. GD_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	RESERVED	R	0h	Reserved
28	RESERVED	R	0h	Reserved
27-26	SLEW_RATE	R/W	0h	Slew rate 0h = Not Applicable 1h = Not Applicable 2h = Slew rate is 125 V/µs 3h = Slew rate is 200 V/µs
25-24	RESERVED	R	0h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R	0h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R	0h	Reserved
19	OVP_SEL	R/W	0h	Overvoltage level 0h = VM overvoltage level is 34-V 1h = VM overvoltage level is 22-V
18	OVP_EN	R/W	0h	Enable overvoltage 0h = Overvoltage protection is disabled 1h = Overvoltage protection is enabled
17	RESERVED	R	0h	Reserved
16	OTW_REP	R/W	0h	Overtemperature warning reporting 0h = Over temperature warning reporting is disabled 1h = Over temperature warning reporting is enabled
15	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

Table 7-27. GD_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RESERVED	R	0h	Reserved
13-12	OCP_DEG	R/W	0h	OCP deglitch time 0h = OCP deglitch time is 0.2 µs 1h = OCP deglitch time is 0.6 µs 2h = OCP deglitch time is 1.2 µs 3h = OCP deglitch time is 1.6 µs
11	RESERVED	R	0h	Reserved
10	OCP_LVL	R/W	0h	Overcurrent level 0h = OCP level is 9 A (Typical) 1h = OCP level is 13 A (Typical)
9-8	OCP_MODE	R/W	0h	OCP fault mode 0h = Overcurrent causes a latched fault 1h = Overcurrent causes an automatic retry after 500ms 2h = Not Applicable 3h = Not Applicable
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1-0	CSA_GAIN	R/W	0h	Current sense amplifier's gain (used only if DYNAMIC_CSA_GAIN_EN = 0x0) 0h = CSA gain is 0.24 V/A 1h = CSA gain is 0.48 V/A 2h = CSA gain is 0.96 V/A 3h = CSA gain is 1.92 V/A

Copyright © 2025 Texas Instruments Incorporated

7.3.6 GD_CONFIG2 Register (Offset = AEh) [Reset = 00000000h]

GD_CONFIG2 is shown in Figure 7-22 and described in Table 7-28.

Return to the Summary Table.

Register to configure gated driver settings2

Figure 7-22. GD_CONFIG2 Register

31	30	29	28	27	26	25	24
PARITY	RESERVED	RESERVED				RESERVED	BUCK_PS_DIS
R/W-0h	R-0h	R-0h				R-0h	R/W-0h
23	22	21	20	19	18	17	16
BUCK_CL	BUCK_SEL		BUCK_DIS	MIN_ON_TIME			RESERVED
R/W-0h	R/W-0h		R/W-0h	R/W-0h			R-0h
15	14	13	12	11	10	9	8
RESERVED			RESERVED				
R-0h			R-0h				
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 7-28. GD_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	RESERVED	R	0h	Reserved
29-26	RESERVED	R	0h	Reserved
25	RESERVED	R	0h	Reserved
24	BUCK_PS_DIS	R/W	0h	Buck power sequencing disable 0h = Buck power sequencing is enabled 1h = Buck power sequencing is disabled
23	BUCK_CL	R/W	0h	Buck current limit 0h = Buck regulator current limit is set to 600 mA 1h = Buck regulator current limit is set to 150 mA
22-21	BUCK_SEL	R/W	0h	Buck output voltage 0h = Buck voltage is 3.3 V 1h = Buck voltage is 5.0 V 2h = Buck voltage is 4.0 V 3h = Buck voltage is 5.7 V
20	BUCK_DIS	R/W	0h	Buck disable 0h = Buck regulator is enabled 1h = Buck regulator is disabled

Copyright © 2025 Texas Instruments Incorporated

Table 7-28. GD_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-17	MIN_ON_TIME	R/W	0h	Minimum ON time for low side MOSFET 0h = 0 µs 1h = Automatic based on slew rate 2h = 0.5 µs 3h = 0.75 µs 4h = 1 µs 5h = 1.25 µs 6h = 1.5 µs 7h = 2 µs
16-13	RESERVED	R	0h	Reserved
12-0	RESERVED	R	0h	Reserved

7.4 Internal_Algorithm_Configuration Registers

Table 7-29 lists the memory-mapped registers for the Internal_Algorithm_Configuration registers. All register offset addresses not listed in Table 7-29 should be considered as reserved locations and the register contents should not be modified.

Table 7-29. INTERNAL_ALGORITHM_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
A0h	INT_ALGO_1	Internal Algorithm Configuration1	Section 7.4.1
A2h	INT_ALGO_2	Internal Algorithm Configuration2	Section 7.4.2

Complex bit access types are encoded to fit into small table cells. Table 7-30 shows the codes that are used for access types in this section.

Table 7-30. Internal_Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2025 Texas Instruments Incorporated

7.4.1 INT_ALGO_1 Register (Offset = A0h) [Reset = 00000000h]

INT_ALGO_1 is shown in Figure 7-23 and described in Table 7-31.

Return to the Summary Table.

Register to configure internal algorithm parameters1

Figure 7-23. INT_ALGO_1 Register

31	30	29	28	27	26	25	24
PARITY	ACTIVE_BRAKE_SPEED__DELTA_LIMIT_EXIT		SPEED_PIN_GLITCH_FILTER		FAST_ISD_EN	ISD_STOP_TIME	
R/W-0h	R/W-0h		R/W-0h		R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
ISD_RUN_TIME		ISD_TIMEOUT		AUTO_HANDOFF_MIN_BEMF			BRAKE_CURRENT_PERSIST
R/W-0h		R/W-0h		R/W-0h			R/W-0h
15	14	13	12	11	10	9	8
BRAKE_CURRENT_PERSIST	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED					REV_DRV_OPEN_LOOP_DEC		
R-0h					R/W-0h		

Table 7-31. INT_ALGO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	ACTIVE_BRAKE_SPEED__DELTA_LIMIT_EXIT	R/W	0h	Difference between final speed and present speed below which active braking will be stopped 0h = 2.5% 1h = 5% 2h = 7.5% 3h = 10%
28-27	SPEED_PIN_GLITCH_FILTER	R/W	0h	Glitch filter applied on speed pin input 0h = No Glitch Filter 1h = 0.2 µs 2h = 0.5 µs 3h = 1.0 µs
26	FAST_ISD_EN	R/W	0h	Enable fast speed detection during ISD 0h = Disable fast ISD 1h = Enable fast ISD
25-24	ISD_STOP_TIME	R/W	0h	Persistence time for declaring motor is in stopped state during ISD 0h = 1 ms 1h = 5 ms 2h = 50 ms 3h = 100 ms

Copyright © 2025 Texas Instruments Incorporated

Table 7-31. INT_ALGO_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-22	ISD_RUN_TIME	R/W	0h	Persistence time for declaring motor is in running state during ISD 0h = 1 ms 1h = 5 ms 2h = 50 ms 3h = 100 ms
21-20	ISD_TIMEOUT	R/W	0h	Timeout in case ISD is unable to reliably detect speed or direction 0h = 500ms 1h = 750 ms 2h = 1000 ms 3h = 2000 ms
19-17	AUTO_HANDOFF_MIN_BEMF	R/W	0h	Minimum BEMF for handoff. Applicable when auto handoff is enabled. 0h = 0 mV 1h = 50 mV 2h = 100 mV 3h = 250 mV 4h = 500 mV 5h = 1000 mV 6h = 1250 mV 7h = 1500 mV
16-15	BRAKE_CURRENT_PERSIST	R/W	0h	Persistence time for current below threshold during current based ISD brake 0h = 50 ms 1h = 100 ms 2h = 250 ms 3h = 500 ms
14-3	RESERVED	R	0h	Reserved
2-0	REV_DRV_OPEN_LOOP_DEC	R/W	0h	% of open loop acceleration to be applied during open loop deceleration in reverse drive 0h = 50% 1h = 60% 2h = 70% 3h = 80% 4h = 90% 5h = 100% 6h = 125% 7h = 150%

Copyright © 2025 Texas Instruments Incorporated

7.4.2 INT_ALGO_2 Register (Offset = A2h) [Reset = 00000000h]

INT_ALGO_2 is shown in Figure 7-24 and described in Table 7-32.

Return to the Summary Table.

Register to configure internal algorithm parameters2

Figure 7-24. INT_ALGO_2 Register

31	30	29	28	27	26	25	24
PARITY	FLUX_WEAK_KP						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
FLUX_WEAK_KP			FLUX_WEAK_KI				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
FLUX_WEAK_KI					FLUX_WEAK_ENABLE	CL_SLOW_ACC	
R/W-0h					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
CL_SLOW_ACC		ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE			ISD_BEMF_FILT_ENABLE	CIRCULAR_CURRENT_LIMIT_ENABLE	IPD_HIGH_RESOLUTION_EN
R/W-0h		R/W-0h			R/W-0h	R/W-0h	R/W-0h

Table 7-32. INT_ALGO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-21	FLUX_WEAK_KP	R/W	0h	10-bit value for flux weakening loop Kp. Kp = 8LSB of 0.1 * FLUX_WEAK_KP / 10^2MSB of FLUX_WEAK_KP.
20-11	FLUX_WEAK_KI	R/W	0h	10-bit value for current Iq and Id loop Ki. Ki = 10 * 8LSB of FLUX_WEAK_KI / 10^2MSB of FLUX_WEAK_KI.
10	FLUX_WEAK_ENABLE	R/W	0h	Enable flux weakening 0h = Flux Weakening is disabled 1h = Flux Weakening is enabled

Copyright © 2025 Texas Instruments Incorporated

Table 7-32. INT_ALGO_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-6	CL_SLOW_ACC	R/W	0h	Close loop acceleration when estimator is not yet fully aligned (only in speed mode) and acceleration/deacceleration during power/speed limit (Speed mode: Hz/s Power mode: deciWatts/s Torque mode: centiA/s duty cycle mode: milliUnit/s) deciWatt: 0.1W centiA: 0.01A milliUnit: 0.001% 0h = 0.1 Hz/s 1h = 1 Hz/s 2h = 2 Hz/s 3h = 3 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 20 Hz/s 7h = 30 Hz/s 8h = 40 Hz/s 9h = 50 Hz/s Ah = 100 Hz/s Bh = 200 Hz/s Ch = 500 Hz/s Dh = 750 Hz/s Eh = 1000 Hz/s Fh = 2000 Hz/s
5-3	ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE	R/W	0h	Bus current slew rate during active braking 0h = 10 A/s 1h = 50 A/s 2h = 100 A/s 3h = 250 A/s 4h = 500 A/s 5h = 1000 A/s 6h = 5000 A/s 7h = No Limit A/s
2	ISD_BEMF_FILT_ENABLE	R/W	0h	Enable BEMF filter during ISD. 0h = Disable 1h = Enable
1	CIRCULAR_CURRENT_LIMIT_ENABLE	R/W	0h	Configuration for ILIMIT vs. peak phase current 0h = Circular current limit is disabled: ILIMIT * sqrt(2) can be peak phase current 1h = Circular current limit is enabled: ILIMIT is peak phase current
0	IPD_HIGH_RESOLUTION_EN	R/W	0h	IPD high resolution enable 0h = Disable 1h = Enable

Copyright © 2025 Texas Instruments Incorporated

8 RAM (Volatile) Register Map

8.1 Fault_Status Registers

Table 8-1 lists the memory-mapped registers for the Fault_Status registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. FAULT_STATUS Registers

Offset	Acronym	Register Name	Section
E0h	GATE_DRIVER_FAULT_STATUS	Fault Status Register	Section 8.1.1
E2h	CONTROLLER_FAULT_STATUS	Fault Status Register	Section 8.1.2
32Ch	EEPROM_FAULT_STATUS		Section 8.1.3

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. Fault_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2025 Texas Instruments Incorporated

8.1.1 GATE_DRIVER_FAULT_STATUS Register (Offset = E0h) [Reset = 00000000h]

GATE_DRIVER_FAULT_STATUS is shown in Figure 8-1 and described in Table 8-3.

Return to the Summary Table.

Status of various gate driver faults

Figure 8-1. GATE_DRIVER_FAULT_STATUS Register

31	30	29	28	27	26	25	24
DRIVER_FAULT	RESERVED	RESERVED	OCP	RESERVED	OVP	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
OTW	OTS	OCP_HC	OCP_LC	OCP_HB	OCP_LB	OCP_HA	OCP_LA
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED	RESERVED	BUCK_OCP	BUCK_UV	VCP_UV	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 8-3. GATE_DRIVER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRIVER_FAULT	R	0h	Logic OR of gate driver fault status bits
30	RESERVED	R	0h	Reserved
29	RESERVED	R	0h	Reserved
28	OCP	R	0h	Over current protection status 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
27	RESERVED	R	0h	Reserved
26	OVP	R	0h	Supply (VM) overvoltage protection status 0h = No overvoltage condition is detected on VM 1h = Overvoltage condition is detected on VM
25	RESERVED	R	0h	Reserved
24	RESERVED	R	0h	Reserved
23	OTW	R	0h	Overtemperature warning status 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
22	OTS	R	0h	Overtemperature shutdown status 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected
21	OCP_HC	R	0h	Overcurrent status on high-side switch of OUTC 0h = No overcurrent detected on high-side switch of OUTC 1h = Overcurrent detected on high-side switch of OUTC

Copyright © 2025 Texas Instruments Incorporated

Table 8-3. GATE_DRIVER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	OCP_LC	R	0h	Overcurrent status on low-side switch of OUTC 0h = No overcurrent detected on low-side switch of OUTC 1h = Overcurrent detected on low-side switch of OUTC
19	OCP_HB	R	0h	Overcurrent status on high-side switch of OUTB 0h = No overcurrent detected on high-side switch of OUTB 1h = Overcurrent detected on high-side switch of OUTB
18	OCP_LB	R	0h	Overcurrent status on low-side switch of OUTB 0h = No overcurrent detected on low-side switch of OUTB 1h = Overcurrent detected on low-side switch of OUTB
17	OCP_HA	R	0h	Overcurrent status on high-side switch of OUTA 0h = No overcurrent detected on high-side switch of OUTA 1h = Overcurrent detected on high-side switch of OUTA
16	OCP_LA	R	0h	Overcurrent status on low-side switch of OUTA 0h = No overcurrent detected on low-side switch of OUTA 1h = Overcurrent detected on low-side switch of OUTA
15	RESERVED	R	0h	Reserved
14	RESERVED	R	0h	Reserved
13	BUCK_OCP	R	0h	Buck regulator overcurrent status 0h = No buck regulator overcurrent is detected 1h = Buck regulator overcurrent is detected
12	BUCK_UV	R	0h	Buck regulator undervoltage status 0h = No buck regulator undervoltage is detected 1h = Buck regulator undervoltage is detected
11	VCP_UV	R	0h	Charge pump undervoltage status 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
10	RESERVED	R	0h	Reserved
9	RESERVED	R	0h	Reserved
8	RESERVED	R	0h	Reserved
7-0	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

8.1.2 CONTROLLER_FAULT_STATUS Register (Offset = E2h) [Reset = 00000000h]

CONTROLLER_FAULT_STATUS is shown in Figure 8-2 and described in Table 8-4.

Return to the Summary Table.

Status of various controller faults

Figure 8-2. CONTROLLER_FAULT_STATUS Register

31	30	29	28	27	26	25	24
CONTROLLER_FAULT	RESERVED	IPD_FREQ_FAULT	IPD_T1_FAULT	IPD_T2_FAULT	RESERVED	MPET_IPD_FAULT	MPET_BEMF_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
ABN_SPEED	ABN_BEMF	NO_MTR	MTR_LCK	LOCK_LIMIT	HW_LOCK_LIMIT	MTR_UNDER_VOLTAGE	MTR_OVER_VOLTAGE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
SPEED_LOOP_SATURATION	CURRENT_LOOP_SATURATION	MAX_SPEED_SATURATION	BUS_POWER_LIMIT_SATURATION	EEPROM_WRITE_LOCK_SET	EEPROM_READ_LOCK_SET	RESERVED	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	
7	6	5	4	3	2	1	0
RESERVED	I2C_CRC_FAULT_STATUS	EEPROM_ERR_STATUS	BOOT_STL_FAULT	WATCHDOG_FAULT	CPU_RESET_FAULT_STATUS	WWDT_FAULT_STATUS	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-4. CONTROLLER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CONTROLLER_FAULT	R	0h	Logic OR of controller fault status bits
30	RESERVED	R	0h	Reserved
29	IPD_FREQ_FAULT	R	0h	IPD frequency fault status
28	IPD_T1_FAULT	R	0h	IPD T1 fault status
27	IPD_T2_FAULT	R	0h	IPD T2 fault status
26	RESERVED	R	0h	Reserved
25	MPET_IPD_FAULT	R	0h	Indicates error during MPET resistance and inductance measurement
24	MPET_BEMF_FAULT	R	0h	Indicates error during MPET BEMF constant measurement
23	ABN_SPEED	R	0h	Indicates Abnormal speed motor lock condition
22	ABN_BEMF	R	0h	Indicates Abnormal BEMF motor lock condition
21	NO_MTR	R	0h	Indicates No Motor (loss of phase) fault
20	MTR_LCK	R	0h	Indicates when one of the motor lock (abnormal BEMF/speed, no motor) is triggered
19	LOCK_LIMIT	R	0h	Indicates lock current limit fault
18	HW_LOCK_LIMIT	R	0h	Indicates hardware lock current limit fault
17	MTR_UNDER_VOLTAGE	R	0h	Indicates configurable under voltage fault on VM
16	MTR_OVER_VOLTAGE	R	0h	Indicates configurable over voltage fault on VM
15	SPEED_LOOP_SATURATION	R	0h	Indicates speed loop saturation
14	CURRENT_LOOP_SATURATION	R	0h	Indicates current loop saturation

Copyright © 2025 Texas Instruments Incorporated

Table 8-4. CONTROLLER_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	MAX_SPEED_SATURATION	R	0h	Indicates maximum speed limit saturation
12	BUS_POWER_LIMIT_SATURATION	R	0h	Indicates maximum (input DC bus) power limit saturation
11	EEPROM_WRITE_LOCK_SET	R	0h	Indicates EEPROM write lock is set
10	EEPROM_READ_LOCK_SET	R	0h	Indicates EEPROM read lock is set
9-8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	I2C_CRC_FAULT_STATUS	R	0h	Indicates CRC fault in I2C packet
5	EEPROM_ERR_STATUS	R	0h	Indicates error in EEPROM
4	BOOT_STL_FAULT	R	0h	Indicates self test fault during boot-up (applicable to MCF8315DUL only)
3	WATCHDOG_FAULT	R	0h	Indicates watchdog timeout fault
2	CPU_RESET_FAULT_STATUS	R	0h	Indicates unexpected CPU reset fault (applicable to MCF8315DUL only)
1	WWDT_FAULT_STATUS	R	0h	Indicates windowed watchdog reset fault (applicable to MCF8315DUL only)
0	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

8.1.3 EEPROM_FAULT_STATUS Register (Offset = 32Ch) [Reset = 0000h]

EEPROM_FAULT_STATUS is shown in Figure 8-3 and described in Table 8-5.

Return to the Summary Table.

Figure 8-3. EEPROM_FAULT_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			EEPROM_CRC_FLT_STS	RESERVED	EEPROM_PARITY_FLT_STS	RESERVED	RESERVED
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-5. EEPROM_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0h	Reserved
4	EEPROM_CRC_FLT_STS	R	0h	EEPROM CRC error fault status 0h = EEPROM CRC Error fault condition is not detected 1h = EEPROM CRC Error fault condition is detected
3	RESERVED	R	0h	Reserved
2	EEPROM_PARITY_FLT_STS	R	0h	EEPROM parity error fault status 0h = EEPROM Parity error fault condition is not detected 1h = EEPROM Parity error fault condition is detected
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.2 System_Status Registers

Table 8-6 lists the memory-mapped registers for the System_Status registers. All register offset addresses not listed in Table 8-6 should be considered as reserved locations and the register contents should not be modified.

Table 8-6. SYSTEM_STATUS Registers

Offset	Acronym	Register Name	Section
E4h	ALGO_STATUS	System Status Register	Section 8.2.1
E6h	MTR_PARAMS	System Status Register	Section 8.2.2
E8h	ALGO_STATUS_MPET	System Status Register	Section 8.2.3

Complex bit access types are encoded to fit into small table cells. Table 8-7 shows the codes that are used for access types in this section.

Table 8-7. System_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2025 Texas Instruments Incorporated

8.2.1 ALGO_STATUS Register (Offset = E4h) [Reset = 00000000h]

ALGO_STATUS is shown in Figure 8-4 and described in Table 8-8.

Return to the Summary Table.

Status of various system and algorithm parameters

Figure 8-4. ALGO_STATUS Register

31	30	29	28	27	26	25	24
VOLT_MAG							
R-0h							
23	22	21	20	19	18	17	16
VOLT_MAG							
R-0h							
15	14	13	12	11	10	9	8
DUTY_CMD							
R-0h							
7	6	5	4	3	2	1	0
DUTY_CMD				RESERVED	SYS_ENABLE_FLAG	RESERVED	
R-0h				R-0h	R-0h	R-0h	

Table 8-8. ALGO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VOLT_MAG	R	0h	16-bit value indicating applied modulation index. Modulation index applied = (VOLT_MAG * 100 / 32768)%
15-4	DUTY_CMD	R	0h	12-bit value indicating input duty command in PWM/Analog/Freq mode DUTY_CMD (%) = (DUTY_CMD/4095 * 100)%.
3	RESERVED	R	0h	Reserved
2	SYS_ENABLE_FLAG	R	0h	1 indicates GUI can control the register 0 indicates GUI is still copying default parameters from shadow memory
1-0	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

8.2.2 MTR_PARAMS Register (Offset = E6h) [Reset = 00000000h]

MTR_PARAMS is shown in Figure 8-5 and described in Table 8-9.

Return to the Summary Table.

Status of various motor parameters

Figure 8-5. MTR_PARAMS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOTOR_R								MOTOR_BEMF_CONST							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOTOR_L								RESERVED							
R-0h								R-0h							

Table 8-9. MTR_PARAMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MOTOR_R	R	0h	8-bit value indicating MPET measured motor resistance
23-16	MOTOR_BEMF_CONST	R	0h	8-bit value indicating MPET measured BEMF constant
15-8	MOTOR_L	R	0h	8-bit value indicating MPET measured motor inductance
7-0	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

8.2.3 ALGO_STATUS_MPET Register (Offset = E8h) [Reset = 00000000h]

ALGO_STATUS_MPET is shown in Figure 8-6 and described in Table 8-10.

Return to the Summary Table.

Status of various MPET parameters

Figure 8-6. ALGO_STATUS_MPET Register

31	30	29	28	27	26	25	24
MPET_R_STATUS	MPET_L_STATUS	MPET_KE_STATUS	MPET_MECH_STATUS	MPET_PWM_FREQ			
R-0h	R-0h	R-0h	R-0h	R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 8-10. ALGO_STATUS_MPET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MPET_R_STATUS	R	0h	Indicates status of resistance measurement 0h = Measurement of motor resistance during MPET routine is not completed if resistance measurement is initiated during MPET 1h = Measurement of motor resistance during MPET routine is completed
30	MPET_L_STATUS	R	0h	Indicates status of inductance measurement 0h = Measurement of motor inductance during MPET routine is not completed if inductance measurement is initiated during MPET 1h = Measurement of motor inductance during MPET routine is completed
29	MPET_KE_STATUS	R	0h	Indicates status of BEMF constant measurement 0h = Measurement of motor BEMF constant during MPET routine is not completed if BEMF constant measurement is initiated during MPET 1h = Measurement of motor BEMF constant during MPET routine is completed
28	MPET_MECH_STATUS	R	0h	Indicates status of mechanical parameter measurement 0h = Auto Calculation of Speed loop Kp, Ki values during MPET routine is not completed if mechanical parameters measurement(speed loop kp,ki values) is initiated during MPET 1h = Auto Calculation of Speed loop Kp, Ki values during MPET routine is completed

Copyright © 2025 Texas Instruments Incorporated

Table 8-10. ALGO_STATUS_MPET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-24	MPET_PWM_FREQ	R	0h	4-bit value indicating MPET recommended PWM switching frequency based on electrical time constant. Follows same enum list as PWM_FREQ_OUT
23-0	RESERVED	R	0h	Reserved

8.3 Device_Control Registers

Table 8-11 lists the memory-mapped registers for the Device_Control registers. All register offset addresses not listed in Table 8-11 should be considered as reserved locations and the register contents should not be modified.

Table 8-11. DEVICE_CONTROL Registers

Offset	Acronym	Register Name	Section
EAh	ALGO_CTRL1	Device Control Register	Section 8.3.1

Complex bit access types are encoded to fit into small table cells. Table 8-12 shows the codes that are used for access types in this section.

Table 8-12. Device_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1 ALGO_CTRL1 Register (Offset = EAh) [Reset = 00000000h]

ALGO_CTRL1 is shown in Figure 8-7 and described in Table 8-13.

Return to the Summary Table.

Control settings

Figure 8-7. ALGO_CTRL1 Register

31	30	29	28	27	26	25	24
EEPROM_WRT	EEPROM_READ	CLR_FLT	CLR_FLT_RETRY_COUNT	EEPROM_WRITE_ACCESS_KEY			
R/W-0h	R/W-0h	W-0h	W-0h	W-0h			
23	22	21	20	19	18	17	16
EEPROM_WRITE_ACCESS_KEY				FORCED_ALIGN_ANGLE			
W-0h				W-0h			
15	14	13	12	11	10	9	8
FORCED_ALIGN_ANGLE					WATCHDOG_TICKLE	STL_CMD	STL_KEY
W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
STL_KEY							RESERVED
R/W-0h							R-0h

Table 8-13. ALGO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EEPROM_WRT	R/W	0h	Write the configuration from RAM/shadow to EEPROM
30	EEPROM_READ	R/W	0h	Read the default configuration from EEPROM to RAM/shadow
29	CLR_FLT	W	0h	Clears all faults
28	CLR_FLT_RETRY_COUNT	W	0h	Clears automatic fault retry count
27-20	EEPROM_WRITE_ACCESS_KEY	W	0h	EEPROM write access key (0xA5)
19-11	FORCED_ALIGN_ANGLE	W	0h	9-bit value (in degrees) used during forced align state (applicable when FORCE_ALIGN_EN = 0x1) For example if FORCED_ALIGN_ANGLE value is 225 degrees then angle applied during Forced Align will be 225 degrees, similarly if FORCED_ALIGN_ANGLE value is 395 degrees then angle applied during Forced Align will be 395%360 which is 35 degrees Angle applied = (FORCED_ALIGN_ANGLE % 360)deg
10	WATCHDOG_TICKLE	R/W	0h	RAM bit to tickle watchdog in I2C mode. 0x1 should be written to this bit by external controller every EXT_WDT_CFG. Device will reset this bit to 0x0.
9	STL_CMD	R/W	0h	Command to initiate self test (applicable to MCF8315DUL only)
8-1	STL_KEY	R/W	0h	Key(0xBE) to initiate self test on demand (applicable to MCF8315DUL only)
0	RESERVED	R	0h	Reserved

8.4 Algorithm_Control Registers

Table 8-14 lists the memory-mapped registers for the Algorithm_Control registers. All register offset addresses not listed in Table 8-14 should be considered as reserved locations and the register contents should not be modified.

Copyright © 2025 Texas Instruments Incorporated

Table 8-14. ALGORITHM_CONTROL Registers

Offset	Acronym	Register Name	Section
ECh	ALGO_DEBUG1	Algorithm Control Register	Section 8.4.1
EEh	ALGO_DEBUG2	Algorithm Control Register	Section 8.4.2
F0h	CURRENT_PI	Current PI Controller used	Section 8.4.3
F2h	SPEED_PI	Speed PI controller used	Section 8.4.4
F4h	DAC_1	DAC1 Control Register	Section 8.4.5
F6h	DAC_2	DAC2 Control Register	Section 8.4.6
F8h	EEPROM_SECURITY	EEPROM Security Control Register	Section 8.4.7

Complex bit access types are encoded to fit into small table cells. Table 8-15 shows the codes that are used for access types in this section.

Table 8-15. Algorithm_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.4.1 ALGO_DEBUG1 Register (Offset = ECh) [Reset = 00000000h]

ALGO_DEBUG1 is shown in Figure 8-8 and described in Table 8-16.

Return to the Summary Table.

Algorithm control register for debug

Figure 8-8. ALGO_DEBUG1 Register

31	30	29	28	27	26	25	24
OVERRIDE	DIGITAL_SPEED_CTRL						
W-0h	W-0h						
23	22	21	20	19	18	17	16
DIGITAL_SPEED_CTRL							
W-0h							
15	14	13	12	11	10	9	8
CLOSED_LOOP_DIS	FORCE_ALIGN_EN	FORCE_SLOW_FIRST_CYCLE_EN	FORCE_IPD_EN	FORCE_ISD_EN	FORCE_ALIGN_ANGLE_SRC_SEL	RESERVED	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

Table 8-16. ALGO_DEBUG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVERRIDE	W	0h	Use to control the reference input mode. If OVERRIDE = 0x1, speed command can be written by the user through I2C interface irrespective of SPEED_MODE setting. 0h = SPEED_CMD using Analog/PWM/Frequency mode 1h = SPEED_CMD using DIGITAL_SPEED_CTRL
30-16	DIGITAL_SPEED_CTRL	W	0h	Reference input when OVERRIDE is set 0x1 or SPEED_MODE is set to 0x2. Reference input = (DIGITAL_SPEED_CTRL/32768 *100)%
15	CLOSED_LOOP_DIS	W	0h	Use to disable closed loop operation 0h = Enable closed Loop 1h = Disable closed loop, motor commutation in open loop
14	FORCE_ALIGN_EN	W	0h	Enable force align state 0h = Disable force align state 1h = Enable force align state, device stays in align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN
13	FORCE_SLOW_FIRST_CYCLE_EN	W	0h	Enable force slow first cycle 0h = Disable force slow first Cycle state 1h = Enable force slow first cycle state, device stays in slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE
12	FORCE_IPD_EN	W	0h	Enable force IPD 0h = Disable force IPD state 1h = Enable force IPD state, device stays in IPD state if MTR_STARTUP is selected as IPD

Copyright © 2025 Texas Instruments Incorporated

Table 8-16. ALGO_DEBUG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	FORCE_ISD_EN	W	0h	Enable force ISD 0h = Disable force ISD state 1h = Enable force ISD state, device stays in ISD state if ISD_EN is set
10	FORCE_ALIGN_ANGLE_SRC_SEL	W	0h	Select force align angle source 0h = Force align angle defined by ALIGN_ANGLE 1h = Force align angle defined by FORCED_ALIGN_ANGLE
9-0	RESERVED	R	0h	Reserved

Copyright © 2025 Texas Instruments Incorporated

8.4.2 ALGO_DEBUG2 Register (Offset = EEh) [Reset = 00000000h]

ALGO_DEBUG2 is shown in Figure 8-9 and described in Table 8-17.

Return to the Summary Table.

Algorithm control register for debug

Figure 8-9. ALGO_DEBUG2 Register

31	30	29	28	27	26	25	24
RESERVED	FORCE_RECIRCULATE_STOP_SECTOR			FORCE_RECIRCULATE_STOP_EN	CURRENT_LOOP_DIS	FORCE_VD_CURRENT_LOOP_DIS	
R-0h	W-0h			W-0h	W-0h	W-0h	
23	22	21	20	19	18	17	16
FORCE_VD_CURRENT_LOOP_DIS							
W-0h							
15	14	13	12	11	10	9	8
FORCE_VQ_CURRENT_LOOP_DIS							
W-0h							
7	6	5	4	3	2	1	0
FORCE_VQ_CURRENT_LOOP_DIS		MPET_CMD	MPET_R	MPET_L	MPET_KE	MPET_MECH	MPET_WRITE_SHADOW
W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 8-17. ALGO_DEBUG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	FORCE_RECIRCULATE_STOP_SECTOR	W	0h	Select the specific sector for recirculation stop if FORCE_RECIRCULATE_STOP_EN is set to 0x1 0h = The last sector before stop condition 1h = Sector1 2h = Sector2 3h = Sector3 4h = Sector4 5h = Sector5 6h = Sector6 7h = The last sector before stop condition
27	FORCE_RECIRCULATE_STOP_EN	W	0h	Enable force recirculate stop 0h = Enable force recirculate stop 1h = Disable force recirculate stop
26	CURRENT_LOOP_DIS	W	0h	Use to control the FORCE_VD_CURRENT_LOOP_DIS and FORCE_VQ_CURRENT_LOOP_DIS. If CURRENT_LOOP_DIS = 0x1, Current loop and speed loop are disabled 0h = Enable current loop 1h = Disable current loop

Copyright © 2025 Texas Instruments Incorporated

Table 8-17. ALGO_DEBUG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	FORCE_VD_CURRENT_LOOP_DIS	W	0h	Sets Vd when current loop speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vd is control using FORCE_VD_CURRENT_LOOP_DIS mdRef = (FORCE_VD_CURRENT_LOOP_DIS /500) if FORCE_VD_CURRENT_LOOP_DIS < 500 (FORCE_VD_CURRENT_LOOP_DIS - 1024)/500 if FORCE_VD_CURRENT_LOOP_DIS > 512 Valid values: 0 to 500 and 512 to 1000
15-6	FORCE_VQ_CURRENT_LOOP_DIS	W	0h	Sets Vq when current loop speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vq is control using FORCE_VQ_CURRENT_LOOP_DIS mqRef = (FORCE_VQ_CURRENT_LOOP_DIS /500) if FORCE_VQ_CURRENT_LOOP_DIS < 500 (FORCE_VQ_CURRENT_LOOP_DIS - 1024)/500 if FORCE_VQ_CURRENT_LOOP_DIS > 512 Valid values: 0 to 500 and 512 to 1000
5	MPET_CMD	W	0h	Initiates motor parameter measurement (MPET) routine when set to 0x1
4	MPET_R	W	0h	Enables motor resistance measurement during motor parameter measurement routine 0h = Disables Motor Resistance measurement during motor parameter measurement routine 1h = Enable Motor Resistance measurement during motor parameter measurement routine
3	MPET_L	W	0h	Enables motor inductance measurement during motor parameter measurement routine 0h = Disables Motor Inductance measurement during motor parameter measurement routine 1h = Enable Motor Inductance measurement during motor parameter measurement routine
2	MPET_KE	W	0h	Enables motor BEMF constant measurement during motor parameter measurement routine 0h = Disables Motor BEMF constant measurement during motor parameter measurement routine 1h = Enable Motor BEMF constant measurement during motor parameter measurement routine
1	MPET_MECH	W	0h	Enables motor mechanical parameter measurement during motor parameter measurement routine 0h = Disables Motor mechanical parameter measurement during motor parameter measurement routine 1h = Enable Motor mechanical parameter measurement during motor parameter measurement routine
0	MPET_WRITE_SHADOW	W	0h	Write measured parameters to shadow register when set to 0x1

Copyright © 2025 Texas Instruments Incorporated

8.4.3 CURRENT_PI Register (Offset = F0h) [Reset = 00000000h]

CURRENT_PI is shown in Figure 8-10 and described in Table 8-18.

Return to the Summary Table.

Current PI controller used

Figure 8-10. CURRENT_PI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT_LOOP_KI																CURRENT_LOOP_KP															
R-0h																R-0h															

Table 8-18. CURRENT_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CURRENT_LOOP_KI	R	0h	10 bit value for current loop Ki Same Scaling as CURR_LOOP_KI
15-0	CURRENT_LOOP_KP	R	0h	10 bit value for current loop Kp Same Scaling as CURR_LOOP_KP

Copyright © 2025 Texas Instruments Incorporated

8.4.4 SPEED_PI Register (Offset = F2h) [Reset = 00000000h]

SPEED_PI is shown in Figure 8-11 and described in Table 8-19.

Return to the Summary Table.

Speed PI controller used

Figure 8-11. SPEED_PI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_LOOP_KI																SPEED_LOOP_KP															
R-0h																R-0h															

Table 8-19. SPEED_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SPEED_LOOP_KI	R	0h	10 bit value for Speed loop Ki Same Scaling as SPD_LOOP_KI
15-0	SPEED_LOOP_KP	R	0h	10 bit value for Speed loop Kp Same Scaling as SPD_LOOP_KP

Copyright © 2025 Texas Instruments Incorporated

8.4.5 DAC_1 Register (Offset = F4h) [Reset = 00110000h]

DAC_1 is shown in Figure 8-12 and described in Table 8-20.

Return to the Summary Table.

DAC1 Control Register

Figure 8-12. DAC_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED			DACOUT1_ENUM_SCALING				DACOUT1_SCALING
R-0h			W-8h				W-8h
15	14	13	12	11	10	9	8
DACOUT1_SCALING			DACOUT1_UNIPOLAR	DACOUT1_VAR_ADDR			
W-8h			W-0h	R/W-0h			
7	6	5	4	3	2	1	0
DACOUT1_VAR_ADDR							
R/W-0h							

Table 8-20. DAC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-17	DACOUT1_ENUM_SCALING	W	8h	Multiplication Factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR multiplied with $2^{DACOUT1\_ENUM\_SCALING}$. DACOUT1_ENUM_SCALING comes into effect only if DACOUT1_SCALING is 0x0

Copyright © 2025 Texas Instruments Incorporated

Table 8-20. DAC_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-13	DACOUT1_SCALING	W	8h	Scaling factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR scaled with DACOUT1_SCALING. Actual voltage depends on DACOUT1_UNIPOLAR. If DACOUT1_UNIPOLAR = 0x1, Actual Value= ((DAC Voltage*Base Value))/((3* DACOUT1_SCALING)) If DACOUT1_UNIPOLAR = 0x0, Actual Value= (((DAC Voltage-1.5)*Base Value))/((1.5* DACOUT1_SCALING)) Base Current is 6.25/8 A, Base Speed is MAX_SPEED in Hz, Base Voltage for DC Bus Voltage is 60V, Base voltage for phase voltages is 60V/Sqrt(3) Note: For currents recommended DACOUT1_SCALING is 2/8, for Voltages 8/8 and for Speed 7/8 0h = Treated s Enum with max value being 31 1h = 1 / 8 2h = 2 / 8 3h = 3 / 8 4h = 4 / 8 5h = 5 / 8 6h = 6 / 8 7h = 7 / 8 8h = 8 / 8 9h = 9 / 8 Ah = 10 / 8 Bh = 11 / 8 Ch = 12 / 8 Dh = 13 / 8 Eh = 14 / 8 Fh = 15 / 8
12	DACOUT1_UNIPOLAR	W	0h	Configures output of DACOUT1 If DACOUT1_UNIPOLAR = 0x1, Actual Value= ((DAC1 Voltage*Base Value))/((3* DACOUT1_SCALING)) If DACOUT1_UNIPOLAR = 0x0, Actual Value= (((DAC2 Voltage-1.5)*Base Value))/((1.5* DACOUT1_SCALING)) Base Current is 6.25/8 A, Base Speed is MAX_SPEED in Hz, Base Voltage for DC Bus Voltage is 60V, Base voltage for phase voltages is 60V/Sqrt(3) 0h = Bipolar (Offset of 1.5 V) 1h = Unipolar (No Offset)
11-0	DACOUT1_VAR_ADDR	R/W	0h	12-bit address of variable to be monitored on DACOUT1

Copyright © 2025 Texas Instruments Incorporated

8.4.6 DAC_2 Register (Offset = F6h) [Reset = 00XX0000h]

DAC_2 is shown in Figure 8-13 and described in Table 8-21.

Return to the Summary Table.

DAC2 Control Register

Figure 8-13. DAC_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED	DACOUT2_ENUM_SCALING				DACOUT2_SCALING		
R-0h	W-Xh				W-8h		
15	14	13	12	11	10	9	8
DACOUT2_SCALING	DACOUT2_UNIPOLAR	DACOUT2_VAR_ADDR					
W-8h	W-0h	R/W-0h					
7	6	5	4	3	2	1	0
DACOUT2_VAR_ADDR							
R/W-0h							

Table 8-21. DAC_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-19	DACOUT2_ENUM_SCALING	W	Xh	Multiplication Factor for DACOUT2 Algorithm Variable extracted from the address contained in DACOUT2_VAR_ADDR multiplied with $2^{DACOUT2\_ENUM\_SCALING}$. DACOUT2_ENUM_SCALING comes into effect only if DACOUT2_SCALING is 0x0

Copyright © 2025 Texas Instruments Incorporated

Table 8-21. DAC_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	DACOUT2_SCALING	W	8h	Scaling factor for DACOUT2 Algorithm Variable extracted from the address contained in DACOUT2_VAR_ADDR scaled with DACOUT2_SCALING . Actual voltage depends on DACOUT2_UNIPOLAR. If DACOUT2_UNIPOLAR = 0x1, Actual Value= ((DAC2 Voltage*Base Value))/((3* DACOUT2_SCALING)) If DACOUT2_UNIPOLAR = 0x0, Actual Value= (((DAC2 Voltage-1.5)*Base Value))/((1.5* DACOUT2_SCALING)) Base Current is 6.25/8 A, Base Speed is MAX_SPEED in Hz, Base Voltage for DC Bus Voltage is 60V, Base voltage for phase voltages is 60V/Sqrt(3) Note: For currents recommended DACOUT1_SCALING is 2/8, for Voltages 8/8 and for Speed information 7/8 0h = Treated s Enum with max value being 31 1h = 1 / 8 2h = 2 / 8 3h = 3 / 8 4h = 4 / 8 5h = 5 / 8 6h = 6 / 8 7h = 7 / 8 8h = 8 / 8 9h = 9 / 8 Ah = 10 / 8 Bh = 11 / 8 Ch = 12 / 8 Dh = 13 / 8 Eh = 14 / 8 Fh = 15 / 8
14	DACOUT2_UNIPOLAR	W	0h	Configures output of DACOUT2 If DACOUT2_UNIPOLAR = 0x1, Actual Value= ((DAC2 Voltage*Base Value))/((3* DACOUT2_SCALING)) If DACOUT2_UNIPOLAR = 0x0, Actual Value= (((DAC2 Voltage-1.5)*Base Value))/((1.5* DACOUT2_SCALING)) Base Current is 6.25/8 A, Base Speed is MAX_SPEED in Hz, Base Voltage for DC Bus Voltage is 60V, Base voltage for phase voltages is 60V/Sqrt(3) Note: For currents recommended DACOUT1_SCALING is 2/8, for Voltages 8/8 and for Speed information 7/8 0h = Bipolar (Offset of 1.5 V) 1h = Unipolar (No Offset)
13-0	DACOUT2_VAR_ADDR	R/W	0h	14-bit address of variable to be monitored on DACOUT2

Copyright © 2025 Texas Instruments Incorporated

8.4.7 EEPROM_SECURITY Register (Offset = F8h) [Reset = 0000h]

EEPROM_SECURITY is shown in Figure 8-14 and described in Table 8-22.

Return to the Summary Table.

EEPROM Security Control Register

Figure 8-14. EEPROM_SECURITY Register

15	14	13	12	11	10	9	8
RESERVED	USER_EEPROM_KEY						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
USER_EEPROM_KEY							
R/W-0h							

Table 8-22. EEPROM_SECURITY Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-0	USER_EEPROM_KEY	R/W	0h	User input key to unlock EEPROM for read/writes. Value in EEPROM_LOCK_KEY should be written here for unlocking EEPROM

8.5 Algorithm_Variables Registers

Table 8-23 lists the memory-mapped registers for the Algorithm_Variables registers. All register offset addresses not listed in Table 8-23 should be considered as reserved locations and the register contents should not be modified.

Table 8-23. ALGORITHM_VARIABLES Registers

Offset	Acronym	Register Name	Section
18Eh	ALGORITHM_STATE	Current Algorithm State Register	Section 8.5.1
194h	FG_SPEED_FDBK	FG Speed Feedback Register	Section 8.5.2
400h	VBETA	VBETA Voltage Register	Section 8.5.3
40Ch	BUS_CURRENT	Calculated DC Bus Current Register	Section 8.5.4
444h	PHASE_CURRENT_A	Measured Current on Phase A Register	Section 8.5.5
446h	PHASE_CURRENT_B	Measured Current on Phase B Register	Section 8.5.6
448h	PHASE_CURRENT_C	Measured Current on Phase C Register	Section 8.5.7
46Ch	CSA_GAIN_FEEDBACK	CSA Gain Register	Section 8.5.8
477h	VOLTAGE_GAIN_FEEDBACK	Voltage Gain Register	Section 8.5.9
47Ch	VM_VOLTAGE	VM Voltage Register	Section 8.5.10
484h	PHASE_VOLTAGE_VA	Phase A Voltage Register	Section 8.5.11
486h	PHASE_VOLTAGE_VB	Phase B Voltage Register	Section 8.5.12
488h	PHASE_VOLTAGE_VC	Phase C Voltage Register	Section 8.5.13
4BCh	SIN_COMMUTATION_ANGLE	Sine of Commutation Angle	Section 8.5.14
4BEh	COS_COMMUTATION_ANGLE	Cosine of Commutation Angle	Section 8.5.15
4DCh	IALPHA	IALPHA Current Register	Section 8.5.16
4DEh	IBETA	IBETA Current Register	Section 8.5.17
4E0h	VALPHA	VALPHA Voltage Register	Section 8.5.18
4ECh	ID	Measured d-axis Current Register	Section 8.5.19
4EEh	IQ	Measured q-axis Current Register	Section 8.5.20
4F0h	VD	VD Voltage Register	Section 8.5.21

Copyright © 2025 Texas Instruments Incorporated

Table 8-23. ALGORITHM_VARIABLES Registers (continued)

Offset	Acronym	Register Name	Section
4F2h	VQ	VQ Voltage Register	Section 8.5.22
52Ah	IQ_REF_ROTOR_ALIGN	Align Current Reference	Section 8.5.23
540h	SPEED_REF_OPEN_LOOP	Open Loop Speed Register	Section 8.5.24
550h	IQ_REF_OPEN_LOOP	Open Loop Current Reference	Section 8.5.25
5D2h	SPEED_REF_CLOSED_LOOP	Speed Reference Register	Section 8.5.26
612h	ID_REF_CLOSED_LOOP	Reference for Current Loop Register	Section 8.5.27
614h	IQ_REF_CLOSED_LOOP	Reference for Current Loop Register	Section 8.5.28
6AEh	ISD_STATE	ISD State Register	Section 8.5.29
6B8h	ISD_SPEED	ISD Speed Register	Section 8.5.30
6EAh	IPD_STATE	IPD State Register	Section 8.5.31
72Eh	IPD_ANGLE	Calculated IPD Angle Register	Section 8.5.32
772h	ED	Estimated BEMF EQ Register	Section 8.5.33
774h	EQ	Estimated BEMF ED Register	Section 8.5.34
782h	SPEED_FDBK	Speed Feedback Register	Section 8.5.35
786h	THETA_EST	Estimated rotor Position Register	Section 8.5.36

Complex bit access types are encoded to fit into small table cells. Table 8-24 shows the codes that are used for access types in this section.

Table 8-24. Algorithm_Variables Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

Copyright © 2025 Texas Instruments Incorporated

8.5.1 ALGORITHM_STATE Register (Offset = 18Eh) [Reset = 0000h]

ALGORITHM_STATE is shown in Figure 8-15 and described in Table 8-25.

Return to the Summary Table.

Current Algorithm State Register

Figure 8-15. ALGORITHM_STATE Register

15	14	13	12	11	10	9	8
ALGORITHM_STATE							
R-0h							
7	6	5	4	3	2	1	0
ALGORITHM_STATE							
R-0h							

Table 8-25. ALGORITHM_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ALGORITHM_STATE	R	0h	16-bit value indicating current state of device 0h = MOTOR_IDLE 1h = MOTOR_ISD 2h = MOTOR_TRISTATE 3h = MOTOR_BRAKE_ON_START 4h = MOTOR_IPD 5h = MOTOR_SLOW_FIRST_CYCLE 6h = MOTOR_ALIGN 7h = MOTOR_OPEN_LOOP 8h = MOTOR_CLOSED_LOOP_UNALIGNED 9h = MOTOR_CLOSED_LOOP_ALIGNED Ah = MOTOR_CLOSED_LOOP_ACTIVE_BRAKING Bh = MOTOR_SOFT_STOP Ch = MOTOR_RECIRCULATE_STOP Dh = MOTOR_BRAKE_ON_STOP Eh = MOTOR_FAULT Fh = MOTOR_MPET_MOTOR_STOP_CHECK 10h = MOTOR_MPET_MOTOR_STOP_WAIT 11h = MOTOR_MPET_MOTOR_BRAKE 12h = MOTOR_MPET_ALGORITHM_PARAMETERS_INIT 13h = MOTOR_MPET_RL_MEASURE 14h = MOTOR_MPET_KE_MEASURE 15h = MOTOR_MPET_STALL_CURRENT_MEASURE 16h = MOTOR_MPET_TORQUE_MODE 17h = MOTOR_MPET_DONE 18h = MOTOR_MPET_FAULT

Copyright © 2025 Texas Instruments Incorporated

8.5.2 FG_SPEED_FDBK Register (Offset = 194h) [Reset = 00000000h]

FG_SPEED_FDBK is shown in Figure 8-16 and described in Table 8-26.

Return to the Summary Table.

Speed Feedback from FG

Figure 8-16. FG_SPEED_FDBK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FG_SPEED_FDBK																															
R-0h																															

Table 8-26. FG_SPEED_FDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FG_SPEED_FDBK	R	0h	32-bit value indicating absolute (unsigned) value of estimated motor speed based on FG Estimated Motor Speed (in Hz) = (FG_SPEED_FDBK / 2^{27}) * MAX_SPEED (in Hz)

Copyright © 2025 Texas Instruments Incorporated

8.5.3 VBETA Register (Offset = 400h) [Reset = 00000000h]

VBETA is shown in Figure 8-17 and described in Table 8-27.

Return to the Summary Table.

VBETA Voltage Register

Figure 8-17. VBETA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBETA																															
R-0h																															

Table 8-27. VBETA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VBETA	R	0h	32-bit signed value indicating applied phase voltage in alpha-beta domain. Negative value represented in two's complement. VBeta (in Volts)) = (VBETA / 2^{27}) * 60 / sqrt(3)

Copyright © 2025 Texas Instruments Incorporated

8.5.4 BUS_CURRENT Register (Offset = 40Ch) [Reset = 00000000h]

BUS_CURRENT is shown in Figure 8-18 and described in Table 8-28.

Return to the Summary Table.

Calculated Supply Current Register

Figure 8-18. BUS_CURRENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUS_CURRENT																															
R-0h																															

Table 8-28. BUS_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUS_CURRENT	R	0h	32-bit signed value indicating DC bus current. Negative value represented in two's complement. DC bus Current (in Amps) = (BUS_CURRENT / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.5 PHASE_CURRENT_A Register (Offset = 444h) [Reset = 00000000h]

PHASE_CURRENT_A is shown in Figure 8-19 and described in Table 8-29.

Return to the Summary Table.

Measured current on Phase A Register

Figure 8-19. PHASE_CURRENT_A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_A																															
R-0h																															

Table 8-29. PHASE_CURRENT_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_A	R	0h	32-bit signed value indicating measured continuous Phase A current. Negative value represented in two's complement. Phase A current (in Amps) = (PHASE_CURRENT_A / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.6 PHASE_CURRENT_B Register (Offset = 446h) [Reset = 00000000h]

PHASE_CURRENT_B is shown in Figure 8-20 and described in Table 8-30.

Return to the Summary Table.

Measured current on Phase B Register

Figure 8-20. PHASE_CURRENT_B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_B																															
R-0h																															

Table 8-30. PHASE_CURRENT_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_B	R	0h	32-bit signed value indicating measured continuous Phase B current. Negative value represented in two's complement. Phase B current (in Amps) = (PHASE_CURRENT_B / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.7 PHASE_CURRENT_C Register (Offset = 448h) [Reset = 00000000h]

PHASE_CURRENT_C is shown in Figure 8-21 and described in Table 8-31.

Return to the Summary Table.

Measured current on Phase C Register

Figure 8-21. PHASE_CURRENT_C Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_CURRENT_C																															
R-0h																															

Table 8-31. PHASE_CURRENT_C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_C	R	0h	32-bit signed value indicating measured continuous Phase C current. Negative value represented in two's complement. Phase C current (in Amps) = (PHASE_CURRENT_C / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.8 CSA_GAIN_FEEDBACK Register (Offset = 46Ch) [Reset = 0000h]

CSA_GAIN_FEEDBACK is shown in Figure 8-22 and described in Table 8-32.

Return to the Summary Table.

VM Voltage Register

Figure 8-22. CSA_GAIN_FEEDBACK Register

15	14	13	12	11	10	9	8
CSA_GAIN_FEEDBACK							
R-0h							
7	6	5	4	3	2	1	0
CSA_GAIN_FEEDBACK							
R-0h							

Table 8-32. CSA_GAIN_FEEDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CSA_GAIN_FEEDBACK	R	0h	16-bit value indicating current sense gain. MIN_CSA_GAIN = 0.24V/A 0h = MIN_CSA_GAIN * 8 1h = MIN_CSA_GAIN * 4 2h = MIN_CSA_GAIN * 2 3h = MIN_CSA_GAIN * 1

Copyright © 2025 Texas Instruments Incorporated

8.5.9 VOLTAGE_GAIN_FEEDBACK Register (Offset = 477h) [Reset = 0000h]

VOLTAGE_GAIN_FEEDBACK is shown in Figure 8-23 and described in Table 8-33.

Return to the Summary Table.

Voltage Gain Register

Figure 8-23. VOLTAGE_GAIN_FEEDBACK Register

15	14	13	12	11	10	9	8
VOLTAGE_GAIN_FEEDBACK							
R-0h							
7	6	5	4	3	2	1	0
VOLTAGE_GAIN_FEEDBACK							
R-0h							

Table 8-33. VOLTAGE_GAIN_FEEDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VOLTAGE_GAIN_FEEDBACK	R	0h	16-bit value indicating voltage gain 0h = 40V 1h = 30V 2h = 15V

Copyright © 2025 Texas Instruments Incorporated

8.5.10 VM_VOLTAGE Register (Offset = 47Ch) [Reset = 00000000h]

VM_VOLTAGE is shown in Figure 8-24 and described in Table 8-34.

Return to the Summary Table.

Supply voltage register

Figure 8-24. VM_VOLTAGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VM_VOLTAGE																															
R-0h																															

Table 8-34. VM_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VM_VOLTAGE	R	0h	32-bit value indicating DC bus voltage DC Bus Voltage (in Volts) = VM_VOLTAGE * 60 / 2^{27}

Copyright © 2025 Texas Instruments Incorporated

8.5.11 PHASE_VOLTAGE_VA Register (Offset = 484h) [Reset = 00000000h]

PHASE_VOLTAGE_VA is shown in Figure 8-25 and described in Table 8-35.

Return to the Summary Table.

Phase A Voltage Register

Figure 8-25. PHASE_VOLTAGE_VA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VA																															
R-0h																															

Table 8-35. PHASE_VOLTAGE_VA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VA	R	0h	32-bit signed value indicating measured A phase voltage during ISD. Negative value represented in two's complement. Phase A voltage (in Volts) = PHASE_VOLTAGE_VA * 60 / (sqrt(3) * 2^{27})

Copyright © 2025 Texas Instruments Incorporated

8.5.12 PHASE_VOLTAGE_VB Register (Offset = 486h) [Reset = 00000000h]

PHASE_VOLTAGE_VB is shown in Figure 8-26 and described in Table 8-36.

Return to the Summary Table.

Phase B Voltage Register

Figure 8-26. PHASE_VOLTAGE_VB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VB																															
R-0h																															

Table 8-36. PHASE_VOLTAGE_VB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VB	R	0h	32-bit signed value indicating measured B phase voltage during ISD. Negative value represented in two's complement. Phase B voltage (in Volts) = PHASE_VOLTAGE_VB * 60 / (sqrt(3) * 2^{27})

Copyright © 2025 Texas Instruments Incorporated

8.5.13 PHASE_VOLTAGE_VC Register (Offset = 488h) [Reset = 00000000h]

PHASE_VOLTAGE_VC is shown in Figure 8-27 and described in Table 8-37.

Return to the Summary Table.

Phase C Voltage Register

Figure 8-27. PHASE_VOLTAGE_VC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHASE_VOLTAGE_VC																															
R-0h																															

Table 8-37. PHASE_VOLTAGE_VC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VC	R	0h	32-bit signed value indicating measured C phase voltage during ISD. Negative value represented in two's complement. Phase C voltage (in Volts) = PHASE_VOLTAGE_VC * 60 / (sqrt(3) * 2^{27})

Copyright © 2025 Texas Instruments Incorporated

8.5.14 SIN_COMMUTATION_ANGLE Register (Offset = 4BCh) [Reset = 00000000h]

SIN_COMMUTATION_ANGLE is shown in Figure 8-28 and described in Table 8-38.

Return to the Summary Table.

Sine of Commutation Angle

Figure 8-28. SIN_COMMUTATION_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIN_COMMUTATION_ANGLE																															
R-0h																															

Table 8-38. SIN_COMMUTATION_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SIN_COMMUTATION_ANGLE	R	0h	32-bit signed value indicating sine of rotor Angle. Negative value represented in two's complement. sin(rotor angle) = (SIN_COMMUTATION_ANGLE / 2^{27})

Copyright © 2025 Texas Instruments Incorporated

8.5.15 COS_COMMUTATION_ANGLE Register (Offset = 4BEh) [Reset = 00000000h]

COS_COMMUTATION_ANGLE is shown in Figure 8-29 and described in Table 8-39.

Return to the Summary Table.

Cosine of Commutation Angle

Figure 8-29. COS_COMMUTATION_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COS_COMMUTATION_ANGLE																															
R-0h																															

Table 8-39. COS_COMMUTATION_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COS_COMMUTATION_ANGLE	R	0h	32-bit signed value indicating cosine of rotor angle. Negative value represented in two's complement. cos(rotor angle) = (COS_COMMUTATION_ANGLE / 2^{27})

Copyright © 2025 Texas Instruments Incorporated

8.5.16 IALPHA Register (Offset = 4DCh) [Reset = 00000000h]

IALPHA is shown in Figure 8-30 and described in Table 8-40.

Return to the Summary Table.

IALPHA Current Register

Figure 8-30. IALPHA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IALPHA																															
R-0h																															

Table 8-40. IALPHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IALPHA	R	0h	32-bit signed value indicating phase current in alpha- beta domain. Negative value represented in two's complement. IAlpha (in Amps) = (IALPHA / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.17 IBETA Register (Offset = 4DEh) [Reset = 00000000h]

IBETA is shown in Figure 8-31 and described in Table 8-41.

Return to the Summary Table.

IBETA Current Register

Figure 8-31. IBETA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IBETA																															
R-0h																															

Table 8-41. IBETA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IBETA	R	0h	32-bit signed value indicating phase current in alpha- beta domain. Negative value represented in two's complement. IBeta (in Amps) = (IBETA / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.18 VALPHA Register (Offset = 4E0h) [Reset = 00000000h]

VALPHA is shown in Figure 8-32 and described in Table 8-42.

Return to the Summary Table.

VALPHA Voltage Register

Figure 8-32. VALPHA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALPHA																															
R-0h																															

Table 8-42. VALPHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALPHA	R	0h	32-bit signed value indicating applied phase voltage in alpha-beta domain VAlpha (in Volts) = (VALPHA / 2^{27}) * 60 / sqrt(3)

Copyright © 2025 Texas Instruments Incorporated

8.5.19 ID Register (Offset = 4ECh) [Reset = 00000000h]

ID is shown in Figure 8-33 and described in Table 8-43.

Return to the Summary Table.

Measured d-axis Current Register

Figure 8-33. ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															
R-0h																															

Table 8-43. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID	R	0h	32-bit signed value indicating d-axis(flux component) phase current in d-q domain. Negative value represented in two's complement. Flux component phase current (in Amps) = (ID / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.20 IQ Register (Offset = 4EEh) [Reset = 00000000h]

IQ is shown in Figure 8-34 and described in Table 8-44.

Return to the Summary Table.

Measured q-axis Current Register

Figure 8-34. IQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ																															
R-0h																															

Table 8-44. IQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ	R	0h	32-bit signed value indicating q-axis(torque component) phase current in d-q domain. Negative value represented in two's complement. Torque component phase current (in Amps) = (IQ / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.21 VD Register (Offset = 4F0h) [Reset = 00000000h]

VD is shown in Figure 8-35 and described in Table 8-45.

Return to the Summary Table.

VD Voltage Register

Figure 8-35. VD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VD																															
R-0h																															

Table 8-45. VD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VD	R	0h	32-bit signed value indicating applied phase voltage in d-q domain. Negative value represented in two's complement. Vd (in Volts) = (VD / 2^{27}) * 60 / sqrt(3)

Copyright © 2025 Texas Instruments Incorporated

8.5.22 VQ Register (Offset = 4F2h) [Reset = 00000000h]

VQ is shown in Figure 8-36 and described in Table 8-46.

Return to the Summary Table.

VQ Voltage Register

Figure 8-36. VQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VQ																															
R-0h																															

Table 8-46. VQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VQ	R	0h	32-bit signed value indicating applied phase voltage in d-q domain. Negative value represented in two's complement. Vq (in Volts) = (VQ / 2^{27}) * 60 / sqrt(3)

Copyright © 2025 Texas Instruments Incorporated

8.5.23 IQ_REF_ROTOR_ALIGN Register (Offset = 52Ah) [Reset = 00000000h]

IQ_REF_ROTOR_ALIGN is shown in Figure 8-37 and described in Table 8-47.

Return to the Summary Table.

Align Current Reference

Figure 8-37. IQ_REF_ROTOR_ALIGN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_ROTOR_ALIGN																															
R-0h																															

Table 8-47. IQ_REF_ROTOR_ALIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_ROTOR_ALIGN	R	0h	32-bit signed value indicating current reference during align state. Negative value represented in two's complement. Current reference during Align State (in Amps) = (IQ_REF_ROTOR_ALIGN / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.24 SPEED_REF_OPEN_LOOP Register (Offset = 540h) [Reset = 00000000h]

SPEED_REF_OPEN_LOOP is shown in Figure 8-38 and described in Table 8-48.

Return to the Summary Table.

Speed at which motor transitions to close loop

Figure 8-38. SPEED_REF_OPEN_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_REF_OPEN_LOOP																															
R-0h																															

Table 8-48. SPEED_REF_OPEN_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_OPEN_LOOP	R	0h	32-bit signed value indicating open loop speed reference. Negative value represented in two's complement. Speed reference during open loop (in Hz) = (SPEED_REF_OPEN_LOOP / 2^{27}) * MAX_SPEED (in Hz)

Copyright © 2025 Texas Instruments Incorporated

8.5.25 IQ_REF_OPEN_LOOP Register (Offset = 550h) [Reset = 00000000h]

IQ_REF_OPEN_LOOP is shown in Figure 8-39 and described in Table 8-49.

Return to the Summary Table.

Open Loop Current Reference

Figure 8-39. IQ_REF_OPEN_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_OPEN_LOOP																															
R-0h																															

Table 8-49. IQ_REF_OPEN_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_OPEN_LOOP	R	0h	32-bit signed value indicating current reference during open loop. Negative value represented in two's complement. Current reference during open loop (in Amps) = (IQ_REF_OPEN_LOOP / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.26 SPEED_REF_CLOSED_LOOP Register (Offset = 5D2h) [Reset = 00000000h]

SPEED_REF_CLOSED_LOOP is shown in Figure 8-40 and described in Table 8-50.

Return to the Summary Table.

Speed Reference Register

Figure 8-40. SPEED_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_REF_CLOSED_LOOP																															
R-0h																															

Table 8-50. SPEED_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_CLOSED_LOOP	R	0h	32-bit signed value indicating reference for closed loop. Negative value represented in two's complement. In speed control mode, speed reference in closed loop (in Hz)= (SPEED_REF_CLOSED_LOOP/ 2^{27}) * MAX_SPEED (in Hz). In power mode, power reference in closed loop (in Watts) = (SPEED_REF_CLOSED_LOOP/ 2^{27}) * MAX_POWER (in Watts) In current mode, Iq current reference in closed loop (in Amps) = (SPEED_REF_CLOSED_LOOP / 2^{27}) * ILIMIT(in Amps)

Copyright © 2025 Texas Instruments Incorporated

8.5.27 ID_REF_CLOSED_LOOP Register (Offset = 612h) [Reset = 00000000h]

ID_REF_CLOSED_LOOP is shown in Figure 8-41 and described in Table 8-51.

Return to the Summary Table.

Reference for Current Loop Register

Figure 8-41. ID_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID_REF_CLOSED_LOOP																															
R-0h																															

Table 8-51. ID_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID_REF_CLOSED_LOOP	R	0h	32-bit signed value indicating d-axis(flux component) phase current reference in closed loop . Negative value represented in two's complement. Flux component phase current reference in closed loop (in Amps) = (ID / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.28 IQ_REF_CLOSED_LOOP Register (Offset = 614h) [Reset = 00000000h]

IQ_REF_CLOSED_LOOP is shown in Figure 8-42 and described in Table 8-52.

Return to the Summary Table.

Reference for Current Loop Register

Figure 8-42. IQ_REF_CLOSED_LOOP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IQ_REF_CLOSED_LOOP																															
R-0h																															

Table 8-52. IQ_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_CLOSED_LOOP	R	0h	32-bit signed value indicating q-axis(torque component) phase current reference in closed loop. Negative value represented in two's complement. Torque component phase current reference in closed loop (in Amps) = (IQ / 2^{27}) * 6.25/8

Copyright © 2025 Texas Instruments Incorporated

8.5.29 ISD_STATE Register (Offset = 6AEh) [Reset = 0000h]

ISD_STATE is shown in Figure 8-43 and described in Table 8-53.

Return to the Summary Table.

ISD state Register

Figure 8-43. ISD_STATE Register

15	14	13	12	11	10	9	8
ISD_STATE							
R-0h							
7	6	5	4	3	2	1	0
ISD_STATE							
R-0h							

Table 8-53. ISD_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ISD_STATE	R	0h	16-bit value indicating current ISD state 0h = ISD_INIT 1h = ISD_MOTOR_STOP_CHECK 2h = ISD_ESTIM_INIT 3h = ISD_RUN_MOTOR_CHECK 4h = ISD_MOTOR_DIRECTION_CHECK 5h = ISD_COMPLETE 6h = ISD_FAULT

Copyright © 2025 Texas Instruments Incorporated

8.5.30 ISD_SPEED Register (Offset = 6B8h) [Reset = 00000000h]

ISD_SPEED is shown in Figure 8-44 and described in Table 8-54.

Return to the Summary Table.

ISD Speed Register

Figure 8-44. ISD_SPEED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISD_SPEED																															
R-0h																															

Table 8-54. ISD_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ISD_SPEED	R	0h	32-bit value indicating calculated absolute speed during ISD state Speed estimated during ISD (in Hz) = (ISD_SPEED / 2^{27}) * MAX_SPEED (in Hz)

Copyright © 2025 Texas Instruments Incorporated

8.5.31 IPD_STATE Register (Offset = 6EAh) [Reset = 0000h]

IPD_STATE is shown in Figure 8-45 and described in Table 8-55.

Return to the Summary Table.

IPD state Register

Figure 8-45. IPD_STATE Register

15	14	13	12	11	10	9	8
IPD_STATE							
R-0h							
7	6	5	4	3	2	1	0
IPD_STATE							
R-0h							

Table 8-55. IPD_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IPD_STATE	R	0h	16-bit value indicating current IPD state 0h = IPD_INIT 1h = IPD_VECTOR_CONFIG 2h = IPD_RUN 3h = IPD_SLOW_RISE_CLOCK 4h = IPD_SLOW_FALL_CLOCK 5h = IPD_WAIT_CURRENT_DECAY 6h = IPD_GET_TIMES 7h = IPD_SET_NEXT_VECTOR 8h = IPD_CALC_SECTOR_RISE 9h = IPD_CALC_ROTOR_POSITION Ah = IPD_CALC_ANGLE Bh = IPD_COMPLETE Ch = IPD_FAULT

Copyright © 2025 Texas Instruments Incorporated

8.5.32 IPD_ANGLE Register (Offset = 72Eh) [Reset = 00000000h]

IPD_ANGLE is shown in Figure 8-46 and described in Table 8-56.

Return to the Summary Table.

Calculated IPD Angle Register

Figure 8-46. IPD_ANGLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPD_ANGLE																															
R-0h																															

Table 8-56. IPD_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPD_ANGLE	R	0h	32-bit signed value indicating measured IPD angle. Negative value represented in two's complement. IPD Angle (in degrees) = (IPD_ANGLE / 2^{27}) * 360

8.5.33 ED Register (Offset = 772h) [Reset = 00000000h]

ED is shown in Figure 8-47 and described in Table 8-57.

Return to the Summary Table.

Estimated BEMF EQ Register

Figure 8-47. ED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ED																															
R-0h																															

Table 8-57. ED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ED	R	0h	32-bit signed value indicating estimated Back EMF along the D-Axis (Ed). Negative value represented in two's complement. Ed (in Volts) = (ED / 2^{27}) * 60 / sqrt(3)

Copyright © 2025 Texas Instruments Incorporated

8.5.34 EQ Register (Offset = 774h) [Reset = 00000000h]

EQ is shown in Figure 8-48 and described in Table 8-58.

Return to the Summary Table.

Estimated BEMF ED Register

Figure 8-48. EQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EQ																															
R-0h																															

Table 8-58. EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EQ	R	0h	32-bit signed value indicating estimated Back EMF along the Q-Axis (Eq). Negative value represented in two's complement. Eq (in Volts) = (EQ / 2^{27}) * 60 / sqrt(3)

Copyright © 2025 Texas Instruments Incorporated

8.5.35 SPEED_FDBK Register (Offset = 782h) [Reset = 00000000h]

SPEED_FDBK is shown in Figure 8-49 and described in Table 8-59.

Return to the Summary Table.

Speed Feedback Register

Figure 8-49. SPEED_FDBK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPEED_FDBK																															
R-0h																															

Table 8-59. SPEED_FDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_FDBK	R	0h	32-bit signed value indicating estimated motor speed. Negative value represented in two's complement. Estimated Motor Speed (in Hz) = (SPEED_FDBK / 2^{27}) * MAX_SPEED (in Hz)

Copyright © 2025 Texas Instruments Incorporated

8.5.36 THETA_EST Register (Offset = 786h) [Reset = 00000000h]

THETA_EST is shown in Figure 8-50 and described in Table 8-60.

Return to the Summary Table.

Estimated rotor Position Register

Figure 8-50. THETA_EST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THETA_EST																															
R-0h																															

Table 8-60. THETA_EST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	THETA_EST	R	0h	32-bit signed value indicating estimated rotor angle. Angle should be modulo 360 degrees. For example if the estimated Angle value 380 degrees then it means 380%360 = 20 degrees Estimated rotor Angle (in degrees) = (THETA_EST / 2^{27})*360

Copyright © 2025 Texas Instruments Incorporated

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The MCF8315D device is used in sensorless 3-phase BLDC motor control. The driver provides a high performance, high-reliability, flexible solution for appliances, fans, pumps, residential and living fans, seat cooling fans, automotive fans and blowers. The following section shows a common application of the MCF8315D device.

9.2 Typical Applications

Figure 9-1 shows the typical schematic of MCF8315D.

Copyright © 2025 Texas Instruments Incorporated

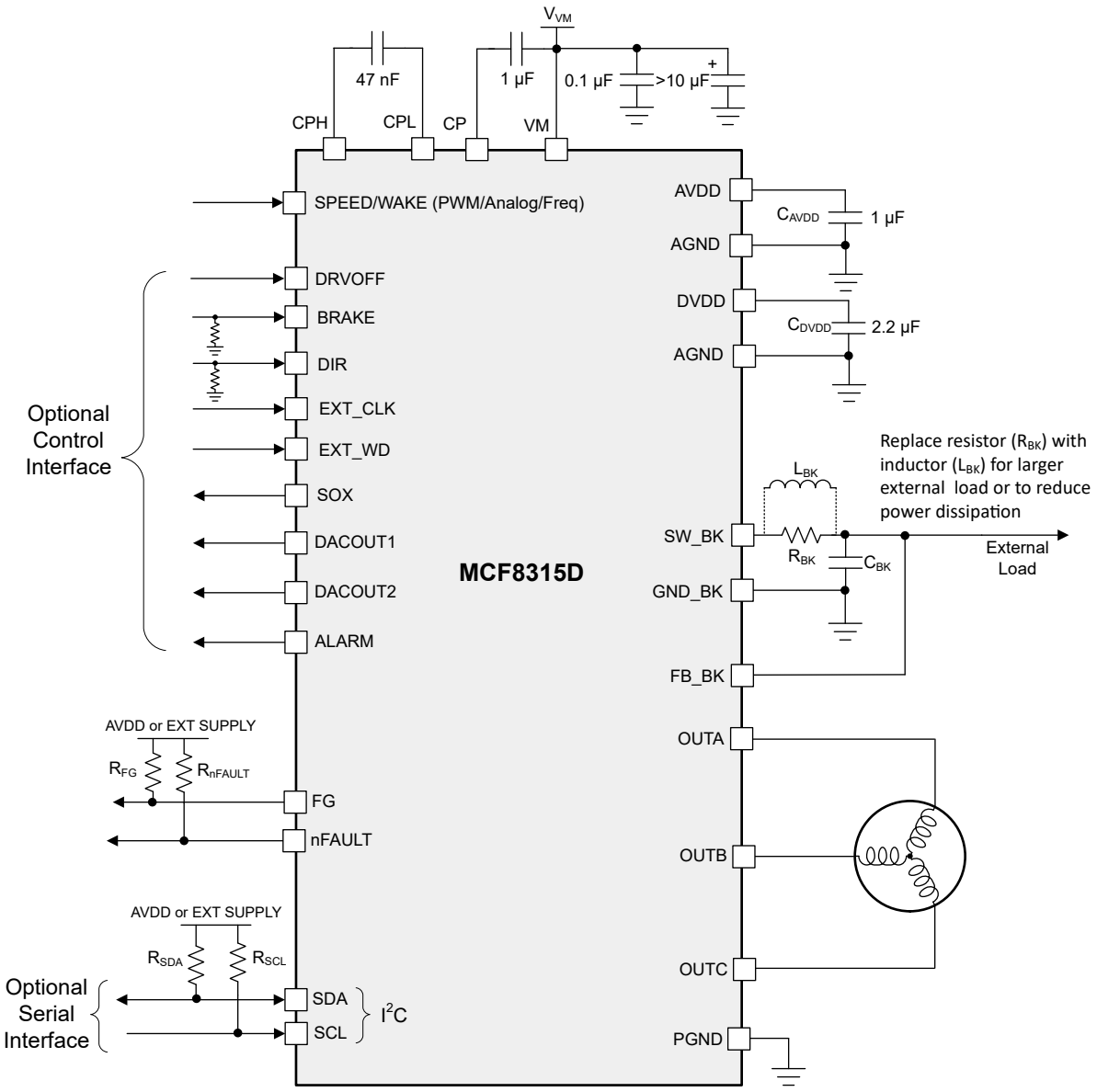


Figure 9-1. Example Applications Schematic

Note

- DAC output(s) are available in RGF and RRY packages only. In PWP package, internal variables can be monitored over I^2C.
- ALARM and DIR pins are available in RGF and RRY packages only. In PWP package, direction can be changed using DIR_INPUT bitfield in PERI_CONFIG1 register.
- SOX output is available only in RGF package. In RRY and PWP packages, phase currents can be monitored over I^2C.

Table 9-1 lists the recommended values of the external components for MCF8315D.

Table 9-1. MCF8315D External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X7R, 0.1µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device

Copyright © 2025 Texas Instruments Incorporated

Table 9-1. MCF8315D External Components (continued)

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM2}	VM	PGND	≥ 10µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{CP}	CP	VM	X7R, 16V, 1µF capacitor
C_{FLY}	CPH	CPL	X7R, 47nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin
C_{AVDD}	AVDD	AGND	X7R, 1µF, ≥ 10V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7µF to 1.3µF at 3.3V across operating temperature.
C_{DVDD}	DVDD	DGND	X7R, 1µF, ≥ 6.3V. In order for DVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7µF to 2.5µF at 1.5V across operating temperature.
C_{BK}	FB_BK	GND_BK	X7R, buck-output rated capacitor
L_{BK}	SW_BK	FB_BK	Buck-output inductor
R_{FG}	1.8 to 5V Supply	FG	5.1kΩ, Pull-up resistor
R_{nFAULT}	1.8 to 5V Supply	nFAULT	5.1kΩ, Pull-up resistor
R_{SDA}	1.8 to 3.3V Supply	SDA	5.1kΩ, Pull-up resistor
R_{SCL}	1.8 to 3.3V Supply	SCL	5.1kΩ, Pull-up resistor

Recommended application range for MCF8315D is shown in Table 9-2.

Table 9-2. Recommended Application Range

Parameter	Min	Max	Unit
Motor voltage	4.5	35	V
Back-EMF constant (see Section 6.3.13.3)	0.6	2000	mV/Hz
Motor resistance (see Section 6.3.13.1)	0.006	20	Ω
Motor inductance (see Section 6.3.13.2)	0.006	20	mH
Motor electrical speed	-	1500	Hz
Peak motor phase current	-	4	A

9.2.1 Application Curves

9.2.1.1 Motor startup

Figure 9-2 shows the FG waveform and the phase current waveform at different motor operations.

Copyright © 2025 Texas Instruments Incorporated

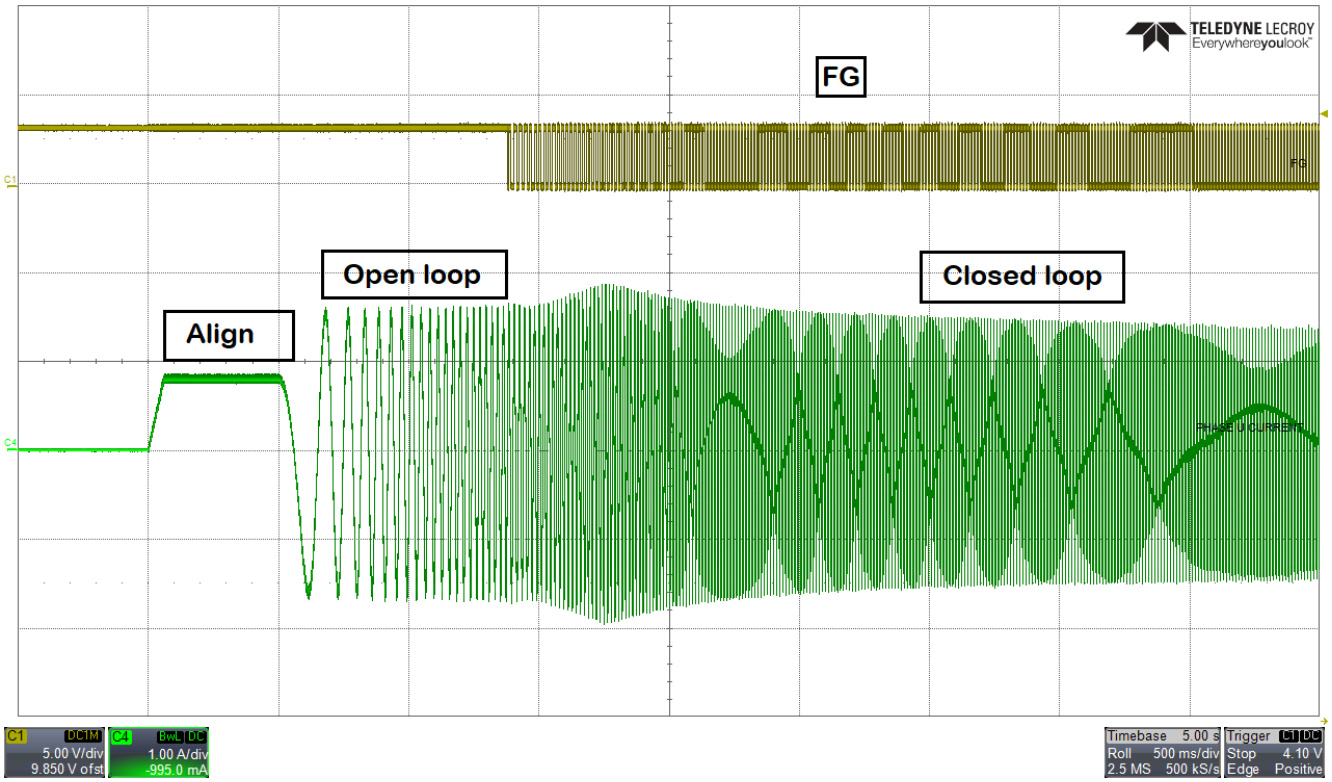


Figure 9-2. Motor Startup - FG and Phase current

9.2.1.2 MPET

Figure 9-3 shows the phase current waveform during motor parameter measurement. Figure 9-4 shows the IPD current waveform during R, L and Ke measurement. Bottom half of Figure 9-4 shows the IPD current waveform during R and L measurement. R is measured during the rising of phase current and L is measured during the falling of phase current. After R and L measurement, motor spins in open loop. Once the speed reaches MPET open loop speed reference [MPET_OPEN_LOOP_SPEED_REF], motor is coasted. BEMF voltage of all three phases are measured and Ke is calculated.

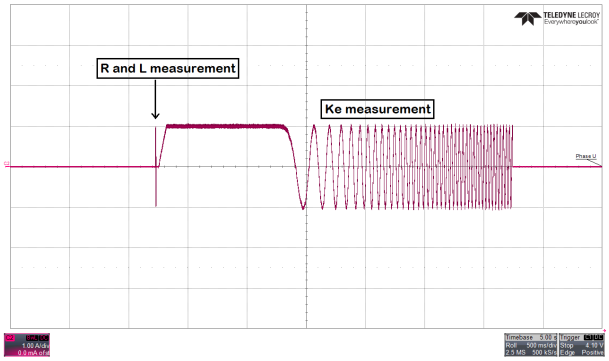


Figure 9-3. MPET - Phase current

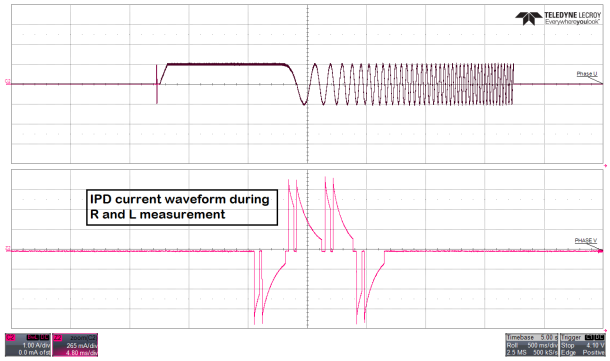


Figure 9-4. IPD current waveform during Rand L measurement

9.2.1.3 Dead time compensation

Figure 9-5 shows the phase current waveform when dead time compensation is disabled. Fundamental frequency of phase current is 40 Hz. Fast Fourier transform (FFT) of phase current plot shows harmonics at

Copyright © 2025 Texas Instruments Incorporated

160 Hz and 220 Hz. Figure 9-6 shows the phase current waveform when dead time compensation is enabled. Phase current looks more sinusoidal and the FFT of phase current plot does not have any harmonics.

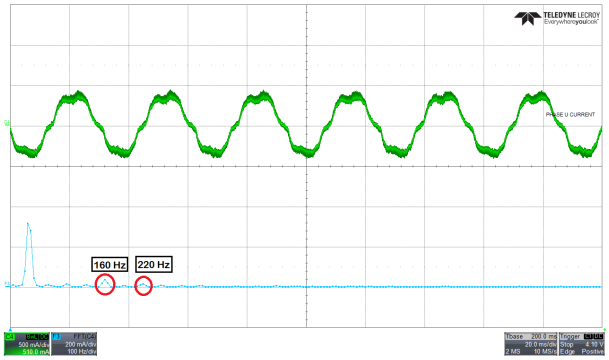


Figure 9-5. Phase current and FFT - Dead time compensation disabled

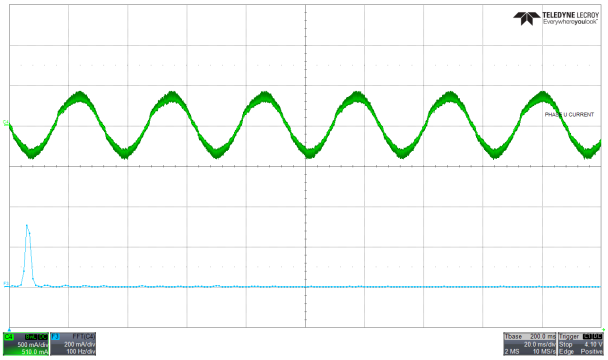


Figure 9-6. Phase current and FFT - Dead time compensation enabled

9.2.1.4 Auto handoff

Figure 9-7 shows the auto handoff feature in MCF8315D where the motor transitions seamlessly from open loop to closed loop.

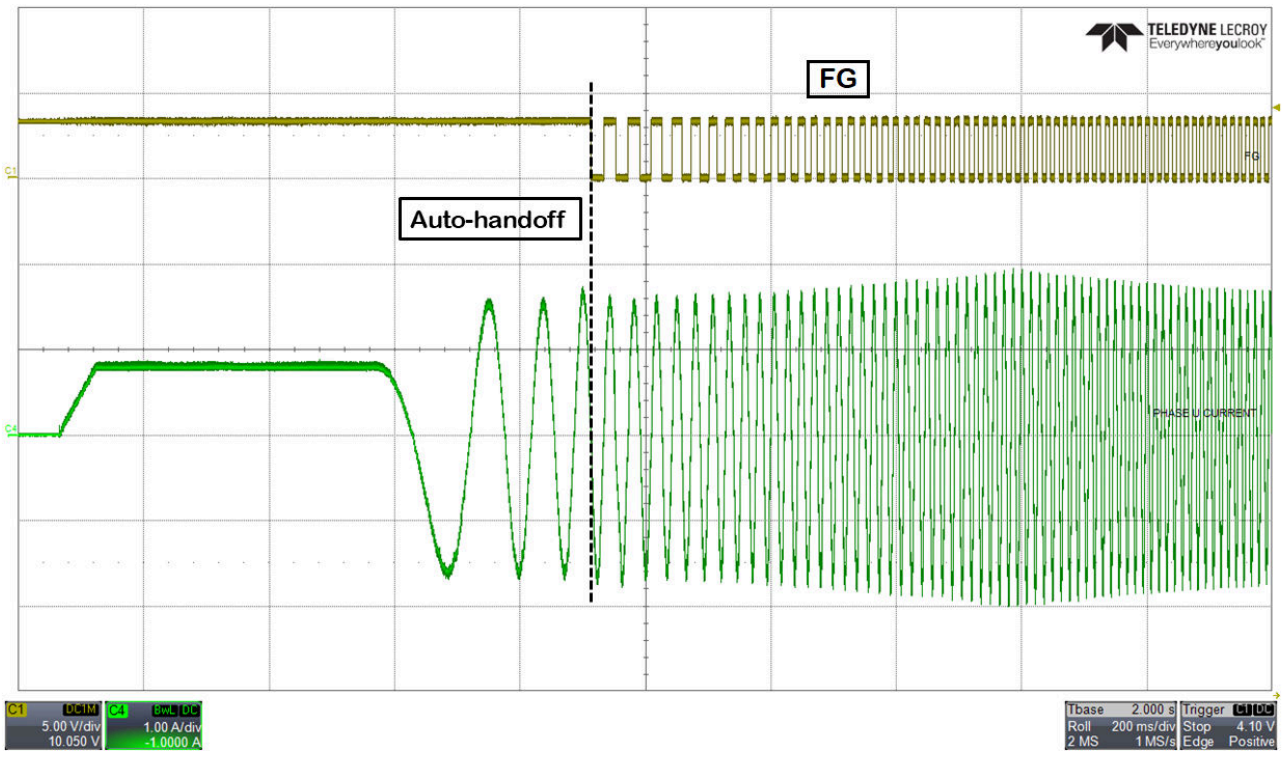


Figure 9-7. Auto-handoff

9.2.1.5 Anti voltage surge (AVS)

When motor speed decelerates at a very high deceleration rate, mechanical energy from the motor returns to the power supply which could result in pumping up the supply voltage, VM. Figure 9-8 shows overshoot in power supply voltage when AVS is disabled. Motor decelerates from 100% duty cycle to 10% duty cycle at a deceleration rate of 70,000 Hz/sec. Figure 9-9 shows no overshoot in power supply voltage when AVS is enabled.

Copyright © 2025 Texas Instruments Incorporated

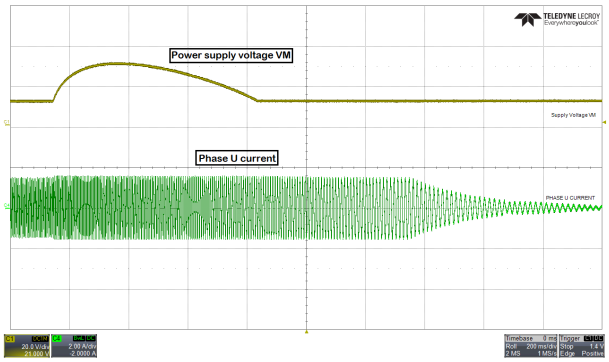


Figure 9-8. Power supply voltage and phase current waveform when AVS is disabled

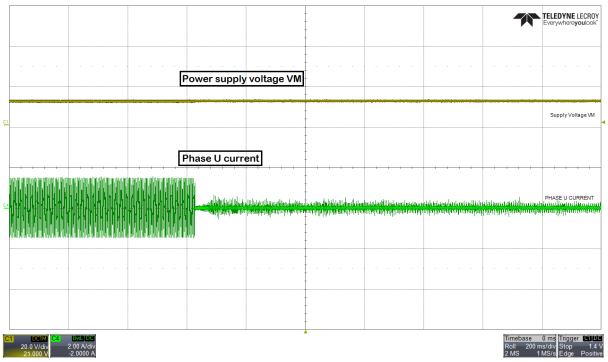


Figure 9-9. Power supply voltage and phase current waveform when AVS is enabled

9.2.1.6 Real time variable tracking using DACOUT

Note

DAC output(s) available in RGF and RRY packages only

MCF8315D has two 12-bit DAC which outputs analog voltage equivalent of digital variables on DACOUT1 and DACOUT2 pins with resolution of 12 bits and max voltage of 3V. Signals available on DACOUT pins can be used for tuning speed controller or other driver configuration or bus current monitoring. Check algorithm variable registers in datasheet for list of all algorithm variables.

The addresses for variables for DACOUT1 and DACOUT2 are configured using register bits DACOUT1_VAR_ADDR and DACOUT2_VAR_ADDR. This is useful in applications which require tracking algorithm variables in real time without having any delay from the communication bus. Pin 37 and 38 should be configured as DACOUT1 and DACOUT2.

For example, if the user wants to read phase A current from pin 37, configure pin 37 as DACOUT1 and program the phase A current register address (0x00000440) in Hex in [DACOUT1_VAR_ADDR]. If the user wants to read estimated rotor angle from pin 38, configure pin 38 as DACOUT2 and program the estimated rotor angle register address (0x00000736) in Hex in [DACOUT2_VAR_ADDR].

Figure 9-10 shows the outputs of DACOUT1 and DACOUT2. DACOUT1 is configured to read phase A current and DACOUT2 is configured to read estimated rotor angle.

Copyright © 2025 Texas Instruments Incorporated

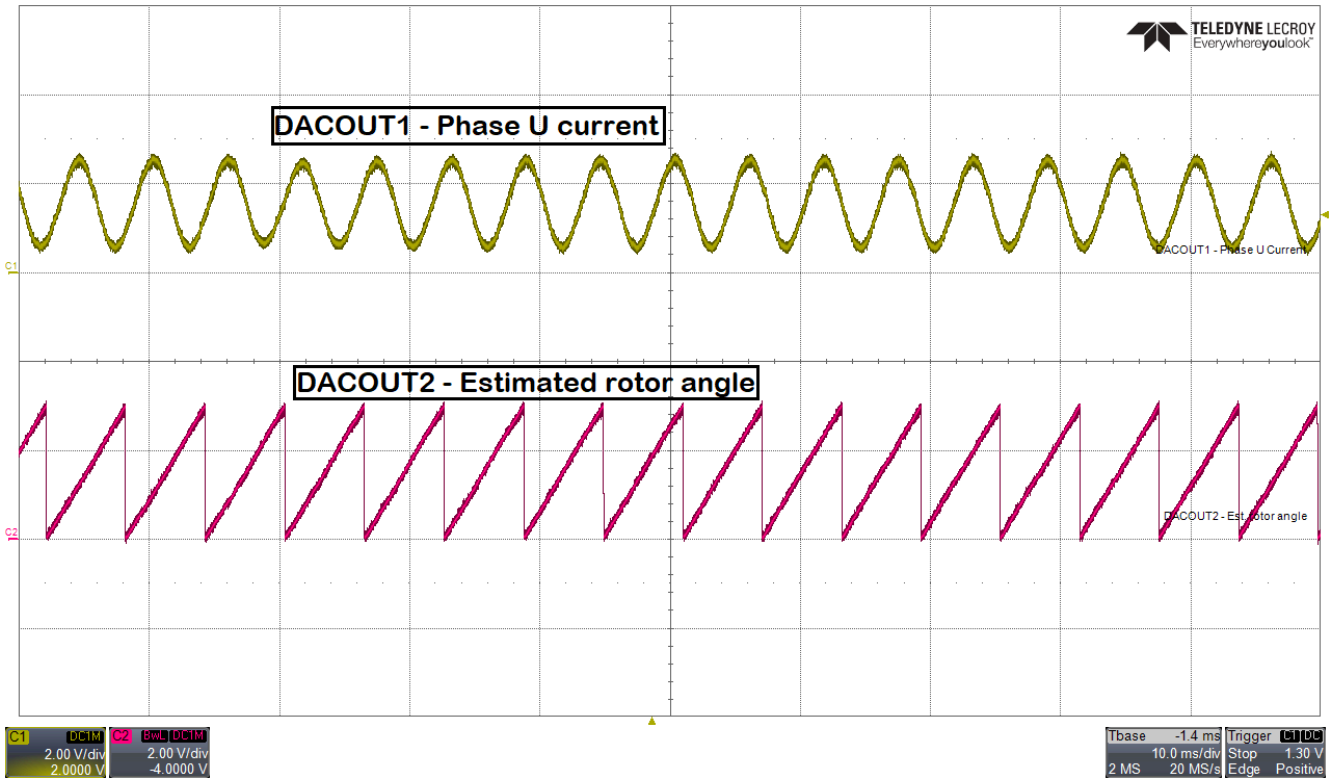


Figure 9-10. DACOUT1 and DACOUT2

9.3 Power Supply Recommendations

9.3.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in VM voltage. When adequate bulk capacitance is used, the VM voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate bulk capacitor.

Copyright © 2025 Texas Instruments Incorporated

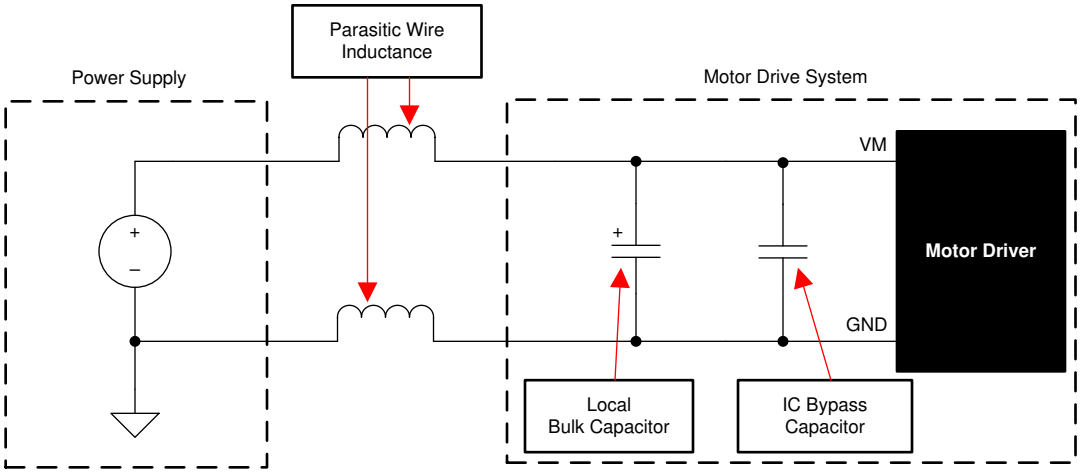


Figure 9-11. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

9.4 Layout

9.4.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize parasitic inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND_BK can be split. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW_BK and FB_BK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB_BK trace as much as possible to allow for faster load switching.

Figure 9-12 shows a layout example for the MCF8315D . Also, for layout example, refer to MCF8315D EVM .

Copyright © 2025 Texas Instruments Incorporated

9.4.2 Layout Example

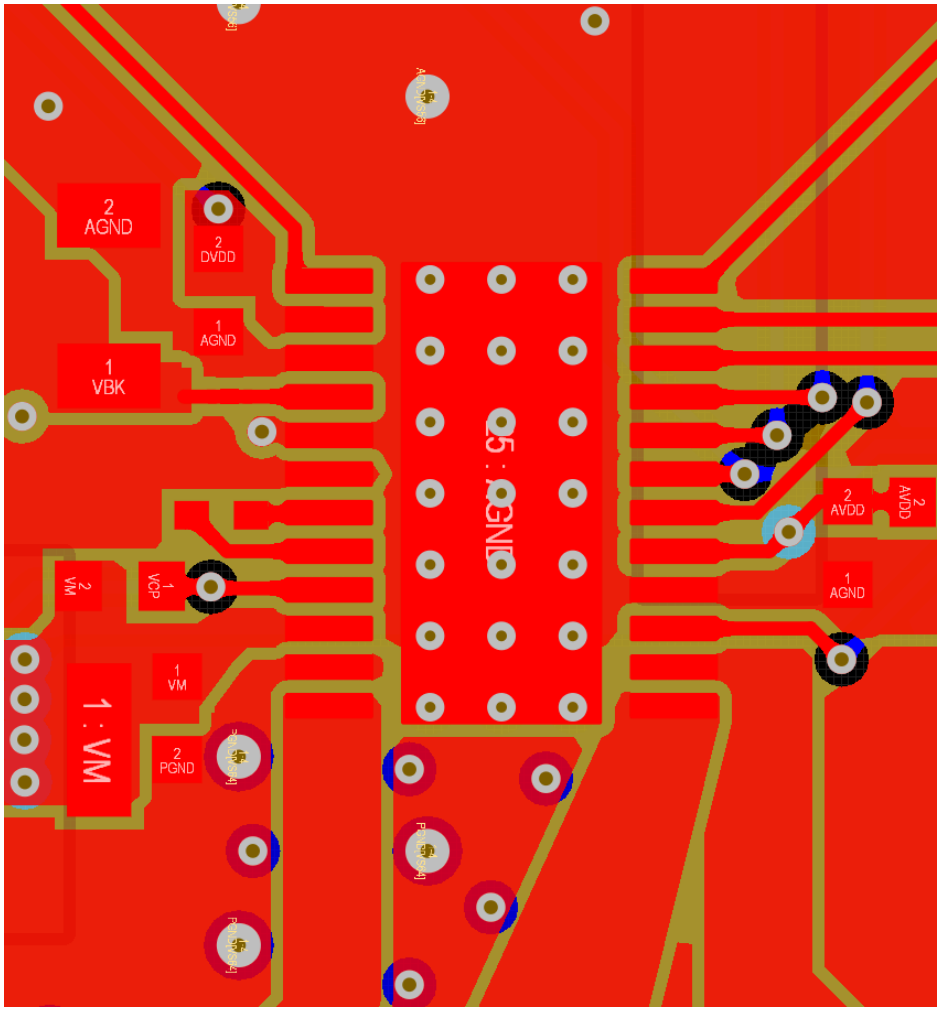


Figure 9-12. Recommended Layout Example (PWP)

Copyright © 2025 Texas Instruments Incorporated

9.4.3 Thermal Considerations

The MCF8315D has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

9.4.3.1 Power Dissipation

The power dissipated in the output FET resistance ($R_{DS(on)}$) dominates power dissipation in MCF8315D.

At start-up and fault conditions, the FET current is much higher than normal operating FET current; remember to take these peak currents and their duration into consideration.

The total device power dissipation is the power dissipated in each of the three half-bridges added together along with standby power, LDO and buck regulator losses.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

A summary of equations for calculating each loss is shown below in Table 9-3.

Table 9-3. Power Losses for MCF8315D

Loss type	MCF8315D
Standby power	$P_{standby} = VM \times I_{VM\_TA}$
LDO	$P_{LDO} = (VM-V_{AVDD}) \times I_{AVDD}$, if BUCK_PS_DIS = 1b $P_{LDO} = (V_{BK}-V_{AVDD}) \times I_{AVDD}$, if BUCK_PS_DIS = 0b
FET conduction	$P_{CON} = 3 \times (I_{RMS(FOC)})^2 \times R_{ds,on(TA)}$
FET switching	$P_{SW} = 3 \times I_{PK(FOC)} \times V_{PK(FOC)} \times t_{rise/fall} \times f_{PWM}$
Diode	$P_{diode} = 3 \times I_{PK(FOC)} \times V_{diode} \times t_{dead} \times f_{PWM}$
Buck	$P_{BK} = 0.11 \times V_{BK} \times I_{BK}$ (η_{BK} = 90%)

Copyright © 2025 Texas Instruments Incorporated

10 Device and Documentation Support

10.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

Copyright © 2025 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MCF8315DVPWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MCF15DV
MCF8315DVPWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MCF15DV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

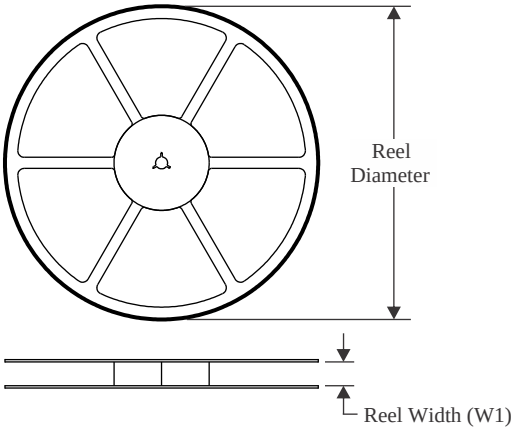
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

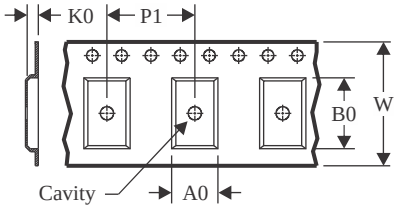
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

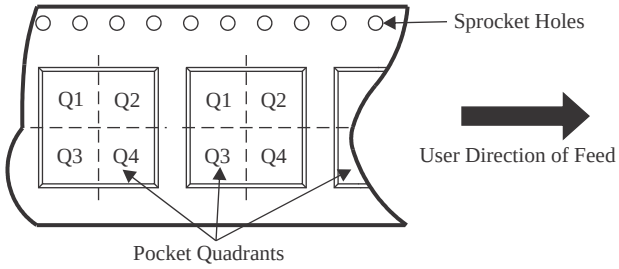


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

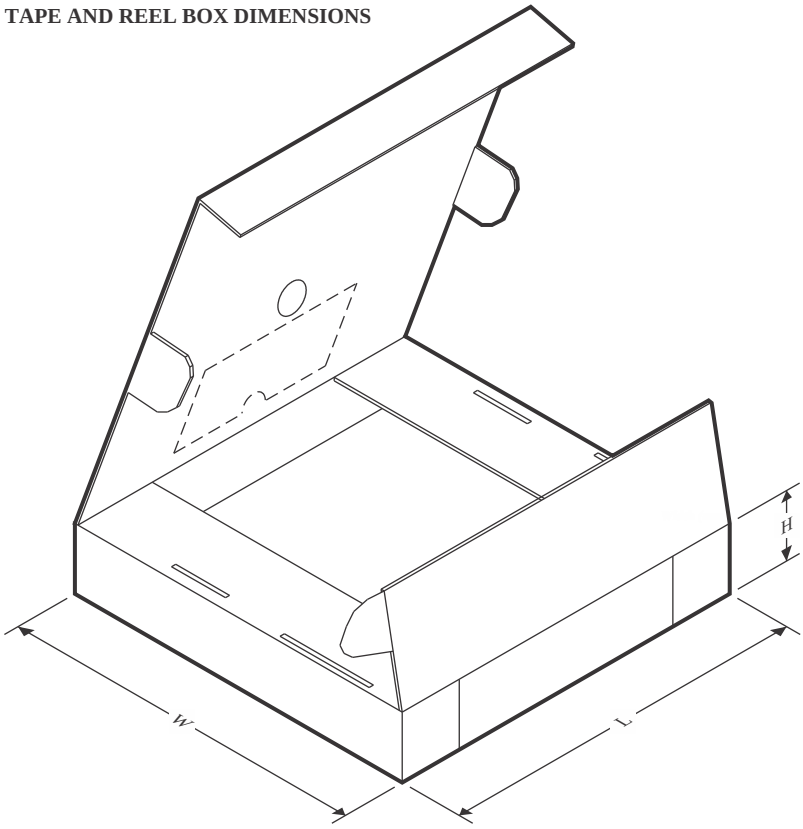
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCF8315DVPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCF8315DVPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

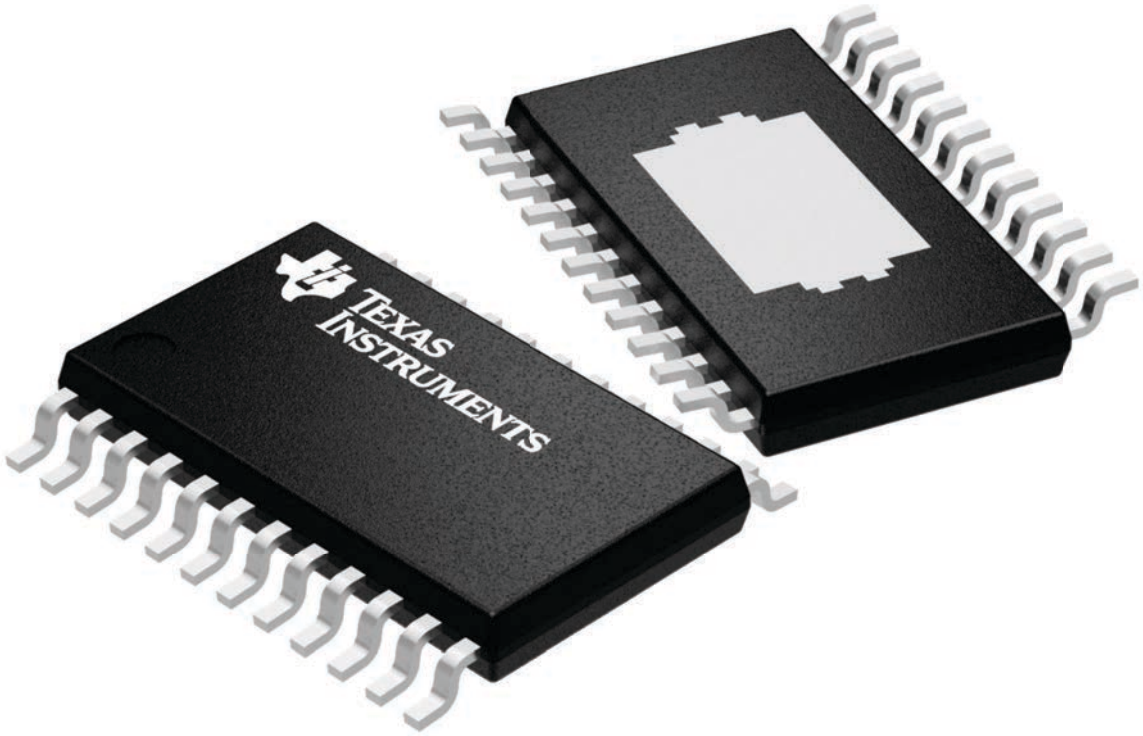
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

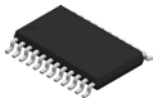
4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

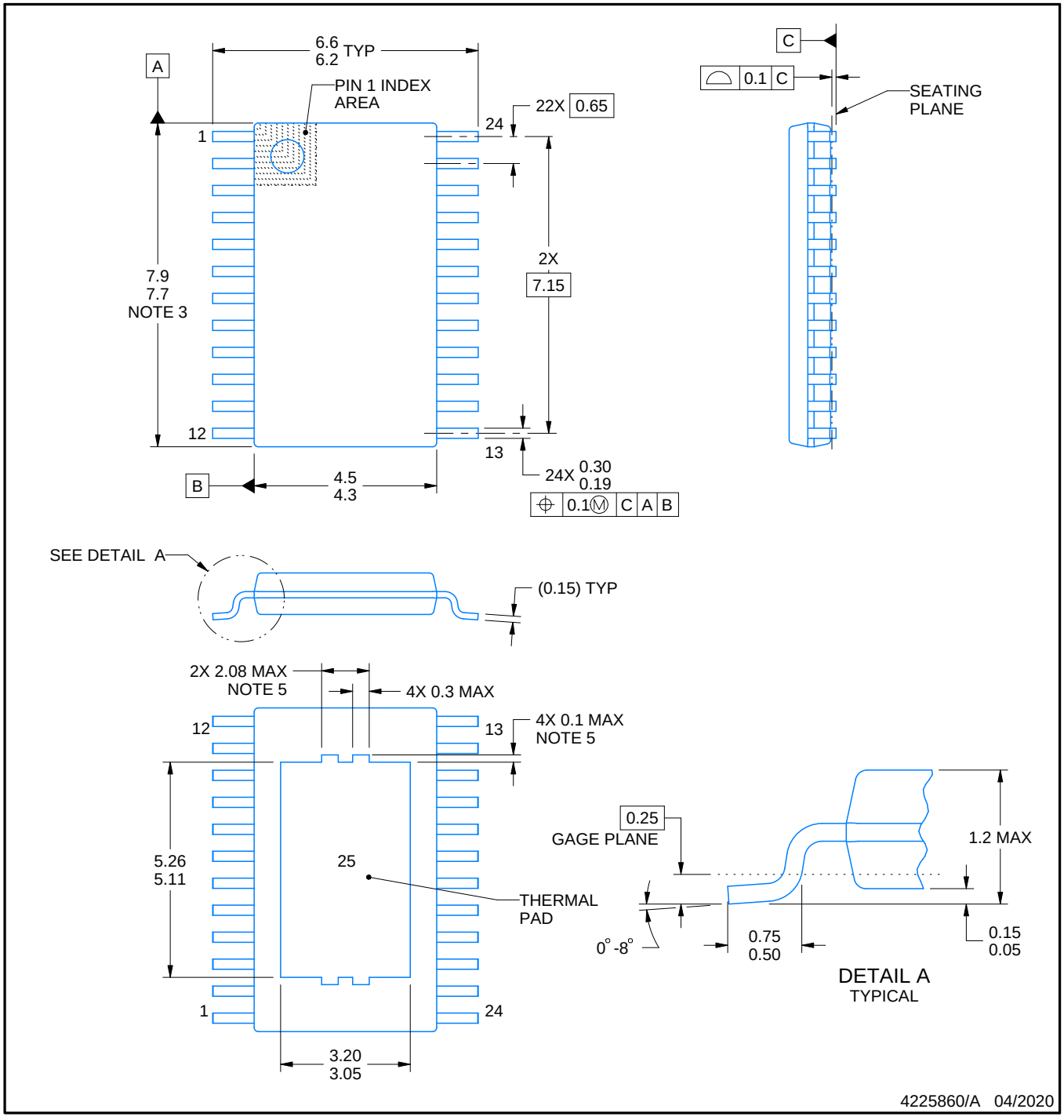


PACKAGE OUTLINE

PWP0024J

PowerPAD™ TSSOP - 1.2 mm max height

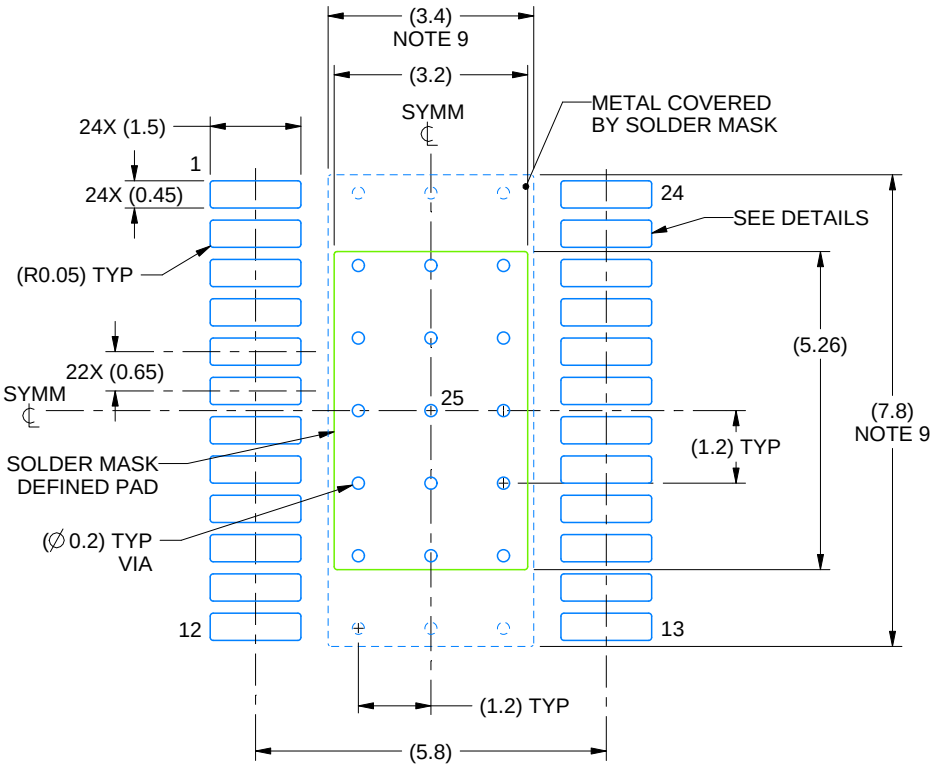
SMALL OUTLINE PACKAGE



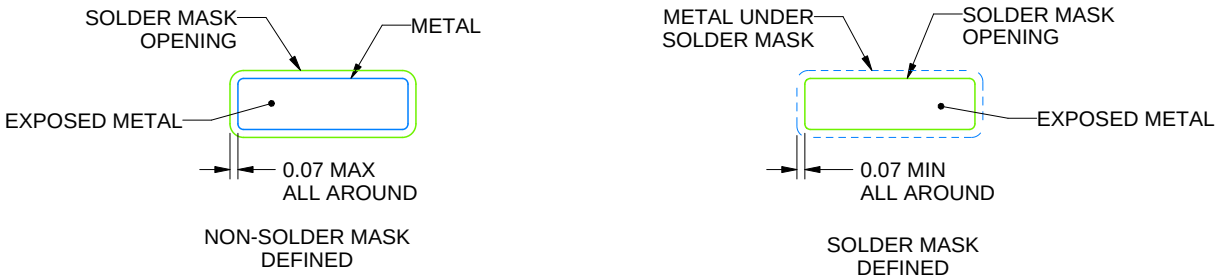
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

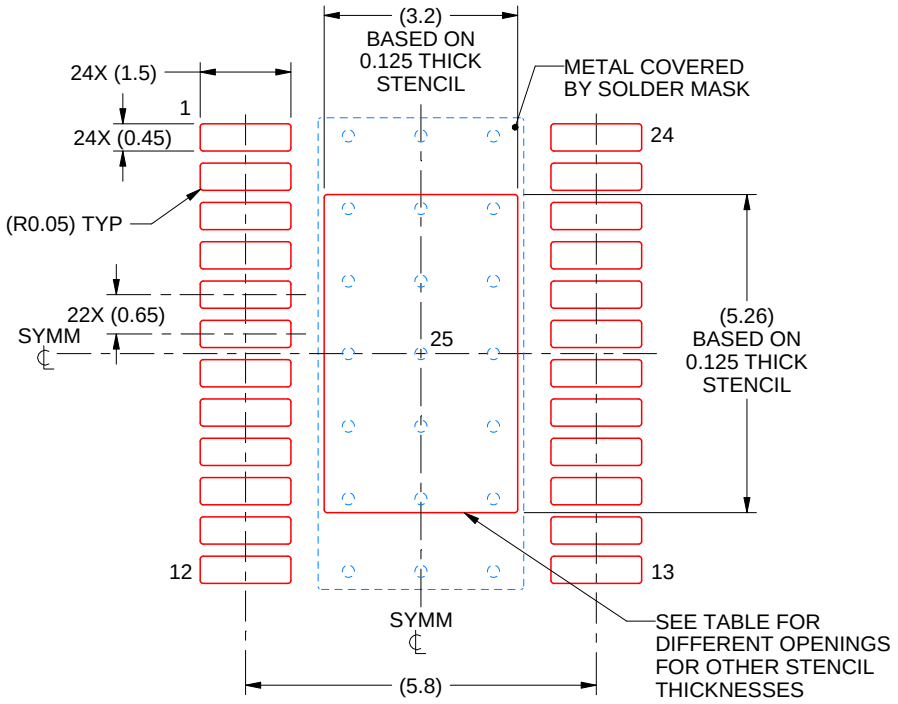


SOLDER MASK DETAILS

4225860/A 04/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.88
0.125	3.20 X 5.26 (SHOWN)
0.15	2.92 X 4.80
0.175	2.70 X 4.45

4225860/A 04/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025