Application Note

Modelling, Analysis and Compensation of the Current-Mode Converter

Kurt Hesse *PMP Systems Powers*

Abstract

This application note describes how the performance of any current-mode converter can be improved (and the previously mentioned peculiarities reduced) by adding a fixed amount of *slope compensation* to the sensed current waveform.

Table of Contents

1 Introduction 2
2 Peculiarities of the Peak-Current Control Converter 3
2.1 Open Loop Instability 3
2.2 Ringing Inductor Current 3
2.3 Subharmonic Oscillation 5
2.4 Peak Current Sensing Versus Average Current Sensing 7
2.5 Small Ripple Current 8
3 Small Signal Ac Model 10
3.1 AC Model Derivation 10
3.2 AC Model Discussion 11
4 Slope Compensation of the UC1846 Control Device 13
5 References 14
6 Revision History 14

Copyright © 2026 Texas Instruments Incorporated

1 Introduction

The recent introduction of integrated control circuits designed specifically for current mode control has led to a dramatic upswing in the application of this technique to new designs. As current-mode conversion increases in popularity, several peculiarities associated with fixed-frequency, peak-current detecting schemes have surfaced. These include instability above 50% duty cycle (D> 0.5), a tendency towards subharmonic oscillation, non-ideal loop response, and an increased sensitivity to noise. Although the advantages of current-mode control over conventional voltage-mode control has been amply demonstrated, see *References* section, there still exist several drawbacks to a fixed frequency peak-sensing current mode converter. They are:

- open loop instability above 50% duty cycle
- less than ideal loop response caused by peak instead of average inductor current sensing
- tendency towards subharmonic oscillation
- noise sensitivity, particularly when inductor ripple current is small

Although the benefits of current mode control, in most cases, far out-weight these drawbacks, a simple solution does appear to be available. It has been shown by a number of authors that adding slope compensation to the current waveform (see Figure 1-1) stabilizes a system above 50% duty cycle.

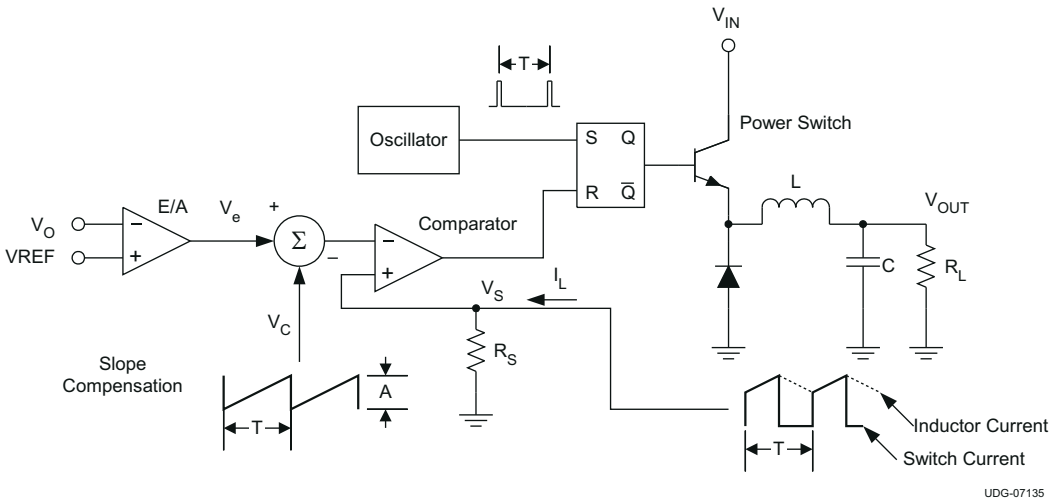


Figure 1-1. Current-Mode Controlled Buck Regulator with Slope Compensation

It becomes apparent that this same compensation technique can be used to minimize many of the drawbacks stated above. In fact, any practical converter nearly always performs better with some slope compensation added to the current waveform.

The simplicity of adding slope compensation - usually a single resistor - adds to its attractiveness. However, this introduces a new problem - that of analyzing and predicting converter performance. Small signal ac models for both current and voltage-mode PWM's have been extensively developed in the literature. However, the slope compensated or *dual control* converter possesses properties of both with an equivalent circuit different from yet containing elements of each. Although this has been addressed in part by several authors[1,2], there remains a need for a simple circuit model that can provide both qualitative and quantitative results for the power supply designer.

The first objective of this application note is to familiarize the reader with the peculiarities of a peak-current control converter and at the same time demonstrate the ability of slope compensation to reduce or eliminate many problem areas, and is described in Section 2, *Peculiarities of the Peak-Current Control Converter*. Second, in Section 3, *Small Signal AC Model*, a circuit model for a slope compensated buck converter in continuous conduction will be developed using the state-space averaging technique outlined in (1). This provides the analytical basis for Section 4, *Slope Compensation of the UC1846 Control Device*, where the practical implementation of slope compensation is discussed.

Copyright © 2026 Texas Instruments Incorporated

2 Peculiarities of the Peak-Current Control Converter

2.1 Open Loop Instability

An unconditional instability of the inner current loop exists for any fixed-frequency current-mode converter operating above 50% duty cycle - regardless of the state of the voltage feedback loop. While some topologies (most notably two transistor forward converters) cannot operate above 50% duty cycle, many others would suffer serious input limitations if greater duty cycle could not be achieved. Injection of a small amount of slope compensation into the inner loop yields greater stability for all values of duty cycle. Following is a brief review of this technique.

Figure 2-1 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_0. By perturbing the current I_L by an amount ΔI, ΔI decreases with time for D < 0.5 (Figure 2-1A), and increase with time for D > 0.5 (Figure 2-1B). Mathematically this can be stated as

$$\Delta l_1 = -\Delta l_0\left(\frac{m_2}{m_1}\right) \tag{1}$$

A linear ramp of slope –m as shown in Figure 2-1C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta l_1 = -\Delta l_0\left(\frac{m_2 + m}{m_1 + m}\right) \tag{2}$$

Solving for m at 100% duty cycle gives

$$m > -\frac{1}{2}(m_2) \tag{3}$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1-1, m_2 is a constant equal to $V_0/L \times R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T \times R_S \times \left(\frac{V_0}{L}\right) \tag{4}$$

to guarantee stability above 50% duty cycle.

2.2 Ringing Inductor Current

Deeper consideration of the inductor current waveform reveals two additional phenomenon related to the previous instability. Generalizing Figure 2-1 and plotting I_N vs. N_T for all n, Figure 2-2, shows a damped sinusoidal response at one-half the switching frequency, similar to that of an R-L-C circuit. This ring-out is undesirable in the following two ways.

- it produces a ringing response of the inductor current to line and load transients
- it peaks the control loop gain at ½ the switching frequency, producing a marked tendency towards instability

Copyright © 2026 Texas Instruments Incorporated

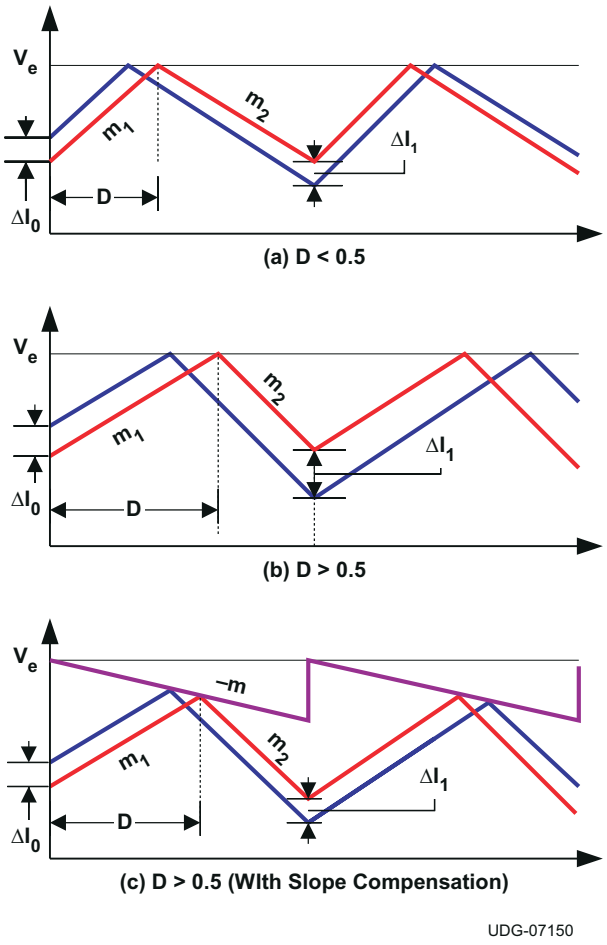


Figure 2-1. Open-Loop Instability in a Current-Mode Converter

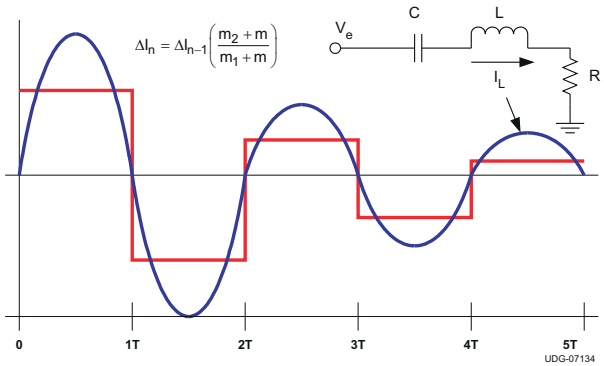


Figure 2-2. Inductor Current Response to R-L-C Circuit

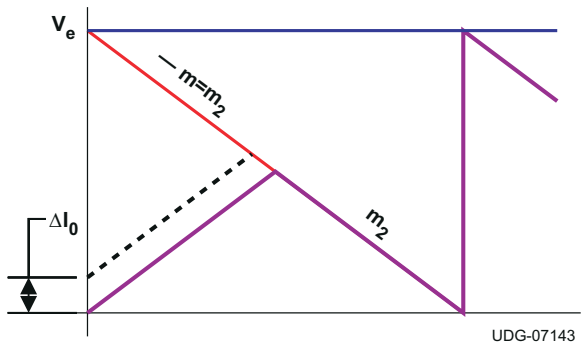


Figure 2-3. Current Purtubation

As shown in Figure 1-1, and easily verified from Equation 2, that by choosing the slope compensation m to be equal to -m2 (the down slope of the inductor current), the best possible transient response is obtained. This is analogous to critically damping the R-L-C circuit, allowing the current to correct itself in exactly one cycle, as illustrated in Figure 2-3 Note that while this may optimize inductor current ringing, it has little bearing on the transient response of the voltage control loop itself.

Copyright © 2026 Texas Instruments Incorporated

2.3 Subharmonic Oscillation

Gain peaking by the inner current loop can be one of the most significan problems associated with current-mode controllers. This peaking occurs at one-half the switching frequency, ans because of excess phase shift in the modulator, can cause the voltage feedback loop to break into oscillation at one-half the switching frequency. This instability, sometimes called subharmonic oscillation, is easily detected as duty cycle asymmetry between consecutive drive pulses in the power stage. Figure 2-4 shows the inductor current of a current-mode controller in subharmonic oscillation (red waveform through period 2T).

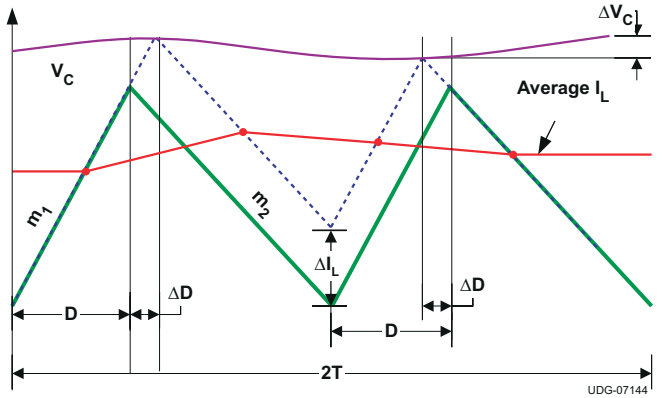


Figure 2-4. Current Wave Form of a Current-Mode Converter in Subharmonic Oscillation

To determine the bounds of stability, it is first necessary to develop an expression for the gain of the inner loop at one-half the switching frequency. The technique used in (2) will be paralleled for a buck converter with the addition of terms to include slope compensation

Copyright © 2026 Texas Instruments Incorporated

2.3.1 Loop Gain Calcluation at ½f_S

Referring to Figure 2-4 and Figure 2-5, relate the input stimulus, ΔV_e, to an output current, and two equations are derived.

$$\Delta I_L = \Delta D(m_1) \times T - \Delta D(m_2) \times T \tag{5}$$

$$\Delta V_C = \Delta D(m_1) \times T + \Delta D(m_2) \times T \tag{6}$$

Adding slope compensation as in Figure 2-5 gives the following equation.

$$\Delta V_e = \Delta V_C + 2 \times \Delta D(m) \times T \tag{7}$$

Using Equation 5 to eliminate ΔV_c from Equation 6 and solving for $\Delta I_L/\Delta V_e$ yields Equation 8.

$$\frac{\Delta I_L}{\Delta V_e} = \frac{m_1 - m_2}{m_1 + m_2 + m} \tag{8}$$

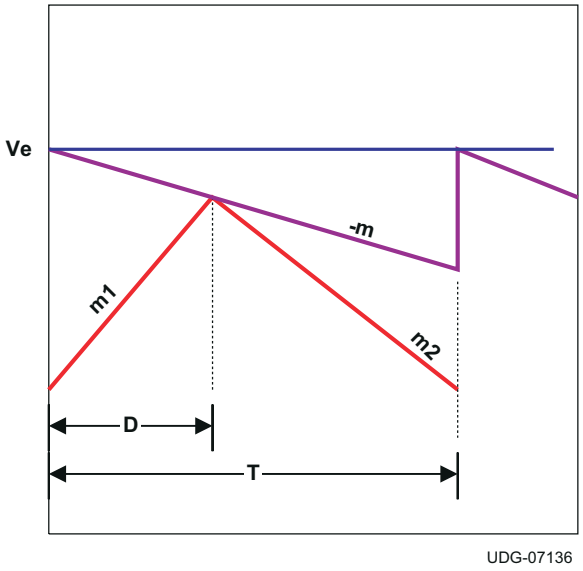


Figure 2-5. Addition of Slope Compensation to the Control Signal

For steady state condition

$$D_{(m1)}T = (1 - D)_{(m2)}T \text{ or } D = \left(\frac{-m2}{m1 - m2}\right) \tag{9}$$

By using Equation 9 to reduce Equation 7

$$\frac{\Delta I_L}{\Delta V_e} = \frac{1}{(1 - 2D)(1 + (m/m_2))} \tag{10}$$

By recognizing that ΔI_L is simply a square wave of period 2T, relate the first harmonic amplitude to ΔI_L by the factor 4/π and write the small signal gain at f = ½f_S as

$$\frac{i_L}{v_e} = \frac{4\pi}{(1 - 2D)(1 + (m/m_2))} \tag{11}$$

Assuming a capacitive load of C at the output and an error amplifier gain of A, the expression for loop gain at f = ½f_S is

Copyright © 2026 Texas Instruments Incorporated

$$\text{Loop Gain} = \frac{\left(\frac{4\pi}{n^2 C}\right)}{(1-2D)(1+(m/m_2))} \tag{12}$$

2.3.2 Using Slope Compensation to Eliminate Subharmonic Oscillation

From Equation 13, the expression for maximum error amplifier gain at f = ½f_S to guarantee stability is

$$A_{MAX} = \frac{(1-2D)(1+(m/m_2))}{\left(\frac{4\pi}{n^2 C}\right)} \tag{13}$$

Equation 13 clearly shows that the maximum allowable error amplifier gain, A_{MAX}, is a function of both duty cycle and slope compensation A normalized plot of A_{MAX} versus duty cycle for several values of slope compensation is shown in Figure 2-6. Assuming the amplifier gain cannot be reduced to zero at f = ½f_S, then for the case of m = 0 (no compensation) we see the same instability previously discussed at 50% duty cycle. As the compensation is increased to m = -½m_2, the point of instability moves out to a duty cycle of 1.0, however in any practical system, the finite value of A,,will drive the feedback loop into subharmonic oscillation well before full duty cycle is reached. If we continue to increase m, we reach a point, m = -m2, where the maximum. gain becomes independent of duty cycle. This is the point of critical damping as discussed earlier, and increasing m above this value will do little to improve stability for a regulator operating over the full duty cycle range.

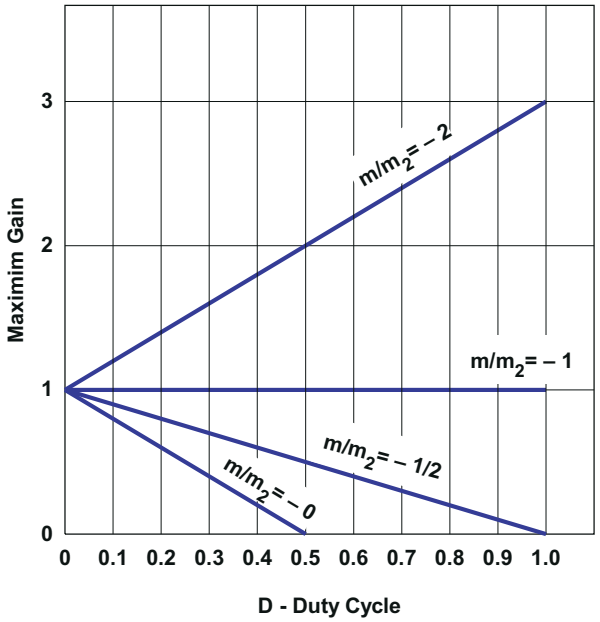


Figure 2-6. Maximum Error Amplifier Gain vs Duty Cycle

2.4 Peak Current Sensing Versus Average Current Sensing

True current-mode conversion, by definition, should force the average inductor current to follow an error voltage. This in effect replaces the inductor with a current source and reducing the order of the system by one. As shown in Figure 2-7, however, peak current detecting schemes are generally used which allow the average inductor current to vary with duty cycle while producing less than perfect input to output (or feedforward) characteristics. If slope compensation is added to equal to m = -½ rn2 as shown in Figure 2-8, a peak current detecting scheme can be converted into an average current detector, again allowing for perfect current mode control. As mentioned in the last section, however, the designer must be careful of subharmonic oscillations as a duty cycle of 1 is approached when using m = -½ m2.

Copyright © 2026 Texas Instruments Incorporated

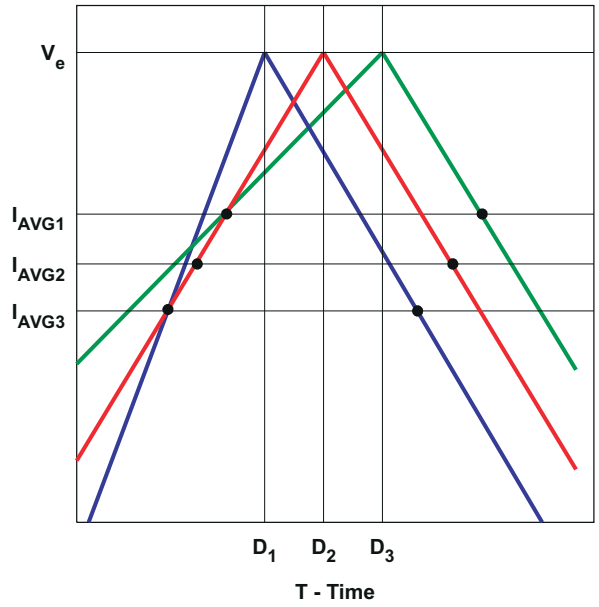


Figure 2-7. Peak Current Sensing Without Slope Compensation

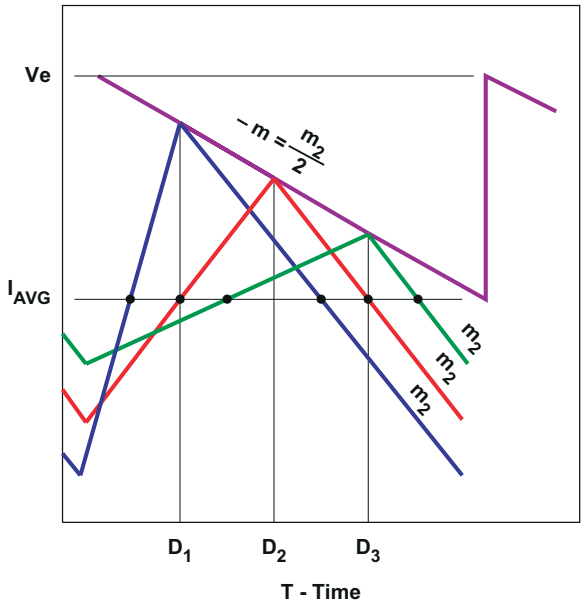


Figure 2-8. Average Inductor Current Independent of Duty Cycle

2.5 Small Ripple Current

From a systems standpoint, small inductor ripple currents are desirable for a number of reasons:

- reduced output capacitor requirements
- continuous current operation with light loads
- less output ripple

However, because of the shallow slope presented to the current sense circuit, a small ripple current can, in many cases, lead to pulse width jitter caused by both random and synchronous noise Figure 2-9. Again, if slope compensation is added to the current waveform, a more stable switchpoint is generated. To be of benefit, the amount of slope added needs to be significant compared to the total inductor current and not just the ripple current. This usually dictates that the slope, m be considerably greater than m2 and while this is desirable for subharmonic stability, any slope greater than m = -½ m_2 causes the converter to behave less like an ideal current mode converter and more like a voltage mode converter. A proper trade-off between inductor ripple current and slope compensation can only be made based on the equivalent circuit model derived in the *Small Signal AC Model* section.

Copyright © 2026 Texas Instruments Incorporated

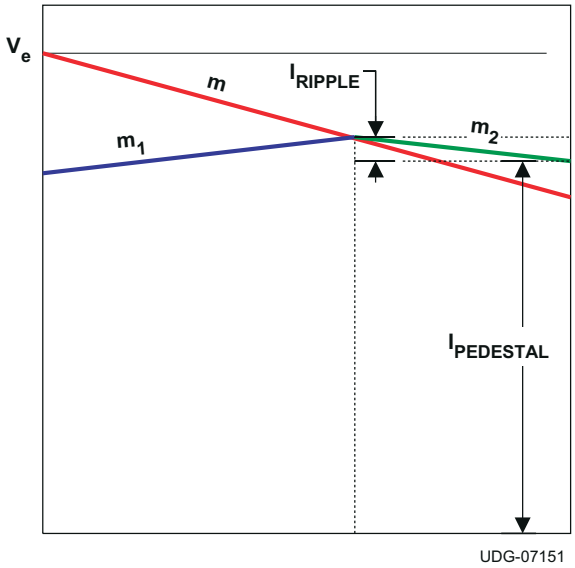


Figure 2-9. Large Pedestal-to-Ripple Current Ratio

Copyright © 2026 Texas Instruments Incorporated

3 Small Signal Ac Model

As previously described, many drawbacks associated with current-mode control can be reduced or eliminated by adding slope compensation in varying degrees to the current waveform. In an attempt to determine the full effects of this same compensation on the closed loop response, a small signal equivalent circuit model for a buck regulator is developed using the state-space averaging technique developed in Equation 1.

3.1 AC Model Derivation

Figure 3-1(a) shows an equivalent circuit for a buck regulator power stage. From this can be written a two state-space averaged differential equation corresponding to the inductor current and capacitor voltage as functions of duty cycle D.

$$\dot{i}_L = \left(\frac{V_1 - V_0}{L}\right) \times D - \left(\frac{V_0(1-D)}{L}\right) \tag{14}$$

$$\dot{V}_0 = \left(\frac{I_L}{C}\right) - \left(\frac{V_0}{R}\right) \tag{15}$$

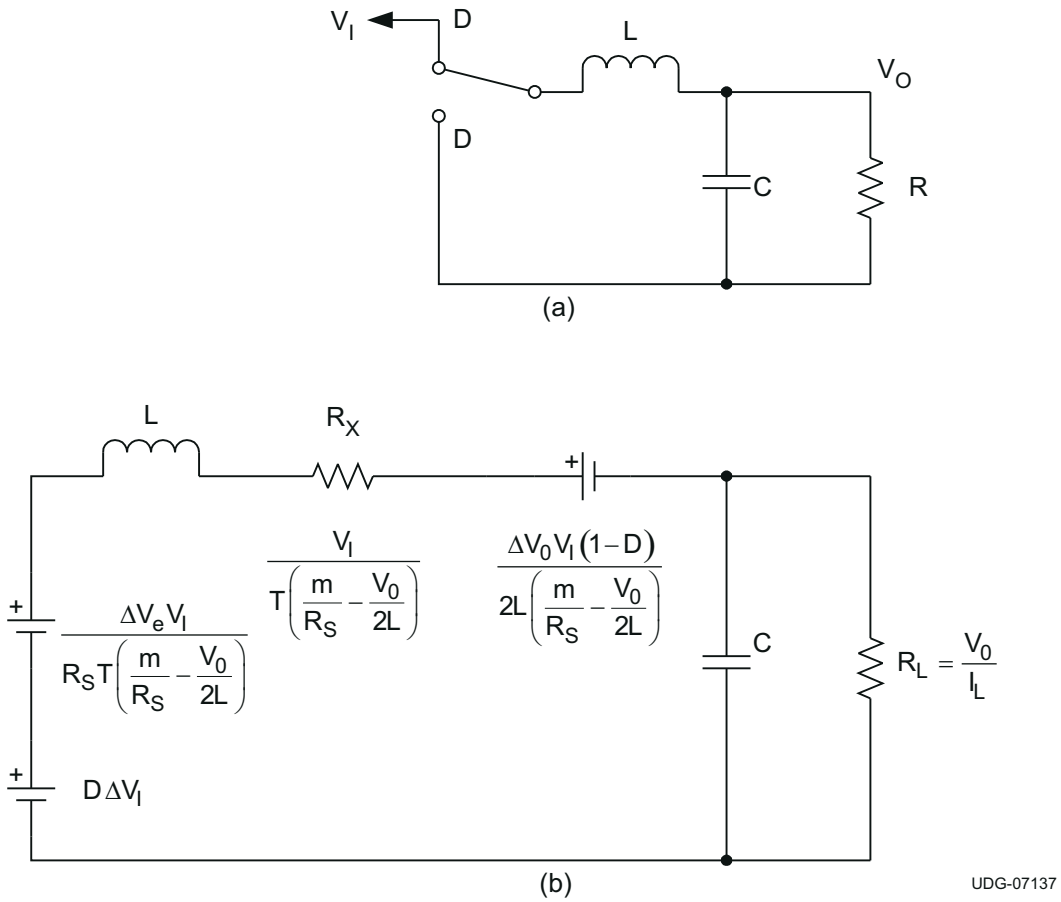


Figure 3-1. (a) Basic Buck Converter and (b) Small Signal Equivalent Circuit Model

$$\Delta l_n = \Delta l_n - 1\left(\frac{m_2 + m}{m_1 + m}\right) \tag{16}$$

If these equations are perturbed (in other words, substitute $V_I + \Delta V_I$, $V_0 + \Delta V_0$, $D + \Delta D$ and $I_L + \Delta I_L$, for their respective variables) and ignore second order terms, it yields the small signal averaged equations.

Copyright © 2026 Texas Instruments Incorporated

$$\Delta\dot{i}_L = \left(\frac{D\Delta I_L}{L}\right) - \left(\frac{\Delta V_0}{L}\right) + \left(\frac{V_1\Delta D}{L}\right) \quad (17)$$

$$\Delta\dot{V}_0 = \left(\frac{\Delta I_L}{C}\right) - \left(\frac{\Delta V_0}{CR}\right) \quad (18)$$

A third equation (the control equation) relating error voltage, V_e, to duty cycle may be written from Figure 2-5 as

$$I_L \times R_S - V_e - mDT - \frac{(1-D)V_0 \times T \times R_S}{2L} \quad (19)$$

Perturbing this equation as before gives

$$\Delta I_L = \frac{\Delta V_e}{R_S} - \Delta DT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right) - \frac{T}{2L}(1-D)\Delta V_0 \quad (20)$$

By using Equation 20 to eliminate ΔD from Equation 17 and Equation 18, the state space equations become

$$\Delta\dot{I}_L = \frac{D}{L}\Delta V_1 + \frac{\Delta V_e \times V_1}{R_S \times LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta V_0 \times V_1}{(2L)^2\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta I_L V_1}{LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} \quad (21)$$

$$\Delta\dot{V}_0 = \left(\frac{\Delta I_L}{C}\right) - \left(\frac{\Delta V_0}{CR}\right) \quad (22)$$

An equivalent circuit model for these equations is shown in Figure 3-1(b) and discussed in the *AC Model Discusion* section.

3.2 AC Model Discussion

The model of Figure 3-1(b) can be used to verify and expand upon the previous observations. Key to understanding this model is the interaction between R_X and L as the slope compensation, m is changed. In most cases, the dependent source between R_X and C can be ignored.

If R_X is much greater than L, as is the case for little or no compensation (m = 0), the converter has a single pole response and acts as a true current mode converter. If R_X is small compared to L $m \gg \left(\frac{R_S \times V_0}{2L}\right)$, then a double pole response is formed by the L-R-C output filter similar to any voltage-mode converter. By appropriately adjusting m, any condition between these two extremes can be generated.

Of particular interest is the case when m = $\left(\frac{R_S \times V_0}{2L}\right)$. Since the down slope of the inductor current (m2 from Figure 2-5) is equal to (R_S V_0)/L the equation m = -½ m_2 can be derived. At this point, R_X goes to infinity, resulting in an ideal current mode converter. This is the same point, discussed in *Peak Current Sensing vs. Average Current Sensing* section , where the average inductor current exactly follows the error voltage. Note that although this compensation is ideal for line rejection and loop response, maximum error amplifier gain limitations as higher duty cycles are approached (see the *Subharmonic Oscillation* section) may necessitate using more compensation.

Having derived an equivalent circuit model, its application to more specific design examples can be discussed. Figure 3-2 plots open loop ripple rejection ($\Delta V_0/\Delta V_I$) at 120 Hz versus slope compensation for a typical 12-V buck regulator operating under the following conditions:

- V_0 = 12 V
- V_I= 25 V
- L = 200 µH
- C = 300 µF
- T = 20 µs
- R = 0.5 Ω
- R_L = 1Ω, 12Ω

Copyright © 2026 Texas Instruments Incorporated

$$m_2 = \left(\frac{V_0}{L}\right)R_s$$

Again, as the slope compensation approaches m = -½ m_2, the theoretical ripple rejection is seen to become infinite. As larger values of m are introduced ripple rejection slowly degrades to that of a voltage-mode converter (-6.4 dB for this example).

If a small ripple to DC current ratio is used, as is the case for R_L = 1 Ω in the example, proportionally larger values of slope compensation UC1846 may be injected while still maintaining a high ripple rejection ratio. In other words, to obtain a given ripple rejection ratio, the allowable slope compensation may be injected while maintaining a high ripple-rejection ratio, the allowable slope compensation varies proportionally to the average DC current, not the ripple current. This is an important concept when attempting to minimize noise jitter on a low ripple converter.

Figure 3-3 shows the small signal loop response ($\Delta V_0/\Delta Ve$) versus frequency for the same example of Figure 3-2. The gains have all been normalized to 0 dB at low frequency to reflect the actual difference in frequency response as slope compensation m is varied. At , m = -½ m_2 an ideal single-pole roll-off at 6 dB/octave is obtained. As higher ratios are used. the response approaches that of a double-pole with a 12-dB/octave roll-off and associated 180° phase shift.

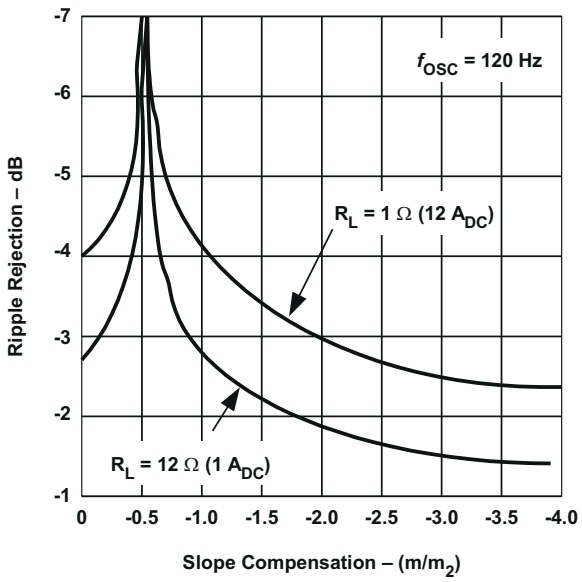


Figure 3-2. Ripple Rejection vs Slope Compensation

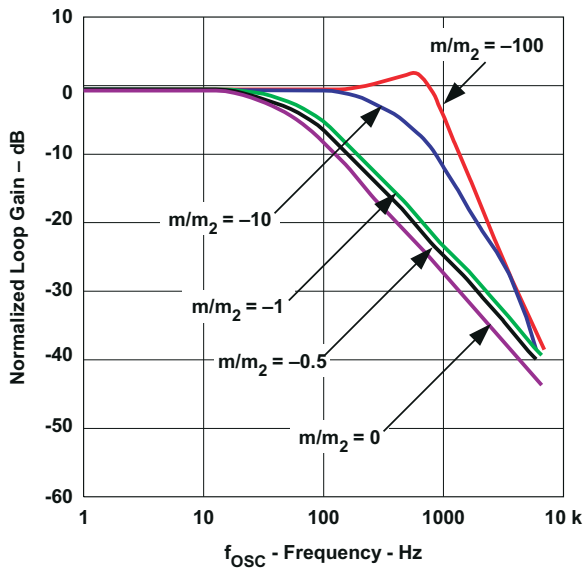


Figure 3-3. Normalized Loop Gain vs Frequency

Copyright © 2026 Texas Instruments Incorporated

4 Slope Compensation of the UC1846 Control Device

Implementing a practical, cost effective current-mode converter has recently been simplified with the introduction of the UC1846 integrated control device. This device contains all of the control and support circuitry required for the design of a fixed frequency current-mode converter. Figure 4-1 and Figure 4-2 demonstrate two alternative methods of implementing slope compensation using the UC1846. Direct summing of the compensation and current sense signal at Pin 4 is easily accomplished, however, this introduces an error in the current limit sense circuitry. The alternative method is to introduce the compensation into the negative input terminal of the error amplifier. This works only if both of the following statements are true

- the gain of the error amplifier is fixed and constant at the switching frequency (R_1/R_2 for this case)

  AND
- both error amplifier and current amplifier gains are taken into consideration when calculating the required slope compensation

In either case, once the value of R_2 has been calculated, the loading effect on C_T can be determined and, if necessary, a buffer stage added as in Figure 4-3.

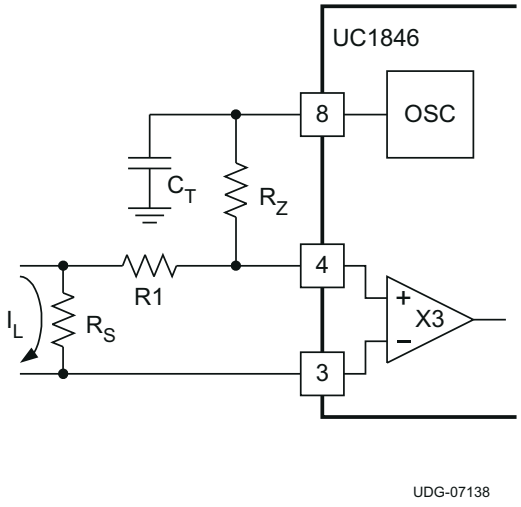


Figure 4-1. Sensed Current Signal

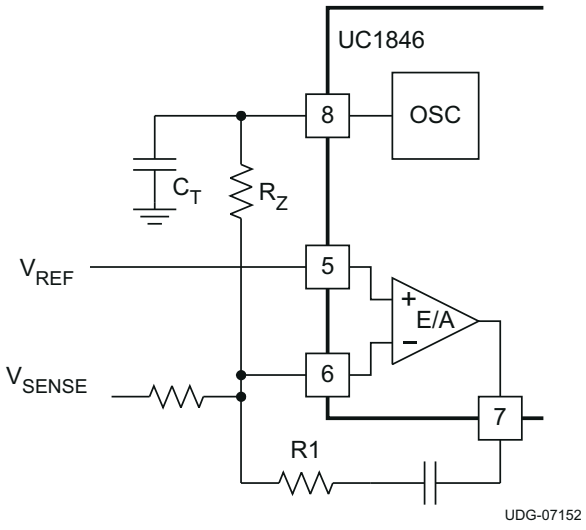


Figure 4-2. Error Signal

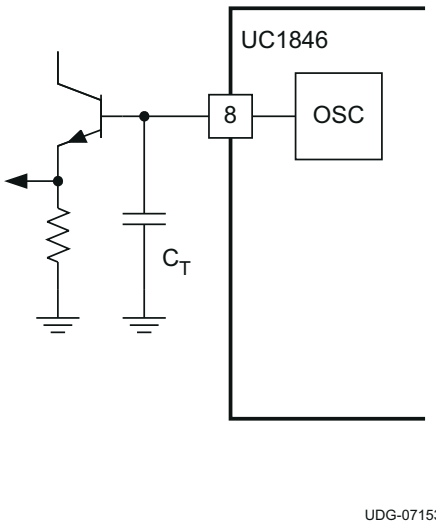


Figure 4-3. Emmitter Follower to Lower Oscillator Output Impedance

Copyright © 2026 Texas Instruments Incorporated

5 References

1. Shi-Ping Hsu, A. Brown, L. Rensink, R. Middlebrook *Modelling and Analysis of Switching DC-to-DC Converters in Constant- Frequency Current-Programmed Mode*, PESC '79 Record (IEEE Publication 79CH1461-3 AES), pp. 284-301.
2. E. Pivit, J. Saxarra, *On Dual Control Pulse Width Modulators for Stable Operation of Switched Mode Power Supplies*, Wiss. Ber. AEG-Telefunken 52 (1979) 5, pp. 243-249.
3. R. Redl, I. Novak *Instabilities in Current-Mode Controlled Switching Voltage Regulators*, PESC '81 Record (IEEE Publication 81CH1652-7 AES), pp. 17-28
4. W. Bums, A. Ohri, *Improving Off-Line Converter Performance with Current-Mode Control*, Powercon 10 Proceedings, Paper B-2, 1983.
5. B. Holland, *A New Integrated Circuit for Current-Mode Control*, Powercon 10 Proceedings, Paper C-2, 1983.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 1999) to Revision A (November 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

Copyright © 2026 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025