Application Note

SR Stress Suppression in LLC Converters Under Output Short-Circuit Using UCD3138 Automatic Mode Switching Capability

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Abstract

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In LLC converter applications, the current through the synchronous rectifier (SR) may reverse when the output is short-circuited. When the SR is turned off, inductive energy due to this negative current cannot be released and may put the SR at risk of over-voltage stress. To address this issue, a detailed timing analysis of the abnormal SR stress under output short-circuit is first performed. Based on this, a solution based on the automatic mode switching capability of the UCD3138 digital controller is proposed. This solution, via a hardware-based approach, quickly reduces the SR on-time when a loop change due to output short-circuit is detected, forcing the SR to turn off early before the current crosses zero. This fundamentally avoids the generation of negative current and eliminates the stress risk of SR. Experimental results demonstrate that this approach provides a fast response and reduces the SR stress from 69V to 29.6V, which validates its effectiveness.

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1 Issue Description: Abnormal SR Voltage Stress Under Output Short-Circuit

The LLC resonant converter is widely used due to its high efficiency and soft switching characteristics, and its synchronous rectification (SR) technology can further improve the overall efficiency. However, under extreme failure conditions such as output short-circuit, the SR may be at risk of over-voltage damage due to abnormal operating conditions. This chapter will analyze in particular the phenomenon and root cause of this issue.

1.1 Abnormal Phenomenon: SR Voltage Stress Exceeds the Limit in Short-Circuit Testing

Figure 1-1 illustrates a typical LLC resonant converter topology with a discrete capacitor structure. In the diagram, Q1 and Q2 are primary-side switches, Cr1 and Cr2 are resonant capacitors, Lr is the resonant inductor, Lm is the magnetizing inductor, and SR1 and SR2 are secondary-side synchronous rectifiers.

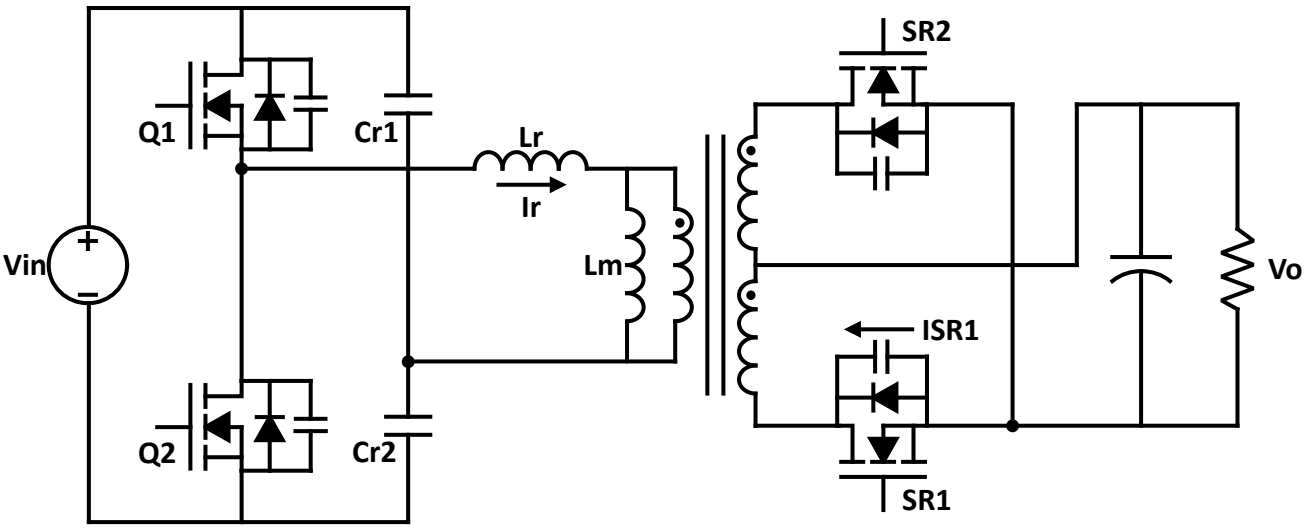

Figure 1-1. LLC Resonant Converter Topology With a Discrete Capacitor Structure

Figure 1-2 shows the waveforms for output short-circuit testing based on the 1kW reference design, the PMP40586. As shown in the figure, when the output is short-circuited, SR1 has an abnormal oscillating peak at its drain-to-source voltage (Vds) upon its turn-off. The maximum stress reaches 69V. This voltage exceeds the device safety margin, posing a risk of damage during repeated short circuits. Therefore, the control timing must be optimized to limit the SR stress within a safe range.

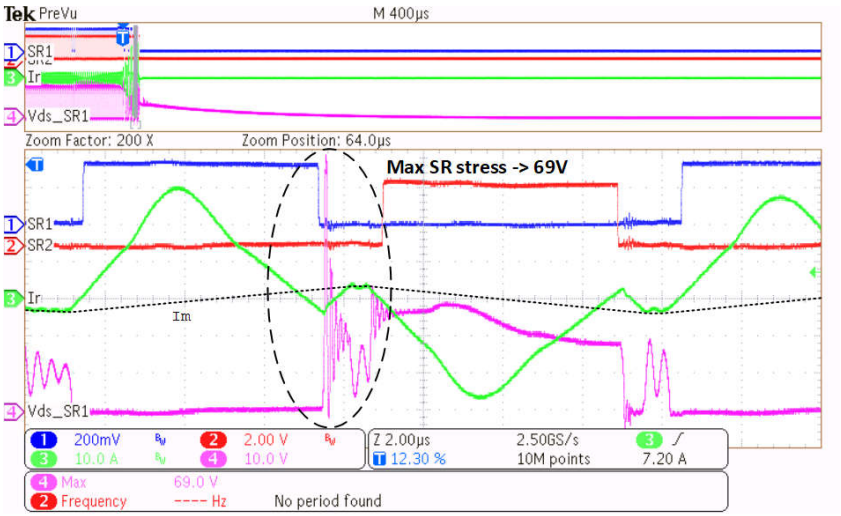

Figure 1-2. Abnormal Waveform of SR Stress Under Output Short-Circuit

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1.2 Root Cause Analysis: Timing Mechanism of Turn-Off Stress Caused by Negative Current

This section provides the basis for subsequent timing optimization by performing a timing analysis of the abnormal SR stress during output short-circuit. The process is divided into five stages (t0-t5).

Stage t0-t1: At t0, the resonant current is equal to the magnetizing current. Because SR1 is still on, its current (ISR1) starts to cross zero and increases in the reverse direction. Here, the black arrow indicates the reference positive direction, and the red arrow indicates the actual current direction.

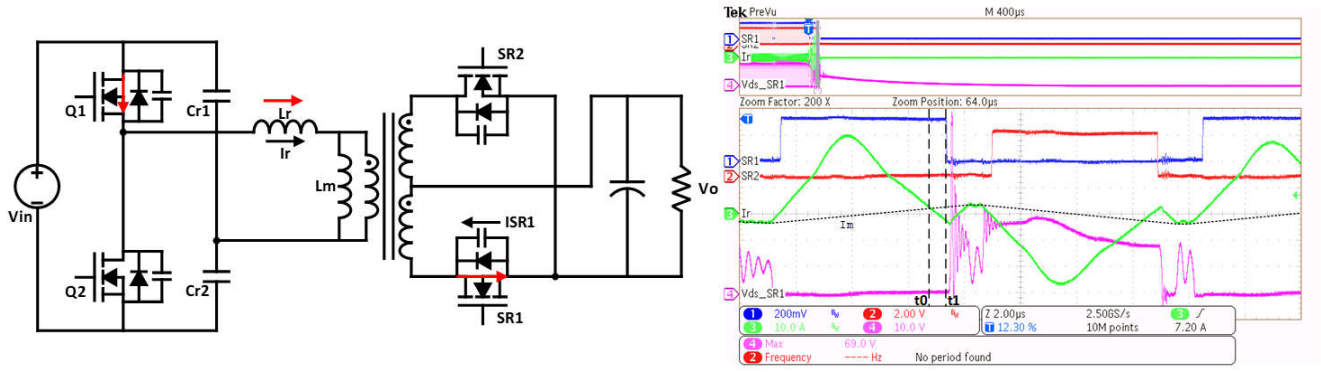

Figure 1-3. Timing Analysis of Abnormal SR Stress - Stage I (t0-t1): Zero Current Crossing and Current Reversal

Stage t1-t2: At t1, the negative current continues to increase due to the turn-off delay.

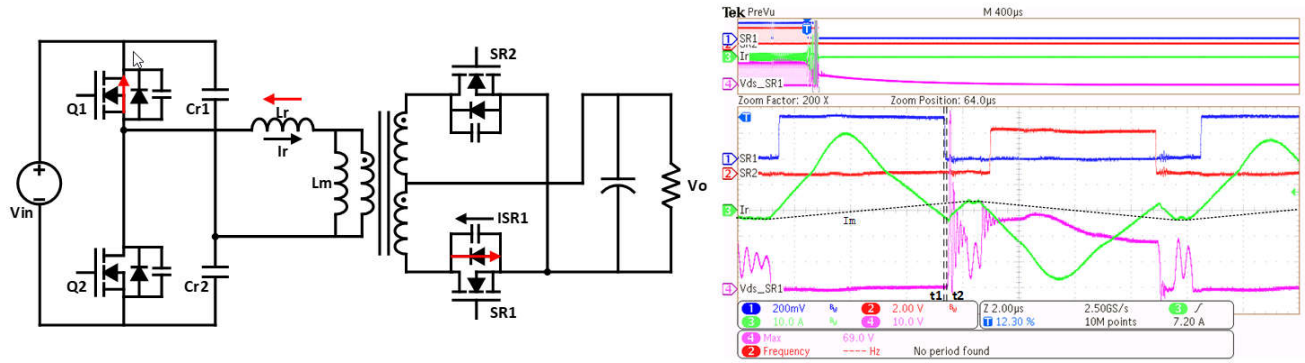

Figure 1-4. Timing Analysis of Abnormal SR Stress - Stage II (t1-t2): The Negative Current Continues to Increase Due to Turn-Off Delay

Stage t2-t3: SR1 is completely turned off at t2. Because the inductive energy stored by the negative current has no release path at this time, the current is forced to freewheel through the SR2 body diode, and the voltage of the transformer's secondary winding is clamped. Simultaneously, the primary-side resonant inductor Lr, the leakage inductor Ls referred to the secondary side, and the output capacitor Csr of SR1 form a resonant tank with a resonant frequency of fr1. According to the design parameters of the PMP40586 reference design (Csr=4,000pF, n=16, Lr=15µH, Lm=150µH, and the leakage inductance Ls estimated to be 1% of the magnetizing inductance, that is, Ls = (Lm * 1%) /n²), fr1 is approximately 9.912MHz.

$$fr1 = 1/\left[2\pi * sqrt\left(\left(Lr/n^2 + Ls\right) * Csr\right)\right] = 9.912MHz \quad (1)$$

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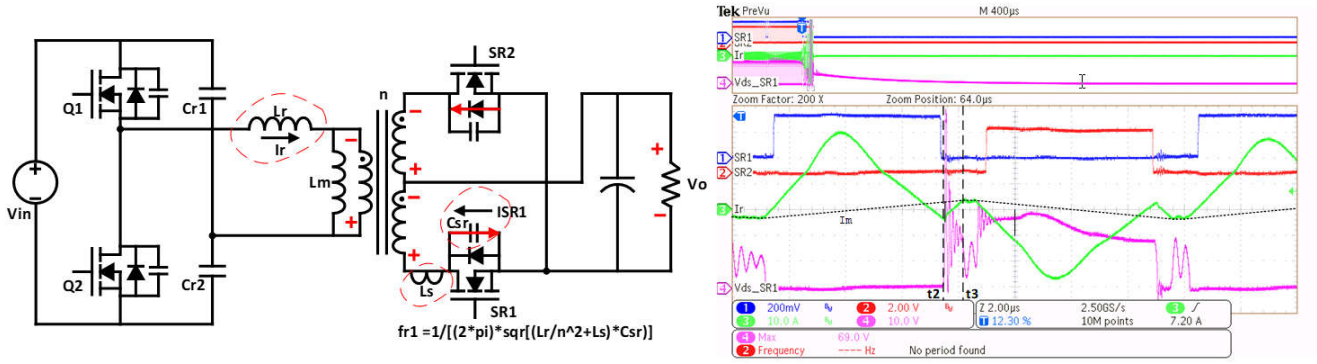

Figure 1-5. Timing Analysis of Abnormal SR Stress - Stage III (t2-t3): Winding Clamping and First Resonance (fr1)

Stage t3-t4: At t3, leakage inductance energy is completely released, the transformer winding voltage is unclamped, and the magnetizing inductor Lm begins to participate in resonance. In this case, Lr, Lm, Ls, and Csr are resonating together, and the resonant frequency becomes fr2, which is approximately 3.12MHz.

$$fr2 = 1/\{2\pi * sqrt[(Ls + Lm/n^2 + Lr/n^2) * Csr]\} = 3.12MHz \quad (2)$$

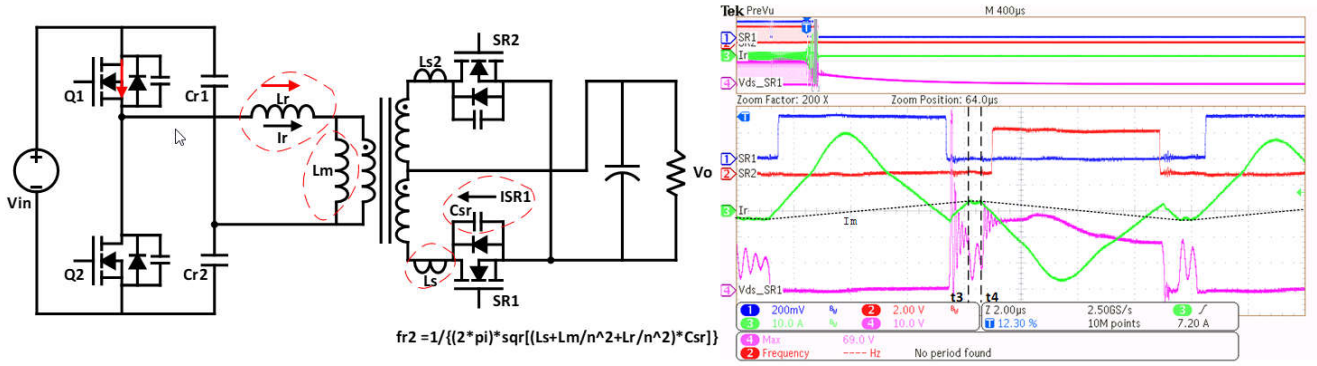

Figure 1-6. Timing Analysis of Abnormal SR Stress - Stage IV (t3-t4): The Magnetizing Inductor Participates in Resonance (fr2)

Stage t4-t5: At t4, the primary-side switch Q1 is turned off, the SR2 body diode conducts and clamps the winding voltage again, and the resonant tank reverts to Lr, Ls, and Csr, with the resonant frequency being fr1.

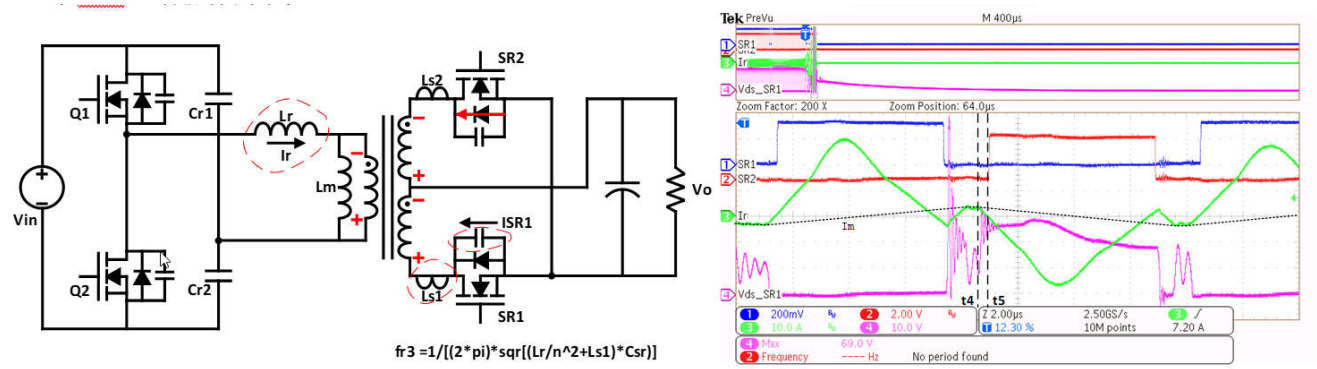

Figure 1-7. Timing Analysis of Abnormal SR Stress - Stage V (t4-t5): Primary-Side Turn-off and Resonance Return (fr1)

A comprehensive analysis shows that abnormal voltage stress is mainly generated in Stage t2-t3. The root cause is that the SR fails to turn off in time before the current crosses zero after an output short-circuit, resulting

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in a large negative current. When the SR is turned off, the leakage inductance energy corresponding to this negative current is released through the resonant process with the SR parasitic capacitor, creating a high voltage spike across the SR.

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2 Solution: SR Stress Optimization Based on the UCD3138 Automatic Mode Switching Capability

For the above analysis, the key to addressing the issue is to prevent negative current from flowing through the SR. The traditional method of adjusting the SR on-time through software is too slow to respond in a timely manner. In this article, we propose a hardware-based solution based on the UCD3138 automatic mode switching capability to quickly adjust the action of the SR when a short circuit is detected.

2.1 Key Technology: Principle of the UCD3138 Automatic Mode Switching Capability

The DPWM module configuration of the UCD3138 is controlled by multiple sets of registers. As shown in Figure 2-1, the Control Register 0, Auto Config Mid, and Auto Config High register sets all contain DPWM parameters. When automatic mode switching is enabled, the system automatically switches among these three sets of configurations based on the magnitude of the real-time loop (Filter Duty value).

To achieve smooth switching and prevent oscillations, the capability has a built-in hysteretic comparator. There are four threshold points:

- When the Filter Duty value increases, the switching point is determined by the High-Lower Threshold and Low-Lower Threshold.
- When the Filter Duty value decreases, the switching point is determined by the High-Upper Threshold and Low-Upper Threshold.

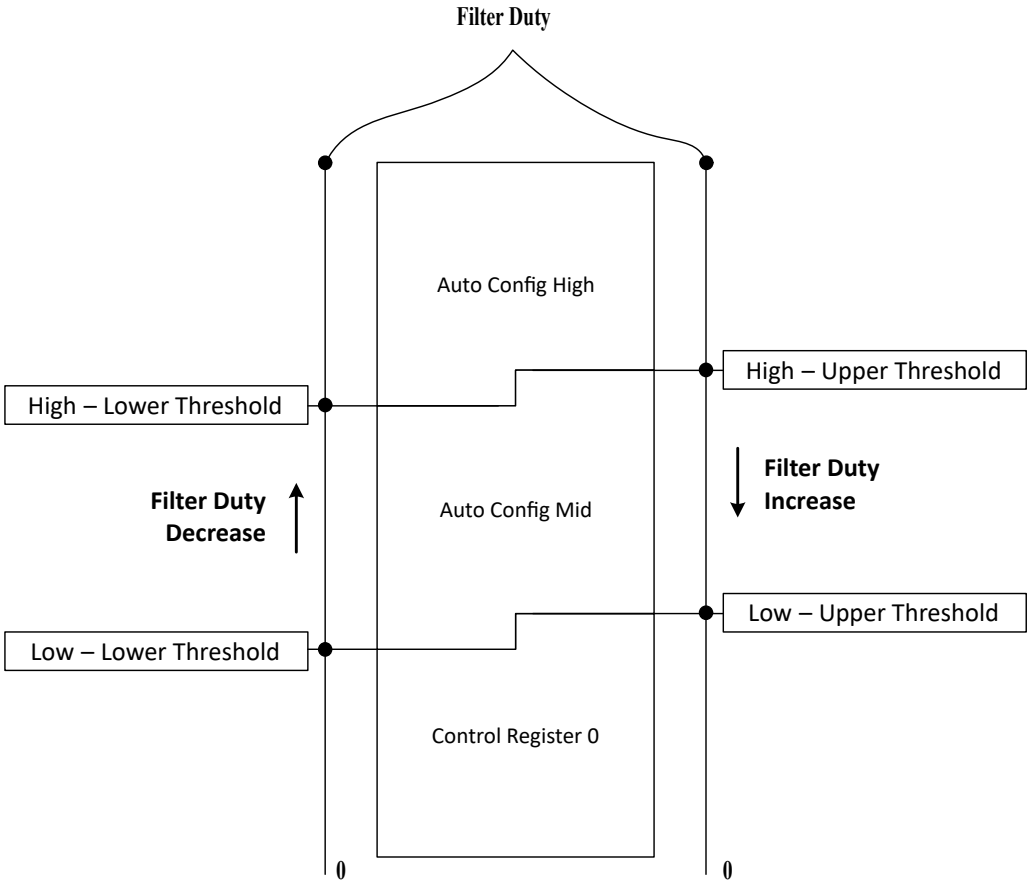

Figure 2-1. Schematic Diagram of the UCD3138 Automatic Mode Switching Mechanism

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2.2 Solution Implementation: Dynamically Adjusting the Control Timing of the SR On-Time With Mode Switching

This solution utilizes the automatic mode switching capability of the UCD3138 to set different operating modes for the SR, as shown in Figure 2-2:

- Light-load/standby mode (Filter Duty < Low-Lower Threshold): DPWM is configured by Control Register 0, and the SR is set to off.
- Normal operating mode (Low-Lower Threshold < Filter Duty < High-Lower Threshold): DPWM switches to be configured by the Auto Config Mid register set. At this point, the maximum SR on-time is set to Time1 (typically close to and slightly less than half the resonant period) to achieve high-efficiency synchronous rectification.
- Output short-circuit/overload mode (Filter Duty > High-Lower Threshold): When the output is short-circuited, the loop adjusts rapidly, causing the Filter Duty to increase dramatically. Once the High-Lower Threshold is exceeded, DPWM immediately switches to be configured by the Auto Config High register set. In this mode, the maximum SR on-time can be set to a smaller value, Time2.

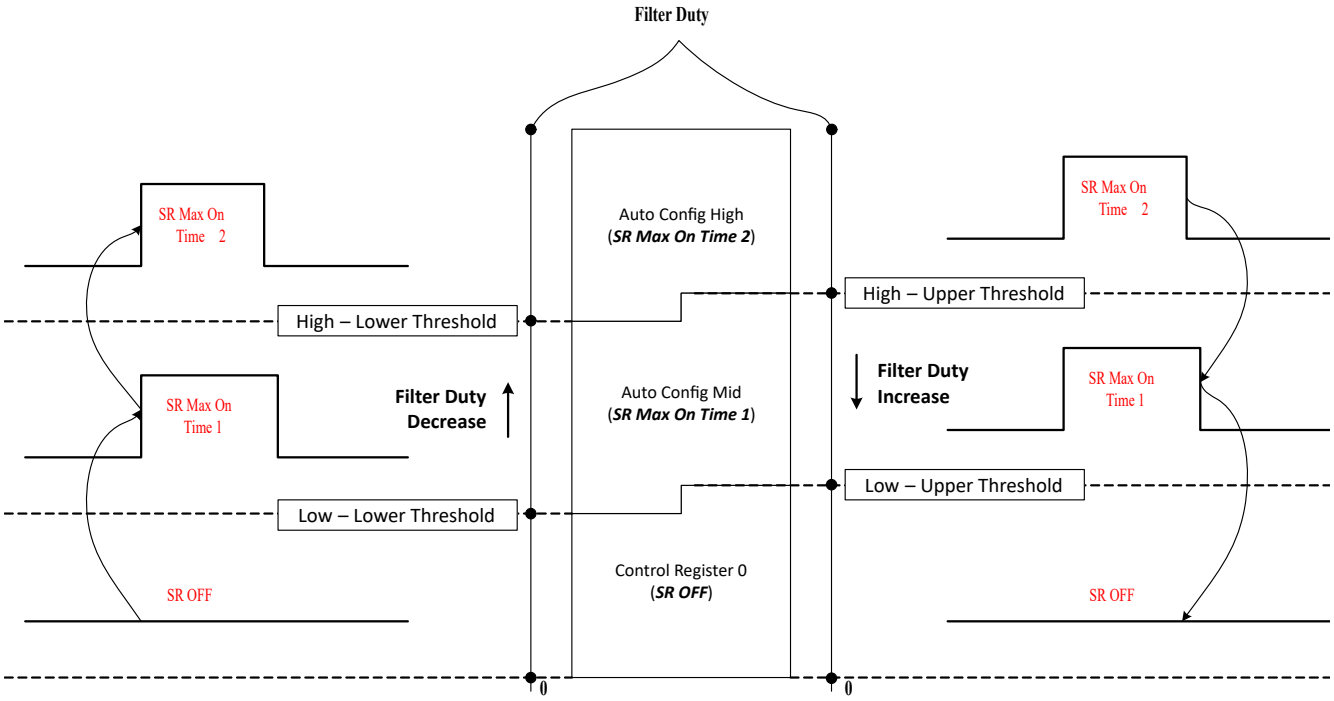

Figure 2-2. Register Configuration Relationship Diagram for Automatic Mode Switching Used for SR Control

Figure 2-3 shows the timing diagram for the SR stress optimization solution, where the SR is operating normally before the output is short-circuited, with its on-time configured by the Auto Config Mid register set to Time1. After the output is short-circuited, the loop output (Filter Duty) ramps up quickly, and when it is greater than the set switching threshold, the High-Lower Threshold, the SR will enter the output short-circuit/overload mode, and its on-time will also be switched to the value controlled by the Auto Config High register set, Time2. The core mechanism is to set Time2 properly so that during output short-circuits, the SR drive signal is forced off before the resonant current crosses zero and becomes negative (as shown in Figure 3-3). Since the SR is turned off before the current reverses, the generation of negative current is fundamentally prevented, thus avoiding voltage stress due to the resonant release of leakage inductance energy as well as possible risk of failure.

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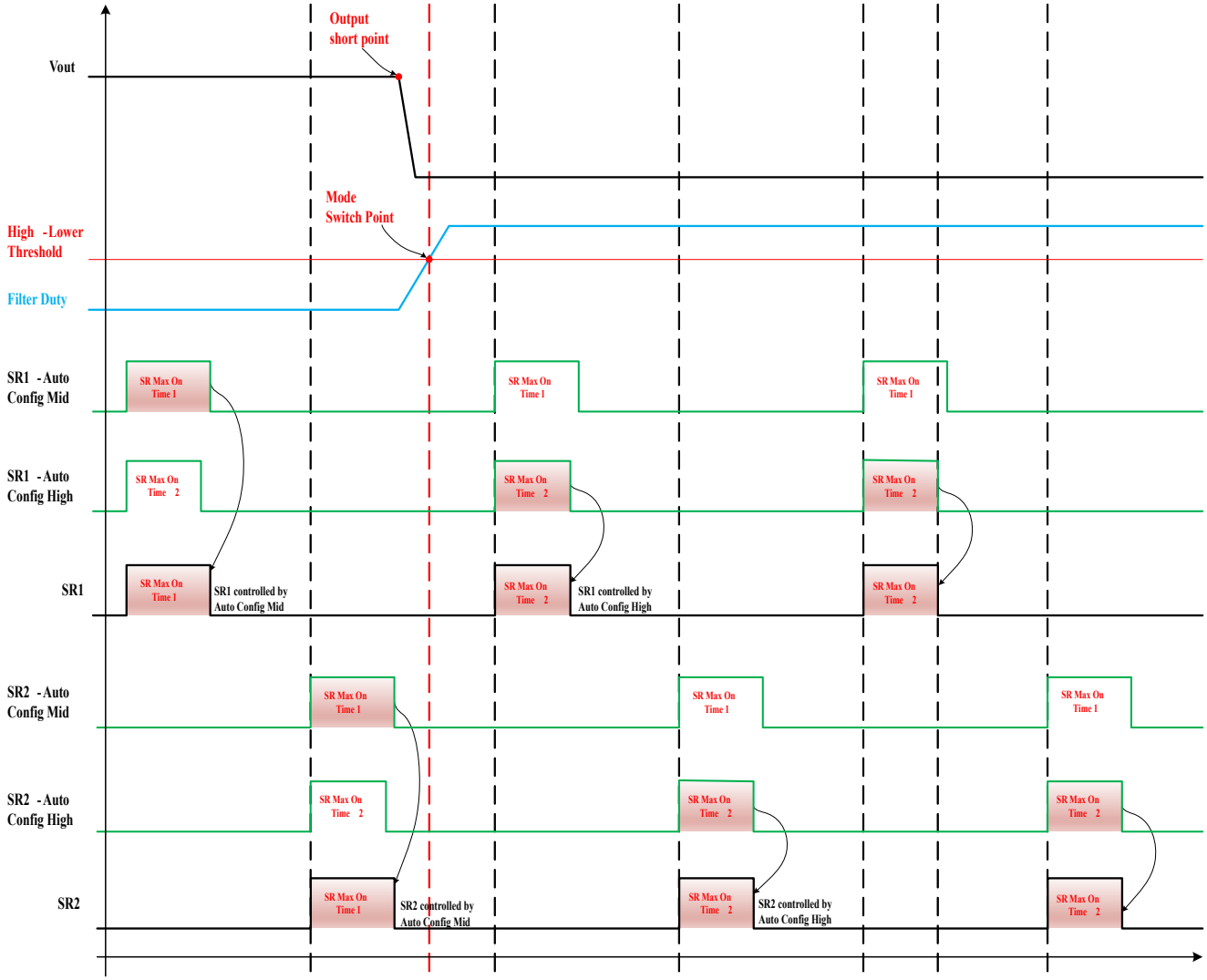

Figure 2-3. Timing Diagram for the SR Stress Optimization Solution Based on Automatic Mode Switching

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3 Experimental Verification: Effectiveness Testing of the Optimization Solution

To verify the above solution, tests were performed on the PMP40586 reference design platform.

3.1 Result Comparison: SR Stress Reduced From 69V to 29.6V

To verify the effectiveness of the above solution, tests were performed on the PMP40586 reference design platform. Figure 3-1 shows the waveforms for output short-circuit testing after optimization using the automatic mode switching capability. It is clearly shown that the maximum voltage stress across the SR is limited to 29.6V, which is significantly lower than the 69V (Figure 1-2) before optimization and is within the safe operating range of the device.

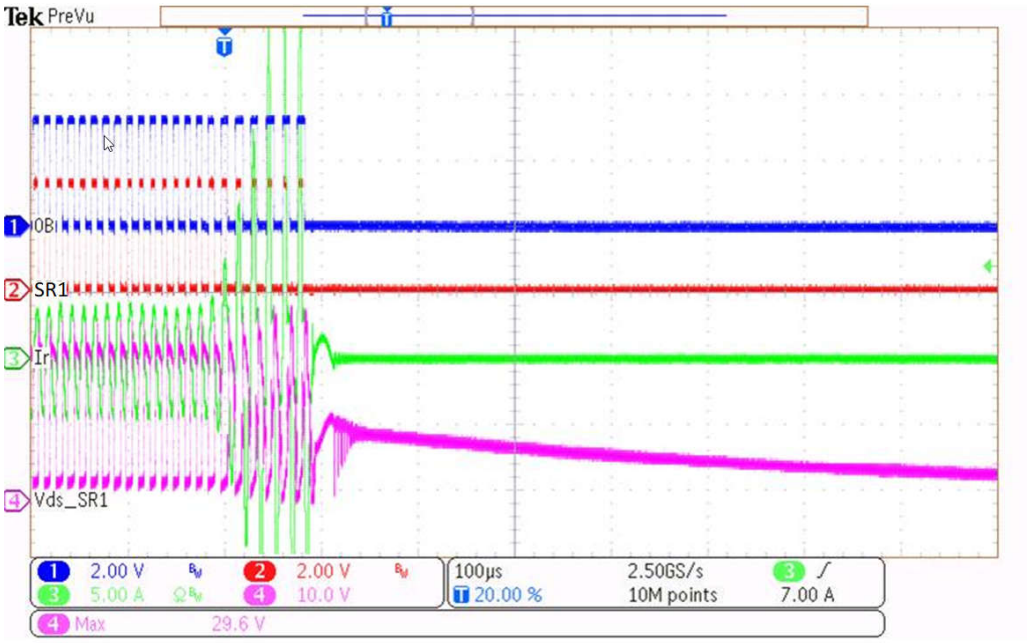

Figure 3-1. SR Stress Waveform Under Output Short-Circuit Using the Optimization Solution

3.2 Waveform Analysis: Dynamic Switching of the SR On-Time and Early Turn-Off

The waveforms in Figure 3-2 clearly show that the SR on-time is switched from Time1 to Time2 (inside the black dashed box) after the short-circuit event, verifying the fast response and execution of the automatic mode switching capability.

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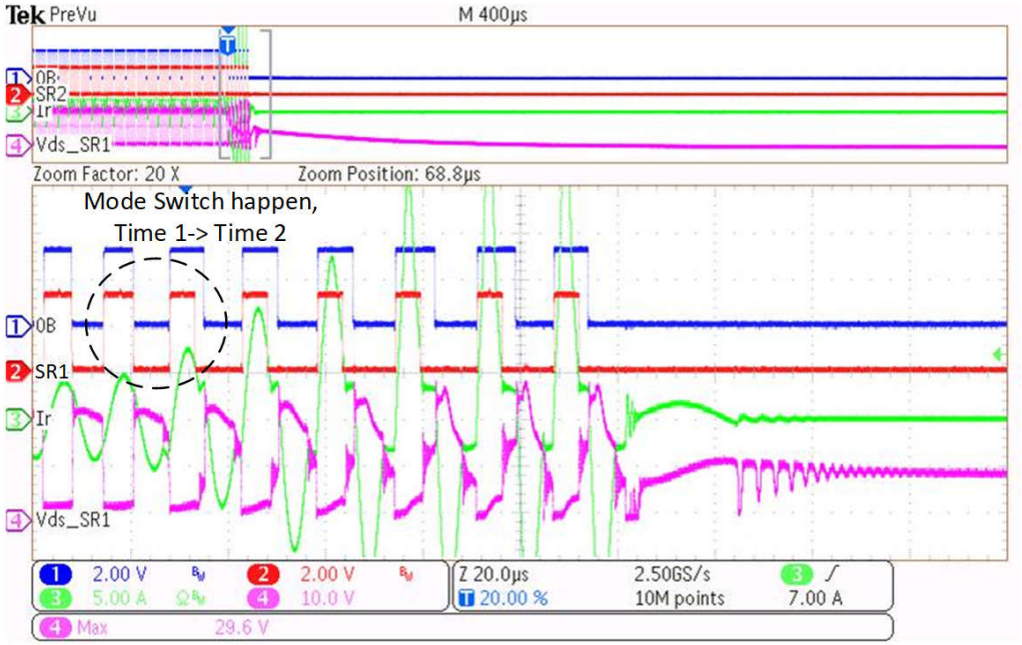

Figure 3-2. Waveform of Dynamic Switching of the Maximum SR On-Time Using Automatic Mode Switching

In Figure 3-3, the early SR drive signal turn-off is visualized in detail. As shown by the waveforms, this solution successfully prevents the generation of negative current, thus demonstrating its effectiveness.

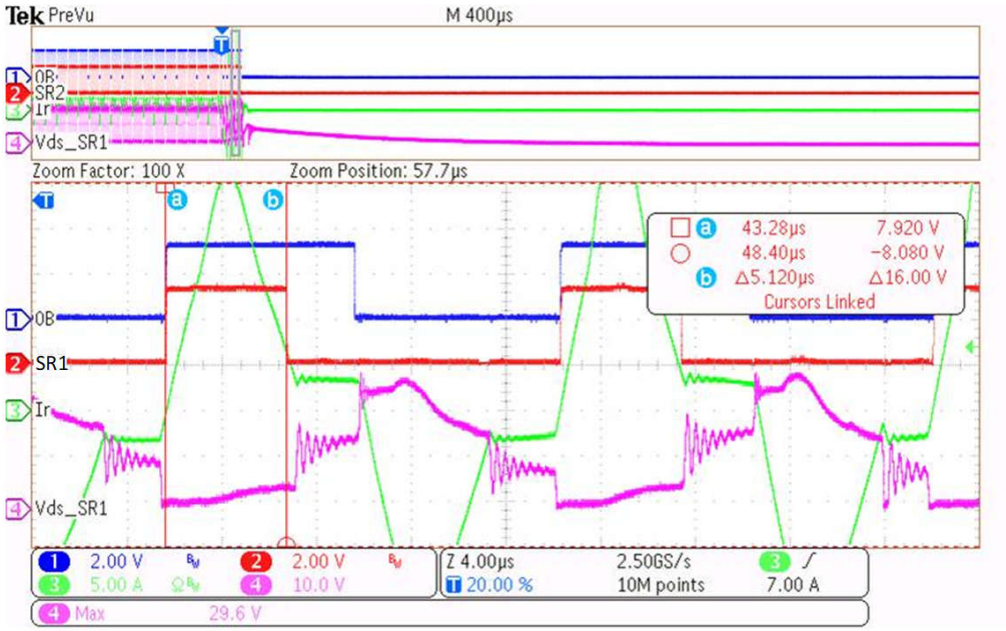

Figure 3-3. Illustrative Waveform of Early SR Drive Signal Turn-Off to Avoid Negative Current

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4 Conclusion

In this article, we analyzed in depth the mechanism of stress caused by negative SR current during output short-circuit in LLC converters. We also proposed and implemented an innovative hardware-based solution based on the UCD3138 automatic mode switching capability. This solution dynamically reduces the maximum SR on-time by monitoring the loop signal, leveraging hardware to quickly switch the DPWM configuration when a short circuit is detected, forcing the SR to turn off before the current crosses zero. This eliminates negative current and its resulting voltage stress. Experimentally proven, this solution achieves single-switching-cycle response, reducing the short-circuit stress from 69V to 29.6V, thereby providing an effective and practical reference for the short-circuit protection design of high-reliability LLC converters.

5 References

1. UCD31xx Digital Power Supply Controller Family - Technical Reference Manual.
2. Reference design - PMP40586.

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