

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric1	FR-4 High Tg	59.20mil	4.8	
2	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

**DESIGN INFORMATION**

MIN. TRACK WIDTH: 6 MIL  
 MIN. CLEARANCE: 7.974 MIL  
 MIN. VIA PAD SIZE: 24 MIL  
 MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

**MATERIAL:**  
 FR-408  FR-4 High Tg  OTHER \_\_\_\_\_  
 THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_  
 TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_  
 BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

**DRILLING:**  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

**BOARD FINISH:**  
 SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER RED  
 MATTE  SEMI-GLOSS

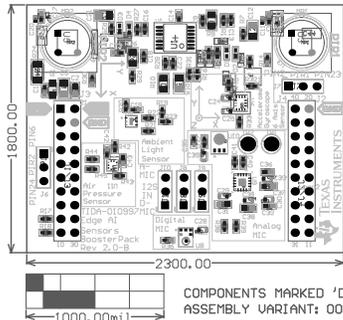
**SURFACE FINISH:**  IMMERSION GOLD (ENIG)  ENEPG  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

**ARRAY/PANEL:**  CUT AND TRIM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

**CERTIFICATION:** MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS ->  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL D NUMBER

**ADDITIONAL REQUIREMENTS:**  
 MICROSECTION:  YES  
 BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT NAME = TIDA-01097_Edge_AI_Sensor_BoosterPack	BOARD REF ID = TIDA-01097	DATE = 3/18/2020	DESIGNER = SUN JIN	DESIGNED BY = SUN JIN	DESIGNED DATE = 3/18/2020	DESIGNED TIME = 10:00:00	DESIGNED LOCATION = TMS
LAYER NAME = TOP	TID #: N/A	#: 011					
PLT W/ NAME = TOP	ASSEMBLY VARIANT: 001	GENERATED DATE: 3/18/2020	4:31:56 PM	PLT W/ NAME = TOP	ASSEMBLY VARIANT: 001	GENERATED DATE: 3/18/2020	4:31:56 PM

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ENGINEER: Kong Jin	LAYOUT BY: Kong Jin
SCALE: 0.70	ALTIUM DESIGNER VERSION: 25.8.1.18

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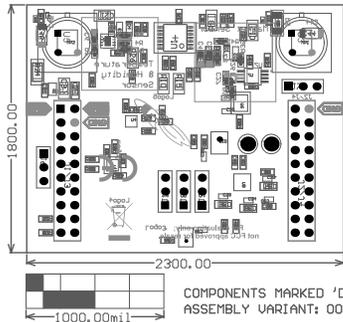
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COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED.  
 ASSEMBLY VARIANT: 001

PCB: 001	BOARD: 001	DATE: 3/18/2023	DESIGNER: J. B. S.	TEXAS INSTRUMENTS
LAYER NAME = Bottom	TID #: N/A	REV: 001	DATE: 3/18/2023	DESIGNER: J. B. S.
PLT: 001				

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ENGINEER: Kong Jin	LAYOUT BY: Kong Jin
SCALE: 0.70	ALTIUM DESIGNER VERSION: 25.8.1.18

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Last updated 10/2025