Wide Range Input TPS40055 Converter Delivers 5 Volts at 2 Amps

User’s Guide

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System Power

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1 Introduction

The TPS40055EVM−002 wide range input dc-to-dc converter uses the TPS40055 synchronous rectifier controller to step down a 10-V to 40-V input to 5 V. The output current is 3 A with an input of 10 V and should be linearly derated to 2 A at V_{IN} = 40 V. The TPS40055 is used because it offers a variety of user programmable functions such as operating frequency, soft start, voltage feed-forward, high-side current limit, and external loop compensation. This controller provides a regulated 10-V gate drive supply which feeds the bootstrap charging circuit for the high-side N-channel MOSFET along with a driver for the low-side synchronous rectifier MOSFET. The device operation is specified in the TPS40055 datasheet[1].

2 Features

- Operates from an input source varying from 10 V_{DC} to 40 V_{DC}
- Output current 3 A with V_{IN} = 10 V, 2 A with V_{IN} = 40 V
- Low cost high voltage conversion

3 Schematic

The schematic for TPS40055EVM−002 is shown in Figure 1.

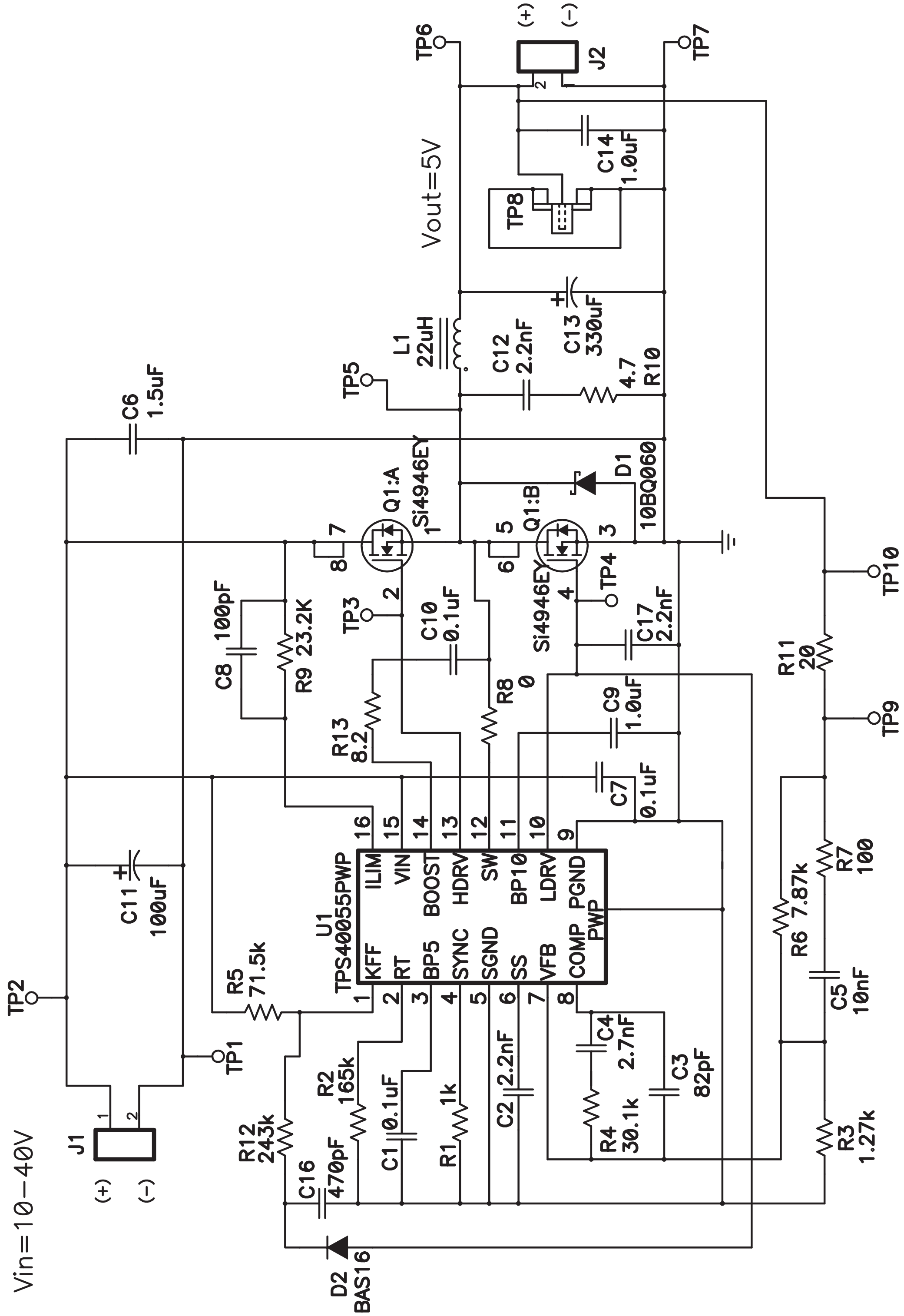


Figure 1. HPA071 Schematic

4 Component selection

4.1 TPS40055 Device Selection

The TPS4005x family of parts offers a range of output current configurations including source only (TPS40054), source/sink (TPS40055), or source/sink with V_{OUT} prebias (TPS40057). In this converter the TPS40055 with source/sink capability is selected. This serves to maintain continuous inductor ripple current all the way to zero load to improve the small signal loop response by preventing the inductor current from transitioning to the discontinuous current mode.

The TPS4005X family is packaged in TI's PWP PowerPAD™ thermally enhanced package which should be soldered to the PCB using standard solder flow techniques. In the PowerPAD™, a thermally conductive epoxy is used to attach the integrated circuit die to the leadframe die pad, which is exposed on the bottom of the completed package. The PWP PowerPAD™ package has a θ_{JC} = 2°C/W which helps keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra small packaging while maintaining high component reliability.

The Texas Instrument Technical Brief, PowerPAD™ Thermally Enhanced Package Application Report[2] should be consulted for more information on the PowerPAD™ package.

4.2 Frequency of Operation

The clock oscillator frequency for the TPS40055 is programmed with a single resistor from RT (pin 2) to signal ground. The following equation (1) from the datasheet allows selection of RT in kΩ for a given switching frequency in kHz.

$$R_T = R2 = \frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23\ k\Omega \tag{1}$$

For 300-kHz RT is selected to be 165 kΩ.

In addition to programming the operating frequency, the PWM ramp time must be programmed via the resistor R_{KFF} up to V_{IN}. Also, the selection of R_{KFF} programs the V_{IN} voltage at which the circuit starts operation. This helps keep the circuit from starting at low voltages, which can lead to current flow larger than desired. Now, R_{KFF} is programmed using equation (2)

$$R_{KFF} = R5 = \left(V_{IN(min)} - 3.5\right) \times \left(58.14 \times R_T + 1340\ k\Omega\right) \tag{2}$$

where $V_{IN(min)}$ should be the minimum startup input voltage, and R_T is in kΩ. Note that internal tolerances have been incorporated into this equation, so the actual $V_{IN(min)}$ of the input voltage should be used here. For 300-kHz R_{KFF} is selected to be 71.5 kΩ.

4.3 UVLO circuitry

The user programmable UVLO built into the TPS4005X provides hysteresis for transients shorter than a total count of seven cycles. If the input voltage to the converter can be slowly rising around the minimum V_{IN} range, external hysteresis can be incorporated to prevent multiple on/off cycles during startup or shutdown. These on/off cycles are a result of line impedance external to the EVM causing V_{IN} to the module to drop when under load, causing the programmable UVLO threshold to be crossed repetitively.

In this converter, C16 and D2 are added to form a peak detector from the lower gate drive which is only active when the converter is operating. This provides a bias source to deliver hysteresis current from the peak detector voltage through R12 to the lower KFF voltage of 3.5 V, enabling one to alter the programmable UVLO shutdown point. The bias is not present during startup, so the circuit starts as expected from the R_{KFF} calculation.

In this application, R12 is selected to provide a hysteresis current of 20% I_{KFF} and can be calculated from

$$R_{HYS} = R12 = \frac{R_{KFF} \times \left(V_{PD} - 3.5\right)}{0.2 \times \left(V_{IN(min)} - 3.5\right)} \tag{3}$$

where V_{PD} is the voltage on the peak detector, and $V_{IN(min)}$ is the desired start voltage used in the determination of R_{KFF}. In our typical case, V_{PD} = 8 V, and R12 is found to be 247 kΩ, and a standard value of 243 kΩ is selected. Testing shows the startup voltage to be 9.2 V, and the shutdown voltage to be 8.5 V.

4.4 Inductance value

The output inductor value for a buck converter can be selected from equation (4).

$$L = \frac{V_{OUT}}{f \times I_{RIPPLE}}\left(1 - \frac{V_{OUT}}{V_{IN(min)}}\right) \tag{4}$$

in which I_{RIPPLE} is usually chosen to be in the range of 10% to 40% of I_{OUT}. With I_{RIPPLE} = 20% of $I_{OUT(max)}$ there is a ripple current of 0.6 A, and the inductance value is found to be 24 µH for a maximum V_{IN} of 40 V. In a wide range V_{IN} design the inductor value selection involves a lot of compromise. This design specifically targets the higher voltage range of operation attainable with the TPS40055 controller, so a standard value 22-µH inductor is selected. With a 22-µH inductor, the ripple current with V_{IN} = 10 V is 0.38 A, and the ripple with V_{IN} = 40 V is 0.66 A. Using the larger inductor at lower voltages helps to reduce the number of output capacitors required to meet the output noise specification, as discussed in a later section. If the input range was constrained to a lower voltage range such as 10 V to 16 V a smaller inductor would be selected.

A ferrite drum core with a surface mount carrier provides a low-cost solution inductors in this inductance/current range. Inductors rated 22 µH are available in a couple of sizes, with the larger versions generally rated to carry higher saturation current, which is the current for 30% inductor value rolloff. In this example an inductor with a ½ inch diameter drum core is selected because the saturation current is rated 7.6 A. The next physically smaller inductor has a saturation rating of 3.7 A, and does not allow sufficient margin for the tolerances in the current limit circuitry.

4.5 Input capacitor selection

The bulk input capacitor selection is based on several factors such as size, cost, and meeting voltage ripple requirements. There are multiple configurations of various capacitor technologies that can function in the application. In this example the goal is to achieve reduced overall cost in the solution provided.

The RMS current required by the power stage will be supplied by both the onboard capacitance and the input source, with the relative impedances determining the magnitude of RMS current carried by each component. In typical applications, this reference design would be fed from an upstream dc-to-dc converter with its own bulk output capacitance, so the impedance presented to this converter could be rather low and less onboard capacitance would be required. On the other hand, if conductors used to bring input power to this converter have high series impedance then the onboard capacitors would be forced to carry more of the RMS ripple current, and capacitors with higher current rating would be needed.

The maximum RMS current required for the buck power stage can be estimated as shown in equation (5),

$$I \approx I_{OUT} \times \sqrt{D} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} = 3 \times \sqrt{\frac{5}{10}} = 2.1\ A \qquad (5)$$

It is also important to consider a minimum capacitance value which would limit the voltage ripple to a specified value if all the current is supplied by the onboard capacitor. For a typical ripple voltage of 150 mV the minimum capacitance is calculated in equation (6) as:

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{I \times V_O}{\Delta V \times V_{IN} \times F_S} = \frac{3.3\ A \times 5\ V}{0.5\ V \times 10\ V \times 300\ kHz} = 11\ \mu F \qquad (6)$$

Initially, this design was fitted with a ceramic capacitor rated 10 µF, 50 V because some of the current would also be supplied from the input source, limiting the voltage ripple to a value below the estimate. However, when testing with a fast switch-on time there was voltage overshoot of 15 V to 20 V above the input source voltage. This is a result of parasitic inductance in series with the input source interacting with the low-ESR ceramic capacitor. To eliminate this issue the capacitor was changed to a 1.5-µF, 50-V ceramic capacitor in parallel with a 100-µF aluminum electrolytic capacitor.

The 1.5-µF ceramic capacitor C6 is positioned as a power bypass component located close to the MOSFET packages to keep the high frequency current flow in a small, tight loop. The 100-µF capacitor C11 has an ESR of 0.35 Ω, max which serves to dampen out the transient overshoot.

4.6 Output capacitor selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. The minimum allowable output capacitance is determined by the amount of inductor ripple current and the allowable output ripple, as given in equation (7)

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} = \frac{0.66\ A}{8 \times 300\ kHz \times 15\ mV} = 18\ \mu F \tag{7}$$

In this design, $C_{OUT(min)}$ is 18-µF with V_{RIPPLE} = 15 mV. However, this only affects the capacitive component of the ripple voltage, and the final value of capacitance is generally influenced by ESR and transient considerations. To limit the voltage to 15 mV, the capacitor ESR should be less than equation (8),

$$R_C \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{15\ mV}{0.66\ A} = 0.023\ m\Omega \tag{8}$$

An additional consideration in the selection of the output inductor and capacitance value can be derived from examining the transient voltage overshoot which can be initiated with a load step from full load to no load. By equating the inductive energy with the capacitive energy the equation (9) can be derived:

$$C_O = \frac{L \times I^2}{V^2} = \frac{L \times \left(I_{OH}{}^2 - I_{OL}{}^2\right)}{\left(V_f{}^2 - V_I{}^2\right)} = \frac{22\ \mu H \times (3\ A)^2}{(5.1\ V)^2 - (5.0\ V)^2} = 196\ \mu F \tag{9}$$

where I_{OH} = full load, I_{OL} = no load, V_f = allowed transient voltage rise, and V_I = initial voltage. In this 3-A design the capacitance required for limiting the transient is significantly larger than the capacitance required to keep the ripple acceptably low. A single 330-µF POSCAP capacitor C13 is installed in parallel with a 1-µF ceramic capacitor.

4.7 MOSFET selection

This wide range design required selection of a MOSFET capable of withstanding the maximum input voltage of 40 V, and still capable of carrying the maximum load current of 3 A without overheating. This low cost design uses a single SO-8 package which contains two MOSFETs, each rated for 55 V, and an $R_{DS(on)}$ of 55mΩ.

In a synchronous buck converter the fast-rising switch node voltage drives current through the drain-gate and gate-source capacitance of the synchronous rectifier. This can raise the gate of the lower MOSFET to threshold level even though the gate driver is attempting to hold the gate low.[3] C17 is added to the gate of Q1:B to increase the capacitance ratio between the gate-source and drain-gate, reducing the voltage which appears on the lower MOSFET gate.

4.8 Short circuit protection

The TPS40055 implements short circuit protection by comparing the voltage across the topside MOSFET while it is ON to a voltage developed across R_{LIM} due to an internal current source of 10 μA inside pin 16. Both of these voltages are negative with respect to V_{IN}. From the datasheet equation, R_{LIM} is defined as:

$$R_{LIM} = R9 = \frac{I_{OC} \times R_{DS(on)}}{1.12 \times I_{SINK}} + \frac{V_{OS}}{I_{SINK}} \ \Omega \tag{10}$$

Here, I_{OC} is the overcurrent set point equal to the dc output current plus one half the inductor ripple current, V_{OS} is the overcurrent comparator offset, and I_{SINK} is the current into the I_{LIM} pin 16. Using worst case tolerances the value of R_{LIM} should be maximized to ensure that the converter can deliver full rated current under all conditions. Looking at worst case conditions, R_{LIM} = R9 is found to be:

$$R_{LIM} = \frac{(3\text{ A} + 0.3\text{ A}) \times (55\text{ m}\Omega \times 1.4)}{1.12 \times 8.65\ \mu\text{A}} + \frac{-23\text{ mV}}{8.65\ \mu\text{A}} = 23.5\text{ k}\Omega \tag{11}$$

The standard value of 23.5 kΩ was selected. This ensures that we can deliver a minimum of 3 A before current limit is activated. There is also a small capacitor, C8, placed in parallel with R9 to filter the signal.

4.9 Snubber component selection

The junction of Q1, Q2, and L1 rises fast enough to contribute to dV/dT induced voltage on the gate of Q1:B. A snubber consisting of C12 and R10 is added to slow down the rise time of the switch node.

4.10 Compensation components

The TPS40055 uses voltage mode control in conjunction with a high frequency error amplifier. The power circuit L/C double pole corner frequency fc is situated at 1.8 kHz. The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed at the origin to improve dc regulation.

The two zeros are placed near 1.96 kHz,

$$f_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_4} \tag{12}$$

and

$$f_{Z2} = \frac{1}{2 \times \pi \times \left(R_6 + R_7\right) \times C_5} \tag{13}$$

The second pole is placed at 66 kHz,

$$f_{p1} = \frac{1}{2 \times \pi \times R_4 \left(\frac{C_3 \times C_4}{C_3 + C_4}\right)} \tag{14}$$

and the third pole is placed at 159 kHz, which is near one-half of the switching frequency.

$$f_{p2} = \frac{1}{2 \times \pi \times R_7 \times C_5} \tag{15}$$

5 Test Setup

Figure 2 illustrates the basic test setup needed to evaluate the TPS40055EVM−001.

5.1 DC Input Source

The input voltage source should be capable of supplying from 10 V_{DC} to 40 V_{DC} and rated for at least 3 A of current. For best results the input leads should be made with a wire of 22 gauge or larger wire.

5.2 Output Load

The output load can be either an electronic load or a resistive load configured to draw between 0 A and 3 A. The output leads should be made with a wire of 20 AWG or larger diameter wire. A voltmeter should be connected to TP6 and TP7 to monitor the output voltage on the PCB.

5.3 Oscilloscope Probe Test Jacks

An oscilloscope probe test jack (TP8) has been included to allow monitoring the output voltage ripple.

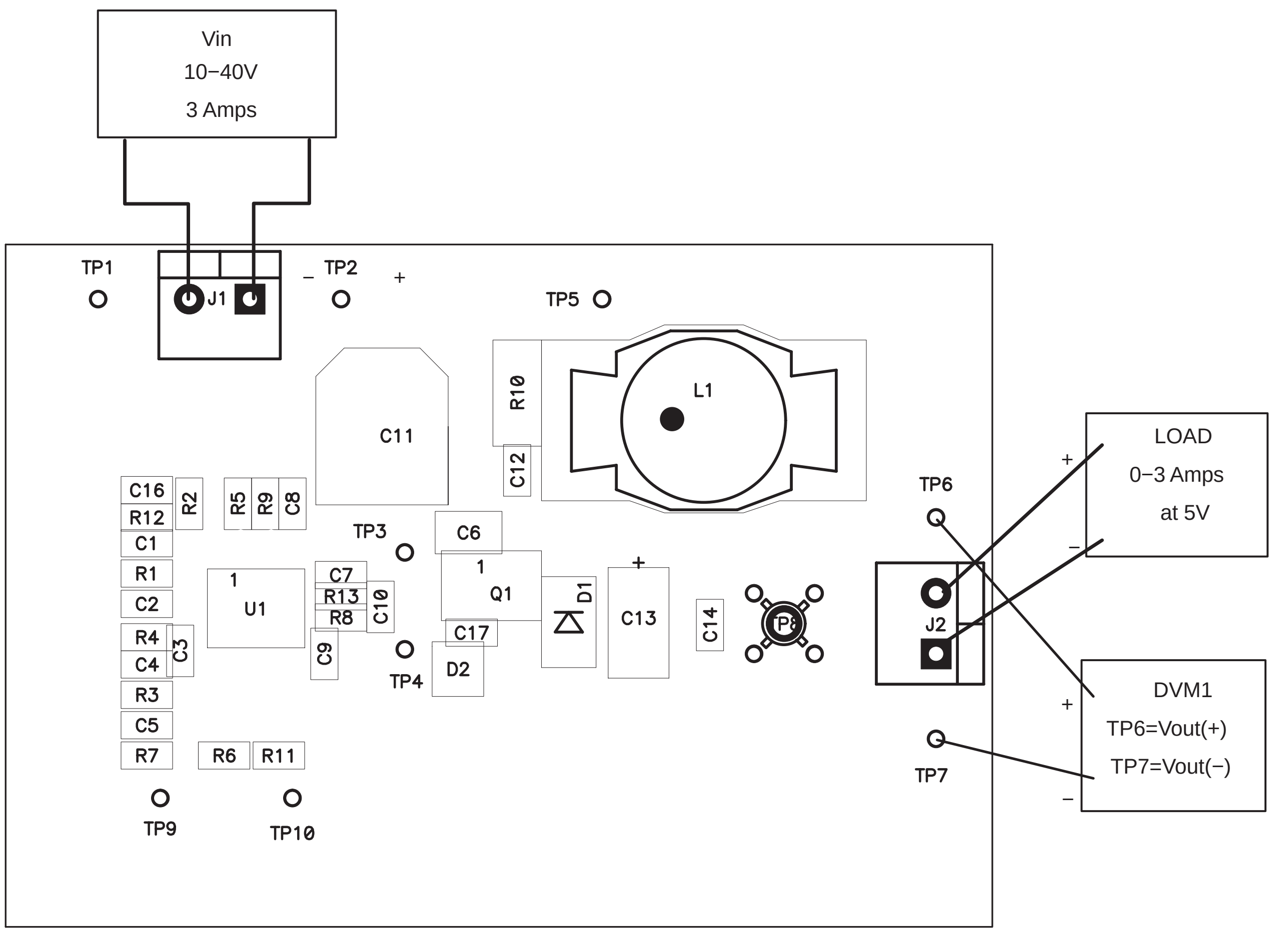


Figure 2. Test Setup

6 Test Results/Performance Data

6.1 Efficiency

Figure 3 shows the efficiency as the load is varied from 0.5 A to over 3 A.

6.2 Closed loop performance

The TPS40055 uses voltage mode control with feed-forward in conjunction with a high frequency error amplifier to implement closed loop control.

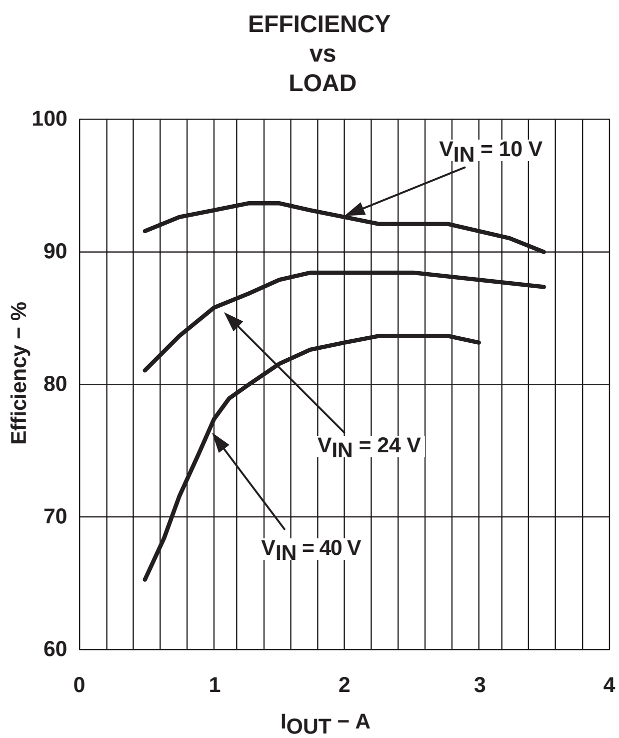


Figure 3

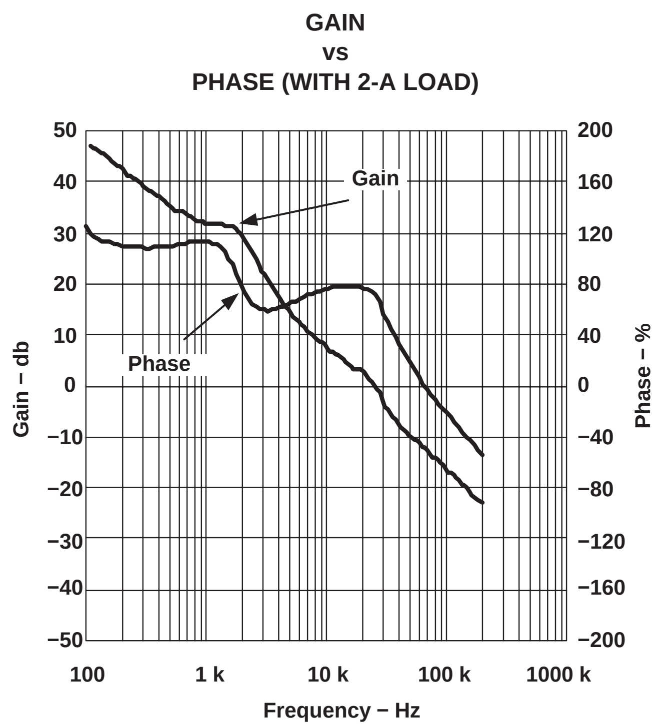
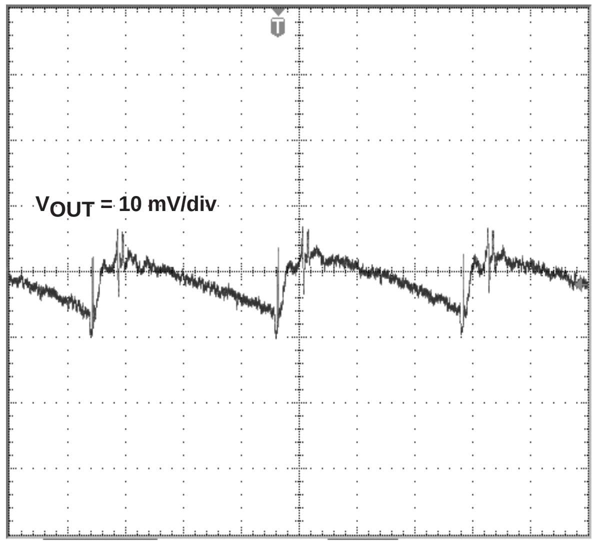


Figure 4

6.3 Output Ripple and Noise

Figure 5 shows typical output noise with V_{IN} = 40 V, I_{OUT} = 2 A.

OUTPUT VOLTAGE RIPPLE WITH V_{IN} = 40 V

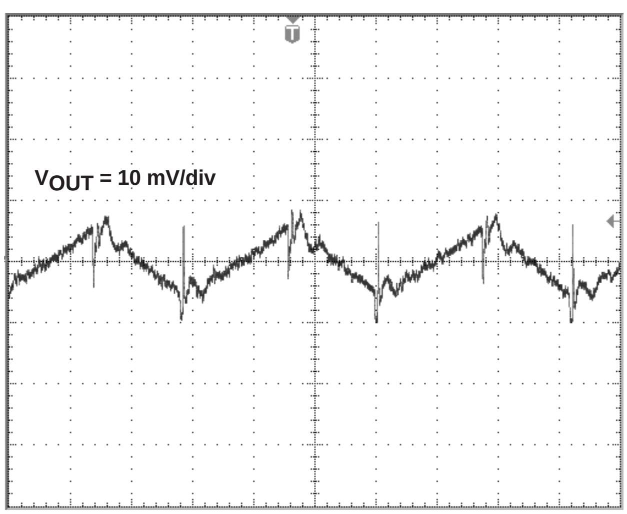


t − Time − 1.0 μs/div

Figure 5

Figure 6 shows typical output noise with V_{IN} = 10 V, I_{OUT} = 3 A.

OUTPUT VOLTAGE RIPPLE WITH V_{IN} = 10 V



t − Time − 1.0 μs/div

Figure 6

6.4 Transient Response

The transient response is shown in Figure 7 as the load is stepped from 0.5 A to 2.5 A with V_{IN} = 24 V. With the 2-A load step the output deviation is approximately 30 mV.

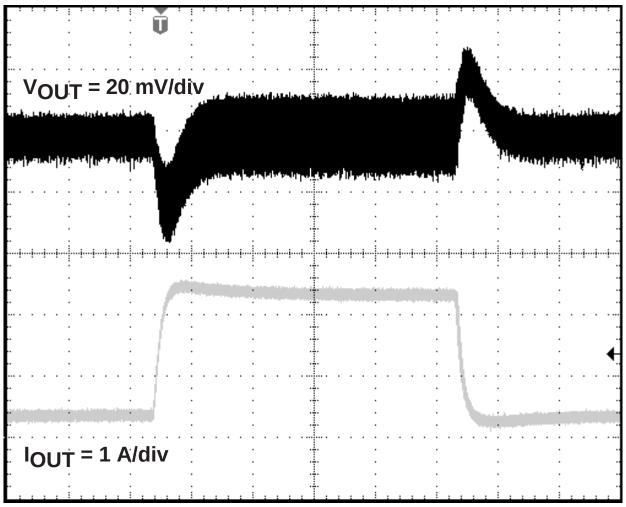


Figure 7

7 EVM Assembly Drawing and PCB Layout

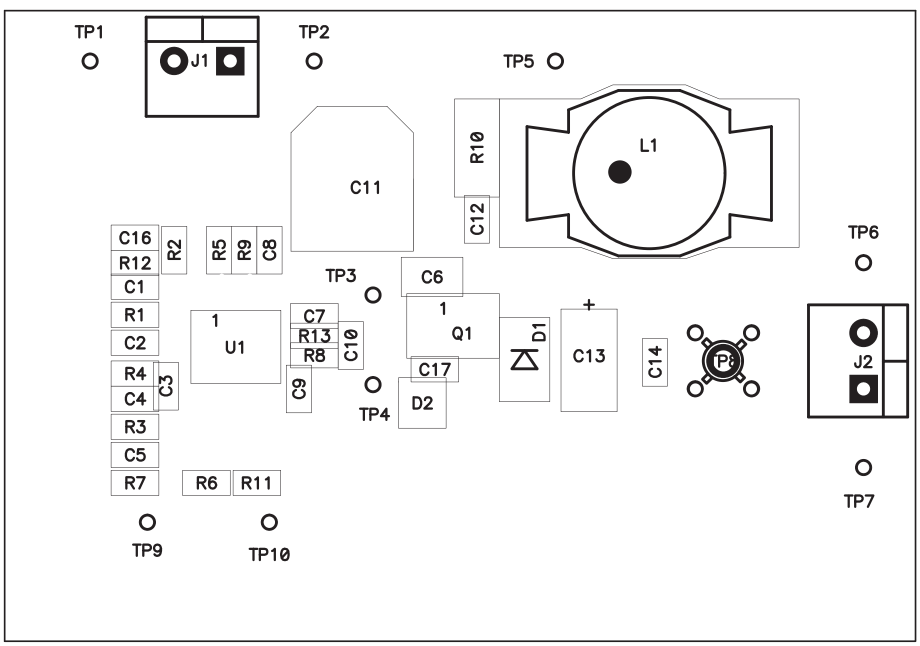


Figure 8. Top Side Component Assembly

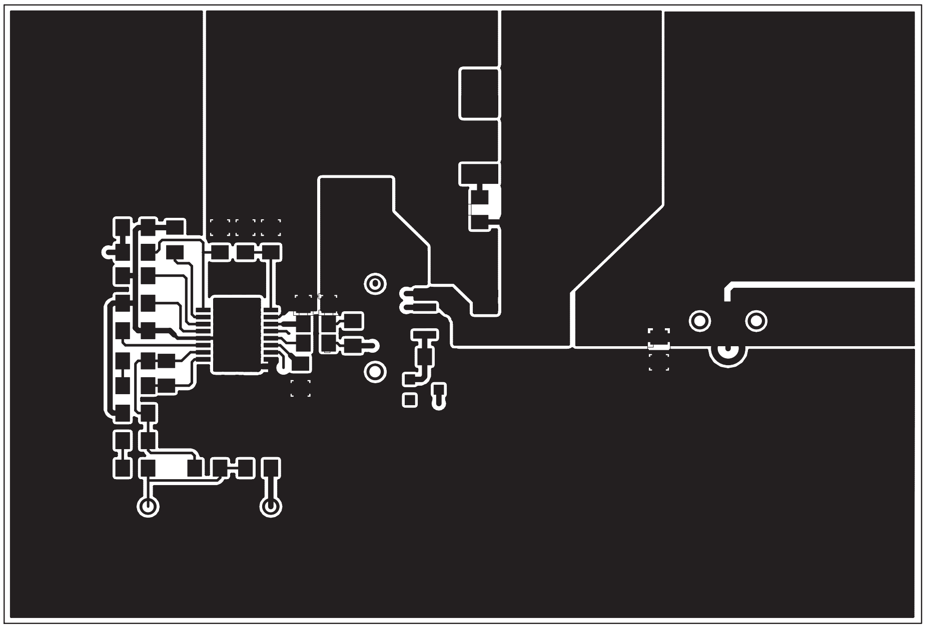


Figure 9. Top Layer Copper

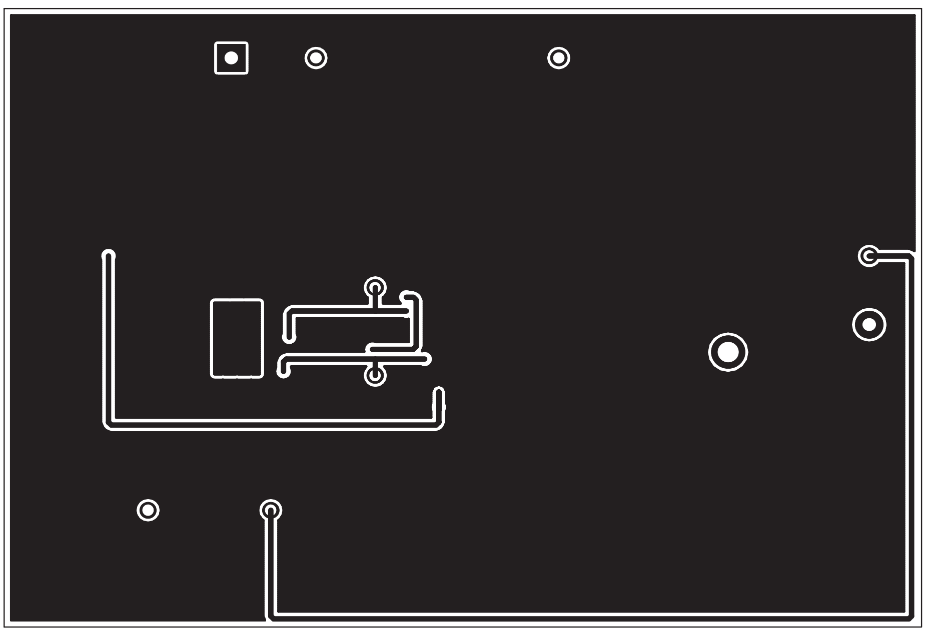


Figure 10. Bottom Layer Copper

8 List of Materials

The following table lists the TPS40055EVM−002 components corresponding to the schematic shown in Figure 1.

Table 1. TPS40055EVM−002 (HPA071) List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	MFR	PART NUMBER
C1, C7, C10	3	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%, 805	Vishay	VJ0805Y104KXXAT
C11	1	Capacitor, aluminum, 100 μF, 63 V, 20%, 0.457 x 0.406	Panasonic	EEVFK1J101P
C13	1	Capacitor, POSCAP, 330 μF, 6.3 V, 10 mΩ, 20%, 7343 (D)	Sanyo	6TPD330M
C9, C14	2	Capacitor, ceramic, 1.0 μF, 16 V, X5R, 20%, 805	TDK	C2012X5R1C105KT
C16	1	Capacitor, ceramic, 470 pF, 50 V, X5R, 20%, 805	Vishay	VJ0805Y471KXAAT
C2, C12, C17	3	Capacitor, ceramic, 2.2 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y222KXAAT
C3	1	Capacitor, ceramic, 82 pF, 50 V, NPO, 5%, 805	Panasonic	VJ0805A820KXAAT
C4	1	Capacitor, ceramic, 2.7 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y272KXAAT
C5	1	Capacitor, ceramic, 10 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y103KXAAT
C6	1	Capacitor, ceramic, 1.5 μF, 50 V, X7R, 10%, 1210	TDK	C3225X7R1H155KT
C8	1	Capacitor, ceramic, 100 pF, 50 V, X7R, 10%, 805	Vishay	VJ0805A101KXAAT
D1	1	Diode, schottky, 1 A, 60 V, SMB	IR	10BQ060
D2	1	Diode, switching, 10 mA, 85 V, 350 mW, SOT23	Vishay−Liteon	BAS16
J1, J2	2	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 x 0.35	OST	ED1609
L1	1	Inductor, SMT, 22 μH, 4.5 A, 34 mΩ, 0.87x0.59	Coiltronics	UP4B−220
Q1	1	MOSFET, dual N−channel, 60 V, 3.8 A, 55 mΩ, SO8	Siliconix	Si4946EY
R1	1	Resistor, chip, 1 kΩ, 1/10 W, 1%, 805	Std	Std
R2	1	Resistor, chip, 165 kΩ, 1/10 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 1.27 kΩ, 1/10 W, 1%, 805	Std	Std
R4	1	Resistor, chip, 30.1 kΩ, 1/10 W, 1%, 805	Std	Std
R5	1	Resistor, chip, 71.5 kΩ, 1/10 W, 1%, 805	Std	Std
R6	1	Resistor, chip, 7.87 kΩ, 1/10 W, 1%, 805	Std	Std
R7	1	Resistor, chip, 100 Ω, 1/10 W, 1%, 805	Std	Std
R8	1	Resistor, chip, 0 Ω, 1/10 W, 5%, 805	Std	Std
R9	1	Resistor, chip, 23.2 kΩ, 1/10 W, 1%, 805	Std	Std
R10	1	Resistor, chip, 4.7 Ω, 1 W, 5%, 2512	Std	Std
R11	1	Resistor, chip, 20 Ω, 1/10 W, 1%, 805	Std	Std
R12	1	Resistor, chip, 243 kΩ, 1/10 W, 1%, 805	Std	Std
R13	1	Resistor, chip, 8.2 Ω, 1/10 W, 5%, 805	Std	Std
TP1, TP7	2	Jack, test point, black	Farnell	240−333
TP2, TP3, TP4, TP5, TP6, TP9, TP10	7	Jack, test point, red	Farnell	240−345
TP8	1	Adaptor, 3.5-mm probe clip (or 131−5031−00), 0.2	Tektronix	131−4244−00
U1	1	IC, Wide Input Synchronuos Buck Controller, PWP-16	TI	TPS40055PWP
−−	1	PCB, 3.25 In x 2.25 In x .031 In	Any	HPA071

9 References

1. Data Sheet, *TPS40054/5/7 Wide-Input Synchronous Buck Controller*, (SLUS593).
2. Technical Brief, *PowerPAD™ Thermally Enhanced Package*, (SLMA002).
3. Seminar Topic, *A Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, (SLUP169).

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2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d’usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered “Radio Frequency Products” in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265