User's Guide

TPS53313 Step-Down Converter Evaluation Module User's Guide

Table of Contents

List of Figures

List of Tables

1 Introduction

The TPS53313EVM-078 evaluation module (EVM) is a step-down regulator featuring the TPS53313. The TPS53313 is a fully integrated step-down regulator employing voltage mode control.

2 Description

The TPS53313EVM-078 is designed to use a 12-V voltage rail to produce a regulated 1.2-V output with up to 6-A load current. The TPS53313EVM-078 is designed to demonstrate the TPS53313 in a typical Point-Of-Load (POL) application while providing a number of test points to evaluate the performance of the TPS53313.

2.1 Typical Applications

- POL applications for 5-V or 12-V step-down rails

2.2 Features

The TPS53313EVM-078 features include:

- Continuous 6-A output current capability
- Support all MLCC output capacitors
- Voltage mode control
- Selectable light-load operation modes (forced continuous conduction mode (FCCM) and skip mode)
- Selectable switching frequency settings (600 kHz and 1.00 MHz)
- Support synchronization to external clock
- Selectable overcurrent threshold
- Soft-stop output discharge during disable
- Overcurrent, overvoltage, undervoltage, and overtemperature protections
- Power-good indication
- Pre-bias output voltage start-up
- Convenient test points for probing critical waveforms

3 Electrical Performance Specifications

Table 3-1. TPS53313EVM-078 Electrical Performance Specifications(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristic					
Voltage range	VIN	8.0	12	14	V
Maximum input current	VIN = 12 V		0.8		A
No load input current	VIN = 12 V, IOUT = 0 A, f_{SW} = 600 kHz under skip mode		8.0		mA
Output Characteristics					
Output voltage			1.2		V
Output voltage regulation	Setpoint accuracy, (VIN = 8.0 V – 14 V, IOUT = 0 A – 6 A)	-1%		1%	
	Line regulation, (VIN = 8.0 V – 14 V, IOUT = 6 A)		0.1%		
	Load regulation, (VIN = 12 V, IOUT = 0 A – 6 A)		0.2%		
Output voltage ripple	VIN = 12 V, IOUT = 6 A		10		mV_{PP}
Output load current		0		6.0	A
Over current limit (peak)	VIN = 12 V		9		
Systems Characteristics					
Switching frequency			600/1000		kHz
Peak efficiency	VIN = 12 V, IOUT = 3.0 A, f_{SW} = 600 kHz		85.5%		
Full load efficiency	VIN = 12 V, IOUT = 6.0 A, f_{SW} = 600 kHz		82.4%		
Operating temperature			25		°C

(1) Jumpers set to default locations, See section 6 of this user's guide

4 Schematic

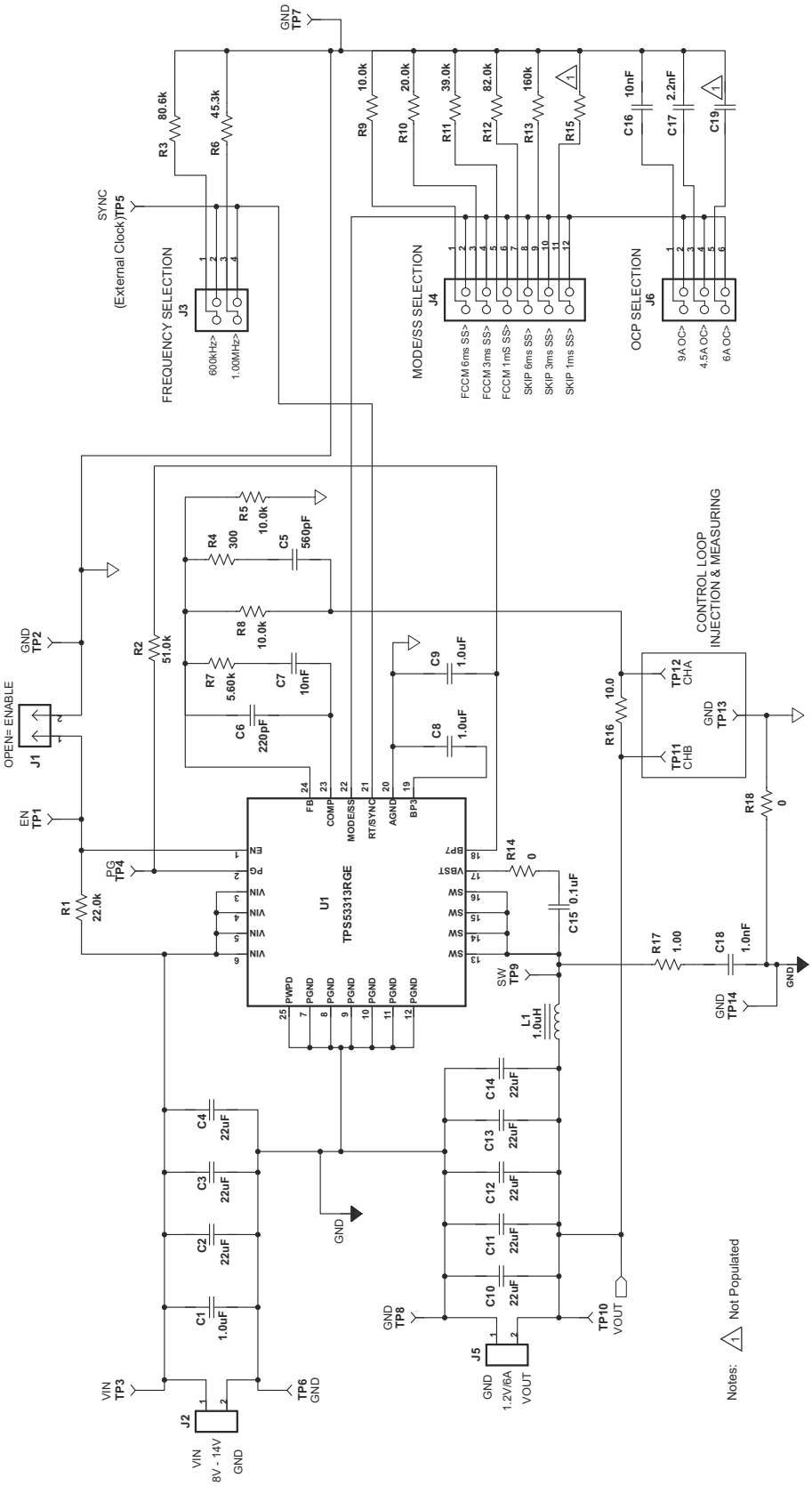

Figure 4-1. TPS53313EVM-078 Schematic

5 Test Setup

5.1 Test Equipment

Voltage Source (VIN): The input voltage source, (VIN), should be a 0-V to 15-V variable DC source capable of supplying 2 A_{DC}. Connect VIN to J2 as shown in Figure 5-2.

Multimeters:

- **V1:** VIN at TP3 (VIN) and TP6 (GND), 0-V to 15-V voltmeter
- **V2:** VOUT at TP10 (VOUT) and TP8 (GND)
- **A1:** VIN input current, 0-A_{DC} to 2-A_{DC} Ammeter

Output Load: The output load should be an electronic constant resistance mode load capable of 0 A_{DC} to 6 A_{DC} at 1.2 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, AC coupling, 1-µs/div. horizontal resolution, 20-mV/div. vertical resolution. Test points TP10 and TP8 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP10 and holding the ground barrel on TP8 as shown in Figure 5-1. Using a leaded ground connection may induce additional noise due to the large ground loop.

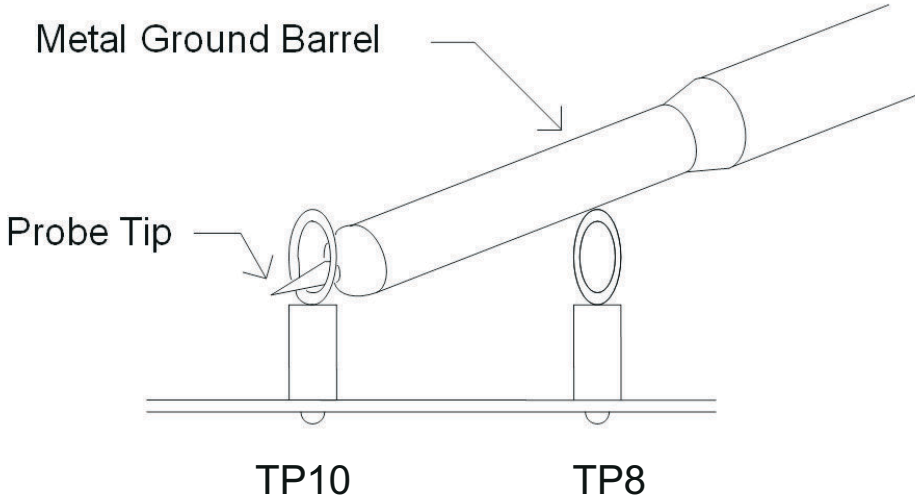

Figure 5-1. Tip and Barrel Measurement for VOUT Ripple

Fan: Some of the components in this EVM may approach temperatures of 80°C during operation. A small fan capable of 200 LFM to 400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM should not be probed while the fan is not running.

Recommended Wire Gauge:

- **VIN to J2:** The recommended wire size is 1x AWG #16 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).
- **J5 to LOAD:** The minimum recommended wire size is 1x AWG #16, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

5.2 Recommended Test Setup

Figure 5-2 is the recommended test set up to evaluate the TPS53313EVM-078. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM.

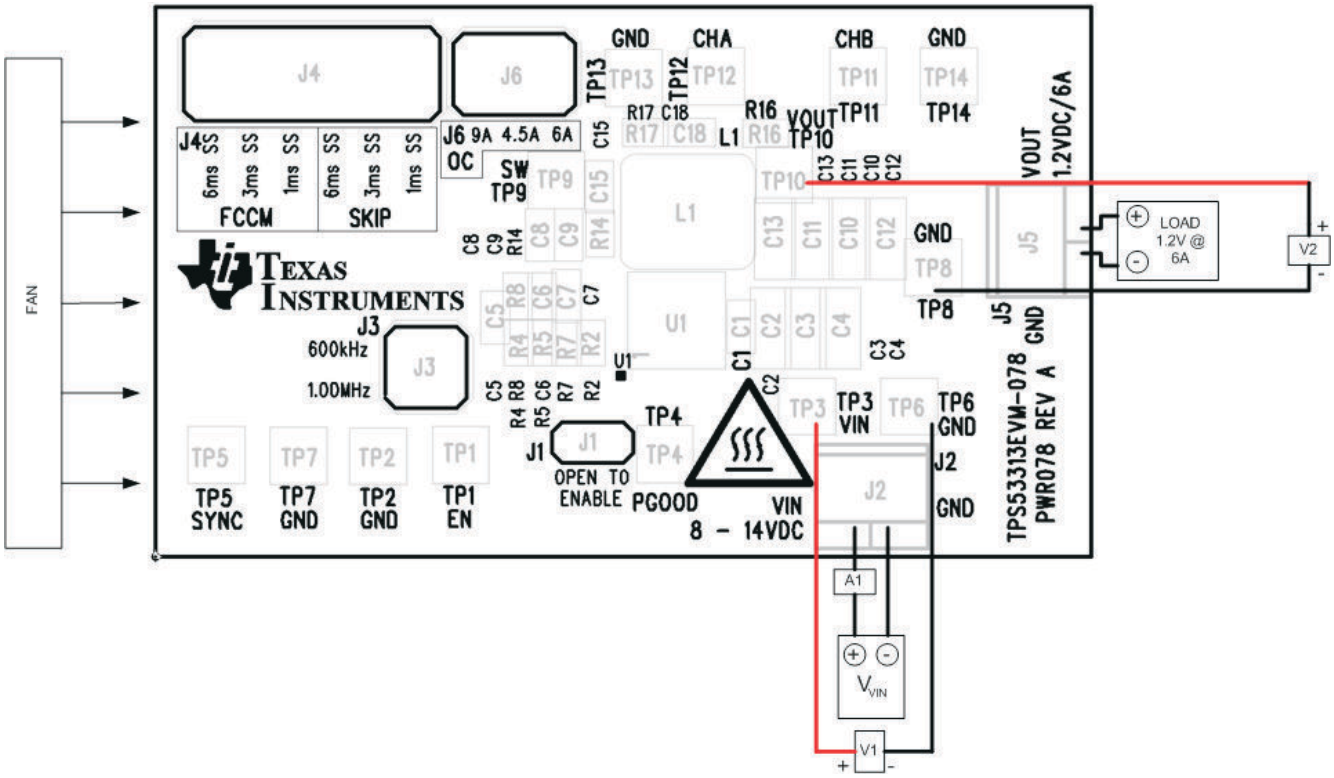

Figure 5-2. TPS53313EVM-078 Recommended Test Set Up

5.2.1 Input Connections

- Prior to connecting the DC input source (VIN), it is advisable to limit the source current from VIN to 2 A maximum. Make sure VIN is initially set to 0 V and connected to J2 as shown in Figure 5-2.
- Connect a current meter A1 between VIN and J2 to measure the input current.
- Connect a voltmeter V1 at TP3 (VIN) and TP6 (GND) to measure the input voltage.

5.2.2 Output Connections

- Connect Load to J5 and set load to constant resistance mode to sink 0 A_{DC} before VIN is applied.
- Connect a voltmeter V2 at TP10 (VOUT) and TP8 (GND) to measure the output voltage.

5.2.3 Other Connections

- Place a fan as shown in Figure 5-2 and turn on, making sure air is flowing across the EVM.

6 Configurations

All Jumper selections should be made prior to applying power to the EVM. User can configure this EVM per following configurations.

6.1 Mode and Soft-Start Time Selection

The operation mode and soft-start time can be set by J4.

6.1.1 Default Setting: Skip Mode, 6-ms SS

Table 6-1. MODE Selection

MODE RESISTANCES	OPERATION MODE	SOFT-START TIME
10.0 kΩ	FCCM	6 ms
20.0 kΩ	FCCM	3 ms
39.0 kΩ	FCCM	1 ms
82.0 kΩ	Skip	6 ms
160 kΩ	Skip	3 ms
Open	Skip	1 ms

6.2 Overcurrent Protection (OCP) Selection

The OCP threshold can be set by J6.

6.2.1 Default Setting: 9-A OCP

Table 6-2. OCP Selection

OCP SETTING CAPACITANCE	OVERCURRENT LIMIT
10 nF	9 A
2.2 nF	4.5 A
Open	6 A

6.3 Enable Selection

The converter can be enabled and disabled by J1.

6.3.1 Default Setting: Short to Disable the Converter

6.4 Switching Frequency Selection or External Clock Input for Synchronization

The switching frequency can be set by J3. If the external clock is used for synchronization, the external clock should be connected to TP5 (SYNC) and TP7 (GND).

6.4.1 Default setting: 600 kHz

Table 6-3. Switching Frequency Selection

SWITCHING FREQUENCY SETTING RESISTANCES	SWITCHING FREQUENCY
80.6 kΩ	600 kHz
45.3 kΩ	1.00 MHz

7 Test Procedure

7.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Set up EVM as described in Section 5 and Figure 5-2.
2. Ensure Load is set to constant resistance mode and to sink 0 A_{DC}.
3. Ensure all jumpers set per Section 6.
4. Increase VIN from 0 V to 12 V. Using V1 to measure VIN voltage.
5. Open jumper J1 to enable the controller.
6. Use V2 to measure VOUT voltage, A1 to measure VIN current.
7. Vary load from 0 A_{DC} to 6 A_{DC}, VOUT should remain in load regulation.
8. Vary VIN from 8.0 V to 14 V, VOUT should remain in line regulation.
9. Short jumper J1 to disable the controller.
10. Decrease load to 0 A.
11. Decrease VIN to 0 V.

7.2 Control Loop Gain and Phase Measurement Procedure

TPS53313EVM-078 contains a 10-Ω series resistor in the feedback loop for loop response analysis.

1. Set up EVM as described in Section 5 and Figure 5-2.
2. Connect isolation transformer to test points marked TP12 and TP11.
3. Connect input signal amplitude measurement probe (channel A) to TP12. Connect output signal amplitude measurement probe (channel B) to TP11.
4. Connect ground lead of channel A and channel B to TP13.
5. Inject around 10-mV or less signal through the isolation transformer.
6. Sweep the frequency from 500 Hz to 500 kHz with 10-Hz or lower post filter. The control loop gain and phase margin can be measured.
7. Disconnect isolation transformer from bode plot test points before making other measurements (Signal injection into feedback may interfere with accuracy of other measurements).

7.3 List of Test Points

Table 7-1. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	EN	Enable pin
TP2	GND	GND
TP3	VIN	Input voltage
TP4	PG	Power good output
TP5	SYNC	Input of external clock for synchronization
TP6	GND	GND
TP7	GND	GND
TP8	GND	GND
TP9	SW	Switching node
TP10	VOUT	Output voltage
TP11	CHB	Input B for loop injection
TP12	CHA	Input A for loop injection
TP13	GND	GND
TP14	GND	GND

7.4 Equipment Shutdown

1. Shut down VIN
2. Shut down Load
3. Shut down FAN

8 Performance Data and Typical Characteristic Curves

Figure 8-1 through Figure 8-17 present typical performance curves for TPS53313EVM-078.

8.1 Efficiency

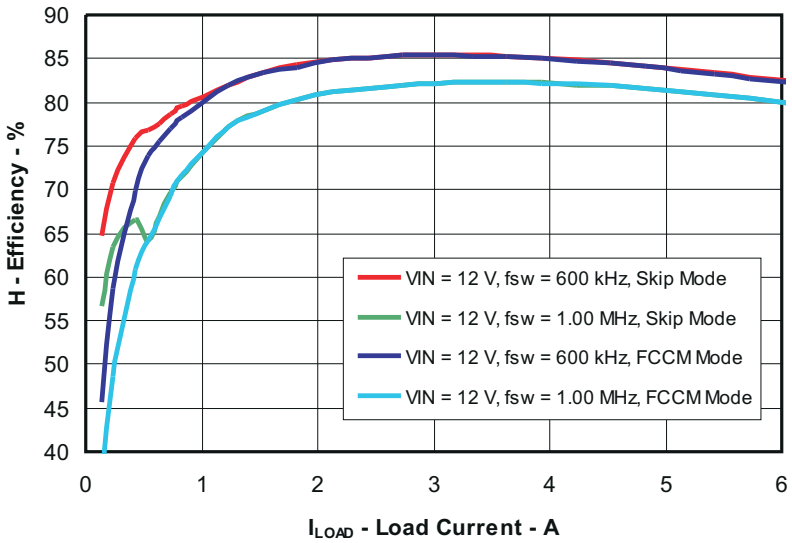

Figure 8-1. Efficiency

8.2 Load Regulation

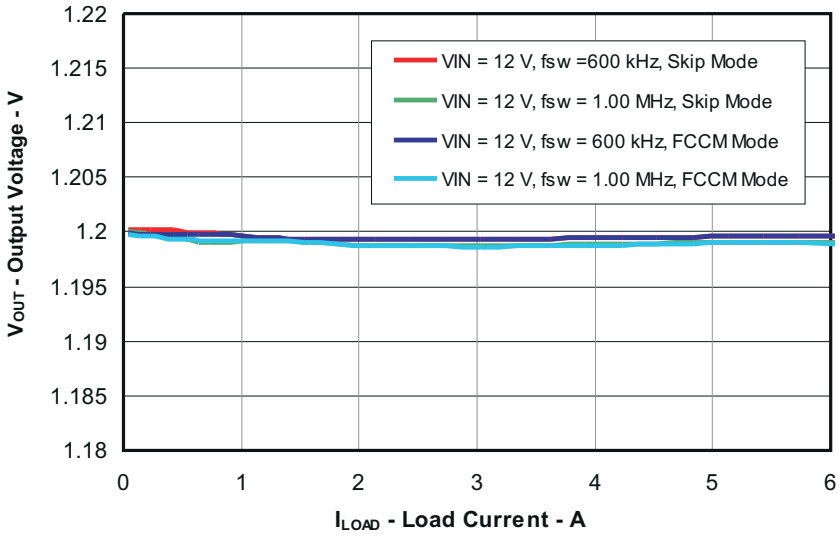

Figure 8-2. Load Regulation

8.3 Line Regulation

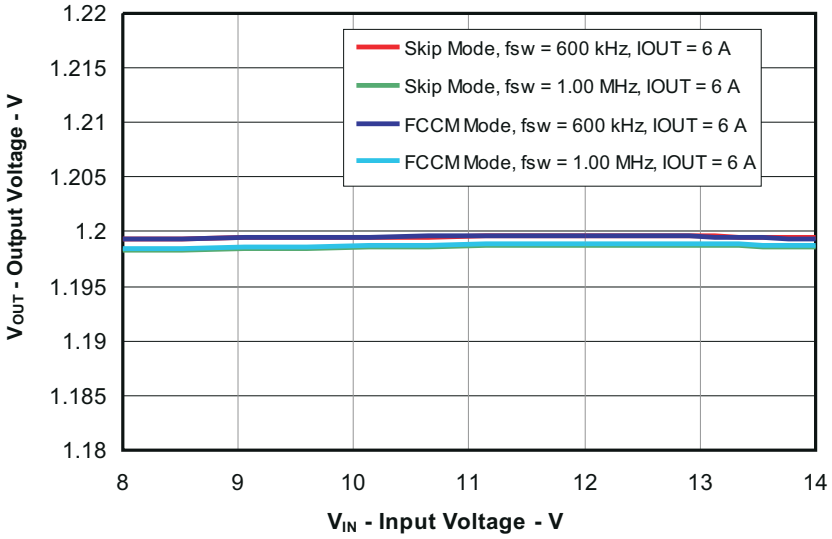

Figure 8-3. Line Regulation

8.4 Output Transient

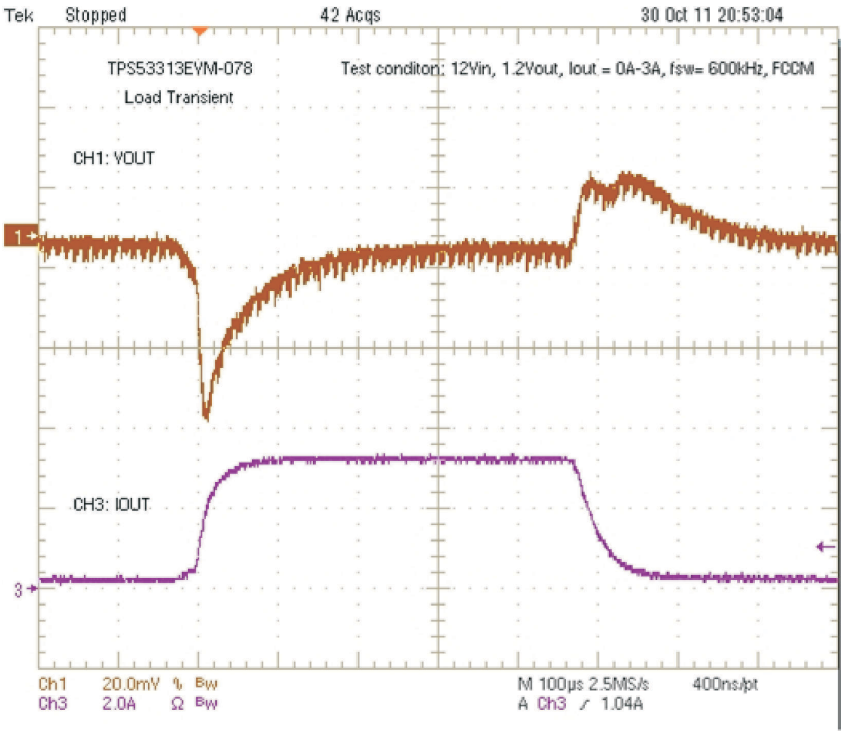

Figure 8-4. Output Load 0-A to 3-A Transient Under FCCM Mode (12-V VIN, 1.2-V VOUT, f_{SW} = 600 kHz)

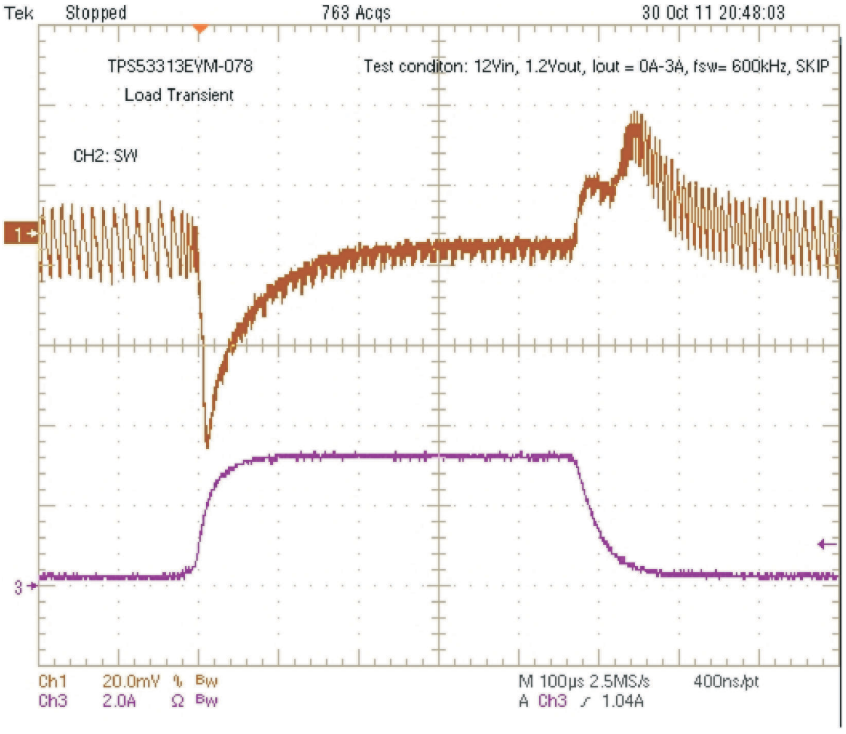

Figure 8-5. Output Load 0-A to 3-A Transient Under Skip Mode (12-V VIN, 1.2-V VOUT, f_{SW} = 600 kHz)

8.5 Output Ripple

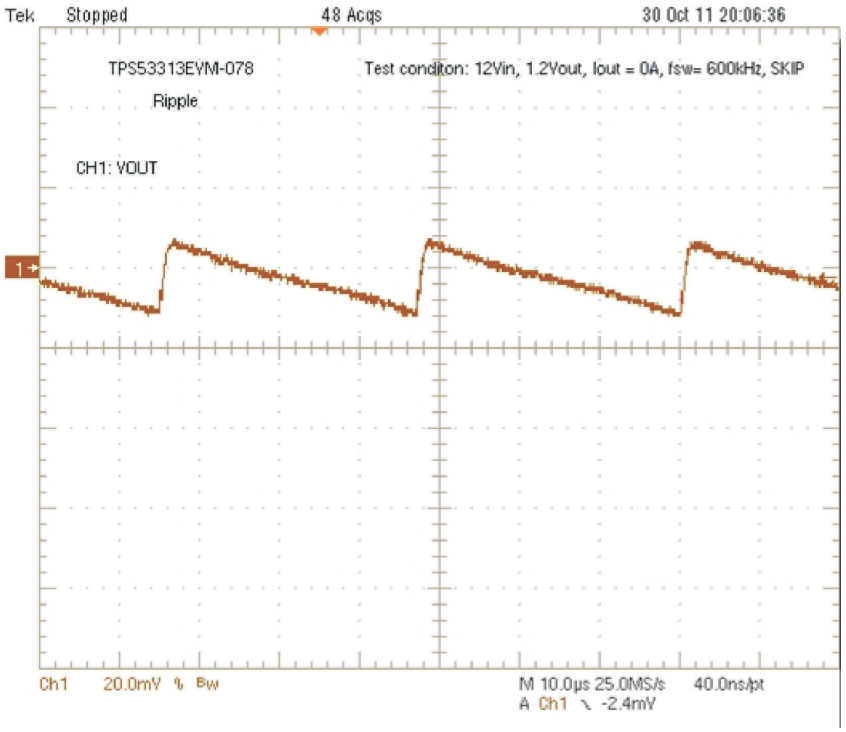

Figure 8-6. Output Ripple at No Load (12-V VIN, 1.2-V VOUT, 0-A, Skip Mode, f_{SW} = 600 kHz)

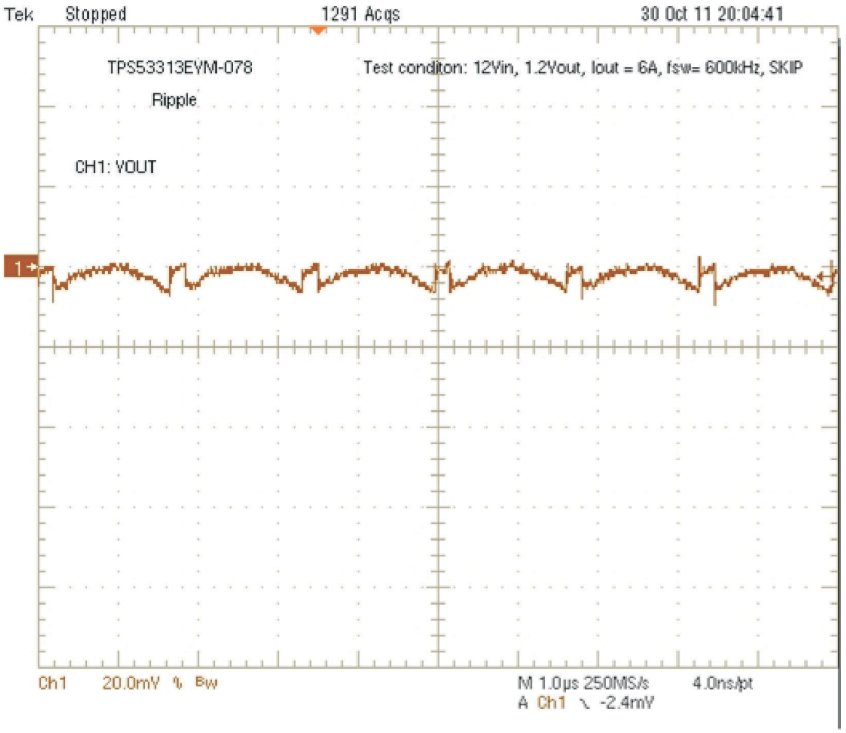

Figure 8-7. Output Ripple at Full Load (12-V VIN, 1.2-V VOUT, 6-A, Skip Mode, f_{SW} = 600 kHz)

8.6 Switching Node

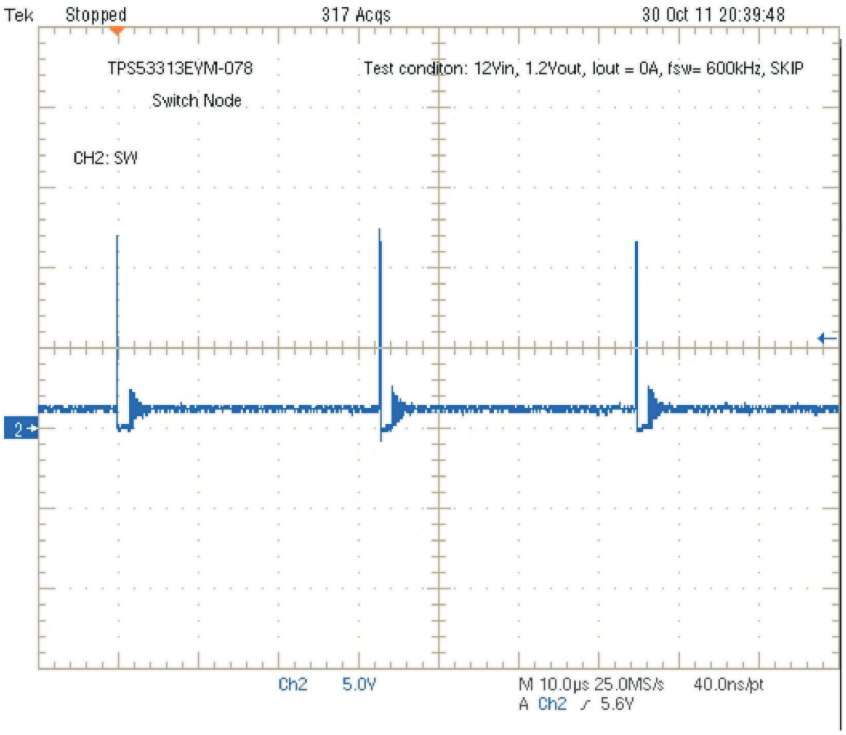

Figure 8-8. Switching Node at No Load (12-V VIN, 1.0-V VOUT, 0-A, Skip Mode, f_{SW} = 600 kHz)

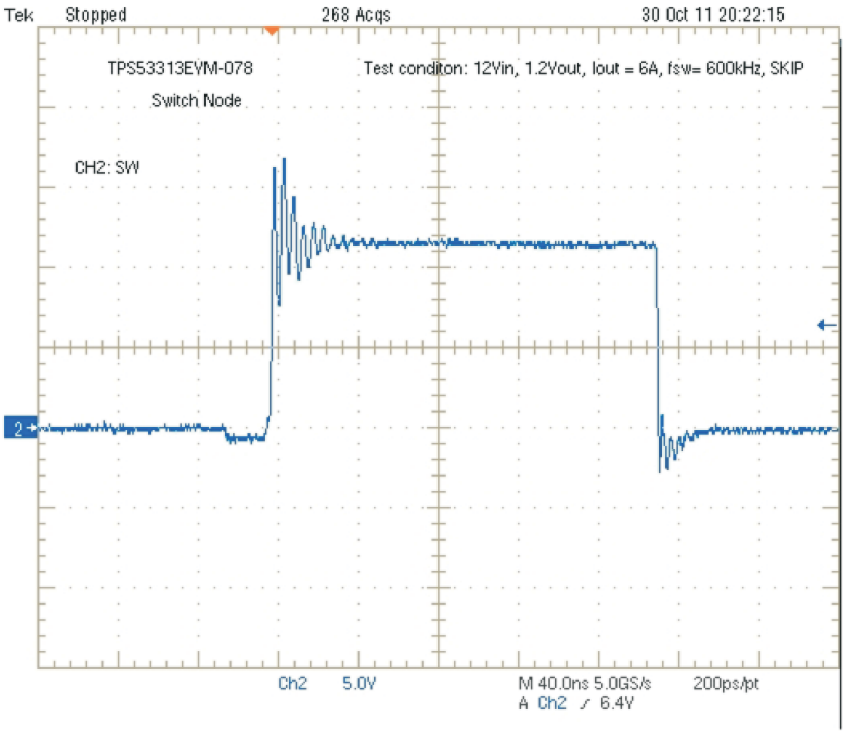

Figure 8-9. Switching Node at Full Load (12-V VIN, 1.2-V VOUT, 6-A, Skip Mode, f_{SW} = 600 kHz)

8.7 Start Up

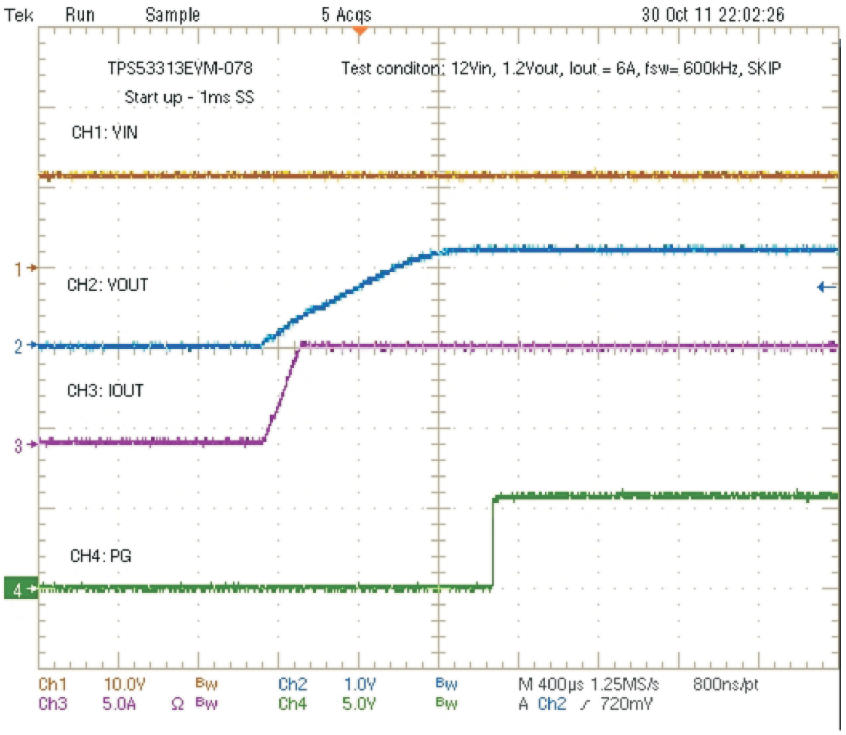

Figure 8-10. Start-Up Waveform (12-V VIN, 1.2-V VOUT, 6-A IOUT, 1-ms SS)

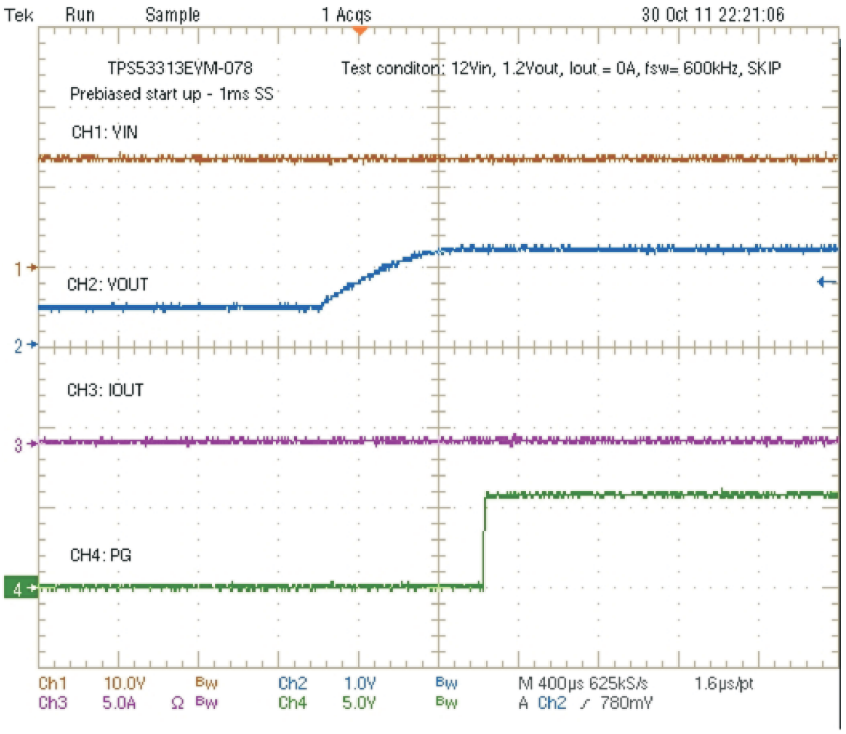

Figure 8-11. Pre-bias Start-Up Waveform (12-V VIN, 1.2-V VOUT, 0-A IOUT, 1-ms SS)

8.8 Shut Down

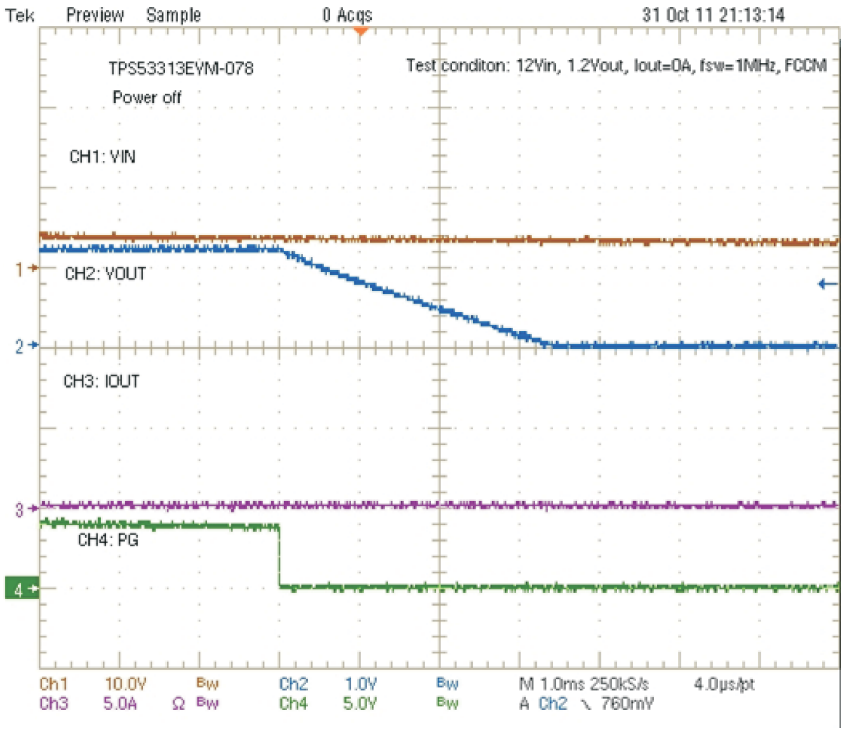

Figure 8-12. Shut-Down Waveform (12-V VIN, 1.2-V VOUT, 0-A IOUT)

8.9 Over-Current Protection

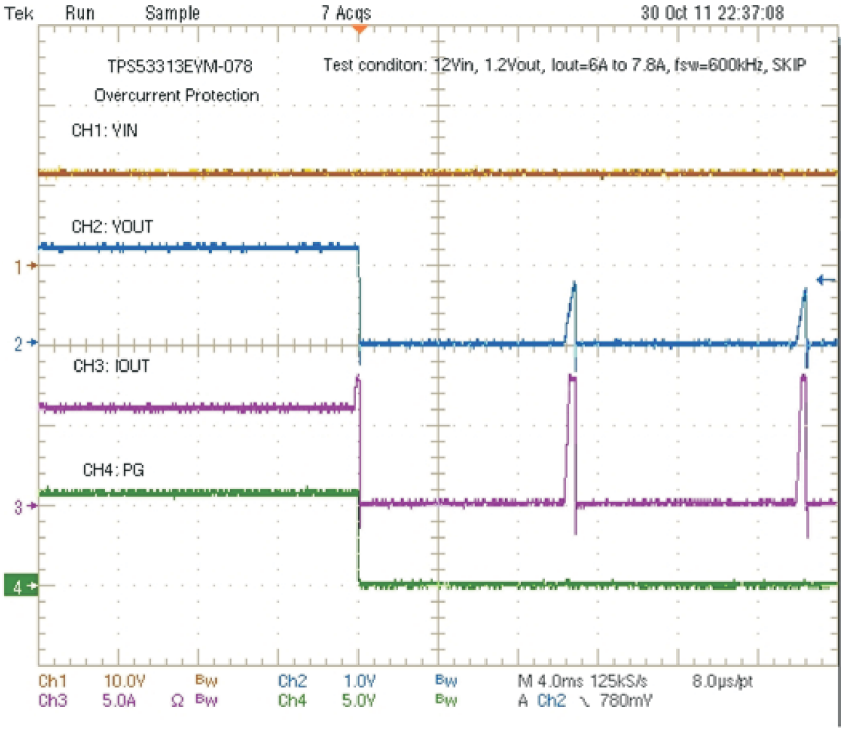

Figure 8-13. Over-Current Protection Waveform (12-V VIN, 1.2-V VOUT, IOUT increases from 6 A to 7.8 A)

8.10 Synchronization

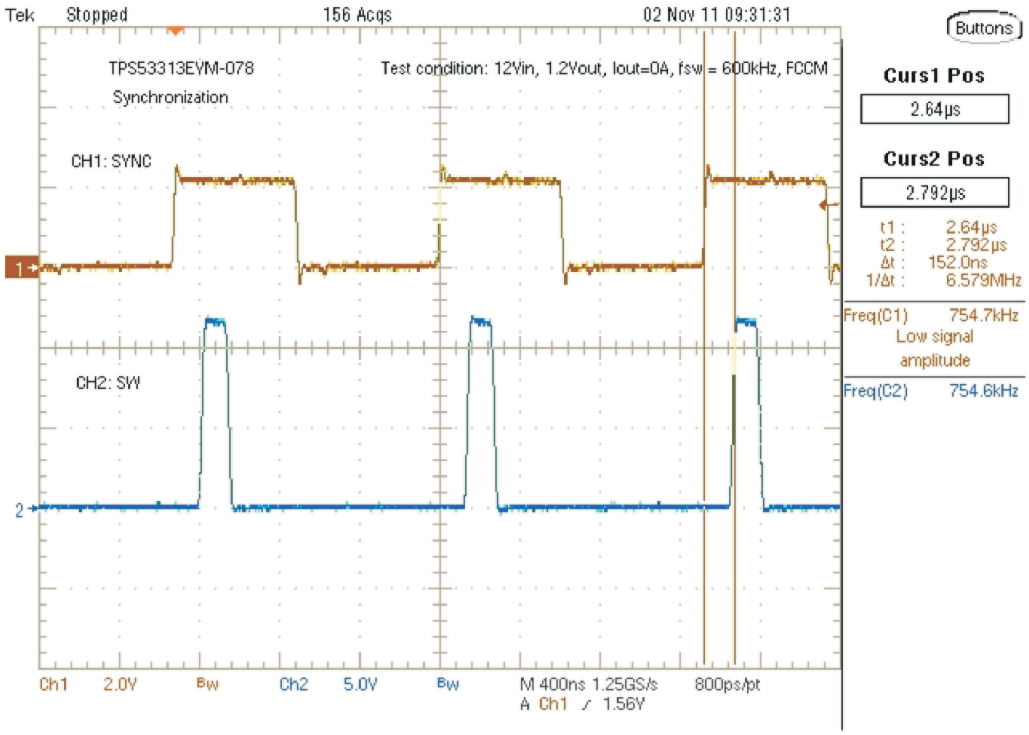

Figure 8-14. Synchronization Waveform (12-V VIN, 1.2-V VOUT, 0-A IOUT, free-running frequency = 600 kHz, SYNC frequency = 750 kHz)

8.11 Bode Plot

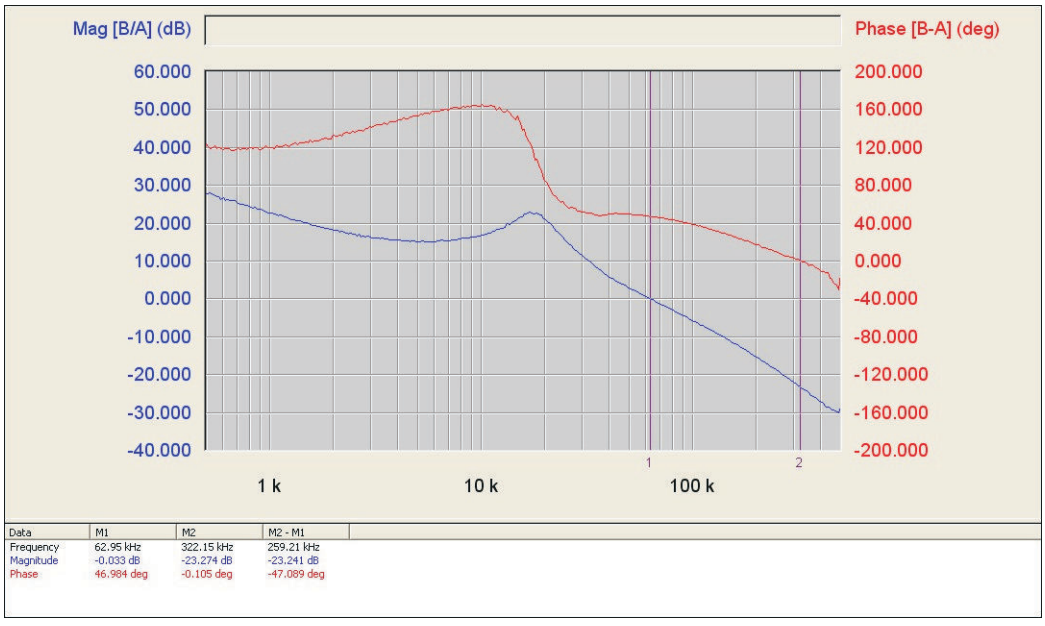

Figure 8-15. Loop Gain (12-V VIN, 1.2-V VOUT, 6-A IOUT, Skip Mode, f_{SW} = 600 kHz)

8.12 Thermal Image

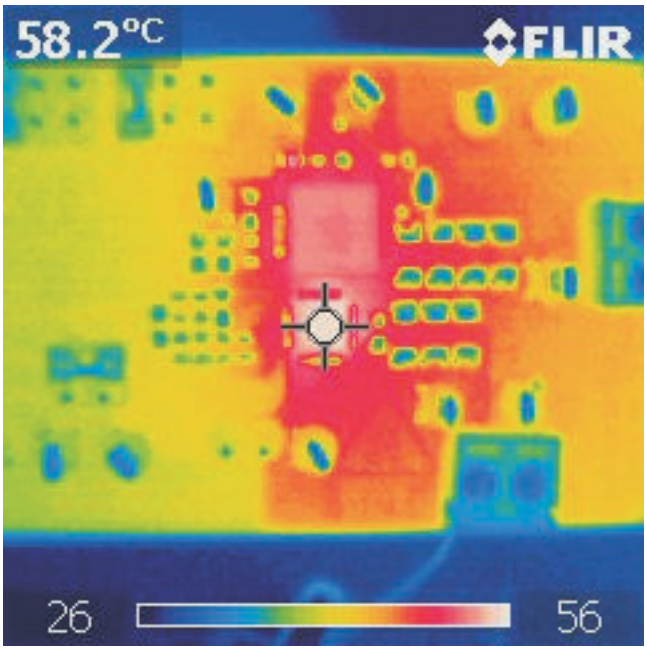

Figure 8-16. Thermal Image (12-V VIN, 1.2-V VOUT, 6-A IOUT, FCCM Mode, f_{SW} = 600 kHz)

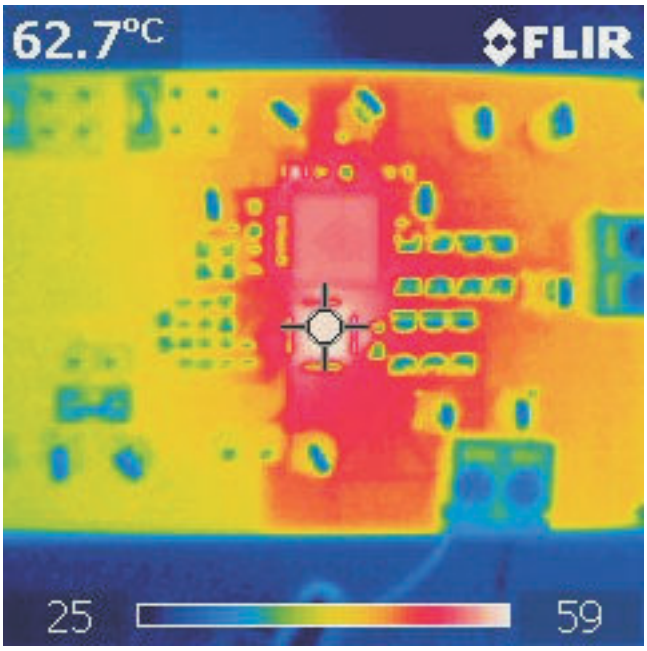

Figure 8-17. Thermal Image (12-V VIN, 1.2-V VOUT, 6-A IOUT, FCCM Mode, f_{SW} = 1.00 MHz)

9 EVM Assembly Drawing and PCB Layout

The following figures (Figure 9-1 through Figure 9-6) show the design of the TPS53313EVM-078 printed circuit board. The EVM has been designed using 4 Layers, 2-oz copper circuit board.

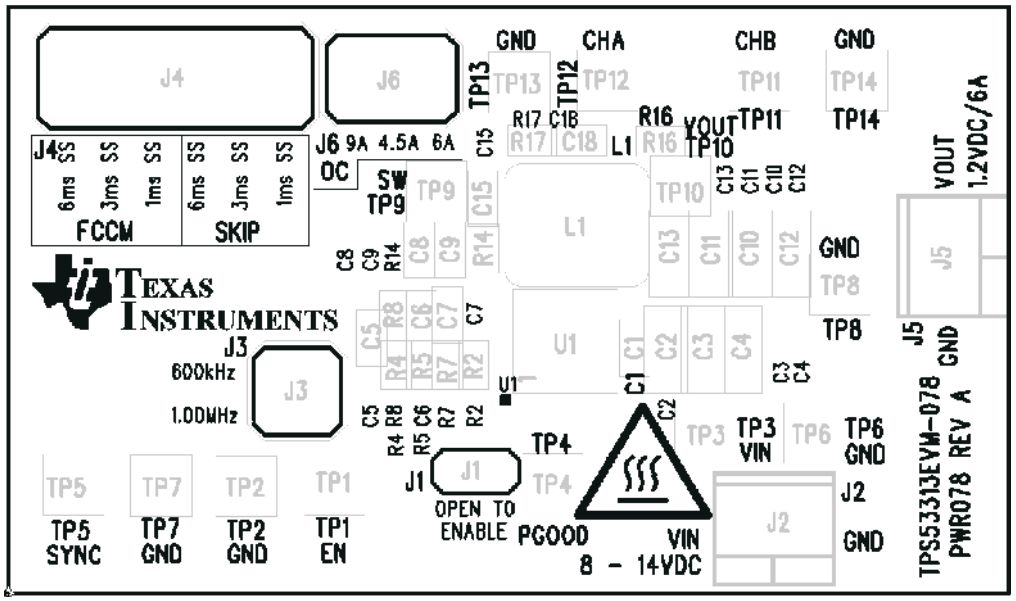

Figure 9-1. TPS53313EVM-078 Top Layer Assembly Drawing (top view)

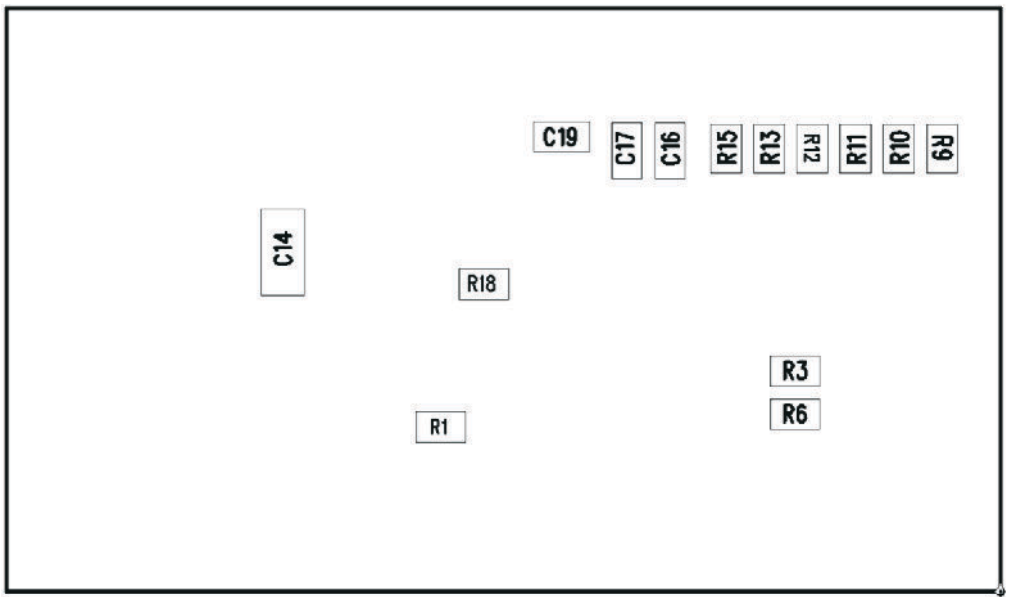

Figure 9-2. TPS53313EVM-078 Bottom Assembly Drawing (bottom view)

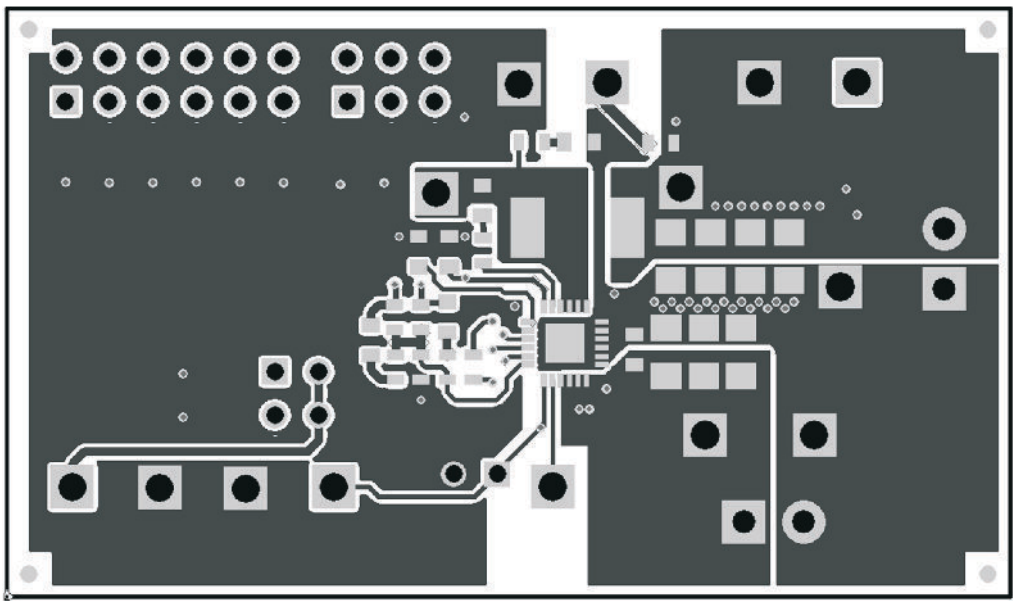

Figure 9-3. TPS53313EVM-078 Top Copper (top view)

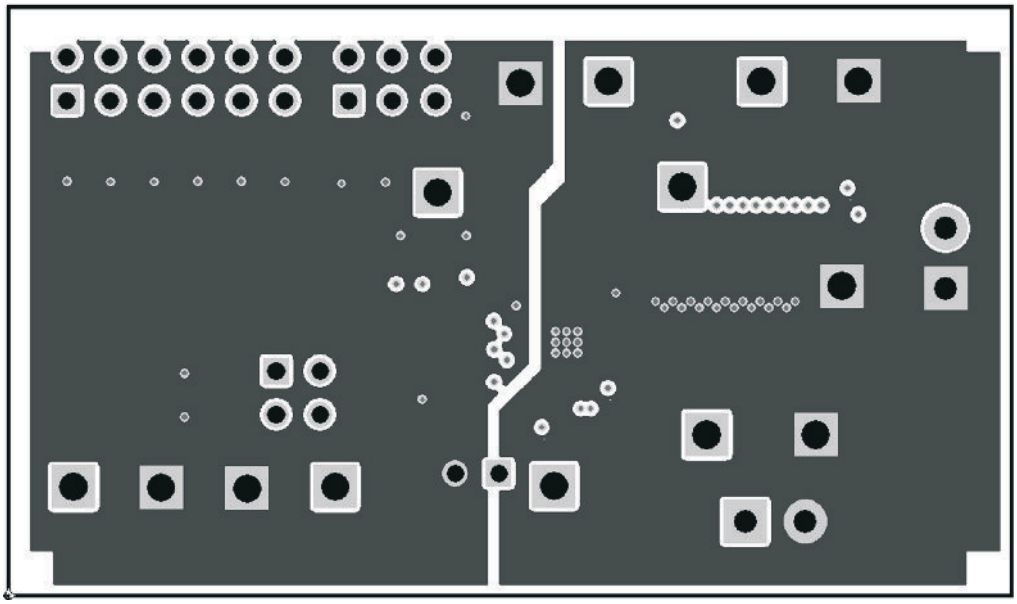

Figure 9-4. TPS53313EVM-078 Layer 2 (top view)

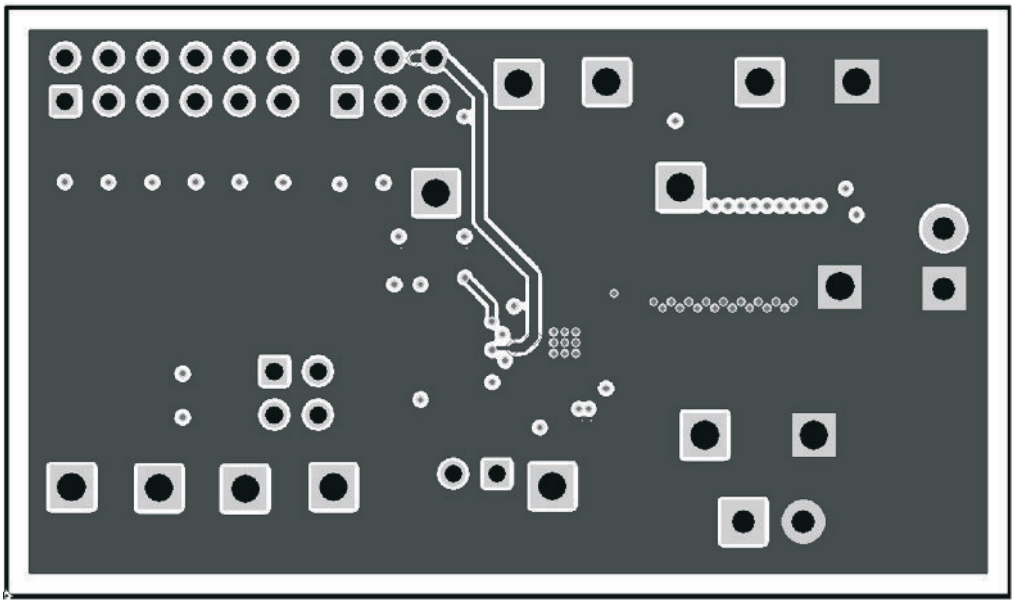

Figure 9-5. TPS53313EVM-078 Layer 3 (top view)

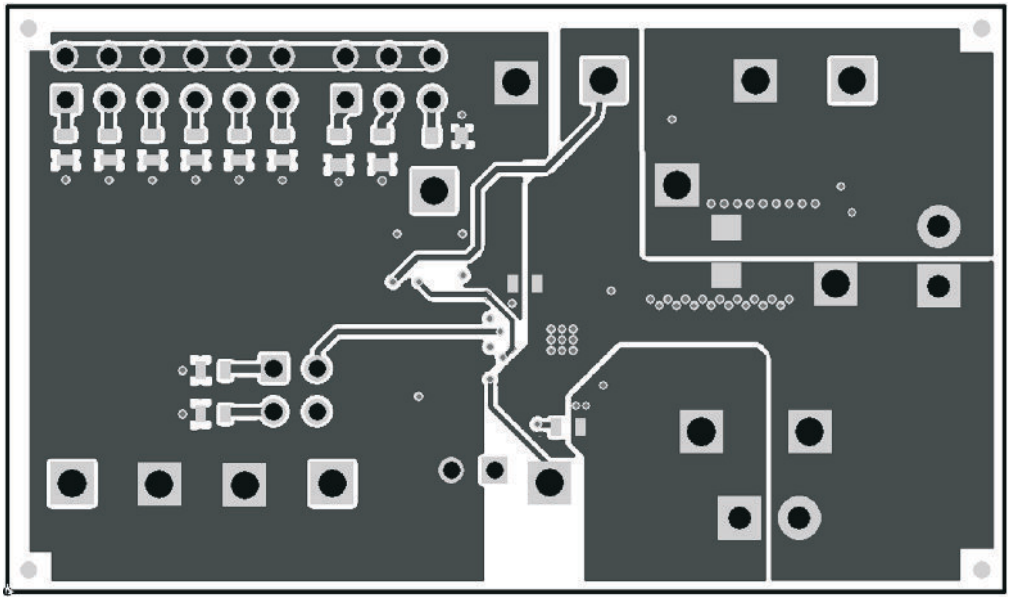

Figure 9-6. TPS53313EVM-078 Bottom Layer (top view)

10 List of Materials

The EVM components list according to the schematic shown in Figure 4-1

Table 10-1. TPS53313EVM-078 List of Materials

QTY	REF DES	DESCRIPTION	PART NUMBER	MFR
3	C1, C8, C9	Capacitor, ceramic, 16 V, X7R, 10%, 1.0 µF, 0603	Std	Std
8	C2, C3, C4, C10, C11, C12, C13, C14	Capacitor, ceramic, 25 V, X5R, 10%, 22 µF, 1206	Std	Std
1	C5	Capacitor, ceramic, 16 V, X7R, 10%, 560 pF, 0603	Std	Std
1	C6	Capacitor, ceramic, 16 V, X7R, 10%, 220 pF, 0603	Std	Std
2	C7, C16	Capacitor, ceramic, 16 V, X7R, 10%, 10 nF, 0603	Std	Std
1	C15	Capacitor, ceramic, 50 V, X7R, 10%, 0.1 µF, 0603	Std	Std
1	C17	Capacitor, ceramic, 16 V, X7R, 10%, 2.2 nF, 0603	Std	Std
1	C18	Capacitor, ceramic, low inductance, 50 V, X7R, 10%, 1.0 nF, 0603	Std	Std
0	C19	Capacitor, ceramic, 16 V, X7R, 10%, 0603	Std	Std
1	J1	Header, male 2 pin, 100-mil spacing, 0.100 inch x 2 inch	PEC02SAAN	Sullins
2	J2, J5	Terminal block, 2-pin, 6-A, 3.5mm, 0.27 inch x 0.25 inch	ED555/2DS	OST
1	J3	Header, 2 x 2 pin, 100-mil spacing, 0.20 inch x 0.20 inch	PEC02DAAN	Sullins
1	J4	Header, male 2 x 6 pin, 100-mil spacing, 0.100 inch x 2 inch x 6 inch	PEC06DAAN	Sullins
1	J6	Header, male 2 x 3 pin, 100-mil spacing, 0.20 inch x 0.30 inch	PEC03DAAN	Sullins
1	L1	Inductor, 1.0 µH, 5.6 mΩ, ±20%, 6.6 mm x 7 mm	PCMC065T-1R0MN	Cyntec Co.
1	R1	Resistor, chip, 1/16 W, 1%, 22.0 kΩ, 0603	Std	Std
1	R2	Resistor, chip, 1/16 W, 1%, 51.0 kΩ, 0603	Std	Std
1	R3	Resistor, chip, 1/16 W, 1%, 80.6 kΩ, 0603	Std	Std
1	R4	Resistor, chip, 1/16 W, 1%, 300 Ω, 0603	Std	Std
3	R5, R8, R9	Resistor, chip, 1/16 W, 1%, 10.0 kΩ, 0603	Std	Std
1	R6	Resistor, chip, 1/16 W, 1%, 45.3 kΩ, 0603	Std	Std
1	R7	Resistor, chip, 1/16 W, 1%, 5.60 kΩ, 0603	Std	Std
1	R10	Resistor, chip, 1/16 W, 1%, 20.0 kΩ, 0603	Std	Std

Table 10-1. TPS53313EVM-078 List of Materials (continued)

QTY	REF DES	DESCRIPTION	PART NUMBER	MFR
1	R11	Resistor, chip, 1/16 W, 1%, 39.0 kΩ, 0603	Std	Std
1	R12	Resistor, chip, 1/16 W, 1%, 82.0 kΩ, 0603	Std	Std
1	R13	Resistor, chip, 1/16 W, 1%, 160 kΩ, 0603	Std	Std
2	R14, R18	Resistor, chip, 1/16 W, 1%, 0 Ω, 0603	Std	Std
0	R15	Resistor, chip, 1/16 W, 1%, 0603	Std	Std
1	R16	Resistor, chip, 1/16 W, 1%, 10.0 Ω, 0603	Std	Std
1	R17	Resistor, chip, 1/8 W, 1%, 1.00 Ω, 0603	Std	Std
4	TP1, TP4, TP11, TP12	Test point, white, thru hole, 0.125 inch x 0.125 inch	5012	Keystone
6	TP2, TP6, TP7, TP8, TP13, TP14	Test point, black, thru hole, 0.125 inch x 0.125 inch	5011	Keystone
4	TP3, TP5, TP9, TP10	Test point, red, thru hole, 0.125 inch x 0.125 inch	5010	Keystone
1	U1	6A Step-down Regulator with Integrated Switcher, QFN-24	TPS53313RGE	TI
4	--	Shunt, 100 mil, black, 0.100 inch	929950-00	3M
1	--	PCB, 2.3 inch x 1.35 inch x 0.062 inch	PWR078	Any

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2011) to Revision A (December 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 3
- Updated the user's guide title..... 3

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Last updated 10/2025