User's Guide

TAS5822M Process Flows

Abstract

The TAS522M device has a powerful µCDSP audio processing core, which supports one process flow for each speaker configuration. This user's guide explains the details of the process flows.

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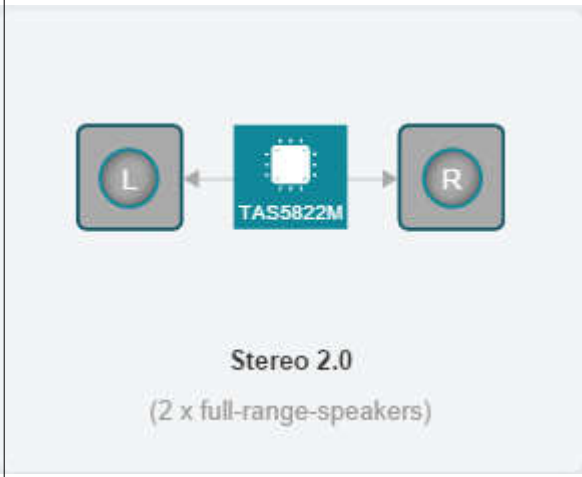
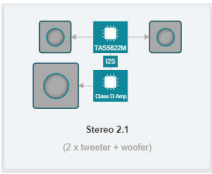
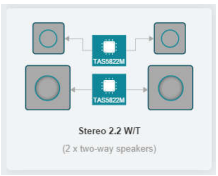
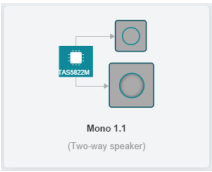
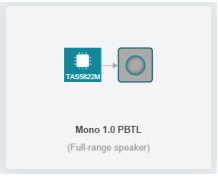
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1 General Overview

1.1 Supported Use Cases

The TAS5822 process flows have been generated based upon several popular configurations, primarily around the number and type of amplified outputs. Table 1-1 shows the use cases supported by available process flows and PPC3 GUI.

Table 1-1. Supported Use Cases

Mode	Also Known As	Amplifier Output Configuration	Symbol in PPC3 GUI
Stereo	2.0	One device drives two full-range speakers in stereo.	
Stereo	2.1	One device drives two tweeters in stereo. An I2S signal is provided to drive a woofer using another digital-in no-processing amplifier (for example, TAS5720 or TAS5760).	
Stereo	2.2	Two devices drive 2 two-way speakers in stereo. One device drives two tweeters and one device drives two woofers.	
Mono	1.1	Two input channels are mixed into one. One device drivers a tweeter on one channel and a woofer on the other.	
Mono	1.0	Two input channels are mixed into one. One device drivers a single full-range speaker on once channel.	

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2 Process Flows

2.1 Overview

Table 2-1 shows the processing features of each process flow available in the current PPC3 GUI.

Table 2-1. Processing Features Comparison Table

Feature	Process Flow 1 (2-Band DRC, 96kHz, 2.0)	Process Flow 2 (2-Band DRC, 48kHz, 1.1)	Process Flow 3 (2-Band DRC, 48kHz, 2.1)	Process Flow 4 (2-Band DRC, 96kHz, 2.2)	Process Flow 5 (2-Band DRC, 96kHz, 1.0)
Speaker Configuration	Stereo 2.0	Mono 1.1	Stereo 2.1	Stereo 2.2	Mono 1.0
Maximum Internal Sample Rate	96kHz	48kHz	48kHz	96kHz	96kHz
SRC and Automatic Detect	✓	✓	✓	✓	✓
Supported Input Sample Rates (32k, 44.1k, 48k, 88.2k and 96k)	✓	88.2k and 96k are not supported	88.2k and 96k are not supported	✓	✓
Biquads (BQs) for EQ Filtering (Individual Left and Right)	14	14	14	14	14
Input Mixer	✓	✓	✓	✓	✓
Click and Pop Free Volume	✓	✓	✓	✓	✓
DRC	2-Band 4^{th} Order Crossover	2-Band 4^{th} Order Crossover	2-Band 4^{th} Order Crossover	2-Band 4^{th} Order Crossover	2-Band 4^{th} Order Crossover
Automatic Gain Limiter	✓	✓	✓	✓	✓
Output Clipper	✓	✓	✓	✓	✓
Hybrid PWM Mode	✓	✓	✓	✓	✓

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2.2 Process Flow 1

The PPC3 tuning and audio processing window varies based on the speaker configuration. If a woofer + tweeter configuration is used, then the configuration follows the process flow outlined in Figure 2-1. All other process flows (stereo 2.0, stereo 2.2, and mono 1.0), follow that of Figure 2-2. These diagrams depict the flow of the signal path, with the blocks below corresponding to the functions found in the PPC3 GUI.

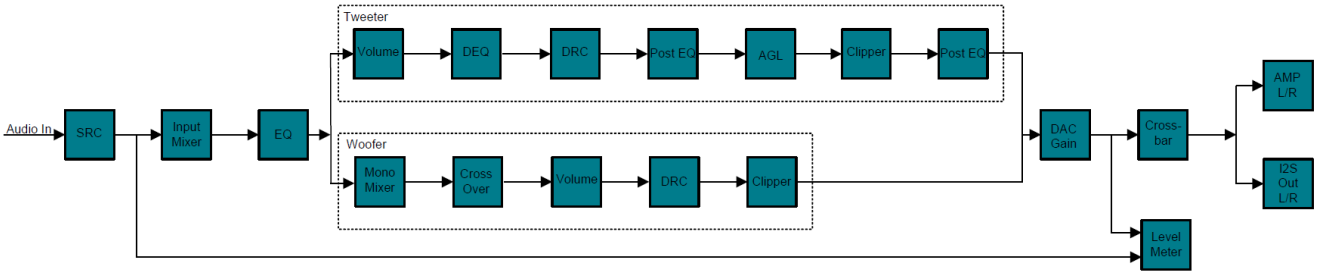


Figure 2-1. Process Flow for Mono 1.1 and Stereo 2.1 (Woofer + Tweeter)

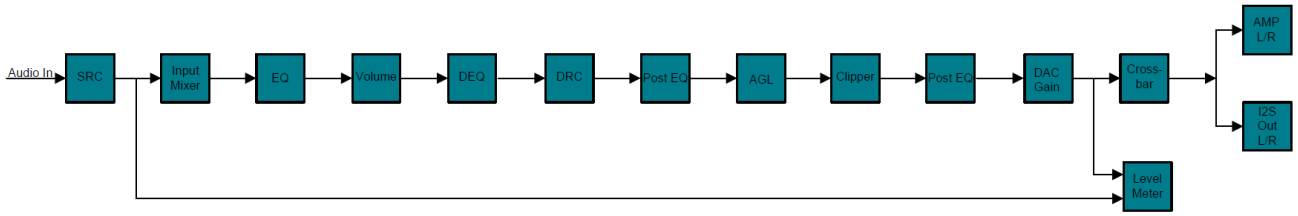


Figure 2-2. Process Flow for Stereo 2.0, Mono 1.0, and Stereo 2.2

2.2.1 SRC

The sample rate converter (SRC) supports 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz input sample rates. These input sample rates can be converted to 88.2 or 96kHz sample rate.

2.2.2 Input Mixer

The input mixer is used to mix the left and right channel input signals. Refer to Section 3.1 for more details.

2.2.3 Equalizer

The equalizer contains 14 independent filters for both left and right channels. Refer to Section 3.2 for more details.

2.2.4 Volume

This volume block is click and pop free. Refer to Section 3.3 for more details.

2.2.5 DPEQ

The dynamic parametric equalizer is used to mix the audio signals through two signal paths (low level and high level). These two paths are used with separate equalization properties. A third path monitors the incoming audio and determines the thresholds and mixing characteristics between these two paths. Thus, the mix between the two high- and low-level channels is dynamic in nature and depends on the incoming audio. Refer to Section 3.4 for more details.

2.2.6 2-Band DRC

The 2-Band DRC can be used to automatically control the audio signal amplitude or the dynamic range within specified limits. Refer to Section 3.5 for more details.

2.2.7 AGL

The AGL can also be used to automatically control the audio signal amplitude or dynamic range within specified limits. Refer to Section 3.6 for more details.

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2.2.8 Clipper

A THD boost and fine volume control can be used together for clipping. The clipper block allows the user to programmatically increase the THD by clipping at an operating point earlier than that defined by the supply rails to achieve a higher output power. Refer to Section 3.7 for more details.

2.2.9 Output Crossbar

The crossbar provides the end user with a very flexible way to control what finally appears on amplifier outputs and I2S SDOUT. Refer to Section 3.8 for more details.

2.2.10 DSP Memory Map

Refer to Section A.1 for details.

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3 Audio Processing Blocks

3.1 Input Mixer

The input mixer can be used to mix the left and right channel input signals as shown in Figure 3-1. The input mixer has four coefficients, which control the mixing and gains of the input signals.

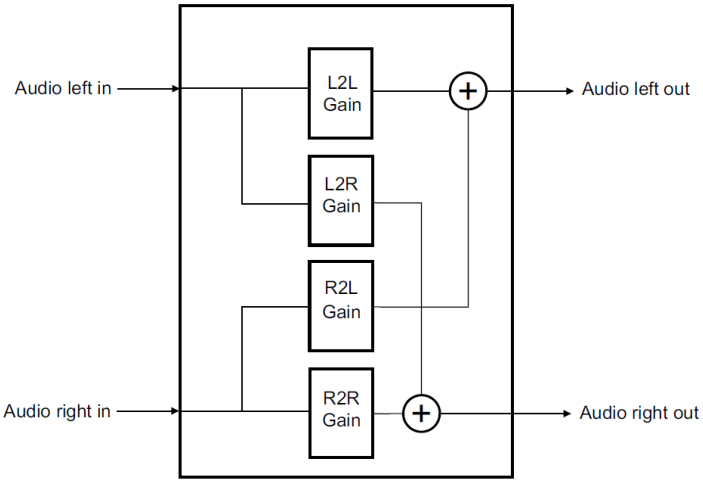


Figure 3-1. Input Mixer

The *Basic* tab (see Figure 3-2) provides the easiest way for configuration in PPC3 GUI. Switch to the *Advanced* tab (see Figure 3-3) to adjust all the four coefficients manually.

Note

The four parameters must be specified in decibels (dB).

Users can invert the result of any of the gains by selecting the + that is placed after the coefficient box in the GUI.

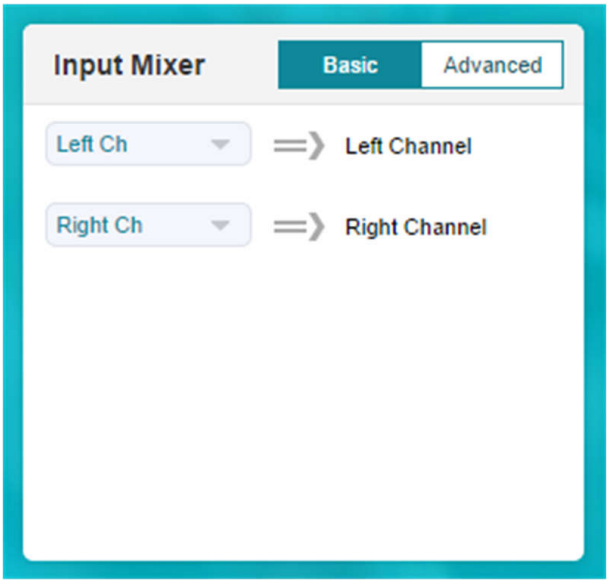


Figure 3-2. Input Mixer (Basic Tab)

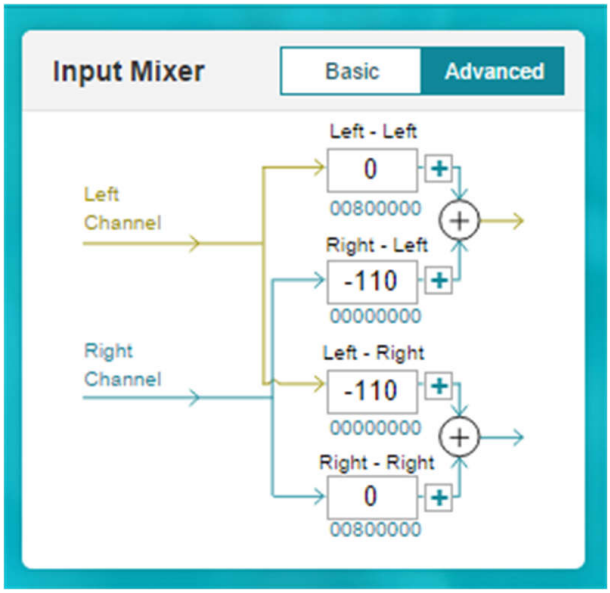


Figure 3-3. Input Mixer (Advanced Tab)

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3.2 Equalizer

The equalizers are implemented using cascaded *direct form 1* BQ structures as shown in Figure 3-4.

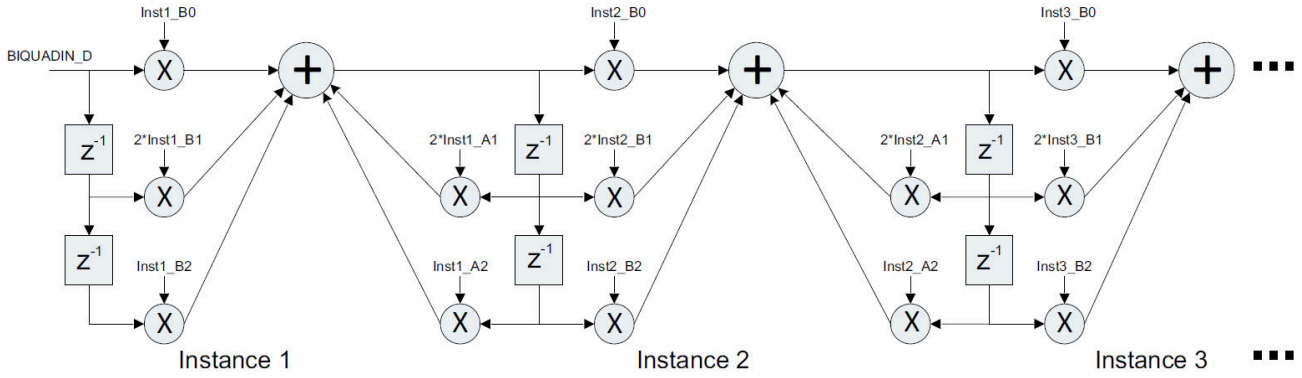


Figure 3-4. Cascaded BQ Structure

All BQ coefficients are normalized with a0 to insure that B0 is equal to 1. The structure requires five BQ coefficients as shown in Table 3-1.

Table 3-1. BQ Coefficients Normalization

BQ Coefficient	Coefficient Calculation
B0_DSP	b0 / a0
B1_DSP	b1 / (a0 × 2)
B2_DSP	b2 / a0
A1_DSP	–a1 / (a0 × 2)
A2_DSP	–a2 / a0

The *Equalizer Tuning* window shown in Figure 3-5 contains 14 independent filters for both left and right channels. The filters are designed for tuning the frequency response of the overall system. These filters are where the bulk of the frequency compensation occurs. Complex tuning shapes can be made to compensate for deficiencies in speaker response.

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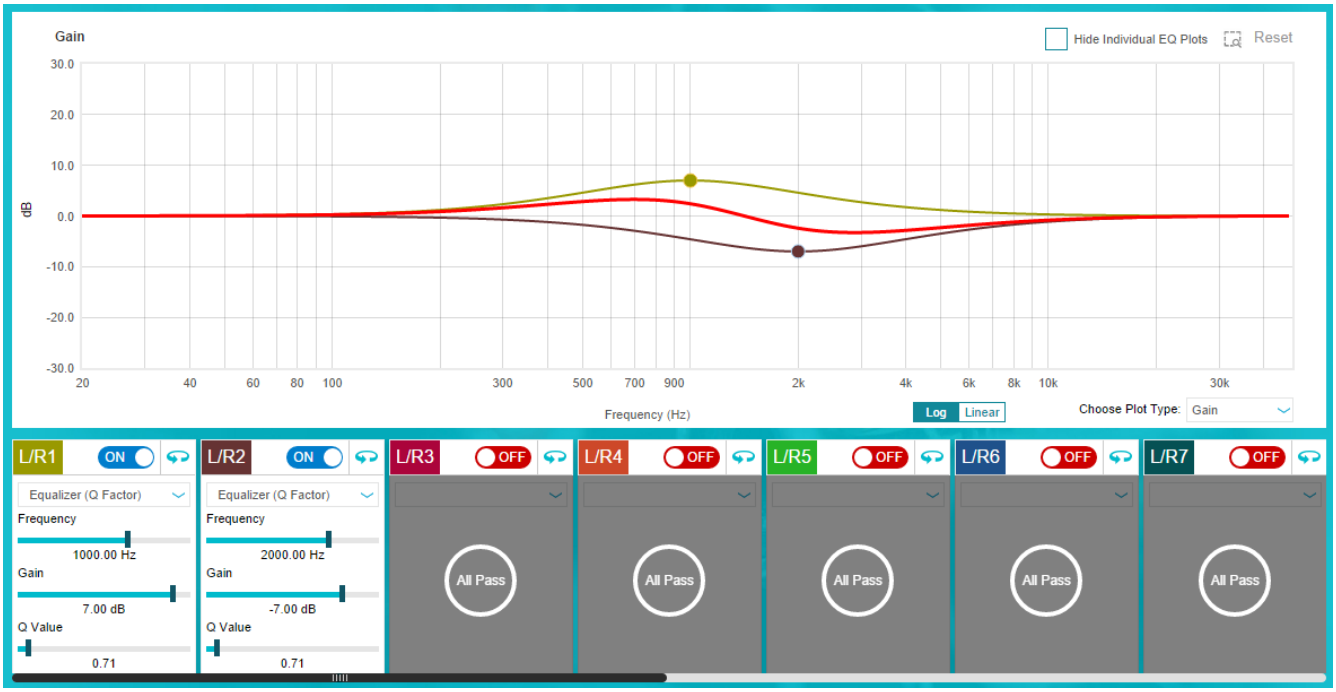


Figure 3-5. Equalizer Tuning Window

As Figure 3-5 shows, each filter has quite a few different filter types and can be turned on or off independently. All the changes to these filters are reflected in the plot above. The composite plot (red) shows the overall frequency response alteration applied to the incoming digital audio data.

The equalizers for left and right channels are ganged by default, but these equalizers can be configured independently by deselecting the *Gang* option.

3.3 Volume

Figure 3-6 shows the default volume in PPC3 GUI.

Note

The volume must be specified in decibels (dB).

An independent volume change for the left and right channel can be achieved by deselecting the *Gang* option.

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Figure 3-6. Volume

The volume block is implemented using an alpha filter structure. As Figure 3-7 shows, when a volume level change is initiated, the volume block provides a smooth transition to the newly commanded volume level without producing artifacts such as pops and clicks.

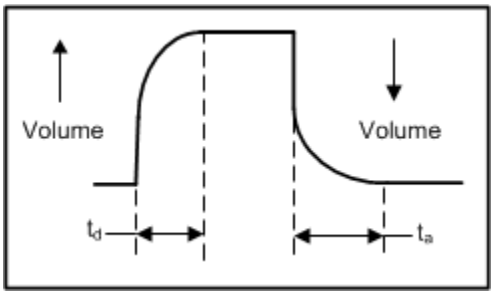


Figure 3-7. Volume Attack and Release

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3.4 DPEQ

The dynamic parametric equalizer (DPEQ) mixes the audio signals routed through two paths containing one biquad each, based upon the signal level detected by the sense path, as shown in Figure 3-8.

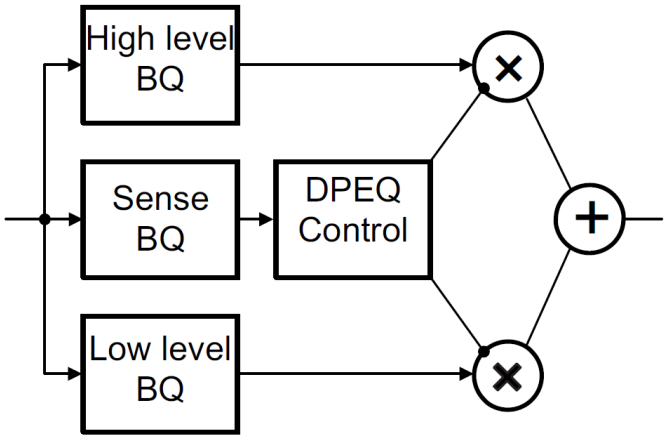


Figure 3-8. DPEQ

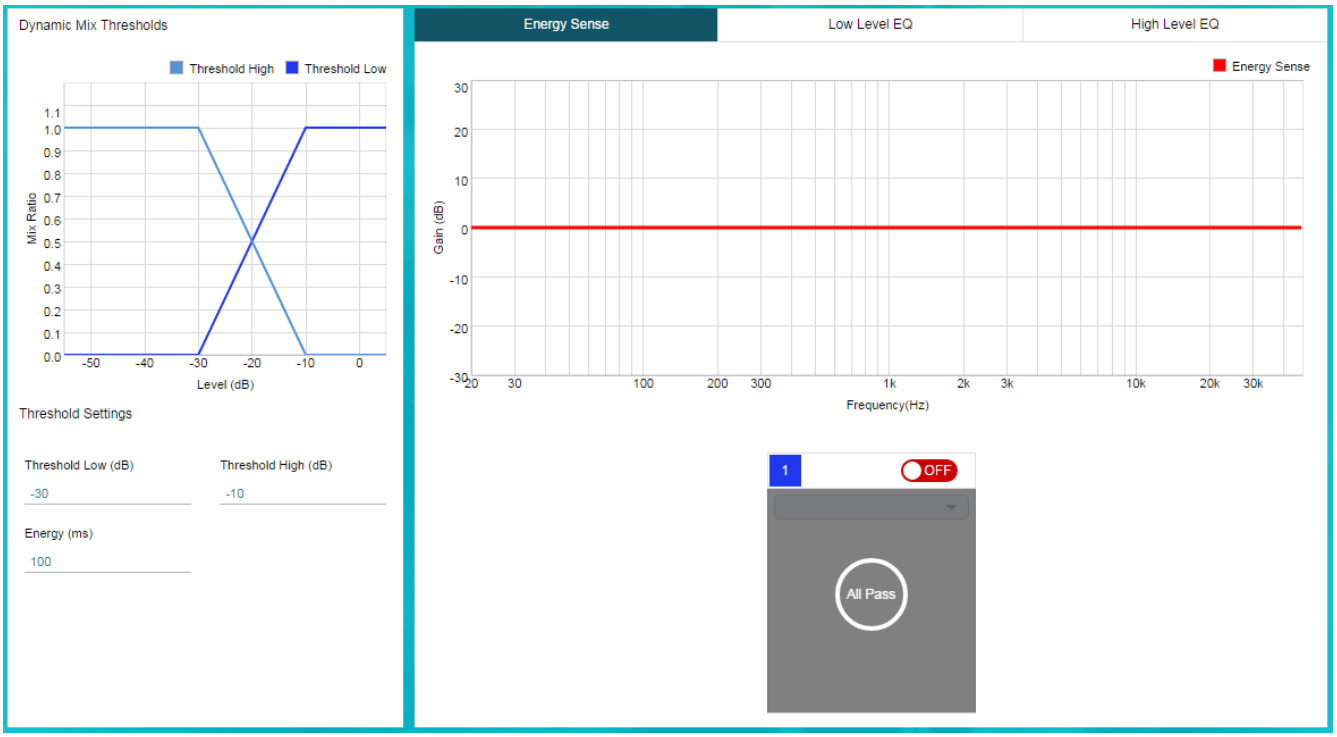


Figure 3-9. DPEQ Tuning Window

3.4.1 DPEQ

Energy (ms) simply tells the algorithm for how long to average the samples of audio before determining how the sample compares to the mixing thresholds. The shorter the time, the faster the mixer reacts to changes in the input signal level. The longer the time, the slower the mixer reacts to changes in level.

The mixing of the two paths (low-level and high-level) is controlled by setting *Threshold Low (dB)* and *Threshold High (dB)*. When the averaged signal (as set by the *Energy*) is below the *Threshold Low*, the dynamic mixer sends all of the audio through the low-level path. When the signal is above the *Threshold High*, the signal is sent

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through the upper-level path. When the signal is between the two, the signal is mixed together by the dynamic mixer level.

3.4.2 Energy Sense

The sense path contains one configurable biquad, which can be used to focus the DEQ sensing on a specific frequency bandwidth.

3.4.3 Low Level EQ

The low-level path also has one configurable biquad to establish the EQ curve the audio is sent through when the time average signal is at a low-level. This fully-functional biquad can be assigned to several filter types. This assignment determines the frequency response when low-level is active based on the *Energy* configuration and the mixing thresholds.

3.4.4 High Level EQ

The high-level path, similar to the low-level path, has one biquad that can set the EQ curve used when the time averaged input signal is above the upper mixing threshold.

3.5 2-Band DRC

The dynamic range control (DRC) is a feed-forward mechanism that can be used to automatically control the audio signal amplitude or the dynamic range within specified limits. The dynamic range control is done by sensing the audio signal level using an estimate of the alpha filter energy then adjusting the gain based on the region and slope parameters that are defined. The 2-Band DRC is shown in Figure 3-10.

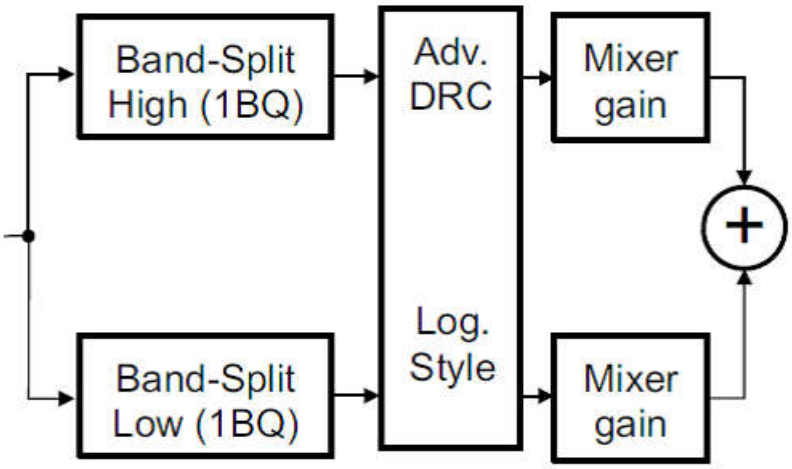


Figure 3-10. 2-Band DRC

The DRC works to reduce the peak of energy if the energy goes beyond the programmable threshold level. The DRC starts an attack event (reduces gain) if energy goes above the threshold. Similarly, DRC starts a release event if the level goes below the threshold (increases gain back to the original value). Attack and release events occur only when the level remains above or below the threshold continuously during the time-constant time. The constant time is controlled by the attack and release rate. If the attack and release rate is short, the DRC operates frequently. The attack time defines how fast to cut the signal to bring the signal under the threshold. Similarly, the release time defines how fast to release the cut back to normal.

The 2-band DRC is comprised of two DRCs that can be split into two bands using the BQ at the input of each band. The DRC in each band is equipped individual with energy, attack, and decay time constants as shown in Figure 3-11.

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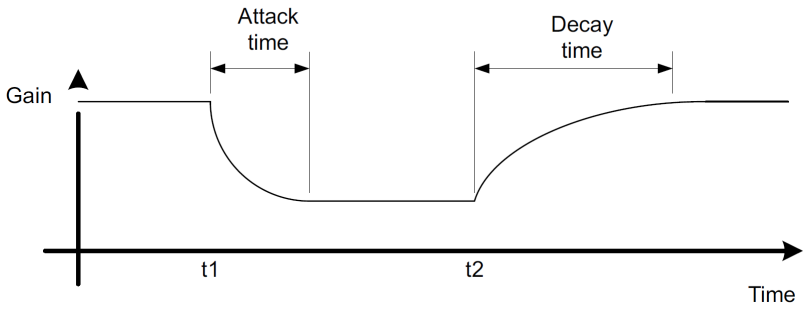


Figure 3-11. 2-Band DRC Attack and Decay

This DRC can be used for power limiting and signal compression. Therefore, the DRC must be tested with maximum signal levels for the desired application. Use a resistive load for initial testing. However, the speaker used in the end application must be used for final testing and tweaking.

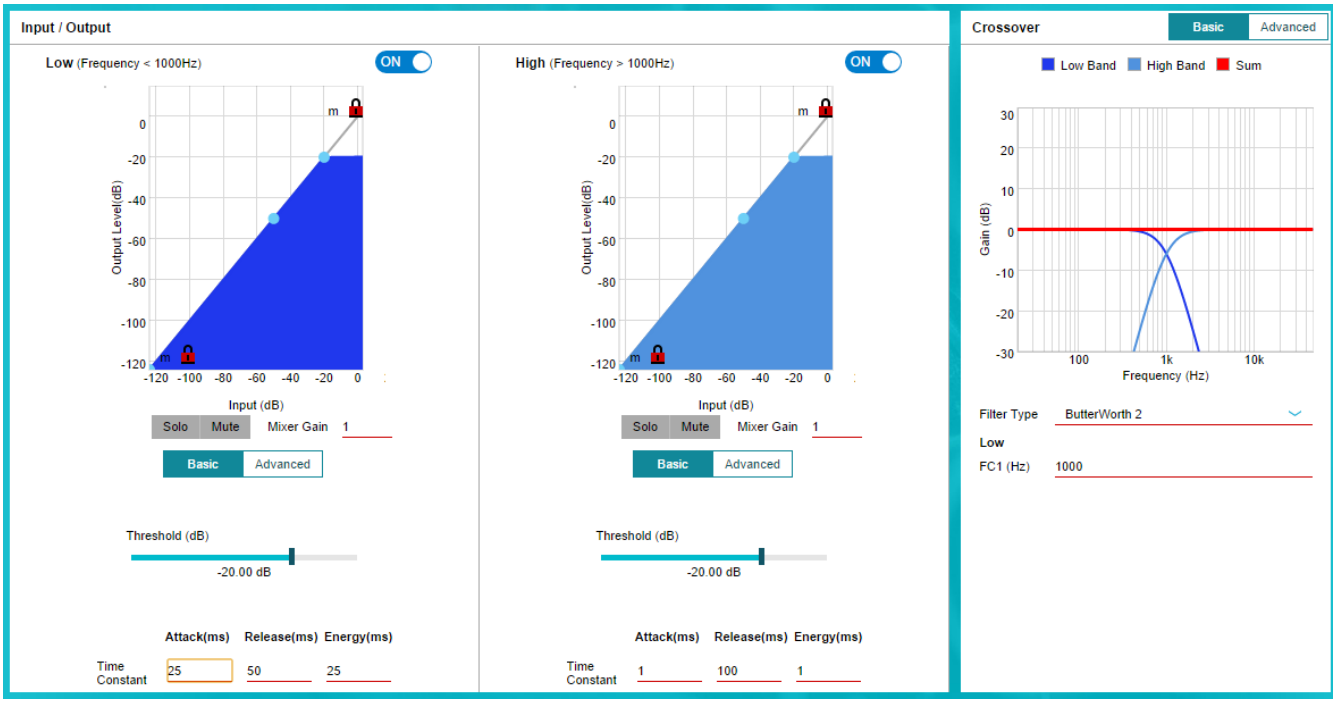


Figure 3-12. 2-Band DRC Tuning Window

The *2-Band DRC Tuning* window as shown in Figure 3-12 consists of two identical windows for low and high bands. Each has a DRC curve that offers three regions of compression. The points on the DRC curve can be dragged and dropped.

Below each DRC plot, parameters such as threshold, offset, and ratio can be manually typed in for each of the three regions. By typing a value and pressing *Enter* on the keyboard, the DRC curve automatically adjusts to the entered parameter.

3.5.1 DRC Time Constant

Change time constants by entering new values for each band. Attack(ms) determines the attack time of the DRC and Release(ms) determines the release time once the windowed energy band passes. Energy(ms) controls the time averaging windowing used to determine the average signal energy, and therefore, how the incoming signal compares to the set DRC curve. Having control over the DRC time constant for a given frequency band is beneficial for avoiding beating tones caused by the DRC attack and the incoming signal frequency.

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The mixer gain controls the relative gain of each of the two frequency bands after the DRCs when the frequencies are mixed together. This function is used to attenuate one of the frequency bands relative to the other, if needed. Make note of the sign of the gain coefficients. Since filters affect phase, a phase reversal or a 180 degree phase shift is potentially necessary. Use a negative sign on the coefficient to reverse the phase for the second order LR filter.

3.5.2 Crossover

By default, the two-band crossover frequencies are set to 1000Hz, using second-order Linkwitz-Riley filters. This filter type is chosen because the total sum of the two-band signals has a flat response without having to calculate individual crossover frequencies for unity summation. The crossover frequencies must be separated far enough in the frequency range from each other to avoid any dip caused by the filter sum response.

3.6 AGL

The automatic gain limiter (AGL) is a feedback mechanism that can be used to automatically control the audio signal amplitude or dynamic range within specified limits. Automatic gain limiting is done by sensing the audio signal level using an alpha filter energy structure at the output of the AGL, then adjusting the gain based on whether the signal level is above or below the defined threshold. Three decisions made by the AGL are engage, disengage, or do nothing. The rate at which the AGL engages or disengages depends on the attack and release settings respectively.

Figure 3-13 shows the *AGL Tuning* window. By default, the AGL is disabled and can be enabled by clicking the ON or OFF switch at the top right corner.

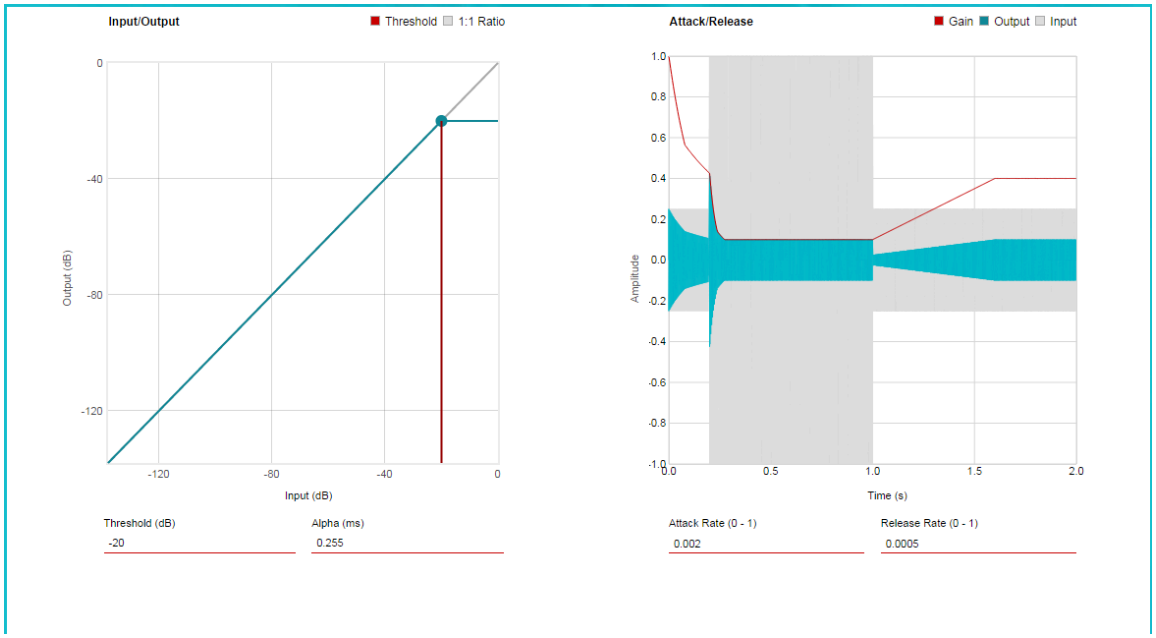


Figure 3-13. AGL Tuning Window

Threshold (db)	This parameter sets the threshold at which the compressor is activated. Lowering the threshold causes the compression to be activated at lower volume levels. Once the signal exceeds this threshold, compression is applied.
Alpha (ms)	This parameter configures the sharpness of the compression knee of the AGL.
Attack Rate (0 – 1)	This parameter controls how quickly compression is applied to the signal. Higher values cause the compressor to respond to signals quickly, while lower values decrease the response time.
Release Rate (0 – 1)	This parameter controls how quickly compression is removed from the signal as the signal gets quieter. Higher values cause the compressor to release from signals quickly, while lower values decrease the release time.

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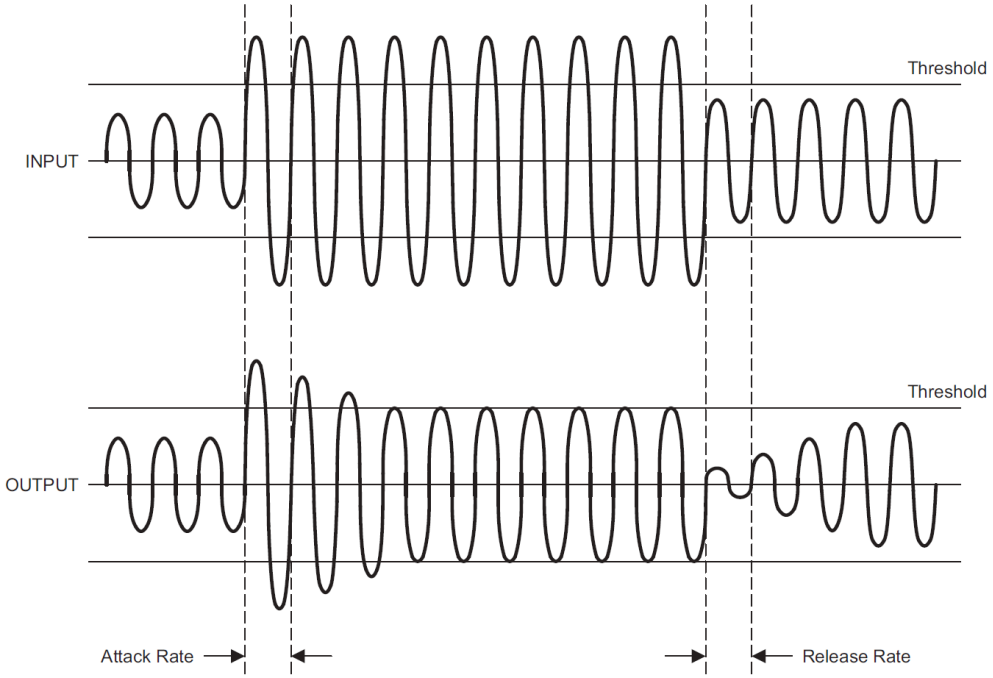


Figure 3-14. AGL Attack and Release

3.7 Clipper

The Clipper, shown in Figure 3-15, can be used to achieve digitally the specified THD levels without voltage clipping. Clipper allows users to achieve the same THD (for example, 10% THD) for different power levels (15W, 10W, 5W) with same the PVDD level.

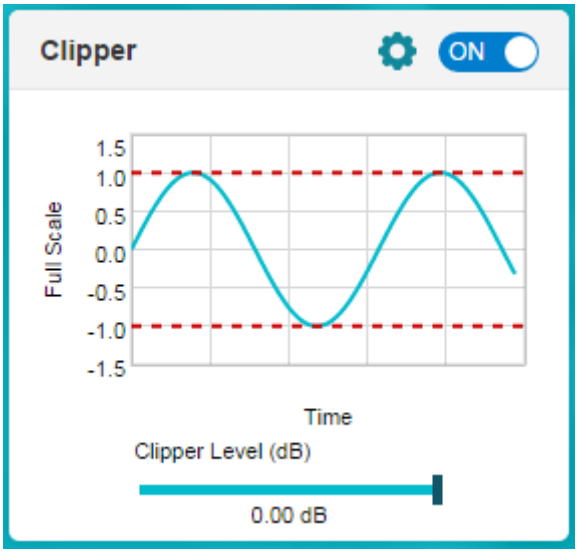


Figure 3-15. Clipper

Clipper Level (dB)	The clipper level controls the signal level at which clipping occurs.
Makeup Gain (dB)	The makeup gain sets additional gain steps from –110dB to 6dB.

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3.8 Output Crossbar

The crossbar provides the end user with a very flexible way to control what finally appears on amplifier outputs and I2S SDOUT. The *Basic* tab shown in Figure 3-16 provides the easiest way for configuration. Go to the *Advanced* tab, shown in Figure 3-17, if more parameters must be adjusted.

Note

All the parameters must be specified in decibels (dB).

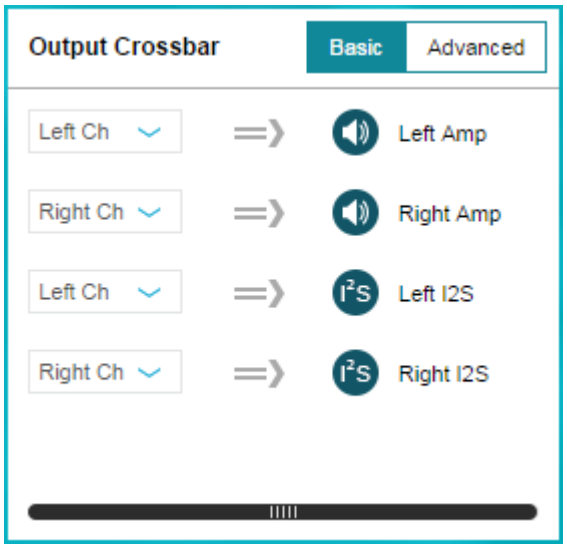


Figure 3-16. Output Crossbar (Basic Tab)

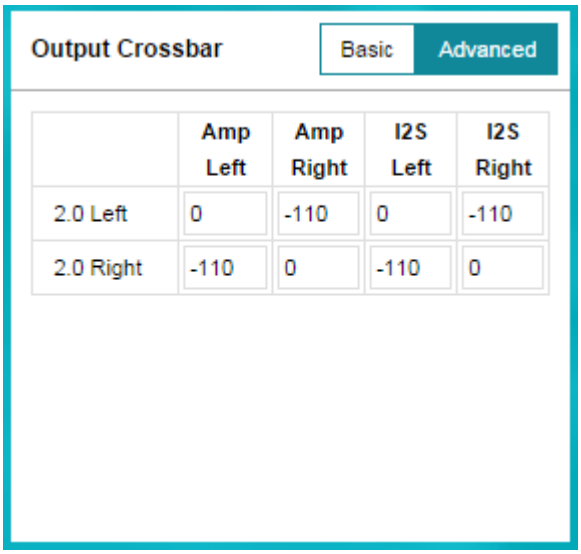


Figure 3-17. Output Crossbar (Advanced Tab)

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A Appendix

A.1 DSP Memory Map

Table A-1. Mode Memory Map — Book 0x78

Sub Address	Page	Register Name	Number of Bytes | Format	Default Value	Description
Level Meter					
0x60	0x02	Level Meter Left Output	4 | 1.31	0x00000000	Level Meter Left Output Flag
0x64	0x02	Level Meter Right Output	4 | 1.31	0x00000000	Level Meter Right Output Flag

Table A-2. Mode Memory Map — Book 0x8C

Sub Address	Page	Register Name	Number of Bytes | Format	Default Value	Description
Input Mixer					
0x18	0x29	Left to Left	4 | 9.23	0x00800000	Left Channel Mixer Left Input Gain
0x1C	0x29	Right to Left	4 | 9.23	0x00000000	Left Channel Mixer Right Input Gain
0x20	0x29	Left to Right	4 | 9.23	0x00000000	Right Channel Mixer Left Input Gain
0x24	0x29	Right to Right	4 | 9.23	0x00800000	Right Channel Mixer Right Input Gain
Volume Control					
0x24	0x2A	CH-L Volume	4 | 9.23	0x00800000	Left Channel Volume Coefficient
0x28	0x2A	CH-R Volume	4 | 9.23	0x00800000	Right Channel Volume Coefficient
0x30	0x2A	Softening Filter Alpha	4 | 1.31	0x00E2C46B	Volume Time Constant
DRC					
0x34	0x2B	DRC1 Energy	4 | 1.31	0x7FFFFFFF	DRC1 Energy Time Constant
0x38	0x2B	DRC1 Attack	4 | 1.31	0x7FFFFFFF	DRC1 Attack Time Constant
0x3C	0x2B	DRC1 Decay	4 | 1.31	0x7FFFFFFF	DRC1 Decay Time Constant
0x40	0x2B	K0_1	4 | 9.23	0x00000000	DRC1 Region 1 Slope (Comp/Exp)
0x44	0x2B	K1_1	4 | 9.23	0x00000000	DRC1 Region 2 Slope (Comp/Exp)
0x48	0x2B	K2_1	4 | 9.23	0x00000000	DRC1 Region 3 Slope (Comp/Exp)
0x4C	0x2B	T1_1	4 | 9.23	0xE7000000	DRC1 Threshold 1
0x50	0x2B	T2_1	4 | 9.23	0xFE800000	DRC1 Threshold 2
0x54	0x2B	off1_1	4 | 9.23	0x00000000	DRC1 Offset 1
0x58	0x2B	off2_1	4 | 9.23	0x00000000	DRC1 Offset 2
Level Meter					
0x0C	0x2C	LM Left from Left Input	4 | 9.23	0x00000000	Level Meter Left Gain from Left Input
0x10	0x2C	LM Left from Right Input	4 | 9.23	0x00000000	Level Meter Left Gain from Right Input
0x14	0x2C	LM Left from Left Output	4 | 9.23	0x00800000	Level Meter Left Gain from Left Output
0x18	0x2C	LM Left from Right Output	4 | 9.23	0x00800000	Level Meter Left Gain from Right Output
Output Crossbar					
0x1C	0x2C	Analog Left from Left Output	4 | 9.23	0x00800000	Analog Left Output Gain from left Output
0x20	0x2C	Analog Left from Right Output	4 | 9.23	0x00000000	Analog Left Output Gain from Right Output
0x28	0x2C	Analog Right from Left Output	4 | 9.23	0x00000000	Analog Right Output Gain from left Output
0x2C	0x2C	Analog Right from Right Output	4 | 9.23	0x00800000	Analog Right Output Gain from Right Output
0x34	0x2C	Digital Left from Left Output	4 | 9.23	0x00800000	I2S Left Output Gain from left Output
0x38	0x2C	Digital Left from Right Output	4 | 9.23	0x00000000	I2S Left Output Gain from Right Output
0x40	0x2C	Digital Left from Left Input	4 | 9.23	0x00000000	I2S Left Output Gain from left Input
0x44	0x2C	Digital Left from Right Input	4 | 9.23	0x00000000	I2S Left Output Gain from Right Input
0x48	0x2C	Digital Right from Left Output	4 | 9.23	0x00000000	I2S Right Output Gain from left Output
0x4C	0x2C	Digital Right from Right Output	4 | 9.23	0x00800000	I2S Right Output Gain from Right Output
0x54	0x2C	Digital Right from Left Input	4 | 9.23	0x00000000	I2S Right Output Gain from left Input
0x58	0x2C	Digital Right from Right Input	4 | 9.23	0x00000000	I2S Right Output Gain from Right Input
AGL					
0x5C	0x2C	Release Rate	4 | 1.31	0x00005762	AGL Release Time Constant

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Table A-2. Mode Memory Map — Book 0x8C (continued)

Sub Address	Page	Register Name	Number of Bytes | Format	Default Value	Description
0x60	0x2C	Attack Rate	4 | 1.31	0x000369D0	AGL Attack Time Constant
0x64	0x2C	Threshold	4 | 5.27	0x40000000	Threshold Linear
0x68	0x2C	AGL Enable	4 | 1.31	0x40000000	AGL Enable Flag
0x6C	0x2C	Softening Filter Alpha	4 | 1.31	0x051EB852	AGL Energy Time Constant
0x18	0x2D	Softening Filter Omega	4 | 1.31	0x7AE147AE	AGL Omega Time Constant
Level Meter					
0x1C	0x2D	LM Softening Filter Alpha	4 | 1.31	0x00005762	Level Meter Energy Time Constant
0x20	0x2D	LM Right from Left Input	4 | 9.23	0x00000000	Level Meter Right Gain from Left Input
0x24	0x2D	LM Right from Right Input	4 | 9.23	0x00000000	Level Meter Right Gain from Right Input
0x28	0x2D	LM Right from Left Output	4 | 9.23	0x00800000	Level Meter Right Gain from Left Output
0x2C	0x2D	LM Right from Right Output	4 | 9.23	0x00800000	Level Meter Right Gain from Right Output
DPEQ Control					
0x30	0x2D	Alpha	4 | 1.31	0x02DEAD00	DPEQ Sense Energy Time Constant
0x34	0x2D	Offset	4 | 1.31	0x0020C49B	DPEQ Threshold Offset
0x38	0x2D	Gain	4 | 1.31	0x74013901	DPEQ Threshold Gain
DRC					
0x58	0x2D	DRC2 Energy	4 | 1.31	0x7FFFFFFF	DRC2 Energy Time Constant
0x5C	0x2D	DRC2 Attack	4 | 1.31	0x7FFFFFFF	DRC2 Attack Time Constant
0x60	0x2D	DRC2 Decay	4 | 1.31	0x7FFFFFFF	DRC2 Decay Time Constant
0x64	0x2D	k0_2	4 | 9.23	0x00000000	DRC2 Region 1 Slope (Comp/Exp)
0x68	0x2D	k1_2	4 | 9.23	0x00000000	DRC2 Region 2 Slope (Comp/Exp)
0x6C	0x2D	k1_2	4 | 9.23	0x00000000	DRC2 Region 3 Slope (Comp/Exp)
0x70	0x2D	t1_2	4 | 9.23	0xE7000000	DRC2 Threshold 1
0x74	0x2D	t2_2	4 | 9.23	0xFE800000	DRC2 Threshold 2
0x78	0x2D	off1_2	4 | 9.23	0x00000000	DRC2 Offset 1
0x7C	0x2D	off2_2	4 | 9.23	0x00000000	DRC2 Offset 2
0x08	0x2E	DRC 1 Mixer Gain	4 | 9.23	0x00800000	DRC 1 Mixer Gain Coefficient
0x10	0x2E	DRC 2 Mixer Gain	4 | 9.23	0x00000000	DRC 2 Mixer Gain Coefficient
FS Clipper					
0x18	0x2E	CH-LR THD Boost	4 | 9.23	0x00800000	THD LR Channel Prescale Coefficient
0x1C	0x2E	CH-L Fine Volume	4 | 2.30	0x3FFFFFFF	THD L Channel Postscale Coefficient
0x20	0x2E	CH-R Fine Volume	4 | 2.30	0x3FFFFFFF	THD R Channel Postscale Coefficient

Table A-3. Mode Memory Map — Book 0xAA

Sub Address	Page	Register name	Number of Bytes | Format	Default Value	Description
EQ Left 14 BQS					
0x18	0x24	CH-L BQ 1 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x1C	0x24	CH-L BQ 1 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x20	0x24	CH-L BQ 1 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x24	0x24	CH-L BQ 1 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x28	0x24	CH-L BQ 1 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x2C	0x24	CH-L BQ 2 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x30	0x24	CH-L BQ 2 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x34	0x24	CH-L BQ 2 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x38	0x24	CH-L BQ 2 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x3C	0x24	CH-L BQ 2 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x40	0x24	CH-L BQ 3 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x44	0x24	CH-L BQ 3 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x48	0x24	CH-L BQ 3 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x4C	0x24	CH-L BQ 3 A1	4 | 5.27	0x00000000	Left BQ Coefficient

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Table A-3. Mode Memory Map — Book 0xAA (continued)

Sub Address	Page	Register name	Number of Bytes | Format	Default Value	Description
0x50	0x24	CH-L BQ 3 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x54	0x24	CH-L BQ 4 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x58	0x24	CH-L BQ 4 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x5C	0x24	CH-L BQ 4 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x60	0x24	CH-L BQ 4 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x64	0x24	CH-L BQ 4 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x68	0x24	CH-L BQ 5 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x6C	0x24	CH-L BQ 5 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x70	0x24	CH-L BQ 5 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x74	0x24	CH-L BQ 5 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x78	0x24	CH-L BQ 5 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x7C	0x24	CH-L BQ 6 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x08	0x25	CH-L BQ 6 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x0C	0x25	CH-L BQ 6 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x10	0x25	CH-L BQ 6 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x14	0x25	CH-L BQ 6 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x18	0x25	CH-L BQ 7 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x1C	0x25	CH-L BQ 7 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x20	0x25	CH-L BQ 7 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x24	0x25	CH-L BQ 7 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x28	0x25	CH-L BQ 7 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x2C	0x25	CH-L BQ 8 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x30	0x25	CH-L BQ 8 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x34	0x25	CH-L BQ 8 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x38	0x25	CH-L BQ 8 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x3C	0x25	CH-L BQ 8 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x40	0x25	CH-L BQ 9 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x44	0x25	CH-L BQ 9 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x48	0x25	CH-L BQ 9 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x4C	0x25	CH-L BQ 9 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x50	0x25	CH-L BQ 9 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x54	0x25	CH-L BQ 10 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x58	0x25	CH-L BQ 10 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x5C	0x25	CH-L BQ 10 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x60	0x25	CH-L BQ 10 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x64	0x25	CH-L BQ 10 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x68	0x25	CH-L BQ 11 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x6C	0x25	CH-L BQ 11 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x70	0x25	CH-L BQ 11 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x74	0x25	CH-L BQ 11 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x78	0x25	CH-L BQ 11 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x7C	0x25	CH-L BQ 12 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x08	0x26	CH-L BQ 12 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x0C	0x26	CH-L BQ 12 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x10	0x26	CH-L BQ 12 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x14	0x26	CH-L BQ 12 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x18	0x26	CH-L BQ 13 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x1C	0x26	CH-L BQ 13 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x20	0x26	CH-L BQ 13 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x24	0x26	CH-L BQ 13 A1	4 | 5.27	0x00000000	Left BQ Coefficient

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Table A-3. Mode Memory Map — Book 0xAA (continued)

Sub Address	Page	Register name	Number of Bytes | Format	Default Value	Description
0x28	0x26	CH-L BQ 13 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x2C	0x26	CH-L BQ 14 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x30	0x26	CH-L BQ 14 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x34	0x26	CH-L BQ 14 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x38	0x26	CH-L BQ 14 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x3C	0x26	CH-L BQ 14 A2	4 | 5.27	0x00000000	Left BQ Coefficient
Post EQ1					
0x40	0x26	CH-L BQ 1 B0	4 | 5.27	0x08000000	Left Post BQ Coefficient
0x44	0x26	CH-L BQ 1 B1	4 | 5.27	0x00000000	Left Post BQ Coefficient
0x48	0x26	CH-L BQ 1 B2	4 | 5.27	0x00000000	Left Post BQ Coefficient
0x4C	0x26	CH-L BQ 1 A1	4 | 5.27	0x00000000	Left Post BQ Coefficient
0x50	0x26	CH-L BQ 1 A2	4 | 5.27	0x00000000	Left Post BQ Coefficient
EQ Right 14 BQS					
0x18	0x24	CH-L BQ 1 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x1C	0x24	CH-L BQ 1 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x20	0x24	CH-L BQ 1 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x24	0x24	CH-L BQ 1 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x28	0x24	CH-L BQ 1 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x2C	0x24	CH-L BQ 2 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x30	0x24	CH-L BQ 2 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x34	0x24	CH-L BQ 2 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x38	0x24	CH-L BQ 2 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x3C	0x24	CH-L BQ 2 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x40	0x24	CH-L BQ 3 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x44	0x24	CH-L BQ 3 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x48	0x24	CH-L BQ 3 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x4C	0x24	CH-L BQ 3 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x50	0x24	CH-L BQ 3 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x54	0x24	CH-L BQ 4 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x58	0x24	CH-L BQ 4 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x5C	0x24	CH-L BQ 4 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x60	0x24	CH-L BQ 4 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x64	0x24	CH-L BQ 4 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x68	0x24	CH-L BQ 5 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x6C	0x24	CH-L BQ 5 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x70	0x24	CH-L BQ 5 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x74	0x24	CH-L BQ 5 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x78	0x24	CH-L BQ 5 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x7C	0x24	CH-L BQ 6 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x08	0x25	CH-L BQ 6 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x0C	0x25	CH-L BQ 6 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x10	0x25	CH-L BQ 6 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x14	0x25	CH-L BQ 6 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x18	0x25	CH-L BQ 7 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x1C	0x25	CH-L BQ 7 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x20	0x25	CH-L BQ 7 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x24	0x25	CH-L BQ 7 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x28	0x25	CH-L BQ 7 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x2C	0x25	CH-L BQ 8 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x30	0x25	CH-L BQ 8 B1	4 | 5.27	0x00000000	Left BQ Coefficient

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Table A-3. Mode Memory Map — Book 0xAA (continued)

Sub Address	Page	Register name	Number of Bytes | Format	Default Value	Description
0x34	0x25	CH-L BQ 8 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x38	0x25	CH-L BQ 8 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x3C	0x25	CH-L BQ 8 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x40	0x25	CH-L BQ 9 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x44	0x25	CH-L BQ 9 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x48	0x25	CH-L BQ 9 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x4C	0x25	CH-L BQ 9 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x50	0x25	CH-L BQ 9 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x54	0x25	CH-L BQ 10 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x58	0x25	CH-L BQ 10 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x5C	0x25	CH-L BQ 10 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x60	0x25	CH-L BQ 10 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x64	0x25	CH-L BQ 10 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x68	0x25	CH-L BQ 11 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x6C	0x25	CH-L BQ 11 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x70	0x25	CH-L BQ 11 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x74	0x25	CH-L BQ 11 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x78	0x25	CH-L BQ 11 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x7C	0x25	CH-L BQ 12 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x08	0x26	CH-L BQ 12 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x0C	0x26	CH-L BQ 12 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x10	0x26	CH-L BQ 12 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x14	0x26	CH-L BQ 12 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x18	0x26	CH-L BQ 13 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x1C	0x26	CH-L BQ 13 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x20	0x26	CH-L BQ 13 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x24	0x26	CH-L BQ 13 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x28	0x26	CH-L BQ 13 A2	4 | 5.27	0x00000000	Left BQ Coefficient
0x2C	0x26	CH-L BQ 14 B0	4 | 5.27	0x08000000	Left BQ Coefficient
0x30	0x26	CH-L BQ 14 B1	4 | 5.27	0x00000000	Left BQ Coefficient
0x34	0x26	CH-L BQ 14 B2	4 | 5.27	0x00000000	Left BQ Coefficient
0x38	0x26	CH-L BQ 14 A1	4 | 5.27	0x00000000	Left BQ Coefficient
0x3C	0x26	CH-L BQ 14 A2	4 | 5.27	0x00000000	Left BQ Coefficient
Post EQ1					
0x7C	0x28	CH-R BQ B0	4 | 5.27	0x08000000	Right Post BQ Coefficient
0x08	0x29	CH-R BQ B1	4 | 5.27	0x00000000	Right Post BQ Coefficient
0x0C	0x29	CH-R BQ B2	4 | 5.27	0x00000000	Right Post BQ Coefficient
0x10	0x29	CH-R BQ A1	4 | 5.27	0x00000000	Right Post BQ Coefficient
0x14	0x29	CH-R BQ A2	4 | 5.27	0x00000000	Right Post BQ Coefficient
DRC Low Band BQS					
0x34	0x2A	DRC low BQ 1 B0	4 | 1.31	0x7FFFFFFF	DRC Low BQ Coefficient
0x38	0x2A	DRC low BQ 1 B1	4 | 2.30	0x00000000	DRC Low BQ Coefficient
0x3C	0x2A	DRC low BQ 1 B2	4 | 1.31	0x00000000	DRC Low BQ Coefficient
0x40	0x2A	DRC low BQ 1 A1	4 | 2.30	0x00000000	DRC Low BQ Coefficient
0x44	0x2A	DRC low BQ 1 A2	4 | 1.31	0x00000000	DRC Low BQ Coefficient
0x48	0x2A	DRC low BQ 2 B0	4 | 1.31	0x7FFFFFFF	DRC Low BQ Coefficient
0x4C	0x2A	DRC low BQ 2 B1	4 | 2.30	0x00000000	DRC Low BQ Coefficient
0x50	0x2A	DRC low BQ 2 B2	4 | 1.31	0x00000000	DRC Low BQ Coefficient
0x54	0x2A	DRC low BQ 2 A1	4 | 2.30	0x00000000	DRC Low BQ Coefficient
0x58	0x2A	DRC low BQ 2 A2	4 | 1.31	0x00000000	DRC Low BQ Coefficient

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Table A-3. Mode Memory Map — Book 0xAA (continued)

Sub Address	Page	Register name	Number of Bytes | Format	Default Value	Description
DPEQ High Level Path BQ					
0x5C	0x2A	BQ 1 B0	4 | 5.27	0x08000000	DPEQ High BQ Coefficient
0x60	0x2A	BQ 1 B1	4 | 5.27	0x00000000	DPEQ High BQ Coefficient
0x64	0x2A	BQ 1 B2	4 | 5.27	0x00000000	DPEQ High BQ Coefficient
0x68	0x2A	BQ 1 A1	4 | 5.27	0x00000000	DPEQ High BQ Coefficient
0x6C	0x2A	BQ 1 A2	4 | 5.27	0x00000000	DPEQ High BQ Coefficient
DPEQ Low Level Path BQ					
0x70	0x2A	BQ 1 B0	4 | 5.27	0x08000000	DPEQ Low BQ Coefficient
0x74	0x2A	BQ 1 B1	4 | 5.27	0x00000000	DPEQ Low BQ Coefficient
0x78	0x2A	BQ 1 B2	4 | 5.27	0x00000000	DPEQ Low BQ Coefficient
0x7C	0x2A	BQ 1 A1	4 | 5.27	0x00000000	DPEQ Low BQ Coefficient
0x08	0x2B	BQ 1 A2	4 | 5.27	0x00000000	DPEQ Low BQ Coefficient
DRC High Band BQS					
0x0C	0x2B	DRC high BQ 1 B0	4 | 1.31	0x7FFFFFFF	DRC High BQ Coefficient
0x10	0x2B	DRC high BQ 1 B1	4 | 2.30	0x00000000	DRC High BQ Coefficient
0x14	0x2B	DRC high BQ 1 B2	4 | 1.31	0x00000000	DRC High BQ Coefficient
0x18	0x2B	DRC high BQ 1 A1	4 | 2.30	0x00000000	DRC High BQ Coefficient
0x1C	0x2B	DRC high BQ 1 A2	4 | 1.31	0x00000000	DRC High BQ Coefficient
0x20	0x2B	DRC high BQ 2 B0	4 | 1.31	0x7FFFFFFF	DRC High BQ Coefficient
0x24	0x2B	DRC high BQ 2 B1	4 | 2.30	0x00000000	DRC High BQ Coefficient
0x28	0x2B	DRC high BQ 2 B2	4 | 1.31	0x00000000	DRC High BQ Coefficient
0x2C	0x2B	DRC high BQ 2 A1	4 | 2.30	0x00000000	DRC High BQ Coefficient
0x30	0x2B	DRC high BQ 2 A2	4 | 1.31	0x00000000	DRC High BQ Coefficient
DPEQ Sense BQ					
0x40	0x2E	BQ 1 B0	4 | 5.27	0x08000000	DPEQ Sense BQ Coefficient
0x44	0x2E	BQ 1 B1	4 | 5.27	0x00000000	DPEQ Sense BQ Coefficient
0x48	0x2E	BQ 1 B2	4 | 5.27	0x00000000	DPEQ Sense BQ Coefficient
0x4C	0x2E	BQ 1 A1	4 | 5.27	0x00000000	DPEQ Sense BQ Coefficient
0x50	0x2E	BQ 1 A2	4 | 5.27	0x00000000	DPEQ Sense BQ Coefficient
Post EQ2					
0x7C	0x2E	CH –L BQ B0	4 | 5.27	0x08000000	Left Post BQ Coefficient
0x08	0x2F	CH-L BQ B1	4 | 5.27	0x00000000	Left Post BQ Coefficient
0x0C	0x2F	CH-L BQ B2	4 | 5.27	0x00000000	Left Post BQ Coefficient
0x10	0x2F	CH-L BQ A1	4 | 5.27	0x00000000	Left Post BQ Coefficient
0x14	0x2F	CH-L BQ A2	4 | 5.27	0x00000000	Left Post BQ Coefficient
0x1C	0x2F	CH-R BQ B0	4 | 5.27	0x08000000	Right Post BQ Coefficient
0x20	0x2F	CH-R BQ B1	4 | 5.27	0x00000000	Right Post BQ Coefficient
0x24	0x2F	CH-R BQ B2	4 | 5.27	0x00000000	Right Post BQ Coefficient
0x28	0x2F	CH-R BQ A1	4 | 5.27	0x00000000	Right Post BQ Coefficient
0x2C	0x2F	CH-R BQ A2	4 | 5.27	0x00000000	Right Post BQ Coefficient

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