Technical White Paper

Improving Thermal Performance in High Ambient Temperature Environments With Thermally Enhanced Packaging

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ABSTRACT

In today's communication equipment and enterprise markets, power requirements are ever increasing to meet the demands of evolving SoCs and FPGAs. This trend has pushed DC/DC buck switching regulators and power stages to be both rated for higher power and placed in greater density in limited board space. DC/DC regulators naturally generate heat due to power losses during conversion. Operating in environments with high ambient temperatures such as active antennae systems, baseband units, or small cell base stations, an also cause unavoidable thermal rise within the device as well. Buck converters and power stages must stay within a junction temperature range, rated by the vendor, in order to stay within the safe operating area (SOA) and prevent heating up neighboring devices. As device junction temperature rises with ambient temperature, the amount of current a given device can safely output decreases. This poses significant constraints for systems where high ambient temperatures are unavoidable but power requirements are high. It is, therefore, imperative to optimize heat dissipation in order to lessen thermal constraints and increase overall system efficiency.

This technical white paper covers common known methods of heat dissipation, what a Thermally Enhanced Package (TEP) is, and how TEP can improve heat dissipation with little to no drawbacks. Discussion will be on how heat is dissipated through existing packages, how PCB layout affects thermal dissipation, and how TEP can unlock a new way for heat to be dissipated from the IC.

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1 Understanding Thermals

DC/DC buck converter and power stage efficiency is inversely correlated with its power loss. Minimizing power loss is key to maximizing system efficiency. Two major sources of power loss include switching loss from the controller and conduction loss from the high-side and low-side MOSFETs within the power stage. As output currents increase, the contribution of conduction loss to overall power dissipation increases while that of the switching loss decreases.

Conduction loss manifests through the dissipation of heat energy, which causes the device's junction temperature to rise and is therefore directly related to thermal performance. High ambient temperatures cause an additional temperature rise at the junction, leaving even less margin for safe operation.

The junction-to-ambient thermal resistance, $R_{\theta JA}$, measures thermal resistance between the FET's junction and the ambient environment and is the most commonly reported metric for thermal performance. As show in Figure 1-1, it can be broken into two components: the upward thermal resistance between the junction through the top surface of the device to the surrounding ambient environment and the downward thermal resistance through the bottom of the device through the PCB board to the surrounding medium.

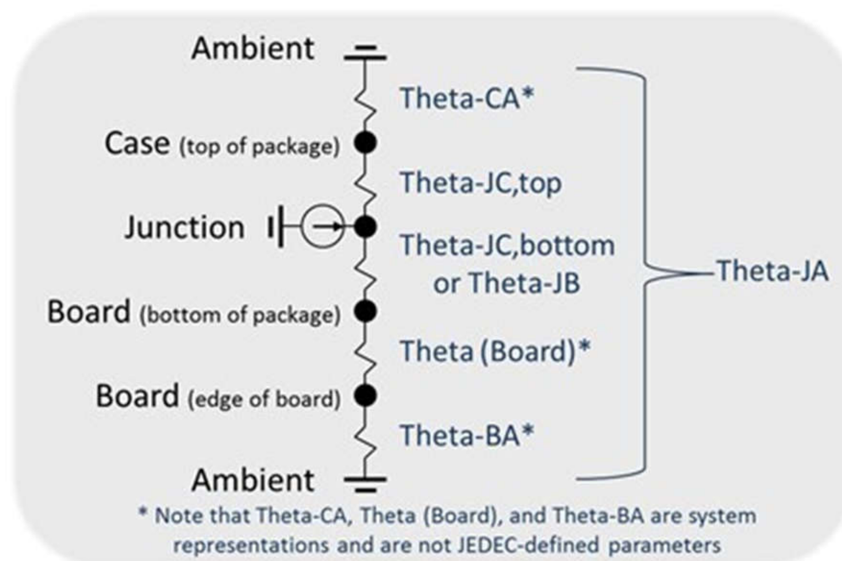

Figure 1-1. $R_{\theta JA}$ Breakdown

The most influential portion of heat dissipation is through the bottom side of the package, which is why most methods of heat dissipation today focus on PCB layout. However, optimizing the top side heat dissipation can also contribute to a lower overall $R_{\theta JA}$. This document addresses how the device packaging can be leveraged to lower the topside junction-to-case θ_{Jc}(top) to near zero, using Thermally Enhanced Packaging.

It is important to note that although $R_{\theta JA}$ is reported as a set value on many data sheets, the value is measured off a standard layout, often following the JEDEC standard. While the silicon chip design itself can affect thermal performance, PCB design and packaging technology are a much heavier influence in how efficiently a device can dissipate heat.

2 Methods of Heat Dissipation

To address optimizing $R_{\theta JA}$ through the bottom side of the device, the most common methods involve efficiently managing heat flow evenly throughout the PCB. Maximizing areas of conduction throughout the PCB is key to maximizing heat dissipation. This includes maximizing trace thickness, layer thickness, and board size.

V_{OUT}, GND, SW, and V_{IN} are all nodes from a buck converter that are recommended to have thicker traces and wider copper pours. Increasing the number of layers, and maximizing the thickness of the layers, within the PCB is another way to maximize copper area. A 6-layer board, for example, has much more copper area to dissipate heat than a 4-layer board. The same can be seen with the usage of thicker board layers.

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Fully utilizing the advantage of multiple layers requires using the correct thermal vias as well. As show in Figure 2-1, blind vias, which connect an outer layer to the inner layers, limit the heat dissipation to just one side of the board. A buried via, which connects inner layers, limits heat dissipation to just the inner layers of the board. A through hole via goes through all PCB layers, allowing heat to dissipate from the top side, through the inner layers, and out the bottom of the board.

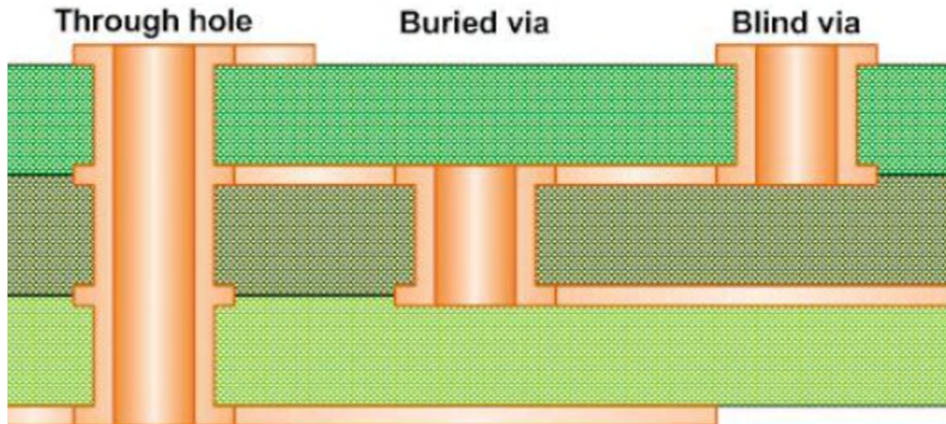

Figure 2-1. Types of Thermal Vias

Maximizing conduction surface area allows greater contact with ambient air, which leads to better heat dissipation.

2.1 Routable Lead Frame

While optimizing PCB layout has the greatest influence on overall system heat dissipation, the package of the IC itself must be carefully selected as well in order to optimize heat dissipation. The lead frame construction within the package can have significant influence in getting heat out of the silicon die and into the PCB and its surrounding environment.

Recent advancements in packaging technology have enabled the dissipation of heat from the package much more efficiently. In traditional wire bond QFN packaging shown in Figure 2-2, the bond wires that connect the silicon die to the outer pins add resistances that contribute to additional conduction loss. This conduction loss produces heat within the package that does not dissipate heat optimally out of the package, due to limited contact with the PCB.

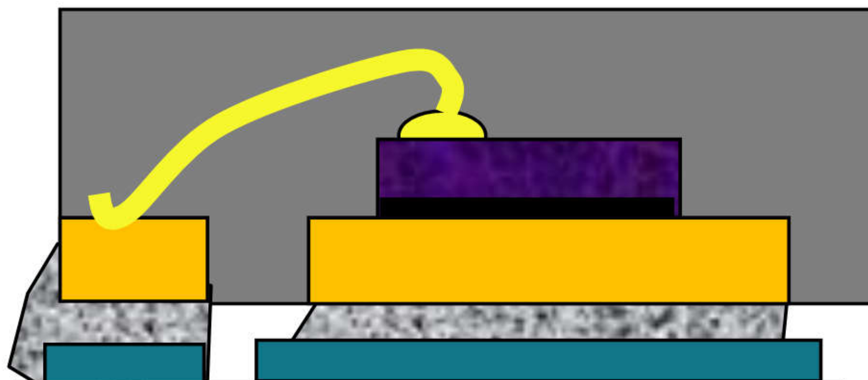

Figure 2-2. Wire-Bond QFN Package

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HotRod™ QFN packaging, shown in Figure 2-3, flips the chip and places the pins directly onto the lead frame using copper posts and gold or tin solder. This eliminates the need for bond wires, which decreases conduction loss and increases conductor contact with the PCB. However, pin-out design in a single layer lead frame can often limit the ground pad size, lowering the area of heat conduction within the package.

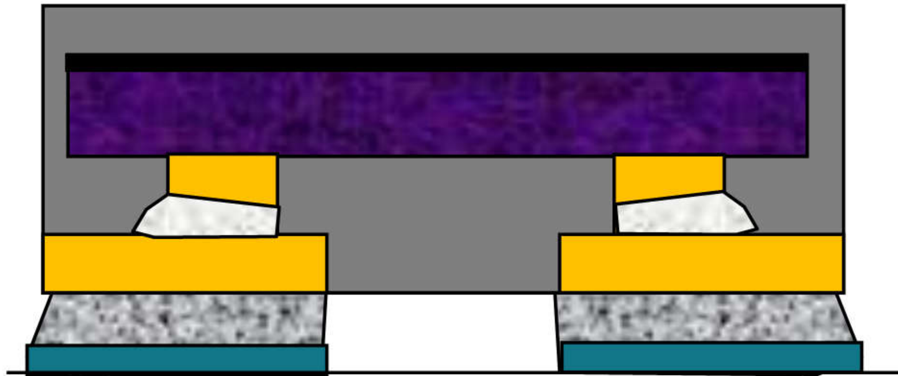

Figure 2-3. HotRod QFN Package

In order to enable more flexible pinout design, Routable lead frame QFN, the latest packaging technology, separates the lead frame into three layers of substrate with inner-layer trace connections, as shown in Figure 2-4. This enables most devices with this package to be designed with the maximum ground pad area on the bottom-most layer of the lead frame, allowing even better heat conduction contact with the PCB.

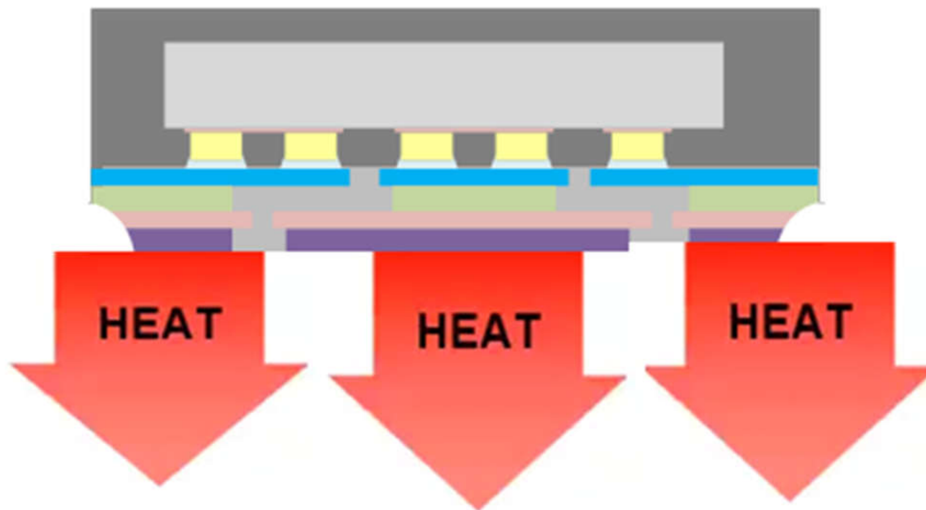

Figure 2-4. Routable Lead frame Package

3 Thermally Enhanced Package

For cooling through the top side of the package, heat sinks are commonly used to transfer heat out of IC packages into the ambient environment. Board designs, especially ones that include resource-intensive computing chipsets, will often have a heat sink covering the entire board in order to maximize surface area exposure to a fluid medium. The fluid medium could either be ambient static air, ambient airflow, or a liquid medium such as water, refrigerants, or oil. Figure 3-1 shows a visual diagram of component placement.

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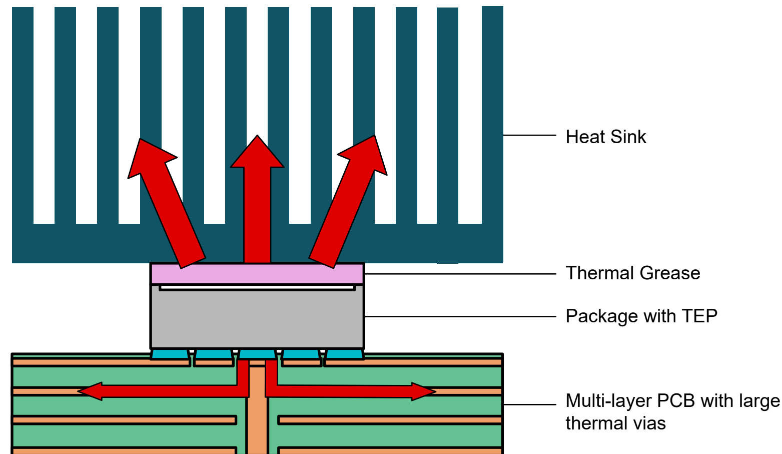

Figure 3-1. Converter With Heat Sink

A thermal paste is applied to the top of the device to evenly coat the conduction surface, then the heat sink is attached to maximize surface area for heat dissipation. Since most power management ICs are over-molded with a mold compound, package technology needs slight adjustments to optimized heat transfer to the heat sink.

Thermally Enhanced Package (TEP) technology exposes the inner silicon die on the top side of the package in order to have direct contact with a thermal paste and heat sink, enabling better heat conduction through the top side of the package. TEP is formed using a selective "film assist" mold process in which a thin film is used during the molding process to prevent mold flow over the die. The process flow is almost identical to the standard over-mold process, with the exception that the top side mold compound is left out in order to expose the silicon. Figure 3-2 shows a photo of TPS543B25T, a buck converter in a TEP, from the top side of the TPS543B25TEVM.

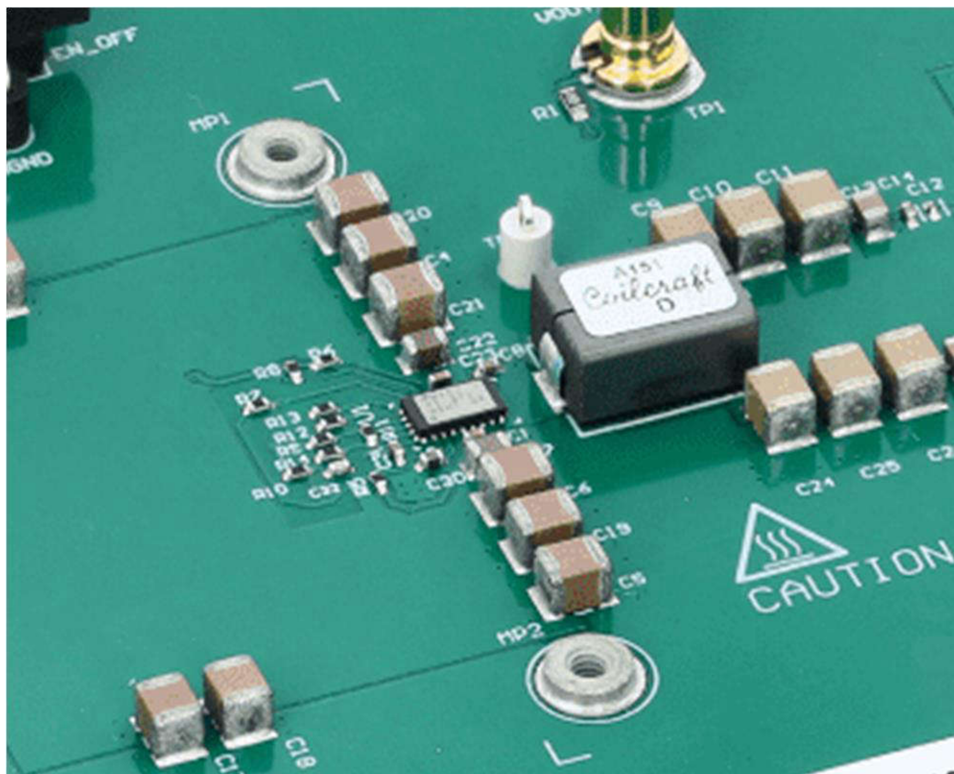

Figure 3-2. TPS543B25T Board Photo

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With the top side mold compound removed, the θ_{Jc}(top) of TPS543B25T is 0.2°C/W, a 0.6°C/W reduction from the over-molded version of the same device, TPS543B25. This yields a reduction in overall thermal resistance when a heat sink is applied, as shown in Table 3-1.

Table 3-1. $R_{\theta JA}$ Comparison, TPS543B25T vs TPS543B25

Device	$R_{\theta JA}$ (°C/W)
TPS543B25	12.3
TPS543B25 with heat sink	12.16
TPS543B25T without heat sink	11.8
TPS543B25T with heat sink	10.2
TPS543B25T with heat sink and airflow (200LFM)	7

A device with TEP with a heat sink can lower thermal resistance by approximately 2.1°C/W compared to a device with standard packaging without a heat sink. If airflow is applied, thermal resistance is reduced by a further 3.2°C/W.

When the device is under load, a lower thermal resistance yields a significant reduction in temperature rise, especially at higher current. Figure 3-3 shows the junction temperature (T_J) of TPS543B25T and TPS543B25 across load at 80°C ambient temperature (T_A). Both were tested on the TPS543B25EVM. Temperature rise was approximated by multiplying the measured power loss on the PG diode by the thermal resistance. T_J was calculated by adding the temperature rise to the 80°C T_A. Note that the rated maximum junction temperature for both TPS543B25 and TPS543B25T is 150°C.

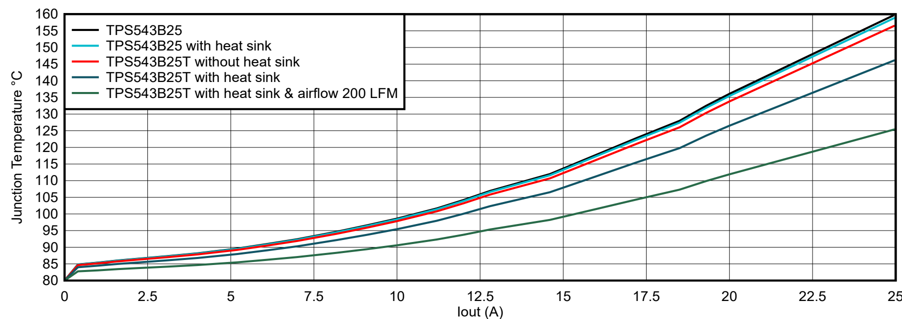

Figure 3-3. T_J Across Load, TPS543B25T vs TPS543B25

The T_J of TPS543B25T with a heat sink applied is 13.7°C cooler than TPS543B25 at full load, and can be cooled by an additional 20.8°C with air flow.

4 SOA Comparison

Lower junction temperatures across load widens the SOA of a given device, enabling higher current output in high ambient temperatures.

Figure 4-1 shows the SOA curve of the TPS543B25 buck converter vs the SOA curve of TPS543B25T.

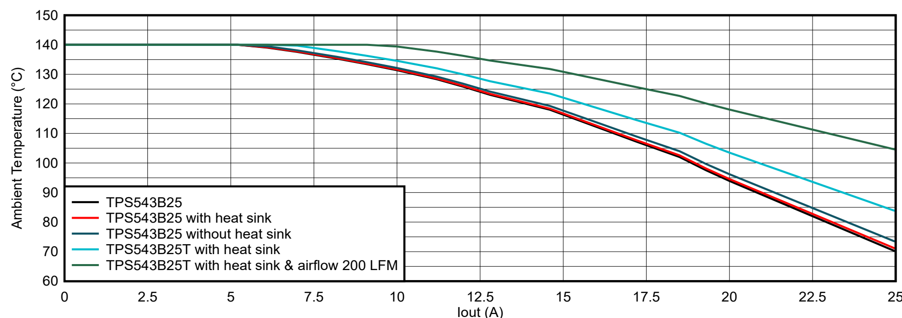

Figure 4-1. SOA Curve, TPS543B25T vs TPS543B25

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Standard package TPS543B25 would not be able to output full load at T_A above 70°C. A heat sink applied to the over-molded package also yields very little benefits. TPS543B25T with a heat sink can safely output full load at up to 83°C T_A, and up to 105°C T_A with airflow added.

Since the TEP benefits in SOA and junction temperature increase with output current, we can also extrapolate this data to infer that TEP will be even more beneficial in higher current (>25A) devices, especially in higher ambient temperature (85°C+ environments).

Note that there were no significant differences between the SOA of TPS543B25 and TPS543B25T when there is no heat sink used. The exposed silicon die is only able to conduct heat to ambient through a heat sink. There were also no significant differences found between the SOA of the standard package with heat sink and without heat sink, confirming that the top side mold compound prevents heat dissipation.

5 Conclusions

High ambient temperatures can significantly limit the power output of DC/DC buck converters and power stages in telecommunication and data center applications due to junction temperature rise. Optimizing heat dissipation is key to maximizing overall systems efficiency and cost. Thermally Enhanced Packaging (TEP) unlocks a new way for designers to dissipate heat to the ambient environment through exposing the silicon die. This package, combined with all the traditional methods of heat dissipation through the PCB and lead frame, makes an all-around solution that is fully optimized for thermal performance.

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