Application Note

DRV89xx-Q1 Open Load Detection (OLD) Application Guide and Analysis of Typical Problems

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ABSTRACT

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The DRV89xx-Q1 is a TI automotive-grade multi-channel half-bridge driver chip, widely used in automotive relay control, solenoid valve drive, LED lighting, and low-power DC motor drive applications. This paper systematically reviews three types of Active OLD related problems encountered by customers during development: OLD false alarms caused by active freewheeling in PWM mode, how to maintain output voltage in the OLD state through a Sleep-Wake cycle, and how LOLD (Low-Current Open-Load Detection) is triggered, providing correct register configuration methods and system design recommendations for practical applications.

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1 Application Background

1.1 Device Overview

The DRV89xx-Q1 series includes multiple versions corresponding to different numbers of output channels, with each output supporting a maximum continuous current of 1A, achieving complete configuration and diagnostic functions via a 5MHz 16-bit SPI interface, and integrating protection features such as overcurrent protection (OCP), undervoltage lockout (UVLO), overvoltage protection (OVP), overtemperature warning, and overtemperature shutdown (OTW/OTSD).

In practical engineering applications, besides typical motor loads, the DRV89xx-Q1 can also be used in various driving scenarios such as relays, valves, and LEDs; the DRV8908-Q1 integrates eight independent PWMs and can be used as a PWM generator, providing a certain driving capability compared to MCU outputs to directly control external loads, such as serving as fan control signals. Common applications are shown in the table below:

Table 1-1. DRV89xx-Q1 Typical Application Scenarios

Drive Mode	Typical Load	Current Range	Control Method
High-Side Switch (HSS)	Relay and valve control	200–300 mA	On/Off
High-Side Switch (HSS)	Indicator light	10–200 mA	PWM (200 Hz-1kHz)
High-Side Switch (HSS)	Ambient light	300mA–1A	PWM (200 Hz)
Low-Side Switch (LSS)	Relay control	200–300 mA	On/Off
Low-Side Switch (LSS)	Solenoid valve	1A	On/Off
PWM Generator	Pump control, seat fan control	≤20 mA	PWM (200 Hz)
Half-Bridge (H-Bridge)	HVAC damper motor	≤300 mA	PWM/On-Off

The control modes in the table include both PWM and On/off control; PWM control is achieved by setting the frequency and duty cycle of the half-bridge switching and depends on the chip's PWM generator mapping; On/off control is achieved by the MCU continuously rewriting the HBx_HS_EN or HBx_LS_EN registers via SPI to perform switching, which inherently does not support active freewheeling.

In application scenarios involving safety-related loads (such as engine start relay control), the system needs real-time diagnostics of the load connection status, making the Open Load Detection (OLD) function an indispensable diagnostic method.

1.2 Overview of OLD Function

The DRV89xx-Q1 provides four open load detection schemes to cover the diagnostic requirements of different driving scenarios, as detailed below:

Table 1-2. DRV89xx-Q1 Open Load Detection Scheme Comparison

OLD Scheme	Trigger Condition	Applicable Scenarios	Main Limitation
Active OLD	IOUTX < IOLD and sustained for > tOLD	Real-time detection during load driving	Risk of continuous false alarms in PWM mode when active freewheeling is enabled
Low-Current OLD (LOLD)	IOUTX < IOLD_LOW and sustained for > tOLD	Loads with small operating currents	Applies only to the low-side FET; must be used in conjunction with Active OLD
Neg-Current OLD	IOUTX > -IOLD_NEG	Prevents false alarms in synchronous rectification mode	Must be used in conjunction with Active OLD
Passive OLD	Abnormal output voltage/current (Hi-Z state)	Power-on diagnostics before output enable	Supported only by DRV8908/06/04-Q1

2 OLD Application Issues and Analysis

2.1 Problem 1: OLD False Alarms Under Active Freewheeling with PWM Control

2.1.1 Problem Description

When the DRV89xx-Q1 is configured in high-side switch (HSS) mode and active freewheeling is enabled (HBx_FW = 1b), the system will experience continuous OLD false alarms during the PWM control process. After the first correct detection of an OLD fault, even if the load has actually recovered to a normal connection, subsequent OLD detection false alarms persist and do not clear. This issue is independent of the load type and can be reproduced on both resistive and inductive loads.

2.1.2 Cause Analysis

The internal OLD comparator of the DRV89xx-Q1 exhibits a specific behavior: once the OLD comparator detects and reports an OLD fault for the first time (in either the HS or LS direction), all subsequent OLD detections will no longer execute the deglitch timer.

During normal operation, the Active OLD circuit continuously monitors the output current while the FET is turned on. When the current is below the threshold I_{OLD}, it must wait for the deglitch time t_{OLD} to expire before reporting a fault. This deglitching mechanism is designed to prevent false alarms during the current rising edge stage (such as the instant an inductive load starts). Once this deglitch protection is lost, at each PWM transition, the current at the moment the freewheeling FET turns on has not yet been established, and the OLD comparator immediately judges it as an open-load fault and reports it, forming continuous false alarms.

In addition, for resistive loads or inductive loads with small inductance values, the freewheeling current itself is very small and easily falls below the OLD trigger threshold, causing the chip to falsely judge the load as an open circuit; in this case, if active freewheeling needs to be enabled, Negative-Current OLD (Neg-Current OLD) must be used, with the chip's OLD decision threshold set to $-I_{OLD\_NEG}$, to avoid false triggering of OLD detection during the freewheeling process.

Note

This behavior affects only Active OLD and does not affect Passive OLD.

2.1.3 Application Recommendations

The table below summarizes the risk of continuous OLD false alarms under different configuration combinations:

Table 2-1. Summary of Continuous OLD False Alarm Scenarios in Active Freewheeling Mode

Control Method	Active Freewheeling	Risk of Repeated OLD False Alarms	Description
ON/OFF	Active switching	None	The deglitch timer is unaffected, preventing repeated false alarms of OLD faults
PWM	Enabled	Yes (High Risk)	Both HSS/LSS will continuously report OLD, and deglitch protection is lost
PWM	Disabled	None	No freewheeling FET switching, this issue is not triggered[DW1]

For purely resistive loads or inductive loads with small inductance values, active freewheeling can be left disabled to directly avoid the possibility of false alarms. For low-frequency loads, consider using the ON/OFF control mode, where freewheeling is implemented during high-side and low-side switching transitions; this process does not affect the deglitch time and will not cause continuous OLD false alarms.

For operating conditions that must be set to PWM control mode and have active freewheeling enabled, the Passive OLD detection method can be adopted to detect the load connection status before the output is enabled. Among common loads, currently only LED driving and PWM generators require PWM control; the PWM generator can use LOLD detection without encountering continuous false alarm issues, and the LED itself, as a light-emitting diode, has a very low parasitic inductance value on the nH order, which typically does not require freewheeling.

For continuous OLD false alarms occurring in already mass-produced systems, a software patch approach can be adopted; that is, after the first OLD fault is triggered, the MCU software layer masks subsequent OLD fault alarms for the same half-bridge, only recording and responding to the first alarm.

Note

If the tested load belongs to a safety-critical type, disabling OLD requires a full FMEA analysis, and complementary diagnostic measures must be added at the system level to meet functional safety requirements.

2.2 Problem 2: How to Maintain Output in the OLD State Through a Sleep-Wake Cycle

2.2.1 Problem Description

The DRV89xx-Q1 operates normally after initial power-on, with the output voltage stable at 11V. However, after going through a sleep-wake (nSLEEP low-to-high transition) cycle, even if OLD_OP = 1b is set (maintain high output when an OLD fault occurs), the output voltage remains low; subsequently, if CLR_FLT is executed again, the output will experience a brief high level but cannot be maintained, and the voltage drop rate between channels varies depending on the load.

In some application scenarios, even when the chip detects an open circuit, the output voltage needs to be maintained continuously. For example, the OLD channel output might supply power to both inside and outside the board simultaneously; when an off-board load experiences an open circuit, it is desirable for the inside-board supply voltage to be maintained.

2.2.2 Cause Analysis

The cause of the issue involves the interaction between sleep mode register resets and software control logic, analyzed at two levels:

1. Sleep mode causes all registers to reset: When the DRV89xx-Q1 enters sleep mode (nSLEEP low), the chip turns off the digital core for low power consumption, and the corresponding user configuration register settings are all lost, automatically restoring to default values upon wake-up. The key default values among them are: OLD_OP = 0b (turn off output and enter Hi-Z when an OLD fault occurs); HBx_OLD_DIS = 0b (OLD function is enabled by default), which means that after a sleep-wake cycle, OLD detection is turned on by default, and the voltage output is turned off by default once OLD is triggered.
2. The channel produces an output accompanying the CLR_FLT command but cannot maintain it: After the chip wakes up, the registers have returned to their default values, at which point it is configured to turn off the OLD output; there is a certain time delay from the CLR_FLT/enable output command until the chip detects the open circuit, during which the high-side channel enables the chip to output voltage normally until OLD triggers and the output enters Hi-Z. The voltage drop rate depends on the load, and it can discharge quickly if a direct path to ground exists.

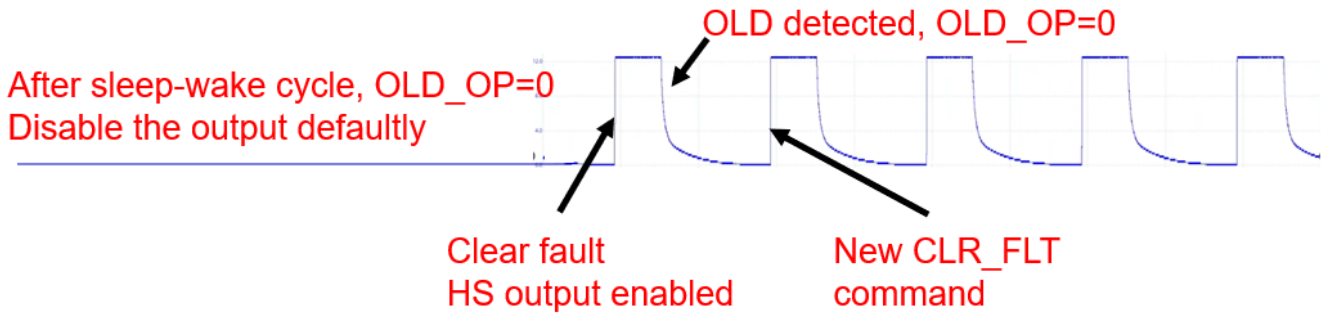

Figure 2-1. Schematic Diagram of OLD Output Transition Process

2.2.3 Waveform Verification

Verifying in combination with waveforms, under the load open-circuit condition, with nSLEEP set to a 5ms PWM and SPI sending commands every 10ms to set OLD_OP = 1b:

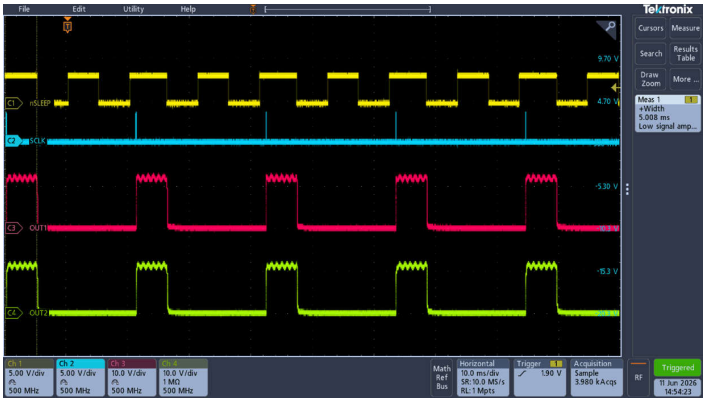

Figure 2-2. Channel Output Waveform Diagram Relative to nSLEEP Cycles and SPI Commands

According to the waveform, the starting point of the output voltage establishment in the OLD state aligns with the timing of the SPI command transmission, and the output duration is consistent with the nSLEEP high level, indicating that once sleep mode is entered, the OLD_OP setting returns to the default value and the channel output turns off.

2.2.4 Application Recommendations

The recommended software wake-up procedure is as follows:

1. Pull nSLEEP high → Wait for SPI Ready time (tWAKE ≈ 1ms);
2. Read the IC_STAT register and check the status of the NPOR bit;
3. If NPOR = 0b (a digital core reset occurred), immediately rewrite all necessary register configurations via SPI (including OLD_CTRL_1/2/3/4, OP_CTRL, FW_CTRL, etc.);
4. After register configuration is complete, write HBx_HS_EN / HBx_LS_EN to enable the output.

Note

The NPOR bit is a key indicator to judge whether a digital core reset has occurred. NPOR = 0b indicates that all registers have been reset to default values and must be fully reconfigured before enabling the output. For applications that frequently enter Sleep, a fixed execution path should be reserved in the software architecture for "register reconfiguration after wake-up", and it must not be assumed that the register state is identical to that before entering Sleep.

For scenarios with high requirements for diagnostic continuity, consider temporarily avoiding the use of Sleep mode and instead use a low-power standby configuration (maintain nSLEEP = H and turn off the output FETs solely via registers) to retain all register configurations.

2.3 Problem 3: How LOLD (Low-Current Open-Load Detection) is Triggered

2.3.1 Problem Description

In the application, it was found that when configuring Low-Current Active OLD (LOLD), even if the load is disconnected from the output terminal, the fault cannot be triggered (nFAULT is not pulled low, and the OLD bit in IC_STAT is not set). After changing to the standard Active OLD configuration, under the same load disconnection condition, the open-circuit state can be correctly detected and the fault reported.

The actual register settings are as follows: HB3_LS_EN = 1b (low-side FET enabled), HB3_OLD_DIS = 1b (OLD function disabled), HB3_LOLD_EN = 1b (LOLD enabled).

Test conditions: VM = 13.5V, a 3135Ω load is connected and then disconnected. Result: nFAULT remains high at all times, and the LOLD fault is not detected (FAIL).

2.3.2 Cause Analysis

The root cause of the problem lies in the control hierarchy relationship between the two register bits HBx_OLD_DIS and HBx_LOLD_EN:

HBx_OLD_DIS = 1b completely disables all OLD detection functions for that half-bridge, including Active OLD, Negative-Current OLD, and Low-Current LOLD. This bit is the master switch for OLD and has the highest priority.

The scenario for HBx_LOLD_EN = 1b is: under the premise that OLD is globally enabled (HBx_OLD_DIS = 0b), the OLD threshold of the low-side FET of that half-bridge is switched to the low-current mode (IOLD_LOW), while simultaneously disabling OLD detection for the high-side FET to prevent the high-side FET from generating false alarms due to the excessively low IOLD_LOW threshold.

Therefore, when HBx_OLD_DIS = 1b, regardless of the value of HBx_LOLD_EN, the entire OLD function is turned off and LOLD cannot operate.

The complete OLD/LOLD control logic is shown in the table below:

Table 2-2. HBx_OLD_DIS / HBx_LOLD_EN Control Logic

HBx_OLD_DIS	HBx_LOLD_EN	LS FET OLD	HS FET OLD	OLD Threshold	Fault Reporting
0b	0b	Enabled	Enabled	IOLD (Active OLD)	Enabled
0b	1b	Enabled	Disabled	IOLD_LOW (LOLD)	Enabled
1b	/	Disabled	Disabled	/	Disabled[DW1]

2.3.3 Waveform Verification

The following verifies the corresponding results of register configurations through four sets of test waveforms; the tests are all conducted on the OUT3 channel, where CH1: OUT3 output voltage, CH2: nFAULT signal, and CH4: channel current.

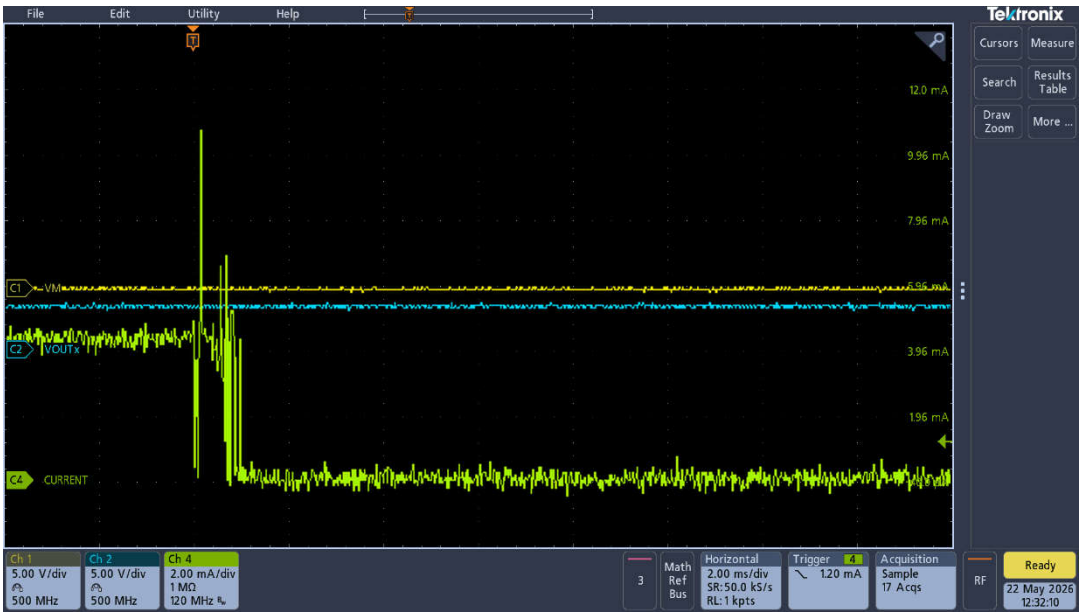

Figure 2-3. Test 1: HB3_OLD_DIS = 1b, HB3_LOLD_EN = 1b, 3135Ω load

As shown in the waveform in Figure 2-3, the load current is approximately 4.3mA, which is higher than the maximum range of the LOLD trigger threshold (2mA), so LOLD is not triggered when the load is normally connected; after the load is disconnected, nFAULT still remains high at all times, OUT3 continues to output, and no fault is reported. The OLD function is completely turned off by HB3_OLD_DIS = 1b, rendering the LOLD setting invalid.

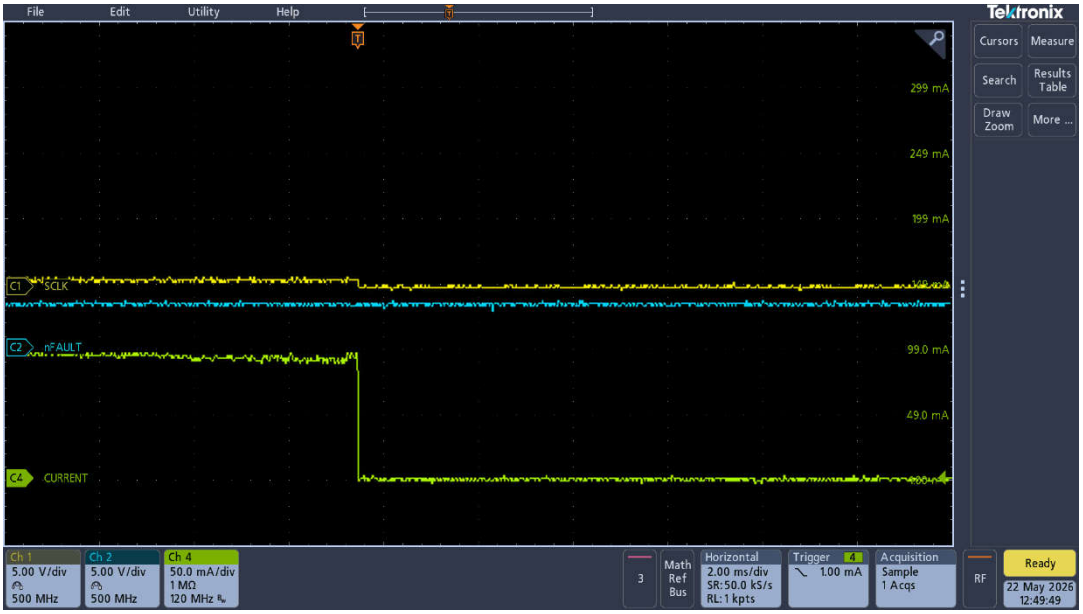

Figure 2-4. Test 1: HB3_OLD_DIS = 1b, HB3_LOLD_EN = 1b, 135Ω load

Reducing the load resistance to 135Ω (increasing the current), nFAULT still shows no response. At this time, neither OLD nor LOLD can be triggered.

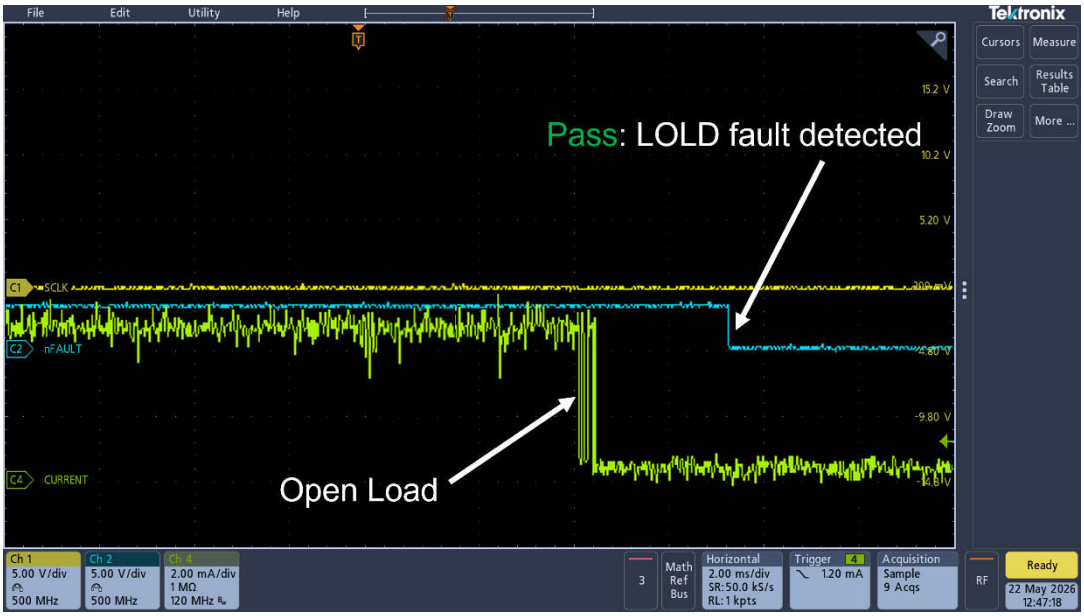

Figure 2-5. Test 3: HB3_OLD_DIS = 0b, HB3_LOLD_EN = 1b, 3135Ω load

As shown in the waveform in Figure 2-5, under the correct register configuration, OLD or LOLD is not triggered when the load current is 4.3mA; at this time, the current is below the I_{OLD} threshold (typical value 9mA), indicating that Active OLD is not taking effect; after the load is disconnected, nFAULT is pulled low, and the OLD bit in the chip's IC_STAT is set to 1, successfully reporting the open-circuit fault, which proves that the LOLD function is operating normally and rules out the influence of Active OLD.

2.3.4 Application Recommendations

The correct LOLD configuration steps are as follows: ① set HBx_OLD_DIS to 0b (enable global OLD function); ② set HBx_LOLD_EN to 1b (switch to low-current OLD mode); ③ enable output; ④ monitor the nFAULT signal and the OLD bit in IC_STAT.

Note

In LOLD mode, the RDS(on) of the LS FET increases by approximately 11-fold (typical value around 7.5Ω), and the overcurrent protection (OCP) threshold decreases synchronously to approximately 1/11 of its original value (minimum value around 120mA). When using LOLD, it is necessary to evaluate whether heat dissipation and protection margins meet design requirements; it is recommended to use LOLD only in small-current scenarios, such as for PWM control signal generation.

3 Conclusion

This paper introduces some extended application scenarios of the DRV89xx-Q1 beyond motor driving, and systematically analyzes three types of typical OLD detection problems encountered in extended applications, with the core conclusions as follows:

Problem 1 (Active OLD continuous false alarms): It is necessary to determine the OLD type based on the load type and current size, paying attention to OLD false triggering caused on the freewheeling tube due to an excessively small freewheeling current. Regarding the continuous false alarm issue, most load types do not need to satisfy both the PWM control mode and active freewheeling simultaneously, which can be directly avoided during mode selection; if such a special operating condition exists, it can be handled via software by accepting the first reported alarm and masking subsequent OLD faults, or by using Passive OLD detection.

Problem 2 (Periodic output drop): Sleep mode causes registers to reset to default values (OLD is enabled by default and turns off output upon fault), causing the output before and after the CLR_FLT (including enable output) command to rise in a pulse-like manner and then drop. The solution is to detect the reset event via the NPOR bit after wake-up and rewrite all necessary registers before enabling the output.

Problem 3 (LOLD cannot be triggered): HBx_OLD_DIS = 1b completely disables all OLD functions including LOLD, and the functionality of HBx_LOLD_EN depends on the premise of HBx_OLD_DIS = 0b. The correct configuration is HBx_OLD_DIS = 0b and HBx_LOLD_EN = 1b, and LOLD can only be triggered via the low-side FET.

These three types of problems are all caused by unclear application boundaries and device behaviors when the DRV89xx-Q1 is used in new application scenarios beyond motor driving, rather than device design defects. Fully understanding the control hierarchy of the OLD function, the register reset behavior of Sleep mode, and the prerequisites for using each OLD sub-function in the early stage of system design can effectively avoid the reliability risks caused by the aforementioned problems during the mass production stage.

4 References

1. DRV8908-Q1 Datasheet (SLVSEC9C), Texas Instruments, Revised February 2020.
2. DRV8908-Q1 Functional Safety, FIT Rate, Failure Mode Distribution and Pin FMA
3. Open Load Detection in Integrated Drivers (Rev. C)

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