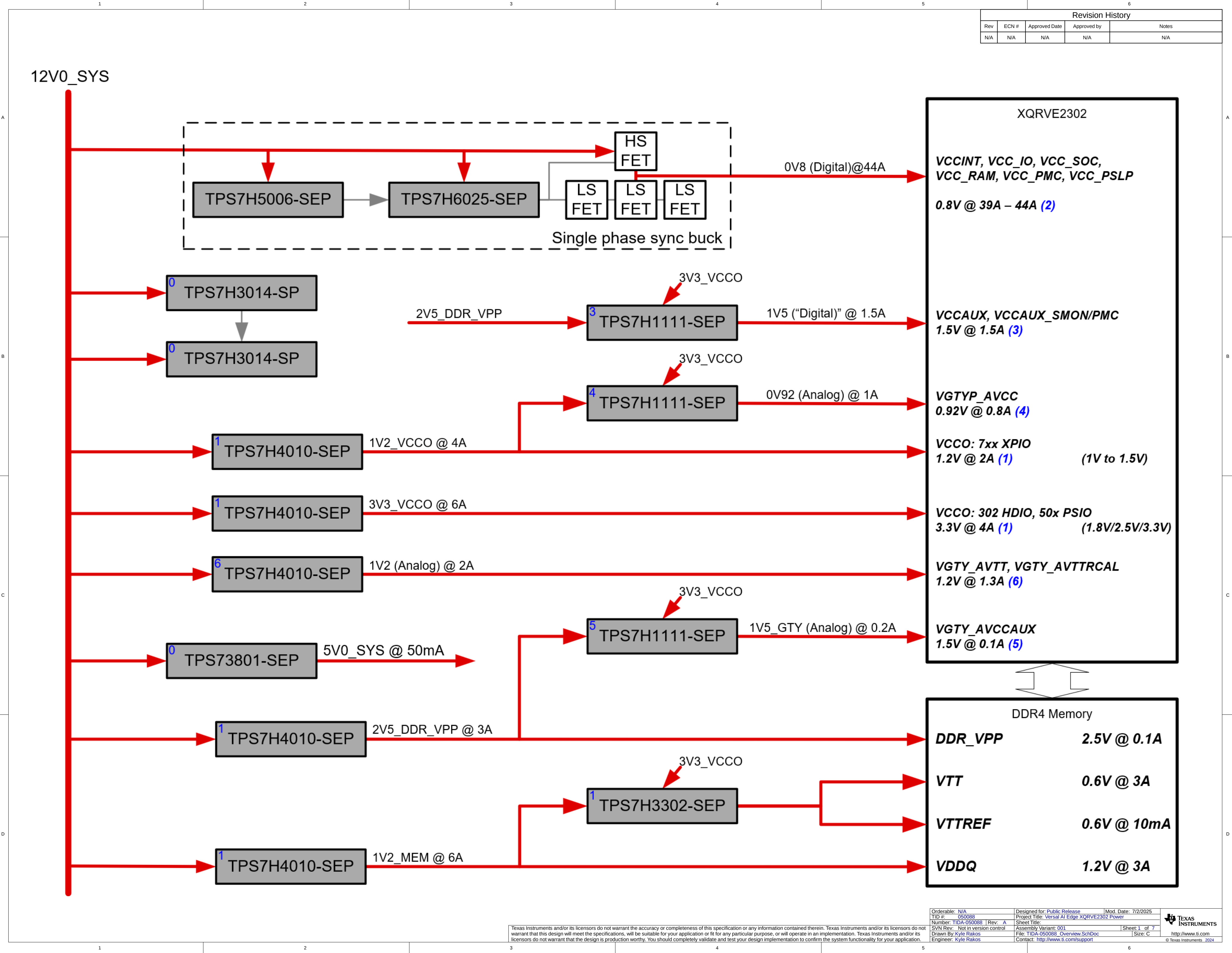
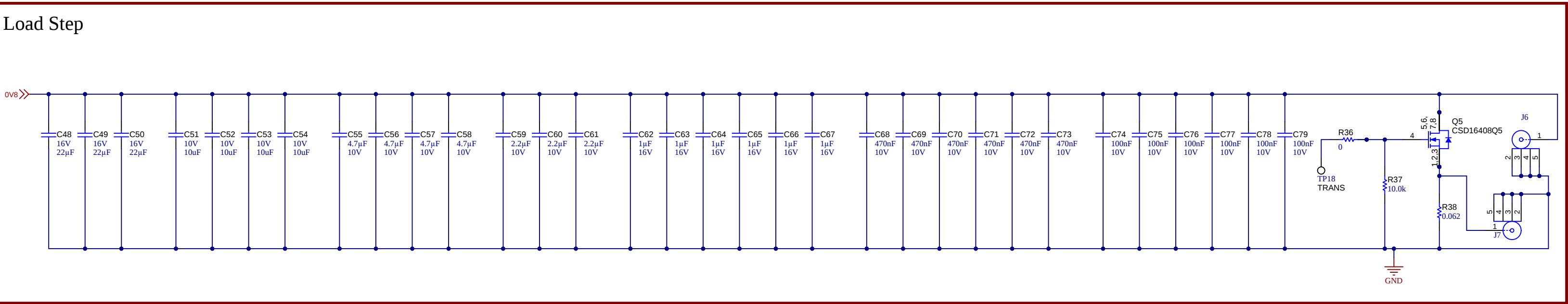
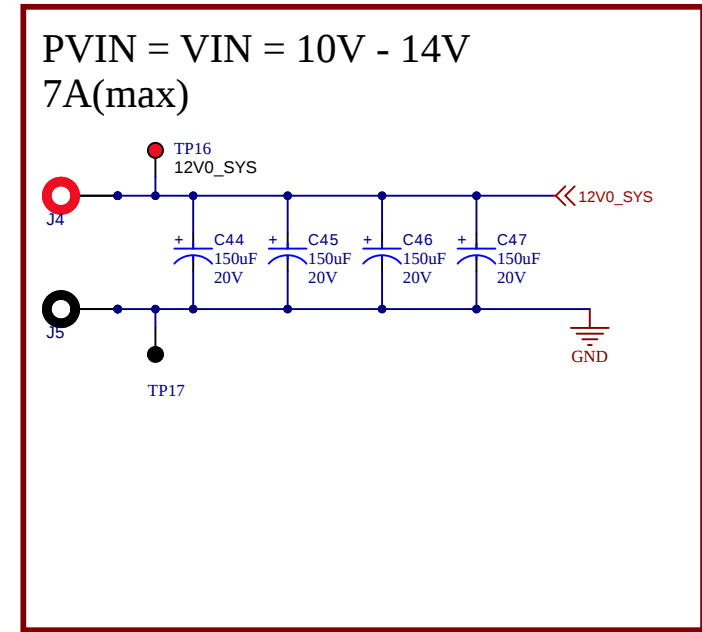
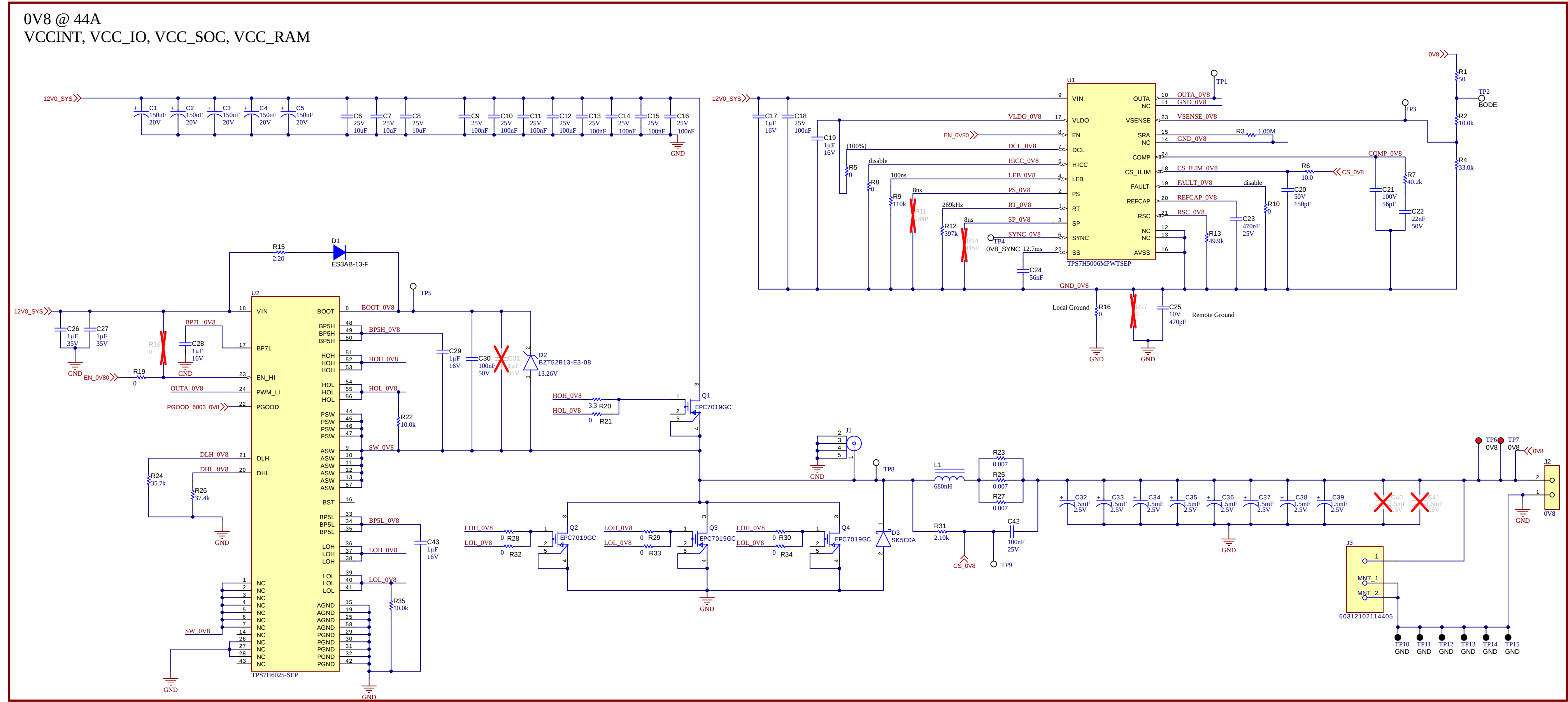




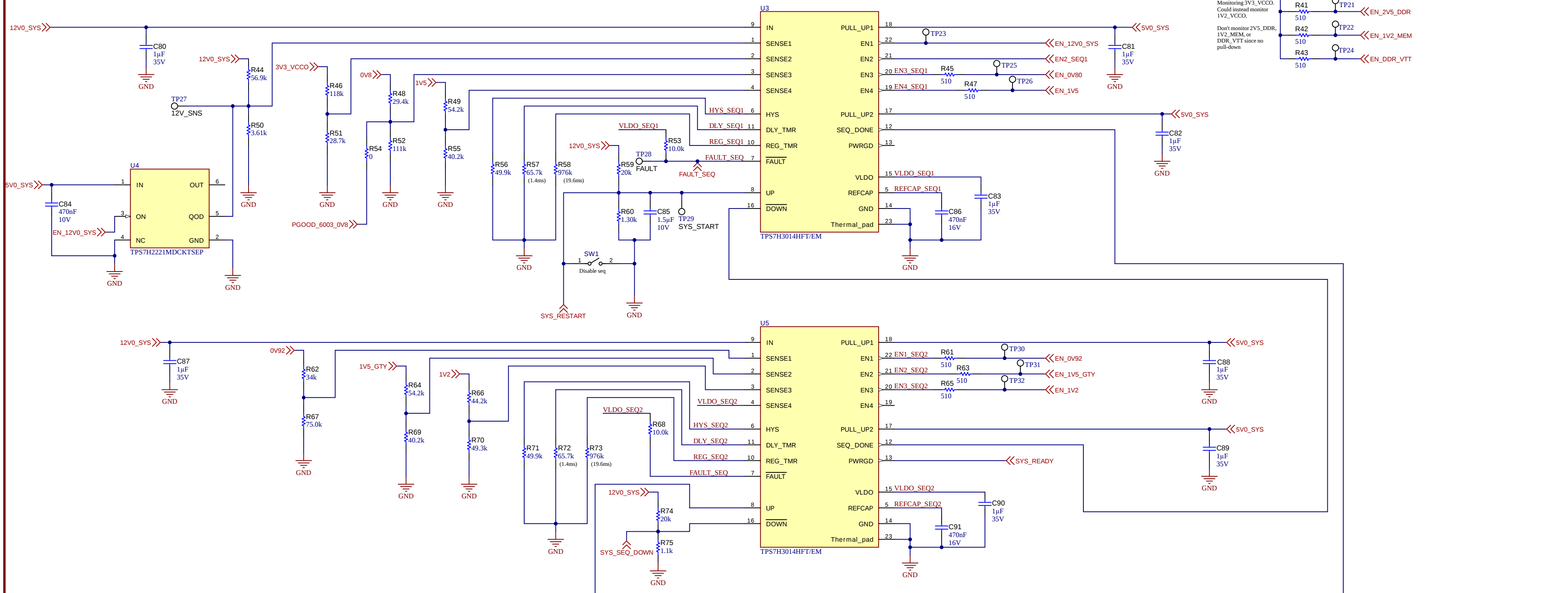
Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

Core Rail

0V8 @ 44A
VCCINT, VCC_IO, VCC_SOC, VCC_RAM

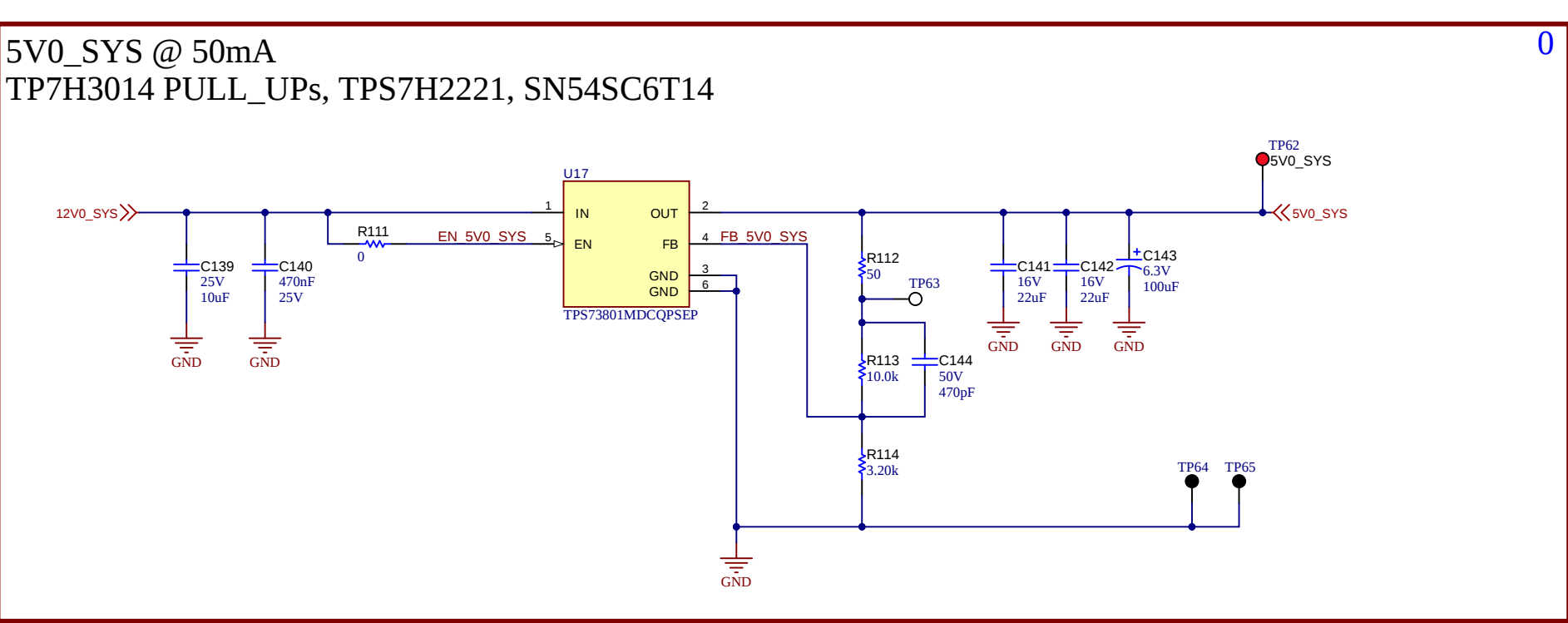
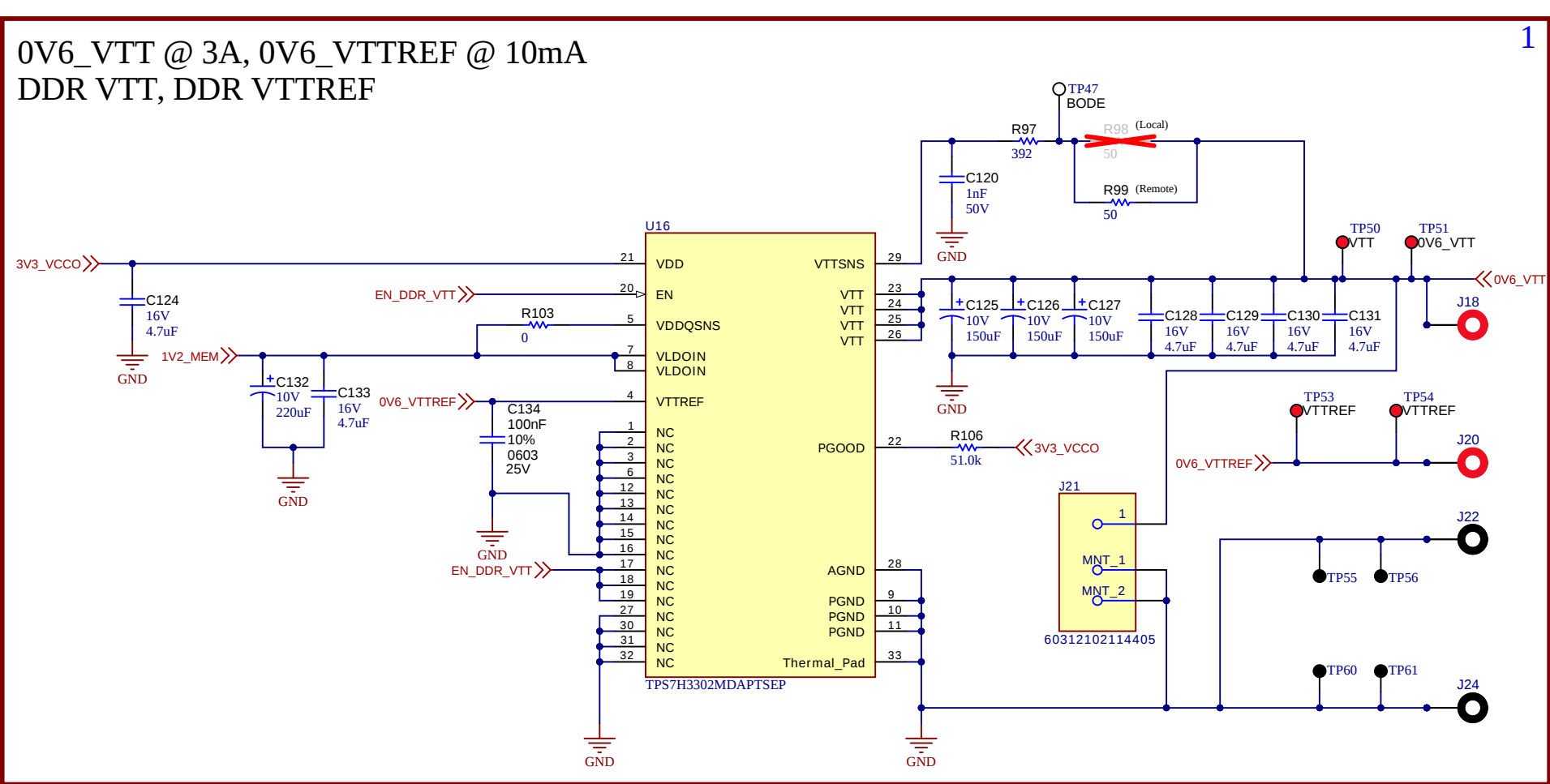
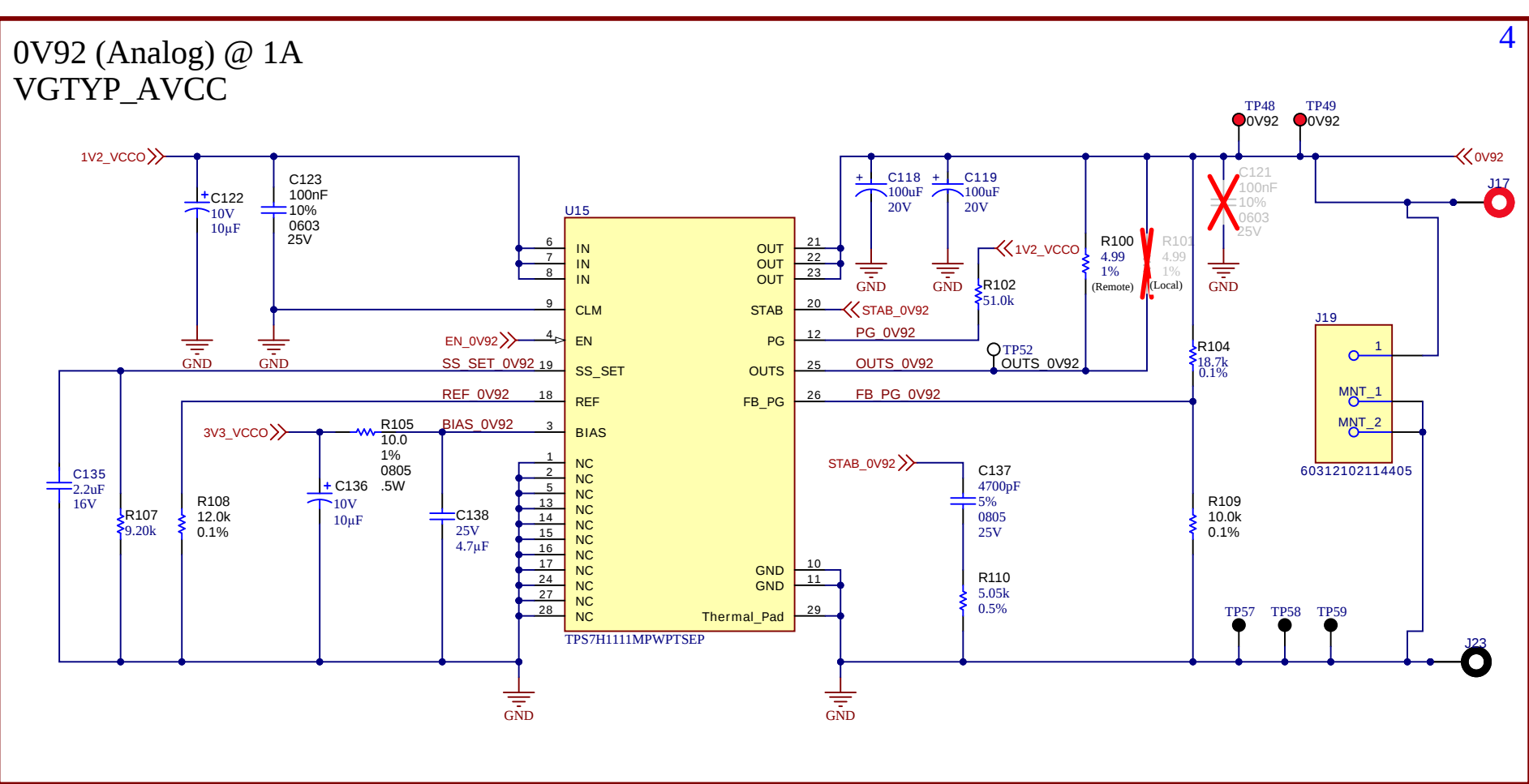
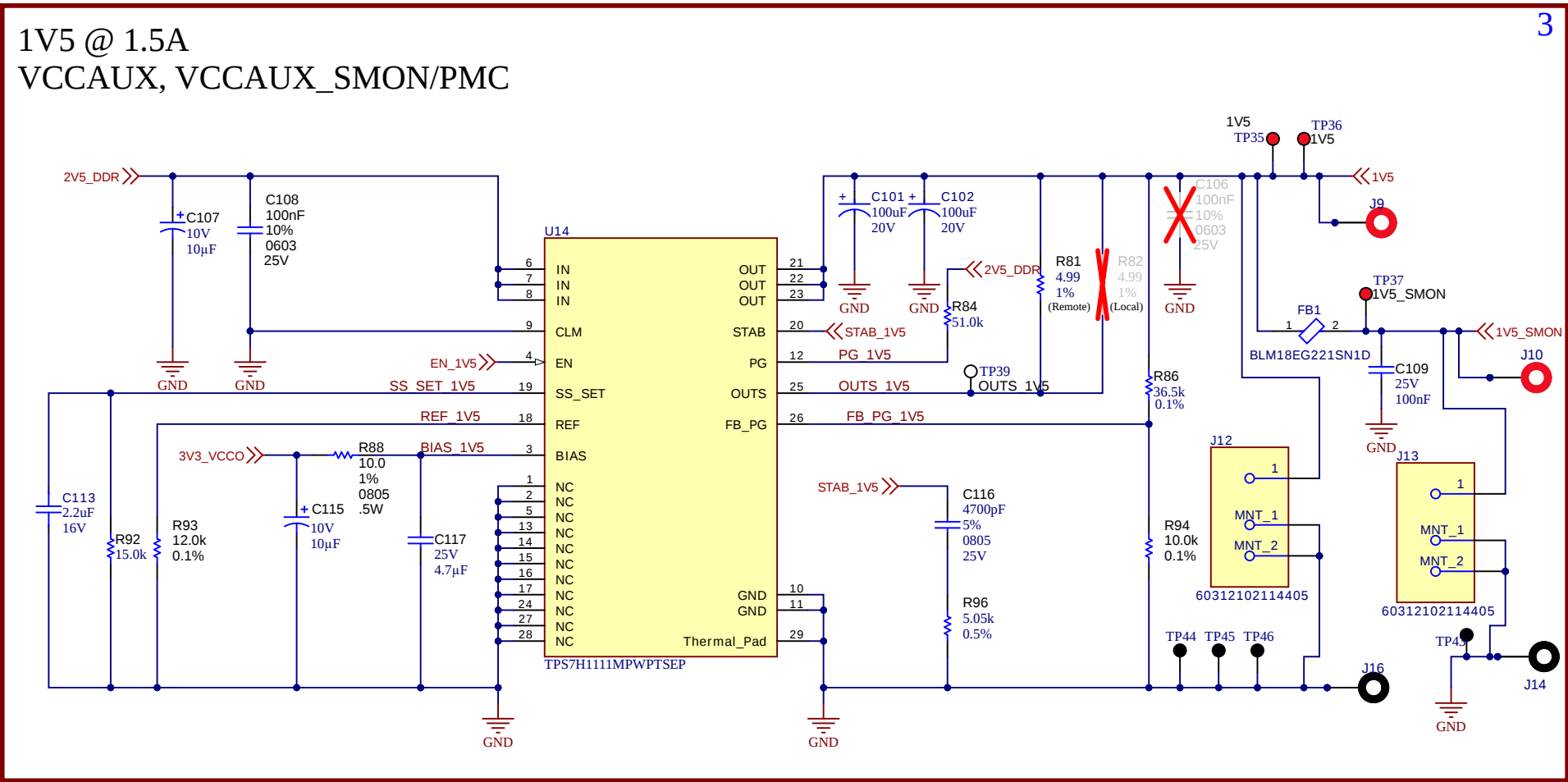
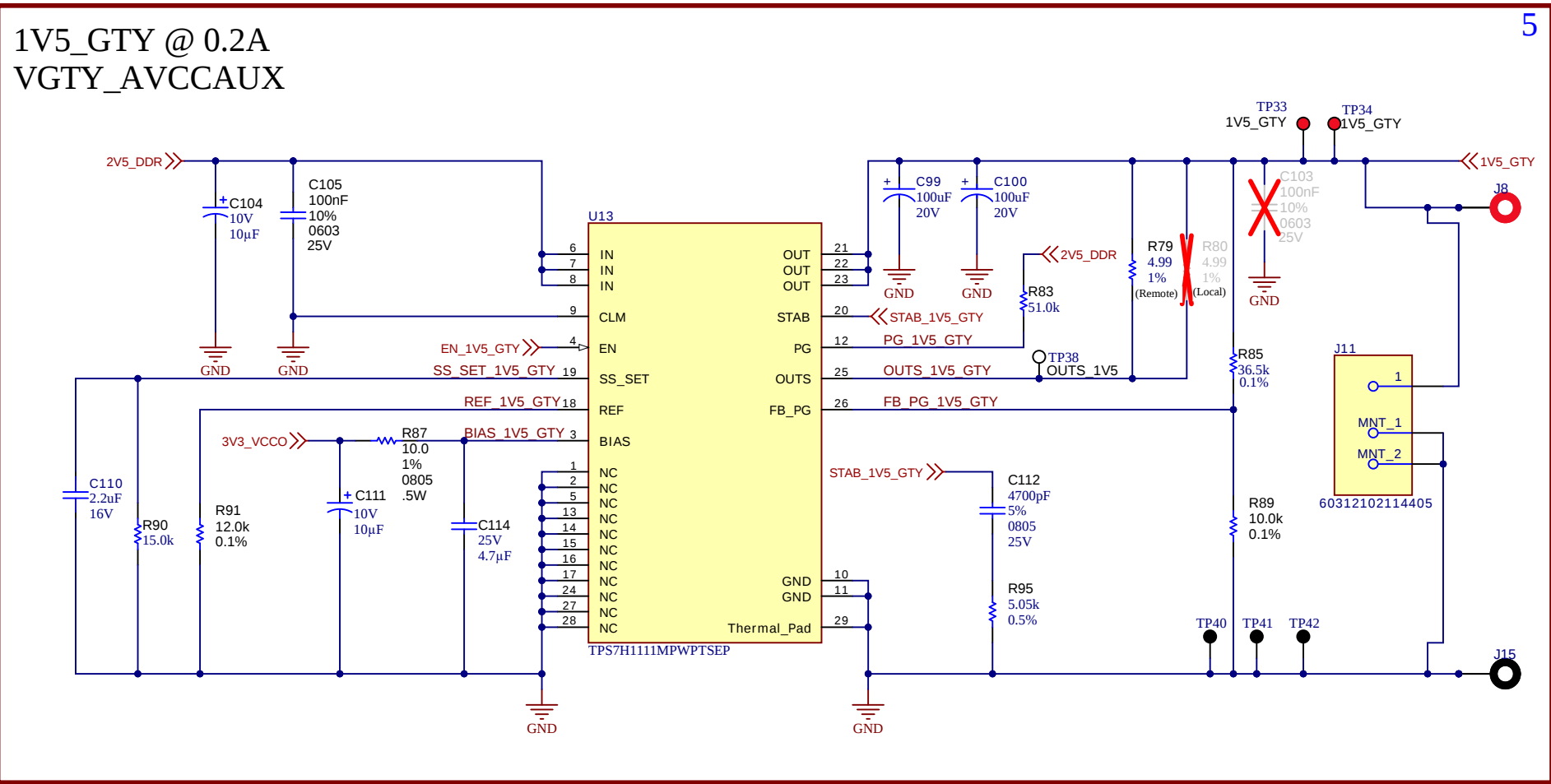


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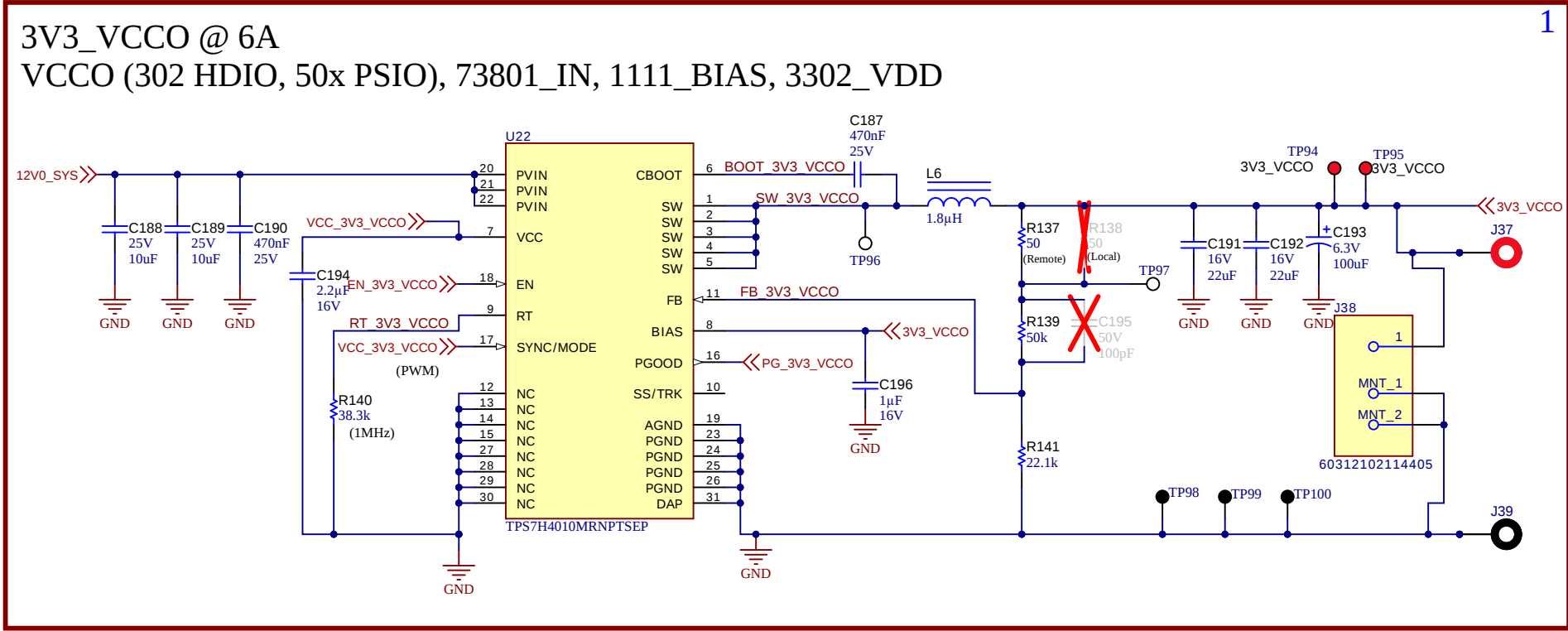
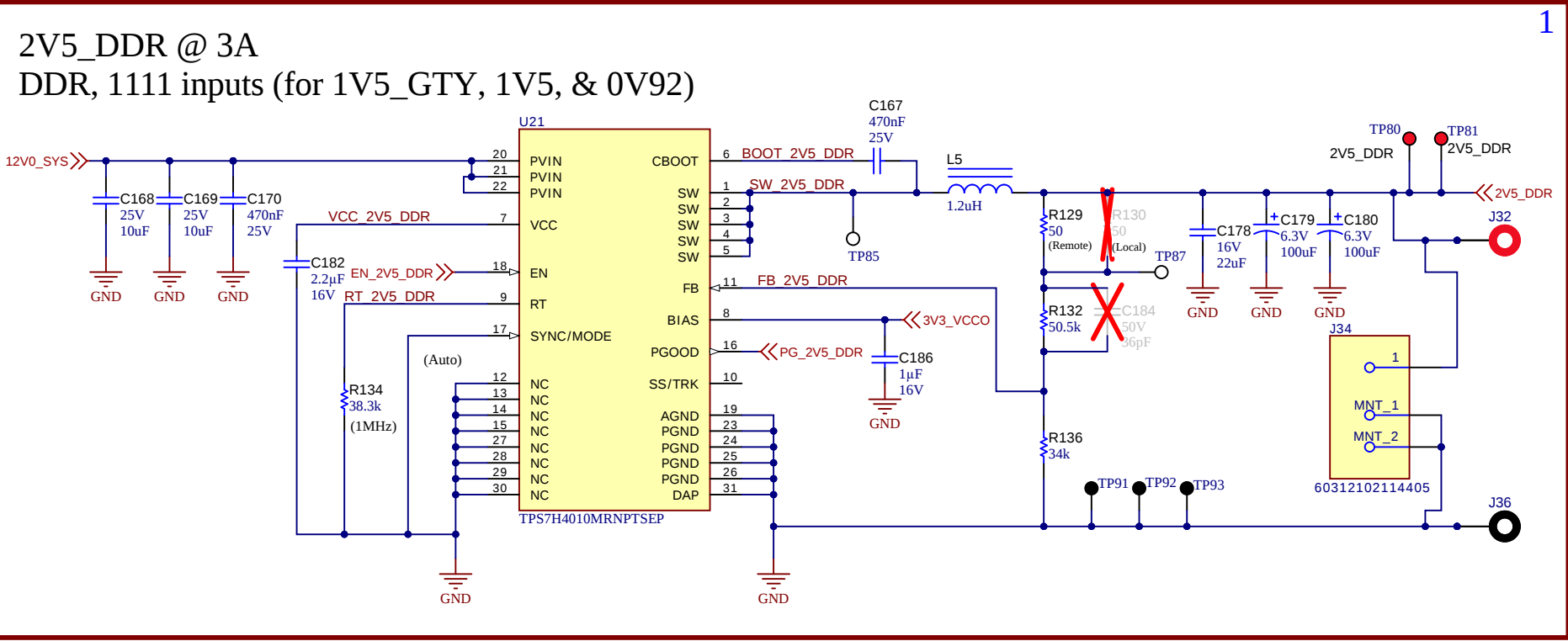
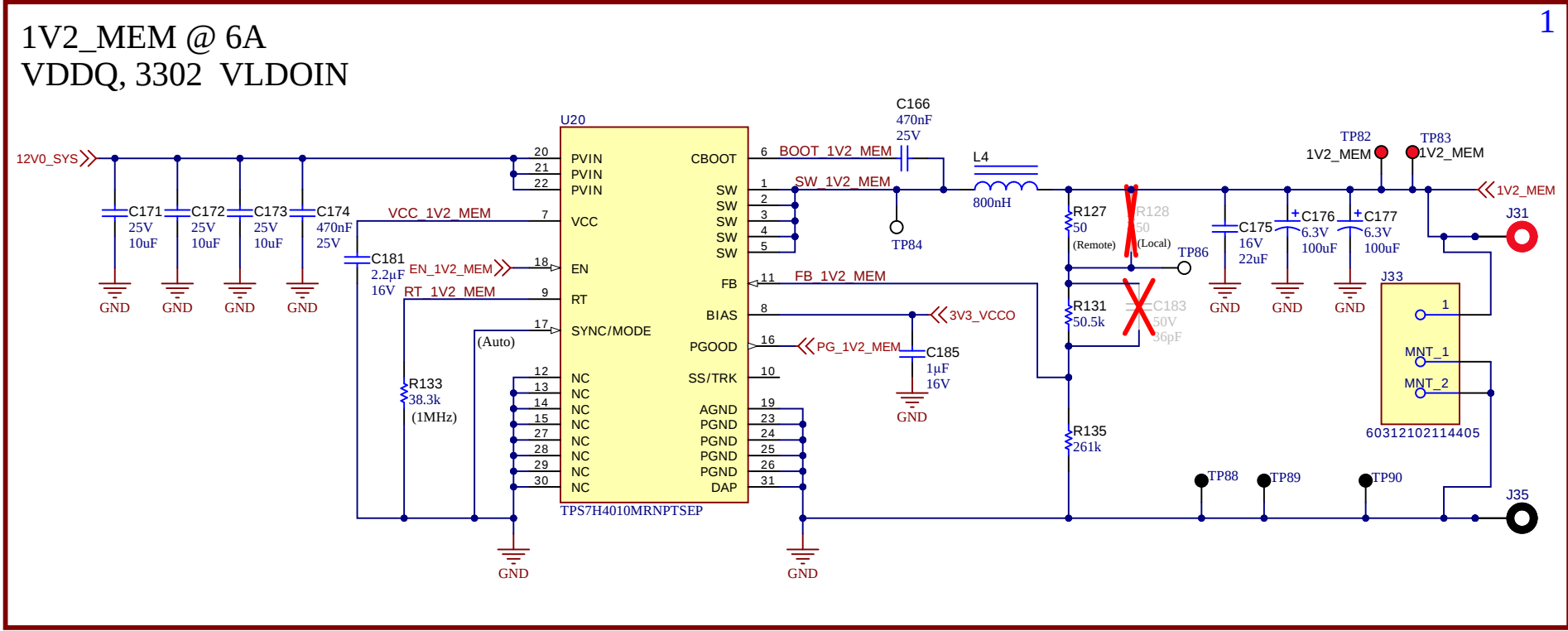
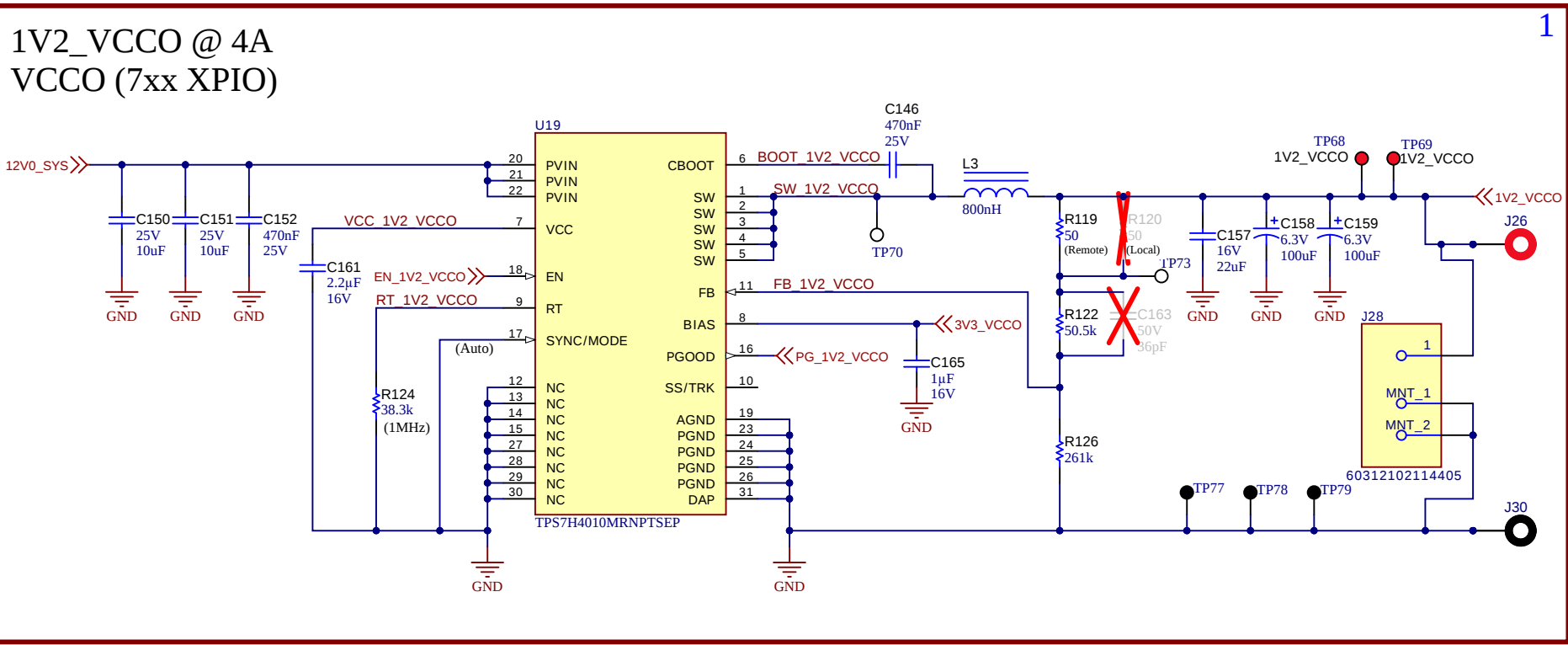
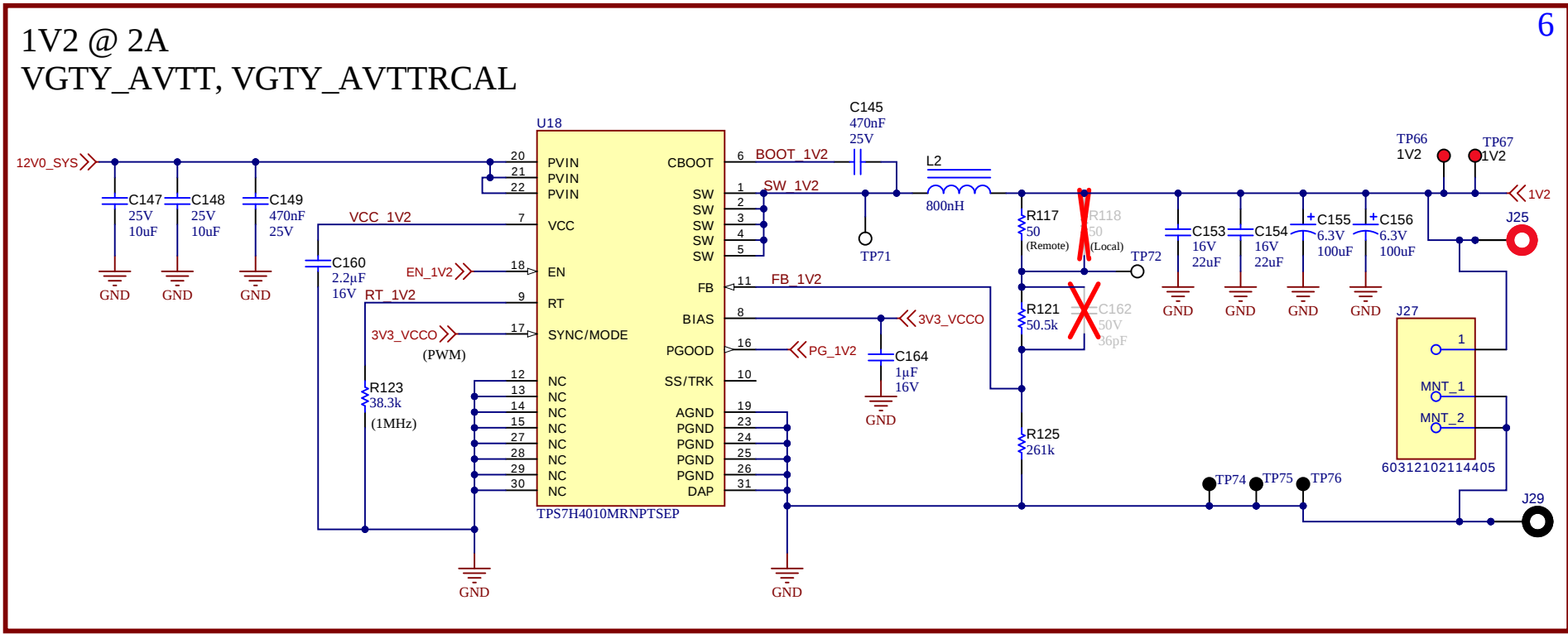
[illegible]

0.3ohms, ~10ms discharge, 2.3A peak

LDO Rails



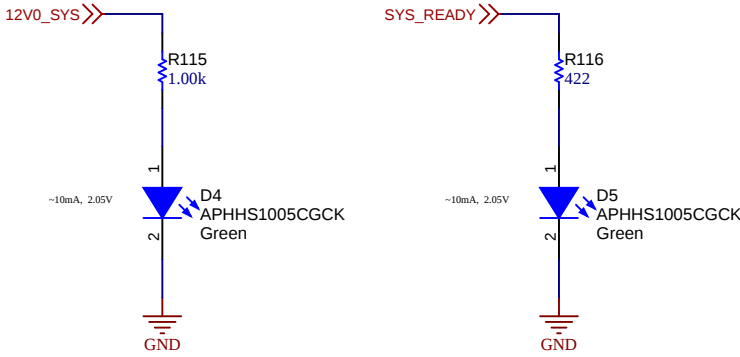
Buck Rails



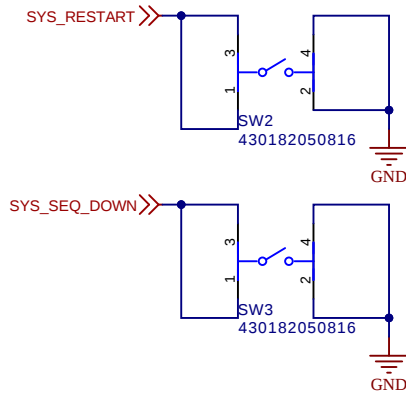
Aux (Enable, LEDs, Monitoring)

(Not required for Versal Edge solution, used for debugging)

LED Monitors



Push-Buttons



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