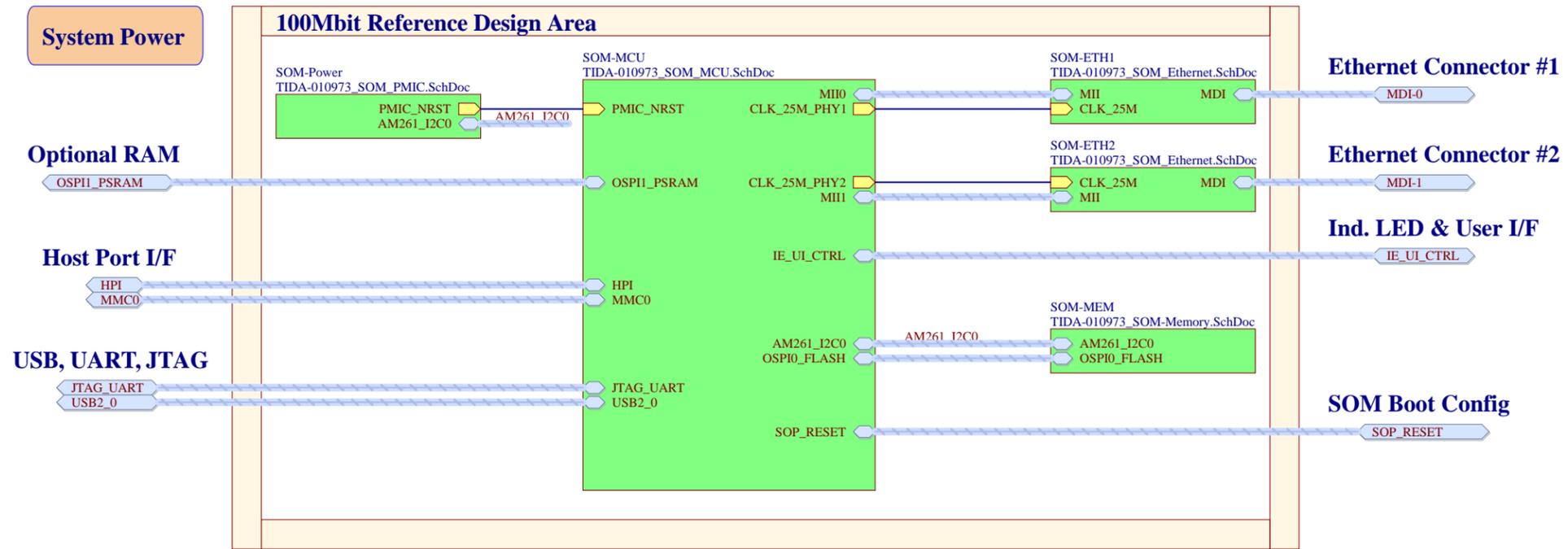


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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 2/13/2026
TID #: TIDA-010973	Project Title: 100Mbit IE Comm Module	
Number: TIDA-010973 Rev: E2	Sheet Title:	
SVN Rev: 16154 [Locally Modified]	Assembly Variant: 001	Sheet: 1 of 15
Drawn By:	File: TIDA-010973_BaseBoard.SchDoc	Size: B
Engineer: Thomas Mauer	Contact: http://www.ti.com/support	

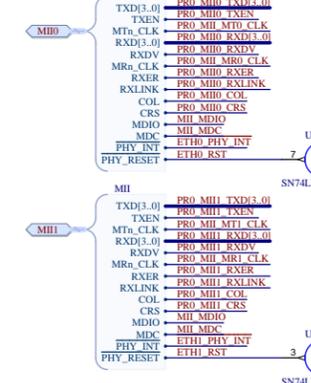


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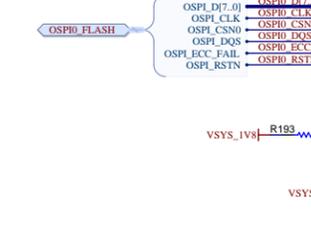
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Number: TIDA-010973	Rev: E2	Sheet: 2 of 15
SVN Rev: 16154	Assembly Variant: 001	Size: B
Drawn By:	File: TIDA-010973_SOM_BlockDiagram.SchDoc	Contact: http://www.ti.com/support
Engineer: Thomas Mauer		



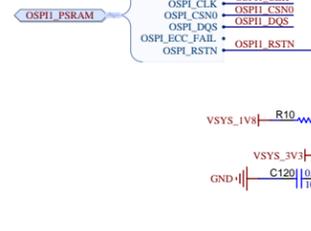
Industrial Ethernet



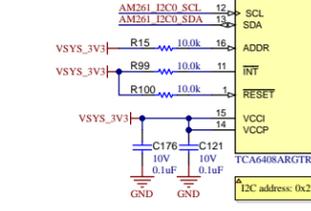
OSPI FLASH



OSPI PSRAM



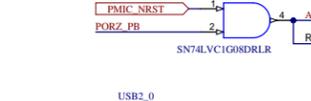
I2C IO Expanders



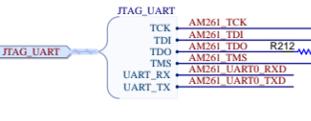
AM261x SOP3:0



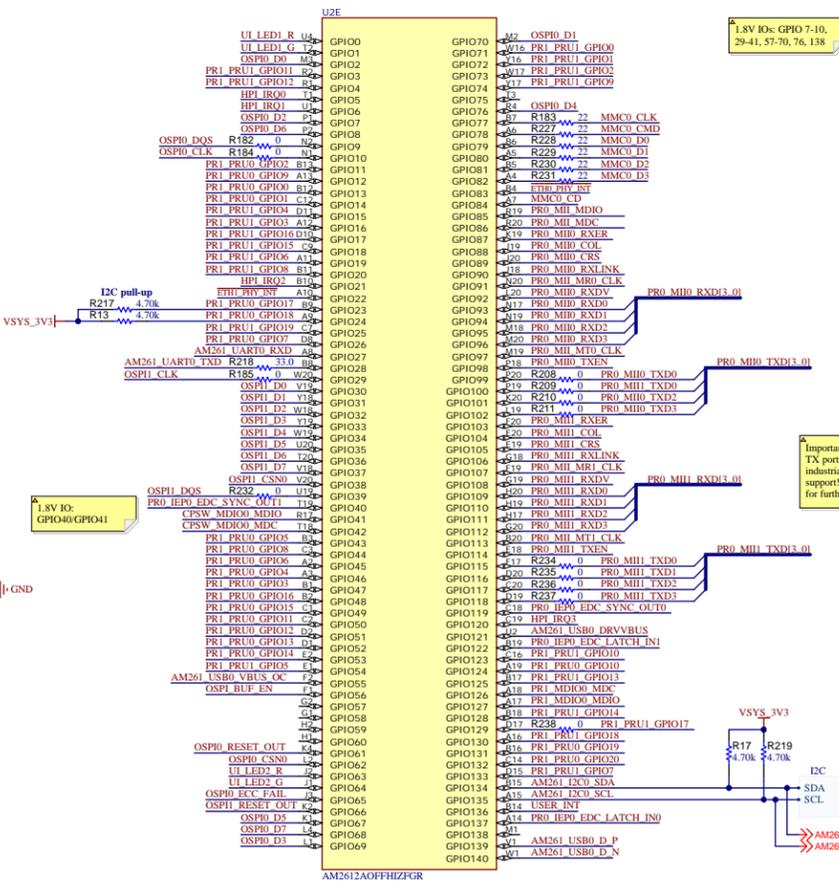
POR Generation



AM261 JTAG



Length match the following buses
MII_RX, MII_TX, OSPI Flash, OSPI PSRAM, SD Card



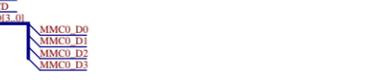
1.8V IOs: GPIO 7-10, 29-41, 57-70, 76, 138

Important note: ICSS MII TX port are swapped for industrial Ethernet firmware support! See TI design guide for further details.

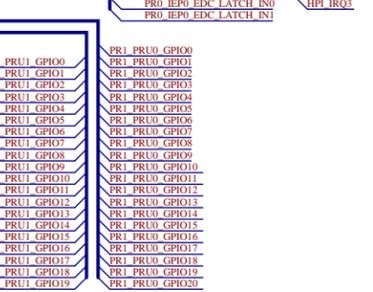
AM261 I2CO SDA, AM261 I2CO_SCL

PHY: 3.3V level
AM261x: 1.8V level

MMC



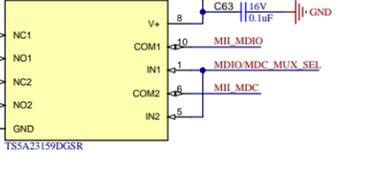
HPI



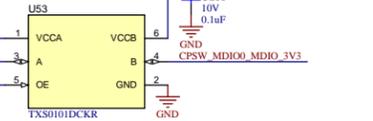
IE_UI_CTRL



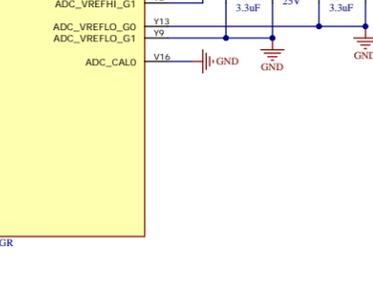
MDIO ICSS0/CPSW MUX



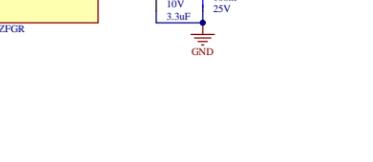
TS5A23159DQSR



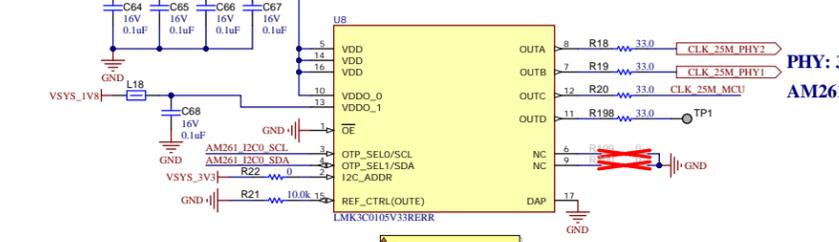
ADC



DAC



Clock Buffer with BAW oscillator



A

B

C

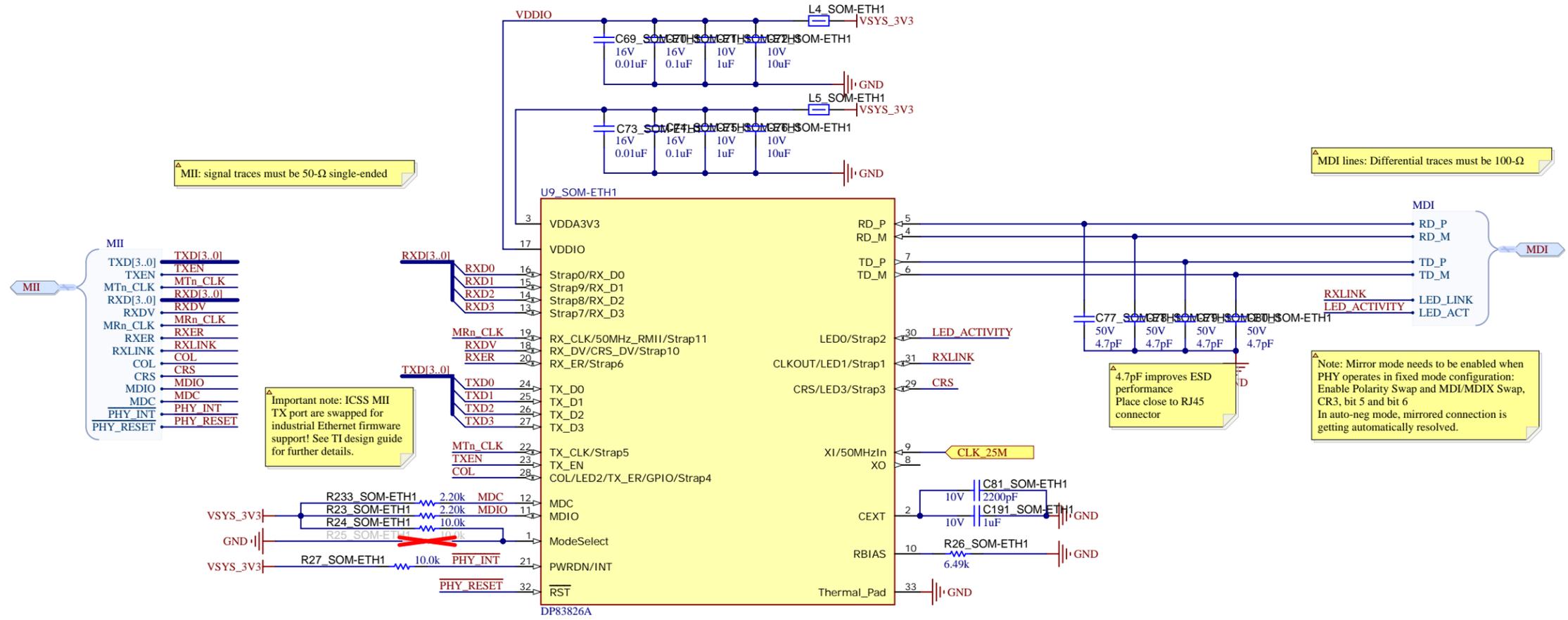
D

A

B

C

D



MII: signal traces must be 50-Ω single-ended

MDI lines: Differential traces must be 100-Ω

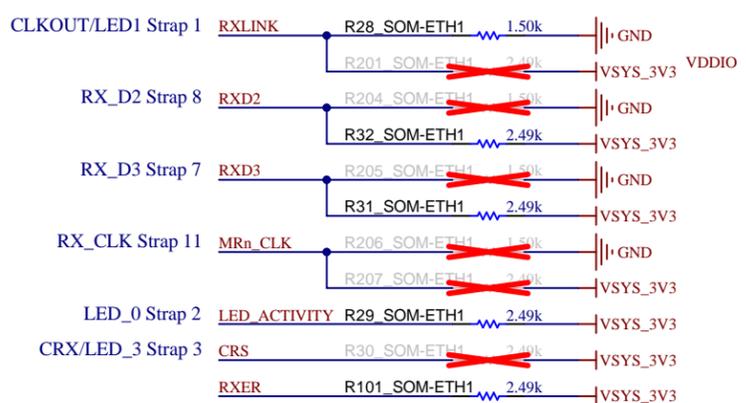
- MII
- TXD[3..0] TXD[3..0]
 - TXEN TXEN
 - MTn_CLK MTn_CLK
 - RXD[3..0] RXD[3..0]
 - RXDV RXDV
 - MRn_CLK MRn_CLK
 - RXER RXER
 - RXLINK RXLINK
 - COL COL
 - CRS CRS
 - MDC MDC
 - MDIO MDIO
 - PHY_INT PHY_INT
 - PHY_RESET PHY_RESET

Important note: ICSS MII TX port are swapped for industrial Ethernet firmware support! See TI design guide for further details.

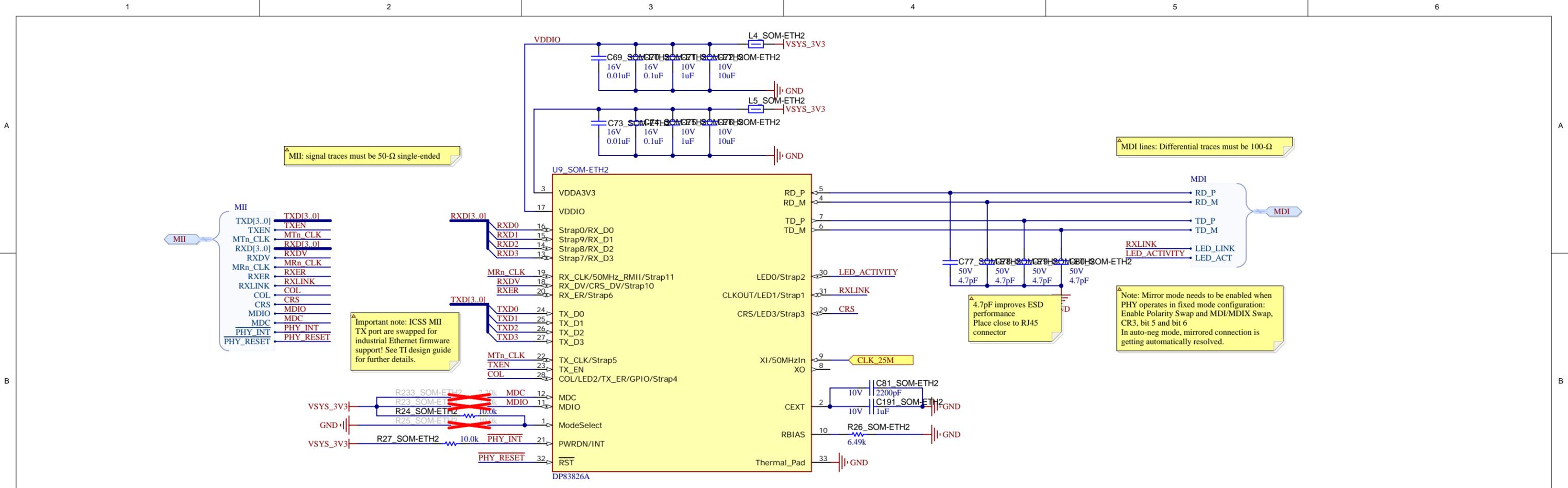
4.7pF improves ESD performance Place close to RJ45 connector

Note: Mirror mode needs to be enabled when PHY operates in fixed mode configuration: Enable Polarity Swap and MDI/MDIX Swap, CR3, bit 5 and bit 6 In auto-neg mode, mirrored connection is getting automatically resolved.

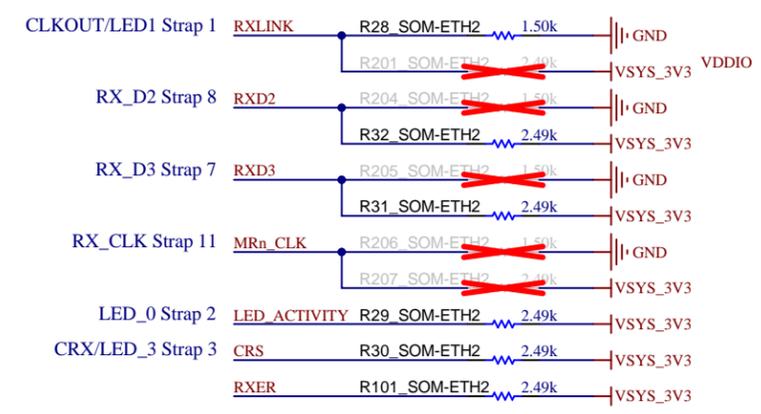
Bootstrap



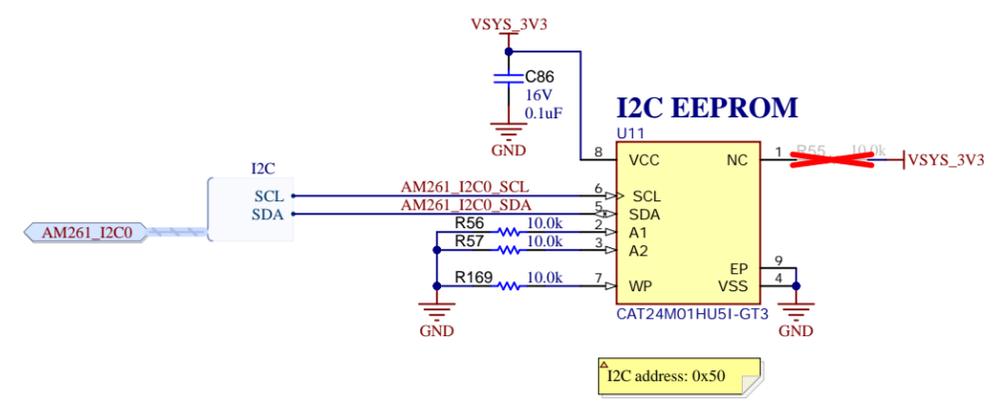
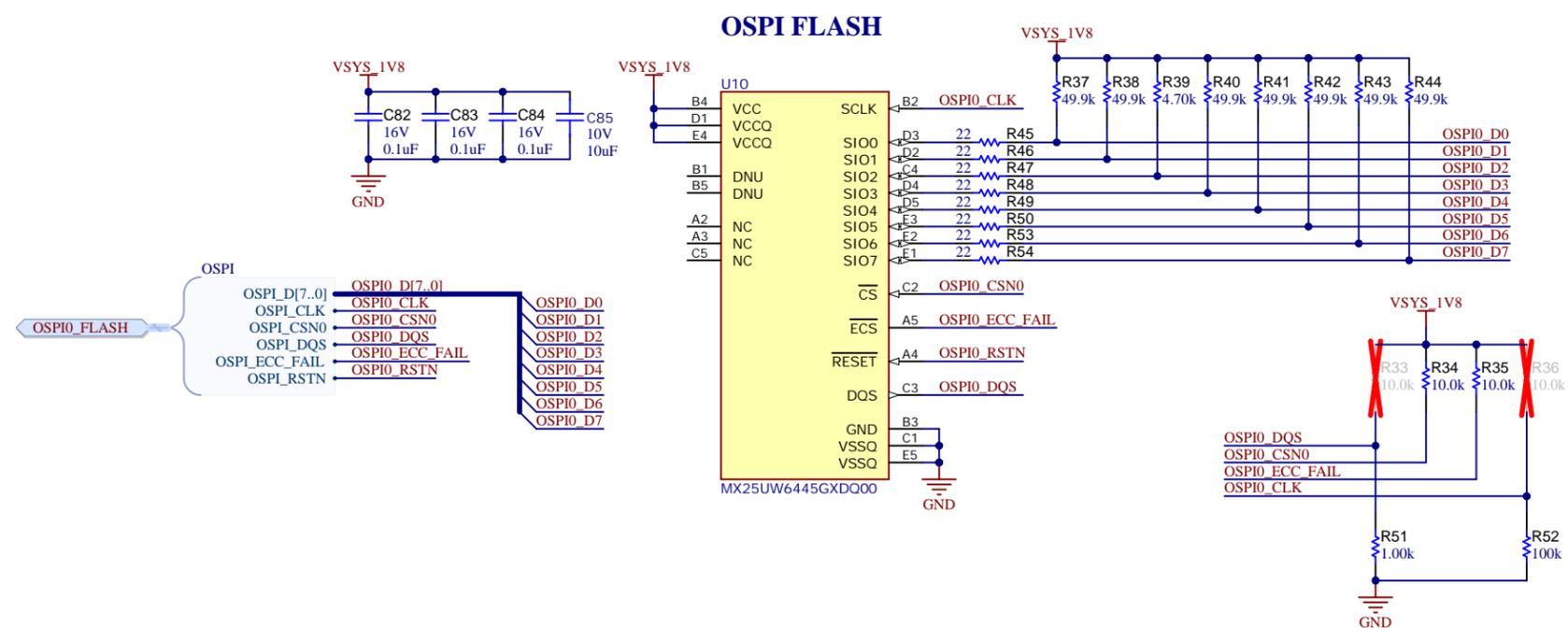
Bootstrap:
 PHY1 ID: 1
 PHY2 ID: 3
 Enhanced Mode
 Odd nibble detection disabled
 FLD enabled
 FLD: RX_ER and Signal Detection
 DISABLE_CLKOUT
 Bootstrap resistors can be minimized pending



Bootstrap

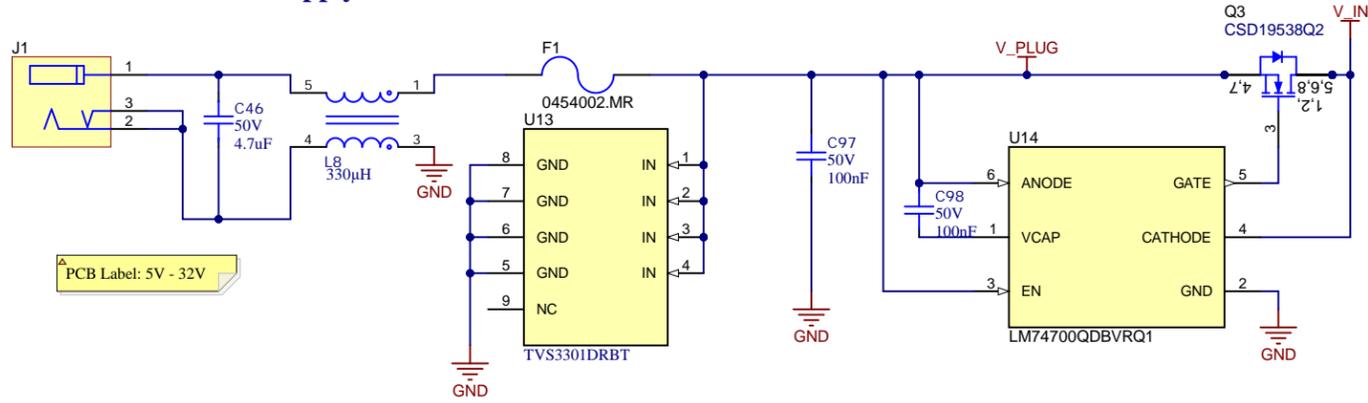


Bootstrap:
 PHY1 ID: 1
 PHY2 ID: 3
 Enhanced Mode
 Odd nibble detection disabled
 FLD enabled
 FLD: RX_ER and Signal Detection
 DISABLE_CLKOUT
 Bootstrap resistors can be minimized pending



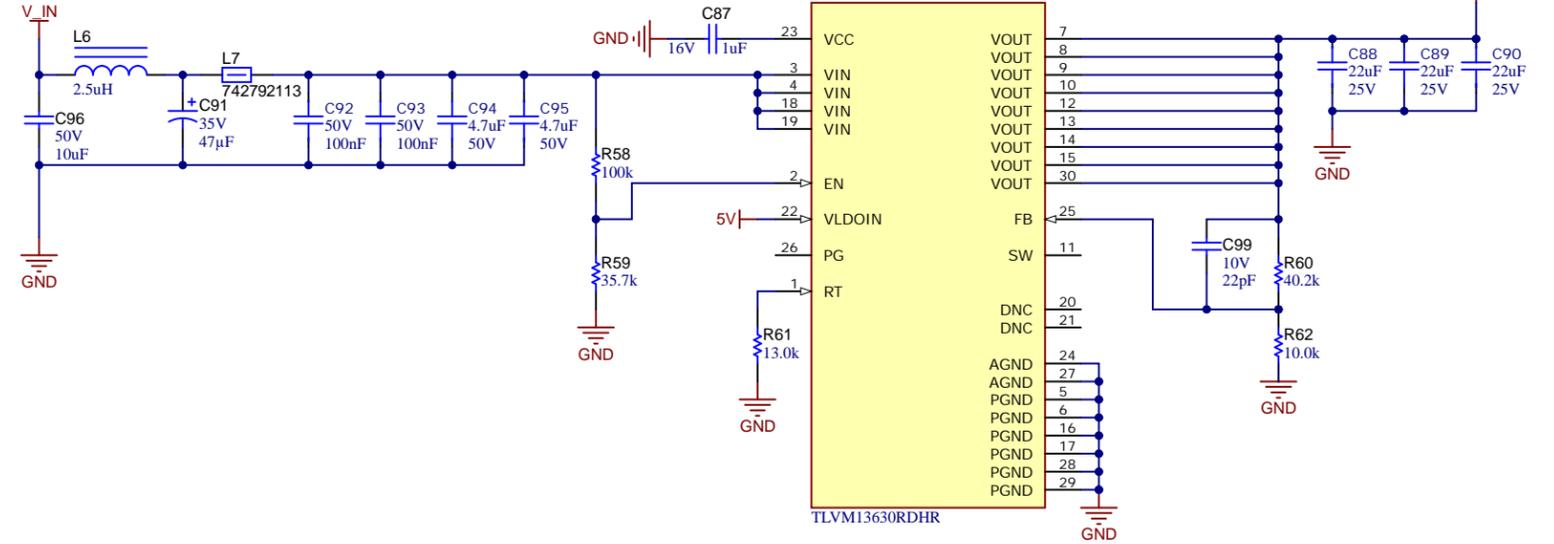
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Main Power Supply

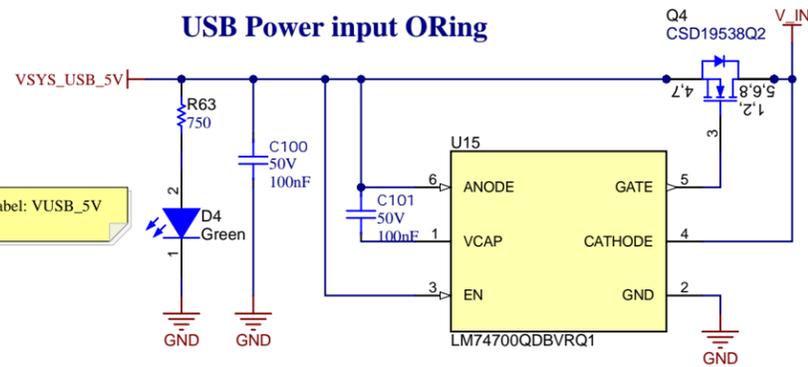


PCB Label: 5V - 32V

V_IN to 5V

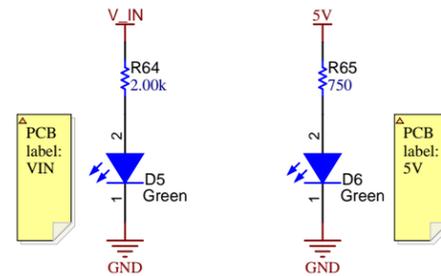


USB Power input ORing

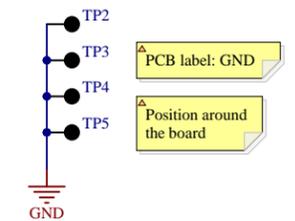


PCB label: VUSB_5V

Power Good LEDs



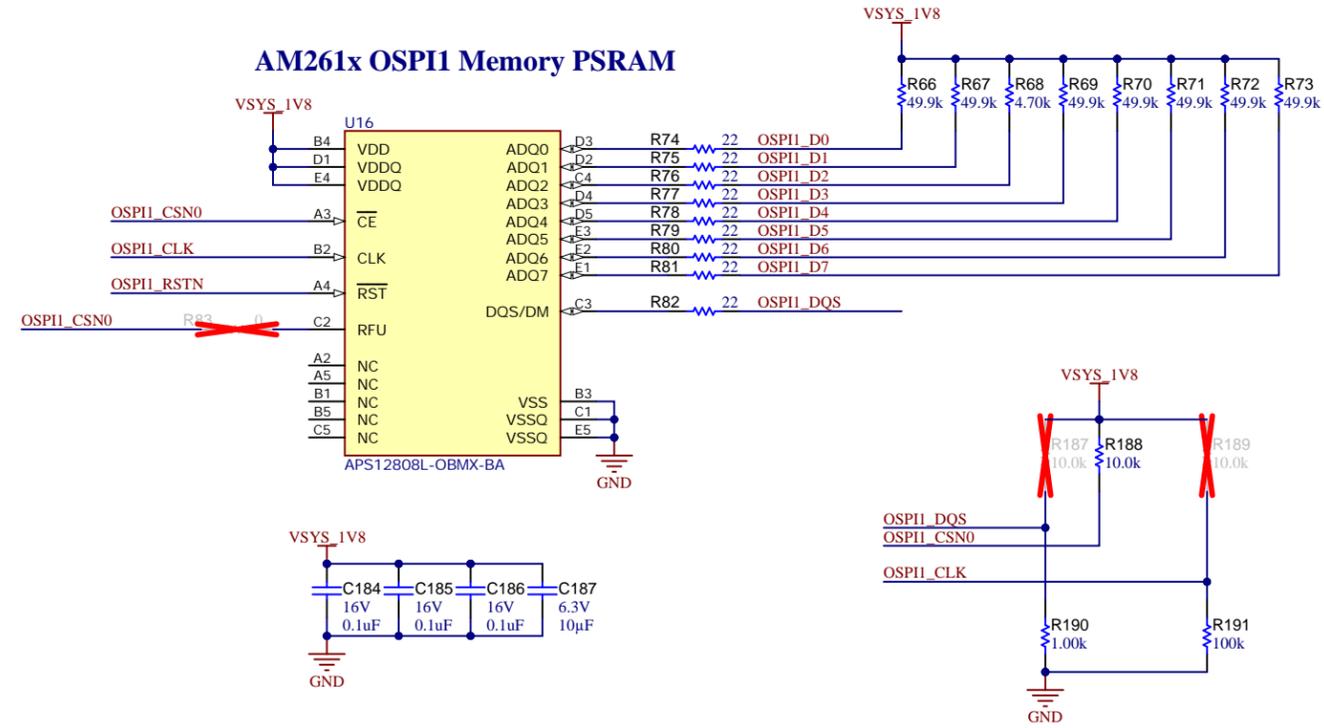
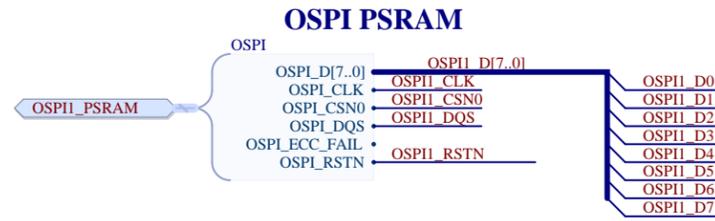
GND Test Points



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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 1/15/2026
TID #: TIDA-010973	Project Title: 100Mbit IE Comm Module	
Number: TIDA-010973	Rev: E2	Sheet Title:
SVN Rev:	Assembly Variant: 001	Sheet: 7 of 15
Drawn By:	File: TIDA-010973_SystemPower.SchDoc	Size: B
Engineer: Thomas Mauer	Contact: http://www.ti.com/support	



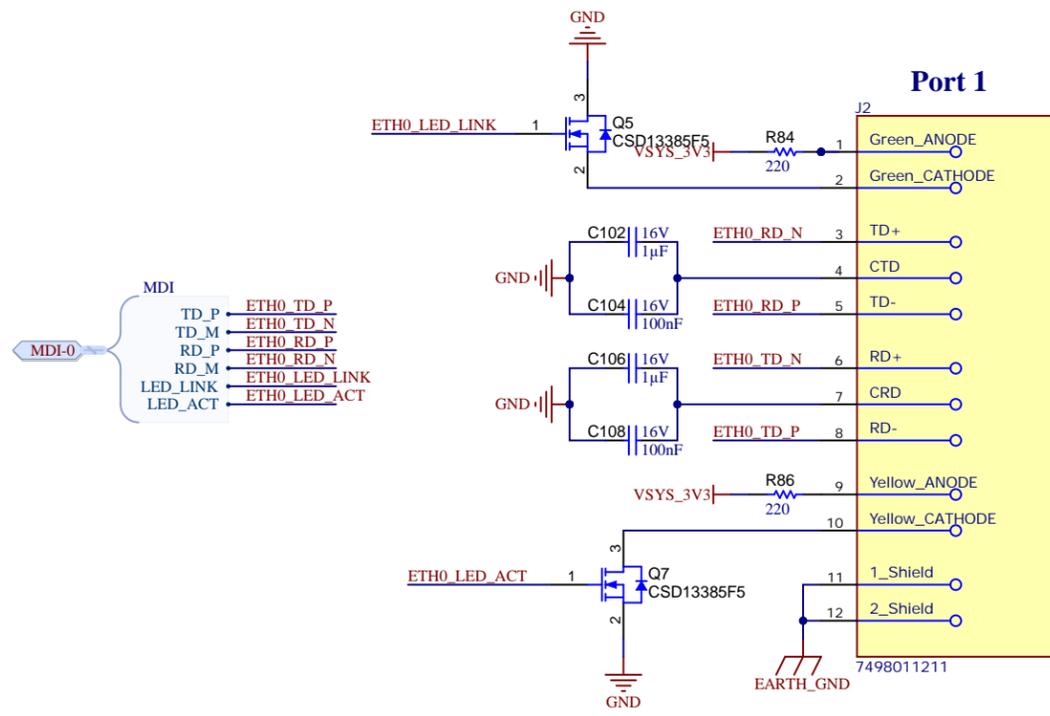


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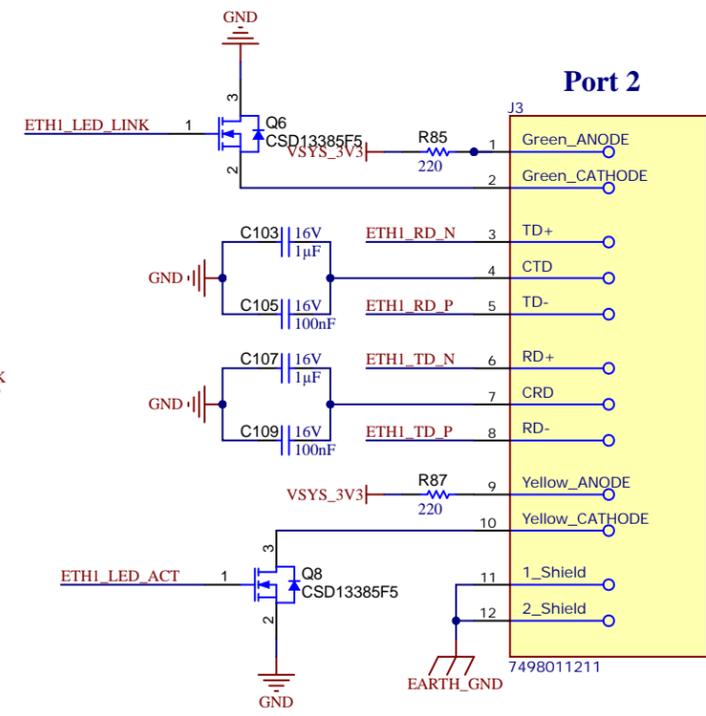
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Number: TIDA-010973	Rev: E2	Sheet Title:
SVN Rev:	Assembly Variant: 001	Sheet: 8 of 15
Drawn By:	File: TIDA-010973_Memory.SchDoc	Size: B
Engineer: Thomas Mauer	Contact: http://www.ti.com/support	

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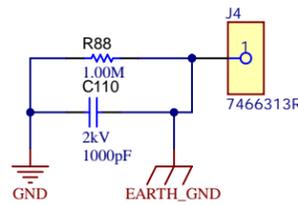


Note: Connected MDI to RJ45 in mirrored moded to simplify routing. See dev note at SOM Ethernet schematic for further information.

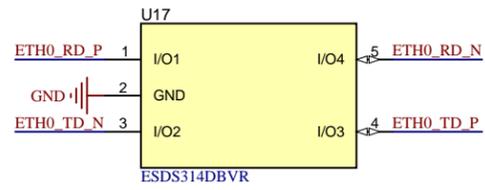


Note: Connected MDI to RJ45 in mirrored moded to simplify routing. See dev note at SOM Ethernet schematic for further information.

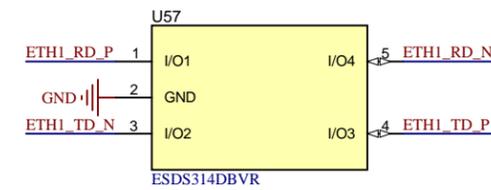
EMC Test Port



ESD protection

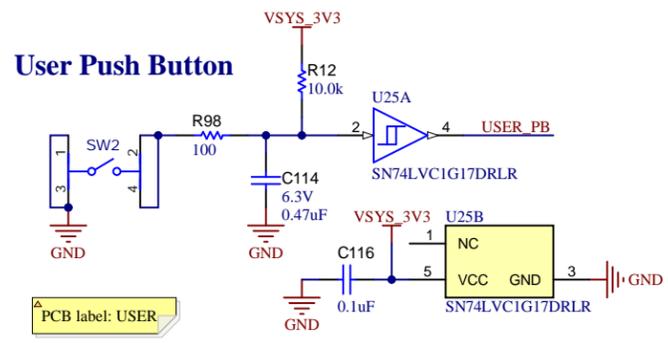
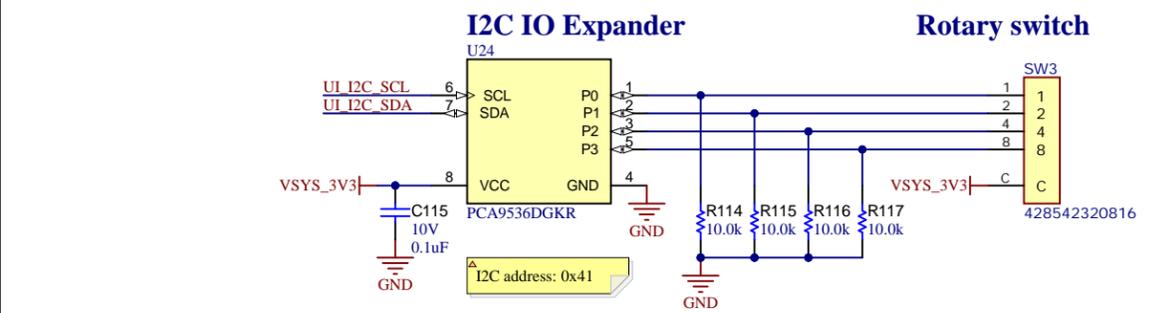
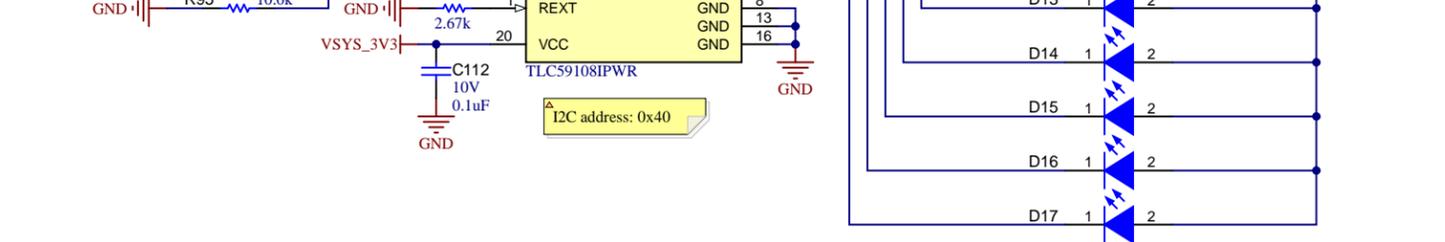
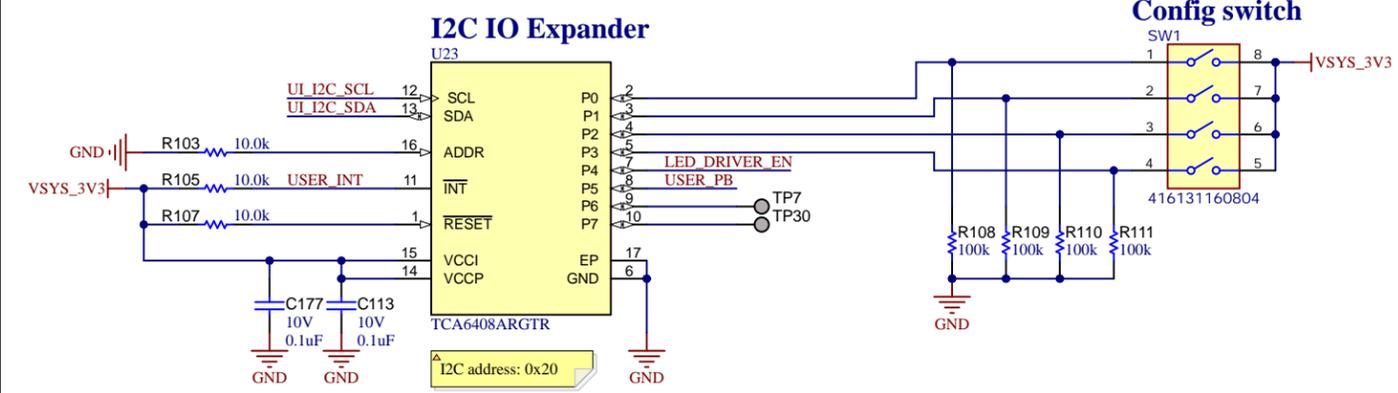
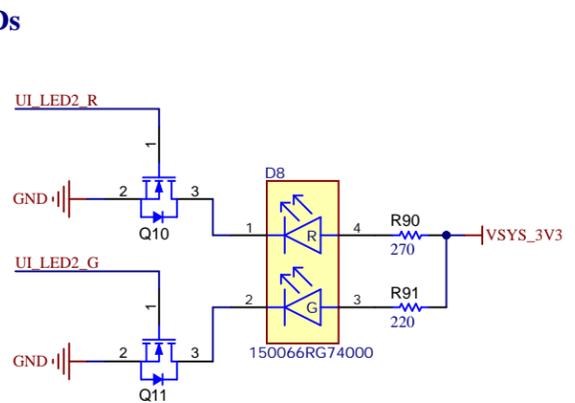
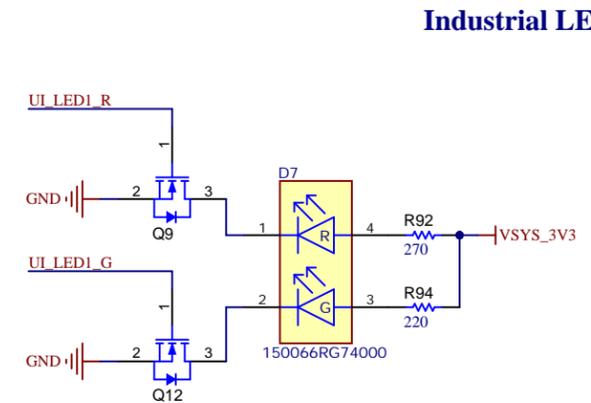
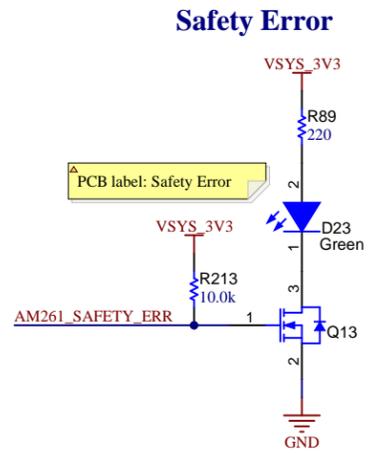
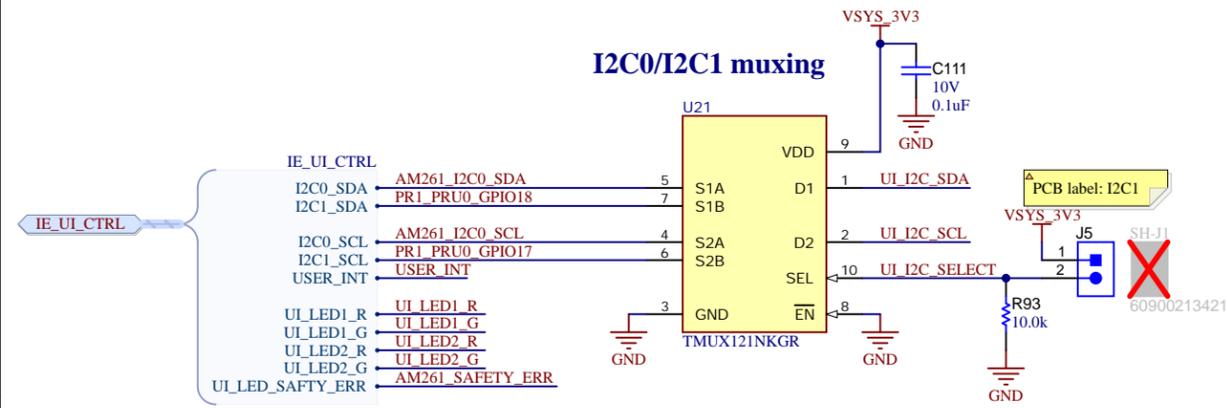


ESD protection



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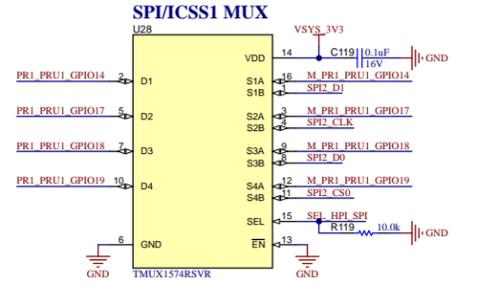
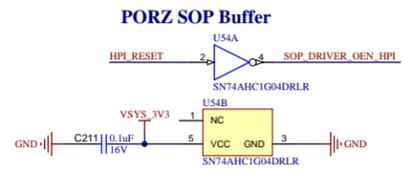
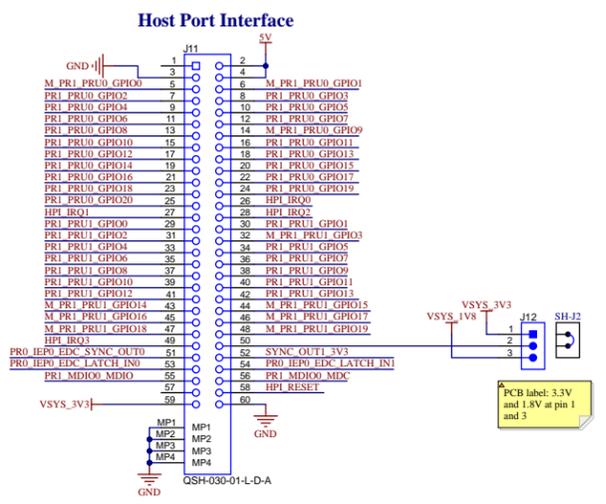
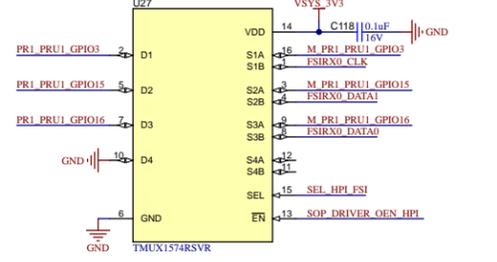
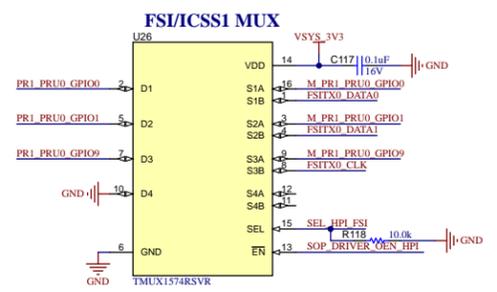
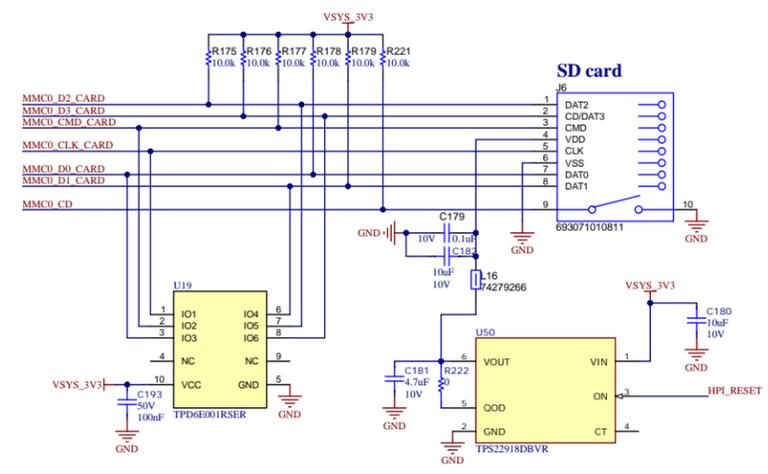
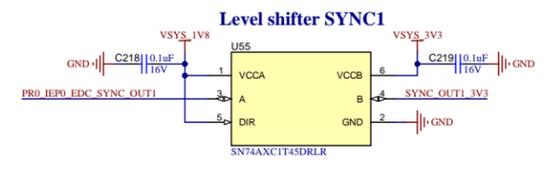
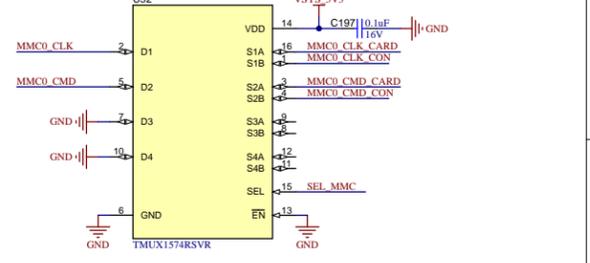
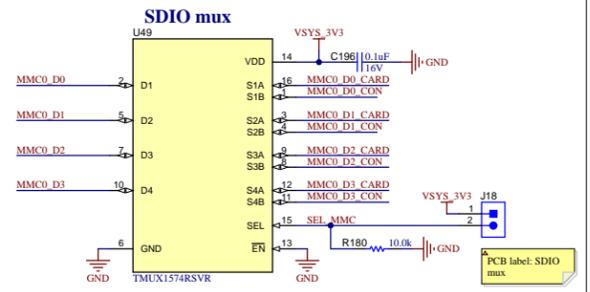
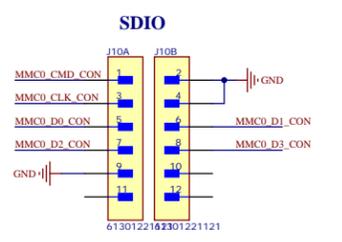
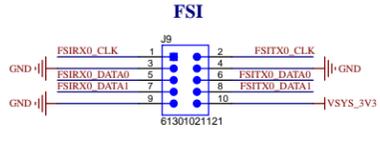
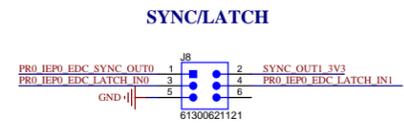
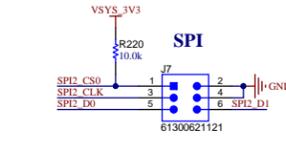
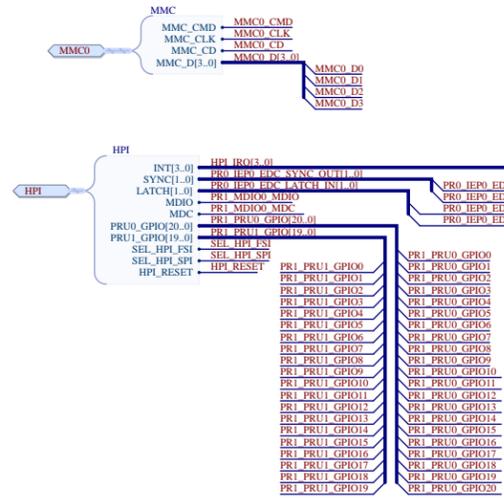
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Drawn By:	File: TIDA-010973_EthernetConnector.SchDoc	Size: B
Engineer: Thomas Mauer	Contact: http://www.ti.com/support	



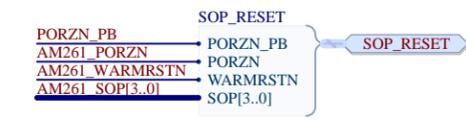
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TID #: TIDA-010973	Project Title: 100Mbit IE Comm Module	
Number: TIDA-010973	Rev: E2	Sheet Title:
SVN Rev: 16175	Assembly Variant: 001	Sheet: 10 of 15
Drawn By:	File: TIDA-010973_SystemLED.SchDoc	Size: B
Engineer: Thomas Mauer	Contact: http://www.ti.com/support	





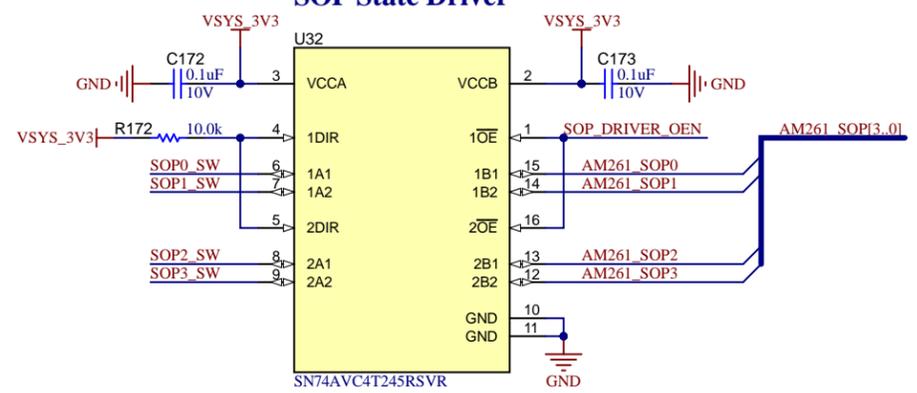
1.25V



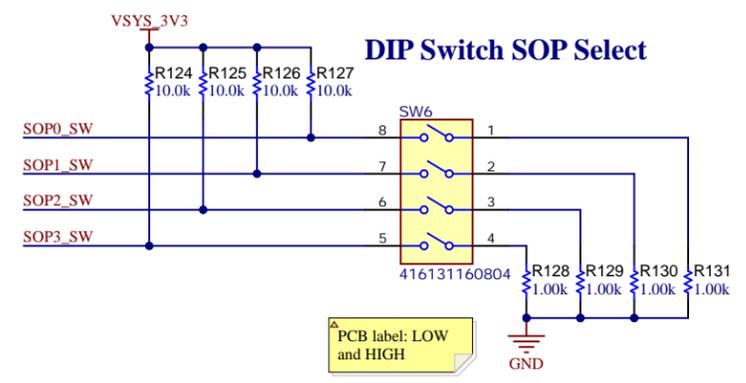
PORZ SOP Driver RC Delay



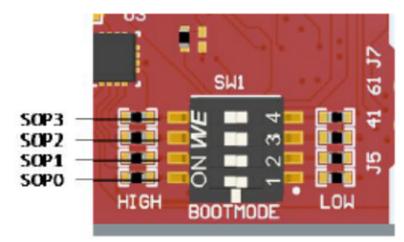
SOP State Driver



DIP Switch SOP Select

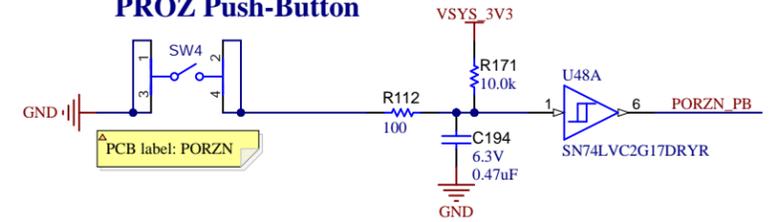


PCB label: LOW and HIGH

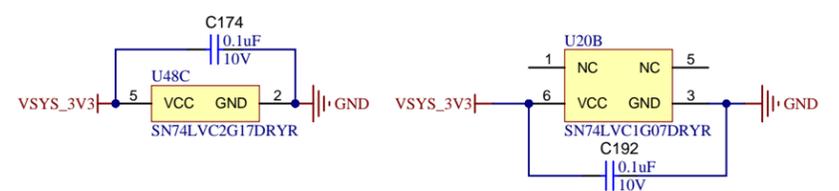
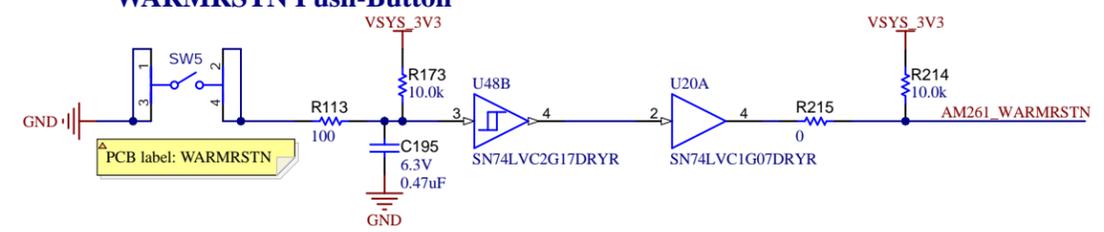


A SOP[3:0] switch description:
 - Switch "off" SOPx high
 - Switch "on" SOPx low
 - SOP[3:0] = 0b0001 -> UART
 - SOP[3:0] = 0b1100 -> OSPI0(1S->8D)
 - SOP[3:0] = 0b0011 -> OSPI0(8S),SDR
 - SOP[3:0] = 0b1011 -> DevBoot
 - SOP[3:0] = 0b1110 -> USB2.0 DFU

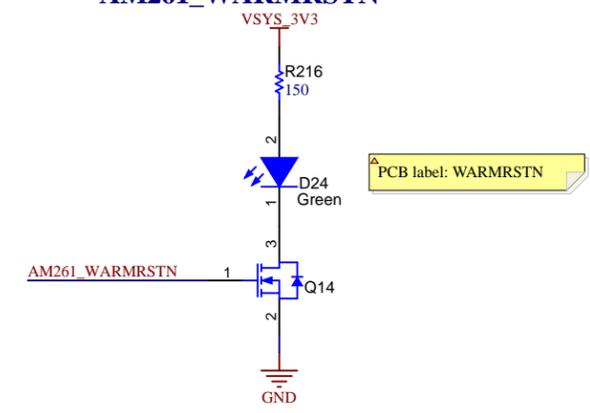
PROZ Push-Button



WARMRSTN Push-Button

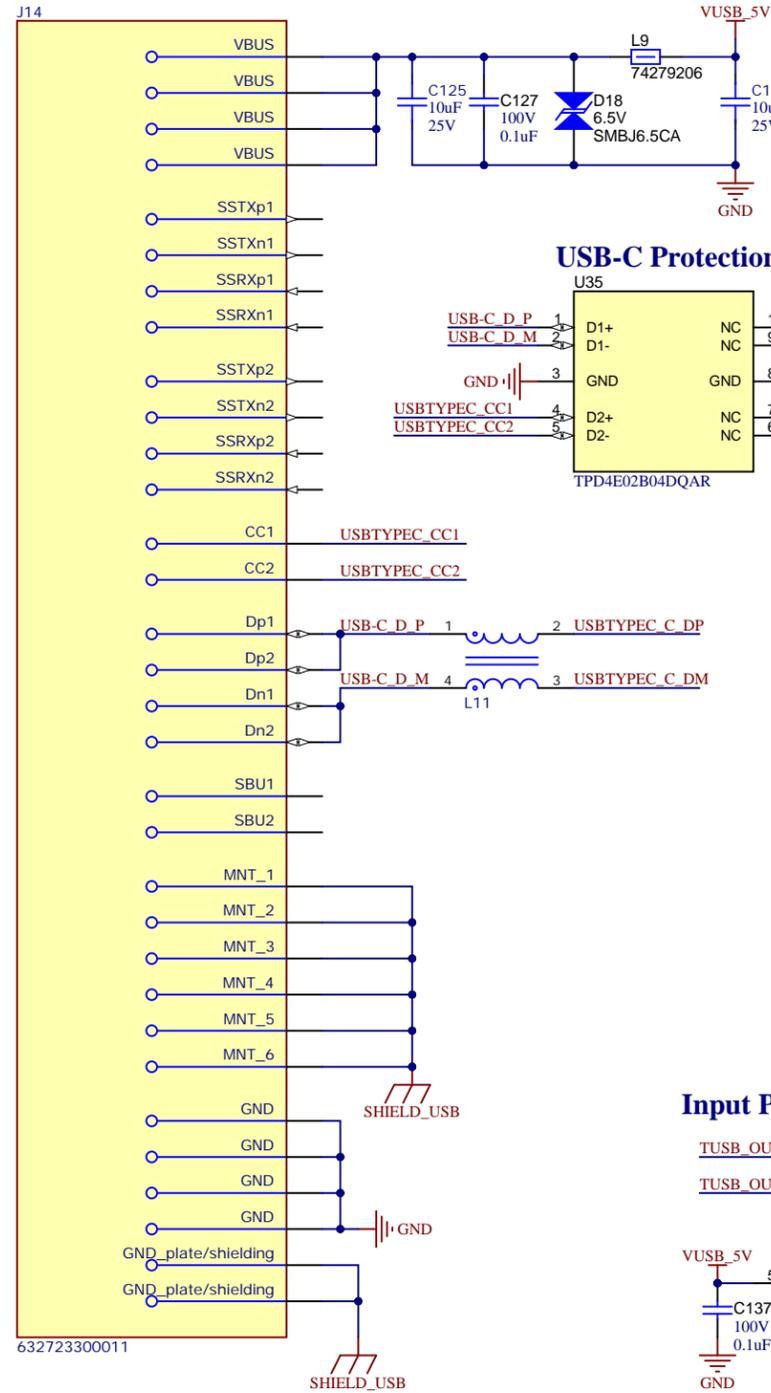


AM261_WARMRSTN

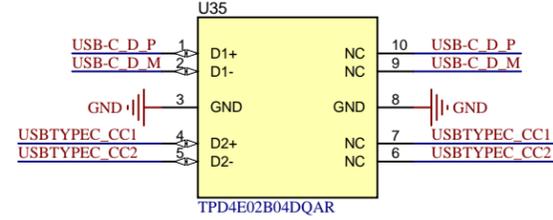


PCB label: WARMRSTN

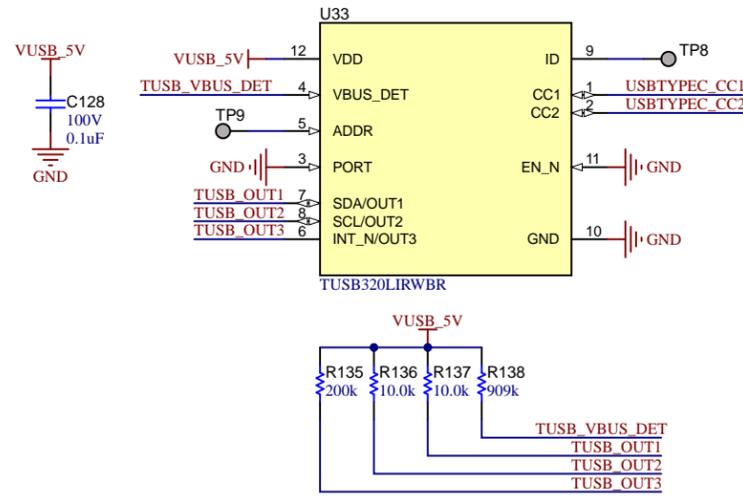
USB Type-C Power Input: 5.0V, 3.1A



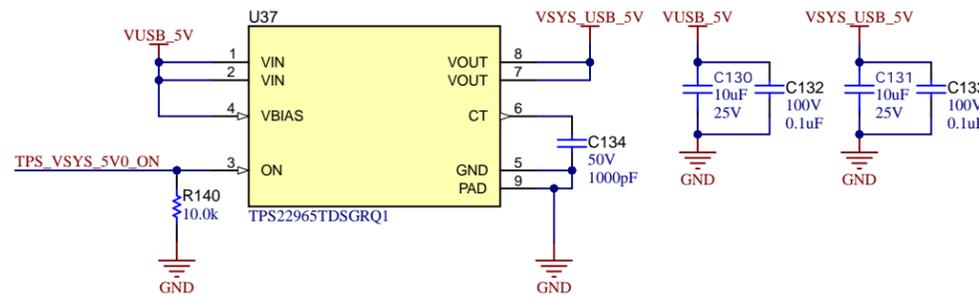
USB-C Protection



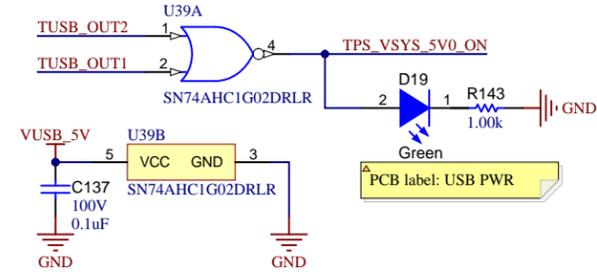
USB Type-C CC Logic Controller



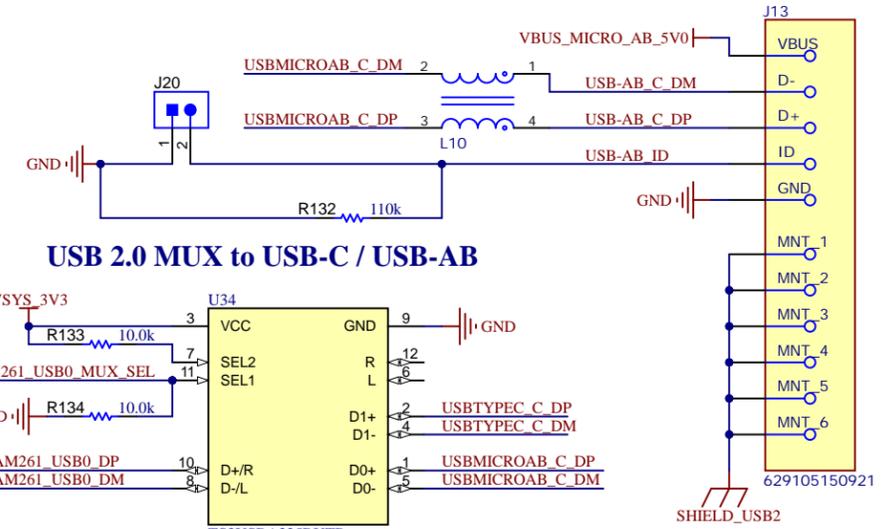
USB 5.0V Input Power Load Switch (4A max)



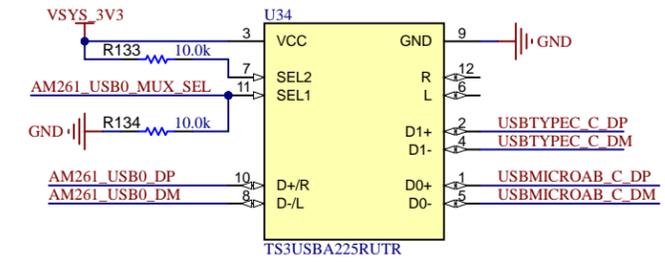
Input Power Load Switch Enable



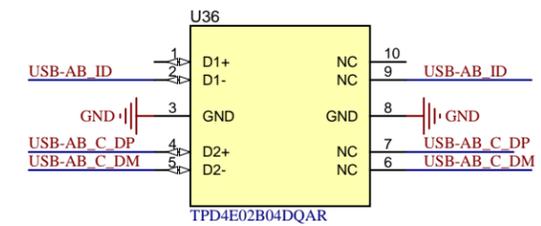
USB Type-AB



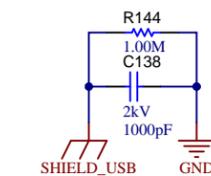
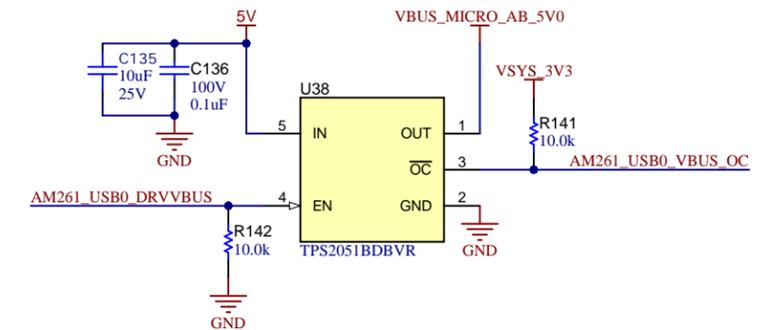
USB 2.0 MUX to USB-C / USB-AB



USB-AB Protection



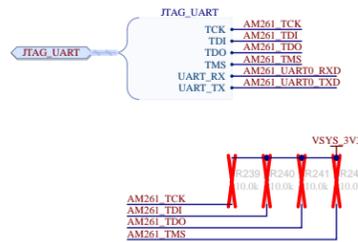
USB micro AB Power-Distribution Switch



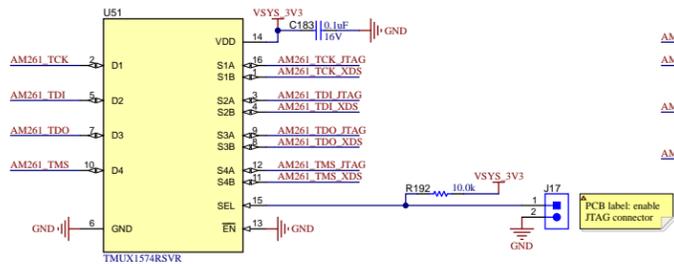
Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 1/15/2026
TID #: TIDA-010973	Project Title: 100Mbit IE Comm Module	
Number: TIDA-010973	Rev: E2	Sheet Title:
SVN Rev:	Assembly Variant: 001	Sheet: 13 of 15
Drawn By:	File: TIDA-010973_USB2.SchDoc	Size: B
Engineer: Thomas Mauer	Contact: http://www.ti.com/support	

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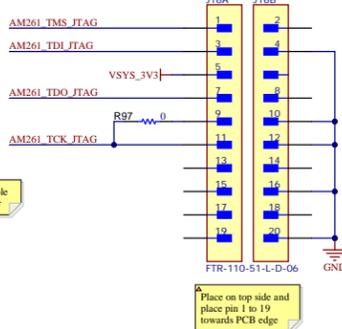
JTAG/UART i/F



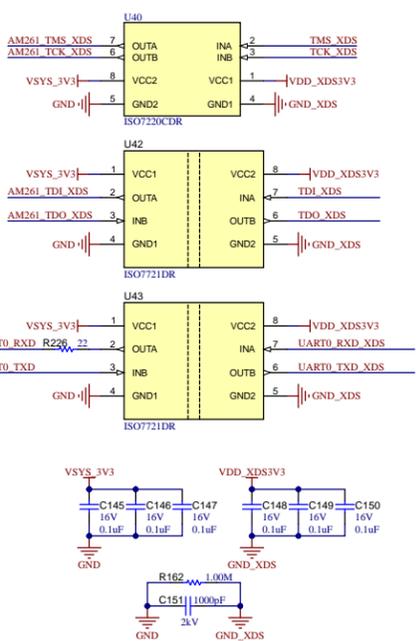
XDS / 20-pin JTAG MUX



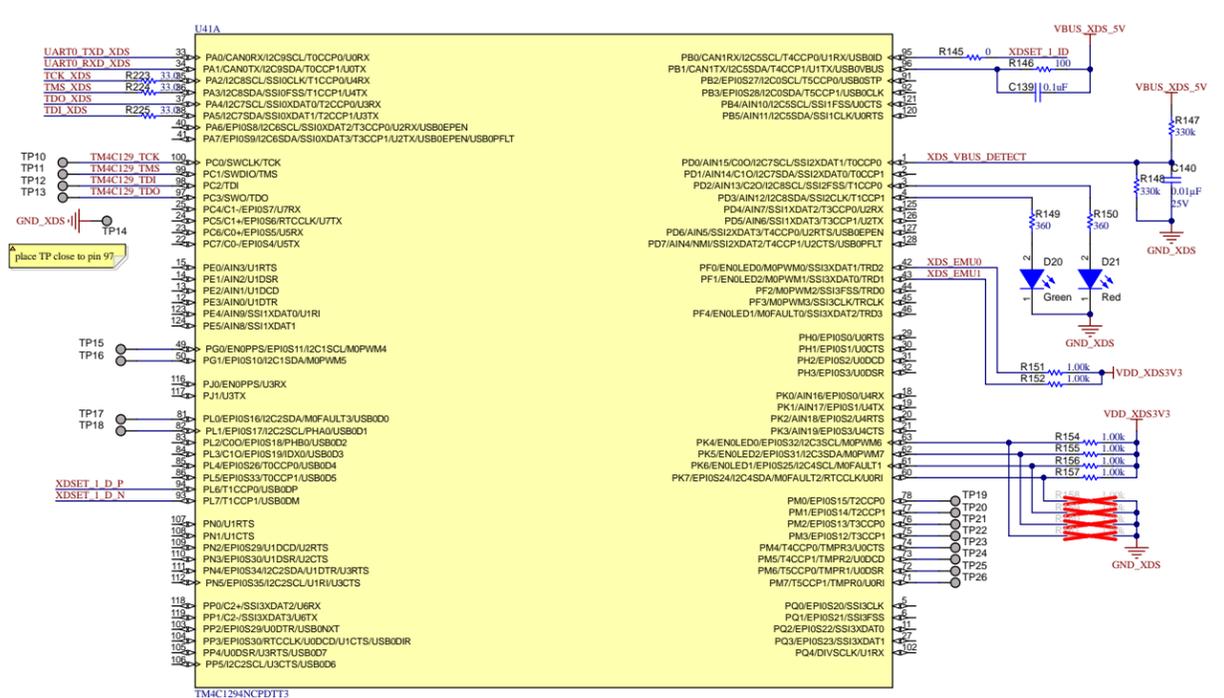
20-pin JTAG



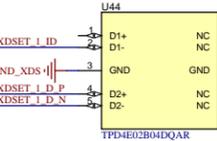
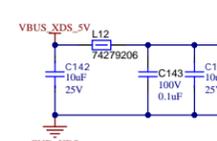
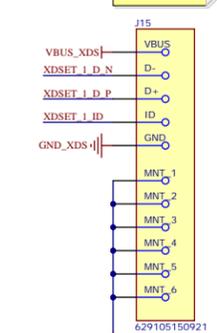
PWR isolation barrier



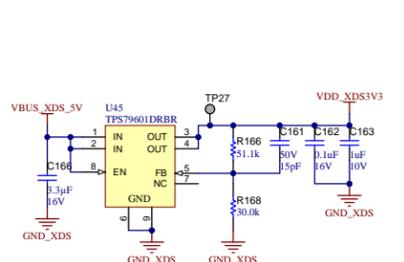
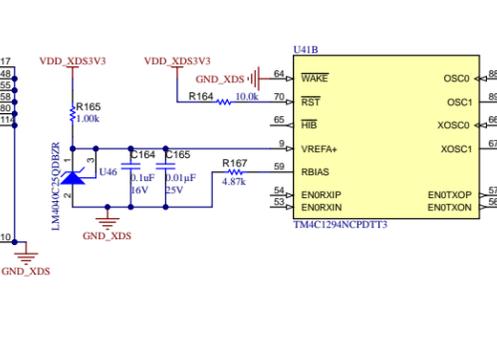
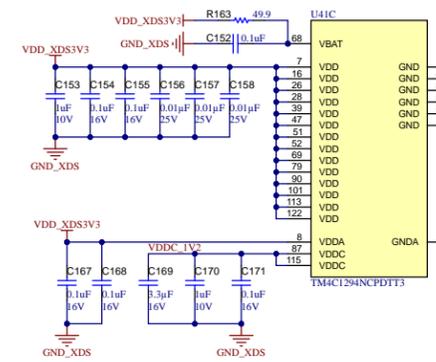
XDS110 JTAG/USB-to-UART Bridge



PCB label: XDS110



Place TM4 (and additional related parts, if possible) on bottom side.





PCB Number: TIDA-010973
PCB Rev: E2

PCB LOGO
Texas Instruments



PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

Variant/Label Table

Variant	Label Text
001	ChangeMe!
002	ChangeMe!

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 2/13/2026	 http://www.ti.com <small>© Texas Instruments 2026</small>
TID #: TIDA-010973	Project Title: 100Mbit IE Comm Module		
Number: TIDA-010973 Rev: E2	Sheet Title:		
SVN Rev: 16154 [Locally Modified]	Assembly Variant: 001	Sheet: 15 of 15	
Drawn By:	File: TIDA-010973_Hardware.SchDoc	Size: B	
Engineer: Thomas Mauer	Contact: http://www.ti.com/support		

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