# LM317M, LM317MQ Adjustable Floating Regulators

## 1 Features

- LM317MQ (new chip) AEC-Q100 qualified for automotive applications
  - Temperature grade 2: –40°C ≤ $T_A$ ≤ 105°C
- Adjustable output voltage range ($V_{OUT}$): 1.25V to 37V
- Output current ($I_{OUT}$): Up to 500mA
- Built-in, short-circuit current limiting and thermal protection
- Stable without any output capacitor
- Operating junction temperature: –40°C to +125°C
- Packages:
  - 4-pin, 6.5mm × 7mm SOT-223 ($R_{\theta JA}$[new chip] : 77.7°C/W)
  - 3-pin, 6.6mm × 10.11mm TO-252 ($R_{\theta JA}$[new chip] : 31.7°C/W)

## 2 Applications

- Cordless vacuum cleaners
- Building security gateways
- Multifunction printers
- Onboard charging

## 3 Description

The LM317M and LM317MQ are adjustable floating, positive-voltage regulators capable of supplying an output current of 0.5A over an output voltage range of 1.25V to 37V. The device requires only two external resistors to set the output voltage. The device features a typical line regulation of 0.01% and typical load regulation of 0.1%. The device includes current limiting, thermal overload protection, and safe operating area protection.

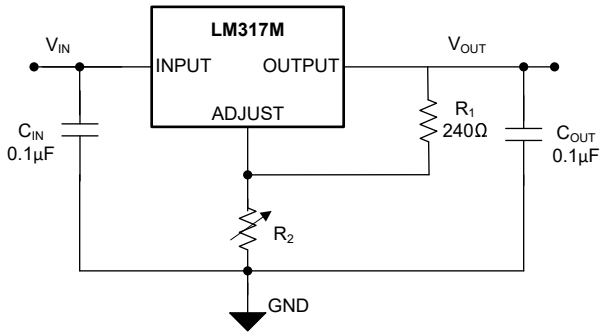
The device is a floating regulator meaning there is no device ground terminal. Quiescent current flows to the load instead of being wasted flowing to ground. Regulated output voltage of hundreds of volts is possible if the maximum input to output differential does not exceed 37V at any time. The device can function as a floating current source controlled by a single resistor.

Additionally, the device does not need an output capacitor for stable operation across the load current range. Optionally, the transient performance of the device can be improved using an electrolytic or tantalum output capacitor. Bypass the ADJUST pin with any type of capacitor to achieve high ripple-rejection ratios.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| LM317M, LM317MQ | DCY (SOT-223, 4) | 6.5mm × 7mm |
| | KVU (TO-252, 3) | 6.6mm × 10.11mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Circuit**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

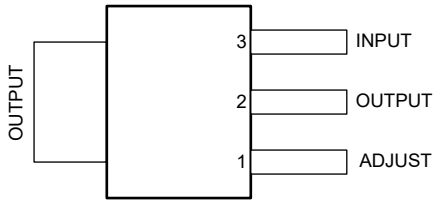


**Figure 4-1. DCY Package, 4-Pin SOT-223 (Top View)**

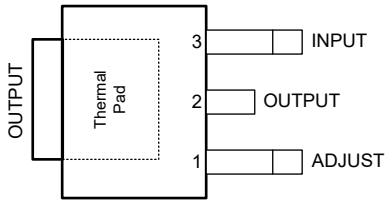


**Figure 4-2. KVU Package, 3-Pin TO-252 (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ADJUST | 1 | I | Output feedback voltage |
| OUTPUT | 2 | O | Regulated output voltage. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUTPUT and COMMON pins of the device as possible. |
| INPUT | 3 | – | Input supply voltage, 2.5V to 37V relative to OUTPUT pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the INPUT and COMMON pins of the device as possible. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Vi - Vo | Input-to-output differential voltage | | 40 | V |
| $T_J$ | Operating junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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## 5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ - $V_O$ | Input-to-output differential voltage | 2.5 | | 37 | V |
| $V_O$ | Output voltage | 1.25 | | 37 | V |
| $I_O$ | Output current | 0.01 | | 0.5 | A |
| $C_{IN}$ | Input capacitor | | 0.1 | | µF |
| $C_{OUT}$ (1) | Output capacitor | | 0.1 | | µF |
| ESR(1) | Output capacitor | 0.01 | | 2 | Ω |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) LM317M regulator doesn't need any output capacitor for LDO stability.

## 5.4 Thermal Information

| THERMAL METRIC(1) | | LM317M, LM317MQ | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DCY (Legacy Chip) | DCY (New Chip) | KVU (Legacy Chip) | KVU (New Chip) | |
| | | 4 PINS | 4 PINS | 3 PINS | 3 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 60.2 | 77.7 | 34.8 | 31.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 42 | 44.6 | 46.3 | 39.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 9.4 | 15.1 | 15.6 | 10.1 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 3.4 | 5.3 | 6.9 | 3.8 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 9.3 | 14.7 | 15.6 | 10.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | 6.2 | 3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.


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## 5.5 Electrical Characteristics (Both Legacy and New Chip)

Over recommended operating virtual-junction temperature range $T_J$ = –40°C to 125°C, $V_I – V_O$ = 5V, $I_O$ = 0.1A (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Line regulation | $V_I – V_O$ = 3V to 40V | $T_J$ = 25°C | Legacy chip and new chip | | 0.01 | 0.04 | %/V |
| | | Legacy chip and new chip | | | 0.02 | 0.07 | |
| Load regulation | $I_O$= 10mA to 500mA | $T_J$ = 25°C | Legacy chip | | 0.1 | 0.5 | % |
| | | | New chip | | 0.1 | 0.24 | |
| | | Legacy chip | | | 0.3 | 1.5 | |
| | | New chip | | | 0.1 | 0.8 | |
| ADJUST terminal current | | | Legacy chip | | 50 | 100 | uA |
| | | | New chip | | 45 | 65 | |
| Change in ADJUST terminal current | $V_I – V_O$ = 3V to 40V, $I_O$ = 10mA to 500mA | | Legacy chip | | 0.2 | 5 | uA |
| | $V_I – V_O$ = 3V to 15V, $I_O$ = 10mA to 500mA<br>$V_I – V_O$ = 15V to 40V, $I_O$ = 100mA | | New chip | | 0.2 | 5 | uA |
| Reference voltage | $V_I – V_O$ = 3V to 40V, $I_O$ = 10mA to 500mA | | Legacy chip | 1.2 | 1.25 | 1.3 | V |
| | $V_I – V_O$ = 3V to 15V, $I_O$ = 10mA to 500mA<br>$V_I – V_O$ = 15V to 40V, $I_O$ = 100mA | | New chip | 1.2 | 1.25 | 1.3 | V |
| Minimum load current to maintain regulation | | | Legacy chip | | 3.5 | 10 | mA |
| | | | New chip | 1.1 | 2 | 3.5 | |
| Output-voltage temperature stability | | | Legacy chip and new chip | | 0.7 | | % |
| Maximum output current | $V_I – V_O$ ≤ 15V | | Legacy chip | 500 | 900 | | mA |
| | | | New chip | 500 | 1000 | 1600 | |
| | $V_I – V_O$ = 40V, PD ≤ PD(max) (1) | $T_J$ = 25°C | Legacy chip | 150 | 250 | | |
| | | | New chip | 110 | 220 | 350 | |
| RMS output noise voltage (% of VO) | f = 10Hz to 10kHz, | $T_J$ = 25°C | Legacy chip and new chip | | 0.003 | | $\%V_O$ |
| Long-term stability | | $T_J$ = 25°C | Legacy chip | | 0.3 | 1 | %/1k hrs |
| | $I_O$=10mA | $T_J$ = 25°C | New chip | | 0.3 | 1 | |
| Ripple rejection | $V_O$ = 10 V, f = 120Hz, $C_{ADJ}$ = 0 | $T_J$ = 25°C | Legacy chip | | 65 | | dB |
| | | | New chip | | 65 | | |
| | $V_O$ = 10 V, f = 120Hz, $C_{ADJ}$ = 10µF | $T_J$ = 25°C | Legacy chip | 66 | 80 | | |
| | | | New chip | 66 | 80 | | |

(1) Maximum power dissipation is a function of $T_J$ (max), $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is PD = ($T_J$ (max) – $T_A$) / $\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.

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## 5.6 Typical Characteristics

Over recommended operating virtual-junction temperature range $T_J$ = –40°C to 125°C, $V_I$ – $V_O$ = 5V, $I_O$ = 0.1A (unless otherwise noted)

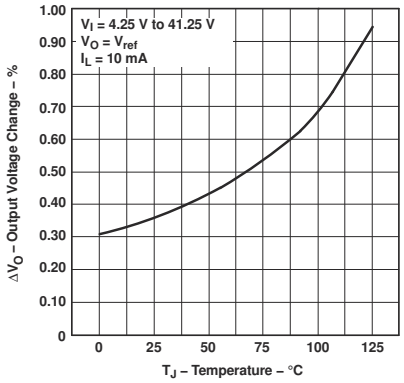


**Figure 5-1. Line Regulation vs Temperature (Legacy Chip)**

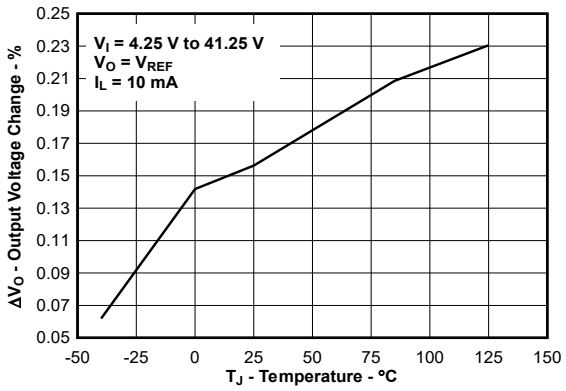


**Figure 5-2. Line Regulation vs Temperature (New Chip)**

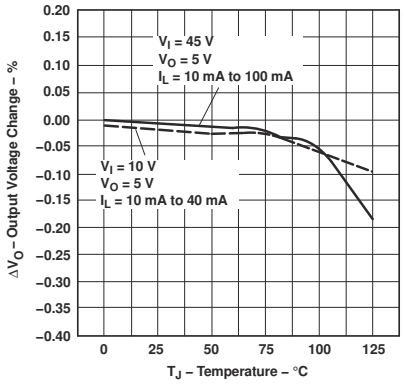


**Figure 5-3. Load Regulation vs Temperature (Legacy Chip)**

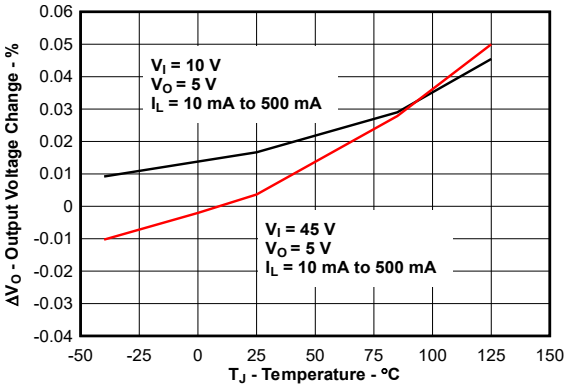


**Figure 5-4. Load Regulation vs Temperature (New Chip)**

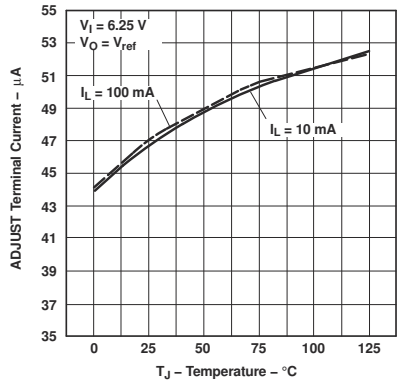


**Figure 5-5. Adjust Pin Current vs Temperature (Legacy Chip)**

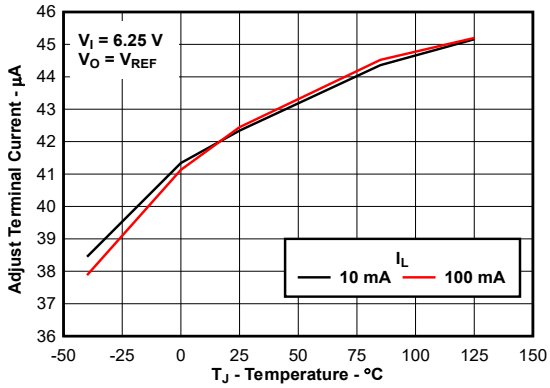


**Figure 5-6. Adjust Pin Current vs Temperature (New Chip)**


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## 5.6 Typical Characteristics (continued)

Over recommended operating virtual-junction temperature range $T_J$ = –40°C to 125°C, $V_I – V_O$ = 5V, $I_O$ = 0.1A (unless otherwise noted)

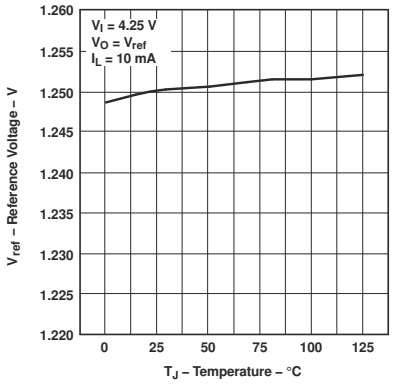


**Figure 5-7. $V_{REF}$ Temperature Stability vs Temperature (Legacy Chip)**

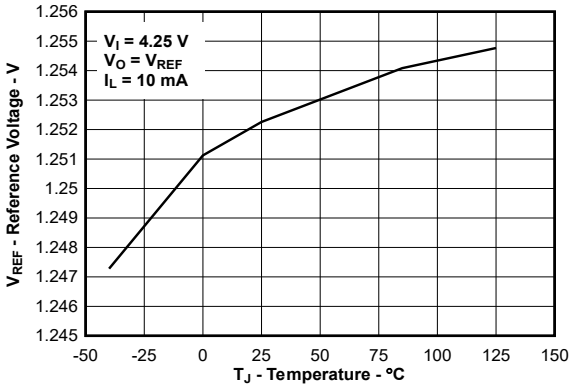


**Figure 5-8. $V_{REF}$ Temperature Stability vs Temperature (New Chip)**

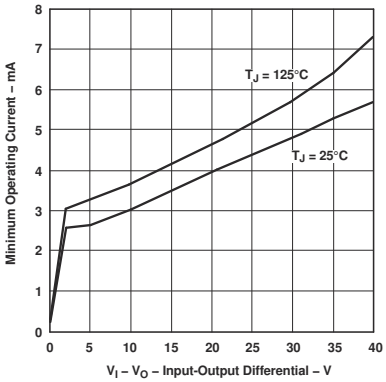


**Figure 5-9. Minimum Operating Current vs Input-Output Differential Voltage (Legacy Chip)**

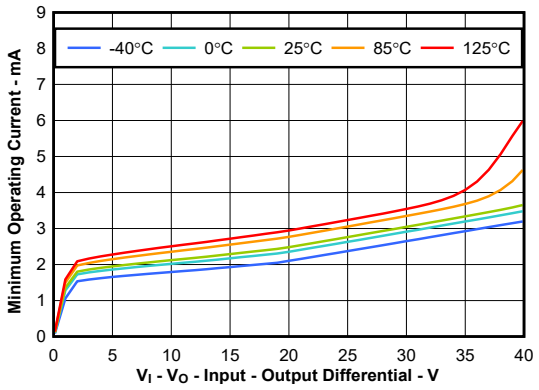


**Figure 5-10. Minimum Operating Current vs Input-Output Differential Voltage (New Chip)**

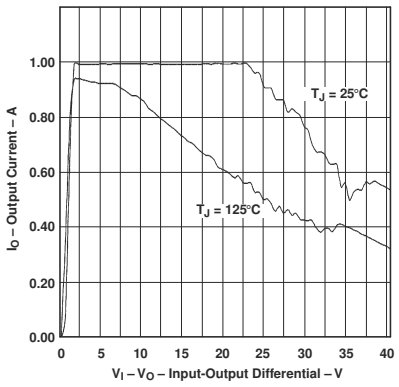


**Figure 5-11. Output Current Limit vs Input-Output Differential Voltage (Legacy Chip)**

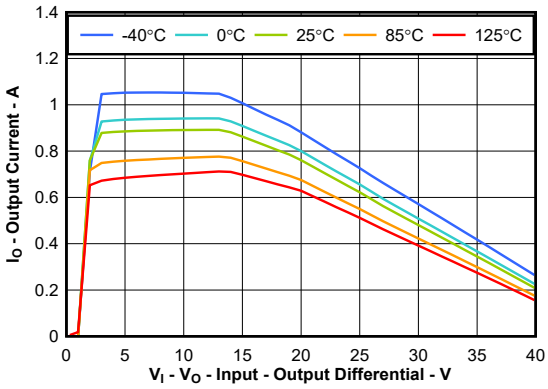


**Figure 5-12. Output Current Limit vs Input-Output Differential Voltage (New Chip)**

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## 5.6 Typical Characteristics (continued)

Over recommended operating virtual-junction temperature range $T_J$ = –40°C to 125°C, $V_I – V_O$ = 5V, $I_O$ = 0.1A (unless otherwise noted)

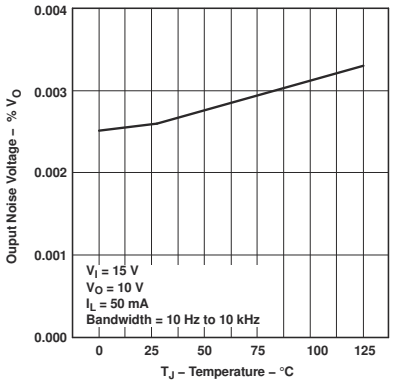
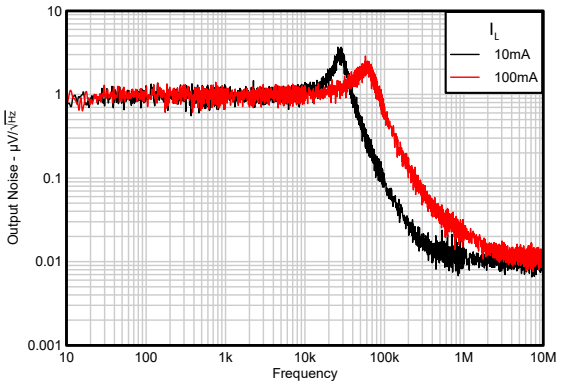



**Figure 5-13. Output Noise Voltage vs Temperature (Legacy Chip)**




$V_I$ = 15V, $V_O$ = 10V, $I_L$ = 100mA, $C_L$ = 1µF, $C_{ADJ}$ = 0µF

**Figure 5-14. Output Noise Voltage vs Output current (New Chip)**

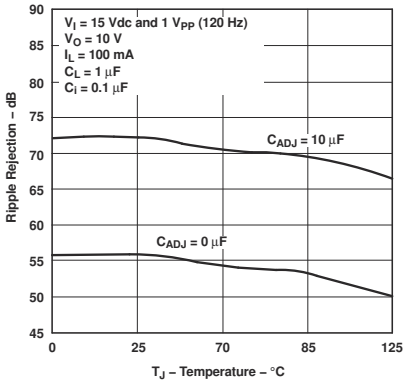



**Figure 5-15. Ripple Rejection vs Temperature (Legacy Chip)**

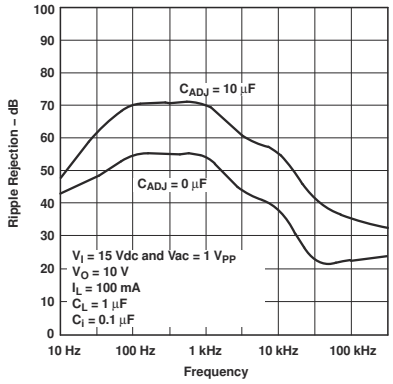
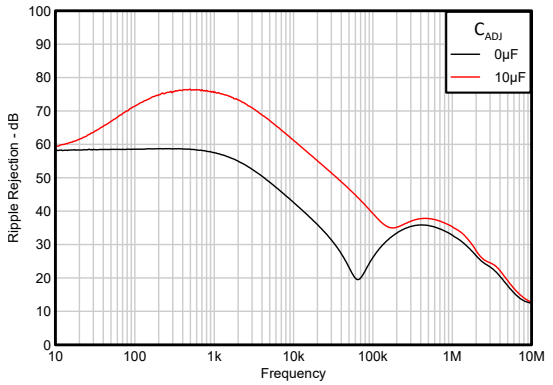



**Figure 5-16. Ripple Rejection vs Frequency (Legacy Chip)**




$V_I$ = 15V, $V_{AC}$ = $1_{VPP}$, $V_O$ = 10V, $I_L$ = 100mA, $C_L$ = 1µF

**Figure 5-17. Ripple Rejection vs Frequency (New Chip)**

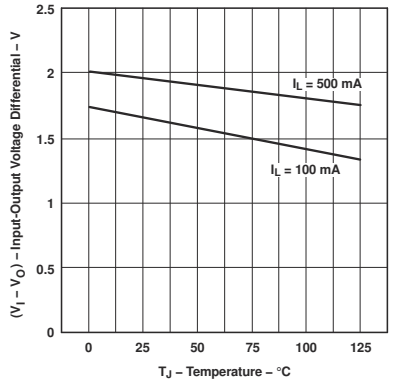



**Figure 5-18. Input-Output Voltage Differential (Dropout) vs Temperature (Legacy Chip)**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## 5.6 Typical Characteristics (continued)

Over recommended operating virtual-junction temperature range $T_J$ = –40°C to 125°C, $V_I$ – $V_O$ = 5V, $I_O$ = 0.1A (unless otherwise noted)

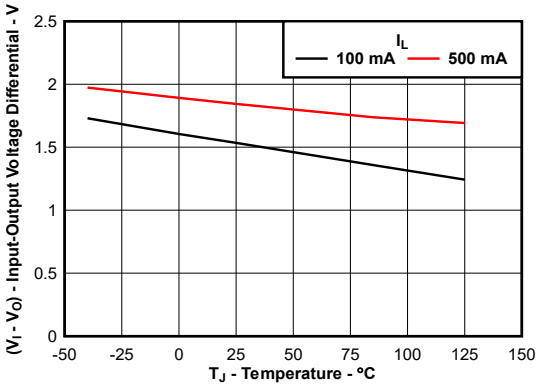



**Figure 5-19. Input-Output Voltage Differential (Dropout) vs Temperature (New Chip)**

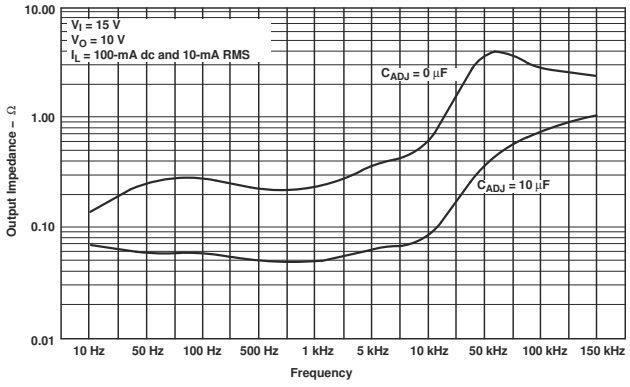


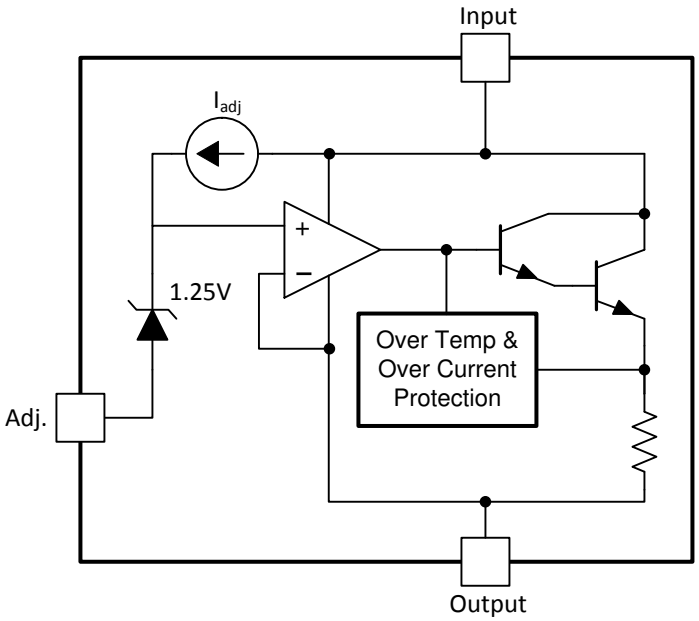

**Figure 5-20. Output Impedance vs Frequency (Legacy Chip)**

# 6 Detailed Description

## 6.1 Overview

The LM317M and LM317MQ is an adjustable floating, positive-voltage regulator capable of supplying up to 500mA over an output voltage range of 1.25V to 37V. The device has a feedback voltage relative to the output instead of ground. The device requires only two external resistors to set the output voltage. The LM317MQ includes current limiting, thermal overload protection, and safe operating area protection. Overload protection remains functional even if the ADJUST pin is disconnected. By connecting a fixed resistor between the ADJUST and OUTPUT pins, the device can function as a precision current regulator. Add an optional output capacitor to improve transient response. Bypass the ADJUST pin to achieve very high ripple-rejection ratios, which are difficult to achieve with standard three-terminal regulators.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### *6.3.1 Current Limit*

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. In a high-load current fault, the current limit scheme limits the output current to the current limit ($I_{CL}$). $I_{CL}$ is listed in the *Electrical Characteristics (Both Legacy and New Chip)* table.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in current limit, the pass transistor dissipates power [$(V_I – V_O) \times I_{CL}$]. For more information on current limits, see the *Know Your Limits* application note.

To achieve a safe operation across a wide range of Input voltage, the device also has a built-in protection mechanism with current limit. The protection mechanism decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. This protection is designed to provide some output current at all values of input-to-output voltage limits defined in the *Recommended Operating Conditions* table. Figure 6-1 illustrates the behavior of the current limit variation.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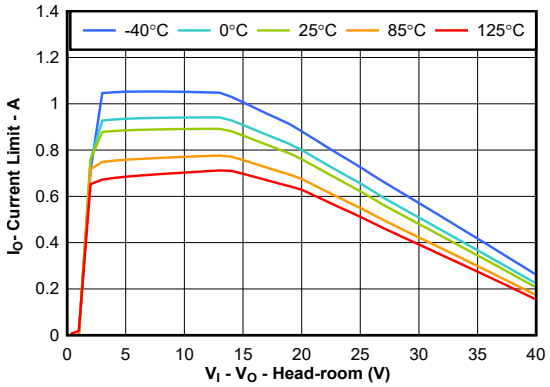


**Figure 6-1. Current-Limit vs $V_{Head\text{-}room}$ Behavior (New Chip)**

### *6.3.2 Dropout Voltage ($V_{DO}$)*

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_I$ – $V_O$) at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $I_{RATED}$ is the maximum $I_O$ listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

### *6.3.3 Thermal Shutdown*

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large $V_I$ – $V_O$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

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## 6.4 Device Functional Modes

### 6.4.1 Normal Operation

The device OUTPUT pin regulates to 1.25V greater than the ADJUST pin under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)}$ + $V_{DO}$).
- The output current is less than the current limit ($I_O$ < $I_{CL}$).
- The device passes the bias current to the OUTPUT pin. The load or feedback consumes this minimum current for regulation.
- The device junction temperature is greater than –40°C and less than +125°C.

### 6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_I$ < $V_{OUT(NOM)}$ + $V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)}$ + $V_{DO}$), the output voltage overshoots for a short period of time while the device pulls the pass transistor back into the linear region.


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# 7 Applications and Implementation

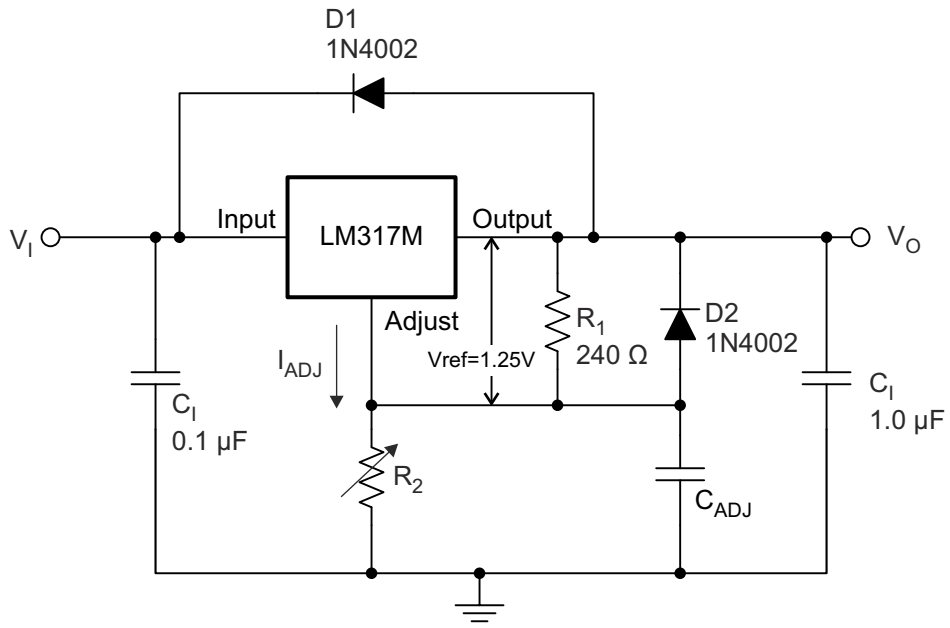
**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The LM317M and LM317MQ are linear voltage regulators. The feedback is the output pin to adjust pin differential. Set the output voltage to any value from 1.25V to $V_O$ maximum with two resistors.

## 7.2 Typical Application




### *7.2.1 Design Requirements*

For this design example, use the parameters listed in Table 7-1.

**Table 7-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | (Output voltage + 2.5V) to 37V |
| Output voltage | $V_{ref}$ × (1 + R2 / R1) + $I_{adj}$ × R2 |

### *7.2.2 Detailed Design Procedure*

#### 7.2.2.1 Input and Output Capacitor Requirements (Legacy Chip)

An input capacitor is not required, but is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1µF ceramic or 1µF tantalum capacitor provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used. An output capacitor improves transient response, but is not needed for stability.

#### 7.2.2.2 Input and Output Capacitor Requirements (New Chip)

Although the input and output capacitors are not required for stability, good analog design practice is to connect a capacitor from INPUT to ground and from OUTPUT to ground. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source

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impedance is more than 0.5Ω. A higher value capacitor is necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

#### 7.2.2.3 Feedback Resistors

The feedback resistor sets the output voltage using the following equation.

$$V_{ref} \times (1 + R2/R1) + I_{adj} \times R2 \quad (1)$$

#### 7.2.2.4 Adjustment Pin Capacitor

The optional adjustment pin capacitor improves ripple rejection by preventing the amplification of the ripple. When the capacitor is used and $V_{OUT}$ > 6V, a protection diode from adjust to output is recommended.

#### 7.2.2.5 Protection Diodes

If the input is shorted to ground during a fault condition, protection diode (D1) prevents discharge through the device. If the output is shorted to ground during a fault condition, protection diode (D2) prevents adjust pin capacitor discharge through the device.

#### 7.2.2.6 Overload Recovery

Because the input voltage rises when power is first turned on, the output follows the input, allowing the regulator to start up into very heavy loads. The input-to-output voltage differential is small during start up when the input voltage is rising, allowing the regulator to supply large output currents. With a high input voltage, a problem occurs where removing an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so the behavior is not unique to the LM317M and LM317MQ.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately when removing a short circuit after the input voltage is already turned on. The load line for such a load has the possibility to intersect the output current curve at two points. If this condition happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply is potentially cycled down to zero and brought up again to make the output recover to the desired voltage operating point.

#### 7.2.2.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter ($\psi_{JT}$) and junction-to-board characterization parameter ($\psi_{JB}$). These parameters provide two methods for calculating the junction temperature ($T_J$), as described in the following equations. Use the junction-to-top characterization parameter ($\psi_{JT}$) with the temperature at the center-top of device package ($T_T$) to calculate the junction temperature. Use the junction-to-board characterization parameter ($\psi_{JB}$) with the PCB surface temperature 1mm from the device package ($T_B$) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (2)$$

where:

- $P_D$ is the dissipated power
- $T_T$ is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (3)$$

where:


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- $T_B$ is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

#### 7.2.2.8 Polarity Reversal Protection

In many applications, a voltage regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of the opposite polarity (for example, operational amplifiers, level-shifting circuits, and so on). During start-up and short-circuit events, this connection leads to polarity reversal of the regulator output and damages the internal components of the regulator.

To avoid polarity reversal on the regulator output, use external protection to protect the device.

Figure 7-1 shows one approach for protecting the device.

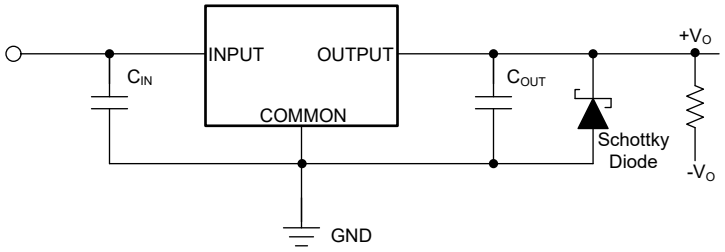


**Figure 7-1. Example Circuit for Polarity Reversal Protection Using a Schottky Diode**

#### 7.2.2.9 Reverse Current

Excessive reverse current damages this device. Reverse current flows through the emitter-base junction of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which exceed the absolute maximum rating of $V_O \leq V_I + 7V$. These conditions are:

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

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Figure 7-2 shows one approach for protecting the device.

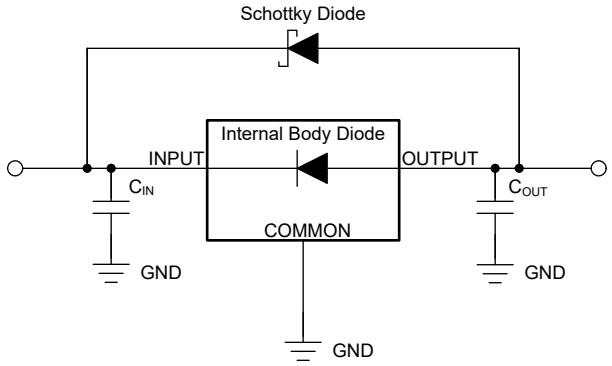


**Figure 7-2. Example Circuit for Reverse Current Protection Using a Schottky Diode**

#### 7.2.2.10 Power Dissipation ($P_D$)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation ($P_D$).

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

**Note**

Power dissipation is minimized, and therefore greater efficiency be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ($T_A$) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, $R_{\theta JA}$ is improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization.


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### 7.2.3 Application Curves

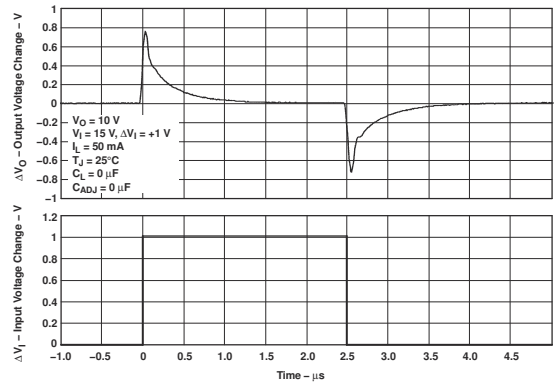
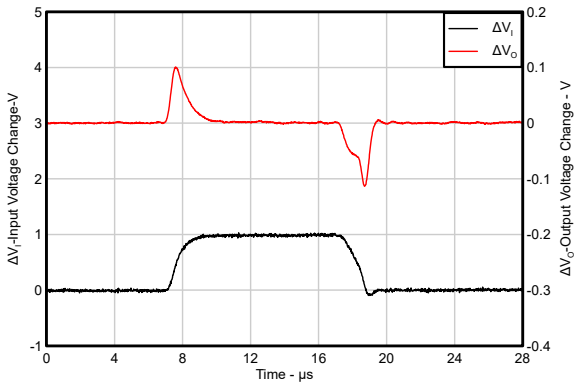



**Figure 7-3. Line Transient Response vs Time (Legacy Chip)**




$V_{IN}$ = 14.5V to 15.5V, $V_{OUT}$ = 1.25V, $I_L$ = 50mA, $C_{ADJ}$ = 0µF, $C_{OUT}$ = 0µF

**Figure 7-4. Line Transient Response vs Time (New Chip)**

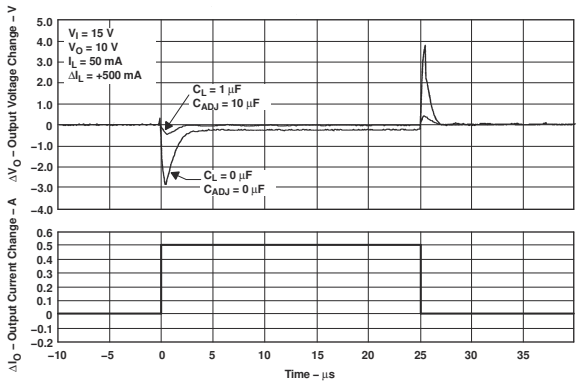
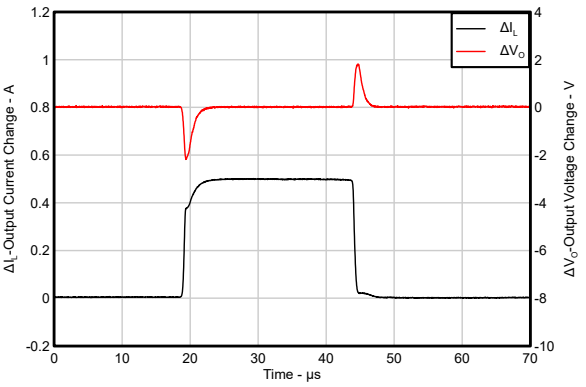
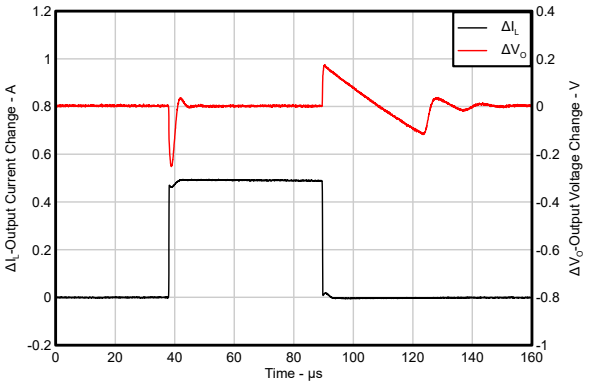



**Figure 7-5. Load Transient Response vs Time (Legacy Chip)**




$V_{IN}$ = 15V, $V_{OUT}$ = 1.25V, $I_L$ = 10mA to 500mA, $C_{ADJ}$ = 0µF, $C_{OUT}$ = 0µF

**Figure 7-6. Load Transient Response vs Time (New Chip)**




$V_{IN}$ = 15V, $V_{OUT}$ = 1.25V, $I_L$ = 10mA to 500mA, $C_{ADJ}$ = 10µF, $C_{OUT}$ = 1µF

**Figure 7-7. Load Transient Response vs Time (New Chip)**

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## 7.3 Power Supply Recommendations

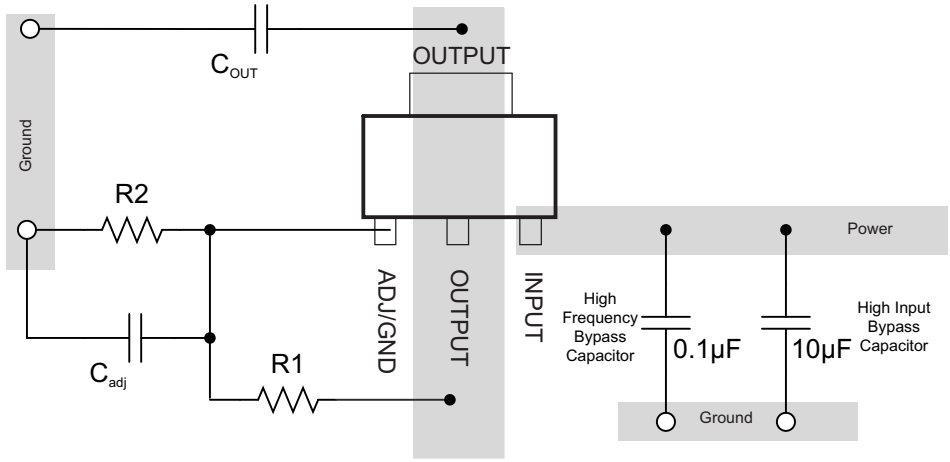
Keep trace widths large enough to eliminate problematic I×R voltage drops at the input and output pins. Place bypass capacitors as close to the device as possible. Additional copper and vias connected to ground facilitate additional thermal dissipation, preventing the device from reaching thermal overload.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

- Bypass the input pin to ground with a bypass capacitor.
- The optimum placement is closest to the VIN and GND pins of the device. Make sure to minimize the loop area formed by the bypass capacitor connection, the VIN pin, and the GND pin of the device.
- For operation at full-rated load, use wide trace lengths to eliminate IR drop and heat dissipation.

### *7.4.2 Layout Example*





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# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Development Support*

#### 8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the UA78L. Request the LM317MEVM (and related user guide) at the Texas Instruments website through the product folders or purchase directly from the TI eStore.

### *8.1.2 Device Nomenclature*

**Table 8-1. Available Options**

| PRODUCT[1] | DESCRIPTION |
|---|---|
| LM317M**Q***yyyz*<br>LM317M**QDCY***z* ***M3*****Q1** | **Q** indicates that the device is a grade-1 device in accordance with the AEC-Q100 standard.<br>**yyy** is the package designator.<br>**z** is the package quantity.<br>Devices either ship with the legacy chip (CSO: SFB) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the document. **M3** is a suffix designator only significant for the new chip with CSO:RFB, which uses the latest manufacturing flow |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

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## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision Q (July 2025) to Revision R (April 2026) | Page |
|---|---|
| • Added details about AEC-Q100 qualification for LM317MQ in Features section | 1 |
| • Updated *Description* section for better readability and corrected pin-count for SOT-223 package | 1 |
| • Corrected maximum input to output differential from 40V to 37V | 1 |
| • Corrected maximum input to output differential from 40V to 37V | 3 |
| • Corrected pin-count for SOT-223 (DCY) package | 4 |
| • Added test conditions used to capture typical characterisitcs plots | 6 |
| • Updated *Overview* section for better readability | 10 |
| • Added details about **M3** devices in *Device Nomenclature* section | 19 |

| Changes from Revision P (February 2014) to Revision Q (July 2025) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Deleted KTP package and information from document | 1 |
| • Changed entire document to align with current family format | 1 |
| • Added new silicon (M3) devices to document | 1 |
| • Added new silicon curves to *Typical Characteristics* section | 1 |
| • Added *Current Limit* section | 10 |
| • Changed *LM317M* to *LM317M and LM317MQ* in *Protection Diodes* section | 14 |
| • Changed *Power Supply Recommendations* section | 18 |
| • Added *Device Nomenclature* section | 19 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM317MDCY | Active | Production | SOT-223 (DCY) \| 4 | 80 \| TUBE | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | L4 |
| LM317MDCY.A | Active | Production | SOT-223 (DCY) \| 4 | 80 \| TUBE | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | L4 |
| LM317MDCYG3 | Active | Production | SOT-223 (DCY) \| 4 | 80 \| TUBE | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | L4 |
| LM317MDCYR | Active | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | L4 |
| LM317MDCYR.A | Active | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | L4 |
| LM317MDCYRG3 | Active | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | L4 |
| LM317MDCYRM3 | Active | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | L5 |
| LM317MKVURG3 | Active | Production | TO-252 (KVU) \| 3 | 2500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | LM317M |
| LM317MKVURG3.A | Active | Production | TO-252 (KVU) \| 3 | 2500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | LM317M |
| LM317MQDCYR | Active | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-2-260C-1 YEAR | -40 to 125 | L5 |
| LM317MQDCYR.A | Active | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | L5 |
| LM317MQDCYRG4 | NRND | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | L5 |
| LM317MQDCYRG4.A | NRND | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | L5 |
| LM317MQDCYRM3Q1 | Active | Production | SOT-223 (DCY) \| 4 | 2500 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | L5 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

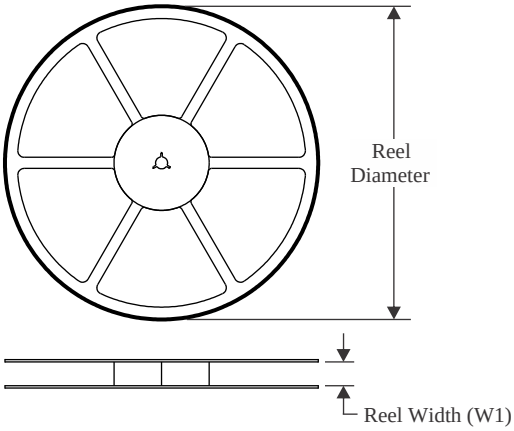
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

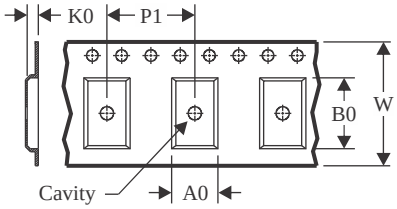
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

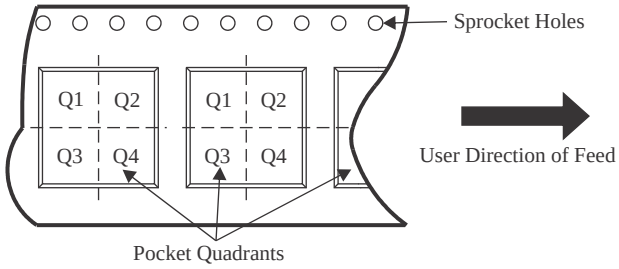



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

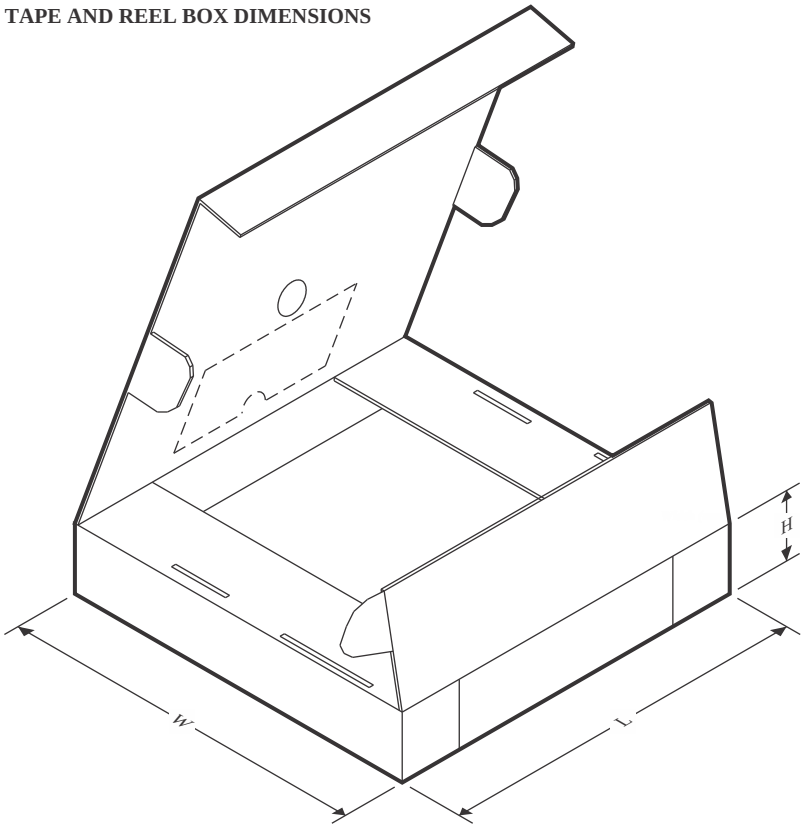
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM317MDCYR | SOT-223 | DCY | 4 | 2500 | 330.0 | 12.4 | 7.05 | 7.4 | 1.9 | 8.0 | 12.0 | Q3 |
| LM317MDCYR | SOT-223 | DCY | 4 | 2500 | 330.0 | 12.4 | 6.55 | 7.25 | 1.9 | 8.0 | 12.0 | Q3 |
| LM317MDCYRM3 | SOT-223 | DCY | 4 | 2500 | 330.0 | 12.4 | 7.05 | 7.4 | 1.9 | 8.0 | 12.0 | Q3 |
| LM317MKVURG3 | TO-252 | KVU | 3 | 2500 | 330.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |
| LM317MQDCYR | SOT-223 | DCY | 4 | 2500 | 330.0 | 12.4 | 7.05 | 7.4 | 1.9 | 8.0 | 12.0 | Q3 |
| LM317MQDCYR | SOT-223 | DCY | 4 | 2500 | 330.0 | 12.4 | 6.83 | 7.42 | 1.88 | 8.0 | 12.0 | Q3 |
| LM317MQDCYRG4 | SOT-223 | DCY | 4 | 2500 | 330.0 | 12.4 | 6.83 | 7.42 | 1.88 | 8.0 | 12.0 | Q3 |
| LM317MQDCYRM3Q1 | SOT-223 | DCY | 4 | 2500 | 330.0 | 12.4 | 7.05 | 7.4 | 1.9 | 8.0 | 12.0 | Q3 |

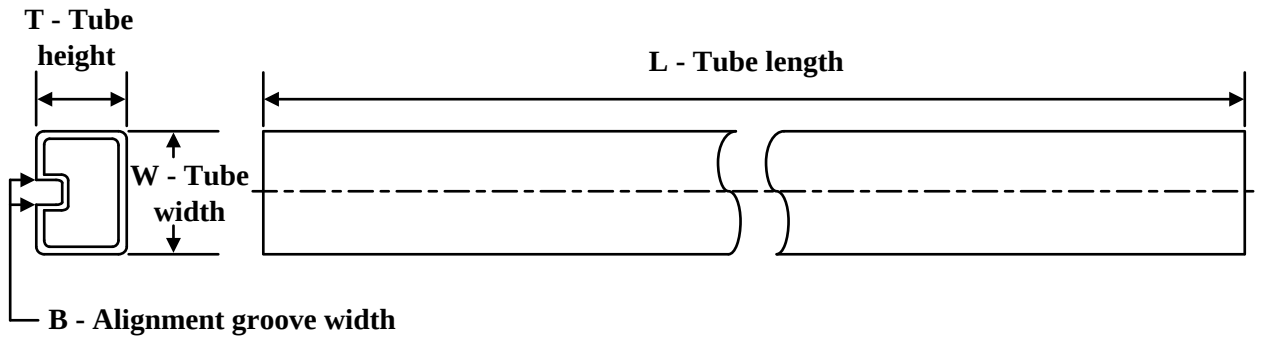
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM317MDCYR | SOT-223 | DCY | 4 | 2500 | 340.0 | 340.0 | 38.0 |
| LM317MDCYR | SOT-223 | DCY | 4 | 2500 | 336.0 | 336.0 | 48.0 |
| LM317MDCYRM3 | SOT-223 | DCY | 4 | 2500 | 340.0 | 340.0 | 38.0 |
| LM317MKVURG3 | TO-252 | KVU | 3 | 2500 | 340.0 | 340.0 | 38.0 |
| LM317MQDCYR | SOT-223 | DCY | 4 | 2500 | 340.0 | 340.0 | 38.0 |
| LM317MQDCYR | SOT-223 | DCY | 4 | 2500 | 346.0 | 346.0 | 29.0 |
| LM317MQDCYRG4 | SOT-223 | DCY | 4 | 2500 | 346.0 | 346.0 | 29.0 |
| LM317MQDCYRM3Q1 | SOT-223 | DCY | 4 | 2500 | 340.0 | 340.0 | 38.0 |

## TUBE



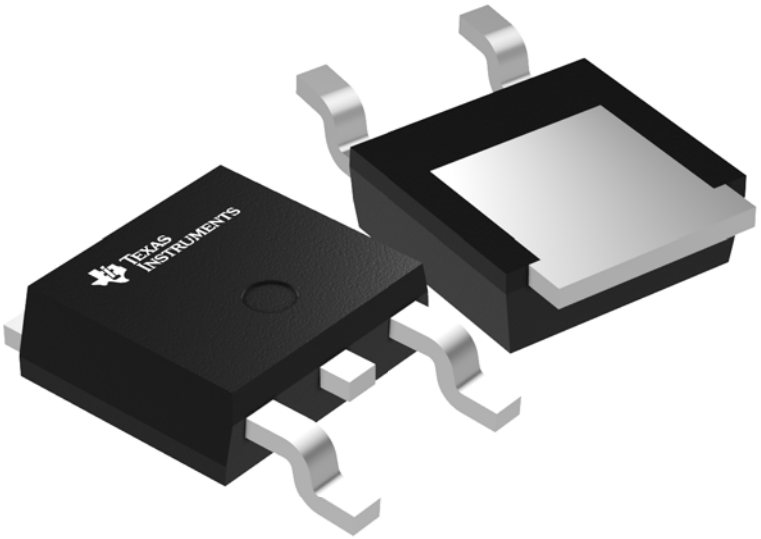

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM317MDCY | DCY | SOT-223 | 4 | 80 | 559 | 8.6 | 500 | 3.6 |
| LM317MDCY.A | DCY | SOT-223 | 4 | 80 | 559 | 8.6 | 500 | 3.6 |
| LM317MDCYG3 | DCY | SOT-223 | 4 | 80 | 559 | 8.6 | 500 | 3.6 |

# KVU 3

# TO-252 - 2.52 mm max height

TRANSISTOR OUTLINE



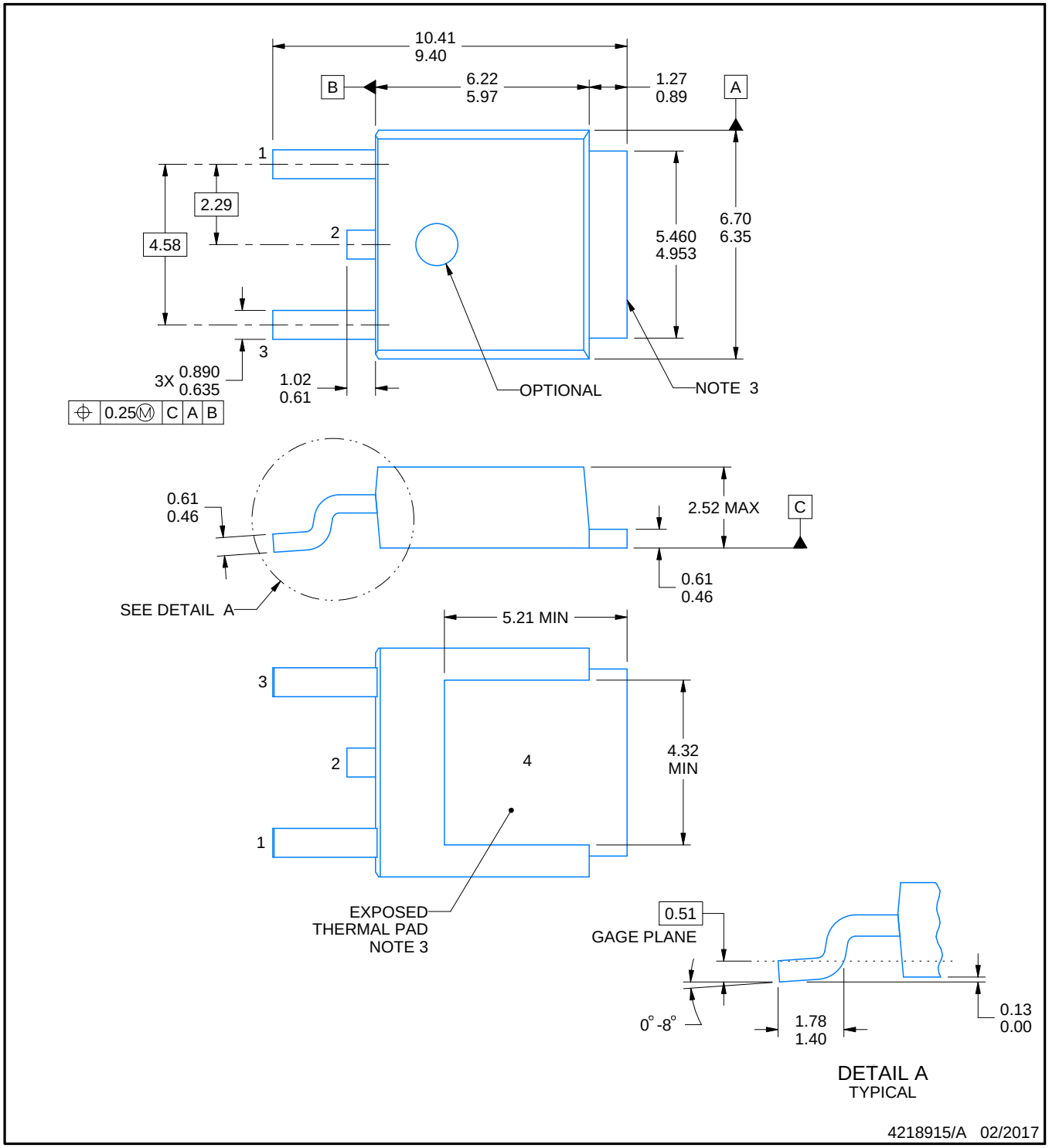

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## KVU0003A

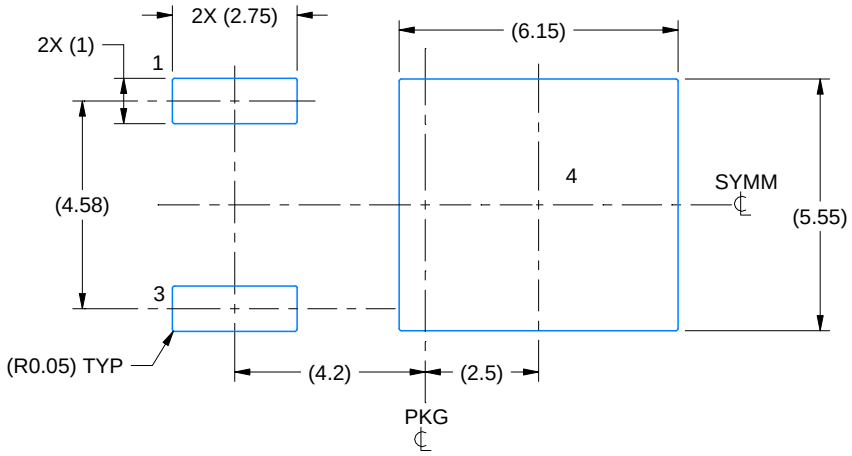
## TO-252 - 2.52 mm max height

TO-252

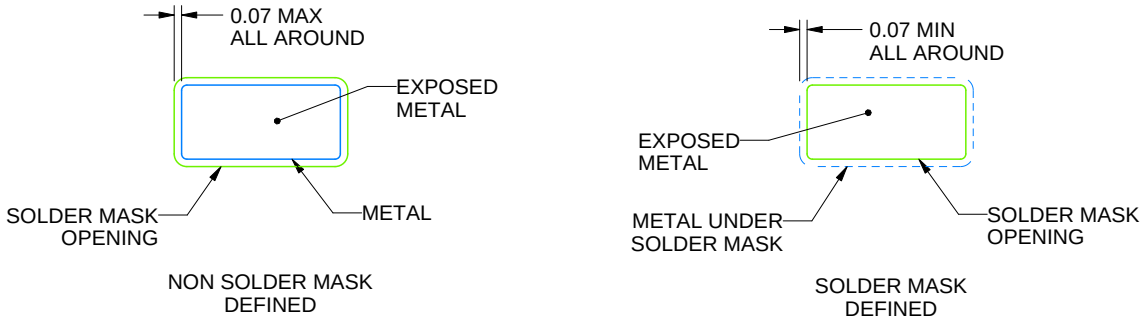



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X




SOLDER MASK DETAILS
NOT TO SCALE

4218915/A 02/2017

NOTES: (continued)

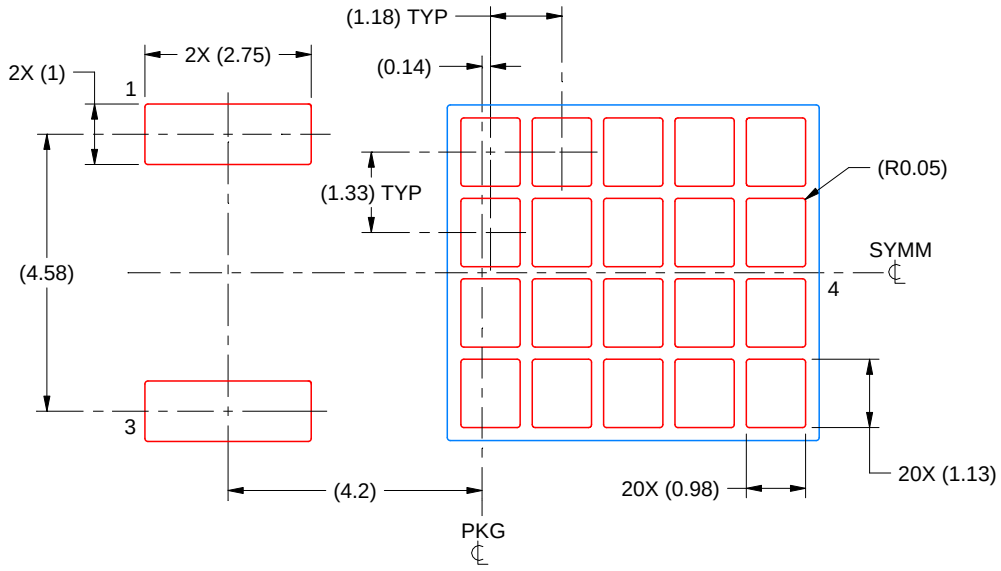
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## KVU0003A

## TO-252 - 2.52 mm max height

TO-252




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A 02/2017

NOTES: (continued)

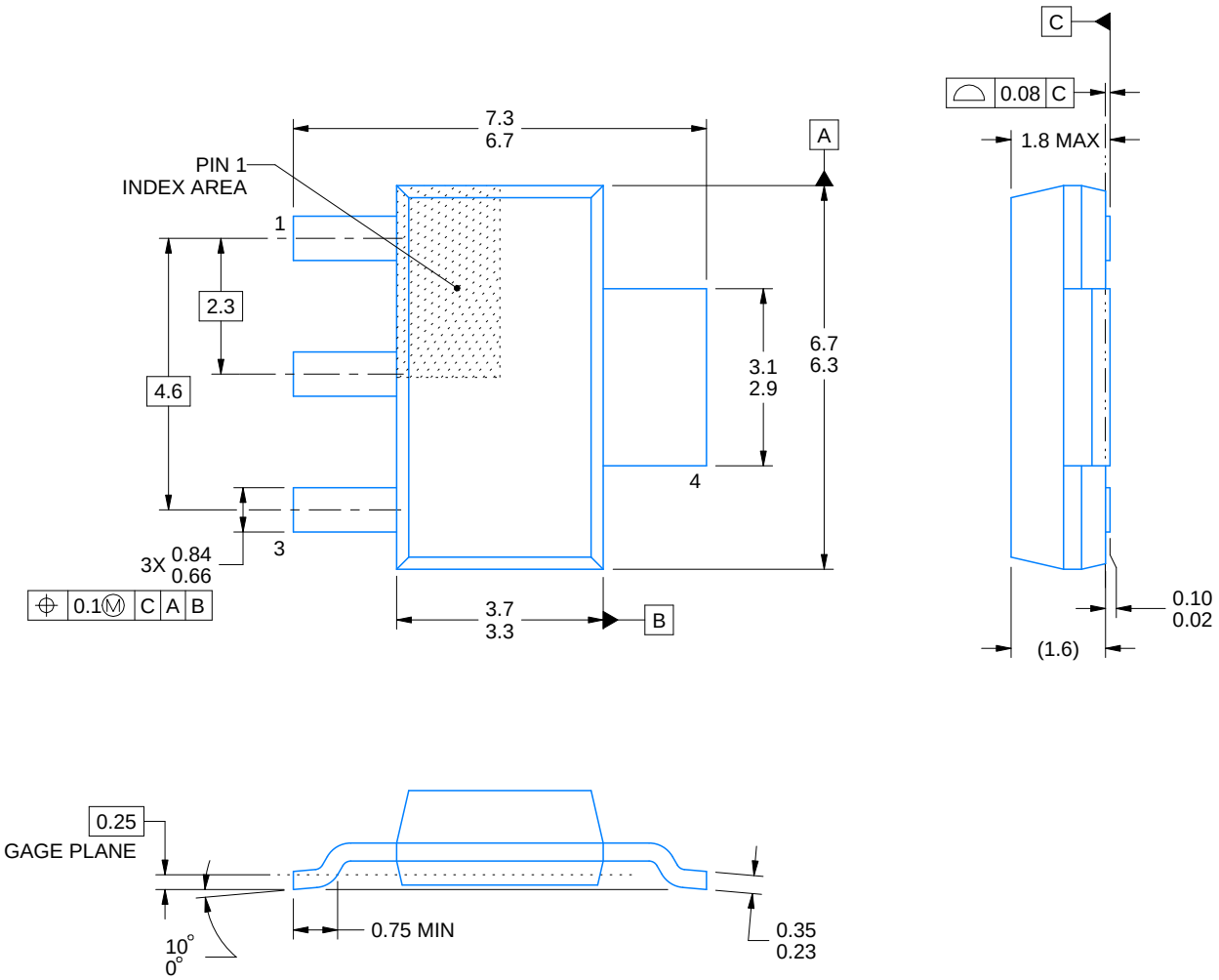
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DCY0004A

## SOT-223 - 1.8 mm max height

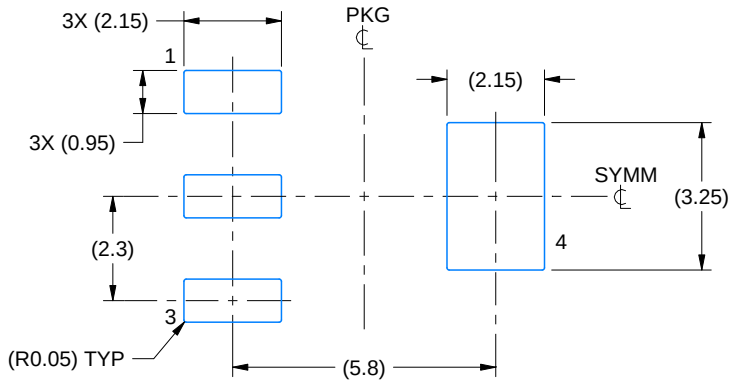
PLASTIC SMALL OUTLINE



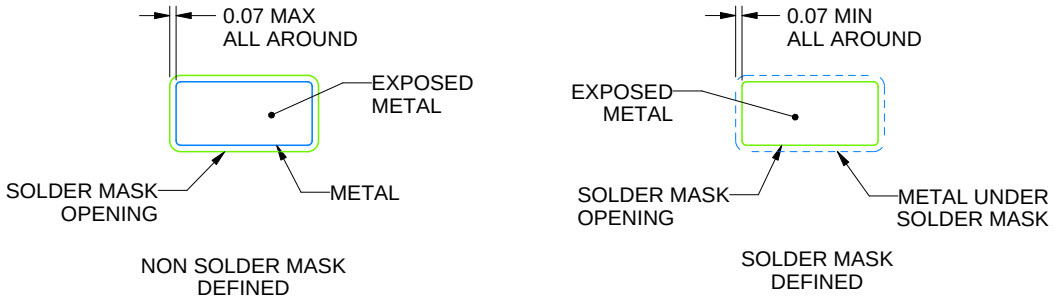

4214843/C 05/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC TO-261.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X




SOLDER MASK DETAILS

4214843/C 05/2026

NOTES: (continued)

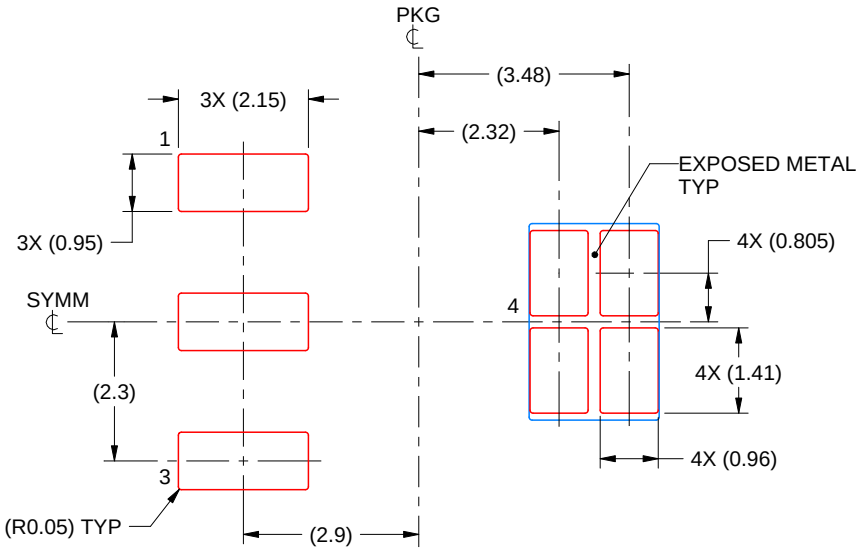
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DCY0004A

## SOT-223 - 1.8 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4214843/C 05/2026

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