TEXAS INSTRUMENTS
TPS61099
SLVSD88L – JULY 2016 – REVISED AUGUST 2021

TPS61099x Synchronous Boost Converter with Ultra-Low Quiescent Current

1 Features

- 600-nA ultra-low I_Q into V_{OUT} pin
- 400-nA ultra-low I_Q into V_{IN} pin
- Operating input voltage from 0.7 V to 5.5 V
- Adjustable output voltage from 1.8 V to 5.5 V
- Fixed output voltage versions available
- Minimum 0.8-A switch peak current limit
- Regulated output voltage in down mode
- True disconnection during shutdown
- Up to 75% efficiency at 10-µA load with fixed output voltage versions
- Up to 93% efficiency from 10-mA to 300-mA load
- 6-ball 1.23-mm × 0.88-mm WCSP package and 2-mm × 2-mm WSON package
- Create a custom design using the TPS61099x with the WEBENCH® Power Designer

2 Applications

- Memory LCD bias
- Optical heart rate monitor LED bias
- Wearable applications
- Low-power wireless applications
- Portable products
- Battery powered systems

3 Description

The TPS61099x device is a synchronous boost converter with 1-µA ultra-low quiescent current. The device is designed for products powered by an alkaline battery, NiMH rechargeable battery, Li-Mn battery, or rechargeable Li-Ion battery where high efficiency under light-load condition is critical to achieve long battery life operation.

The TPS61099x boost converter uses a hysteretic control topology to obtain maximal efficiency at minimal quiescent current. It only consumes 1-µA quiescent current under light-load condition and can achieve up to 75% efficiency at 10-µA load with fixed output voltage version. It can also support up to 300-mA output current from 3.3-V to 5-V conversion, and achieve up to 93% at 200-mA load.

The TPS61099x also offers both Down mode and Pass-Through operations for different applications. In Down mode, the output voltage can still be regulated at target value even when input voltage is higher than the output voltage. In Pass-Through mode, the output voltage follows input voltage. The TPS61099x exits Down mode and enters into Pass-Through mode when $V_{IN} > V_{OUT} + 0.5$ V.

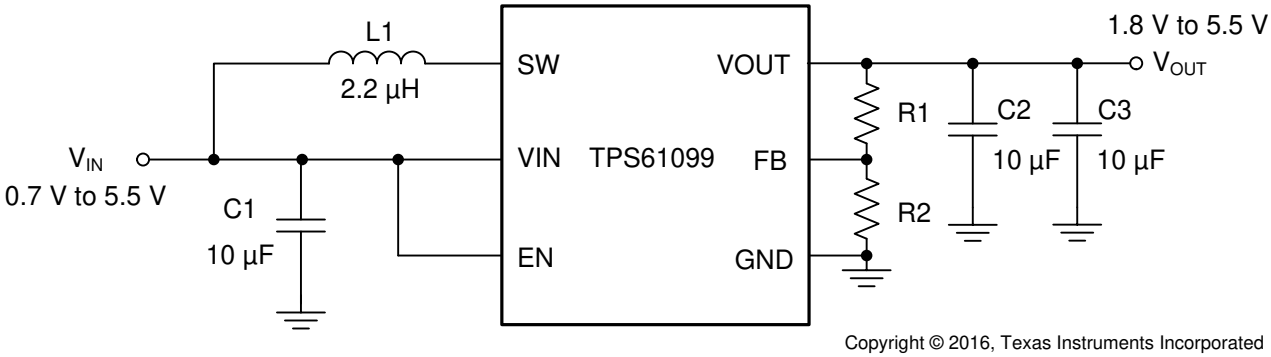
The TPS61099x supports true shutdown function when it is disabled, which disconnects the load from the input supply to reduce the current consumption.

The TPS61099x offers both adjustable output voltage version and fixed output voltage versions. It is available in a 6-ball 1.23-mm × 0.88-mm WCSP Package and a 6-pin 2-mm × 2-mm WSON package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS61099	WCSP (6)	1.23 mm × 0.88 mm
TPS61099x		
TPS61099	WSON(6)	2 mm × 2 mm
TPS61099x		

(1) For all available packages, see the orderable addendum at the end of this document.



Typical Application Circuit

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (May 2018) to Revision L (August 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document.	1

Changes from Revision J (October 2017) to Revision K (May 2018)	Page
• Added Load Efficiency graph for TPS610995 device	7

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE
TPS61099	Adjustable
TPS610997	5.0 V
TPS610996	4.5 V
TPS610995	3.6 V
TPS610994	3.3 V
TPS610993	3.0 V
TPS610992	2.5 V
TPS610991(1)	1.8 V

(1) Product Preview. Contact TI factory for more information.

6 Pin Configuration and Functions

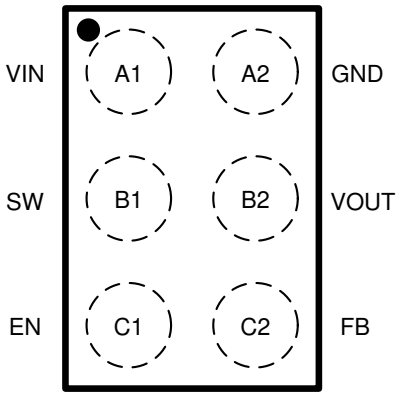


Figure 6-1. YFF Package 6-Pin YFF Top View

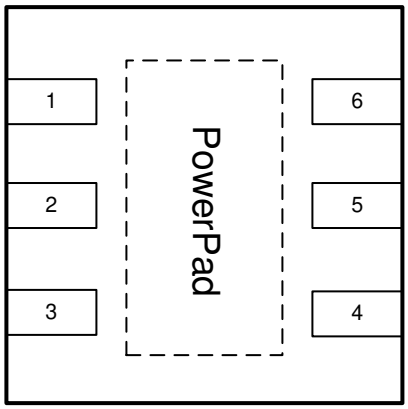


Figure 6-2. DRV Package 6-Pin DRV Top View

Table 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	YFF	DRV		
VIN	A1	6	I	IC power supply input
SW	B1	5	PWR	Switch pin of the converter. It is connected to the inductor
EN	C1	4	I	Enable logic input. Logic high voltage enables the device; logic low voltage disables the device. Do not leave it floating.
GND	A2	1	PWR	Ground
VOUT	B2	2	PWR	Boost converter output
FB	C2	3	I	Voltage feedback of adjustable output voltage. Connect to the center tap of a resistor divider to program the output voltage. Connect to GND pin for fixed output voltage versions.
PowerPad		7		Connect to GND

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals(2)	VIN, SW, VOUT, FB, EN	-0.3	6.0	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged Device Model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM rating allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM rating allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	0.7		5.5	V
V_{OUT}	Output voltage range	1.8		5.5	V
L	Inductor	0.7	2.2	2.86	µH
C_{IN}	Input capacitor	1.0	10		µF
C_{OUT}	Output capacitor	10	20	100	µF
T_J	Operating virtual junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61099		UNIT
		YFF (6 BALLS, WCSP)	DRV(6 PINS, WSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.4	71.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.9	83.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	33.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.2	33.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	14.4	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 0.7 V to 5.5 V. Typical values are at V_{IN} = 3.7 V, T_J = 25°C, unless otherwise noted.

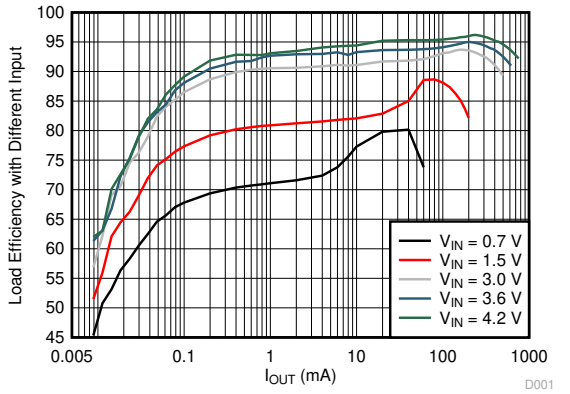
PARAMETER		Version	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{IN}	Input voltage range	TPS61099x		0.7		5.5	V
V_{UVLO}	Input under voltage lockout threshold	TPS61099x	V_{IN} rising		0.6	0.7	V
	UVLO hysteresis	TPS61099x			200		mV
I_Q	Quiescent current into VIN pin	TPS61099x	IC enabled, no Load, no Switching T_J = -40 °C to 85 °C		0.4	1.1	µA
	Quiescent current into VOUT pin	TPS61099x	IC enabled, no Load, no Switching, Boost or Down Mode T_J = -40 °C to 85 °C		0.6	1.5	µA
I_{SD}	Shutdown current into VIN pin	TPS61099x	IC disabled, V_{IN} = 3.7 V, V_{OUT} = 0 V T_J = -40 °C to 85 °C		0.5	1.6	µA
OUTPUT							
V_{OUT}	Output voltage range	TPS61099		1.8		5.5	V
Output accuracy		TPS610997	VIN < VOUT, PWM mode	4.90	5.00	5.10	V
			VIN < VOUT, PFM mode		5.15		V
		TPS610994	VIN < VOUT, PWM mode	3.23	3.30	3.37	
			VIN < VOUT, PFM mode		3.4		
		TPS610993	VIN < VOUT, PWM mode	2.94	3.0	3.06	V
			VIN < VOUT, PFM mode		3.1		
		TPS610996	VIN < VOUT, PWM mode	4.4	4.5	4.6	V
			VIN < VOUT, PFM mode		4.63		
		TPS610992	VIN < VOUT, PWM mode	2.45	2.5	2.55	V
			VIN < VOUT, PFM mode		2.58		
		TPS610995	VIN < VOUT, PWM mode	3.53	3.6	3.67	V
			VIN < VOUT, PFM mode		3.71		
V_{REF}	Feedback reference voltage	TPS61099	V_{IN} < V_{OUT}, PWM mode	0.98	1.00	1.02	V
		TPS61099	V_{IN} < V_{OUT}, PFM mode		1.03		V
V_{OVP}	Output overvoltage protection threshold	TPS61099x	V_{OUT} rising	5.6	5.8	6.0	V
	OVP hysteresis	TPS61099x			100	200	mV
I_{FB_LKG}	Leakage current into FB pin	TPS61099x	V_{FB} = 1.0 V		10	50	nA
POWER SWITCH							
$R_{DS(on)\_LS}$	Low side switch on resistance	TPS61099x	V_{OUT} = 5.0 V		250		mΩ
			V_{OUT} = 3.3 V		300		mΩ
			V_{OUT} = 1.8 V		400		mΩ
$R_{DS(on)\_HS}$	Rectifier on resistance	TPS61099x	V_{OUT} = 5.0 V		300	350	mΩ
			V_{OUT} = 3.3 V		350	450	mΩ
			V_{OUT} = 1.8 V		500	750	mΩ
I_{LH}	Inductor current ripple	TPS61099x	V_{OUT} = 5.0 V		350		mA
			V_{OUT} = 3.3 V		300		mA
			V_{OUT} = 1.8 V		250		mA
I_{LIM}	Current limit threshold	TPS61099x	V_{OUT} ≥ 2.5 V, boost operation	0.8	1	1.25	A
			V_{OUT} < 2.5 V, boost operation	0.5	0.75		A
I_{SW_LKG}	Leakage current into SW pin (from SW pin to GND)	TPS61099x	V_{SW} = 5.0 V, no switch, T_J = -40 °C to 85 °C			200	nA

7.5 Electrical Characteristics (continued)

T_J = -40°C to 125°C and V_{IN} = 0.7 V to 5.5 V. Typical values are at V_{IN} = 3.7 V, T_J = 25°C, unless otherwise noted.

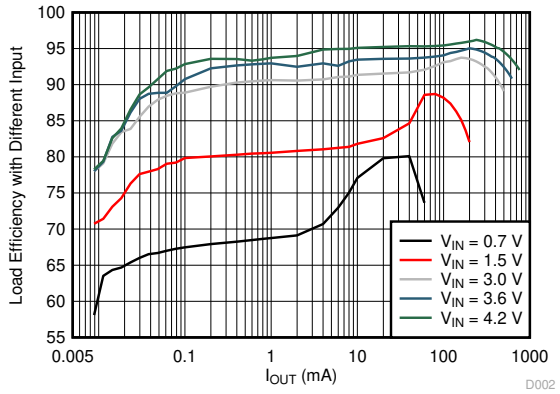
PARAMETER		Version	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL LOGIC							
V_{IL}	EN input low voltage threshold	TPS61099x	V_{IN} ≤ 1.5 V	0.2 x VIN			V
V_{IH}	EN input high voltage threshold	TPS61099x	V_{IN} ≤ 1.5 V			0.8 x VIN	V
V_{IL}	EN input low voltage threshold	TPS61099x	V_{IN} > 1.5 V	0.4			V
V_{IH}	EN input high voltage threshold	TPS61099x	V_{IN} > 1.5 V			1.2	V
I_{EN_LKG}	Leakage current into EN pin	TPS61099x	V_{EN} = 5.0 V			50	nA
	Overtemperature protection	TPS61099x			150		°C
	Overtemperature hysteresis	TPS61099x			25		°C

7.6 Typical Characteristics



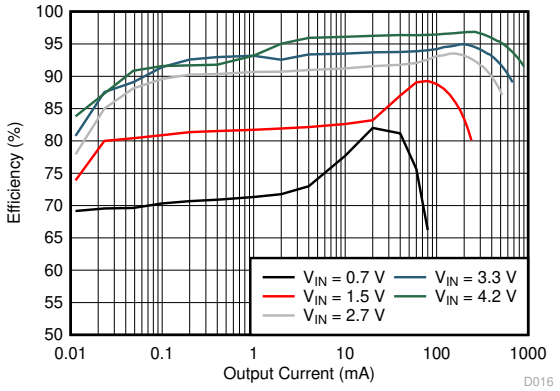
TPS61099, V_{IN} = 0.7 V, 1.5 V, 3.0 V, 3.6 V, 4.2 V, V_{OUT} = 5.0 V

Figure 7-1. TPS61099 Load Efficiency with Different Inputs



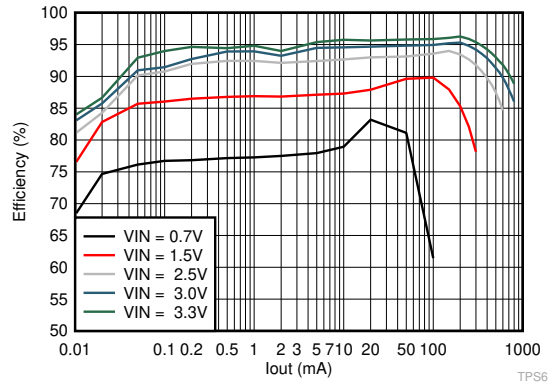
TPS610997, V_{IN}= 0.7 V, 1.5 V, 3.0 V, 3.6 V, 4.2 V

Figure 7-2. TPS610997 Load Efficiency with Different Inputs



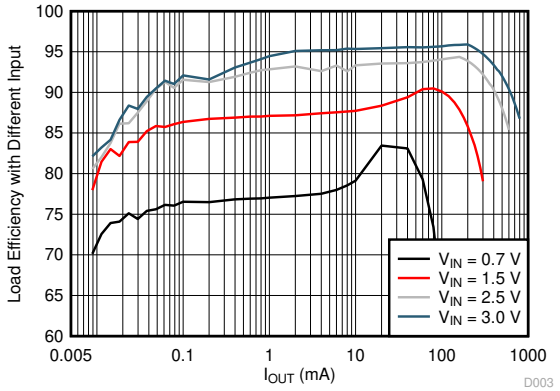
TPS610996, V_{IN}= 0.7 V, 1.5 V, 2.7, 3.3 V, 4.2 V

Figure 7-3. TPS610996 Load Efficiency with Different Inputs



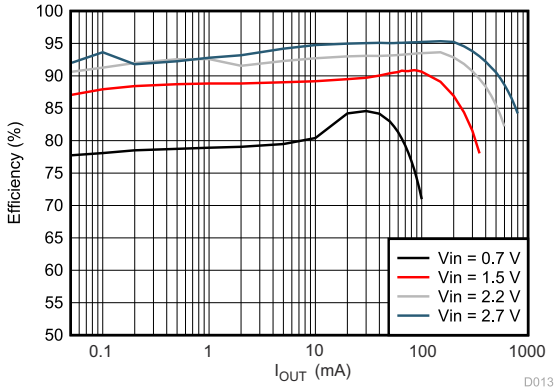
TPS610995, V_{IN}= 0.7 V, 1.5 V, 2.0, 3.0 V, 3.3 V

Figure 7-4. TPS610995 Load Efficiency with Different Inputs



TPS610994, V_{IN}= 0.7 V, 1.5 V, 2.5 V, 3.0 V

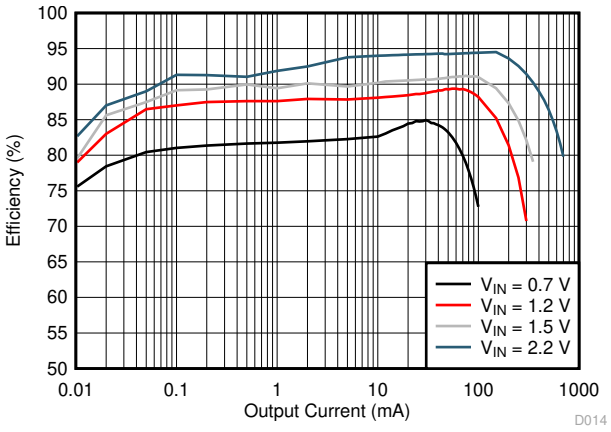
Figure 7-5. TPS610994 Load Efficiency with Different Inputs



TPS610993, V_{IN}= 0.7 V, 1.5 V, 2.2 V, 2.5 V

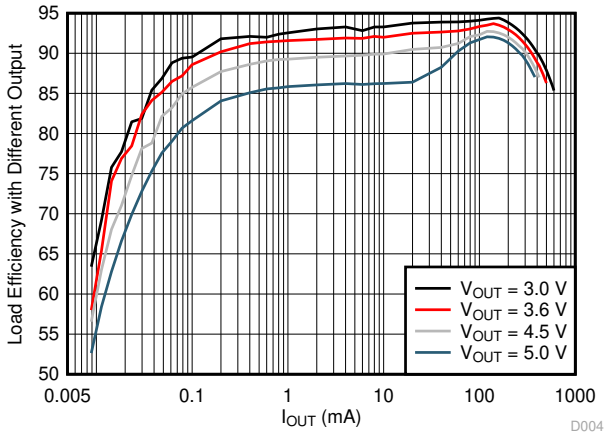
Figure 7-6. TPS610993 Load Efficiency with Different Inputs

7.6 Typical Characteristics (continued)



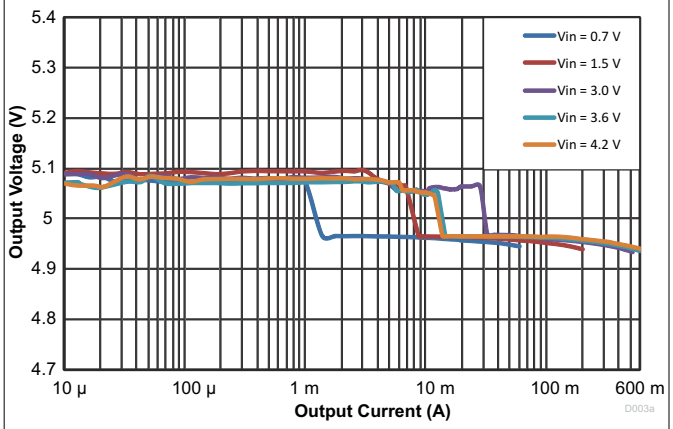
TPS610992, V_{IN}= 0.7 V, 1.2 V, 1.5 V, 2.2 V

Figure 7-7. TPS610992 Load Efficiency with Different Inputs



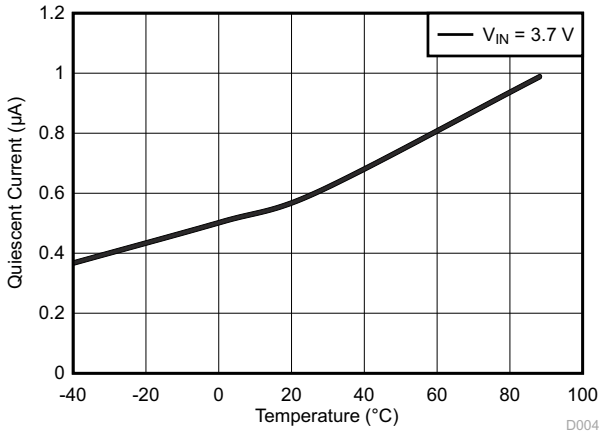
TPS61099, V_{IN} = 2.4 V, V_{OUT} = 3.0 V, 3.6 V, 4.5 V, 5.0 V

Figure 7-8. Load Efficiency with Different Outputs



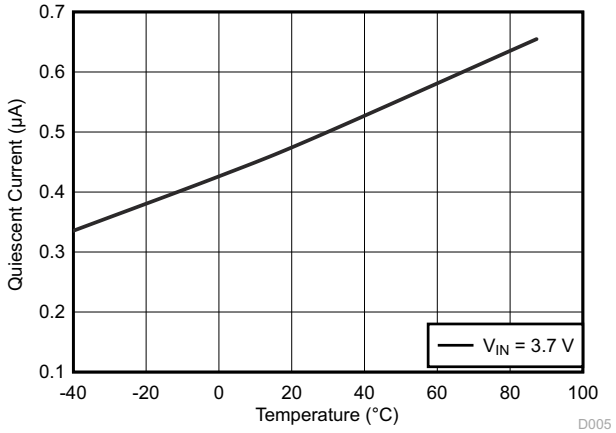
TPS61099, V_{IN} = 0.7 V, 1.5 V, 3.0 V, 3.6 V, 4.2 V, V_{OUT} = 5.0 V

Figure 7-9. Load Regulation



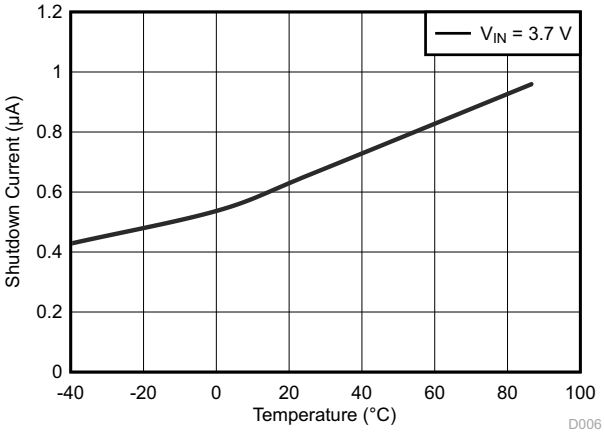
V_{IN} = 3.7 V No Switching

Figure 7-10. Quiescent Current into V_{OUT} vs Temperature



V_{IN} = 3.7 V No Switching

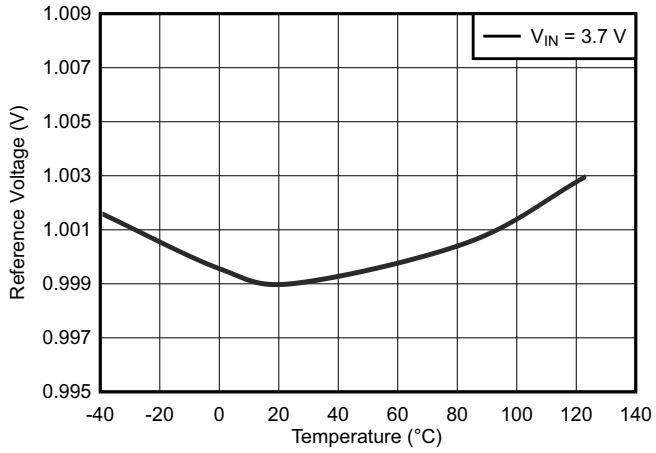
Figure 7-11. Quiescent Current into V_{IN} vs Temperature



V_{IN} = 3.7 V, Into V_{IN} and SW

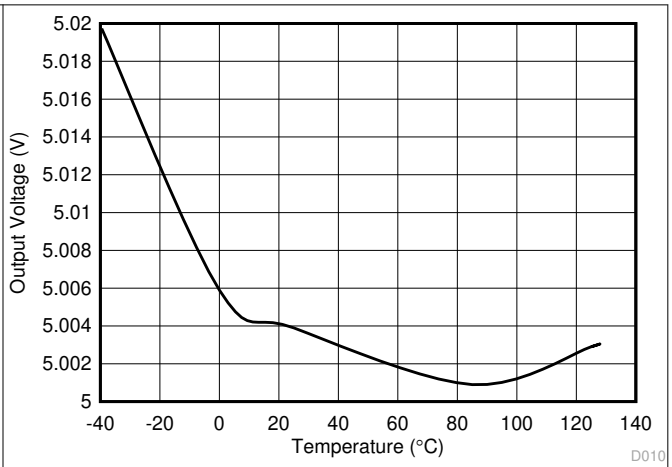
Figure 7-12. Shutdown Current vs Temperature

7.6 Typical Characteristics (continued)



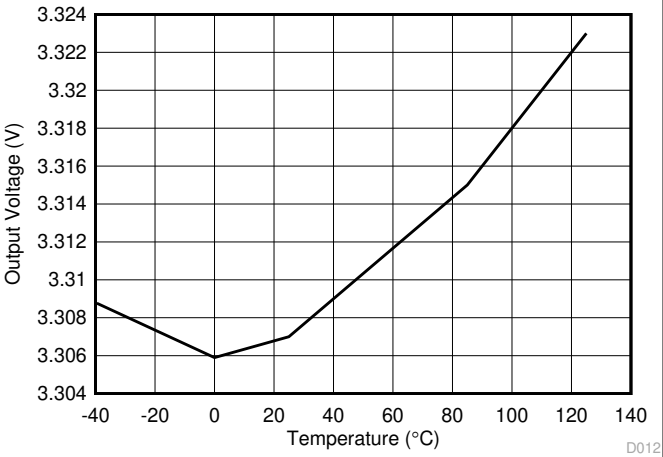
TPS61099, V_{IN} = 3.7 V T_J = –40°C to 125°C

Figure 7-13. Reference Voltage vs Temperature



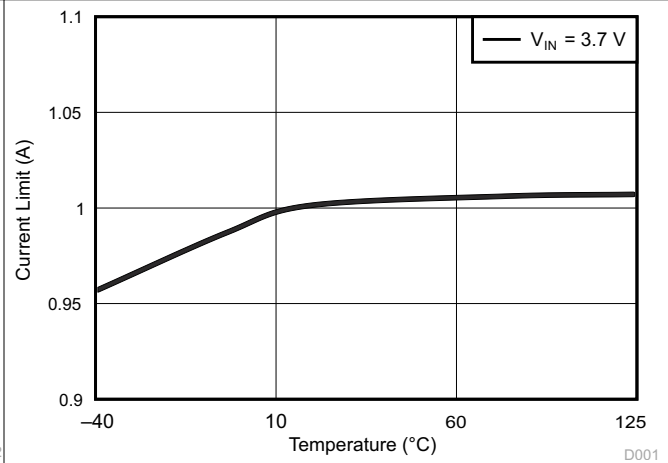
TPS610997, V_{IN}= 3.7 V, T_J = –40°C to 125°C

Figure 7-14. Output Voltage vs Temperature



TPS610994, V_{IN}= 2.5 V, T_J = –40°C to 125°C

Figure 7-15. TPS610994 Output Voltage vs Temperature



V_{IN} = 3.7 V T_J = –40°C to 125°C

Figure 7-16. Current Limit vs Temperature

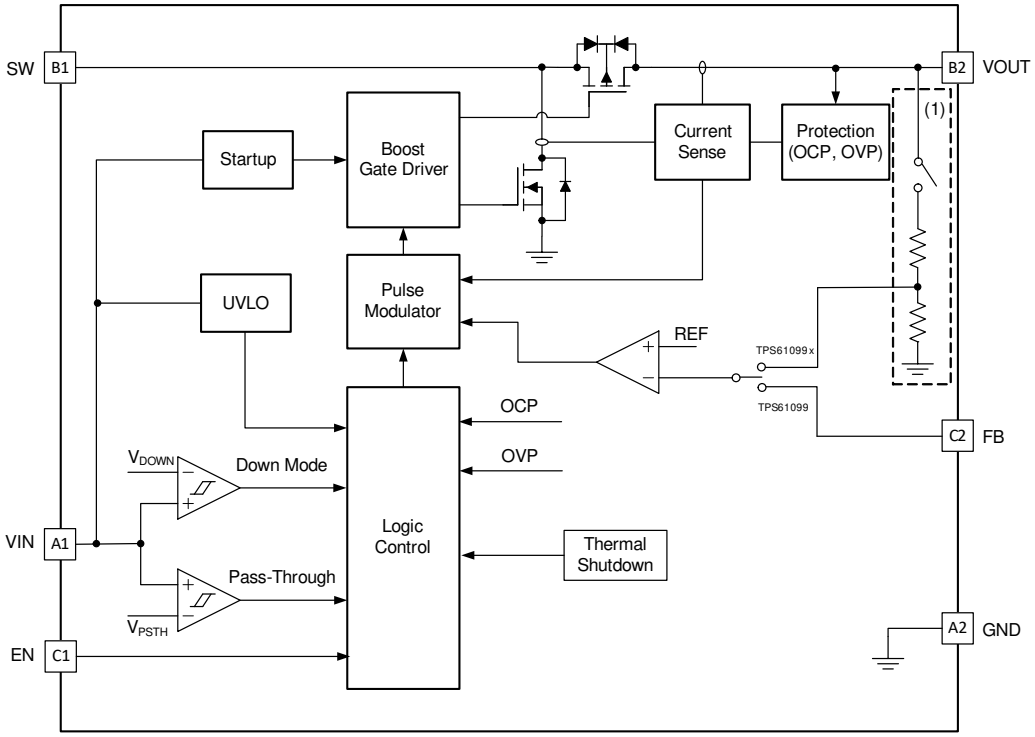
8 Detailed Description

8.1 Overview

The TPS61099x synchronous step-up converter is designed for alkaline battery, coin-cell battery, Li-ion or Li-polymer battery powered systems, which requires long battery running time and tiny solution size. The TPS61099x can operate with a wide input voltage from 0.7 V to 5.5 V. It only consumes 1 μA quiescent current and can achieve high efficiency under light load condition.

The TPS61099x operates in a hysteretic control scheme with typical 1-A peak switch current limit. The TPS61099x provides the true shutdown function and the load is completely disconnected from the input so as to minimize the leakage current. It also adopts Down Mode and Pass-Through operation when input voltage is close to or higher than the regulated output voltage. The TPS61099x family is available in both adjustable and fixed output voltage versions. Adjustable version offers programmable output voltage for flexible applications while fixed versions offer minimal solution size and achieve up to 75% high efficiency under 10-μA load.

8.2 Functional Block Diagram



A. Internal FB resistor divider is implemented in fixed output voltage versions.

Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Boost Controller Operation

The TPS61099x boost converter is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 300 mA and adjusting the offset of this inductor current depending on the output load. Since the input voltage, output voltage and inductor value all affect the rising and falling slopes of inductor ripple current, the switching frequency is not fixed and is determined by the operation condition. If the required average input current is lower than the average inductor current defined by this constant ripple, the inductor current goes discontinuously to keep the efficiency high under light load condition. Figure 8-2 illustrates the hysteretic current operation. If the load current is reduced further, the boost converter enters into Burst mode. In Burst mode, the boost converter ramps up the output voltage with several switching cycles. Once the output voltage exceeds a setting threshold, the device stops switching and goes into a sleep status. In sleep status, the device consumes less quiescent current. It resumes

switching when the output voltage is below the setting threshold. It exits the Burst mode when the output current can no longer be supported in this mode. Refer to Figure 8-3 for Burst mode operation details.

To achieve high efficiency, the power stage is realized as a synchronous boost topology. The output voltage V_{OUT} is monitored via an external or internal feedback network which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly.

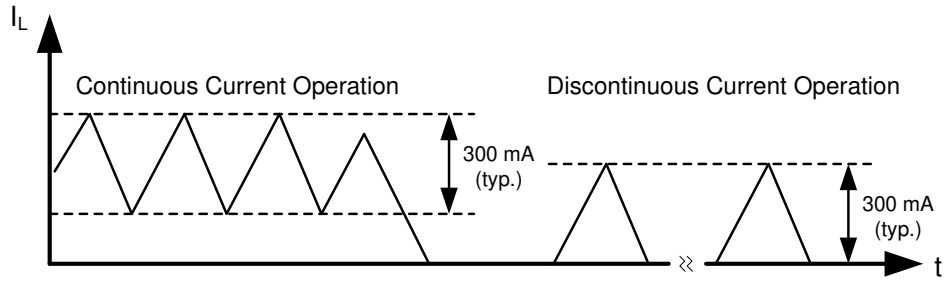


Figure 8-2. Hysteretic Current Operation

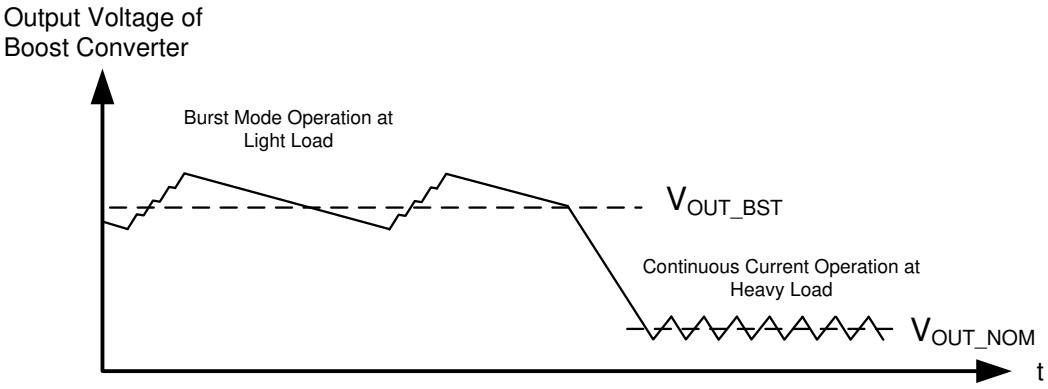


Figure 8-3. Burst Mode Operation

8.3.2 Under-Voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 0.4 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 0.6 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 0.4 V and 0.6 V.

8.3.3 Enable and Disable

When the input voltage is above UVLO rising threshold and the EN pin is pulled to high voltage, the TPS61099x is enabled. When the EN pin is pulled to low voltage, the TPS61099x goes into shutdown mode. In shutdown mode, the device stops switching and the rectifying PMOS fully turns off, providing the completed disconnection between input and output. Less than 0.5-µA input current is consumed in shutdown mode.

8.3.4 Soft Start

After the EN pin is tied to high voltage, the TPS61099x begins to startup. At the beginning, the device operates at the boundary of Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM), and the inductor peak current is limited to around 200 mA during this stage. When the output voltage is charged above approximately 1.6 V, the device starts the hysteretic current mode operation. The current limit threshold is gradually increasing to 0.7× I_{LIM} within 500 µs. In this way, the soft start function reduces the inrush current during startup. After V_{OUT} reaches the target value, soft start stage ends and the peak current is now determined by the output of an internal error amplifier which compares the feedback of the output voltage and the internal reference voltage.

The TPS61099x is able to start up with 0.7-V input voltage with larger than 3-kΩ load. However, if the load during startup is so heavy that the TPS61099x fails to charge the output voltage above 1.6 V, the TPS61099x can't start up successfully until the input voltage is increased or the load current is reduced. The startup time depends on input voltage and load current.

8.3.5 Current Limit Operation

The TPS61099x employs cycle-by-cycle over-current protection (OCP) function. If the inductor peak current reaches the current limit threshold I_{LIM}, the main switch turns off so as to stop further increase of the input current. In this case the output voltage will decrease until the power balance between input and output is achieved. If the output drops below the input voltage, the TPS61099x enters into Down Mode. The peak current is still limited by I_{LIM} cycle-by-cycle in Down Mode. If the output drops below 1.6 V, the TPS61099 enters into startup process again. In Pass-Through operation, current limit function is not enabled.

8.3.6 Output Short-to-Ground Protection

The TPS61099x starts to limit the switch current to 200 mA when the output voltage is below 1.6 V. If short-to-ground condition occurs, switch current is limited at 200 mA. Once the short circuit is released, the TPS61099x goes back to soft start again and regulates the output voltage.

8.3.7 Over Voltage Protection

TPS61099x has an output over-voltage protection (OVP) to protect the device in case that the external feedback resistor divider is wrongly populated. When the output voltage of the TPS61099 exceeds the OVP threshold of 5.8 V, the device stops switching. Once the output voltage falls 0.1 V below the OVP threshold, the device starts operating again.

8.3.8 Down Mode Regulation and Pass-Through Operation

The TPS61099x features Down Mode and Pass-Through operation when input voltage is close to or higher than output voltage.

In the Down Mode, output voltage is regulated at target value even when $V_{IN} > V_{OUT}$. The control circuit changes the behavior of the rectifying PMOS by pulling its gate to input voltage instead of to ground. In this way, the voltage drop across the PMOS is increasing as high as to regulate the output voltage. The power loss also increases in this mode, which needs to be taken into account for thermal consideration.

In the Pass-Through operation, the boost converter stops switching. The rectifying PMOS constantly turns on and low side switch constantly turns off. The output voltage is the input voltage minus the voltage drop across the dc resistance (DCR) of the inductor and the on-resistance of the rectifying PMOS.

With V_{IN} ramping up, the TPS61099x goes into Down Mode first when $V_{IN} > V_{OUT}$ – 50mV. It stays in Down Mode until $V_{IN} > V_{OUT}$ + 0.5 V and then goes automatically into Pass-Through operation. In the Pass-Through operation, output voltage follows input voltage. The TPS61099x exits Pass-Through Mode and goes back to Down Mode when V_{IN} ramps down to 103% of the target output voltage. It stays in Down Mode until input voltage falls 100mV below the output voltage, returning to Boost operation.

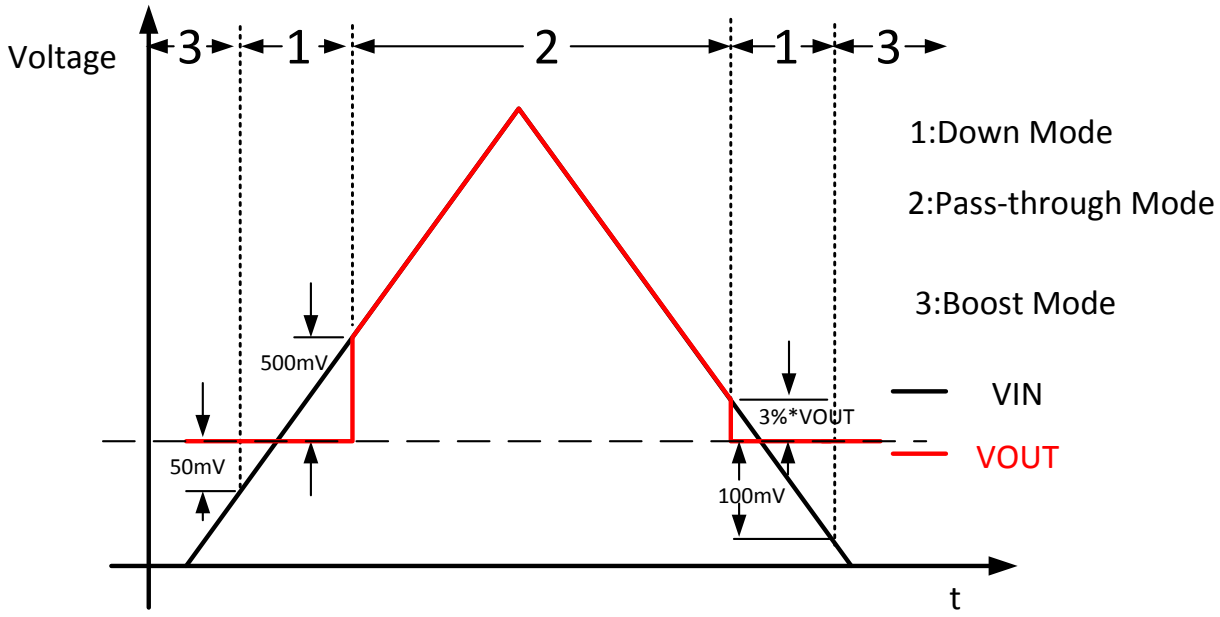


Figure 8-4. Down Mode and Pass-Through Operation

8.3.9 Thermal Shutdown

The TPS61099x has a built-in temperature sensor which monitors the internal junction temperature in boost mode operation. If the junction temperature exceeds the threshold 150°C, the device stops operating. As soon as the junction temperature drops below the shutdown temperature minus the hysteresis, typically 125°C, it starts operating again.

8.4 Device Functional Modes

8.4.1 Burst Mode Operation under Light Load Condition

The boost converter of TPS61099x enters into Burst Mode operation under light load condition. Refer to *Boost Controller Operation* for details.

8.4.2 Down Mode Regulation and Pass-Through Mode Operation

The boost converter of TPS61099x automatically enters into Down Mode or pass-through mode operation when input voltage is higher than the target output voltage. Refer to *Down Mode Regulation and Pass-Through Operation* for details.

9 Application and Implementation

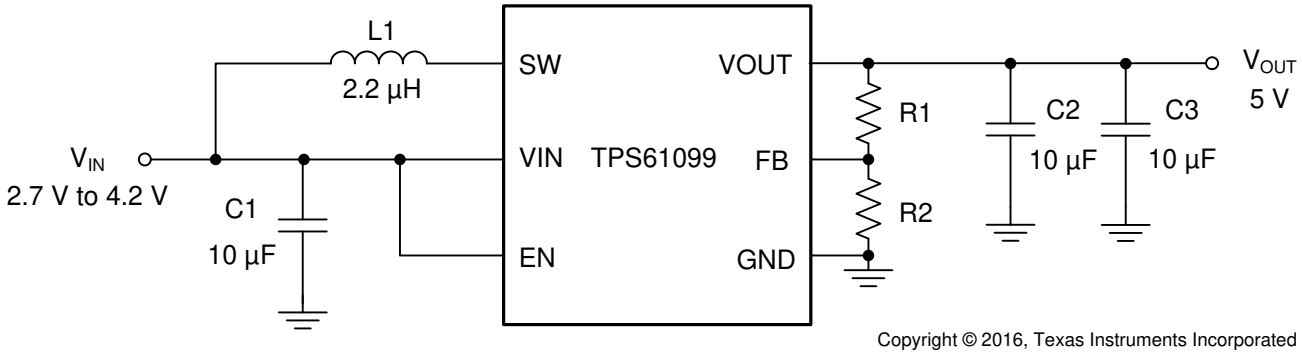
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS61099x is a synchronous boost converter designed to operate at a wide input voltage from 0.7 V to 5.5 V with 1-A peak switch current limit. The device adopts a hysteretic control scheme so the operating frequency is not a constant value, which varies with different input/output voltages and inductor values. It only consumes 1-µA quiescent current under light load condition. It also supports true shutdown to disconnect the load from the input in order to minimize the leakage current. Therefore, it is very suitable for alkaline battery, coin-cell battery, Li-ion or Li-polymer battery powered systems to extend the battery running time.

9.2 Typical Application - 5 V Output Boost Converter



9.2.1 Design Requirements

A typical application example is the memory LCD, which normally requires 5-V output as its bias voltage and only consumes less than 1 mA current. The following design procedure can be used to select external component values for the TPS61099x.

Table 9-1. Design Requirements

PARAMETERS	VALUES
Input Voltage	2.7 V ~ 4.2 V
Output Voltage	5 V
Output Current	1 mA
Output Voltage Ripple	± 50 mV

9.2.1.1 Detailed Design Procedure

9.2.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61099 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance

- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.1.2 Programming the Output Voltage

There are two ways to set the output voltage of the TPS61099x. For adjustable output voltage version, select the external resistor divider R1 and R2, as shown in Equation 1, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is V_{REF} of 1.0 V.

$$V_{OUT} = V_{REF} \cdot \frac{R1 + R2}{R2} \tag{1}$$

For fixed output voltage versions, the FB pin should be connected to the GND. The TPS61099x offers diverse fixed voltage versions, refer to *Device Comparison Table* for version details.

In this example, 5-V output is required to bias the memory LCD. For the best accuracy, the current following through R2 should be 100 times larger than FB pin leakage current. Changing R2 towards a lower value increases the robustness against noise injection. Changing R2 towards higher values reduces the FB divider current for achieving the highest efficiency at low load currents. 1-MΩ and 249-kΩ resistors are selected for R1 and R2 in this example. High accuracy resistors are recommended for better output voltage accuracy.

9.2.1.1.3 Maximum Output Current

The maximum output capability of the TPS61099x is determined by the input to output ratio and the current limit of the boost converter. It can be estimated by Equation 2.

$$I_{OUT(max)} = \frac{V_{IN} \cdot (I_{LIM} - \frac{I_{LH}}{2}) \cdot \eta}{V_{OUT}} \tag{2}$$

where

- η is the conversion efficiency, use 85% for estimation
- I_{LH} is the current ripple value
- I_{LIM} is the switch current limit

Minimum input voltage, maximum boost output voltage and minimum current limit I_{LIM} should be used as the worst case condition for the estimation.

9.2.1.1.4 Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The TPS61099x is optimized to work with inductor values between 1 µH and 2.2 µH. For best stability consideration, a 2.2-µH inductor is recommended under Vout > 3.0V condition while choosing a 1-µH inductor for applications under Vout ≤ 3.0V condition. Follow Equation 3 and Equation 4 to calculate the inductor's peak current for the application. Depending on different load conditions, the TPS61099x works in continuous current mode or discontinuous mode. In different modes, the peak currents of the inductor are also different. Equation 3 provides an easy way to estimate whether the device works in CCM or DCM. As long as the Equation 3 is true, continuous current mode is typically established. Otherwise, discontinuous current mode is typically established.

$$\frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \times \eta} > \frac{I_{LH}}{2} \tag{3}$$

The inductor current ripple I_{LH} is fixed by design. Therefore, the peak inductor current is calculated with Equation 4.

$$I_{L,peak} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \times \eta} + \frac{I_{LH}}{2}; \quad \text{continuous current mode operation}$$
$$I_{L,peak} = I_{LH}; \quad \text{discontinuous current mode operation} \tag{4}$$

where

- $I_{L,peak}$ is the peak inductor current.

The inductor's saturation current must be higher than the calculated peak inductor current. Table 9-2 lists the recommended inductors for TPS61099x device.

After choosing the inductor, the estimated switching frequency *f* in continuous current mode can be calculated by Equation 5. The switching frequency is not a constant value, which is determined by L, V_{IN} and V_{OUT}.

$$f = \frac{V_{IN} \cdot (V_{OUT} - V_{IN} \cdot \eta)}{L \cdot I_{LH} \cdot V_{OUT}} \tag{5}$$

Table 9-2. List of Inductors

VOUT [V](1)	INDUCTANCE [µH]	SATURATION CURRENT [A]	DC RESISTANCE [mΩ]	SIZE (LxWxH)	PART NUMBER	MANUFACTURER
> 3.0	2.2	1.95	80	2.5 x 2.0 x 1.2	74404024022	Würth Elektronik
	2.2	1.7	92	2.5 x 2.0 x 1.1	LQH2HPN2R2MJR	muRata
	2.2	1.45	163	2.0 x 1.6 x 1.0	VLS201610CX-2R2M	TDK
≤ 3.0	1.0	2.6	37	2.5 x 2.0 x 1.2	74404024010	Würth Elektronik
	1.0	2.3	48	2.5 x 2.0 x 1.0	MLP2520W1R0MT0S1	TDK
	1.0	1.5	80	2.0 x 1.2 x 1.0	LQM21PN1R0MGH	muRata

(1) See *Third-Party Products* disclaimer

9.2.1.1.5 Capacitor Selection

For best output and input voltage filtering, low ESR X5R or X7R ceramic capacitors are recommended.

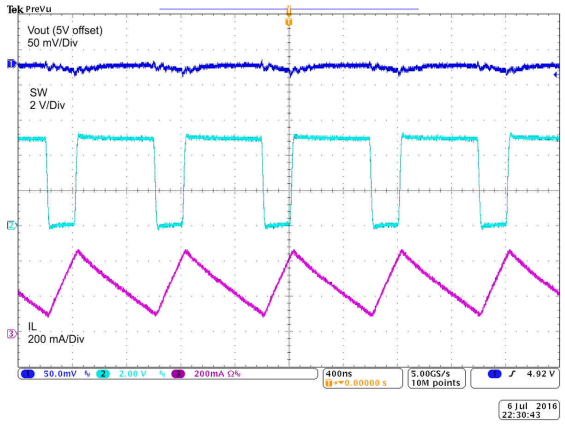
The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. An input capacitor value of 10 µF is normally recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

For the output capacitor of VOUT pin, small ceramic capacitors are recommended, placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, the use of a small ceramic capacitor with a capacitance value of 1 µF in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

From the power stage point of view, the output capacitor sets the corner frequency of the converter while the inductor creates a Right-Half-Plane-Zero. Consequently, with a larger inductor, a larger output capacitor must be used. The TPS61099x is optimized to work with the inductor from 1 µH to 2.2 µH, so the minimal output capacitor value is 20 µF (nominal value). Increasing the output capacitor makes the output ripple smaller in PWM mode.

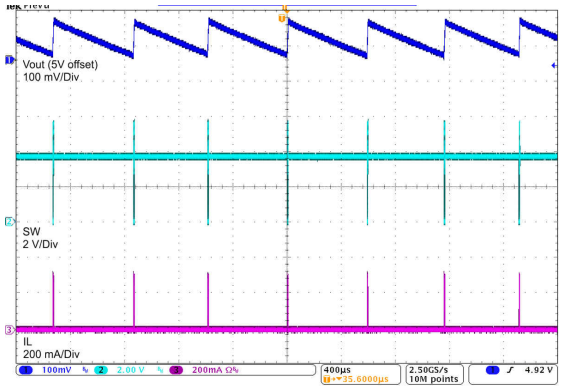
When selecting capacitors, ceramic capacitor's derating effect under bias should be considered. Choose the right nominal capacitance by checking capacitor's DC bias characteristics. In this example, GRM188R60J106ME84D, which is a 10-µF ceramic capacitor with high effective capacitance value at DC biased condition, is selected for V_{OUT} rail. The performance of TPS61099x is shown in *Application Curves* section.

9.2.1.2 Application Curves



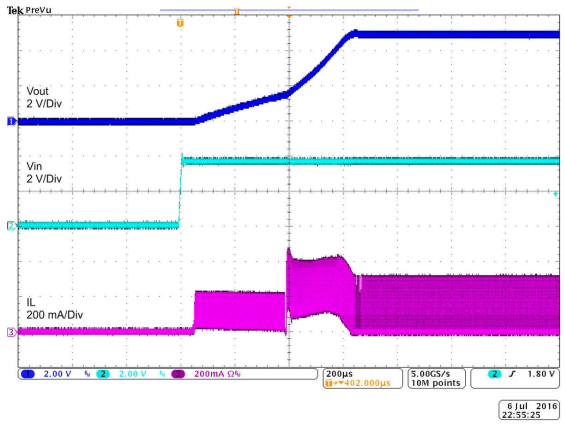
V_{IN} = 3.7 V V_{OUT} = 5 V I_{OUT} = 200 mA

Figure 9-1. Switching Waveform at Heavy Load



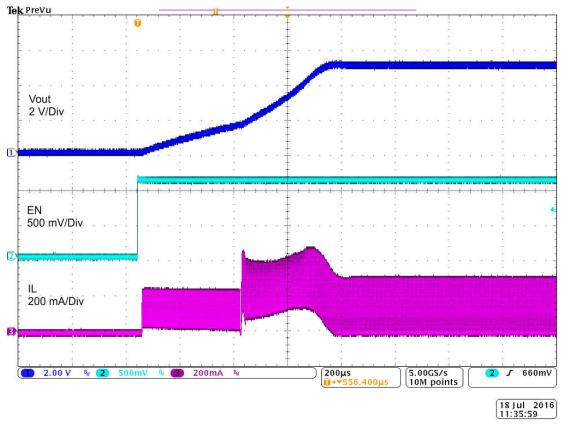
V_{IN} = 3.7 V V_{OUT} = 5 V I_{OUT} = 10 mA

Figure 9-2. Switching Waveform at Light Load



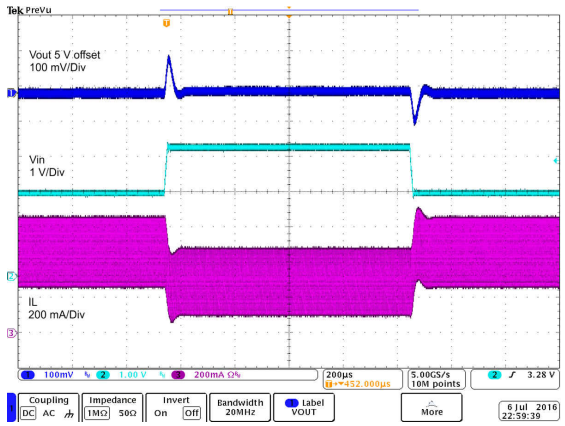
V_{IN} = 3.7 V V_{OUT} = 5 V I_{OUT} = 50 mA

Figure 9-3. Startup by V_{IN}



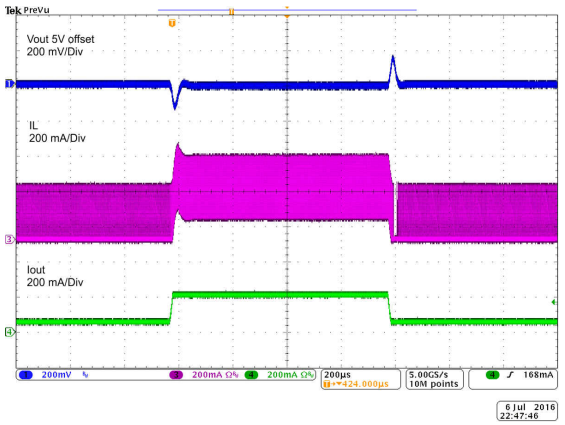
V_{IN} = 3.7 V V_{OUT} = 5 V I_{OUT} = 100 mA

Figure 9-4. Startup by EN



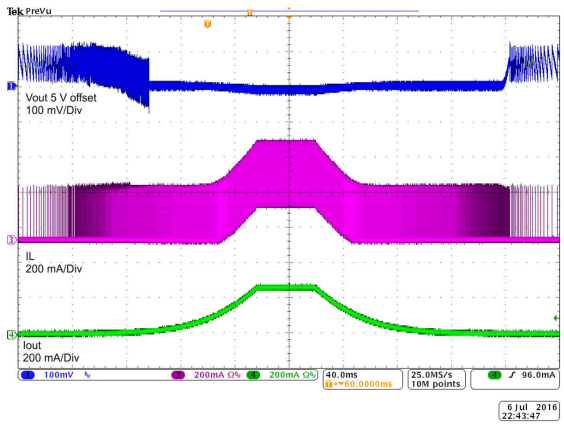
V_{IN} = 2.4 V to 3.7 V V_{OUT} = 5 V I_{OUT} = 200 mA

Figure 9-5. Line Transient



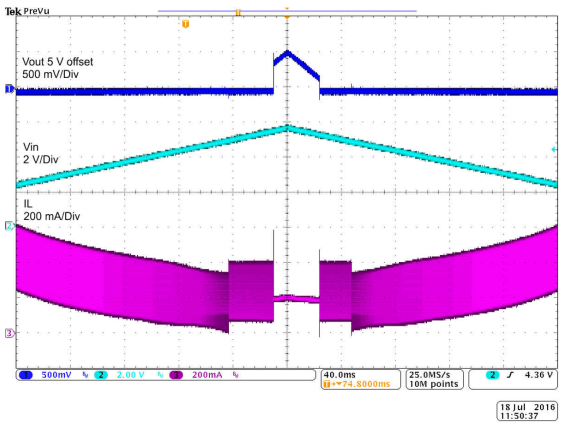
V_{IN} = 3.7 V V_{OUT} = 5 V I_{OUT} = 50 mA to 200 mA

Figure 9-6. Load Transient



V_{IN} = 3.7 V V_{OUT} = 5 V I_{OUT} = 0 mA to 250 mA

Figure 9-7. Load Regulation



V_{IN} = 2.4 to 5.5 V V_{OUT} = 5 V I_{OUT} = 200 mA

Figure 9-8. Line Regulation

10 Power Supply Recommendations

The TPS61099x family is designed to operate from an input voltage supply range between 0.7 V to 5.5 V. The power supply can be alkaline battery, NiMH rechargeable battery, Li-Mn battery or rechargeable Li-Ion battery. The input supply should be well regulated with the rating of TPS61099x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

11.2 Layout Example

The bottom layer is a large GND plane connected by vias.

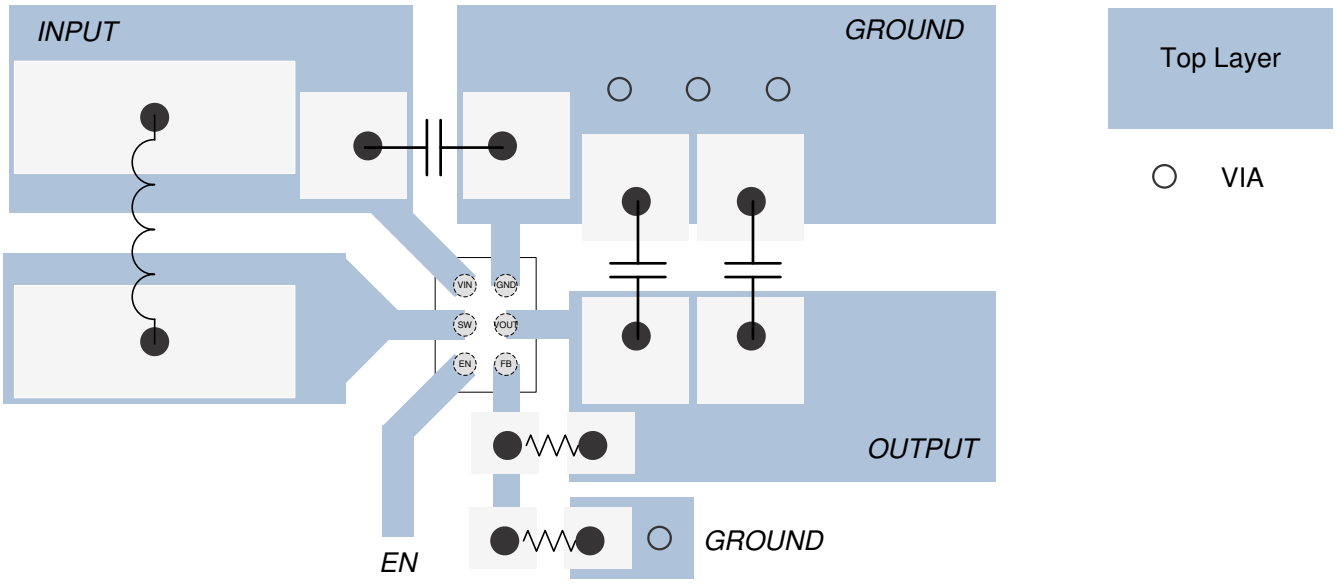


Figure 11-1. Layout -YFF

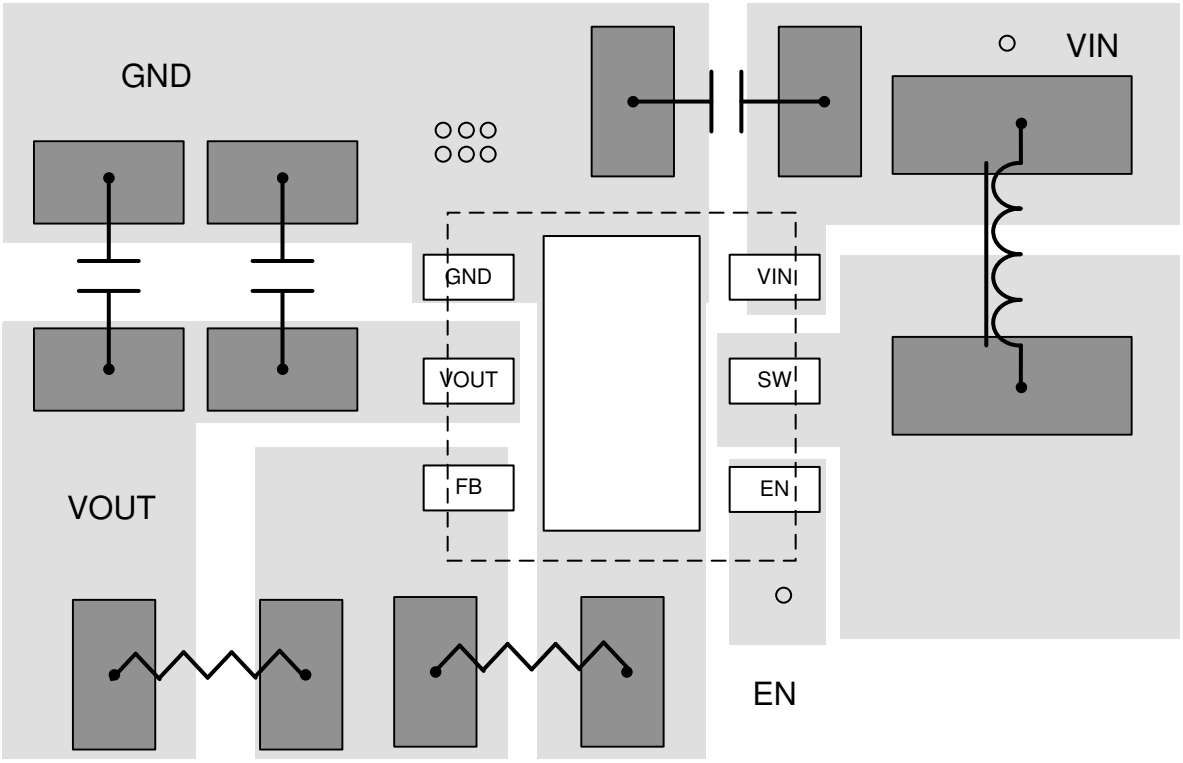


Figure 11-2. Layout - DRV

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61099x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.1.2 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Performing Accurate PFM Mode Efficiency Measurements*, SLVA236
- *Accurately measuring efficiency of ultralow-IQ devices*, SLYT558
- *IQ: What it is, what it isn't, and how to use it*, SLYT412

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
is a registered trademark of Texas Instruments.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS610992YFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19J
TPS610992YFFR.B	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19J
TPS610992YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19J
TPS610992YFFT.B	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19J
TPS610993YFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17X
TPS610993YFFR.B	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17X
TPS610993YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17X
TPS610993YFFT.B	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17X
TPS610994YFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17N
TPS610994YFFR.B	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17N
TPS610994YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17N
TPS610994YFFT.B	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17N
TPS610995DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NDU
TPS610995DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NDU
TPS610995DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NDU
TPS610995DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NDU
TPS610995YFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19K
TPS610995YFFR.B	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19K
TPS610995YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19K
TPS610995YFFT.B	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19K
TPS610996YFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19I
TPS610996YFFR.B	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19I
TPS610996YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19I
TPS610996YFFT.B	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	19I
TPS610997YFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	14K
TPS610997YFFR.B	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	14K
TPS610997YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	14K
TPS610997YFFT.B	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	14K
TPS61099DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1I8U

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61099DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1I8U
TPS61099YFFR	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	12G
TPS61099YFFR.B	Active	Production	DSBGA (YFF) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	12G
TPS61099YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	12G
TPS61099YFFT.B	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	12G

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

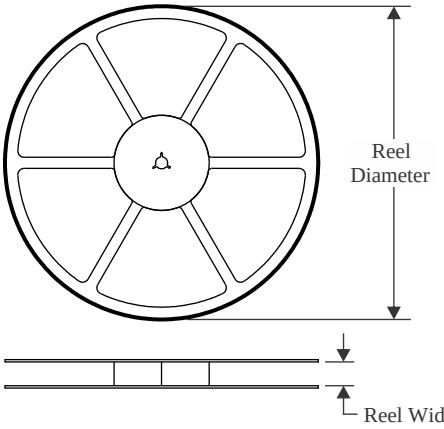
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

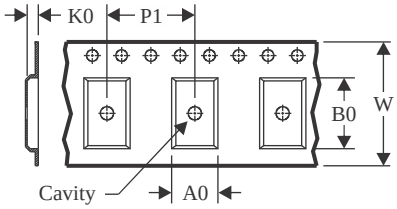
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

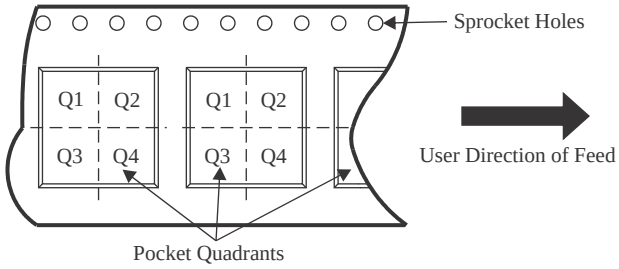


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

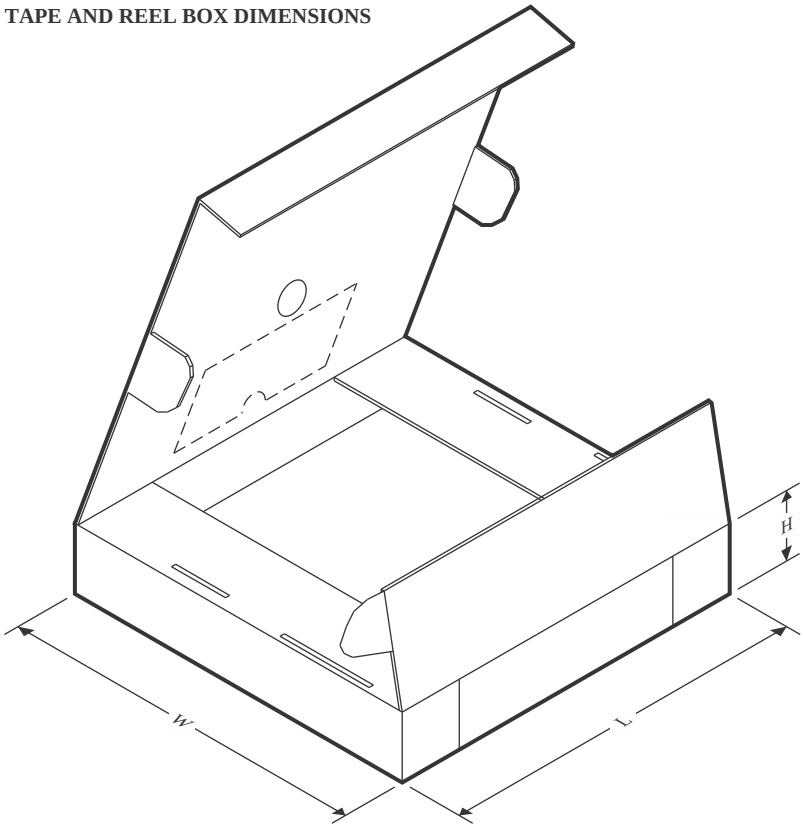


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS610992YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610992YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610993YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610993YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610994YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610994YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610995DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS610995DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS610995YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610995YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610996YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610996YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610997YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS610997YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1
TPS61099DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61099YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61099YFFT	DSBGA	YFF	6	250	180.0	8.4	0.96	1.36	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

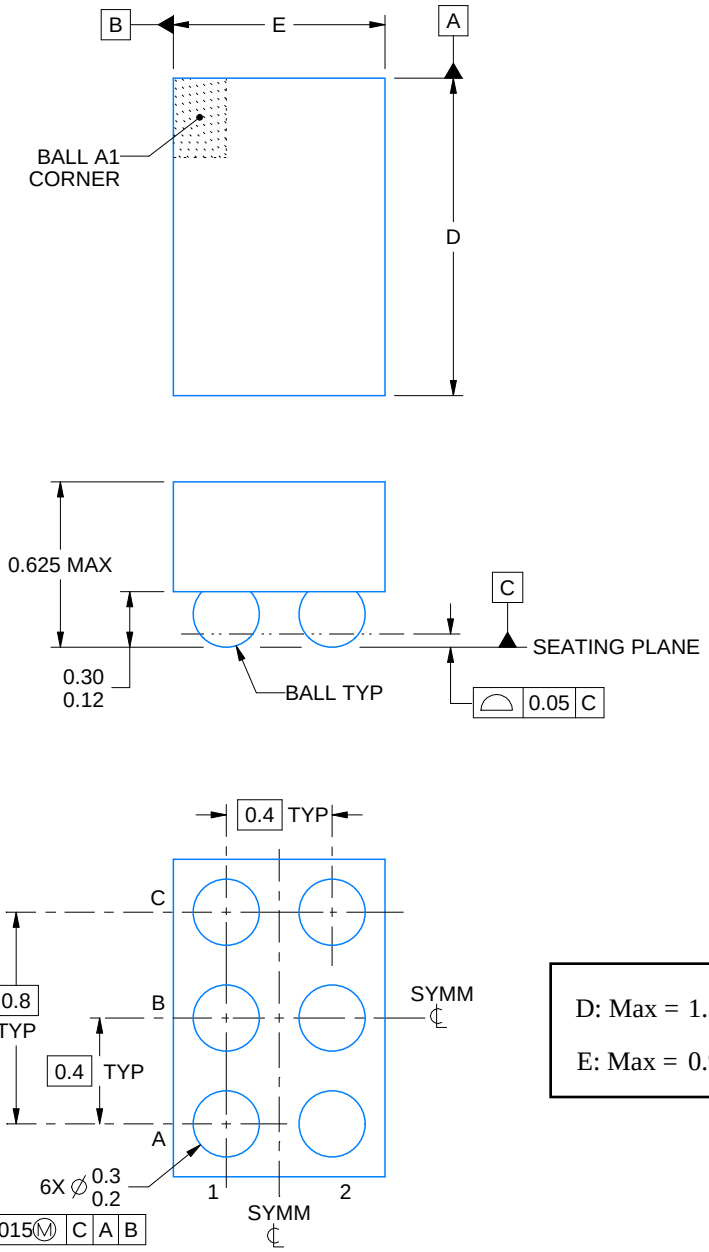
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS610992YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS610992YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS610993YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS610993YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS610994YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS610994YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS610995DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS610995DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS610995YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS610995YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS610996YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS610996YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS610997YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS610997YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS61099DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS61099YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS61099YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



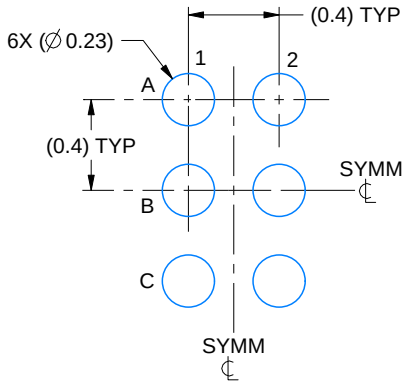
D: Max = 1.256 mm, Min =1.196 mm

E: Max = 0.914 mm, Min =0.854 mm

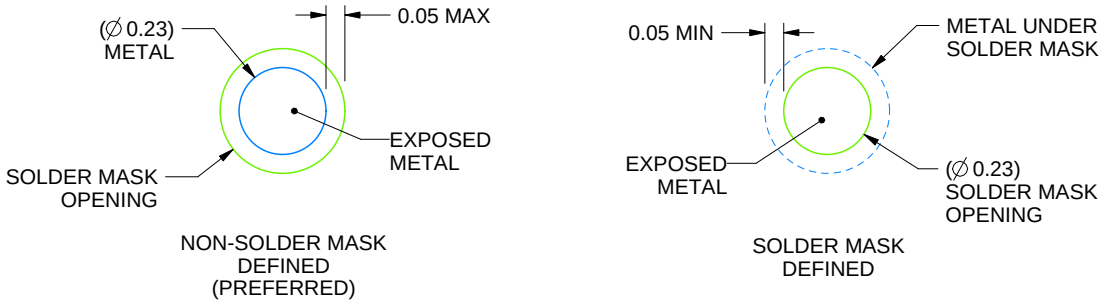
4223785/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

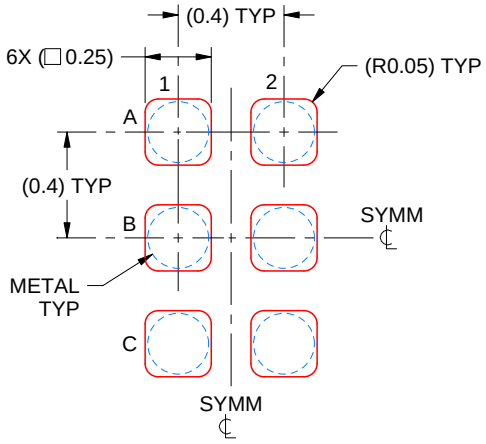


SOLDER MASK DETAILS
NOT TO SCALE

4223785/A 06/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

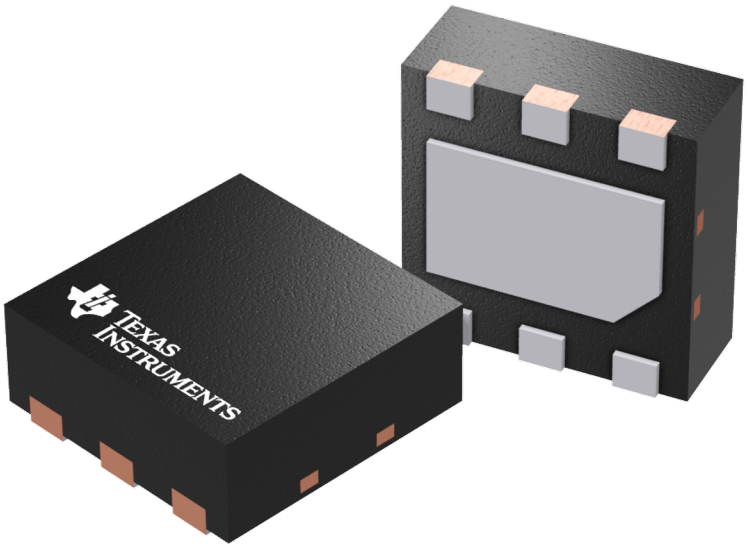
4223785/A 06/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

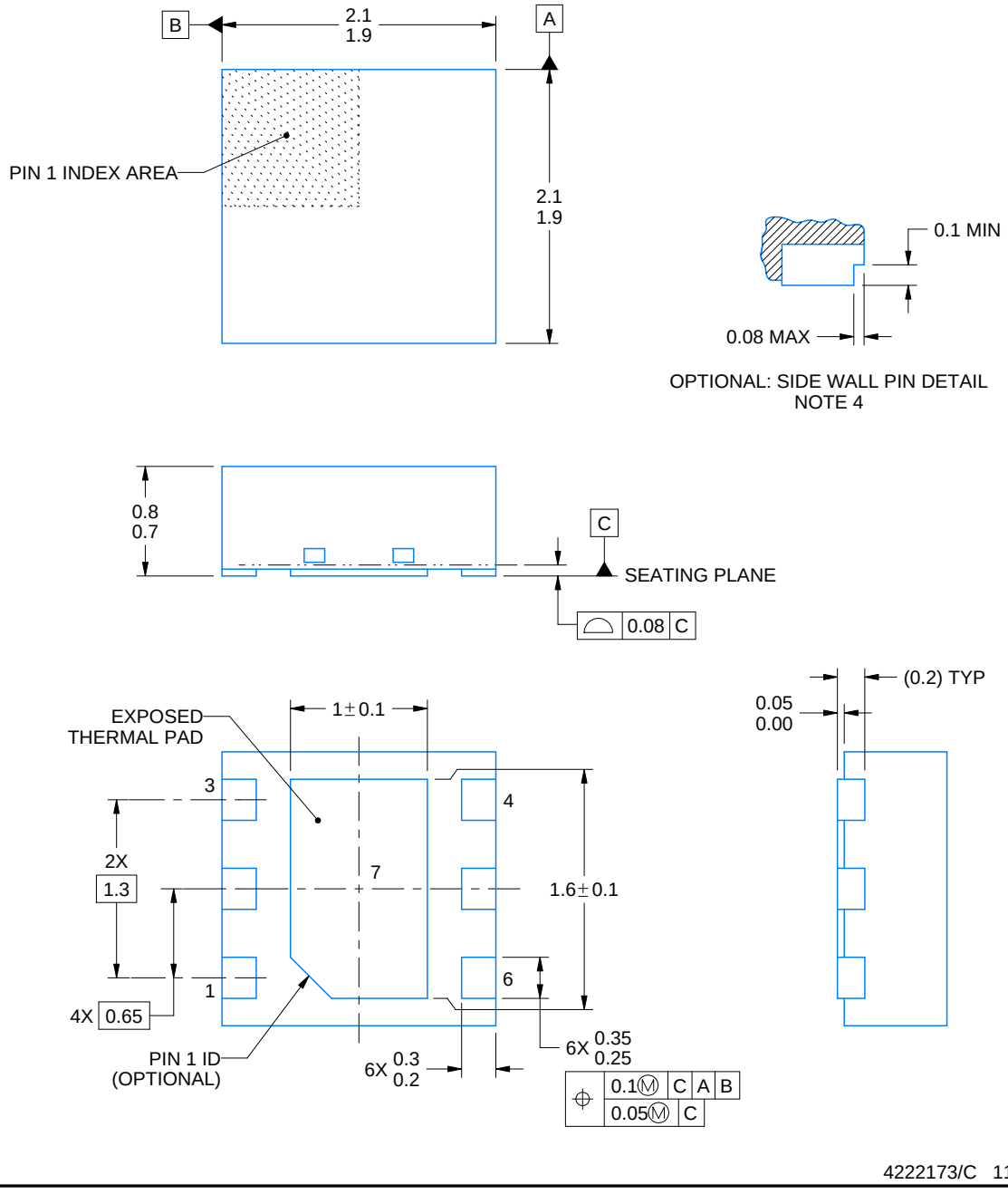
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



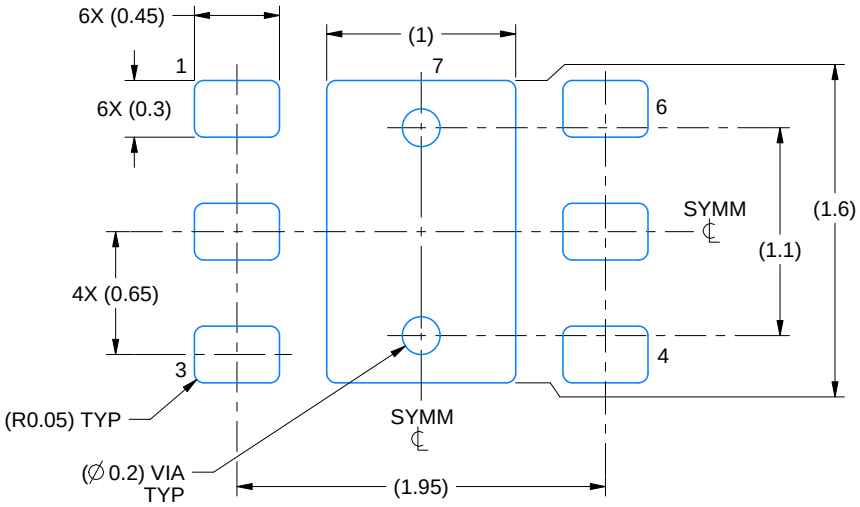
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

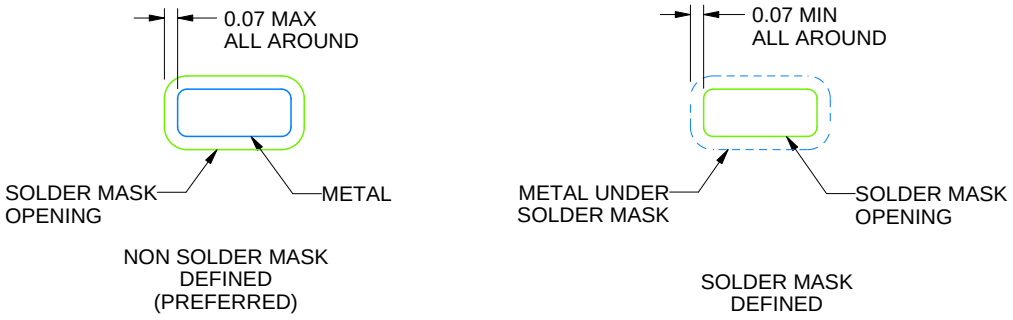


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

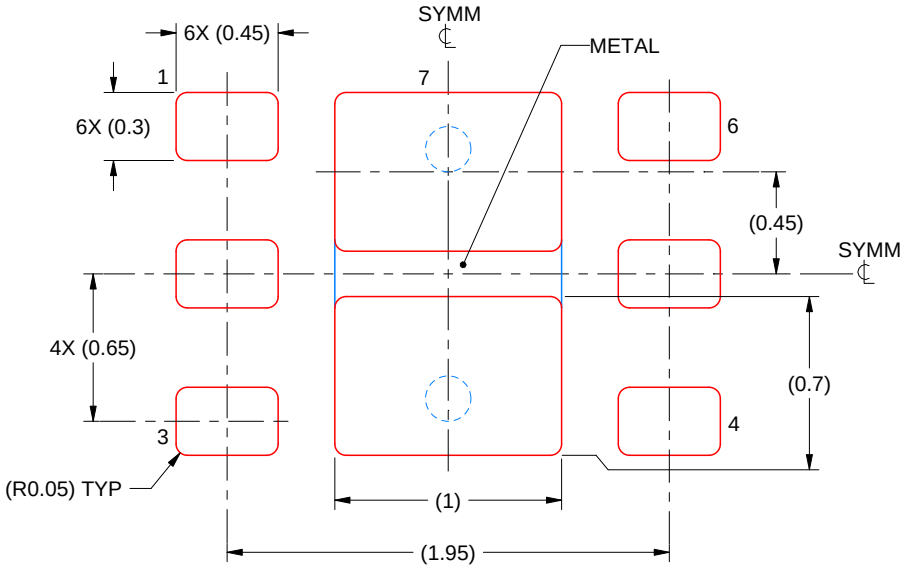


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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