TPS25221 2.5-V to 5.5-V, 2-A Continuous Current Limited Switch

1 Features

- 2.5-V to 5.5-V $V_{OPERATING}$
- Pin-to-Pin with TPS2553
- 2-A I_{CONT_MAX}
- 0.275-A to 2.7-A Adjustable I_{LIMIT} (±6.5% at 1.7 A)
- 70-mΩ (typical) R_{ON}
- 1.5-µs Short Circuit Response
- 8-ms Fault Reporting Deglitch
- Reverse Current Blocking (when disabled)
- Built-In Soft Start
- UL 60950 and UL 62368 Recognition
- 15-kV ESD Protection per IEC 61000-4-2 (with external capacitance)

2 Applications

- USB Ports/Hubs, Laptops, Desktops
- HDTV
- Set Top Boxes
- Optical Socket Protection

3 Description

The TPS25221 is intended for applications where heavy capacitive loads and short circuits may be encountered. The programmable current-limit threshold maybe set between 275 mA and 2.7 A (typical) using an external resistor. I_{LIMIT} accuracy as tight as ±6% can be achieved at the higher current-limit settings. Power-switch rise and fall times are controlled to minimize current surges during turn on and turn off.

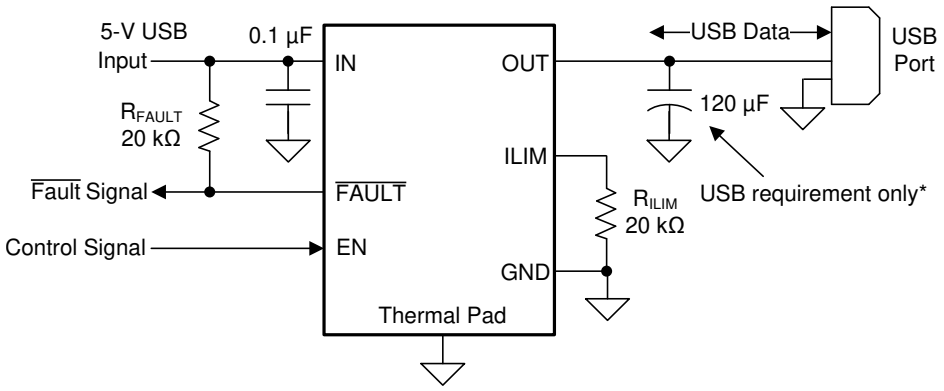
When a load attempts to draw current exceeding the programmed I_{LIMIT} the internal FET enters constant current mode in order to keep I_{LOAD} at or below I_{LIMIT}. The $\overline{FAULT}$ output will assert low during over-current conditions after the built in de-glitch time.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25221	SOT-23 (6)	2.90 mm x 1.60 mm
	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



*USB requirement that downstream facing ports are bypassed with at least 120 µF per hub.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision C (May 2019) to Revision D **Page**

- Removed content from the *Programming the Current-Limit Threshold* section ... 13

Changes from Revision B (November 2018) to Revision C **Page**

- Changed the Storage temperature From: TBD to: MIN = –65°C MAX = 150°C in the *Absolute Maximum Ratings* ... 4

Changes from Revision A (May 2018) to Revision B **Page**

- Deleted pending from the Features list items ... 1

Changes from Original (January 2018) to Revision A **Page**

- Released to Production ... 1

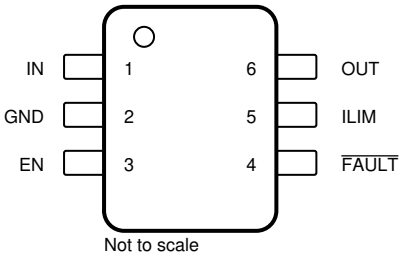
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5 Device Comparison Table

MAX OPERATING CURRENT	OUTPUT DISCHARGE	ENABLE	CURRENT LIMIT	LATCH OFF	Package	BASE PART NUMBER
2	N	High	Adjustable	N	SOT-23 (6)	TPS25221DBV
2	N	High	Adjustable	N	WSON (6)	TPS25221DRV

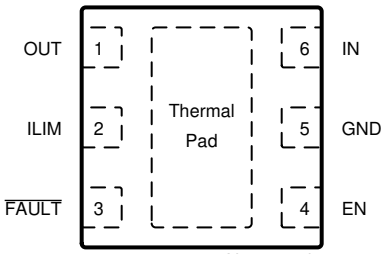
6 Pin Configuration and Functions

DBV PACKAGE
SOT-23 6-Pin
Top View



Not to scale

DRV PACKAGE
WSON 6-Pin
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	WSON		
IN	1	6	I	Input voltage and power switch drain; connect a 0.1 μF or greater ceramic capacitor from IN to GND close to IC
GND	2	5	--	Ground connection
EN	3	4	I	Enable input, logic high/low turns on power switch
$\overline{\text{FAULT}}$	4	3	O	Active-low open-drain output, asserted during over-current, or over-temperature conditions
ILIM	5	2	O	External resistor used to set current limit threshold
OUT	6	1	O	Power switch output, connect to load
Thermal Pad	--	PAD	--	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect thermal pad to GND pin externally.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage range on IN, OUT, EN, $\overline{\text{FAULT}}$,ILIM	–0.3	6	V
Voltage range from IN to OUT	–6	6	
Continuous $\overline{\text{FAULT}}$ sink current	0	25	mA
ILIM source current	0	1	mA
Maximum junction temperature, T_j	Internally Limited		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	V
		IEC 61000-4-2 contact discharge(3)	±8000	V
		IEC 61000-4-2 air-gap discharge(3)	±15000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Surges per EN61000-4-2. 1999 applied to output terminals of EVM. These are passing tests levels, not failure threshold.

7.3 Recommended Operating Conditions

Voltages are respect to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	IN	2.5		5.5	V
V_{EN}	Input voltage	EN	0		5.5	V
V_{IH}	High-level input voltage	EN	1.7			V
V_{IL}	Low-level input voltage	EN			0.66	V
I_{CON}	Output continuous current	OUT	0		2	A
R_{ILIM}	Current-limit threshold resistor range (nominal 1%) from ILIM to GND		20		210	kΩ
$I_{/FAULT}$	Sink current into $\overline{\text{FAULT}}$	$\overline{\text{FAULT}}$	0		10	mA
T_J	Operating junction temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS25221		UNIT
		DBV (SOT-23)	DRV (WSON)	
		6-PIN	6-PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.2	83	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.1	100.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.6	46.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	49.0	8.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.3	46.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	--	24.4	°C/W

(1) Proper thermal design is required to ensure T_J <125°C for best long term reliability. This is particularly important at higher currents, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

over recommended operating conditions, $V_{EN} = V_{IN}$, R_{FAULT} = 10 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance	DBV package, T_J = 25°C			70	80	mΩ
		DBV package, –40°C ≤T_J ≤125°C				110	
		DRV package, T_J = 25°C			70	92	
		DRV package, –40°C ≤T_J ≤125°C				122	
t_r	Rise time, output	V_{IN} = 5.5 V	C_L = 1 µF, R_L = 100 Ω, (see Figure 1)		0.55	0.95	ms
		V_{IN} = 2.5 V			0.35	0.62	
t_f	Fall time, output	V_{IN} = 5.5 V			0.24	0.3	
		V_{IN} = 2.5 V			0.22	0.28	
ENABLE INPUT EN OR $\overline{EN}$							
	Enable pin turn on/off threshold			0.8		1.6	V
I_{EN}	Input current	V_{EN} = 0 V or 5.5 V		-0.5	0	0.5	µA
t_{on}	Turnon time	C_L = 1 µF, R_L = 100 Ω, (see Figure 2)				3	ms
t_{off}	Turnoff time	C_L = 1 µF, R_L = 100 Ω, (see Figure 2)				0.7	ms
CURRENT LIMIT							
I_{OS}	Current-limit threshold (Maximum DC output current I_{OUT} delivered to load) and Short-circuit current, OUT connected to GND	R_{ILIM} = 20 kΩ	T_J = 25°C	2585	2720	2850	mA
			–40°C ≤T_J ≤125°C	2560		2880	
		R_{ILIM} = 30 kΩ	T_J = 25°C	1710	1820	1930	
			–40°C ≤T_J ≤125°C	1700		1945	
		R_{ILIM} = 80 kΩ	T_J = 25°C	630	690	755	
			–40°C ≤T_J ≤125°C	610		790	
		R_{ILIM} = 210 kΩ	T_J = 25°C	220	275	330	
			–40°C ≤T_J ≤125°C	210		370	
t_{IOS}	Response time to short circuit	V_{IN} = 5 V (see Figure 4)			1.5		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disable	V_{IN} = 5.5 V, No load on OUT, V_{EN} = 0 V,R_{ILIM} = 20 kΩ			0.02	0.5	µA
I_{SE}	Supply current, switch enable	V_{IN} = 5.5 V, No load on OUT ,R_{ILIM} = 20 kΩ			75	90	µA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising			2.37	2.47	V
	Hysteresis, IN	T_J = 25 °C			45		mV
$\overline{FAULT}$ FLAG							
V_{OL}	Output low voltage, $\overline{FAULT}$	$I_{/FAULT}$ = 1 mA				180	mV
	Off-state leakage	$V_{/FAULT}$ = 5.5 V				0.5	µA
	$\overline{FAULT}$ deglitch	$\overline{FAULT}$ assertion or de-assertion due to overcurrent condition		6	8	12	ms
THERMAL SHUTDOWN							
	Thermal shutdown threshold				165		°C
	Thermal shutdown threshold in current-limit				145		°C
	Hysteresis				20		°C

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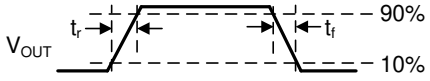


Figure 1. Power-On and Off Timing

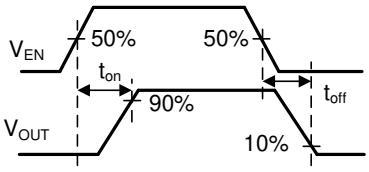


Figure 2. Enable Timing, Active High Enable

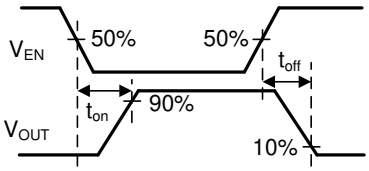


Figure 3. Enable Timing, Active Low Enable

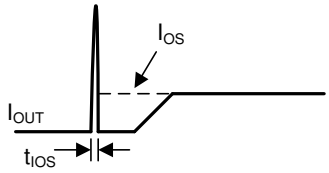
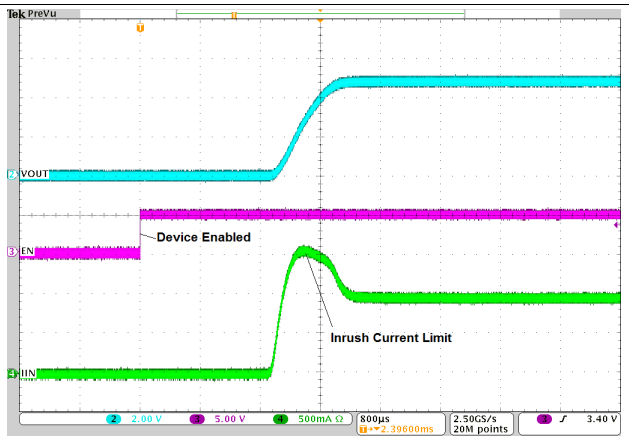


Figure 4. Output Short Circuit Parameters

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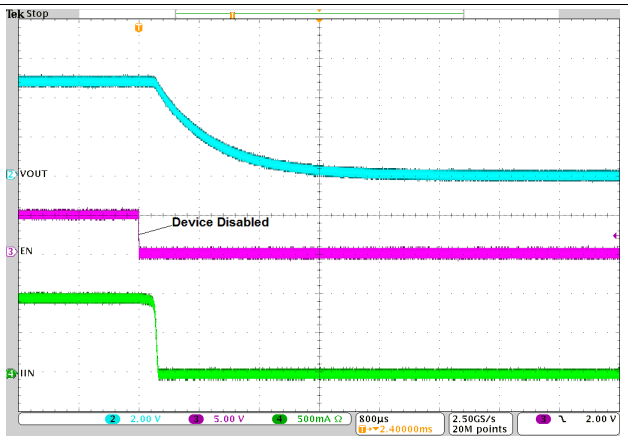
7.6 Typical Characteristics

See Figure 21 for reference schematic



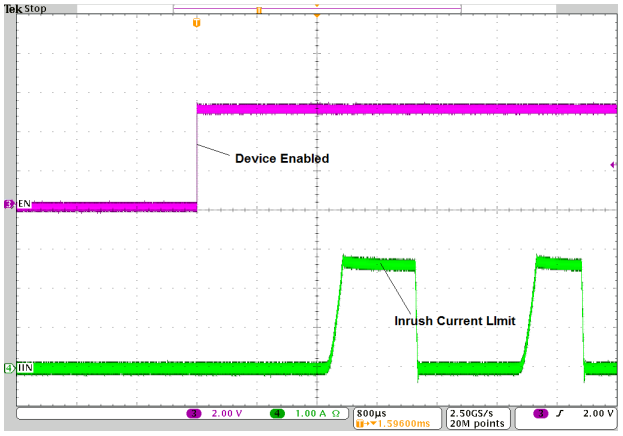
V_{IN} = 5 V, R_{ILIM} = 20 kΩ, R_{OUT} = 5 Ω

Figure 5. Turnon Delay and Rise Time



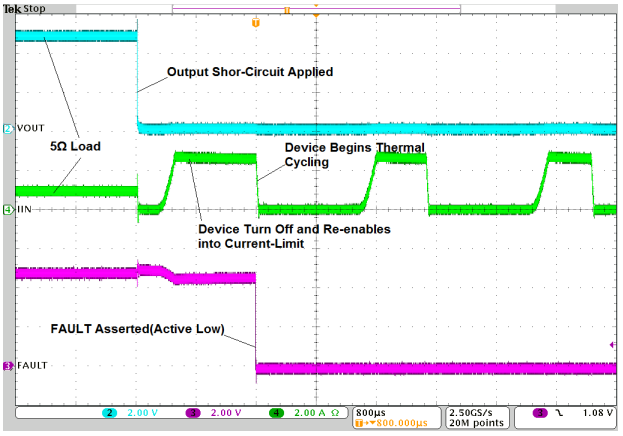
V_{IN} = 5 V, R_{ILIM} = 20 kΩ, R_{OUT} = 5 Ω

Figure 6. Turnoff Delay and Fall Time



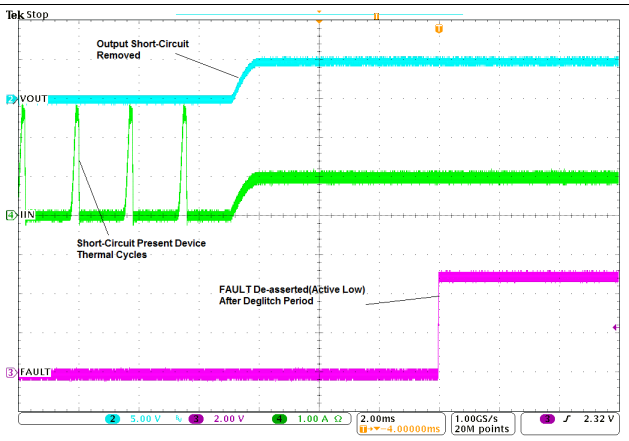
V_{IN} = 5 V, R_{ILIM} = 20 kΩ, R_{OUT} = 0 Ω

Figure 7. Device Enabled into Short-Circuit



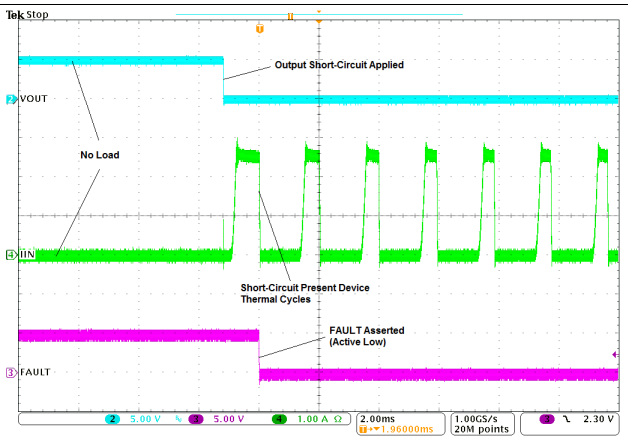
V_{IN} = 5 V, R_{ILIM} = 20 kΩ

Figure 8. Full-Load to Short-Circuit Transient Response



V_{IN} = 5 V, R_{ILIM} = 20 kΩ

Figure 9. Short-Circuit to Full-Load Recovery Response



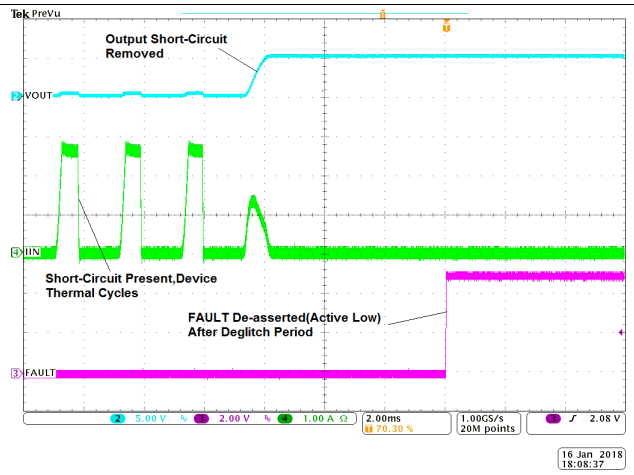
V_{IN} = 5 V, R_{ILIM} = 20 kΩ

Figure 10. No-Load to Short-Circuit Transient Response

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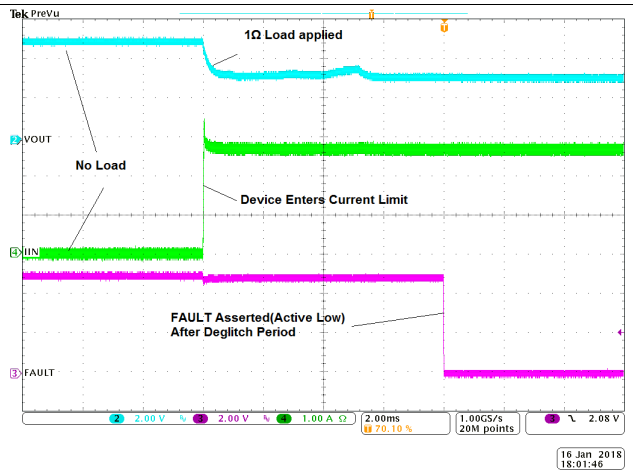
Typical Characteristics (continued)

See Figure 21 for reference schematic



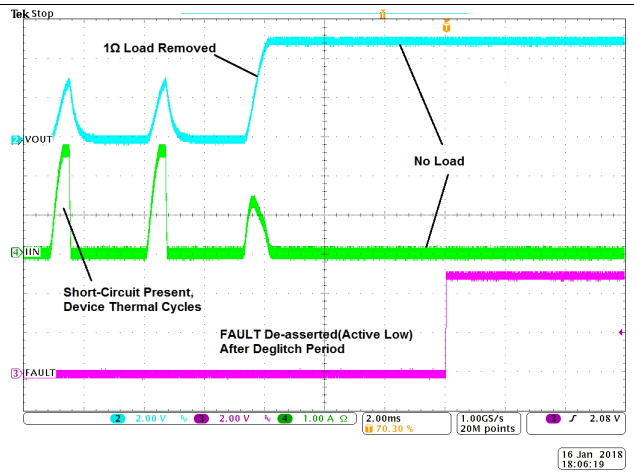
V_{IN} = 5 V, R_{ILIM} = 20 kΩ

Figure 11. Short-Circuit to No-Load Recovery Response



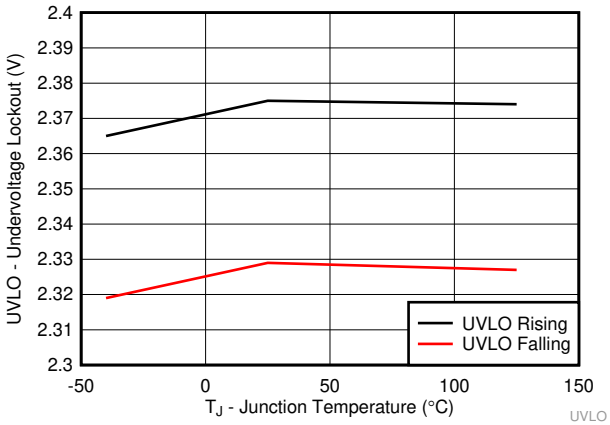
V_{IN} = 5 V, R_{ILIM} = 20 kΩ

Figure 12. No Load to 1-Ω Transient Response



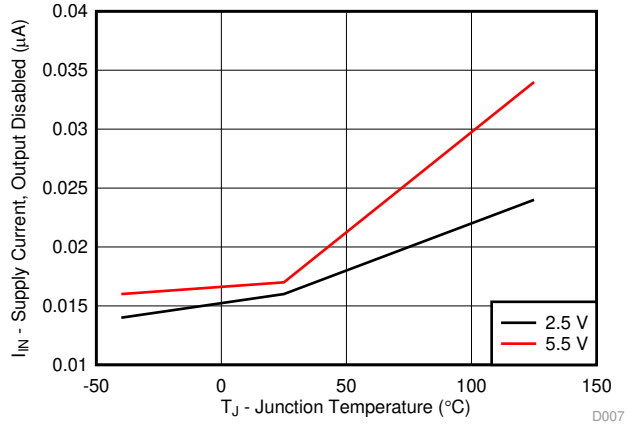
V_{IN} = 5 V, R_{ILIM} = 20 kΩ

Figure 13. 1-Ω to No Load Transient Response



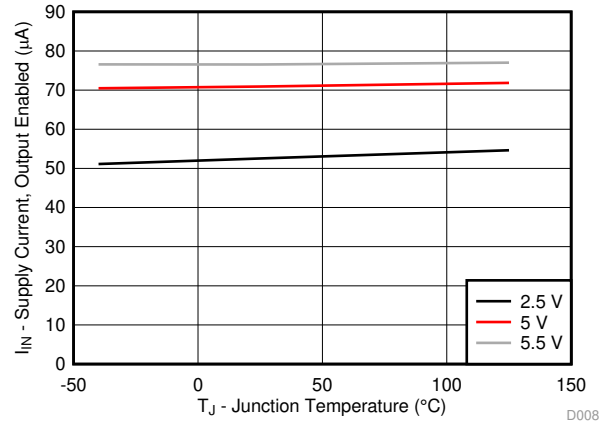
R_{ILIM} = 20 kΩ

Figure 14. UVLO – Undervoltage Lockout – V



R_{ILIM} = 20 kΩ

Figure 15. I_{IN} – Supply Current, Output Disabled – µA



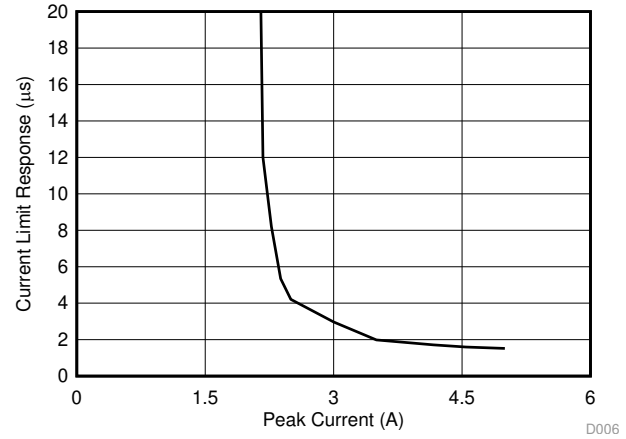
R_{ILIM} = 20 kΩ

Figure 16. I_{IN} – Supply Current, Output Enabled – µA

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Typical Characteristics (continued)

See Figure 21 for reference schematic



V_{IN} = 5 V, R_{ILIM} = 20 kΩ, T_A = 25°C

Figure 17. Current Limit Response – µs

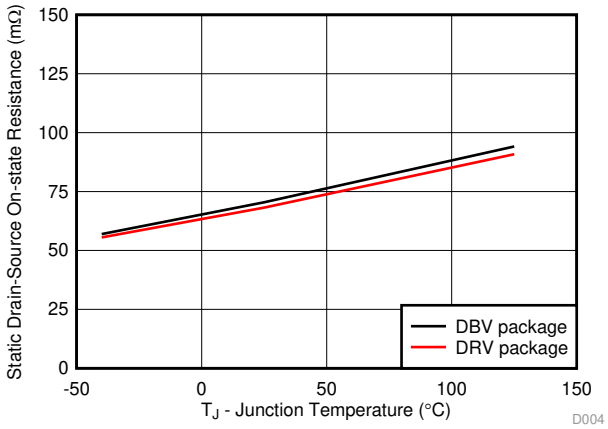
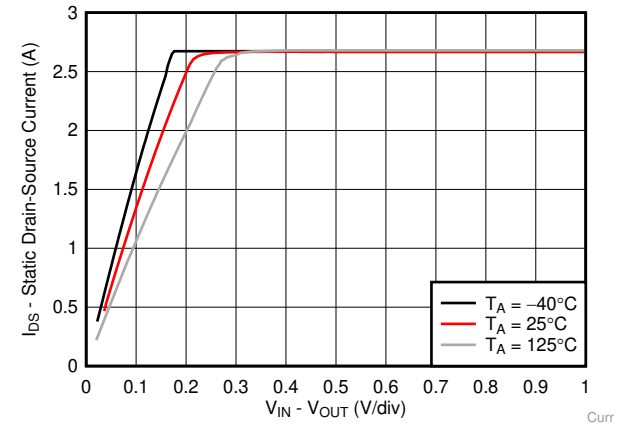
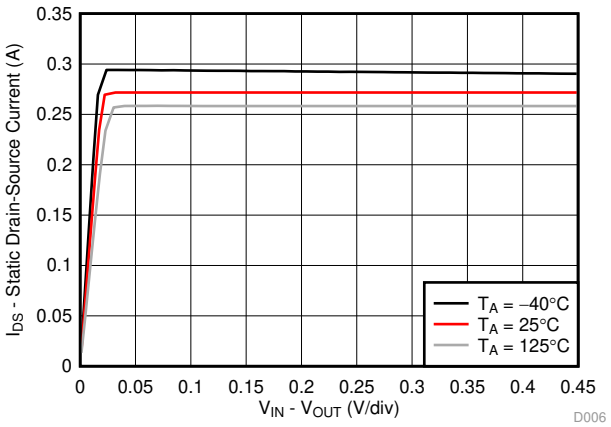


Figure 18. On-Resistance Vs. Junction Temperature



V_{IN} = 5.5 V, R_{ILIM} = 20 kΩ

Figure 19. Switch Current Vs. Drain-Source Voltage Across Switch



V_{IN} = 5.5 V, R_{ILIM} = 210 kΩ

Figure 20. Switch Current Vs. Drain-Source Voltage Across Switch

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8 Parameter Measurement Information

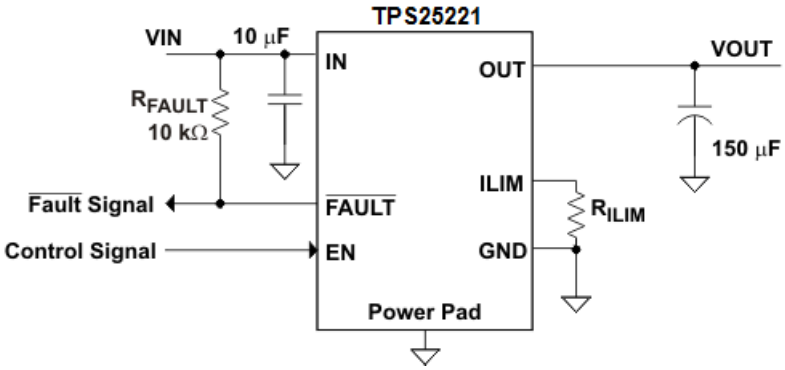


Figure 21. Typical Characteristics Reference Schematic

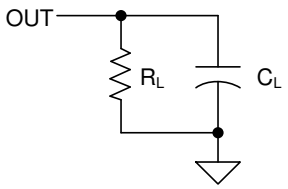


Figure 22. Output Rise / Fall Test Load

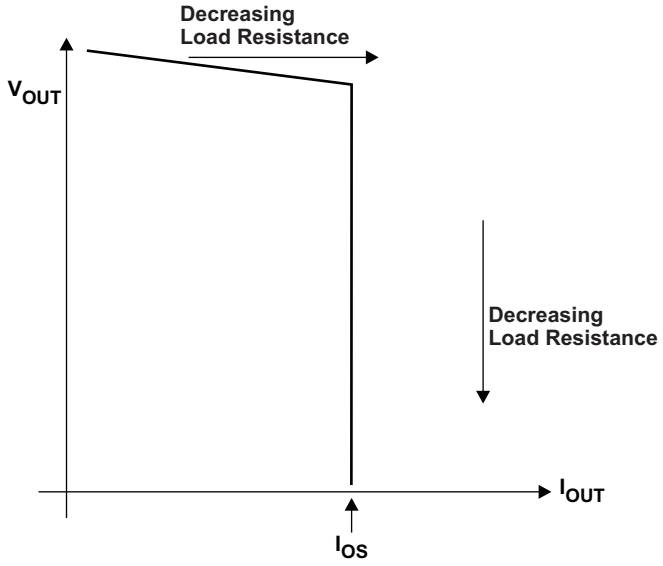


Figure 23. Output Voltage vs Current-Limit Threshold

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9 Detailed Description

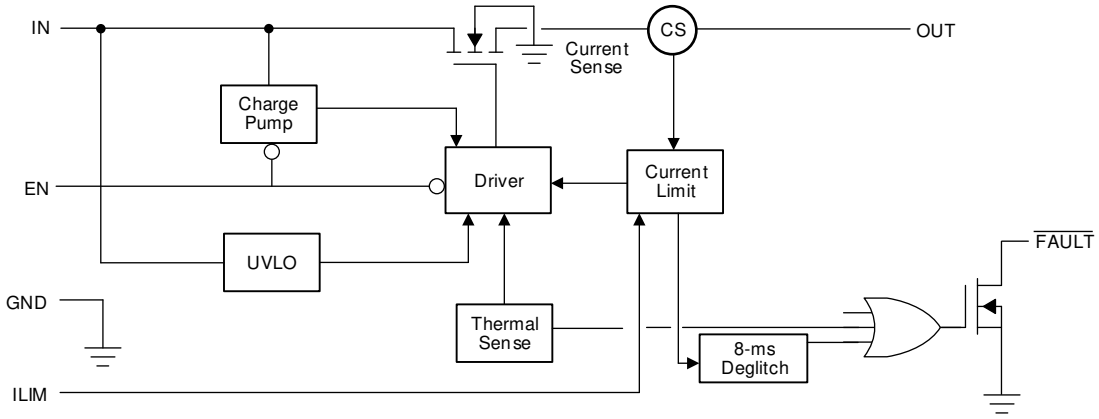
9.1 Overview

The TPS25221 is current-limited, power-distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads are encountered. The TPS25221 allows the user to program the current limit threshold between 275 mA to 2.7A (typical) through an external resistor.

This device incorporates an internal charge pump and the gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality.

The TPS25221 limits the output current to the current-limit threshold I_{OS} during an over-current or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the saturation region. The result of limiting the output current to I_{OS} reduces the output voltage at OUT because N-channel MOSFET is no longer fully enhanced (see Figure 22).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Over-current Conditions

The TPS25221 responds to over-current conditions by limiting output current to I_{OS} as show in Figure 24. When an overload condition occurs, the device maintains a constant output current and the output voltage reduces accordingly. Two possible overload conditions can occur.

1. The first condition is when a short circuit or overload is present when the device is powered-up or enabled. The short circuit and overload holds the output near zero potential with respect to ground and the TPS25221 ramps the output current to I_{OS}. The TPS25221 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.
2. The second condition is when a short circuit, partial short circuit, or transient overload occurs when the device is on and the internal NFET is fully enhanced. The device responds to the over-current condition by turning off the NFET within the time limit specified by t_{IOS} (see Figure 4). The current-sense amplifier is over-driven during this time and momentarily disables the internal N-channel MOSFET. The current-sense amplifier then recovers and ramps the output current to I_{OS}. Similar to the previous case, the TPS25221 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS25221 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. Thermal limiting turns off the internal NFET and starts when the junction temperature exceeds 145°C (typical). The device remains off until the junction temperature cools 20°C (typical) and then restarts.

9.3.2 $\overline{\text{Fault}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an over-current or over-temperature condition. The TPS25221 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS25221 is designed to eliminate nuisance $\overline{\text{FAULT}}$ reporting by using an internal 8 ms deglitch delay when reporting a fault. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal transient conditions, such as starting into a heavy capacitive load. The deglitch circuitry delays asserting and de-asserting current limit induce FAULT reports. The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an over-temperature condition, but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULT}}$ oscillation during an over-temperature event.

9.3.3 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

9.3.4 Enable, (EN)

The logic enable controls the power switch and device supply current. The supply current is reduced to less than 0.5 μA.

The TPS25221 is active high logic, when a logic low is present on EN, the part is disabled. A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

9.3.5 Thermal Sense

The TPS25221 has self-protection features using two independent thermal-sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds the Over Temperature Shutdown Threshold (OTSD). The TPS25221 device operates in constant-current mode during overload conditions, which increases the voltage drop across power-switch. Power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an over-current condition. The first thermal sensor turns off the power switch when the die temperature exceeds 145°C (typical) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C (typical). The TPS25221 continues to cycle off and on until the fault condition is removed.

The ambient thermal sensor turns off the power-switch when the junction temperature exceeds 165°C (typical) in non-current limit condition. The part will turn the switch back on once the junction temperature has cooled approximately 20°C (typical).

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Feature Description (continued)

The open-drain fault reporting output $\overline{\text{FAULT}}$ is asserted (active low) immediately during an over-temperature shutdown condition.

9.4 Device Functional Modes

Table 1. Protection Function Table

EVENT	CONDITION	ACTION
Overload on OUT	$I_{LOAD} > I_{OS}$	The device outputs I_{OS} x R_{LOAD} until thermal shutdown. The fault indicator asserts when the over-current condition persists for more 8 ms, the fault does not de-assert until over-current is removed and persists for 8 ms.
Overheating	T_J > 165 C	The device immediately shuts off the internal power switch and the fault indicator asserts immediately when the junction temperature exceeds 165°C (typical). The device has a thermal hysteresis of 20°C (typical). The fault indicator de-asserts when the junction temperature falls below 145°C (typical).
Undervoltage on IN	V_{IN} < 2.37 V	The device immediately shuts off the internal current-limited switch.

9.5 Programming

9.5.1 Programming the Current-Limit Threshold

The over-current threshold is user programmable through an external resistor. The TPS25221 uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 20 kΩ ≤ R_{ILIM} ≤ 210 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the over-current threshold when selecting a value for R_{ILIM}. The following equations and Figure 24 can be used to calculate the resulting over-current threshold for a given external resistor value (R_{ILIM}). Figure 24 includes current-limit tolerance due to variations caused by temperature and process. However, the equations do not account for tolerance due to external resistor variation, so it is important to account for this tolerance when selecting R_{ILIM}. The traces routing the R_{ILIM} resistor to the TPS25221 must be as short as possible to reduce parasitic effects on the current-limit accuracy.

R_{ILIM} can be selected to provide a current-limit threshold that occurs: 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start-up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(max)}$ curve.

To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies, causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(min)}$ curve.

Current-Limit Threshold Equation (I_{OS}):

$$I_{OSmax}(mA) = \frac{52640V}{R_{ILIM}^{0.97}k\Omega}$$

$$I_{OSnom}(mA) = \frac{55960V}{R_{ILIM}^{1.004}k\Omega}$$

$$I_{OSmin}(mA) = \frac{56850V}{R_{ILIM}^{1.033}k\Omega}$$

where:

20 kΩ ≤ R_{ILIM} ≤ 210 kΩ. (1)

Programming (continued)

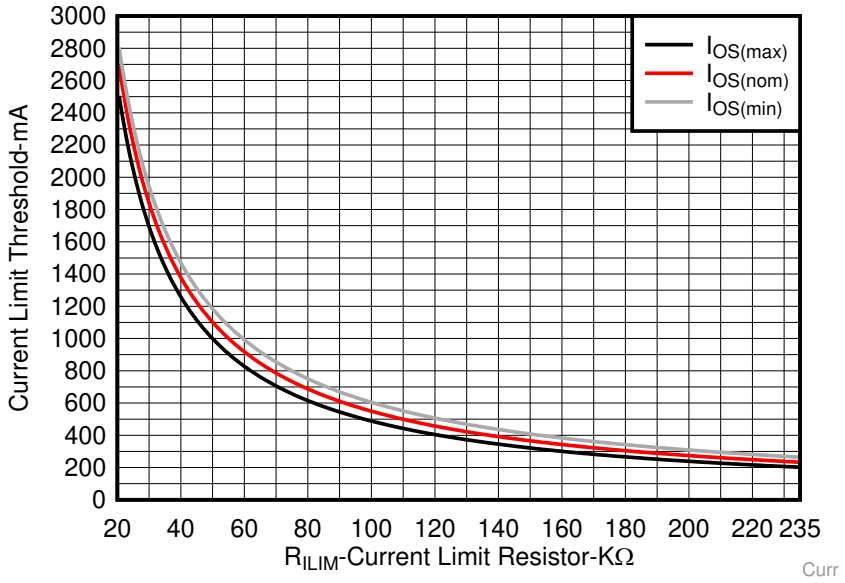


Figure 24. Current-Limit Threshold vs Current-Limit Resistor (R_{ILIM})

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Constant-Current

During normal operation, the TPS25221 load current is less than the current-limit threshold and the device is not limiting current. During normal operation the N-channel MOSFET is fully enhanced, and $V_{OUT} = V_{IN} - (I_{OUT} \times r_{DS(on)})$. The voltage drop across the MOSFET is relatively small compared to V_{IN}, and V_{OUT} is approximately equal to V_{IN}.

The TPS25221 limits current to the programmed current-limit threshold, set by R_{ILIM}, reducing gate drive to the internal NFET, which increases Rds(on) and reduces load current. This allows the device to effectively regulate the current to the current-limit threshold. Increasing the resistance of the MOSFET means that the voltage drop across the device is no longer negligible ($V_{IN} \neq V_{OUT}$), and V_{OUT} decreases. The amount that V_{OUT} decreases is proportional to the magnitude of the overload condition. The expected V_{OUT} can be calculated by:

$$I_{OS} \times R_{LOAD}$$

where:

I_{OS} is the current-limit threshold and R_{LOAD} is the magnitude of the overload condition. (2)

For example, if I_{OS} is programmed to 1 A and a 1 Ω overload condition is applied, the resulting V_{OUT} is 1 V.

While in current limit the power dissipation in the package can raise the die temperature above the thermal shutdown threshold (145°C typical), and the device turns off until the die temperature decreases by the hysteresis of the thermal shutdown circuit (20°C typical). The device then turns on and continues to thermal cycle until the overload condition is removed.

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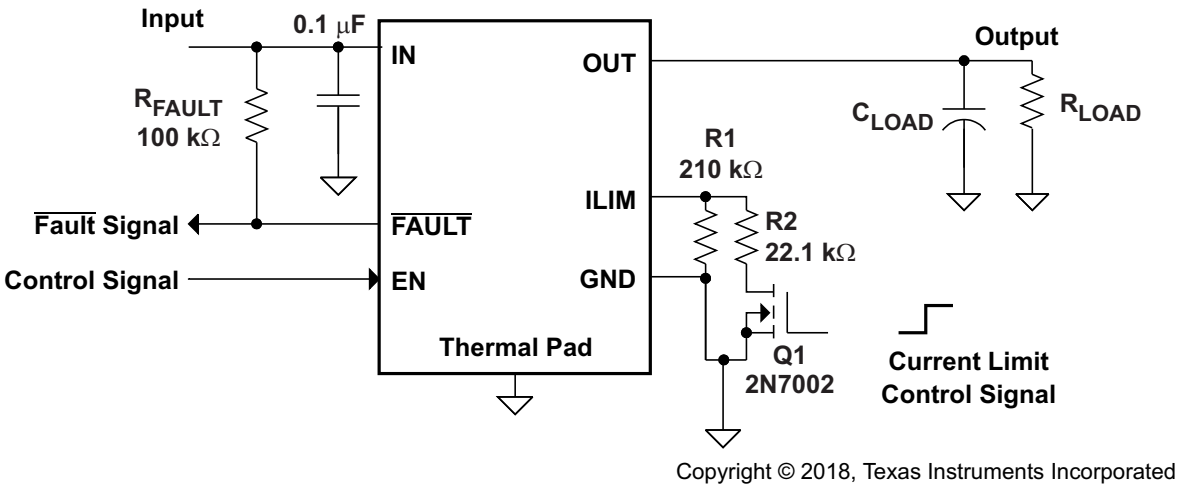
10.2 Typical Applications

10.2.1 Two-Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. Figure 25 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see the *Programming the Current-Limit Threshold* section). A logic-level input enables or disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET and resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

NOTE

ILIM must never be driven directly with an external signal.



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Figure 25. Two-Level Current-Limit Circuit

10.2.1.1 Design Requirements

For this example, use the parameters shown in Table 2.

Table 2. Design Requirements

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Above a minimum current limit	1000 mA
Below a maximum current limit	500 mA

10.2.1.2 Detailed Design Procedures

10.2.1.2.1 Designing Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 1 A must be delivered to the load so that the minimum desired current-limit threshold is 1000 mA. Use the I_{OS} equations and Figure 24 to select R_{ILIM}.

$$I_{OSmin}(mA) = 1000mA$$
$$I_{OSmin}(mA) = \frac{56850V}{R_{ILIM}{}^{1.033}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{56850V}{I_{OSmin}mA}\right)^{\frac{1}{1.033}}$$
$$R_{ILIM}(k\Omega) = 50k\Omega \quad (3)$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 49.9 kΩ. This sets the minimum current-limit threshold at 1 A . Use the I_{OS} equations, Figure 24, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 49.9k\Omega$$
$$I_{OSmax}(mA) = \frac{52640V}{R_{ILIM}{}^{0.97}k\Omega}$$
$$I_{OSmax}(mA) = \frac{52640V}{49.9^{0.97}k\Omega}$$
$$I_{OSmax}(mA) = 1186mA \quad (4)$$

The resulting maximum current-limit threshold is 1186 mA with a 49.9 kΩ resistor.

10.2.1.2.2 Designing Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 500 mA to protect an up-stream power supply. Use the I_{OS} equations and Figure 24 to select R_{ILIM}.

$$I_{OSmax}(mA) = 500mA$$
$$I_{OSmax}(mA) = \frac{52640V}{R_{ILIM}{}^{0.97}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{52640V}{I_{OSmax}mA}\right)^{\frac{1}{0.97}}$$
$$R_{ILIM}(k\Omega) = 121.6k\Omega \quad (5)$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 124 kΩ. This sets the maximum current-limit threshold at 500 mA . Use the I_{OS} equations, Figure 24, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 124k\Omega$$
$$I_{OSmin}(mA) = \frac{56850V}{R_{ILIM}{}^{1.033}k\Omega}$$
$$I_{OSmin}(mA) = \frac{56850V}{124^{1.033}k\Omega}$$
$$I_{OSmin}(mA) = 391mA \quad (6)$$

The resulting minimum current-limit threshold is 391 mA with a 124 kΩ resistor.

10.2.1.2.3 Accounting for Resistor Tolerance

The previous sections described the selection of R_{ILIM} given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on TPS25221 performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts

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for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the I_{OS} equations to calculate the threshold limits. It is important to use tighter tolerance resistors, for example, 0.5% or 0.1%, when precision current limiting is desired.

Table 3. Common R_{ILIM} Resistor Selections

DESIRED NOMINAL CURRENT LIMIT (mA)	IDEAL RESISTOR (kΩ)	CLOSEST 1% RESISTOR (kΩ)	RESISTOR TOLERANCE		ACTUAL LIMITS		
			1% LOW (kΩ)	1% HIGH (kΩ)	$I_{OS(min)}$ (mA)	$I_{OS(nom)}$ (mA)	$I_{OS(max)}$ (mA)
275	199.2	200	198	202	236	274	312
400	137.2	137	135.6	138.4	349	401	450
500	109.8	110	108.9	111.1	438	499	556
600	91.6	90.9	90.0	91.8	533	605	669
700	78.6	78.7	77.9	79.5	619	699	770
800	68.8	68.1	67.4	68.8	719	808	886
900	61.2	61.9	61.3	62.5	793	889	972
1000	55.1	54.9	54.4	55.4	898	1003	1092
1200	45.9	46.4	45.9	46.9	1068	1188	1285
1400	39.4	39.2	38.8	39.6	1272	1407	1514
1600	34.5	34.8	34.5	35.1	1438	1585	1699
1800	30.7	30.9	30.6	31.2	1626	1786	1907
2000	27.6	27.4	27.1	27.7	1841	2015	2143
2200	25.1	24.9	24.7	25.1	2032	2219	2351
2400	23.0	23.2	23.0	23.4	2186	2382	2518
2600	21.3	21.5	21.3	21.7	2365	2571	2711
2700	20.5	20.5	20.3	20.7	2484	2697	2839

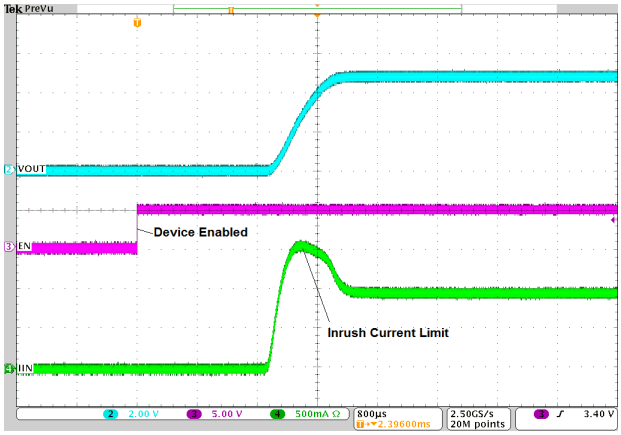
10.2.1.2.4 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, TI recommends placing a 0.1 µF or greater ceramic bypass capacitor between IN and GND as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power-supply.

TI recommends placing a high-value electrolytic capacitor on the output pin when large transient currents are expected on the output.

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10.2.1.3 Application Curve

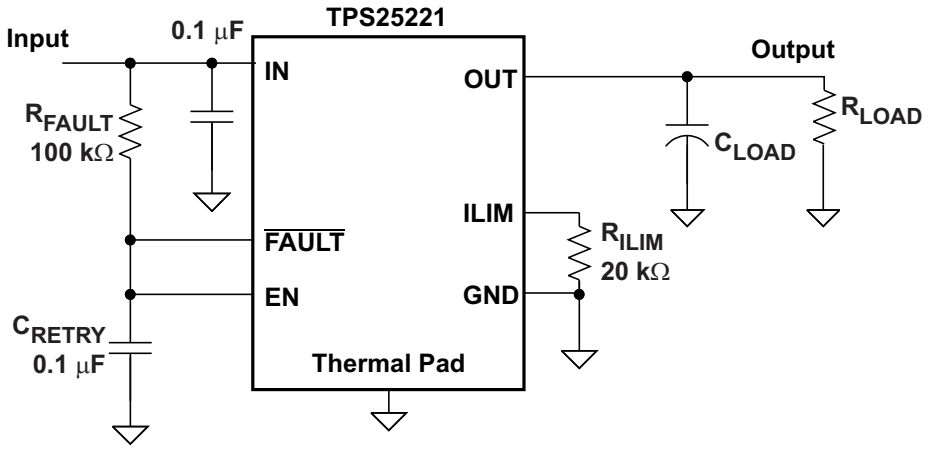


V_{IN} = 5 V, R_{ILIM} = 20 kΩ, R_{OUT} = 5 Ω

Figure 26. Turnon Delay and Rise Time

10.2.2 Auto-Retry Functionality

Some applications require that an over-current condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{FAULT}$ pulls low disabling the part. The part is disabled when EN is pulled low, and $\overline{FAULT}$ goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on EN reaches the turn-on threshold, and the auto-retry time is determined by the resistor-capacitor time constant. The device continues to cycle in this manner until the fault condition is removed.

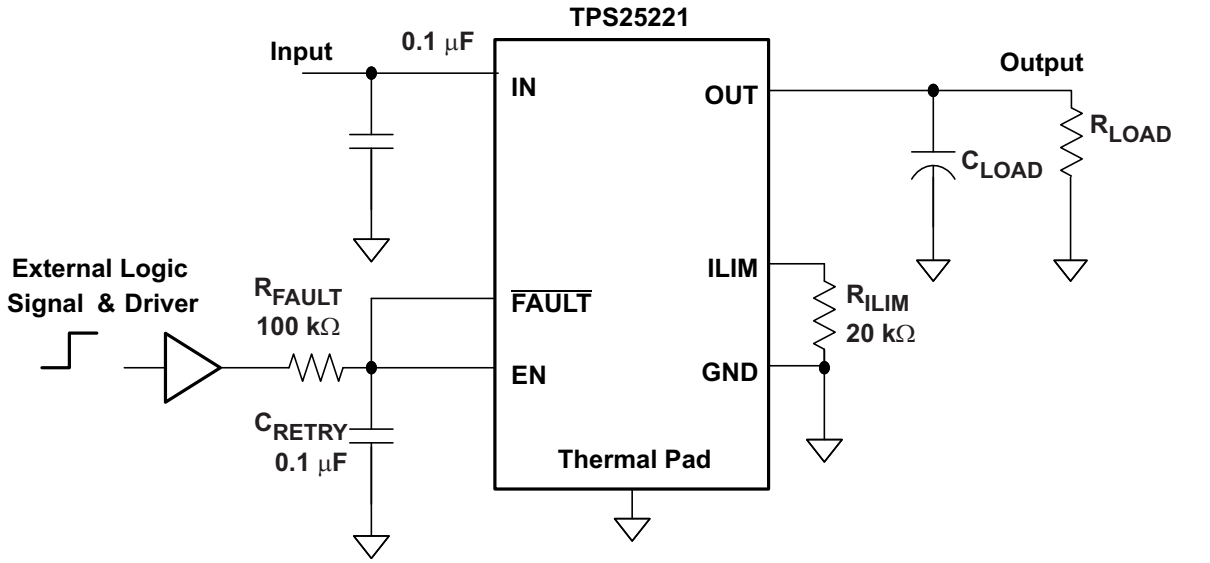


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Figure 27. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable or disable with an external logic signal. Figure 28 shows how an external logic signal can drive EN through R_{FAULT} and maintain auto-retry functionality. The resistor-capacitor time constant determines the auto-retry time-out period.

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Figure 28. Auto-Retry Functionality With External EN Signal

10.2.2.1 Design Requirements (added)

For this example, use the parameters shown in Table 4.

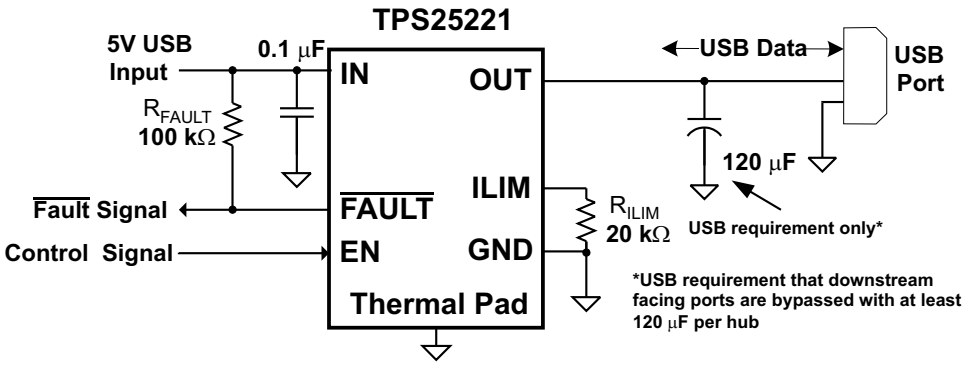
Table 4. Design Requirements

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Above a minimum current limit	1000 mA
Below a maximum current limit	500 mA

10.2.2.2 Detailed Design Procedure

Refer to *Programming the Current-Limit Threshold* section for the current limit setting. For auto-retry functionality, once FAULT asserted, EN pull low, TPS25221 is disabled, FAULT des-asserted, C_{RETRY} is slowly charged to EN logic high through R_{FAULT}, then enable, after deglitch time, FAULT asserted again. In the event of an overload, TPS25221 cycles and has output average current. ON-time with output current is decided by FAULT deglitch time. OFF-time without output current is decided by R_{FAULT} x C_{RETRY} constant time to EN logic high and t_{on} time. Therefore, set the R_{FAULT} × C_{RETRY} to get the desired output average current during overload.

10.2.3 Typical Application as USB Power Switch



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Figure 29. Typical Application as USB Power Switch

10.2.3.1 Design Requirements

For this example, use the parameters shown in Table 5.

Table 5. Design Requirements

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Current	1200 mA

10.2.3.1.1 USB Power-Distribution Requirements

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

- Self Powered Hub (SPH) must:
  - Current limit downstream ports
  - Report over-current conditions
- Bus Powered Hub (BPH) must:
  - Enable or disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS25221 meets each of these requirements. The integrated current limiting and over-current reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

10.2.3.2 Detailed Design Procedure

10.2.3.2.1 Universal Serial Bus (USB) Power-Distribution Requirements

One application for this device is for current limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mbps or 1.5-Mbps, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480 Mbps. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

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USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current-limit threshold of the current-limiting power-switch exceed the maximum current-limit draw of the intended application. The latest USB standard must always be referenced when considering the current-limit threshold

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS25221 has higher current capability than required for a single USB port allowing it to power multiple downstream ports.

11 Power Supply Recommendations

11.1 Self-Powered and Bus-Powered Hubs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, keep the power to the embedded function off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power-switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

11.2 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting.

11.3 Power Dissipation and Junction Temperature

The low ON-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is required design practice to determine power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature expected and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated using Equation 7:

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Power Dissipation and Junction Temperature (continued)

$$P_D = r_{DS(on)} \times I_{OUT}^2 \quad (7)$$

where

- P_D = Total power dissipation (W)
- $r_{DS(on)}$ = Power switch on-resistance (Ω)
- I_{OUT} = Maximum current-limit threshold (A)
- This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A \quad (8)$$

where

- T_A = Ambient temperature (°C)
- θ_{JA} = Thermal resistance (°C/W)
- P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the *refined* $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout. The table provides example thermal resistances for specific packages and board layouts.

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12 Layout

12.1 Layout Guidelines

- TI recommends placing the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- TI recommends placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin when large transient currents are expected on the output.
- The traces routing the RILIM resistor to the device must be as short as possible to reduce parasitic effects on the current limit accuracy.
- The thermal pad must be directly connected to PCB ground plane using wide and short copper trace.

12.2 Layout Example

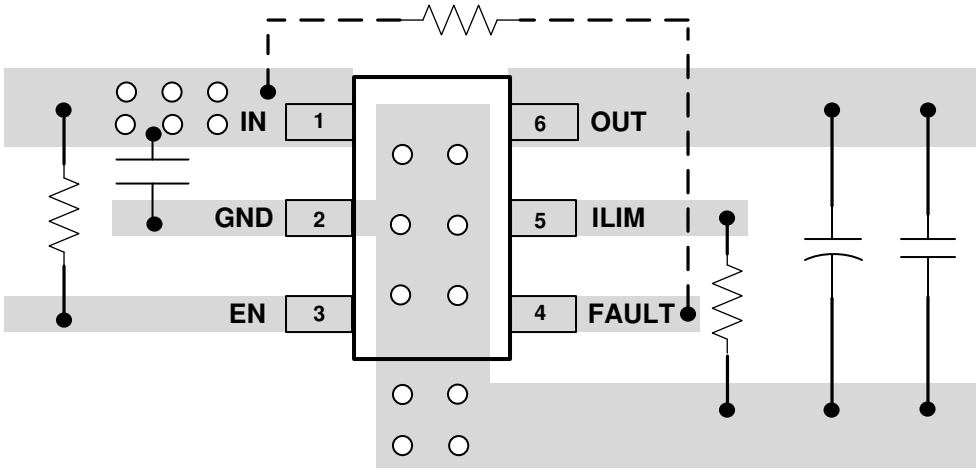


Figure 30. TPS25221DBV Board Layout

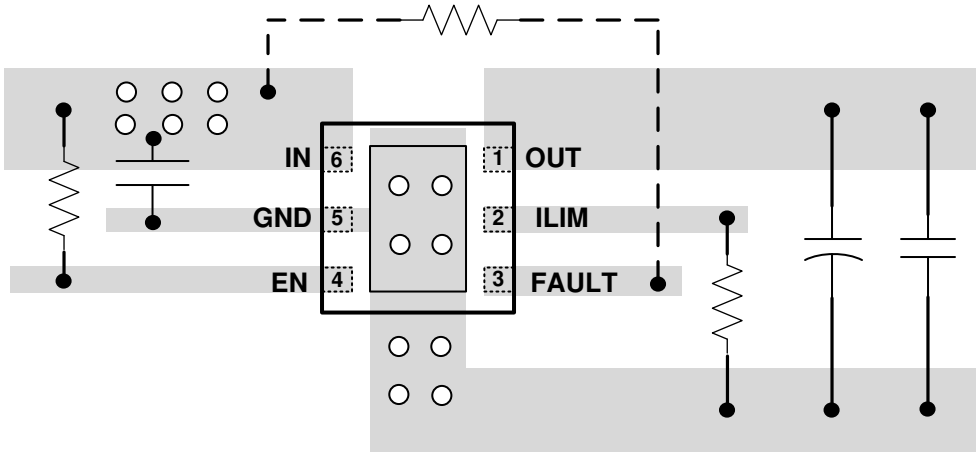


Figure 31. TPS25221DRV Board Layout

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- TPS25221 Evaluation Module User's Guide (SLVUBD1)

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

E2E is a trademark of Texas Instruments.

13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25221DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1B4F
TPS25221DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1B4F
TPS25221DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1B4F
TPS25221DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1B4F
TPS25221DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C7H
TPS25221DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C7H
TPS25221DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C7H
TPS25221DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C7H
TPS25221DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C7H
TPS25221DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C7H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

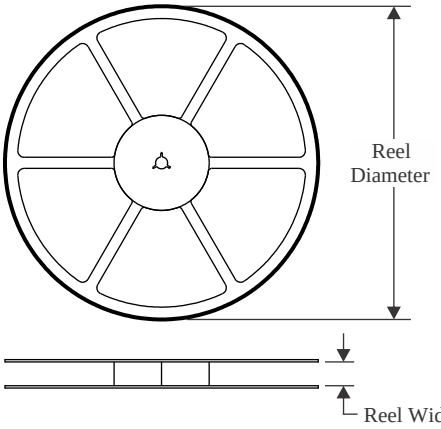
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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

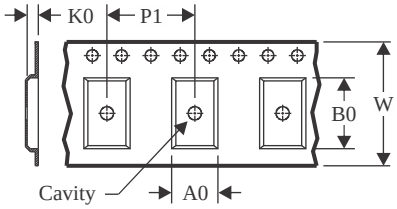
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

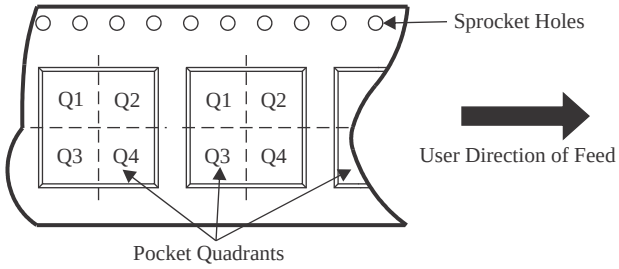


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

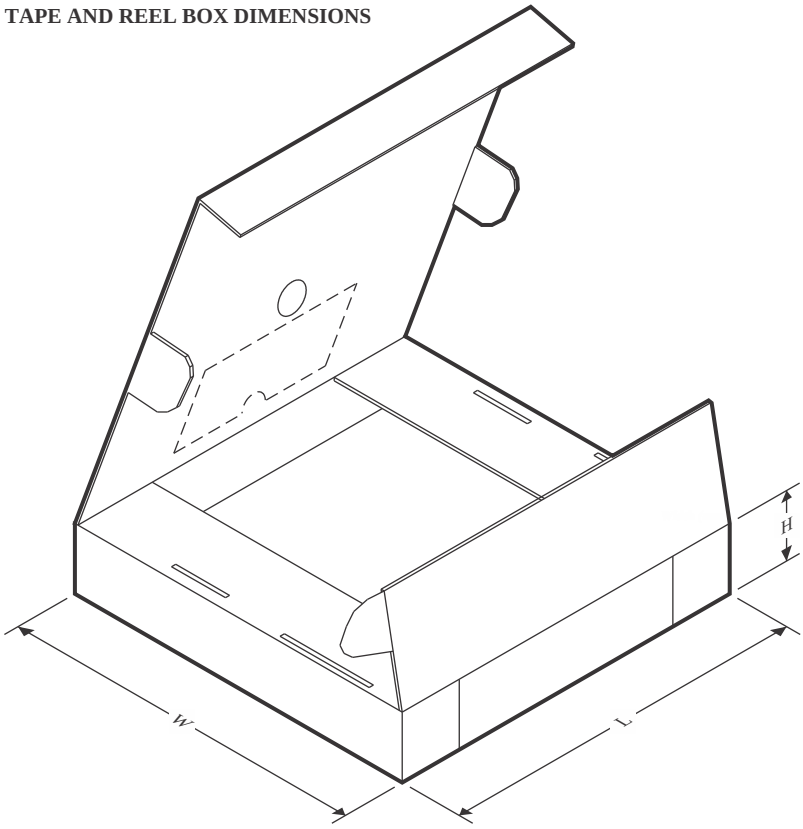
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25221DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS25221DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS25221DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS25221DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS25221DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25221DRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS25221DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

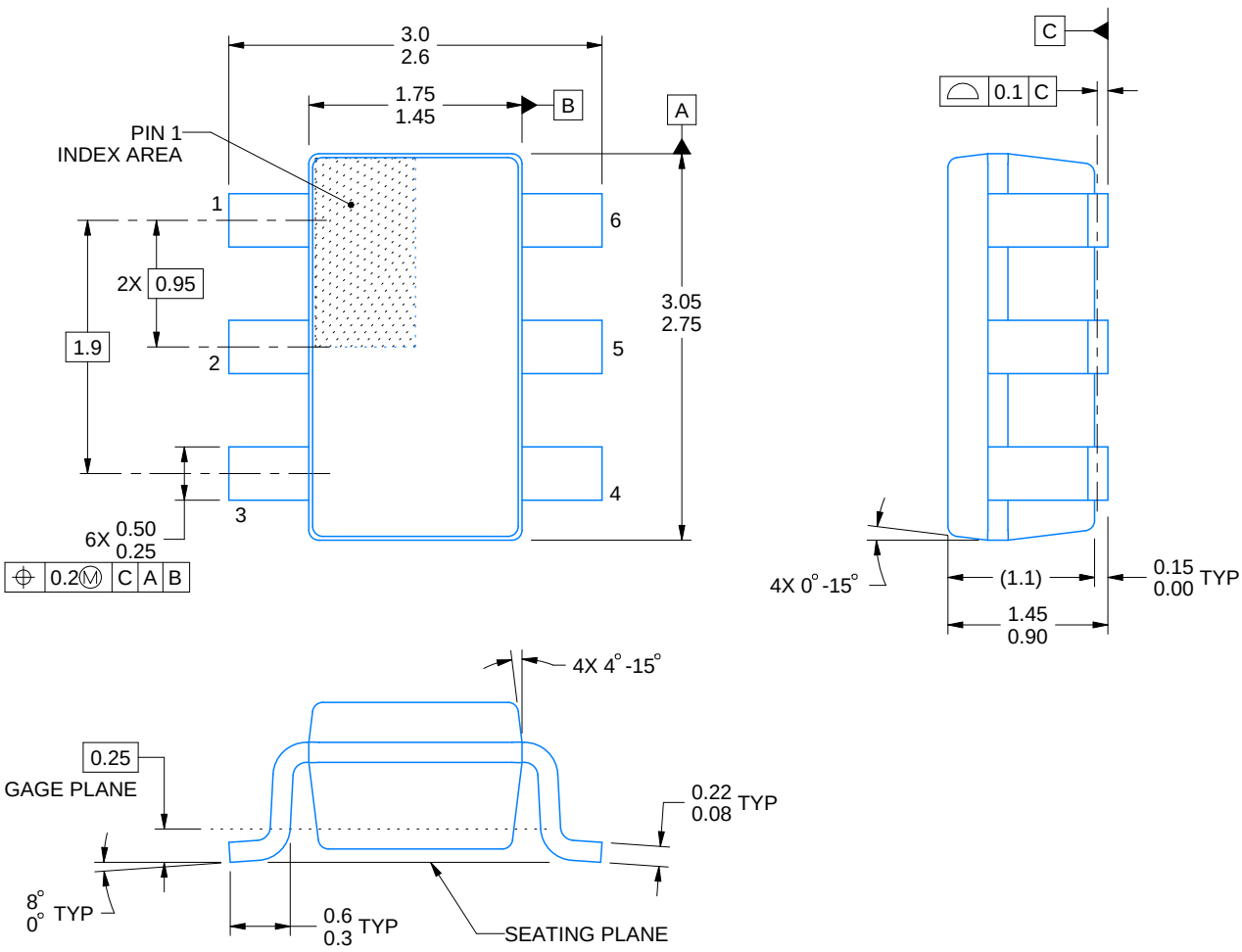
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25221DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS25221DBVT	SOT-23	DBV	6	250	183.0	183.0	20.0
TPS25221DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TPS25221DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS25221DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS25221DRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TPS25221DRVT	WSON	DRV	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

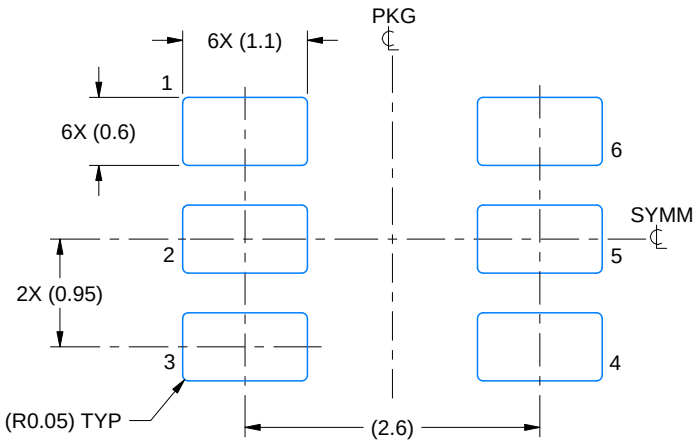
SMALL OUTLINE TRANSISTOR



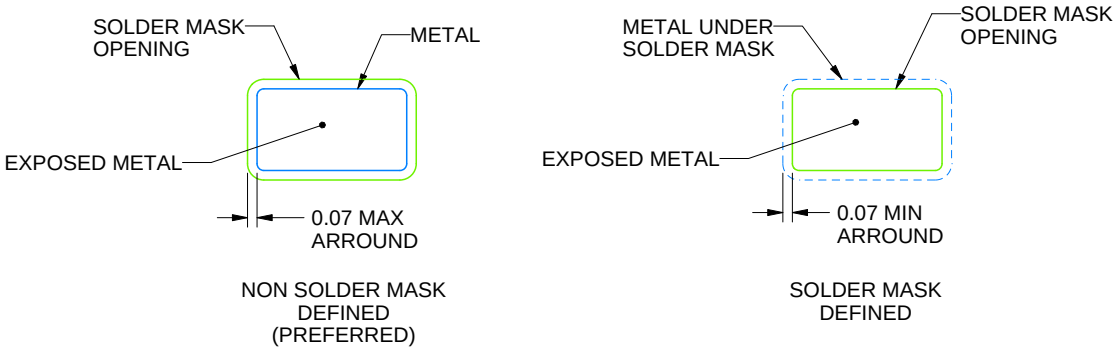
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

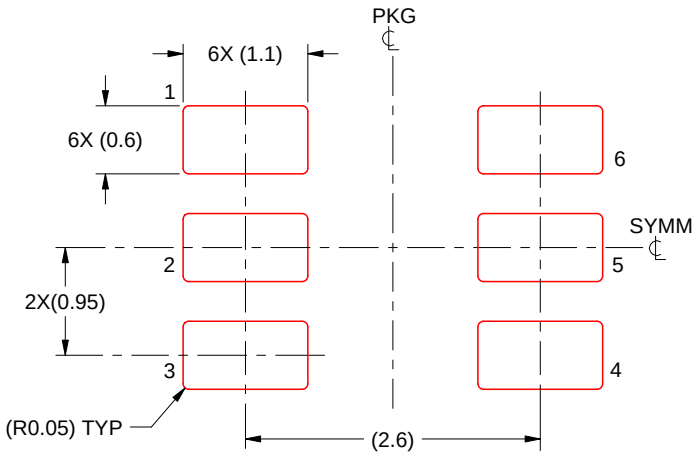


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

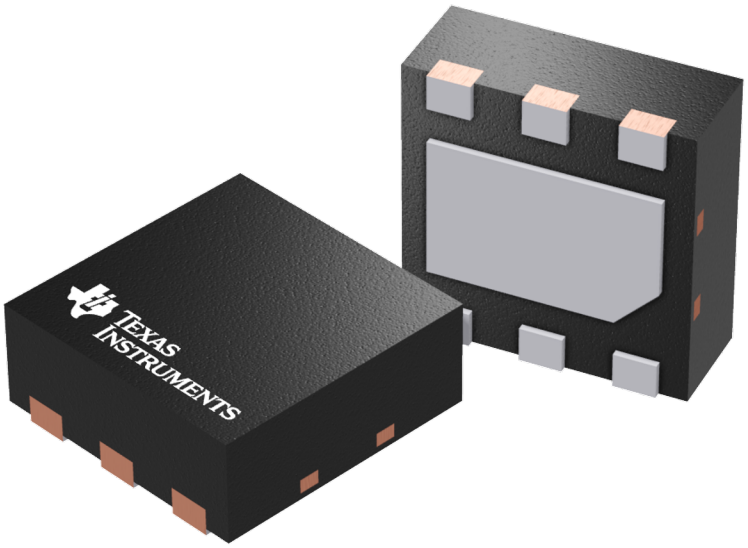
4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

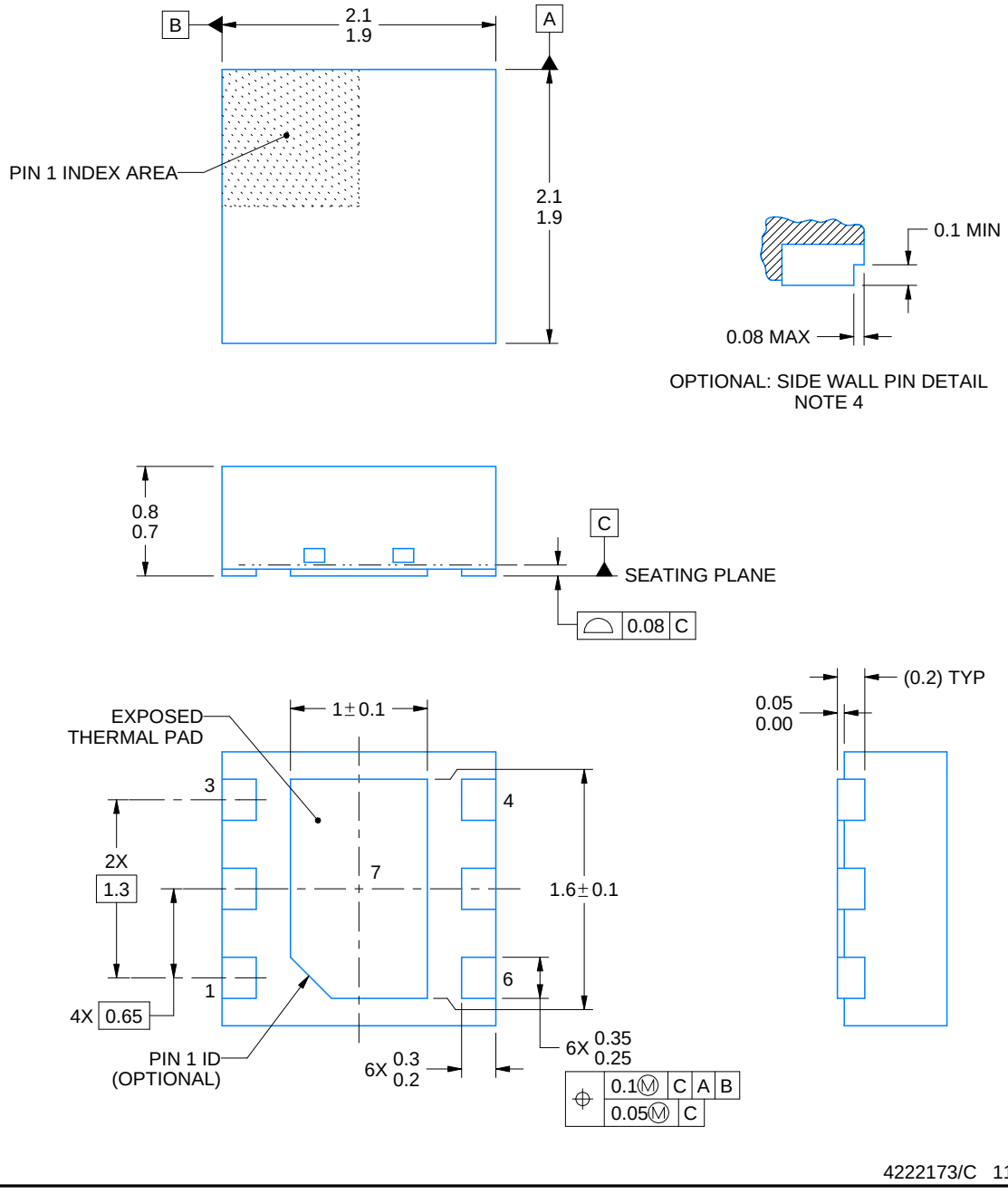
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



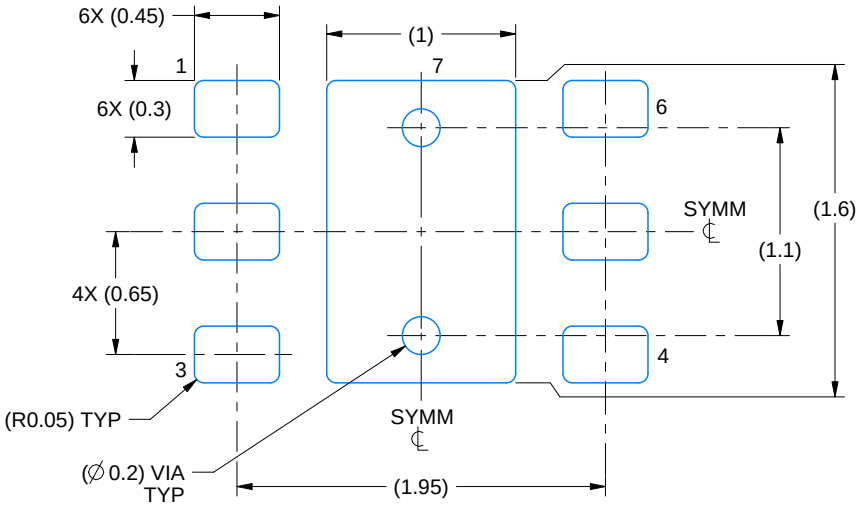
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

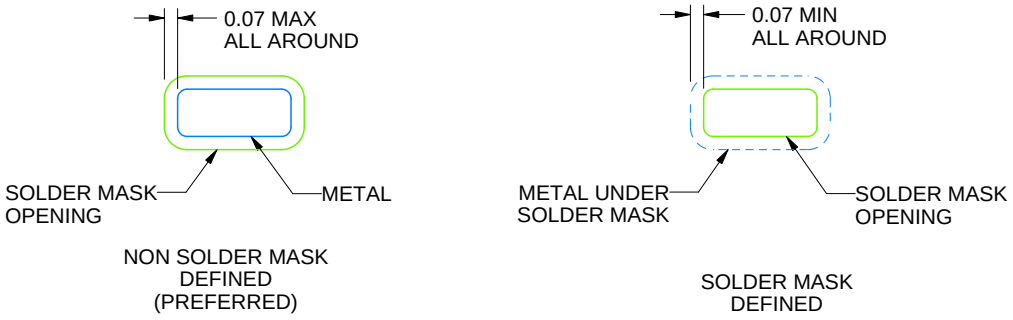


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

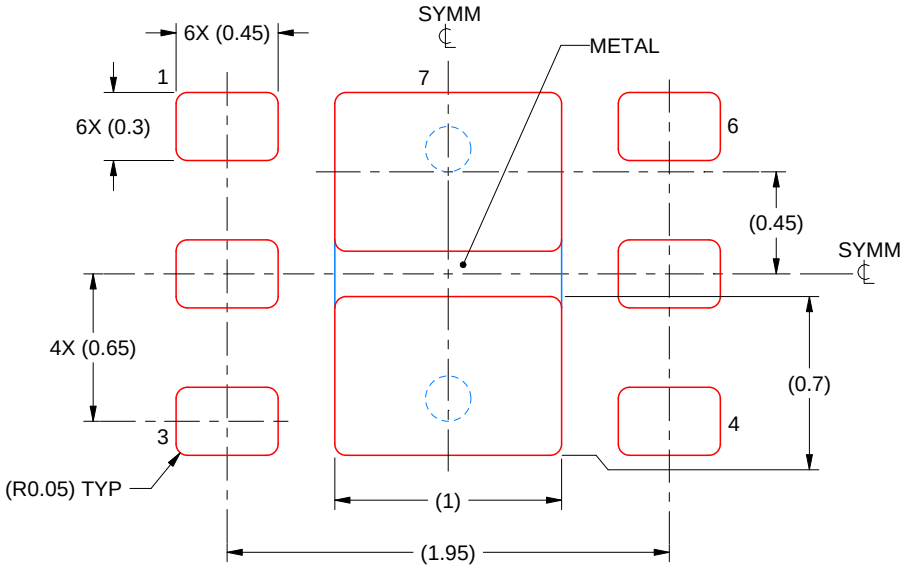


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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