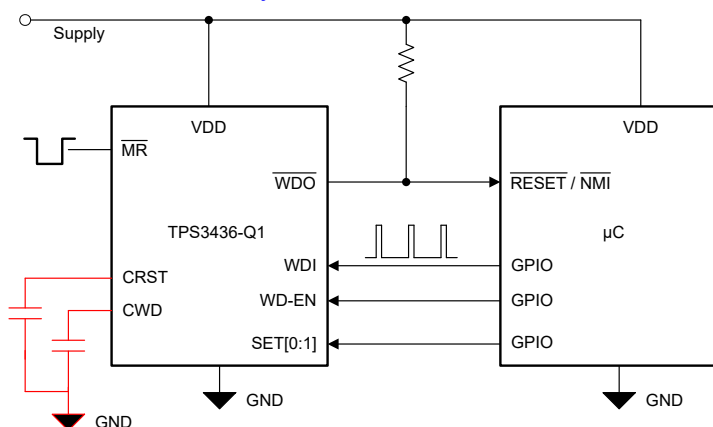**TEXAS INSTRUMENTS**

TPS3436-Q1 Automotive Nano IQ Precision Window Watchdog Timer

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Factory programmed or user-programmable watchdog timeout
  - ±10% Accurate timer (maximum)
  - Factory programmed close window: 1msec to 100 sec
- Factory programmed or user-programmable reset delay
  - ±10% Accurate timer (maximum)
  - Factory programmed option: 2 msec to 10 sec
- Input voltage range: V_{DD} = 1.04 V to 6.0 V
- Ultra low supply current: I_{DD} = 250 nA (typical)
- Open-drain, push-pull; active-low outputs
- Various programmability options:
  - Watchdog enable-disable
  - Watchdog startup delay: no delay to 10 sec
  - Open window to close window ratio option: 1X to 511X
  - Latched output option
- $\overline{MR}$ functionality support

2 Applications

- On-board (OBC) and wireless charger
- Driver monitoring
- Battery Management System (BMS)
- Front camera
- Surround view system ECU

3 Description

The TPS3436-Q1 is an ultra-low power consumption (250 nA typical) device offering a programmable window watchdog timer.

The TPS3436-Q1 offers a high accuracy window watchdog timer with host of features for a wide variety of applications. The close window timer can be factory programmed or user programmed using an external capacitor. The open window to close window ratio can be changed on-the-fly using a combination of logic pins. The watchdog also offers unique features such as enable-disable, start-up delay.

The $\overline{WDO}$ delay can be set by factory-programmed default delay settings or programmed by an external capacitor. The device also offers a latched output operation where the output is latched until the watchdog fault is cleared.

The TPS3436-Q1 provides a performance upgrade alternative to TPS3430-Q1 device family. The TPS3436-Q1 is available in a small 8-pin SOT-23 package.

Device Information

PART NUMBER	PACKAGE [1]	BODY SIZE (NOM)
TPS3436-Q1	DDF (8)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

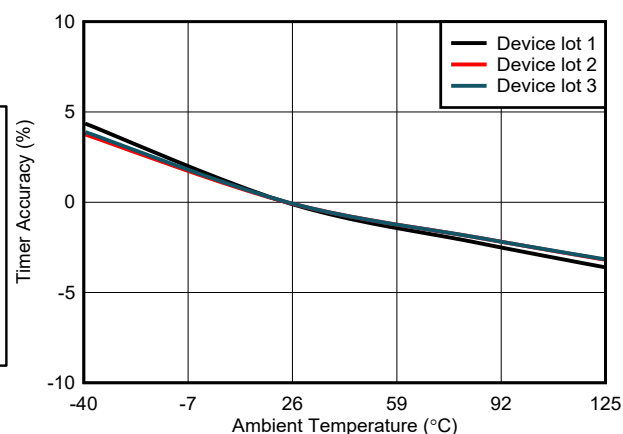TPS3436-Q1 offers various pinout options to support different features. Choose the suitable pinout based on application needs.

Typical Application Circuit
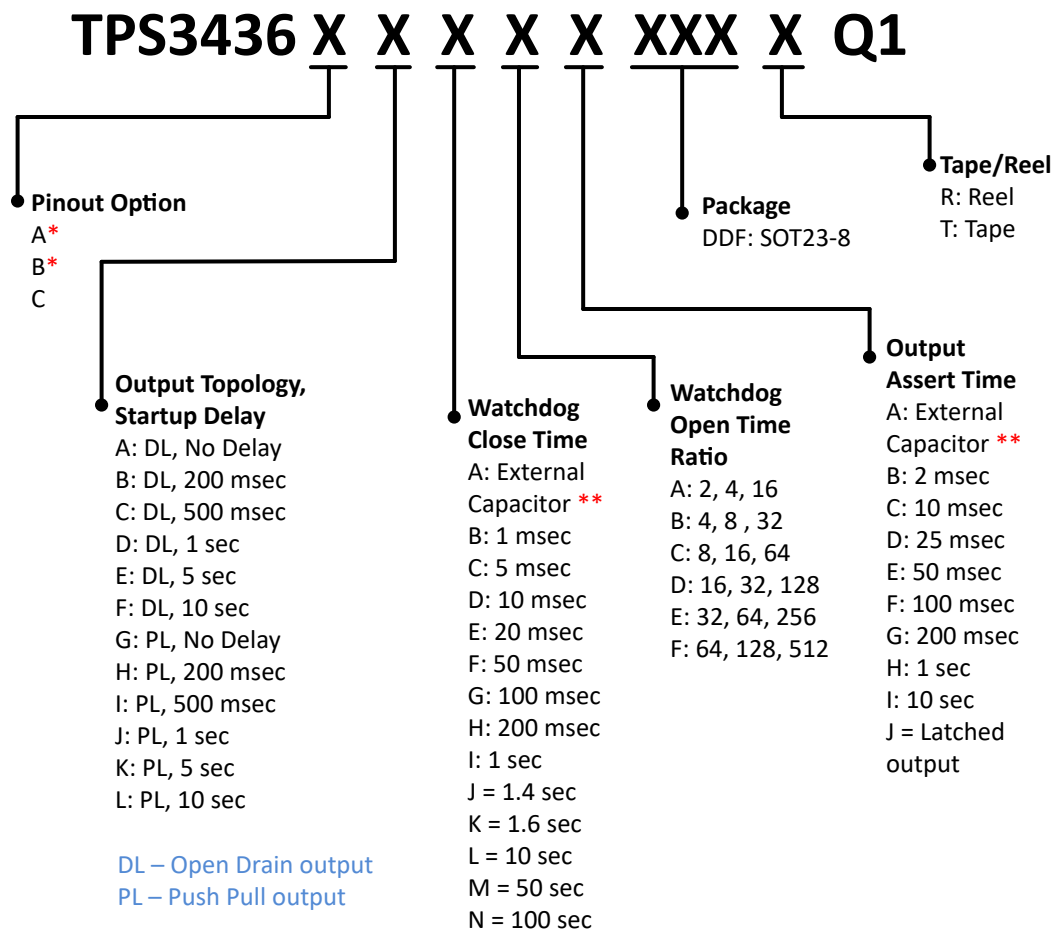
Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2022) to Revision A (June 2023)	**Page**
• Advance Information to Production Data release..	1

5 Device Comparison

Figure 5-1 shows the device naming nomenclature of the TPS3436-Q1. For all possible output types, watchdog time options and output assert delay options, see Section 8 for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.

TPS3436 X X X X X XXX X Q1

Pinout Option
A*
B*
C

Output Topology, Startup Delay
A: DL, No Delay
B: DL, 200 msec
C: DL, 500 msec
D: DL, 1 sec
E: DL, 5 sec
F: DL, 10 sec
G: PL, No Delay
H: PL, 200 msec
I: PL, 500 msec
J: PL, 1 sec
K: PL, 5 sec
L: PL, 10 sec

DL – Open Drain output
PL – Push Pull output

Watchdog Close Time
A: External Capacitor **
B: 1 msec
C: 5 msec
D: 10 msec
E: 20 msec
F: 50 msec
G: 100 msec
H: 200 msec
I: 1 sec
J = 1.4 sec
K = 1.6 sec
L = 10 sec
M = 50 sec
N = 100 sec

Watchdog Open Time Ratio
A: 2, 4, 16
B: 4, 8 , 32
C: 8, 16, 64
D: 16, 32, 128
E: 32, 64, 256
F: 64, 128, 512

Package
DDF: SOT23-8

Output Assert Time
A: External Capacitor **
B: 2 msec
C: 10 msec
D: 25 msec
E: 50 msec
F: 100 msec
G: 200 msec
H: 1 sec
I: 10 sec
J = Latched output

Tape/Reel
R: Reel
T: Tape

* Pinout option supports Start up Delay settings of "No Delay" and "10 sec" only.
** Capacitor programmable time feature available with pinout options A & B. For fixed time and latched output features use pinout option C.
Refer 'Mechanical, Packaging and Orderable Information' section for list of released orderable.
For any other orderable, contact local TI support.

Figure 5-1. Device Naming Nomenclature

TPS3436-Q1 belongs to family of pin compatible devices offering different feature sets as highlighted in Table 5-1.

Table 5-1. Pin Compatible Device Families

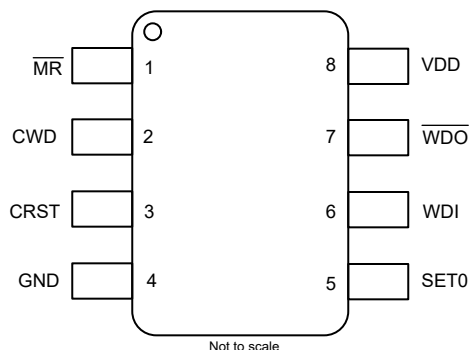| DEVICE	VOLTAGE SUPERVISOR	TYPE OF WATCHDOG
TPS35-Q1	Yes	Timeout
TPS36-Q1	Yes	Window
TPS3435-Q1	No	Timeout
TPS3436-Q1	No	Window

6 Pin Configuration and Functions

**Figure 6-1. Pin Configuration Option A
DDF Package, 8-Pin SOT-23,
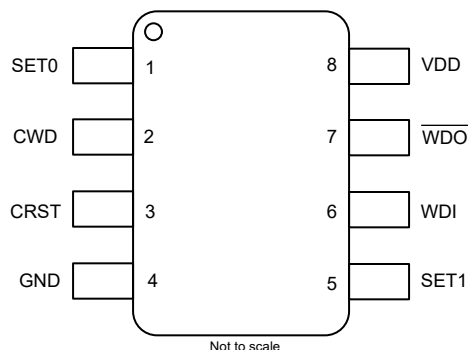TPS3436-Q1 Top View**

**Figure 6-2. Pin Configuration Option B
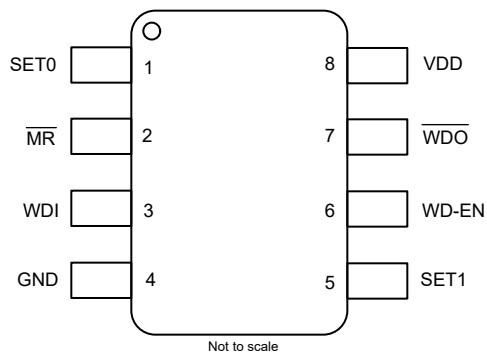DDF Package, 8-Pin SOT-23,
TPS3436-Q1 Top View**

**Figure 6-3. Pin Configuration Option C
DDF Package, 8-Pin SOT-23,
TPS3436-Q1 Top View**

Product Folder Links: *TPS3436-Q1*

Table 6-1. Pin Functions

PIN NAME	PIN NUMBER			I/O	DESCRIPTION
	PINOUT A	PINOUT B	PINOUT C		
CRST	3	3	—	I	Programmable WDO assert time pin. Connect a capacitor between this pin and GND to program the WDO assert time period. See *Section 8.3.3* for more details.
CWD	2	2	—	I	Programmable watchdog timeout input. Watchdog close time is set by connecting a capacitor between this pin and ground. See Section 8.3.1.1 for more details.
GND	4	4	4	—	Ground pin
$\overline{MR}$	1	—	2	I	Manual reset pin. A logic low on this pin asserts the $\overline{WDO}$ output. See *Section 8.3.2* for more details.
$\overline{WDO}$	7	7	7	O	Watchdog output. Connect $\overline{WDO}$ to VDD using pull up resistance when using open drain output. $\overline{WDO}$ is asserted when a watchdog error occurs or $\overline{MR}$ pin is driven LOW. See *Section 8.3.3* for more details.
SET0	5	1	1	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog window ratios and enable-disable the watchdog; see Section 8.3.1.5 for more details.
SET1	—	5	5	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog window ratios and enable-disable the watchdog; see Section 8.3.1.5 for more details.
VDD	8	8	8	I	Supply voltage pin. For noisy systems, connecting a 0.1-µF bypass capacitor is recommended.
WD-EN	—	—	6	I	Logic input. Logic high input enables the watchdog monitoring feature. See *Section 8.3.1.3* for more details.
WDI	6	6	3	I	Watchdog input. A falling transition (edge) must occur at this pin during the open window in order for $\overline{WDO}$ to not assert. See Section 8.3.1 for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted[1]

		MIN	MAX	UNIT
Voltage	VDD	−0.3	6.5	V
Voltage	C$_{WD}$, C$_{RST}$, WD–EN, SETx, WDI, $\overline{MR}$ [2], $\overline{WDO}$ (Push Pull)	−0.3	V$_{DD}$+0.3 [3]	V
	$\overline{WDO}$ (Open Drain)	−0.3	6.5	
Current	$\overline{WDO}$ pin	−20	20	mA
Temperature [4]	Operating ambient temperature, T$_A$	−40	125	℃
Temperature	Storage, T$_{stg}$	−65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If the logic signal driving $\overline{MR}$ is less than V$_{DD}$, then additional current flows into V$_{DD}$ and out of $\overline{MR}$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller
(4) As a result of the low dissipated power in this device, it is assumed that T$_J$ = T$_A$.

7.2 ESD Ratings

			VALUE	UNIT
V$_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (Active Low output)	0.9		6	V
	C$_{WD}$, C$_{RST}$, WD–EN, SETx, WDI, $\overline{MR}$ [1]	0		VDD	
	$\overline{WDO}$ (Open Drain)	0		6	
	$\overline{WDO}$ (Push Pull)	0		VDD	
Current	$\overline{WDO}$ pin current	−5		5	mA
C$_{RST}$	C$_{RST}$ pin capacitor range	1.5		1800	nF
C$_{WD}$	C$_{WD}$ pin capacitor range	1.5		1000	nF
T$_A$	Operating ambient temperature	−40		125	℃

(1) If the logic signal driving $\overline{MR}$ is less than V$_{DD}$, then additional current flows into V$_{DD}$ and out of $\overline{MR}$. V$_{MR}$ should not be higher than V$_{DD}$.

Product Folder Links: *TPS3436-Q1*

7.4 Thermal Information

THERMAL METRIC[1]		TPS3436-Q1	UNIT
		DDF (SOT23-8)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At 1.04 V ≤ V_{DD} ≤ 6 V, $\overline{MR}$ = Open, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40℃ to 125℃, unless otherwise noted. VDD ramp rate ≤ 1 V/µs. Typical values are at T_A = 25℃

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage	Active LOW output	1.04		6	V
I_{DD}	Supply current into VDD pin [1]	T_A = –40℃ to 85℃		0.25	0.8	µA
				0.25	3	
V_{IL}	Low level input voltage WD–EN, WDI, SETx, $\overline{MR}$ [3]				$0.3V_{DD}$	V
V_{IH}	High level input voltage WD–EN, WDI, SETx, $\overline{MR}$ [3]		$0.7V_{DD}$			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		kΩ
$\overline{WDO}$ (Open-drain active-low)						
V_{OL}	Low level output voltage	V_{DD} =1.5 V $I_{OUT(Sink)}$ = 500 µA			300	mV
		V_{DD} = 3.3 V $I_{OUT(Sink)}$ = 2 mA			300	
$I_{lkg(OD)}$	Open-Drain output leakage current	V_{DD} = V_{PULLUP} = 6V T_A = –40℃ to 85℃		10	30	nA
		V_{DD} = V_{PULLUP} = 6V		10	60	nA
$\overline{WDO}$ (Push-pull active-low)						
V_{POR}	Power on $\overline{WDO}$ voltage [5]	$V_{OH(min)}$ = 0.8 VDD $I_{out (source)}$ = 15 µA			900	mV
V_{OL}	Low level output voltage	V_{DD} = 1.5 V $I_{OUT(Sink)}$ = 500 µA			300	mV
		V_{DD} = 3.3 V $I_{OUT(Sink)}$ = 2 mA			300	
V_{OH}	High level output voltage	V_{DD} = 1.8 V $I_{OUT(Source)}$ = 500 µA	$0.8V_{DD}$			V
		V_{DD} = 3.3 V $I_{OUT(Source)}$ = 500 µA	$0.8V_{DD}$			
		V_{DD} = 6 V $I_{OUT(Source)}$ = 2 mA	$0.8V_{DD}$			

(1)   If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$.
(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state

7.6 Timing Requirements

At 1.04 V ≤ V_{DD} ≤ 6 V, $\overline{MR}$ = Open, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output RESET / WDO load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 1 V/μs. Typical values are at T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\overline{MR}\_PW}$	$\overline{MR}$ pin pulse duration to assert output			100		ns
t_{P-WD}	WDI pulse duration to start next frame [1]		500			ns
$t_{HD-WDEN}$	WD–EN hold time to enable or disable WD operation [1]		200			μs
$t_{HD-SETx}$	SETx hold time to change WD timer setting [1]		150			μs
t_{WC}	Watchdog close window time period	Orderable Option TPS3436xxB	0.8	1	1.2	ms
		Orderable Option TPS3436xxC	4	5	6	
		Orderable Option TPS3436xxD	9	10	11	
		Orderable Option TPS3436xxE	18	20	22	
		Orderable Option TPS3436xxF	45	50	55	
		Orderable Option TPS3436xxG	90	100	110	
		Orderable Option TPS3436xxH	180	200	220	
		Orderable Option TPS3436xxI	0.9	1	1.1	s
		Orderable Option TPS3436xxJ	1.26	1.4	1.54	
		Orderable Option TPS3436xxK	1.44	1.6	1.76	
		Orderable Option TPS3436xxL	9	10	11	
		Orderable Option TPS3436xxM	45	50	55	
		Orderable Option TPS3436xxN	90	100	110	
t_{WO}	Watchdog open window time period	SETx pin decide multipler n		$(n-1)$ X t_{WC}		ms

(1)   Not production tested

Product Folder Links: *TPS3436-Q1*

7.7 Switching Characteristics

At 1.04 V ≤ V_{DD} ≤ 6 V, $\overline{MR}$ = Open, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output RESET / WDO load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40℃ to 125℃, unless otherwise noted. VDD ramp rate ≤ 1 V/µs. Typical values are at T_A = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup delay [1]	C_{CRST} pin = Open or NC			500	µs
t_{SD}	Watchdog startup delay	Orderable part number TPS3436xA, TPS343xG		0		ms
		Orderable part number TPS3436xB, TPS3436xH	180	200	220	
		Orderable part number TPS3436xC, TPS3436xI	450	500	550	
		Orderable part number TPS3436xD, TPS3436xJ	0.9	1	1.1	s
		Orderable part number TPS3436xE, TPS3436xK	4.5	5	5.5	
		Orderable part number TPS3436xF, TPS3436xL	9	10	11	
t_{WDO}	Watchdog assert time delay	Orderable part number TPS3436xxxxB	1.6	2	2.4	ms
		Orderable part number TPS3436xxxxC	9	10	11	ms
		Orderable part number TPS3436xxxxD	22.5	25	27.5	ms
		Orderable part number TPS3436xxxxE	45	50	55	ms
		Orderable part number TPS3436xxxxF	90	100	110	ms
		Orderable part number TPS3436xxxxG	180	200	220	ms
		Orderable part number TPS3436xxxxH	0.9	1	1.1	s
		Orderable part number TPS3436xxxxI	9	10	11	s
$t_{\overline{MR}\_WDO}$	Propagation delay from $\overline{MR}$ low to WDO assertion	V_{DD} ≥ 1.25 V, $\overline{MR}$ = $V_{\overline{MR}\_H}$ to $V_{\overline{MR}\_L}$		100		ns

(1)   Specified by design parameter.

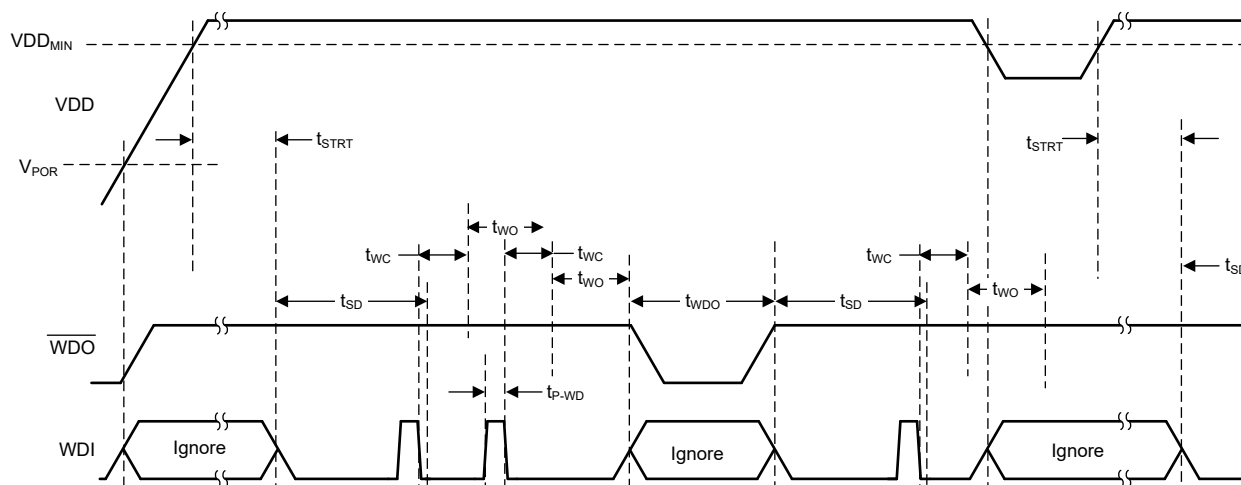Product Folder Links: *TPS3436-Q1*

7.8 Timing Diagrams

Figure 7-1. Functional Timing Diagram

7.9 Typical Characteristics

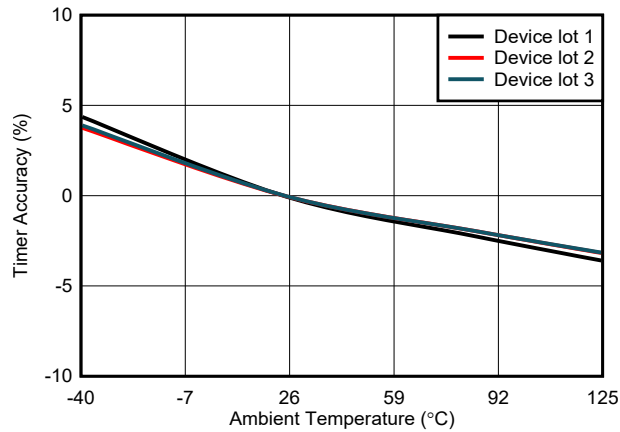all curves are taken at T_A = 25°C (unless otherwise noted)
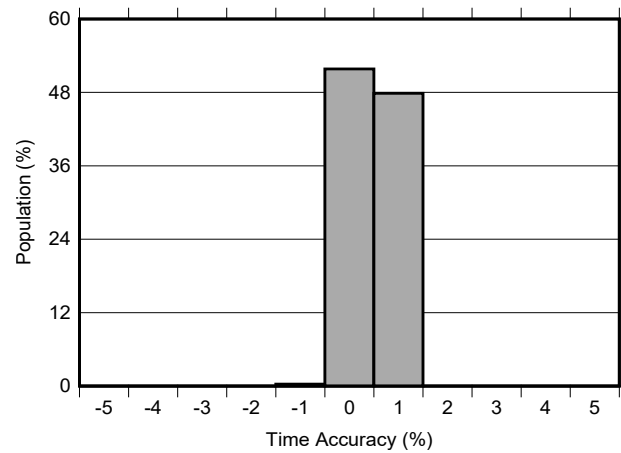

Figure 7-2. Timer Accuracy vs Temperature
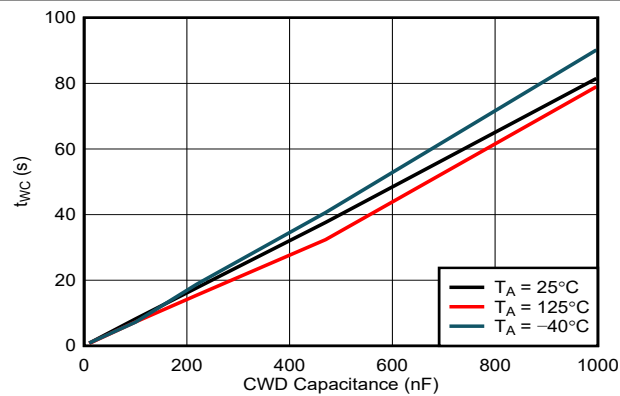

Figure 7-3. Timer Accuracy Histogram
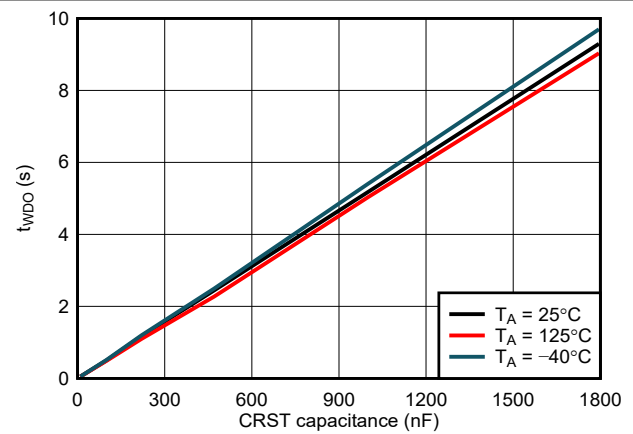

Figure 7-4. t_{WC} vs Capacitance
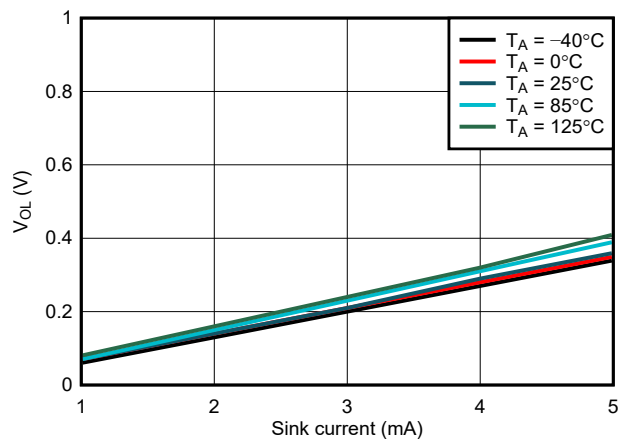

Figure 7-5. t_{WDO} vs Capacitance

Figure 7-6. WDO V_{OL} vs I_{sink}, V_{DD} = 1.5 V
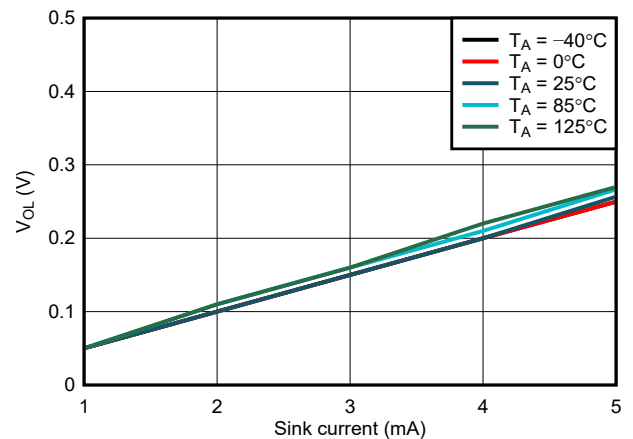
Figure 7-7. WDO V_{OL} vs I_{sink}, V_{DD} = 3.3 V

Product Folder Links: *TPS3436-Q1*

7.9 Typical Characteristics (continued)

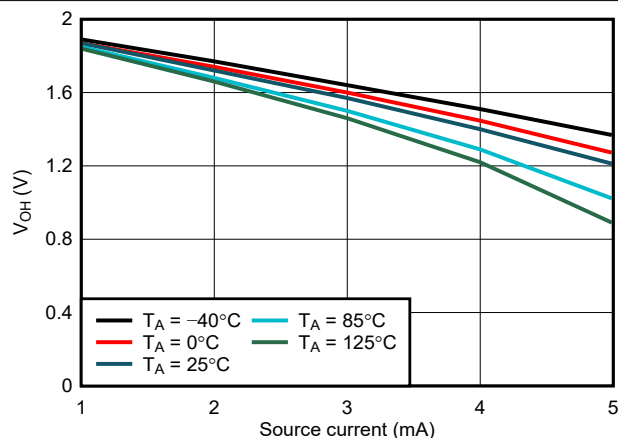all curves are taken at T_A = 25°C (unless otherwise noted)

Figure 7-8. WDO V_{OH} vs I_{source}, V_{DD} = 2.0 V

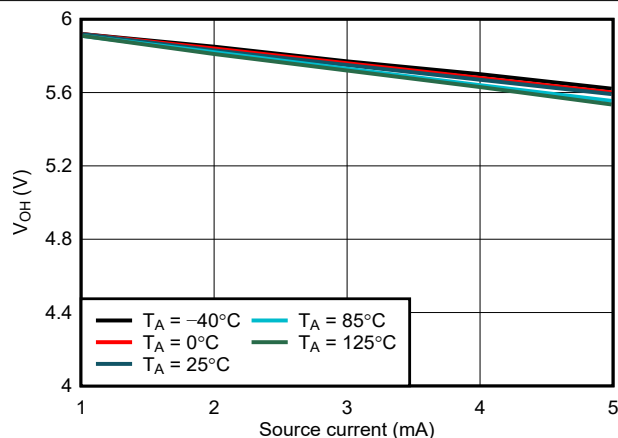**Figure 7-9. WDO V_{OH} vs I_{source}, V_{DD} = 6.0 V**
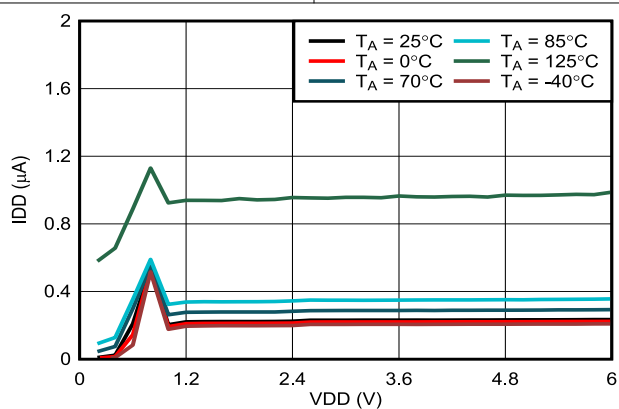
Figure 7-10. Supply Current vs Power-Supply Voltage

Product Folder Links: *TPS3436-Q1*

8 Detailed Description

8.1 Overview

The TPS3436-Q1 is a high-accuracy window watchdog timer device. The device family supports multiple features related to watchdog operation in a compact 8 pin SOT23 package. The devices are available in 3 different pinout configurations. Each pinout offers access to different features to meet the various application requirements. The device family is rated for -Q100 applications.
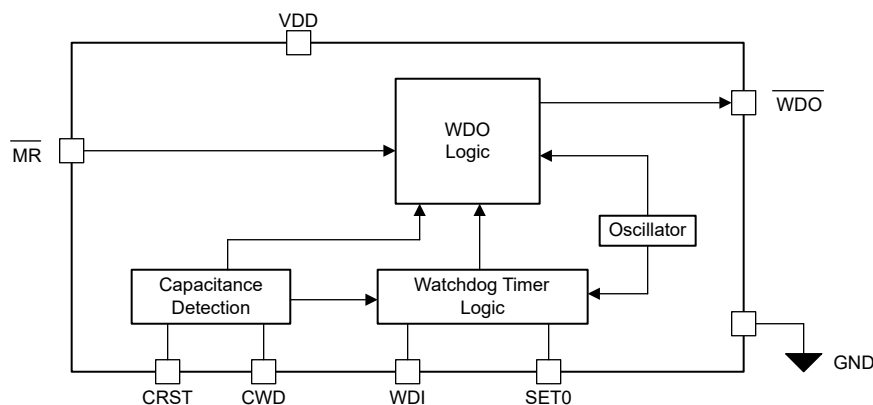
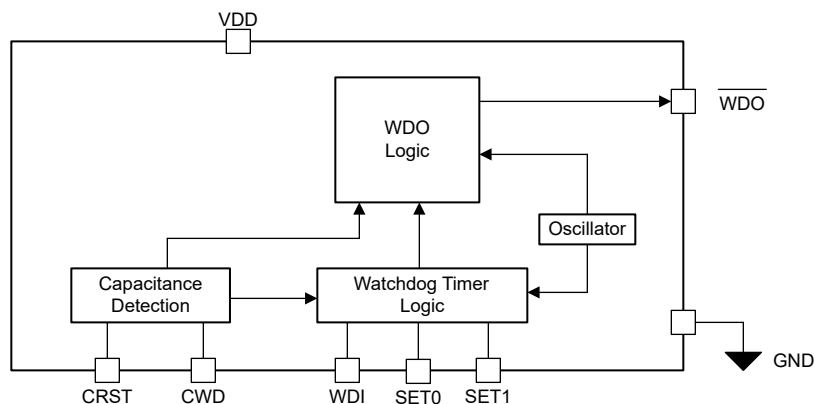## 8.2 Functional Block Diagrams

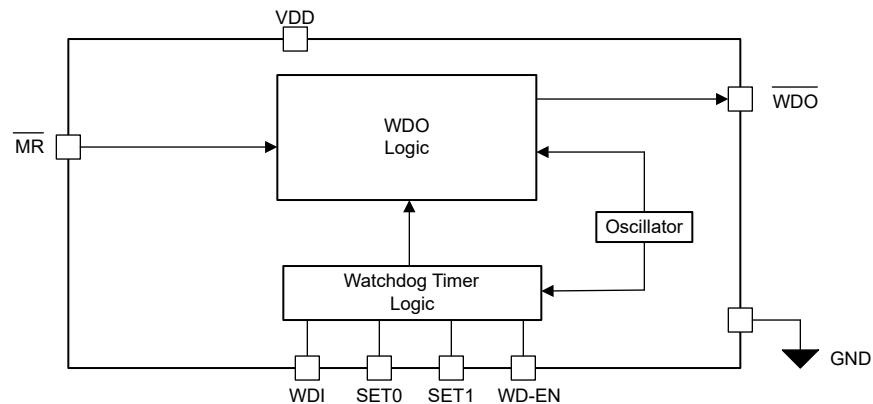**Figure 8-1. Pinout Option A**

Figure 8-2. Pinout Option B

Figure 8-3. Pinout Option C

Product Folder Links: *TPS3436-Q1*

8.3 Feature Description

8.3.1 Window Watchdog Timer

The TPS3436-Q1 offers high precision window watchdog timer monitoring. The device is available in multiple pinout options A to C which support multiple features to meet ever expanding needs of various applications. Ensure a correct pinout is selected to meet the application needs.

The window watchdog is active when the VDD voltage is higher than the VDD_{MIN}, $\overline{MR}$ voltage is held higher than 0.7 x VDD and watchdog is enabled. TPS3436-Q1 family offers various startup time delay options to ensure enough time is available for the host to complete boot operation. Please refer *Section 8.3.1.4* section for additional details.

The window watchdog timer frame consists of two windows namely close window (t_{WC}) followed by open window (t_{WO}). The device monitors the WDI pin for falling edge. User is expected to provide a valid falling edge on WDI pin in the open window. Refer *Section 5* to arrive at the relevant close window and open window values needed for application. The timer value is reset when a valid falling edge is detected on WDI pin in the t_{WO} time duration. An early fault is reported if a WDI falling edge is detected in close window. A late fault is reported if WDI falling edge is not detected in both close and open window. The device asserts WDO output for time t_{WDO} in event of watchdog fault. Refer *Section 8.3.3* to arrive at the relevant t_{WDO} value needed for application.

Figure 8-4 shows the basic operation for window watchdog timer operation. The TPS3436-Q1 watchdog functionality supports multiple features. Details are available in following sub sections.
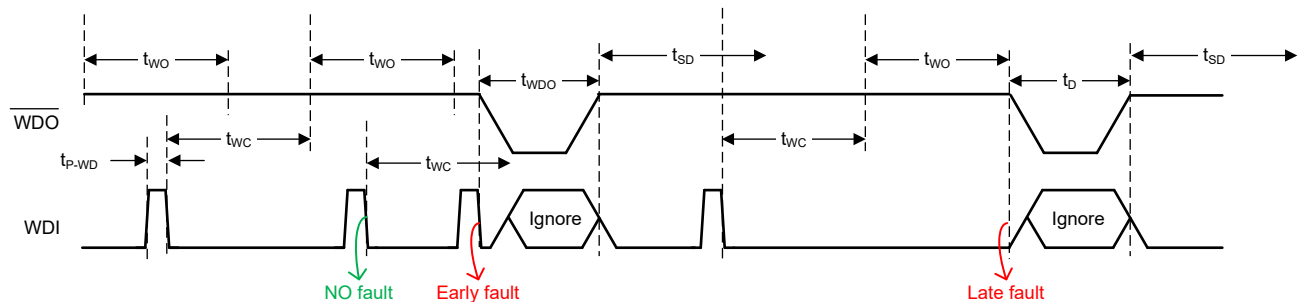

Figure 8-4. Window Watchdog Timer Operation

8.3.1.1 t_{WC} (Close Window) Timer

The window watchdog frame consists of two sub frames t_{WC} followed by t_{WO}. The host is not expected to drive valid WDI transition during t_{WC} time. A valid WDI transition during t_{WC} frame results in early fault condition and the WDO output is asserted. The t_{WC} timer for TPS3436-Q1 can be set using an external capacitor connected between CWD pin and GND pin. This feature is available with pinout options A or B. Applications which are space constrained or need timer values which meet offered timer options, can benefit when using pinout option C. The TPS3436-Q1 offers multiple fixed timer options ranging from 1 msec up-to 100 sec.

The TPS3436-Q1 when using capacitance based timer, senses the capacitance value during the power up. The capacitor is charged and discharged with known internal current source for one cycle to sense the capacitance value. The sensed value is used to arrive at t_{WC} timer for the watchdog operation. This unique implementation helps reduce the continuous charge and discharge current for the capacitor, thus reducing overall current consumption. Continuous charge and discharge of capacitance creates wider dead time (no watchdog monitor functionality) when capacitor is discharging. The dead time is higher for high value of capacitance. The unique implementation of TPS3436-Q1 helps avoid the dead time as the capacitance is not continuously charging or discharging under normal operation. Ensure C_{CWD} is < 200 x C_{CRST} for accurate calibration of capacitance. The close time window is decided based on SETx pin combination and the CWD capacitance. Table 8-1 to Table 8-2 highlights the relationship between t_{WC} in second and CWD capacitance in farad. The t_{WC} timer is 20% accurate for an ideal capacitor. Accuracy of the capacitance will have additional impact on the t_{WC} time. Ensure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

Table 8-1. t_{WC} Equation 1 SET Pin (Pin Configuration A)

SET PIN VALUE	EQUATION
0	t_{WC} (sec) = 79.2 x 10^6 x C_{CWD} (F)
1	t_{WC} (sec) = 39.6 x 10^6 x C_{CWD} (F)

Table 8-2. t_{WC} Equation 2 SET Pin, WD-EN Not Available (Pin Configuration B)

SET PIN VALUE	EQUATION
00	t_{WC} (sec) = 79.2 x 10^6 x C_{CWD} (F)
01	Watchdog disabled
10	t_{WC} (sec) = 39.6 x 10^6 x C_{CWD} (F)
11	t_{WC} (sec) = 9.9 x 10^6 x C_{CWD} (F)

The TPS3436-Q1 also offers wide selection of high accuracy fixed t_{WC} timer options starting from 1 msec to 100 sec including various industry standard values. The TPS3436-Q1 fixed time options are ±10% accurate for $t_{WC} \geq$ 10 msec. For $t_{WC} <$ 10 msec, the accuracy is ±20%. t_{WC} value relevant to application can be identified from the orderable part number. Refer *Section 5* to identify mapping of orderable part number to t_{WC} value.

8.3.1.2 t_{WO} (Open Window) Timer

The window watchdog frame consists of two sub frames t_{WC} followed by t_{WO}. The host is expected to drive valid WDI transition during t_{WO} time. A valid WDI transition before beginning of t_{WO} frame causes early fault condition. Failure to offer valid WDI transition during t_{WC} and t_{WO} frames results in late fault condition. When a fault condition is detected the WDO output is asserted.

The t_{WO} value is derived using t_{WC} value and the window open time ratio value *n*. Equation highlights the relationship between t_{WO} and t_{WC}. Refer Section 5 to select available ratio options.

$$t_{WO} = (n - 1) \times t_{WC} \tag{1}$$

Each orderable can offer up to 3 ratio options based on the available SET pins. Refer Section 8.3.1.5 to identify mapping of ratio value to SET pin control. The maximum t_{WO} value is limited to 640 second. Ensure selected t_{WC} and ratio combination does not lead to t_{WO} value greater than 640 second.

8.3.1.3 Watchdog Enable Disable Operation

The TPS3436-Q1 supports watchdog enable or disable functionality. This functionality is critical for different use cases as listed below.

- Disable watchdog during firmware update to avoid host RESET.
- Disable watchdog during software step-by-step debug operation.
- Disable watchdog when performing critical task to avoid watchdog error interrupt.
- Keep watchdog disabled until host boots up.

The TPS3436-Q1 supports watchdog enable or disable functionality through either WD-EN pin (pin configuration C) or SET[1:0] = 0b'01 (pin configuration B) logic combination. For a given pinout only one of these two methods is available for the user to disable watchdog operation.

For a pinout which offers a WD-EN pin, the watchdog enable disable functionality is controlled by the logic state of WD-EN pin. Drive WD-EN = 1 to enable the watchdog operation or drive WD-EN = 0 to disable the watchdog operation. The WD-EN pin can be toggled any time during the device operation. The Figure 8-5 diagram shows timing behavior with WD-EN pin control.
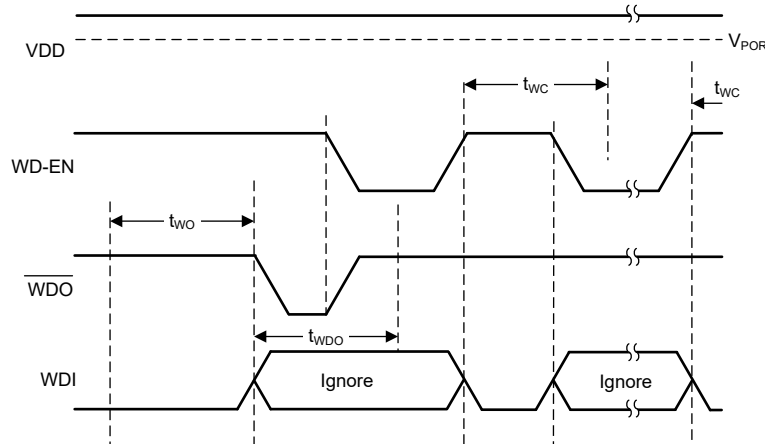
Figure 8-5. Watchdog Enable: WD-EN Pin Control

SET[1:0] = 0b'01 combination can be used to disable watchdog operation with a pinout which offers SET1 and SET0 pins, but does not include WD-EN pin. The SET pin logic states can be changed at any time during watchdog operation. Refer Section 8.3.1.5 section for additional details regarding SET[1:0] pin behavior.

Pinout options A, B offer watchdog timer control using a capacitance connected between CWD and GND pin. A capacitance value higher than recommended or connect to GND leads to watchdog functionality getting disabled. Capacitance based disable operation overrides the other two options mentioned above. Changing capacitance on the fly does not enable or disable watchdog operation. A power supply recycle is needed to detect change in capacitance.

Ongoing watchdog frame is terminated when watchdog is disabled. WDO stays deasserted when watchdog operation is disabled. When enabled the device immediately enters t_{WC} frame and start watchdog monitoring operation.

8.3.1.4 t_{SD} Watchdog Start Up Delay

The TPS3436-Q1 supports watchdog startup delay feature. This feature is activated after power up or after WDO assert event. When t_{SD} frame is active, the device monitors the WDI pin but the WDO output is not asserted. This feature allows time for the host complete boot process before watchdog monitoring can take over. The start up delay helps avoid unexpected WDO assert events during boot. The t_{SD} time is predetermined based on the device part number selected. Refer *Section 5* section for details to map the part number to t_{SD} time. Pinout option A, B are available only in no delay or 10 sec start up delay options.

The t_{SD} frame is complete when the time duration selected for t_{SD} is over or host provides a valid transition on the WDI pin. The host must provide a valid transition on the WDI pin during t_{SD} time. The device exits the t_{SD} frame and enters watchdog monitoring phase after valid WDI transition. Failure to provide valid transition on WDI pin triggers the watchdog error by asserting the WDO output pin.

The t_{SD} frame is not initiated when the watchdog functionality is enabled using WD-EN pin or SET[1:0] pin combination as described in *Section 8.3.1.3* section.

Figure 8-6 shows the operation for t_{SD} time frame.
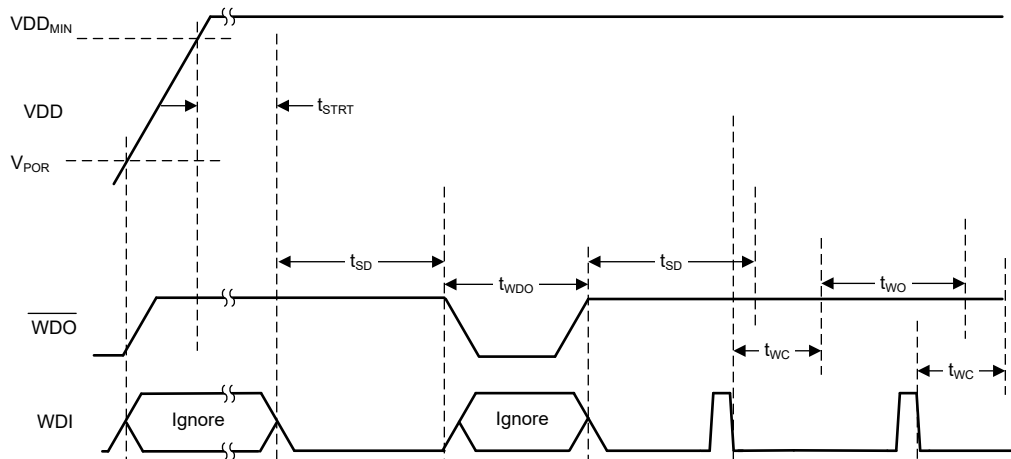
Figure 8-6. t_{SD} Frame Behavior

8.3.1.5 SET Pin Behavior

The TPS3436-Q1 offers one or two SET pins based on the pinout option selected. SET pins offer flexibility to the user to program the t_{WO} timer on the fly to meet various application requirements. Typical use cases where SET pin can be used are

- Use wide open window timer when host is in sleep mode, change to small timeout operation when host is operational. Watchdog can be used to wake up the host after long duration to perform the application related activities before going back to sleep.
- Change to wide open window timer when performing system critical tasks to ensure watchdog does not interrupt the critical task. Change timer to application specified interval after the critical task is complete.

The t_{WO} timer value for the device is combination of t_{WC} timer selection based on the CWD pin or fixed timer value along with SET pin logic level. The t_{WC} timer value is decided based on the Watchdog Close Time selector in the *Section 5* section. The SET pin logic level is decoded during the device power up. The SET pin value can be changed any time during the operation. SETx pin change which leads to change of watchdog timer value or enable disable state, terminates the ongoing watchdog frame immediately. SETx pins can be updated when WDO output is asserted as well. The updated t_{WO} timer value will be applied after output is deasserted and the t_{SD} timer is over or terminated.

For a pinout which offers only SET0 pin to the user, the t_{WO} ratio value is decided based on the Watchdog Open Time Ratio selector field in the orderable part number. Refer *Section 5* for available options. Table 8-3 showcases an example of the t_{WO} values for different SET0 logic levels when using Watchdog Close Time setting as option D = 10 msec.

Table 8-3. t_{WO} Values with SET0 Pin Only (Pin Configuration A)

Watchdog Open Time Ratio Selection	t_{WO}	
	SET0 = 0	SET0 = 1
A	10 msec	30 msec
B	30 msec	70 msec
C	70 msec	150 msec
D	150 msec	310 msec
E	310 msec	630 msec
F	630 msec	1270 msec

Pinout which offer both SET0 & SET1 pins to the user, the t_{WO} ratio value is decided based on the Watchdog Open Time Ratio selector field in the orderable part number. Refer *Section 5* for available options. Two SETx pins offer 3 different time scaling options. The SET[1:0] = 0b'01 combination disables the watchdog operation.

Table 8-4 showcases an example of the t_{WO} values for different SET[1:0] logic levels when using Watchdog Close Time setting as option G = 100 msec. The package pin out selected does not offer WD-EN pin.

Table 8-4. t_{WO} Values with SET0 & SET1 Pins, WD-EN Pin Not Available (Pin Configuration B)

Watchdog Open Time Ratio selection	t_{WO}			
	SET[1:0] = 0b'00	SET[1:0] = 0b'01	SET[1:0] = 0b'10	SET[1:0] = 0b'11
A	100 msec	Watchdog disable	300 msec	1500 msec
B	300 msec	Watchdog disable	700 msec	3100 msec
C	700 msec	Watchdog disable	1500 msec	6300 msec
D	1500 msec	Watchdog disable	3100 msec	12700 msec
E	3100 msec	Watchdog disable	6300 msec	25500 msec
F	6300 msec	Watchdog disable	12700 msec	51100 msec

1. Example for Watchdog Close Time setting = 100 msec.

Selected pinout option can offer WD-EN pin along with SET[1:0] pins (Pin Configuration C). With this pinout, the WD-EN pin controls watchdog enable and disable operation. The SET[1:0] = 0b'01 combination operates as SET[1:0] = 0b'00.

Ensure the t_{WO} value with SETx ratio does not exceed 640 sec. If a selection of close window timer and ratio results in t_{WO} > 640 sec, the timer value will be restricted to 640 sec.

Figure 8-7 to Figure 8-9 show the timing behavior with respect to SETx status changes.
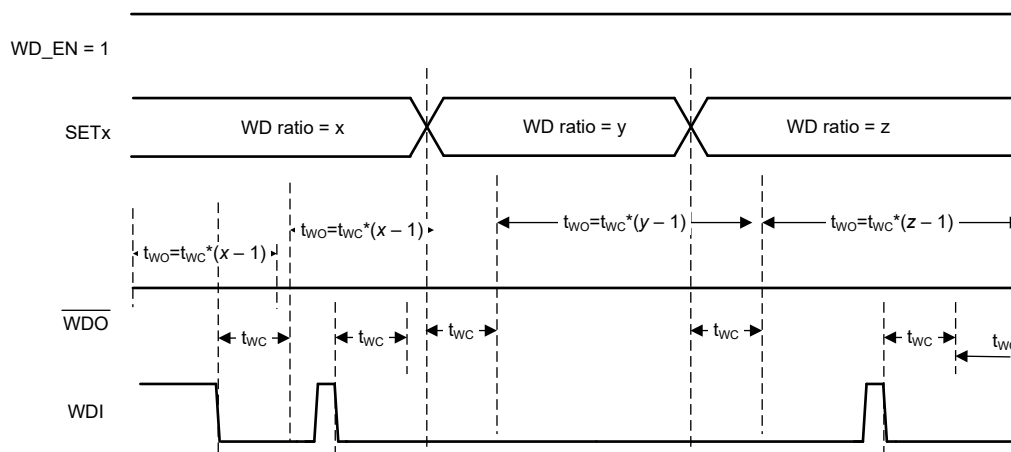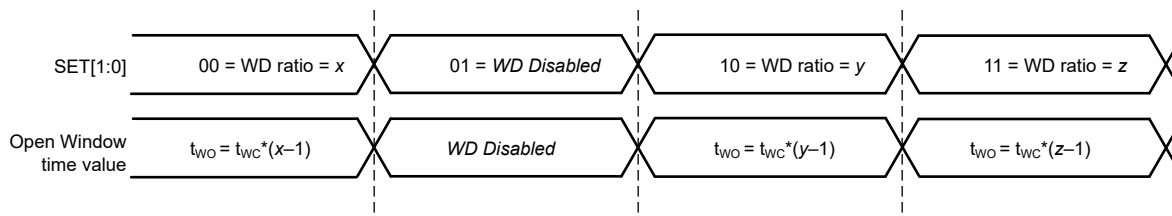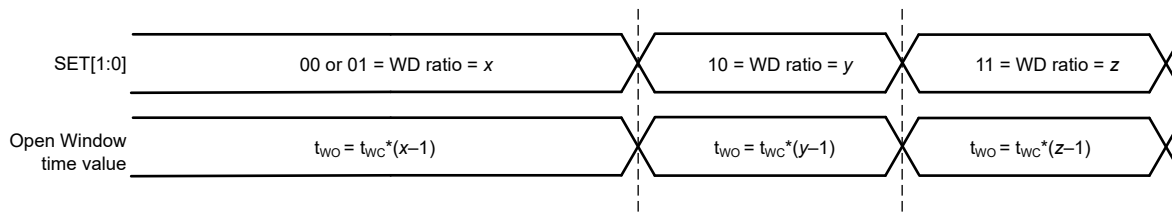

Figure 8-7. Watchdog Behavior with SETx Pin Status

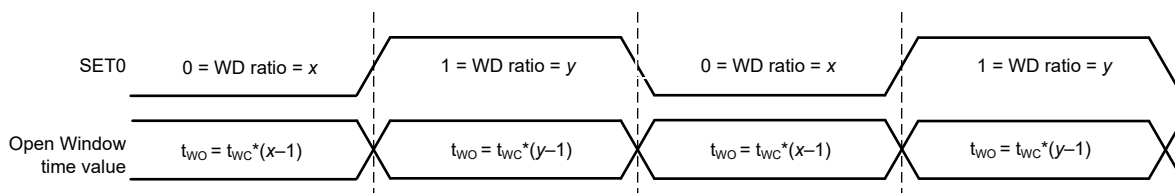**SET Pin (2 Pins) Operation; WD_EN Pin Not Available**

| SET[1:0] | 00 = WD ratio = x | 01 = *WD Disabled* | 10 = WD ratio = y | 11 = WD ratio = z |
| Open Window time value | $t_{WO} = t_{WC}*(x-1)$ | *WD Disabled* | $t_{WO} = t_{WC}*(y-1)$ | $t_{WO} = t_{WC}*(z-1)$ |

SET Pin (2 Pins) Operation; WD_EN Available = 1

| SET[1:0] | 00 or 01 = WD ratio = x | 10 = WD ratio = y | 11 = WD ratio = z |
| Open Window time value | $t_{WO} = t_{WC}*(x-1)$ | $t_{WO} = t_{WC}*(y-1)$ | $t_{WO} = t_{WC}*(z-1)$ |

t_{WC} = Fixed based on OPN or programmable using capacitor
x, y, z = Fixed based on ratio chosen

Figure 8-8. Watchdog Operation with 2 SET Pins

| SET0 | 0 = WD ratio = x | 1 = WD ratio = y | 0 = WD ratio = x | 1 = WD ratio = y |
| Open Window time value | $t_{WO} = t_{WC}*(x-1)$ | $t_{WO} = t_{WC}*(y-1)$ | $t_{WO} = t_{WC}*(x-1)$ | $t_{WO} = t_{WC}*(y-1)$ |

t_{WC} = Fixed based on OPN or programmable using capacitor
X, y = Fixed based on ratio chosen

Figure 8-9. Watchdog Operation with 1 SET Pin

Product Folder Links: *TPS3436-Q1*

8.3.2 Manual RESET

The TPS3436-Q1 supports manual reset functionality using $\overline{MR}$ pin. $\overline{MR}$ pin when driven with voltage lower than 0.3 x VDD, asserts the WDO output. The $\overline{MR}$ pin has 100 kΩ pull up to VDD. The $\overline{MR}$ pin can be left floating. The internal pull up makes sure the output is not asserted due to $\overline{MR}$ pin trigger.

The output is deasserted after $\overline{MR}$ pin voltage rises above 0.7 x VDD voltage. Refer Figure 8-10 for more details.
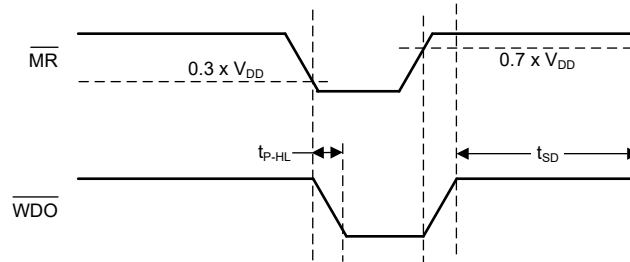

Figure 8-10. $\overline{MR}$ Pin Response

8.3.3 WDO Output

The TPS3436-Q1 device offers WDO output pin. WDO output is asserted when $\overline{MR}$ pin voltage is lower than 0.3 X VDD or watchdog timer error is detected.

The output will be asserted for t_{WDO} time when any relevant events described above are detected, except for $\overline{MR}$ event. The time t_{WDO} can be programmed by connecting a capacitor between CRST pin and GND or device will assert t_{WDO} for fixed time duration as selected by orderable part number. Refer *Section 5* section for all available options.

Equation 2 describes the relationship between capacitor value and the time t_{WDO}. Ensure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_{WDO} \text{ (sec)} = 4.95 \times 10^6 \times C_{CRST} \text{ (F)} \tag{2}$$

TPS3436-Q1 also offers a unique option of latched output. An orderable with latched output will hold the output in asserted state indefinitely until the device is power cycled or the error condition is addressed. If the output is latched due to $\overline{MR}$ pin low voltage, the output latch will be released when $\overline{MR}$ pin voltage rises above 0.7 x V_{DD} level. If the output is latched due to watchdog timer error, the output latch will be released when a WDI negative edge is detected or the device is shutdown and powered up again. *Figure 8-11* shows timing behavior of the device with latched output configuration.
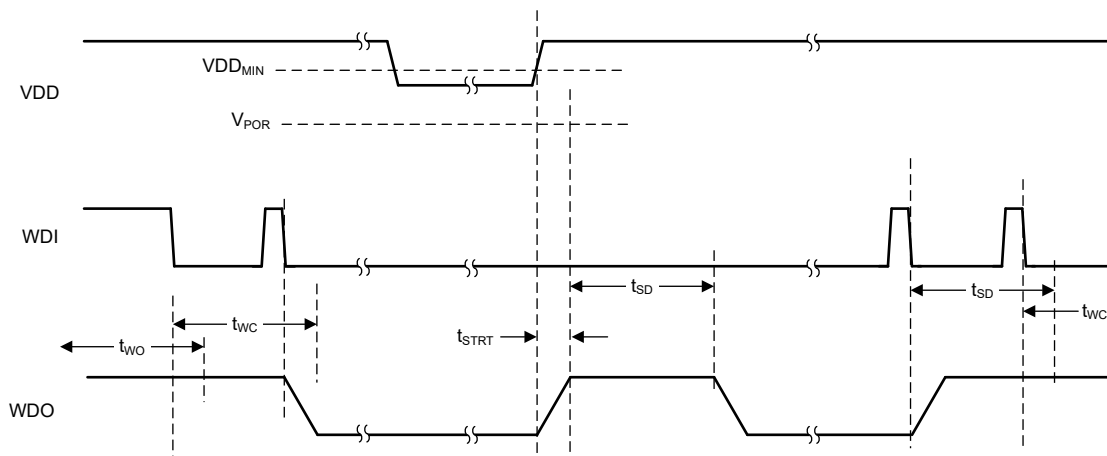

Figure 8-11. Output Latch Timing Behavior

Product Folder Links: *TPS3436-Q1*

8.4 Device Functional Modes

Table 8-5 summarizes the functional modes of the TPS3436-Q1.

Table 8-5. Device Functional Modes

VDD	WATCHDOG STATUS	WDI	$\overline{\text{WDO}}$
$V_{DD} < V_{POR}$	Not Applicable	—	Undefined
$V_{POR} \leq V_{DD} < V_{DDmin}$	Not Applicable	Ignored	High
$V_{DD} \geq V_{DDmin}$	Disabled	Ignored	High
	Enabled	$t_{WC(max)} \leq t_{pulse}$ [1] $\leq t_{WC(max)} + t_{WO(min)}$	High
	Enabled	$t_{WC(max)} > t_{pulse}$ [1]	Low
	Enabled	$t_{WC(max)} + t_{WO(max)} < t_{pulse}$ [1]	Low

(1)   Where t_{pulse} is the time between falling edges on WDI.

9 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

9.1.1 Output Assert Delay

The TPS3436-Q1 features two options for setting the output assert delay (t_{WDO}): using a fixed timing and programming the timing through an external capacitor.

9.1.1.1 Factory-Programmed Output Assert Delay Timing

Fixed output assert delay timings are available using pinout C . Using these timings enables a high-precision, 10% accurate output assert delay timing.

9.1.1.2 Adjustable Capacitor Timing

The TPS3436-Q1 also utilizes a programmable output assert delay, using a precision current source to charge an external capacitor upon device startup. The typical delay time resulting from a given external capacitance on the CRST pin can be calculated by Equation 3, where t_{WDO} is the output assert delay time in seconds and C_{CRST} is the capacitance in microfarads.

$$t_{WDO} \text{ (sec)} = 4.95 \times 10^6 \times C_{CRST} \text{ (F)} \tag{3}$$

Note that in order to minimize the difference between the calculated output assert delay time and the actual output assert delay time, use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. Table 9-1 lists the output assert delay time for ideal capacitor values.

Table 9-1. Output Assert Delay Time for Common Ideal Capacitor Values

C_{CRST}	OUTPUT ASSERT DELAY TIME (t_{WDO})			UNIT
	MIN[1]	TYP	MAX[1]	
10 nF	39.6	49.5	59.4	ms
100 nF	396	495	594	ms
1 µF	3960	4950	5940	ms

(1)   Minimum and maximum values are calculated using ideal capacitors.

9.1.2 Watchdog Window Functionality

The TPS3436-Q1 features two options for setting the close window watchdog timer (t_{WC}): using a fixed timing and programming the timing through an external capacitor.

9.1.2.1 Factory-Programmed Timing Options

Fixed watchdog timeout options are available using pinout C. Using these timings enables a high-precision, 10% accurate watchdog timer t_{WC}.

#### 9.1.2.2 Adjustable Capacitor Timing

Adjustable t_{WC} timing is achievable by connecting a capacitor to the CWD pin. If this method is used, please consult Table 8-1 to Table 8-2 for equations to calculate typical t_{WC} values using ideal capacitors as the effect

of C_{CWD} depends on the SETx pin values. Capacitor tolerances cause the actual device timing to vary such that the minimum of t_{WC} can decrease and the maximum of t_{WC} can increase by the capacitor tolerance. For the most accurate timing, use ceramic capacitors with COG dielectric material.

9.2 Typical Applications

9.2.1 Design 1: Monitoring a Microcontroller Watchdog During Operational and Sleep Modes

The TPS3436-Q1 can utilize high-accuracy voltage monitoring and on-the-fly SETx assigning to monitor a microcontroller that has both an operational and sleep mode.
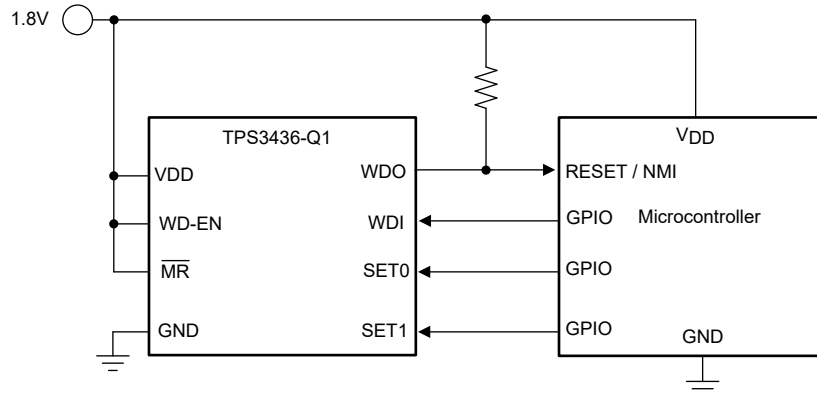
Copyright © 2023, Texas Instruments Incorporated

Figure 9-1. Microcontroller Window Watchdog Monitoring with Sleep Watchdog Mode

9.2.1.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Window Close Time During Operation	Typical t_{WC} of 50 ms during operation	Typical t_{WC} of 50ms
Window Open Time During Operation	Typical t_{WO} of 1.4 s during operation	Typical t_{WO} of 1.55 s
Window Close Time During Sleep	Typical t_{WC} of 50 ms during sleep	Typical t_{WC} of 50ms
Window Open Time During Sleep	Typical t_{WO} of 12 s during sleep	Typical t_{WO} of 12.75 s
Output Assert Delay	Typical t_{WDO} of 200 ms	Typical t_{WDO} of 200 ms
Output logic voltage	Open-drain	Open-drain
Maximum device current consumption	20 µA	250 nA typical current consumption

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Determining Window Timings During Operation and Sleep Modes

The TPS3436-Q1 allows for precise 10% accurate watchdog timings. This application requires two different window timings in order to maximize power efficiency: one for the microcontroller's operational state and one for its sleep state. To achieve this, the host can reassign the SETx pins when it transitions between states. A window close time, t_{WC}, of 50 ms typical is chosen because of the application's 50 ms typical t_{WC} requirement. The application requires a typical watchdog open time, t_{WO}, of 1.4 s during operation and a t_{WO} of 12 s during sleep. Thus, the possible variant options are narrowed to TPS3436xxFExDDFRQ1.

9.2.1.2.2 Meeting the Output Assert Delay

The TPS3436-Q1 features two options for selecting reset delays: fixed delays and capacitor-programmable delays. The TPS3436-Q1 supports only fixed watchdog timings and fixed output assert delays or programmable watchdog timings and programmable output assert delays. The application requires a 200 ms minimum output assert delay, thus output assert delay option G is used. Because of these requirements and no need for a startup delay, the TPS3436CAFEGDDFRQ1 is used.

9.2.1.2.3 Calculating the $\overline{\text{WDO}}$ Pullup Resistor

The TPS3436-Q1 uses an open-drain configuration for the $\overline{\text{WDO}}$ circuit, as shown in Figure 9-2. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below its maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{\text{WDO}}$ pin current (I_{RST}), and V_{OL}. The maximum V_{OL} is 0.3 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.3 V with I_{RST} kept below 2 mA for $V_{DD} \geq 3$ V and 500 µA for $V_{DD} = 1.5$ V. For this example, with a $V_{PU} = V_{DD} = 1.5$ V, a resistor must be chosen to keep I_{RST} below 500 µA because this value is the maximum consumption current allowed. To ensure this specification is met, a pullup resistor value of 10 kΩ was selected, which sinks a maximum of 180 µA when $\overline{\text{WDO}}$ is asserted.
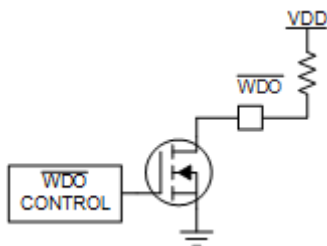

Figure 9-2. Open-Drain $\overline{\text{RESET}}$ Configuration

9.3 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.04 V and 6 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin.
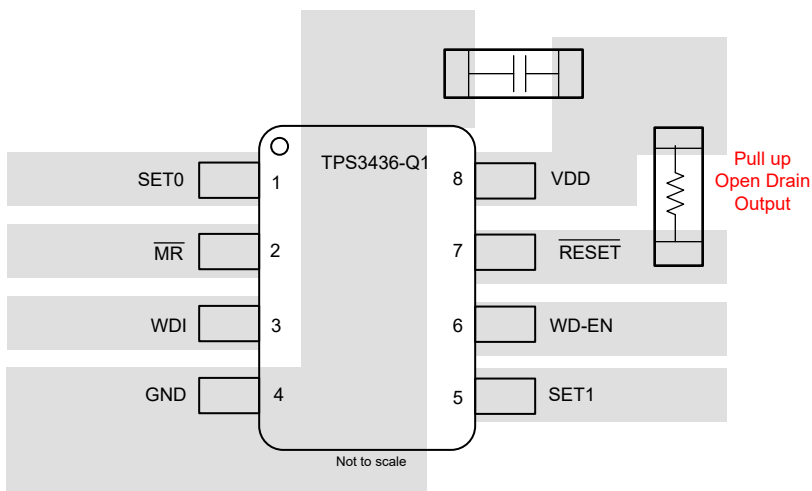
9.4 Layout

9.4.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1-µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the $\overline{\text{WDO}}$ delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- Place C_{CRST} capacitor as close as possible to the CRST pin.
- Place C_{CWD} capacitor as close as possible to the CWD pin.
- Place the pullup resistor on the $\overline{\text{WDO}}$ pin as close to the pin as possible.

9.4.2 Layout Example

Copyright © 2023, Texas Instruments Incorporated

Figure 9-3. Typical Layout for the Pinout C of TPS3436-Q1

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3436BFACADDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-45 to 125	NLHOI	Samples
TPS3436CCCBGDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

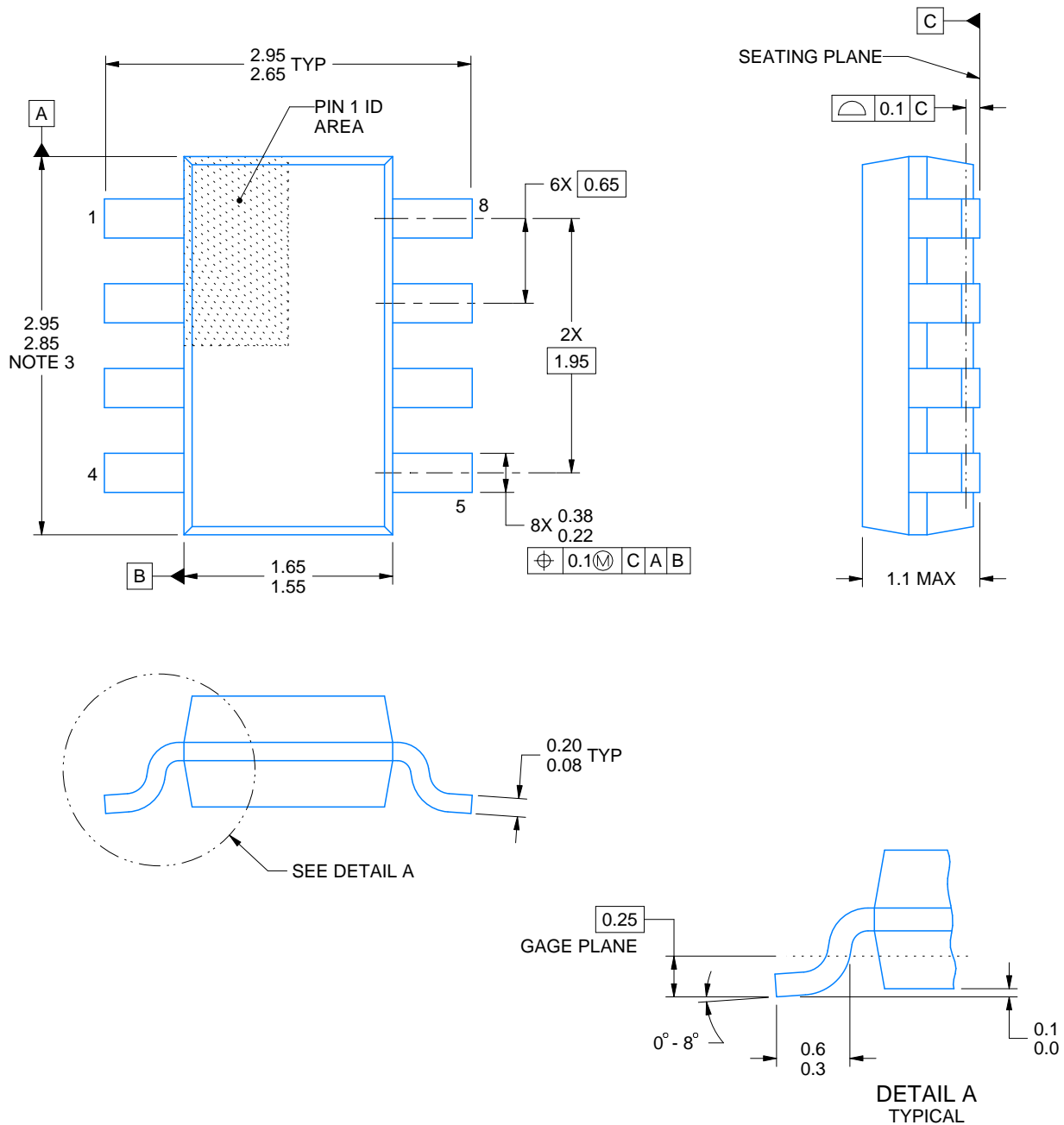## TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3436BFACADDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3436CCCBGDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3436BFACADDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3436CCCBGDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PLASTIC SMALL OUTLINE

2.95 / 2.65 TYP

A

PIN 1 ID AREA

1

2.95 / 2.85 NOTE 3

4

B

1.65 / 1.55

8

6X 0.65

2X 1.95

5

8X 0.38 / 0.22

⊕ 0.1 Ⓜ C A B

C

SEATING PLANE

◯ 0.1 C

1.1 MAX

SEE DETAIL A

0.20 / 0.08 TYP

0.25

GAGE PLANE

0° - 8°

0.6 / 0.3

0.1 / 0.0

DETAIL A
TYPICAL

4222047/C   10/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

8X (1.05)

SYMM

1

8X (0.45)

8

6X (0.65)

SYMM

4

5

(R0.05)
TYP

(2.6)

LAND PATTERN EXAMPLE
SCALE:15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING
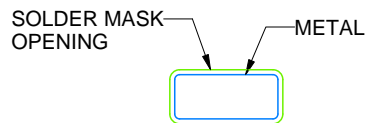
NON SOLDER MASK
DEFINED
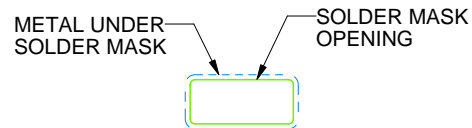
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C   10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.05)

1

8X (0.45)

6X (0.65)

4

SYMM

(R0.05) TYP

8

SYMM

5

(2.6)
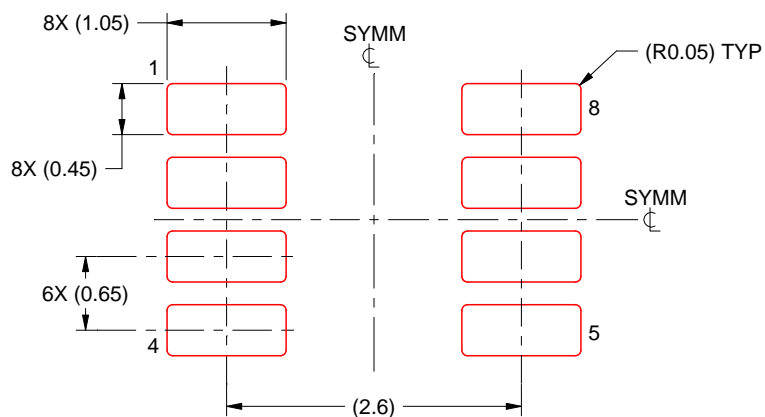
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C   10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER