TPS7H2140-SEP Radiation-Tolerant 32-V, 160-mΩ Quad-Channel eFuse

1 Features

- Vendor item drawing available, *VID V62/23610*
- Total ionizing dose (TID) characterized to 30 krad(Si)
  - RLAT (radiation lot acceptance testing) to 20 krad(Si)
- Single-event effects (SEE) characterized
  - Single-event latch-up (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune to linear energy transfer (LET) of 43 MeV-cm^2/mg
  - Single-event transient (SET) and single-event functional interrupt (SEFI) characterized to effective linear energy transfer (LET) of 43 MeV-cm^2/mg
- Quad-channel 160-mΩ eFuse with full diagnostics and current-sense analog output
- Wide operating voltage 4.5 V to 32 V
- Ultra-low standby current < 500 nA
- High-accuracy current sense: ±15% when I_{LOAD} ≥ 25 mA
- Adjustable current limit with external resistor (R_{CL}), with accuracy of ±15% when I_{LOAD} ≥ 500 mA
- Protection
  - Short-to-GND protection by current limit (internal or external)
  - Thermal shutdown with latch off option and thermal swing
  - Inductive load negative voltage clamp with optimized slew rate
  - Loss-of-GND and loss-of-power protection
- Diagnostics
  - Overcurrent and short-to-ground detection
  - Open-load and short-to-power detection
  - Global fault report for fast interrupt
- 28-pin thermally-enhanced PWP package
- Space Enhanced Plastic (SEP)
- Available in military (–55°C to 125°C) temp range

2 Applications

- Satellite electrical power systems (EPS)
- Space satellite power management and distribution
- Radiation-tolerant power tree applications
- Enables switching power rails for controlled power up and power down
- Solenoid driving

3 Description

The TPS7H2140-SEP device is a fully protected quad-channel eFuse with four integrated 160-mΩ NMOS power FETs.

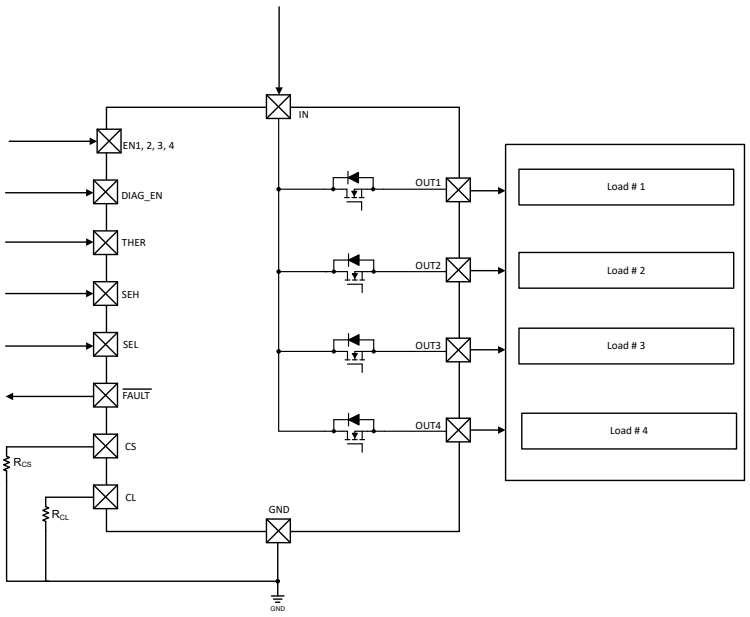
Full diagnostics and high-accuracy current sense enables intelligent control of the loads.

An external adjustable current limit improves the reliability of whole system by limiting the inrush or overload current.

Device Information

PART NUMBER(1)	GRADE(2)	BODY SIZE(4)
TPS7H2140MPWPTSEP	SEP	HTSSOP (28) 6.4 mm × 9.7 mm Mass = 124 mg(3)
TPS7H2140EVM	Evaluation module	Evaluation board

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) For additional information about part grade, view SLYB235.
(3) Mass is a nominal value.
(4) The body size (length × width) is a nominal value and does not include pins.



Typical Application Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2023) to Revision A (October 2023)	Page
• Changed document status from Advance Information to production data	1

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5 Pin Configuration and Functions

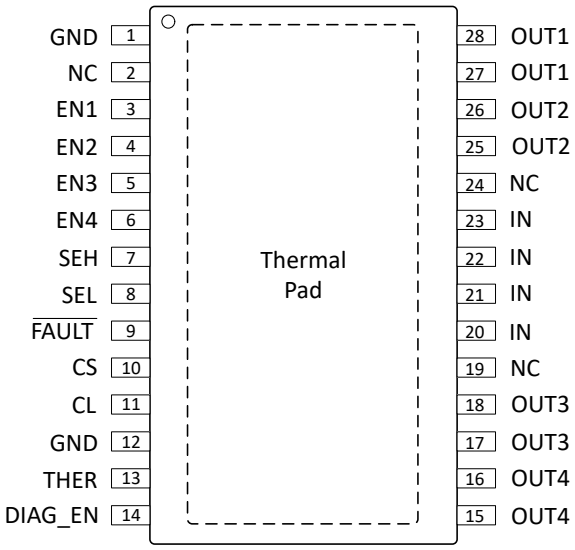

Figure 5-1. PWP Package
28-Pin HTSSOP With Exposed Thermal Pad
(Top View)

Table 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
CL	11	O	Adjustable current limit. Connect to device GND if external current limit is not used.
CS	10	O	Current-sense output.
DIAG_EN	14	I	Enable-disable pin for diagnostics; internal pulldown.
$\overline{\text{FAULT}}$	9	O	Global fault report with open-drain structure, ORed logic for quad-channel fault conditions.
GND	1, 12	—	Ground pin.
EN1	3	I	Input control for channel 1 activation; internal pulldown.
EN2	4	I	Input control for channel 2 activation; internal pulldown.
EN3	5	I	Input control for channel 3 activation; internal pulldown.
EN4	6	I	Input control for channel 4 activation; internal pulldown.
NC	2, 19, 24	—	No connect. This pin is not internally connected. It is recommended to connect this pin to GND to prevent charge buildup; however, this pin can also be left open or tied to any voltage between GND and IN.
SEH	7	I	CS channel-selection high bit; internal pulldown.
SEL	8	I	CS channel-selection low bit; internal pulldown.
THER	13	I	Thermal shutdown behavior control, latch off or auto-retry; internal pulldown.
OUT1	27, 28	O	Output of the channel 1 high side-switch, connected to the load.
OUT2	25, 26	O	Output of the channel 2 high side-switch, connected to the load.
OUT3	17, 18	O	Output of the channel 3 high side-switch, connected to the load.
OUT4	15, 16	O	Output of the channel 4 high side-switch, connected to the load.
IN	20, 21, 22, 23	I	Power supply.
Thermal pad	—	—	Connect to device GND or leave floating.

(1) I = Input, O = Other, — = Other

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage	IN (t < 400 ms)		48	V
	IN		35	
	Reverse polarity voltage (3)	–36		
	ENx, DIAG_EN, SEL, SEH, and THER	–0.3	7	
	$\overline{\text{FAULT}}$	–0.3	7	
	CS	–2.7	7	
	CL	–0.3	7	
Input and output current	ENx, DIAG_EN, SEL, SEH, and THER pins	–10		mA
	GND (t < 120 s)	–100	250	
	$\overline{\text{FAULT}}$	–30	10	
	CS		30	
	CL		6	
Input energy	Inductive load switch-off energy dissipation, single pulse, single channel(4)		40	mJ
Junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to GND.
(3) Reverse polarity condition:time t < 60 s, reverse current < I_{R2}, V_{ENx} = 0 V, GND pin 1-kΩ resistor in parallel with diode.
(4) Test condition: V_{IN} = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2 × 70-µm Cu, 2 × 35-µm Cu. 600 mm^2 thermal pad copper area.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	IN and VOUTx with respect to GND	±4000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except IN and VOUTx	±2000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	All pins	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	IN (1)	4.5	32	V
	ENx, DIAG_EN, SEL, SEH, and THER	0	5	
	$\overline{FAULT}$	0	5	
Output current	OUTx (3)	0	1.35	A
Ambient temperature	T_A	–55	125	°C

(1) All voltage values are with respect to GND.
(2) Transients up to the absolute maximum is allowed.
(3) All channel on.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H2140-SEP HTSSOP (PWP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	8	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over 4.5 V ≤ V_{IN} ≤ 32 V, temperature range (−55°C ≤ T_A ≤ 125°C), unless otherwise specified (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPERATING VOLTAGE							
IN_{UVLOR}	Internal V_{IN} UVLO rising			3.5	3.7	4	V
IN_{UVLOF}	Internal V_{IN} UVLO falling			3	3.2	3.4	
$HYST_{IN-UVLO}$	Internal V_{IN} UVLO hysteresis				0.5		
OPERATING CURRENT							
I_Q	Quiescent current with diagnostics disabled	ENx = 5 V, DIAG_EN = 0 V, I_{OUTx} = 0 A, current limit = 2 A, all channels on				7.0	mA
I_{Q_DIAG}	Quiescent current with diagnostics enabled	ENx = DIAG_EN = 5 V, I_{OUTx} = 0 A, current limit = 2 A, all channels on				6.2	
I_{SD}	Shutdown current with diagnostics disabled	ENx = DIAG_EN = OUTx = THER = 0 V	T_A=25°C			0.5	µA
			T_A=125°C			5	
I_{SD_DIAG}	Shutdown current with diagnostic enabled	ENx = 0 V, DIAG_EN = 5 V, V_{IN} – V_{OUTx} < V_{OL_OFF}, not in open-load mode				5	mA
t_{LOW_OFF}	ENx signal low time during cycling	ENx from high to low, if elapsed time > t_{LOW_OFF}, the device enters into standby mode		10	12.5	15	ms
I_F	IN to OUTx forward leakage current	ENx = DIAG_EN = OUTx = 0	T_A = 25°C			0.5	µA
		ENx = DIAG_EN = OUTx = 0	T_A = 125°C			8	

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6.5 Electrical Characteristics (continued)

over 4.5 V ≤ V_{IN} ≤ 32 V, temperature range (−55°C ≤ T_A ≤ 125°C), unless otherwise specified (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER STAGE							
R_{ON}	On-state resistance		T_A = 25°C		165		mΩ
			T_A = 125°C			280	
ΔR_{ON}	Percentage Difference in On-state resistance between channels (R_{ON_CHx} – R_{ON_CHy})		T_A = 25°C			6%	
$I_{CL_INTERNAL}$	Internal current limit	Internal current limit value, CL pin connected to GND			11		A
$I_{CL_INTERNAL_TSD}$	Current limit during thermal shutdown	Internal current limit value under thermal shutdown			6.5		
I_{CL_TSD}	Current limit during thermal shutdown	External current limit value under thermal shutdown. The percentage of the external current limit setting value			70%		
V_{DS_CLAMP}	Source-to-drain body diode voltage			50		70	V
OUTPUT DIODE CHARACTERISTICS							
V_F	Drain−source diode voltage	ENx = 0, I_{OUTX} = −0.15 A.		0.3	0.7	0.9	V
I_{R1}	Continuous reverse current from source to drain	t < 60 s, V_{IN} = 24 V, ENx = 0 V. Single channel reversed current to supply	T_A = 25°C		2.5		A
I_{R2}	Continuous reverse current from source to drain	t < 60 s, V_{IN} = 24 V, ENx = 0 V. GND pin 1-kΩ resistor in parallel with diode. Reverse-current condition, All channels reversed	T_A = 25°C		2.0		
LOGIC INPUT (ENx, DIAG_EN, SEL, SEH, THER)							
V_{IH}	Logic high-level voltage			2			V
V_{IL}	Logic low-level voltage					0.8	
R_{PULL_DOWN}	Logic-pin pulldown resistor	V_{IN} = V_{DIAG_EN} = 5 V		200	275	350	kΩ
		V_{IN} = V_{ENx} = V_{SEL} = V_{SEH} = V_{THER} = 5 V		100	175	250	
DIAGNOSTICS							
I_{GND_LOSS}	Output leakage current under GND loss condition					100	µA
V_{OL_OFF}	Open load detection threshold	V_{ENx} = 0 V, when V_{IN} – V_{OUTx} > V_{OL_OFF}. Duration longer than t_{OL_OFF}, then open load is detected, off state.		1.6		2.6	V
t_{OL_OFF}	Open-load detection threshold deglitch time	V_{ENx} = 0 V, when V_{IN} – V_{OUTx}> V_{OL_OFF}. Duration longer than t_{OL_OFF}, then open load is detected, off state		300	550	800	µs
I_{OL_OFF}	Off-state output sink current	V_{ENx} = 0 V, V_{DIAG_EN}= 5 V, V_{IN} – V_{OUTx} = 24 V, open load	T_A = 125°C			100	µA
$V_{OL_\overline{FAULT}}$	Fault low-output voltage	$I_{\overline{FAULT}}$ = 2 mA				0.2	V
$t_{CL_DEGLITCH}$	Deglitch time when current limit occurs	ENx = DIAG_EN = 5 V. The deglitch time from current limit event to $\overline{FAULT}$ = Low and V_{CS_FAULT}				220	µs
T_{SD}	Thermal shutdown threshold			160	175		°C
T_{SD_RST}	Thermal shutdown status reset threshold				155		
T_{sw}	Thermal swing shutdown threshold				60		
T_{HYS}	Hysteresis for resetting the thermal shutdown or thermal swing				10		
CURRENT SENSE AND CURRENT LIMIT							
K_{CS}	Current sense ratio				300		
K_{CL}	Current limit ratio				2500		
V_{CL_TH}	Current limit internal threshold voltage(3)				0.8		V
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) / I_{OUT} × 100	V_{IN} = 13.5 V, I_{OUTx} ≥ 5 mA		–65%		65%	
dK_{CS} / K_{CS}		V_{IN} = 13.5 V, I_{OUTx} ≥ 25 mA		–15%		15%	
dK_{CS} / K_{CS}		V_{IN} = 13.5 V, I_{OUTx} ≥ 50 mA		–8%		8%	
dK_{CS} / K_{CS}		V_{IN} = 13.5 V, I_{OUTx} ≥ 100 mA		–4%		4%	

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6.5 Electrical Characteristics (continued)

over 4.5 V ≤ V_{IN} ≤ 32 V, temperature range (−55°C ≤ T_A ≤ 125°C), unless otherwise specified (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
dK_{CL} / K_{CL}	External current limit accuracy, (I_{OUTx} – I_{CL} × K_{CL}) × 100 / (I_{CL} × K_{CL})	V_{IN} = 13.5 V, I_{LIMIT} ≥ 250 mA		–20%		20%	
		V_{IN} = 13.5 V, 2 A ≤ I_{LIMIT} ≤ 4 A		–15%		15%	
V_{CS_LINEAR}	Current-sense voltage linear range	V_{IN} ≥ 6.5 V		0		4	V
		5 V ≤ V_{IN} < 6.5 V		0		V_{IN} – 2.5	
I_{OUTx_LINEAR}	Output-current linear range	V_{IN} ≥ 6.5 V, V_{CS_LINEAR} ≤ 4 V		0		2.5	A
		5 V ≤ V_{IN} < 6.5 V, V_{CS_LINEAR} ≤ V_{IN} – 2.5 V		0		2.5	
$V_{CS_\overline{FAULT}}$	Current sense pin output voltage	V_{IN} ≥ 7 V, $\overline{FAULT}$ mode		4.5		6.5	V
		5 V ≤ V_{IN} < 7 V, $\overline{FAULT}$ mode		Min(V_{IN} – 2.3, 4.5)		6.5	
$I_{CS_\overline{FAULT}}$	Current-sense pin output current available in fault mode	V_{CS} = 4.5 V, V_{IN} > 7 V		15			mA
I_{CS_LEAK}	Current-sense leakage current in disabled mode	V_{DIAG_EN} = 0 V	T_A = 125ºC			0.5	µA

(1) All voltage values are with respect to GND.
(2) V_{CL_TH} tolerance is included in the dK_{CL} / K_{CL} tolerance.

6.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER STAGE						
t_{ON}	Turn-on delay time	V_{IN} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 500 mA, from ENx rising edge to 10% of V_{OUTx}	20	50	90	µs
t_{OFF}	Turn-off delay time	V_{IN} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 500 mA, from ENx falling edge to 90% of V_{OUTx}	20	50	90	
t_{RISE}	Channel turn-on time	V_{IN} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 500 mA, from 50% of ENx to 90% of V_{OUTx}	66	88	125	
t_{FALL}	Channel turn-off time	V_{IN} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 500 mA, from 50% of ENx to 10% of V_{OUTx}	66	88	125	
t_{MATCH}	t_{RISE} – t_{FALL}	V_{IN} = 13.5 V, I_{OUT} = 500 mA. t_{RISE} is the ENx rising edge to V_{OUTx} = 90%. t_{FALL} is the ENx falling edge to V_{OUTx} = 10%.	–50		50	
SR_{ON}	Turn-on slew rate	V_{IN} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 500 mA, from ENx rising edge to 10% of V_{OUTx}	0.1	0.3	0.55	V/µs
SR_{OFF}	Turn-off slew rate	V_{IN} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 500 mA, from ENx falling edge to 90% of V_{OUTx}	0.1	0.3	0.55	
CURRENT SENSE						
t_{CS_OFF1}	CS settling time from DIAG_EN disabled	V_{IN} = 13.5 V, V_{ENx} = 5 V, I_{OUTx} = 500 mA. Current Limit = 2 A. From V_{DIAG_EN} falling edge to 10% of V_{CS}.			20	µs
t_{CS_ON1}	CS settling time from DIAG_EN enabled	V_{IN} = 13.5 V, V_{ENx} = 5 V, I_{OUTx} = 500 mA. Current Limit = 2 A. From V_{DIAG_EN} rising edge to 90% of V_{CS}.			20	
t_{CS_OFF2}	CS settling time from IN falling edge	V_{IN} = 13.5 V, V_{ENx} = 5 V, I_{OUTx} = 500 mA. Current Limit = 2 A. From V_{ENx} falling edge to 10% of V_{CS}.	30		100	
t_{CS_ON2}	CS settling time from IN rising edge	V_{IN} = 13.5 V, V_{ENx} = 5 V, I_{OUTx} = 500 mA. Current Limit = 2 A. From V_{ENx} rising edge to 90% of V_{CS}.	50		150	
t_{MUX}	Multi-sense transition delay from channel to channel	V_{DIAG_EN} = 5V, current sense output delay when multi-sense pins SEL and SEH transition from channel to channel			50	

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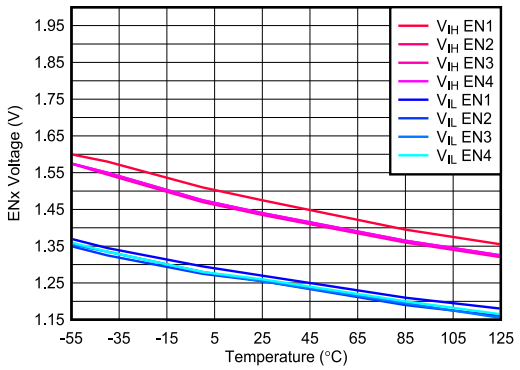
6.7 Typical Characteristics



V_{IN} = 12 V

Figure 6-1. ENx Voltage Threshold

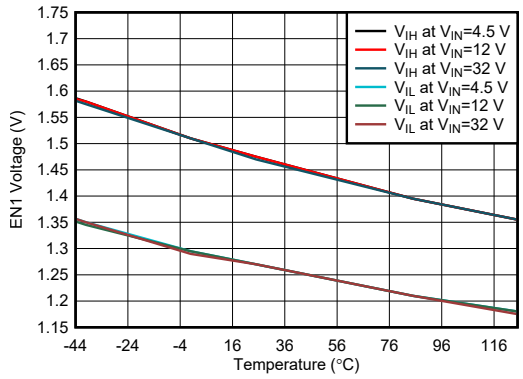
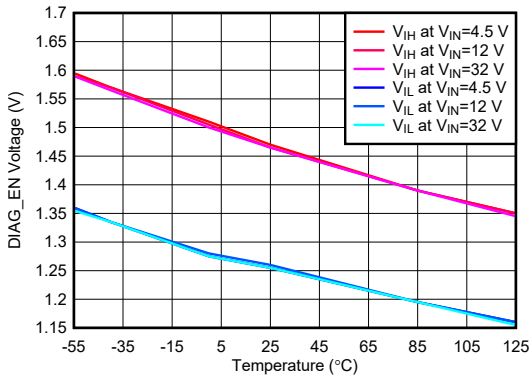
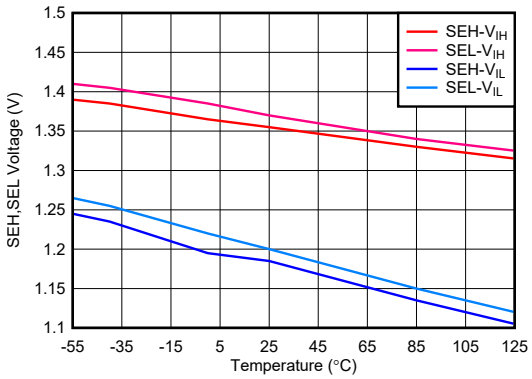


Figure 6-2. EN1 Voltage Threshold vs V_{IN}



V_{IN} = 12 V

Figure 6-3. DIAG_EN Voltage Threshold



V_{IN} = 12 V

Figure 6-4. SEH,SEL Voltage Threshold

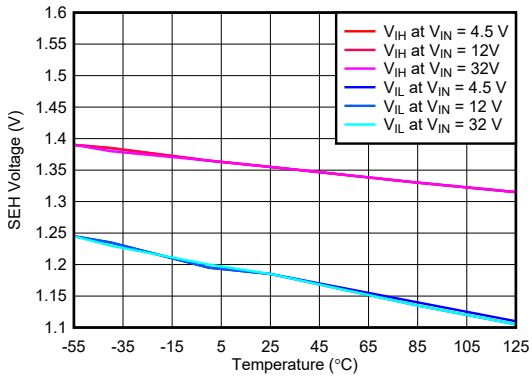
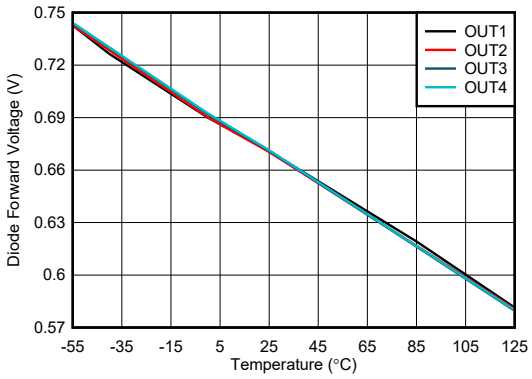


Figure 6-5. SEH Voltage Threshold vs V_{IN}



I_{Fx} = 150 mA

Figure 6-6. Body-Diode Forward Voltage

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6.7 Typical Characteristics (continued)

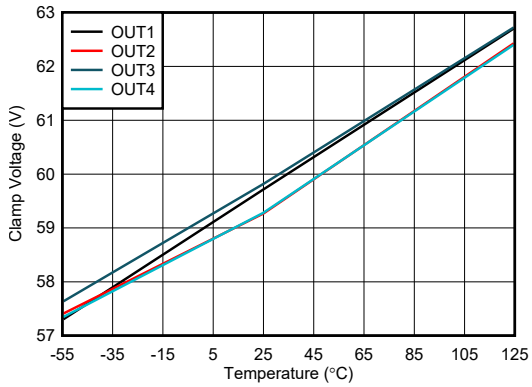
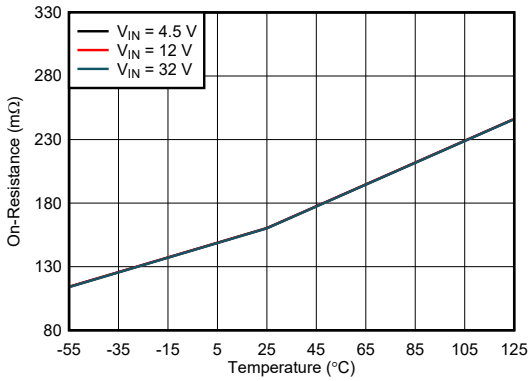
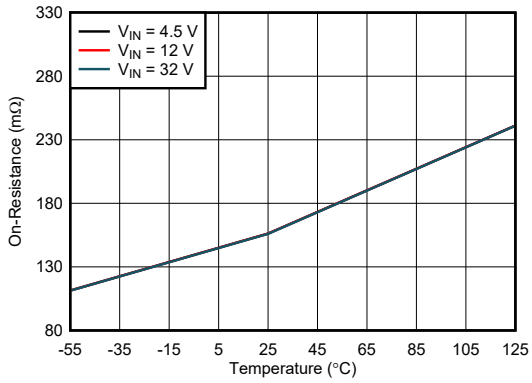


Figure 6-7. Drain-to-Source Clamp Voltage



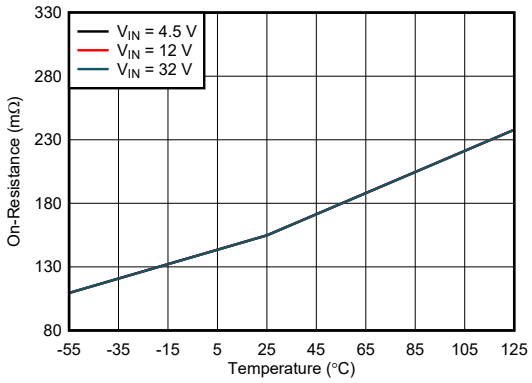
I_{OUT1} = 490 mA

Figure 6-8. Channel-1 FET On-Resistance



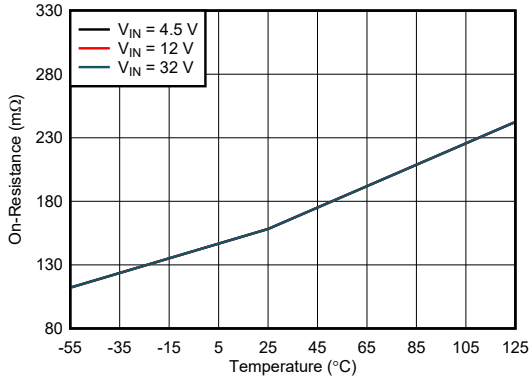
I_{OUT2} = 490 mA

Figure 6-9. Channel-2 FET On-Resistance



I_{OUT3} = 490 mA

Figure 6-10. Channel-3 FET On-Resistance



I_{OUT4} = 490 mA

Figure 6-11. Channel-4 FET On-Resistance

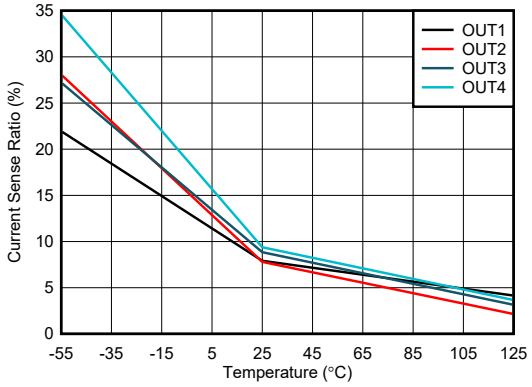


Figure 6-12. Current-Sense Ratio at 5 mA

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6.7 Typical Characteristics (continued)

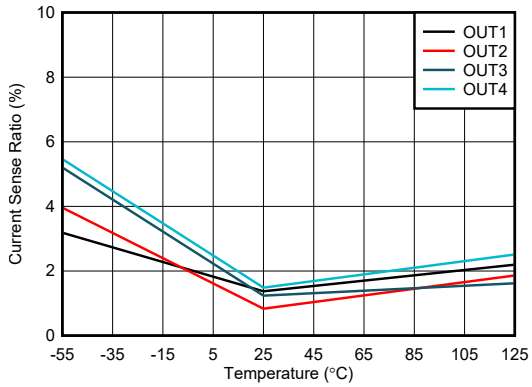

Figure 6-13. Current-Sense Ratio at 25 mA

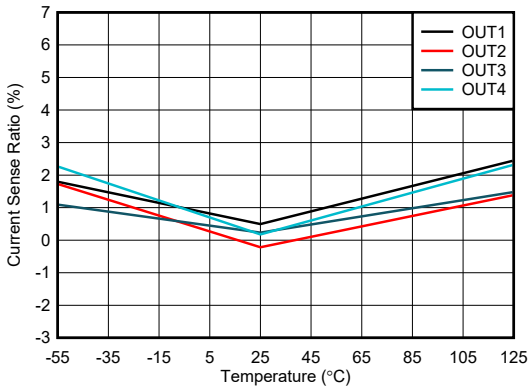

Figure 6-14. Current-Sense Ratio at 50 mA

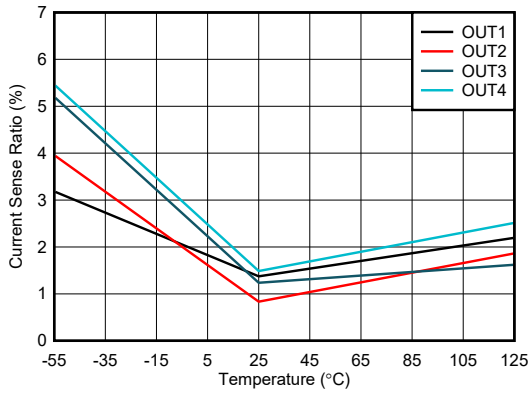

Figure 6-15. Current-Sense Ratio at 100 mA

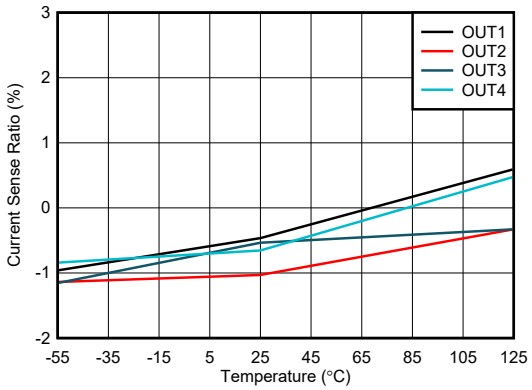

Figure 6-16. Current-Sense Ratio at 500 mA

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7 Parameter Measurement Information

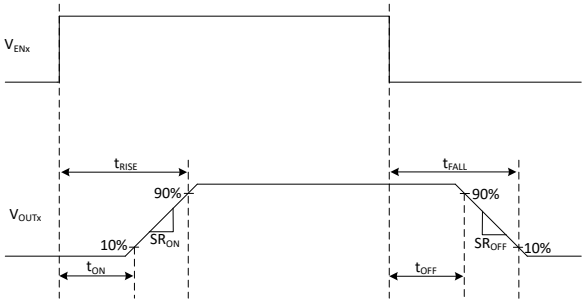


Figure 7-1. Output Delay Characteristics

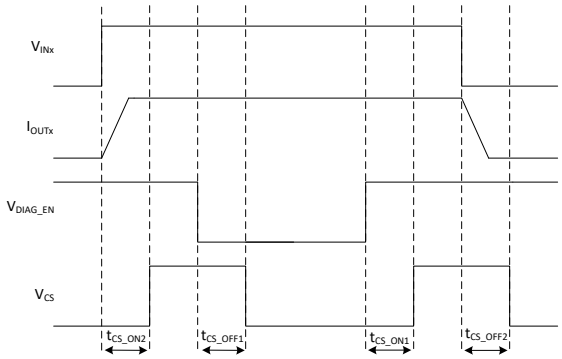


Figure 7-2. CS Delay Characteristics

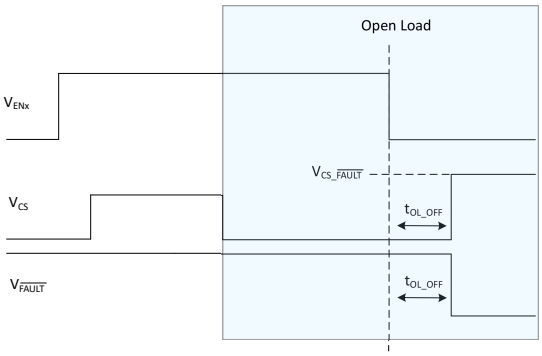


Figure 7-3. Open-Load Blanking-Time Characteristics

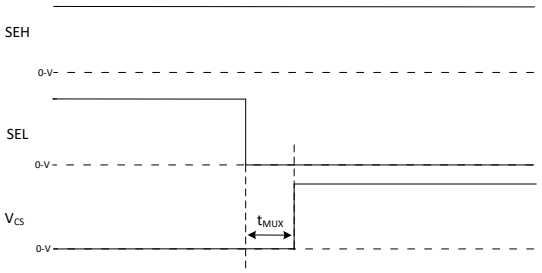


Figure 7-4. Multi-sense Transition Delay

8 Detailed Description

8.1 Overview

The TPS7H2140-SEP device is a eFuse, with internal charge pump and quad-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system. The device includes diagnostic reporting, which includes an global open-drain digital output and the current-sense analog output.

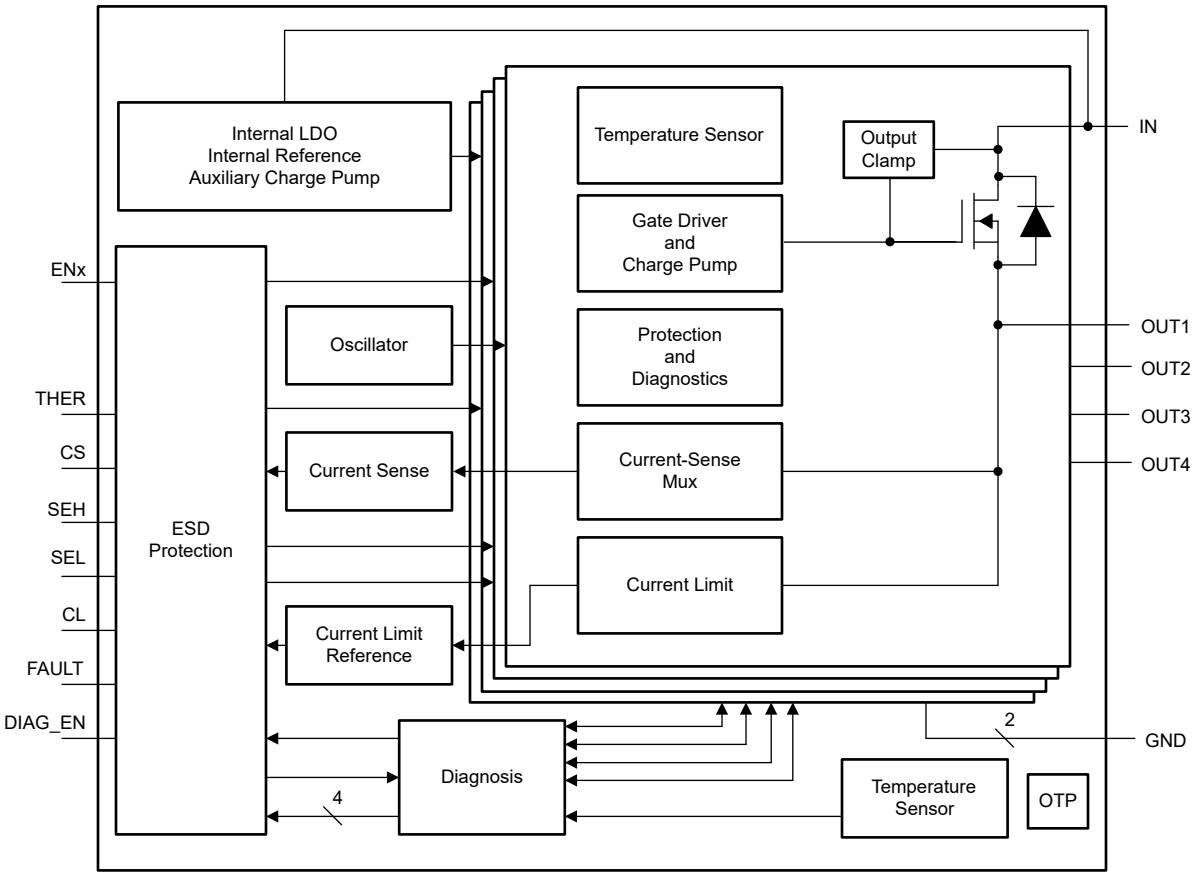
High-accuracy current sense makes the diagnostics more accurate without further calibration. One integrated current mirror can source 1 / K_{CS} of the load current. The mirrored current flows into the CS-pin resistor to become a voltage signal. K_{CS} is a constant value (300) across temperature and supply voltage. A wide linear region from 0 V to 4 V allows a better real-time load-current monitoring. The CS pin can also report a fault with pullup voltage of $V_{CS_\overline{FAULT}}$.

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system area by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. Additional, the device also implements an internal current limit ($I_{CL_INTERNAL}$) with a fixed value, between 8 to 14 A.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source to protect itself. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

The TPS7H2140-SEP device is a eFuse for a wide variety of resistive, inductive, and capacitive loads, including: relays, solenoids, heaters, and sub-modules.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Pin Current and Voltage Conventions

For reference purposes throughout the data sheet, current directions on their respective pins are as shown by the arrows in Figure 8-1. All voltages are measured relative to the ground plane.

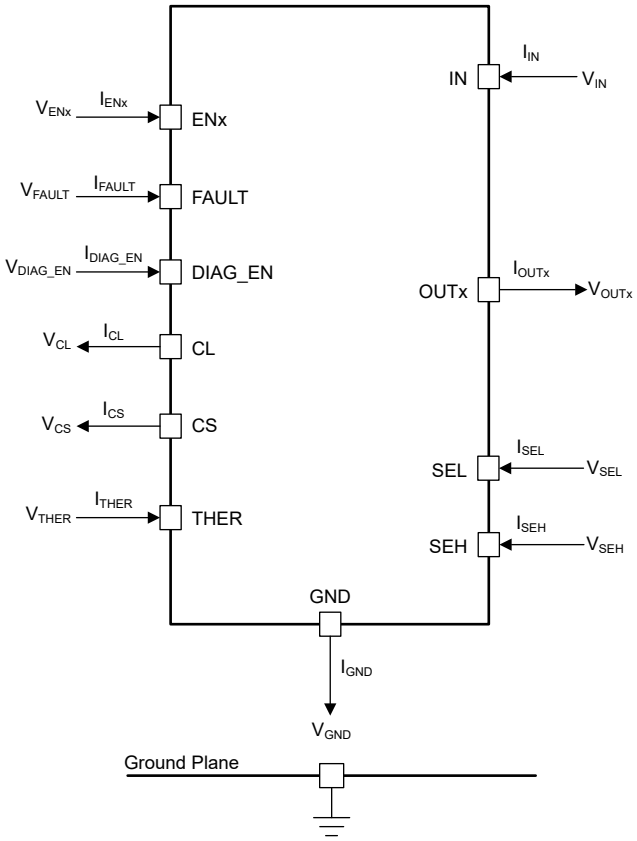

Figure 8-1. Voltage and Current Conventions

8.3.2 Accurate Current Sense

High-accuracy current sense is implemented in the TPS7H2140-SEP. It allows a better real-time monitoring effect and more-accurate diagnostics without further calibration.

The integrated current mirror sources a ratio of the load current as: 1 / K_{CS} (where: K_{CS} = 300). This mirrored current flows into the external current sense resistor to become a voltage signal. The current mirror is shared by the four channels. Channel selection is accomplished by using the multiplexer digital inputs (SEL and SEH). I_{CS} can be calculated using Equation 1.

$$I_{CS} = \frac{I_{OUTx}}{K_{CS}} = \frac{I_{OUTx}}{300} \quad (1)$$

K_{CS} is the ratio of the output current and the sense current (CS). It is a constant value across the temperature and supply voltage (IN). Each device is calibrated accurately during production, so post-calibration is not required. See Figure 8-2 for more details.

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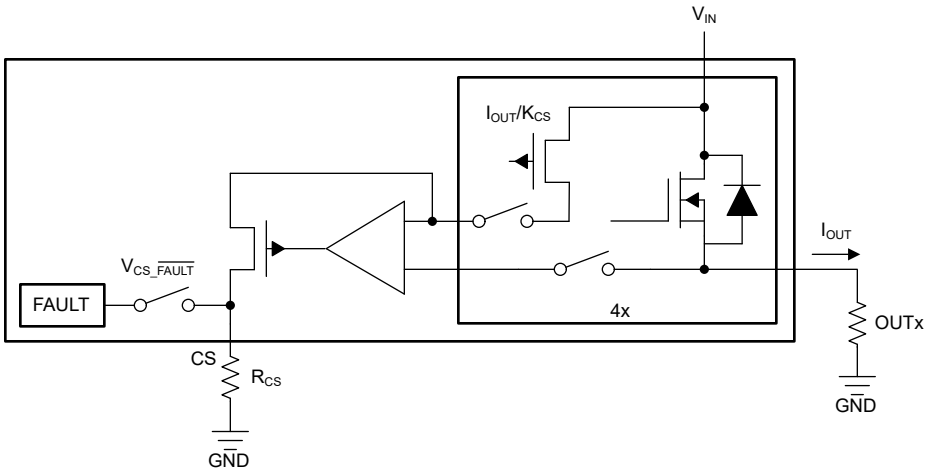

Figure 8-2. Current-Sense Block Diagram

When a fault occurs, the CS pin also works as a fault report with a pullup voltage of $V_{CS_\overline{FAULT}}$. During a fault the maximum available current in CS is $I_{CS_\overline{FAULT}}$ (15 mA). See Figure 8-3 for more details.

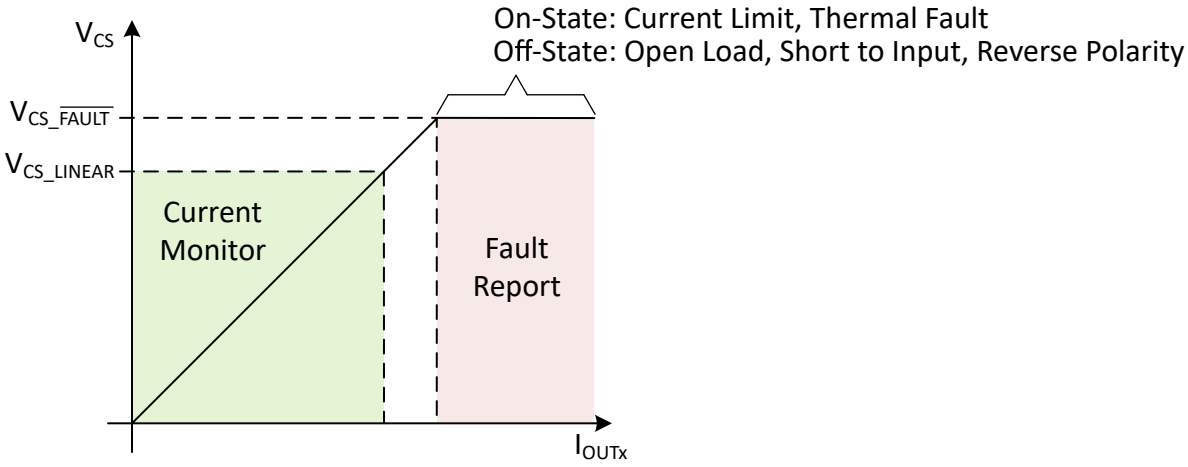

Figure 8-3. Current-Sense Output-Voltage Curve

Use Equation 2 to calculate R_{CS}.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{CS}}{I_{OUTx}} \quad (2)$$

Take the following points into consideration when calculating R_{CS}.

- Ensure V_{CS} is within the current-sense linear region (V_{CS_LINEAR}, I_{OUTx_LINEAR}) across the full range of the load current. Check R_{CS} with Equation 3.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} \leq \frac{V_{CS_LINEAR(MAX)} \times K_{CS}}{I_{OUTx(MAX)}} \quad (3)$$

- In fault mode, ensure I_{CS} is within the source capacity of the CS pin ($I_{CS_\overline{FAULT}}$). Check R_{CS} with Equation 4 .

$$R_{CS} = \frac{V_{CS}}{I_{CS}} \geq \frac{V_{CS_FAULT(MAX)}}{I_{CS_FAULT(MIN)}} \quad (4)$$

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8.3.3 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to I_{CL_TSD} (if set externally) or $I_{CL_INTERNAL_TSD}$ (when using internal) to reduce the power dissipation on the power FET. See Figure 8-4 for more details.

The device has two current-limit thresholds.

- **Internal current limit** – The internal current limit is fixed at $I_{CL_INTERNAL}$, typically 11 A. Tie the CL pin directly to the device GND for large-transient-current applications.
- **External adjustable current limit** – An external resistor is used to set the current-limit threshold. Use the Equation 5 and Equation 6 to calculate the R_{CL}. V_{CL_TH} (0.8 V) is the internal band-gap voltage. K_{CL} (2500) is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

$$I_{CL} = \frac{V_{CL_TH}}{R_{CL}} = \frac{I_{OUT}}{K_{CL}} \tag{5}$$

$$R_{CL} = \frac{V_{CL_TH} \times K_{CL}}{I_{OUT}} \tag{6}$$

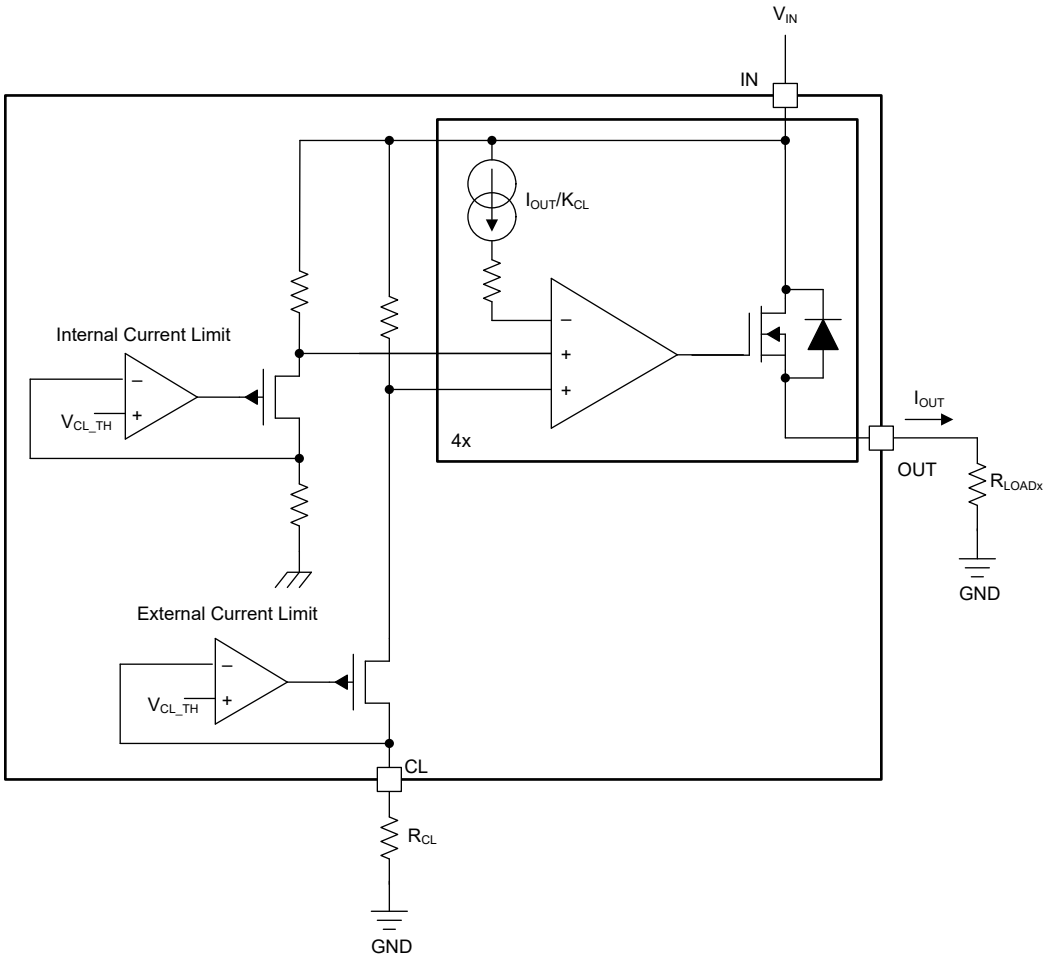

Figure 8-4. Current-Limit Block Diagram

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected with device GND.

For better protection from a hard short-to-GND condition (when the ENx pins are enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the related channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 µs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

8.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is internally implemented, namely V_{DS_CLAMP}.

$$V_{DS_CLAMP} = V_{IN} - V_{OUTx} \quad (7)$$

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch (E_{HSS}). Total energy includes the energy of the power supply (E_{IN}) and the energy of the load (E_{LOAD}). If resistance is in series with inductance, some of the load energy is dissipated on the resistance (E_R) and the inductor itself (E_L).

$$E_{HSS} = E_{IN} + E_{LOAD} = E_{IN} + E_L + E_R \quad (8)$$

When an inductive load switches off, E_{HSS} causes high thermal stressing on the device. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

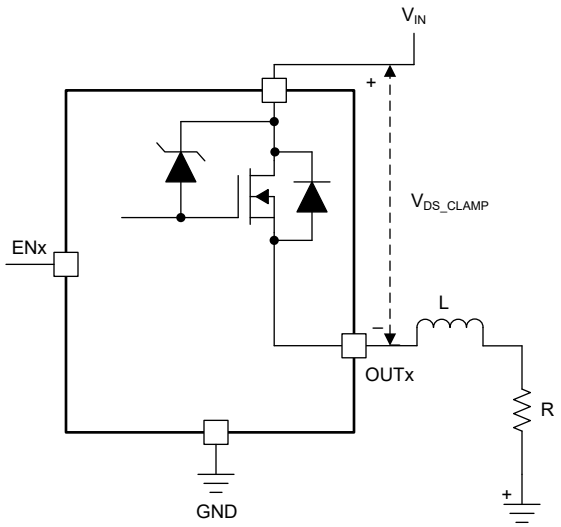

Figure 8-5. Drain-to-Source Clamping Structure

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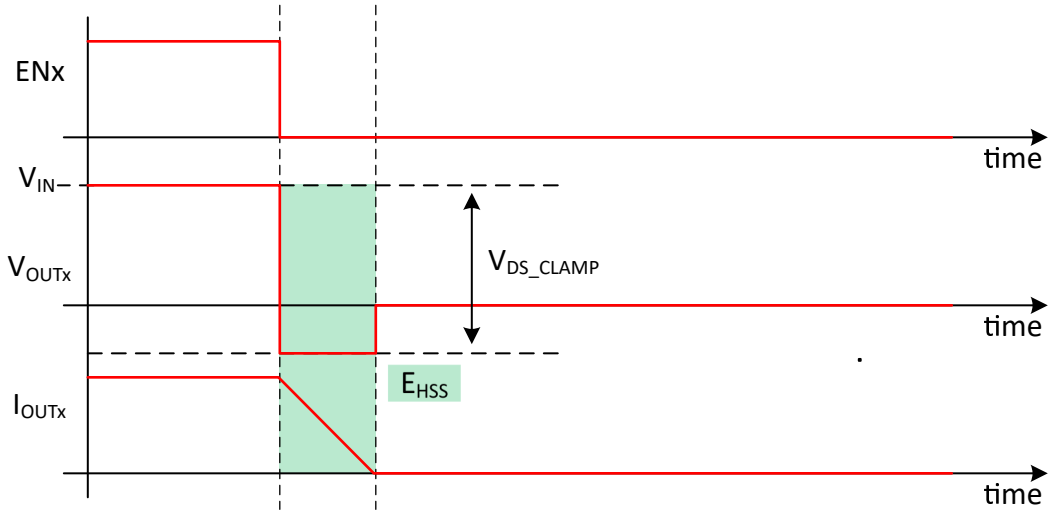

Figure 8-6. Inductive Load Switching-Off Diagram

From the perspective of the high-side switch, E_{HSS} equals the integration value during the demagnetization period.

$$E_{HSSx} = \int_0^{t_{DECAYx}} V_{DS_CLAMP} \times I_{OUTx}(t)\,dt \tag{9}$$

$$t_{DECAYx} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \tag{10}$$

$$E_{HSSx} = L \times \frac{V_{IN} + |V_{OUT}|}{R^2} \times \left\{\left(R \times I_{OUT(MAX)}\right) - \left[|V_{OUT}| \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right)\right]\right\} \tag{11}$$

When R approximately equals 0, $E_{HSS)}$ can be given simply as:

$$E_{HSSx} = \frac{1}{2} \times L \times I^2_{OUT(MAX)} \times \left[\frac{(V_{IN} + |V_{OUT}|)}{|V_{OUT}|}\right] \tag{12}$$

Figure 8-7 is a waveform of the device driving an inductive load and dissipating 40 mJ of energy across the NMOS pass-element (across IN and OUT1) during the inductive kick-back. The energy was controlled by turning off the channel # 1 at 2.8 (at I_{OUT1}).

The displayed signal definitions are shown in Scope Signals Description

Table 8-1. Scope Signals Description

Channel #	Name of the Signal	Signal Color
1	V_{EN1}	Blue
2	V_{IN}	Red
3	V_{OUT1}	Green
4	I_{OUT1}	Magenta
Math	E_{HSS1}	Cyan

The device also optimizes the switching-off slew rate when the clamp is active. This optimization can help the system design by keeping the effects of transient power and EMI to a minimum.

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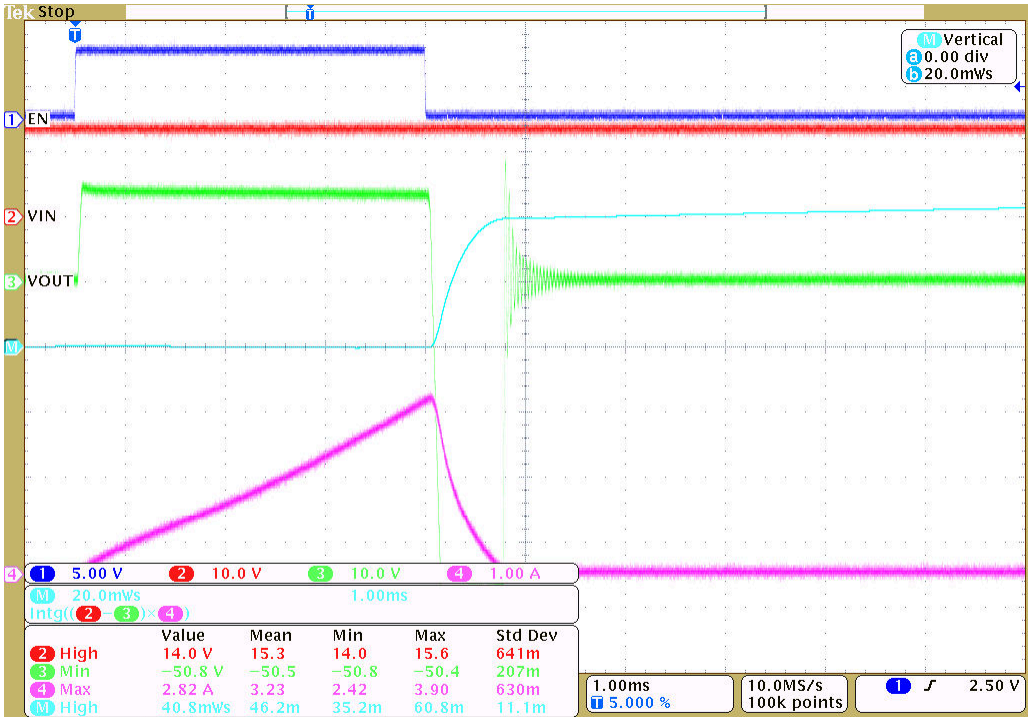

Figure 8-7. Inductive Load Switching-Off Waveform of 40mJ

A. The nominal inductor value use for this waveform is 8mH.

Note that for PWM-controlled inductive loads, it is recommended to add the external freewheeling circuitry shown in Figure 8-8 to protect the device from repetitive power stressing. TVS is used to achieve the fast decay. See Figure 8-8 for more details.

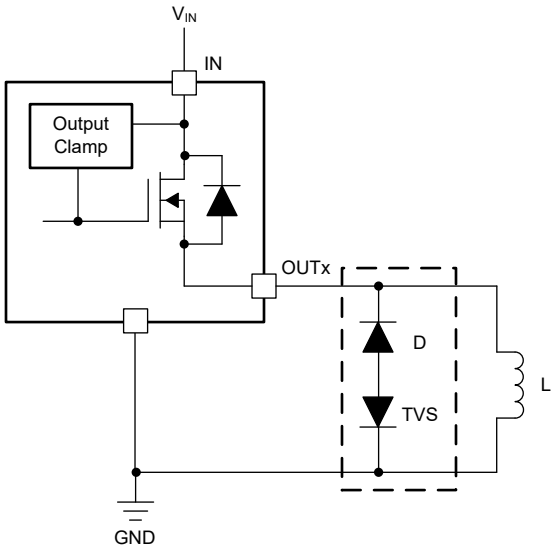

Figure 8-8. Protection With External Circuitry

8.3.5 Fault Detection and Reporting

8.3.5.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the house-keeping microcontroller, the MCU can use GPIOs to set DIAG_EN high to

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enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and ENx low.

8.3.5.2 Multiplexing of Current Sense

SEL and SEH are the multiplexer selector high and low digital inputs. The multiplexer controls the channel selection for the current-sense function. As this function is shared among all four channels, only one at a time can be observed. See Table 8-2 for more details.

Table 8-2. Diagnosis Configuration Table

DIAG_EN(1)	ENx(1)	SEH(1)	SEL(1)	CS ACTIVATED CHANNEL	CS, $\overline{\text{FAULT}}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	—	High impedance	Diagnostics disabled, full protection
	L					Diagnostics disabled, no protection
H	—	0	0	Channel # 1	See Table 8-3	See Table 8-3
		0	1	Channel # 2		
		1	0	Channel # 3		
		1	1	Channel # 4		

(1) L = 0 = logical zero (false), H = 1 = logical one (true), — = don't care

8.3.5.3 Fault Table

Table 8-3 applies when the DIAG_EN pin is enabled.

Table 8-3. Fault Table

CONDITIONS	ENx(2)	OUTx(2)	THER(2)	CRITERION(2)	CS	FAULT	FAULT RECOVERY
Normal	L	L	—	—	0	H	—
	H	H	—	—	In linear region	H	—
Overlaod, short to ground	H	L	—	Current limit triggered	V_{CS_FAULT}	L	Auto
Open load(1), short to power, reverse polarity	L	H	—	$V_{IN} - V_{OUTx} < V_{OL_OFF}$	V_{CS_FAULT}	L	Auto
Thermal shutdown	H	—	L	T_{SD} triggered	V_{CS_FAULT}	L	Output auto-retry. Fault recovers when $T_J < T_{(SD,rst)}$ or when INx toggles.
			H				Output latch off. Fault recovers when INx toggles.
Thermal swing	H	—	—	T_{SW} triggered	V_{CS_FAULT}	L	Auto

(1) An external pullup is required for open-load detection.
(2) L = logical zero (false), H = logical one (true), — = don't care

8.3.5.4 $\overline{\text{FAULT}}$ Reporting

A global $\overline{\text{FAULT}}$ pin is used to monitor the global fault condition among all the channels. When a fault condition occurs on any channel, the $\overline{\text{FAULT}}$ pin is pulled down to GND. A 3.3-V or 5-V external pullup is required to match the supply level of the house-keeping processor.

After the $\overline{\text{FAULT}}$ report, the processor can check and identify the channel in fault status by using the multiplexed current sensing pin. The CS pin also works as a fault report with an internal pullup voltage, V_{CS_FAULT}.

8.3.6 Full Diagnostics

8.3.6.1 Short-to-GND and Overload Detection

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown

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occurs, the current limit is I_{CL_TSD} (70% of the externally set current limit) or $I_{CL_INTERNAL_TSD}$ (6.5 A when using the internal current limit) to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

8.3.6.2 Open-Load Detection

8.3.6.2.1 Channel On

When a channel is on (ENx = High), benefiting from the high-accuracy current sense in a small current range, if an open-load event occurs, it can be detected as an ultra-low V_{CS} and handled by the microcontroller. Note that the detection is not reported on the $\overline{FAULT}$ pin. The microcontroller must multiplex the SEL and SEH pins to detect the channel-on open-load fault proactively.

8.3.6.2.2 Channel Off

When a channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{IN} – V_{OUTx} < V_{OL_OFF}$), and the fault is reported out. V_{OL_OFF} is between 1.6 and 2.6 V.

There is always a leakage current I_F (maximum of 0.5 µA at 25℃ or 8 µA at 125℃), present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 20 kΩ.

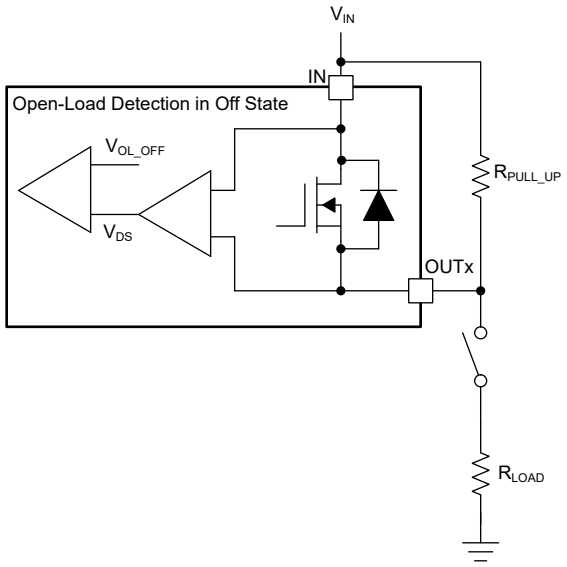

Figure 8-9. Open-Load Detection in Off-State

8.3.6.3 Short-to-Input Detection

Short-to-Input has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See Table 8-3 for more details.

In the on-state, reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state.

- If $V_{OUTx} – V_{IN} < V_F$ (body diode forward voltage), no reverse current occurs.
- If $V_{OUTx} – V_{IN} > V_F$, reverse current occurs. The current must be limited to less than I_{R1}. Setting an ENx pin high can minimize the power stress on its channel. Also, for external reverse protection, see Reverse-Current Protection for more details.

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8.3.6.4 Reverse Polarity Detection

Reverse polarity detection has the same detection mechanism and behavior as open-load detection both in the on-state and off-state. See Table 8-3 for more details.

In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state. The reverse current must be limited to less than I_{R2}. Set the related ENx pin high to keep the power dissipation to a minimum. For external reverse-blocking circuitry, see Reverse-Current Protection for more details.

8.3.6.5 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

8.3.6.5.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{SD}$. When thermal shutdown occurs, the respective output turns off. The THER pin is used to configure the behavior after the thermal shutdown occurs.

- When the **THER** pin is low, thermal shutdown operates in the auto-retry mode. The output automatically recovers when $T_J < T_{SD} – T_{HYS}$, but the current is limited to I_{CL_TSD} or $I_{CL_INTERNAL_TSD}$ (depending if the internal or external current limit is used) to avoid repetitive thermal shutdown. The thermal shutdown fault signal is cleared when $T_J < T_{SD_RST}$ or after toggling the related ENx pin.
- When the **THER** pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related ENx pin.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{FET} – T_{LOGIC} > T_{SW}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{FET} – T_{LOGIC} < T_{SW} – T_{HYS}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation. As shown in Figure 8-10, multiple thermal swings are triggered before thermal shutdown occurs.

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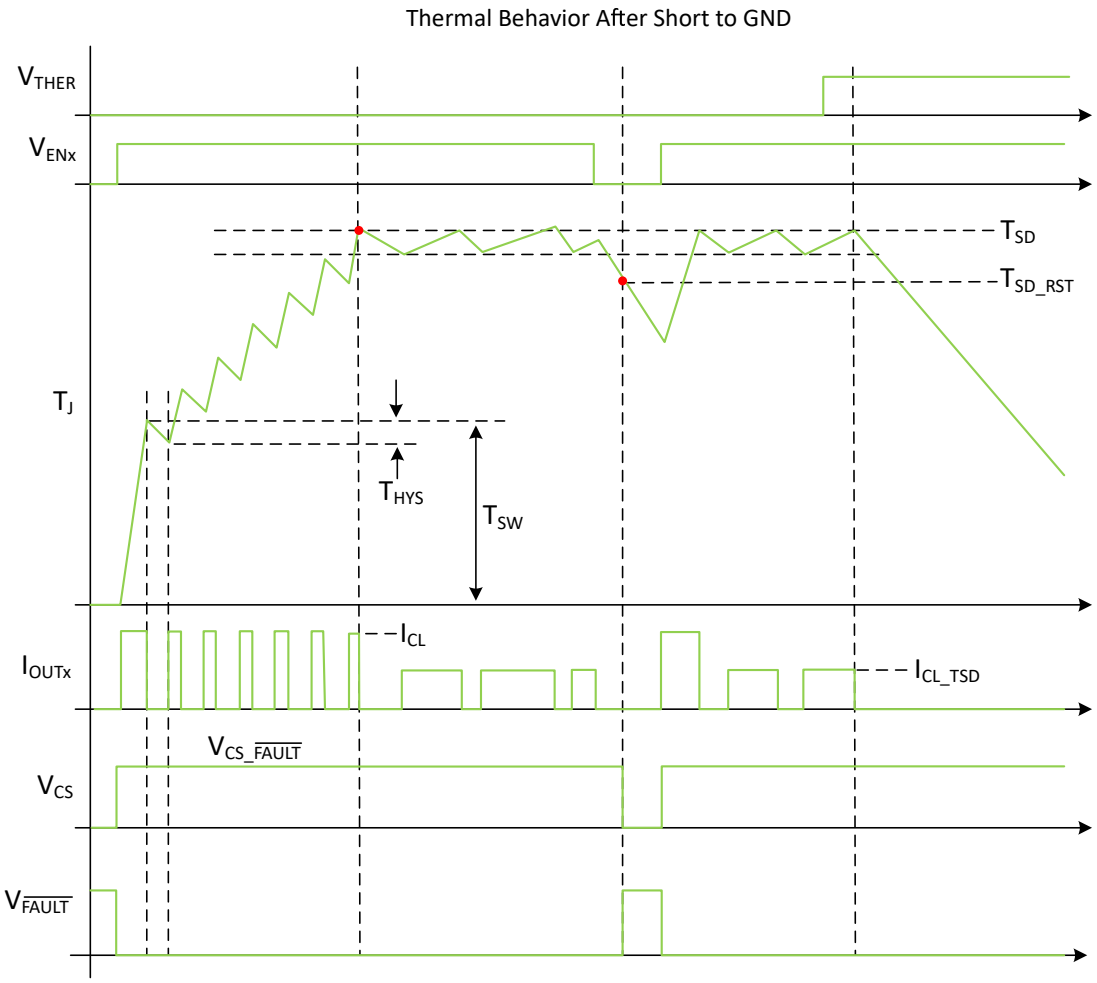

Figure 8-10. Thermal Behavior Diagram

8.3.7 Full Protections

8.3.7.1 UVLO Protection

The device monitors the supply voltage V_{IN}, to prevent unpredicted behaviors when V_{IN} is too low. When V_{IN} falls down to IN_{UVLOF}, the device shuts down. When V_{IN} rises up to IN_{UVLOR}, the device turns on.

8.3.7.2 Loss-of-GND Protection

When loss of GND occurs, output is shut down regardless of whether the ENx pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

8.3.7.3 Protection for Loss of Power Supply

When loss of supply occurs, the output is shut down regardless of whether the ENx pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the I/O pins to maintain the inductance current. To protect the system in this condition, TI recommends two types of external protections: the GND network or the external free-wheeling diode.

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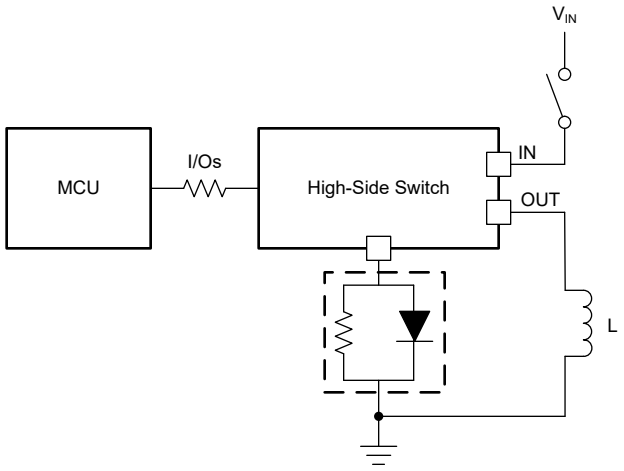

Figure 8-11. Protection for Loss of Power Supply, Method 1

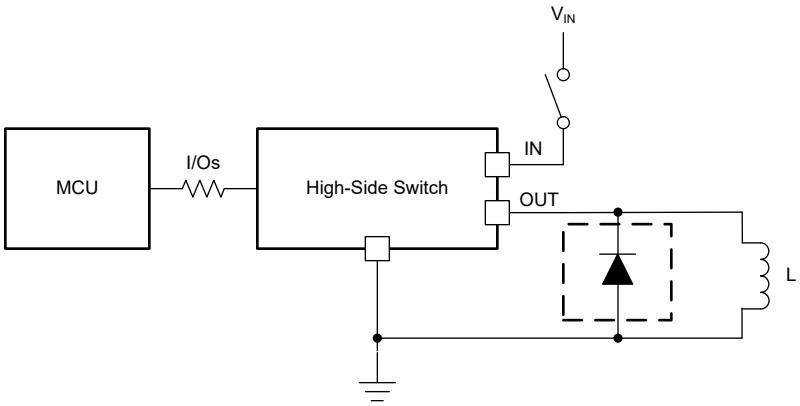

Figure 8-12. Protection for Loss of Power Supply, Method 2

8.3.7.4 Reverse-Current Protection

Reverse current occurs in two conditions: short to power and reverse polarity.

- When a short to the input occurs, there is only reverse current through the body diode. I_{R1} specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. I_{R2} specifies the limit of the reverse current. The GND pin maximum current is specified in the Absolute Maximum Ratings.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.

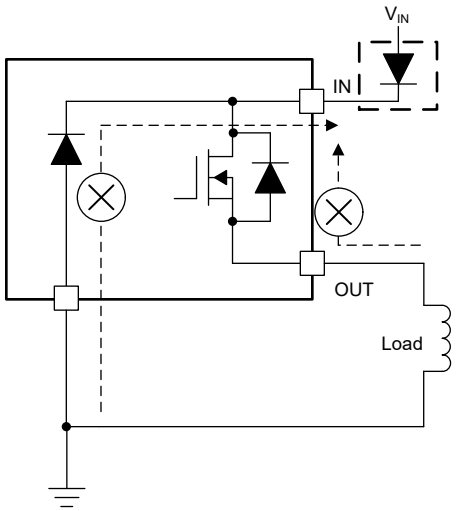

Figure 8-13. Reverse-Current External Protection, Method 1

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-kΩ resistor in parallel with a >100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 kΩ is recommended on the I/O pins.

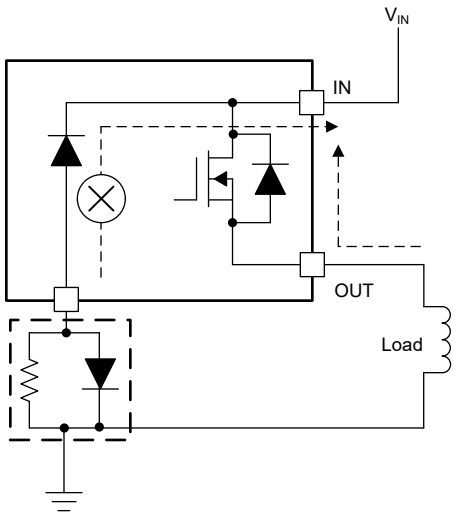

Figure 8-14. Reverse-Current External Protection, Method 2

8.3.7.5 MCU I/O Protection

In some severe systems conditions the loss of power with inductive loads, results on a negative pulse on the GND pin This pulse can cause damage on the connected microcontroller. TI recommends serial resistors to protect the microcontroller, for example, 4.7 kΩ when using a 3.3-V microcontroller and 10 kΩ for a 5-V microcontroller.

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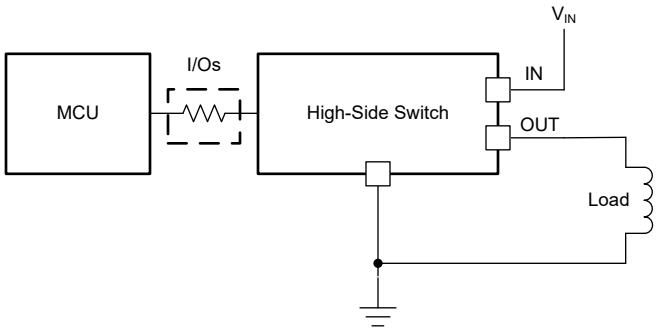

Figure 8-15. MCU I/O External Protection

8.3.8 Parallel Operation

The TPS7H2140-SEP can be configured in parallel operation either to increase the current capability, up to 5.4 A, or to reduce the R_{ON} (on-state resistance). Any channels combination can be parallel by connecting the desired channels outputs (OUTx) and enable (ENx) signals together. Figure 8-16 shows the input/output connections when paralleling all 4 channels of the TPS7H2140-SEP

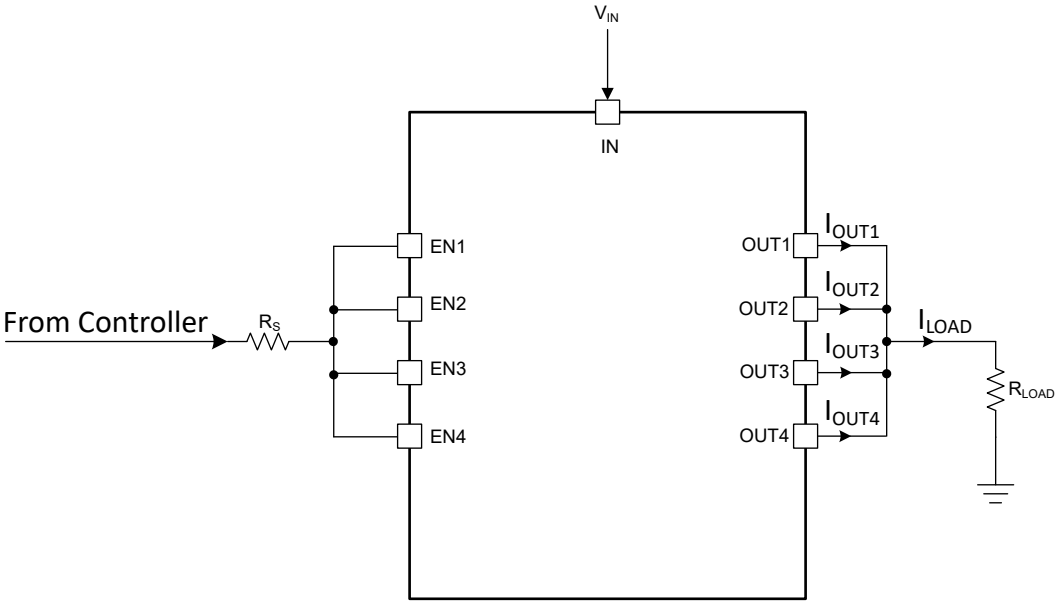

Figure 8-16. Input and Output Connections when paralleling all channels in the TPS7H2140-SEP

For proper device operation follow the following recommendations:

1. Connect the ENx inputs signals of the channels to be parallel together and as close to the device (I.C.) as possible.
2. Connect the OUTx output signals of the channels to be parallel together and as close to the device (I.C.) as possible.
3. Take in consideration the deviations (or errors) in the R_{ON}, current limit and voltage clamp for the system design.

Due to imbalance of currents in each channel (due to ΔR_{ON}) the total load current is not equally distributed. The channel current bounds are:

- $$I_n\left(max\right) = \frac{I_{LOAD}}{N} \times \left(\frac{1 + \Delta R_{ON}}{1 - \Delta R_{ON}}\right) \quad (13)$$

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- $$I_n\left(min\right) = \frac{I_{LOAD}}{N} \times \left(\frac{1 - \Delta R_{ON}}{1 + \Delta R_{ON}}\right) \quad (14)$$

where N is equal to the # of parallel channels and ΔR_{ON} is the difference between the on-state resistance for any given channel.

At 25 °C the ΔR_{ON} maximum value is specified at 6 % (or 0.06), using this value and assuming the I_{LOAD} is 5 A the current by each channel can be calculated (using Equation 13and Equation 14) as:

$$1.11 \leq I_n \leq 1.41 \quad (15)$$

When paralleling channels is important to known that the current limit is programmed per channel based (or the same for all channels). The sensed current ratio on the current limit circuit have variations (as specified by dK_{CL}/K_{CL}). To deliver the expected load before reaching the current limit the designer most account for variation on the sensed current gain and variations on the channels currents due to on-resistance mismatch as described before. To select the current limit resistor when accounting for all system errors (ΔR_{ON} and dK_{CL}/K_{CL}) use:

$$R_{CL}\left(max\right) = \frac{V_{CL_TH} \times K_{CL}\left(1 - \left|\frac{dK_{CL}}{K_{CL}}\right|\right)}{I_n(max)} \quad (16)$$

As the sensed current is measured in a per channel based and reported on the CS pin. To measured the total load current of parallel channels, the individual current most be measured and added together. The individual currents are measured by using the SEH and SEL (mux inputs) in conjunction with the CS voltage.

The diagnostics as specified by Fault Table are globally reported, as the fault conditions affects all channels simultaneously. When using the internal clamp (V_{DS_CLAMP}) to dissipate the inductive kick-back energy the energy most be limited to the maximum of a single channel.

Note

The energy does not scale with the number of parallel channels and most be limited to the absolute maximum value of 40mJ.

8.4 Device Functional Modes

8.4.1 Working Modes

The device has three working modes: normal mode, standby mode, and standby mode with diagnostics.

Note that ENx must be low for t > t_{LOW_OFF} to enter the standby mode, where t_{LOW_OFF} is the standby mode deglitch time used to avoid false triggering. Figure 8-17 shows a working-mode diagram.

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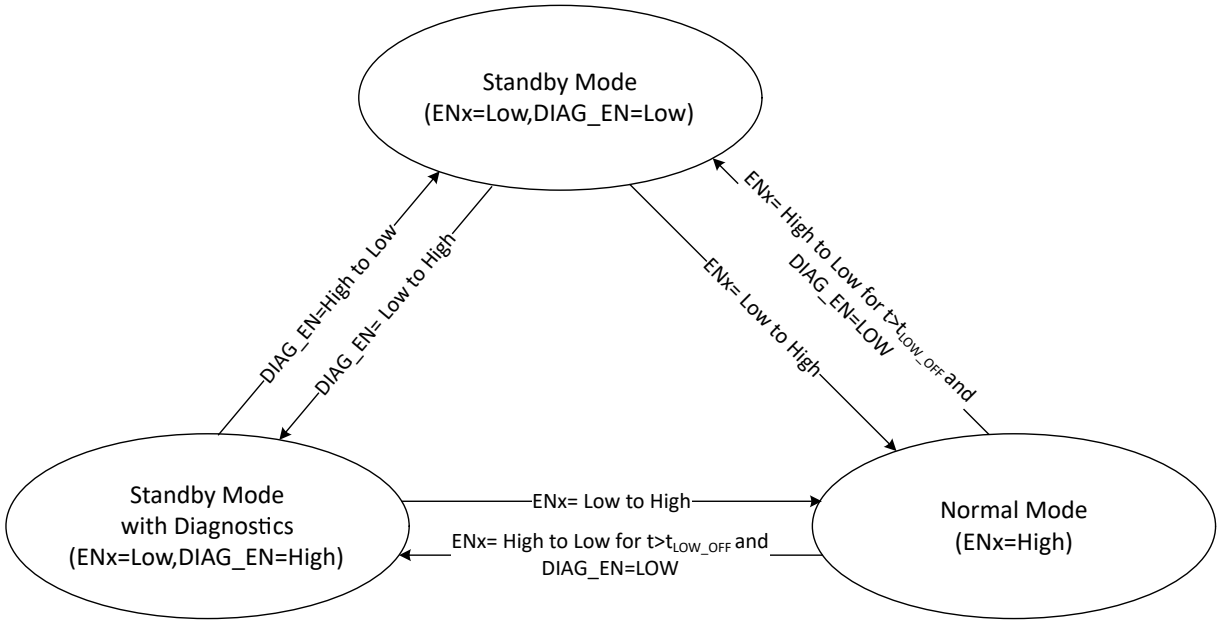

Figure 8-17. Working Modes

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H2140-SEP device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including: relays, solenoids, heaters, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

9.2 Typical Application

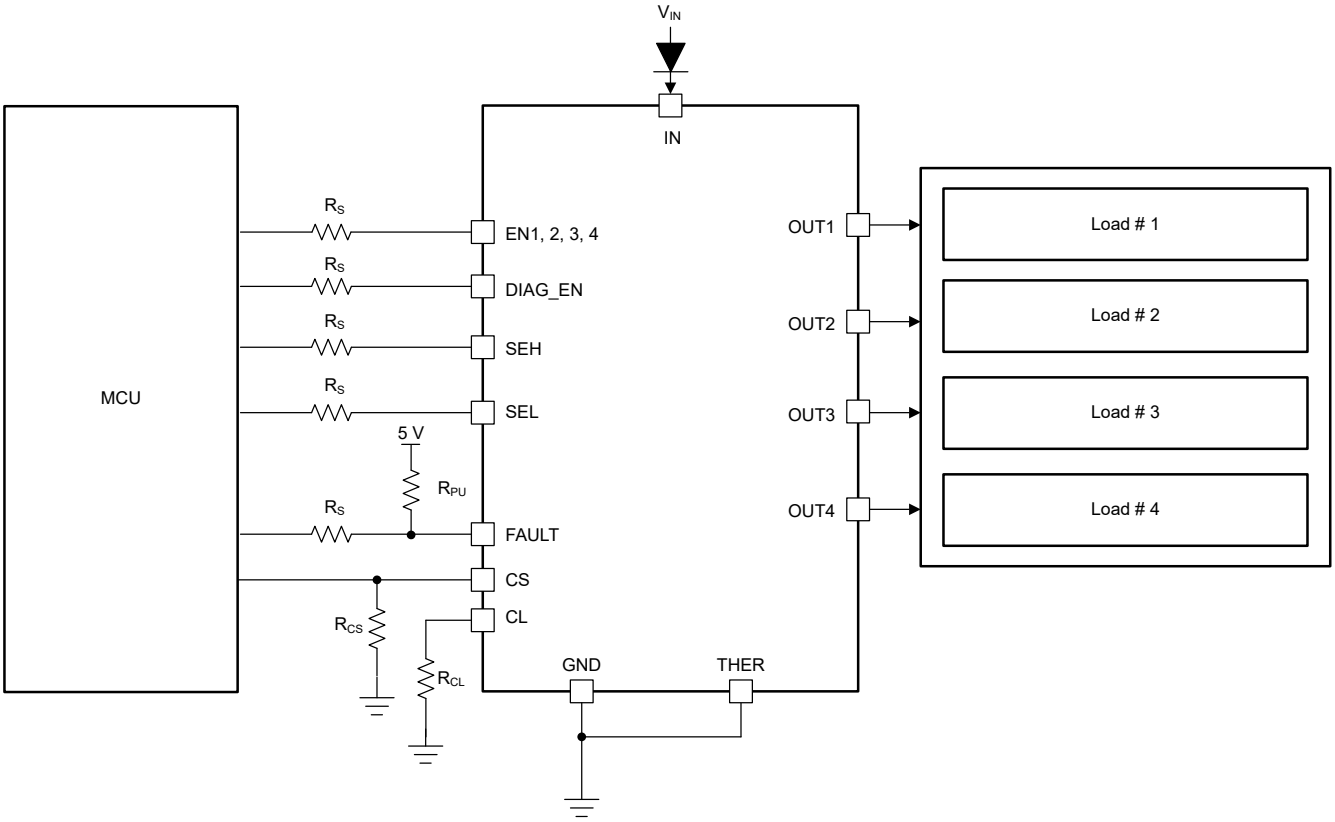

Figure 9-1. Typical Application Diagram

9.2.1 Design Requirements

- V_{IN} = 12 V
- Maximum load current up to 1 A (nominal) and for each channel
- Up to 1.1 A during transients before the current is limited.
- Current sense for fault monitoring
- Expected current-limit value of 1.1 A
- Automatic recovery mode when thermal shutdown occurs
- Full diagnostics with 5-V MCU/FPGA
- Reverse-voltage protection with a blocking diode in the power-supply line

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9.2.2 Detailed Design Procedure

When selecting the current limit resistor we most account for the accuracy of the limit. The accuracy on the range of the desired current limit is ± 20 %.

As the current limit can be shifted up to -20%, is desired to boost the load current by this factor. In which case the load current for the calculation of the current limit is: 1.375 A.

To keep the 1.1 A nominal current in the 0 to 4 V current-sense range, calculate the R_{CS} resistor using Equation 17. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{CS}}{I_{OUTx}} = \frac{4 \times 300}{1.1} = 1.09\ k\Omega \quad (17)$$

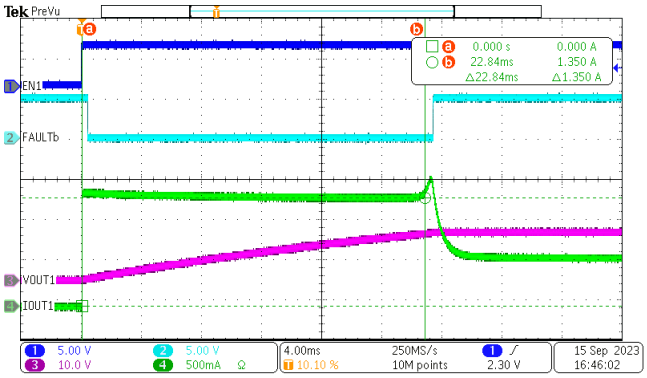
To set the adjustable current limit value at 2.5 A, calculate R_{CL} using Equation 18.

$$R_{CL} = \frac{V_{CL_TH} \times K_{CL}}{I_{OUTx}} = \frac{0.8 \times 2500}{1.375} = 1.45\ k\Omega \quad (18)$$

TI recommends R_S = 10 kΩ for 5-V MCU, and R_{PU} = 10 kΩ as the pullup resistor.

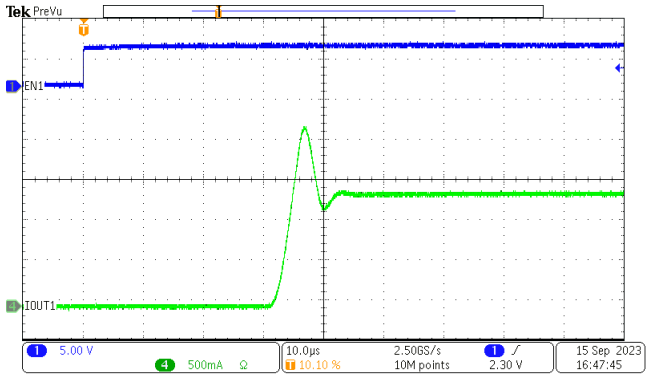
9.2.3 Application Curves

Figure 9-2 shows a test example of soft-start when driving a big capacitive load. Figure 9-3 shows an expanded waveform of the output current.



V_{IN} = 12 V ENx = ↑ I_{CL} = 1.35 A
R_{OUT1} = 20 Ω C_{OUT1} = 2.201 mF CH1 = V_{EN1} = Blue
CH2 = $V_{\overline{FAULT}}$ = Cyan CH3 = V_{OUT1} = Magenta CH4 = I_{OUT1} = Green

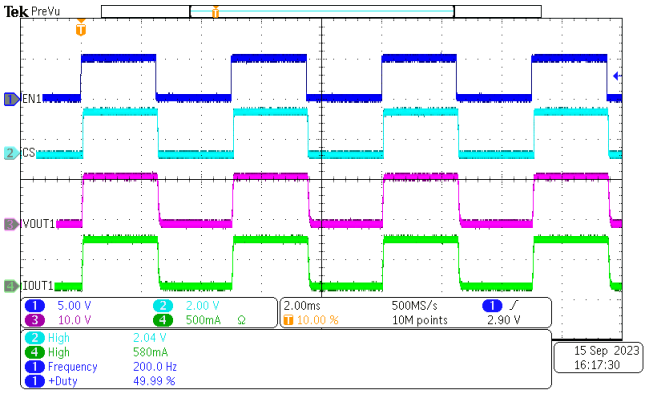
Figure 9-2. Driving a Capacitive Load With Adjustable Current Limit



V_{IN} = 12 V ENx = ↑ I_{CL} = 1.35 A
R_{OUT1}= 20 Ω C_{OUT1} = 2.201 mF
CH1 = V_{EN1} = Blue CH4 = I_{OUT1} = Green

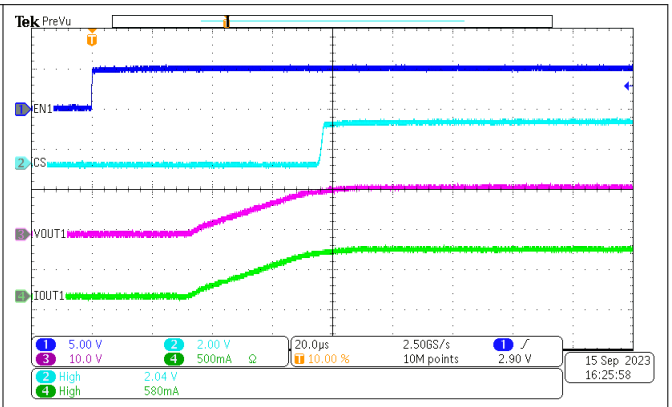
Figure 9-3. Driving a Capacitive Load, Expanded Waveform

Figure 9-4 shows a test example of PWM-mode driving. Figure 9-5 shows the expanded waveform of the rising edge. Figure 9-6 shows the expanded waveform of the falling edge.



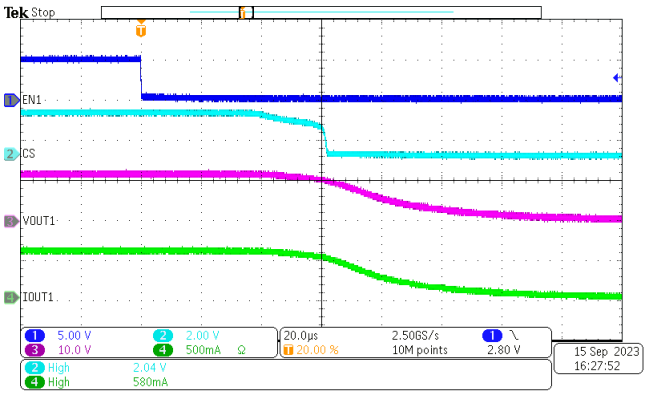
V_{IN} = 12 V EN1 = 200-Hz PWM with 50% duty-cycle R_{OUT1}= 20 Ω
C_{OUT1} = 1.1 µF CH1 = V_{EN1} = Blue CH2 = V_{CS} = Cyan
CH3 = V_{OUT1} = Magenta CH4 = I_{OUT1} = Green

Figure 9-4. PWM Signal Driving



V_{IN} = 12 V EN1 = 200-Hz PWM with 50% duty-cycle R_{OUT1} = 20 Ω
C_{OUT1} = 1.1 µF CH1 = V_{EN1} = Blue CH2 = V_{CS} = Cyan
CH3 = V_{OUT1} = Magenta CH4 = I_{OUT1} = Green

Figure 9-5. Expanded Waveform of Rising Edge



V_{IN} = 12 V EN1 = 200-Hz PWM with 50% duty-cycle R_{OUT1}= 20 Ω
C_{OUT1} = 1.1 µF CH1 = V_{EN1} = Blue CH2 = V_{CS} = Cyan
CH3 = V_{OUT1} = Magenta CH4 = I_{OUT1} = Green

Figure 9-6. Expanded Waveform of Falling Edge

9.3 Power Supply Recommendations

The TPS7H2140-SEP is designed to operate from an input range between 4.5 V to 32 V. This supply voltage must be well regulated and proper local bypass capacitors should be used for proper electrical performance from V_{IN} to GND. Due to stringent requirements for space applications, typically numerous input bypass capacitors are used and the total capacitance is much larger than for commercial applications. The TPS7H2140-SEP evaluation module uses one 33-µF tantalum capacitor in parallel with one 10-µF, one 1-µF, and one 0.1-µF ceramic capacitor.

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9.4 Layout

9.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, is recommended a solder coverage greater than 85%.

9.4.2 Layout Examples

9.4.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

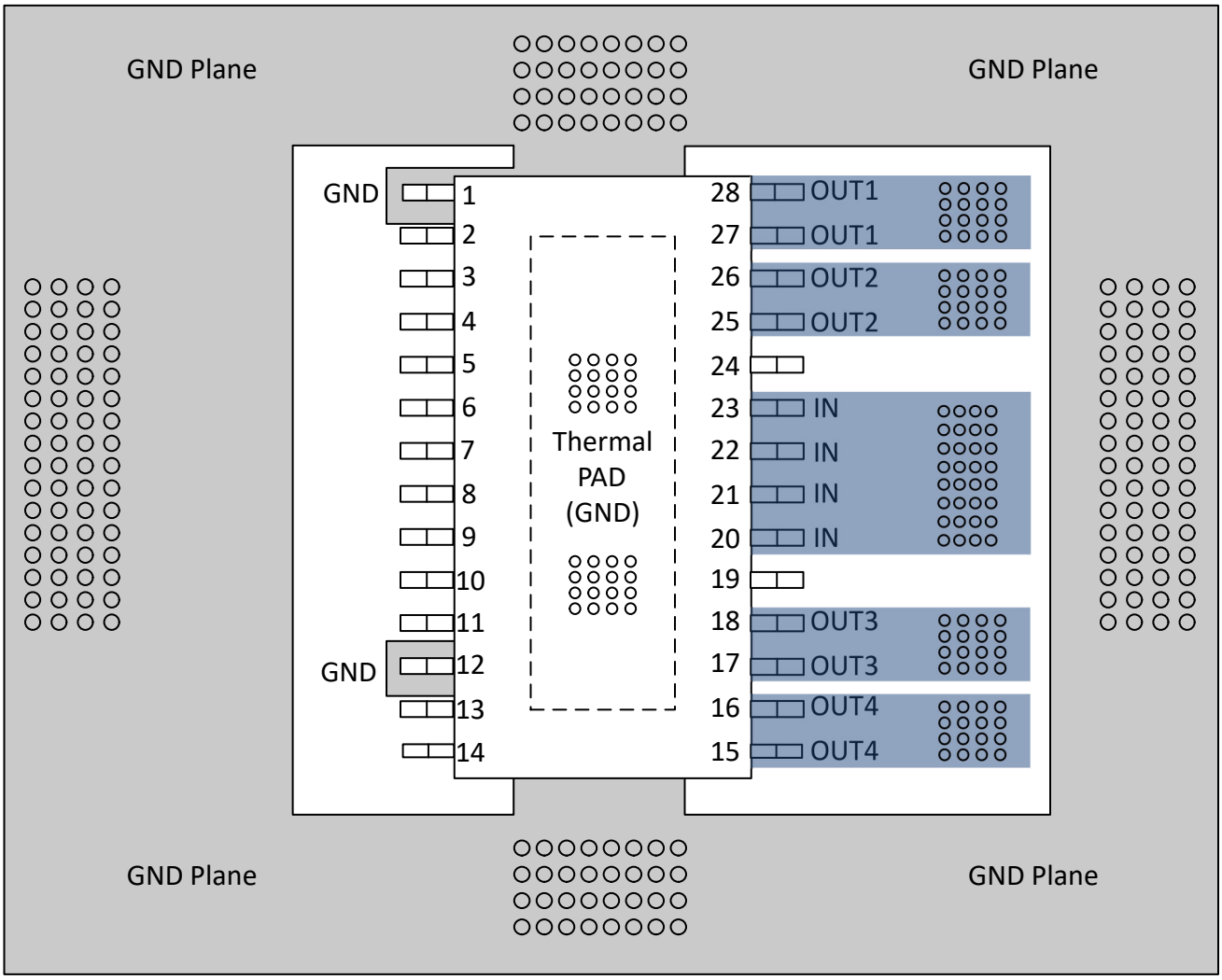

Figure 9-7. Layout Example Without a GND Network

9.4.2.2 With a GND Network

With a GND network, tie the thermal pad as one trace to the board GND copper.

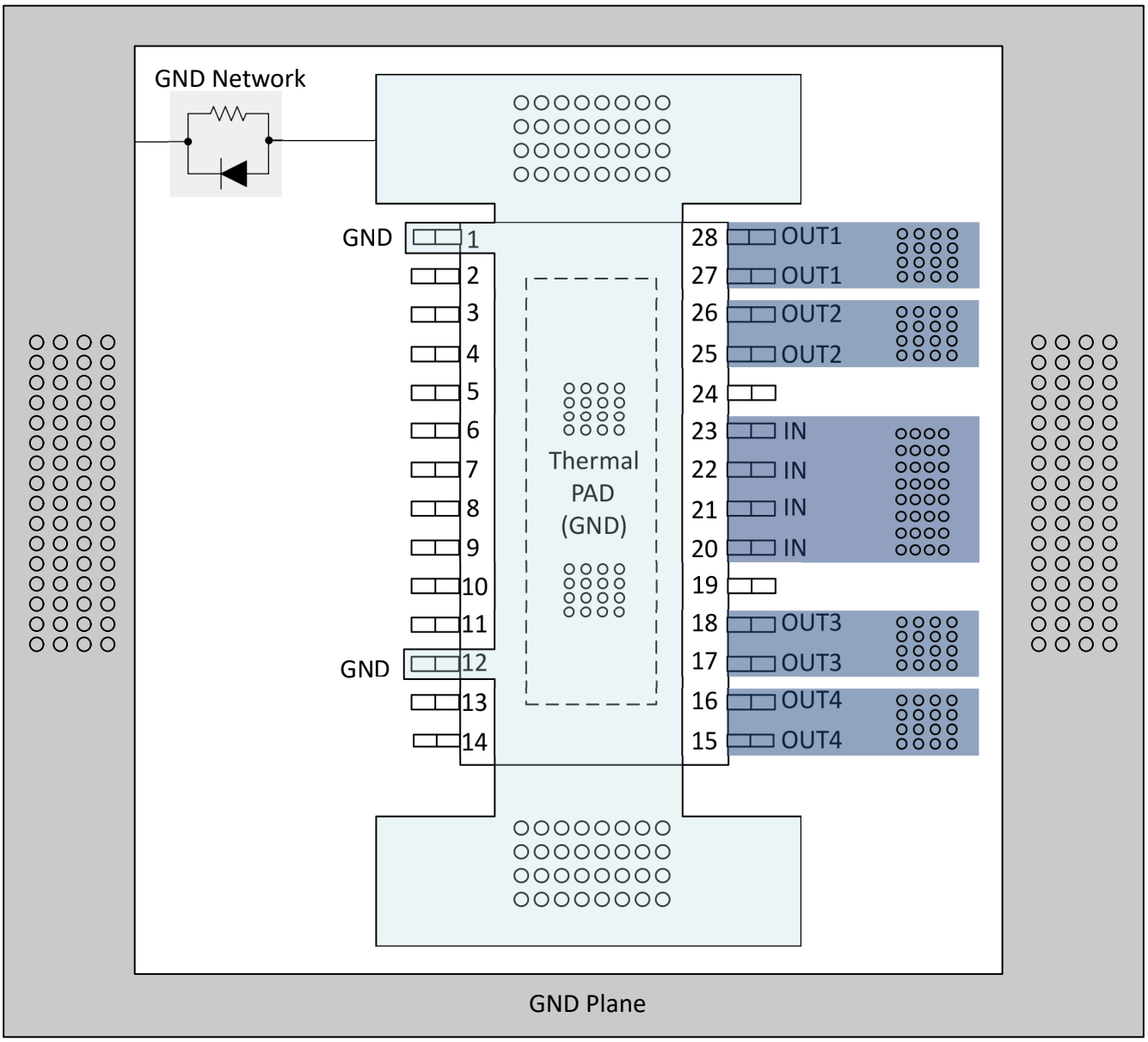

Figure 9-8. Layout Example With a GND Network

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7H2140-SEP Total Ionizing Dose (TID)*
- Texas Instruments, *Single-Event-Effects Test Report of the TPS7H2140-SEP Quad-channel eFuse*
- Texas Instruments, *TPS7H2140-SEP NDD Report*
- Texas Instruments, TPS7H2140EVM Evaluation Module (EVM)
- Texas Instruments, Unencrypted PSpice Transient Model
- Texas Instruments, *Load Switch Thermal Considerations*
- Texas Instruments, *Basics of eFuses*
- Texas Instruments, *Basics of Load Switches*
- Vendor Item Drawing, V6223610

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7H2140MPWPTSEP	Active	Production	HTSSOP (PWP) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H2140PWP
TPS7H2140MPWPTSEP.A	Active	Production	HTSSOP (PWP) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H2140PWP
V62/23610-01XE	Active	Production	HTSSOP (PWP) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	See TPS7H2140MPWPTSEP	7H2140PWP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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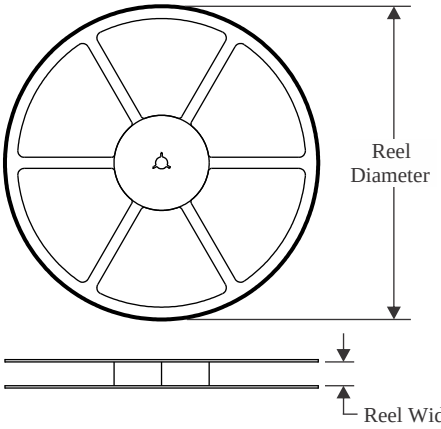
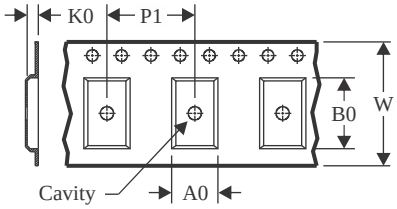
TAPE AND REEL INFORMATION

REEL DIMENSIONS

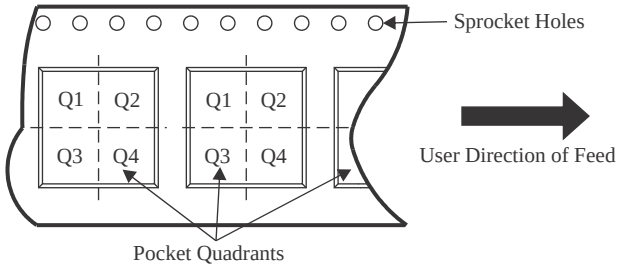


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

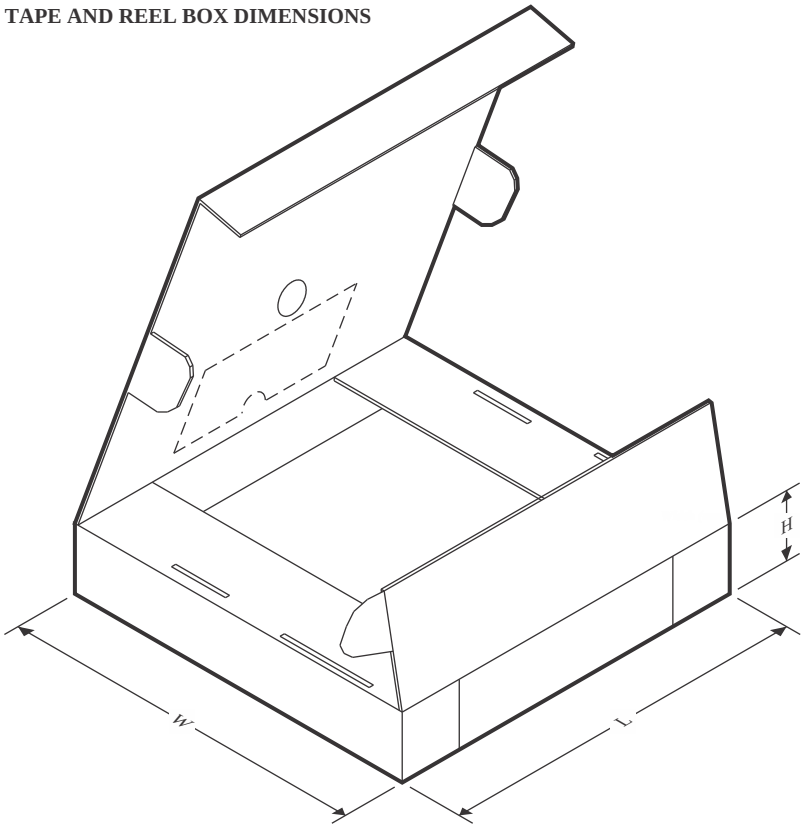
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7H2140MPWPTSEP	HTSSOP	PWP	28	250	178.0	16.4	6.95	10.0	1.7	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7H2140MPWPTSEP	HTSSOP	PWP	28	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

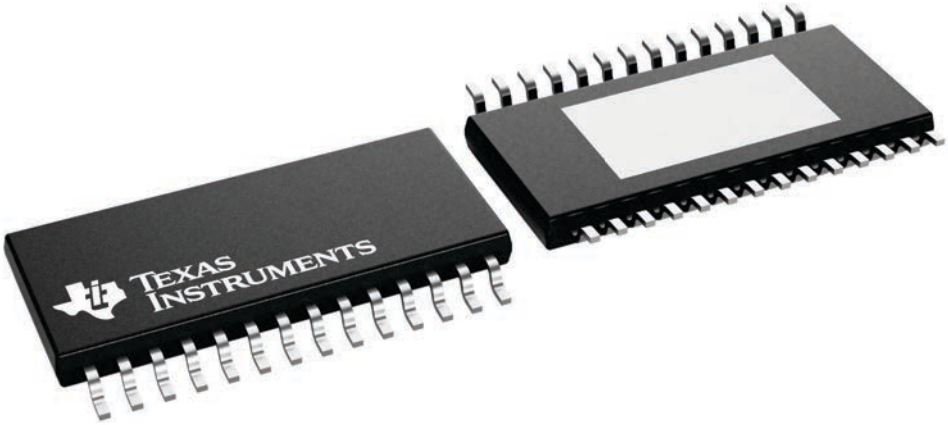
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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