*User's Guide*
# TPS542951 Step-Down Converter Evaluation Module User's Guide

TEXAS INSTRUMENTS

**ABSTRACT**

This user's guide contains information for the TPS542951EVM-057 evaluation module as well as for the TPS542951. Included are the performance specifications, schematic, and the bill of materials of the TPS542951 EVM.

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# 1 Introduction

The TPS542951 is a dual, adaptive on-time, D-CAP2™-mode, synchronous buck converter requiring a low, external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal of 700 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS542951 package along with the gate drive circuitry. The low, drain-to-source on-resistance of the MOSFETs allows the TPS542951 to achieve high efficiencies and helps keep the junction temperature low at high-output currents. The TPS542951 also features auto-skip Eco-mode operation for improved light-load efficiency. The TPS542951 dual DC/DC synchronous converter is designed to provide up to 3 A output on CH1 and 3 A output on CH2 from an input voltage source of 4.5 V to 18 V. The output voltage range is from 0.76 V to 7 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1.

The TPS542951 EVM evaluation module is a dual, synchronous buck converter providing 3.3 V at 2 A on CH1 and 1.5 V at 3 A on CH2 from 5 V to 18 V input. This user's guide describes the TPS542951 EVM performance.

**Note**

Throughout the document, x means 1 or 2, for example, VFBx means VFB1 or VFB2.

**Table 1-1. Input Voltage, Output Voltage and Output Current Summary**

| TPS542951EVM | Input Voltage Range | Output Voltage | Output Current Range |
|---|---|---|---|
| CH1 | $V_{IN1}$ = 6 V to 18 V | 3.3 V | 0 A to 2 A |
| CH2 | $V_{IN2}$ = 5 V to 18 V | 1.5 V | 0 A to 3 A |

## 2 Performance Specification Summary

A summary of the TPS542951EVM performance specifications is provided in Table 2-1. Specifications are given for an input voltage of $V_{INx}$ = 12 V and an output voltage of 3.3 V and 1.5 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

**Table 2-1. TPS542951EVM Performance Specifications Summary**

| Specifications | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range ($V_{INx}$) | | | [1] | 12 | 18 | V |
| Output voltages | $V_{OUT1}$ | | | 3.3 | | V |
| | $V_{OUT2}$ | | | 1.5 | | |
| Operating frequency | | $V_{IN1}$, $V_{IN2}$ = 12 V, $I_{OUT1}$ = 1 A, $I_{OUT2}$ = 1.5 A | | 700 | | kHz |
| Output current range | CH1 | | 0 | | 4 | A |
| | CH2 | | 0 | | 2 | |
| Line regulation, $V_{OUT1}$ | | $I_{OUT1}$ = 1 A, $I_{OUT2}$ = 0 A, $V_{IN1}$, $V_{IN2}$= 6 V to 18 V | | +0.25 , -0.55 | | % |
| Line regulation, $V_{OUT2}$ | | $I_{OUT2}$ = 1.5 A, $I_{OUT1}$ = 0 A, $V_{IN1}$, $V_{IN2}$= 5 V to 18 V | | +0.15, -0.35 | | % |
| Load regulation, $V_{OUT1}$ | | $V_{IN1}$, $V_{IN2}$ = 12 V, $I_{OUT1}$ = 0 A to 2 A | | +0.4, -0.1 | | % |
| Load regulation, $V_{OUT2}$ | | $V_{IN1}$, $V_{IN2}$ = 12 V, $I_{OUT2}$ = 0 A to 3 A | | +0.5, -0.05 | | % |
| Over current limit, $V_{OUT1}$ | | $V_{IN1}$ = 12 V, $L_1$ = 2.2 μH | 2.7 | 3.9 | 4.5 | A |
| Over current limit, $V_{OUT2}$ | | $V_{IN2}$ = 12 V, $L_1$ = 1.5 μH | 3.5 | 4.7 | 5.4 | A |
| Output ripple voltage, $V_{OUT1}$ | | $V_{IN1}$ = 12 V, $I_{OUT1}$ = 2 A | | 20 | | $mV_{PP}$ |
| Output ripple voltage, $V_{OUT2}$ | | $V_{IN2}$ = 12 V, $I_{OUT2}$ = 3 A | | 20 | | $mV_{PP}$ |
| Maximum efficiency, $V_{OUT1}$ | | $V_{IN1}$ = 6 V, $I_{OUT1}$= 0.6 A | | 94.1% | | |
| Maximum efficiency, $V_{OUT2}$ | | $V_{IN2}$ = 5 V, $I_{OUT2}$= 0.5 A | | 88.8% | | |

(1)    See Table 1-1

# 3 Modifications

This evaluation module is designed to provide access to the features of the TPS542951. Some modifications can be made to this module.

## 3.1 Output Voltage Setpoint

To change the output voltages of the EVM, it is necessary to change the value of the top resistor of the feedback divider, R1 or R3. Please refer to the top assembly in Figure 5-1 to locate the resistors close to the output connectors. Changing the value of R1 or R3 can change the output voltage above 0.765 V. The value of R1 or R3 for a specific output voltage can be calculated using Equation 1.

For output voltage from 0.76 V to 7 V:

$$V_{OUT1} = 0.765\ V \times \left(1 + \frac{R1}{R2}\right)\ ;\ V_{OUT2} = 0.765\ V \times \left(1 + \frac{R3}{R4}\right) \tag{1}$$

Table 3-1 lists the R1 or R3 values for some common output voltages. For output voltages of 1.8 V or above, a feedforward capacitor (C21 or C20) may be required to improve the phase margin. Pads for this component (C21 or C20) are provided on the printed-circuit board. Note that the resistor values given in Table 3-1 are standard values and not the exact values calculated using Equation 1.

**Table 3-1. Output Voltages**

| Output Voltage (V) | R1, R3 (kΩ) | R2, R4 (kΩ) | C21, C20 (pF) | L1, L2 (µH) | C14, C15, C18 Total Capacitance, C16, C17, C19 Total Capacitance (µF) |
|---|---|---|---|---|---|
| 1 | 6.81 | 22.1 | | 1.5 - 2.2 | 22 - 68 |
| 1.05 | 8.25 | 22.1 | | 1.5 - 2.2 | 22 - 68 |
| 1.2 | 12.7 | 22.1 | | 1.5 - 2.2 | 22 - 68 |
| 1.5 | 21.5 | 22.1 | | 1.5 - 2.2 | 22 - 68 |
| 1.8 | 30.1 | 22.1 | 5 - 22 | 2.2 - 3.3 | 22 - 68 |
| 2.5 | 49.9 | 22.1 | 5 - 22 | 2.2 - 3.3 | 22 - 68 |
| 3.3 | 73.2 | 22.1 | 5 - 22 | 2.2 - 3.3 | 22 - 68 |
| 5 | 124 | 22.1 | 5 - 22 | 4.7 | 22 - 68 |
| 6.5 | 165 | 22.1 | 5 - 22 | 4.7 | 22 - 68 |

## 3.2 Output Filter and Closed-Loop Response

The TPS542951 relies on the output filter characteristics to ensure stability of the control loop. The recommended output filter components for common output voltages are given in Table 3-1. It may be possible for other output filter component values to provide acceptable closed-loop characteristics. R11 and R12 are provided for convenience in breaking the control loop and measuring the closed-loop response.

# 4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS542951EVM. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

## 4.1 Input/Output Connections

The TPS542951EVM is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The loads must be connected to J3 and/or J2 through a pair of 20 AWG wires. The maximum load current capability is 2 times 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the input voltage ($V_{IN}$) with TP7 providing a convenient ground reference. TP4 and TP3 are used to monitor the output voltages with TP5 and TP6 as the ground references.

**Table 4-1. Connection and Test Points**

| Reference Designator | Function |
|---|---|
| J1 | $V_{IN}$ (see Table 1-1 for $V_{IN}$ range) |
| J2 | $V_{OUT2}$, 1.5 V at 3 A maximum |
| J3 | $V_{OUT1}$, 3.3 V at 2 A maximum |
| J4 | EN1 control. Connect EN1 to off to disable converter 1; connect EN1 to on to enable converter 1. |
| J5 | EN2 control. Connect EN2 to off to disable converter 2; connect EN2 to on to enable converter 2. |
| JP1 | Jumper to give the possibility to use another input voltage for converter 2. |
| TP1 | $V_{IN}$ test point at $V_{IN}$ connector |
| TP2 | $V_{IN2}$ test point after JP1. |
| TP3 | Output voltage test point for converter 2. |
| TP4 | Output voltage test point for converter 1. |
| TP5, TP6, TP7 | Ground test points at input and output connectors. |
| TP8 | EN2 test point. |
| TP9 | EN1 test point. |
| TP10 | Switch node test point of converter 1. |
| TP11 | Switch node test point of converter 2. |
| TP12 | VREG5 test point. |
| TP13 | PG1 test point. |
| TP14 | PG2 test point. |
| TP15 | Analog ground test point. |

## 4.2 Start-Up Procedure

1. Ensure that the jumper at J4 and/or J5 (Enable control) are set from ENx to off.
2. Apply appropriate $V_{IN}$ voltage to VIN and PGND terminals at J1.
3. Move the jumper at J4 and/or J5 (Enable control) to cover ENx and on. The EVM enables the according output voltage.

## 4.3 Efficiency

### 4.3.1 Efficiency of Converter 1

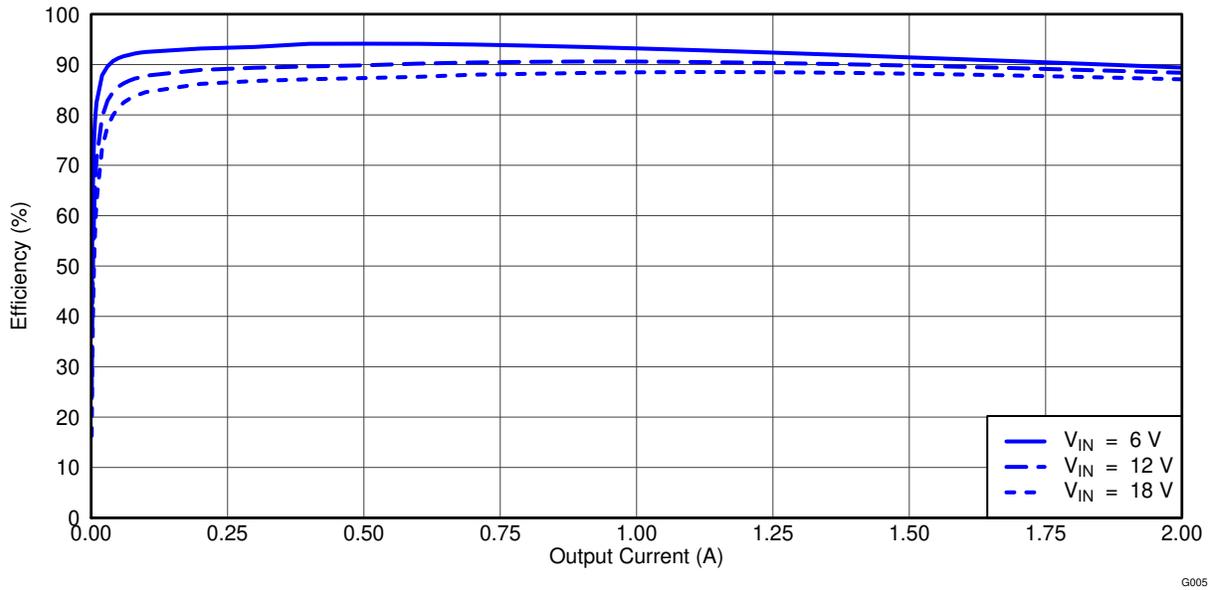Figure 4-1 shows the efficiency for the converter 1 on the TPS542951EVM at an ambient temperature of 25°C.



**Figure 4-1. TPS542951EVM Converter 1 Efficiency**

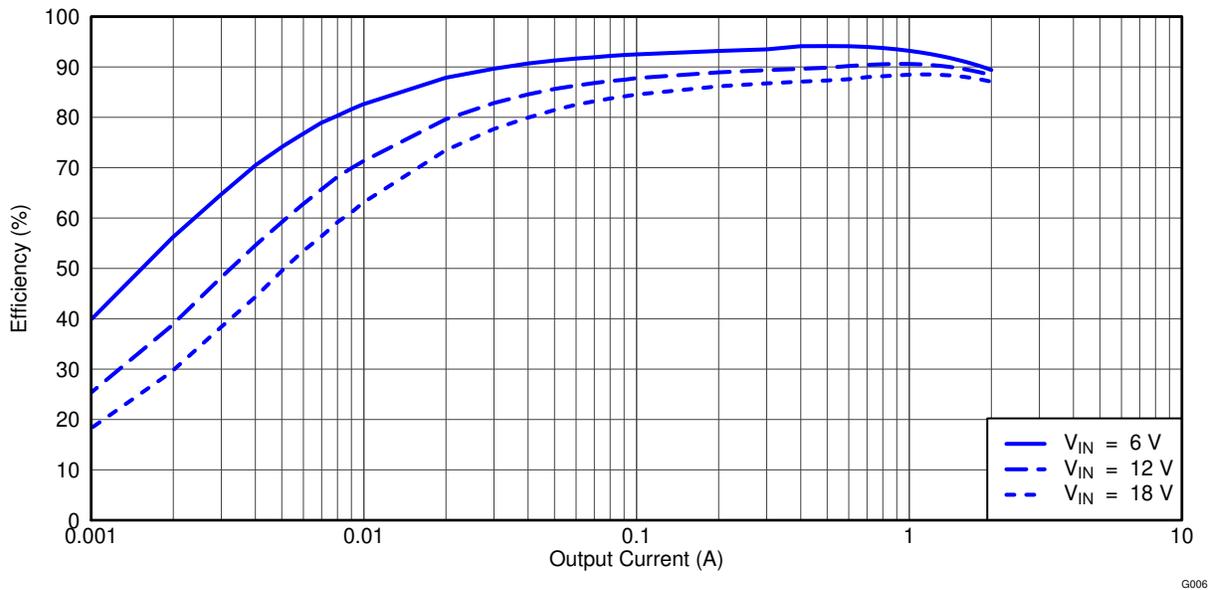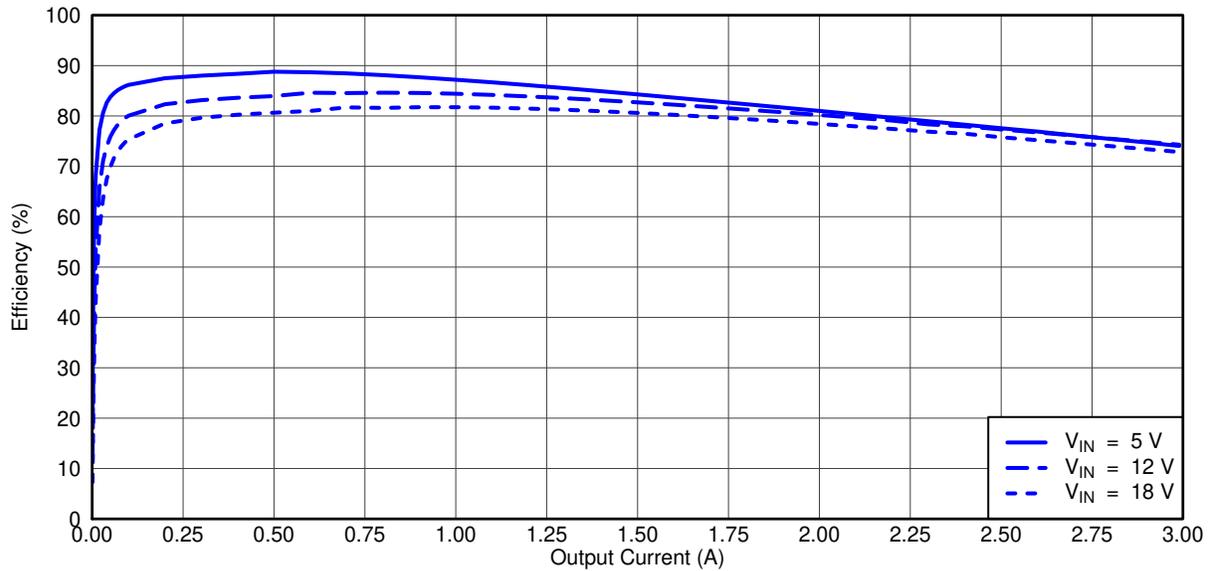Figure 4-2 shows the light load efficiency for converter 1 on the TPS542951EVM at an ambient temperature of 25°C.



**Figure 4-2. TPS542951EVM Converter 1 Light Load Efficiency**
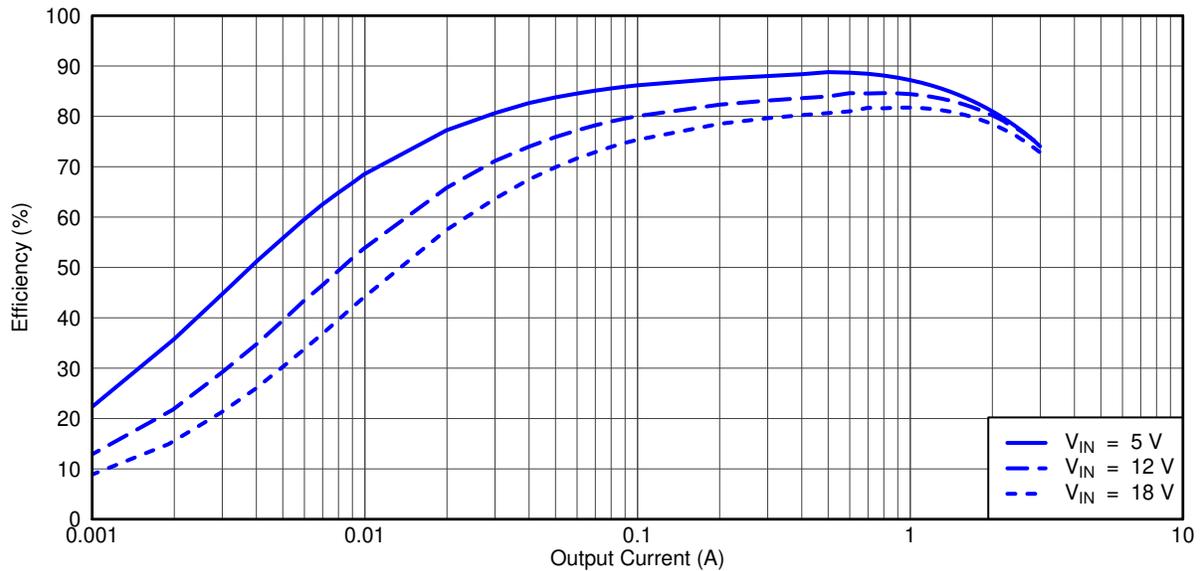
### 4.3.2 Efficiency of Converter 2

Figure 4-3 shows the efficiency for the converter 2 on the TPS542951EVM at an ambient temperature of 25°C.



**Figure 4-3. TPS542951EVM Converter 2 Efficiency**

Figure 4-4 shows the light load efficiency for the converter 2 on the TPS542951EVM at an ambient temperature of 25°C.



**Figure 4-4. TPS542951EVM Converter 2 Light Load Efficiency**

## 4.4 Load Regulation

### 4.4.1 Load Regulation of Converter 1

The load regulation for the converter 1 on the TPS542951EVM is shown in Figure 4-5. On the EVM, the load regulation of converter 1 is independent on the load of converter 2.
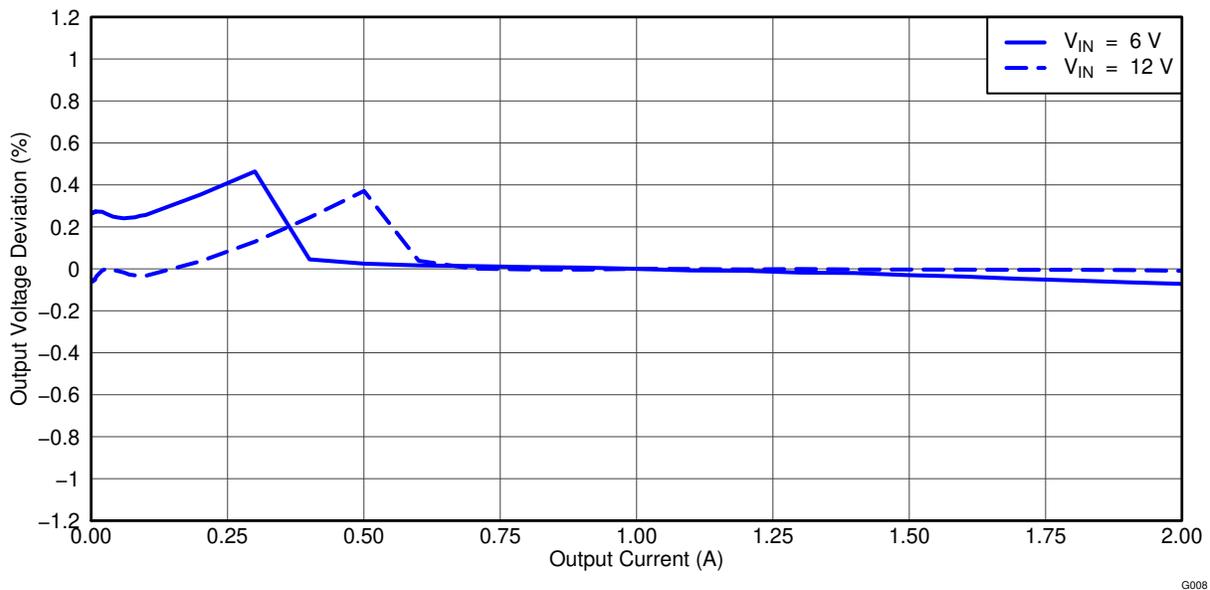


**Figure 4-5. TPS542951EVM Converter 1 Load Regulation**

### 4.4.2 Load Regulation of Converter 2

The load regulation for the converter 2 on the TPS542951EVM is shown in Figure 4-6. For 5V input voltage, the converter 2 shows on the EVM some dependency on the load of converter 1.
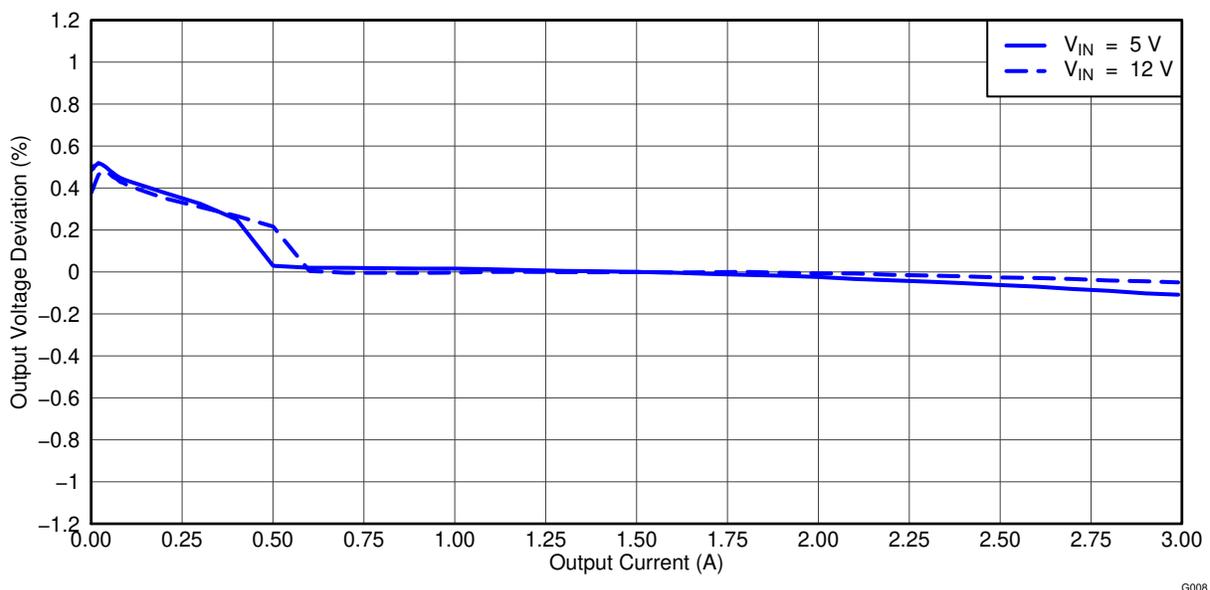


**Figure 4-6. TPS542951EVM Converter 2 Load Regulation**

## 4.5 Line Regulation

### 4.5.1 Line Regulation Converter 1

The line regulation of converter 1 on the TPS542951EVM is shown in Figure 4-7.
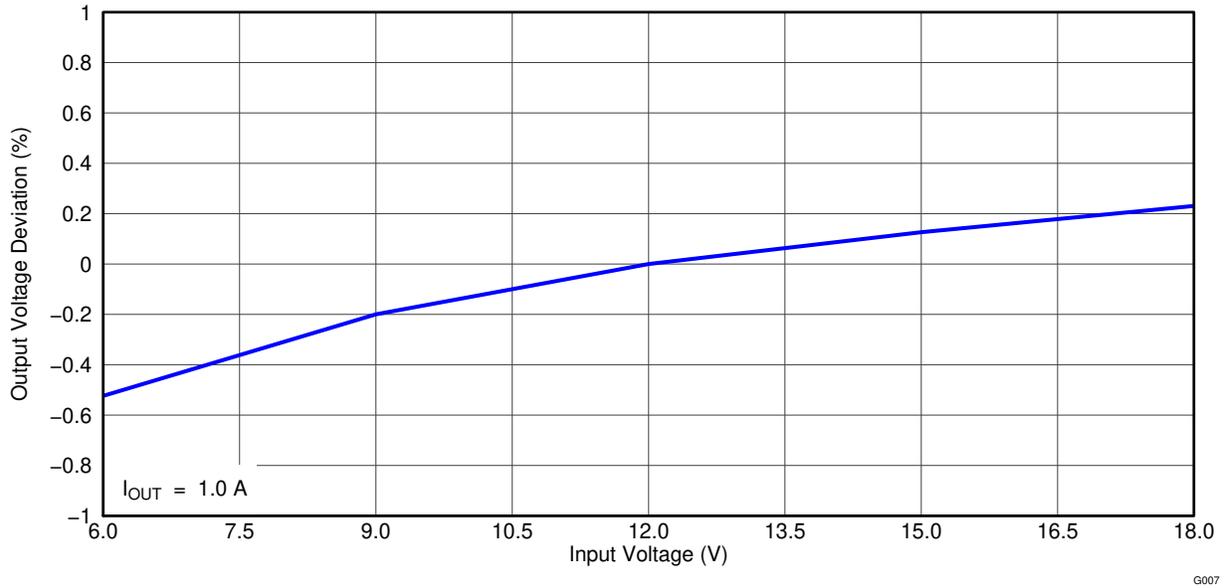


**Figure 4-7. TPS542951EVM Converter 1 Line Regulation**

### 4.5.2 Line Regulation Converter 2

The line regulation of converter 2 on the TPS542951EVM is shown in Figure 4-8.
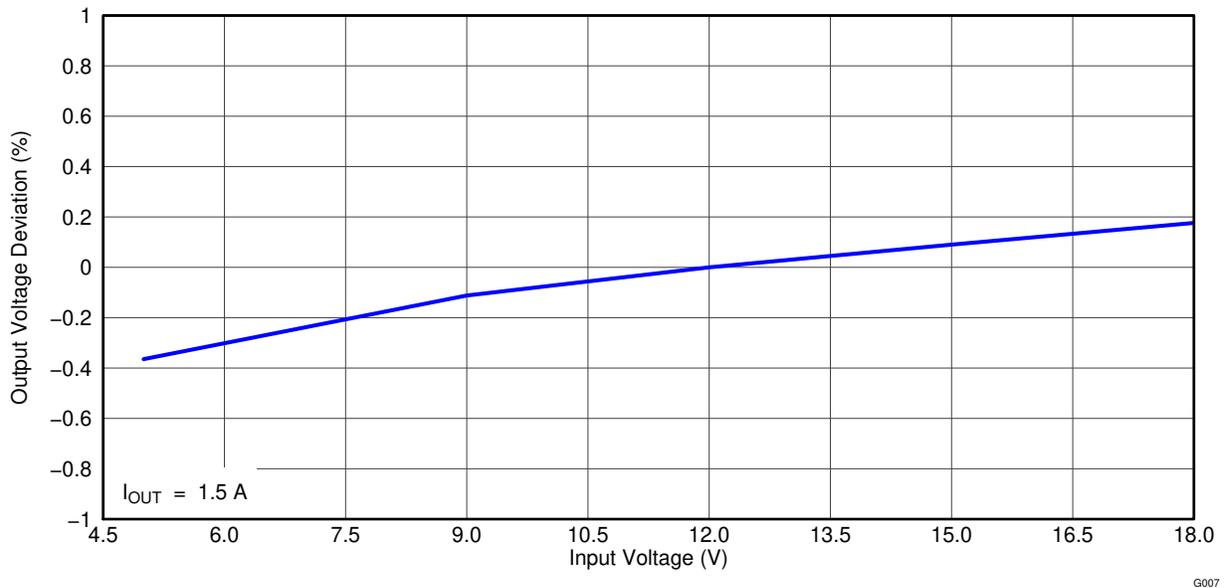


**Figure 4-8. TPS542951EVM Converter 2 Line Regulation**

## 4.6 Load Transient Response

### 4.6.1 Load Transient Response Converter 1

The response of converter 1 on the TPS542951EVM to a load transient is shown in Figure 4-9.
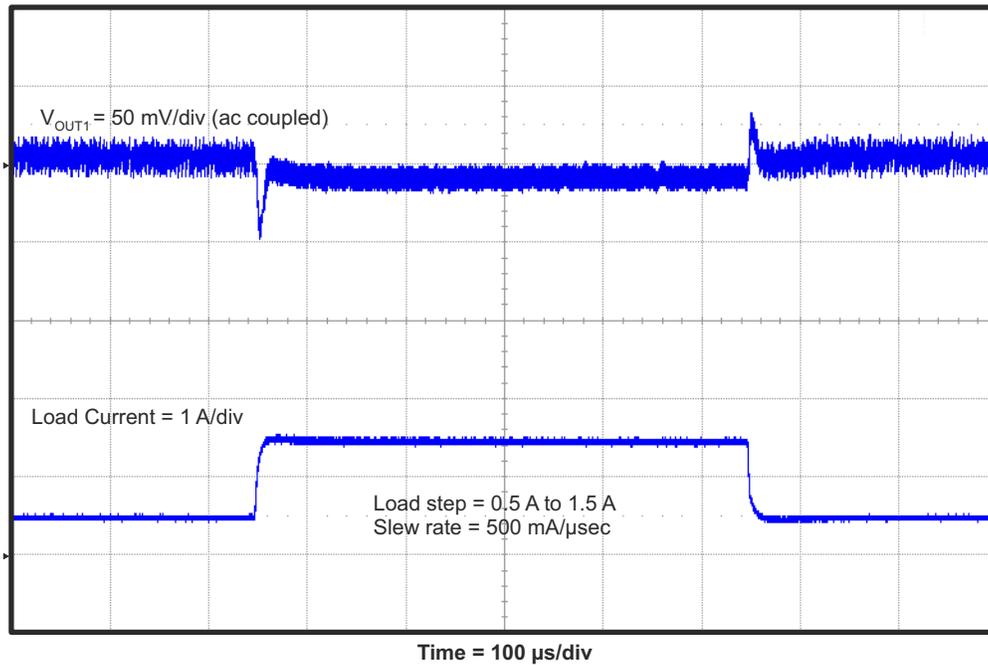


**Figure 4-9. TPS542951EVM Converter 1 Load Transient Response**

### 4.6.2 Load Transient Response Converter 2

The response of converter 2 on the TPS542951EVM to a load transient is shown in Figure 4-10.
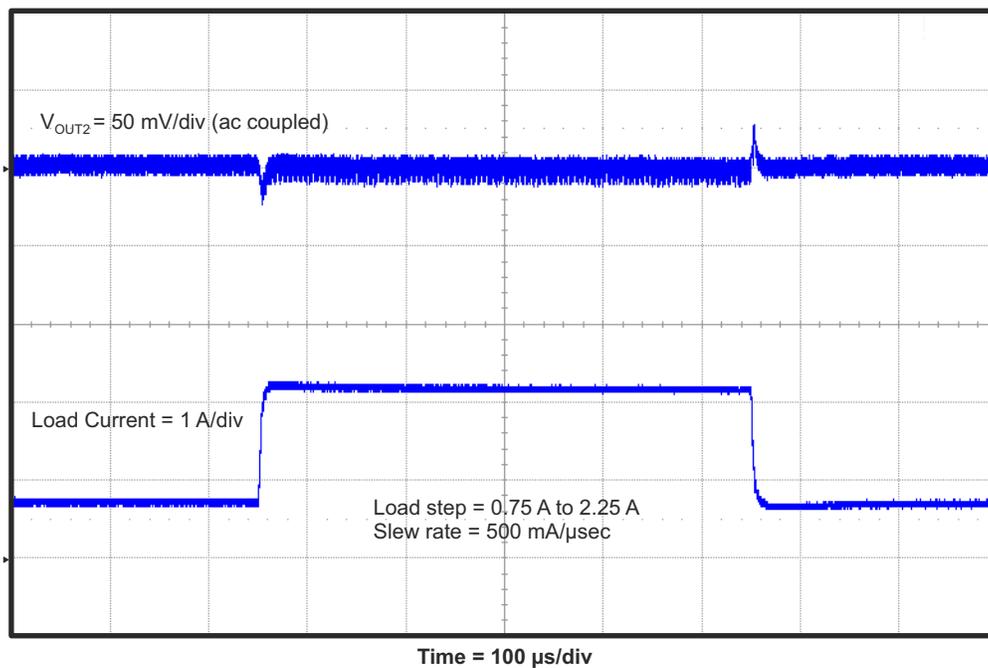


**Figure 4-10. TPS542951EVM Converter 2 Load Transient Response**

## 4.7 Output Voltage Ripple

### 4.7.1 Output Voltage Ripple Converter 1

The output voltage ripple of converter 1 on the TPS542951EVM is shown in Figure 4-11. The output current is the rated full load of 2 A.



**Time = 1 µs/div**
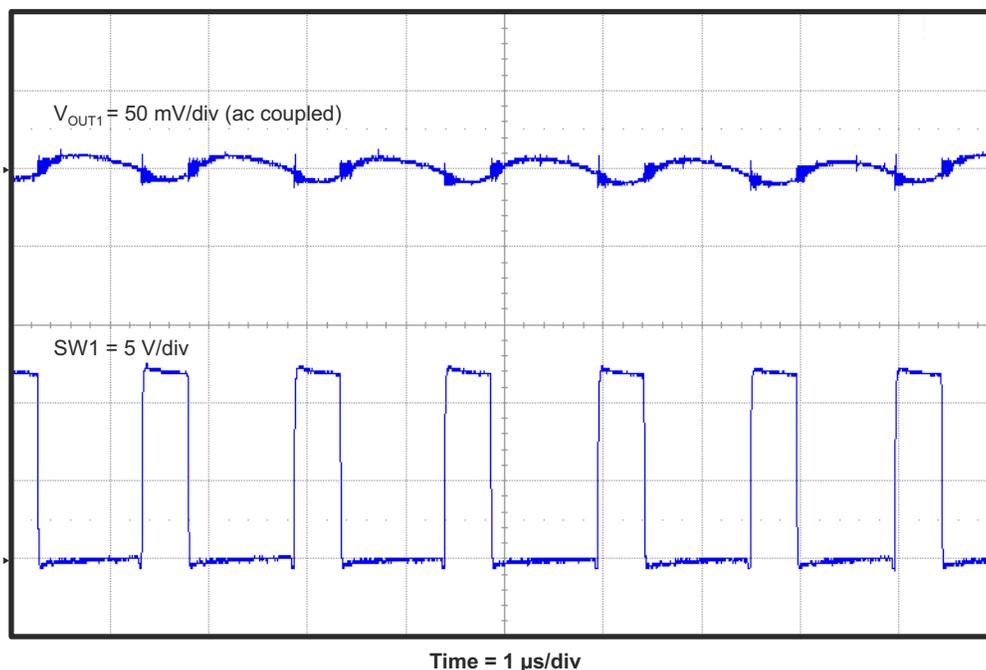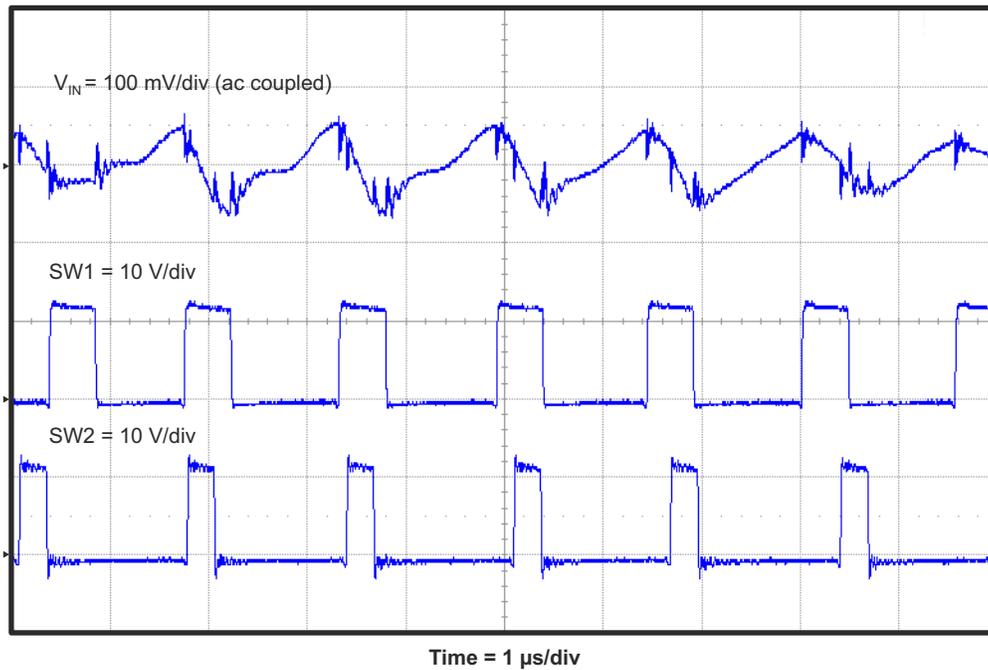
**Figure 4-11. TPS542951EVM Converter 1 Output Voltage Ripple**

The output voltage ripple of converter 1 on the TPS542951EVM during Eco-mode™ operation at no load is shown in Figure 4-12.



**Time = 10 ms/div**
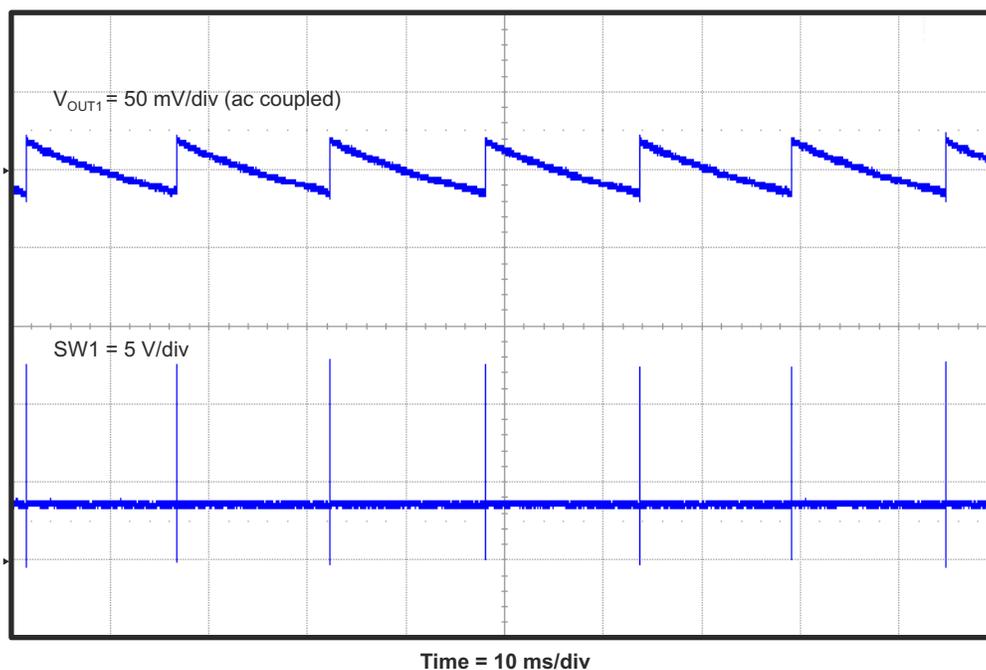
**Figure 4-12. TPS542951EVM Converter 1 Eco-mode™ Output Voltage Ripple at No Load**

### 4.7.2 Output Voltage Ripple Converter 2

The output voltage ripple of converter 2 on the TPS542951EVM is shown in Figure 4-13. The output current is the rated full load of 3 A.



**Time = 1 µs/div**
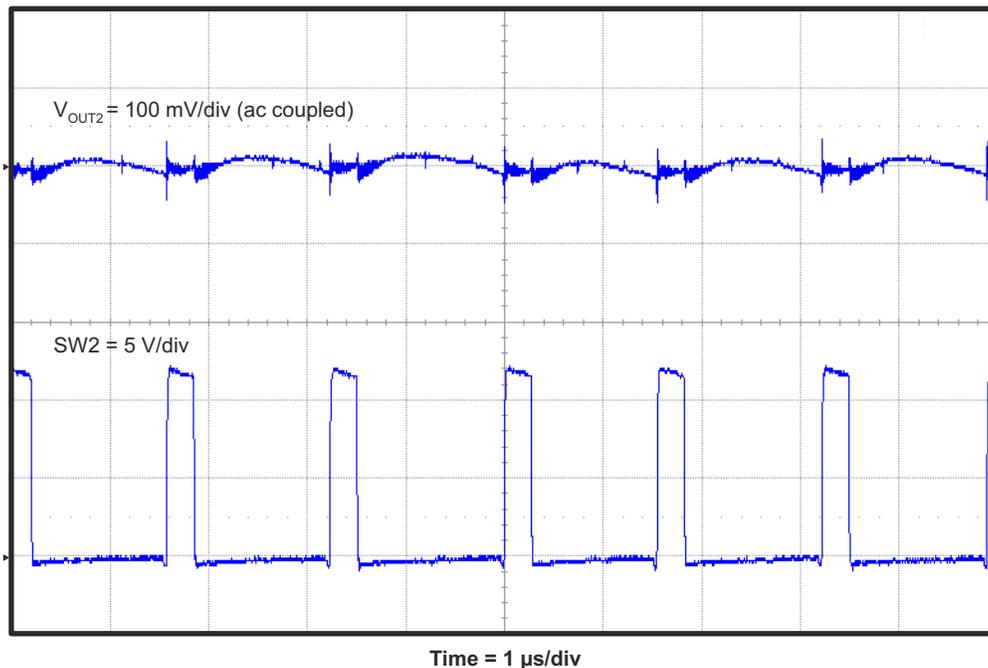
**Figure 4-13. TPS542951EVM Converter 2 Output Voltage Ripple**

The output voltage ripple of converter 2 on the TPS542951EVM during Eco-mode™ operation at no load is shown in Figure 4-14.



**Time = 10 ms/div**
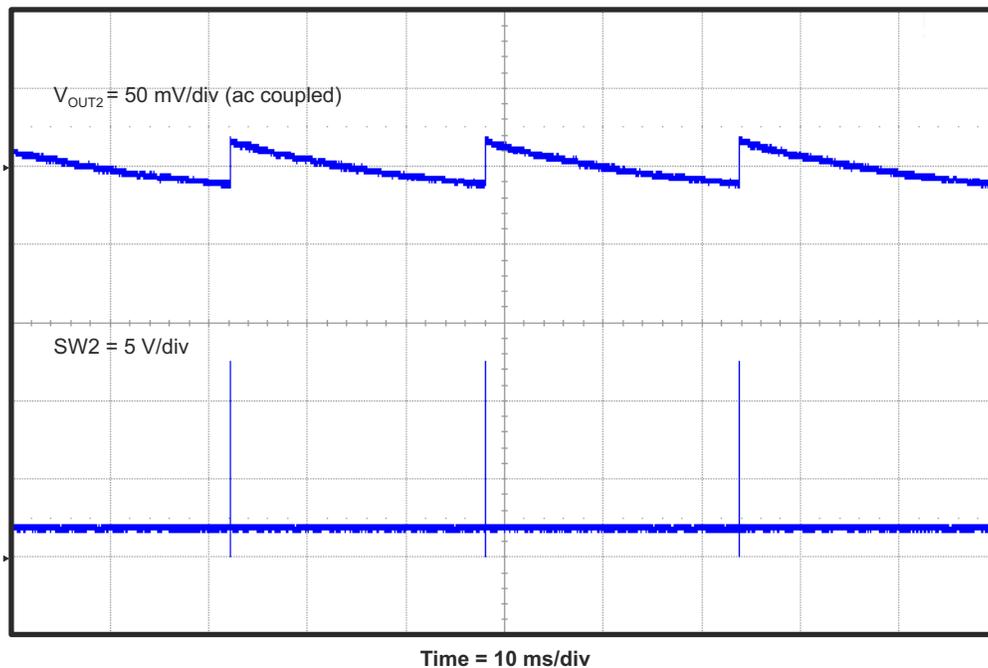
**Figure 4-14. TPS542951EVM Converter 2 Eco-mode™ Output Voltage Ripple at No Load**

## 4.8 Input Voltage Ripple

The TPS542951EVM input voltage ripple is shown in Figure 4-15. The output currents are the rated full load currents of 2 A CH1 and 3 A CH2.



**Time = 1 µs/div**

**Figure 4-15. TPS542951EVM Input Voltage Ripple**

## 4.9 Start-Up

### 4.9.1 Converter 1 Start-Up

The TPS542951EVM start-up waveform of converter 1 relative to $V_{IN}$ is shown in Figure 4-16.
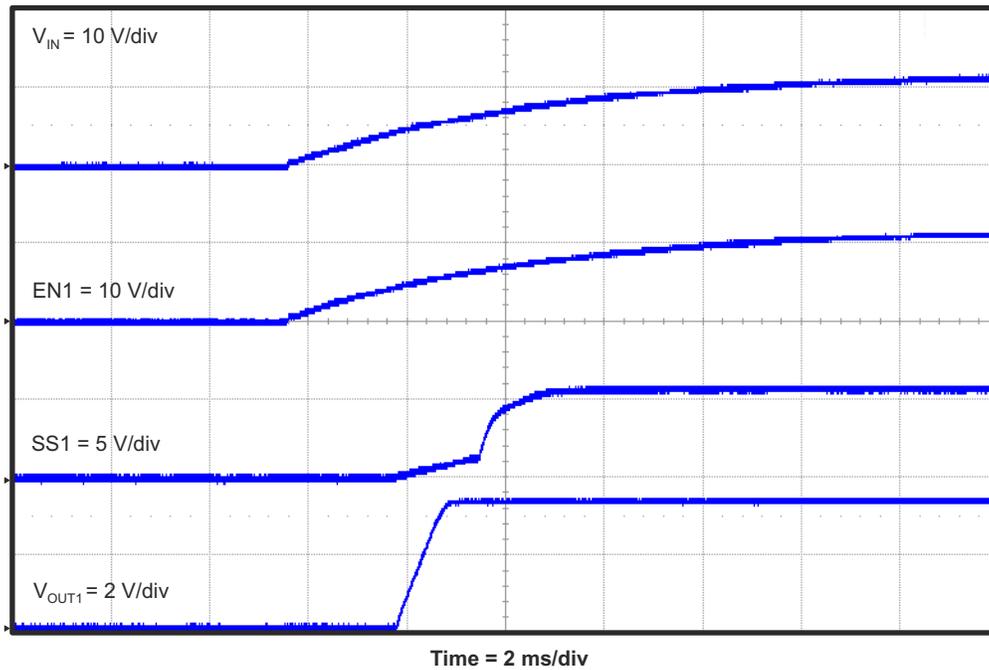


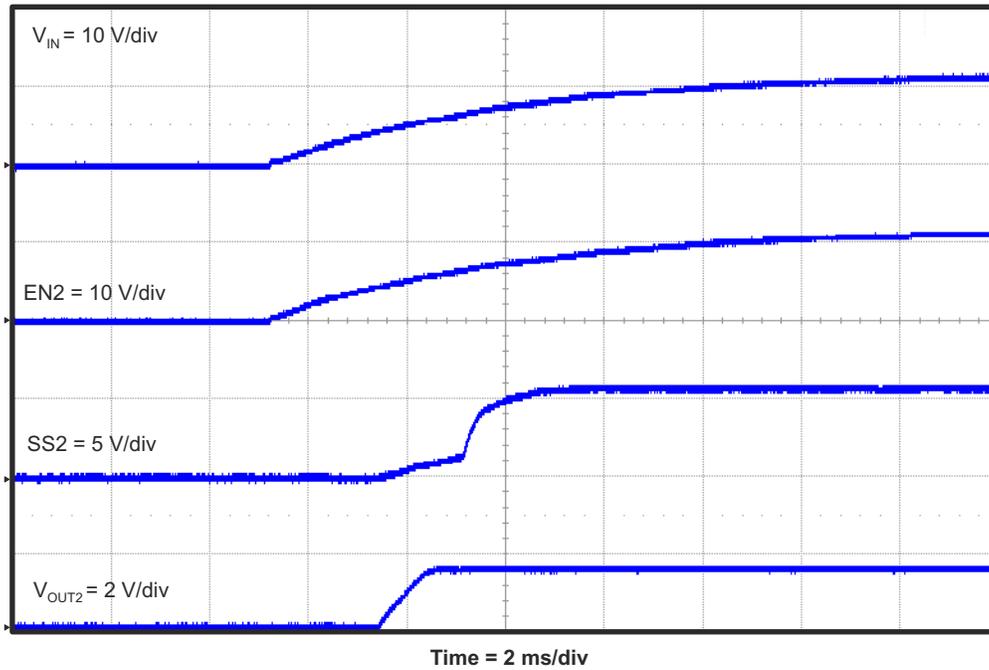**Figure 4-16. TPS542951EVM Converter 1 Start-Up Relative to $V_{IN}$**

The TPS542951EVM start-up waveform of converter 1 relative to EN1 is shown in Figure 4-17.
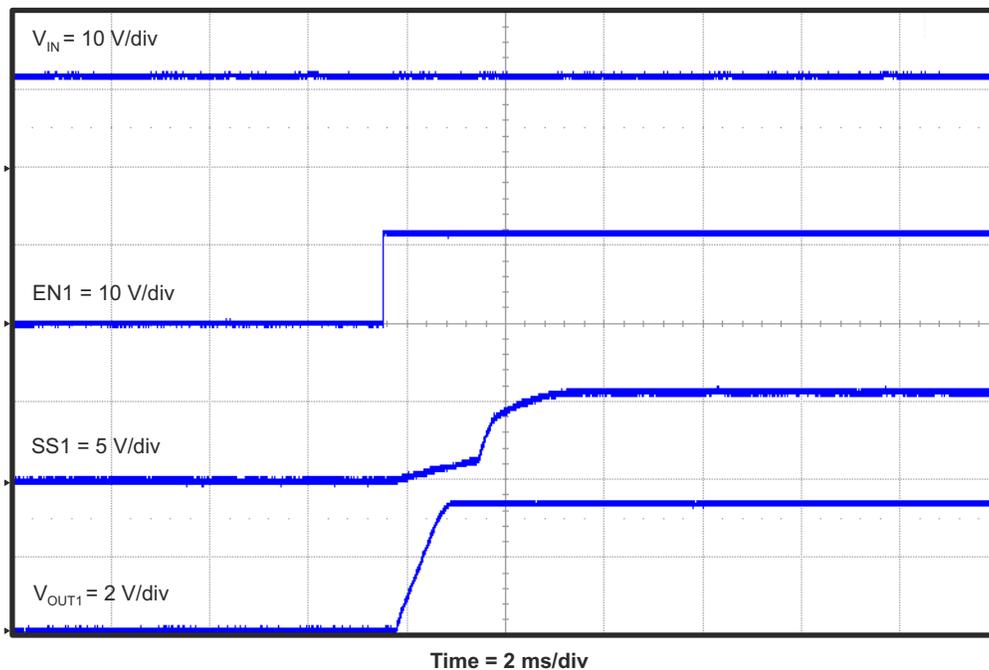


**Figure 4-17. TPS542951EVM Start-Up Relative to EN1**

### 4.9.2 Converter 2 Start-Up

The TPS542951EVM start-up waveform of converter 2 relative to $V_{IN}$ is shown in Figure 4-18.



**Figure 4-18. TPS542951EVM Converter 2 Start-Up Relative to $V_{IN}$**

The TPS542951EVM start-up waveform of converter 2 relative to EN2 is shown in Figure 4-19.
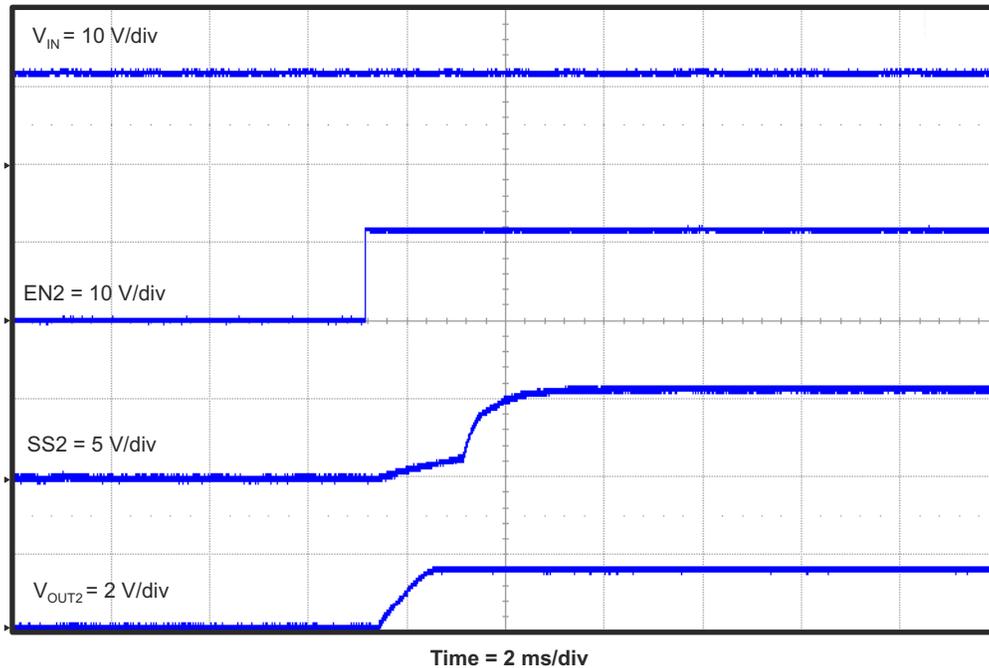


**Figure 4-19. TPS542951EVM Start-Up Relative to EN2**

# 5 Board Layout

This section provides a description of the TPS542951EVM, board layout, and layer illustrations.

## 5.1 Layout

The board layout for the TPS542951EVM is shown in Figure 5-1 through Figure 5-6. The top layer contains the main power traces for VIN and VOUTx. Also on the top layer are connections for the pins of the TPS542951 and a large area filled with ground. Many of the signal traces also are located on the top side. The input decoupling capacitors are located as close to the IC as possible. The input and output connectors, test points, and all of the assembled components are located on the top side. An analog ground (GND) area is provided on the top side. Analog ground (GND) and power ground (PGND) are connected at a single point on the top layer near the IC. The other layers are primarily power ground but the bottom layer has some traces to connect the test points for SSx and ENx.
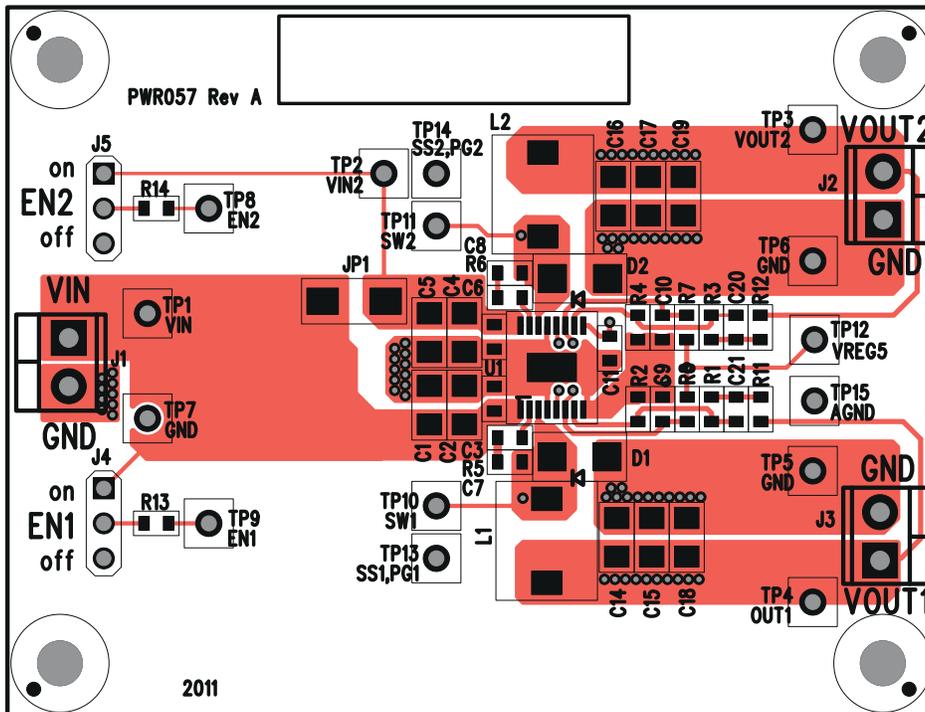


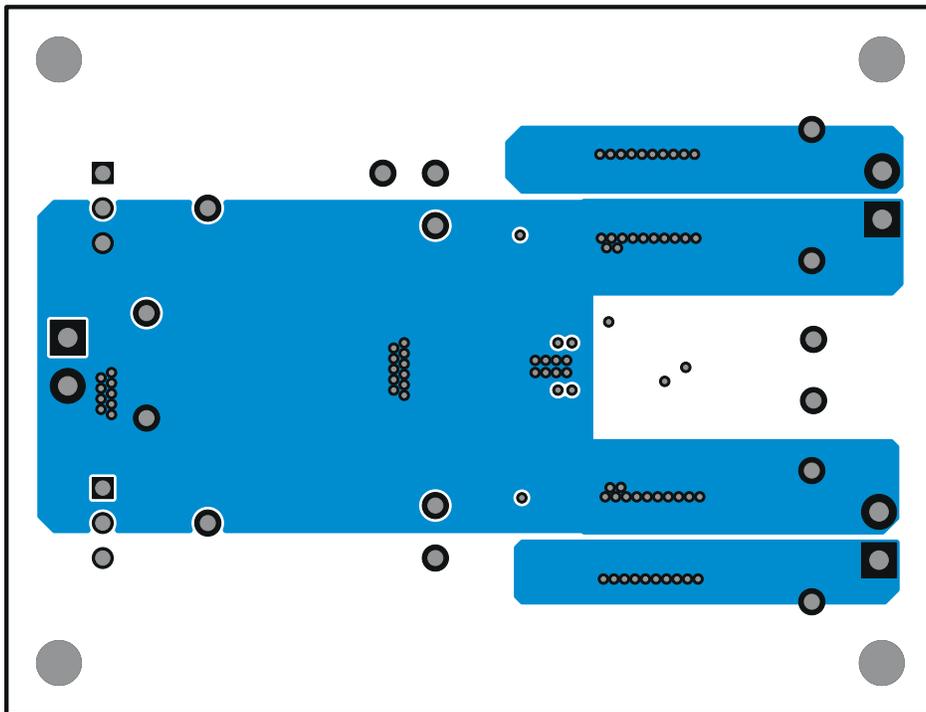**Figure 5-1. Top Assembly**
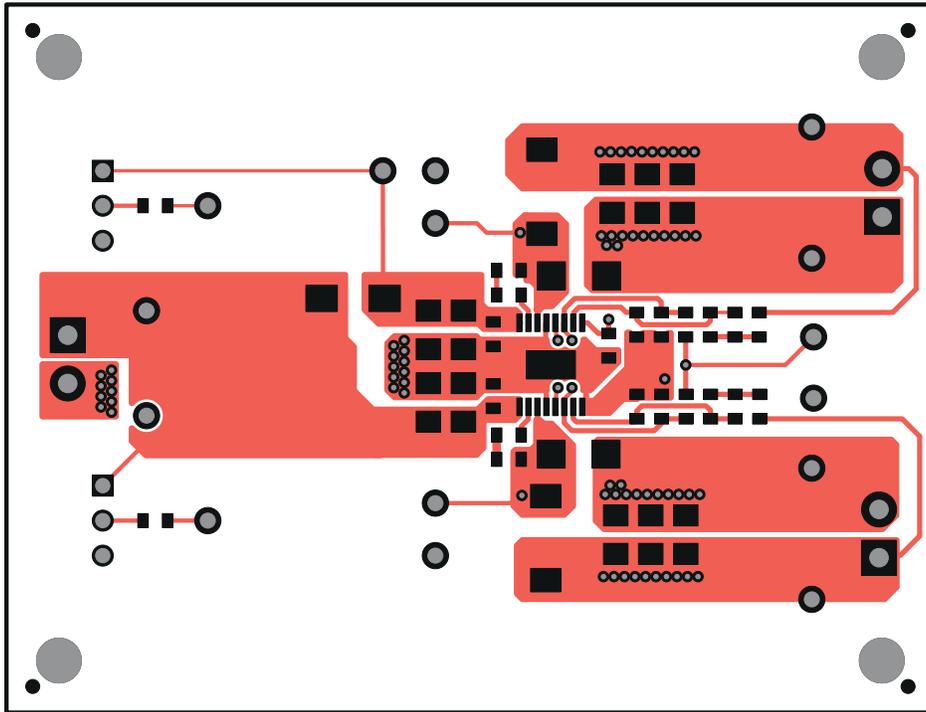
**Figure 5-2. Top Layer**



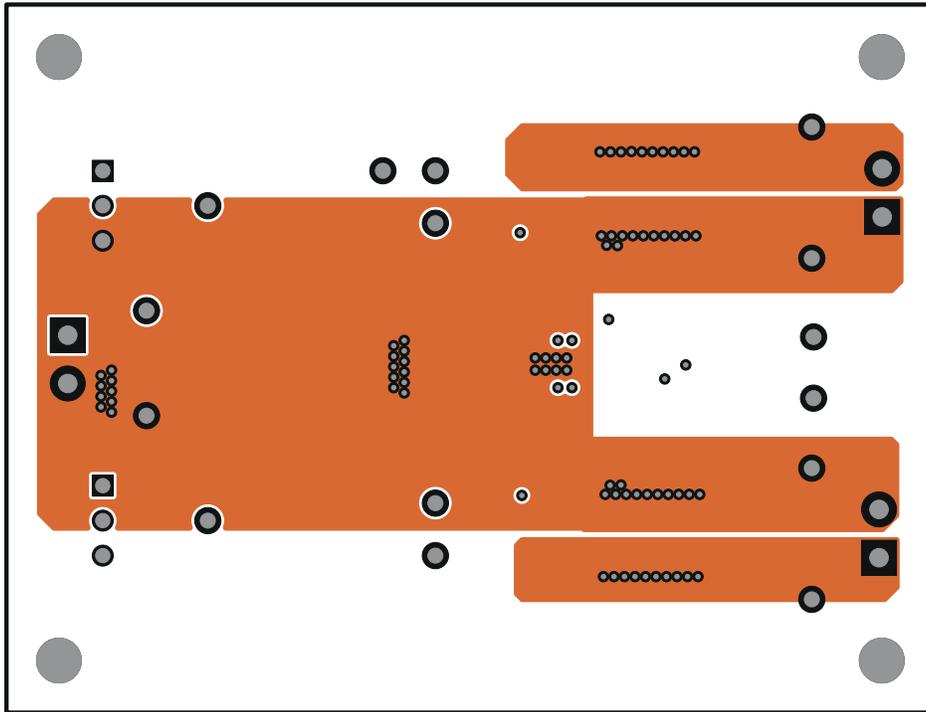**Figure 5-3. Internal 1 Layer**

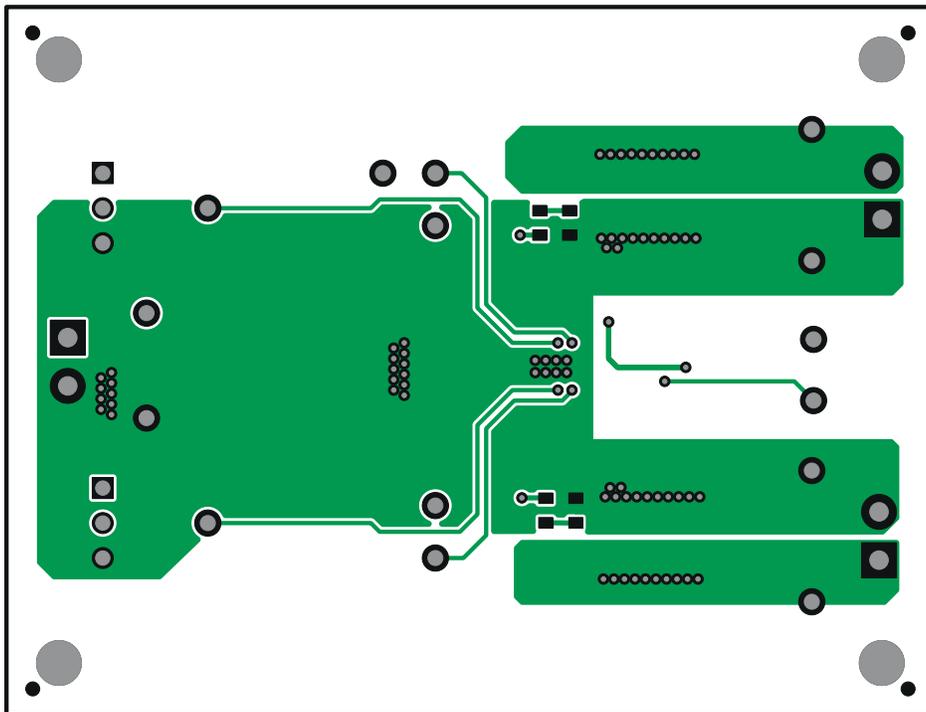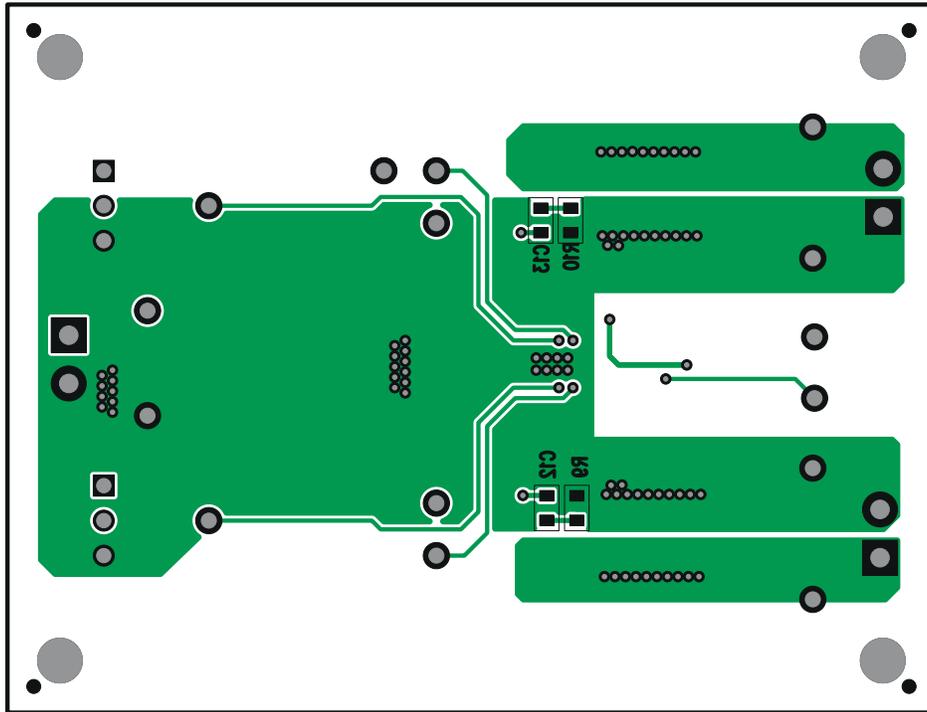**Figure 5-4. Internal 2 Layer**



**Figure 5-5. Bottom Layer**

**Figure 5-6. Bottom Assembly**

# 6 Schematic, Bill of Materials, and Reference

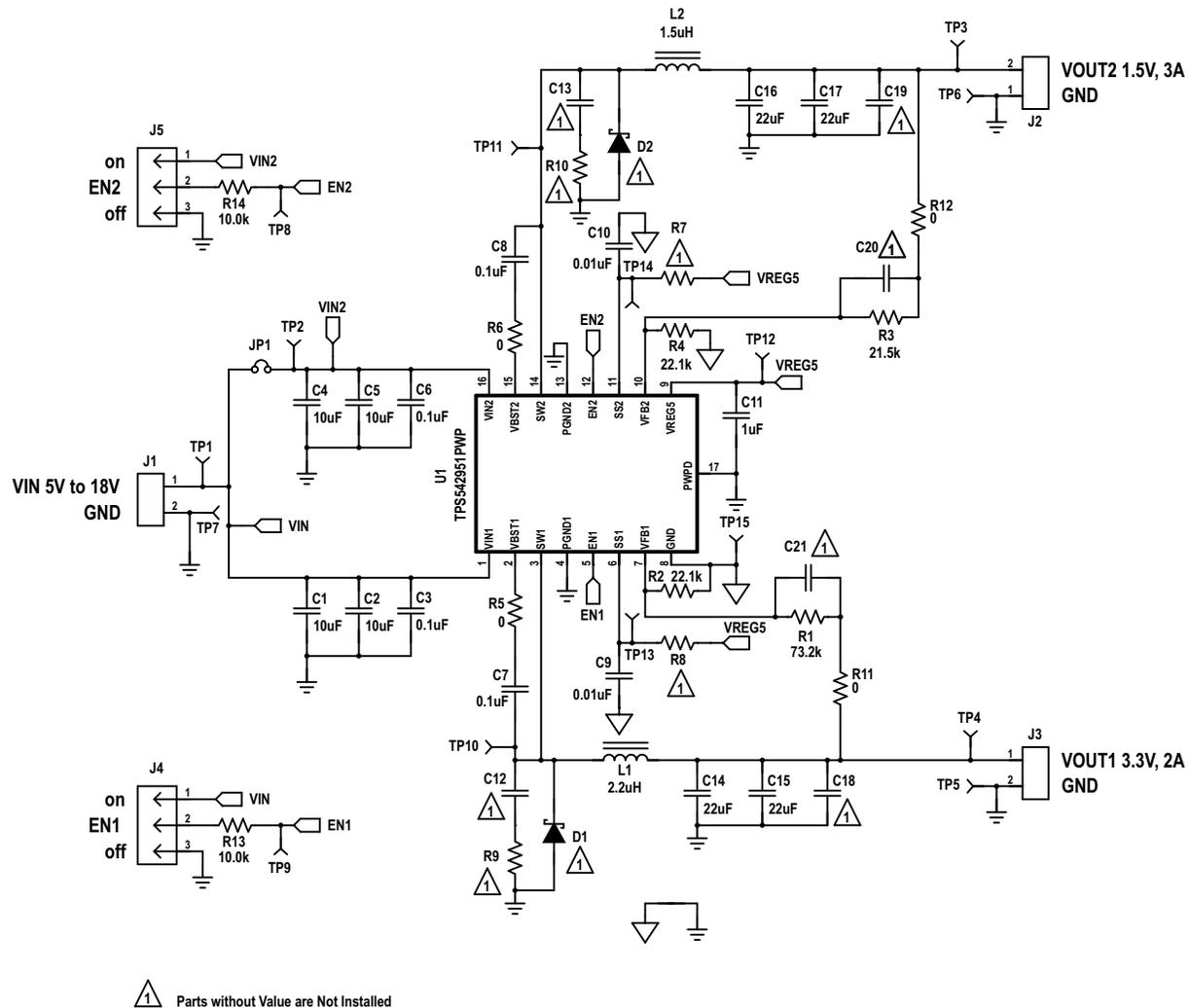## 6.1 Schematic

Figure 6-1 is the schematic for the TPS542951EVM.



**Figure 6-1. TPS542951EVM Schematic Diagram**

## 6.2 Bill of Materials

### Table 6-1. Bill of Materials

| Count | RefDes | Value | Description | Size | Part Number | Manufacturer |
|-------|--------|-------|-------------|------|-------------|--------------|
| 1 | C11 | 1 µF | Capacitor, ceramic, 16 V, X7R, 10% | 0603 | GRM188R71C105KA12 | Murata |
| 4 | C1-2 C4-5 | 10 µF | Capacitor, ceramic, 25 V, X7R, 10% | 1206 | GRM31CR71E106KA12 | Murata |
| 0 | C12-13 | open | Capacitor, ceramic, 50 V, X7R, 10% | 0603 | GRM188R71H104KA93 | Murata |
| 4 | C14-17 | 22 µF | Capacitor, ceramic, 6.3 V, X7R, 10% | 1206 | GRM31CR70J226KE19 | Murata |
| 0 | C18-19 | open | Capacitor, ceramic, 6.3 V, X7R, 10% | 1206 | | |
| 0 | C20-21 | open | Capacitor, ceramic, 50 V, X7R, 10% | 0603 | Std | Std |
| 4 | C3 C6-8 | 0.1 µF | Capacitor, ceramic, 50 V, X7R, 10% | 00603 | GRM188R71H104KA93 | Murata |
| 2 | C9-10 | 0.01 µF | Capacitor, ceramic, 50 V, X7R, 10% | 0603 | Std | Std |
| 0 | D1-2 | open | Diode, Schottky | SMA | STD | STD |
| 1 | L1 | 2.2 µH | Inductor, power line, magnetic shielded, ±30%, 4.3 A | 6.9 × 7.2 mm | SPM6530-2R2M | TDK |
| 1 | L2 | 1.5 µH | Inductor, power line, magnetic shielded, ±30%, 4.1 A | 6.9 × 7.2 mm | SPM6530-1R5M | TDK |
| 1 | R1 | 73.2 kΩ | Resistor, chip, 1/16W, 1% | 0603 | STD | STD |
| 2 | R11-12 | 0 Ω | Resistor, chip, 1/16W, 5% | 0603 | STD | STD |
| 2 | R13-14 | 10.0 kΩ | Resistor, chip, 1/16W, 1% | 0603 | STD | STD |
| 2 | R2 R4 | 22.1 kΩ | Resistor, chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | R3 | 21.5 kΩ | Resistor, chip, 1/16W, 1% | 0603 | STD | STD |
| 2 | R5-6 | 0 Ω | Resistor, chip, 1/16W, 1% | 0603 | STD | STD |
| 0 | R7-8 | open | Resistor, chip, 1/16W, 1% | 0603 | STD | STD |
| 0 | R9-10 | open | Resistor, chip, 1/16W, 1% | 0603 | STD | STD |
| 1 | U1 | TPS542951PWP | IC, 2A/3A, dual output fully synchronous buck converter with integrated FET | TSSOP | TPS542951PWP | TI |

C14-C19 must be replaced with capacitors which have a higher voltage rating when the output voltage is set above 4V.

## 6.3 Reference

Texas Instruments, *TPS542951, 3-A Dual Channel Synchronous Step-Down Switcher With Integrated FETs Data Sheet*

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

# IMPORTANT NOTICE AND DISCLAIMER