

TPS61021A-PWR723 Evaluation Module

This user's guide describes the characteristics, operation, and the use of the TPS61021EVM-723 evaluation module (EVM). The EVM contains the TPS61021A, which is a 3-A boost converter with 0.5-V ultra-low input voltage. This user's guide includes EVM specifications, recommended test setup, test results, a schematic diagram, bill of materials (BOM), and the board layout.

Contents

1	Introduction	2
2	Setup	2
3	Test Results	3
4	Schematic and Bill of Materials	6
5	Board Layout	8

List of Figures

1	Startup Waveforms (No Load)	3
2	TPS61021A EVM Efficiency vs Load Current	3
3	Load Transient ($V_o = 3.3$ V, $I_o = 1$ A to 2 A)	4
4	Loop Bode Plot ($V_{IN} = 2.4$ V, $V_o = 3.3$ V / $I_o = 2$ A)	4
5	Output Ripple in CCM ($V_{IN} = 2.4$ V, $V_o = 3.3$ V / $I_o = 2$ A)	5
6	Output Ripple in PFM ($V_{IN} = 2.4$ V, $V_o = 3.3$ V / $I_o = 160$ mA)	5
7	TPS61021EVM-723 Schematic	6
8	TPS61021EVM-723 Top-Side Layout	8
9	TPS61021EVM-723 Bottom-Side Layout	8

List of Tables

1	Performance Specification Summary	2
2	TPS61021EVM-723 Bill of Materials	7

1 Introduction

1.1 Performance Specification

Table 1 provides a summary of the TPS61021A EVM performance specifications. All the specifications are given for an ambient temperature of 25°C.

Table 1. Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input voltage		0.9	2.4	3.2	V
Output voltage	TPS61021A EVM, $V_{IN} = 2.4$ V, $I_o \leq 2$ A	3.2	3.3	3.4	V
Output current	$V_{IN} = 1.2$ V			1	A
	$V_{IN} = 2.4$ V			2.3	A

1.2 Modification

The printed-circuit board (PCB) for this EVM is designed to accommodate some modifications by the user. The external component can be changed according to the real application.

1.3 Input Capacitor

A 150- μ F tantalum capacitor, C1, is added as the input capacitor in the EVM. The ESR of the tantalum capacitor is 0.1 Ω , to damp the ringing of the input voltage when the EVM is powered by a power supply with a long cable. The capacitor is not required for proper operation and can be removed in a real application.

1.4 Feedforward Capacitor

A feedforward capacitor, C7 in Figure 7, is used to improve the phase margin of the boost converter. Equation 1 calculates the zero frequency formed by the feedforward capacitor C7, and the resistor R1 of the feedback resistor divider.

$$f_z = \frac{1}{2\pi \times R1 \times C7} \quad (1)$$

TI recommends setting f_z at 50 kHz to boost the phase margin at the crossover frequency. When $R1 = 316$ k Ω , C7 is 10 pF on the EVM.

2 Setup

This section describes how to properly connect, set up, and use the TPS61021EVM-723.

2.1 Input/Output Connector Descriptions

The following :

J1-VIN	Positive input connection from the input supply for the EVM
J2-GND	Return connection from the input supply for the EVM
J5-VOUT	Positive connection for the output voltage
J6-GND	Return connection for the output voltage
J7-EN	EN pin input jumper. Place a jumper across EN and pin 1 to turn on the IC, place a jumper across EN and pin 3 to turn off the IC

3 Test Results

3.1 Startup Waveform

The startup waveform is shown in [Figure 1](#).

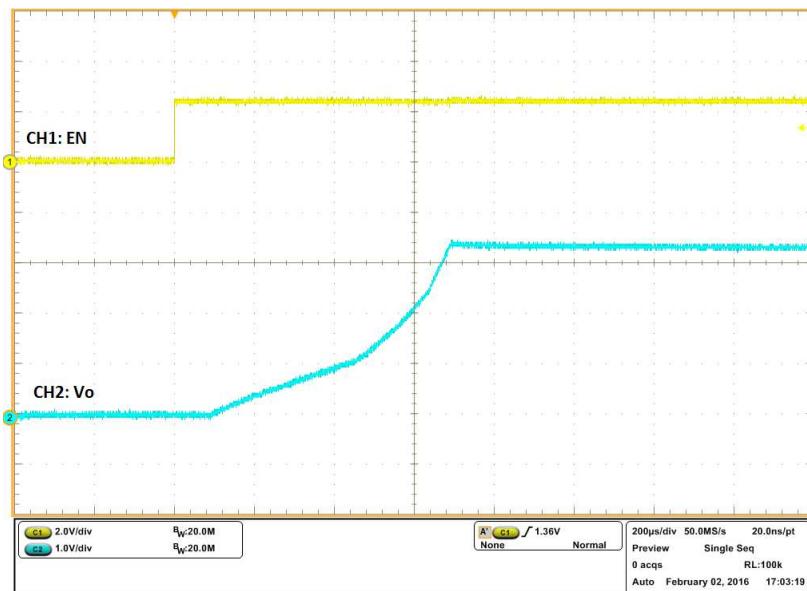


Figure 1. Startup Waveforms (No Load)

3.2 Efficiency

The conversion efficiency is shown in [Figure 2](#).

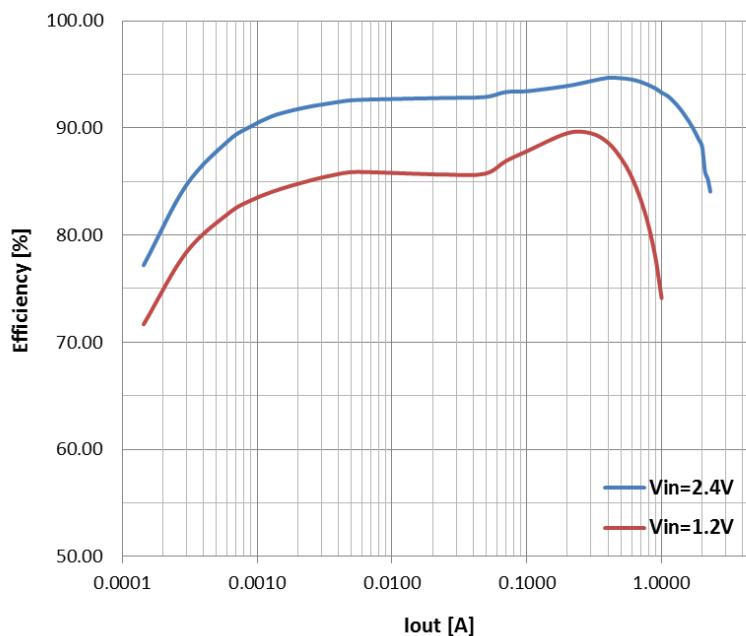


Figure 2. TPS61021A EVM Efficiency vs Load Current

3.3 Load Transient

The load transient waveform is shown in [Figure 3](#). Note that the effective output capacitance is about 31 μF under $V_o = 3.3$ V DC bias, although two 22- μF ceramic capacitors are used in the EVM. Larger effective capacitance helps to improve the load transient.

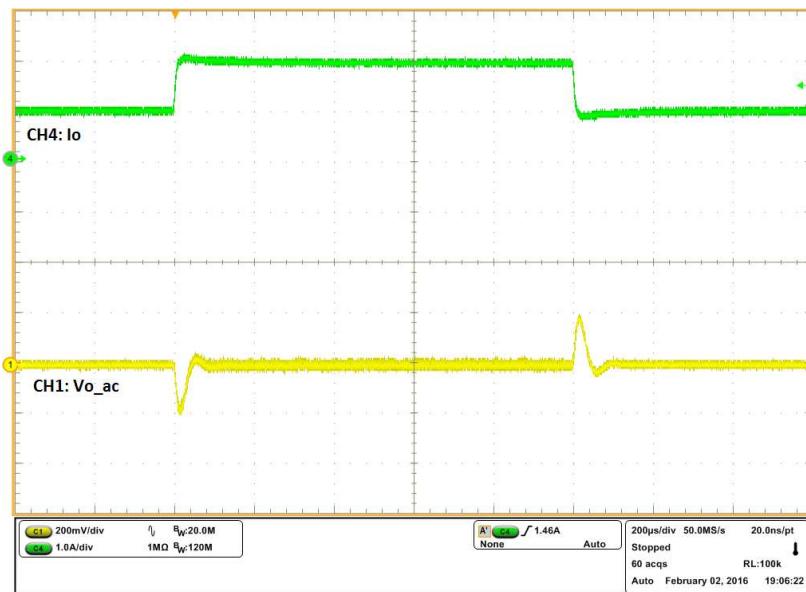


Figure 3. Load Transient ($V_o = 3.3$ V, $I_o = 1$ A to 2 A)

3.4 Loop Characteristics

The loop Bode plot is shown in [Figure 4](#).

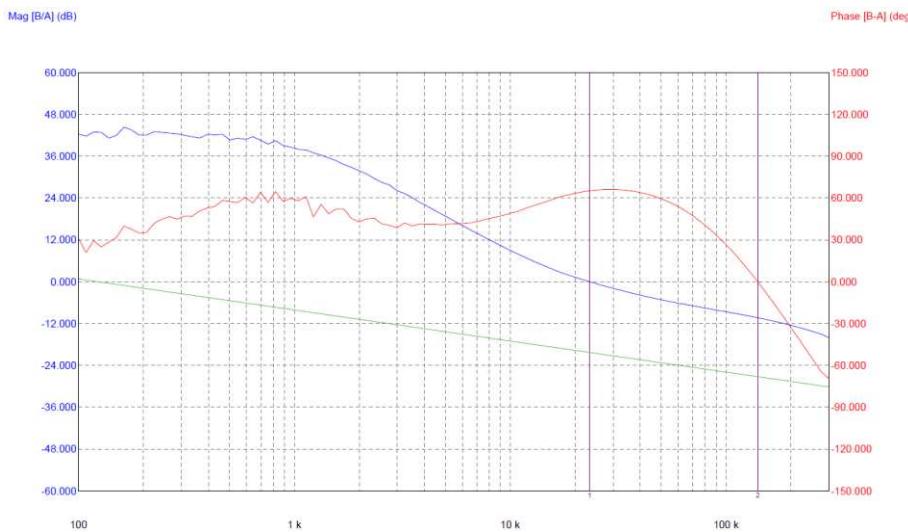


Figure 4. Loop Bode Plot ($V_{IN} = 2.4$ V, $V_o = 3.3$ V / $I_o = 2$ A)

3.5 Output Voltage Ripple

Figure 5 shows the output voltage ripple, switching waveforms, and the inductor current ripple in CCM mode.

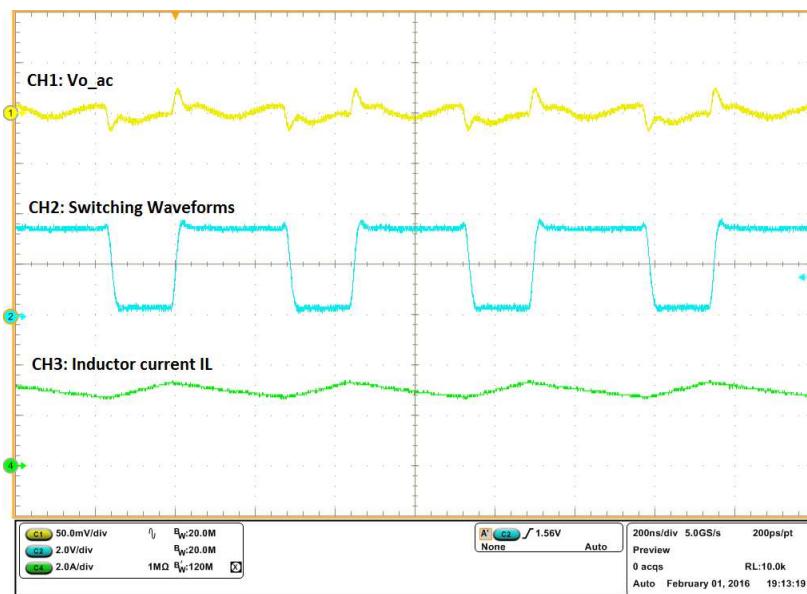


Figure 5. Output Ripple in CCM ($V_{IN} = 2.4$ V, $V_O = 3.3$ V / $I_O = 2$ A)

Figure 6 shows the output voltage ripple, switching waveforms, and the inductor current ripple in PFM mode when the converter is operating at light load.

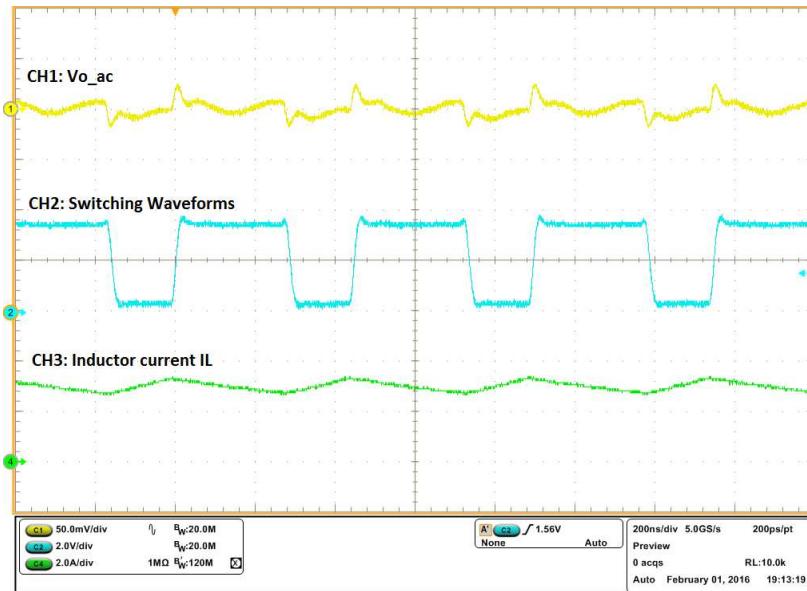


Figure 6. Output Ripple in PFM ($V_{IN} = 2.4$ V, $V_O = 3.3$ V / $I_O = 160$ mA)

4 Schematic and Bill of Materials

This section provides the TPS61021EVM-723 schematic, bill of materials (BOM), and board layout.

4.1 Schematic

Figure 7 illustrates the EVM schematic.

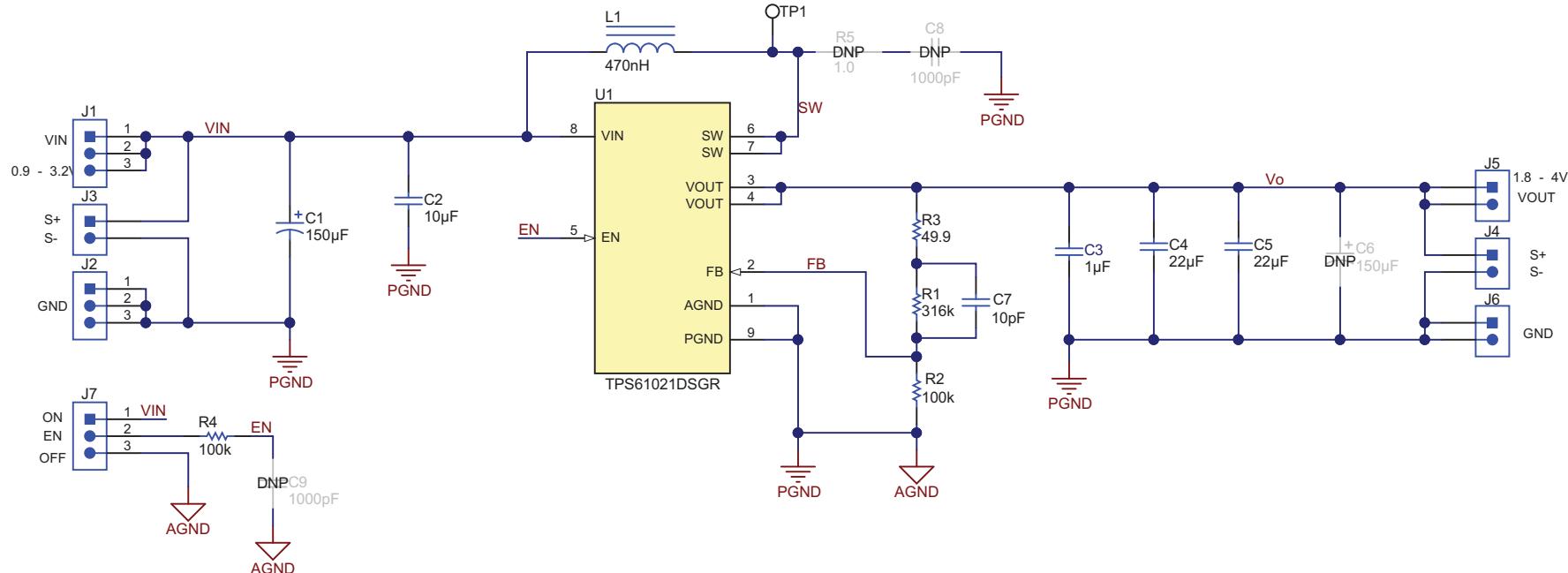


Figure 7. TPS61021EVM-723 Schematic

4.2 Bill of Materials

Table 2 displays the EVM bill of materials.

Table 2. TPS61021EVM-723 Bill of Materials

Designator	QTY	Value	Description	Package	Part Number	MFG
C1	1	150uF	CAP, TA, 150 μ F, 10 V, +/- 10%, 0.1 ohm, SMD	7343-31	T495D157K010ATE100	Kemet
C2	1	10uF	CAP, CERM, 10 μ F, 6.3 V, +/- 20%, X5R, 0603	0603	GRM188R60J106ME47D	MuRata
C3	1	1uF	CAP, CERM, 1 μ F, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E105KA12D	MuRata
C4, C5	2	22uF	CAP, CERM, 22 μ F, 10 V, +/- 20%, X5R, 0805	0805	GRM21BR61A226ME44L	MuRata
C7	1	10pF	CAP, CERM, 10 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C2A100JA01D	MuRata
J1, J2, J7	3		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J3, J4, J5, J6	4		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
L1	1	470nH	Inductor, Shielded, Composite, 470 nH, 3.5 A, 0.0076 ohm, SMD	SMD, 4x4x1.5mm	XFL4015-471MEC	Coilcraft
R1	1	316k	RES, 316 k, 1%, 0.1 W, 0603	0603	RC0603FR-07316KL	Yageo America
R2, R4	2	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R3	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo America
U1	1		3-A BOOST CONVERTER WITH 0.5V ULTRA-LOW INPUT VOLTAGE, DSG0008A	DSG0008A	TPS61021ADSGR	Texas Instruments
C6	0	150uF	CAP, TA, 150 μ F, 10 V, +/- 10%, 0.1 ohm, SMD	7343-31	T495D157K010ATE100	Kemet
C8, C9	0	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	0603	C0603C102K5RACTU	Kemet
R5	0	1.0	RES, 1.0, 5%, 0.1 W, 0603	0603	CRCW06031R00JNEA	Vishay-Dale

5 Board Layout

Figure 8 and Figure 9 show the design of the TPS61021EVM-723 PCB layout.

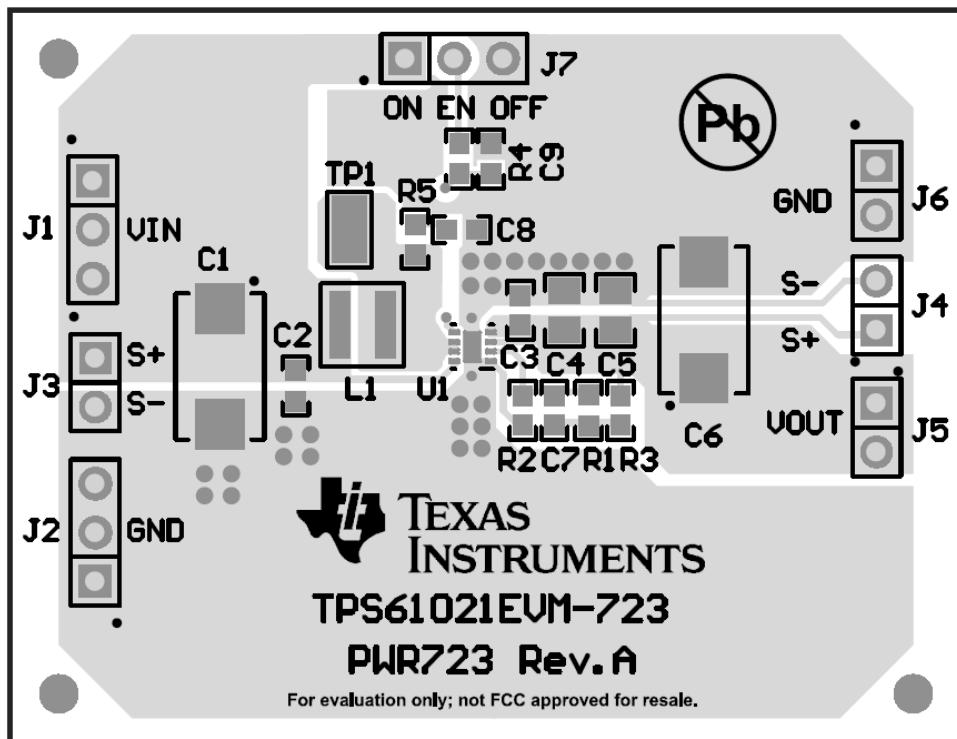


Figure 8. TPS61021EVM-723 Top-Side Layout

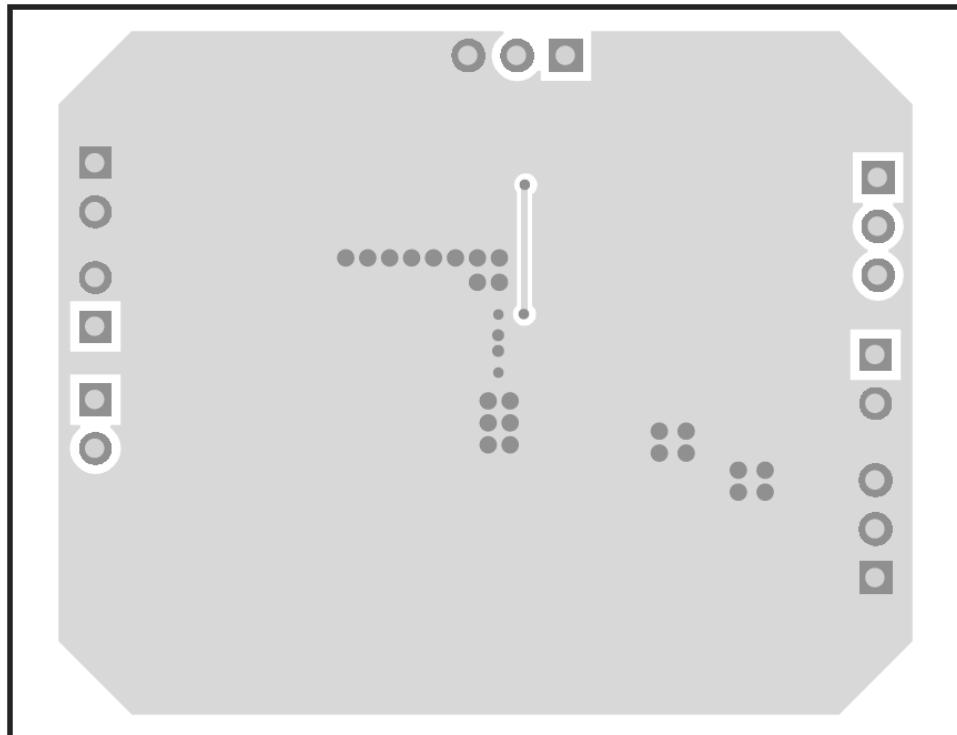


Figure 9. TPS61021EVM-723 Bottom-Side Layout

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2016) to A Revision	Page
• Changed device name to TPS61021A throughout document.	1

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 Canada

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