EVM User's Guide: ADC34RF72EVM ADC34RF75EVM ADC32RF77EVM

ADC3xRF7x Evaluation Module

Description

The ADC3xRF7xEVM is an evaluation module (EVM) designed to evaluate the ADC3xRF7x family of high-speed ADCs. The ADC3xRF7xEVM is populated with either the ADC34RF72 (1.5 GSPS quad channel ADC), the ADC34RF75 (3 GSPS quad Channel ADC) or ADC32RF77 (6 GSPS dual channel ADC) as denoted by board orderable. It is also easily identifiable by the "DUT Option" resistor on the EVM by the ADC device. The ADC3xRF7xEVM allows for evaluation of all device speed grades and number of channels.

Get Started

1. Order the correspoding EVM from ti.com for the device you would like to evaluate

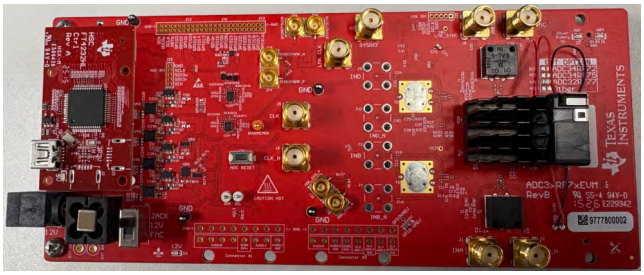
   (ADC34RF72 -> ADC34RF72EVM) (ADC34RF75->ADC34RF75EVM) (ADC32RF77->ADC32RF77EVM)
2. Download the latest revision of the data sheet (SBASAL0).
3. Download the latest software.
4. Download the comprehensive reference design files from the tools page of the EVM

Features

- Noise spectral density:
  - ADC34RF72EVM -164.2dBFS/Hz
  - ADC34RF75EVM -160dBFS/Hz
  - ADC32RF77EVM -161.8dBFS/Hz
- Full power input bandwidth:
  - ADC34RF72EVM 1.8GHz
  - ADC34RF75EVM 5GHz
  - ADC32RF77EVM 5GHz
- Power consumption:
  - ADC34RF72EVM 0.95W/channel
  - ADC34RF75EVM 1.6W/ Channel
  - ADC32RF77EVM 3.5W/ Channel
- Max sample rate:
  - ADC34RF72EVM 1.5GSPS
  - ADC34RF75EVM 3GSPS
  - ADC32RF77EVM 6GSPS
- Max JESD lane rate:
  - ADC34RF72EVM 24.75Gbps
  - ADC34RF75EVM 24.75Gbps
  - ADC32RF77EVM 24.75Gbps
- Eight digital down-converters, can be configured in single band, dual band and octal band configurations. Supporting real and complex decimation with factors starting at /2,/3,/5 up to 32768.
- 48-bit NCO phase coherent frequency hopping.
- Multiple integrated DSP features such as 96-tap/ch PFIR equalizer an fractional delay filter.

Applications

- Phase array radar
- Wafer inspection
- Spectrum analyzers
- Software defined radio (SDR)
- Electronic warfare
- High-speed digitizer
- Cable infrastructure
- Communications infrastructure



ADC3xRF7xEVM (ADC32RF77 EVM pictured)

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1 Evaluation Module Overview

1.1 Introduction

The ADC3xRF7xEVM allows for evaluation of the ADC3xRF7x family of high speed ADC. The EVM is configured to receive external single-ended analog inputs as the EVM utilizes on board baluns for single-ended to differential conversion. The ADC sampling clock is sourced externally and is single-ended, the EVM also utilizes an on board balun for single-ended to differntial conversion for the ADC's sample clock. For data capture, the ADC3xRF7xEVM is paired with the TSW14J58EVM. The TSW14J58EVM is an FPGA based data capture card which features a AMD Kintex Ultra Scale FPGA. The ADC data, captured by the FPGA, is then transferred to the PC and displayed in the High Speed Data Converter Pro capture software. This user's guide describes the characteristics, operation, and use of the ADC3xRF7x evaluation module (EVM).

1.2 Kit Contents

Table 1-1. Kit Contents

Item	Description	Quantity
ADC3xRF7xEVM	PCB	1
Mini - USB Type X Cable	Cable	1
Power Cable for 12V Jack	Cable	1

1.3 Specifications

The specifications for the ADC3xRF72 can be found in the corresponding device-specific data sheet

- *ADC34RF72 Quad Channel 16-bit 1.5 GSPS RF Sampling Data Converter Data Sheet*
- *ADC35RF75 Quad Channel 16-bit 3 GSPS RF Sampling Data Converter Data Sheet*
- *ADC32RF77 Quad Channel 14-bit 6 GSPS RF Sampling Data Converter Data Sheet*

1.4 Device Information

The ADC3xRF7x EVM is configured to receive external single-ended analog inputs as the EVM includes baluns for single-ended to differential conversion. The ADC sampling clock is also sourced externally and is single-ended.

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2 Hardware and Software Setup

This section describes the necessary hardware and software for evaluating the full performance of the ADC3xRF7x EVM.

2.1 Board Overview

Figure 2-1 highlights some key features of the board required for evaluation.

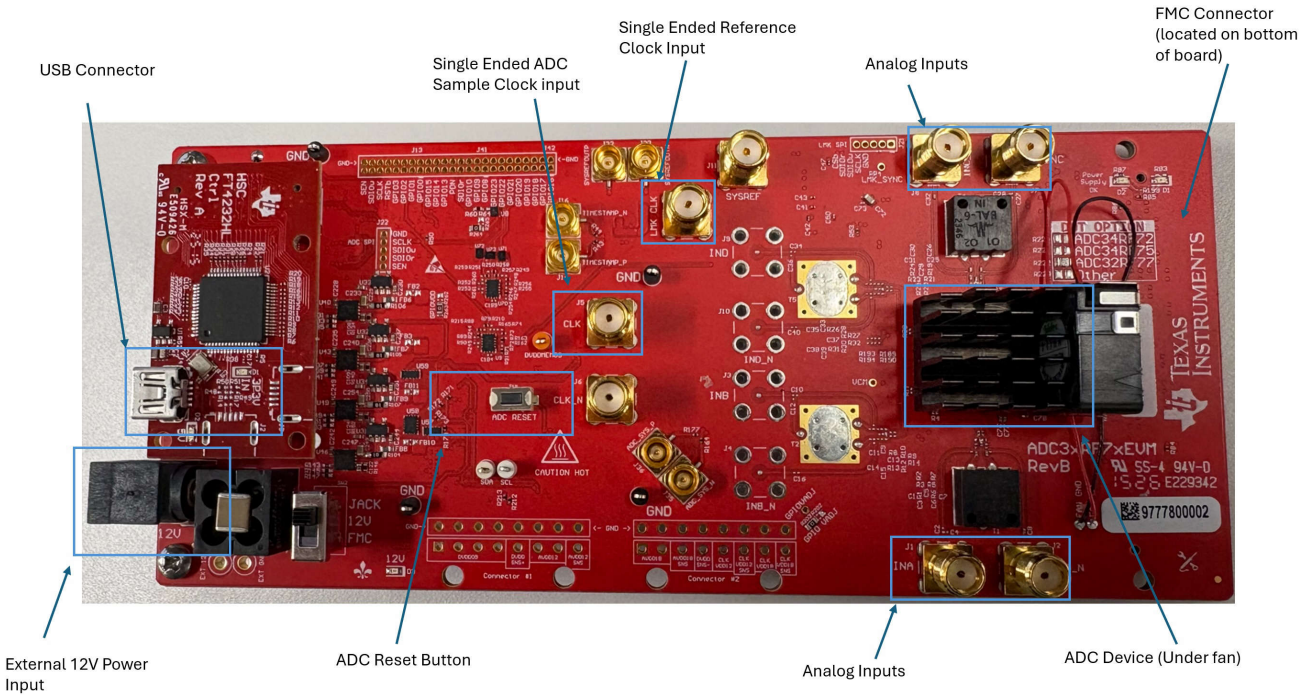


Figure 2-1. ADC3xRF72EVM Features

2.2 Required Equipment

In addition to the provided equipment detailed in Section 1.2, the following equipment is not included with the EVM kit, but is required for proper evaluation.

- TSW14J58EVM FPGA Capture card for capturing data from the ADC, and everything required for operation according to the TSW14J58EVM User's Guide TSW14J58EVM.
- High-Speed Data Converter Pro Software (HSDC Pro) High Speed Data Converter Pro
- FPGA Server - Included in GUI install path
- One 12 Volt power supply capable of supplying 5Amps for ADC EVM and 6V capable of supplying 6Amps for TSW14J58 FPGA Capture card.
- At least two low-noise signal generators to provide the ADC sampling clock and analog inputs to the ADC. TI recommends either of the following signal generators:
  - Rohde and Schwarz SMA100A
  - Rohde and Schwarz SMA100B
- A lower performance signal generator is also required as a reference clock to the ADC:
  - This clock does not affect ADC performance and is only be used for functionality.
- Bandpass filters for the sample clock and analog inputs. It is recommended to use filters with a narrow passband (within 5%-15% of the desired bandwidth), and minimal insertion loss.
- SMA cables to connect the inputs

By default, the EVM is configured for an external reference clock to be provided, there are optional board modifications that can be done to allow for only a single clock be supplied to the ADC EVM. These modifications are noted in Section 6.2.

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2.3 Required Software Installation

In this section, all of the necessary software installations for the ADC3xRF7x EVM are detailed. To operate the ADC correctly the following software must be installed.

2.4 Required TI Software to Install

- ADC3xRF7x EVM GUI

  This is used for programming the ADC and clocking chips properly into the desired mode of operation for evaluation of the ADC. This can be found on the Ti.com product page for the EVM. ADC3xRF7xEVM GUI download
- High Speed Data Converter Pro (HSDC Pro)

  This is used for live plotting and analysis of signals captured by the ADC to allow for simple and quick evaluation of the ADC. Minimum required version is 5.2, if user already has a version installed that meets the requirement this step can be skipped. High Speed Data Conveter Pro Download
- JESD Controller

  This is used for connecting and controlling the TSW14J58EVM capture card with the ADC EVM GUI Software. It is used to program the Capture card into the required mode of operation as well as handle all data collection from the high speed ADC. JESD Controller Download

2.5 3rd Party Software to Install

In addition to software provided by TI there are some additional software packages required to evaluate the ADC.

- FTDI D3xx Driver
  - Download
    - **WU_Driver_Installers.7z** - FTDI D3XX v1.4.1.0 — Windows Update Driver Installers (required version)
  - Extract the Archive

    The **.7z** format requires 7-Zip or a compatible tool:

    1. Right-click the file
    2. Select **7-Zip** → **Extract Here**

    Installation Steps

    1. Extract **WU_Driver_Installers.7z** to a folder of your choice.
    2. Inside the extracted folder, locate the installer for your Windows version:
       - For Windows 10/11 x64: run the **x64** installer
    3. Run the installer as Administrator and follow the prompts.
    4. Connect the TSW14J58 board's USB3-A cable to a **USB 3.0 port** on your PC (blue port or marked **SS**).
    5. Open **Device Manager** and verify the device appears as **TSW14J58** under Universal Serial Bus controllers.
    6. **Reboot after installation.**

    Important Notes

    - **USB 3.0 is required.** Plugging into a USB 2.0 port will cause device enumeration to fail.
    - If the device does not enumerate after driver install:
      - Try a different USB3 port or cable
      - Ensure the board is fully powered on before connecting
      - Plug USB3 directly into PC and not through any USB hubs as this may also cause issues
- FT_Prog FTDI Software:

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- This is an optional piece of software but is useful for checking USB handle name is correct and serial number is valid
- Can be installed from the FTDI website

2.6 Hardware Setup and Connections

This section describes all necessary hardware and connections.

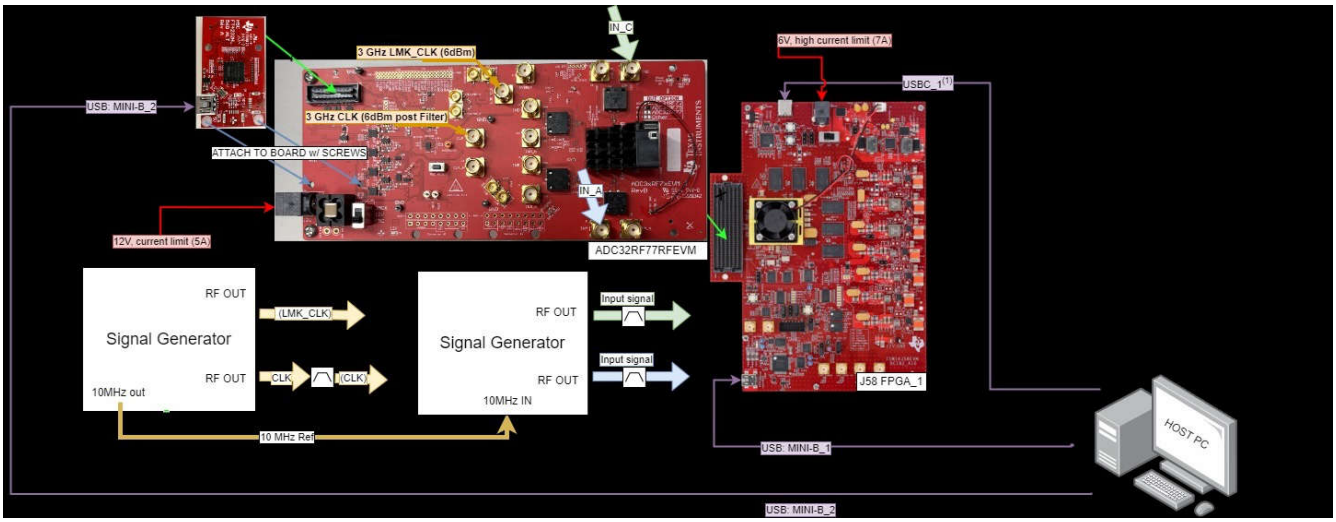


Figure 2-2. Hardware Connection Block Diagram

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2.7 ADC3xRF7x EVM Connections

This section describes all of the necessary connections on the ADC3xRF7x EVM in order. At this time, all power supplies and signal generators must be powered off.

1. Connect USB mini connector to FTDI Daughter Card.
   a. On connection LED D1 on daughter card lights up green, if not the daughter card can be broken and needs to be inspected.
2. Connect low-noise signal generator to SMA connector J5 (labeled CLK on EVM), this serves as the high-speed sampling clock to the ADC.
   a. Set Signal generator to desired sampling rate of ADC and output power to 6dBm.
   b. On connection, the signal generator must be in the off state.
3. Connect low-noise signal generator to SMA connector J12 (labeled LMK CLK on EVM), this serves as the reference clock source to the ADC EVM.
   a. Set Signal generator to match the sampling rate of the device and the output power to 6dBm.
   b. On connection the signal generator must be in the off state.
4. Connect low-noise signal generator to SMA connector J1 (labeled INA on EVM), this serves as the analog input signal to channel A of the ADC.
5. Connect 12V 5A to barrel connector J31.
6. Ensure power switch is set in the "Jack" position, indicating that power is sourced to the EVM from the external barrel connector and not the FMC connector.
7. Power on all signal generators to EVM.
8. Verify that all signal generators are also phase locked to each other.

For best performance TI recommends the use of Bandpass filter for the ADC clock input signals and ADC Analog input signals, this is to help limit the addition of external noise to the ADC.

There are a number of muxes on the EVM for advanced control and extended features. For more information, see section detailing possible hardware modifications for the EVM to change power on default, but full control is avaliable via EVM GUI and the EVM's I2C bus. By default the EVM will come configured to work with TI evaluation platform, any modification to these muxes may cause errors in evaluation of EVM.

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2.8 TSW14J58 Data Capture Card Connections

This section describes all the hardware connections for the TSW14J58 capture card.

1. Connect power supply at 6V 6A to barrel connector J2 (labeled PWRIN on capture card).
2. Verify that the power switch is in the “ON” position.
3. Connect USBC Cable for USB3 path. It's reccomended to directly connect this cable to your host device to prevent issues that occur when routing through a USB hub.
4. Connect Mini USB Cable for USB2 path.
5. Connect ADC EVM to FMC connector.

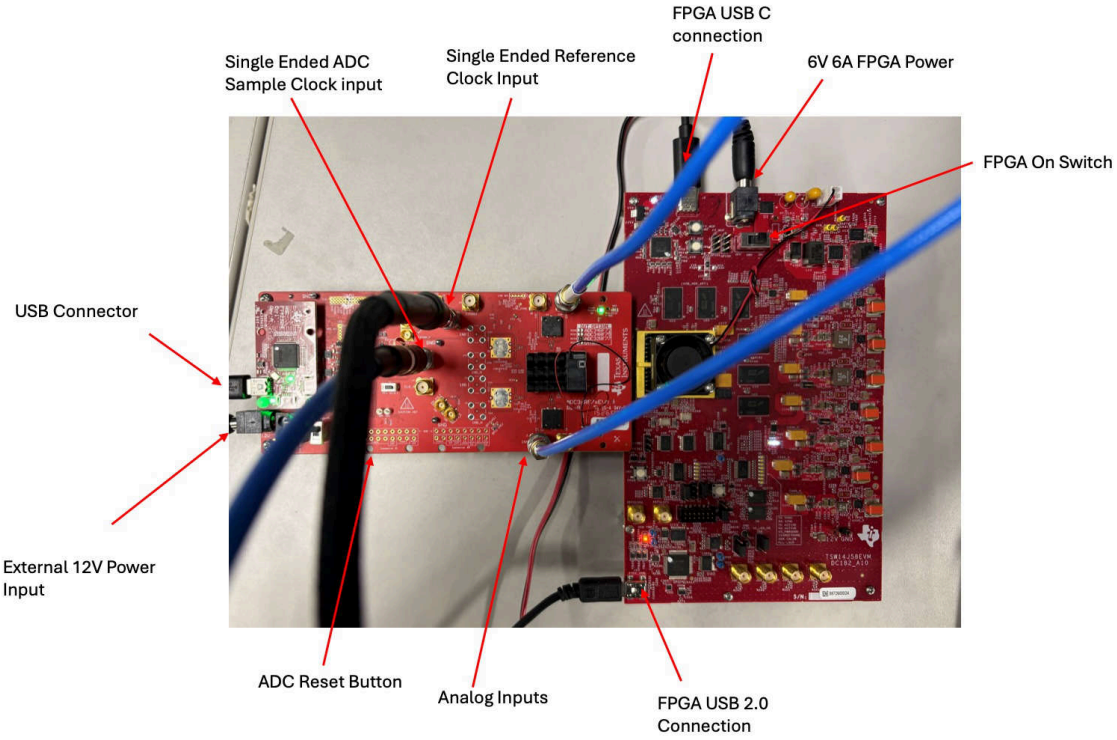


Figure 2-3. Example HW Setup

2.9 Debug LEDs

This section details all the debug LEDs on the EVM to verify that the hardware is functioning properly.

Table 2-1. Debug LEDs

LED Number	Description
D2	All power rails on EVM good
D3	12V power on EVM

3 ADC3xRF7x EVM Configuration and Programming

This section details the bringup and programming of the ADC3xRF7x EVM into the desired mode of operation.

3.1 ADC EVM Quick Start

The first test with the ADC EVM serves as an initial “quick start” to verify there are no hardware issues and everything is functioning as expected. This section walks through step by step the setup, programming and finally capturing and analysis of signals. This section assumes steps in Section 2 have been followed and all necessary hardware connections are made but power supplies and signal generators are turned off.

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3.2 Power On All Boards and Signal Generators

1. Turn on 12V at 5A power supply for ADC3xRF7x EVM. To verify that all of the power rails of the ADC EVM have successfully powered up, LED D2 can be checked. If this is lit up, then all power supplies have successfully powered on.
2. Power on 6V at 6A Power supply for TSW14J58 capture card and verify that the power switch is in the “ON” position.
3. Set the ADC clock signal generator to either 1.5GHz for ADC34RF72 or 3GHz for ADC34RF75 and ADC32RF77 at 6dBm power. Turn this signal generator on.
4. Set the LMK clock signal generator to match frequency and power of the ADC clock signal generator. Turn this signal generator on.
5. Set the ADC input signal generator to desired frequency (for the example an input of 125MHz is used) with power set to 0dBm.

3.3 Launch J58 FPGA Server

Before beginning to program the ADC EVM, you must first launch the JESD Controller applciation to allow for programming and data capture. This can be done by launching the JESD Controller application mentioned in section TI Software to install. Once this is done click the J58/GSOM Server button to launch the FPGA Server to communicate with TSW14J58 Capture Card. Once this is done you will see a second window popup that will indicate if the TSW14J58 was succesffuly connected to. If you do not get this result please look at section Troubleshooting and FAQ.

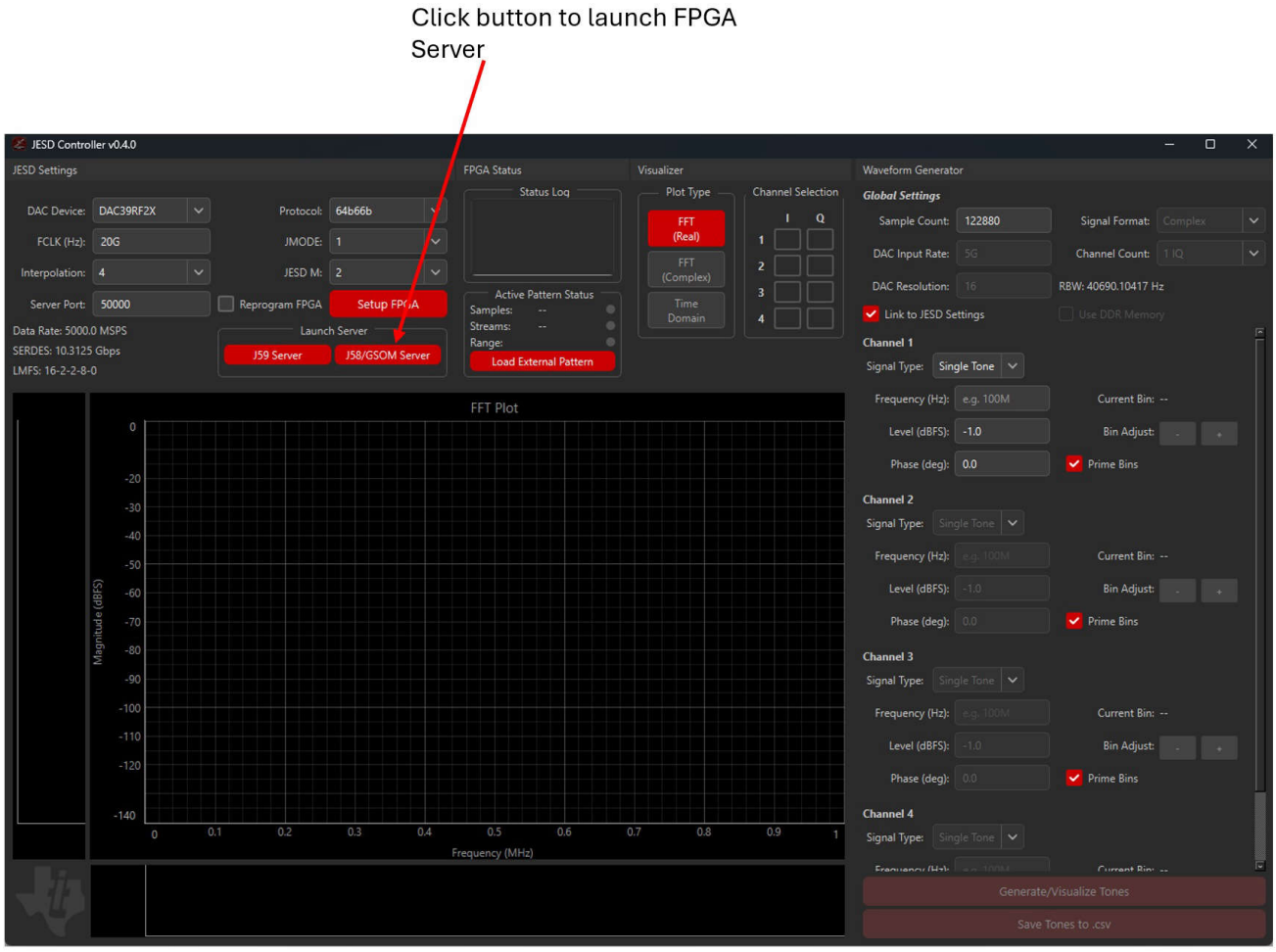


Figure 3-1. JESD Controller

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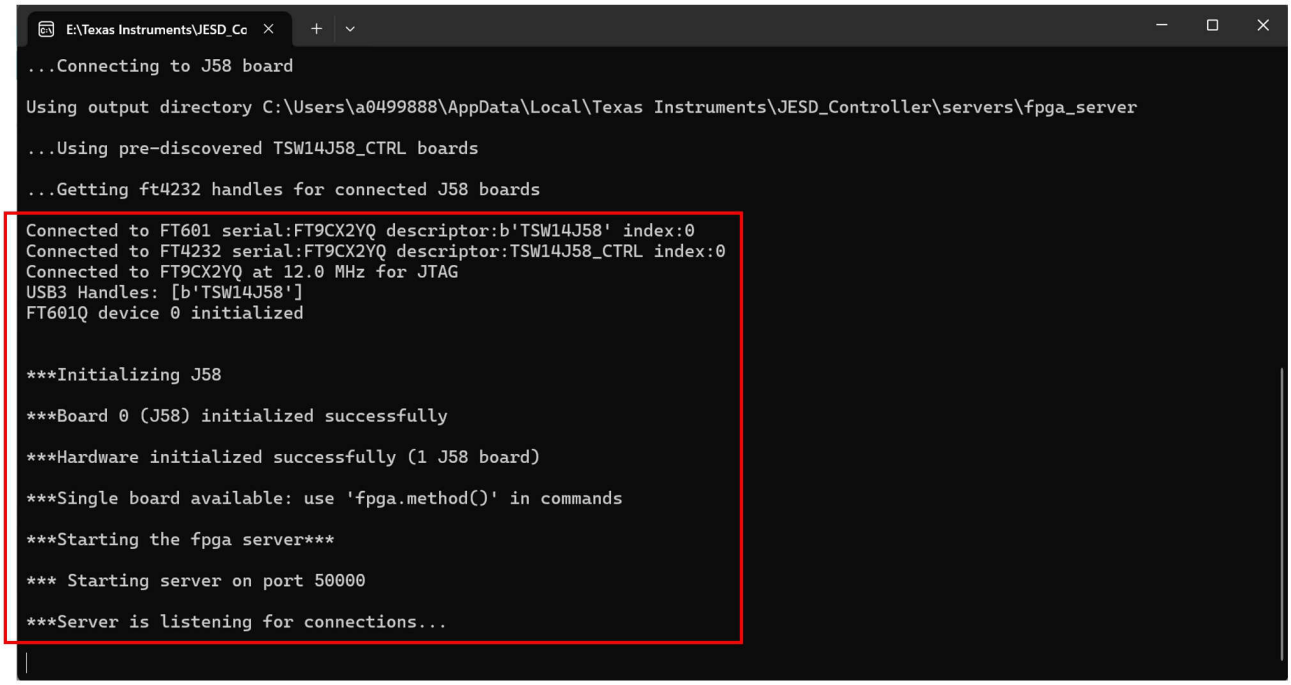


Figure 3-2. Successful FPGA Server Launch

Once the server is launched, it does not have to be interacted with directly. All necessary communication happens via the ADC GUI.

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3.4 Launch High-Speed Data Converter Professional (HSDC Pro) SW

For signal plotting and analysis High speed Data convert pro is used. To launch, locate the application and click "OK". The blank plotting screen shows, as shown in Figure 3-3. Similar to the server, this can be left on in the background and the ADC GUI can handle all of the necessary communication.

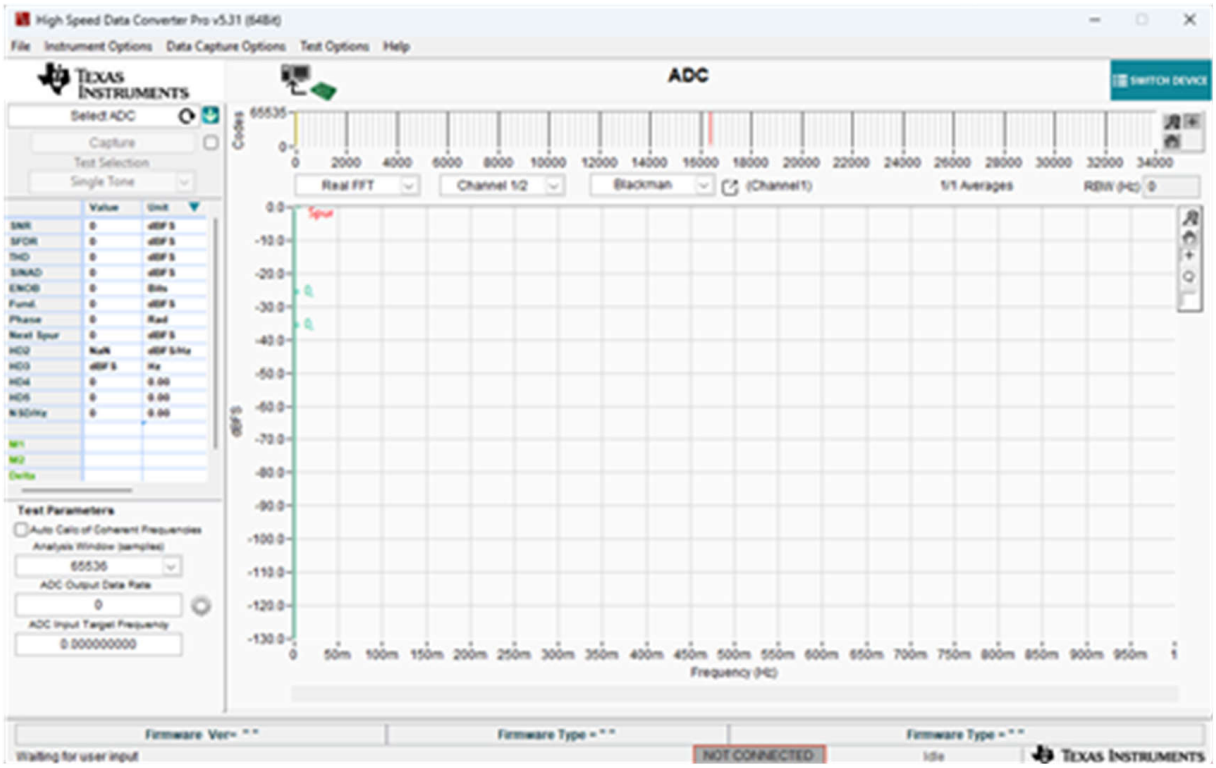


Figure 3-3. HSDC Pro

3.5 First Time Programming the ADC EVM

For programming, the ADC3xRF7x comes with a GUI that allows the user to configure the EVM into their desired mode of operation. The GUI can be found at the product page for the EVM on . Launch the GUI.

If the ADC EVM successfully connects to the GUI, it looks like Figure 3-4. The GUI comes preset to a default configuration of Sampling frequency = max sample rate supported by that device and all internal digital signal processing bypassed. If the hardware is configured as mentioned in Section 6, then the user can simply click "program ADC" and the GUI programs the ADC, the FPGA and tries to initialize the FPGA link so that data can start to be captured. Progress can be monitored in the below message console. If the ADC successfully programs the message, “ADC programming Success!” prints out in the console. Now the GUI starts to program the FPGA, debug messages can be seen in the message console as well but progress can also be monitored in the FPGA tab of the GUI. If the FPGA is successfully programmed and the link is successfully initialized then the following status shows in the FPGA tab. If not, then refer to Section 5 for further support.

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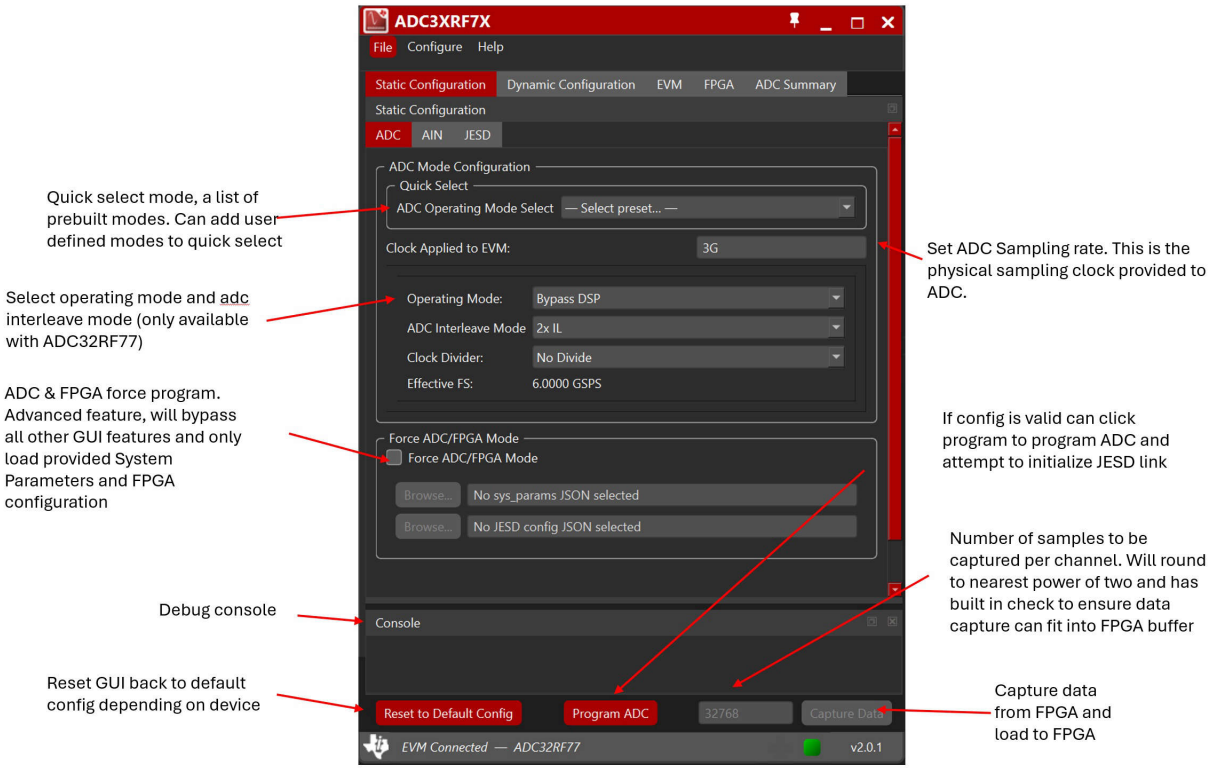


Figure 3-4. EVM GUI Program ADC

FPGA Status & Control Tab

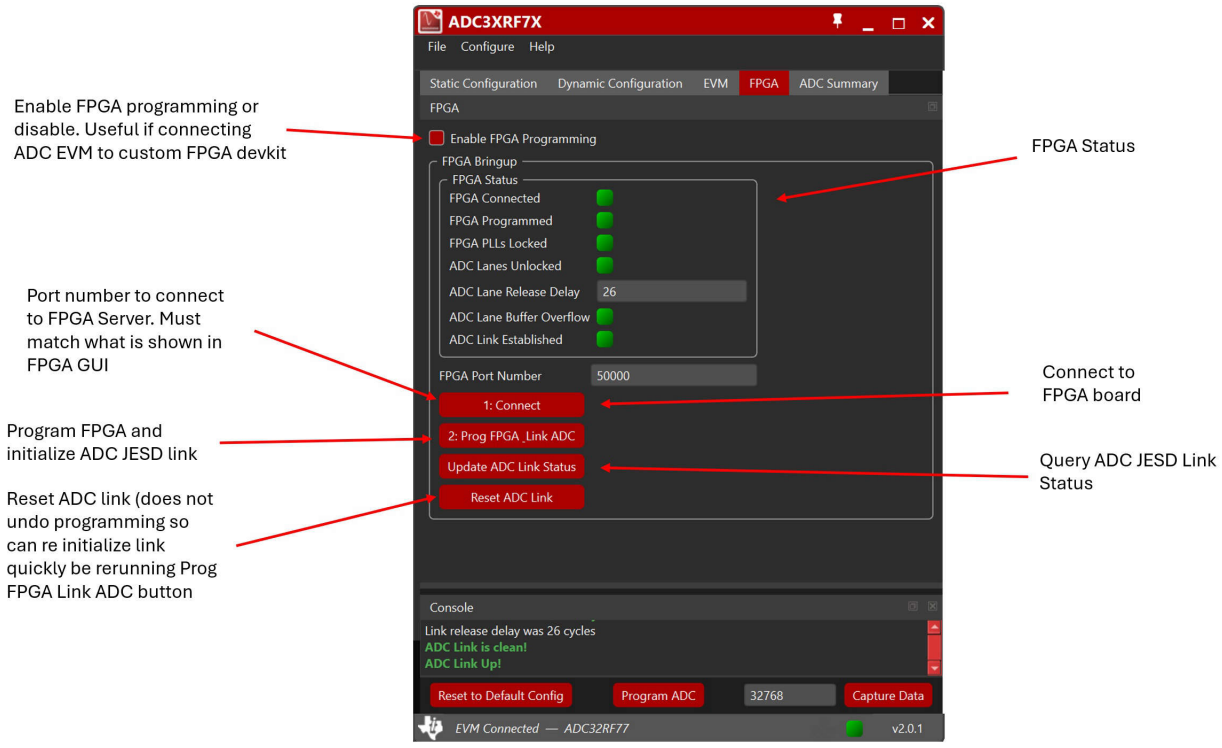


Figure 3-5. ADC GUI FPGA

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If the status matches what is shown in the figure, then the data can be captured and plotted in HSDC Pro. To do this press the “Capture Data” button in the ADC GUI. The resulting data can be seen in HSDC Pro as shown in Figure 3-6.

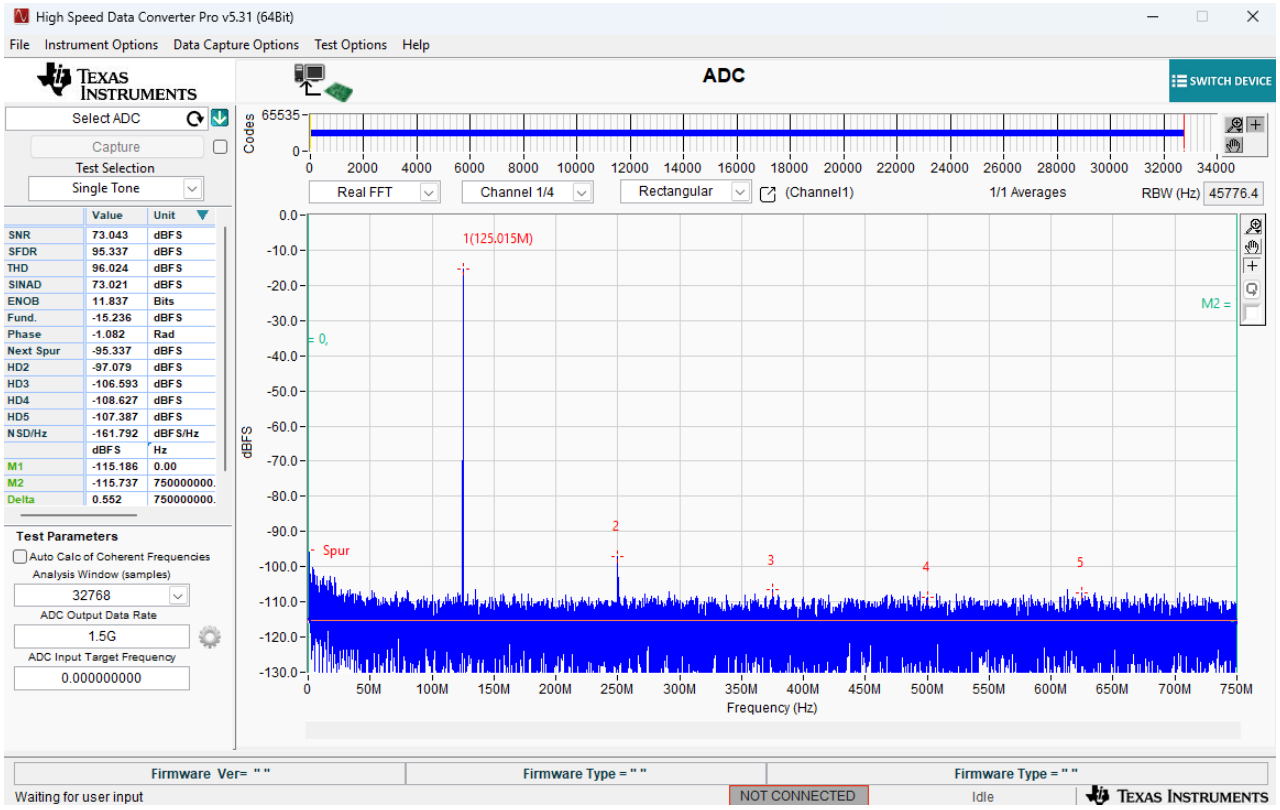


Figure 3-6. Example FFT Output Spectrum for ADC34RF72EVM

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4 ADC Configuration Using GUI

The ADC programming sequence is split into two modes Static Configuration and Dynamic configuration. Where the static configuration sets the device mode of operation e.g. Number of Digital Down converters active, JESD interface configuration etc. Whereas dynamic configruation happens after the device is configured e.g. NCO tuning loading equalizer coefficients and configuring GPIOs etc. This section will cover these two sections as well as other GUI tips and tricks.

On launching the GUI it will search for any connected FTDI devices that match the supported string descriptiors. "ADC34RF72EVM_RevA", "ADC32RF77EVM_RevA", "ADC34RF75EVM_RevA", "ADC34RF72EVM_RevC", "ADC32RF77EVM_RevC", "ADC34RF75EVM_RevC" If your EVM does not match one of these the GUI will not be able to detect the board and hence will not connect. The USB string descriptor can be reprogrammed using FT_Prog.

Once a valid EVM is found the GUI gives the option to connect to hardware or startup in demo mode which does not require hardware to be connected. If demo mode is selected the user will be prompted to enter which device they are looking to simulate. If the user selects connect to hardware the GUI will try and query the EVM to see if its programmed, if it is the GUI will initalize into that mode of operation and the JESD link try to initalize. If the ADC was not previously programmed it will launch into default mode of operation and will not attempt to initalize the JESD link. This feature can be disabled by one of the global GUI parameters discussed in Global GUI Parameters.

4.1 ADC Static Configuration

The GUI initalizes to a default configuration according to the device part detected/selected, see table below for details. On top of this default a number of features can be configured, the sample rate, DSP, Analog inputs and JESD interface can all be included. See future sections for more details.

Device EVM	Sampling Rate	Mode Description
ADC34RF72EVM	1.5 GSPS	Quad Channel all DSP bypassed Max Sample Rate
ADC34RF75EVM	3 GSPS	Quad Channel all DSP bypassed Max Sample Rate
ADC32RF77EVM	6 GSPS	Dual channel 2x Interleaved, all DSP bypassed.

Force ADC/FPGA Mode

This mode assumes the user already has a valid ADC System parameters JSON and JESD configuration JSON, both can be exported from GUI, see Exporting ADC3xRF7x Configuration. See ADC Datasheet and progamming reference for System parameters reference. The strucutre for the JESD Configuration can be seen below, this data is stored in json files.

```
Class jesd_cfg():
     links : int=None
     lanes : int=None
     channels : int=None
     frame_octets : int=None
     samples_per_frame : int=None
     high_density : bool=None
     scrambling : bool=None
     frames_per_multiframe : int=None
     e : int=None
     channel_resolution : int=None
     jesd_sample_resolution : int=None
     format_twos_complement : bool=None
     lane_map : list=None
     lane_polarity : list=None
     encoding : str=None
     int1 : int=1
     int2 : int=1
     decimation_factor : int=None
```


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```
    complex_signal : bool=None
    channel_repeat_factors : list=None
```

Selecting this mode of configuration disables and bypasses all other methods of config in the GUI for both static and dynaminc configurations.

4.2 GUI Analog Input Control

This tab lets the user configure the number of active channels used by the ADC with the constraint that channel A must always be active and only power of two number of channels are valid. The input termination for each ADC channel is also programmable here with valid values differing depending on device in use. The nyquist zone of operation is also selectable here there are two default opions picked here, if operation in a higher nyquit is desired a custom mode is avlaible in the run time option see NLC tab. This will affect device non-linearity performance.

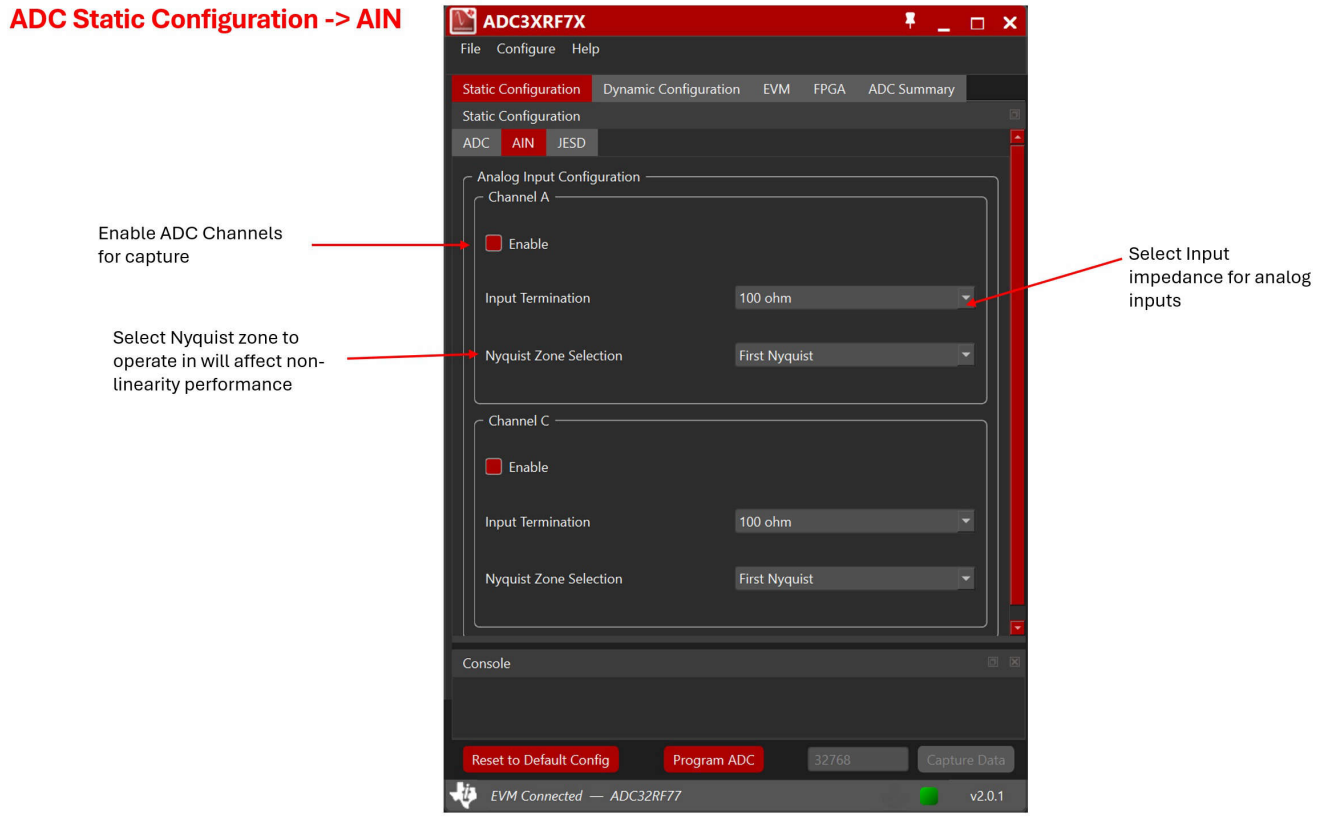


Figure 4-1. Static Configuration -> AIN

4.3 GUI Fractional Delay Filter Configuration

This tab lets the user program the fractional delay filter for each ADC channel. Entry is a 12 bit number the represents the code loaded to the ADC. The effective delay is calculated based on clock rate and fdf code entered. See datasheet for more details on the fractional delay filter.

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ADC Static Configuration -> FDF

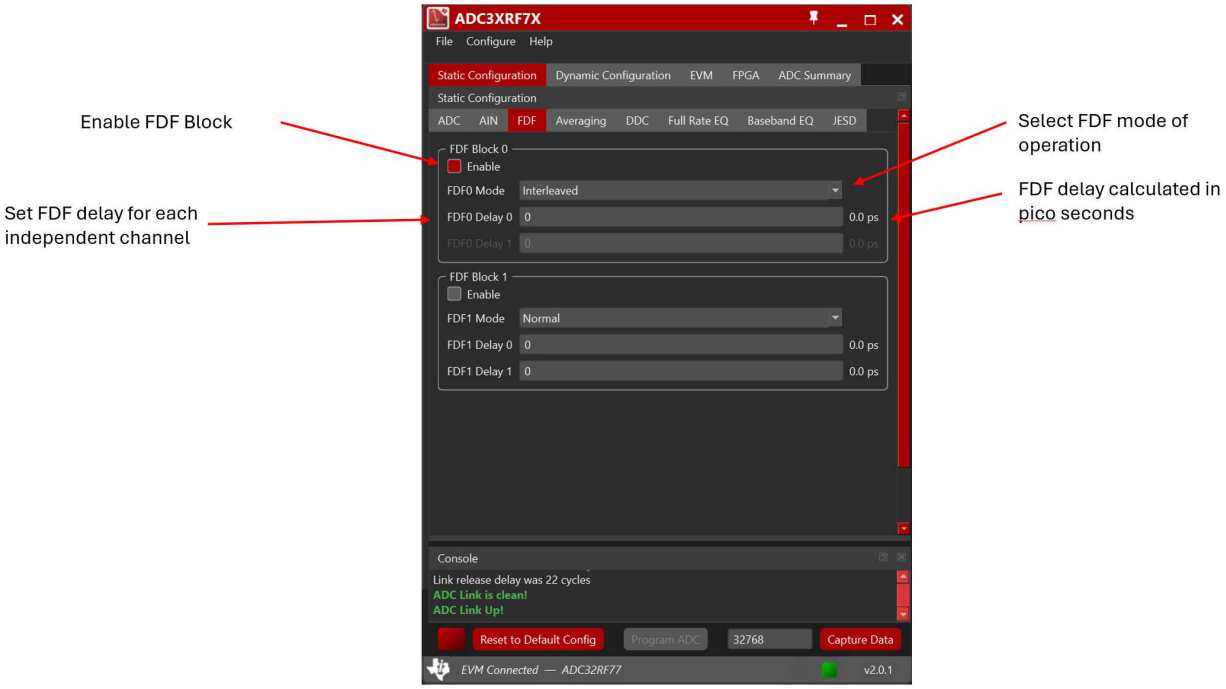


Figure 4-2. ADC Fractional Delay Filter

4.4 GUI Digital Down Converter Tab

This tab lets the user configure the ADC's Digital Down Converters for operation. It lets the user set DDC parameters globally (same is copied to each DDC index) and analog inputs are split equally across all DDCs. Or Per DDC in which case the user can set Input source, decimation factor and NCO frequencies per DDC. This lets the user configure single, dual quad or octal band modes as well as configure different DDCs to different decimation factors. See ADC datasheet for more details on Digital Down Converter Configuration.

When the ADC linerate drops below the minimum value of 4 Gbps the ADC starts to repeat data to artifically increase the SERDES rate. This data repetition is automatically handled by the GUI when plotting samples in HSDC pro but it will limit the max number of samples avalaible for capture.

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ADC Static Configuration -> DDC (Global Mode)

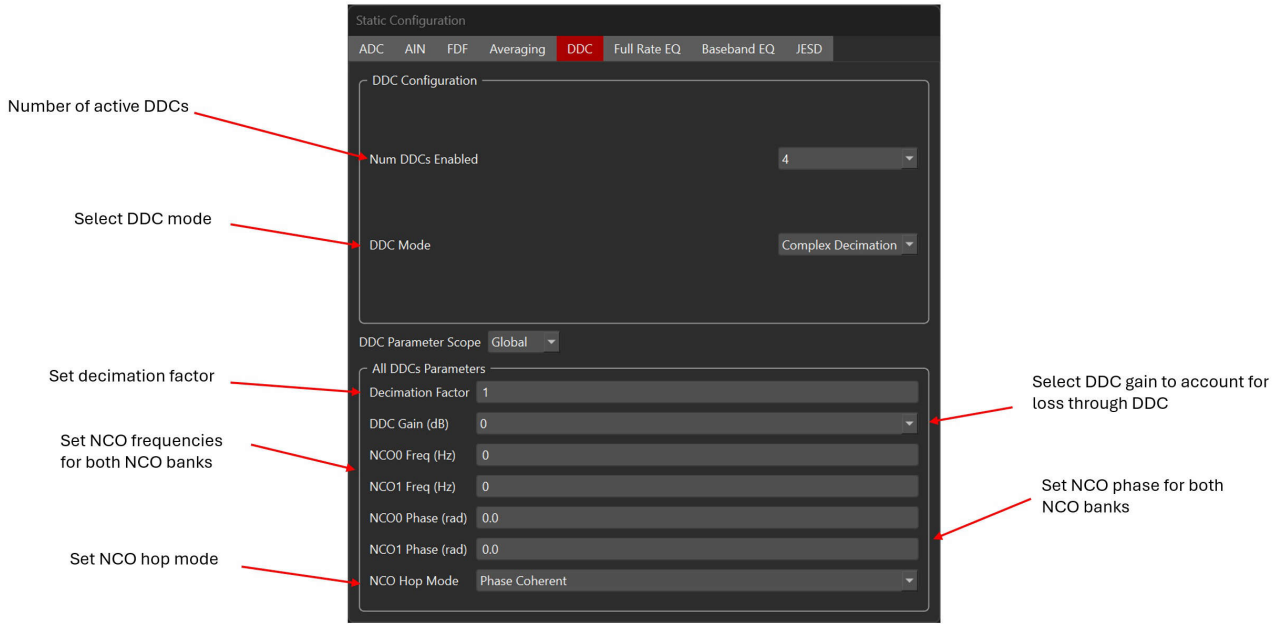


Figure 4-3. ADC DDC tab

4.5 GUI Full Rate and Baseband Equalizer Tab

This tab lets the user configure the full rate equalizer and baseband equalizer. This section serves both settings as the configuration is very similar for each, with the exception that the baseband equalizer is only avaliable if the DDC's are used. For the full rate equalizer the input source is selectable whereas the baseband equalizer is tied to a ddc output and maps one to one. For more details about supported equalizer modes see adc datasheet. Enabling DDCs in the static configuration tab will enable the corresponding equalizer tab in the runtime tab which will allow coefficinets to be programmed to the ADC.

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ADC Static Configuration -> Full rate equalizer

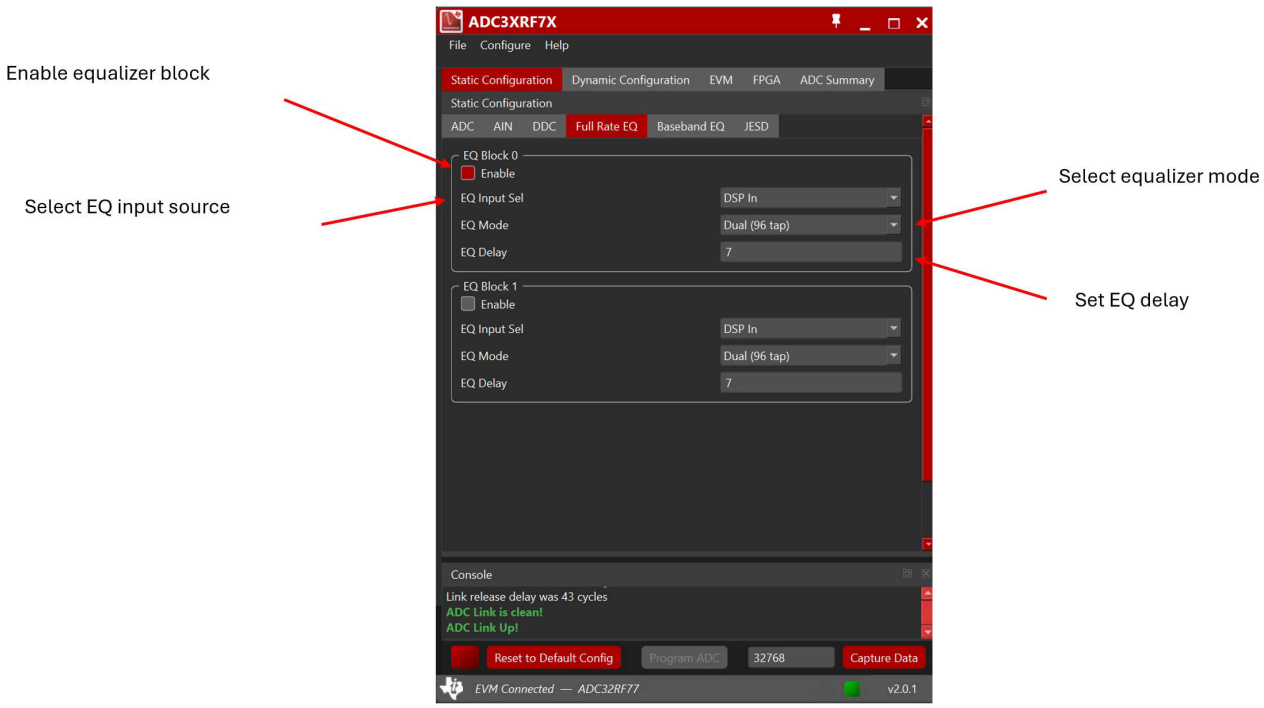


Figure 4-4. ADC Full rate EQ tab

4.6 GUI JESD Tab and Asynchonous FIFO Calibration Control

This tab details the JESD interface of the ADC and displays the calcualted lane rate and required FPGA Clocks and SYSREF frequencies. This tab inherits most of its parameters from the other tabs in the GUI and hence parameters such as M,F and S are not directly programmable they are infered from how the user has configured the ADC. This is to avoid any mismatch between the desired ADC use and how the JESD interface needs to be configured to acheive this. The only parameter that is directly programmed for LMFS is the number of lanes provided the resulting lane rate is still within valid range. For instance if a device mode results in a lane rate of 12.375 Gbps with 4 lanes active going to both 2 lanes (24.75 Gbps) and 8 lanes (6.1875 Gbps) are valid configurations and this is supported by the GUI. The other selections the user can update are the Encoding to switch between 8b10b and 64b66b encodings as well as K and E parameters. Again the resulting lane rate must fall within valid range for the encoding format. See datasheet for more details.

This tab also lets the user control wheter the GUI runs the ADC's Asynchouns FIFO calibration each time it is programmed or it loads from a user provided set of afifo cal values. For more details on this see datasheet.

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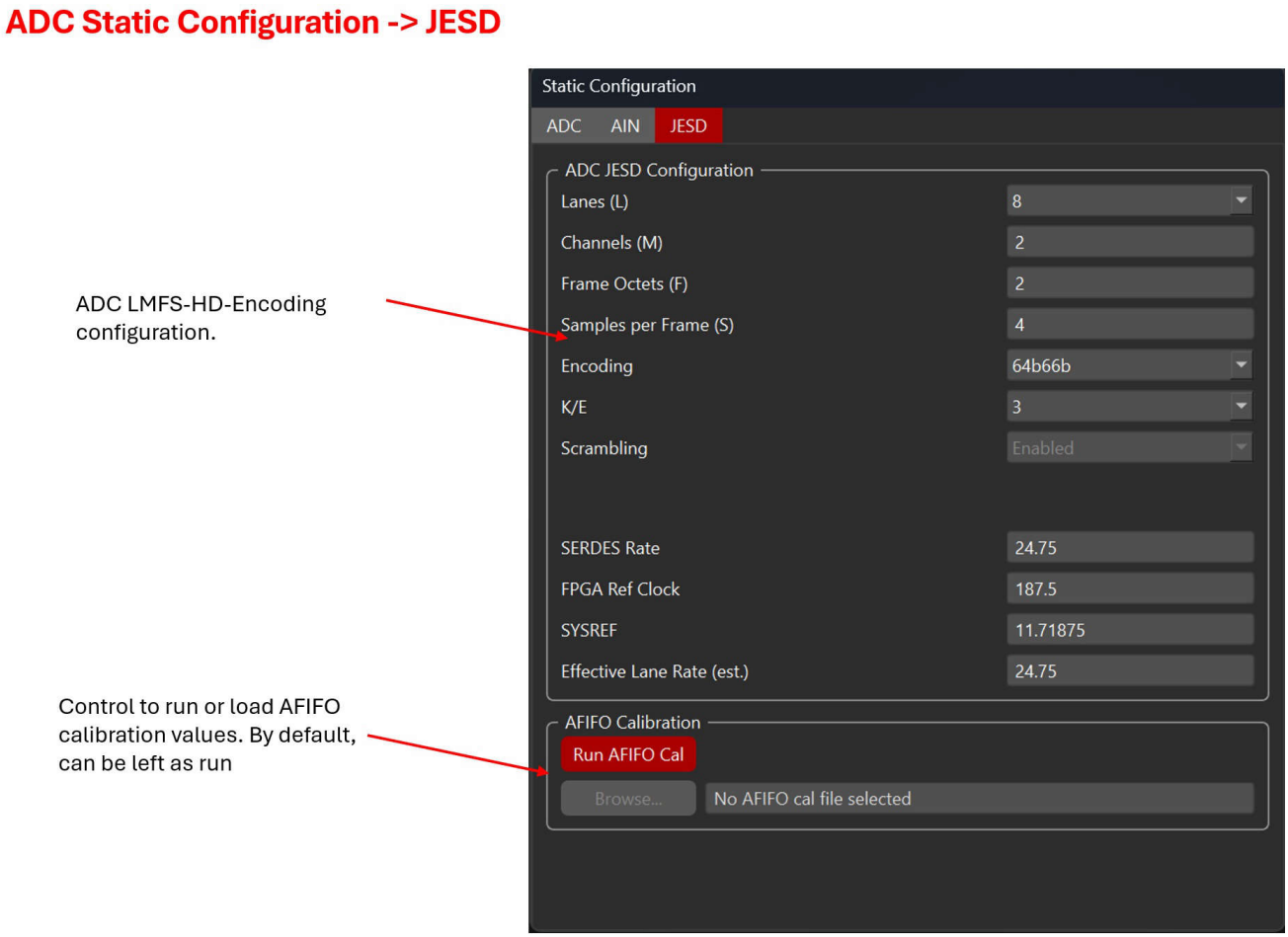


Figure 4-5. JESD Tab

4.7 Runtime Configuration

The GUI also supports a number of runtime configurations and monitoring. These are aplit into ADC specific runtime features and EVM specific features. These include editing NCO values, real time power monitoring of ADC power rails, SYSREF features a full list can be seen below.

ADC Specific runtime features...

- NCO – In this tab, the NCO frequency and phase can be edited and adjusted real time at a per DDC level. This is only enabled and shown if the DDCs are used.
- SYSREF - In this tab the ADC SYSREF can be re armed to allow for re-synchronization.
- JESD Test Pattern - In this tab a JESD ramp can be used for JESD link debug. Please note that after enabling this ramp you must go execute the sysref sequence on the sysref page. It is also possible to perform a PRBS test for the ADC to measure BER and debug link issues.
- Full rate EQ and Baseband EQ - Option to either generate Filter tap coefficinets for low pass, high pass and bandpass filters or load in pre calculated coefficinets with different formats. Note full rate equalizer mode is not directly configurable in this tab as it is done as part of the static configuration.
- GPIO - Option to allocate, deallocate and force GPIO state for all ADC GPIOs.
- NLC- Option to load custom Non-Linear correction coefficients to the ADC to improve ADC non-linearity performance in different nyquist zones or with different analog front ends.
- Status - Readback various status from the ADC for live debug of any issues.
- Misc - Readback hardware and software version of the ADC.EVM Runtime features
- ADC Power - Readback all ADC power rail voltages and currents to calculate the ADC's power consumption. There is also the option to margin all of the ADC power rails to their nominal values.

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- Board Temp - Readback board temp from temp sensors located near the ADC, near the power supply and from the internal ADC temp sensor itself.
- Board Mux control - Options to change the default state of all on board muxes. Should not be changed for regular GUI operation.
- Clocking - Adjust LMK04828 dividers to get specific reference clock and sysref frequencies. Should not be changed for regular GUI operation.

4.8 Exporting ADC3xRF7x Configuration

To transfer the ADC's desired configuration from the GUI to a users application there is a feature that allows for exporting a configuration file for the ADC's desired mode of operation. To export the configuration, navigate to the "ADC Summary tab" of the GUI. Once here there is a button labeled "Export ADC System Parameters as JSON" click this button and select a valid location to save this file. Once this is done you can access the Python API files which are avaliable for download from the EVM and device product page under the software development tab. Using these files, you are able to replicate the exact programming sequence performed by the GUI. For additional help with the API ,see the documentation included in the API release folder. There is also the ability to export the exact JESD configuration used by the fpga for reference as well as loading into the GUI in its "force" mode of programming. The system parameters are also avaliable for export in C header form for use in embedded systems with the provided C software library also avalaible for download from the from the EVM and device product page.

Also shown on this page is a live view of the ADC system parameters currently shown. This will update to reflect how the GUI is being setup to program the ADC.

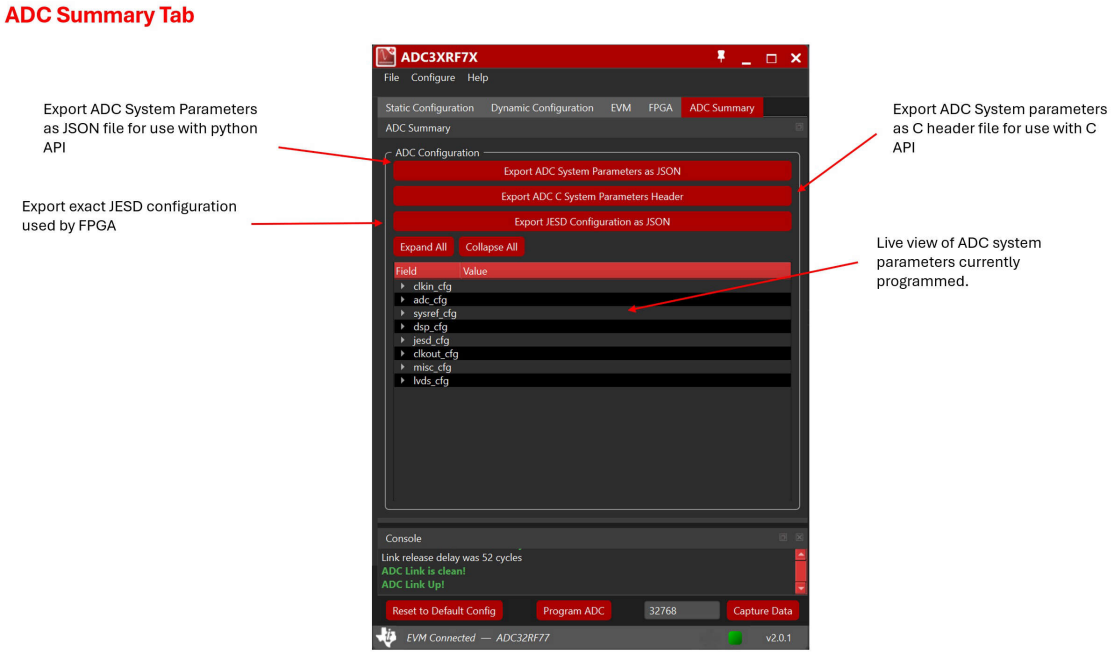


Figure 4-6. ADC Summary tab

4.9 Global GUI Parameters

This section details all the global paramters the GUI loads with when it opens, they control things such as data save path defaults and logging controls. It can be accessed by selecting Configure->Gui Configure. Doing so will result in the following popup to appear. Editing any of these varaibles will only take affect in the GUI after a relaunch. So for instance if chaning the device log level to record SPI writes user must first edit the Device log level dropdown and then re launch the GUI to actually start recording SPI writes. These values are also accessible via the gui_config.ini file in the preferences folder.

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Table 4-1. Global GUI Parameters

Parameter	Description
Reconnect to Programmed ADC on Launch	GUI will try and query ADC on launch to see if it was previously configured, if so the GUI will open to reflect that mode. Toggle this button to enable disable this feature
Device Log Level	The GUI logs all ADC functions and this dropdown sets the log depth (API functions logged, Warning, Errors and SPI trace)
Default Log File Directory	Set the default directory for log files to be stored to
Default Sys Params JSON Export Directory	Set the default directory for ADC System parameters JSON to be stored to
Default Sys Params C Header Export Directory	Set the default directory for ADC System parameters C header to be stored to
Default Capture Data Directory	Set default directory for FPGA to save ADC data to.

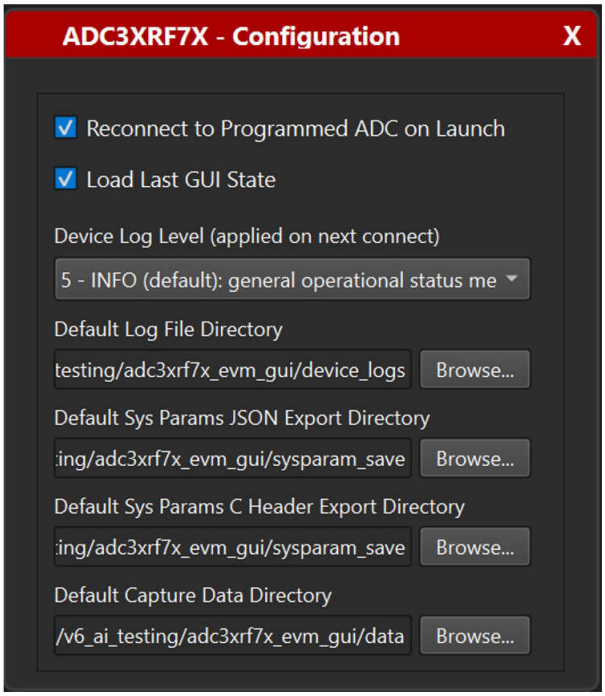


Figure 4-7. ADC3xRF7x GUI Global Configurations

5 Troubleshooting and FAQ

Table 5-1. Troubleshooting and FAQ

Issue	Troubleshooting Step
General Issues	• Verify test setup shown in Section 2 and repeat “ADC EVM quick start” section to verify basic functionality. • Check power supply to ADC EVM and TI Capture Card. If Power good LEDs on ADC EVM are not lit up then there is likely a power supply issue. • Check signal and clock connections • Make sure that the FMC connector is tightly secured

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Table 5-1. Troubleshooting and FAQ (continued)

Issue	Troubleshooting Step
TI Capture Card cannot connect in JESD Controller Server Application	• Make sure that all steps to setup 3**rd** party software are followed in Section 2.5. • Make sure that the USBC path is directly plugged into the PC and does not go through and USB hubs. • Using FT Prog check for USB 2.0 connection shows a usb connection with usb descriptor "TSW14J58_CTRL" • Check device manager to ensure that the USB 3.0 path shows up as "TSW14J58" under the Universal Serial Bus device. • Additonaly ensure in device manager that the driver for the TSW14J58 is version 1.4.0.1 • If connection of board in JESD controller server is still unsuccessfu, uninstall and reinstall the application
ADC EVM cannot connect in GUI	• Verify that the USB cable and daughter card are making solid connection. • Using FT_Prog verify that the ADC FTDI handle is found and matches one of the valid options "ADC34RF72EVM_RevA", "ADC32RF77EVM_RevA", "ADC34RF75EVM_RevA", "ADC34RF72EVM_RevC", "ADC32RF77EVM_RevC", "ADC34RF75EVM_RevC"
ADC EVM fails programming	• Make sure that device clock to ADC has enough power to the EVM (9dBm) and the frequency matches what is programmed in the GUI. • Check that the resetb signal is not held low. Using the multimeter probe RSTb signal located on the GPIO header. This signal reads approximately 1.8V indicating the ADC is not being held in reset. If this is not the case the EVM can be damaged or broken.
ADC Link fails to come up	• In FPGA tab of the ADC EVM GUI there are a number of LEDs to indicate the FPGAs status. Refer to this and the corresponding table entries below.
FPGA Connect LED not lit up	See above table Entry "TI Capture Card cannot connect in GSPS FPGA Server Application"
FPGA Programmed LED not lit up	• Verify that power supply meets the criteria of 6V, 6A. Programming the FPGA is one of the highest current draws on the FPGA. Check that during this time the power supply is not hitting its current compliance.
FPGA PLLs Unlocked	• Verify that EVM hardware is setup as shown in Section 2.6 and reference clock to the EVM is at least 6dBm and the frequency matches what is selected in the GUI for the ADC sample frequency. • Verify that ADC Clock and reference clock are phase locked to each other with 10MHz signal. • Using Oscilloscope probe on resistor R62 and make sure that frequency matches what is shown in the ADC EVM GUI in the Bringup>JESD tab in the “FPGA Ref Clock” box.
ADC Lanes Unlocked	• Verify that programmed JESD params in the GSPS FPGA Server match what is shown in the ADC EVM GUI in the Bringup>JESD tab. • Probe resistor R204 and make sure that ADC SYSREF signal is present and matches the frequency shown in the Bringup>JESD tab in the “SYSREF” box.
ADC Lanes Lock but release delay is stuck at zero	• Probe resistor R204 and make sure that ADC SYSREF signal is present and matches the frequency shown in the Bringup>JESD tab in the “SYSREF” box.
ADC Lane Buffer Overflow	• Probe resistor R204 and make sure that ADC SYSREF signal is present and matches the frequency shown in the Bringup>JESD tab in the “SYSREF” box. • Verify that ADC Clock and reference clock are phase locked to each other.
Sub Optimal Performance	• Verify signal quality of both clock and ADC inputs as these directly limit the ADCs performance. • Make sure that the bandpass filters are used for both ADC clock and any inputs.

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6 Important Signal Routing

This section details all important signal routing on the EVM.

Table 6-1. JESD FMC Data Routing

ADC JESD Output (p,n)	FMC Pin Number (p,n)	Physical Routing P/N Inversion	Schematic Net Name (p,n)
STXOUT0	(A18,A19)	Y	DOUT0_FMC
STXOUT1	(B16,B17)	Y	DOUT1_FMC
STXOUT2	(A14,A15)	Y	DOUT2_FMC
STXOUT3	(B12,B13)	Y	DOUT3_FMC
STXOUT4	(A2,A3)	Y	DOUT4_FMC
STXOUT5	(C6,C7)	Y	DOUT5_FMC
STXOUT6	(A6,A7)	Y	DOUT6_FMC
STXOUT7	(A10,A11)	Y	DOUT_7_FMC

Table 6-2. Additional JESD FMC Signal Routing

Signal Description	FMC Pin Number	Schematic Net Name
Transceiver Reference Clock 0 (P,N)	D4,D5	MGTREFCLK0_FMC_P/N
Transceiver Reference Clock 1 (P,N)	D4,D5	MGTREFCLK1_FMC_P/N
JESD Application Layer Clock	G6,G7	LMK_CORECLK_P/N
SYSREF	G9,G10	FPGA_SYSREF_P/N
Hardware Sync	H31	GPIO_MUX_0_FPGA

Table 6-3. Other FMC Signals

Signal Description	FMC Pin Number	Schematic Net Name
Carrier card IO voltage level adjust	E39,F40,G39,H40	VADJ
SCLK from carrier card at carrier voltage IO level	G12	SCLK_FMC_VADJ
SDI write from carrier card at carrier voltage IO level. Is SDI line for both ADC3xRF7x and LMK04828	G13	SDI_FMC_VADJ
SDO read from carrier card at carrier voltage IO level. Is SDO line for both ADC3xRF7x and LMK04828	G15	SDO_FMC_VADJ
SPI chip select for LMK04828	G16	CSb_LMK_FMC_VADJ
SPI chip select for ADC3xRF7x SPI from carrier card at carrier voltage IO level	C18	SEN_ADC_FMC_VADJ
Active low ADC3xRF7x hardware reset	H13	RSTb_ADC_FMC_VADJ
ADC3xRF7x power down	H14	PDN_ADC_FMC_VADJ
I2C clock	C30	SCL_FMC
I2C data	C31	SDA_FMC

6.1 ADC Device Clock Routing

Figure 6-1 shows the clocking system for the EVM. In addition, optional clocking modifications are listed below and highlighted in red in the block diagram. A schematic snippet is also included for clarity. The on board balun is designed to support a wide range of clock input frequenceis as it has an input bandwidth of 30MHz-6GHz. This allows for full range of operation for all devices in the family.

- Differential Clock input to ADC (Bypass on board balun).
  - By default the EVM is configured to accept a single ended clock for convenience but the board can be modified so an external differential signal can be provided. This modification can be done by making the following modification.
  - Remove C20, C19, C22
  - Install C17, C18, C23 as 0.1uF 0201 capacitors.

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- LMK04828 source clock shared from device clock input.
  - By default the board is configured so the device clock and LMK04828 reference clock come from two separate sources. There is an option to split the device clock input so it can be used as the reference clock to the LMK04828 as well. Note, this requires a higher power clock signal input to the EVM to account for the extra loss introduced by the splitting of the signal. This modification can be done by making the following modification.
  - Remove R15, R16 and R33.
  - Install R15, R16, R18 as 16 0201 resistors.
  - Install C55 as 0.1uF capacitor.

Figure 6-1 shows the clocking sub system for the EVM board. The red lines indicate the various optional clocking modifications.

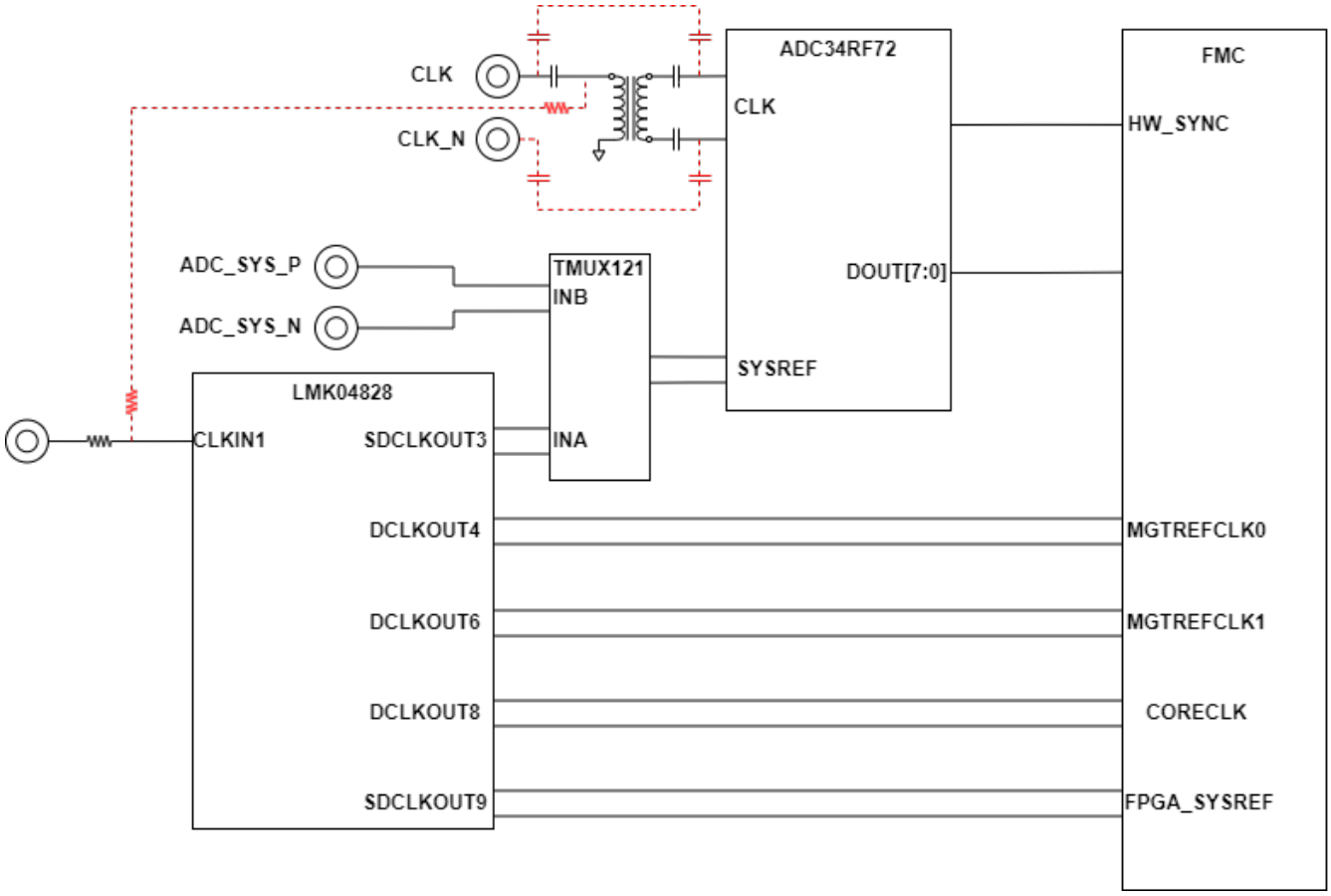


Figure 6-1. ADC3xRF7x Clock Routing

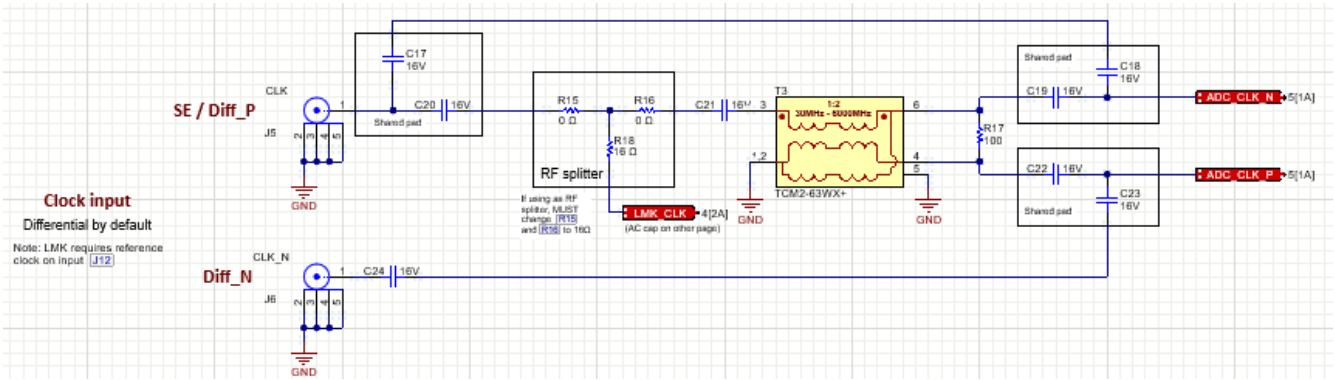


Figure 6-2. ADC3xRF7x EVM Clock Input Schematic Snippet

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6.2 Board Modifications

6.2.1 ADC3xRF7x Analog Inputs

The ADC3xRF7x has four analog inputs and the EVM routes all four as length matched signals. The default comes configured as single ended inputs that are AC couple and then SE-DIFF converted using the on board balun. There is also space on the EVM for a matching network to experiment with different matching networks depending on the application requirements.

The input networks are slightly different across the three part variants, the ADC34RF72 uses the BAL003SMG from Marki Microwave and the ADC34RF75 and ADC32RF77 use the BAL006SMG from Marki Microwave. The ADC32RF77 also only populates two out of the four input networks as it is only a two channel device whereas the ADC34RF72 and ADC34RF75 populate all four analog inputs.

The EVM can also be configured to accept an external differential signal with the following modifications. For components to bypass on board baluns, see Figure 6-3 through Figure 6-6.

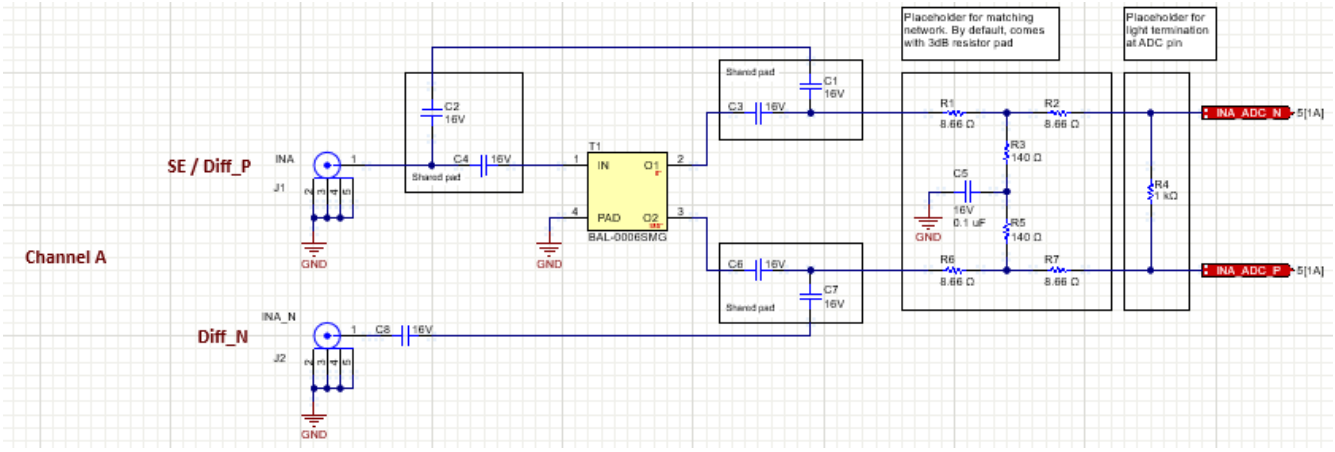


Figure 6-3. ADC3xRF72 EVM Input A Analog Input Schematic Snippet

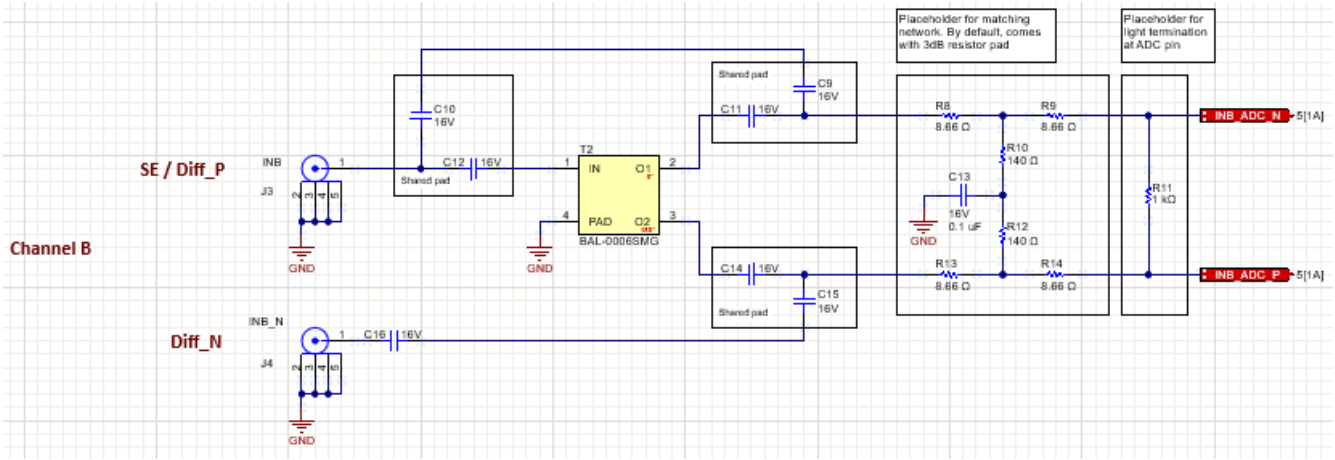


Figure 6-4. ADC3xRF72 EVM Input B Analog Input Schematic Snippet

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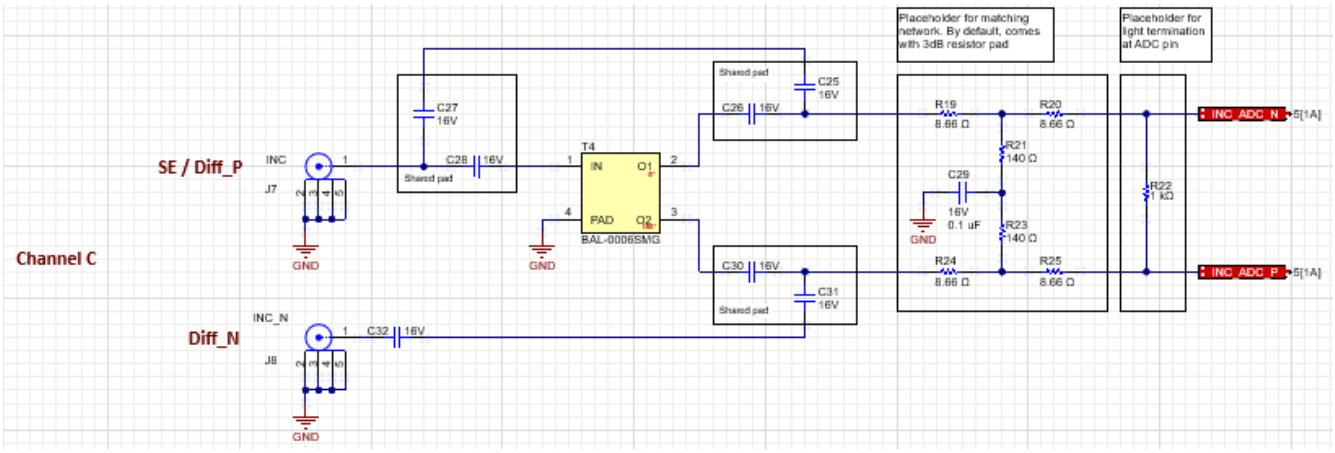


Figure 6-5. ADC3xRF72 EVM Input C Analog input Schematic Snippet

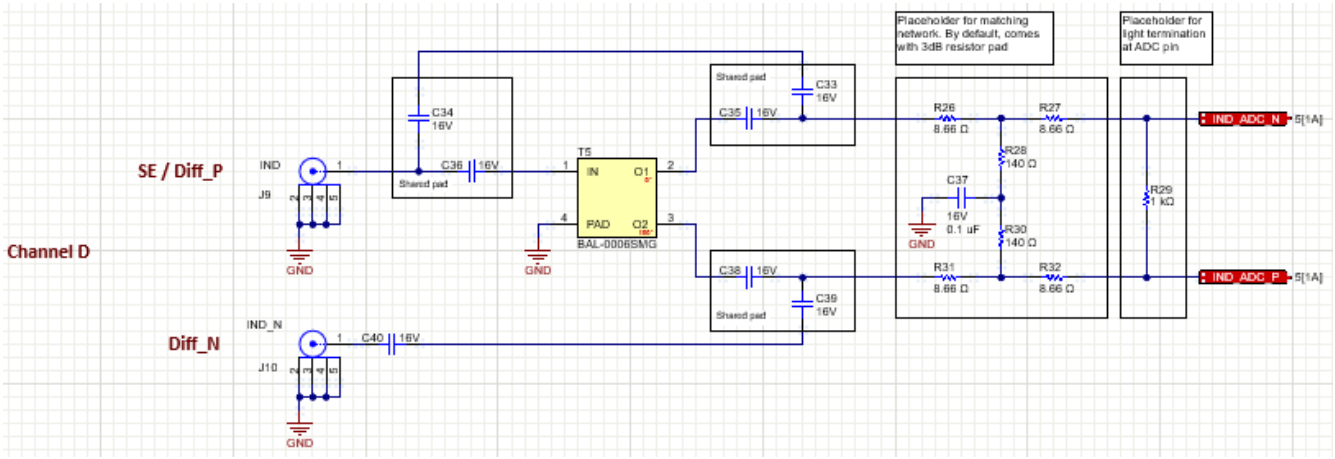


Figure 6-6. ADC3xRF72 EVM Input D Analog Input Schematic Snippet

6.2.2 EVM on Board Mux Control

The EVM uses a number of muxes and switches for controlling different aspects of control a full list can be seen below. By default all of the muxes will forced to a know state that the GUI and capture card infrastrucutre expects for normal operation. But for advanced modes it is possible to either change the state through SW via I2C controlled from the GUI. But you can also modify the pullup/pulldown resistor that set the default power on state. A full list can be seen down below as well as the default state.

Table 6-4. EVM on Board Mux Control

Mux Name	If State High	If State Low	Default State
MGTREFCLK0_MUX_SEL	MGTREFCLK0 is sourced from ADC_JESDCLK Output	MGTREFCLK0 is sourced from LMK04828 CLK Output	Low
FPGA_SYSREF_MUX_SEL	FPGA SYSREF is sourced from LMK04828 SYSREF Output	FPGA SYSREF is sourced from ADC_SYSREFOUT Output	High
SYSREFIN_MUX_SEL	ADC SYSREF Input is sourced from external SMP connectors	ADC SYSREF Input is sourced from on board LMK04828	Low
GPIO_PDN_MUX_SEL	ADC PDN GPIO is sourced from FMC connector	ADC PDN GPIO is sourced from USB	High
RSTb_MUX_SEL	ADC RSTb is sourced from FMC connector	ADC RSTb is sourced from USB connector	Low
SPI_MUX_SEL	ADC and LMK04828 SPI are source from FMC connector	ADC and LMK04828 SPI are source from USB connector	Low
USB_GPIO_DIR	USB -> ADC GPIOs	USB <- ADC GPIOs	High

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Table 6-4. EVM on Board Mux Control (continued)

Mux Name	If State High	If State Low	Default State
ADC_GPIO_MUX0	See EVM Schematic for Truth Table	See EVM Schematic for Truth Table	Low
ADC_GPIO_MUX1	See EVM Schematic for Truth Table	See EVM Schematic for Truth Table	Low
FMC_GPIO_DIR1	GPIOs 16,17,18,19 FPGA -> ADC GPIO	GPIOs 16,17,18,19 FPGA <- ADC GPIO	Low
FMC_GPIO_DIR2	GPIOs 20,21,22,23 FPGA -> ADC GPIO	GPIOs 20,21,22,23 FPGA <- ADC GPIO	Low
FMC_GPIO_DIR3	SYNCb, GPIOs 1,14,15 FPGA -> ADC GPIO	SYNCb, GPIOs 1,14,15 FPGA <- ADC GPIO	High

7 Hardware Design Files

7.1 Schematics

The schematics are available on the product page: (ADC34RF72EVM web page).

7.2 PCB Layouts

The PCB layout is available on the product page: (ADC34RF72EVM web page).

7.3 Bill of Materials (BOM)

The bill of materials is available on the product page: (ADC34RF72EVM web page).

8 Additional Information

8.1 Trademarks

All trademarks are the property of their respective owners.

9 References

- *ADC3xRF72 Quad Channel 14-bit 1.3 GSPS RF Sampling Data Converter Data Sheet* (SBASAL0)

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2025) to Revision A (November 2026) **Page**

- Added ADC34RF75EVM and ADC32RF77EVM information to document ... 1
- Updated Section Features ... 1
- Updated ADC3xRF7xEVM (ADC32RF77 EVM pictured) ... 1
- Updated Table 1-1 ... 2
- Updated Figure 2-1 ... 3
- Updated Section 2.5 ... 4
- Deleted Software Environment Setup section ... 4
- Updated Figure 2-2 ... 5
- Updated Section 2.7 ... 6
- Updated Section 2.8 ... 7
- Deleted EVM Jumpers and Switches section ... 7
- Updated Section 3.3 ... 8
- Changed Programming the ADC section title to First Time Programming the ADC EVM and updated the content ... 10
- Deleted Quick Start Mode, System level Configuration Mode, and Advanced Mode sections ... 13
- Added Section 4 ... 13
- Updated Section 4.7 ... 18

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- Changed Exporting ADC3xRF7x Configuration and Python API Usage title to Exporting ADC3xRF7x Configuration and updated content..... 19
- Deleted Further GUI Help section and added Section 4.9..... 19
- Added Section 6.2.2..... 25

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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