EVM User's Guide: DAC39RF20EVM

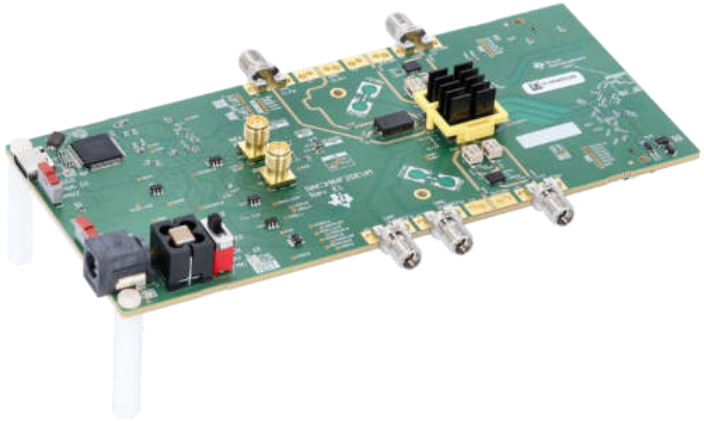
DAC39RF20 Evaluation Module

Description

The DAC39RF20EVM is an evaluation board for evaluating the DAC39RF20 family of digital-to-analog converters (DAC) from Texas Instruments. The EVM can be used to evaluate the performance of the DAC up to 22-GSPS sampling rate. The EVM is designed to work with the FPGA-based pattern generator card TSW14J59EVM. The available FMC connector on the EVM also makes interfacing the DAC to FPGA development boards from third-party vendors possible. An easy-to-use software interface GUI to control the DAC and an onboard LMK04828 clock chip through SPI are also available.

Features

- Two balun-coupled output networks per DAC output allowing singled ended signal evaluation
- A 5MHz to 10GHz low band balun for first Nyquist evaluation
- A 2GHz to 18GHz high band balun for second and third Nyquist evaluation
- A LMK04828 clock distribution chip for distributing FPGA reference clocks and SYSREF for subclass 1 operation
- A balun-coupled clock input network to test the DAC performance with an external low-noise clock source
- An FMC+ with high-speed serial data connections for full JESD204C testing of all 16 lanes
- A USB to serial chip to allow programming of the DAC or LMK with a simple USB connection
- The ability to program the DAC or LMK from an FPGA using the FMC+ connector
- Device register programming through USB connector and FTDI USB-to-SPI bus translator with option to program from FGPA using SPI through FMC+ connector



DAC39RF20EVM

1 Evaluation Module Overview

1.1 Introduction

This user's guide contains information and support documentation for the DAC39RF20EVM evaluation module (EVM), included are the circuit description, jumper settings, and required connections of the DAC39RF20EVM. This document describes the DAC39RF20EVM hardware and the software GUIs that are associated with the EVM to change, configure and evaluate the DAC in the various modes and features. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the DAC39RF20EVM.

1.2 Kit Contents (Required Equipment)

The following equipment and documents are included in the DAC39RF20EVM kit:

- Evaluation board (EVM)
- USB-C® to USB-A cable
- Power cable

The following equipments are **not** included in the DAC39RF20EVM kit, but are required for evaluation of this product:

- TSW14J59EVM data capture board and related items
- PC computer running Microsoft® Windows® 10 or higher
- Low phase-noise signal generator for DEVCLK (Sampling clock).
- Additional signal generator for FPGA reference clock generation.
  - Both signal generators need to be 10MHz reference locked.
- Two low noise power supplies: 12V/5A (TSW14J59EVM) and 12V/3A (DAC39RF20EVM)
- Three SMA type low loss cables

1.3 Specification

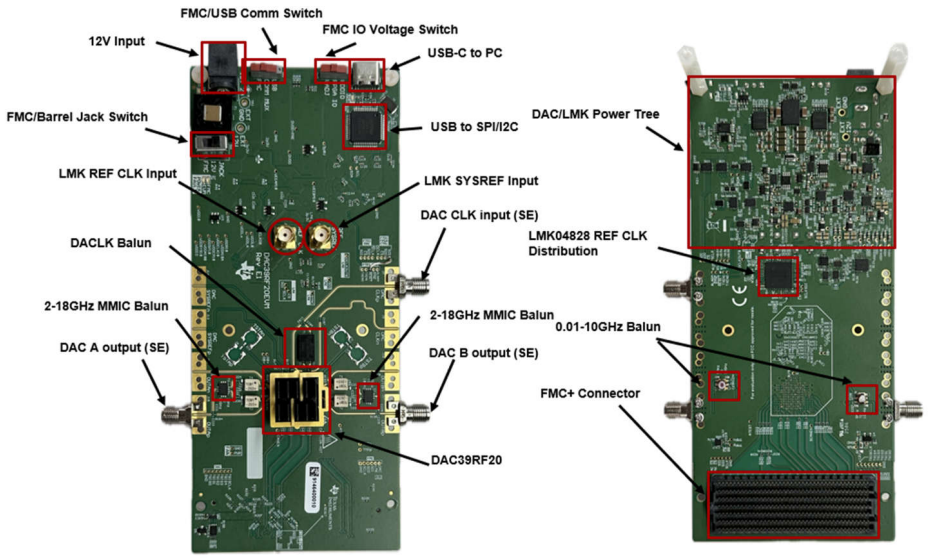


Figure 1-1. DAC39RF20EVM Key Components - Top View and Bottom View

The DAC39RF20EVM is paired with the TSW14J59EVM data capture and pattern generator card. If the DAC39RF20EVM is only used in DDS mode, then data capture EVM is not required.

To improve signal routing quality, serial lane polarity is inverted with respect to the standard FMC VITA-57 signal mapping. Signal mapping and polarity is shown in Section 2.3).

1.4 Device Information

The DAC39RF20 is a family of single and dual channel DACs with 16-bit resolution. The devices can be used in noninterpolation modes (real) as well as interpolation modes (complex IQ). At 22GSPS, single channel 16-bit real data is supported. In addition, 21GSPS, dual channel 12-bit real data is supported. Up to 4.4GHz of complex bandwidth is also supported.

2 Hardware

2.1 Setup Procedure

This section describes how to setup the DAC and TSW14J59 EVMs on the bench with the proper equipment to evaluate the performance of the DAC device.

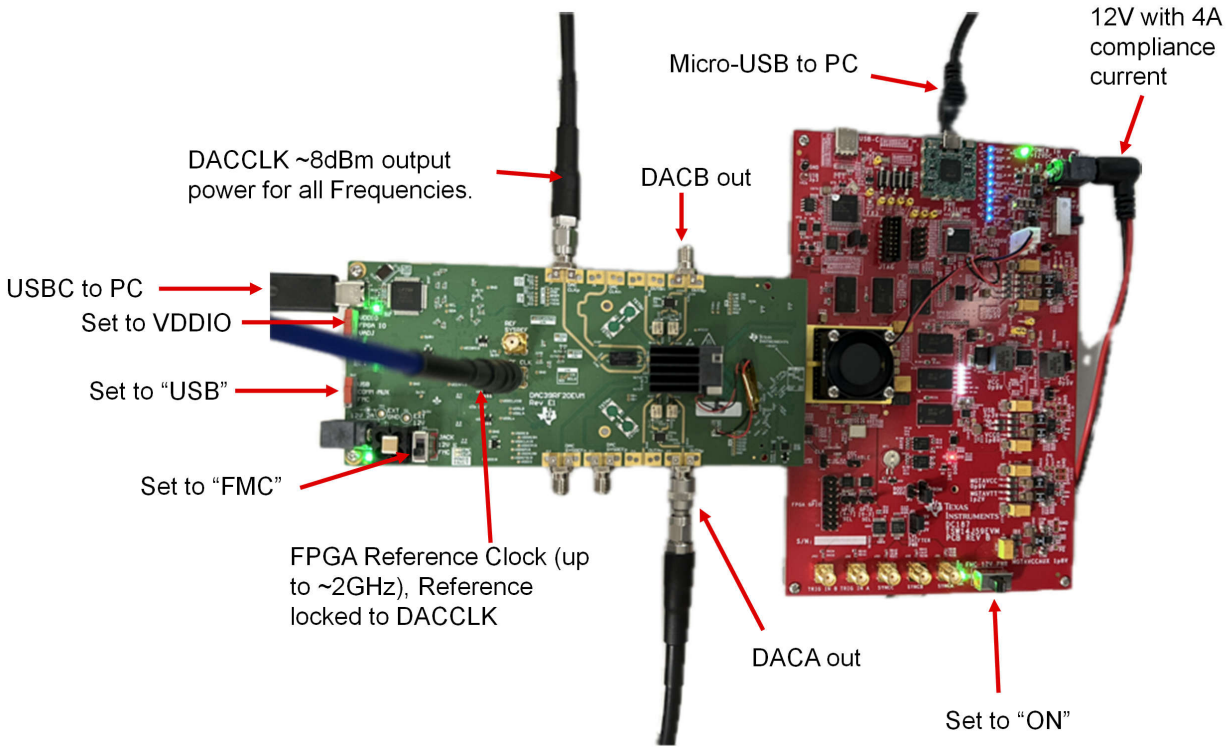


Figure 2-1. DAC39RF20EVM Test Setup

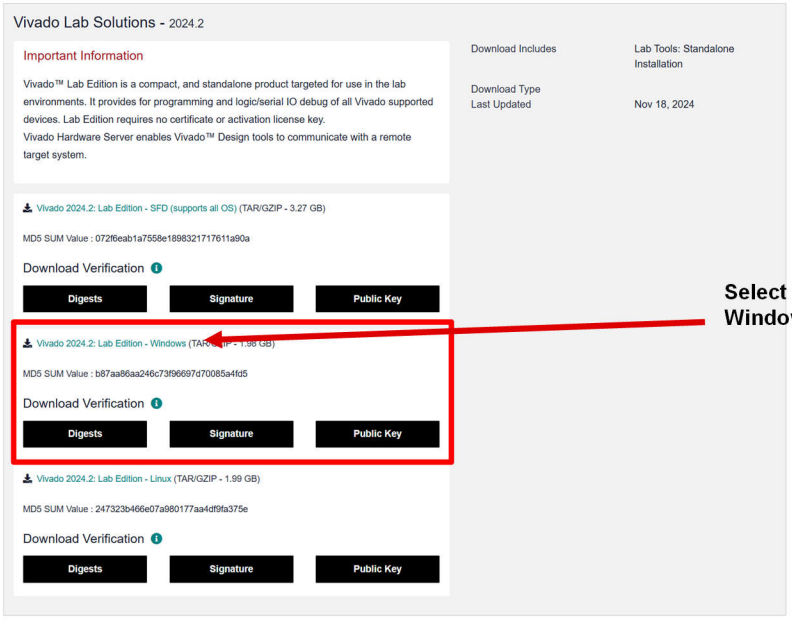
2.1.1 Installing the DAC39RF20EVM Configuration GUI Software

1. Download the DAC39RF20EVM Configuration GUI software from the EVM tool folder at DAC39RF12EVM GUI.
   a. The GUI download includes the following:
      i. DAC39RF20EVM GUI
      ii. J59 Commander
         1. DAC WaveGen
      iii. J59 Server
2. Run the executable file (DAC39RF20EVM_SW_Package_vXXXX.exe).
3. Install Vivado Lab Tools.
   a. Go to the next section for instructions on how to install the Xilinx™ tools and add environment variables path to the desktop PC.

2.1.1.1 Installing and Setting Up Vivado™ Lab Tools

For the DAC39RF20EVM, Vivado™ Lab Tools needs to be installed. Follow the steps outlined in this section.

1. Create a user account for AMD and sign in.
   a. Fill out the appropriate information before downloading.
   b. When complete, click the download button.
2. The download file type is a .tar file. In Windows, open the .tar file and explore.
3. Next, find <xsetup.exe> in the Vivado_Lab_Win_2024.2_1113_1001 folder.
   a. Right-click and execute. Operating systems with Windows need consent to *Extract All*.
4. Once the files are extracted, open the folder and find *xsetup.exe*.
   a. Right-click on this file and install. Operating systems with Windows need permissions.
5. Follow the sequence of steps in the figures below to finish the Xilinx Lab Tools installation.



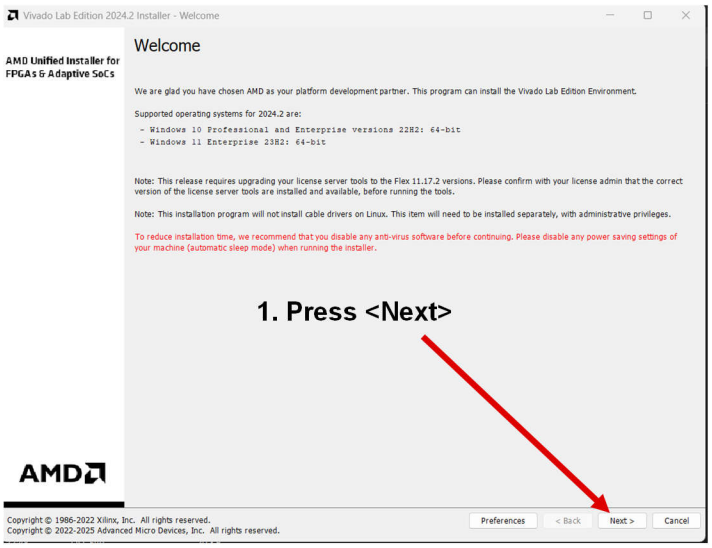
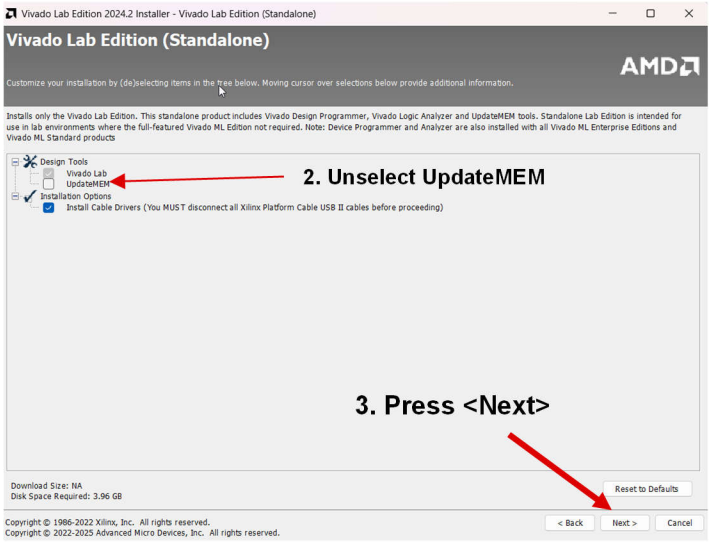
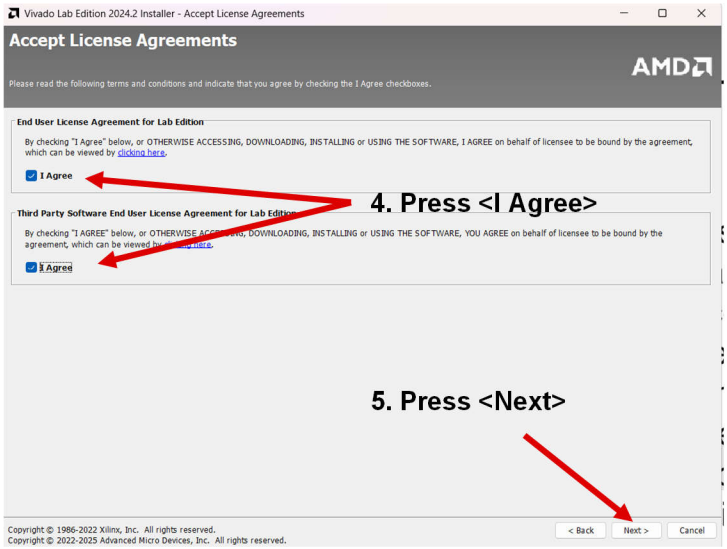
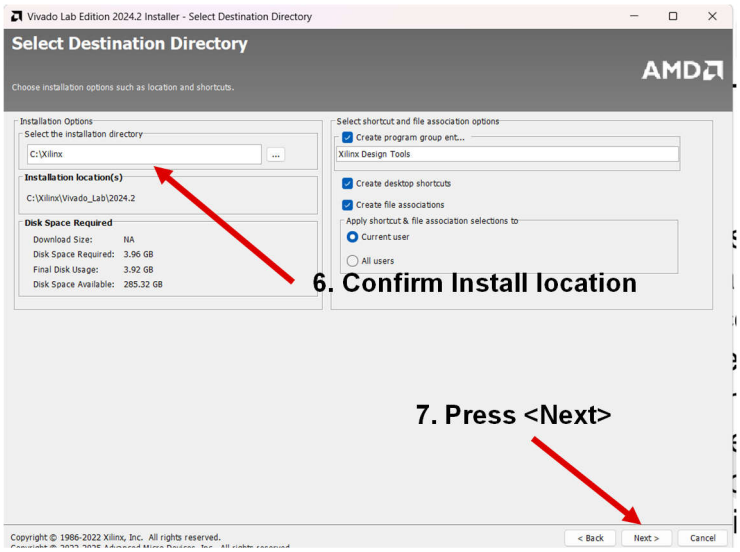
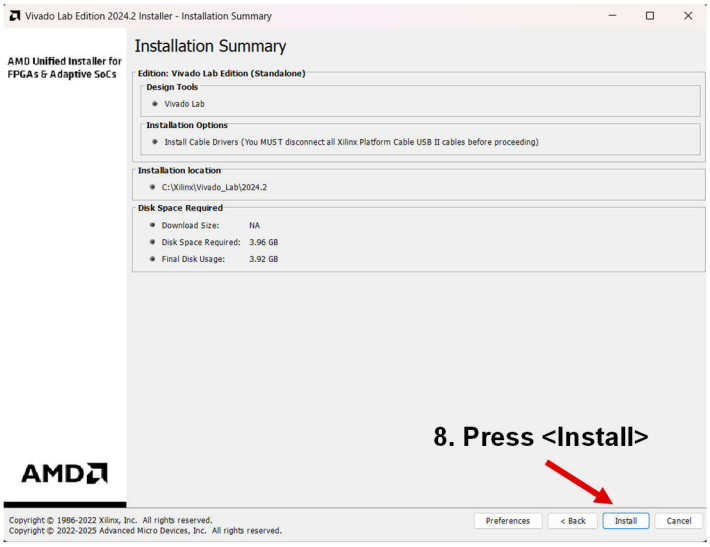


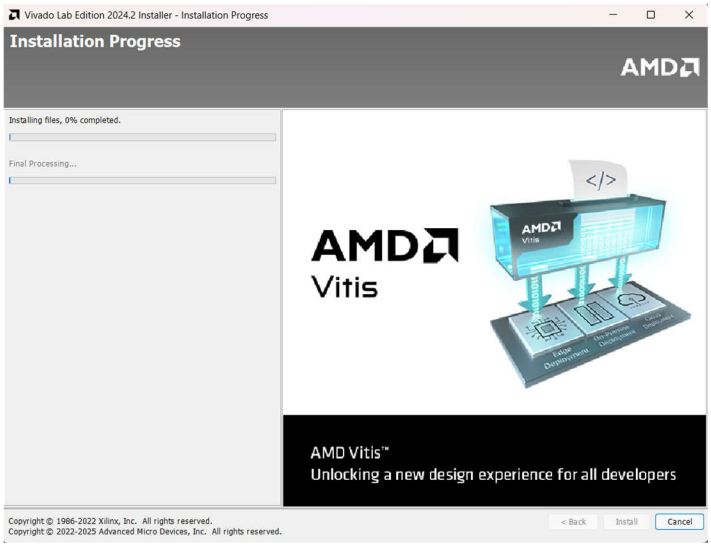
Figure 2-2. Installing Vivado Lab Tools

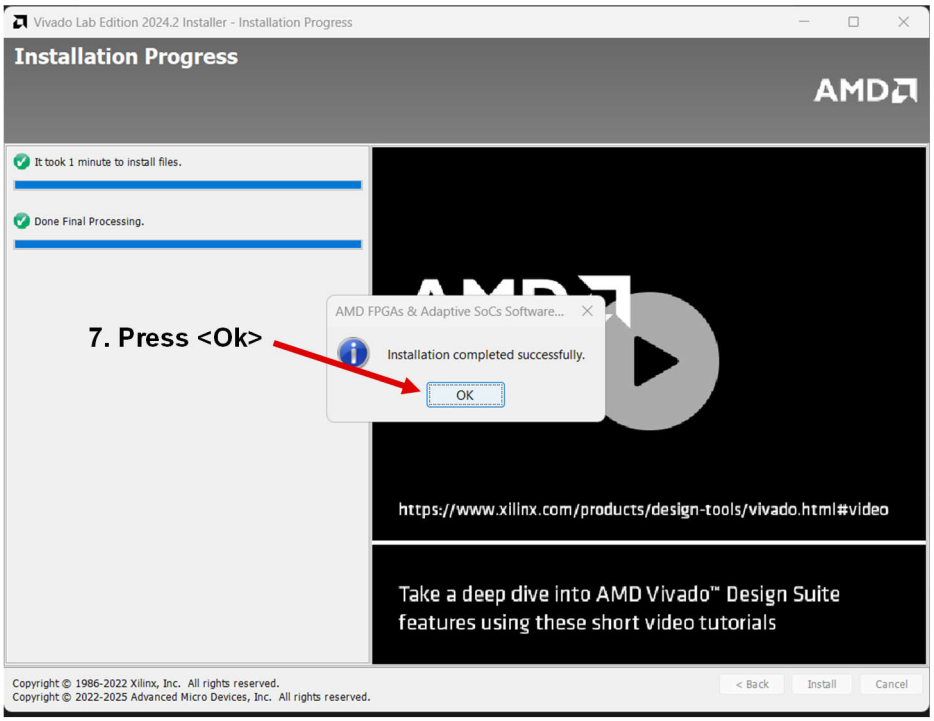












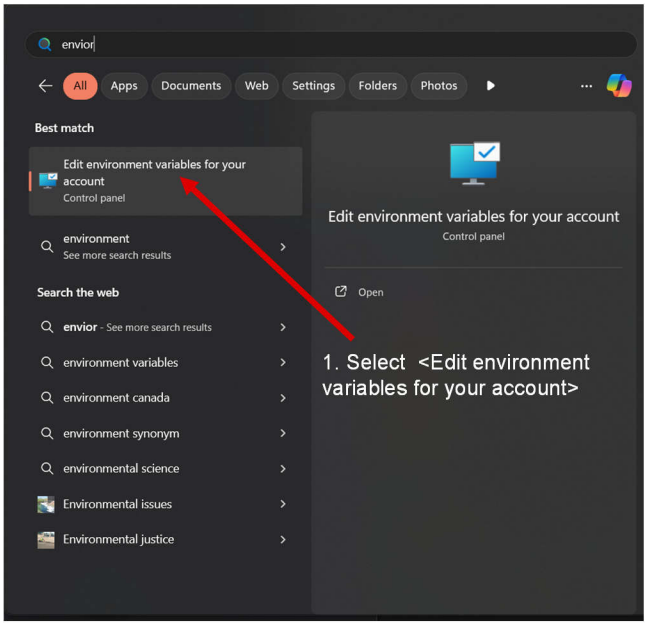
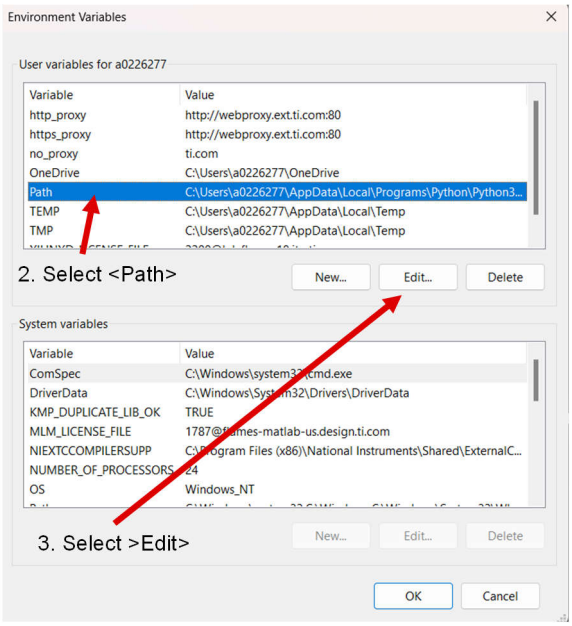
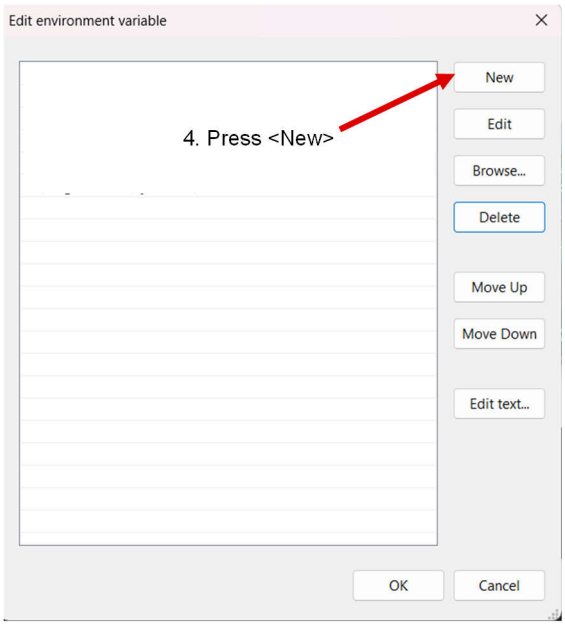
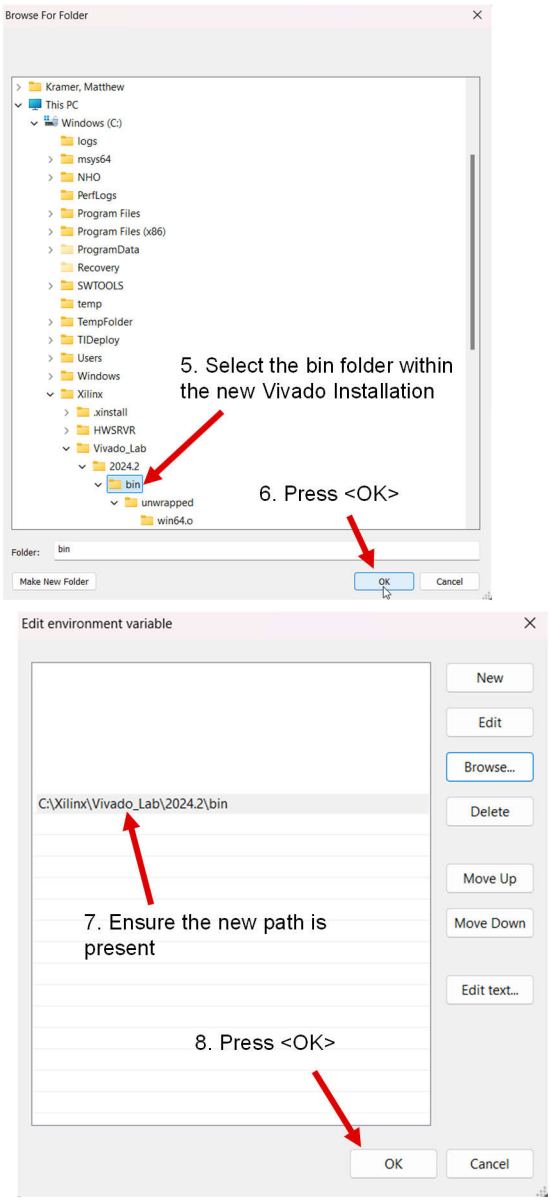


Figure 2-3. Adding Vivado Lab Tools to the Windows PATH







Once this is complete, the J59_Server can run.

2.1.2 Connect the DAC39RF20EVM and TSW14J59EVM

With the power off, connect the DAC39RF20EVM to the TSW14J59EVM through the FMC+ connector as shown in Section 2.1.

2.1.3 Connect the Power Supplies to the Boards (Power Off)

1. Confirm the power switch on the TSW14J59EVM is in off position. Connect the power cable to a 12V DC (minimum 5A) power supply. Make sure the proper supply polarity by confirming the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the TSW14J59EVM power connector.
2. DAC39RF20EVM can be powered with 12V DC (minimum 3A) though the connector jack (J2) on the DAC39RF20EVM, or the EVM can be powered from the TSW14J59EVM by FMC+ connector. There is a switch (SW1) which can be used to select power from the barrel jack on the DAC EVM, or from TSW14J59EVM through FMC+ connector. Confirm that the power switch for the DAC39RF20EVM power supply is set to the opposite position (jack) from where the the EVM is drawing power. If using barrel jack option, then connect the power cable to a 12V DC (minimum 3A) power supply. Make sure the proper supply polarity by confirming that the outer surface of the barrel connector is GND and the inner portion of the connector is 12V. Connect the power cable to the EVM power connector. Table 2-1 is used as a reference to power the DAC39RF12EVM.

Table 2-1. Powering the DAC39RF12EVM

DAC39RF20 Powered From	DAC39RF20 Power Switch Position	TSW14J59EVM FMC Switch Position	Power Supply Needed
TSW14J59EVM by FMC+ connector	FMC	ON	12V 5A for TSW14J59EVM
External supply with jack on DAC39RF20EVM	JACK	OFF	12V 3A for TSW14J59 and 12V 3A for DAC39RF20EVM

CAUTION

Make sure the power connections to the EVMs are the correct polarity. Failure to do so can result in immediate damage. Leave the power switches in the off position until directed later.

2.1.4 Connect the Spectrum Analyzer to the EVM

Connect a spectrum analyzer to the OUTAp (J15) SMA connector of the DAC39RF20EVM.

1. The FPGA REF clock frequency can be obtained from the DAC39RF20EVM GUI once the DAC39RF20EVM GUI is configured to the desired JMODE mode and clock rate. The reference clock frequency required by the EVM is shown in Figure 1-1.
2. Make sure that the DEVCLK and reference clock sources are frequency-locked using a common 10MHz reference to for functionality.
3. Do not turn on the RF output of any signal generator at this time.
4. In all of these examples, the FPGA REF clock = 1250MHz, the DAC sampling clock = 20.0GHz.

2.1.5 Turn On the TSW14J59EVM Power and Connect to the PC

1. Turn on the power switch to the TSW14J59EVM.
2. Connect a micro-USB cable from the PC to the TSW14J59EVM.

2.1.6 Turn On the DAC39RF20EVM Power Supplies and Connect to the PC

1. The default option uses the power from FMC+ connector on TSW14J59EVM. For this option, the FMC power switch on the TSW14J59EVM must be set to the on position, and power switch on the DAC39RF20EVM must be set to FMC(default). If external power supply is used to power the DAC EVM. Then turn on the 12V power supply connected to the barrel jack on the DAC EVM and set the power switch position on DAC39RF20EVM to JACK position.
2. Connect the DAC EVM to the PC with the USB-C cable to the EVM.

2.1.7 Turn On the Signal Generators

1. Turn on the output of the low phase noise RF signal generator and connect to DAC CLKp (J7) by SMA cable. Set the signal generator to 20GHz at a +6dBm output level.
2. Turn on the output of the RF signal generator and connect to REF_CLK (J5) by SMA cable.
3. Set the signal generator to 1250MHz at a +6dBm output level. Using another SMA cable, connect to OUTAp (J15), which is the output of the DAC to a spectrum analyzer.

Note

The max clock rate supported by DAC39RF20EVM is 22GHz.

2.1.8 Launching the DAC39RF20EVM GUI and Programming the DAC EVM - JMODE 0 (Bypass Mode)

The configuration example of DAC39RF20EVM in JMODE 0, (bypass mode) is shown below.

1. JMODE 0 is considered bypass mode or real data mode, interpolate x1.
   a. Configuration details:
      i. 20GSPS at +6dBm
      ii. 20.625Gbps SERDES rate
      iii. 16 lanes
      iv. JESD_M = 1

2. Follow the steps in the following figures to launch the DAC GUI. Following the steps as shown to configure the EVM.

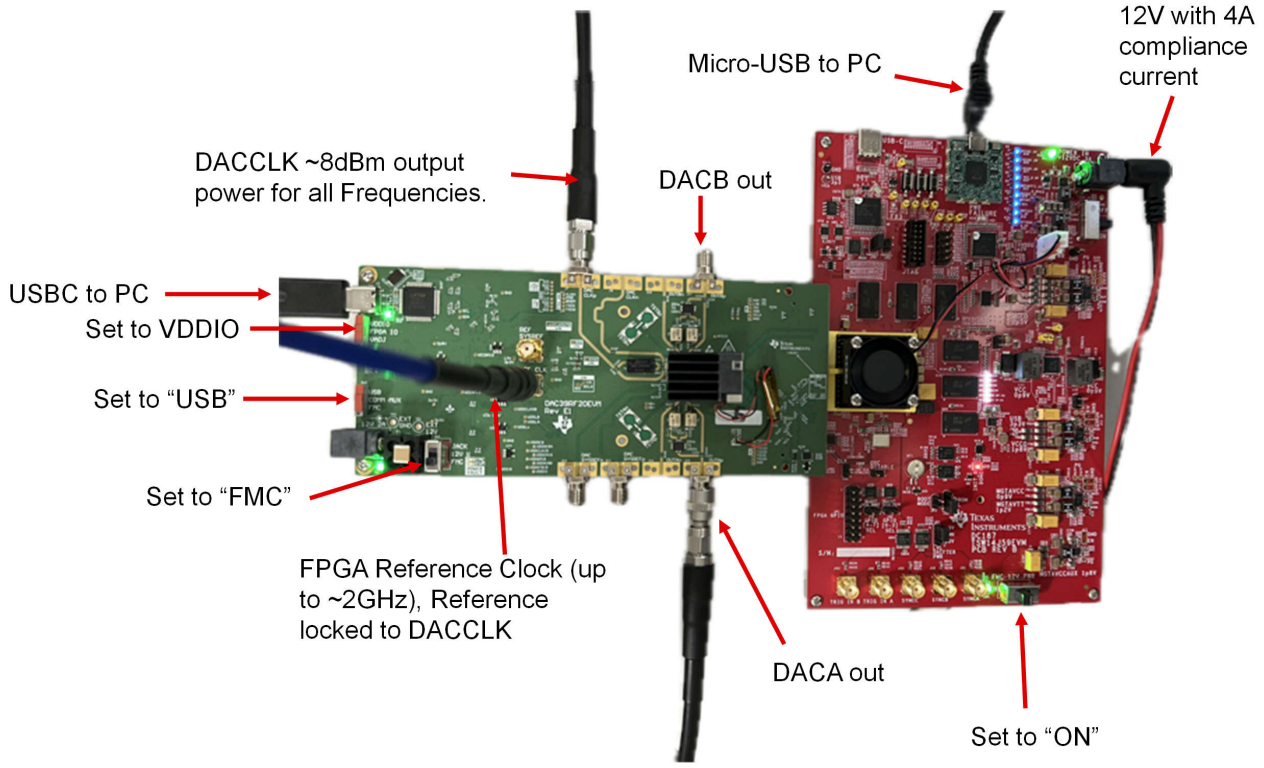
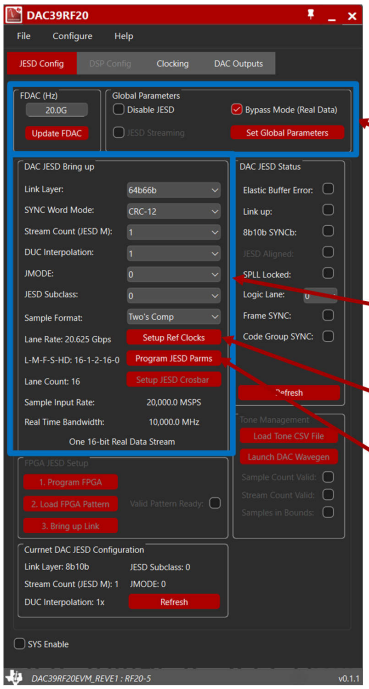


Figure 2-4. DAC39RF20EVM EVM Hardware Setup, JMODE 0



1. **Launch the DAC39RF20 GUI**.

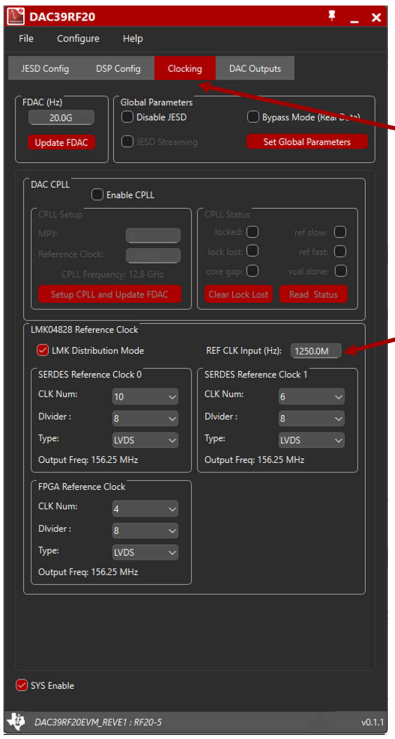
2. **Uncheck "Disable JESD" and check "Bypass Mode" and press"Set Global Parameters".** This will reset the device and setup bypass mode. One can also set FDAC here. FDAC = 20GSPS by default. This will disable all DSP functionality of the DAC.

3. Default JESD parameters for bypass mode are JMODE0. This is a single stream with 16 bits of resolution and a full 10GHz of IBW. Additional JMODES may be available at lower update rates. Other JMODES with lower resolution (8 and 12 bit) are also available.

4. **Press "Setup Ref Clocks".** This will setup the onboard LMK04828 to destitute the provided reference clock to the FPGA. It automatically will set the dividers. (See next slide for more information).

5. Press "Program JESD Parms". This will load the current configuration into the DAC and set SYS_EN to 1. The DAC will be waiting for the FPGA to setup the link.

Figure 2-5. EVM GUI Configuration for JMode 0 - JESD Config Tab



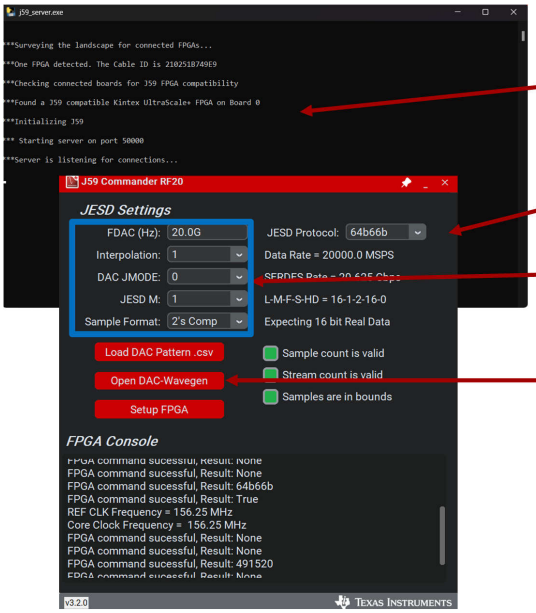
1. **Press "Clocking" Tab**

2. **Provide this clock to REF input.** Note that pressing "Setup Ref Clocks" on the JESD Config tab brought the LMK04828 into distribution mode and setup the necessary outputs and dividers for this board for the given lane rate.

Additional Notes. One could Provide 675MHz to the LMK and set the dividers to 2 manually if they have a limitation in their setup. The important thing is to make sure the final output frequency of the LMK matches the output the GUI setup when "Setup Ref Clocks" was pressed. This should all be done before the link is established.

Figure 2-6. EVM GUI Configuration for JMode 0 - Clocking Tab

1. Then, launch the J59_Server.exe as shown in the figure.
2. Next, launch the J59_Commander.
3. Then, open the DAC Wavegen GUI.



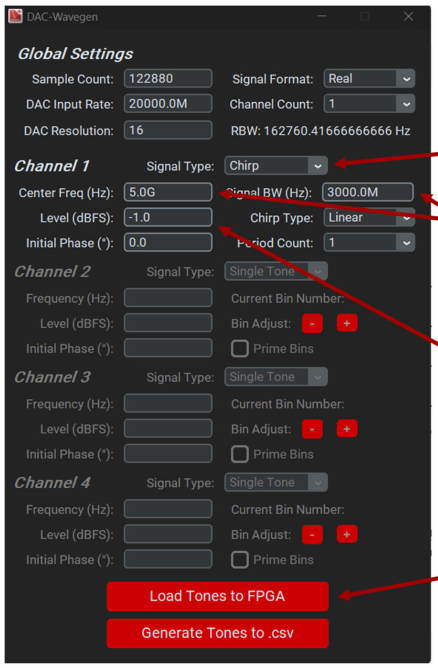
1. **Launch J59_server.exe.** If the FPGA is connected to the PC and necessary Xilinx drivers are installed the server should output the following.

2. **Launch J59-Commander-v3.2.0.exe.** It will default to the same configuration as the DAC EVM GUI.

3. **Adjust JESD parameters.** Set the DAC Interpolation to 1. This should automatically set the JMODE to 0 and JESD_M to 1. Note that the Parameters listed should match the DAC GUI.

4. **Launch DAC-Wavegen.** If a .csv file has been saved with enough streams in it one can also Load the DAC pattern .csv file.

Figure 2-7. J59 Server.exe and J59 Commander, Setup Part 1



1. **Set Channel 1 Signal Type to “Chirp”.** In this example there is one complex channel. This complex channel will have a 2GHz wide chirp on it to demonstrate modulation with the DAC.

2. **Set the Center Frequency to 5Hz**. There is no NCO in bypass mode to upconvert.

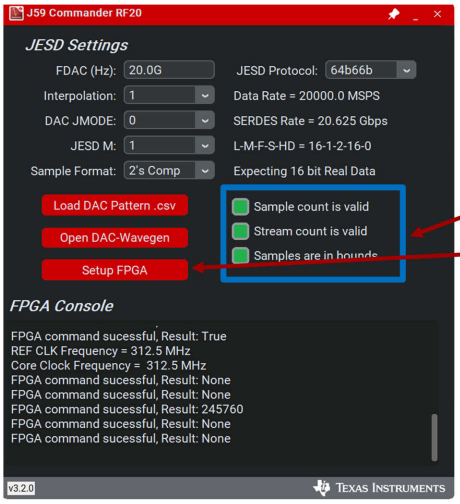
3. **Set the Bandwidth of the tone**. 2GHz is being used for this example. Up to 4GHz can be used when the tone is centered at 0Hz. The center frequency must be set first so the the bandwidth is known to be valid by the tool.

4. **Set the Level in dBFS and initial phase**. -1 is being used for the level to help with lineary. The initial phase is left at 0.

5. **Press “Load Tones to FPGA”.** This will point the tool to the new tone to load into FPGA memory. One can also save it as a .csv file to load later.

* The DAC Wavegen is automatically configured by the J59 Commander to match the DAC configuration.

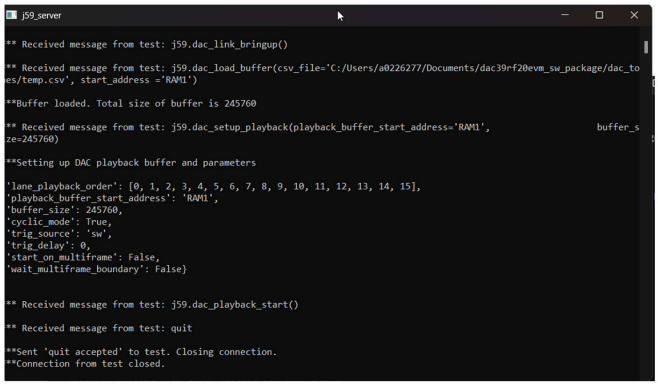
Figure 2-8. DAC Wavegen GUI Setup Details



1. Once the tone is loaded, These 3 indicators should turn green.

2. Press "Setup FPGA". The J59 Commander will being communicating with the J59 Server. It will program the FPGA (if necessary) and setup the FPGA JESD parameters and load the tone.

Figure 2-9. J59 Commander Setup Details, Part 2



Once the FPGA is setup the J59 server should show dac_playback_start() followed by quit.

The J59 Commander will show the following once the FPGA is setup

Figure 2-10. J59 Server.exe and J59 Commander, Setup Part 2

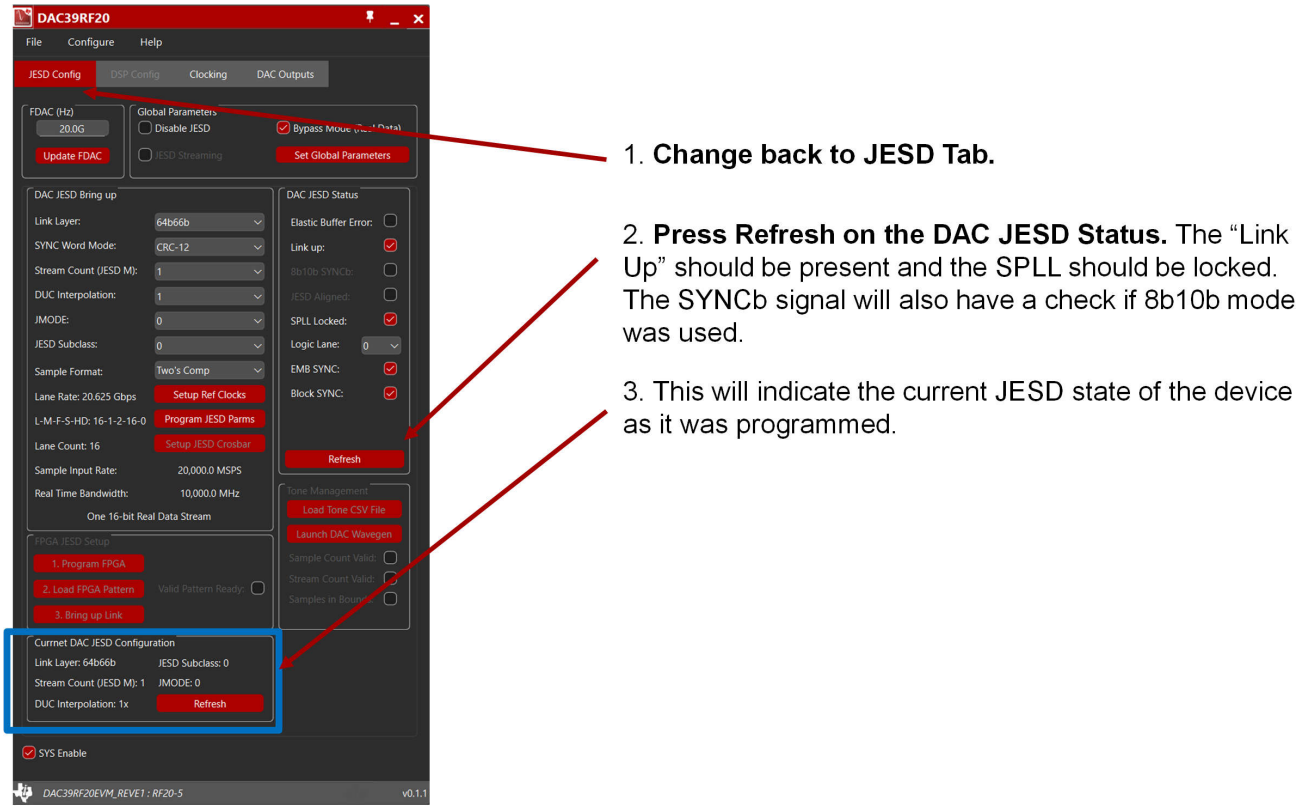
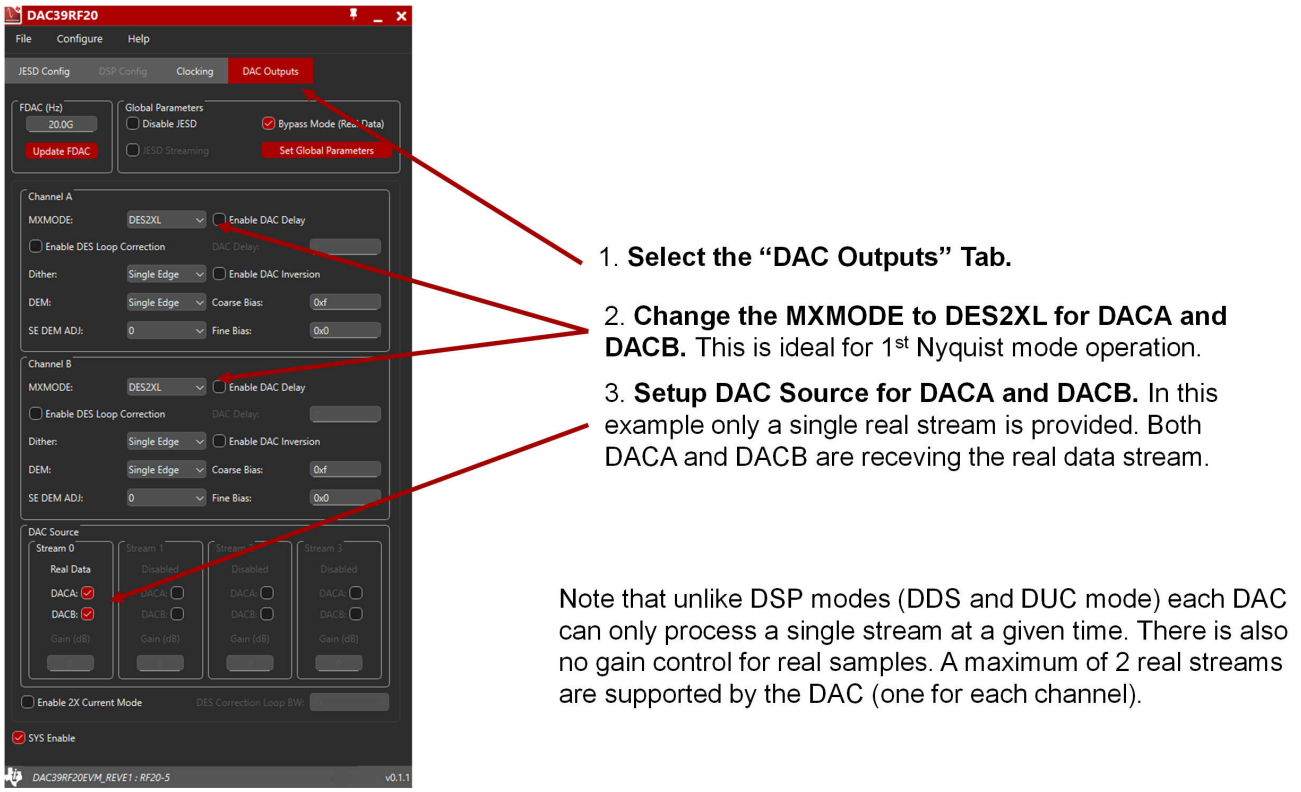


Figure 2-11. EVM GUI Configuration for JMode 0 - JESD Config Tab, Checking Status



Note that unlike DSP modes (DDS and DUC mode) each DAC can only process a single stream at a given time. There is also no gain control for real samples. A maximum of 2 real streams are supported by the DAC (one for each channel).

Figure 2-12. EVM GUI Configuration for JMode 0 - Setup DAC Outputs Tab

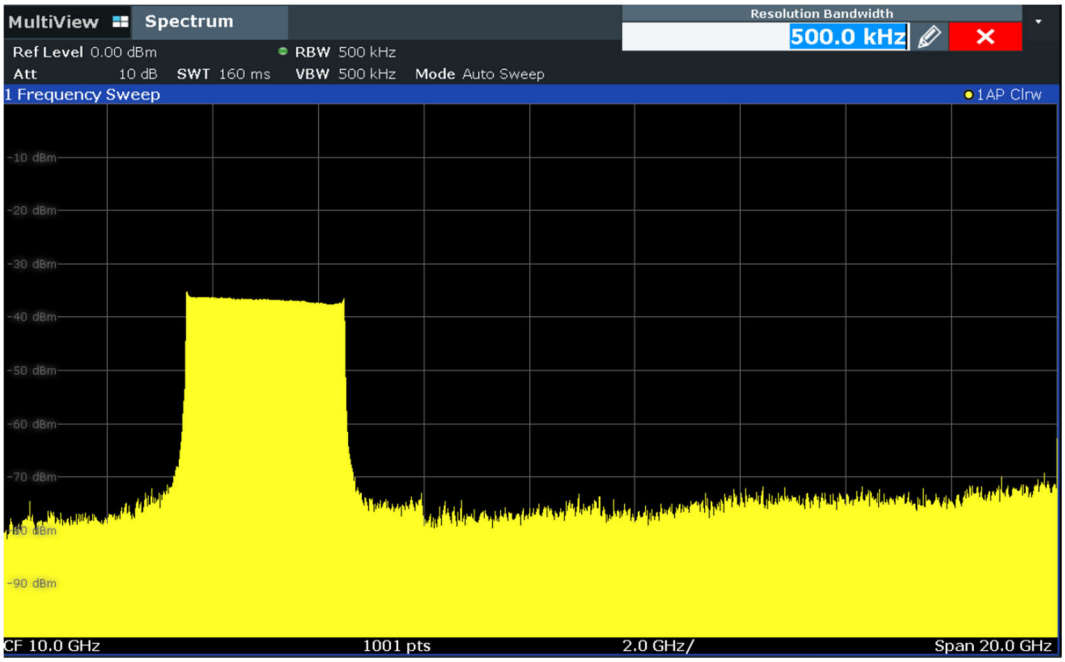


Figure 2-13. DAC Output Spectrum, JMODE 0, Single Stream at 20GSPS

A 3GHz wide LMF can be seen in the output spectrum. Note, that no NCO was used and this chirp was synthesized as a single real data stream.

2.1.9 Launching the DAC39RF20EVM GUI and Programming the DAC EVM - JMODE 1 (DUC Mode)

The configuration example of DAC39RF20EVM in JMODE 1 is shown below.

1. JMODE 1: complex data, interpolate x4.
   a. Configuration details:
      i. 20GSPS at +6dBm
      ii. 10.3125Gbps SERDES rate
      iii. 16 lanes
      iv. JESD_M = 2

2. Follow the steps in the following figures to launch the DAC GUI. Follow the steps as shown to configure the EVM.

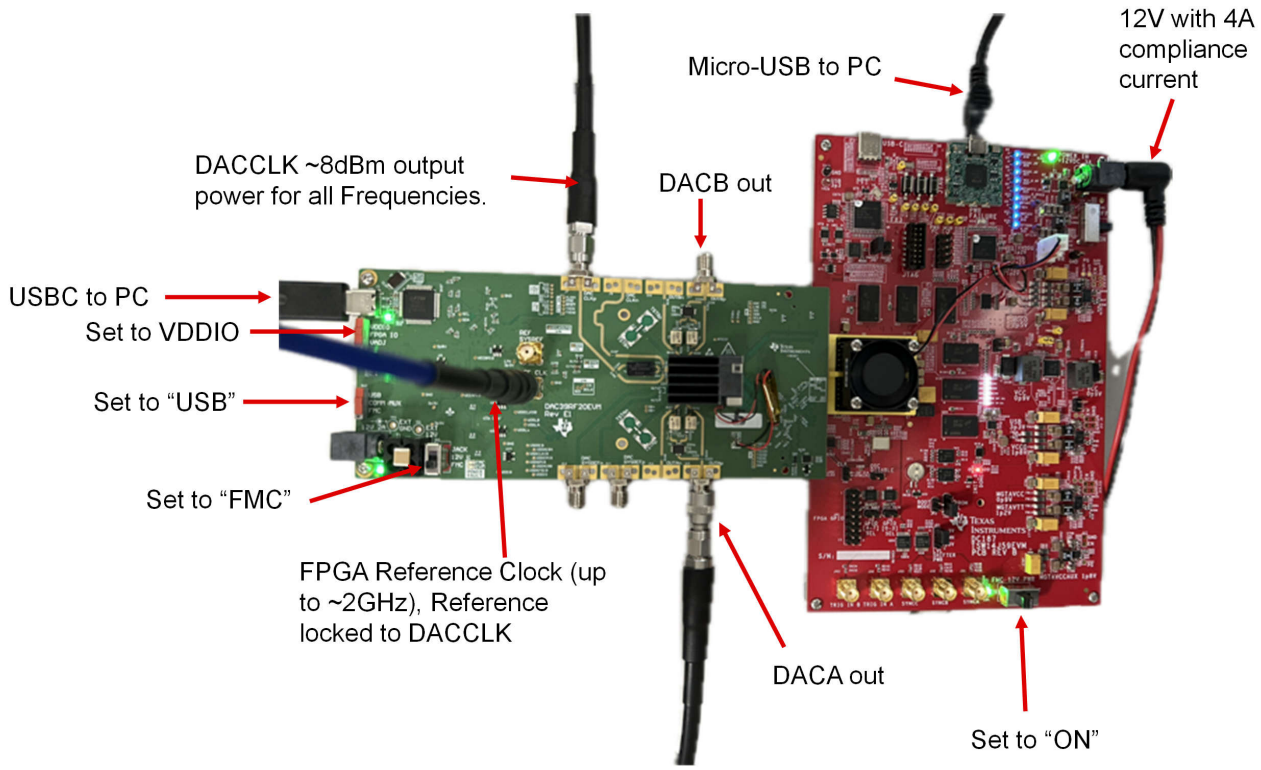
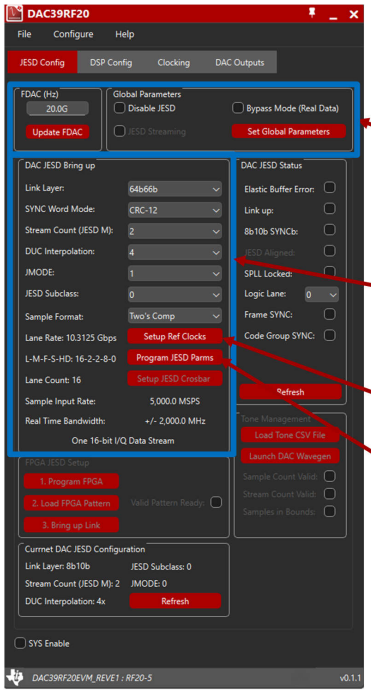


Figure 2-14. DAC39RF20EVM EVM Hardware Setup, JMODE 1



1. **Launch the DAC39RF20 GUI**.

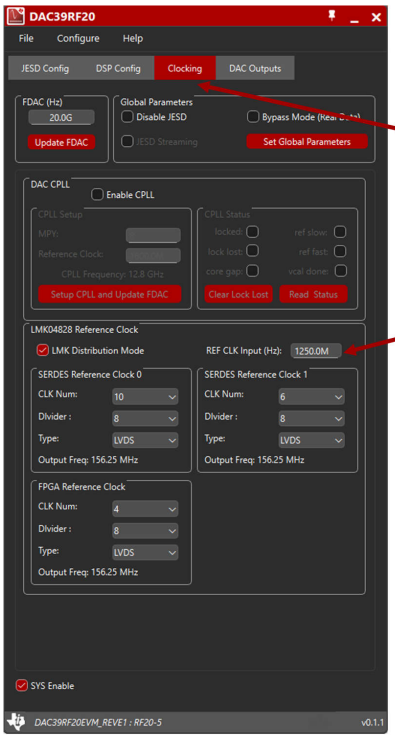
2. **Uncheck Bypass Mode and Disable JESD and press "Set Global Parameters".** This will reset the device and setup DUC up-conversion mode. One can also set FDAC here. FDAC = 20GSPS by default.

3. Default JESD parameters for DUC up-conversion are JMODE1 interpolate by 4. One can increase stream count, interpolation and change the JMODE accordingly. One should start at the top and move down. In this example leave everything default

4. **Press "Setup Ref Clocks".** This will setup the onboard LMK04828 to destitute the provided reference clock to the FPGA. It automatically will set the dividers. (See next slide for more information).

5. Press "Program JESD Parms". This will load the current configuration into the DAC and set SYS_EN to 1. The DAC will be waiting for the FPGA to setup the link.

Figure 2-15. EVM GUI Configuration for JMode 1- JESD Config Tab

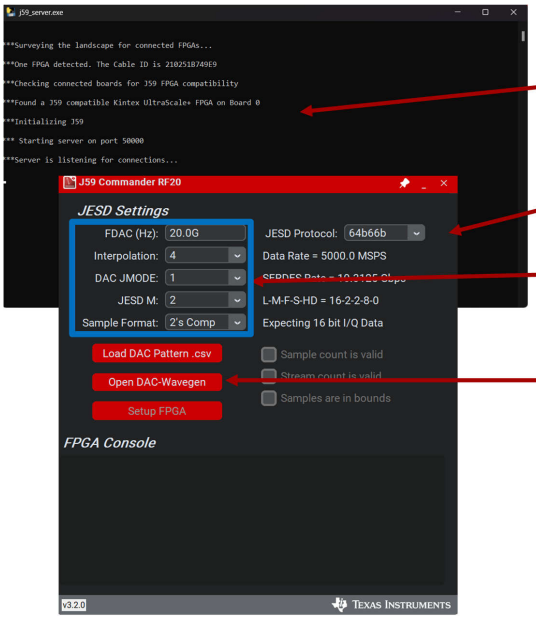


1. **Press "Clocking" Tab**

2. **Provide this clock to REF input.** Note that pressing "Setup Ref Clocks" on the JESD Config tab brought the LMK04828 into distribution mode and setup the necessary outputs and dividers for this board for the given lane rate.

Additional Notes. One could Provide 675MHz to the LMK and set the dividers to 4 manually if they have a limitation in their setup. The important thing is to make sure the final output frequency of the LMK matches the output the GUI setup when "Setup Ref Clocks" was pressed. This should all be done before the link is established. Note that the GUI always assumes FDAC/16 for interpolating JMODES is being provided to the reference clock input. This means the manual change would need to be done each time the clocks are setup. The clock output and type should not be changed with this EVM board.

Figure 2-16. EVM GUI Configuration for JMode 1- Clocking Tab



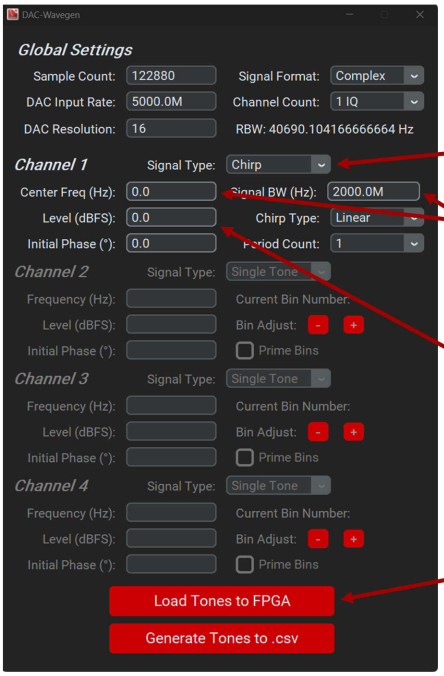
1. **Launch J59_server.exe.** If the FPGA is connected to the PC and necessary Xilinx drivers are installed the server should output the following.

2. **Launch J59-Commander-v3.2.0.exe.** It will default to the same configuration as the DAC EVM GUI.

3. **Adjust JESD parameters.** If the parameters were changed in in the DAC GUI for different interpolation, JMODE and JESDM, adjust the J59 commander to match these settings.

4. **Launch DAC-Wavegen.** If a .csv file has been saved with enough streams in it one can also Load the DAC pattern .csv file.

Figure 2-17. J59 Server.exe and J59 Commander, Setup Part 1



1. **Set Channel 1 Signal Type to “Chirp”.** In this example there is one complex channel. This complex channel will have a 2GHz wide chirp on it to demonstrate modulation with the DAC.

2. **Set the Center Frequency to 0Hz**. This will be mixed up with the NCO on the DAC.

3. **Set the Bandwidth of the tone**. 2GHz is being used for this example. Up to 4GHz can be used when the tone is centered at 0Hz. The center frequency must be set first so the the bandwidth is known to be valid by the tool.

4. **Set the Level in dBFS and initial phase**. 0 is fine for both of these.

5. **Press “Load Tones to FPGA”.** This will point the tool to the new tone to load into FPGA memory. One can also save it as a .csv file to load later.

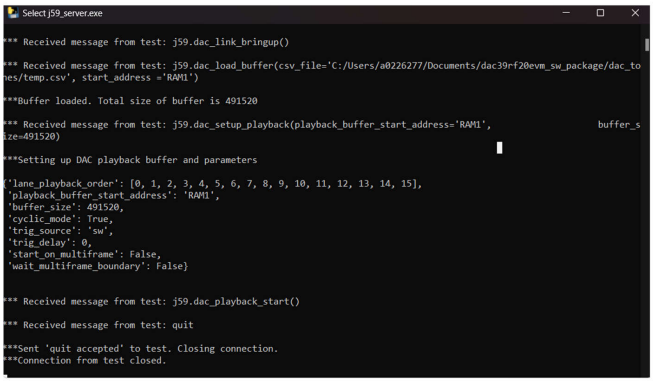
* The DAC Wavegen is automatically configured by the J59 Commander to match the DAC configuration.

Figure 2-18. DAC Wavegen GUI Setup Details

1. Once the tone is loaded, These 3 indicators should turn green.

2. Press "Setup FPGA". The J59 Commander will being communicating with the J59 Server. It will program the FPGA (if necessary) and setup the FPGA JESD parameters and load the tone.

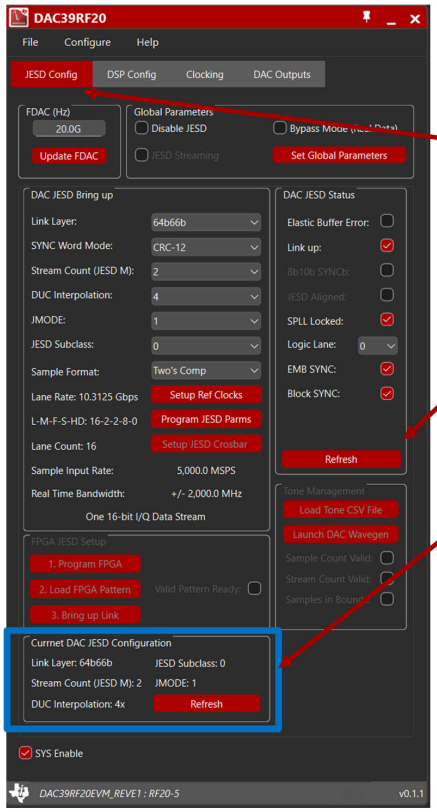
Figure 2-19. J59 Commander Setup Details, Part 2



Once the FPGA is setup the J59 server should show dac_playback_start() followed by quit.

The J59 Commander will show the following once the FPGA is setup

Figure 2-20. J59 Server.exe and J59 Commander, Setup Part 2

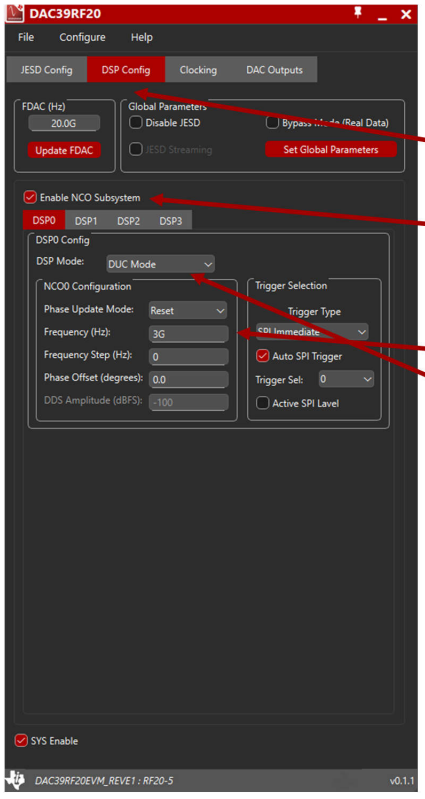


1. **Change back to JESD Tab.**

2. **Press Refresh on the DAC JESD Status.** The "Link Up" should be present and the SPLL should be locked. The SYNCb signal will also have a check if 8b10b mode was used.

3. This will indicate the current JESD state of the device as it was programmed.

Figure 2-21. EVM GUI Configuration for JMode 1- JESD Config Tab, Checking Status



1. **Select the "DSP Config" Tab.**

2. **Check "Enable NCO Subsystem".**

3. **Enter NCO Frequency.** 5GHz is being used for this example as this will center the 2GHz chirp to be 4GHz to 6GHz. Once the Frequency is entered just press "Enter" ("Auto SPI Trigger" should be selected).

4. Note that DSP0 was automatically set to "DUC Mode". When the JESD is configured with an M of 2 (1 IQ) DSP0 is automatically configured for DUC mode. DSPs1, 2 and 3 will all be "disabled" and will not be able to be configured for DUC mode unless JESD M is increased in the JESD configuration (4 will enable DSP1 DUC Mode, 6 will enable DSP2 DUC Mode, etc).

Figure 2-22. EVM GUI Configuration for JMode 1- Setup DSP Config Tab for NCO, Part 1

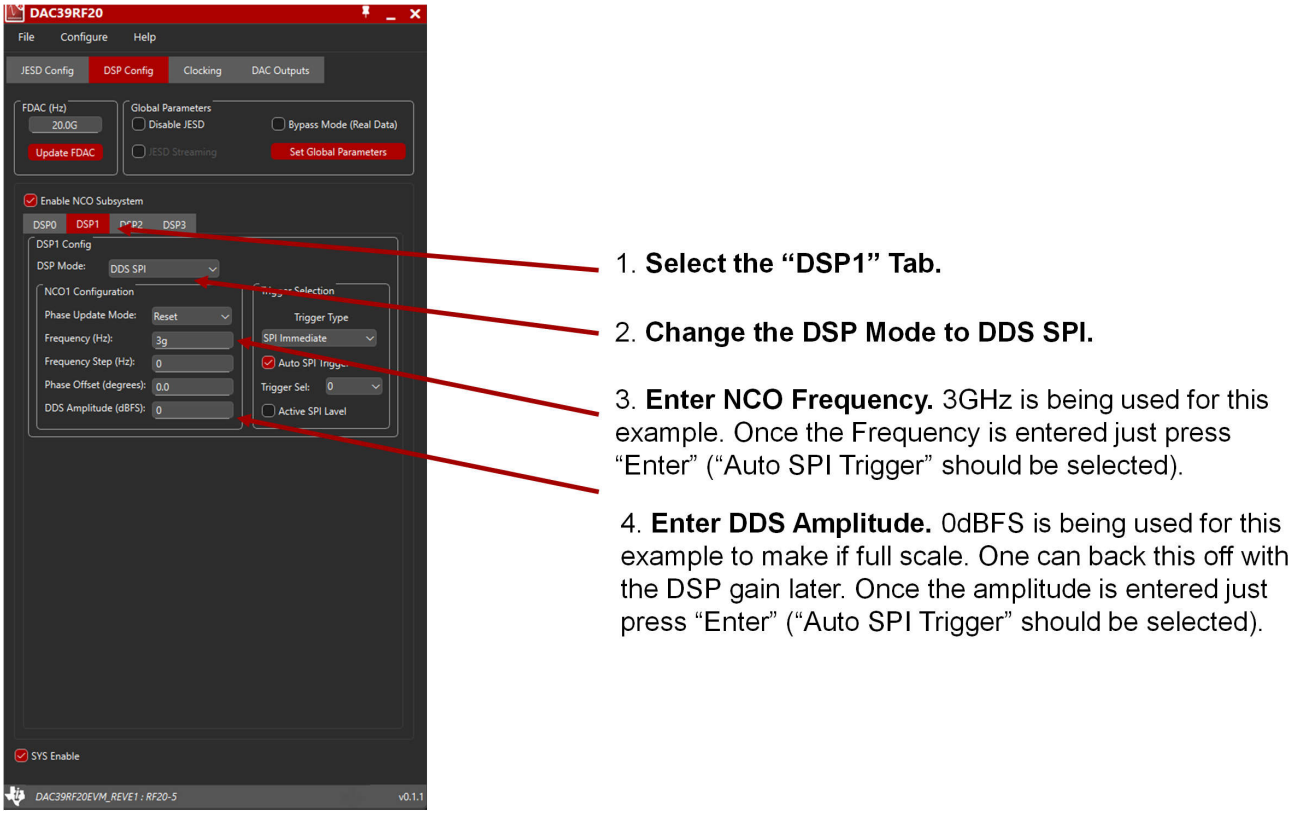


Figure 2-23. EVM GUI Configuration for JMode 1- Setup DSP Config Tab for NCO, Part 2

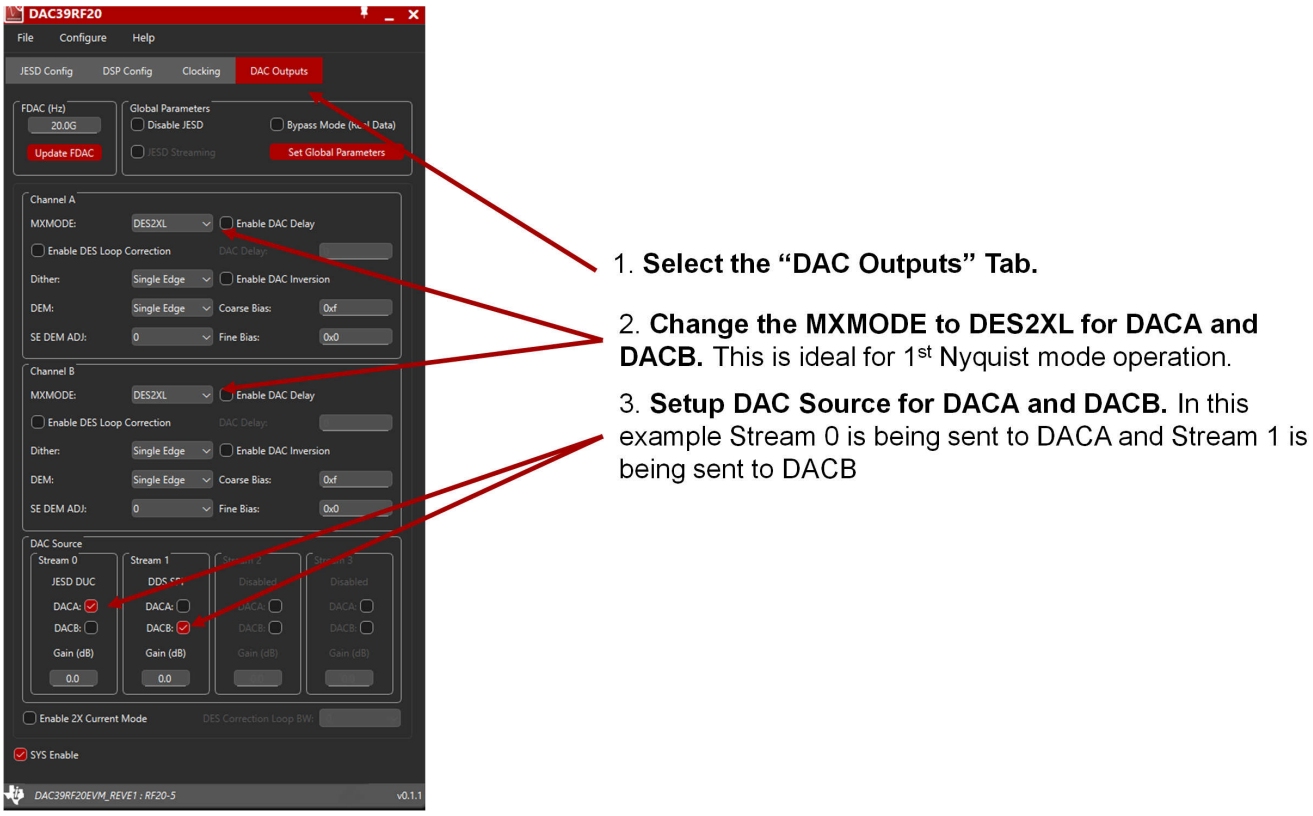


Figure 2-24. EVM GUI Configuration for JMode 1- Setup DAC Outputs Tab

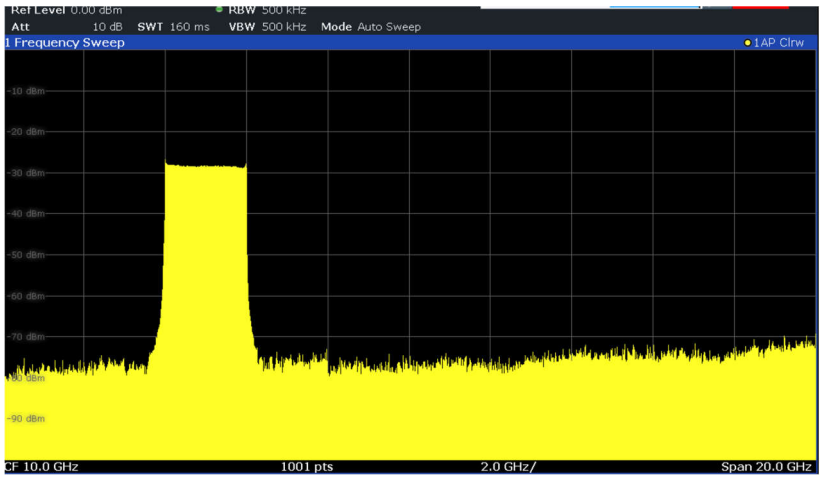


Figure 2-25. DAC Output CHA Spectrum, JMODE 1, Interpolate by 4 at 20GSPS

DACA is getting the modulated LFM chirp. A full 20GHz span is shown (two Nyquist zones). The second Nyquist image suppression is provided by DES2XL mode.

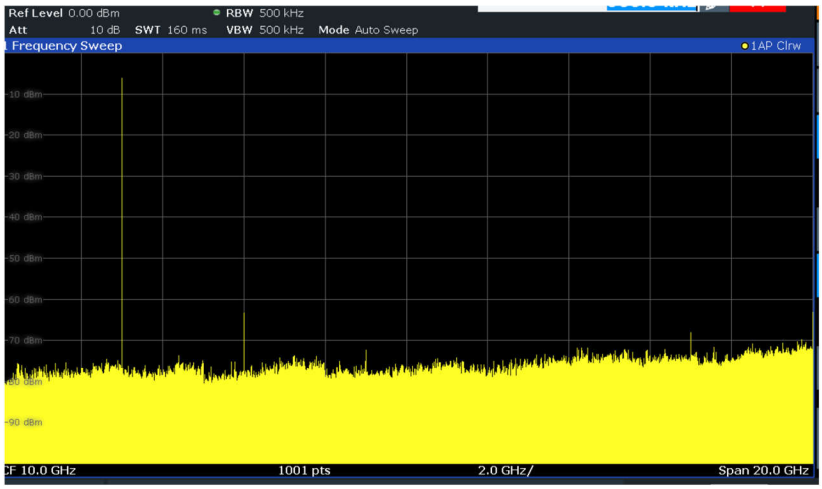
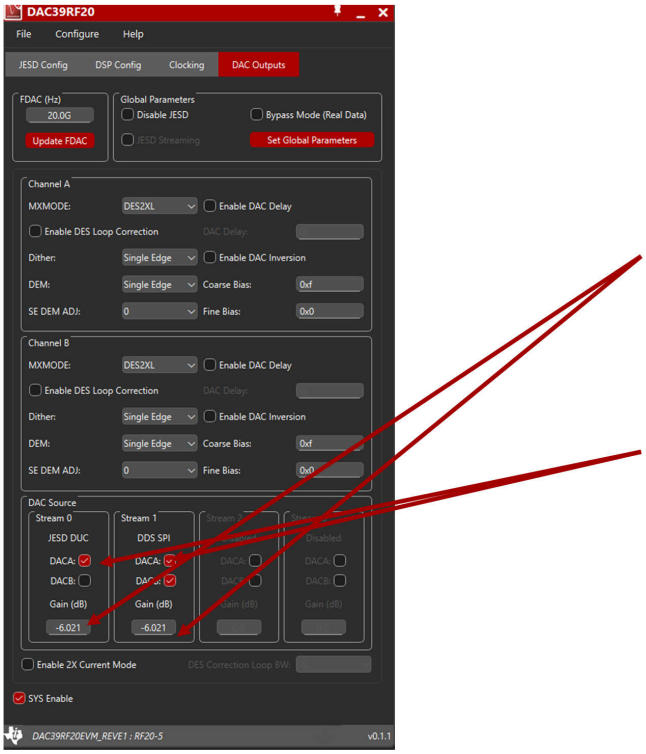


Figure 2-26. DAC Output CHB Spectrum, JMODE 1, Interpolate by 4 at 20GSPS

DACB is generating a sinlge 3GHz tone by DDS. A full 20GHz span is shown (two Nyquist zones). A second Nyquist image suppression is provided by DES2XL mode.



1. **Set each DSP Gain to ~-6dB.** Type in -6 and press "Enter" The GUI will find the closest value. Backing off by 6dB or greater will prevent oversaturation as two streams are being combined.

2. **Setup both streams to go to DACA.** Stream 1 is still going to DACB.

Figure 2-27. Example of DAC39RF20 GUI in JMODE 1 Placing Multiple Streams on a Single DAC Output

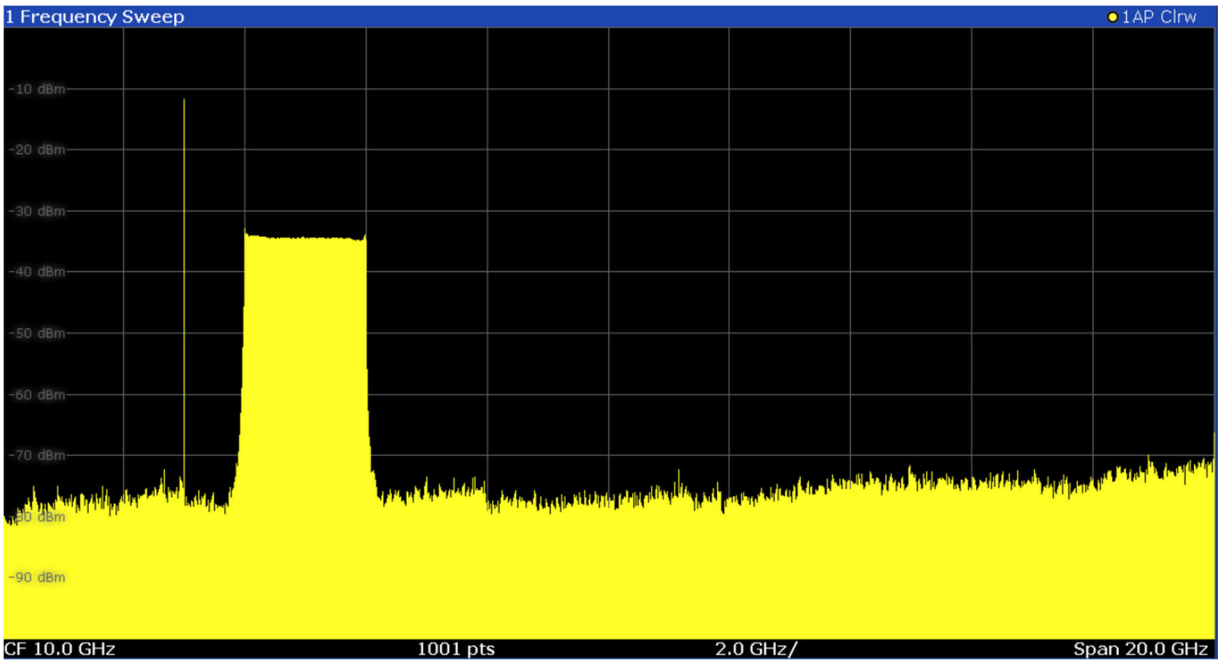


Figure 2-28. Example Spectrum of Both JMODE 1 Streams Sent to DACA Output

Both the single tone and the 2GHz modulated LFM are present on a single DACA output. All four streams can be mapped to either or both DACs when configured.

2.1.10 Configuration Example of DAC39RF20EVM in DDS Mode

1. Enable DDS ModeConfiguration details:
   a. 20GSPS
   b. No Reference clock is required for DDS mode
   c. No TSW14J59EVM is required for DDS mode

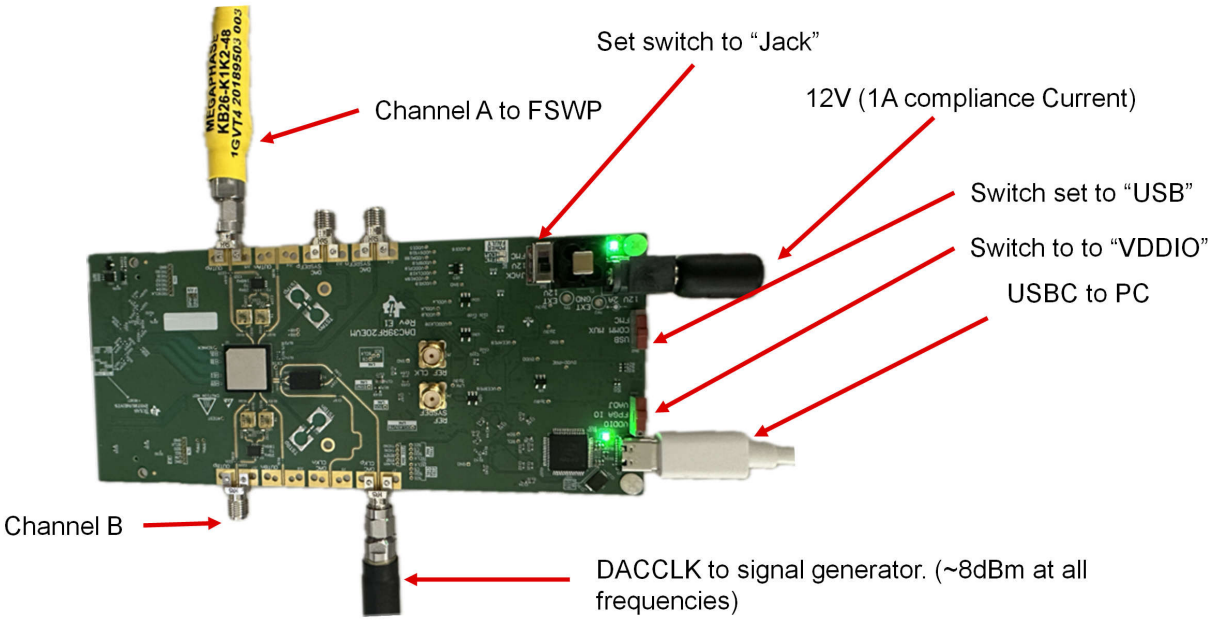


Figure 2-29. DAC EVM Setup in DDS Mode

2. Follow the steps in the figures below after launching the DAC GUI.

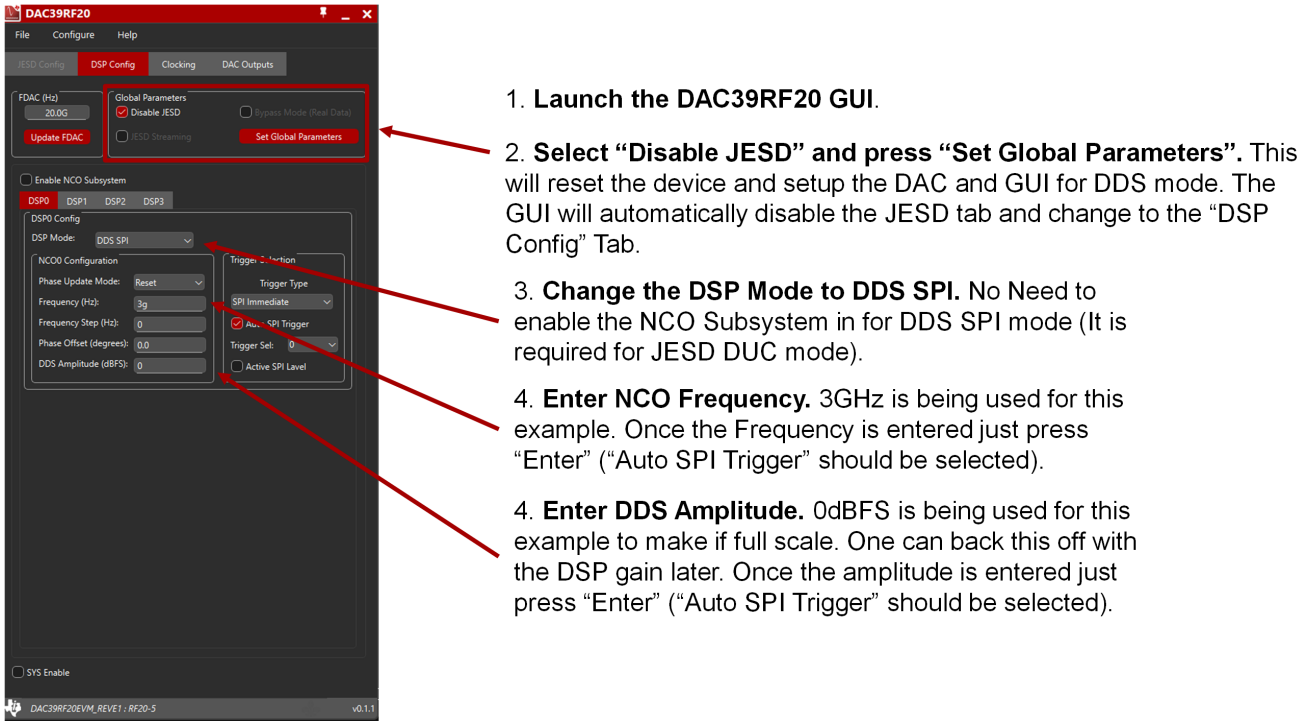
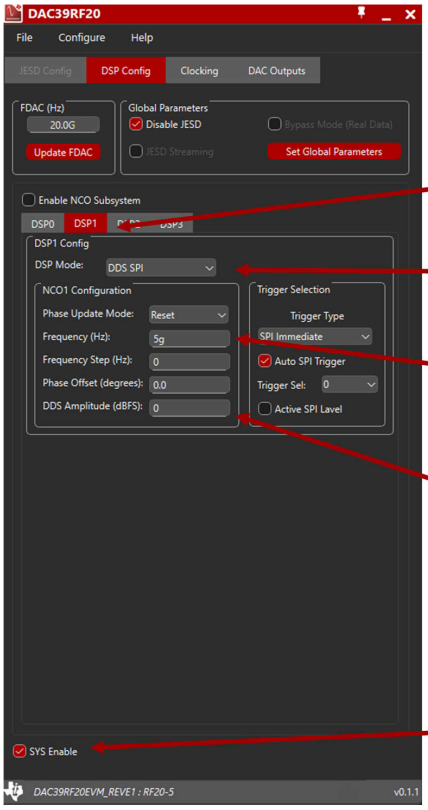


Figure 2-30. EVM GUI Configuration for DDS Mode - DSP Config Tab



1. **Select the “DSP1” Tab.**

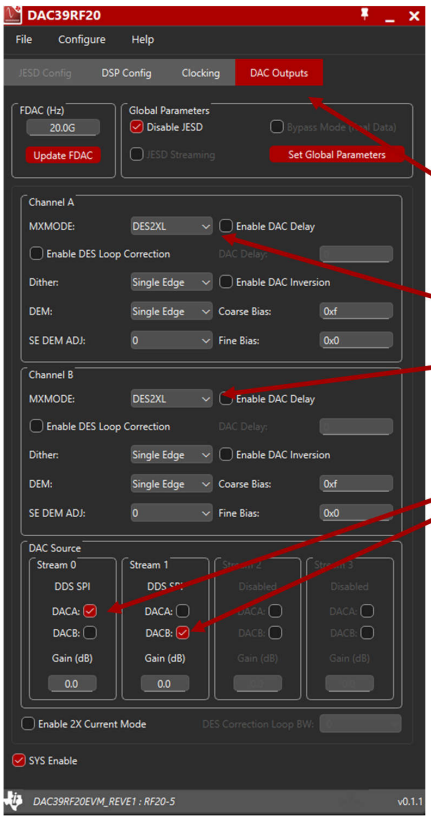
2. **Change the DSP Mode to DDS SPI.**

3. **Enter NCO Frequency.** 5GHz is being used for this example. Once the Frequency is entered just press “Enter” (“Auto SPI Trigger” should be selected).

4. **Enter DDS Amplitude.** 0dBFS is being used for this example to make if full scale. One can back this off with the DSP gain later. Once the amplitude is entered just press “Enter” (“Auto SPI Trigger” should be selected).

5. **Enable SYS_EN.** This can be done at anytime. The DAC API behind the scenes disables SYS_EN and re-enables it any time a device parameter is updated that needs SYS_EN turned off.

Figure 2-31. EVM GUI Configuration for DDS Mode - DSP Config Tab



1. **Select the “DAC Outputs” Tab.**

2. **Change the MXMODE to DES2XL for DACA and DACB.** This is ideal for 1st Nyquist mode operation.

3. **Setup DAC Source for DACA and DACB.** In this example Stream 0 is being sent to DACA and Stream 1 is being sent to DACB

Figure 2-32. EVM GUI Configuration for DDS Mode - DAC Outputs Tab

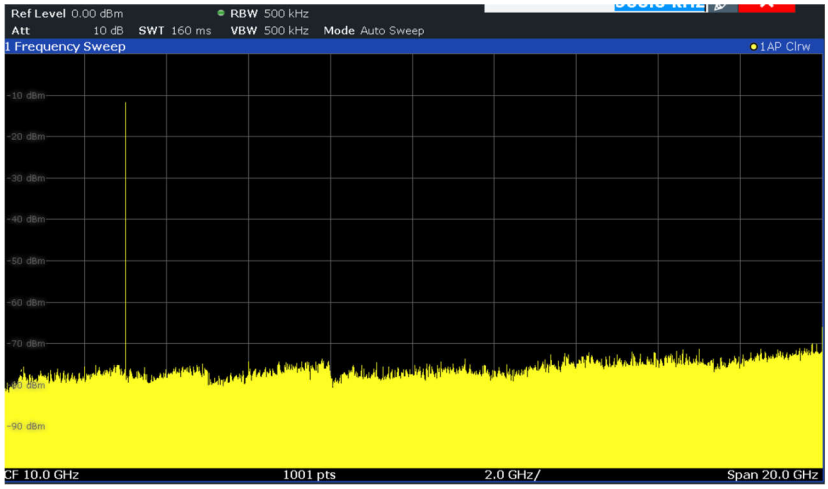


Figure 2-33. DACA Output Getting the DDS0 Stream

A full 20GHz span is shown (two Nyquist zones). A second Nyquist image suppression is provided by DES2XL mode.

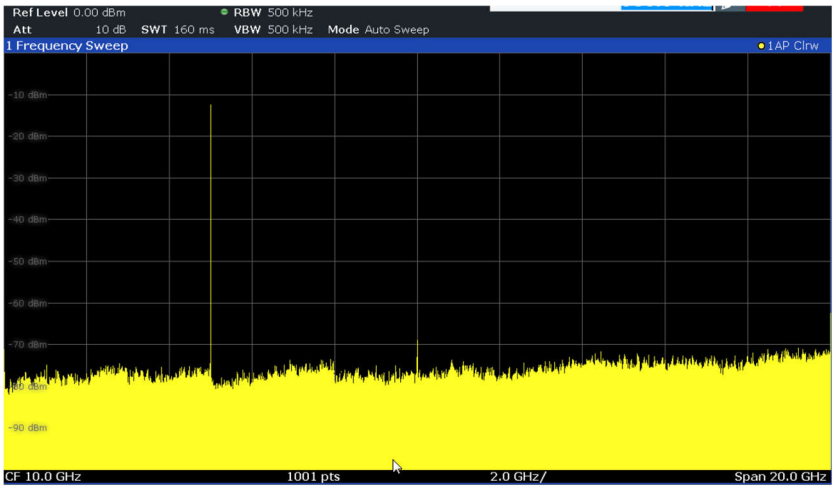
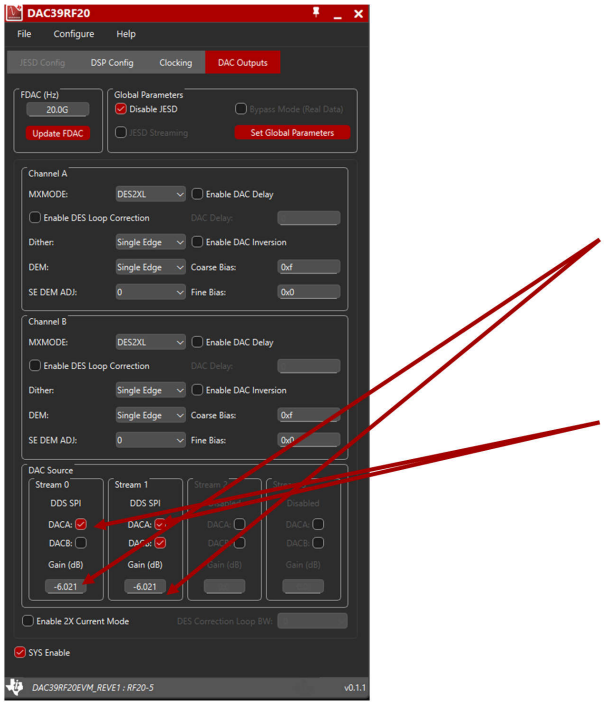


Figure 2-34. DACB Output Getting DDS1 Stream

A full 20GHz span is shown (two Nyquist zones). A second Nyquist image suppression is provided by DES2XL mode.

Update the DAC Outputs Tab as followed.



1. **Set each DSP Gain to ~-6dB.** Type in -6 and press "Enter" The GUI will find the closest value. Backing off by 6dB or greater will prevent oversaturation as two streams are being combined.

2. **Setup both streams to go to DACA.** Stream 1 is still going to DACB.

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Figure 2-35. Example of DAC39RF20 GUI Placing Multiple Streams on a Single DAC Output

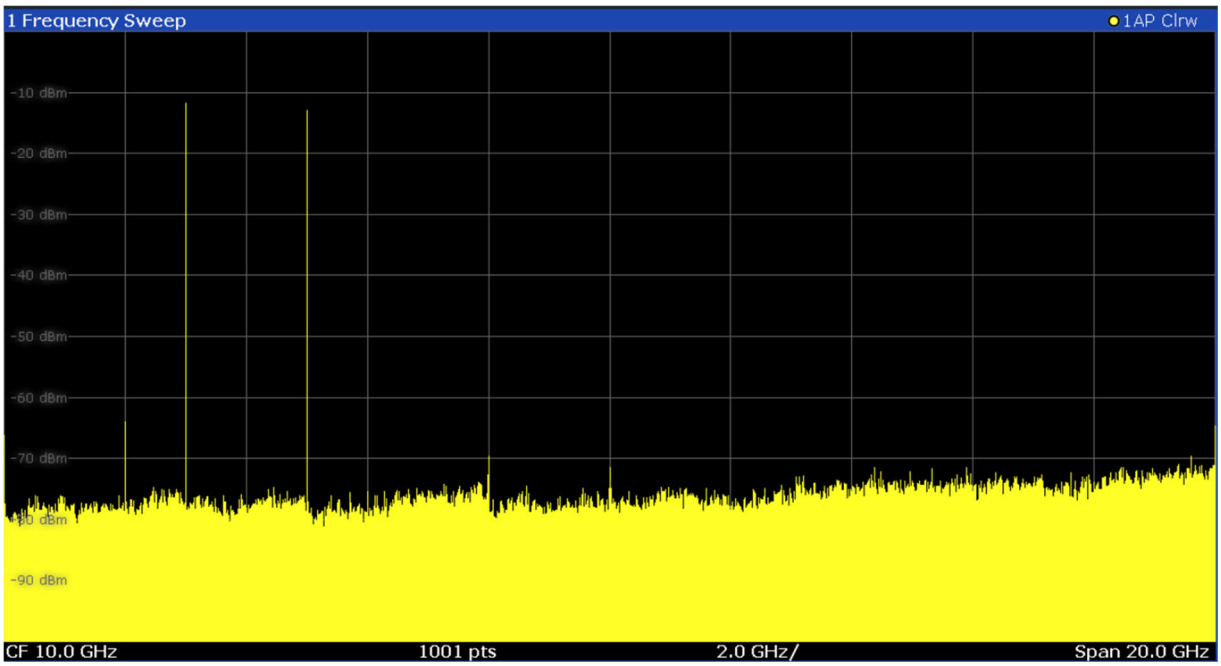


Figure 2-36. Example Spectrum of Both DDS Streams Sent to DACA Output

Note

All four streams can be mapped to either or both DACs when configured.

2.2 Evaluation Board Details: Analog Outputs

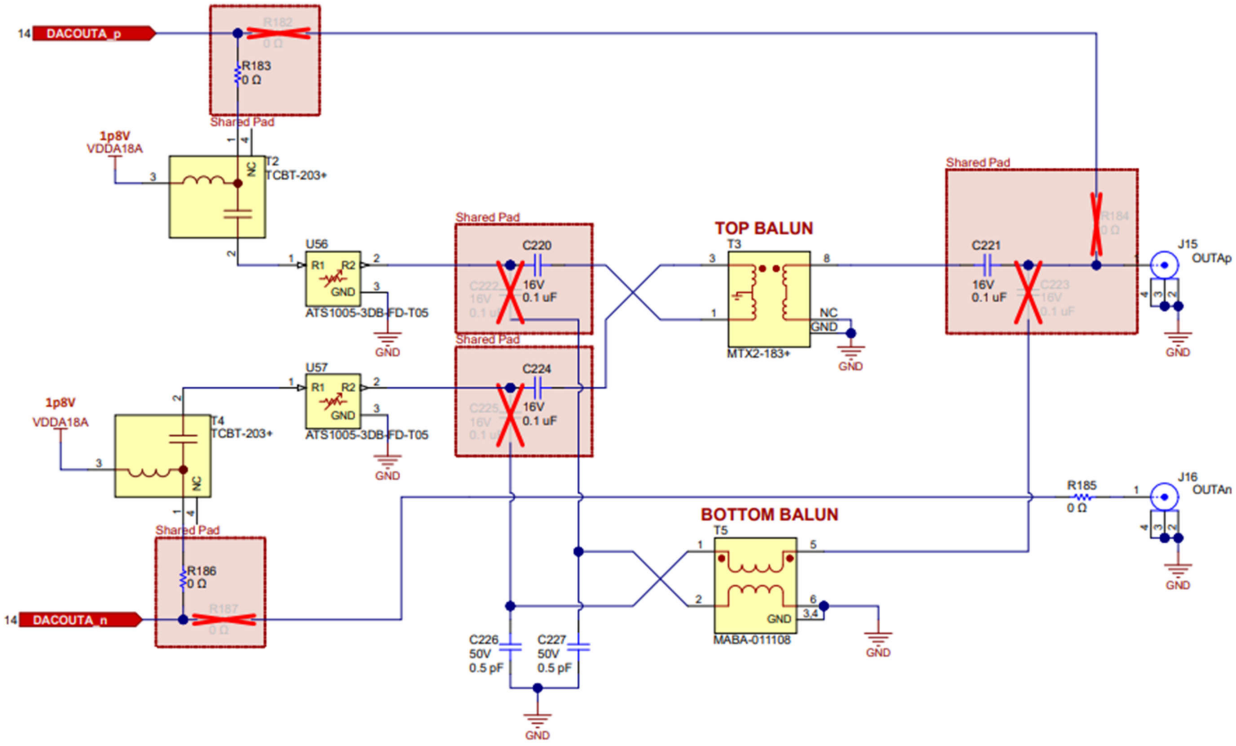
The analog output path can be configured for both a high frequency path (MTX2-183+ balun from mini-circuits) and low frequency path (MABA-011108 balun from Macom). The high frequency path is default on CHA and CHB, and the low frequency path requires some component modifications. See Table 2-2.

Each analog output path also has the ability to bypass both balun options entirely and allow the user to access the outputs differentially. To enable this feature, some components must be changed. See Table 2-3.

Table 2-2. Component Changes to Modify DAC EVM Output Paths

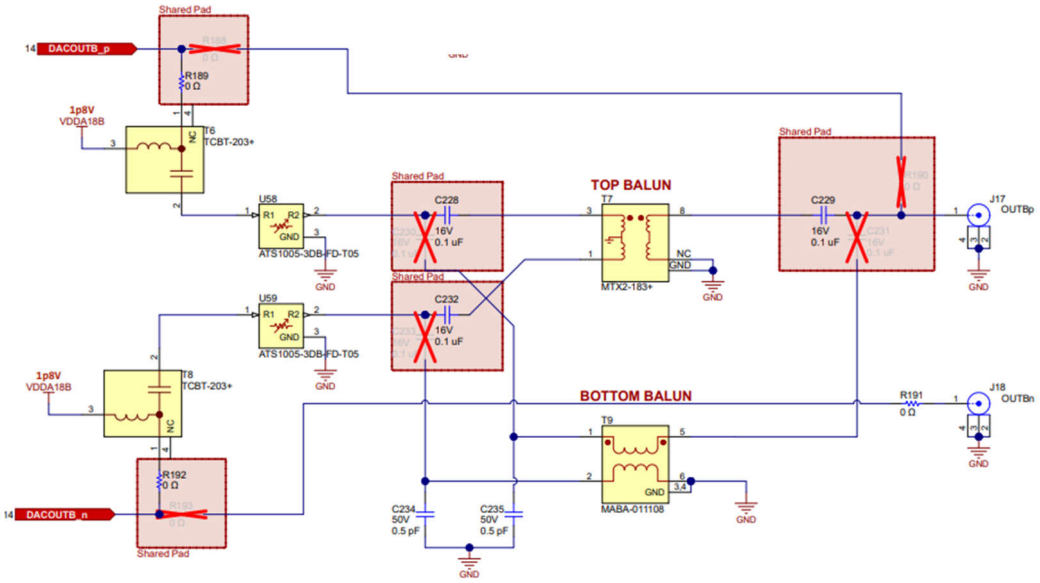
DAC Output Channel	Components to Remove	Components to Populate
CHA - Single-ended (MABA-011108)	C220, C224, C221	C222, C225, C223 = 0.1µF
CHA - Differential (balun bypass)	R183, R186	R182, R184, R187 = 0Ω
CHB - Single-ended (MABA-011108)	C228, C229, C232	C230, C231, C233 = 0.1µF
CHB - Differential (balun bypass)	R189, R192	R168, R190, R193 = 0Ω

Each analog output path has a wideband biasT on each output P/N pin to bias the outputs appropriately across the DAC supported bandwidth.



A. DACA output stage. By default, the MTX2-183+ balun is used for this channel (2GHz to 18GHz).

Figure 2-37. Analog Output Path - CHA



A. DACB output stage. By default, the MTX2-183+ balun is used for this channel (2GHz to 18GHz).

Figure 2-38. Analog Output Path - CHB

2.3 FMC Signal Routing

Table 2-3 provides the signal routing details for the DAC39RF20EVM.

All signal routing is handled by the DAC with the internal JESD crossbar feature.

This is also featured in the JESD crossbar dialogue box within the DAC39RF20EVM GUI.

Table 2-3. Signal Routing

DAC JESD Resource	Inverted	FMC Resource	FMC Pins	TSW14J59 FPGA Resource
Lane 9	Yes	DP0_C2M	C2, C3	Q224 MGTYTXN0
Lane 11	Yes	DP1_C2M	A22, A23	Q224 MGTYTXN1
Lane 15	Yes	DP2_C2M	A26, A27	Q224 MGTYTXN2
Lane 5	Yes	DP3_C2M	A30, A31	Q224 MGTYTXN3
Lane 3		DP4_C2M	A34, A35	Q225 MGTYTXN0
Lane 0	Yes	DP5_C2M	A38, A39	Q225 MGTYTXN1
Lane 1	Yes	DP6_C2M	B36, B37	Q225 MGTYTXN2
Lane 2	Yes	DP7_C2M	B32, B33	Q225 MGTYTXN3
Lane 7	Yes	DP8_C2M	B28, B29	Q226 MGTYTXN0
Lane 13	Yes	DP9_C2M	B24, B25	Q226 MGTYTXN1
Lane 12	Yes	DP10_C2M	Z24, Z25	Q226 MGTYTXN2
Lane 14	Yes	DP11_C2M	Y26, Y27	Q226 MGTYTXN3
Lane 6	Yes	DP12_C2M	Z28, Z29	Q227 MGTYTXN0
Lane 4	Yes	DP13_C2M	Y30, Y31	Q227 MGTYTXN1
Lane 10	Yes	DP20_C2M(1)	Z8, Z9	Q227 MGTYTXN2
Lane 8	Yes	DP21_C2M(1)	Y6, Y7	Q227 MGTYTXN3

(1) DP20_C2M and DP21_C2M can be rerouted to DP14_C2M and DP15_C2M to meet VITA compliance with other FPGA boards.

3 Hardware Design Files

The design files can be downloaded from the DAC39RF20EVM tools page on TI.com.

4 Additional Information

4.1 Trademarks

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NOTE:

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3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

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