EVM User's Guide: DRV81646EVM, DRV81646DGQEVM, DRV81545EVM, DRV81X4XEVM

DRV81X4X Evaluation Module

Description

The DRV81x4x evaluation module (EVM) allows for evaluation of the DRV81545, DRV81646, DRV81646DGQ and DRV81646DGQ-Q1 devices. The EVM has been programmed to work out of the box and begin driving loads right away. To simplify control and configuration, the EVM is accompanied by a graphical user interface (GUI) application.

Get Started

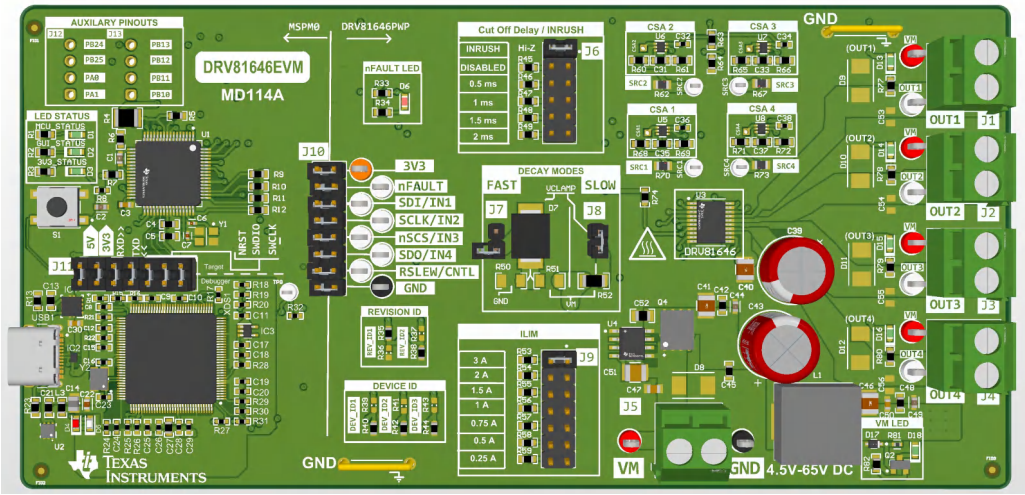
1. Order the EVM.
   a. DRV81545EVM
   b. DRV81646EVM
   c. DRV81646DGQEVM
      i. (Please utilize DRV81646DGQEVM to evaluate both DRV81646DGQ and DRV81646DGQ-Q1 devices.)
2. Use the web-based GUI.
3. Connect USB and external power supply.
4. Launch DRV81x4x-EVM-GUI and select the EVM variant on the home page.

Features

- Onboard 3.3V LDO for digital voltage supply
- XDS110 USB-based on-board emulator for ease of programming and debugging MSPM0 microcontroller
- Main signal header with removable shunts to disconnect main signals going to the load driver IC from the MCU
- GUI software to control EVM and DRV IC

Applications

- Brushed DC motor (BDC) motor drivers
- PLC
- Distributed I/O



DRV81646EVM

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1 Evaluation Module Overview

1.1 Introduction

The DRV81545, DRV81646, and DRV81646DGQ family of devices consist of low side switches with following features:

- DRV81545: 55V / 2A quad low side switches with integrated catch diodes, configurable current limit, configurable over-current cut-off duration and independent over-temperature and over-current protection.
- DRV81646: 65/ 4A quad low side switches with integrated catch diodes, configurable current limit, configurable over-current cut-off duration and independent over-temperature and over-current protection. The device also provides slew rate configuration and support inrush current times of up to 10ms for capacitive loads. The source terminals of each MOSFET are made available externally, enabling optional current sensing.
- DRV81646DGQ: 65/ 3A quad low side switches with integrated catch diodes, configurable current limit, configurable over-current cut-off duration and independent over-temperature and over-current protection. The device also provides slew rate configuration and support inrush current times of up to 10ms for capacitive loads. The source terminals of each MOSFET are made available externally, enabling optional current sensing.

This document is provided with the DRV81545, DRV81646, and DRV81646DGQ evaluation modules (EVM) as a supplement to the DRV81545, DRV81646, and DRV81646DGQ datasheets. This user's guide covers EVM hardware setup instructions, GUI installation, and usage instructions.

1.2 Kit Contents

Table 1-1 lists the contents of the EVM kit. Contact the nearest Texas Instruments Product Information Center if any component is missing.

Table 1-1. Kit Contents

ITEM	QUANTITY
One of DRV81545EVM, DRV81646EVM, DRV81646DGQEVM	1
3ft White USB-A to USB-C® Cable	1

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1.3 Specification

The DRV81x4x EVM connect to a local computer USB port through a USB-A to USB-C cable. An onboard XDS110 USB emulator allows for programming and debugging the main MSPM0 microcontroller without the need for an external debugger. A 3.3V LDO generates a 3.3V rail from the USB 5V supply. This 3.3V is used to power the XDS110 MCU, main MSPM0, and status LEDs. The J10 signal header uses removable shunts to pass the signals from the MCU to the load driver. Remove any of these shunts to easily jump in the control signals to the driver. Provide an external power supply to the J5 screw terminal within the operating range of the device. DRV81545 supports 4.5V to 55V supply voltage range, while DRV81646, and DRV81646DGQ support 4.5 to 65V.

1.4 Device Information

The DRV81545, DRV81646, and DRV81646DGQ provide four low side switches with integrated catch diodes and external TVS/Zener for flexible decay as alternate current path for inductive loads during switch turnoff. Each channel is protected against over current by means of a configurable current limit that can be set externally using appropriate resistor on the ILIM pin. Each channel further also has their own over-temperature protection. The Channels additionally have a cut-off duration setting that limits the persistence of a current limit condition on the respective channel to a duration configurable by setting resistor on COD pin. Also, Faults are indicated by a fault output pin (nFAULT).

The documents in Table 1-2 provide information regarding Texas Instruments integrated circuits used in the assembly of the EVM. This user's guide is available from the TI web site under literature number SLVUDI9. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions are available from the TI web site at www.ti.com, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 1-2. Related Device Documentation

Description	Data Sheet
XDS110 MCU	MSP432E401Y
Main MSPM0 MCU	MSPM0G3507
Quad Low-Side Switches	DRV81545, DRV81646, DRV81646DGQ

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2 Hardware

2.1 Headers and Test Points Information

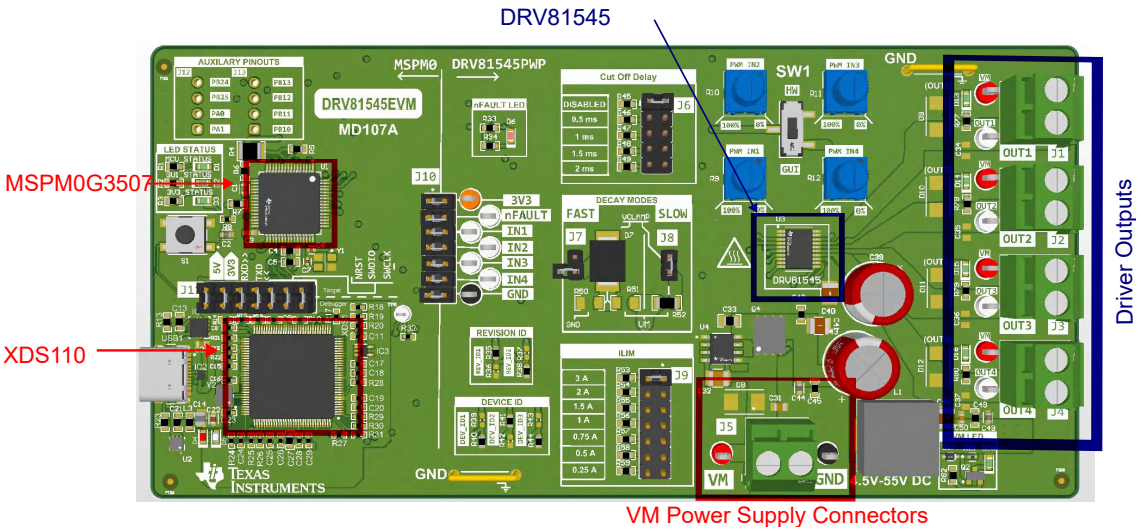


Figure 2-1. DRV81545EVM (MD0107-001) Top View

CAUTION

Hot surface temperature. The EVM can have high surface temperatures marked by the FIRE triangular symbol on the EVM. Avoid touching the marked hot surface area when driving high currents to prevent potential burn damage.

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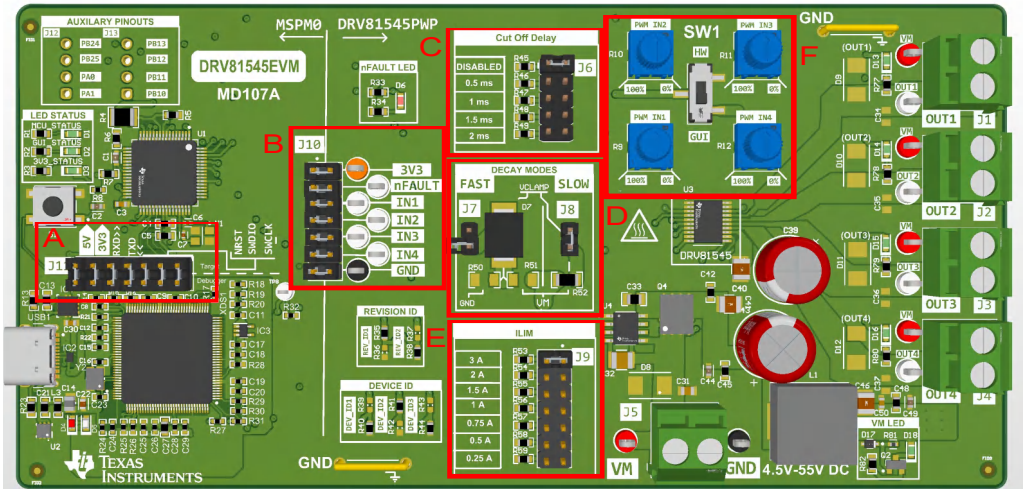


Figure 2-2. DRV81545EVM Header and Test Point Information

Table 2-1. Header and Test Point Description - DRV81545EVM

Component label	Description
A	XDS110 header between MSP432E401Y and MSPM0G3507
B	Main signal header: • **3V3**: 3.3V from LDO. • **GND**: GND test point. • **IN1**: Channel 1 input. • **IN2**: Channel 2 input. • **IN3**: Channel 3 input. • **IN4**: Channel 4 input.
C	Cut-off duration (COD) configuration limits the duration of a current-limiting condition on the respective channel. tCOD can be chosen by setting appropriate pulled down resistors on COD pin. **Do not leave this header unconnected**. **Change the setting when device is powered off.** • **Disabled**: COD is disabled by a 10kΩ pulled down resistor. Output stage and IC are protected by thermal shutdown only. • **0.5ms**: COD pin is pulled down through 60kΩ to GND. The device lasts in current limit condition for 0.5ms. Retries only after an interval of 16ms typical. • **1ms**: COD pin is pulled down through 120kΩ to GND. The device lasts in current limit condition for 1ms. Retries only after an interval of 32ms typical. • **1.5ms**: COD pin is pulled down through 180kΩ to GND. The device lasts in current limit condition for 1.5ms. Retries only after an interval of 48ms typical. • **2ms**: COD pin is pulled down through 240kΩ to GND. The device lasts in current limit condition for 2ms. Retries only after an interval of 64ms typical.

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Table 2-1. Header and Test Point Description - DRV81545EVM (continued)

Component label	Description
D	VCLAMP pin settings can be controlled by connecting to VM or external TVS diode to VM or GND to control different decay modes. Adjusting one setting at a time is essential, maintaining that the corresponding resistor connection is made correctly. **CAUTION** Never populate both R50 and R51 simultaneously, as this creates a short circuit between VM and GND, potentially damaging the device. Additionally, maintaining that the header is not left unconnected and verify that the related resistor is correctly populated. To avoid any issues, make these changes only when the device is powered off. The available decay modes are: • **SLOW**: Slow Decay mode, where VCLAMP is tied to VM (populate R52 and short J8) • **FAST**: Fast Decay mode, which can be configured in two ways: – TVS/Zener VCLAMP to GND (populate R50 and short J7) – TVS/Zener VCLAMP to VM (populate R51 and short J7)
E	Configure the current limit using appropriate pulled down resistor on ILIM pin. **Do not leave this header unconnected**. **Change the setting when device is powered off.** • **3 A:** ILIM pin is pulled down through 10kΩ to GND. Limits the current to 3A typical. • **2 A:** ILIM pin is pulled down through 30kΩ to GND. Limits the current to 2A typical. • **1.5 A:** ILIM pin is pulled down through 45kΩ to GND. Limits the current to 1.5A typical. • **1 A:** ILIM pin is pulled down through 60kΩ to GND. Limits the current to 1A typical. • **0.75 A:** ILIM is pulled down through 80kΩ to GND. Limits the current to 0.75A typical. • **0.5 A:** ILIM pin is pulled down through 120kΩ to GND. Limits the current to 0.5A typical. • **0.25 A:** ILIM is pulled down through 240kΩ to GND. Limits the current to 0.25A typical.
F	The GUI/HW switch allows user to control the driver by either on board potentiometers or web-based GUI controls. • **GUI/HW**: Hardware based or GUI based control switch. For using web-based GUI, make sure the switch is on GUI mode. • **PWM IN1**: Controls the PWM duty cycle of Channel 1 when switch is at HW mode. • **PWM IN2:** Controls the PWM duty cycle of Channel 2 when switch is at HW mode. • **PWM IN3**: Controls the PWM duty cycle of Channel 3 when switch is at HW mode. • **PWM IN4**: Controls the PWM duty cycle of Channel 4 when switch is at HW mode. **Note: Under HW mode, the PWM frequency is set at 20kHz.**

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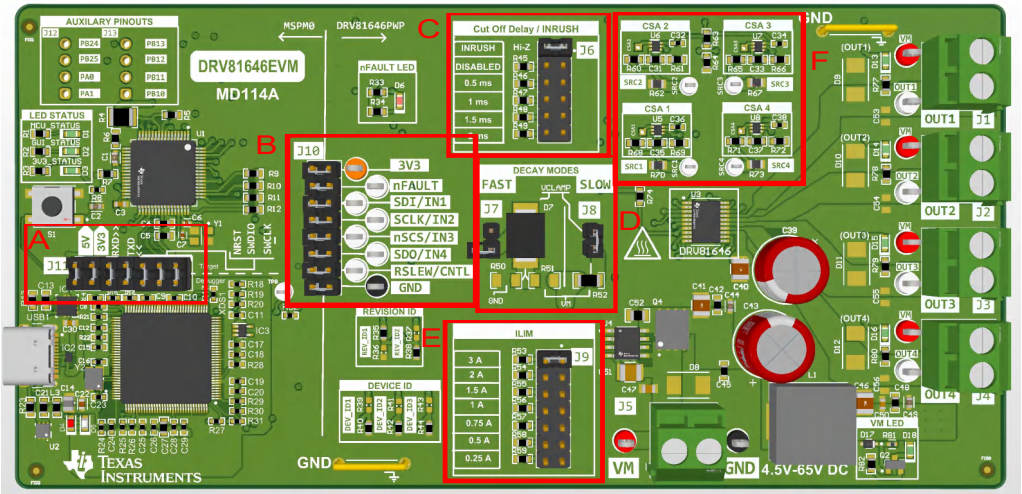


Figure 2-3. DRV81646EVM, and DRV81646DGQEVM Header and Test Point Information

Table 2-2. DRV81646EVM, and DRV1646DGQEVM

Component Label	Description
A	XDS110 header between MSP432E401Y and MSPM0G3507
B	Main signal header: • **3V3**: 3.3V from LDO • **SDI/IN1**: SPI SDI / HW interface channel 1 input. • **SCLK/IN2**: SPI SCLK / HW interface channel 2 input. • **nSCS/IN3**: SPI nSCS / HW interface channel 3 input. • **SDO/IN4**: SPI SDO / HW interface channel 3 input. • **RSLEW/CNT**: Slew rate and control interface (SPI / HW) • **GND**: GND test point.
C	Cut-off duration (COD) configuration limits the duration of a current-limiting condition on the respective channel. tCOD can be chosen by setting appropriate pulled down resistors on COD pin. **Change the setting when device is powered off.** • **INRUSH**: Leave COD pin unconnected (Hi-Z) to boost the current limit for capacitive loads up to 10ms. • **Disabled**: COD is disabled by a 10kΩ pulled down resistor. Output stage and IC are protected by thermal shutdown only. • **0.5ms**: COD pin is pulled down through 60kΩ to GND. The device lasts in current limit condition for 0.5ms. Retries only after an interval of 16ms typical. • **1ms**: COD pin is pulled down through 120kΩ to GND. The device lasts in current limit condition for 1ms. Retries only after an interval of 32ms typical. • **1.5ms**: COD pin is pulled down through 180kΩ to GND. The device lasts in current limit condition for 1.5ms. Retries only after an interval of 48ms typical. • **2ms**: COD pin is pulled down through 240kΩ to GND. The device lasts in current limit condition for 2ms. Retries only after an interval of 64ms typical

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Table 2-2. DRV81646EVM, and DRV1646DGQEVM (continued)

Component Label	Description
D	VCLAMP pin settings can be controlled by connecting to VM or external TVS diode to VM or GND to control different decay modes. Adjusting one setting at a time is essential, maintaining that the corresponding resistor connection is made correctly. **CAUTION** Never populate both R50 and R51 simultaneously, as this create a short circuit between VM and GND, potentially damaging the device. Additionally, maintain that the header is not left unconnected and verify that the related resistor is correctly populated. To avoid any issues, make these changes only when the device is powered off The available decay modes are: • **SLOW**: Slow Decay mode, where VCLAMP is tied to VM (populate R52 and short J8) • **FAST**: Fast Decay mode, which can be configured in two ways: – TVS/Zener VCLAMP to GND (populate R50 and short J7) – DTVS/Zener VCLAMP to VM (populate R51 and short J7)
E	Configure the current limit using appropriate pulled down resistor on ILIM pin. **Do not leave this header unconnected**. **Change the setting when device is powered off.** • **3 A:** ILIM pin is pulled down through 10kΩ to GND. Limits the current to 3A typical. • **2 A:** ILIM pin is pulled down through 30kΩ to GND. Limits the current to 2A typical. • **1.5 A:** ILIM pin is pulled down through 45kΩ to GND. Limits the current to 1.5A typical. • **1 A:** ILIM pin is pulled down through 60kΩ to GND. Limits the current to 1A typical. • **0.75 A:** ILIM is pulled down through 80kΩ to GND. Limits the current to 0.75A typical. • **0.5 A:** ILIM pin is pulled down through 120kΩ to GND. Limits the current to 0.5A typical. • **0.25 A:** ILIM is pulled down through 240kΩ to GND. Limits the current to 0.25A typical
F	The SRCs pins are connected to a 10mΩ sense resistor (R62, R67, R70, and R73), enabling the measurement of load current. The current from each channel is sourced by CSA1 to CSA4 and then amplified by the INA185A2IDRL ICs. The amplified current is subsequently sent to the MCU's ADC for further analysis. For diagnostic and testing purposes, the following test points are available: **CSA1:** SRC1 test point access to raw SRC1 output before amplification. CSA1 test point shows amplified current for channel one, facilitating debugging and analysis. **CSA2:** SRC2 test point access to raw SRC2 output before amplification. CSA2 test point shows amplified current for channel one, facilitating debugging and analysis. **CSA3:** SRC3 test point access to raw SRC3 output before amplification. CSA3 test point shows amplified current for channel one, facilitating debugging and analysis. **CSA4:** SRC4 test point access to raw SRC4 output before amplification. CSA4 test point shows amplified current for channel one, facilitating debugging and analysis

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2.2 Connector Information

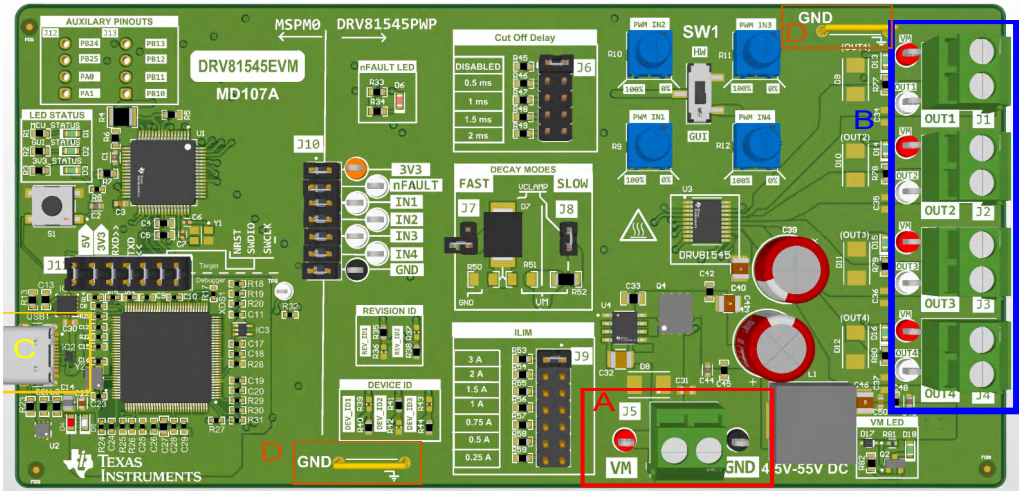


Figure 2-4. DRV81X4X EVMs Connectors

Table 2-3. Connectors Description

Component label	Description
A	Input power supply connector. Power cables can be directly connected to the screw terminals or clipped to the test points on either side of the connector.
B	High-side driver output connectors.
C	USB connector.
D	Ground strap can be used as ground for probes and other connectors.

2.3 Indicator LEDs

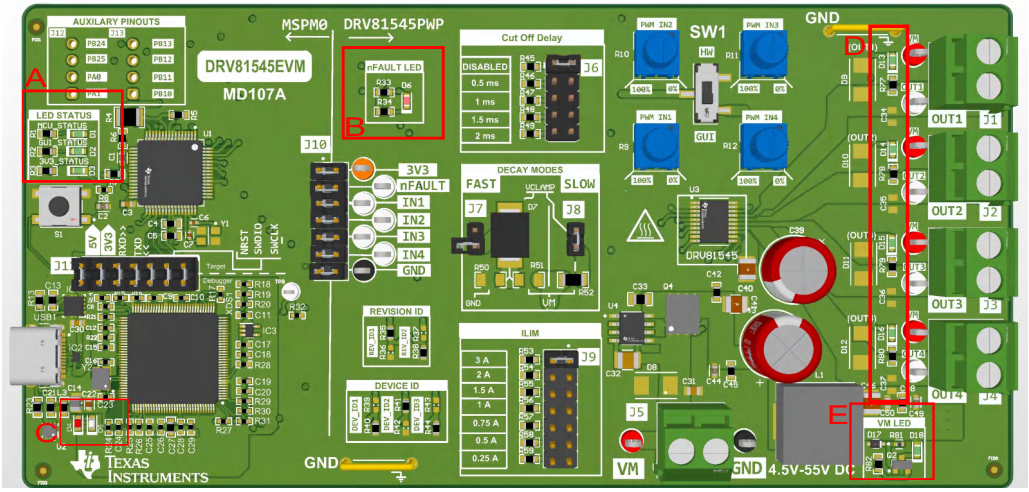


Figure 2-5. DRV81X4X EVMs Indicator LEDs

LED	Function
A/D1	**MCU_STATUS:** LED toggles at a rate of around 1s when MCU is active. Unplug and reconnect the EVM to the computer if this stops flashing.
A/D2	**GUI_STATUS: OFF** EVM is not connected to GUI. **ON** EVM is connected to GUI.
A/D3	**3V3 STATUS: OFF** when 3.3V is not active. **ON** when 3.3V is active.
B/D6	**nFAULT LED: OFF** Device operates normally. **ON** overtemperature, overcurrent protection triggered.

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LED	Function
C/D4,D5	**XDS110 LED: OFF** XDS110 is not connected. **ON** when XDS110 is connected.
D/D13-D16	**OUTx LED: OFF** When the OUTx is OFF. **ON** When OUTx is ON.
E/D18	**VM LED: OFF** when VM is not provided. **ON** when VM is provided

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2.4 Hardware Setup

The EVM hardware is designed and kitted to simplify setup and begin driving loads. The EVM comes with the jumpers placed at the appropriate location in the headers. The description of the jumpers, also called shunts, are exlained in Table 2-1 and Table 2-2.

Note

- The DRV81545EVM can function with or without GUI software. To maintain proper operation, please verify that the SW1 switch (GUI/HW) is set to the correct state.
- Confirm that the shunts on connectors J6 through J11 are properly configured

Before connecting the EVM to the GUI software, follow these steps:

1. Connect EVM to PC via USB connector. LED D5 (XDS110), and LED D3 (3.3V), must be solid ON. LED D1 (MCU STATUS) needs to be toggling ON/OFF at a 1s intervals.
2. Connect power supply (less than 55V for DRV81545, less than 65V for DRV81646 / DRV81646DGQ) to power connector.
3. Turn ON power supply. LED D18 (VM) turns ON. See Figure 2-6 for setup image. The EVM is designed with built-in reverse polarity protection to prevent damage from incorrect power supply connections. If the LED D18 indicator fails to illuminate, maintain that the power supply polarity connection is correctly configured.
4. Connect load to the appropriate output connector.
5. Set up is now complete. See Figure 2-6 for setup image.

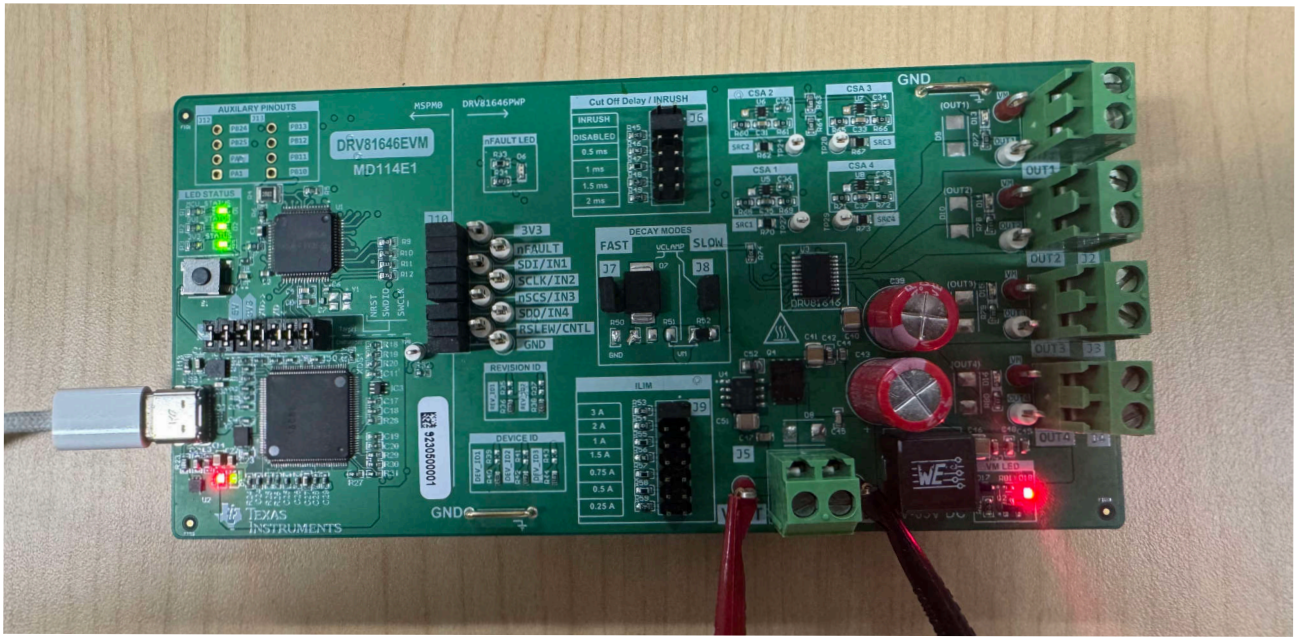


Figure 2-6. Hardware Setup

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3 Software

3.1 Web GUI Access or Local GUI Installation

The EVM is controlled via a GUI application and can be used via a chrome-based browser or installed locally to a PC. Download the latest GUI installer here or use web-based GUI here.

To use the Web GUI (recommended), follow these steps:

1. Open the latest version of the GUI at this link: https://dev.ti.com/gallery/view/MotorDriversBSM/DRV1x4x-EVM-GUI/
   a. Alternatively, log into https://dev.ti.com/gallery/ and search for *DRV81x4x* sorting by *Recently updated*.
   b. Click on the title or blank space of the first search result to open the Web-Based GUI.

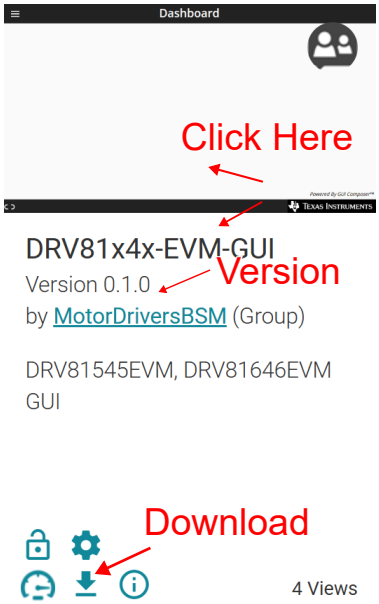


Figure 3-1. TI GUI Composer Gallery Results for Launching or Downloading Local Installer

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To install the GUI locally follow these steps:

1. Log in to https://dev.ti.com/gallery/ using myTI log in credentials. Note that the GUI composer log in searches for a very specific username match including case input at the time of sign up.
2. Open the latest version of the GUI at this link: https://dev.ti.com/gallery/info/MotorDriversBSM/DRV81x4x-EVM-GUI/
   a. Alternatively, search for *DRV81x4x* sorting by *Recently updated*.
3. Hover the mouse over the *Download* icon and select the installer for the relevant operating system from the top list. Refer back to the previous section for a visual depiction of the gallery page.
4. Extract the ZIP folder with the installer and run the installer. The installer contents is self-explanatory and look slightly different for each OS.
5. Click *Next* and then agree to the terms and conditions on the following page.
6. Keep the application and runtime directory to the default locations. Click *Next* to install GUI.
7. Select *Download from Web* to download the GUI Composer Runtime if prompted, then click *Next*.
   a. If a network firewall prevents Runtime download from the web, then the Runtime installer can be downloaded here.
8. Check the box to create a desktop shortcut and click *Finish* to complete installation.
9. GUI is now installed.

3.2 Connecting EVM to GUI

Now that the EVM hardware setup and GUI installation is complete, the EVM can now be connected to the GUI. The following steps outline how to connect the EVM to GUI:

1. With the EVM connected to the PC, open the GUI. The home page is shown in Figure 3-2.

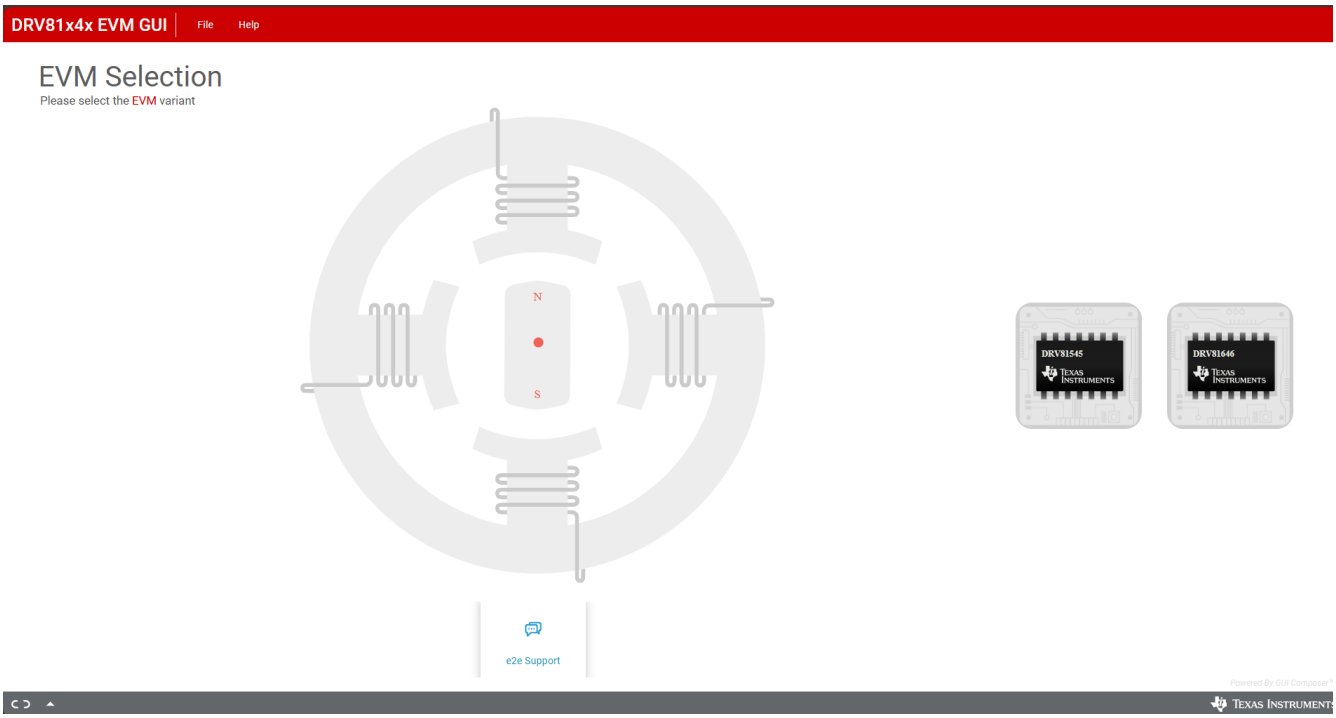


Figure 3-2. GUI Landing Page

2. Program EVM with latest software by clicking on *File -> Program Device*. (See Figure 3-3).

   This needs to be done the first time the user sets up the EVM, as a software update can have been released since the EVM was initially programmed.

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Figure 3-3. Program Device

3. Select the appropriate GUI variant from the two options for the EVM (Figure 3-3).

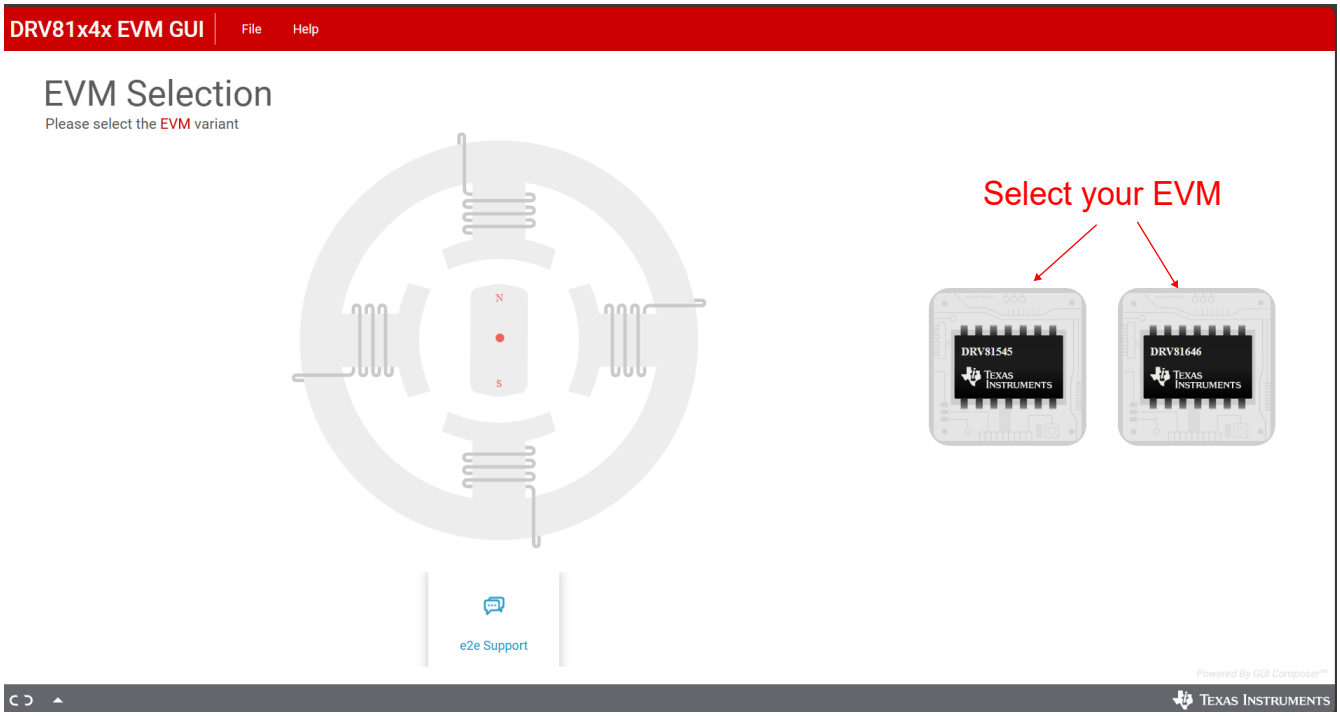


Figure 3-4. Select EVM Variant

4. The GUI attempts to connect with EVM. The GUI displays the following once successfully connected. If there is no successful connection, then double check hardware setup is correct following steps in Section 2.4.

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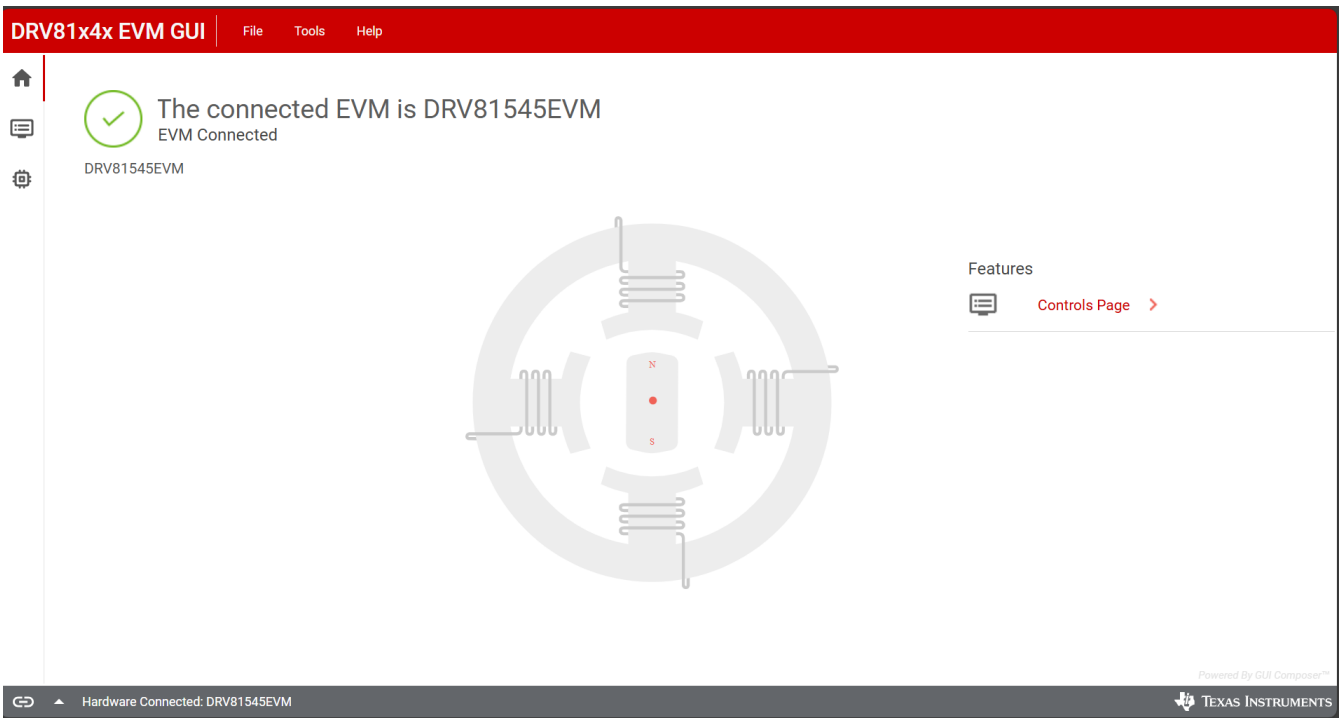


Figure 3-5. Successful GUI connection

5. Once successfully connected, click on Control Page to open the Channel Config. Page.
6. The GUI setup is now complete. The following section provides an overview of the GUI and how to use the GUI to control EVM.

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3.3 GUI Overview

These following sections provides an overview for each of the GUI variants, such as DRV81545EVM versus DRV81646EVM. The GUI variant is selected in the GUI home page.

3.4 DRV81545 GUI

Figure 3-6 provides the overview of all the widgets and features of the DRV81545EVM GUI.



Figure 3-6. DRV81545EVM GUI Driver Control Page

Table 3-1. DRV81545EVM GUI Overview

Component label	Description
A	Block Diagram of DRV81545.
B	OUT1 Channel control parameters. • **IN1 Duty Cycle**: The IN1 PWM duty cycle is adjustable from 0% to 100%. • **IN1 Frequency**: The IN1 PWM frequency can be varied between 0 Hz and 250 kHz, with selectable units (Hz or kHz). • **IN1 Ramp Rate**: ItControls the rate of duty cycle increment. • **OUT1 Enable/Disable:** This toggle switch governs the application of the IN1 PWM signal. – **Enabled**: The IN1 PWM signal is applied to the IN1 pin. – **Disabled**: The IN1 PWM signal is not applied to the IN1 pin.
C	• **Device**: Device name • **Firmware Version**: EVM firmware version • **VM voltage**: supply voltage value
D	• **nFAULT Pin Status**: – **Green**: Indicates normal operation with no active fault conditions. – **Red**: : Indicates that either over-current or over-temperature protection has been activated for one or more channels.

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3.5 DRV81646 GUI

The DRV81646 GUI is utilized in both the DRV81646EVM and DRV81646DGQEVM. The accompanying GUI software supports interaction with the device via both Hardware interface and SPI. The DRV81646 GUI features two primary pages: the Hardware interface page and the SPI page. The Hardware interface page enables control of the device through input PWM, allowing for intuitive management of device settings. The nFAULT LED serves as a visual indicator, signaling that either over-current or over-temperature protection has been triggered for one or more channels. In contrast, the SPI page offers ON/OFF control through the transmission of SPI commands, as well as detailed fault information for each channel, providing a more general understanding of device performance and allowing for targeted troubleshooting.

Figure 3-7 below shows the Load Control Panel under the Hardware mode with the main sections enclosed in red boxes with a letter assigned.

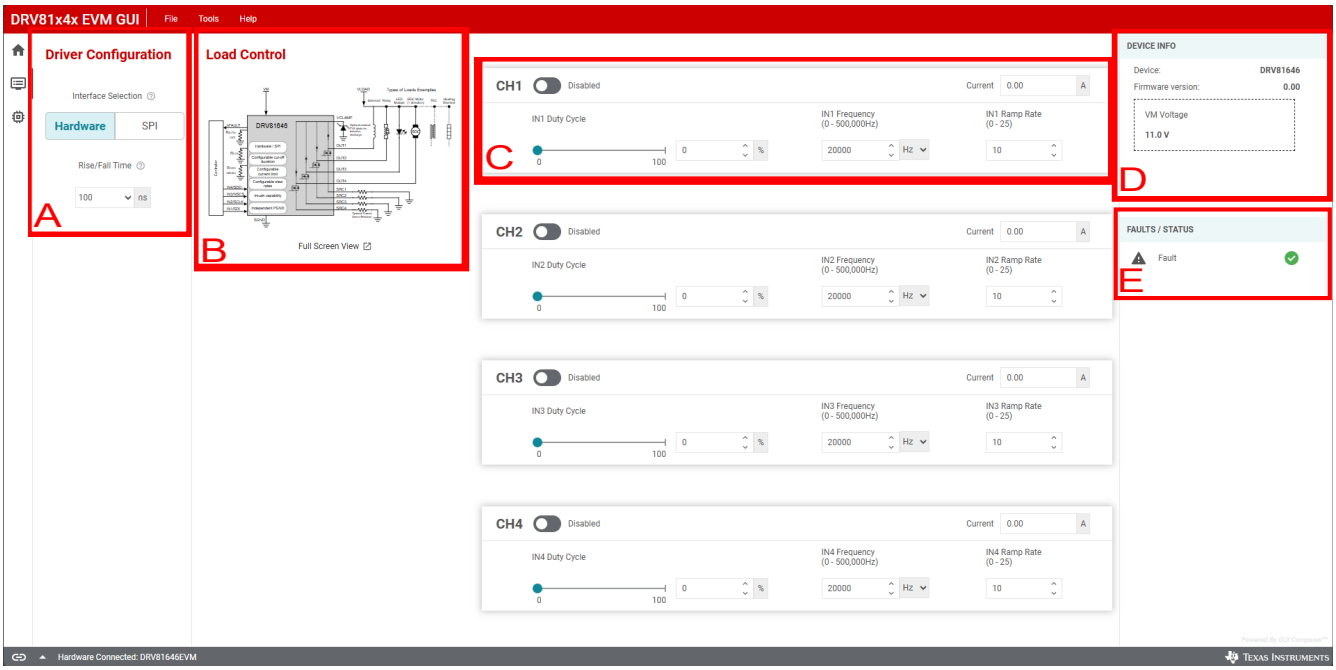


Figure 3-7. DRV81646EVM Driver Control Panel Hardware Interface

Table 3-2. DRV81646 GUI Hardware Interface Overview

Component label	Description
A	**Driver Configuration** Interface Selection: The device offers two interface options: Hardware and SPI. • **Hardware Interface**: Under this configuration, channels are controlled using PWM input. The interface is selected by connecting an appropriate resistor to the RSLEW/CNT pin through the MCU. • **SPI**: The SPI controls the outputs through SPI commands, which are executed by setting the control register bits. **To switch between the Hardware and SPI, powering down the device is essential, before changing the interface, and then powering up.** • **Rise/Fall Time**: This setting configures the output slew rate by connecting an appropriate resistor to the RSLEW/CNT pin. **Note that power cycling is required to apply changes to the slew rate**
B	Block Diagram of DRV81646.

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Table 3-2. DRV81646 GUI Hardware Interface Overview (continued)

Component label	Description
C	OUT1 Channel control parameters. • **IN1 Duty Cycle**: The IN1 PWM duty cycle is adjustable from 0% to 100%. • **IN1 Frequency:** The IN1 PWM frequency can be varied between 0Hz and 250kHz, with selectable units (Hz or kHz). • **IN1 Ramp Rate**: Controls the rate of duty cycle increment. • **OUT1 Enable/Disable**: This toggle switch governs the application of the IN1 PWM signal. – **Enabled**: The IN1 PWM signal is applied to the IN1 pin. – **Disabled**: The IN1 PWM signal is not applied to the IN1 pin. • **Current:** Displays the output current measured at the SRC pin of each channel, providing a real-time indication of the current flow.
D	• **Device**: Device name • **Firmware Version**: EVM firmware version • **VM voltage**: supply voltage value.
E	• nFAULT Pin Status: – **Green**: Indicates normal operation with no active fault conditions. – **Red**: : Indicates that either overcurrent or overtemperature protection has been activated for one or more channels.

Figure 3-7 below shows the Load Control Panel under the SPI mode with the main sections enclosed in red boxes with a letter assigned.



Figure 3-8. DRV81646EVM Driver Control Panel SPI

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Table 3-3. DRV81646 GUI SPI Overview

Component label	Description
A	**Driver Configuration** Interface Selection: The device offers two interface options: Hardware and SPI. • **Hardware Interface**: Under this configuration, channels are controlled using PWM input. The interface is selected by connecting an appropriate resistor to the RSLEW/CNT pin through the MCU. • **SPI**: The SPI controls the outputs through SPI commands, which are executed by setting the control register bits. **To switch between the Hardware and SPI, powering down the device is essential, before changing the interface, and then powering up.** • **Rise/Fall Time**: This setting configures the output slew rate by connecting an appropriate resistor to the RSLEW/CNT pin. **Note that power cycling is required to apply changes to the slew rate**
B	Block Diagram of DRV81646.
C	OUT1 Channel control parameters. • **IN1 Duty Cycle**: The IN1 PWM duty cycle is adjustable from 0% to 100%. • **IN1 Frequency**: The IN1 PWM frequency can be varied between 0Hz and 250kHz, with selectable units (Hz or kHz). • **IN1 Ramp Rate**: Controls the rate of duty cycle increment. • **OUT1 Enable/Disable**: This toggle switch governs the application of the IN1 PWM signal. – **Enabled**: The IN1 PWM signal is applied to the IN1 pin. – **Disabled**: The IN1 PWM signal is not applied to the IN1 pin. • **Current:** Displays the output current measured at the SRC pin of each channel, providing a real-time indication of the current flow.
D	• **Device**: Device name • **Firmware Version**: EVM firmware version • **VM voltage**: supply voltage value.
E	• **Fault_CHx**: – **Green**: Indicates is working normally since last SPI transaction. – **Red**: Fault occurred on channel X. This bit is set if channel X encountered a fault since the last SPI transaction. The bit clears when nSCS is pulled back high at the end of valid SPI transaction (parity checks pass) • **SPI_ERROR**: – **Green**: Indicates SCLK number is correct and parity check is passed. – **Red**: Indicates that the parity checks on received data bits does not match with received parity bits or the number of SCLK pulses received when NSCS is low is not a multiple of 8.
F	**SPI Response Packet**: The current channel states of individual channels are latched on the falling edge of the nSCS pin (when SPI transaction is initiated). Latched faults are cleared on rising edge of the nSCS pin. • **FAULT_CHx** : – **0:** Channel is working normally since last SPI transaction. – **1:** Fault occurred on channel X. This bit is set if channel X encountered a fault since the last SPI transaction. The bit clears when NSCS is pulled back high at the end of valid SPI transaction (parity checks pass) • **SPISTAT**: is defined as SPISTAT = (SDI) & NOT(SPI_ERROR). A SPI error on current transaction is reported in the next transaction by the driver pulling SDO low/high during the t_{H_SCLK} interval. The SDO state is set to SPISTAT = (SDI) & NOT(SPI_ERROR). The easiest way to read the SPISTAT value is to hold SDI=1 during the t_{H_SCLK} interval and read SPISTAT after t_{SDOHIZ}, so that if there is a SPI error then SPISTAT=0, else SPISTAT=1.

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Table 3-3. DRV81646 GUI SPI Overview (continued)

Component label	Description
G	**SPI Input Packet**: • **CHx_N_Stat**: When CHx_N_State bit is set to 1, internal logic switches on the corresponding low side output channel N-FET. Setting CHx_N_State to 0 switches off the corresponding OUTx. The bits are linked to CHx toggle switches. • **R/W** : The R/W (Read/Write) bit determines if the CHx_N_state bit is propagated to outputs or not. Set R/W to 1 to perform write operation. Set R/W to 0 to read the existing channel state and fault information while leaving current output state unchanged. A fault on an output switches off the output and the state returns 0. • **Parity bits P[2:0]**: P[2:0] is a set of 3 parity bits which are used to check the correctness of received data word. If the parity check fails then the output states are not updated. The parity bits are calculated as follows, where ⊕ is XOR: – P[2] : B7 ⊕ B6 ⊕ B5 – P[1] : B6 ⊕ B5 ⊕ B4 – P[0] : B5 ⊕ B4 ⊕ B3 • **SDI:** This bit is used for SPI error detection. See the datasheet for detail.

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4 Hardware Design Files

The schematics, bill of materials (BOM), pcb layout, and 3D model STEP file for each EVM can be downloaded on the respective product folder page under the *Design Files* section.

- https://www.ti.com/tool/DRV81545EVM#design-files
- https://www.ti.com/tool/DRV81646EVM#design-files
- https://www.ti.com/tool/DRV81646DGQEVM#design-files

4.1 Schematics

Figure 4-1shows the schematics for DRV81646EVM. Other variants have minor differences of which components are marked as Do Not Populate (DNP). See schematics of another variant by downloading the *Hardware Design Files* from any EVM tool folder under the *Design Files* section. DRV81545EVM Hardware Files.zip for DRV81545EVM and DRV81646EVM Hardware Files.zip for DRV81646EVM and DRV81646DGQEVM Hardware Files.zip for DRV81646DGQEVM.

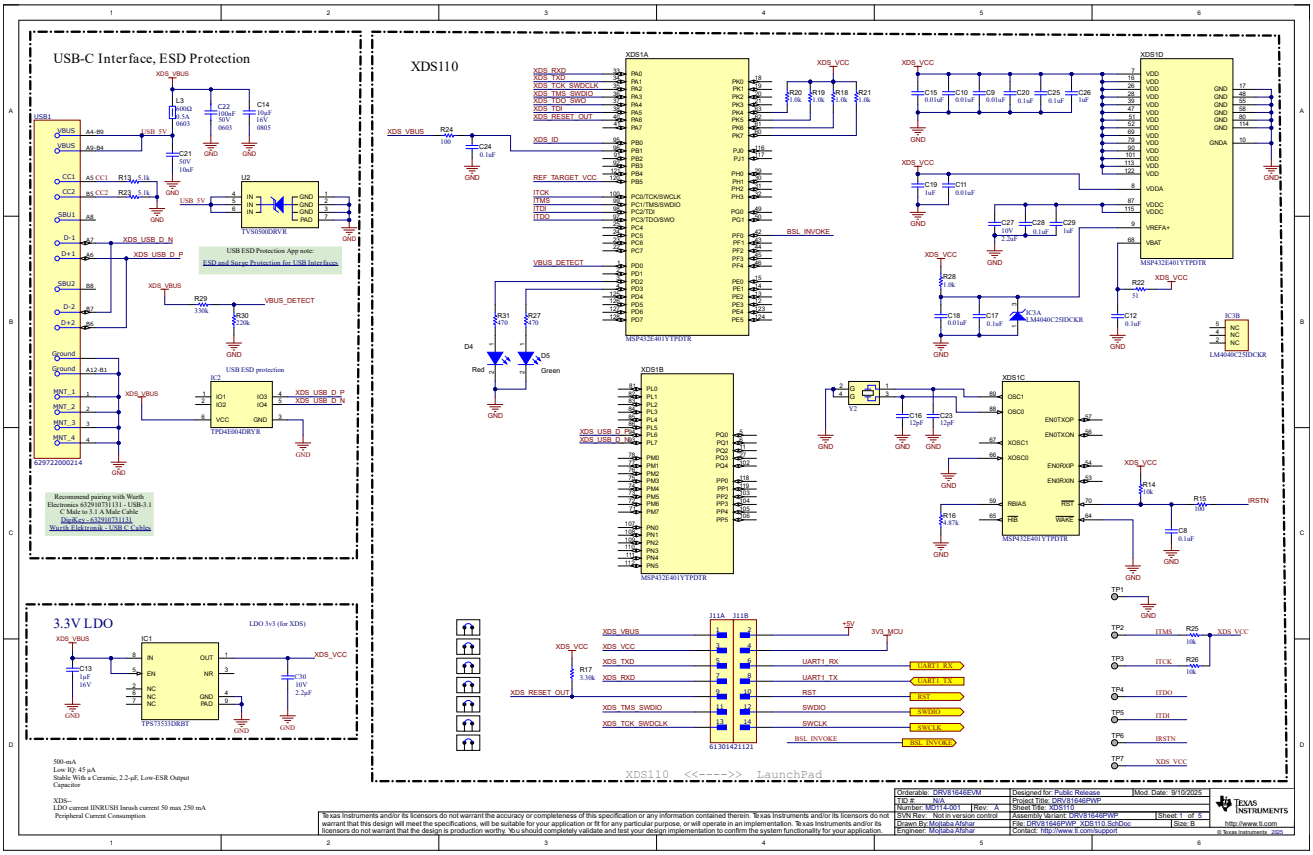


Figure 4-1. XDS110 and USB

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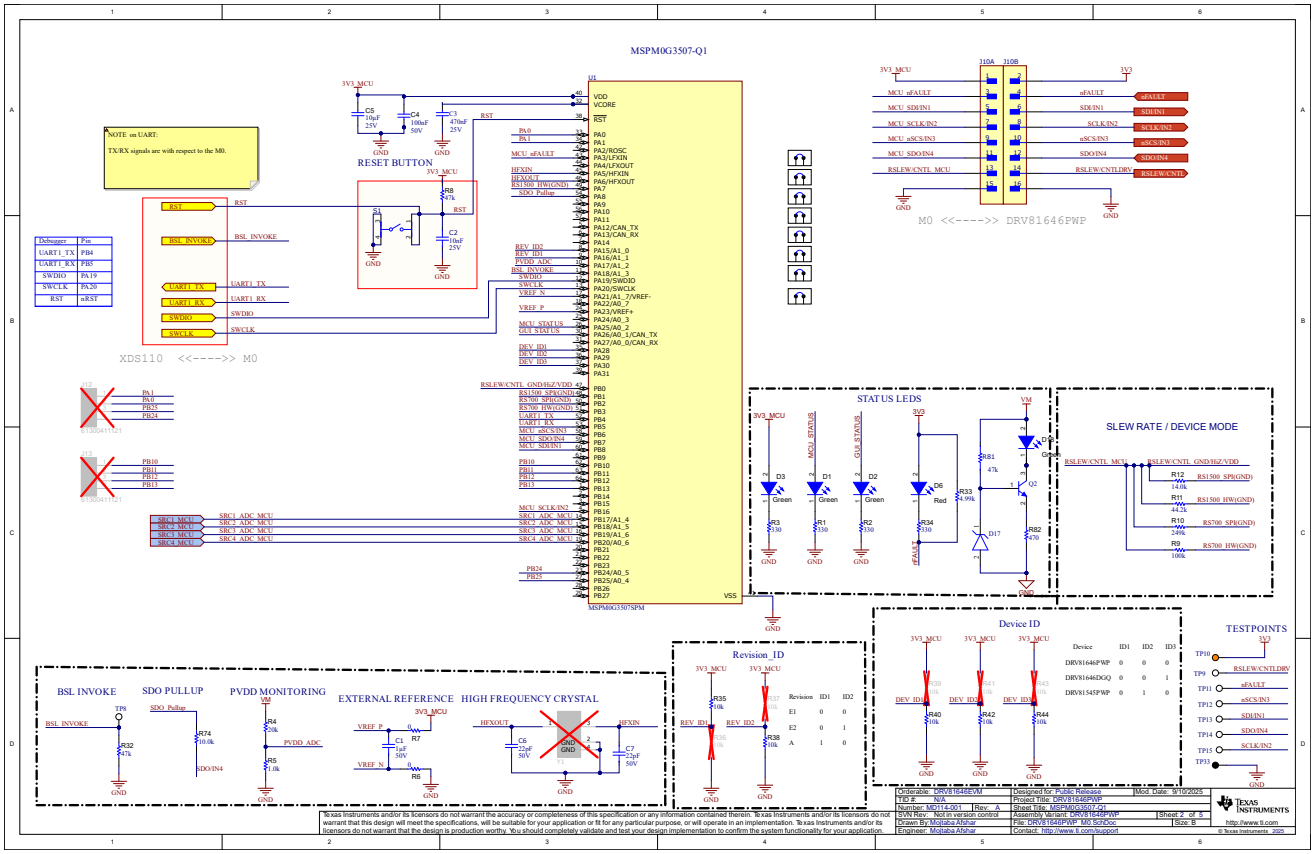


Figure 4-2. MSPM0G3507 Controller

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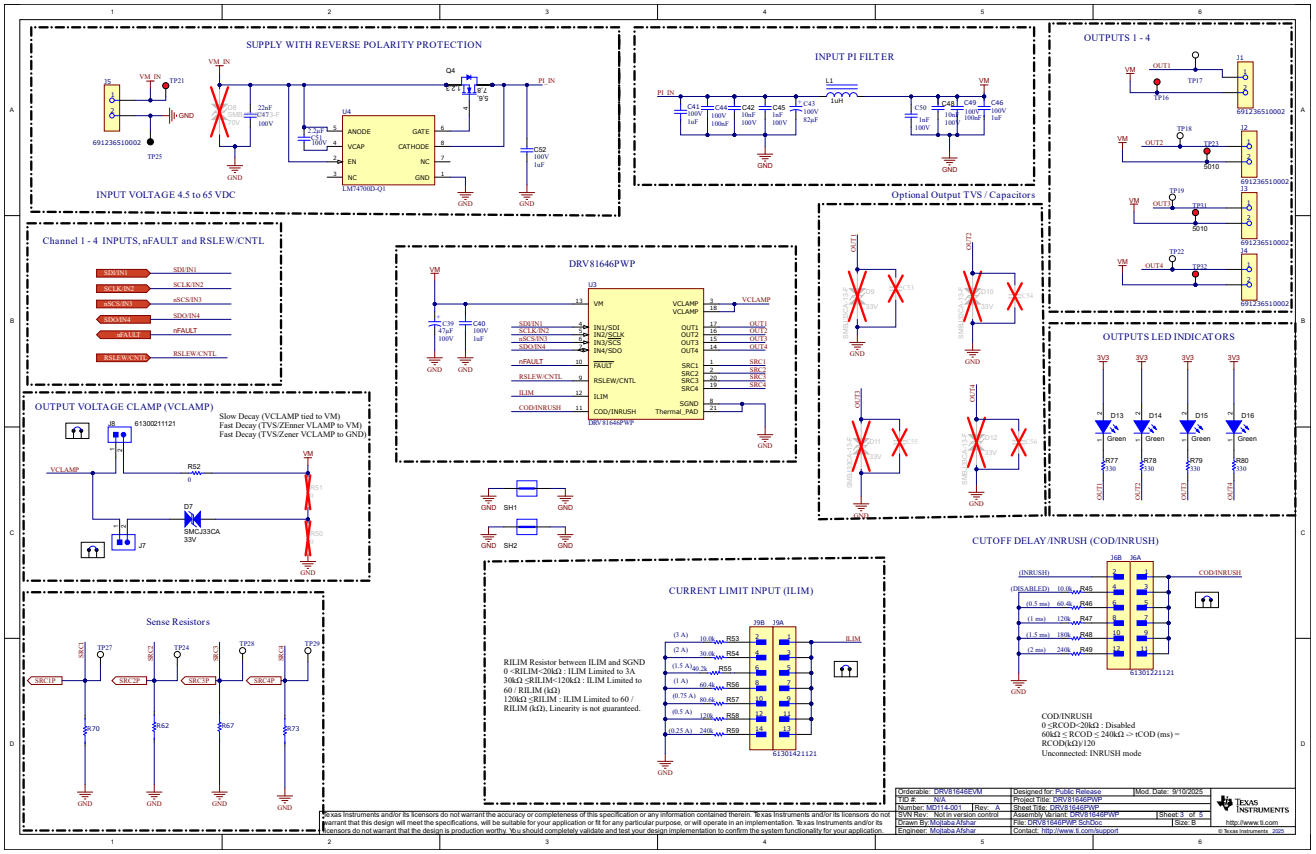


Figure 4-3. DRV81646 Driver

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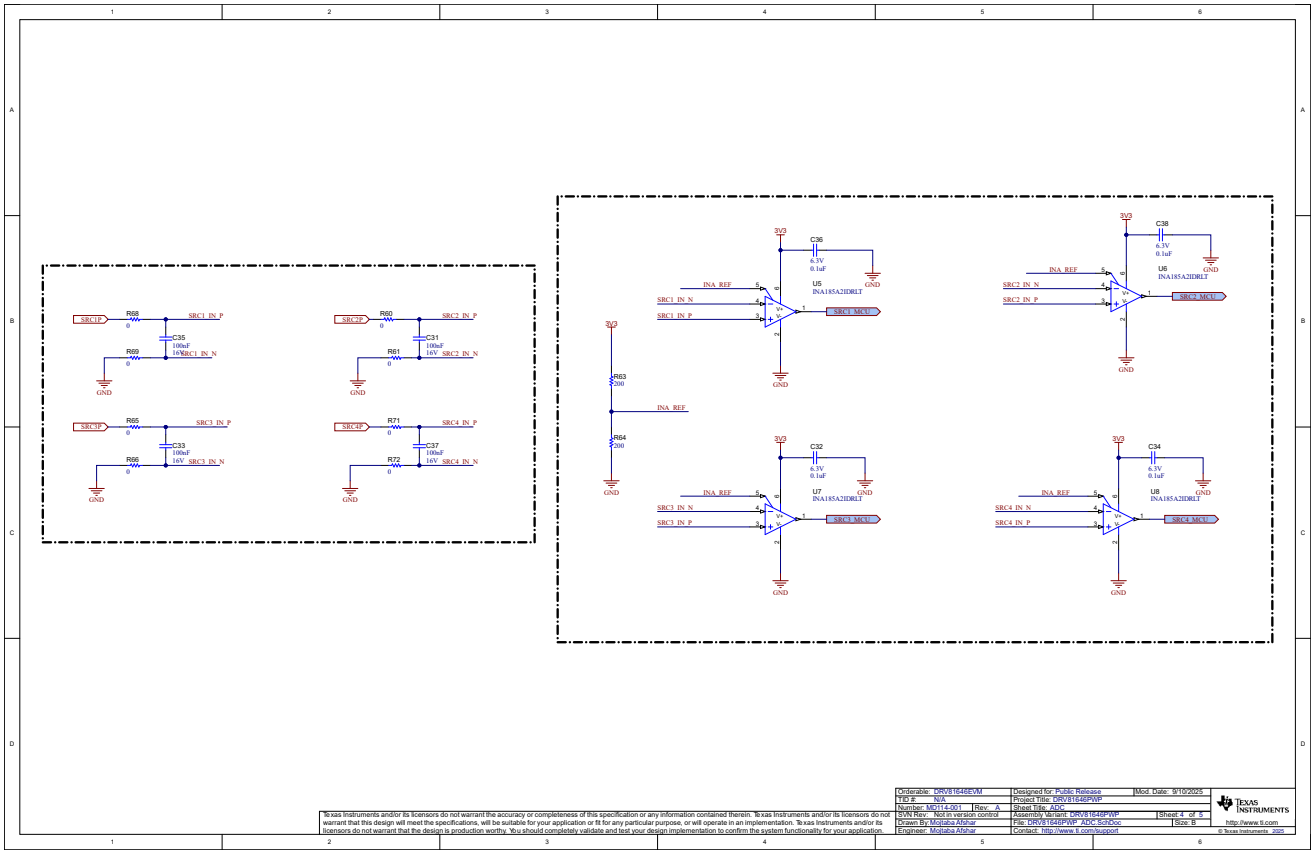


Figure 4-4. Current Sense Resistor and Amplifier

4.2 PCB Layout

Figure 4-5 through Figure 4-8 show the PCB layers of the EVM. The Altium source files can be downloaded in the aforementioned *Hardware Design Files* for a given EVM.

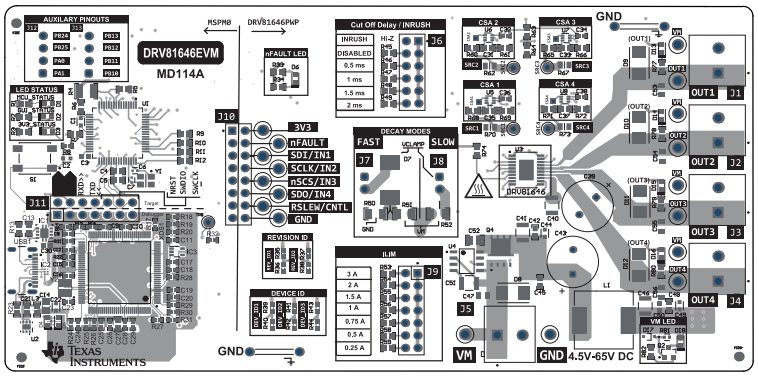


Figure 4-5. Top View

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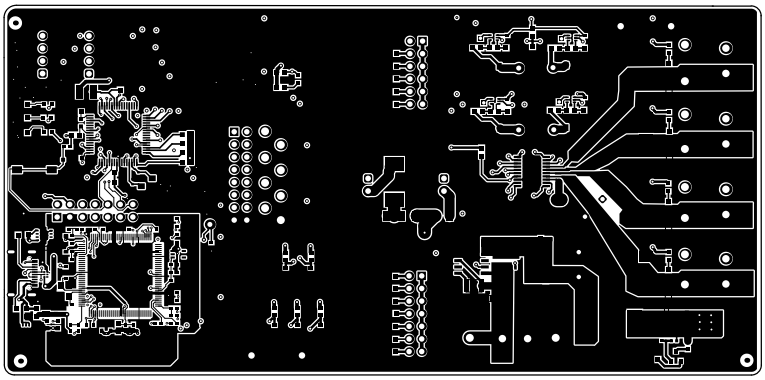


Figure 4-6. Top Layer

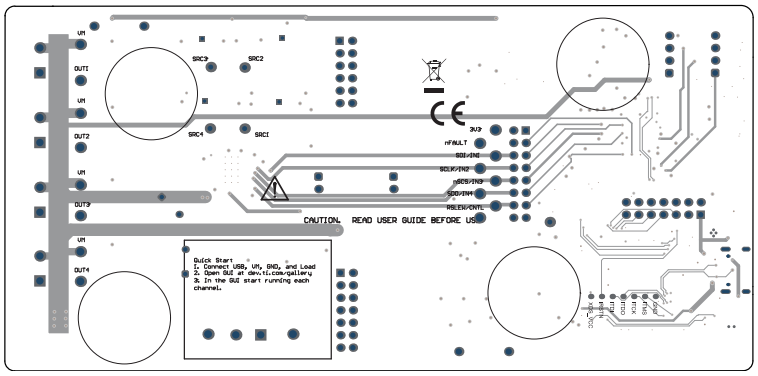


Figure 4-7. Bottom View

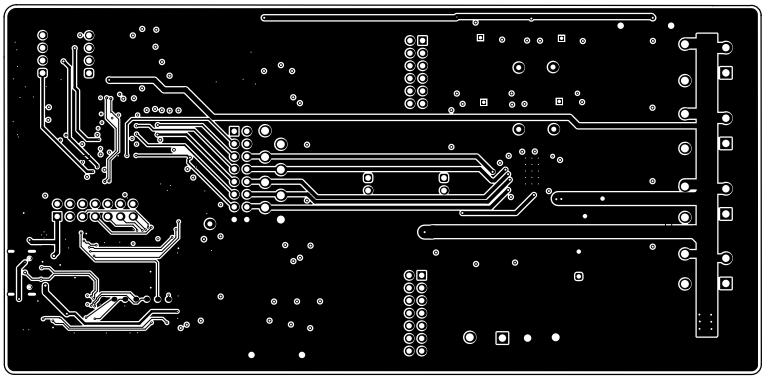


Figure 4-8. Bottom Layers

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4.3 Bill of Materials (BOM)

provides the parts list for DRV81646EVM. Other EVMs have similar BOMs that can be accessed in the aforementioned *Hardware Design Files*.

Table 4-1. Bill of Materials (DRV81646EVM)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
!PCB1	1		Printed Circuit Board		MD114-001	Any
C1	1	1µF	1 µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	0603	8.85012E+11	Wurth Electronics
C2	1	10nF	10000 pF ±10% 25V Ceramic Capacitor X7R 0603 (1608 Metric)	0603	8.85012E+11	Wurth Electronics
C3	1	470nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R Class II, 470nF, 25VDC	0603	885012206075R	Wurth Elektronik
C4	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik
C5	1	10uF	CAP, CERM, 10 µF, 25 V,+/- 10%, X5R, 0603	0603	GRM188R61E106KA73D	MuRata
C6, C7	2	22pF	22 pF ±5% 50V Ceramic Capacitor C0G, NP0 0402 (1005 Metric)	0402	8.85012E+11	Wurth Electronics
C8, C12, C17, C20, C24, C25, C28	7	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X7R, 0402	0402	GRM155R70J104KA01D	MuRata
C9, C10, C11, C15, C18	5	0.01uF	CAP, CERM, 0.01 uF, 25 V, +/- 10%, X7R, 0402	0402	GRM155R71E103KA01D	MuRata
C13	1	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik
C14	1	10uF	CAP, CERM, 10 µF, 16 V,+/- 20%, X5R, 0805	0805	8.85012E+11	Wurth Elektronik
C16, C23	2	12pF	CAP, CERM, 12 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H120JA01D	MuRata

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Table 4-1. Bill of Materials (DRV81646EVM) (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
C19, C26, C29	3	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X5R, 0402	0402	C1005X5R1E105K050BC	TDK
C21	1	0.01uF	CAP, CERM, 0.01 µF, 50 V,+/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik
C22	1	100nF	0.1 µF ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	0603	8.85012E+11	Wurth
C27	1	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X5R, 0603	0603	C0603C225K8PACTU	Kemet
C30	1		WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 2.2µF, 10VDC		8.85012E+11	Wurth Elektronik
C31, C33, C35, C37	4	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik
C32, C34, C36, C38	4	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 20%, X5R, 0402	0402	8.85012E+11	Wurth Elektronik
C39	1		WCAP-ATUL Aluminum Electrolytic Capacitor, Radial, THT, D10 x H12.5mm, 47µF, 100V		8.60041E+11	Wurth Elektronik
C40, C41, C46	3	1µF	1 µF ±10% 100V Ceramic Capacitor X7R 1210 (3225 Metric)	1210	8.85012E+11	Wurth Electronics
C42, C48	2	0.01uF	CAP, CERM, 0.01 µF, 100 V,+/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik
C43	1		WCAP-ATUL Aluminum Electrolytic Capacitor, Radial, THT, D10 x H20mm, 82µF, 100V	10mm diam x 20mm height	8.60041E+11	Wurth Elektronik
C44, C49	2	100nF	0.1 µF ±10% 100V Ceramic Capacitor X7R 0603 (1608 Metric)	0603	8.85012E+11	Wurth Electronics

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Table 4-1. Bill of Materials (DRV81646EVM) (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
C45	1	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 10%, X7R, 0603	0603	06031C102KAT2A	AVX
C47	1	22nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0805, X7R, 22nF, 100VDC	0805	8.85012E+11	Wurth Elektronik
C50	1	1nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 1nF, 100VDC	0603	8.85012E+11	Wurth Elektronik
C51	1	2.2uF	WCAP-CSST Multilayer Ceramic Chip Capacitor, Soft Termination, size 1210, X7R Class II, 2.2µF, 100VDC	1210	8.85382E+11	Wurth Elektronik
C52	1	1uF	CAP, CERM, 1 uF, 100 V, +/- 10%, X7S, 0805	0805	C2012X7S2A105K125AB	TDK
D1, D2, D3, D13, D14, D15, D16, D18	8	Green	LED, Green, SMD	LED_0603	150060VS75000	Wurth Elektronik
D4	1	Red	LED, Red, SMD	Red LED, 1.6x0.8x0.8mm	LTST-C190KRKT	Lite-On
D5	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
D6	1	Red	LED, Red, SMD	LED_0603	150060RS75000	Wurth Elektronik
D7	1	33V	Diode, TVS, Bi, 33 V, SMC	SMC	SMCJ33CA	Bourns
D17	1		DIODE ZENER 4.7V 550MW SOD323F		BZX84J-B4V7,115	
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A

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Table 4-1. Bill of Materials (DRV81646EVM) (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
IC1	1		500mA, Adjustable, Low Quiescent Current, Low-Noise, High-PSRR, Single-Output LDO Regulator, DRB0008A (VSON-8)	DRB0008A	TPS73533DRBT	Texas Instruments
IC2	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	DRY0006A	TPD4E004DRYR	Texas Instruments
IC3	1		Precision Micropower Shunt Voltage Reference, 0.5% accuracy, 2.5 V, 15 ppm / degC, 15 mA, -40 to 85 degC, 5-pin SC70 (DCK), Green (RoHS & no Sb/Br)	DCK0005A	LM4040C25IDCKR	Texas Instruments
J1, J2, J3, J4, J5	5		2 Position Wire to Board Terminal Block Horizontal with Board 0.200" (5.08mm) Through Hole	HHR2	6.91237E+11	Wurth Electronics
J6	1		THT Vertical Pin Header WR-PHD, Pitch 2.54 mm, Dual Row, 12 pins	HDR12	61301221121	Wurth Electronics
J7, J8	2		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300211121	Wurth Elektronik
J9, J11	2		Connector Header Through Hole 14 position 0.100" (2.54mm)	HDR14	61301421121	Wurth Electronics
J10	1		Connector Header Through Hole 16 position 0.100" (2.54mm)	HDR16	61301621121	Wurth

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Table 4-1. Bill of Materials (DRV81646EVM) (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
L1	1	1uH	Inductor, Shielded Drum Core, Ferrite, 1 uH, 24 A, 0.0012 ohm, SMD	12.1x9.5x11.4mm	7443320100	Wurth Elektronik
L3	1	600 ohm	Ferrite Bead, 600 ohm @ 100 MHz, 0.5 A, 0603	0603	742863160	Wurth Elektronik
MP1, MP2, MP3, MP4	4		Bumper Cylindrical, Dome 0.720" Dia (18.30mm) Polyurethane Black	BUMPER_CYLI	RBS-37BK	Essentra Components
Q2	1		General Purpose Transistor, NPN Silicon, 3-Pin SOT-23, Pb-Free, Tape and Reel	SOT-23-3-318-08	BC846BLT1G	On Semiconductor
Q4	1	80V	MOSFET, N-CH, 80 V, 100 A, DNK0008A (VSON-CLIP-8)	DNK0008A	CSD19502Q5B	Texas Instruments
R1, R2, R3, R34, R77, R78, R79, R80	8	330	RES, 330, 5%, 0.1 W, 0603	0603	RC0603JR-07330RL	Yageo
R4	1	20k	RES, 20 k, 5%, 0.5 W, 1210	1210	RC1210JR-0720KL	Yageo
R5	1	1.0k	RES, 1.0 k, 5%, 0.1 W, 0603	0603	RC0603JR-071KL	Yageo
R6, R7	2	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo
R8, R32	2	47k	RES, 47 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040247K0JNED	Vishay-Dale
R9	1	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEYJ104V	Panasonic
R10	1	249k	RES, 249 k, 1%, 0.1 W, 0603	0603	RC0603FR-07249KL	Yageo
R11	1	44.2k	RES, 44.2 k, 1%, 0.1 W, 0603	0603	RC0603FR-0744K2L	Yageo
R12	1	14.0k	RES, 14.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0714KL	Yageo

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Table 4-1. Bill of Materials (DRV81646EVM) (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
R13, R23	2	5.1k	RES, 5.1 k, 5%, 0.1 W, 0603	0603	RC0603JR-075K1L	Yageo
R14, R25, R26	3	10k	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0JNED	Vishay-Dale
R15, R24	2	100	RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100RJNED	Vishay-Dale
R16	1	4.87k	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K87FKED	Vishay-Dale
R17	1	3.30k	RES, 3.30 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF3301X	Panasonic
R18, R19, R20, R21, R28	5	1.0k	RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00JNED	Vishay-Dale
R22	1	51	RES, 51, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040251R0JNED	Vishay-Dale
R27, R31	2	470	RES, 470, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402470RJNED	Vishay-Dale
R29	1	330k	RES, 330 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07330KL	Yageo America
R30	1	220k	RES, 220 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07220KL	Yageo America
R33	1	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K99L	Yageo
R35, R38, R40, R42, R44	5	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	RC0603JR-0710KL	Yageo
R45, R53, R74	3	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R46, R56	2	60.4k	RES, 60.4 k, 1%, 0.1 W, 0603	0603	RC0603FR-0760K4L	Yageo
R47, R58	2	120k	RES, 120 k, 1%, 0.1 W, 0603	0603	RC0603FR-07120KL	Yageo

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Table 4-1. Bill of Materials (DRV81646EVM) (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
R48	1	180k	RES, 180 k, 1%, 0.1 W, 0603	0603	RC0603FR-07180KL	Yageo
R49, R59	2	240k	RES, 240 k, 1%, 0.1 W, 0603	0603	RC0603FR-07240KL	Yageo
R52	1	0	RES, 0, 0.75 W, AEC-Q200 Grade 0, 1206	1206	CRCW12060000Z0EAHP	Vishay-Dale
R54	1	30.0k	RES, 30.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730KL	Yageo
R55	1	40.2k	RES, 40.2 k, 1%, 0.1 W, 0603	0603	RC0603FR-0740K2L	Yageo
R57	1	80.6k	RES, 80.6 k, 1%, 0.1 W, 0603	0603	RC0603FR-0780K6L	Yageo
R60, R61, R65, R66, R68, R69, R71, R72	8	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R62, R67, R70, R73	4	10m	10 mOhms ±1% 0.5W, 1/2W Chip Resistor 0805 (2012 Metric) Current Sense Thick Film	0805	5.80061E+11	Wurth Electronics
R63, R64	2	200	RES, 200, 1%, 0.1 W, 0603	0603	RC0603FR-07200RL	Yageo
R81	1	47k	47 kOhms ±1% 0.125W, 1/8W Chip Resistor 0402 (1005 Metric) Automotive AEC-Q200 Thick Film	0402	RCC040247K0FKED	Vishay Dale
R82	1	470	RES, 470, 1%, 0.1 W, 0603	0603	RC0603FR-07470RL	Yageo
S1	1		Tactile Switch SPST-NO Top Actuated Surface Mount	SMT_SW_6MM2_6MM2	4.30481E+11	Wurth Electronics
SH1, SH2	2		1mm Uninsulated Shorting Plug, 10.16mm spacing, TH	Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin

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Table 4-1. Bill of Materials (DRV81646EVM) (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J14, SH-J15, SH-J16, SH-J17, SH-J18, SH-J19, SH-J20	19		Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik
TP8, TP24, TP27, TP28, TP29	5		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone Electronics
TP9, TP11, TP12, TP13, TP14, TP15, TP17, TP18, TP19, TP22	10		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone Electronics
TP10	1		Test Point, Multipurpose, Orange, TH	Orange Multipurpose Testpoint	5013	Keystone
TP16, TP21, TP23, TP31, TP32	5		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone Electronics
TP25, TP33	2		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone Electronics, Keystone
U1	1		Mixed-Signal Microcontrollers With CAN-FD Interface LQFP64	LQFP64	MSPM0G3507SPM	Texas Instruments
U2	1		5-V Precision Surge Protection Clamp, DRV0006A (WSON-6)	DRV0006A	TVS0500DRVR	Texas Instruments
U3	1		DRV81646PWP	HTSSOP20	DRV81646PWP	Texas Instruments
U4	1		LM74700D-Q1	SOIC8	LM74700D-Q1	Texas Instruments
U5, U6, U7, U8	4		Bidirectional, Precision Low- and High-Side Voltage Output, Current-Sense Amplifier, DRL0006A (SOT-5X3-6)	DRL0006A	INA185A2IDRLR	Texas Instruments
USB1	1		Conenctor USB 2.0 Type C Horizontal SMT	CONN_USB	6.29722E+11	Wurth Electronics

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Table 4-1. Bill of Materials (DRV81646EVM) (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
XDS1	1		MSP432E401YTPDT, PDT0128A (TQFP-128)	PDT0128A	MSP432E401YTPDTR	Texas Instruments
Y2	1		Crystal, 16 MHz, 8pF, SMD	3.2x0.75x2.5mm	NX3225GA-16.000M-STD-CRG-1	NDK
C53, C54, C55, C56	0		WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0805, X7R, 22nF, 100VDC			Wurth Elektronik
D8	0	70V	Diode, TVS, Bi, 70 V, SMB	SMB	SMBJ70CA-13-F	Diodes Inc.
D9, D10, D11, D12	0	33V	Diode, TVS, Bi, 33 V, SMB	SMB	SMBJ33CA-13-F	Diodes Inc.
J12, J13	0		Header, 2.54 mm, 4x1, Gold, TH	Header, 2.54mm, 4x1, TH	61300411121	Wurth Elektronik
R36, R37, R39, R41, R43	0	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	RC0603JR-0710KL	Yageo
R50, R51	0	0	RES, 0, 0.75 W, AEC-Q200 Grade 0, 1206	1206	CRCW12060000Z0EAHP	Vishay-Dale
Y1	0		Crystal 40MHz ±10ppm (Tol) ±20ppm (Stability) 12pF FUND 40Ohm 4-Pin Mini-CSMD T/R	TSX-3225	X1E0000210179	Seiko Epson

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5 Additional Information

5.1 Trademarks

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   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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