

EVM User's Guide: DAC90802EVM-PDK

DAC90802 Evaluation Module



Description

The DAC90802 evaluation board features two programmable output channels controlled through the EVM graphical user interface (GUI). Channel 0 demonstrates general applications including linearity testing, arbitrary waveform generation (AWG), and standard dc voltage output. Channel 1 is specifically configured for multiplying bandwidth applications. The DAC90802EVM board is controlled through USB connection to a personal computer (PC) using an Opal Kelly FPGA card (XEM7310A-75T or XEM7310A-200T) running the DAC90802EVM GUI software. Additionally, a header connector provides access to the general digital pins for functionality verification and device testing.

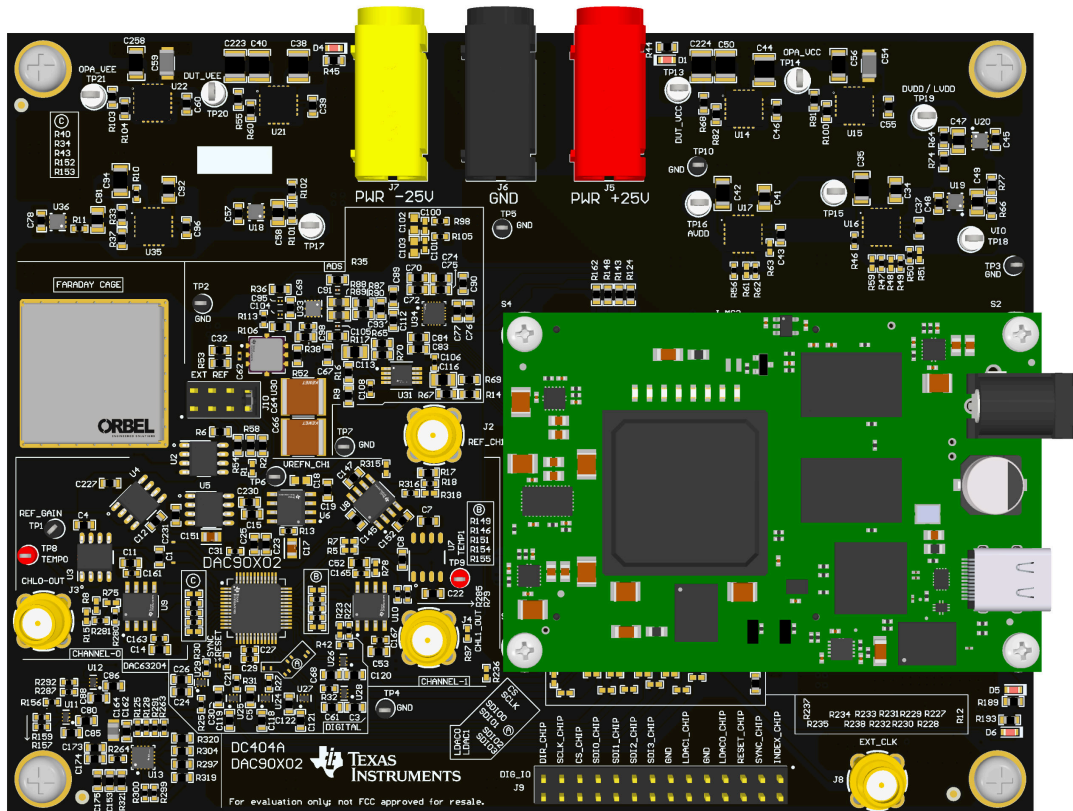
Get Started

1. Order the [EVM](#).

2. Configure EVM jumpers for reference section.
3. Download the DAC90802EVM GUI on ti.com.
4. Connect external power supplies and USB.
5. Launch the DAC90802EVM GUI.

Features

- Two independent output channels, each configured for different applications.
- Channel 0 supports linearity testing, arbitrary waveform generation (AWG), and dc voltage output.
- Channel 1 is specifically designed for multiplying DAC applications.
- Onboard VREF support
- XEM7310 FPGA card integration for seamless communication with the DAC using the DAC90802EVM GUI
- External digital interface header available for direct device control and connectivity.



1 Evaluation Module Overview

1.1 Introduction

The DAC90802EVM is a dual-channel, 18-bit, voltage output, digital-to-analog converter (DAC) utilizing a proprietary multiplying DAC (MDAC) architecture, capable of $\pm 23.5V$ supply span operation. A dynamic signal range of $\pm 21V$ is supported for the reference inputs, and voltage feedback at the RFBx pin, where gain options of 1, 2, and 4 are digitally selectable. 66MHz serial data interface with up to four serial data lines (SDIO0 through SDIO3) in dual data rate (DDR) mode, supports update rates up to 33MUPS in high speed 16-bit mode, and 22MUPS in high resolution 18-bit mode. Per channel edge-sensitive LDACx inputs allow fine skew control of the DAC output from previously loaded input registers. System reset is supported through the RESET pin. RESET forces the DACs to mid code in default mode.

The user guide describes the characteristics, operation, and recommended use cases of the DAC90802EVM. The user guide provides examples and instructions on how to use the DAC90802EVM board and included software. Throughout the document, the terms evaluation board, evaluation module, and EVM are synonymous with the DAC90802EVM. The user guide also includes a schematic, reference printed circuit board (PCB) layout, and a complete bill of materials (BOM).

1.2 Kit Contents

Table 1-1 details the contents of the EVM kit. Contact the TI Product Information Center at (972) 644-5580 if any component is missing. Download the latest version of the related software from www.ti.com.

Table 1-1. DAC90802EVM Kit Contents

ITEM	QUANTITY
DAC90802EVM	1
USB-C cable	1
Opal Kelly FPGA card(XEM7310A75T/200T)	1

1.3 Specification

Figure 1-1 shows the block diagram of the DAC90802EVM board. By default, the DAC90802EVM connects to a PC USB port through a USB-C cable.

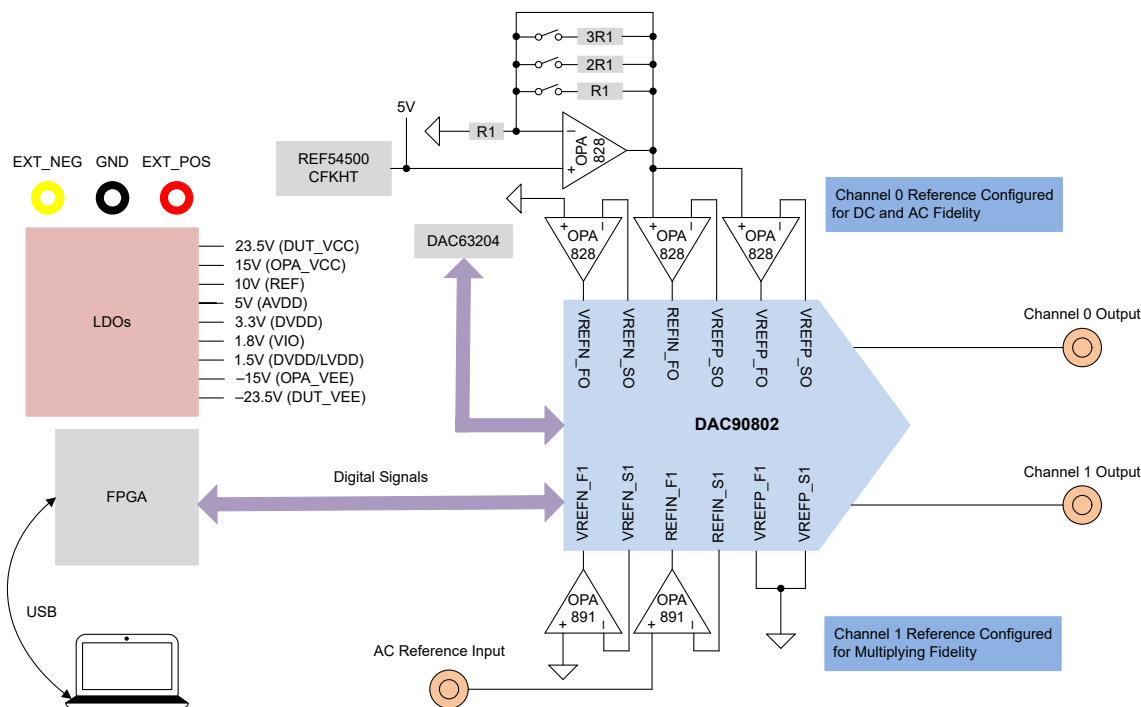


Figure 1-1. DAC90802EVM Block Diagram

An onboard buck converter provides 5V to the FPGA and a LDO regulated VIO supply (1.8V) is used to power the digital buffers. An external bipolar supply is connected to EXT_POS (25V nominal), GND, and EXT_NEG (–25V nominal) to power on the EVM. Onboard LDOs help to generate all other auxiliary supplies used by the EVM.

1.4 Device Information

The DAC90802EVM is a dual-channel 18-bit, multiplying digital-to-analog converter (MDAC) capable of $\pm 23.5V$ supply span operation. A dynamic signal range of $\pm 21V$ is supported for the reference inputs, and voltage feedback at the RFBx pin, where gain options of 1, 2, and 4 are digitally selectable.

Key ICs used in the DAC90802EVM

DAC90802	Dual-channel 18-bit, multiplying digital-to-analog converter (MDAC)
REF545000CFKHT	Precision voltage reference(5V variant)
OPA828IDR	High-speed low-noise JFET operational amplifier
OPA891DR	Operational amplifier with ultra-low THD
TPSM86638RCGR	Buck power module
SN74LXC2T45DTM	Voltage level shifter DTM package 8-Pin X2SON
DAC63204RTER	12-Bit, quad voltage output smart DAC
REF54250CFKHT	Precision voltage reference(2.5V variant)
THS4551IRUNR	Fully differential amplifier
ADS127L21IRUKR	24-Bit, delta-sigma ADC
TPS7A4701QRGWRQ1	Positive low-dropout (LDO) voltage regulator
TPS7A3301RGWR	Negative low-dropout linear regulator
TLV76701DRVR	Positive voltage regulator

2 Hardware

2.1 Power Requirements

The DAC90802EVM requires external power supplies to operate all sections of the evaluation board. The primary power is supplied through two external $\pm 25\text{V}$ connections (EXT_POS and EXT_NEG) with a current limit of 500mA on each supply. EXT_POS and EXT_NEG are the only externally applied power supplies required for the EVM.

All other power supply voltages are derived internally using low dropout (LDO) regulators and a buck converter. The DAC90802EVM core operates on a bipolar supply (DUT_VCC and DUT_VEE) nominally at $\pm 23.24\text{V}$, which are also used by the reference signal chain operational amplifiers in addition to the OPA_VCC and OPA_VEE supplies. Additional analog and digital supply rails are generated through cascaded LDO regulators to support the DAC I/O, digital circuits, and peripheral components.

An onboard reference for the DAC90802EVM is provided by the REF5450 reference IC, which operates on the REF voltage (10V) derived from the OPA_VCC supply rail. The DAC requires three additional supplies: AVDD (5V) for analog supply, DVDD and LVDD (1.5V) for digital, and VIO (1.8V) for the digital interface. The ADS127L21 analog-to-digital converter requires a symmetric dual supply of $\pm 2.5\text{V}$ (ADS_AVDD and ADS_AVSS) generated by dedicated regulators. Power for the Opal Kelly FPGA board is provided through a buck converter (U23) which generates 5V from the external 25V supply. The USB connection is used exclusively for data transfer and does not provide power to the EVM. [Table 2-1](#) summarizes the external power connections and test point terminals. [Figure 2-1](#) shows power supply inputs and internal rails terminal.

Table 2-1. DAC90802EVM Power Supply Terminals, Internal Rails and Test Points

TERMINAL	NAME	FUNCTION
J5	EXT_POS	Banana jack connection to an external +25V supply with a 500mA current limit. J5 terminal provides power to the TPS7A4701QRGWRQ1 regulator (U14) and the FPGA buck converter (U23), which generate DUT_VCC and VDCIN, respectively.
J6	GND	Banana jack connection to board ground reference
J7	EXT_NEG	Banana jack connection to an external -25V supply with a 500mA current limit. J7 terminal provides power to the TPS7A3301RGWR regulator (U21), which generates DUT_VEE.
TP13	DUT_VCC	Test point for the DAC positive core supply (+23.24V). DUT_VCC rail is generated by the TPS7A4701 regulator (U14) from the EXT_POS input. DUT_VCC supplies the operational amplifiers for high-voltage reference generation and serves as the input to the OPA_VCC regulator(U15).
TP14	OPA_VCC	Test point for operational amplifier positive supply (+16.38V). OPA_VCC rail is generated by TPS7A4701QRGWRQ1 (U15) from the DUT_VCC input.
TP15	REF	Test point for the +10V reference voltage supply. REF rail is generated by the TPS7A4701 regulator (U16) from the OPA_VCC input and provides the supply voltage for the REF5450 reference IC used in onboard voltage reference generation.
TP16	AVDD	Test point for DAC analog supply (+5V). AVDD rail is generated by TPS7A4701QRGWRQ1 (U17) from the REF input.
TP18	VIO	Test point for DAC I/O supply voltage (+1.8V). VIO rail is generated by TLV76701DRVR (U19) from the AVDD input. VIO is a DAC digital interface supply voltage.
TP19	DVDD	Test point for DAC digital and low-voltage supply (+1.5V). DVDD rail is generated by TLV76701DRVR (U20) from the AVDD input. DVDD is a DAC supply for digital and low-voltage circuits.
TP17	DVDD_3V3	Test point for 3.3V supply (+3.3V). DVDD_3V3 rail is generated by TLV76701DRVR (U18) from the AVDD input and provides supply for digital buffers.
TP20	DUT_VEE	Test point for DAC negative core supply (-23.24V). DUT_VEE rail is generated by TPS7A3301RGWR (U21) from EXT_NEG. DUT_VEE accommodates operational amplifier supplies for high-voltage reference generation and provides input to OPA_VEE regulator.
TP21	OPA_VEE	Test point for operational amplifier negative supply (-16.38V). OPA_VEE rail is generated by TPS7A3301RGWR (U22) from the DUT_VEE input.

Table 2-1. DAC90802EVM Power Supply Terminals, Internal Rails and Test Points (continued)

TERMINAL	NAME	FUNCTION
-	ADS_AVDD	ADS127L21 positive analog supply (+2.5V). ADS_AVDD rail is generated by TLV76701DRVR (U36) from the AVDD input, which provides supply to ADS127L21 analog circuits.
-	ADS_AVSS	ADS127L21 negative analog supply (–2.5V). ADS_AVSS rail is generated by TPS7A3301RGWR (U35) from OPA_VEE input, which provides negative supply to ADS127L21 analog circuits.
-	VDCIN	Opal Kelly FPGA board supply (+5V). VDCIN rail is generated by buck converter TPSM86638RCGR (U23) from EXT_POS, which provides power to FPGA module.

Banana Jacks for External Supply and Other Power Supply Terminals

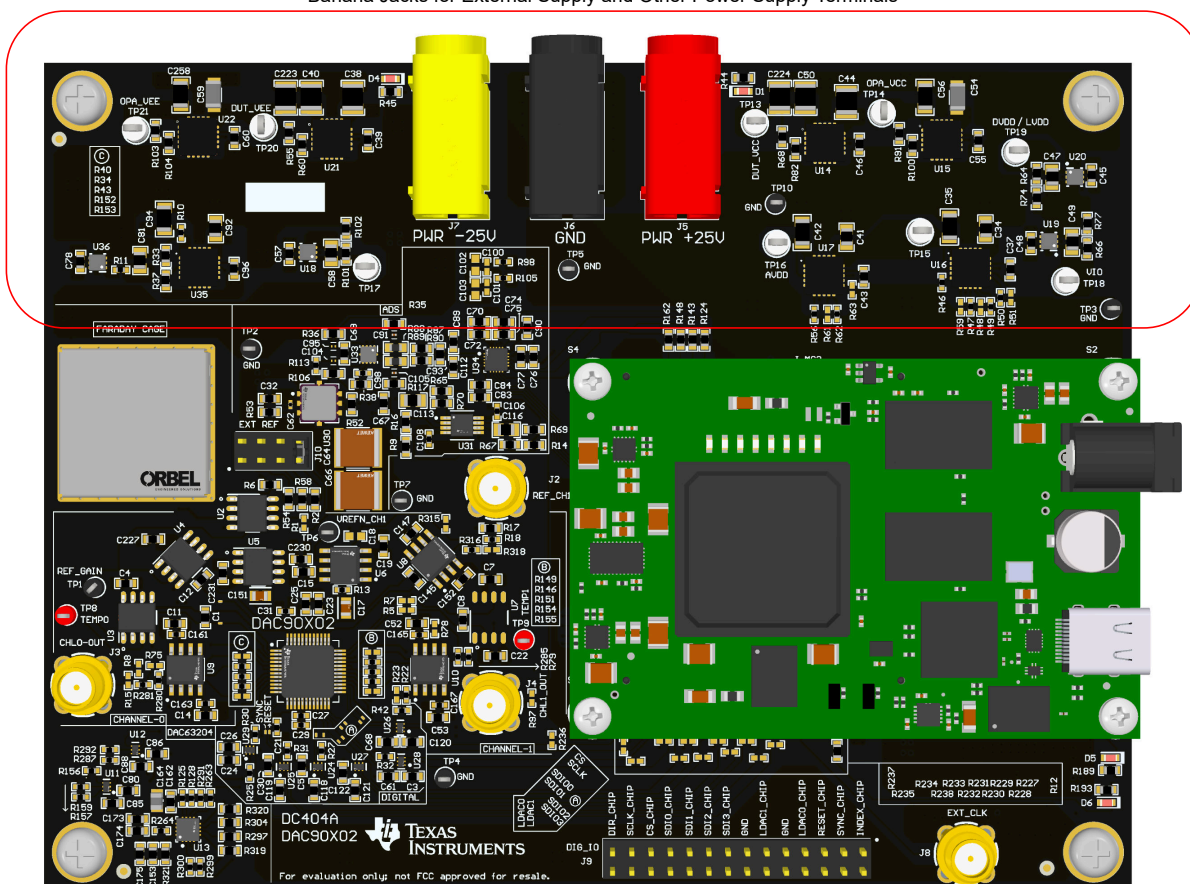


Figure 2-1. Power Supply Terminals, Internal Rails and Test Points

2.2 Jumper Information

The jumper settings on the [DAC90802EVM](#) are crucial to the proper operation of the evaluation module. The EVM provides a single configurable header (J10) with a shunt jumper (SH-J) that allows selection of the reference voltage supplied to the device through a gain amplifier (U2). Four selectable reference voltage options are available: 5V, 10V, 15V, and 20V. The jumper position determines which reference voltage is applied to the DAC device. [Table 2-2](#) summarizes the jumper configuration options.

The default jumper placement is at pins 7-8 for 5V reference voltage. Select only one jumper position at a time. Power off the EVM before changing the jumper configuration. After reconfiguring, verify the selected reference voltage at test point TP1 before applying input signals to the device. [Figure 2-2](#) shows the default jumper settings.

Table 2-2. DAC90802EVM Reference Jumper Configuration

JUMPER	PINS	REFERENCE VOLTAGE	DESCRIPTION
SH-J	7-8(J10)	5V	Default configuration; selects 5V reference voltage to the device through gain amplifier U2
SH-J	5-6(J10)	10V	Selects 10V reference voltage to the device through gain amplifier U2
SH-J	3-4(J10)	15V	Selects 15V reference voltage to the device through gain amplifier U2
SH-J	3-4(J10)	20V	Selects 20V reference voltage to the device through gain amplifier U2

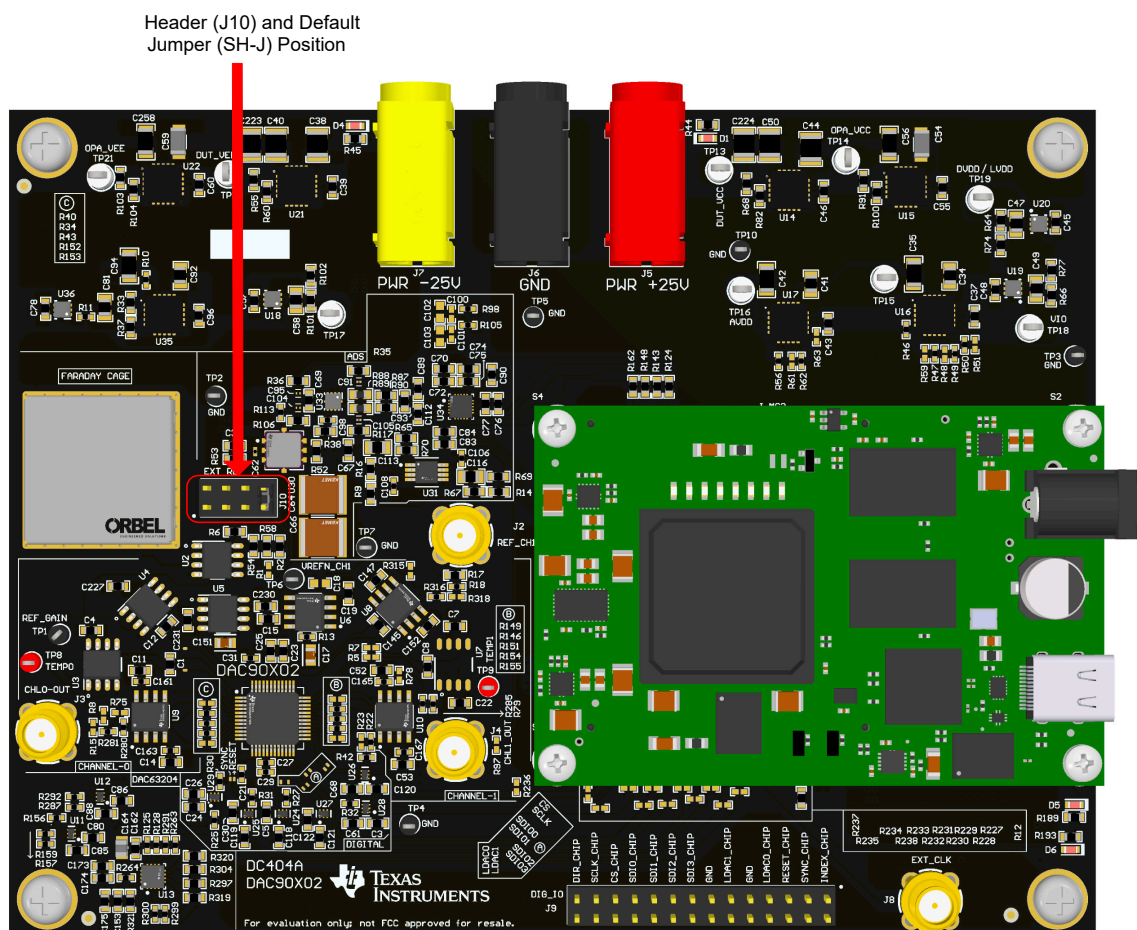


Figure 2-2. Default Jumper Setting for the DAC90802EVM

2.3 Setup

After the power and jumper configurations are setup as per [Table 2-1](#), [Table 2-2](#), [Figure 2-1](#), and [Figure 2-2](#), and the [DAC90802EVM](#) GUI is fully downloaded, connect the USB cable from the [DAC90802EVM](#) FPGA card USB port to the local machine. [Figure 2-3](#) displays the system hardware setup.

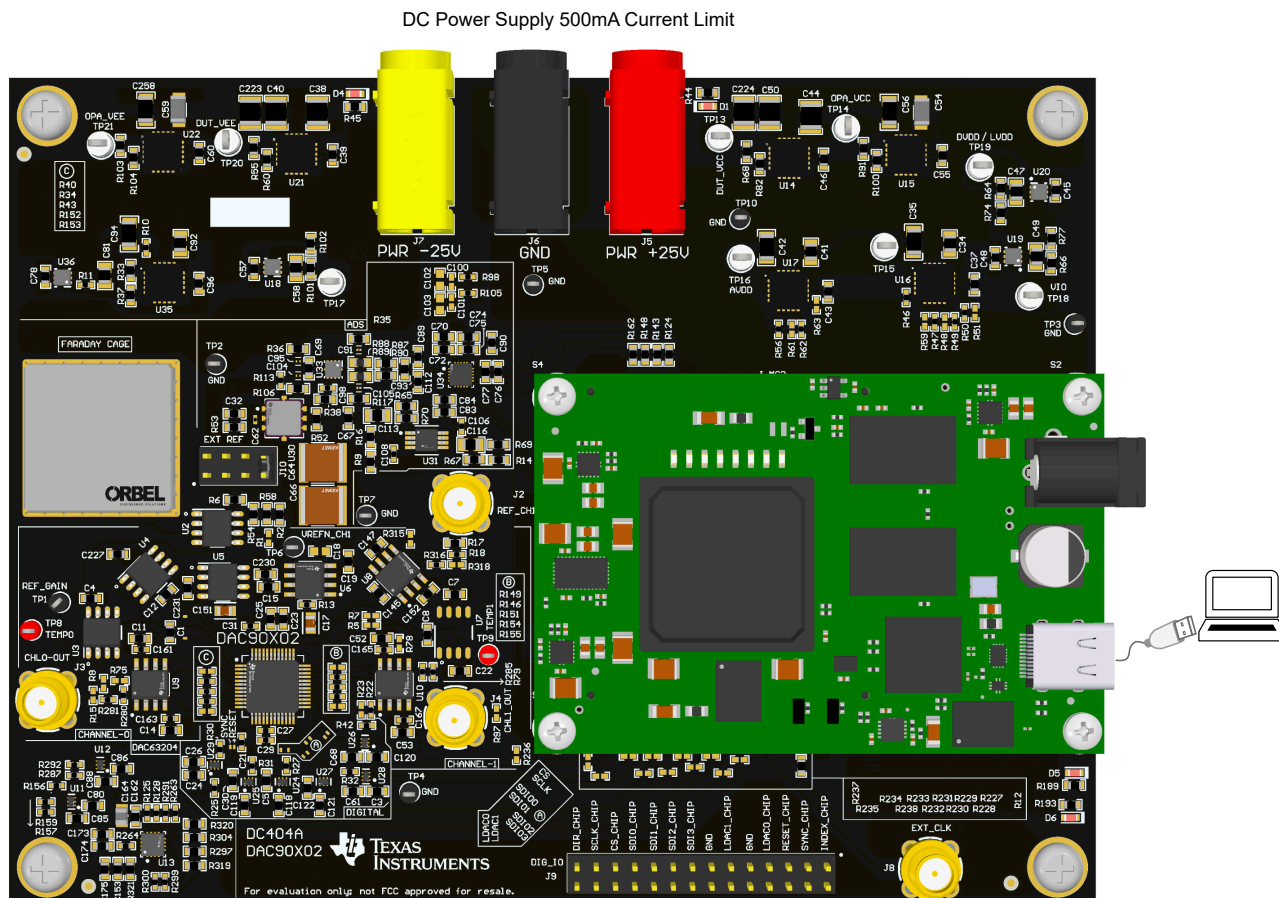


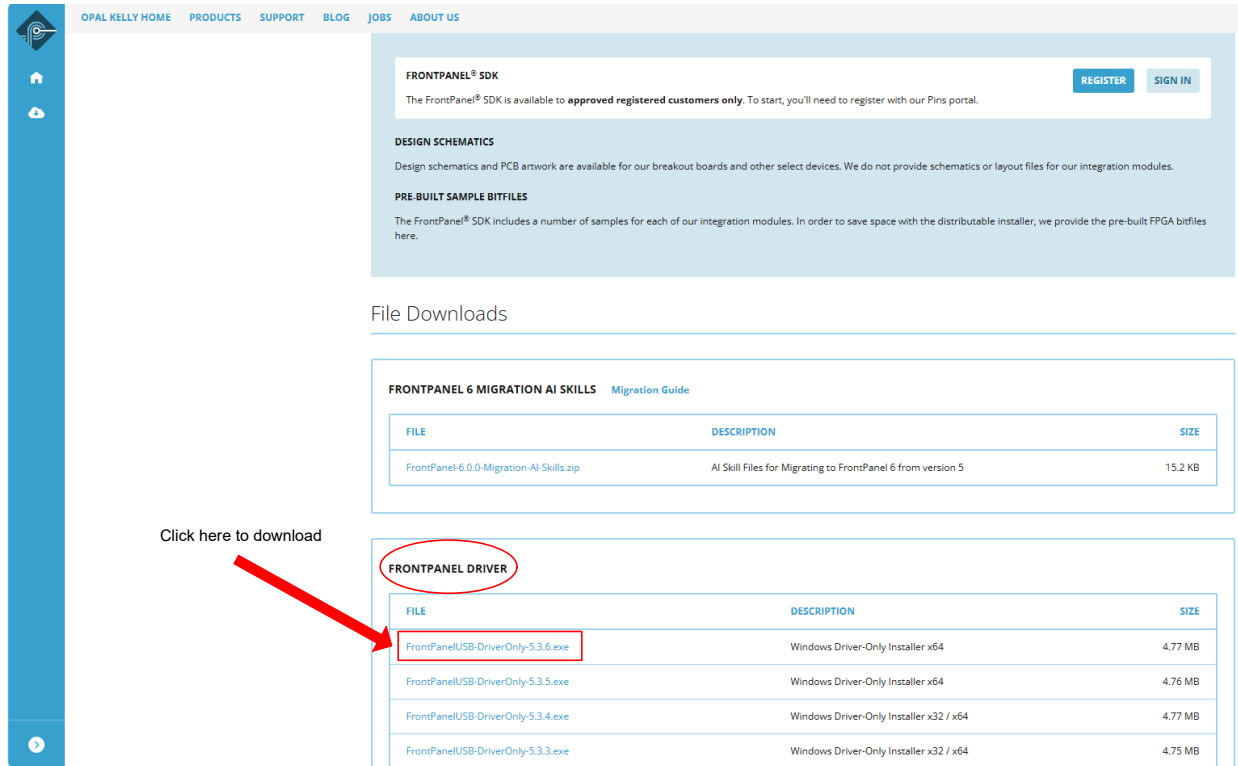
Figure 2-3. DAC90802EVM Hardware Setup

3 Software

3.1 GUI Installation

The section provides procedure for the EVM software installation. The [DAC90802EVM](#) software is portable; there is no GUI installation required other than installing the FPGA controller (Opal Kelly XEM7310A75) front panel driver. The EVM software is compatible with the Windows® 11 operating system. Before installing the software, verify that the [DAC90802EVM](#) is not connected to the local machine. Follow the steps to install the driver, unzip the GUI to a folder of your choice, and prepare the GUI for use:

- Download the Opal Kelly front panel driver from <https://pins.opalkelly.com/downloads> as shown in [Figure 3-1](#).



The screenshot shows the Opal Kelly FrontPanel SDK website. The navigation bar includes links for OPAL KELLY HOME, PRODUCTS, SUPPORT, BLOG, JOBS, and ABOUT US. The main content area has sections for FRONTANEL® SDK, DESIGN SCHEMATICS, and PRE-BUILT SAMPLE BITFILES. Below these is a 'File Downloads' section. Under 'FRONTPANEL 6 MIGRATION AI SKILLS', there is a table with one file: 'FrontPanel-6.0.0-Migration-AI-Skills.zip'. Below that is the 'FRONTPANEL DRIVER' section, which contains a table with four files. A red circle highlights the 'FRONTPANEL DRIVER' section header, and a red arrow points to the first file in the table, 'FrontPanelUSB-DriverOnly-5.3.6.exe'.

FILE	DESCRIPTION	SIZE
FrontPanel-6.0.0-Migration-AI-Skills.zip	AI Skill Files for Migrating to FrontPanel 6 from version 5	15.2 KB

FILE	DESCRIPTION	SIZE
FrontPanelUSB-DriverOnly-5.3.6.exe	Windows Driver-Only Installer x64	4.77 MB
FrontPanelUSB-DriverOnly-5.3.5.exe	Windows Driver-Only Installer x64	4.76 MB
FrontPanelUSB-DriverOnly-5.3.4.exe	Windows Driver-Only Installer x32 / x64	4.77 MB
FrontPanelUSB-DriverOnly-5.3.3.exe	Windows Driver-Only Installer x32 / x64	4.75 MB

Figure 3-1. Driver Download page

- Install the Opal Kelly front panel driver by double-clicking on FrontPanelUSB-DriverOnly-5.3.6.exe.
- Follow the on-screen instructions to complete the Opal Kelly front panel driver installation as shown in [Figure 3-2](#).
- Download the latest version of the EVM GUI software from the order and start development subsection of the DAC90802EVM tool folder on [ti.com](https://www.ti.com).
- Extract the downloaded zip file to a desired location on your local machine.
- After extracting the downloaded zip file, the folder contains the DAC90802EVM GUI.exe application and an internal folder containing the GUI dependencies.
- Keep the internal folder in the same location as the executable file. For proper GUI operation, do not move or delete the internal folder.

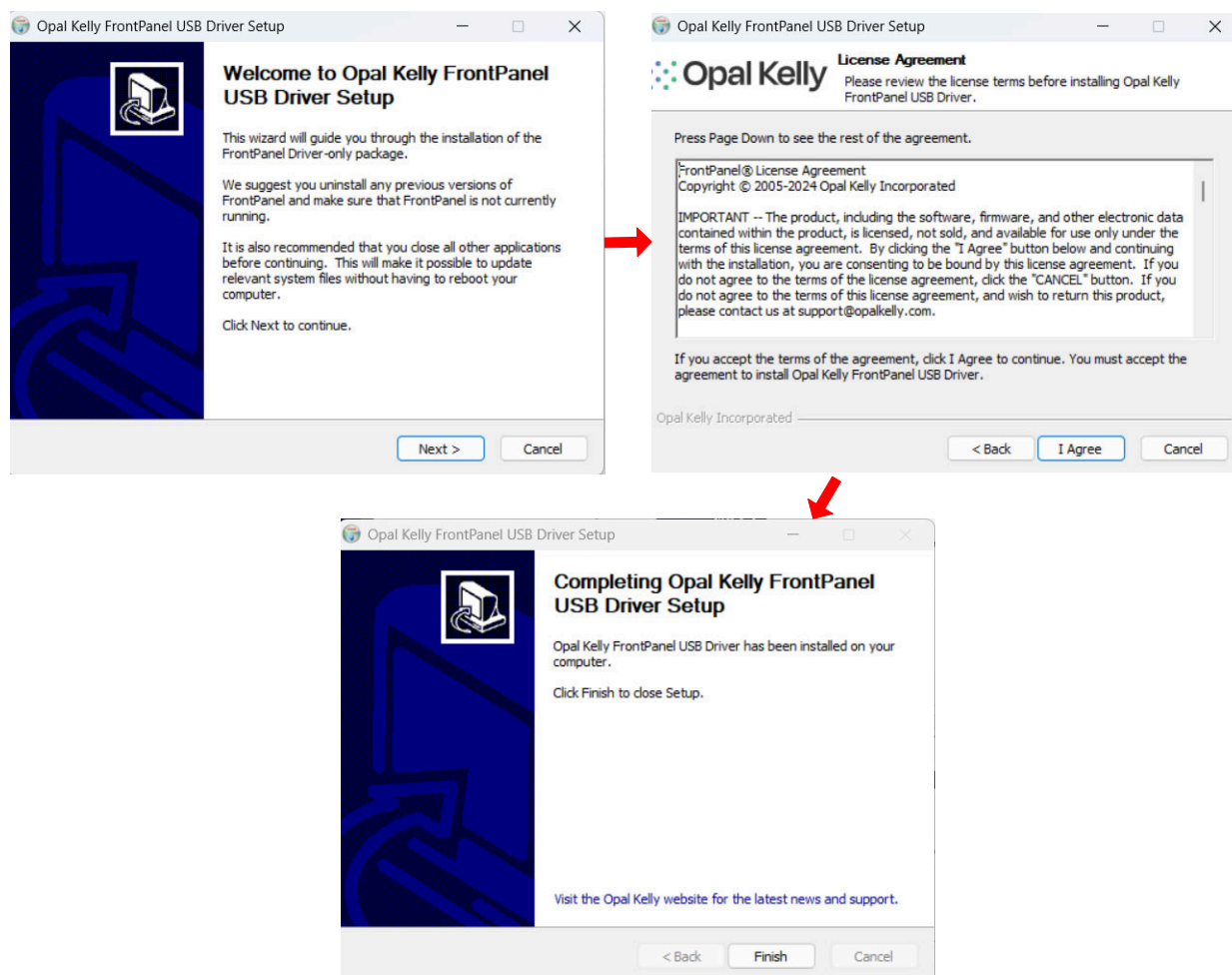


Figure 3-2. Software Installation

3.2 Software Description

To launch the software, locate the downloaded folder and extract the contents. Double-click on the DAC90802EVM GUI executable file. The GUI opens with the main window as shown in DAC90802EVM GUI Home Page.

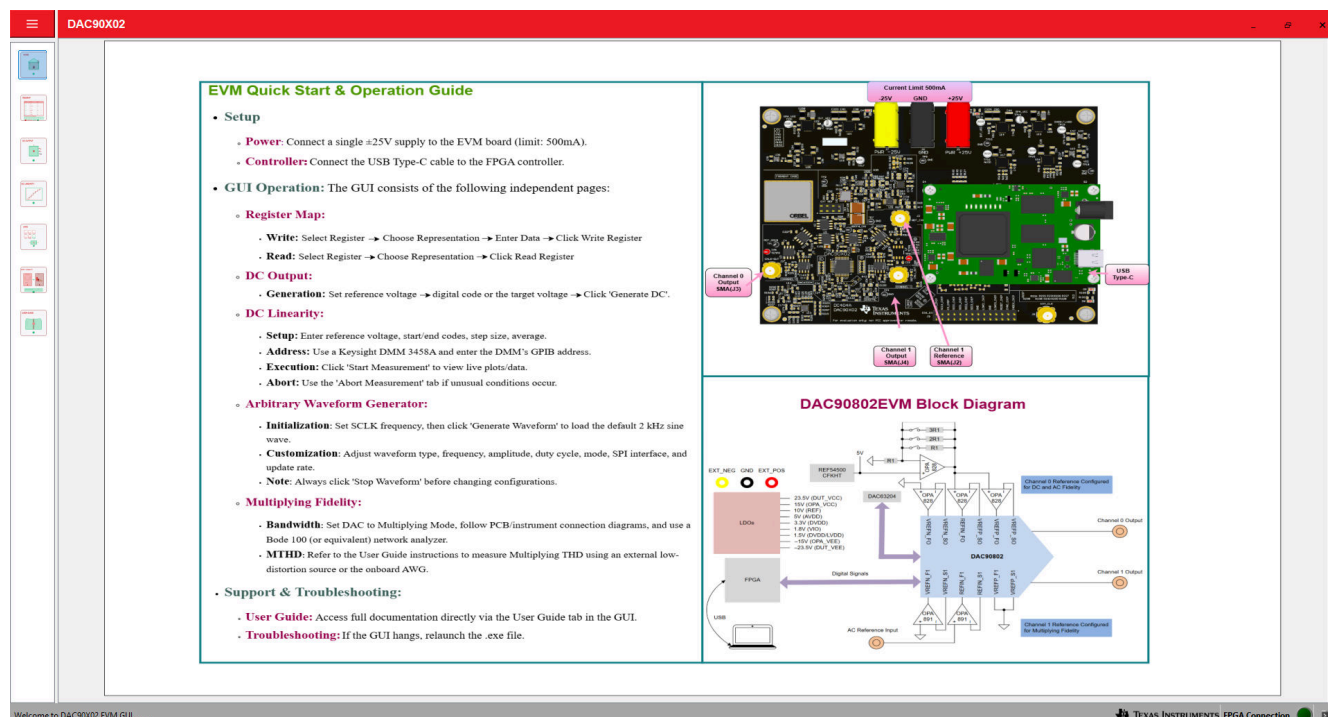


Figure 3-3. DAC90802EVM GUI Home Page

If the status bar LED stays off and the console prints "FPGA configuration failed", refer to DAC90802EVMGUI Connection Detection with FPGA to verify the Opal Kelly front panel driver is installed properly (see GUI Installation), verify no other FPGA devices are connected to the same machine, unplug and reconnect the EVM, relaunch the GUI software, and verify the USB cable connection. If the issue persists, repeat the steps.

Verify that the EVM board is connected to the PC through the provided USB cable. To verify that communication between the GUI and the EVM hardware is established, refer to DAC90802EVMGUI Connection Detection with USB, which shows the status bar at the bottom of the screen. A green connected status indicates that the onboard FPGA controller is communicating with the EVM through USB.

An additional method to verify FPGA connection is to check the RED LEDs on the FPGA mounted on the PCB, which indicate the status of the FPGA connection. Glowing RED LEDs confirms successful FPGA programming and an established connection.

The table below lists all applications supported by the DAC90802EVM GUI.

Table 3-1. DAC90802EVM GUI Supported Application

APPLICATION	DESCRIPTION
Register Read/Write	Provides access to the DAC90802EVM register map, allowing user to read from and write to device registers for configuration and evaluation.
DC output	Enables users to configure and verify the DAC dc output voltage.
DC linearity	Enables measurement of INL and DNL using Keysight 3458A DMM.
Arbitrary waveform generator	Enables generation of various waveform types with configurable parameters.
Multiplying mode	Provides measurement guidance and supporting features for evaluating multiplying mode performance, including multiplying BW and THD.

Table 3-1. DAC90802EVM GUI Supported Application (continued)

APPLICATION	DESCRIPTION
EVM user guide	Provides direct access to the EVM documentation within the GUI for convenient referencing during device evaluation.

Note

The EVM User Guide page provides convenient access to documentation within the application, allowing users to refer to operating and measurement procedures without leaving the GUI.

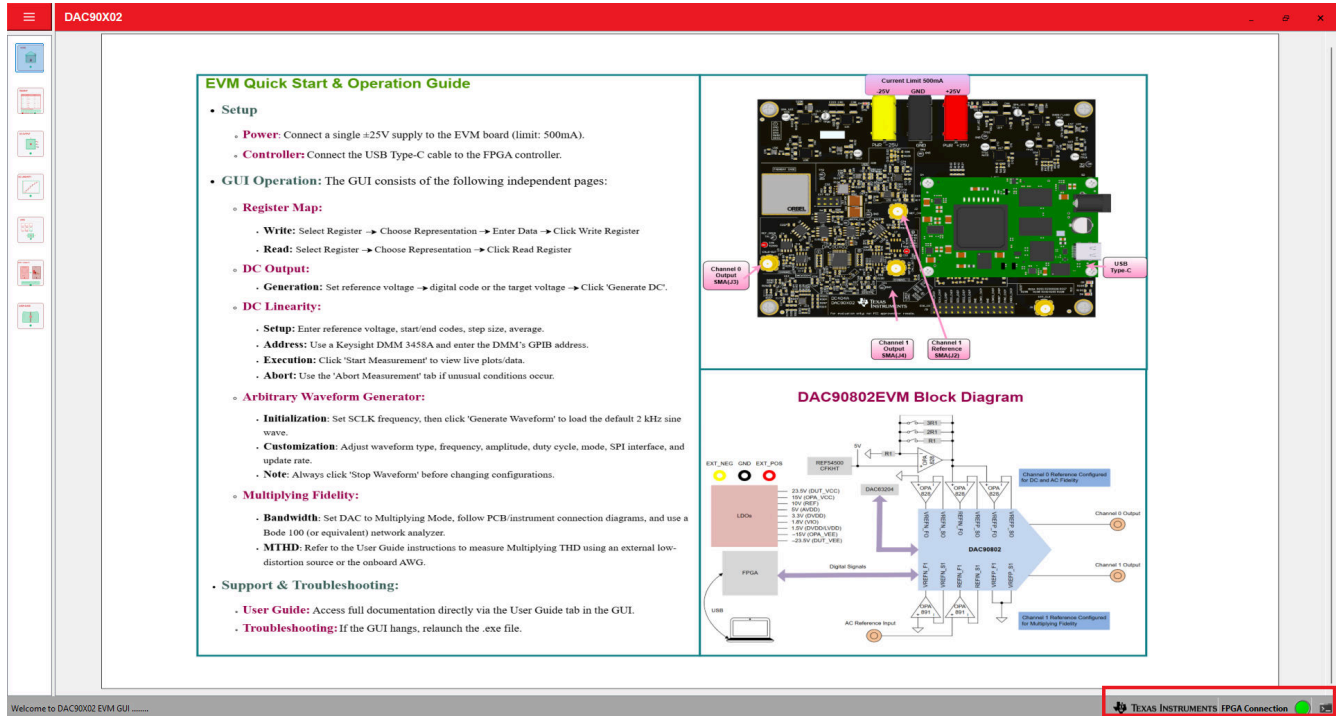


Figure 3-4. DAC90802EVM GUI Connection Detection with USB



3.2.1 DAC90802 Register Page

Figure 3-6 shows the *DAC90802 Register Page* of the DAC90802EVM GUI. The *DAC90802 Register Page* allows direct access to the data registers of the DAC90802EVM device. The GUI handles page address management, allowing seamless access to the registers. The register map section in the center of the page lists all available registers. Directly selecting and clicking on a register enables direct access to the register and associated fields.

Register Name	Register Address	Access	Book	Book Address	Page	Page Address	Block	Block Address
1 NOP	0x0	R	Book 0	0x0	COMMON	0x0	Functional	0x0
2 DEVICE_CFG	0x1	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
3 DEVICE_CTRL	0x2	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
4 CH0_CFG	0x3	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
5 CH1_CFG	0x4	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
6 SPI_CFG	0x5	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
7 CUSTOM_SHAPE_CORRECTION_0	0x6	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
8 CUSTOM_SHAPE_CORRECTION_1	0x7	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
9 ALERT_CFG	0x8	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
10 DAC_DATA_CH0_16	0x9	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
11 DAC_DATA_CH1_16	0xA	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
12 DAC_DATA_CH0_24	0xB	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
13 DAC_DATA_CH1_24	0xC	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
14 DAC_DATA_CH0_18	0xD	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
15 DAC_DATA_CH1_18	0xE	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
16 DAC_DATA_CH0_20	0xF	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0
17 DAC_DATA_CH1_20	0x10	R/W	Book 0	0x0	COMMON	0x0	Functional	0x0

Figure 3-6. DAC90802EVM GUI Register Page

3.2.2 DAC90802 DC Output Page

Figure 3-7 shows the *DAC90802 DC Output page* of the DAC90802EVM GUI. The *DAC90802 DC Output Page* provides two methods for generating dc voltage output at channel 0 of the DAC:

Direct dc voltage generation: Direct dc voltage generation at channel 0 is done by entering either an 18-bit digital code (decimal range 0 to 262143) in the Digital Code tab or the desired dc output voltage in the dc Voltage tab. Upon clicking the Generate DC button, the specified dc voltage is generated at the channel 0 output. Prior to dc voltage generation, the reference voltage applied to channel 0 must be configured in the Set Reference tab of the GUI.

To keep the DAC90802 output within the specified $\pm 21\text{V}$ range, select the appropriate gain setting based on the dc reference voltage (see the [Table 2-2](#) for reference voltage) as follows:

- For a 5V dc reference: All gain settings (1x, 2x, and 4x) are supported.
- For a 10V dc reference: Only 1x and 2x gain settings are supported.
- For a dc reference > 10V: Use the 1x gain setting only.

CSV file-based dc voltage generation: DC voltage generation is accomplished using a CSV file containing hexadecimal data entries in the first column (for example: 0x64AB123000, 0x642B123000, 0x64FB123000, 0x64AB12C000), as shown in [Figure 3-7](#). Specify the CSV file path in the CSV File Path tab, configure the delay interval between successive data transmissions in the delay tab, and click the Generate button to output the dc voltages at channel 0 of the DAC.

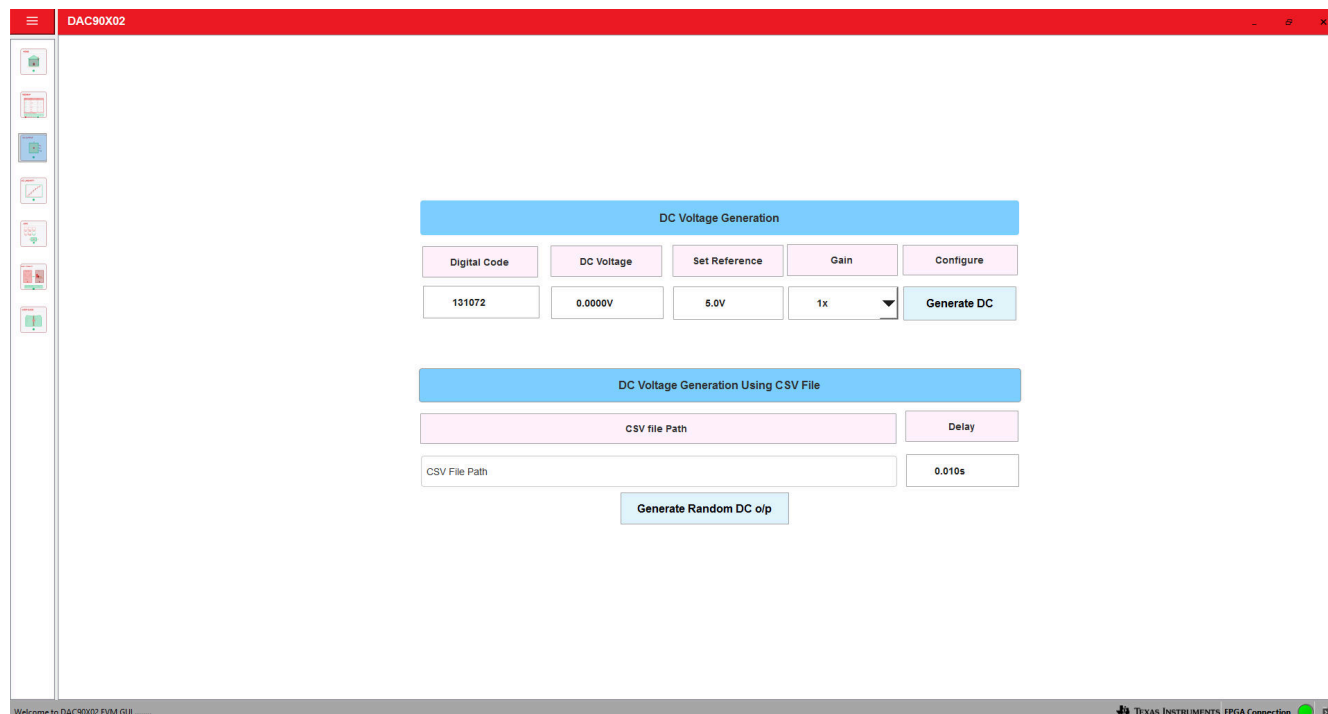


Figure 3-7. DAC90802EVM DC Voltage Page

3.2.3 DC Linearity Page

Figure 3-8 shows the *DC Linearity Page* of the DAC90802EVM GUI. The *DC Linearity Page* provides dc linearity measurement of the DAC90802EVM using the Keysight DMM 3458A instrument.

To configure and perform DC linearity measurement:

- Enter the reference voltage in the Reference Voltage tab.
- Enter the start code, end code, code step, and ensemble average in the respective tabs.
- Enter the GPIB address of the Keysight 3458A DMM (for example: GPIB0::23::INSTR) in the Keysight 3458A GPIB Address tab.
- Click the Start Measurement button to initiate the measurement.

To verify the DAC output remains within the specified $\pm 21V$ range, select the appropriate gain setting (for more detail see [Section 3.2.2](#)) based on the reference voltage (see the [Table 2-2](#) for reference voltage).

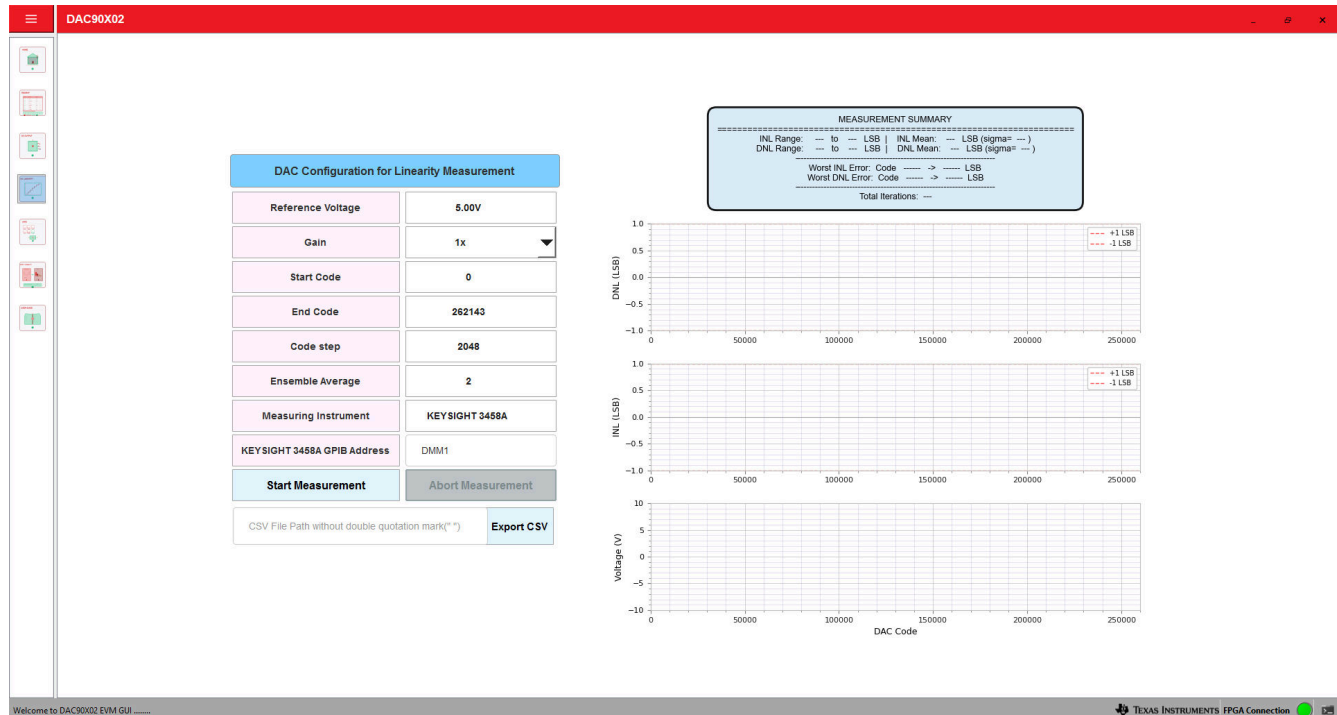


Figure 3-8. DAC90802EVM GUI DC Linearity Page

Figure 3-9 shows the *DC Linearity Page* of the DAC90802EVM GUI during measurement phase.

Upon starting the measurement, the GUI displays live plots and measurement data in a piecewise manner, including measurement summary, INL plot, DNL plot, and output voltage information.

Figure 3-10 shows the *DC Linearity Page* upon completion of the measurement, which includes the measurement summary, INL plot, DNL plot, and output voltage plot.

Note

After clicking the Start Measurement button, an Abort Measurement tab becomes available. If unusual conditions occur during measurement, the measurement can be aborted at any time by clicking the tab.

Note

Upon completion of the measurements, the acquired data including plots, INL and DNL summary can be exported to a CSV file. Specify the folder path and a valid CSV file name in the export configuration, then click the Export tab to save the data to the CSV file.

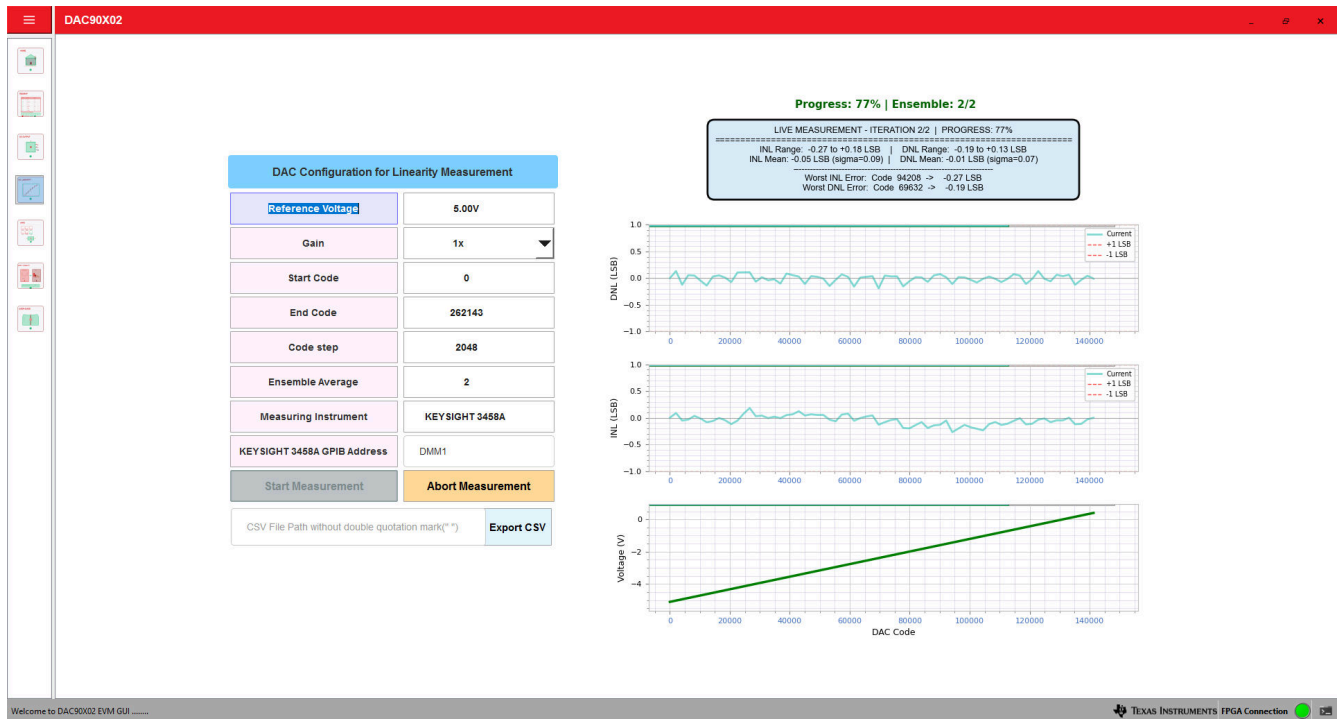


Figure 3-9. DAC90802EVM GUI DC Linearity Page During Measurement



Figure 3-10. DAC90802EVM GUI DC Linearity Page After Measurement

3.2.4 Arbitrary Waveform Generation Page

The *Arbitrary Waveform Generator (AWG) Page* provides an interface for configuring the DAC and generating analog waveforms. The AWG page enables users to configure the device operating mode, communication interface, waveform parameters, and update rate from the GUI. The AWG supports sinusoidal, square, and triangular waveforms. By adjusting waveform parameters such as amplitude and duty cycle, the GUI can generate additional waveform variants including sawtooth, unipolar, bipolar, symmetric, and asymmetric waveforms.

The AWG page also provides a waveform preview and a configuration summary, allowing users to verify all settings before waveform generation as shown in [Figure 3-11](#).

To verify the DAC output remains within the specified $\pm 21V$ range, select the appropriate gain setting (for more detail see [Section 3.2.2](#)) based on the reference voltage (see the [Table 2-2](#) for reference voltage).

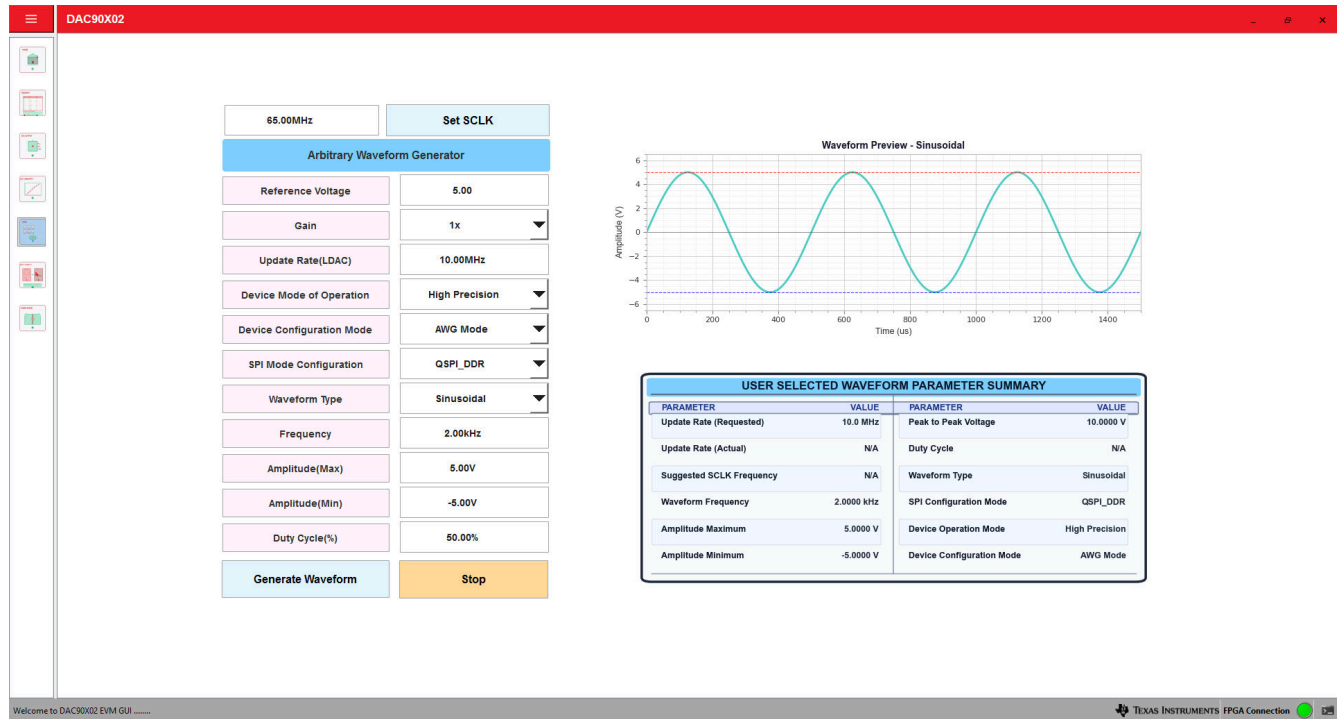


Figure 3-11. DAC90802EVMGUI Arbitrary Waveform Generation Page

3.2.4.1 Quick Start

1. Configure SCLK frequency: Enter the desired serial clock frequency. Click on the set SCLK tab to generate the required serial clock frequency. SCLK determines the available update rates.
2. Click on generate waveform tab: Initializes the AWG using the default configuration (see the [Table 3-2](#) for default parameters).
3. Configure the desired waveform parameters: Modify the device mode operation, device configuration, SPI, waveform type, frequency, amplitude, duty cycle, and DAC update rate as required.
4. Click generate waveform: Applies the selected configuration and starts waveform generation.
5. Click stop waveform: Stops the active waveform before changing the operating configuration or generating a different waveform.

3.2.4.2 GUI Control Reference

[Table 3-2](#) explains required details to use the AWG page of the EVM GUI parameters from SCLK to duty cycles.

Table 3-2. DAC90802EVM GUI Control Reference

PARAMETER	DEFAULT PARAMETER	PARAMETER OPTION	DESCRIPTION
SCLK	65MHz	3MHz to 66MHz	Sets the serial clock frequency used for DAC communication. The serial clock frequency must be configured before waveform generation.
Reference voltage	5V	5V, 10V, 15V, 20V	Selects reference voltage by using appropriate jumper(SH-J) through gain amplifier U2
Update rate	7.22MHz	100kHz to 33MHz	Selecting appropriate SCLK and SPI configuration helps to generate required update rate.
Device mode of operation	High precision	High precision, high speed	High precision: 18-bit DAC resolution is selected. High speed: 16-bit DAC resolution is selected.
Device configuration mode	AWG mode	AWG mode, fast settling, multiplying mode	DAC channel is configured in the selected mode.
SPI configuration	QSPI_DDR	CSPI_SDR, CSPI_DDR, DSPI_SDR, DSPI_DDR, QSPI_SDR, QSPI_DDR, QSPI_DDR_STREAM	DAC is configured in selected SPI mode.
Waveform type	Sinusoidal wave	Sinusoidal wave, rectangular wave and square wave	Select the type of waveform. Default waveform type is sinusoidal waveform.
Frequency	2kHz	100Hz to 1MHz	Any output frequency within the appropriate range can be generated.
Minimum amplitude	-5V	-20V to -0.1V	Based on the reference voltage(see the Table 2-2), any negative reference voltage can be selected digitally.
Maximum amplitude	5V	0.1V to 20V	Based on the reference voltage (see the Table 2-2), any positive reference voltage can be selected digitally.
Duty cycle	50%	0% - 100%	Controls waveform symmetry for square and triangular waveforms. Duty cycle is not applicable for sinusoidal waveform type.

3.2.4.3 Update Rate

The DAC update rate determines the waveform sampling rate and depends on the selected SCLK frequency and SPI. [Table 3-3](#) shows the SPI, maximum update rate and device mode of operation supported by DAC90802EVM GUI. QSPI DDR STREAM is optimized to demonstrate device maximum update rate as per the design specification. Other SPI can be further optimized to get better update rate. For more information see the datasheet of the DAC90802EVM.

Table 3-3. DAC90802EVM GUI Control Reference

SPI	MAXIMUM UPDATE RATE	DEVICE MODE OF OPERATION
CSPI SDR	SCLK/37	High precision
CSPI DDR	SCLK/21	High precision
DSPI SDR	SCLK/21	High precision
DSPI DDR	SCLK/13	High precision
QSPI SDR	SCLK/13	High precision
QSPI DDR	SCLK/9	High precision
QSPI DDR STREAM	SCLK/3	High precision
QSPI DDR STREAM	SCLK/2	High speed

Example: For an SCLK frequency of 66MHz:

- High speed mode → 33MHz DAC update rate.
- High precision + QSPI DDR → 7.333MHz DAC update rate.
- High precision + QSPI DDR STREAM → 22MHz DAC update rate.

3.2.5 Multiplying Mode Page

The *Multiplying Mode page* is designed to evaluate the multiplying bandwidth and fidelity of the DAC on Channel 1. The *Multiplying Mode page* provides the recommended hardware connections and measurement procedure required to characterize the multiplying bandwidth using a network analyzer. In addition to bandwidth characterization channel 1 is also usable for evaluating the multiplying total harmonic distortion (MTHD).

3.2.5.1 Multiplying Bandwidth Measurement Setup

Figure 3-12 illustrates the recommended connections and instructions for multiplying bandwidth measurement using a network analyzer (bode 100 network analyzer). Verify all procedural instructions are completed prior to initiating the measurement:

1. Calibrate the measuring instruments before connecting to the EVM for measurement.
2. Connect the network analyzer as shown in Figure 3-12.
3. Configure the desired frequency sweep in the measuring instrument.
4. Configure the DAC in multiplying mode by clicking on the Configure tab in the GUI page.
5. Measurement can now be started.

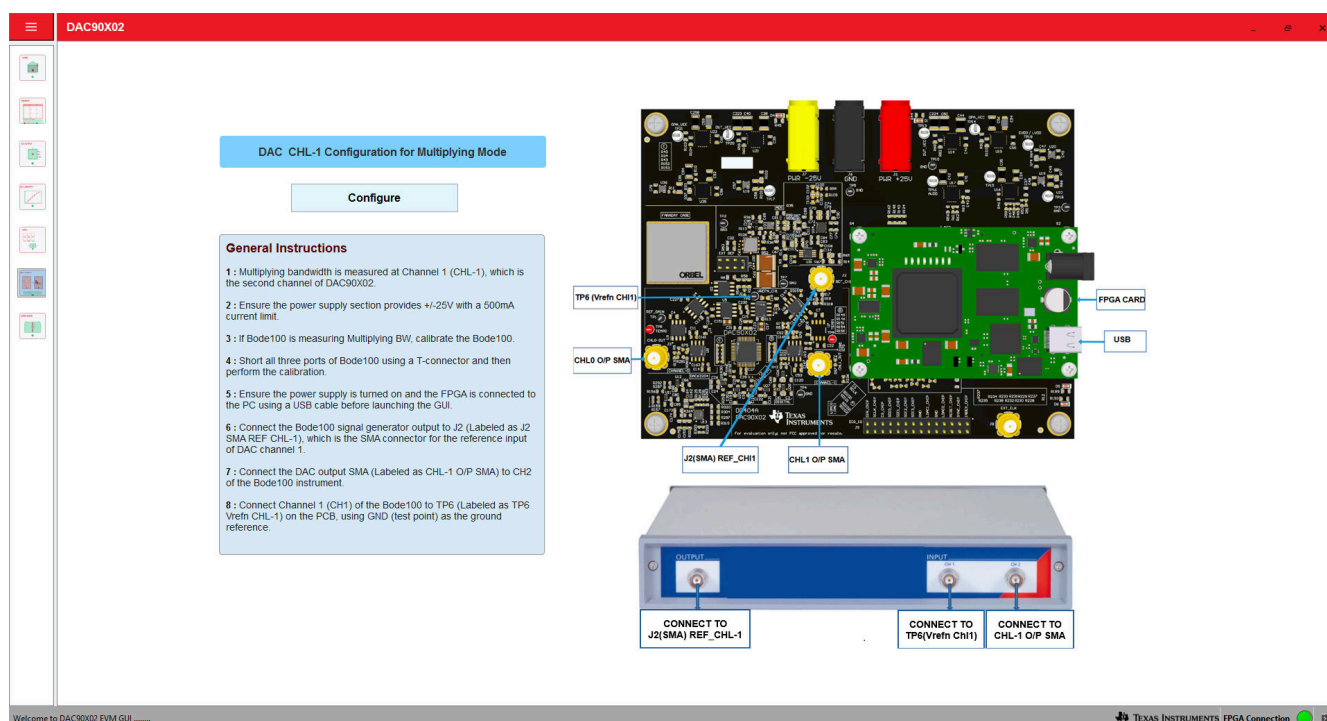


Figure 3-12. DAC90802EVM GUI Multiplying Mode Page

3.2.5.2 Multiplying THD Measurement

The multiplying THD is evaluated using either of the following methods:

1. External Precision Source: Use a low-distortion sinusoidal source (for example, APx555) as the DAC reference input.
 - Configure the DAC in multiplying mode by clicking on the configure tab of the GUI.
 - Apply the external signal to the channel 1 reference SMA (J2).
 - Measure the DAC output at channel 1 SMA (J4) using a distortion analyzer (APx555).
2. AWG loopback of channel 0:
 - Open the AWG page and generate the desired sine wave.
 - The GUI automatically configures channel 0 in AWG mode and channel 1 in multiplying mode.
 - Connect the channel 0 Output SMA (J3) to the channel 1 reference SMA (J2) using a SMA to SMA cable.
 - Measure the DAC output at channel 1 SMA (J4) using a distortion analyzer (APx555).

4 Hardware Design Files

4.1 Schematics

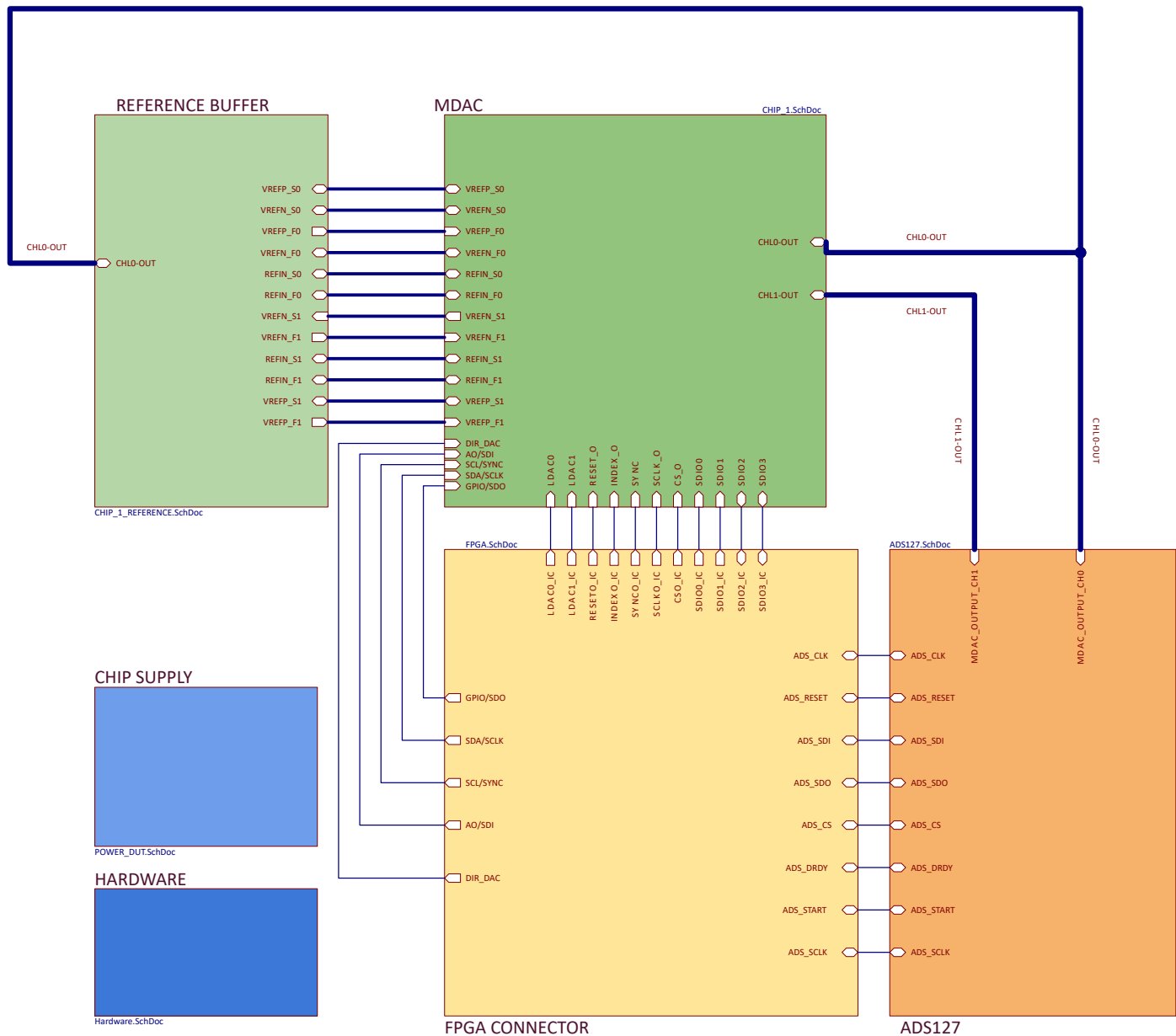


Figure 4-1. DAC90802EVM Schematic: Top Level

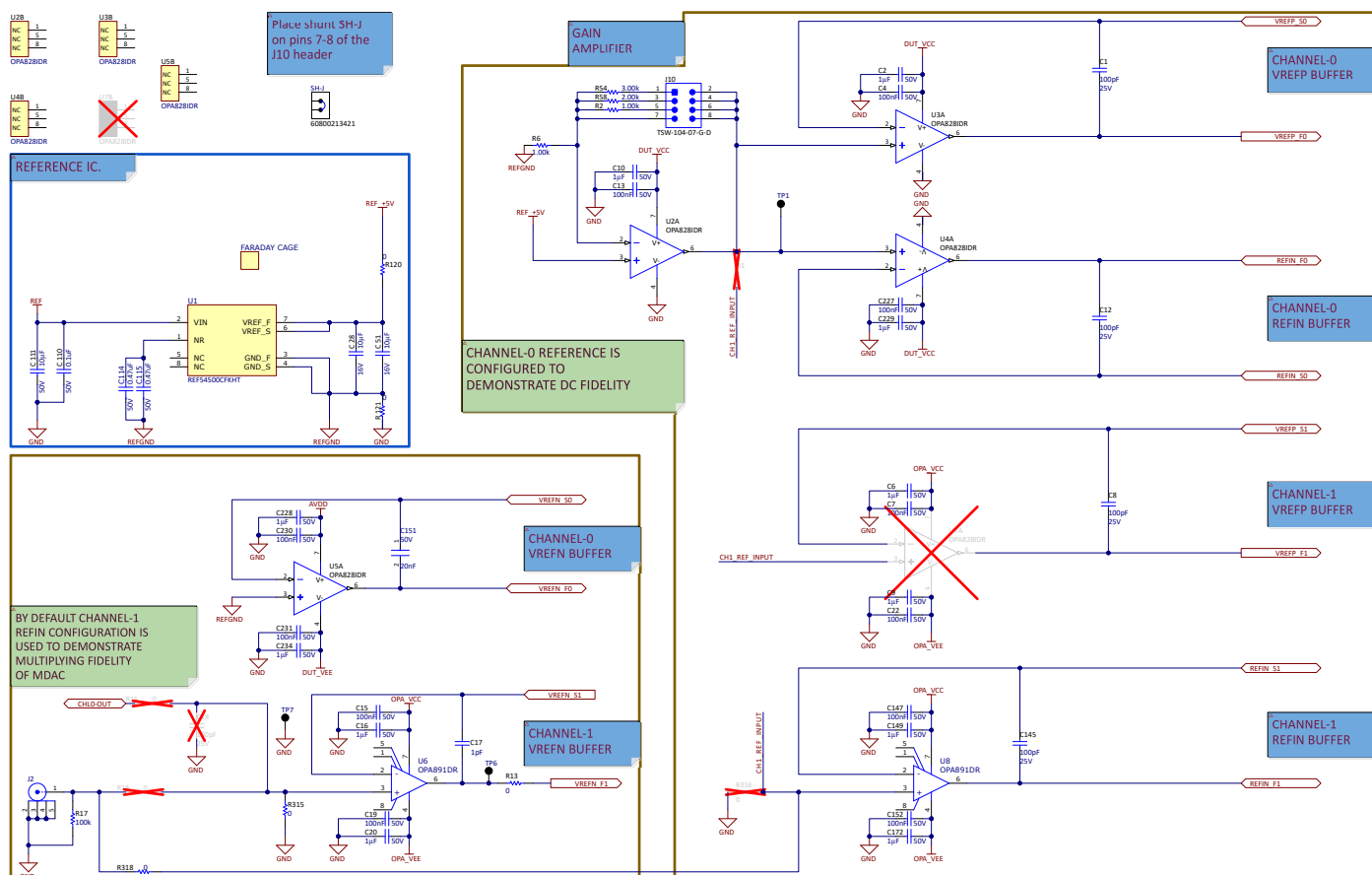


Figure 4-2. DAC90802EVM Schematic: Reference Section

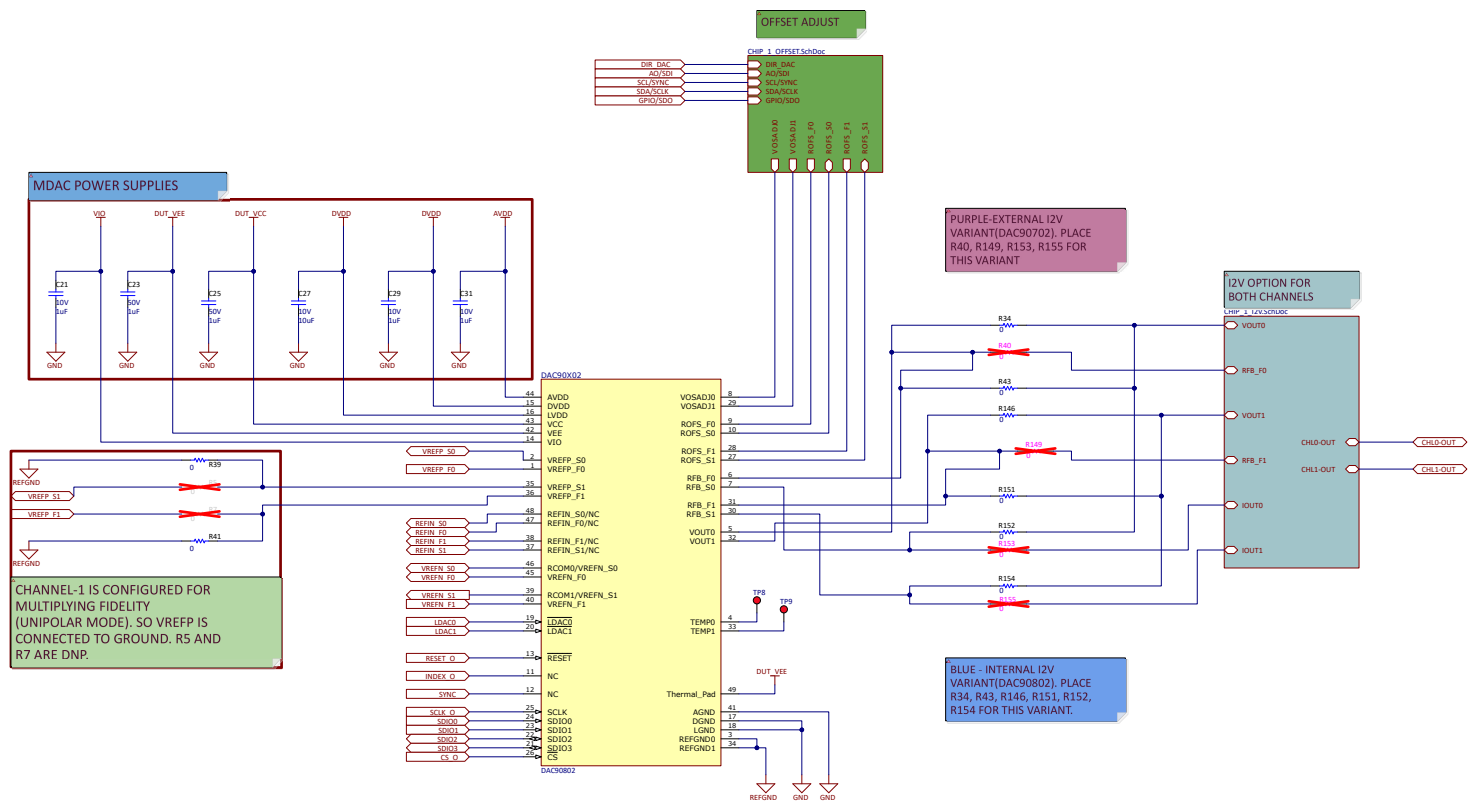


Figure 4-3. DAC90802EVm Schematic: DAC90802 Socket and Power Supplies

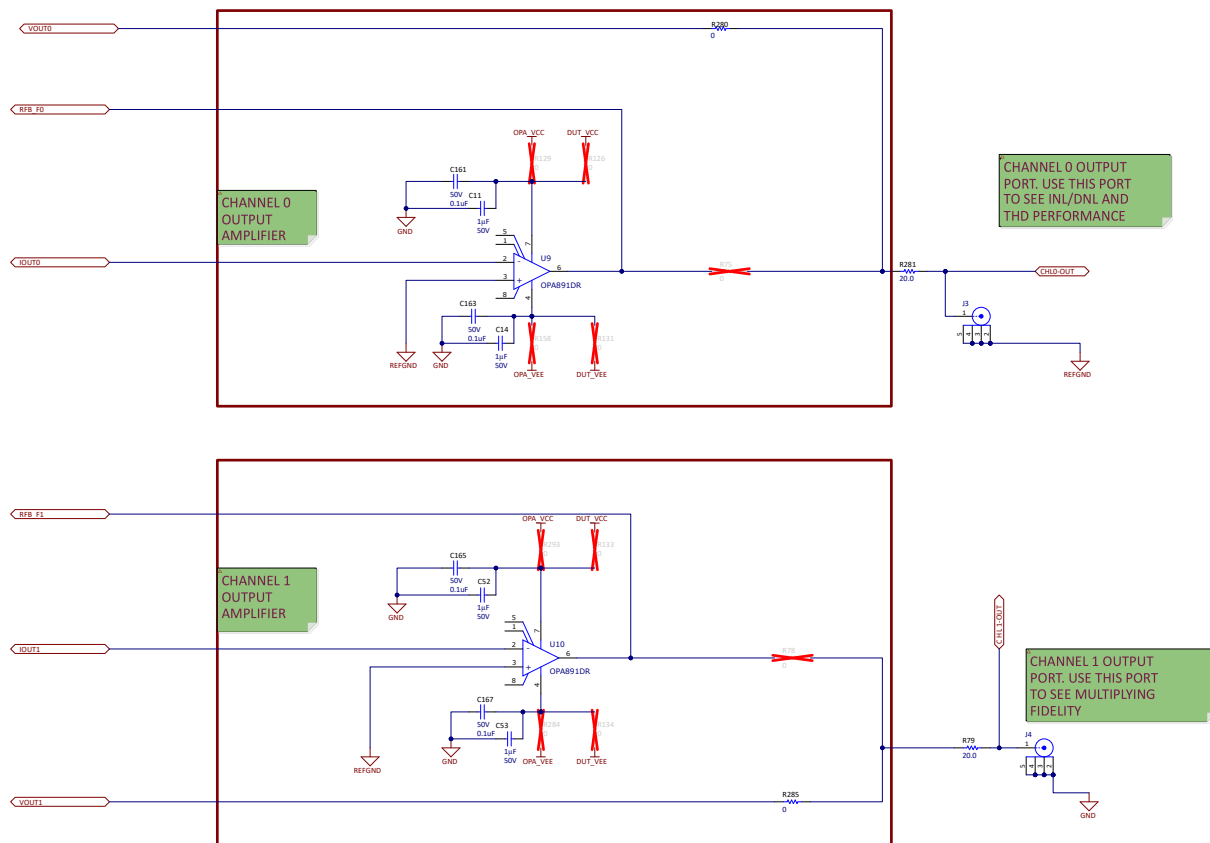


Figure 4-4. DAC90802EVM Schematic: Output



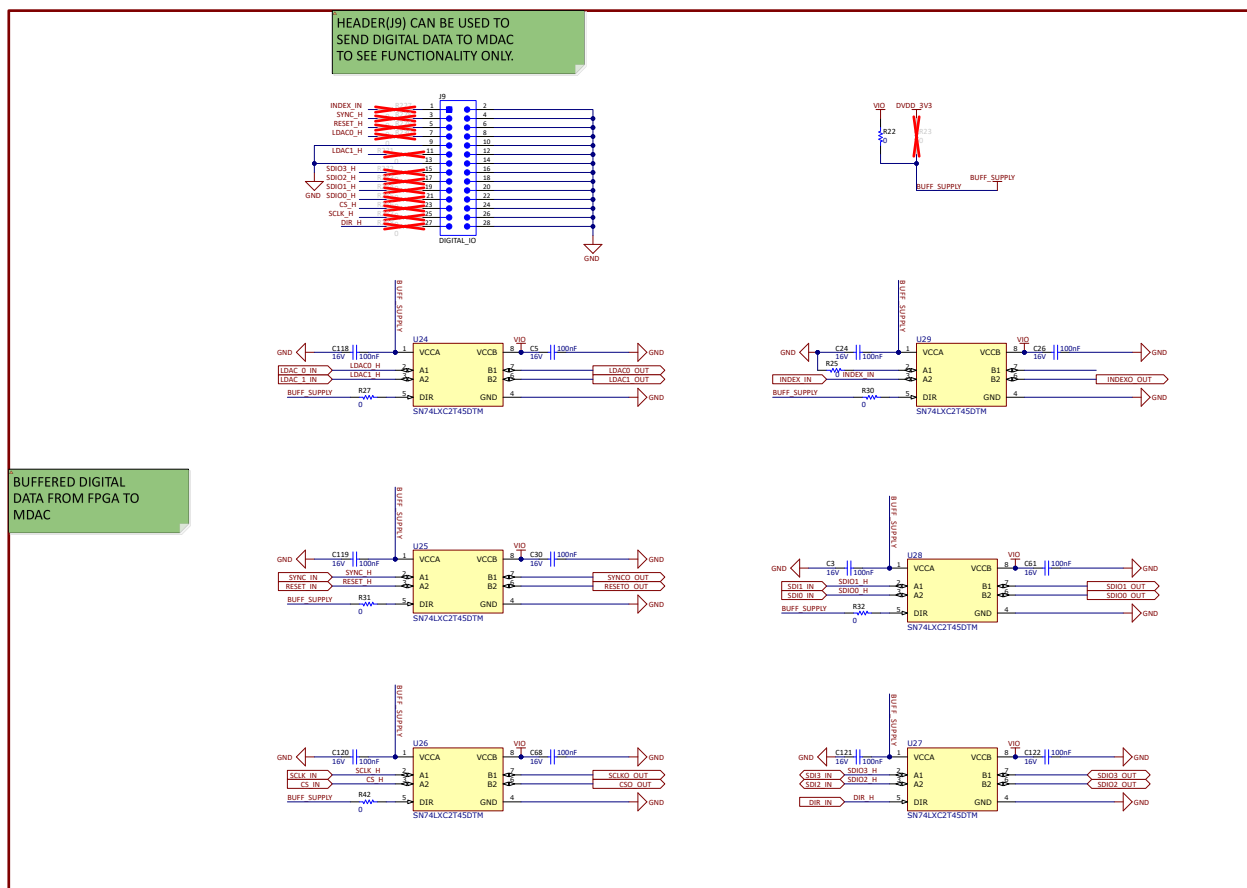


Figure 4-6. DAC90802EVM Schematic: Digital Buffers

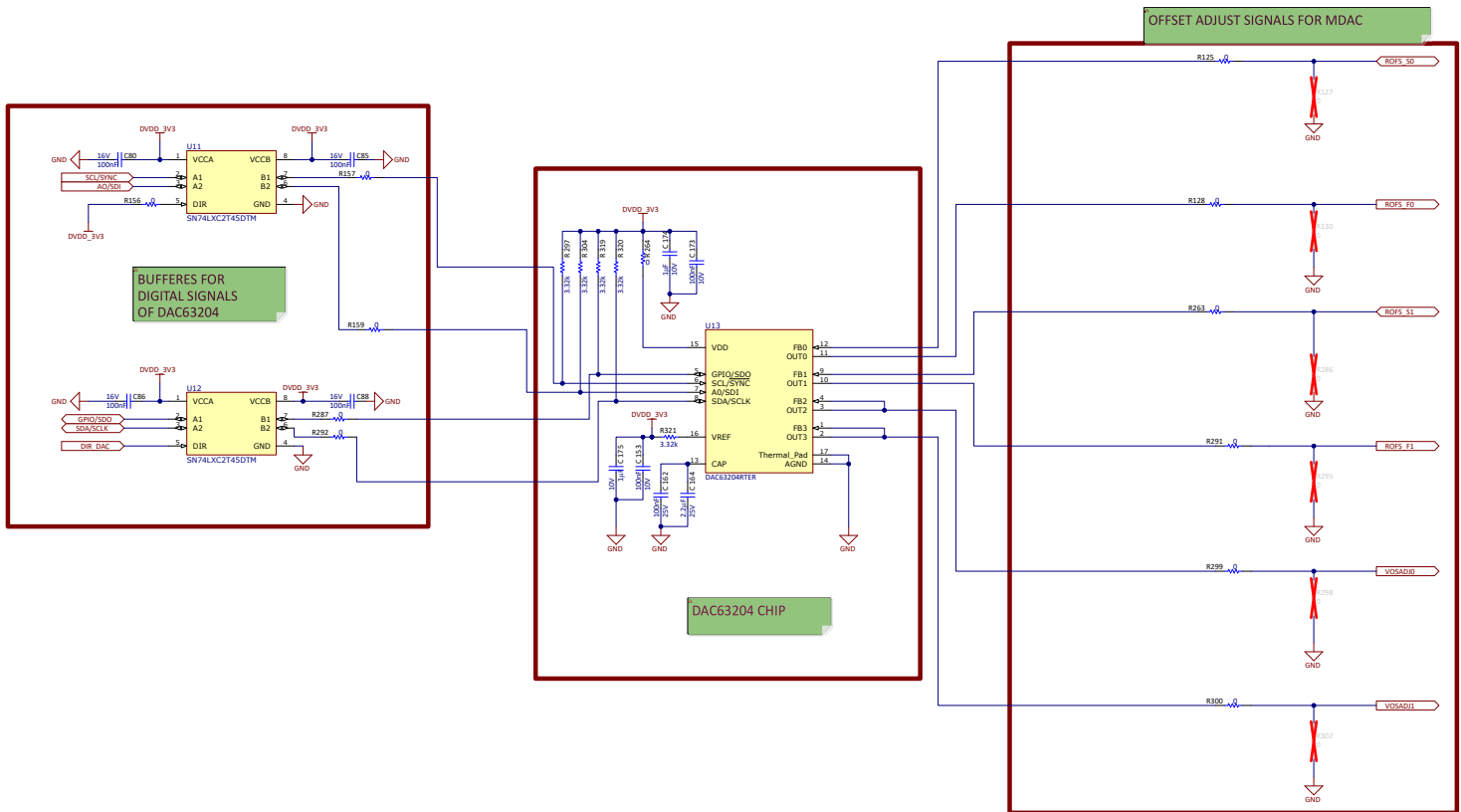


Figure 4-7. DAC90802EVM Schematic: Offset Adjustment

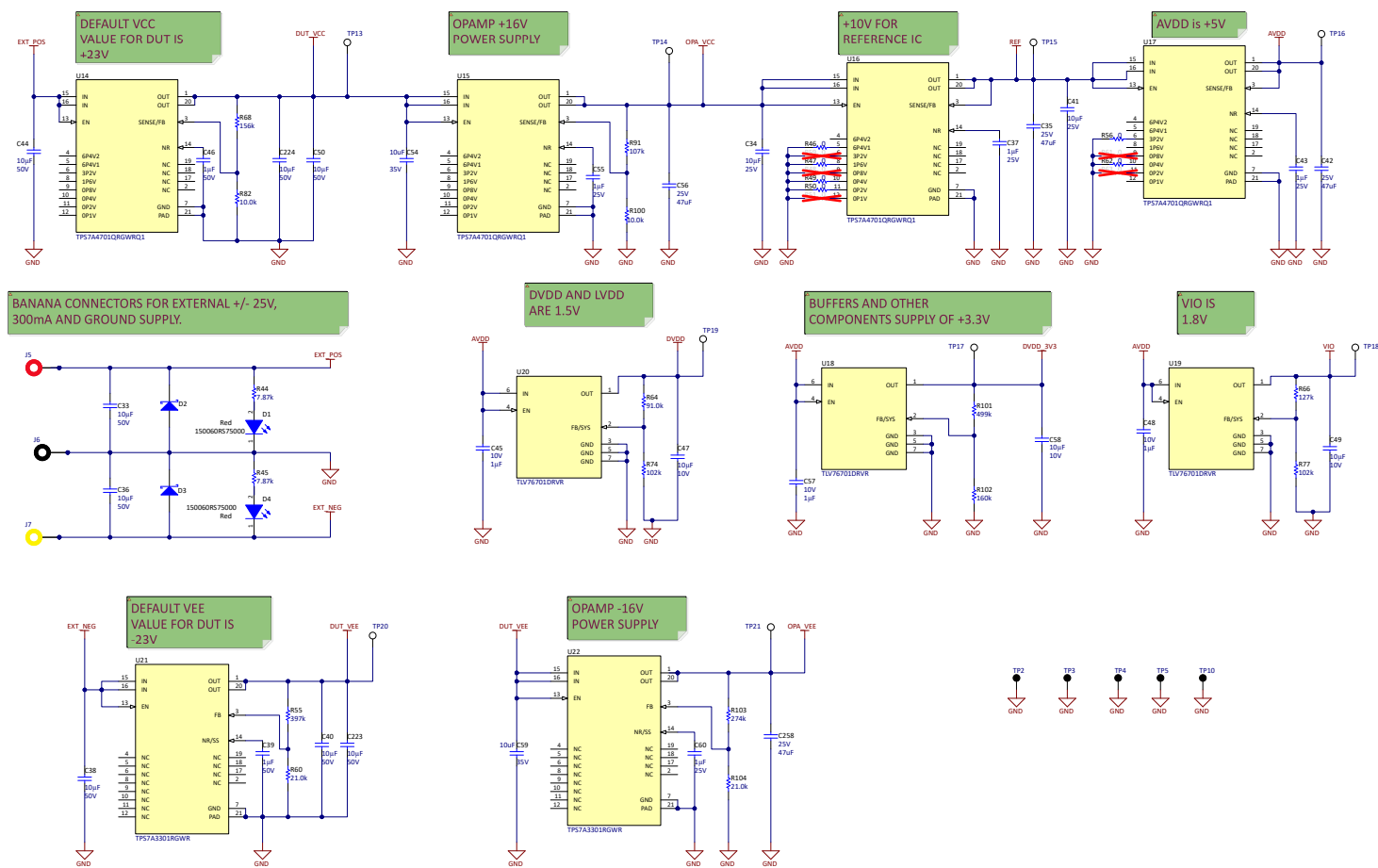
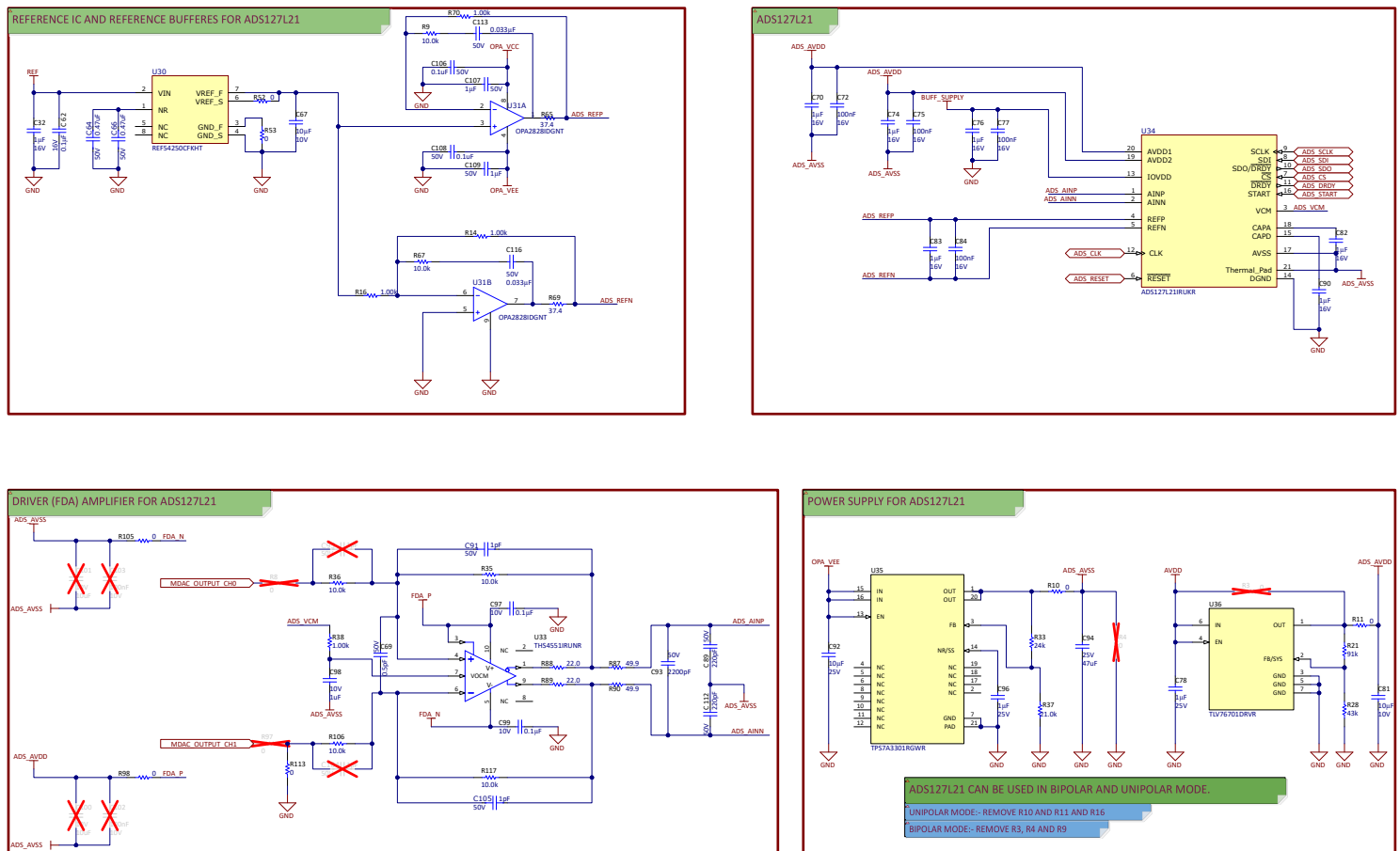


Figure 4-8. DAC90802EVM Schematic: Power Supply



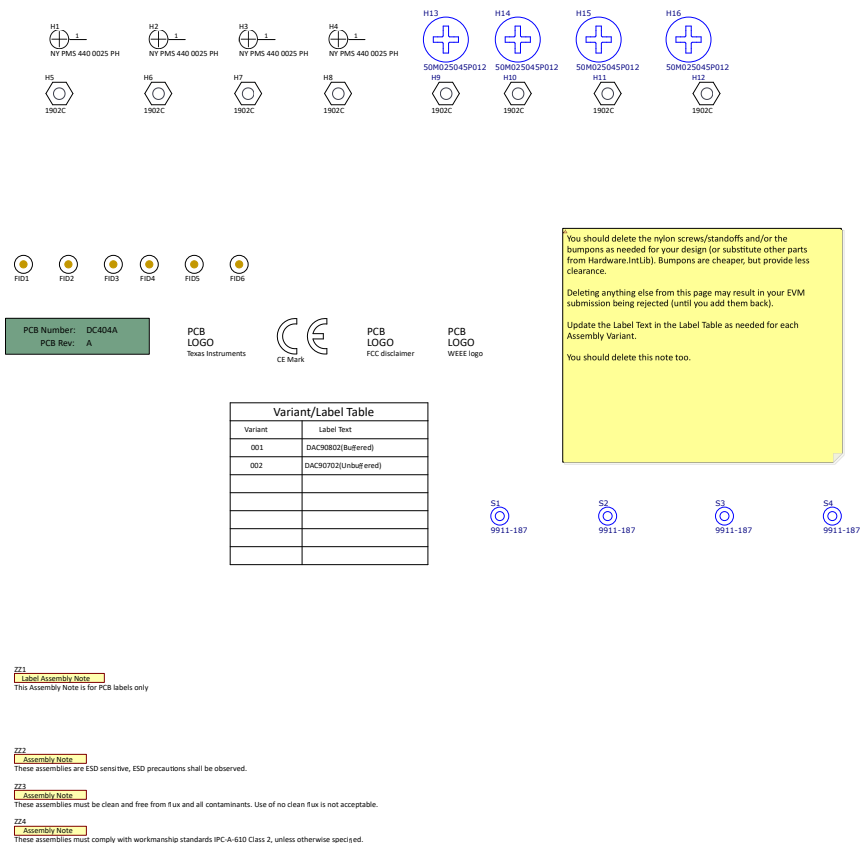


Figure 4-10. DAC90802EVM Schematic: Hardware

4.2 PCB Layouts

Figure 4-11 through Figure 4-20 show the DAC90802EVM board layout.

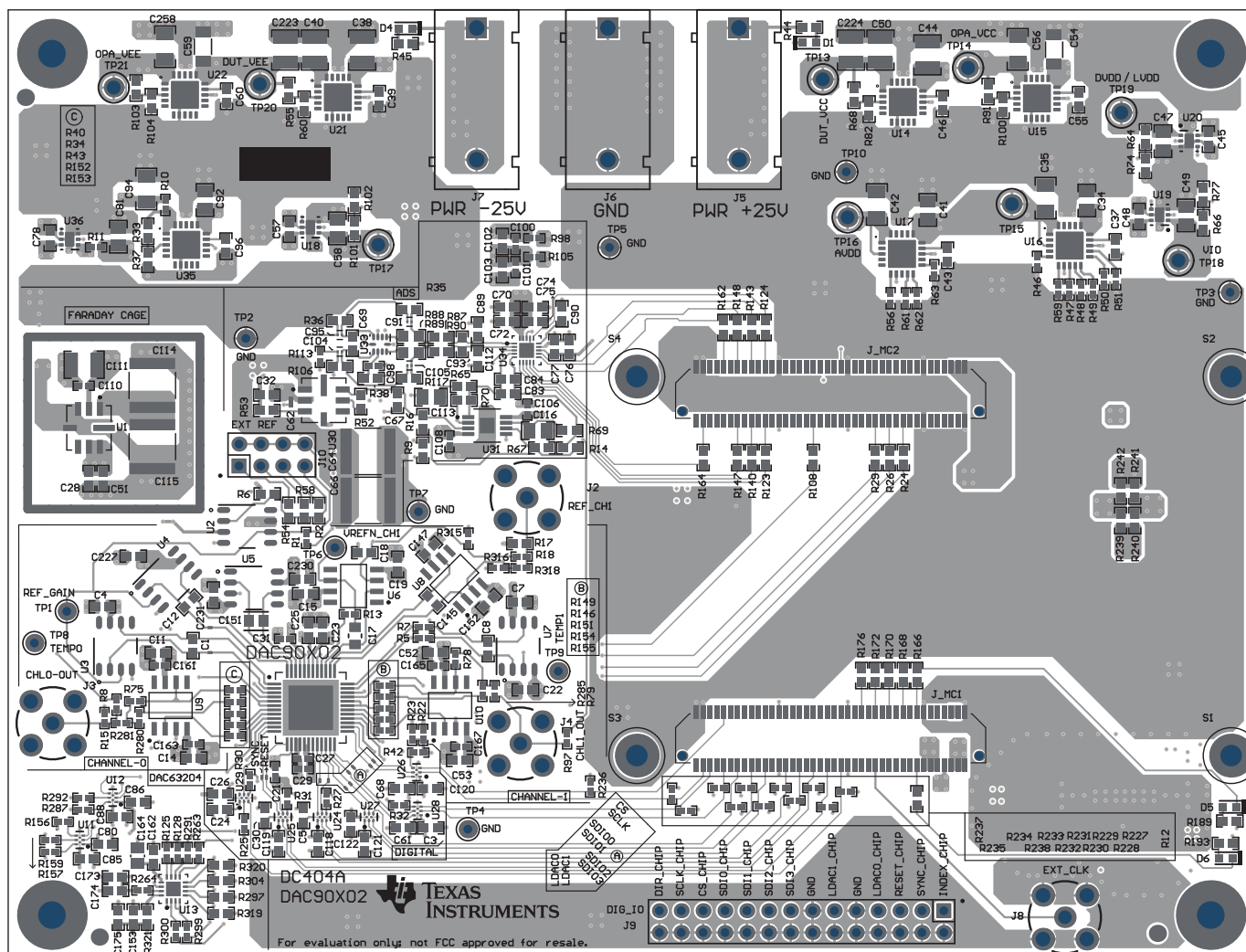


Figure 4-11. DAC90802EVM PCB Top Composite View

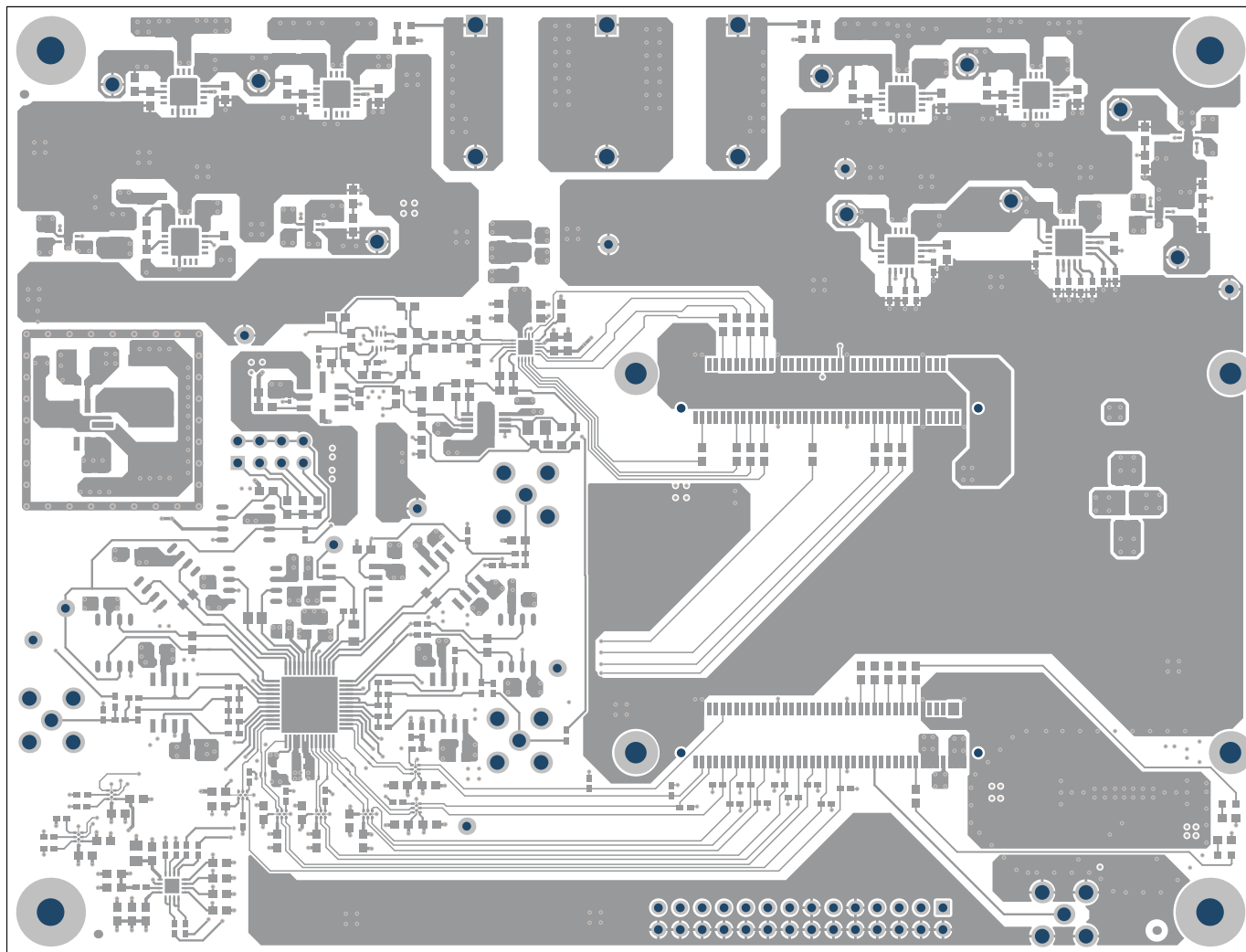


Figure 4-12. DAC90802EVM Top Layer Layout

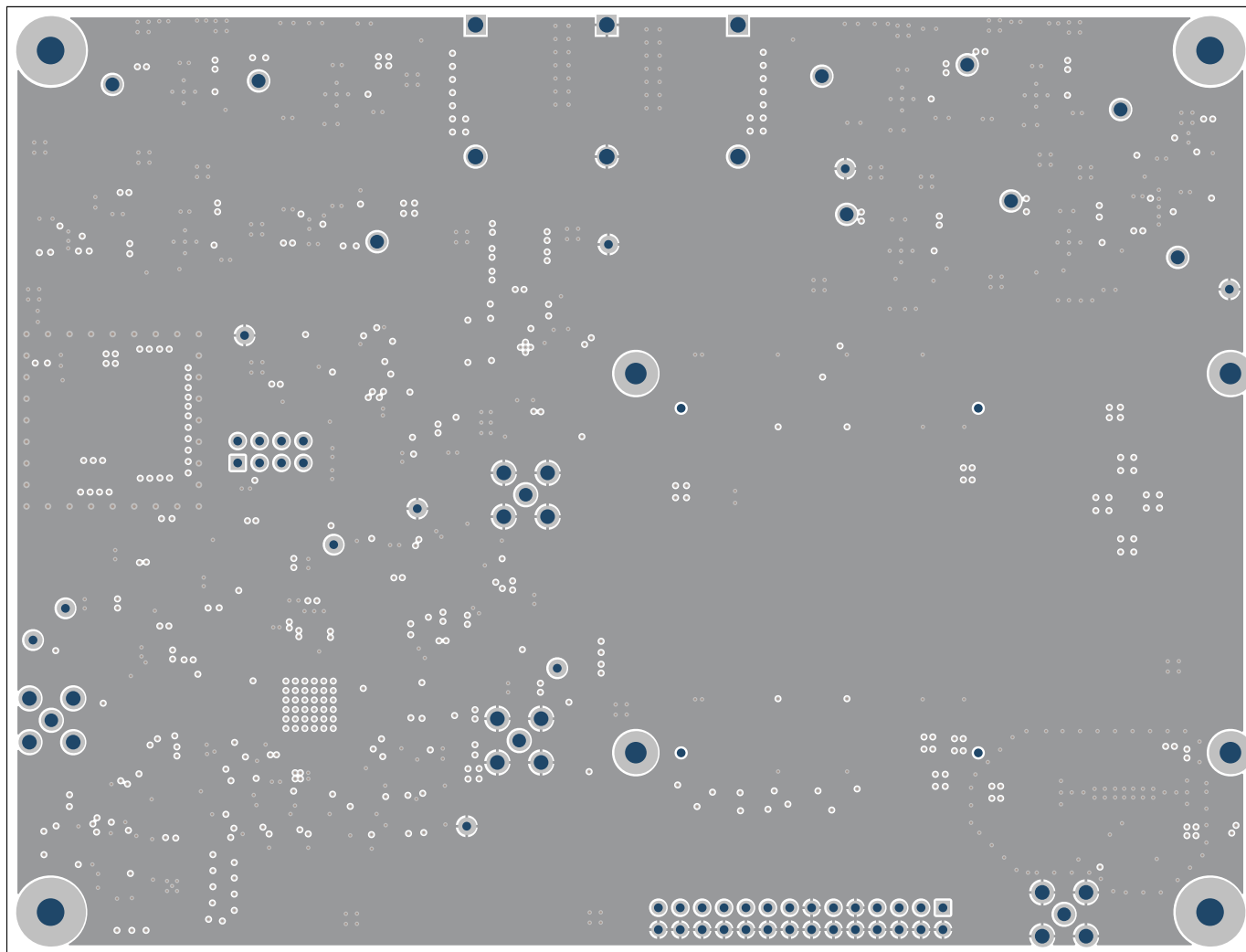


Figure 4-13. DAC90802EVM PCB Ground Layer 2 Layout

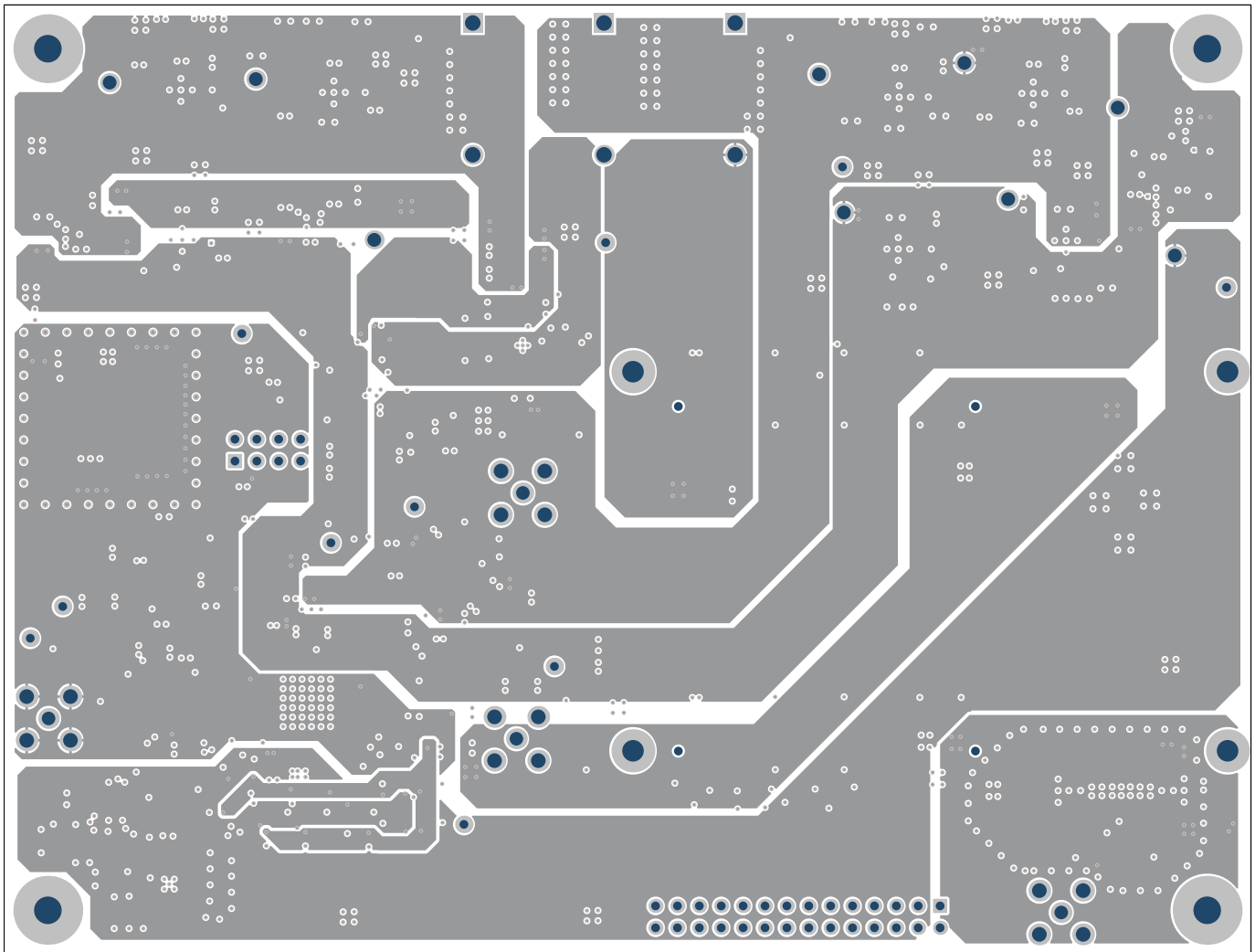


Figure 4-14. DAC90802EVM PCB Power Layer 3 Layout

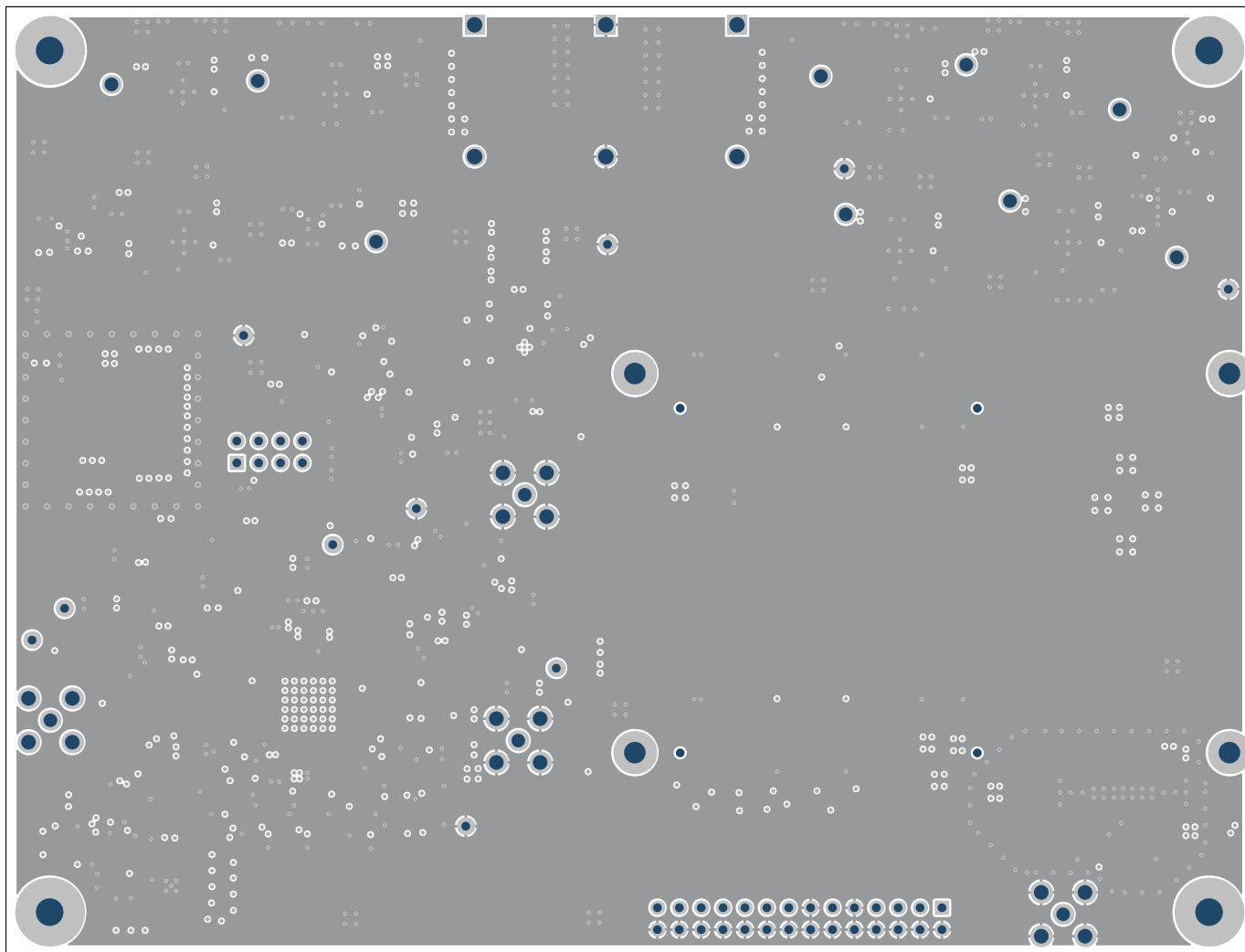


Figure 4-15. DAC90802EVM PCB Ground Layer 4 Layout

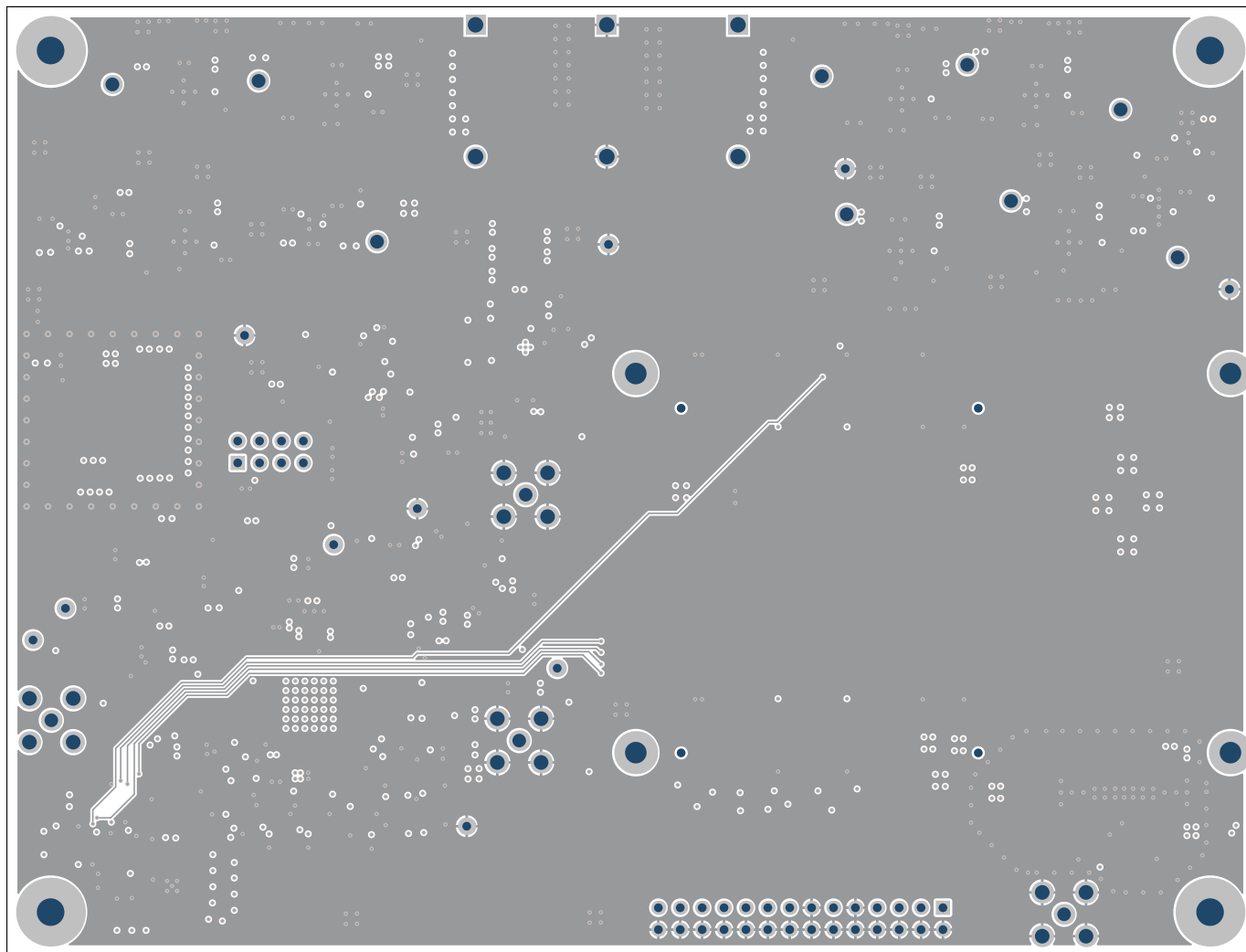


Figure 4-16. DAC90802EVM PCB Ground and Signal Layer 5 Layout

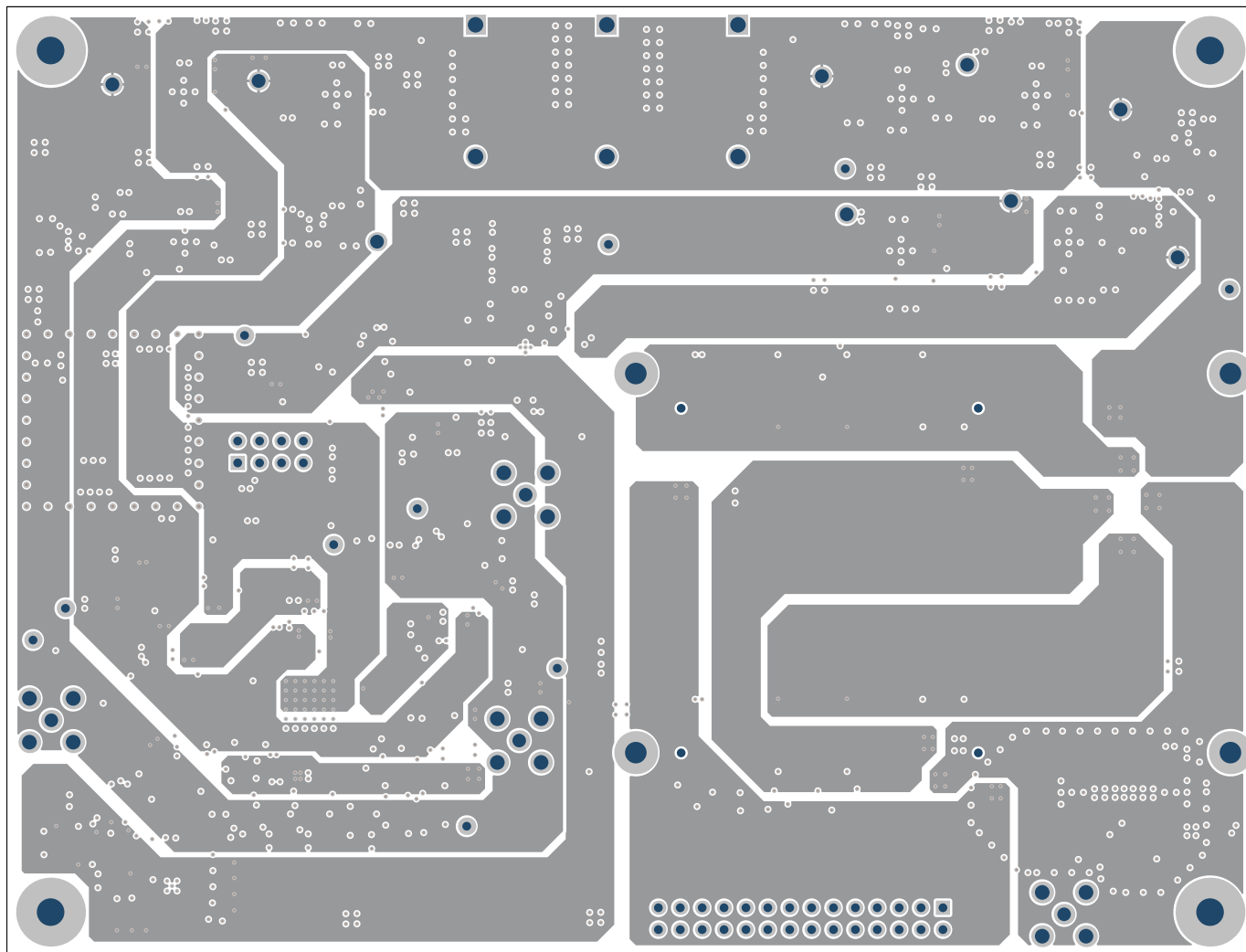


Figure 4-17. DAC90802EVM PCB Power Layer 6 Layout

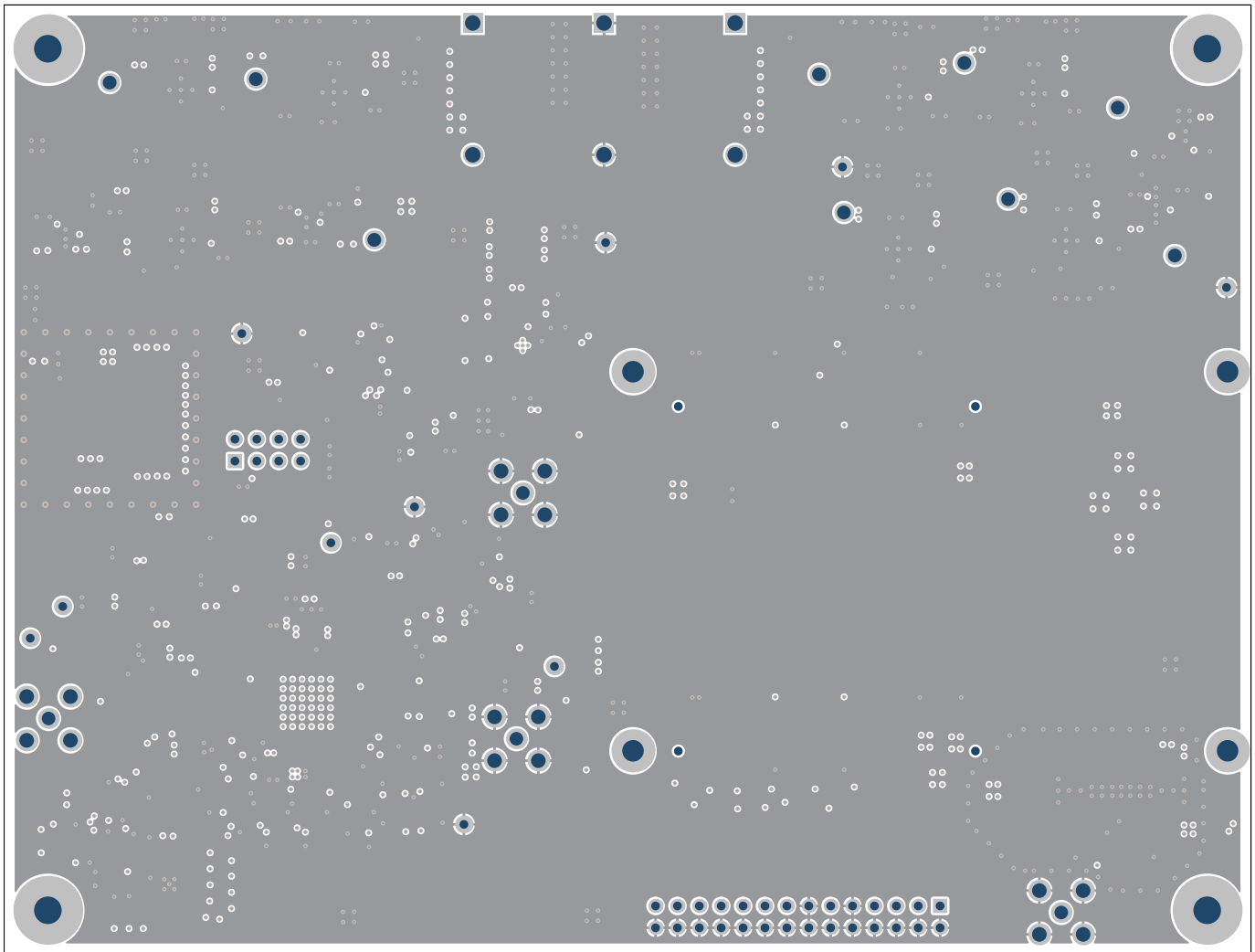


Figure 4-18. DAC90802EVM PCB Ground Layer 7 Layout

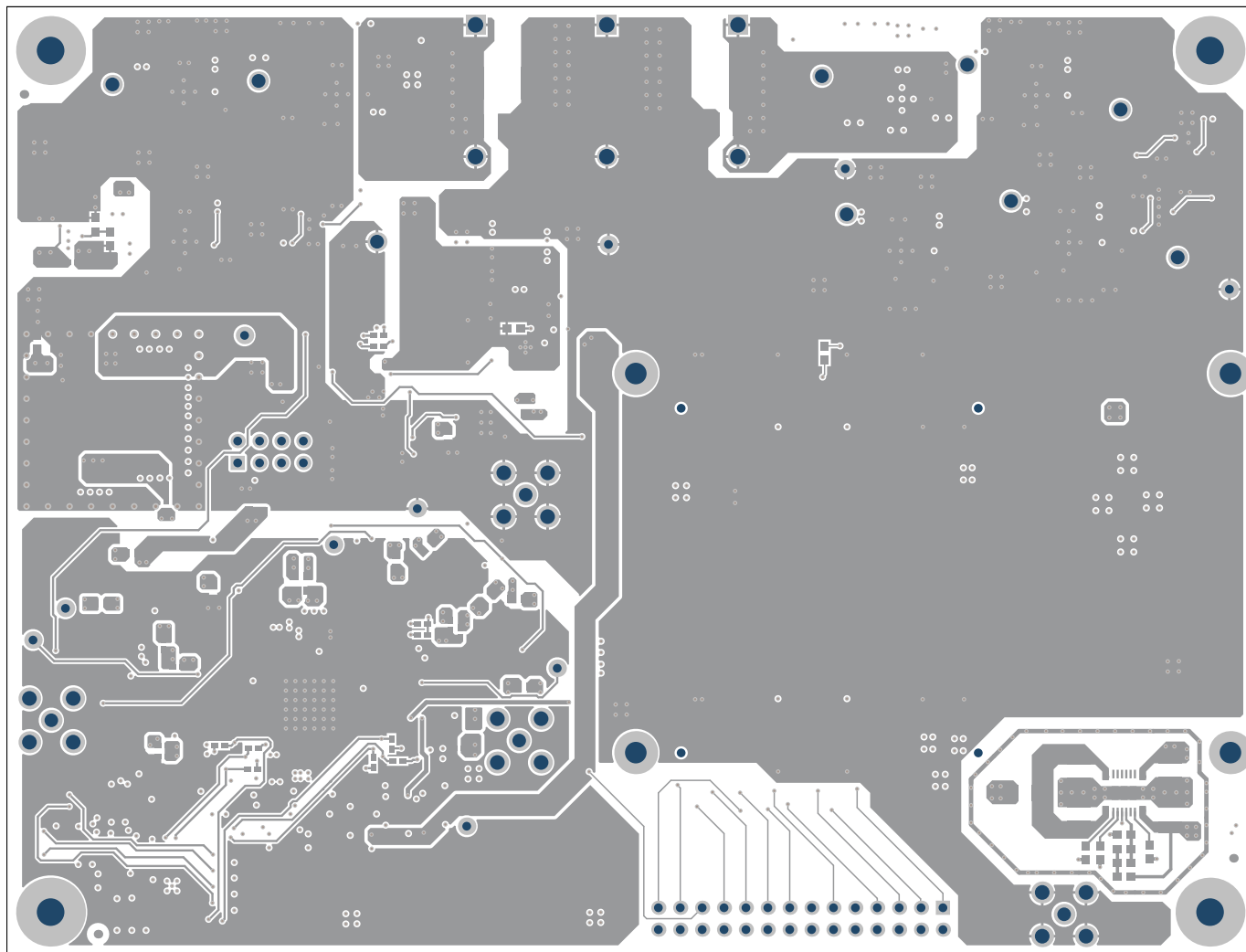


Figure 4-19. DAC90802EVM PCB Bottom Layer Layout

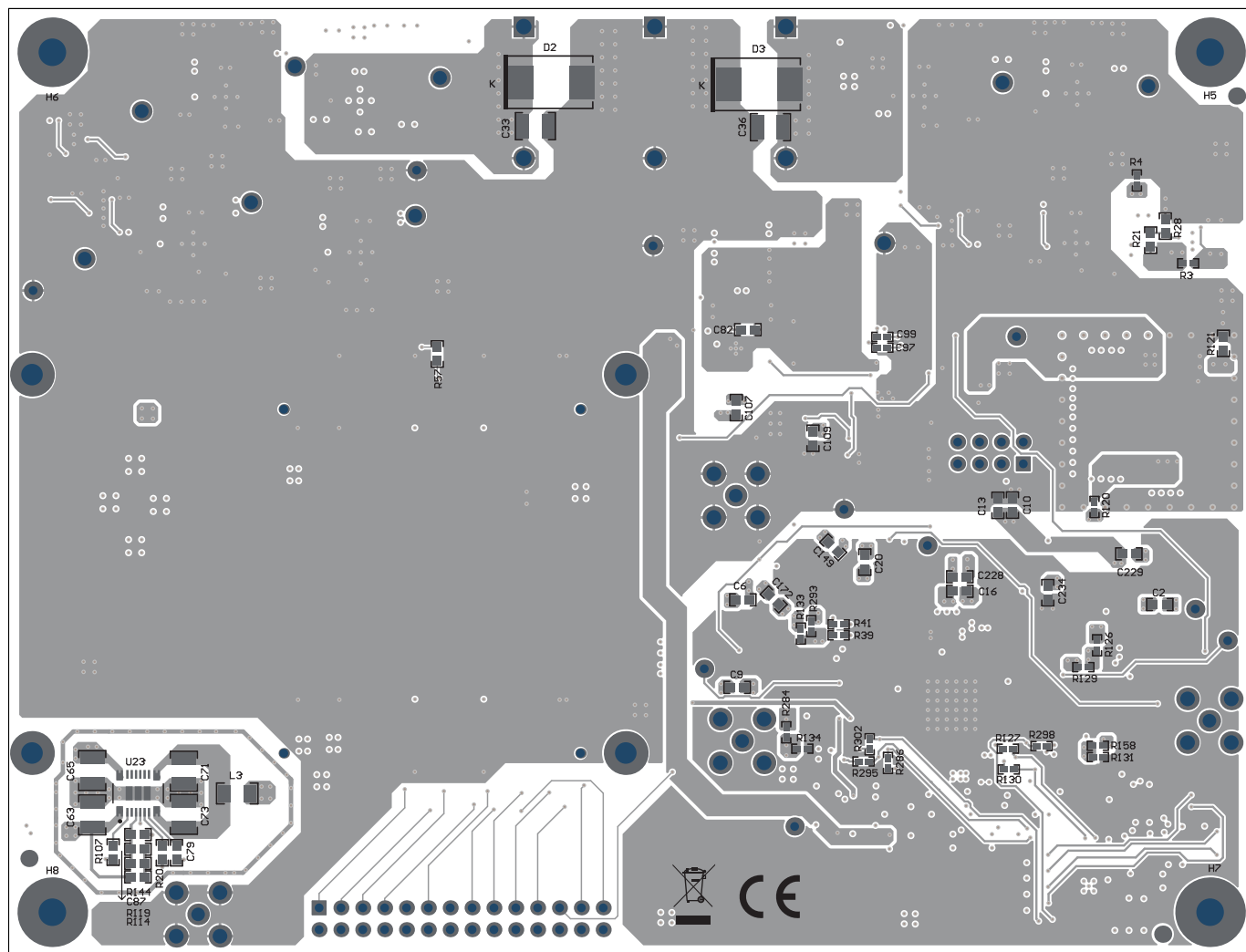


Figure 4-20. DAC90802EVM PCB Bottom Layer Composite View

4.3 Bill of Materials (BOM)

Table 4-1 lists the DAC90802EVM bill of materials (BOM).

Table 4-1. DAC90802EVM Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C1, C8, C12, C145	4	100pF	CAP, CERM, 100pF, 25V, +/- 10%, X7R, 0603	0603	06033C101KAT2A	AVX
C2, C6, C9, C10, C11, C14, C16, C20, C39, C46, C52, C53, C107, C109, C149, C172, C228, C229, C234	19	1uF	CAP, CERM, 1uF, 50V, +/- 10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden
C3, C5, C24, C26, C30, C61, C68, C80, C85, C86, C88, C118, C119, C120, C121, C122	16	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 5%, X7R, 0603	0603	0603YC104JAT2A	AVX
C4, C7, C13, C15, C19, C22, C147, C152, C227, C230, C231	11	0.1uF	CAP, CERM, 0.1 uF, 50V, +/- 5%, X7R, 0603	0603	06035C104JAT2A	AVX
C17	1	1pF	CAP, CERM, 1pF, 50V, +/- 25%, C0G/NP0, 0805	0805	CC0805CRNP09BN1R0	Kemet
C151	1	.02uF	Chip Multilayer Ceramic Capacitors for General Purpose, 0805, 20000pF, C0G, 30ppm/°C, 5%, 50V	0805	GRM21B5C1H203JA01L	Murata Electronics
C21, C29, C31, C98	4	1uF	CAP, CERM, 1uF, 10V, +/- 20%, X5R, 0402	0402	885012105012	Würth Elektronik
C23, C25	2	1uF	CAP, CERM, 1uF, 50V, +/- 10%, X5R, 0603	0603	C1608X5R1H105K080AB	TDK
C27	1	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X5R, 0402	0402	GRM155R61A106ME11D	MuRata
C28, C51	2	10uF	CAP, CERM, 10 uF, 25V, +/- 20%, X5R, 0603	0603	0603W106M250XD	Aillen
C32	1	1uF	CAP, CERM, 1uF, 16V, +/- 10%, X7R, 0603	0603	885012206052	Würth Elektronik
C33, C36, C38, C40, C44, C50, C71, C73, C111, C223, C224	11	10uF	CAP, CERM, 10 uF, 50V, +/- 10%, X7R, 1210	1210	CL32B106KBJNNWE	Samsung Electro-Mechanics
C34, C41, C92	3	10uF	CAP, CERM, 10uF, 25V, +/- 10%, X7R, 0805	0805	GRM21BZ71E106KE15L	MuRata
C35, C42, C56, C94, C258	5	22uF	CAP, CERM, 22uF, 35V, +/- 20%, X5R, 1206	1206	C3216X5R1V226M160DC	TDK
C37, C43, C55, C60, C78, C96	6	1uF	CAP, CERM, 1uF, 25V, +/- 10%, X7R, 0603	0603	06033C105KAT2A	AVX
C45, C48, C57, C174, C175	5	1uF	CAP, CERM, 1 uF, 10V, +/- 10%, X7R, 0603	0603	0603ZC105KAT4A	AVX
C47, C49, C58, C81	4	10uF	CAP, CERM, 10uF, 10V, +/- 10%, X7R, 0805	0805	885012207026	Würth Elektronik
C54, C59	2	10uF	CAP, CERM, 10uF, 35V, +/- 20%, X7R, 1206_190	1206_190	C3216X7R1V106M160AC	TDK
C62	1	0.1uF	CAP, CERM, 0.1 uF, 16V, +/- 10%, X7R, 0201	0201	0201BB104KW160	Passive Plus
C63, C65	2	22uF	CAP, CERM, 22uF, 25V, +/- 10%, X7R, 1210	1210	GRM32ER71E226KE15L	MuRata

Table 4-1. DAC90802EVM Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C64, C66, C114, C115	4	470nF	0.47μF ±5% 50V Ceramic Capacitor C0G, NP0 2220 (5750 Metric)	2220	C2220C474J5GAC TU	Kemet
C67	1	10uF	CAP, CERM, 10uF, 10V, +/- 20%, X7R, 0603	0603	GRM188Z71A106 MA73D	MuRata
C69	1	0.5pF	CAP, CERM, 0.5pF, 50V, +/- 50%, C0G/ NP0, 0603	0603	C0603C508C5GAC TU	Kemet
C70, C74, C76, C82, C83, C90	6	1uF	CAP, CERM, 1 μF, 16V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1C10 5K080AC	TDK
C72, C75, C77, C84	4	0.1uF	CAP, CERM, 0.1uF, 16V, +/- 10%, X7R, 0603	0603	C0603C104K4RAC TU	Kemet
C79	1	0.047uF	CAP, CERM, 0.047uF, 25V, +/- 5%, X7R, 0603	0603	KGM15BR71E473J T	KYOCERA AVX
C87	1	47pF	CAP, CERM, 47pF, 50V, +/- 5%, C0G/ NP0, AEC-Q200 Grade 1, 0603	0603	CGA3E2C0G1H47 0J080AA	TDK
C89, C112	2	220pF	CAP, CERM, 220pF, 50V, +/- 1%, C0G/ NP0, 0603	0603	KGM15ACG1H221 FT	KYOCERA AVX
C91, C105	2	1pF	1pF ±0.05pF 50V Ceramic Capacitor C0G 0201 (0603 Metric)	0201	GCQ0335C1H1R0 WB01D	Murata
C93	1	2200pF	CAP, CERM, 2200pF, 50V, +/- 5%, C0G/ NP0, 0603	0603	GRM1885C1H222J A01D	MuRata
C97, C99	2	0.1uF	CAP, CERM, 0.1 μF, 10V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	C0402C104K8RAC AUTO	Kemet
C106, C108, C161, C163, C165, C167	6	0.1uF	CAP, CERM, 0.1uF, 50V, +/- 10%, X7R, 0402	0402	C1005X7R1H104K 050BB	TDK
C110	1	0.1uF	CAP, CERM, 0.1uF, 50V,+/- 10%, X7R, 0402	0402	C1005X7R1H104K 050BB	TDK
C113, C116	2	0.033uF	CAP, CERM, 0.033 μF, 50V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	0805	CGA4J2C0G1H333 J125AA	TDK
C153, C173	2	0.1uF	CAP, CERM, 0.1uF, 10V, +/- 10%, X7R, 0603	0603	C0603X104K8RAC TU	Kemet
C162	1	0.1uF	CAP, CERM, 0.1uF, 10V, +/- 10%, X7R, 0603	0603	C0603X104K8RAC TU	Kemet
C164	1	2.2uF	CAP, CERM, 2.2uF, 25V, +/- 10%, X7R, 0805	0805	08053C225KAT2A	AVX
D1, D4, D5, D6	4	Red	LED, Red, SMD	LED_0603	150060RS75000	Würth Elektronik
D2, D3	2	200V	Diode, Schottky, 200V, 4A, SMC	SMC	MBRS4201T3G	ON Semiconductor
FARADAY CAGE	1		RF Shield Cover 0.750	RF_SHIELD_COVER	B-0750CC0750-01 75XC	Orbel Corporation
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Machine Screw, Round, #4-40x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8, H9, H10, H11, H12	8		Standoff, Hex, 0.5	Standoff	1902C	Keystone
H13, H14, H15, H16	4		M2.5x0.45 Pan Head Machine Screw Phillips Drive Nylon	SCREW	50M025045P012	Essentra Components
J2, J3, J4, J8	4		Connector, SMA, TH	SMA	142-0701-231	Cinch Connectivity
J5	1		CONN TIP JACK SOLDER RED	973582101	973582101	Altech Corporation
J6	1		CONN TIP JACK SOLDER BLACK	973582100	973582100	Altech Corporation
J7	1		CONN TIP JACK SOLDER YELLOW	105-0757-001	105-0757-001	Cinch Connectivity Solutions Johnson
J9	1		Header, 100mil, 14x2, Gold, TH	14x2 Header	TSW-114-07G-D	Samtec
J10	1		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07G-D	Samtec

Table 4-1. DAC90802EVM Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
J_MC1, J_MC2	2		Header(shrouded), 0.8mm, 40x2, Gold with Tin tail, SMT	36x5x7mm	BTE-040-01F-D-A	Samtec
L3	1	48ohm	Ferrite Bead, 48ohm @ 100MHz, 6A, 1206	1206	742792117	Würth Elektronik
R2, R6, R14, R16, R70	5	1.00k	RES, 1.00k, 0.1%, 0.1W, 0603	0603	RT0603BRD071KL	Yageo America
R9, R67	2	10.0k	RES, 10.0k, 1%, 0.1W, 0603	0603	RC0603FR-0710KL	Yageo
R10, R11, R13, R22, R25, R27, R30, R31, R32, R34, R39, R41, R42, R43, R46, R47, R49, R50, R56, R62, R98, R105, R113, R120, R125, R128, R146, R151, R152, R154, R156, R157, R159, R263, R264, R280, R285, R287, R291, R292, R299, R300, R315, R318	44	0	RES, 0, 5%, 0.063W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R12, R24, R26, R29, R52, R53, R57, R108, R121, R123, R124, R140, R143, R147, R148, R162, R168, R170, R172, R176, R240, R241	22	0	RES, 0, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R17	1	100k	RES, 100k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEYJ104V	Panasonic
R20, R74, R77, R107	4	102k	RES, 102k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW0603102KFKEA	Vishay-Dale
R21	1	91k	RES, 91k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW060391K0JNEA	Vishay-Dale
R28	1	43k	RES, 43k, 5%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW060343K0JNEA	Vishay-Dale
R33	1	24k	RES, 24k, 5%, 0.1W, 0603	0603	RC0603JR-0724KL	Yageo
R35, R36, R106, R117	4	10.0k	RES, 10.0k, 0.01%, 0.1W, 0603	0603	RNCF0603TKY10K0	Stackpole Electronics Inc
R37, R60, R104	3	21.0k	RES, 21.0k, 0.5%, 0.1W, 0603	0603	RT0603DRE0721KL	Yageo America
R38	1	1.00k	RES, 1.00k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R44, R45	2	7.87k	RES, 7.87k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW06037K87FKEA	Vishay-Dale
R54	1	3.00k	RES SMD 3K OHM 0.1% 1/10W 0603	0603	RG1608P-302B-T5	Susumu
R55	1	397k	RES, 397k, 0.1%, 0.125W, 0805	0805	RT0805BRD07397KL	YAGEO
R58	1	2.00k	RES, 2.00k, 0.1%, 0.1W, 0603	0603	RT0603BRD072KL	Yageo America
R64	1	91.0k	RES, 91.0k, 1%, 0.1W, 0603	0603	RC0603FR-0791KL	Yageo
R65, R69	2	37.4	RES, 37.4, 1%, 0.1W, 0603	0603	RC0603FR-0737R4L	Yageo
R66	1	127k	RES, 127k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW0603127KFKEA	Vishay-Dale

Table 4-1. DAC90802EVM Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R68	1	156k	RES, 156k, 0.1%, 0.1W, 0603	0603	RN73R1JTDD1563 F100	KOA Speer Electronics, Inc.
R79, R281	2	20.0	RES, 20.0, 1%, 0.063W, AEC-Q200 Grade 0, 0402	0402	CRCW040220R0F KED	Vishay-Dale
R82, R100, R144	3	10.0k	RES, 10.0k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0F KEA	Vishay-Dale
R87, R90	2	49.9	RES, 49.9, 0.1%, 0.1W, 0603	0603	RT0603BRD0749R 9L	Yageo America
R88, R89	2	22	RES, 22.0, 0.1%, 0.063W, 0603	0603	CPF0603B22RE1	TE Connectivity
R91	1	107k	RES, 107k, 0.5%, 0.1W, 0603	0603	RT0603DRE07107 KL	Yageo America
R101	1	499k	RES, 499k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW0603499KF KEA	Vishay-Dale
R102	1	160k	RES, 160k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW0603160KF KEA	Vishay-Dale
R103	1	274k	RES, 274k, 0.5%, 0.1W, 0603	0603	RT0603DRE07274 KL	Yageo America
R114	1	50	RES, 50, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW060350R0F KEA	Vishay-Dale
R119	1	73.2k	RES, 73.2k, 0.5%, 0.1W, 0603	0603	RT0603DRE0773K 2L	Yageo America
R189, R193	2	18k	RES, 18k, 5%, 0.1W, 0603	0603	RC0603JR-0718KL	Yageo
R297, R304, R319, R320, R321	5	3.32k	RES, 3.32k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	0603	CRCW06033K32F KEA	Vishay-Dale
S1, S2, S3, S4	4		Round Spacer Unthreaded #4 Nylon 0.188	ROUND_SPACER	9911-187	Bivar
SH-J	1		Shunt, 2mm, Gold, Black	2.00mm Jumper	60800213421	Wurth Elektronik
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP10	8		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone Electronics
TP8, TP9	2		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone Electronics
TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21	9		Test Point, Compact, White, TH	White Compact Testpoint	5007	Keystone Electronics
U2, U3, U4, U5	4		36-Volt, High-speed (45MHz GBW and 150V/?s SR), low-noise (4nV/?Hz) RRO JFET operational amplifier, D0008A (SOIC-8)	D0008A	OPA828IDR	Texas Instruments
U6, U8, U9, U10	4		180MHz 0.95nV?Hz operational amplifier with ultra-low total harmonic distortion (THD) 8-SOIC -40 to 85	SOIC8	OPA891DR	Texas Instruments
U11, U12, U24, U25, U26, U27, U28, U29	8		Voltage Level Shifter DTM Package 8-Pin X2SON	X2SON8	SN74LXC2T45DT MR	Texas instruments
U13	1		12-Bit, 10-Bit, and 8-Bit, Quad Voltage and Current Output Smart DACs With Auto-Detected I2C, PMBus?, or SPI	WQFN16	DAC63204RTER	Texas Instruments
U14, U15, U16, U17	4		Automotive 35V, 1A, 4.2?VRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A4701QRGW RQ1	Texas Instruments
U18, U19, U20, U36	4		1A, Positive Voltage Regulator, DRV0006A (WS0N-6)	DRV0006A	TLV76701DRVR	Texas Instruments

Table 4-1. DAC90802EVM Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
U21, U22, U35	3		Vin -3V to -36V, -1A, Ultra-Low-Noise, High-PSRR, Low-Dropout Linear Regulator, RGW0020A (VQFN-20)	RGW0020A	TPS7A3301RGWR	Texas Instruments
U23	1		4.5V - 28V, 6A Buck Power Module	B3QFN19	TPSM86638RCGR	Texas Instruments
U31	1		Low-Offset, Low-Drift, Low-Noise, 45MHz, 36V, JFET-Input Operational Amplifiers	VSSOP8	OPA2828IDGNT	Texas Instruments
U33	1		Low Noise, Precision, 150MHz, Fully Differential Amplifier, RUN0010A (WQFN-10)	RUN0010A	THS4551IRUNR	Texas Instruments
U34	1		512-kSPS, Wide-Bandwidth, 24-Bit, Delta-Sigma ADC	WQFN20	ADS127L21IRUKR	Texas Instruments

5 Compliance Information

5.1 Compliance and Certifications

[DAC90802EVM-PDK EU Declaration of Conformity \(DoC\) for Restricting the use of Hazardous Substances.](#)

6 Related Documentation

The documents in [Table 6-1](#) provide information regarding Texas Instruments integrated circuits used in the assembly of the DAC90802EVM. This user guide is available from the TI web site under literature number SLVUDY9. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions are available from the TI web site at www.ti.com, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 6-1. Related Device Documentation

DOCUMENT	LITERATURE NUMBER
DAC90802 product data sheet	SLASFL3
REF545000CFKHT product data sheet	SBOS456H
OPA828IDR product data sheet	SBOS671D
OPA891DR product data sheet	SBOSAI7B
TPSM86638RCGR product data sheet	SLVSHT0
SN74LXC2T45DTM product data sheet	SCES938B
DAC63204RTER product data sheet	SLASEX3A
REF54250CFKHT product data sheet	SBOS456H
THS4551IRUNR product data sheet	SBOS778D
ADS127L21IRUKR product data sheet	SBASAK4C
TPS7A4701QRGWRQ1 product data sheet	SBVS118
TPS7A3301RGWR product data sheet	SBVS169D
TLV76701DRVR product data sheet	SLVSE84D

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