TI TECH DAYS

How to select the right multiplexer or signal switch to maximize system performance

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Multiplexers and Protection Devices



Agenda

Critical parameters for multiplexers and signal switches

- Critical parameters for precision multiplexers
 - On-resistance
 - On-capacitance
 - Leakage current
 - Charge injection
- Protection multiplexer features and common use cases
 - Powered-off protection
 - Fail-safe logic
 - Latch-up immunity
 - Common use cases
- TI package technology
- Portfolio overview and Q&A

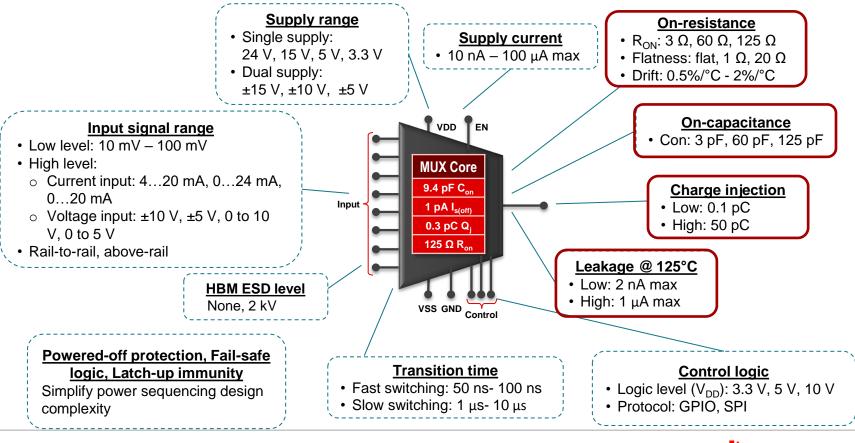


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Critical parameters for multiplexers and signal switches

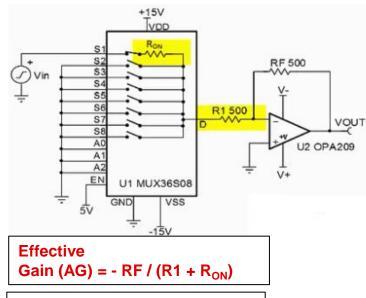


Critical parameters | Multiplexers & signal switches

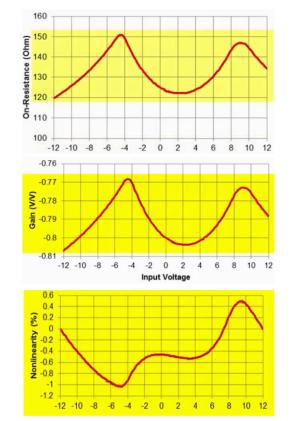




Why is **R**_{ON} important for your system?



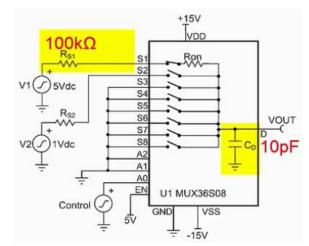
However, if R1 is very high compared to $\rm R_{ON}$ then any gain error non-linearity introduced due to the MUX $\rm R_{ON}$ is negligible



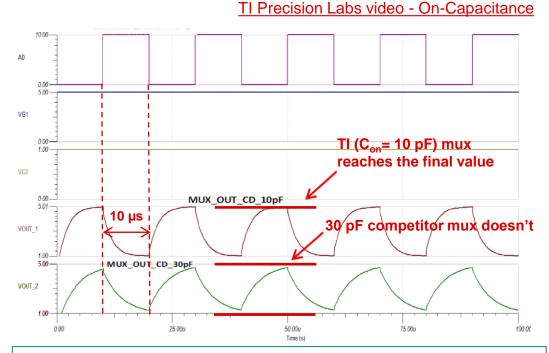
- The on-resistance of a switch can introduce variations and gain error, which produce signal dependent distortion
- R_{ON} drifts over temperature that limits accuracy and degrades linearity of V_{OUT} related to V_{IN}
- To counter gain error introduced due to R_{ON}, it is recommended to interface the MUX output to a high impedance stage R1 (buffer amplifier)



Why is **C**_{ON} important?



Multiplexer examples	Input source impedance	Switching between channels	Outcome
MUX36S08 (C _{on} = 10 pF)	100 kΩ	10 µs	TI mux settles to the input source's final value
Competitor mux (C _{on} = 30 pF)	100 κΩ	10 µs	The other mux doesn't settle to the final value due to long RC time constant formed by mux on-capacitance (30 pF) and 100 k Ω input impedance of source

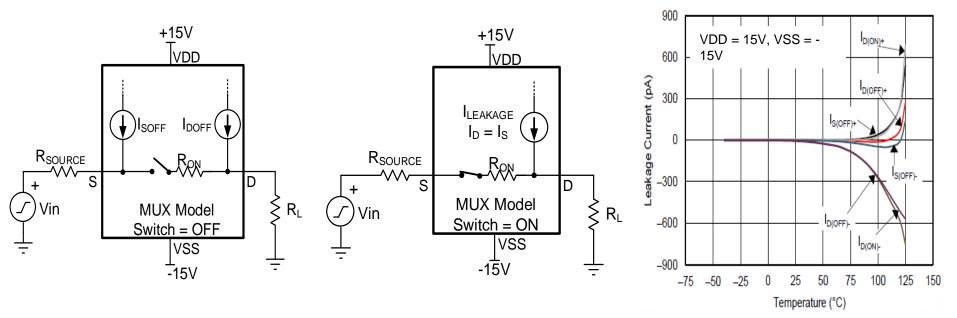


- On-capacitance affects settling behavior of multiplexers, which impacts transient performance of the system
- Higher C_{on} can introduce distortion in systems where input channels are switched at a very fast rate
- □ For high input impedance data acquisition systems and fast switching data acquisition systems, a low C_{on} multiplexer is recommended



Why is ILEAKAGE important for your system?

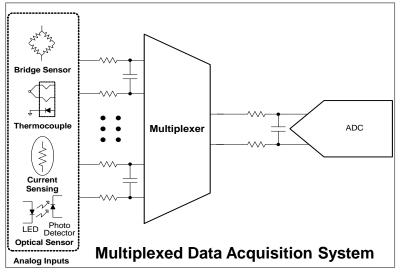
TI Precision Labs video - Leakage Current



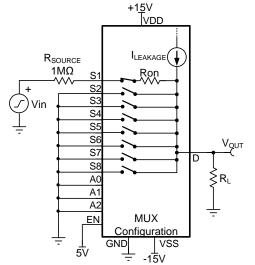
- Switch = OFF: $I_{S(OFF)}$ flows through R_{SOURCE} and $I_{D(OFF)}$ flows through R_L
- Switch = ON: Error introduced by leakage current: $V_{ERROR} = (R_{ON} + R_{SOURCE}) \times I_{D(ON)}$

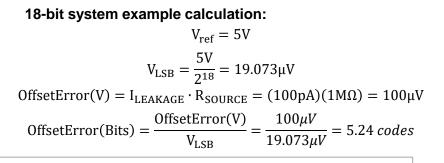


Industrial applications | Factory automation - PLC



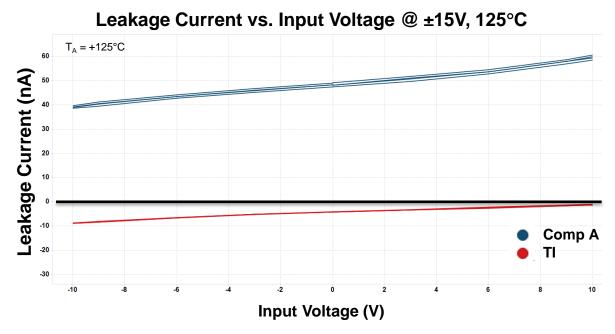
Multiplexer examples	Multiplexer leakage current (25°C/85°C)	Offset error (25°C/85°C) (I _{LEAKAGE} x R _{Source})	Offset error 18-bit system (in bits)
MUX 1 (Low leakage)	10 pA / 50 pA	10 μV / 50 μV	0.52 / 2.62
MUX 2 (High leakage)	100 pA / 500 pA	100 μV / 500 μV	5.24 / 26.22





TEXAS INSTRUMENTS

TMUX7219 benchmarks | Leakage current



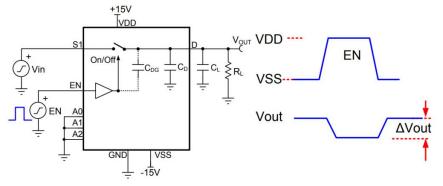
- TMUX7219 is designed to be the lowest leakage low R_{ON} mux in the industry
- Lower leakage with linear scaling means
 - Less error in measurement
 - Less drift
 - Easier to calibrate in high precision systems



Why is **Q**_{INJECTION} important for your system?

TI Precision Labs video - Charge injection

- What is charge injection error?
 - Charge injection is a voltage change introduced at the output of the switch when logic is turned ON or OFF.
 - This can introduce output voltage error when the control logic is switched.



• Voltage change introduced at the output of switch when switch is turned ON or OFF:

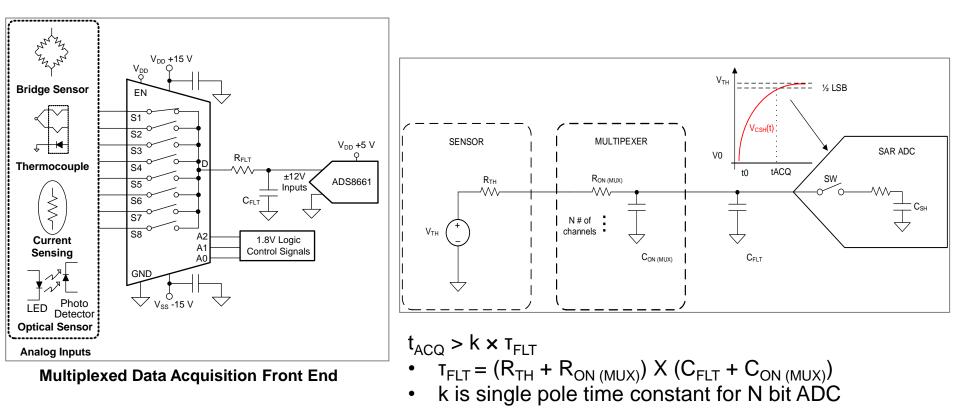
$$Q_{INJ} = (C_D + C_L) \times \Delta V_{OUT}$$

• With large load capacitance, effect of C_D can be ignored:

$$V_{ERROR} = \Delta V_{OUT} \approx \frac{Q_{INJ}}{C_L}$$

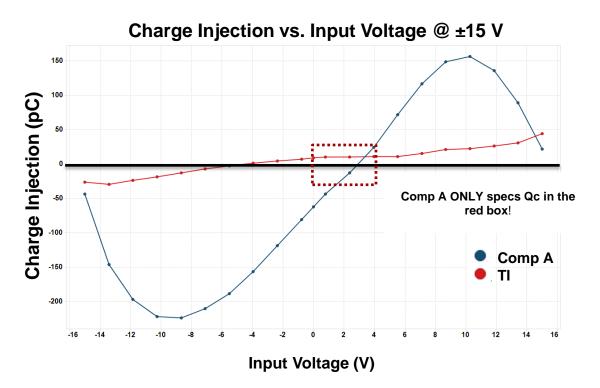


Industrial applications | Analog input modules





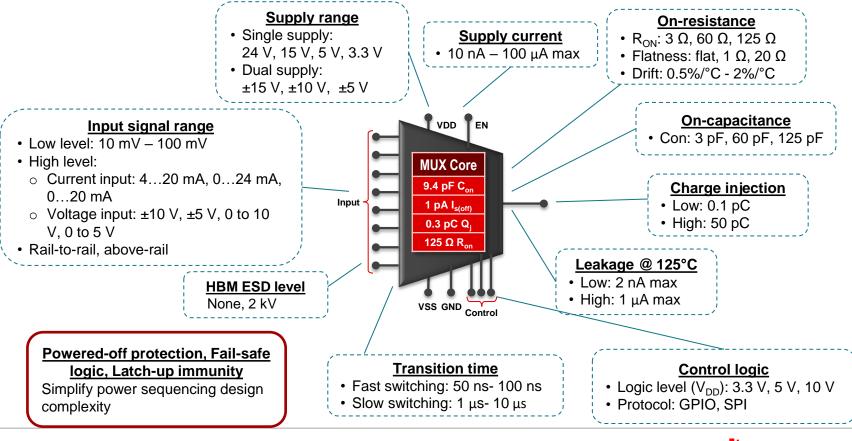
TMUX7219 benchmarks | Charge injection



- TMUX7219 delivers classleading charge injection performance across the entire signal range
- Lower charge injection means
 - Less error in the signal chain
 - Faster sampling
 - Less overshoot & ringing on switching channels

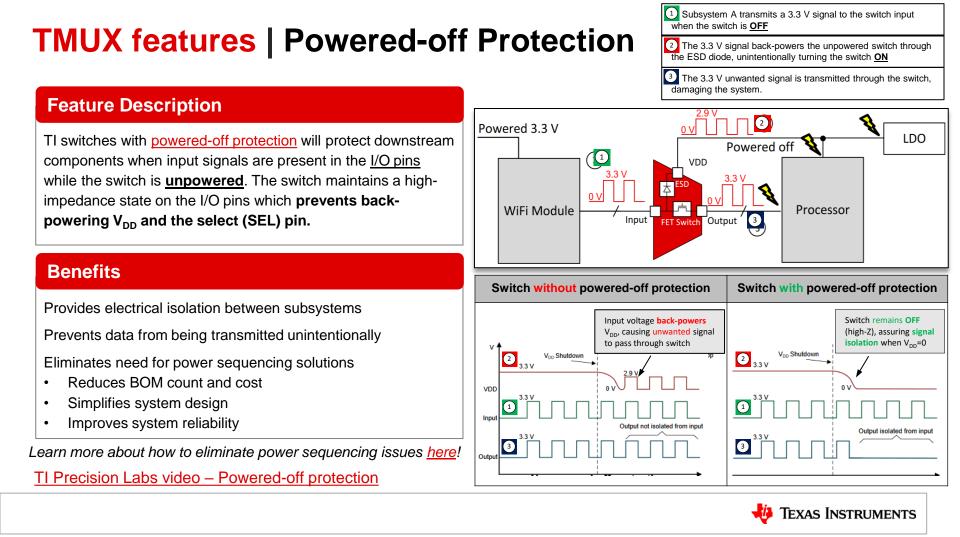


Critical parameters | Multiplexers & signal switches



Texas Instruments

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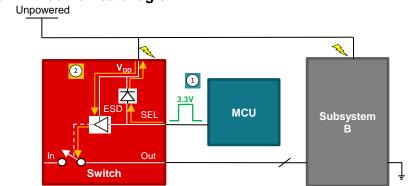


TMUX features | Fail-safe logic

The MCU transmits a 3.3 V logic signal to the switch select (SEL) when the switch is <u>OFF</u>

The 3.3 V logic signal back-powers V_{DD}, back-powering Subsystem B and turning the switch <u>ON</u>

Switch without fail-safe logic:



Switch with fail-safe logic: Unpowered

Switch



Feature Description

TI switches with <u>fail-safe logic</u> will protect downstream components when a logic signal is present in the <u>select (SEL)</u> <u>pins</u> while the switch is unpowered. The switch maintains in a high-impedance state on the SEL logic pins **preventing power from going through V**_{DD} **during power sequencing**.

Benefits

Protects mux and downstream ICs from damage

Eliminates need for power sequencing solutions

- Reduces BOM count and cost
- Simplifies system design
- Improves system reliability

Standard low-voltage <u>TMUX</u> feature

TI Precision Labs video - Fail-safe Logic

TMUX features | Latch-up immunity

Feature Description

TI switches with <u>latch-up immunity</u> prevent undesirable high current events between parasitic structures within the device typically caused by overvoltage events. The TMUX62xx/TMUX72xx family of devices are built in a Silicon On Insulator (SOI) process and will not latch-up when exposed to current injection or overvoltage events.

Benefits

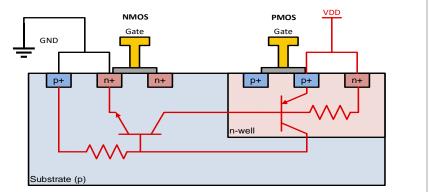
Prevents undesirable high current events between parasitic structures within the device typically caused by overvoltage events.

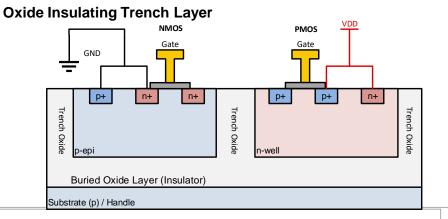
Provides a simpler, more compact protection solution

- Reduces BOM count and cost
- Simplifies system design
- Improves system reliability

TI Precision Labs video – Latch-up Immunity

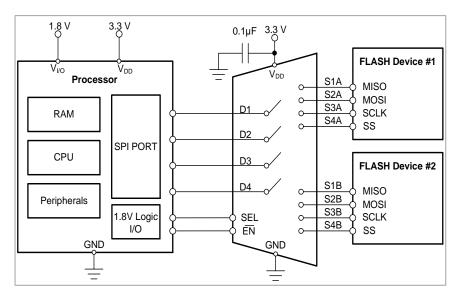
Cross section of CMOS Inverter with SCR







Industrial applications | Protection multiplexers



 V_{DD} V_{I/O} VDD 0.1µF Processor JTAG, SPI, GPIO Port _ FLASH TDI / MISO / GPIO S1 D1 TDO / MOSI / GPIO JTAG S2 D2 DEBUG. RAM SPI. GPIO TCK / SCLK / GPIO S3 D3 TMS / SS / GPIO S4 D4 CPU SEL1 SEL2 1.8V Logic SEL3 Peripherals I/O SEL4 GND GND

Multiplexing Flash Memory

Protocol / Signal Isolation

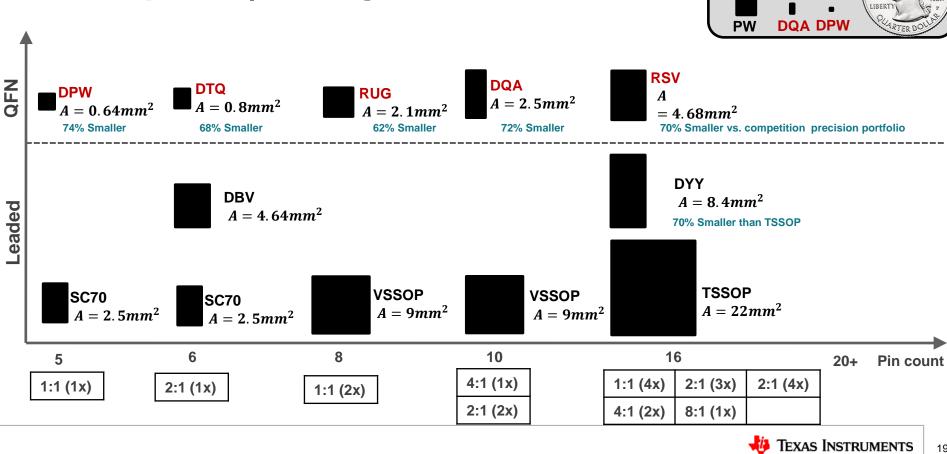


TI packaging & technology



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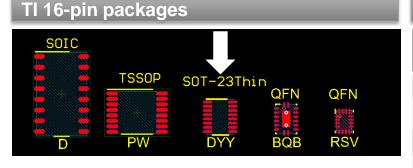
TI multiplexer | Package differentiation

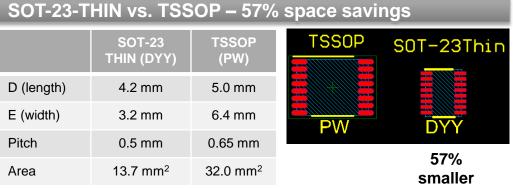


1x scale:

TI package technology | SOT-23-THIN (DYY)

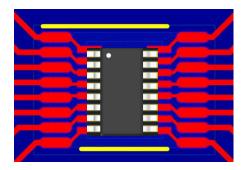
Industry's smallest 16-pin leaded packages





SOT-23-THIN vs. QFN – QFN size with leaded reliability

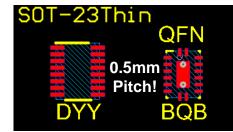
SOT-23-THIN fits inside TSSOP footprint



Dual footprint option SOT-23-THIN will fit inside TSSOP footprint and can be dual routed using conventional PCB design rules.

QFN size with leaded reliability

- SOT-23-THIN package achieves small QFN size and maintains 0.5 mm pitch
- SOT-23-THIN is a QFN alternative for space constrained designs with the added benefits of optical inspection, easier debug, and mechanical reliability of a leaded package

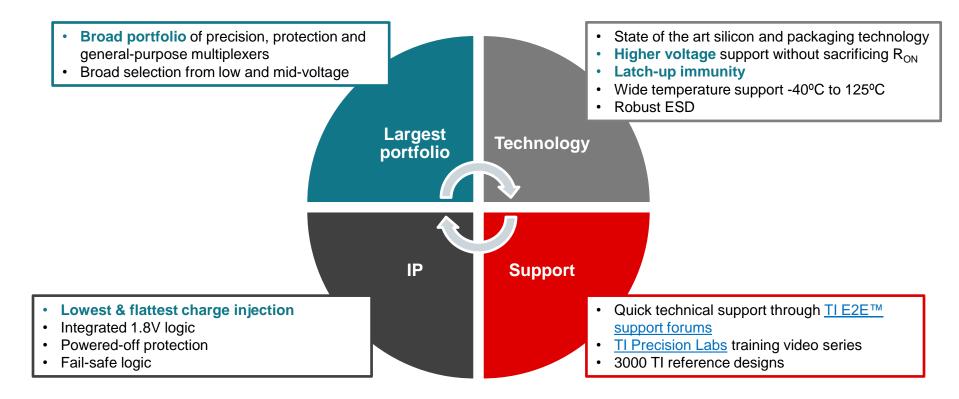




TI multiplexer & signal switch portfolio



TI multiplexer & signal switch portfolio





Backup



Selection guide | Low-voltage V_{SIGNAL} < 24 V

		TMUX1108 TMUX1208			Precision		TMUX	Key Diffe	erences	
	8:1	TMUX1308 SN74LV4051 *CD4051			Protection General Purpose			Precision	Protection	General Purpose
		SN74LV4051	TMUX1109	1	*CD : up to 20 V Supply	Ultra-Low Lea	kage (pA)	1	-	-
		TMUX1104	TMUX1209 TMUX1309 SN74LV4052			Powered-off P	Protection	-	1	-
6	4:1	TMUX1204	SN74CV4052 SN74CBT3253 TS5A5017			Overvoltage P	Protection	-	1	-
atior			*CD4052			1.8 V Logic Co	ontrol	1	1	1
Configuration		TMUX1119 TMUX TMUX1219 TMUX TMUX1247 TMUX SN74LVC3157 TS5237	TMUX1136 TMUX136	5 TMUX1133 E SN74LV4053A 2 CD74HC4053	TMUX1134 TMUX1574 TS3A44159 SN74CBTLV3257	Fail-safe Logi	c	1	1	1
	2:1		TMUX154E TMUX1072 TS5A23157/59			Smallest QFN	packages	1	1	1
	TS5A3159	TS5A22364		TI Device Fam	ilies:	TMUX11xx	TMUX15xx	TMUX12xx, TMUX13xx		
	1:1	TMUX1101 TMUX1102 SN74LVC1G66 TS5A3166	TMUX1121 TMUX1122 TMUX1123 SN74LVC2G66 TS5A2066 TS5A21366		TMUX1111 TMUX1511 TMUX1311 SN74CBTLV3125 SN74HC4066 *CD4066 TMUXxxxX Nomenclature			J		
		1	2	3	4	1 st Digit	2 nd Digi	t 3 rd	& 4 th Digit	Final Letter
			Number of Char	nnels		Supply Range	Product Fa Generatio		annel Count onfiguration	Key Differentiation



Selection guide | Mid-voltage (24 V > V_{SIGNAL} > 100 V)

		MUX36S16		Precision
	16:1	MUX506		Protection
				General Purpose
	8:1	MUX36S08 MUX508	MUX36D08 MUX507	
Configuration	4:1	TMUX6104	MUX36D04 MUX509	
Ŝ	2:1	TMUX6136	TMUX6119	
	1:1		TMUX6121/22/23	TMUX6111/12/13
		1	2	4
		Nu	mber of Channels	

TMUX Key Differences				
	Precision	Protection	General Purpose	
Ultra-Low Leakage (pA)	1	-	-	
Powered-off Protection	-	1	-	
Overvoltage Protection (up to ±60 V)	-	1	-	
Fail-safe Logic	1	1	1	
Smallest QFN packages	1	1	1	
TI Device Families:	TMUX61xx TMUX72xx	TMUX73xxF TMUX74xxF	MUX50x	

TMUXxxxX Nomenclature

1 st Digit	2 nd Digit	3 rd & 4 th Digit	Final Letter
Supply	Product Family	Channel Count	Key
Range	Generation	& Configuration	Differentiation



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