DAC121S101QML-SP Radiation Hardened 12-Bit Micro Power Digital-to-Analog Converter With Rail-to-Rail Output

1 Features

- 5962R07726
  - Total Ionizing Dose 100 krad(Si)
  - Single Event Latch-up Immune 120 MeV-cm^2/mg
  - Single Event Functional Interrupt Immune 120 MeV-cm^2/mg (See *Radiation Report*)
- Ensured Monotonicity
- Low Power Operation
- Rail-to-Rail Voltage Output
- Power-On Reset to Zero Volts Output
- SYNC Interrupt Facility
- Wide Power Supply Range (2.7 V to 5.5 V)
- Small Packages
- Power-Down Feature
- Key Specifications
  - Resolution: 12 Bits
  - DNL: +0.21, –0.10 LSB (Typical)
  - Output Settling Time: 12.5 µs (Typical)
  - Zero Code Error: 2.1 mV (Typical)
  - Full-Scale Error: −0.04% FS (Typical)
  - Power Dissipation
    - Normal Mode: 0.52 mW (3.6 V) and 1.19 mW (5.5 V) Typical
    - Power-Down Mode: 0.014 µW (3.6 V) and 0.033 µW (5.5 V) Typical

2 Applications

- Satellites
  - Altitude and Orbit Control
  - Precision Sensors
  - Motor Control
- High Temperatures

3 Description

The DAC121S101QML-SP device is a full-featured, general-purpose, 12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7-V to 5.5-V supply and consumes just 177 µA of current at 3.6 V. The on-chip output amplifier allows rail-to-rail output swing and the three-wire serial interface operates at clock rates up to 20 MHz over the specified supply voltage range and is compatible with standard SPI, QSPI, MICROWIRE, and DSP interfaces.

The supply voltage for the DAC121S101QML-SP serves as its voltage reference, providing the widest possible output dynamic range. A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt.

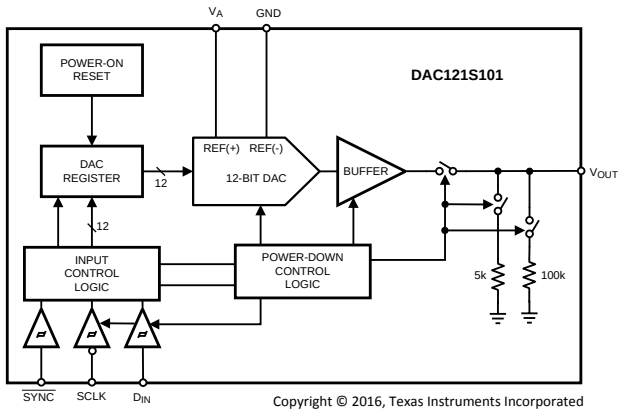
The low power consumption and small packages of the DAC121S101QML-SP make it an excellent choice for use in battery-operated equipment.

Device Information(1)

PART NUMBER	GRADE	PACKAGE
DAC121S101WGRQV	5962R0722601VZA 100 krad	10-lead ceramic SOIC
DAC121S101WGRLV	5962R0722602VZA 100 krad ELDRS-Free	10-lead ceramic SOIC
DAC121S101-MDR	5962R0722601V9A 100 krad	Die
DAC121S101WGMPR	Pre-Flight Engineering Prototype	10-lead ceramic SOIC
DAC121S101CVAL	Ceramic Evaluation Board	10-lead ceramic SOIC

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F **Page**

- Changed data sheet title *DAC121S101QML 12-Bit Micro Power Digital-to-Analog Converter With Rail-to-Rail Output* to *DAC121S101QML-SP Radiation Hardened 12-Bit Micro Power Digital-to-Analog Converter With Rail-to-Rail Output* 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

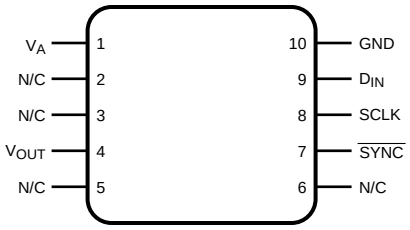
Changes from Revision D (March 2013) to Revision E **Page**

- Changed layout of National Data Sheet to TI format ... 20

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5 Pin Configuration and Functions

NAC Package
10-Pin CFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_A	—	Power supply and reference input; must be decoupled to GND
2	N/C	—	No connect; pin not internally connected to die
3	N/C	—	No connect; pin not internally connected to die
4	V_{OUT}	Output	DAC analog output voltage
5	N/C	—	No connect; pin not internally connected to die
6	N/C	—	No connect; pin not internally connected to die
7	$\overline{SYNC}$	Input	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
8	SCLK	Input	Serial clock input; data is clocked into the input shift register on the falling edges of this pin.
9	D_{IN}	Input	Serial data input; data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
10	GND	—	Ground reference for all on-chip circuitry

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6 Specifications

6.1 Absolute Maximum Ratings[1][2]

		MIN	MAX	UNIT
Supply voltage, V_A			6.5	V
Voltage on any input pin		−0.3	(V_A + 0.3)	V
Input current at any pin[3]			10	mA
Maximum output current[4]			10	mA
V_{OUT} pin in power-down mode			1	mA
Package input current[3]			20	mA
Power dissipation at T_A = 25°C		See[5]		
Maximum junction temperature			175	°C
Lead temperature	CFP package (Soldering 10 Seconds)		260	°C
Package weight (typical)	CFP package		220	mg
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) When the input voltage at any pin exceeds the power supplies (that is, less than GND, or greater than V_A), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(4) Maximum output current may not exceed 10 mA. At V_{DD} = 5.5 V the minimum external resistive load can be no less than 550 Ω (360 Ω at V_{DD} = 3.6 V).
(5) The absolute maximum junction temperature ($T_J$max) for this device is 175°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($R_{\theta JA}$), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max − T_A) / $R_{\theta JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions must be avoided.

6.2 ESD Ratings

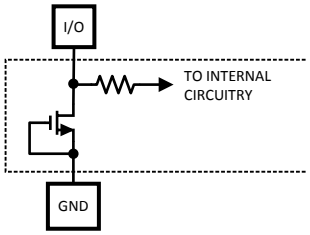
			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1][2]	±5000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model is 100-pF capacitor discharged through a 1.5-kΩ resistor. Machine model is 220 pF discharged through 0 Ω.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Operating temperature	−55	125	°C
Supply voltage, V_A	2.7	5.5	V
Any input voltage[1]	−0.1	(V_A + 0.1)	V
Output load	0	1500	pF
SCLK frequency		20	MHz

(1) The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the conversion result can occur if any input goes above V_A or below GND by more than 100 mV. For example, if V_A is 2.7-V DC , ensure that –100 mV ≤ input voltages ≤ 2.8-V DC to ensure accurate conversions.



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6.4 Thermal Information

THERMAL METRIC[1][2]		DAC121S101QML-SP NAC (CFP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	25.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) 10-pin CFP Package on 2-layer, 1-oz. PCB

6.5 DAC121S101QML-SP Electrical Characteristics DC Parameters

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = ∞, C_L = 200 pF to GND, f_{SCLK} = 20 MHz, input code range 48 to 4047. All limits T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		NOTES	SUB-GROUPS	MIN	TYP[1]	MAX	UNIT
STATIC PERFORMANCE									
	Resolution	$T_{MIN} \le T_A \le T_{MAX}$		See[2]		12			Bits
	Monotonicity	$T_{MIN} \le T_A \le T_{MAX}$		See[2]		12			Bits
INL	Integral non-linearity	Over Decimal codes 48 to 4047			[1, 2, 3]	−8	±2.75	8	LSB
DNL	Differential non-linearity	V_A = 2.7 V to 5.5 V	DNL MAX		[1, 2, 3]		0.21	1	LSB
			DNL MIN			−0.7	−0.1		
ZE	Zero code error	I_{OUT} = 0			[1, 2, 3]		2.12	15	mV
FSE	Full-scale error	I_{OUT} = 0			[1, 2, 3]		−0.04	−1	%FSR
GE	Gain error	All ones Loaded to DAC register			[1, 2, 3]		−0.11	±1	%FSR
ZCED	Zero code error drift			See[2]			−20		µV/°C
TC GE	Gain error tempco	V_A = 3 V		See[2]			−0.7		ppm/°C
		V_A = 5 V					−1		
OUTPUT CHARACTERISTICS									
I_{PD} SINK	Vout pin in power-down mode	All PD Modes, $T_{MIN} \le T_A \le T_{MAX}$		See[2]				1	mA
	Output voltage range	$T_{MIN} \le T_A \le T_{MAX}$		See[2]		0		V_A	V
ZCO	Zero code output	V_A = 3 V, I_{OUT} = 10 µA			[1, 2, 3]		2	6	mV
		V_A = 3 V, I_{OUT} = 100 µA			[1, 2, 3]		4	10	
		V_A = 5 V, I_{OUT} = 10 µA			[1, 2, 3]		2	8	
		V_A = 5 V, I_{OUT} = 100 µA			[1, 2, 3]		4	9	
FSO	Full-scale output	V_A = 3 V, I_{OUT} = 10 µA			[1, 2, 3]	2.99	2.997		V
		V_A = 3 V, I_{OUT} = 100 µA			[1, 2, 3]	2.985	2.991		
		V_A = 5 V, I_{OUT} = 10 µA			[1, 2, 3]	4.985	4.994		
		V_A = 5 V, I_{OUT} = 100 µA			[1, 2, 3]	4.985	4.992		
	Maximum load capacitance	R_L = ∞		See[2]			1500		pF
		R_L = 2 kΩ					1500		
	DC output impedance				[1, 2, 3]		8	16	Ω
LOGIC INPUT									
I_{IN}	Input current				[1, 2, 3]	−200	6	200	nA
V_{IL}	Input low voltage	V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$			[1, 2, 3]			0.8	V
		V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$			[1, 2, 3]			0.5	
V_{IH}	Input high voltage	V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$			[1, 2, 3]	2.4			V
		V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$			[1, 2, 3]	2.1			

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms.
(2) This parameter is ensured by design and/or characterization and is not tested in production.

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DAC121S101QML-SP Electrical Characteristics DC Parameters (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = ∞, C_L = 200 pF to GND, f_{SCLK} = 20 MHz, input code range 48 to 4047. All limits T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	NOTES	SUB-GROUPS	MIN	TYP(1)	MAX	UNIT
C_{IN}	Input capacitance		See(2)			5		pF
POWER REQUIREMENTS								
I_A	Supply current (output unloaded)	Normal Mode 5.5 V f_{SCLK} = 20 MHz		[1, 2, 3]		216	270	µA
		Normal Mode 3.6 V f_{SCLK} = 20 MHz		[1, 2, 3]		145	200	
		Normal Mode 5.5 V f_{SCLK} = 10 MHz		[1, 2, 3]		185	230	
		Normal Mode 3.6 V f_{SCLK} = 10 MHz		[1, 2, 3]		132	175	
		Normal Mode 5.5 V f_{SCLK} = 0		[1, 2, 3]		150	190	
		Normal Mode 3.6 V f_{SCLK} = 0		[1, 2, 3]		115	160	
		All PD Modes, 5.5 V f_{SCLK} = 20 MHz		[1, 2, 3]		22	60	
		All PD Modes, 3.6 V f_{SCLK} = 20 MHz		[1, 2, 3]		12	30	
		All PD Modes, 5.5 V f_{SCLK} = 10 MHz		[1, 2, 3]		12	40	
		All PD Modes, 3.6 V f_{SCLK} = 10 MHz		[1, 2, 3]		6	20	
		All PD Modes, 5.5 V f_{SCLK} = 0		[1, 2, 3]		0.006	1	
		All PD Modes, 3.6 V f_{SCLK} = 0		[1, 2, 3]		0.004	1	
P_C	Power consumption (output unloaded)	Normal Mode, 5.5 V f_{SCLK} = 20 MHz		[1, 2, 3]		1.19	1.49	mW
		Normal Mode 3.6 V f_{SCLK} = 20 MHz		[1, 2, 3]		0.52	0.72	
		Normal Mode, 5.5 V f_{SCLK} = 10 MHz		[1, 2, 3]		1.02	1.27	
		Normal Mode 3.6 V f_{SCLK} = 10 MHz		[1, 2, 3]		0.47	0.63	
		Normal Mode, 5.5 V f_{SCLK} = 0		[1, 2, 3]		0.82	1.05	
		Normal Mode 3.6 V f_{SCLK} = 0		[1, 2, 3]		0.41	0.58	
		All PD Modes, 5.5 V f_{SCLK} = 20 MHz		[1, 2, 3]		0.12	0.33	
		All PD Modes, 3.6 V f_{SCLK} = 20 MHz		[1, 2, 3]		0.07	0.11	
		All PD Modes, 5.5 V f_{SCLK} = 10 MHz		[1, 2, 3]		0.04	0.22	
		All PD Modes, 3.6 V f_{SCLK} = 10 MHz		[1, 2, 3]		0.02	0.08	
		All PD Modes, 5.5 V f_{SCLK} = 0		[1, 2, 3]		0.033	5.5	
		All PD Modes, 3.6 V f_{SCLK} = 0		[1, 2, 3]		0.014	3.6	
I_{OUT}	Power efficiency	I_{LOAD} = 2 mA	See(2)			91%		
I_A						94%		

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6.6 DAC121S101QML-SP Electrical Characteristics AC and Timing Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = ∞, C_L = 200 pF to GND, f_{SCLK} = 20 MHz, input code range 48 to 4047. All limits T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		NOTES	SUB-GROUPS	MIN	TYP(1)	MAX	UNIT
f_{SCLK}	SCLK frequency	(See Figure 31)			[9,10,11]			20	MHz
t_s	Output voltage settling time	FF0 to 00F code change, R_L = ∞	C_L ≤ 200 pF		[9,10,11]		12.5	15	µs
			C_L = 500 pF		[9,10,11]		12.5	15	
		00Fh to FF0h code change, R_L = ∞	C_L ≤ 200 pF		[9,10,11]		12.5	15	
			C_L = 500 pF		[9,10,11]		12.5	15	
SR	Output slew rate			See(2)			1		V/µs
	Glitch impulse	Code change from 800h to 7FFh		See(2)			12		nV-sec
	Digital feedthrough			See(2)			0.5		nV-sec
t_{WU}	Wake-Up Time	V_A = 5 V		See(2)			0.65		µs
		V_A = 3 V					1.1		
$1/f_{SCLK}$	SCLK cycle time	(See Figure 31)			[9,10,11]	50			ns
t_H	SCLK high time	(See Figure 31)			[9,10,11]	20			ns
t_L	SCLK low time	(See Figure 31)			[9,10,11]	20			ns
t_{SUCL}	Setup time $\overline{SYNC}$ to SCLK rising edge	(See Figure 31)			[9,10,11]	0			ns
t_{SUD}	Data setup time	(See Figure 31)			[9,10,11]	6			ns
t_{DHD}	Data hold time	(See Figure 31)			[9,10,11]	4.5			ns
t_{CS}	SCLK fall to rise of $\overline{SYNC}$	V_A = 5.5 V (See Figure 31)			[9,10,11]	10			ns
		V_A = 2.7 V (See Figure 31)			[9,10,11]	18			
t_{SYNC}	$\overline{SYNC}$ high time	V_A = 5.5 V (See Figure 31)			[9,10,11]	37			ns
		V_A = 2.7 V (See Figure 31)			[9,10,11]	36			

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms.
(2) This parameter is ensured by design and/or characterization and is not tested in production.

6.7 DAC121S101QML Electrical Characteristics Radiation Electrical Characteristics(1)

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = ∞, C_L = 200 pF to GND, f_{SCLK} = 20 MHz, input code range 48 to 4047.

PARAMETER		TEST CONDITIONS		SUB-GROUPS	MIN	MAX	UNIT
POWER REQUIREMENTS							
I_A	Supply current (output unloaded)	Normal Mode f_{SCLK} = 20 MHz	5.5 V	[1]		325	µA
			3.6 V	[1]		250	
		Normal Mode f_{SCLK} = 10 MHz	5.5 V	[1]		300	
			3.6 V	[1]		225	
		Normal Mode f_{SCLK} = 0	5.5 V	[1]		275	
			3.6 V	[1]		200	
		All PD Modes, f_{SCLK} = 20 MHz	5.5 V	[1]		125	
			3.6 V	[1]		100	
		All PD Modes, f_{SCLK} = 10 MHz	5.5 V	[1]		115	
			3.6 V	[1]		95	
		All PD Modes, f_{SCLK} = 0	5.5 V	[1]		100	
			3.6 V	[1]		100	

(1) Pre- and post-irradiation limits are identical to those listed in the *DAC121S101QML-SP Electrical Characteristics DC Parameters* and *DAC121S101QML-SP Electrical Characteristics AC and Timing Characteristics* tables, except as listed in the *Radiation Electrical Characteristics* table. When performing post irradiation electrical measurements for any RHA level, T_A = 25°C. See *Radiation Environments* for dose rate and test conditions.

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6.8 DAC121S101QML-SP Electrical Characteristics Operating Life Test Delta Parameters T_A at 25°C[1]

PARAMETER		TEST CONDITIONS	SUB-GROUPS	MIN	MAX	UNIT
INL	Integral non-linearity		[1]		±2	LBS
ts	Output voltage settling time		[1]		±5	µA
I_A	Supply current (output unloaded)	Normal Mode, V_A = 5.5 V, f_{SCLK} = 20 MHz	[1]		±10	µA
		Normal Mode, V_A = 3.6 V, f_{SCLK} = 20 MHz	[1]		±6	
		Normal Mode, V_A = 5.5 V, f_{SCLK} = 10 MHz	[1]		±10	
		Normal Mode, V_A = 3.6 V, f_{SCLK} = 10 MHz	[1]		±6	
		Normal Mode, V_A = 5.5 V, f_{SCLK} = 0	[1]		±8	
		Normal Mode, V_A = 3.6 V, f_{SCLK} = 0	[1]		±6	
		All PD Modes, V_A = 5.5 V, f_{SCLK} = 20 MHz	[1]		±2	
		All PD Modes, V_A = 3.6 V, f_{SCLK} = 20 MHz	[1]		±1	
		All PD Modes, V_A = 5.5 V, f_{SCLK} = 10 MHz	[1]		±1	
		All PD Modes, V_A = 3.6 V, f_{SCLK} = 10 MHz	[1]		±1	
		All PD Modes, V_A = 5.5 V, f_{SCLK} = 0	[1]		±0.1	
		All PD Modes, V_A = 3.6 V, f_{SCLK} = 0	[1]		±0.1	

(1) These parameters are worse case drift. Deltas are performed at room temperature Post OP Life. All other parameters no Deltas are required.

The DAC121S101QML-SP operates over the extended temperature range of –55°C to +125°C.

See *Radiation Environments* for dose rate environment information.

Table 1. Quality Conformance Inspection[1]

SUB-GROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	–55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	–55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	–55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	–55
12	Setting time at	+25
13	Setting time at	+125
14	Setting time at	–55

(1) MIL-STD-883, Method 5005 - Group A

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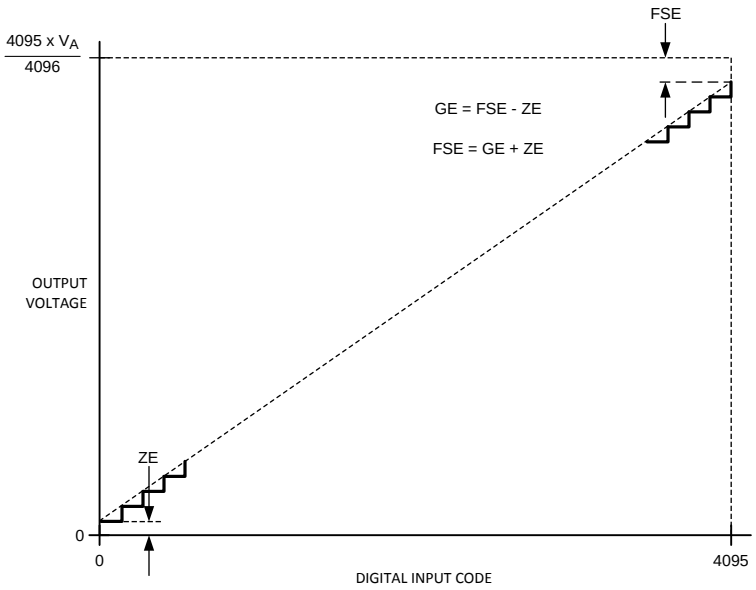


Figure 1. Input / Output Transfer Characteristic

6.9 Typical Characteristics

f_{SCLK} = 20 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated

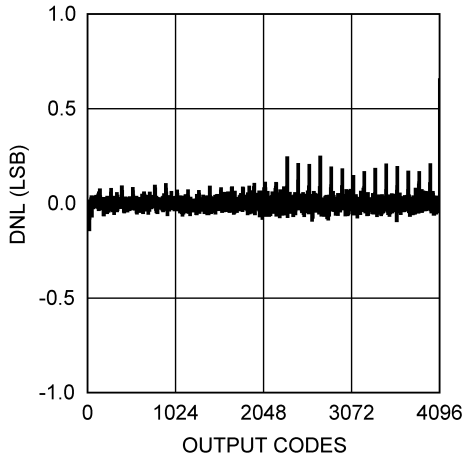


Figure 2. DNL at V_A = 2.7 V

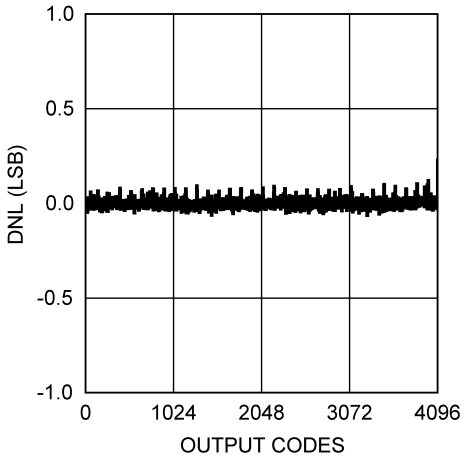


Figure 3. DNL at V_A = 5.5 V

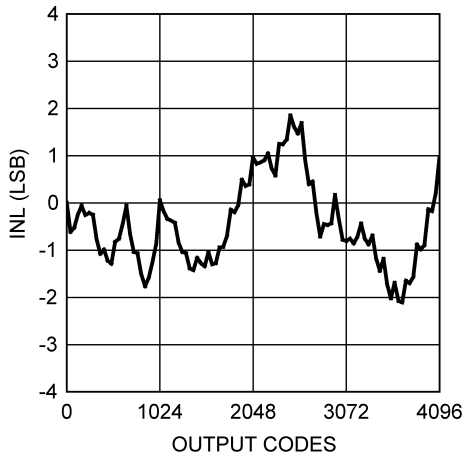


Figure 4. INL at V_A = 2.7 V

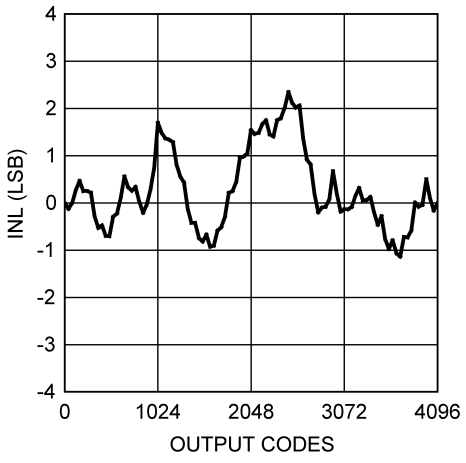


Figure 5. INL at V_A = 5.5 V

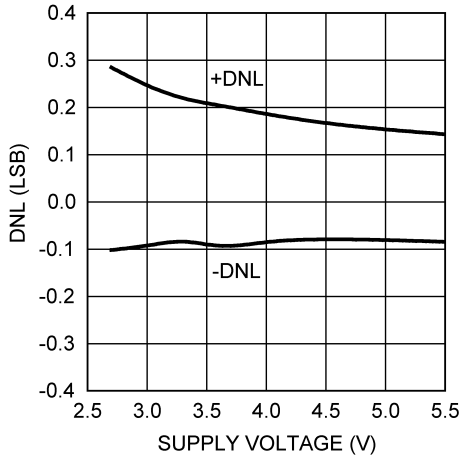


Figure 6. DNL vs V_A

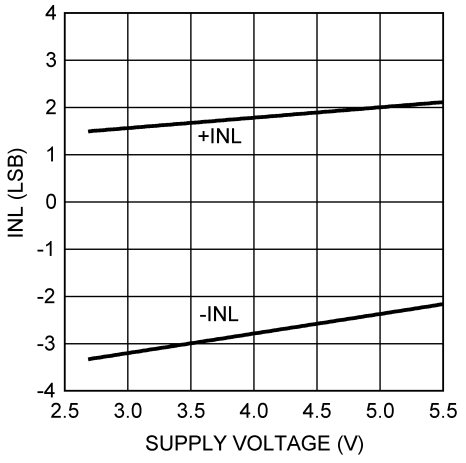


Figure 7. INL vs V_A

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Typical Characteristics (continued)

f_{SCLK} = 20 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated

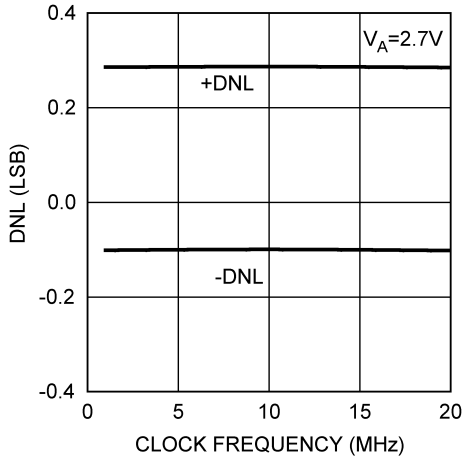


Figure 8. 2.7-V DNL vs f_{SCLK}

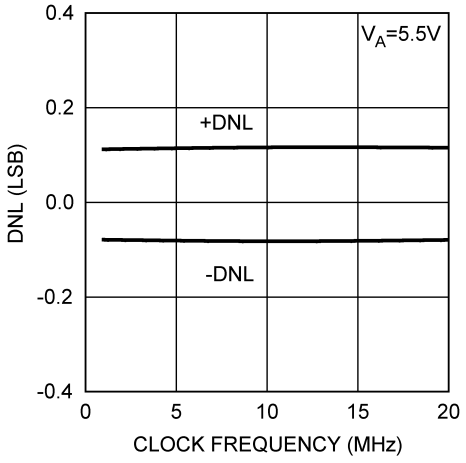


Figure 9. 5.5-V DNL vs f_{SCLK}

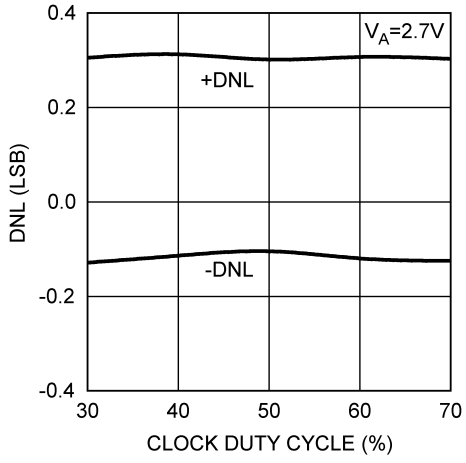


Figure 10. 2.7-V DNL vs Clock Duty Cycle

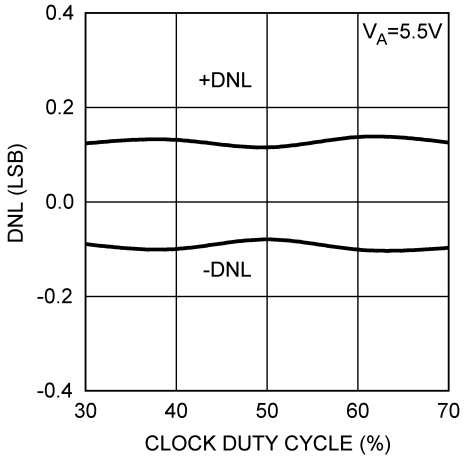


Figure 11. 5.5-V DNL vs Clock Duty Cycle

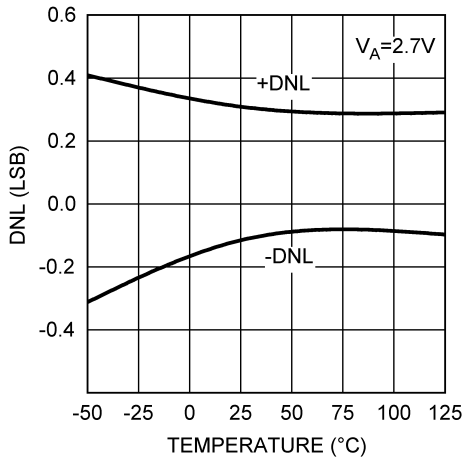


Figure 12. 2.7-V DNL vs Temperature

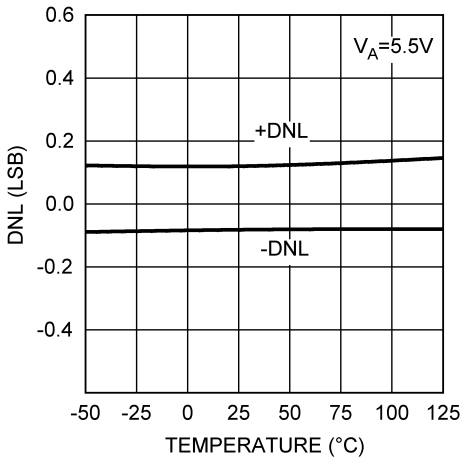


Figure 13. 5.5-V DNL vs Temperature

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Typical Characteristics (continued)

f_{SCLK} = 20 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated

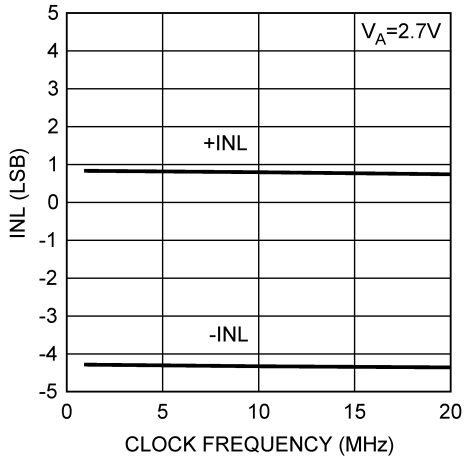


Figure 14. 2.7-V INL vs f_{SCLK}

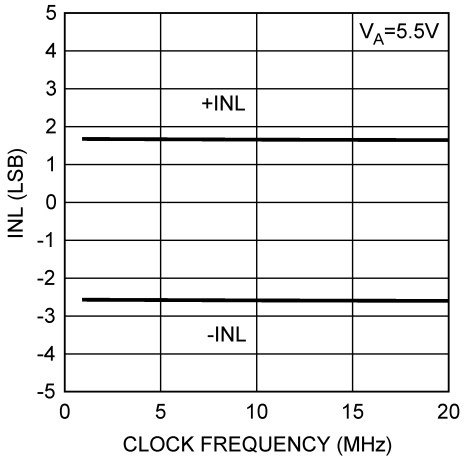


Figure 15. 5.5-V INL vs f_{SCLK}

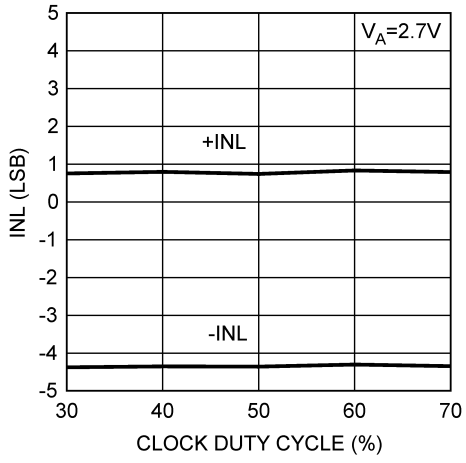


Figure 16. 2.7-V INL vs Clock Duty Cycle

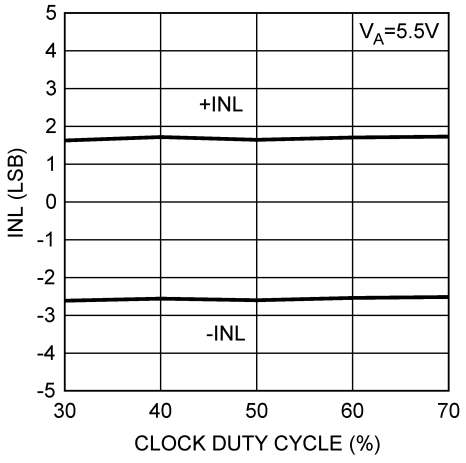


Figure 17. 5.5-V INL vs Clock Duty Cycle

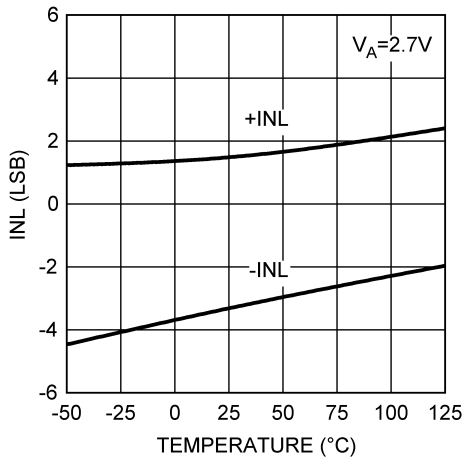


Figure 18. 2.7-V INL vs Temperature

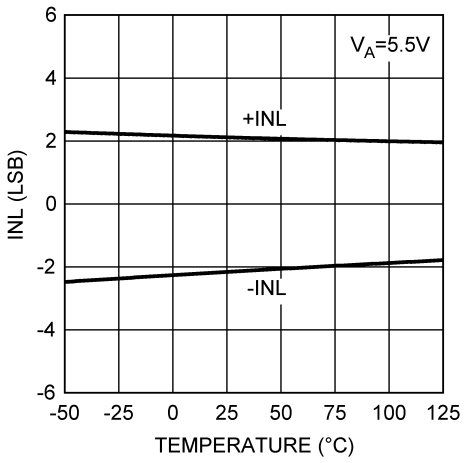


Figure 19. 5.5-V INL vs Temperature

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Typical Characteristics (continued)

f_{SCLK} = 20 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated

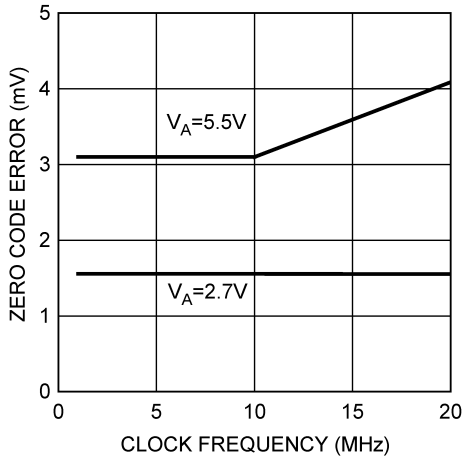


Figure 20. Zero Code Error vs f_{SCLK}

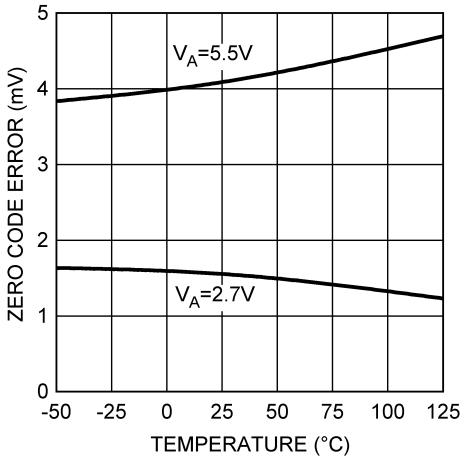


Figure 21. Zero Code Error vs Temperature

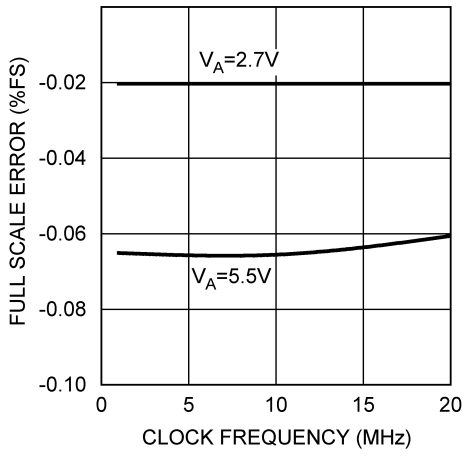


Figure 22. Full-Scale Error vs f_{SCLK}

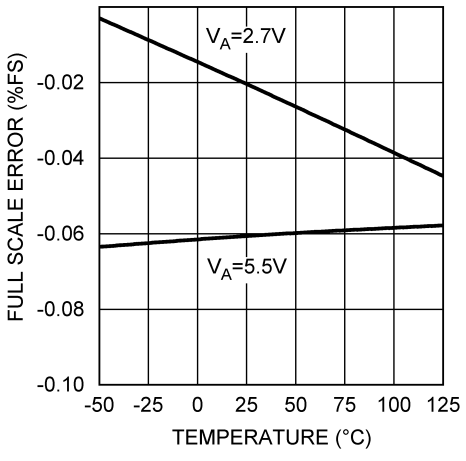


Figure 23. Full-Scale Error vs Temperature

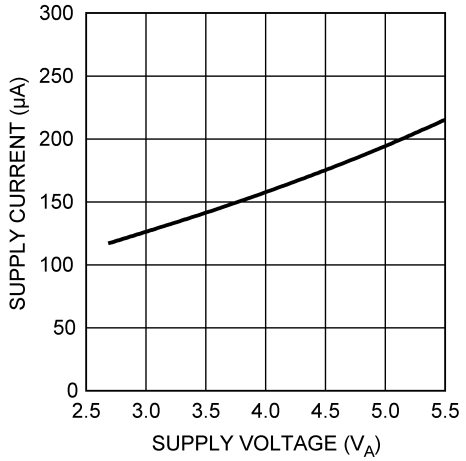


Figure 24. Supply Current vs V_A

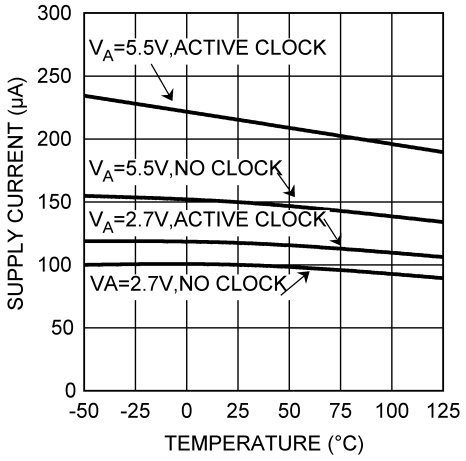


Figure 25. Supply Current vs Temperature

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Typical Characteristics (continued)

f_{SCLK} = 20 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated

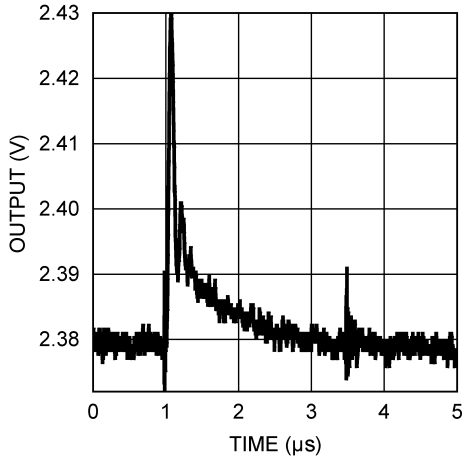


Figure 26. 5-V Glitch Response

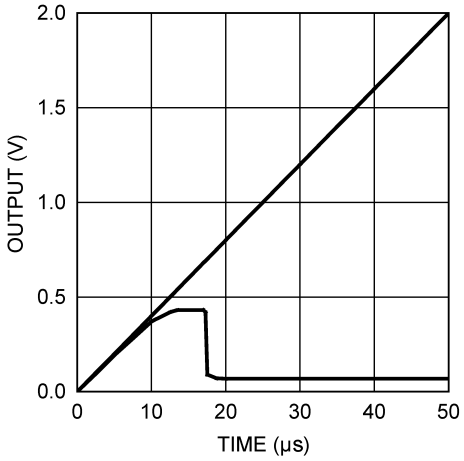


Figure 27. Power-On Reset

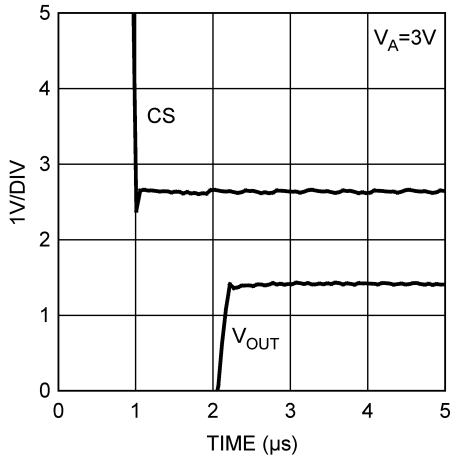


Figure 28. 3-V Wake-Up Time

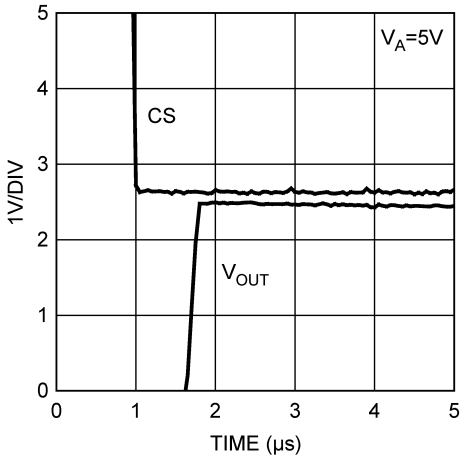


Figure 29. 5-V Wake-Up Time

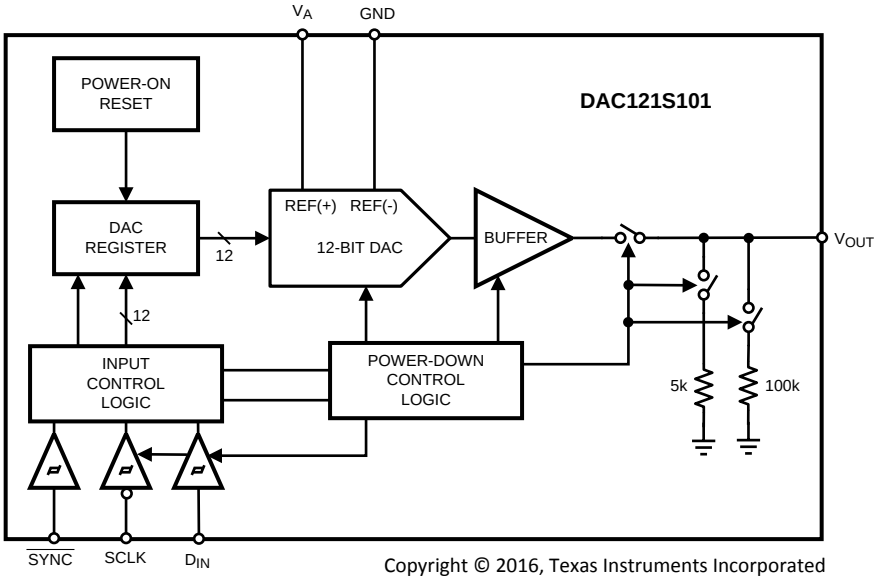
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7 Detailed Description

7.1 Overview

The DAC121S101QML-SP device is a full-featured, general purpose 12-bit voltage-output digital-to-analog converter (DAC). Control of the output of the DAC is achieved over a 3-wire SPI interface. Once the DAC output has been set, additional communication with the DAC is not required unless the output condition needs to be changed. Likewise, the DAC121S101QML-SP power-on state is 0 V. The DAC output will remain at 0 V until a valid write sequence is made.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DAC Section

The DAC121S101QML-SP is fabricated on a CMOS process with an architecture that consists of switches and a resistor string that are followed by an output buffer. The power supply serves as the reference voltage. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_A \times (D / 4096) \quad (1)$$

where

- *D* is the decimal equivalent of the binary code that is loaded into the DAC register and can take on any value between 0 and 4095.

7.3.2 Resistor String

Figure 30 shows the simplified resistor string. Conceptually, this string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. This configuration ensures that the DAC is monotonic.

Feature Description (continued)

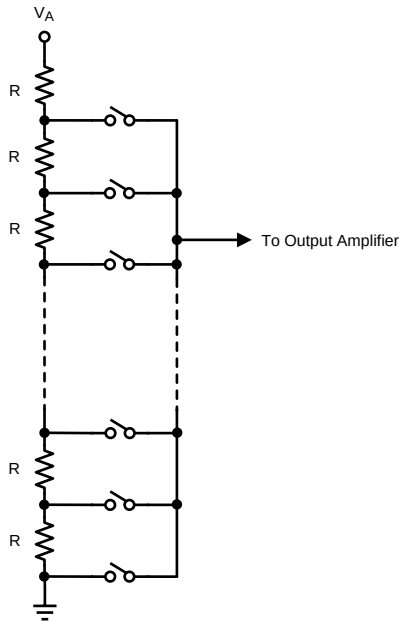


Figure 30. DAC Resistor String

7.3.3 Output Amplifier

The output buffer amplifier is a rail-to-rail type, providing an output voltage range of 0 V to V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0 V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. The output capabilities of the amplifier are described in the electrical tables in *Specifications*.

7.3.4 Power-On Reset

The power-on reset circuit controls the output voltage during power-up. Upon application of power, the DAC register is filled with zeros and the output voltage is 0 V and remains there until a valid write sequence is made to the DAC.

7.4 Device Functional Modes

7.4.1 Power-Down Modes

The DAC121S101QML-SP has four modes of operation. These modes are set with two bits (DB13 and DB12) in the control register.

Table 2. Modes of Operation

DB13	DB12	OPERATING MODE
0	0	Normal Operation
0	1	Power Down with 5 kΩ to GND
1	0	Power Down with 100 kΩ to GND
1	1	Power Down with Hi-Z

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When both DB13 and DB12 are 0, the device operates normally. For the other three possible combinations of these bits the supply current drops to its power-down level and the output is pulled down with either a 5-kΩ or a 100-kΩ resistor, or is in a high impedance state, as described in Table 2.

The bias generator, output amplifier, the resistor string, and other linear circuitry are all shut down in any of the power-down modes. Minimum power consumption is achieved in the power-down mode with SCLK disabled and $\overline{SYNC}$ and D_{IN} idled low.

7.5 Programming

7.5.1 Serial Interface

The three-wire interface is compatible with SPI, QSPI, and MICROWIRE, as well as most DSPs. See Figure 31 for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. When $\overline{SYNC}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the mode of operation or a change in the DAC register contents) is executed. At this point the $\overline{SYNC}$ line may be kept low or brought high. In either case, it must be brought high for the minimum specified time before the next write sequence as a falling edge of $\overline{SYNC}$ can initiate the next write cycle.

Because the $\overline{SYNC}$ and D_{IN} buffers draw more current when they are high, they must be idled low between write sequences to minimize power consumption.

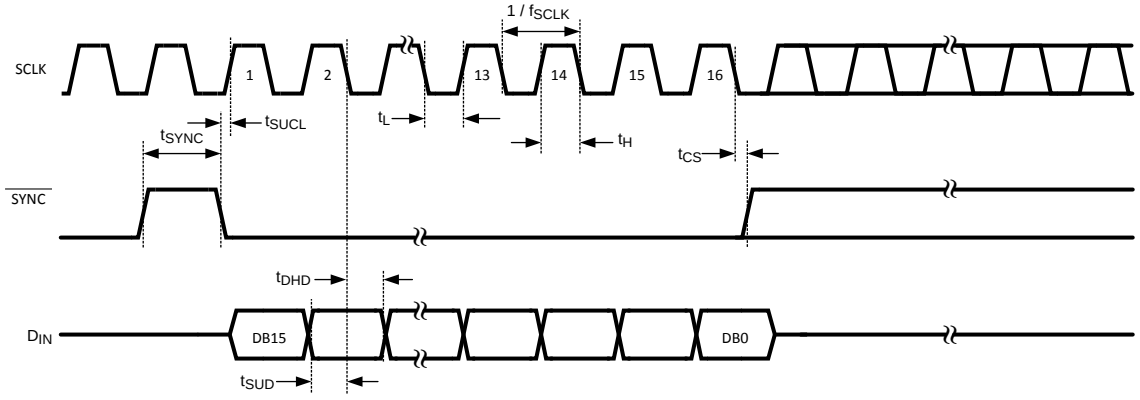


Figure 31. DAC121S101QML-SP Timing

7.5.2 Input Shift Register

The input shift register, Figure 32, has 16 bits. The first two bits are *don't cares* and are followed by two bits that determine the mode of operation (normal mode or one of three power-down modes). The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See the timing diagram, Figure 31.

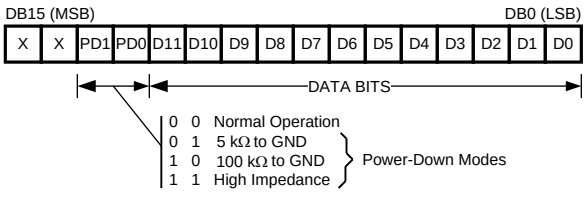


Figure 32. Input Register Contents

Programming (continued)

Normally, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, the shift register is reset and the write sequence is invalid. The DAC register is not updated and there is no change in the mode of operation or in the output voltage.

8 Application and Implementation

NOTE

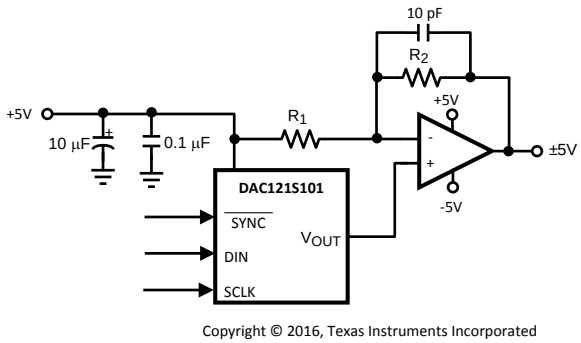
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The simplicity of the DAC121S101QML-SP implies ease of use. However, it is important to recognize that any data converter that uses its supply voltage as its reference voltage will have essentially zero PSRR (Power Supply Rejection Ratio). Therefore, it is necessary to provide a noise-free supply voltage to the device.

8.1.1 Bipolar Operation

The DAC121S101QML-SP is designed for single-supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 33. This circuit will provide an output voltage range of ±5 V. A rail-to-rail amplifier must be used if the amplifier supplies are limited to ±5 V.



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Figure 33. Bipolar Operation

The output voltage of this circuit for any code is found to be:

$$V_O = (V_A \times (D / 4096) \times ((R1 + R2) / R1) - V_A \times R2 / R1) \quad (2)$$

where

- D is the input code in decimal form

With VA = 5 V and R1 = R2,

$$V_O = (10 \times D / 4096) - 5\ V \quad (3)$$

8.1.2 DSP and Microprocessor Interfacing

Interfacing the DAC121S101QML-SP to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

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Application Information (continued)

8.1.2.1 ADSP-2101/ADSP2103 Interfacing

Figure 34 shows a serial interface between the DAC121S101QML-SP and the ADSP-2101/ADSP2103. The DSP must be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and should be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the Tx register after the SPORT mode has been enabled.

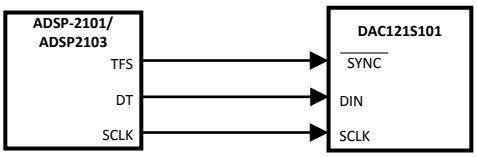


Figure 34. ADSP-2101/2103 Interface

8.1.2.2 80C51/80L51 Interface

Figure 35 shows a serial interface between the DAC121S101QML-SP and the 80C51/80L51 microcontroller. The SYNC signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is to transmitted to the DAC121S101QML-SP. Because the 80C51/80L51 transmits 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51/80L51 transmit routine must recognize that the 80C51/80L51 transmits data with the LSB first while the DAC121S101QML-SP requires data with the MSB first.

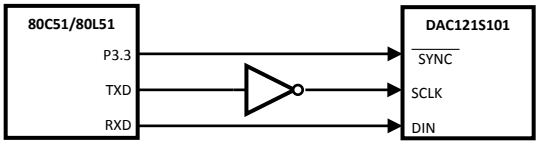


Figure 35. 80C51/80L51 Interface

8.1.2.3 68HC11 Interface

Figure 36 shows a serial interface between the DAC121S101QML-SP and the 68HC11 microcontroller. The SYNC line of the DAC121S101QML-SP is driven from a port line (PC7 in the figure), similar to the 80C51/80L51.

The 68HC11 must be configured with its CPOL bit as a zero and its CPHA bit as a one. This configuration causes data on the MOSI output to be valid on the falling edge of SCLK. PC7 is taken low to transmit data to the DAC. The 68HC11 transmits data in 8-bit bytes with eight falling clock edges. Data is transmitted with the MSB first. PC7 must remain low after the first eight bits are transferred. A second write cycle is initiated to transmit the second byte of data to the DAC, after which PC7 must be raised to end the write sequence.

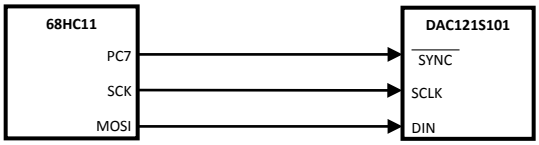


Figure 36. 68HC11 Interface

8.1.2.4 Microwire Interface

Figure 37 shows an interface between a Microwire-compatible device and the DAC121S101QML-SP. Data is clocked out on the rising edges of the SCLK signal.

Application Information (continued)

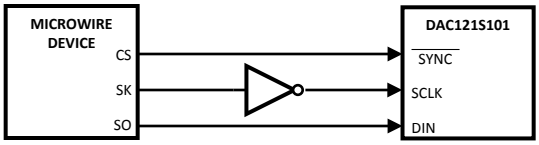


Figure 37. Microwire Interface

8.1.3 Radiation Environments

Carefully consider the environmental conditions when using a product in a radiation environment. Radiation on test reports are available on TI.com/radiation.

8.1.3.1 Total Ionizing Dose

The products with the radiation hardness assurance (RHA) levels listed in the are qualified for low dose rate environments only.

8.1.3.1.1 DAC121S101WGRQV 5962R0722601VZA

This product is tested and qualified per MIL-STD-883 Test Method 1019, Condition A and the *extended room temperature anneal test* where a high-dose irradiation followed by a room temperature anneal is used to simulate a dose rate of 0.027 rad(Si)/s and is qualified for environments with radiation levels of 0.027 rad(Si)/s or lower.

8.1.3.1.2 DAC121S101WGRLV 5962R0722602VZA

This product is tested and qualified per MIL-STD-883 Test Method 1019, Condition D at a dose rate of 0.01 rad(Si)/s and are qualified for environments with radiation levels of 0.01 rad(Si)/s or lower.

8.1.3.2 Single Event Latch-Up and Functional Interrupt

One-time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LETth) shown in *Features* is the maximum LET tested. A test report is available upon request.

8.1.3.3 Single Event Upset

A report on single event upset (SEU) is available at TI.com/radiation.

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8.2 Typical Application

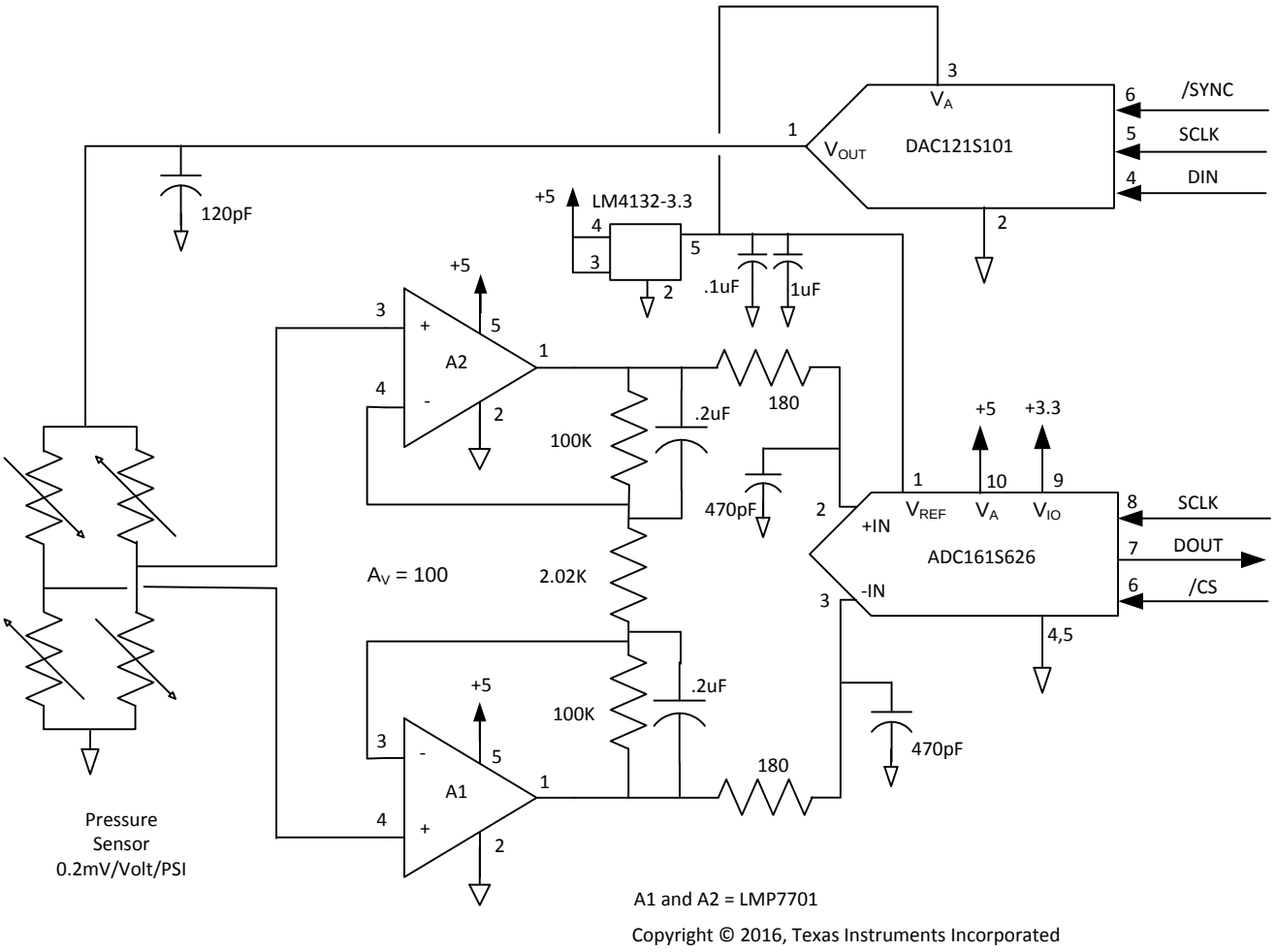


Figure 38. Pressure Sensor Gain Adjust

8.2.1 Design Requirements

The DAC121S101QML-SP is a positive supply-only data acquisition system capable of digitizing a pressure sensor output. In addition to digitizing the pressure sensor output, the system designer can use the DAC121S101 to correct for gain errors in the pressure sensor output by adjusting the bias voltage to the bridge pressure sensor.

8.2.2 Detailed Design Procedure

As shown in Equation 4, the output of the pressure sensor is relative to the imbalance of the resistive bridge times the output of the DAC121S101, thus providing the desired gain correction.

$$\text{Pressure Sensor Output} = (\text{DAC_Output} \times [(R2 / (R1 + R2) - (R4 / (R3 + R4)] \quad (4)$$

Likewise for the ADC161S626, Equation 5 shows that the ADC output is function of the Pressure Sensor Output times relative to the ratio of the ADC input divided by the DAC121S101 output voltage.

$$\text{ADC161S626 Output} = (\text{Pressure Sensor Output} \times 100 / (2 \times \text{VREF})) \times 2^{16} \quad (5)$$

Typical Application (continued)

8.2.3 Application Curve

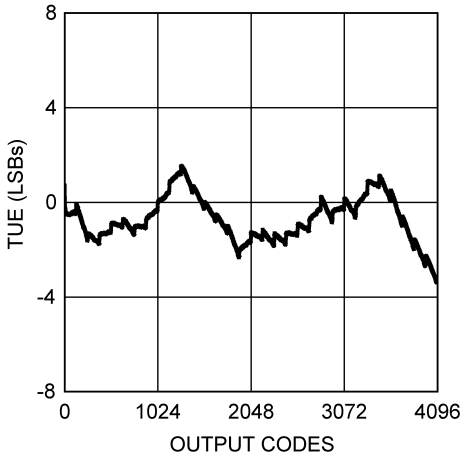


Figure 39. Total Unadjusted Error vs Output Code

9 Power Supply Recommendations

9.1 Using References as Power Supplies

Recall the need for a quiet supply source for devices that use their power supply voltage as a reference voltage.

Because the DAC121S101QML-SP consumes very little power, a reference source may be used as the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low-noise regulators can also be used for the power supply of the DAC121S101QML-SP. The following sections describe a few power supply options for the DAC121S101QML-SP.

9.1.1 LM4050QML-SP

The LM4050QML-SP is a space-grade, radiation-qualified shunt reference within an accuracy of ±0.1% at room temperature and a temperature coefficient of 23 ppm/°C.

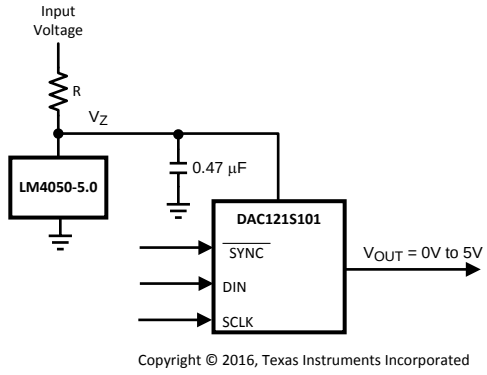


Figure 40. The LM4050 as a Power Supply

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Using References as Power Supplies (continued)

The minimum resistor value in the circuit of Figure 40 must be chosen such that the maximum current through the LM4050 does not exceed its 15-mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, the resistor value at its minimum due to tolerance, and the DAC121S101QML-SP draws zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC121S101QML-SP current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC121S101QML-SP draws its maximum current. These conditions can be summarized as:

$$R(min) = (V_{IN}(max) - V_Z(min) / (I_A(min) + I_Z(max)) \quad (6)$$

and

$$R(max) = (V_{IN}(min) - V_Z(max) / (I_A(max) + I_Z(min)) \quad (7)$$

where

- $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature
- $I_Z(max)$ is the maximum allowable current through the LM4050
- $I_Z(min)$ is the minimum current required by the LM4050 for proper regulation
- $I_A(max)$ is the maximum DAC121S101QML-SP supply current
- $I_A(min)$ is the minimum DAC121S101QML-SP supply current

9.1.2 LP3985

The LP3985 is a low-noise, ultra-low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC121S101QML-SP. It comes in 3-V, 3.3-V, and 5-V versions, among others, and sports a low 30-µV noise specification at low frequencies. Because low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT-23 and 5-bump DSBGA packages.

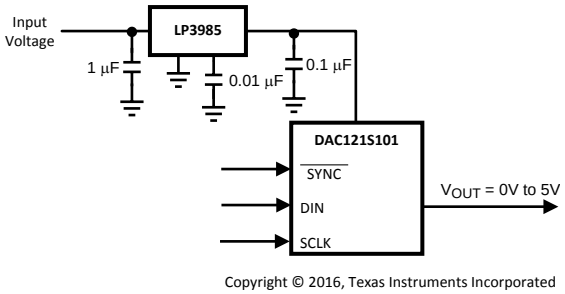


Figure 41. Using the LP3985 Regulator

An input capacitance of 1 µF without any ESR requirement is required at the LP3985 input, while a 1-µF ceramic capacitor with an ESR requirement of 5 mΩ to 500 mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

Using References as Power Supplies (continued)

9.1.3 LP2980-N

The LP2980-N is an ultra-low dropout regulator with a 0.5% or 1% accuracy over temperature, depending upon grade. It is available in 3-V, 3.3-V, and 5-V versions, among others.

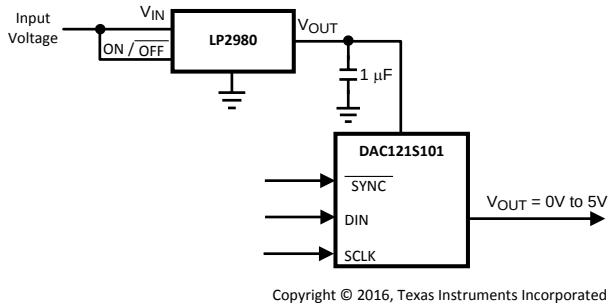


Figure 42. Using the LP2980-N Regulator

Like any low-dropout regulator, the LP2980-N requires an output capacitor for loop stability. This output capacitor must be at least 1 µF over temperature, but values of 2.2 µF or more will provide even better performance. The ESR of this capacitor must be within the range specified in the ***LP2980-N data sheet***. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980-N. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

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10 Layout

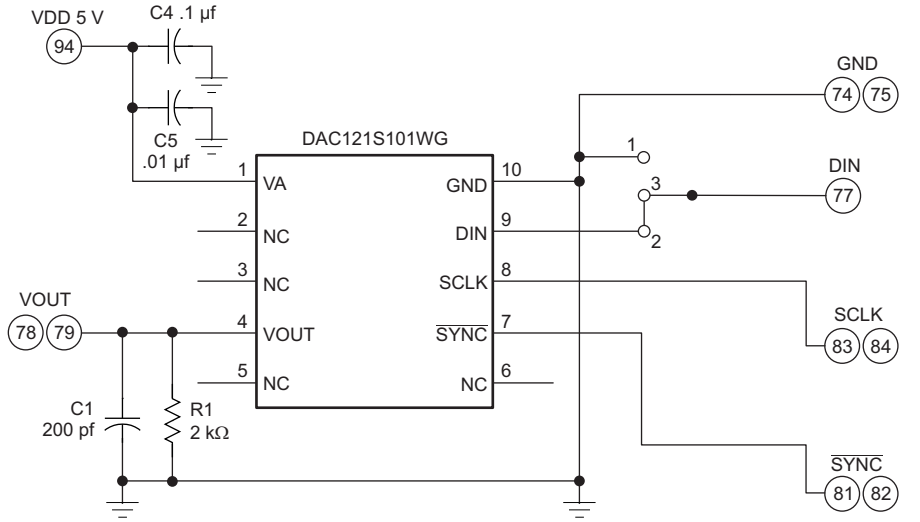
10.1 Layout Guidelines

For best accuracy and minimum noise, the printed-circuit board containing the DAC121S101QML-SP must have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located in the same board layer. There must be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will use a *fencing* technique to prevent the mixing of analog and digital ground current. Separate ground planes must only be used when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC121S101QML-SP. Take special care to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The DAC121S101QML-SP power supply must be bypassed with a 10-µF and a 0.1-µF capacitor as close as possible to the device with the 0.1 µF right at the device supply pin. The 10-µF capacitor must be a tantalum type and the 0.1-µF capacitor should be a low ESL, low ESR type. The power supply for the DAC121S101QML-SP must only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines must have controlled impedances.

10.2 Layout Example



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Note: N/C pins can be left floating or connected to ground

Figure 43. DAC121S101 Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support, see the following:

- 5962R07726
- Radiation Data for Space

11.1.2 Device Nomenclature

11.1.2.1 Specification Definitions

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 4096 = V_A / 4096.

DIGITAL FEEDTHROUGH is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR is the difference between the actual output voltage with a full scale code (FFFh) loaded into the DAC and the value of V_A x 4095 / 4096.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Tables.

LEAST SIGNIFICANT BIT (LSB) is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_{REF} / 2^n \quad (8)$$

where V_{REF} is the supply voltage for this product, and n is the DAC resolution in bits, which is 12 for the DAC121S101QML-SP.

MAXIMUM LOAD CAPACITANCE is the maximum capacitance that can be driven by the DAC with output stability maintained.

MONOTONICITY is the condition of being monotonic, where the DAC has an output that never decreases when the input code increases.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_A.

POWER EFFICIENCY is the ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents is the power consumed by the device without a load.

SETTLING TIME is the time for the output to settle to within 1/2 LSB of the final value after the input code is updated.

WAKE-UP TIME is the time for the output to exit power-down mode. This is the time measured from the falling edge of 16th SCLK pulse to when the output voltage deviates from the power-down voltage of 0 V.

ZERO CODE ERROR is the output error, or voltage, present at the DAC output after a code of 000h has been entered.

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

LP2980-N Micropower 50-mA Ultra Low-Dropout Regulator in SOT-23 Package, SNOS733

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Engineering Samples

Engineering samples are available for order and are identified by the "MPR" in the orderable device name (see Packaging Information in the Addendum). Engineering (MPR) samples meet the performance specifications of the datasheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that would not impact the performance at room temperature, such as radiation or reliability testing.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R0722601VZA	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DAC121S101 WGRQMLV Q 5962R07226 01VZA ACO 01VZA >T
5962R0722602VZA	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DAC121S101 WGRLV Q 5962R07226 02VZA ACO 02VZA >T
DAC121S101 MDR	Active	Production	DIESALE (Y) | 0	10 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
DAC121S101WGMPR	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	25 to 25	DAC121S101 WGMPR ES ACO >T
DAC121S101WGMPR.A	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	25 to 25	DAC121S101 WGMPR ES ACO >T
DAC121S101WGRLV	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DAC121S101 WGRLV Q 5962R07226 02VZA ACO 02VZA >T
DAC121S101WGRLV.A	Active	Production	CFP (NAC) | 10	124 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DAC121S101 WGRLV Q 5962R07226 02VZA ACO 02VZA >T
DAC121S101WGRQV	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DAC121S101 WGRQMLV Q 5962R07226 01VZA ACO 01VZA >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC121S101WGRQV.A	Active	Production	CFP (NAC) | 10	54 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	DAC121S101 WGRQMLV Q 5962R07226 01VZA ACO 01VZA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

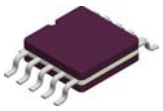
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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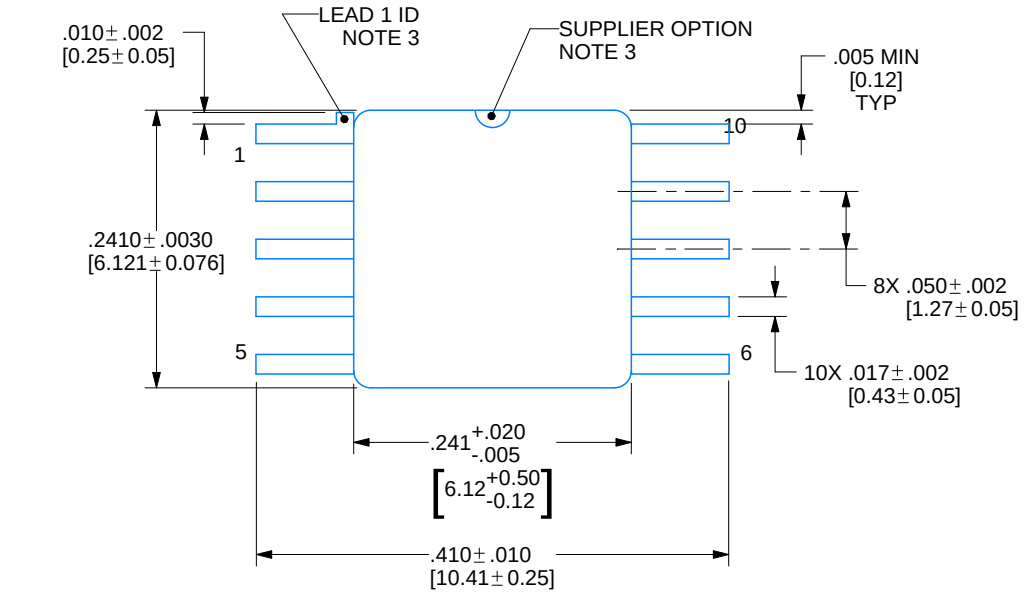


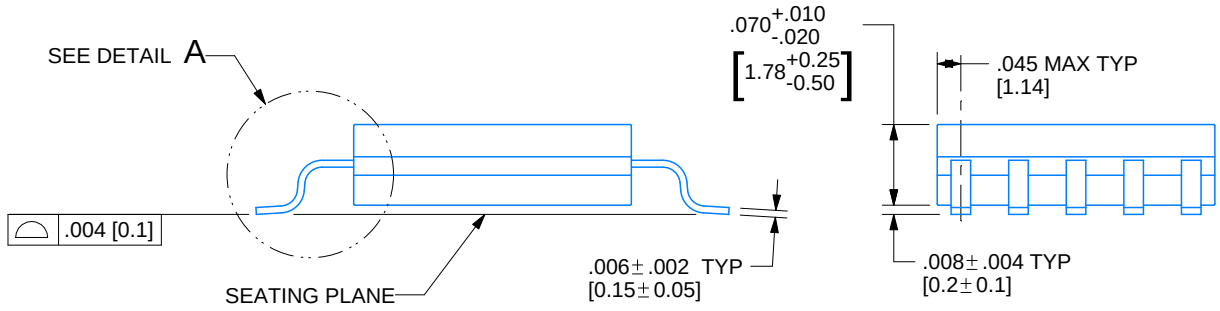
PACKAGE OUTLINE

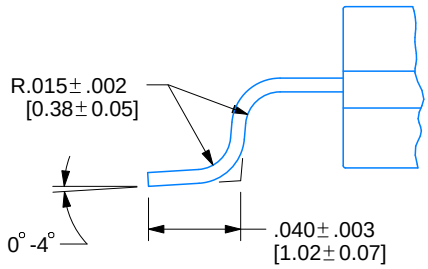
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK







DETAIL A
TYPICAL

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NOTES:

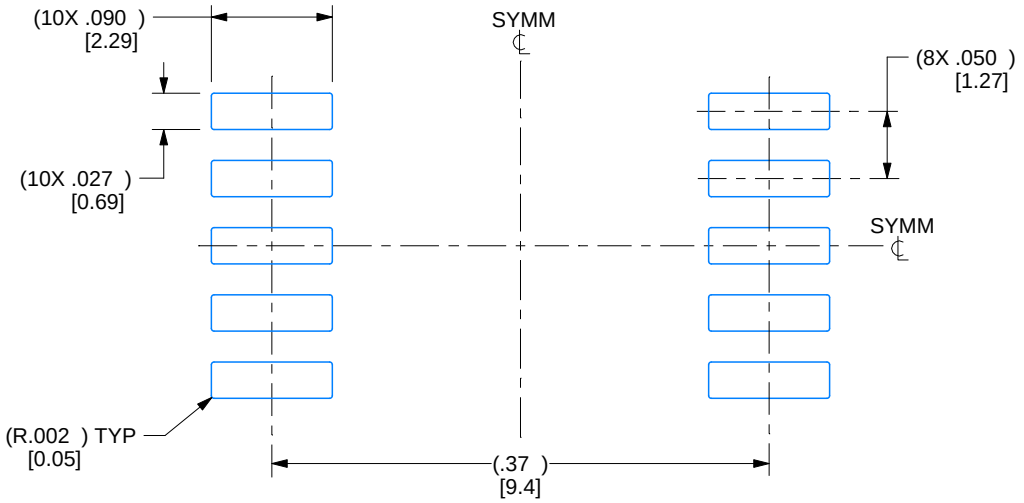
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

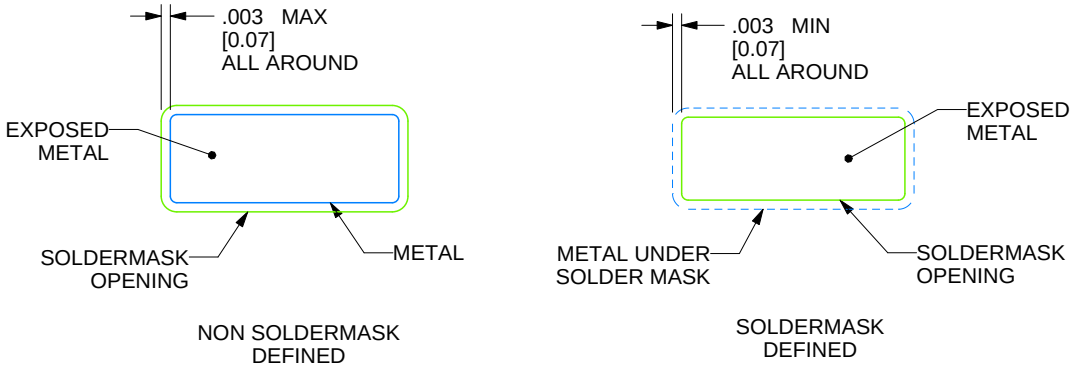
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



4215196/D 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197877	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198820	02/14/2022	K. SINCERBOX
C	CHANGE PIN 1 ID LOCATION ON PIN	2198845	02/18/2022	D. CHIN / K. SINCERBOX
D	.2410± .0030 WAS .2700 +.0012/-.0002;	2200915	08/08/2022	D. CHIN / K. SINCERBOX

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