ADC128S102QML-SP Radiation Hardened 8-Channel, 50 kSPS to 1 MSPS, 12-Bit A/D Converter

1 Features

- 5962R07227
  - Total Ionizing Dose 100 krad(Si)
  - Single Event Latch-Up Immune 120 MeV-cm^2/mg
  - Single Event Functional Interrupt Immune 120 MeV-cm^2/mg
    (See *Radiation Report*)
- Eight Input Channels
- Variable Power Management
- Independent Analog and Digital Supplies
- SPI™/QSPI™/MICROWIRE™/DSP Compatible
- Packaged in 16-Lead Ceramic SOIC
- Key Specifications
  - Conversion Rate: 50 kSPS to 1 MSPS
  - DNL (V_A = V_D = 5 V): +1.5 / −0.9 LSB (Maximum)
  - INL (V_A = V_D = 5 V): +1.4 / −1.25 LSB (Maximum)
  - Power Consumption
    - 3-V Supply: 2.3 mW (Typical)
    - 5-V Supply: 10.7 mW (Typical)

2 Applications

- Satellites
  - Attitude and Orbit Control
  - Precision Sensors
  - Motor Control
- High Temperature
- Medical Systems
- Accelerators

3 Description

The ADC128S102 device is a low-power, eight-channel CMOS 12-bit analog-to-digital converter specified for conversion throughput rates of 50 kSPS to 1 MSPS. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. The device can be configured to accept up to eight input signals at inputs IN0 through IN7.

The output serial data is straight binary and is compatible with several standards, such as SPI, QSPI, MICROWIRE, and many common DSP serial interfaces.

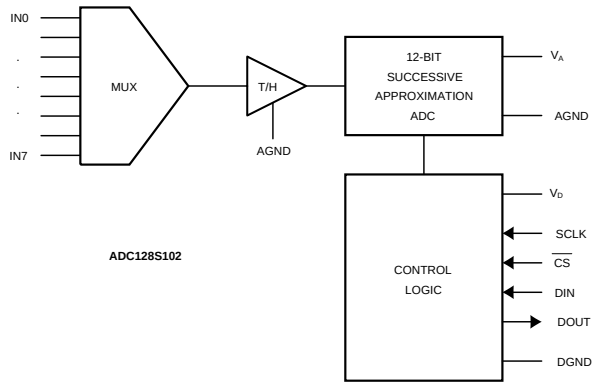
The ADC128S102 may be operated with independent analog and digital supplies. The analog supply (V_A) can range from 2.7 V to 5.25 V, and the digital supply (V_D) can range from 2.7 V to V_A. Normal power consumption using a 3-V or 5-V supply is 2.3 mW and 10.7 mW, respectively. The power-down feature reduces the power consumption to 0.06 µW using a 3-V supply and 0.25 µW using a 5-V supply.

Device Information[1]

PART NUMBER	GRADE	PACKAGE
ADC128S102WGRQV	5962R0722701VZA 100 krad	16-lead ceramic SOIC
ADC128S102WRQV	5962R0722701VFA 100 krad	16-lead ceramic flatpack
ADC128S102-MDR	5962R0722701V9A 100 krad	Die
ADC128S102WGMPR	Pre-Flight Engineering Prototype	16-lead ceramic SOIC
ADC128S102CVAL	Ceramic Evaluation Board	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (November 2016) to Revision P — **Page**

- Changed feature link from 5962R07727 to 5962R07227 ... 1

Changes from Revision N (September 2015) to Revision O — **Page**

- Changed the title of the ADC128S102QML-SP data sheet ... 1
- Added *Radiation Report* link to *Features* ... 1
- Changed *Applications* ... 1
- Changed *Device Information* table ... 1
- Added 14-pin CFP package option to the data sheet ... 1
- Added TYPE column to the *Pin Functions* table ... 4
- Added tablenote for digital supply voltage maximums allowed in the *Absolute Maximum Ratings* table ... 5
- Updated maximum tablenote for the digital supply voltage in the *Absolute Maximum Ratings* table ... 5
- Added tablenote for the voltage on any pin to GND maximums allowed in the *Absolute Maximum Ratings* table ... 5
- Added links to the *Quality Conformance Inspection* table to the *Electrical Characteristics* tables ... 6
- Added MIN and MAX test conditions for the SCLK duty cycle in the *Electrical Characteristics: ADC128S102QML-SP Converter* table ... 8
- Changed *ADC128S102 Operational Timing Diagram* image ... 10
- Changed first sentence and added MIL-STD-883G, Test Method 1019.7 link to the *Total Ionizing Dose* section ... 18
- Changed total ionizing dose rate from 0.16 to 0.027 rad(Si)/s ... 18
- Changed *Single Event Latch-Up* section to *Single Event Latch-Up and Functional Interrupt* ... 18
- Added sentence to *Serial Interface* section: Note that $\overline{CS}$ is asynchronous. ... 19
- Added *Engineering Samples* section ... 27

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Changes from Revision H (October 2009) to Revision N **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision G (October 2009) to Revision H **Page**

- Added reference to Note 11. 5
- Added Note:11. 5
- Deleted 'TYPICAL' numbers from t_{DHID}, t_{DS} and t_{DIH} 6
- Changed Min limit on t_{DHID} from 11 to 7. 6

Changes from Revision F (June 2009) to Revision G **Page**

- Deleted reference to Ta Min and Ta Max under titled sections. 6

Changes from Revision E (April 2009) to Revision F **Page**

- Changed AC Electrical Characteristics - SCLK Duty Cycle, typ limits 8

Changes from Revision C (November 2008) to Revision D **Page**

- Moved Rad information from Key Specifications to *Features* 1
- Deleted ADC128S102WGMLS reference 6
- Added *Burn In Delta* Table 9

Changes from Revision B (August 2008) to Revision C **Page**

- Corrected package reference from 16-lead TSSOP to 16-lead Ceramic SOIC, Removed QV NSID reference and Added SMD Number to RQV NSID in *Features*. 1

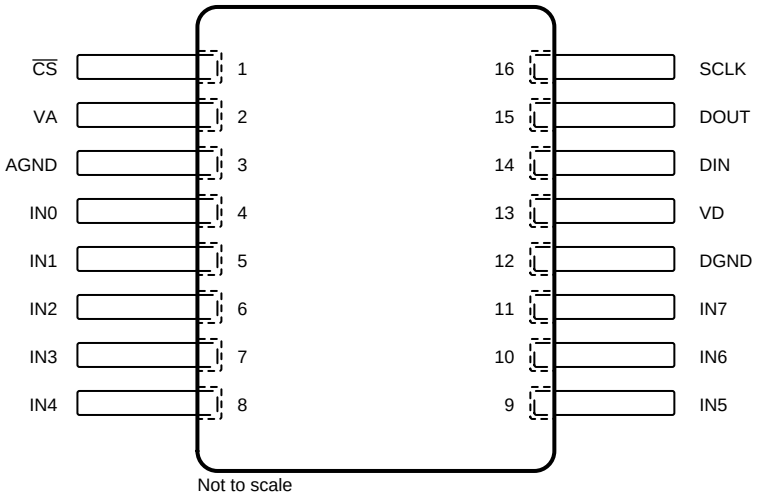
Changes from Revision A (August 2008) to Revision B **Page**

- Typo, Changed Figure 2, t_{DIS} lower left hand side changed to t_{DS} and t_{DIH} lower left hand side change to t_{DH} in Timing Diagrams. 10

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5 Pin Configuration and Functions

NAC Package
16-Pin CFP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ANALOG I/O			
IN0 to IN7	4	Input (Analog)	Analog inputs. These signals can range from 0 V to V_{REF}.
	5		
	6		
	7		
	8		
	9		
	10		
	11		
DIGITAL I/O			
$\overline{CS}$	1	Input (Digital)	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
DIN	14	Input (Digital)	Digital data input. The ADC128S102QML-SP's Control Register is loaded through this pin on rising edges of the SCLK pin.
DOUT	15	Output (Digital)	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
SCLK	16	Input (Digital)	Digital clock input. The specified performance range of frequencies for this input is 0.8 MHz to 16 MHz. This clock directly controls the conversion and readout processes.
POWER SUPPLY			
AGND	3	Ground	The ground return for the analog supply and signals.
DGND	12	Ground	The ground return for the digital supply and signals.
V_A	2	Supply	Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet 2.7 V to 5.25 V source and bypassed to GND with 1-µF and 0.1-µF monolithic ceramic capacitors located within 1 cm of the power pin.
V_D	13	Supply	Positive digital supply pin. This pin should be connected to a 2.7 V to V_A supply, and bypassed to GND with a 0.1-µF monolithic ceramic capacitor located within 1 cm of the power pin.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_A	Analog supply voltage	–0.3	6.5	V
V_D	Digital supply voltage(2)	–0.3	V_A + 0.3	V
	Voltage on any pin to GND	–0.3	V_A + 0.3	V
	Input current at any pin (3)		±10	mA
	Power dissipation T_A = 25°C		See (4)	
	Package input current(3)		±20 mA	mA
	Soldering temperature, 10 seconds		260	°C
	Junction temperature		175	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum voltage is not to exceed 6.5 V
(3) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} less than AGND or V_{IN} greater than V_A or V_D), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(4) The absolute maximum junction temperature ($T_J$max) for this device is 175°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($R_{\theta JA}$), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/R_{\theta JA}$. The values for maximum power dissipation listed above will be reached only when the ADC128S102QML-SP is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±8000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model is 100-pF capacitor discharged through a 1.5-kΩ resistor. Machine model is 220 pF discharged through 0 Ω.

6.3 Recommended Operating Conditions

See (1)(2)

	MIN	MAX	UNIT
Operating temperature	–55	125	°C
V_A supply voltage	2.7	5.25	V
V_D supply voltage	2.7	V_A	V
Digital input voltage	0	V_A	V
Analog input voltage	0	V_A	V
Clock frequency	0.8	16	MHz

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but **do not** verify specific performance limits. For specifications and test conditions, see the *Electrical Characteristics*. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.

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6.4 Thermal Information

THERMAL METRIC[1]		ACD128S102QML-SP NAC (CFP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: ADC128S102QML-SP Converter

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, C_L = 50pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	SUBGROUP	MIN	TYP[1]	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS							
	Resolution with no missing codes					12	Bits
INL	Integral non-linearity (end point method)	$V_A = V_D$ = 3 V	[1, 2, 3]	–1	±0.6	1.1	LSB
		$V_A = V_D$ = 5 V	[1, 2, 3]	–1.25	±0.9	1.4	LSB
DNL	Differential non-linearity	$V_A = V_D$ = 3 V	[1, 2, 3]		0.5	0.9	LSB
			[1, 2, 3]	–0.7	–0.3		LSB
		$V_A = V_D$ = 5 V	[1, 2, 3]		0.9	1.5	LSB
			[1, 2, 3]	–0.9	−0.5		LSB
V_{OFF}	Offset error	$V_A = V_D$ = 3 V	[1, 2, 3]	–2.3	0.8	2.3	LSB
		$V_A = V_D$ = 5 V	[1, 2, 3]	–2.3	1.1	2.3	LSB
OEM	Offset error match	$V_A = V_D$ = 3 V	[1, 2, 3]	–1.5	±0.1	1.5	LSB
		$V_A = V_D$ = 5 V	[1, 2, 3]	–1.5	±0.3	1.5	LSB
FSE	Full scale error	$V_A = V_D$ = 3 V	[1, 2, 3]	–2	0.8	2	LSB
		$V_A = V_D$ = 5 V	[1, 2, 3]	–2	0.3	2	LSB
FSEM	Full scale error match	$V_A = V_D$ = 3 V	[1, 2, 3]	–1.5	±0.1	1.5	LSB
		$V_A = V_D$ = 5 V	[1, 2, 3]	–1.5	±0.3	1.5	LSB
DYNAMIC CONVERTER CHARACTERISTICS							
FPBW	Full power bandwidth (–3 dB)	$V_A = V_D$ = 3 V			6.8		MHz
		$V_A = V_D$ = 5 V			10		MHz
SINAD	Signal-to-noise plus distortion ratio	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]	68	72		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]	68	72		dB
SNR	Signal-to-noise ratio	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]	69	72		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]	68.5	72		dB
THD	Total harmonic distortion	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]		–86	–74	dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]		–87	–74	dB
SFDR	Spurious-free dynamic range	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]	75	91		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]	75	90		dB

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms.

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Electrical Characteristics: ADC128S102QML-SP Converter (continued)

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, C_L = 50pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	SUBGROUP	MIN	TYP(1)	MAX	UNIT
ENOB	Effective number of bits	$V_A = V_D = 3$ V, f_{IN} = 40.2 kHz	[4, 5, 6]	11.1	11.6		Bits
		$V_A = V_D = 5$ V, f_{IN} = 40.2 kHz, −0.02 dBFS	[4, 5, 6]	11.1	11.6		Bits
ISO	Channel-to-channel isolation	$V_A = V_D = 3$ V, f_{IN} = 20 kHz			84		dB
		$V_A = V_D = 5$ V, f_{IN} = 20 kHz, −0.02 dBFS			85		dB
IMD	Intermodulation distortion, second order terms	$V_A = V_D = 3$ V, f_a = 19.5 kHz, f_b = 20.5 kHz	[4, 5, 6]		–93	–78	dB
		$V_A = V_D = 5$ V, f_a = 19.5 kHz, f_b = 20.5 kHz	[4, 5, 6]		–93	–78	dB
	Intermodulation distortion, third order terms	$V_A = V_D = 3$ V, f_a = 19.5 kHz, f_b = 20.5 kHz	[4, 5, 6]		–91	–70	dB
		$V_A = V_D = 5$ V, f_a = 19.5 kHz, f_b = 20.5 kHz	[4, 5, 6]		–91	–70	dB
ANALOG INPUT CHARACTERISTICS							
V_{IN}	Input range				0 to V_A		V
I_{DCL}	DC leakage current		[1, 2, 3]		±0.01	±1	µA
C_{INA}	Input capacitance	Track mode, see (2)			38		pF
		Hold mode, see (2)			4.5		pF
DIGITAL INPUT CHARACTERISTICS							
V_{IH}	Input high voltage	$V_A = V_D = 2.7$ V to 3.6 V	[1, 2, 3]	2.1			V
		$V_A = V_D = 4.75$ V to 5.25 V	[1, 2, 3]	2.4			V
V_{IL}	Input low voltage	$V_A = V_D = 2.7$ V to 5.25 V	[1, 2, 3]			0.8	V
I_{IN}	Input current	V_{IN} = 0 V or V_D	[1, 2, 3]		±1	±1	µA
C_{IND}	Digital input capacitance	See (2)				3.5	pF
DIGITAL OUTPUT CHARACTERISTICS							
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA, $V_A = V_D = 2.7$ V to 5.25 V	[1, 2, 3]	V_D –0.5			V
V_{OL}	Output low voltage	I_{SINK} = 200 µA to 1 mA, $V_A = V_D = 2.7$ V to 5.25 V	[1, 2, 3]			0.4	V
I_{OZH}, I_{OZL}	Hi-impedance output leakage current	$V_A = V_D = 2.7$ V to 5.25 V	[1, 2, 3]		±0.01	±1	µA
C_{OUT}	Hi-impedance output capacitance	See (2)				3.5	pF
	Output coding			Straight (Natural) Binary			
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)							
V_A, V_D	Analog and digital supply voltages	$V_A \geq V_D$	[1, 2, 3]	2.7			V
			[1, 2, 3]			5.25	V
$I_A + I_D$	Total supply current, normal mode ($\overline{CS}$ low)	$V_A = V_D = 2.7$ V to 3.6 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz	[1, 2, 3]		0.9	1.5	mA
		$V_A = V_D = 4.75$ V to 5.25 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz	[1, 2, 3]		2.2	3.1	mA
	Total supply current, shutdown mode ($\overline{CS}$ high)	$V_A = V_D = 2.7$ V to 3.6 V, f_{SCLK} = 0 kSPS	[1, 2, 3]		0.11	1	µA
		$V_A = V_D = 4.75$ V to 5.25 V, f_{SCLK} = 0 kSPS	[1, 2, 3]		0.12	1.4	µA

(2) This parameter is specified by design and/or characterization and is not tested in production.

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Electrical Characteristics: ADC128S102QML-SP Converter (continued)

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, C_L = 50pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		SUBGROUP	MIN	TYP[1]	MAX	UNIT
P_C	Power consumption, normal mode ($\overline{CS}$ low)	$V_A = V_D$ = 3 V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		[1, 2, 3]		2.7	4.5	mW
		$V_A = V_D$ = 5 V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		[1, 2, 3]		11.0	15.5	mW
	Power consumption, shutdown mode ($\overline{CS}$ high)	$V_A = V_D$ = 3 V f_{SCLK} = 0 kSPS		[1, 2, 3]		0.33	3	µW
		$V_A = V_D$ = 5 V f_{SCLK} = 0 kSPS		[1, 2, 3]		0.6	7	µW
AC ELECTRICAL CHARACTERISTICS								
f_{SCLK} MIN	Minimum clock frequency	$V_A = V_D$ = 2.7 V to 5.25 V		[9, 10, 11]	0.8			MHz
f_{SCLK}	Maximum clock frequency	$V_A = V_D$ = 2.7 V to 5.25 V		[9, 10, 11]			16	MHz
f_S	Sample rate continuous mode	$V_A = V_D$ = 2.7 V to 5.25 V		[9, 10, 11]	50			kSPS
				[9, 10, 11]			1	MSPS
$t_{CONVERT}$	Conversion (hold) time	$V_A = V_D$ = 2.7 V to 5.25 V		[9, 10, 11]			13	SCLK cycles
DC	SCLK duty cycle	$V_A = V_D$ = 2.7 V to 5.25 V	MIN			40%		
			MAX			60%		
t_{ACQ}	Acquisition (track) time	$V_A = V_D$ = 2.7 V to 5.25 V		[9, 10, 11]			3	SCLK cycles
	Throughput time	Acquisition time + conversion time $V_A = V_D$ = 2.7 V to 5.25 V		[9, 10, 11]			16	SCLK cycles
t_{AD}	Aperture delay	$V_A = V_D$ = 2.7 V to 5.25 V				4		ns

6.6 Electrical Characteristics: Radiation

The following specifications apply for $V_A = V_D$ = 2.7 V to 5.25 V, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF.[1]

PARAMETER		TEST CONDITIONS	SUBGROUP	MIN	TYP	MAX	UNIT
$I_A + I_D$	Total supply current shutdown mode ($\overline{CS}$ high)	$V_A = V_D$ = 2.7 V to 3.6 V, f_{SCLK} = 0 kSPS	[1]			30	µA
		$V_A = V_D$ = 4.75 V to 5.25 V, f_{SCLK} = 0 kSPS	[1]			100	µA
I_{OZH}, I_{OZL}	Hi-impedance output leakage current	$V_A = V_D$ = 2.7 V to 5.25 V	[1]			±10	µA

(1) Pre and post irradiation limits are identical to those listed in the *DC Parameters* and *AC and Timing Characteristics*, except as listed in *Electrical Characteristics: Radiation*. When performing post irradiation electrical measurements for any RHA level, T_A = 25°C.

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6.7 Electrical Characteristics: Burn in Delta Parameters - T_A at 25°C

The following specifications apply for $V_A = V_D$ = 2.7 V to 5.25 V, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INL	Integral non-linearity	$V_A = V_D$ = 3 V	–0.5	0.106	0.5	LSB
		$V_A = V_D$ = 5 V	–0.35	0.016	0.35	LSB
IMD	Intermodulation distortion, second order terms	$V_A = V_D$ = 3 V	–14	1.35	14	dB
		$V_A = V_D$ = 5 V	–17	1.67	17	dB
IMD	Intermodulation distortion, third order terms	$V_A = V_D$ = 3 V	–10	0.47	10	dB
		$V_A = V_D$ = 5 V	–10	0.9	10	dB

(1) This is worse case drift, Deltas are performed at room temperature post operational life. All other parameters, no deltas are required.

6.8 Timing Requirements

The following specifications apply for $V_A = V_D$ = 2.7 V to 5.25 V, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF.

			SUBGROUP	MIN	NOM(1)	MAX	UNIT
t_{CSH}	$\overline{CS}$ hold time after SCLK rising edge	See (2)	[9, 10, 11]	10	0		ns
t_{CSS}	$\overline{CS}$ setup time prior to SCLK rising edge	See (2)	[9, 10, 11]	10	4.5		ns
t_{EN}	$\overline{CS}$ falling edge to DOUT enabled		[9, 10, 11]		5	30	ns
t_{DACC}	DOUT access time after SCLK falling edge		[9, 10, 11]		17	27	ns
t_{DHLD}	DOUT hold time after SCLK falling edge		[9, 10, 11]	7			ns
t_{DS}	DIN setup time prior to SCLK rising edge		[9, 10, 11]	10			ns
t_{DH}	DIN hold time after SCLK rising edge		[9, 10, 11]	10			ns
t_{CH}	SCLK high time				0.4 × t_{SCLK}		ns
t_{CL}	SCLK low time				0.4 × t_{SCLK}		ns
t_{DIS}	$\overline{CS}$ rising edge to DOUT high-impedance	DOUT falling	[9, 10, 11]		2.4	20	ns
		DOUT rising	[9, 10, 11]		0.9	20	ns

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms.
(2) Clock may be in any state (high or low) when $\overline{CS}$ goes high. Setup and hold time restrictions apply only to $\overline{CS}$ going low.

Table 1. Quality Conformance Inspection(1)

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55
12	Setting time at	25
13	Setting time at	125
14	Setting time at	–55

(1) MIL-STD-883, Method 5005 - Group A

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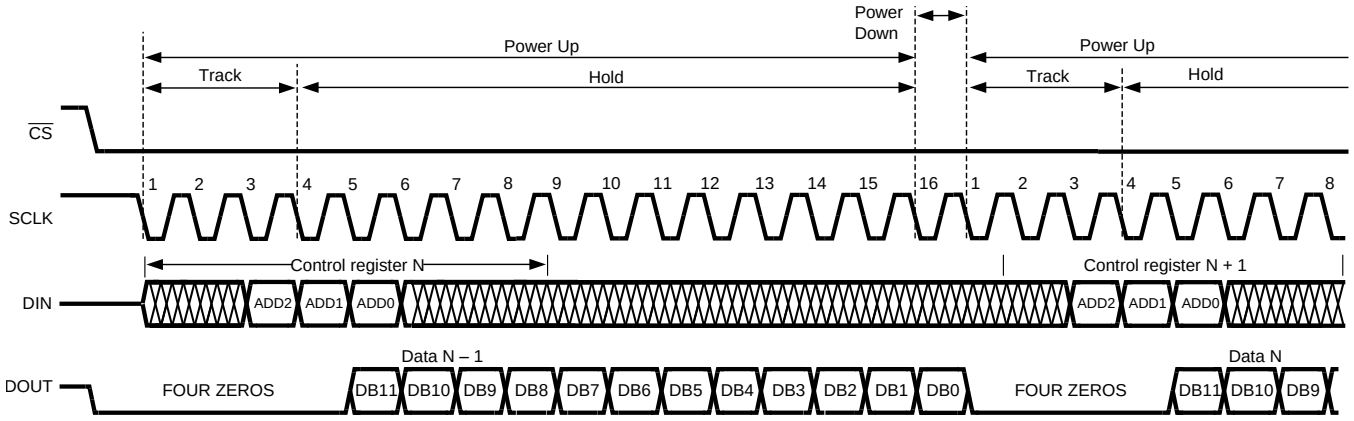


Figure 1. ADC128S102 Operational Timing Diagram

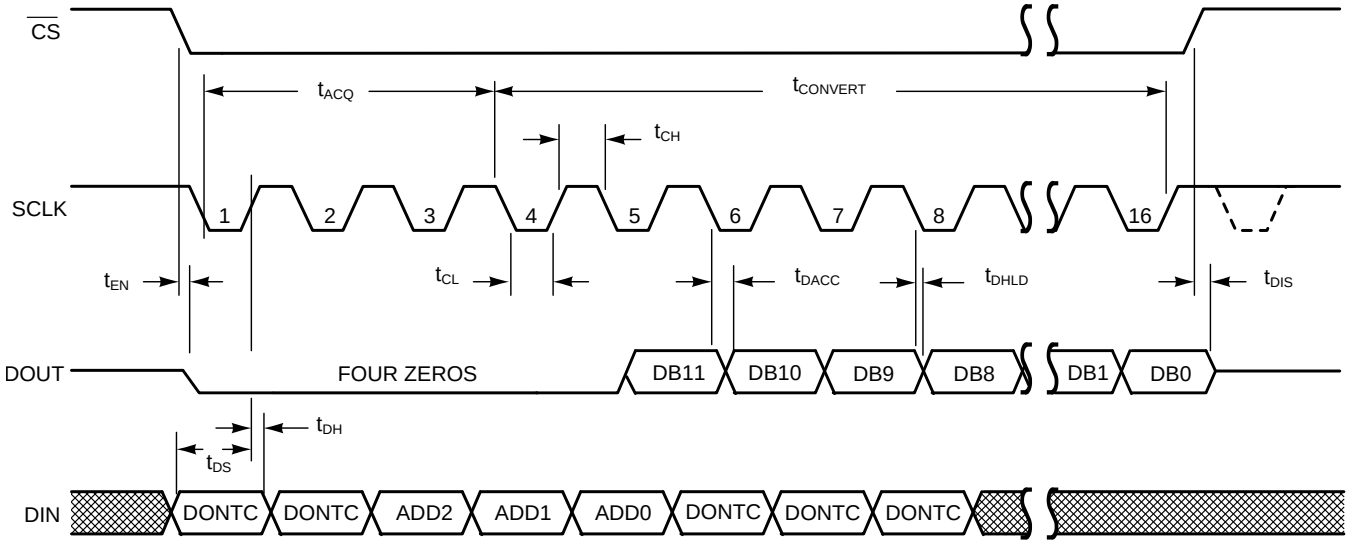


Figure 2. ADC128S102 Serial Timing Diagram

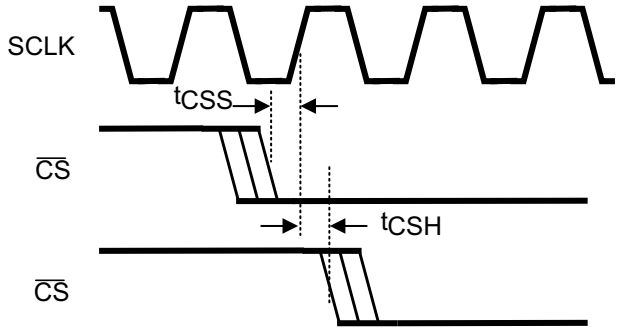


Figure 3. SCLK and $\overline{CS}$ Timing Parameters

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6.9 Typical Characteristics

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

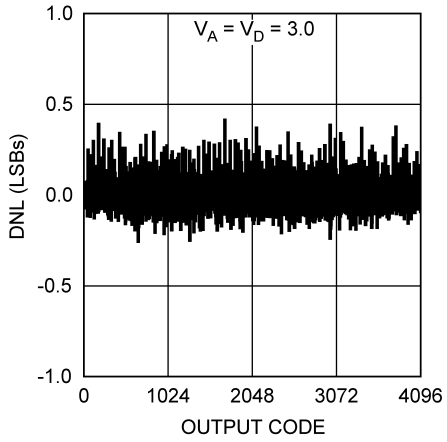


Figure 4. DNL

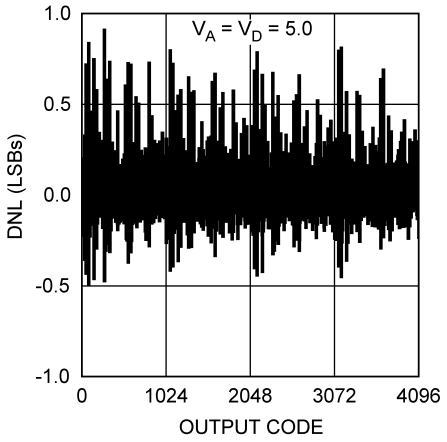


Figure 5. DNL

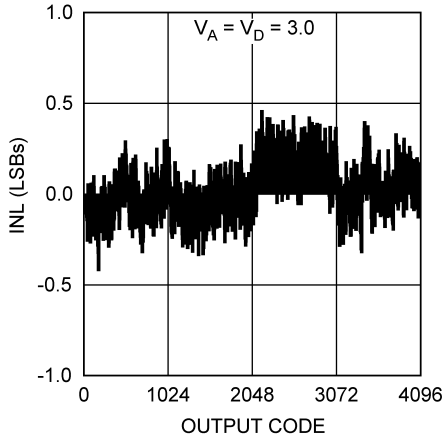


Figure 6. INL

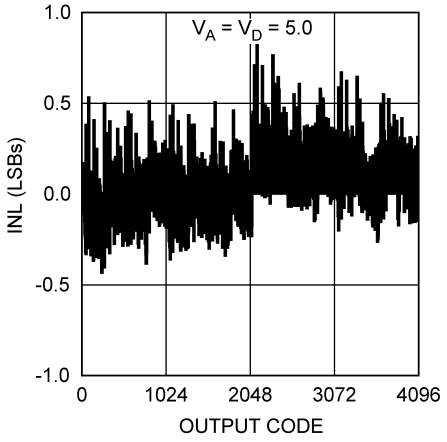


Figure 7. INL

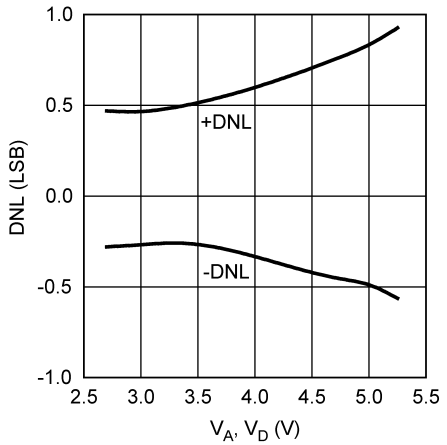


Figure 8. DNL vs Supply

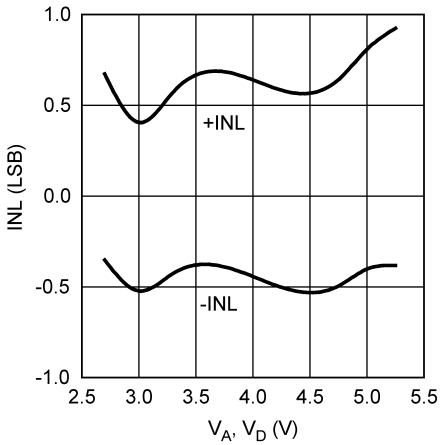


Figure 9. INL vs Supply

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Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

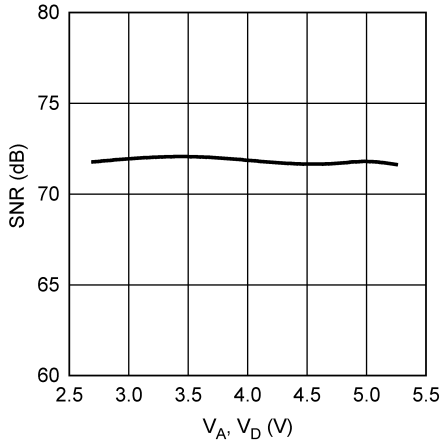


Figure 10. SNR vs Supply

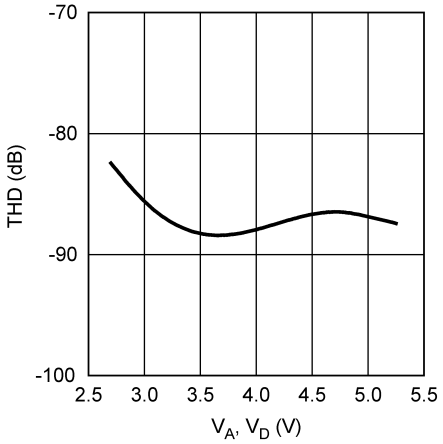


Figure 11. THD vs Supply

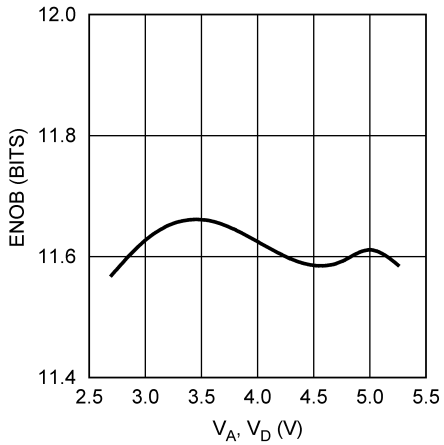


Figure 12. ENOB vs Supply

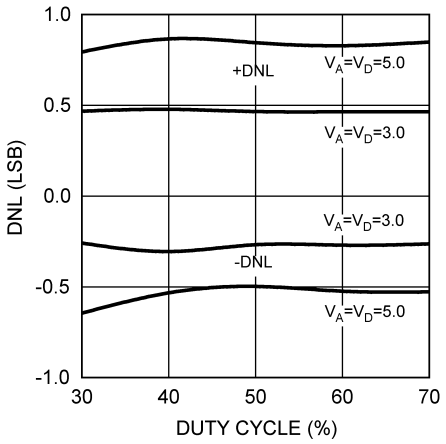


Figure 13. DNL vs SCLK Duty Cycle

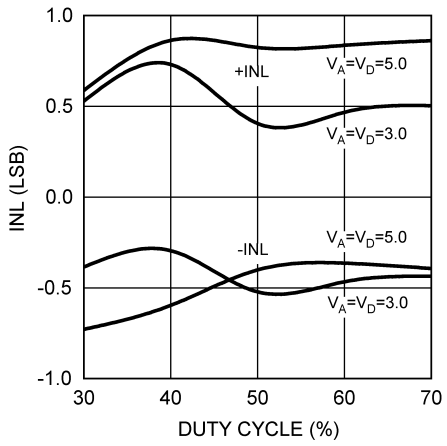


Figure 14. INL vs SCLK Duty Cycle

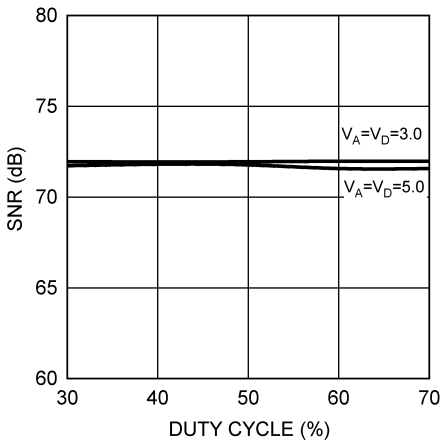


Figure 15. SNR vs SCLK Duty Cycle

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Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

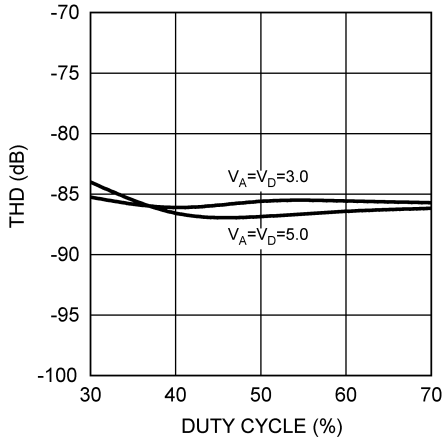


Figure 16. THD vs SCLK Duty Cycle

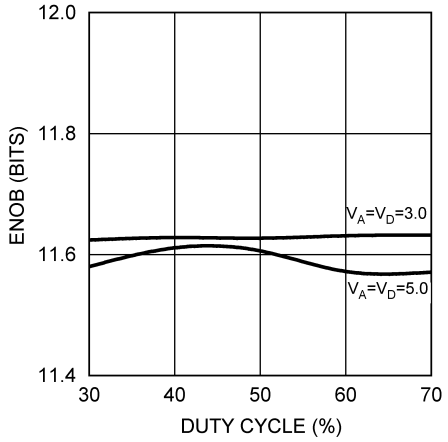


Figure 17. ENOB vs SCLK Duty Cycle

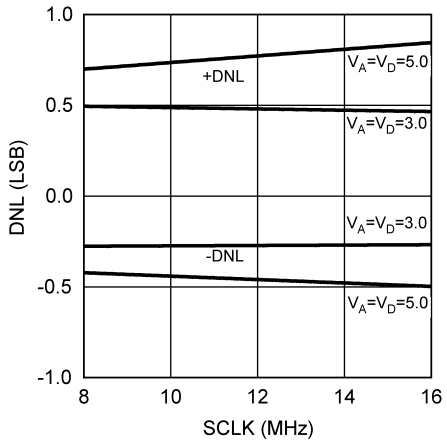


Figure 18. DNL vs SCLK

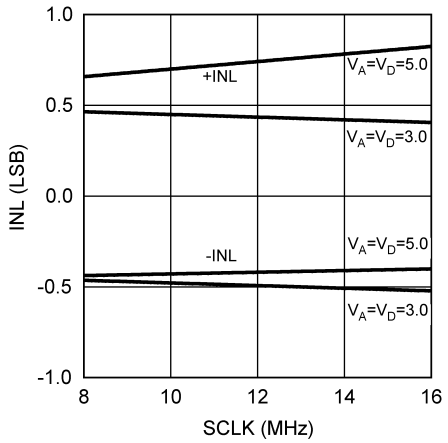


Figure 19. INL vs SCLK

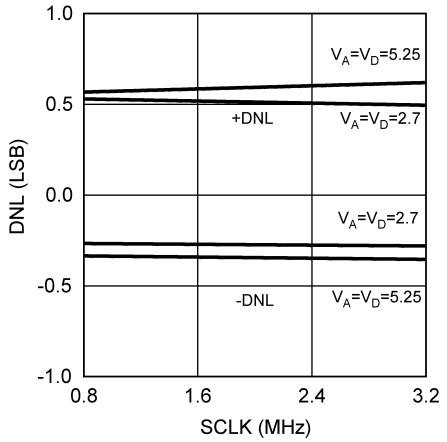


Figure 20. DNL vs SCLK

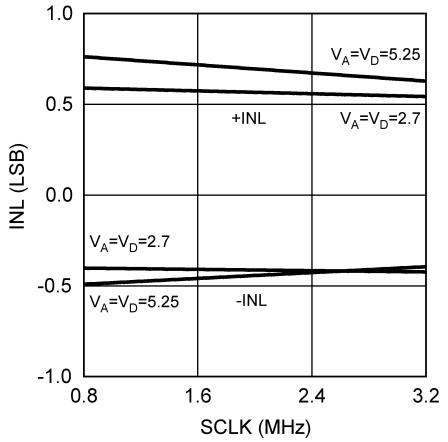


Figure 21. INL vs SCLK

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Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

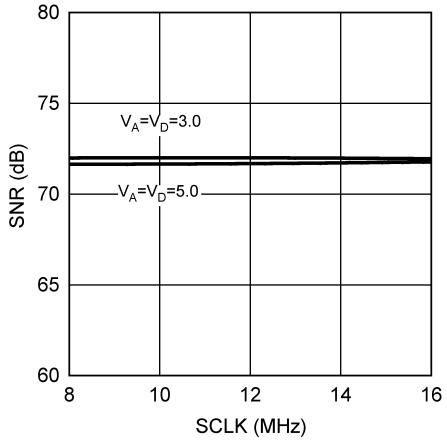


Figure 22. SNR vs SCLK

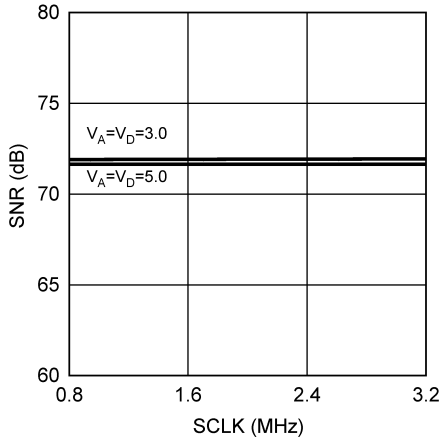


Figure 23. SNR vs SCLK

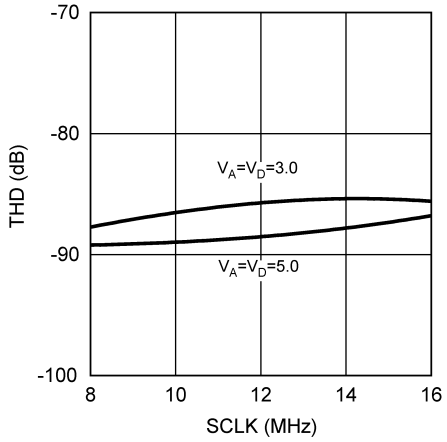


Figure 24. THD vs SCLK

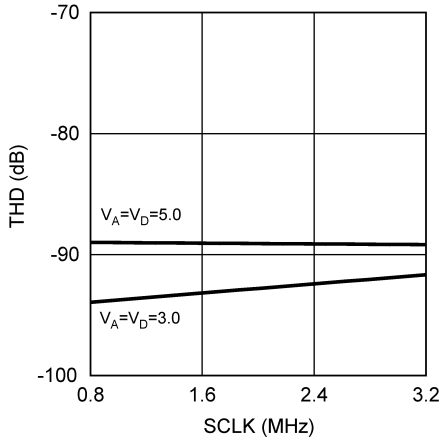


Figure 25. THD vs SCLK

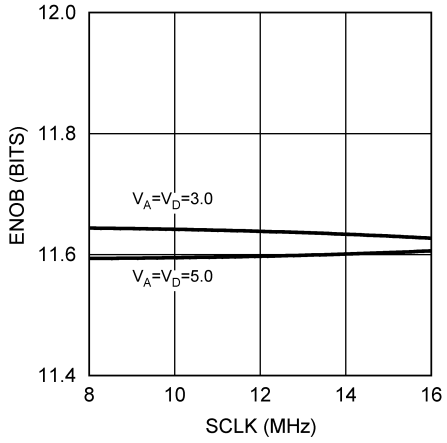


Figure 26. ENOB vs SCLK

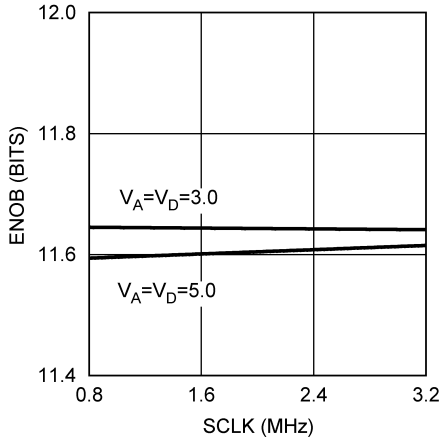


Figure 27. ENOB vs SCLK

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Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

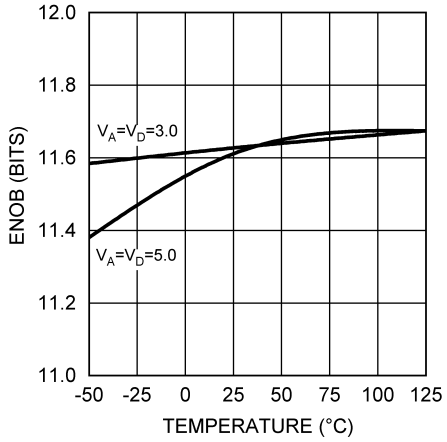


Figure 28. ENOB vs Temperature

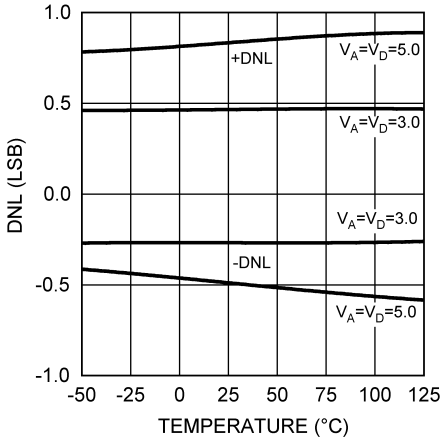


Figure 29. DNL vs Temperature

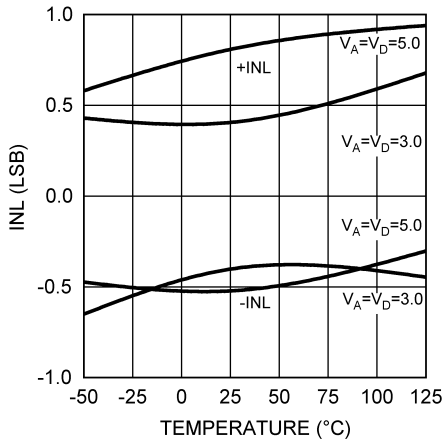


Figure 30. INL vs Temperature

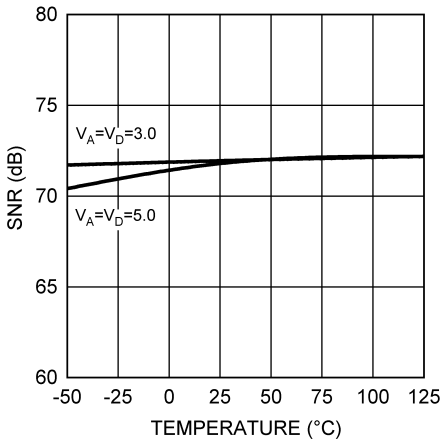


Figure 31. SNR vs Temperature

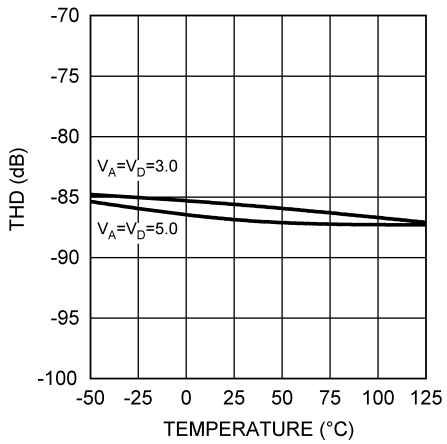


Figure 32. THD vs Temperature

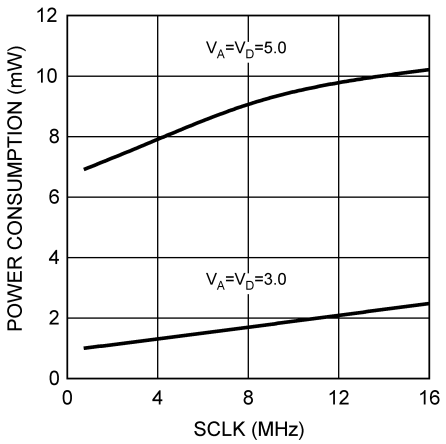


Figure 33. Power Consumption vs SCLK

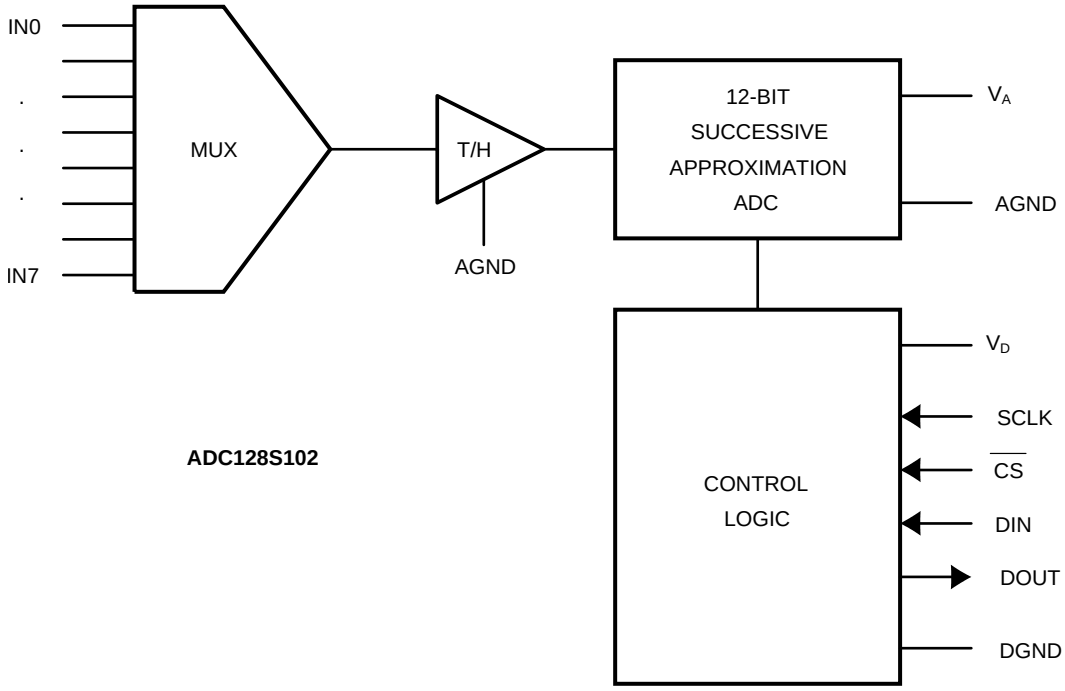
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7 Detailed Description

7.1 Overview

The ADC128S102 is a successive-approximation analog-to-digital converter designed around a charge redistribution digital-to-analog converter.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ADC128S102 Transfer Function

The output format of the ADC128S102 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC128S102 is V_A / 4096. The ideal transfer characteristic is shown in Figure 34. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of V_A / 8192. Other code transitions occur at steps of one LSB.

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Feature Description (continued)

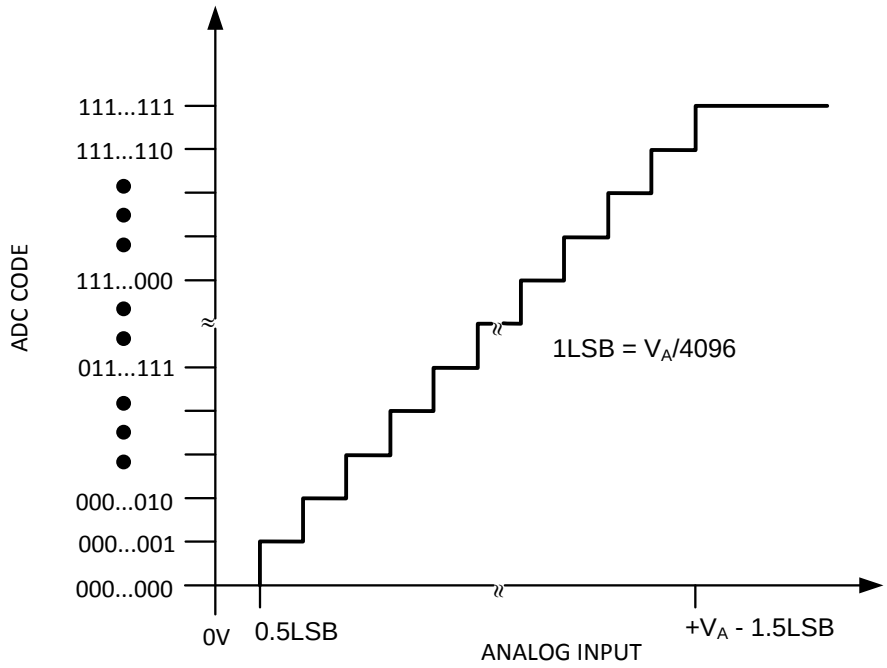


Figure 34. Ideal Transfer Characteristic

7.3.2 Analog Inputs

An equivalent circuit for one of the input channels of the ADC128S102 is shown in Figure 35. Diodes D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0 V to V_A. Going beyond this range will cause the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in Figure 35 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the ON-resistance of the multiplexer and track or hold switch and is typically 500 Ω. Capacitor C2 is the ADC128S102 sampling capacitor, and is typically 30 pF. The ADC128S102 will deliver best performance when driven by a low-impedance source (less than 100 Ω). This is especially important when using the ADC128S102 to sample dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonics and noise in the input. These filters are often referred to as anti-aliasing filters.

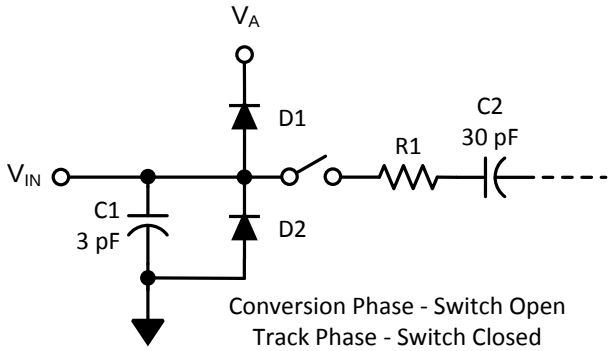


Figure 35. Equivalent Input Circuit

7.3.3 Digital Inputs and Outputs

The digital inputs of the ADC128S102 (SCLK, $\overline{CS}$, and DIN) have an operating range of 0 V to V_A. The inputs are not prone to latch-up and may be asserted before the digital supply (V_D) without any risk. The digital output (DOUT) operating range is controlled by V_D. The output high voltage is V_D – 0.5 V (minimum) while the output low voltage is 0.4 V (maximum).

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Feature Description (continued)

7.3.4 Radiation Environments

Careful consideration should be given to environmental conditions when using a product in a radiation environment.

7.3.4.1 Total Ionizing Dose

Radiation hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level listed in the *Device Information* table in the *Description* section. Testing and qualification of these products is done on a wafer level according to *MIL-STD-883G, Test Method 1019.7*. Testing is done according to Condition A and the Extended room temperature anneal test described in section 3.11 for application environment dose rates less than 0.027 rad(Si)/s. Wafer level TID data is available with lot shipments.

7.3.4.2 Single Event Latch-Up and Functional Interrupt

One-time single event latch-up (SEL) and single event functional interrupt (SEFI) testing was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LETth) shown in *Features* is the maximum LET tested. A test report is available upon request.

7.3.4.3 Single Event Upset

A report on single event upset (SEU) is available upon request.

7.4 Device Functional Modes

7.4.1 ADC128S102 Operation

Simplified schematics of the ADC128S102 in both track and hold operation are shown in Figure 36 and Figure 37 respectively. In Figure 36, the ADC128S102 is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC128S102 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

Figure 37 shows the ADC128S102 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC128S102 is in this state for the last thirteen SCLK cycles after $\overline{CS}$ is brought low.

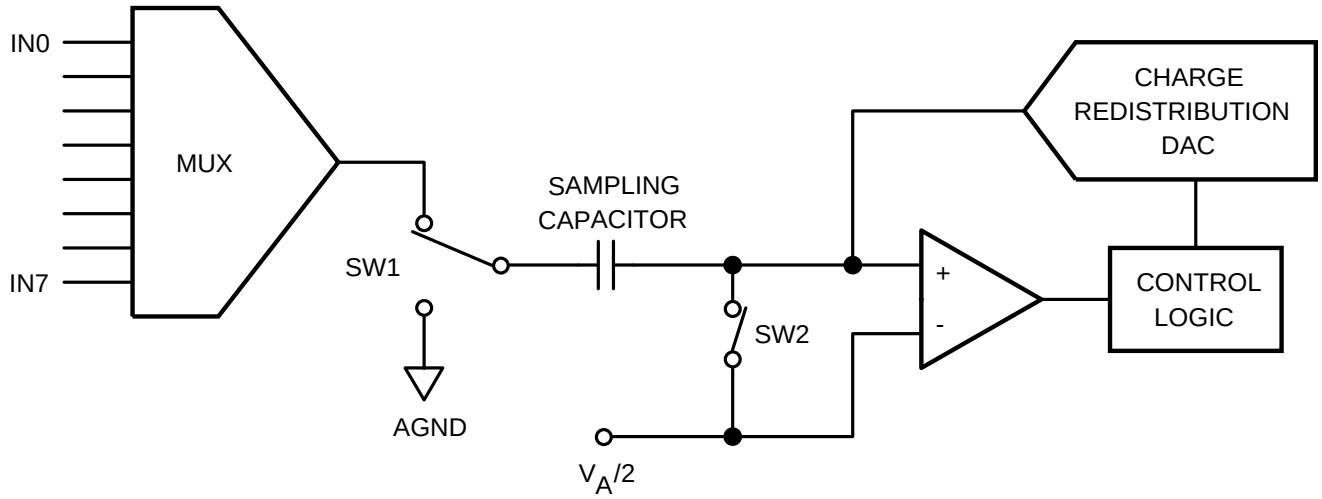


Figure 36. ADC128S102 in Track Mode

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Device Functional Modes (continued)

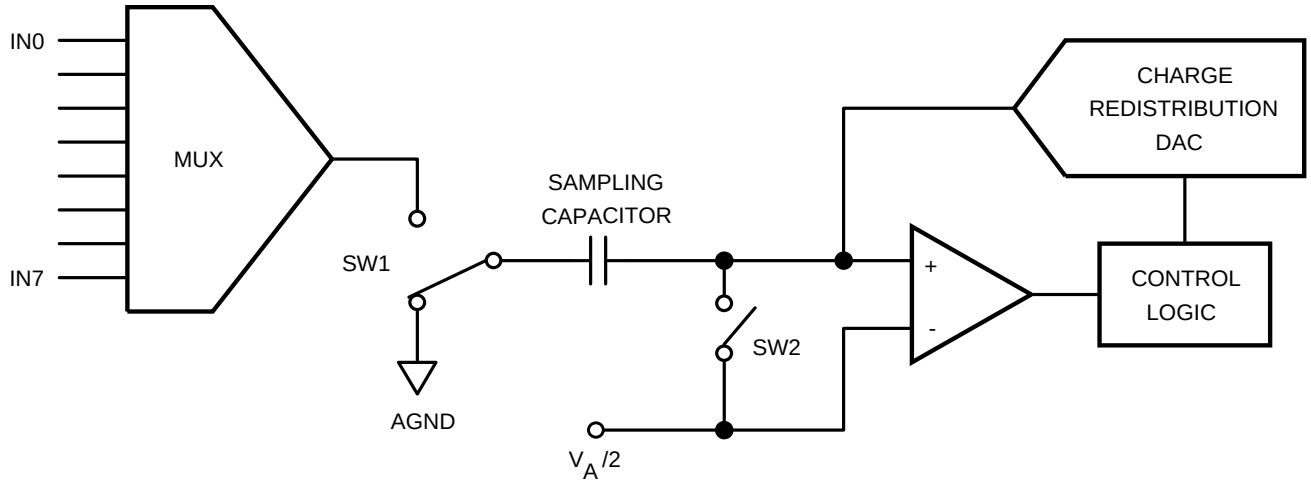


Figure 37. ADC128S102 in Hold Mode

7.5 Programming

7.5.1 Serial Interface

An operational timing diagram and a serial interface timing diagram for the ADC128S102 are shown in Figure 1 to Figure 3. $\overline{CS}$, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC128S102's Control Register is placed on DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC's DOUT pin is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. Note that $\overline{CS}$ is asynchronous. Thus, $\overline{CS}$ acts as an output enable. Similarly, SCLK is internally gated off when $\overline{CS}$ is brought high.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out. SCLK falling edges 1 through 4 clock out leading zeros while falling edges 5 through 16 clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the hold/convert mode on the N×16+4th falling edge of SCLK. "N" is an integer value.

The ADC128S102 enters track mode under three different conditions. In Figure 1, $\overline{CS}$ goes low with SCLK high and the ADC enters track mode on the first falling edge of SCLK. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC automatically enters track mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC enters track mode. While there is no timing restriction with respect to the falling edges of $\overline{CS}$ and SCLK, see Figure 3 for setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK.

During each conversion, data is clocked into a control register through the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. The control register is loaded with data indicating the input channel to be converted on the subsequent conversion (see Table 2, Table 3, and Table 4).

Although the ADC128S102 is able to acquire the input signal to full resolution in the first conversion immediately following power-up, the first conversion result after power-up will be that of a randomly selected channel. Therefore, the user needs to incorporate a dummy conversion to set the required channel that will be used on the subsequent conversion.

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Programming (continued)

Table 2. Control Register Bits

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DONTC	**DONTC**	**ADD2**	**ADD1**	**ADD0**	**DONTC**	**DONTC**	**DONTC**

Table 3. Control Register Bit Descriptions

BIT	SYMBOL	DESCRIPTION
7, 6, 2, 1, 0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel will be sampled and converted at the next conversion cycle. The mapping between codes and channels is shown in Table 4.
4	ADD1	
3	ADD0	

Table 4. Input Channel Selection

ADD2	ADD1	ADD0	INPUT CHANNEL
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ADC128S102 device is a low-power, eight-channel 12-bit ADC with ensured performance specifications from 50 kSPS to 1 MSPS. It is appropriate to utilize the ADC128S102 at sample rates below 50 kSPS by powering the device down (de-asserting CSB) in between conversions. The Electrical Characteristics information highlights the clock frequency where the ADC's performance is ensured. There is no limitation on periods of time for shutdown between conversions.

8.2 Typical Application

A typical application is shown in Figure 38. The split analog and digital supply pins are both powered in this example by the Texas Instruments LP2950-N low-dropout voltage regulator. The analog supply is bypassed with a capacitor network located close to the ADC128S102. The digital supply is separated from the analog supply by an isolation resistor and bypassed with additional capacitors. The ADC128S102 uses the analog supply (V_A) as its reference voltage, so it is very important that V_A be kept as clean as possible. Due to the low power requirements of the ADC128S102, it is also possible to use a precision reference as a power supply.

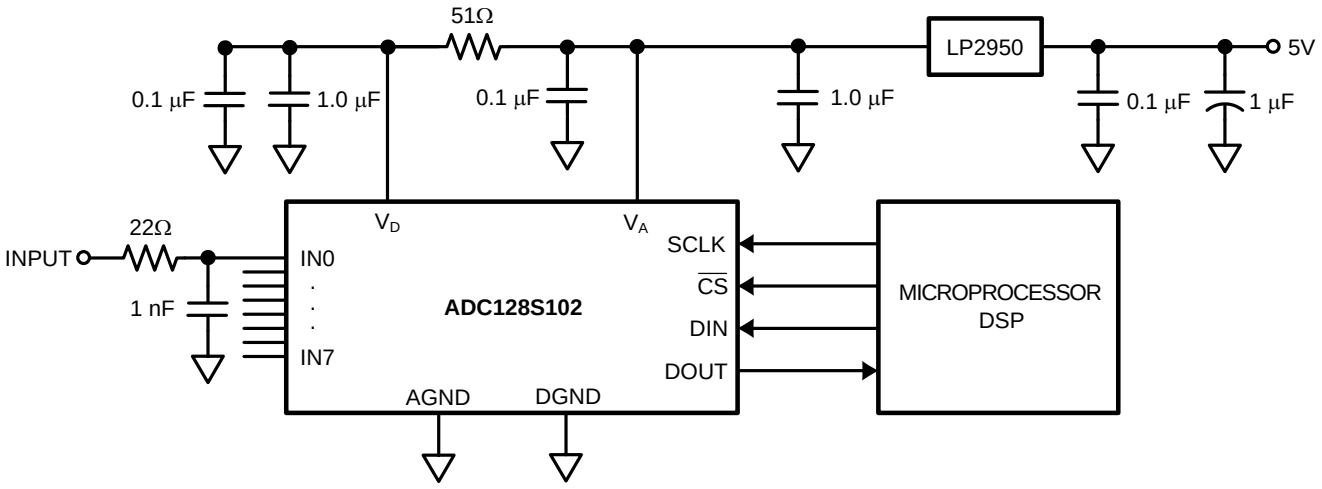


Figure 38. Typical Application Circuit

8.2.1 Design Requirements

A positive supply only data acquisition system capable of digitizing up to eight single-ended input signals ranging from 0 to 5 V with BW = 10 kHz and a throughput up to 500 kSPS. The ADC128S102 has to interface to an MCU whose supply is set at 5 V. If it is necessary to interface with an MCU that operates at 3.3 V or lower, VA and VD will need to be separated and care must be taken to ensure that VA is powered before VD.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

The signal range requirement forces the design to use 5-V analog supply at VA, analog supply. This follows from the fact that VA is also a reference potential for the ADC. If the requirement of interfacing to the MCU changes to 3.3-V, it will be necessary to change the VD supply voltage to 3.3 V. The maximum sampling rate of the ADC128S102 when all channels (eight) are enabled is, Fs = F_{SCLK} / (16 × 8).

Note that faster sampling rates can be achieved when fewer channels are sampled. Single channel can be sampled at the maximum rate of Fs (single) = F_{SCLK} / 16.

The VA and VD pins are separated by a 51-Ω resistor in order to minimize digital noise from corrupting the analog reference input. If additional filtering is required, the resistor can be replaced by a ferrite bead, thus achieving a 2nd-order filter response. Further noise consideration could be given to the SPI interface, especially when the master MCU is capable of producing fast rising edges on the digital bus signals. Inserting small resistances in the digital signal path may help in reducing the ground bounce, and thus improve the overall noise performance of the system. Care should be taken when the signal source is capable of producing voltages beyond VA. In such instances, the internal ESD diodes may start conducting. The ESD diodes are not intended as input signal clamps. To provide the desired clamping action use Schottky diodes.

8.2.3 Application Curve

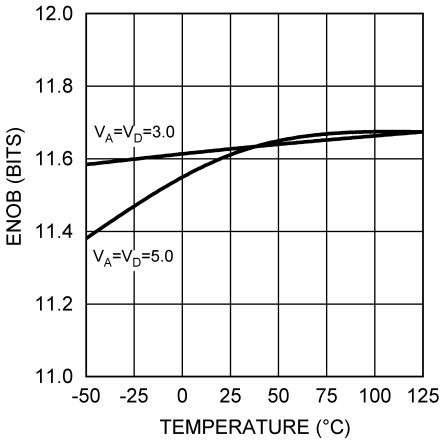


Figure 39. ENOB vs Temperature

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9 Power Supply Recommendations

There are three major power supply concerns with this product: power supply sequencing, power management, and the effect of digital supply noise on the analog supply.

9.1 Power Supply Sequence

The ADC128S102 is a dual-supply device. The two supply pins share ESD resources, so care must be exercised to ensure that the power is applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply (V_D) cannot exceed the analog supply (V_A) by more than 300 mV, during a conversion cycle. Therefore, V_A must ramp up before or concurrently with V_D.

9.2 Power Management

The ADC128S102 is fully powered-up whenever $\overline{CS}$ is low and fully powered-down whenever $\overline{CS}$ is high, with one exception. If operating in continuous conversion mode, the ADC128S102 automatically enters power-down mode between SCLK's 16th falling edge of a conversion and SCLK's 1st falling edge of the subsequent conversion (see Figure 1).

In continuous conversion mode, the ADC128S102 can perform multiple conversions back to back. Each conversion requires 16 SCLK cycles and the ADC128S102 will perform conversions continuously as long as $\overline{CS}$ is held low. Continuous mode offers maximum throughput.

In burst mode, the user may trade off throughput for power consumption by performing fewer conversions per unit time. This means spending more time in power-down mode and less time in normal mode. By utilizing this technique, the user can achieve very low sample rates while still utilizing an SCLK frequency within the electrical specifications. The Power Consumption versus SCLK curve in the *Typical Characteristics* shows the typical power consumption of the ADC128S102. To calculate the power consumption (P_C), simply multiply the fraction of time spent in the normal mode (t_N) by the normal mode power consumption (P_N), and add the fraction of time spent in shutdown mode (t_S) multiplied by the shutdown mode power consumption (P_S) as shown in Equation 1.

$$P_C = \frac{t_N}{t_N + t_S} \times P_N + \frac{t_S}{t_N + t_S} \times P_S \quad (1)$$

9.3 Power Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply, V_D. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the digital supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply will be coupled directly into the analog supply, causing greater performance degradation than would noise on the digital supply alone. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution to keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100-Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance. Because the series resistor and the load capacitance form a low frequency pole, verify signal integrity once the series resistor has been added.

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10 Layout

10.1 Layout Guidelines

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC128S102 due to supply noise, do not use the same supply for the ADC128S102 that is used for digital logic.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (for example, a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

We recommend the use of a single, uniform ground plane and the use of split power planes. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, and so forth) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single, quiet point.

10.2 Layout Example

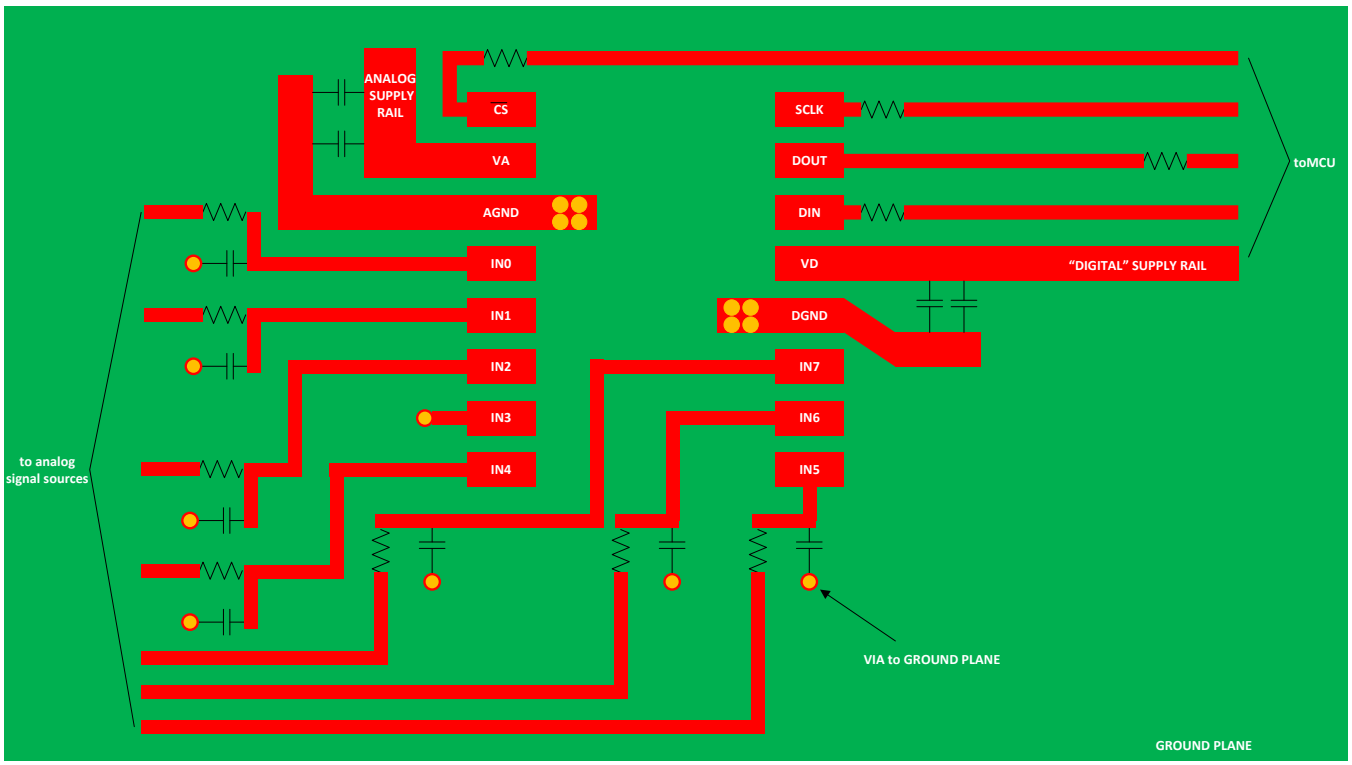


Figure 40. Layout Diagram

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For related documentation, see the following:

- 5962R07727
- *Radiation Report*
- *MIL-STD-883G, Test Method 1019.7*

11.1.2 Device Nomenclature

11.1.2.1 Specification Definitions

ACQUISITION TIME is the time required for the ADC to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage.

APERTURE DELAY is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion.

CHANNEL-TO-CHANNEL ISOLATION is resistance to coupling of energy from one channel into another channel.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

CROSSTALK is the coupling of energy from one channel into another channel. This is similar to Channel-to-Channel Isolation, except for the sign of the data.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} - 1.5 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to an individual ADC input at the same time. It is defined as the ratio of the power in either the second or the third order intermodulation products to the sum of the power in both of the original frequencies. Second order products are $f_a \pm f_b$, where f_a and f_b are the two sine wave input frequencies. Third order products are ($2f_a \pm f_b$) and ($f_a \pm 2f_b$). IMD is usually expressed in dB.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC128S102 is verified not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (that is, GND + 0.5 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not

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Device Support (continued)

including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

THROUGHPUT TIME is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion time.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as:

$$THD = 20 \bullet \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f10}^2}{A_{f1}^2}} \quad (2)$$

where

- A_{f1} is the RMS power of the input frequency at the output
- A_{f2} through A_{f10} are the RMS power in the first 9 harmonic frequencies

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Engineering Samples

Engineering samples are available for order and are identified by the "MPR" in the orderable device name (see Packaging Information in the Addendum). Engineering (MPR) samples meet the performance specifications of the datasheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that would not impact the performance at room temperature, such as radiation or reliability testing.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R0722701V9A	Active	Production	DIESALE (Y) | 0	20 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
5962R0722701VFA	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	ADC128S102 WRQMLV Q 5962R07227 01VFA ACO 01VFA >T
5962R0722701VZA	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	ADC128S102 WGRQMLV Q 5962R07227 01VZA ACO 01VZA >T
ADC128S102 MDR	Active	Production	DIESALE (Y) | 0	20 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
ADC128S102-MDR.A	Active	Production	DIESALE (Y) | 0	20 | OTHER	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	
ADC128S102WGMPR	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	25 to 25	ADC128S102 WGMPR ES ACO WGMPR ES >T
ADC128S102WGMPR.A	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	25 to 25	ADC128S102 WGMPR ES ACO WGMPR ES >T
ADC128S102WGRQV	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	ADC128S102 WGRQMLV Q 5962R07227 01VZA ACO 01VZA >T
ADC128S102WGRQV.A	Active	Production	CFP (NAC) | 16	88 | JEDEC TRAY (5+1)	No	SNPB	Level-1-NA-UNLIM	-55 to 125	ADC128S102 WGRQMLV Q 5962R07227 01VZA ACO 01VZA >T
ADC128S102WRQV	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	ADC128S102 WRQMLV Q 5962R07227 01VFA ACO 01VFA >T

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC128S102WRQV.A	Active	Production	CFP (NAD) | 16	19 | TUBE	No	SNPB	Level-1-NA-UNLIM	-55 to 125	ADC128S102 WRQMLV Q 5962R07227 01VFA ACO 01VFA >T

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

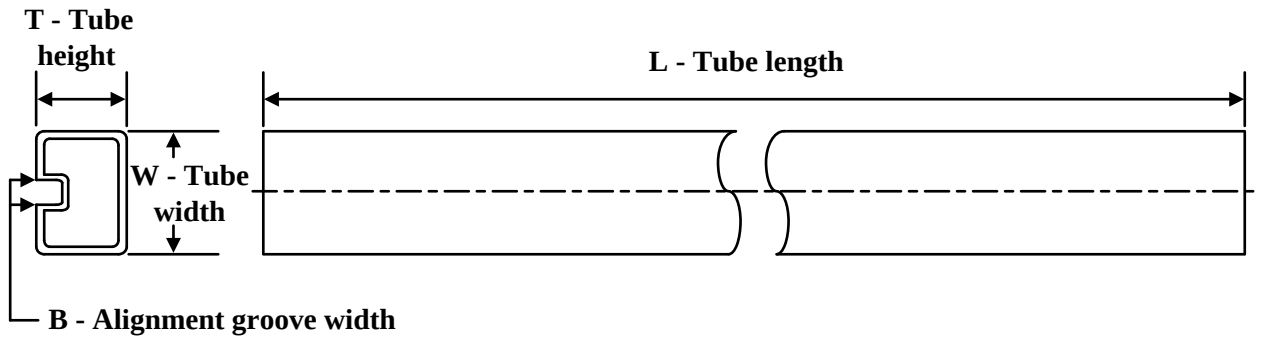
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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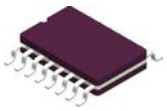
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R0722701VFA	NAD	CFP	16	19	502	23	9398	9.78
ADC128S102WRQV	NAD	CFP	16	19	502	23	9398	9.78
ADC128S102WRQV.A	NAD	CFP	16	19	502	23	9398	9.78

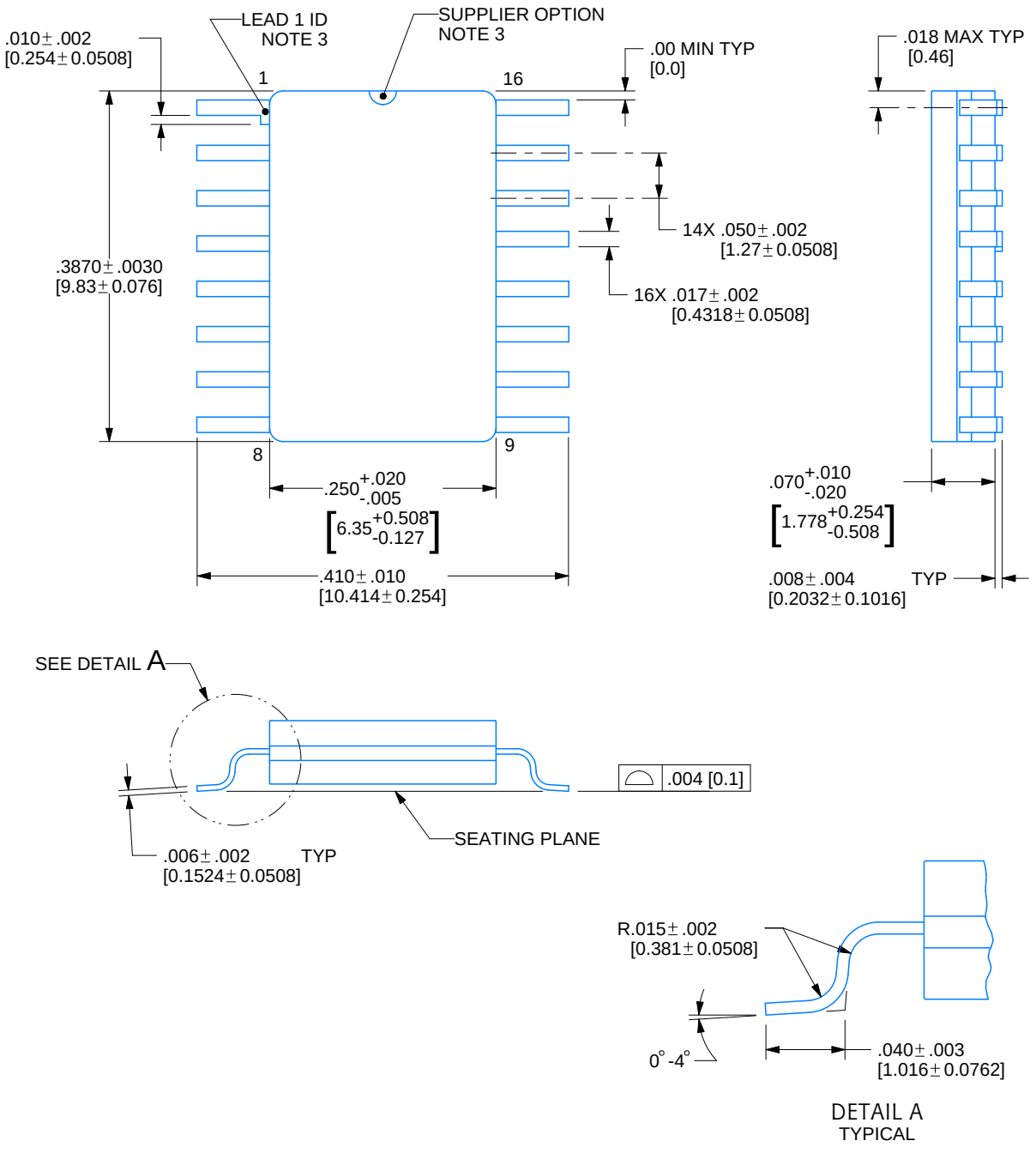


PACKAGE OUTLINE

NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



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NOTES:

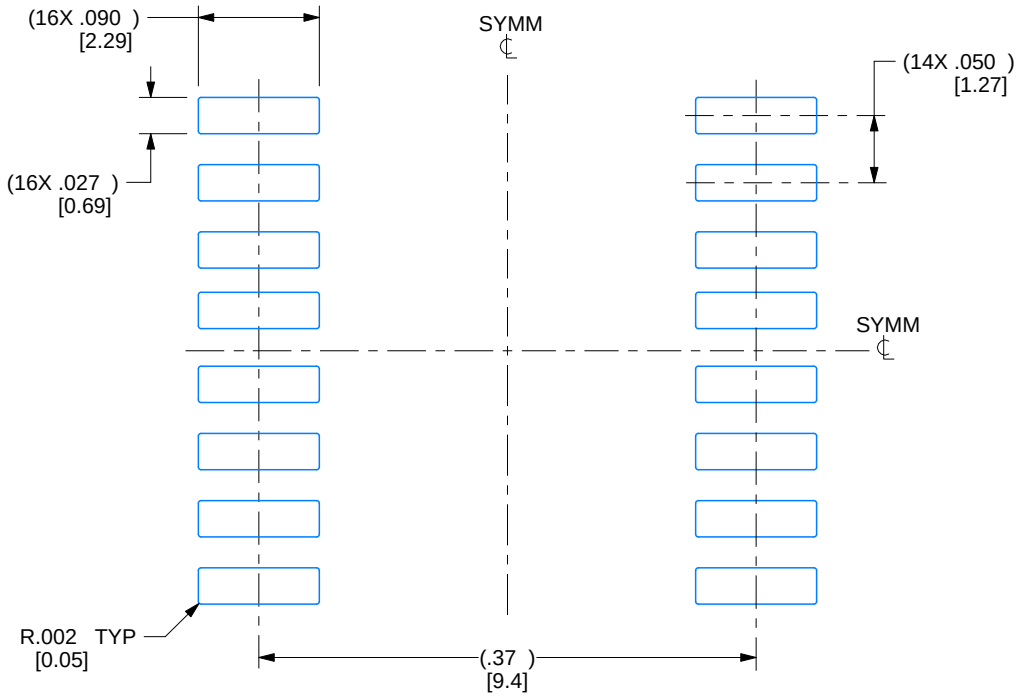
1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

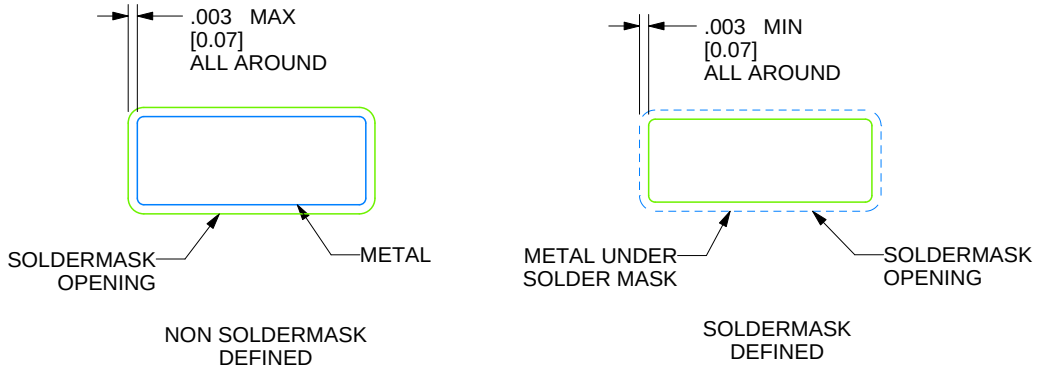
NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



RECOMMENDED LAND PATTERN

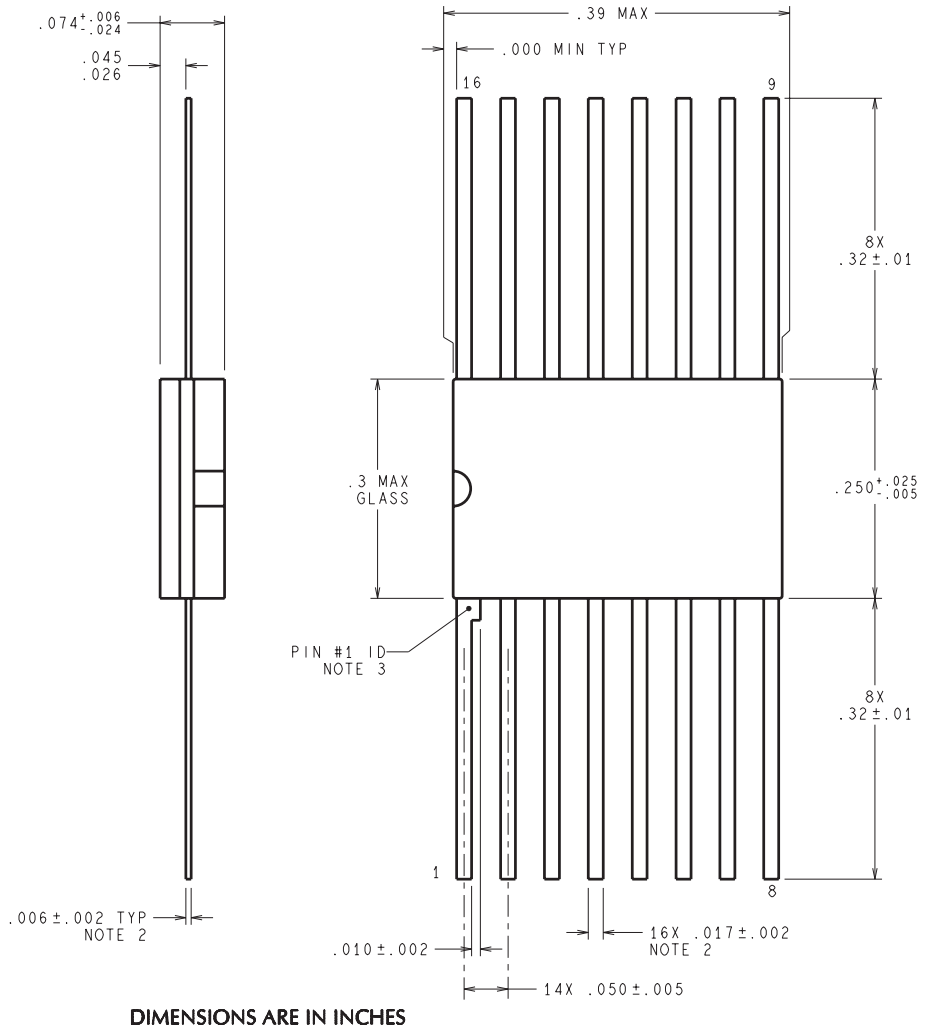


4215198/C 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197879	12/30/2021	TINA TRAN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198832	02/15/2022	K. SINCERBOX
C	.387± .003 WAS .39000± .00012;	2200917	08/08/2022	D. CHIN / K. SINCERBOX

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