LMK3H2104 and LMK3H2108 4- and 8-Output PCIe Gen 1-7 Compliant Low Jitter General Purpose BAW Clock Generator

1 Features

- Integrated BAW resonator
  - No need for external XTAL/XO
- Flexible output frequency
  - 2 fraction output dividers (FOD), individual channel dividers
  - Up to 400MHz output frequency
- Flexible output format
  - 1.2/1.8/2.5/3.3V LVCMOS
  - DC- or AC-coupled LVDS
  - LP-HCSL with programmable swing. LVPECL, CML and other formats can be derived from LP-HCSL
- Very low jitter
  - 61fs max PCIe Gen 5 CC with SSC jitter
  - 36.4fs max PCIe Gen 6 CC with SSC jitter
  - 25.5fs max PCIe Gen 7 CC with SSC jitter
- PCIe Gen 1 to Gen 7 compliant
- Configurable SSC
  - Programmable -0.05% to -3% down spread and ±0.025% to ±1.5% center spread, or preset -0.1%, -0.25%, -0.3% and -0.5% down spread
- 3 inputs (LMK3H2108) or 1 input (LMK3H2104) that can be bypassed to any output
- 5ms max startup time
- Fail-safe input pins can be pulled high when device power is off
- Flexible power supply
  - Each VDD pin can be independently connected to = 1.8, 2.5 or 3.3V
  - Each VDDO pin can be independently connected set to 1.8, 2.5 or 3.3V
- -40 to 105°C ambient temperature

2 Applications

- High Performance Computing Server Motherboard
- NIC, SmartNIC and Hardware Acceleration
- PCIe Gen 1 to Gen 7 clock generation
- General purpose clock generation and XO/XTAL replacement

3 Description

LMK3H2104 and LMK3H2108 are BAW-based clock generators that do not require any external XTAL or XO. The devices can be used as PCIe clock generators or general purpose clock generators. The 2 FODs (Fractional Output Divider) provide frequency flexibility, low power and low jitter at the same time.

LMK3H2104 has up to 4 differential outputs plus 2 LVCMOS outputs or up to 10 LVCMOS outputs. LMK3H2108 has up to 8 differential outputs or 16 LVCMOS outputs.

LMK3H2104 has one clock input and LMK3H2108 has three clock inputs. The clock inputs provide clock multiplexing and buffering ability. Each output bank can independently select any clock source.

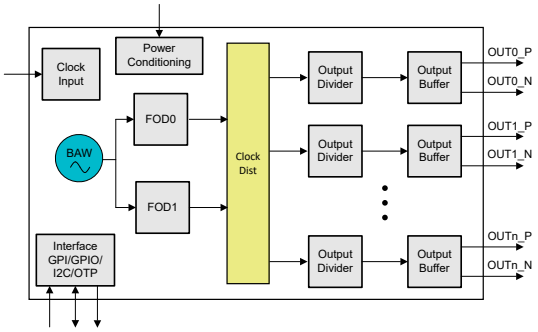
The GPI and GPIO pins provide additional control flexibility. These pins can be configured as individual OE, grouped OE, I2C address selection, OTP page selection, PWRGD/PWRDN#, status output and other functions.

The device supports one-time programmable (OTP) non-volatile memory which can be customized and factory preprogrammed.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMK3H2104	RGE0024AA (QFN, 24)	4.0mm × 4.0mm
LMK3H2104	RGE0024AB (QFN, 24)	4.0mm × 4.0mm
LMK3H2108	RKP0040A (QFN, 40)	5.0mm × 5.0mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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4 Pin Configuration and Functions

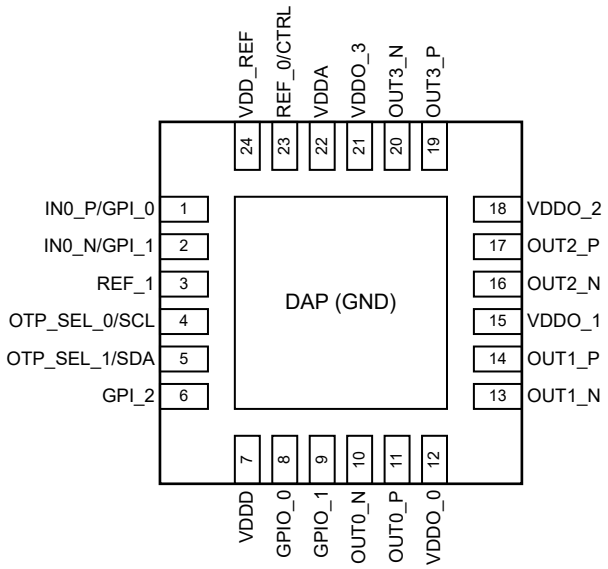


Figure 4-1. LMK3H2104 RGE Package 24-Pin QFN Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IN0_P/GPI_0	1	I	Differential clock input or general purpose inputs. These are fail-safe input pins. Leave floating if unused.
IN0_N/GPI_1	2	I	
REF_1	3	O	1.8, 2.5 or 3.3V LVCMOS clock output. This output can be disabled to low or tristate. Leave floating if unused.
OTP_SEL_0/SCL	4	I	Multifunctional pins. Functionality is determined by Pin 23 at power-up. Internal pull-down resistor on both pins by default. SCL is fail-safe. • OTP mode: OTP_SEL_[1:0] select 1 out of 4 OTP pages • I2C mode: SCL, SDA
OTP_SEL_1/SDA	5	I/O	
GPI_2	6	I	General purpose input. Fail-safe pin. Leave floating if unused
VDDD	7	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
GPIO_0	8	I/O	General purpose input or output. Leave floating if unused.
GPIO_1	9	I/O	General purpose input or output. Leave floating or connect to VDD if unused. GPIO_1 must not be configured as an output if connected to VDD.
OUT0_N	10	O	Differential clock output 0. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT0_P	11	O	
VDDO_0	12	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
OUT1_N	13	O	Differential clock output 1. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT1_P	14	O	
VDDO_1	15	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
OUT2_N	16	O	Differential clock output 2. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT2_P	17	O	
VDDO_2	18	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
OUT3_P	19	O	Differential clock output 3. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT3_N	20	O	
VDDO_3	21	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
VDDA	22	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping

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Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
REF_0/CTRL	23	I/O	Multifunctional pin. At power-up, the state of this pin is latched to decide Pin 4 and Pin 5 functions. No internal pull-up or pull-down resistor is available. This pin must be pulled high or low externally. • Low at power-up: I2C mode. Pin 4, 5 = SCL, SDA • High at power-up: OTP mode. Pin 4, 5 = OTP_SEL_0, OTP_SEL_1 After power-up, this pin can output a 1.8, 2.5, 3.3V LVCMOS clock, or be disabled to low or tristate.
VDD_REF	24	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
DAP	25	G	Connect to ground

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

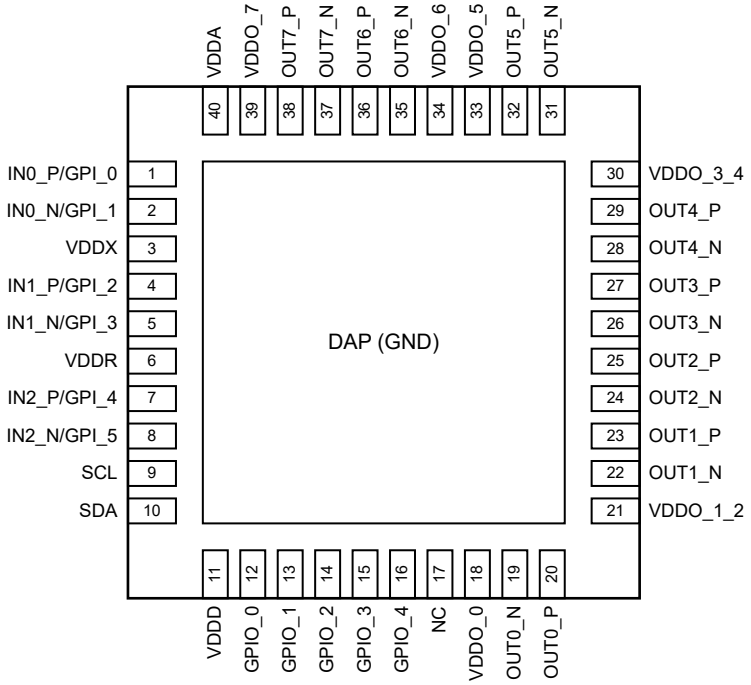


Figure 4-2. LMK3H2108 RKP Package 40-Pin QFN Top View

Table 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN0_P/GPI_0	1	I	Differential clock input or general purpose inputs. These are fail-safe input pins. Leave floating if unused.
IN0_N/GPI_1	2	I	
VDDX	3	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
IN1_P/GPI_2	4	I	Differential clock input or general purpose inputs. These are fail-safe input pins. Leave floating if unused.
IN1_N/GPI_3	5	I	
VDDR	6	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
IN2_P/GPI_4	7	I	Differential clock input or general purpose inputs. These are fail-safe input pins. Leave floating if unused.
IN2_N/GPI_5	8	I	
SCL	9	I	I2C clock
SDA	10	I/O	I2C data
VDDD	11	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping

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Table 4-2. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GPIO_0	12	I/O	General purpose input or output. Leave floating if unused.
GPIO_1	13	I/O	General purpose input or output. Leave floating if unused.
GPIO_2	14	I/O	General purpose input or output. Leave floating if unused.
GPIO_3	15	I/O	General purpose input or output. Leave floating if unused.
GPIO_4	16	I/O	General purpose input or output. Leave floating if unused.
NC	17	N/A	No connect. Leave floating or tie to GND
VDDO_0	18	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
OUT0_N	19	O	Differential clock output 0. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT0_P	20	O	
VDDO_1_2	21	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
OUT1_N	22	O	Differential clock output 1. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT1_P	23	O	
OUT2_N	24	O	Differential clock output 2. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT2_P	25	O	
OUT3_N	26	O	Differential clock output 3. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT3_P	27	O	
OUT4_N	28	O	Differential clock output 4. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT4_P	29	O	
VDDO_3_4	30	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
OUT5_N	31	O	Differential clock output 5. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT5_P	32	O	
VDDO_5	33	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
VDDO_6	34	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
OUT6_N	35	O	Differential clock output 6. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT6_P	36	O	
OUT7_N	37	O	Differential clock output 7. Supports LP-HCSL (85Ω or 100Ω), LVDS and 1.2, 1.8, 2.5 or 3.3V LVCMOS. Leave floating if unused.
OUT7_P	38	O	
VDDO_7	39	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
VDDA	40	P	1.8, 2.5 or 3.3V power supply. See Power Supply Pin Mapping for VDD mapping
DAP	41	G	Connect to ground

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Device supply voltage	–0.3	3.9	V
V_{DDO}	Output supply voltage	–0.3	3.9	V
V_{OUT}	Voltage applied to OUTx_P and OUTx_N pins (when outputs are high or low)	–0.3	VDDO_x + 0.3	V
	Voltage applied to OUTx_P and OUTx_N pins (when outputs are LVCMOS tri-state)	–0.3	1.89	V
	Voltage applied to OUTx_P and OUTx_N pins (when outputs are LP-HCSL or LVDS tri-state)	–0.3	1.5	V
T_{stg}	Storage temperature	–65	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

V_{DD} = V_{DDO} = 1.8, 2.5 or 3.3V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
V_{DDO}	Output supply voltage	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
V_{IN}	IN_x, GPI, OTP_SEL, SCL, SDA pin input voltage	–0.3		3.6	V
	GPIO or CTRL pin input voltage	–0.3		V_{DD} + 0.3	V
T_A	Ambient temperature	–40		105	°C
T_J	Junction temperature	–40		110	°C
t_{ramp}	Power supply ramp time. VDD = 1.8V	0.05		5	ms
	Power supply ramp time. VDD = 2.5 or 3.3V	0.05		5	ms

5.4 Thermal Information

THERMAL METRIC(1)		LMK3H2108 RKP0040A (VQFN) 40 PINS	LMK3H2104 RGE0024AA (VQFN) 24 PINS	LMK3H2104 RGE0024AB (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.8	53.0	39.6	°C/W

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THERMAL METRIC(1)		LMK3H2108 RKP0040A (VQFN) 40 PINS	LMK3H2104 RGE0024AA (VQFN) 24 PINS	LMK3H2104 RGE0024AB (VQFN) 24 PINS	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.0	32.5	32.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.7	26.1	16.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	0.9	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.7	26.0	16.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	5.1	3.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY STABILITY						
Δf_{total}	Total frequency error. This includes all factors and 10-year aging at 25°C	T_A = –40 to 105°C	–25		25	ppm
$\Delta f_{aging,25°C}$	Frequency error due to aging at 25°C	T_A = 25°C, 1-year aging	1.0		3.6	ppm
		T_A = 25°C, 3-year aging	1.2		5.0	ppm
		T_A = 25°C, 5-year aging	1.3		5.7	ppm
		T_A = 25°C, 10-year aging	1.4		6.5	ppm
		T_A = 25°C, 20-year aging	1.6		7.4	ppm
CLOCK INPUT REQUIREMENTS						
f_{IN}	Input frequency	LVCMOS input buffer	0		200	MHz
		Differential input buffer	25		400	MHz
DC_{IN}	Clock input duty cycle		40		60	%
V_{IN}	Differential clock input amplitude (half of differential peak-peak voltage)	$f_0 \le$ 300MHz	150		1200	mV
		300MHz < $f_0 \le$ 400MHz	150		1200	mV
V_{CM}	Differential input common mode		0.2		3.3	V
V_{IH}	Single-ended clock input high voltage		1.2		3.6	V
V_{IL}	Single-ended clock input low voltage		–0.3		0.5	V
dV_{IN}/dt	Clock input slew rate	20% to 80%	0.15			V/ns

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Clock input capacitance per pin. Capacitance at INx_P pin or INx_N pin, when INx is configured as clock input	Common mode voltage = 0.7V. Internal input termination is disabled		2.7		pF
		Common mode voltage = 0.7V Internal 100Ω differential termination is enabled		1.4		pF
		Common mode voltage = 1.2V. Internal input termination is disabled		2.5		pF
		Common mode voltage = 1.2V Internal 100Ω differential termination is enabled		1.3		pF
		Common mode voltage = 3.3V. Internal input termination is disabled		3.4		pF
		Common mode voltage = 3.3V Internal 100Ω differential termination is enabled		1.4		pF
LP-HCSL CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		400	MHz
V_{min}	Output voltage low including undershoot		-85		85	mV
$V_{overshoot}$	Output voltage high overshoot voltage	$V_{max} – V_{OH}$			120	mV

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage[4]	OUTx_LPHCSL_VOD_SEL = 0	612	686	758	mV
		OUTx_LPHCSL_VOD_SEL = 1	638	714	789	mV
		OUTx_LPHCSL_VOD_SEL = 2	663	741	818	mV
		OUTx_LPHCSL_VOD_SEL = 3	687	768	849	mV
		OUTx_LPHCSL_VOD_SEL = 4	712	793	877	mV
		OUTx_LPHCSL_VOD_SEL = 5	734	817	905	mV
		OUTx_LPHCSL_VOD_SEL = 6	704	794	877	mV
		OUTx_LPHCSL_VOD_SEL = 7	727	820	906	mV
		OUTx_LPHCSL_VOD_SEL = 8	726	823	913	mV
		OUTx_LPHCSL_VOD_SEL = 9	748	847	941	mV
		OUTx_LPHCSL_VOD_SEL = 10	769	872	967	mV
		OUTx_LPHCSL_VOD_SEL = 11	792	896	996	mV
		OUTx_LPHCSL_VOD_SEL = 12	815	921	1023	mV
		OUTx_LPHCSL_VOD_SEL = 13	836	945	1050	mV
		OUTx_LPHCSL_VOD_SEL = 14	858	969	1080	mV
		OUTx_LPHCSL_VOD_SEL = 15	879	993	1107	mV
Z_{diff}	LP-HCSL static differential impedance	85Ω LP-HCSL	68	85	102	Ω
		100Ω LP-HCSL	80	100	120	Ω
dV/dt	Output slew rate (rising and falling edge). Measured from -150mV to +150mV on the differential waveform, centered on the zero crossing point.	OUTx_SLEW_RATE = 0[1]	2.4	3.1	3.7	V/ns
		OUTx_SLEW_RATE = 1[1]	2.2	2.9	3.4	V/ns
		OUTx_SLEW_RATE = 2[1]	2	2.6	3.1	V/ns
		OUTx_SLEW_RATE = 3[1]	1.8	2.3	2.8	V/ns
ΔdV/dt	Rising edge rate to falling edge rate matching	[1]			20	%
ODC	Output duty cycle	[1]	45		55	%
		f_{out} ≤ 325MHz	45		55	%
		325MHz < f_{out} ≤ 400 MHz	45		55	%
t_{skew}	Output to output skew	Same clock source			100	ps
V_{cross}	Absolute crossing point voltage	[1]	250		550	mV
ΔV_{cross}	Variation of V_{cross} over all clock edges	[1]			140	mV
$\lvert V_{RB} \rvert$	Absolute value of ring back voltage	[1]	100			mV
t_{stable}	Time before V_{RB} is allowed	[1]	500			ps

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{cycle-to-cycle}$	Cycle to cycle jitter, Common Clock no SSC	(1)			150	ps
$J_{cycle-to-cycle}$	Cycle to cycle jitter, Common Clock, -0.5% SSC	(1)			150	ps
t_{period_abs}	Absolute period including jitter and SSC	(1)	9.949	10	10.101	ns
$t_{period_avg_CC}$	Average clock period accuracy, Common Clock	(1)	–100		2600	ppm
$t_{period_avg_SRIS}$	Average clock period accuracy, SRIS	(1)	–100		1600	ppm
V_{OH-DC}	Output voltage high	DC simulation load, 85Ω LP-HCSL, OUTx_LPHCSL_VOD_SEL = 4	225		270	mV
V_{OL-DC}	Output voltage low		10		150	mV
$V_{cross-DC}$	Absolute crossing point voltage		130		200	mV
LVDS CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		400	MHz
$\|V_{OD}\|$	Steady-state magnitude of the differential output voltage $\|V_{OUTP} - V_{OUTN}\|$		250		450	mV
$\Delta V_{pp-diff}$	Change in differential output voltage swing between complementary output states				50	mV
V_{OS}	Steady-state output offset voltage (common mode voltage)	VDDO_x = 3.3V	1.075		1.425	V
		VDDO_x = 2.5V	1.05		1.4	V
		VDDO_x = 1.8V	1		1.25	V
ΔV_{OS}	Change in V_{OS} between complementary output states				50	mV
I_{SA}, I_{SB}	Short-circuit current. Magnitude of current with the generator output terminals short-circuited to the generator circuit common		–24		24	mA
I_{SAB}	Short-circuit current. Magnitude of current with generator output terminals short-circuited to each other		–12		12	mA
t_R, t_F	20% to 80% differential rise/fall time	OUTx_SLEW_RATE = 0			385	ps
		OUTx_SLEW_RATE = 1			545	ps
		OUTx_SLEW_RATE = 2			710	ps
		OUTx_SLEW_RATE = 3			850	ps
t_{skew}	Output to output skew	Same clock source			100	ps
ODC	Output duty cycle		45		55	%
LVCMOS CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency. Clock source is FOD or edge combiner	OUT0	38.15×10^{-6}		200	MHz
		All other outputs	156.25×10^{-3}		200	MHz
	Output frequency. Clock source is IN0, IN1 or IN2		0		200	MHz
dV/dt	Output slew rate. VDDO = 3.3V ± 5%. Measured from 20% to 80%, 4.7pF load	OUTx_CMOS_SLEW_RATE = 0	2		5.2	V/ns
		OUTx_CMOS_SLEW_RATE = 1	1.7		5	V/ns
		OUTx_CMOS_SLEW_RATE = 2	1.35		4	V/ns
		OUTx_CMOS_SLEW_RATE = 3	1		3.5	V/ns

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dV/dt	Output slew rate. VDDO = 2.5V ± 5%. Measured from 20% to 80%, 4.7pF load	OUTx_CMOS_SLEW_RATE = 0	1.5		3.9	V/ns
		OUTx_CMOS_SLEW_RATE = 1	1.3		3.8	V/ns
		OUTx_CMOS_SLEW_RATE = 2	1		3.1	V/ns
		OUTx_CMOS_SLEW_RATE = 3	0.75		2.7	V/ns
dV/dt	Output slew rate. VDDO = 1.8V ± 5%. Measured from 20% to 80%, 4.7pF load	OUTx_CMOS_SLEW_RATE = 0	1.25		2.9	V/ns
		OUTx_CMOS_SLEW_RATE = 1	1.1		2.8	V/ns
		OUTx_CMOS_SLEW_RATE = 2	0.85		2.4	V/ns
		OUTx_CMOS_SLEW_RATE = 3	0.65		2.1	V/ns
dV/dt	Output slew rate. 1.2V LVCMOS mode. VDDO = 3.3V or 2.5V. Measured from 20% to 80%, 4.7pF load	OUTx_SLEW_RATE = 0	1.5		2.1	V/ns
		OUTx_SLEW_RATE = 1	1.3		1.9	V/ns
		OUTx_SLEW_RATE = 2	1.1		1.6	V/ns
		OUTx_SLEW_RATE = 3	1		1.5	V/ns
dV/dt	Output slew rate. 1.2V LVCMOS mode. VDDO = 1.8V. Measured from 20% to 80%, 4.7pF load	OUTx_SLEW_RATE = 0	1.2		2.3	V/ns
		OUTx_SLEW_RATE = 1	1		2	V/ns
		OUTx_SLEW_RATE = 2	0.9		1.8	V/ns
		OUTx_SLEW_RATE = 3	0.8		1.6	V/ns
V_{OH}	Output high voltage	I_{OH} = –15mA at 3.3V	0.8 × VDDO		VDDO	V
		I_{OH} = –12mA at 2.5V	0.8 × VDDO		VDDO	V
		I_{OH} = –8mA at 1.8V	0.8 × VDDO		VDDO	V
V_{OL}	Output low voltage	I_{OL} = 15mA at 3.3V	0		0.4	V
		I_{OL} = 12mA at 2.5V	0		0.4	
		I_{OL} = 8mA at 1.8V	0		0.4	
$V_{OH,1.2V}$	Output high voltage in 1.2V CMOS mode	Programmed to 1.2V. I_{OH} = –3mA	0.93		1.2	V
		Programmed to 1.1V. I_{OH} = –3mA	0.86		1.1	V
$V_{OL,1.2V}$	Output low voltage in 1.2V CMOS mode	I_{OL} = 3mA	0		0.24	V
$\lvert V_{OD,1.2V\ Diff}\rvert$	$\lvert V_{OUTP} - V_{OUTN}\rvert$. Output swing in 1.2V CMOS mode with differential output termination	Programmed to 1.2V. 100Ω differential external termination. 2pF load.	539	600	660	mV
		Programmed to 1.1V. 100Ω differential external termination. 2pF load.	495	550	617	mV

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OS,1.2V\ Diff}$	Output offset voltage. Output common mode in 1.2V CMOS mode with differential output termination	Programmed to 1.2V. 100Ω differential external termination. 2pF load.	540	600	660	mV
		Programmed to 1.1V. 100Ω differential external termination. 2pF load.	495	550	605	mV
dV/dt	Differential output slew rate in 1.2V CMOS mode with 100Ω differential external termination. VDDO = 3.3V or 2.5V ± 5%. Measured from 20% to 80%, 2pF load	OUTx_SLEW_RATE = 0	2.8		3.3	V/ns
		OUTx_SLEW_RATE = 1	2.2		2.6	V/ns
		OUTx_SLEW_RATE = 2	1.8		2.1	V/ns
		OUTx_SLEW_RATE = 3	1.5		1.7	V/ns
	Differential output slew rate in 1.2V CMOS mode with 100Ω differential external termination. VDDO = 1.8V ± 5%. Measured from 20% to 80%, 2pF load	OUTx_SLEW_RATE = 0	2.5		3.3	V/ns
		OUTx_SLEW_RATE = 1	2		2.6	V/ns
		OUTx_SLEW_RATE = 2	1.6		2.1	V/ns
		OUTx_SLEW_RATE = 3	1.3		1.8	V/ns
I_{leak}	Output leakage current	Output tri-stated. VDD = VDDO = 3.465V	-35		35	µA
R_{out}	Output impedance	3.3V LVCMOS		17		Ω
		2.5V LVCMOS		17		Ω
		1.8V LVCMOS		17		Ω
		1.2V LVCMOS	40	50	60	Ω
ODC	Output duty cycle	f_{out} ≤ 156.25MHz	45		55	%
		f_{out} > 156.25MHz	45		55	%
t_{skew}	Output-to-output skew	Same clock source			100	ps
C_{load}	Maximum load capacitance				15	pF
LVCMOS REFCLK CHARACTERISTICS						
f_{out}	Output frequency		0		200	MHz
dV/dt	Output slew rate, measured from 20% to 80%	VDDO = 3.3V ± 5%(2)	2.2		6.1	V/ns
		VDDO = 2.5V ± 5%(2)	1.7		4.6	V/ns
		VDDO = 1.8V ± 5%(2)	1.45		3.4	V/ns
V_{OH}	Output high voltage	I_{OH} = –15mA at 3.3V ± 5%(2)	0.8 x VDDO		VDDO	V
		I_{OH} = –12mA at 2.5V ± 5%(2)	0.8 x VDDO		VDDO	V
		I_{OH} = –8mA at 1.8V ± 5%(2)	0.8 x VDDO		VDDO	V
V_{OL}	Output low voltage	I_{OL} = 15mA at 3.3V ± 5%(2)	0		0.4	V
		I_{OL} = 12mA at 2.5V ± 5%(2)	0		0.4	V
		I_{OL} = 8mA at 1.8V ± 5%(2)	0		0.4	V
I_{leak}	Output leakage current	Output tri-stated. VDD = VDDO = 3.465V(4)	-6		13	µA

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{out}	Output impedance	3.3V LVCMOS		17		Ω
R_{out}	Output impedance	2.5V LVCMOS		17		Ω
R_{out}	Output impedance	1.8V LVCMOS		17		Ω
ODC	Output duty cycle	f_{out} ≤ 156.25MHz(2)	45		55	%
		f_{out} > 156.25MHz(2)	45		55	%
C_{load}	Maximum load capacitance	(2)			15	pF
RJ	12kHz to 20MHz integrated RMS jitter	f_{out} = 50MHz(2)			1	ps
SSC CHARACTERISTICS						
f_{out}	Output frequency range that supports SSC		2.5		200	MHz
f_{SSC}	SSC modulation frequency		30	31.5	33	kHz
$f_{SSC-deviation}$	SSC deviation (modulation depth)	Down spread (programmable)	-0.05		-3	%
		Center spread (programmable)	±0.025		±1.5	%
df/dt	max SSC frequency slew rate	0 < $f_{SSC-deviation}$ ≤ -0.5%			1250	ppm/us
JITTER CHARACTERISTICS						
$J_{PCIe2-cc-SSC_off}$	PCIe Gen 2 Common Clock jitter, SSC is off (jitter limit = 3ps)	Only FOD0 or FOD1 is enabled. SSC disabled			0.27	ps
$J_{PCIe2-cc-SSC_on}$	PCIe Gen 2 Common Clock jitter, -0.5% ≤ SSC < 0% (jitter limit = 3ps)	Only FOD0 or FOD1 is enabled. SSC enabled			0.48	ps
$J_{PCIe2-SRNS}$	PCIe Gen 2 SRNS jitter	Only FOD0 or FOD1 is enabled. SSC disabled			0.32	ps
$J_{PCIe2-SRIS}$	PCIe Gen 2 SRIS jitter, -0.3% ≤ SSC < 0%	Only FOD0 or FOD1 is enabled. SSC enabled			0.51	ps
$J_{PCIe3-cc-SSC_off}$	PCIe Gen 3 Common Clock jitter, SSC is off (jitter limit = 1ps)	Only FOD0 or FOD1 is enabled. SSC disabled			80	fs
$J_{PCIe3-cc-SSC_on}$	PCIe Gen 3 Common Clock jitter, -0.5% ≤ SSC < 0% (jitter limit = 1ps)	Only FOD0 or FOD1 is enabled. SSC enabled			145	fs
$J_{PCIe3-SRNS}$	PCIe Gen 3 SRNS jitter	Only FOD0 or FOD1 is enabled. SSC disabled			95	fs
$J_{PCIe3-SRIS}$	PCIe Gen 3 SRIS jitter, -0.3% ≤ SSC < 0%	Only FOD0 or FOD1 is enabled. SSC enabled			440	fs
$J_{PCIe4-cc-SSC_off}$	PCIe Gen 4 Common Clock jitter, SSC is off (jitter limit = 500 fs)	Only FOD0 or FOD1 is enabled. SSC disabled			76	fs
$J_{PCIe4-cc-SSC_on}$	PCIe Gen 4 Common Clock jitter, -0.5% ≤ SSC < 0% (jitter limit = 500 fs)	Only FOD0 or FOD1 is enabled. SSC enabled			144	fs
$J_{PCIe4-SRNS}$	PCIe Gen 4 SRNS jitter	Only FOD0 or FOD1 is enabled. SSC disabled			95	fs
$J_{PCIe4-SRIS}$	PCIe Gen 4 SRIS jitter, -0.3% ≤ SSC < 0%	Only FOD0 or FOD1 is enabled. SSC enabled			215	fs
$J_{PCIe5-cc-SSC_off}$	PCIe Gen 5 Common Clock jitter, SSC is off (jitter limit = 150 fs)	Only FOD0 or FOD1 is enabled. SSC disabled			29	fs
$J_{PCIe5-cc-SSC_on}$	PCIe Gen 5 Common Clock jitter, -0.5% ≤ SSC < 0% (jitter limit = 150 fs)	Only FOD0 or FOD1 is enabled. SSC enabled			61	fs
$J_{PCIe5-SRNS}$	PCIe Gen 5 SRNS jitter	Only FOD0 or FOD1 is enabled. SSC disabled			36	fs
$J_{PCIe5-SRIS}$	PCIe Gen 5 SRIS jitter, -0.3% ≤ SSC < 0%	Only FOD0 or FOD1 is enabled. SSC enabled			66	fs
$J_{PCIe6-cc-SSC_off}$	PCIe Gen 6 Common Clock jitter, SSC is off (jitter limit = 100 fs)	Only FOD0 or FOD1 is enabled. SSC disabled			19.3	fs
$J_{PCIe6-cc-SSC_on}$	PCIe Gen 6 Common Clock jitter, -0.5% ≤ SSC < 0% (jitter limit = 100 fs)	Only FOD0 or FOD1 is enabled. SSC enabled			36.4	fs

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe6-SRNS}$	PCIe Gen 6 SRNS jitter	Only FOD0 or FOD1 is enabled. SSC disabled			29.3	fs
$J_{PCIe6-SRIS}$	PCIe Gen 6 SRIS jitter, -0.3% ≤ SSC < 0%	Only FOD0 or FOD1 is enabled. SSC enabled			48.3	fs
$J_{PCIe7-cc-SSC_off}$	PCIe Gen 7 Common Clock jitter, SSC is off	Only FOD0 or FOD1 is enabled. SSC disabled			13.5	fs
$J_{PCIe7-cc-SSC_on}$	PCIe Gen 7 Common Clock jitter, -0.5% ≤ SSC < 0%	Only FOD0 or FOD1 is enabled. SSC enabled			25.5	fs
$J_{PCIe7-SRNS}$	PCIe Gen 7 SRNS jitter	Only FOD0 or FOD1 is enabled. SSC disabled			20.6	fs
$J_{PCIe7-SRIS}$	PCIe Gen 7 SRIS jitter, -0.15% ≤ SSC < 0%	Only FOD0 or FOD1 is enabled. SSC enabled			26.4	fs
RJ_{RMS}	12 kHz to 20MHz RMS jitter	f_{out} = 156.25MHz. Only FOD0 or FOD1 is enabled.		154	211	fs
BUFFER MODE CHARACTERISTICS						
$J_{PCIe1-CC}$	PCIe Gen 1 CC	Differential input slew rate ≥ 3.5V/ns. Differential input swing ≥ 1600mV			977	fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC				229	fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC				88	fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC				88	fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC				34	fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC				22	fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR				268	fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR				72	fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR				72	fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR				28	fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR				23	fs
$J_{PCIe1-CC}$	PCIe Gen 1 CC	Differential input slew rate ≥ 1.5V/ns. Differential input swing ≥ 800mV			977	fs
$J_{PCIe2-CC}$	PCIe Gen 2 CC				231	fs
$J_{PCIe3-CC}$	PCIe Gen 3 CC				90	fs
$J_{PCIe4-CC}$	PCIe Gen 4 CC				90	fs
$J_{PCIe5-CC}$	PCIe Gen 5 CC				34	fs
$J_{PCIe6-CC}$	PCIe Gen 6 CC				23	fs
$J_{PCIe2-IR}$	PCIe Gen 2 IR				273	fs
$J_{PCIe3-IR}$	PCIe Gen 3 IR				73	fs
$J_{PCIe4-IR}$	PCIe Gen 4 IR				73	fs
$J_{PCIe5-IR}$	PCIe Gen 5 IR				28	fs
$J_{PCIe6-IR}$	PCIe Gen 6 IR				23	fs
$J_{RMS-additive}$	Additive 12kHz to 20MHz RMS jitter at 100MHz	Differential input slew rate ≥ 3.5V/ns. Differential input swing ≥ 1600mV		73	145	fs
		Differential input slew rate ≥ 1.5V/ns. Differential input swing ≥ 800mV		77	153	fs

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{RMS\text{-}additive}$	Additive 12kHz to 20MHz RMS jitter at 156.25MHz	Differential input slew rate ≥ 3.5V/ns. Differential input swing ≥ 1600mV		57	122	fs
		Differential input slew rate ≥ 1.5V/ns. Differential input swing ≥ 800mV		59	124	fs
$J_{RMS\text{-}additive}$	Additive 12kHz to 70MHz RMS jitter at 156.25MHz	Differential input slew rate ≥ 3.5V/ns. Differential input swing ≥ 1600mV		106	156	fs
		Differential input slew rate ≥ 1.5V/ns. Differential input swing ≥ 800mV		108	161	fs
$J_{RMS\text{-}additive}$	Additive 12kHz to 20MHz RMS jitter at 312.5MHz	Differential input slew rate ≥ 3.5V/ns. Differential input swing ≥ 1600mV		48	90	fs
		Differential input slew rate ≥ 1.5V/ns. Differential input swing ≥ 800mV		51	94	fs
$J_{RMS\text{-}additive}$	Additive 12kHz to 70MHz RMS jitter at 312.5MHz	Differential input slew rate ≥ 3.5V/ns. Differential input swing ≥ 1600mV		81	123	fs
		Differential input slew rate ≥ 1.5V/ns. Differential input swing ≥ 800mV		82	128	fs
t_{skew}	Output-to-output skew	Same clock source			100	ps
t_{PD}	Input-to-output delay				1.1	ns
Δt_{PD}	Input-to-output delay variation	Single device over temperature and voltage. 100MHz, LP-HCSL output			2	ps/°C
DCD	Duty cycle distortion	Differential input, f ≤ 400MHz, differential input slew rate ≥ 1.5V/ns, differential input swing ≥ 800mV	-3		3	%
		CMOS input, f ≤ 200MHz, rise/fall time ≤ 1ns	-11		11	%
		CMOS input, f ≤ 156.25MHz, rise/fall time ≤ 1ns	-9		9	%
		CMOS input, f ≤ 50MHz, rise/fall time ≤ 1ns	-3		3	%
TIMING CHARACTERISTICS						

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{startup}$	Startup time	VDD = 2.5/3.3V. Time elapsed from all VDD pins reaching 1.62V to the first output clock rising edge		2.4	5	ms
		VDD = 1.8V. Time elapsed from all VDD pins reaching 1.62V to the first output clock rising edge		1.6	5	ms
t_{OE}	Output enable time. After CLOCK_READY status is '1', time elapsed between OE assertion and the first output clock rising edge	Full sync mode	3 output clock cycles		7 output clock cycles + 40ns	
		Self sync mode	3 output clock cycles		7 output clock cycles + 40ns	
		No sync mode	0		40	ns
t_{OD}	Output disable time. Time elapsed between OE deassertion and the last output clock falling edge.	Full sync mode	3 output clock cycles		7 output clock cycles + 40ns	
		Self sync mode	3 output clock cycles		7 output clock cycles + 40ns	
		No sync mode	0		40	ns
t_{OTP}	Dynamic OTP switch time	Measured between the last falling edge and the first rising edge of clock output when OTP page changes		900		µs
SUPPLY CURRENT CHARACTERISTICS						
I_{DDR}	V_{DDR} pin supply current (LMK3H2108 only)	IN1 and IN2 are powered down			5.1	mA
		IN1 or IN2 is enabled			14.1	mA
		IN1 and IN2 are enabled			25.1	mA
I_{DDX}	V_{DDX} pin supply current (LMK3H2108 only)	IN0 is powered down			2.5	mA
		IN0 is enabled			13.4	mA
I_{DDA}	V_{DDA} pin supply current	One FOD is enabled. FOD frequency = 200MHz			49.6	mA
		One FOD is enabled. FOD frequency = 400MHz			55.7	mA
		Both FODs are enabled. FOD frequency = 200MHz			59.2	mA
		Both FODs are enabled. FOD frequency = 400MHz			74.4	mA

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DDD}	V_{DDD} pin supply current	One FOD is enabled. FOD frequency = 200MHz			45.8	mA
		One FOD is enabled. FOD frequency = 400MHz			52.4	mA
		Both FODs are enabled. FOD frequency = 200MHz			58.4	mA
		Both FODs are enabled. FOD frequency = 400MHz			70	mA
I_{DDO_CMOS}	V_{DDO} pin supply current per LVCMOS output pair	V_{DDO} = 1.8V ± 5%. f_{out} = 50MHz			5	mA
		V_{DDO} = 2.5V ± 5%. f_{out} = 50MHz			6.4	mA
		V_{DDO} = 3.3V ± 5%. f_{out} = 50MHz			7.7	mA
		V_{DDO} = 1.8V ± 5%. f_{out} = 200MHz			13.4	mA
		V_{DDO} = 2.5V ± 5%. f_{out} = 200MHz			17.3	mA
		V_{DDO} = 3.3V ± 5%. f_{out} = 200MHz			21.7	mA
$I_{DDO_1.2VCMOS}$	V_{DDO} pin supply current per 1.2V LVCMOS output pair	V_{DDO} = 1.8V ± 5%. 1.2V LVCMOS is enabled. f_{out} = 50MHz. High impedance termination.			11.9	mA
		V_{DDO} = 1.8V ± 5%. 1.2V LVCMOS is enabled. f_{out} = 200MHz. High impedance termination.			15.6	mA
		V_{DDO} = 1.8V ± 5%. 1.2V LVCMOS is enabled. f_{out} = 50MHz. 100Ω differential termination.			15.8	mA
		V_{DDO} = 1.8V ± 5%. 1.2V LVCMOS is enabled. f_{out} = 200MHz. 100Ω differential termination.			18.2	mA
I_{DDO_LPHCSL}	V_{DDO} pin supply current per LP-HCSL output pair	V_{DDO} = 1.8, 2.5 or 3.3V ± 5%. f_{out} = 100MHz			10.8	mA
		V_{DDO} = 1.8, 2.5 or 3.3V ± 5%. f_{out} = 400MHz			16.4	mA
I_{DDO_LVDS}	V_{DDO} pin supply current per LVDS output pair	V_{DDO} = 1.8, 2.5 or 3.3V ± 5%. f_{out} = 100MHz			8	mA
		V_{DDO} = 1.8, 2.5 or 3.3V ± 5%. f_{out} = 400MHz			11.3	mA
I_{DD_PD}	Total power down current	V_{DDO} = 1.8V ± 5%			53	mA
		V_{DDO} = 3.3V ± 5%			67	mA
PSNR CHARACTERISTICS						

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PSNR_{2.5/3.3V_CLK_GEN}$	Power Supply Noise Rejection. VDDx = 2.5 or 3.3V. Clock generator mode (clock source is FOD or edge combiner). Ripple applied to all non-VDDO power supply pins[3]	10kHz		-88.9		dBc
		50kHz		-89.9		dBc
		100kHz		-89.2		dBc
		500kHz		-82.6		dBc
		1MHz		-93.3		dBc
		5MHz		-86.8		dBc
		10MHz		-89.3		dBc
	Power Supply Noise Rejection. VDDx = 2.5 or 3.3V. Clock generator mode (clock source is FOD or edge combiner). Ripple applied to all VDDO pins. LVCMOS output format[3]	10kHz		-72		dBc
		50kHz		-72.6		dBc
		100kHz		-72.1		dBc
		500kHz		-71.4		dBc
		1MHz		-92.5		dBc
		5MHz		-90.7		dBc
		10MHz		-92.6		dBc
	Power Supply Noise Rejection. VDDx = 2.5 or 3.3V. Clock generator mode (clock source is FOD or edge combiner). Ripple applied to all VDDO pins. LVDS output format[3]	10kHz		-87.5		dBc
		50kHz		-87.9		dBc
		100kHz		-83.7		dBc
		500kHz		-72.3		dBc
		1MHz		-91.8		dBc
		5MHz		-87.6		dBc
		10MHz		-89.9		dBc
	Power Supply Noise Rejection. VDDx = 2.5 or 3.3V. Clock generator mode (clock source is FOD or edge combiner). Ripple applied to all VDDO pins. HCSL output format[3]	10kHz		-87.1		dBc
		50kHz		-88.8		dBc
		100kHz		-88.4		dBc
		500kHz		-89.7		dBc
		1MHz		-93.8		dBc
		5MHz		-98.8		dBc
		10MHz		-91.2		dBc

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$PSNR_{1.8V_CLK_GEN}$	Power Supply Noise Rejection. VDDx = 1.8V. Clock generator mode (clock source is FOD or edge combiner). Ripple applied to all non-VDDO power supply pins[3]	10kHz		-74.1		dBc
		50kHz		-75.1		dBc
		100kHz		-73.2		dBc
		500kHz		-67.2		dBc
		1MHz		-89.3		dBc
		5MHz		-78.9		dBc
		10MHz		-83.1		dBc
	Power Supply Noise Rejection. VDDx = 1.8V. Clock generator mode (clock source is FOD or edge combiner). Ripple applied to all VDDO pins. LVCMOS output format[3]	10kHz		-56.9		dBc
		50kHz		-57.5		dBc
		100kHz		-57		dBc
		500kHz		-56.4		dBc
		1MHz		-82.1		dBc
		5MHz		-75.2		dBc
		10MHz		-88.2		dBc
	Power Supply Noise Rejection. VDDx = 1.8V. Clock generator mode (clock source is FOD or edge combiner). Ripple applied to all VDDO pins. LVDS output format[3]	10kHz		-78.4		dBc
		50kHz		-79.1		dBc
		100kHz		-74.5		dBc
		500kHz		-66.6		dBc
		1MHz		-89.4		dBc
		5MHz		-82.8		dBc
		10MHz		-89.4		dBc
	Power Supply Noise Rejection. VDDx = 1.8V. Clock generator mode (clock source is FOD or edge combiner). Ripple applied to all VDDO pins. HCSL output format[3]	10kHz		-78.1		dBc
		50kHz		-81.5		dBc
		100kHz		-81.2		dBc
		500kHz		-89.8		dBc
		1MHz		-93.9		dBc
		5MHz		-90.5		dBc
		10MHz		-91.3		dBc
LMK3H2104 I/O CHARACTERISTICS						
V_{IH}	Input voltage high for OTP_SEL_[1:0] (Pin 4, 5)		0.7 × V_{DDD}		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for OTP_SEL_[1:0] (Pin 4, 5)		GND – 0.3		0.8	V
V_{IH}	Input voltage high for CTRL (Pin 23)		0.65 × V_{DD_REF}		V_{DD_REF} + 0.3	V
V_{IL}	Input voltage low for CTRL (Pin 23)		-0.3		0.4	V
V_{IH}	Input voltage high for GPI_[2:0] (Pin 1, 2, 6)	V_{DDD} = 1.8V ± 5%	0.65 × V_{DDD}		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for GPI_[2:0] (Pin 1, 2, 6)		–0.3		0.35 × V_{DDD}	V
V_{IH}	Input voltage high for GPIO_[1:0] (Pin 8, 9)		0.65 × V_{DDD}		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for GPIO_[1:0] (Pin 8, 9)		–0.3		0.35 × V_{DDD}	V
V_{IH}	Input voltage high for GPI_[2:0] (Pin 1, 2, 6)	V_{DDD} = 2.5V ± 5%	1.7		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for GPI_[2:0] (Pin 1, 2, 6)		–0.3		0.7	V
V_{IH}	Input voltage high for GPIO_[1:0] (Pin 8, 9)		1.7		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for GPIO_[1:0] (Pin 8, 9)		–0.3		0.7	V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input voltage high for GPI_[2:0] (Pin 1, 2, 6)	V_{DDD} = 3.3V ± 5%	2.2		3.6	V
V_{IL}	Input voltage low for GPI_[2:0] (Pin 1, 2, 6)		–0.3		0.8	V
V_{IH}	Input voltage high for GPIO_[1:0] (Pin 8, 9)		2.2		3.6	V
V_{IL}	Input voltage low for GPIO_[1:0] (Pin 8, 9)		–0.3		0.8	V
V_{OH}	Output voltage high for GPIO_[1:0]	V_{DDD} = 1.8V ± 5%, I_{OH} = –2mA	V_{DDD} – 0.45		V_{DDD} + 0.3	V
V_{OL}	Output voltage low for GPIO_[1:0]	V_{DDD} = 1.8V ± 5%, I_{OL} = 2mA			0.45	V
V_{OH}	Output voltage high for GPIO_[1:0]	V_{DDD} = 2.5V ± 5%, I_{OH} = –2mA	1.7		V_{DDD} + 0.3	V
V_{OL}	Output voltage low for GPIO_[1:0]	V_{DDD} = 2.5V ± 5%, I_{OL} = 2mA			0.7	V
V_{OH}	Output voltage high for GPIO_[1:0]	V_{DDD} = 3.3V ± 5%, I_{OH} = –2mA	2.4		V_{DDD} + 0.3	V
V_{OL}	Output voltage low for GPIO_[1:0]	V_{DDD} = 3.3V ± 5%, I_{OL} = 2mA			0.4	V
$R_{pu/pd}$	Recommended external pull-up/pull-down resistor for OTP_SEL_[1:0] and CTRL		0		60	kΩ
	Recommended external pull-up/pull-down resistor for GPI_[2:0] and GPIO_[1:0]		0		10	kΩ
$I_{L,GPI}$	GPI_[2:0] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V, V_{IH} = V_{DD} = 1.8V ± 5%	-32		128	µA
	GPI_[2:0] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V, V_{IH} = V_{DD} = 2.5V ± 5%	-32		143	µA
	GPI_[2:0] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V, V_{IH} = V_{DD} = 3.3V ± 5%	-32		171	µA
$I_{L,GPIO}$	GPIO_[1:0] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V, V_{IH} = V_{DD} = 1.8V ± 5%	-37		32	µA
	GPIO_[1:0] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V, V_{IH} = V_{DD} = 2.5V ± 5%	-47		43	µA
	GPIO_[1:0] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V, V_{IH} = V_{DD} = 3.3V ± 5%	-57		57	µA
C_{in}	Input capacitance for OTP_SEL_[1:0] and CTRL				3	pF
	Input capacitance for GPI_[2:0]				5.5	pF
	Input capacitance for GPIO_[1:0]				3.5	pF
LMK3H2108 I/O CHARACTERISTICS						

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input voltage high for GPI_[1:0] (Pin 1, 2)	V_{DDD}, V_{DDX} or V_{DDR} = 1.8V ± 5%	0.65 × V_{DDX}		V_{DDX} + 0.3	V
V_{IL}	Input voltage low for GPI_[1:0] (Pin 1, 2)		–0.3		0.35 × V_{DDX}	V
V_{IH}	Input voltage high for GPI_[5:2] (Pin 4, 5, 7, 8)		0.65 × V_{DDR}		V_{DDR} + 0.3	V
V_{IL}	Input voltage low for GPI_[5:2] (Pin 4, 5, 7, 8)		–0.3		0.35 × V_{DDR}	V
V_{IH}	Input voltage high for GPIO_[4:3] (Pin 15, 16)		0.65 × V_{DDD}		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for GPIO_[4:3] (Pin 15, 16)		–0.3		0.35 × V_{DDD}	V
V_{IH}	Input voltage high for 2-level GPIO_[2:0] (Pin 12, 13, 14)		0.65 × V_{DDD}		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for 2-level GPIO_[2:0] (Pin 12, 13, 14)		–0.3		0.35 × V_{DDD}	V
V_{IH}	Input voltage high for 3-level GPIO_[2:0] (Pin 12, 13, 14)		0.75 × V_{DDD}		V_{DDD} + 0.3	V
V_{IM}	Input voltage mid for 3-level GPIO_[2:0] (Pin 12, 13, 14)		0.45 × V_{DDD}		0.55 × V_{DDD}	V
V_{IL}	Input voltage low for 3-level GPIO_[2:0] (Pin 12, 13, 14)		–0.3		0.25 × V_{DDD}	V
V_{IH}	Input voltage high for GPI_[1:0] (Pin 1, 2)	V_{DDD}, V_{DDX} or V_{DDR} = 2.5V ± 5%	1.7		V_{DDX} + 0.3	V
V_{IL}	Input voltage low for GPI_[1:0] (Pin 1, 2)		–0.3		0.7	V
V_{IH}	Input voltage high for GPI_[5:2] (Pin 4, 5, 7, 8)		1.7		V_{DDR} + 0.3	V
V_{IL}	Input voltage low for GPI_[5:2] (Pin 4, 5, 7, 8)		–0.3		0.7	V
V_{IH}	Input voltage high for GPIO_[4:3] (Pin 15, 16)		1.7		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for GPIO_[4:3] (Pin 15, 16)		–0.3		0.7	V
V_{IH}	Input voltage high for 2-level GPIO_[2:0] (Pin 12, 13, 14)		1.7		V_{DDD} + 0.3	V
V_{IL}	Input voltage low for 2-level GPIO_[2:0] (Pin 12, 13, 14)		–0.3		0.7	V
V_{IH}	Input voltage high for 3-level GPIO_[2:0] (Pin 12, 13, 14)		0.75 × V_{DDD}		V_{DDD} + 0.3	V
V_{IM}	Input voltage mid for 3-level GPIO_[2:0] (Pin 12, 13, 14)		0.45 × V_{DDD}		0.55 × V_{DDD}	V
V_{IL}	Input voltage low for 3-level GPIO_[2:0] (Pin 12, 13, 14)		–0.3		0.25 × V_{DDD}	V

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input voltage high for GPI_[1:0] (Pin 1, 2)	V_{DDD}, V_{DDX} or V_{DDR} = 3.3V ± 5%	2.2		3.6	V
V_{IL}	Input voltage low for GPI_[1:0] (Pin 1, 2)		–0.3		0.8	V
V_{IH}	Input voltage high for GPI_[5:2] (Pin 4, 5, 7, 8)		2.2		3.6	V
V_{IL}	Input voltage low for GPI_[5:2] (Pin 4, 5, 7, 8)		–0.3		0.8	V
V_{IH}	Input voltage high for GPIO_[4:3] (Pin 15, 16)		2.2		3.6	V
V_{IL}	Input voltage low for GPIO_[4:3] (Pin 15, 16)		–0.3		0.8	V
V_{IH}	Input voltage high for 2-level GPIO_[2:0] (Pin 12, 13, 14)		2.2		3.6	V
V_{IL}	Input voltage low for 2-level GPIO_[2:0] (Pin 12, 13, 14)		–0.3		0.8	V
V_{IH}	Input voltage high for 3-level GPIO_[2:0] (Pin 12, 13, 14)		0.75 × V_{DDD}		3.6	V
V_{IM}	Input voltage mid for 3-level GPIO_[2:0] (Pin 12, 13, 14)		0.45 × V_{DDD}		0.55 × V_{DDD}	V
V_{IL}	Input voltage low for 3-level GPIO_[2:0] (Pin 12, 13, 14)		–0.3		0.25 × V_{DDD}	V
V_{OH}	Output voltage high for GPIO_[4:0]	V_{DDD} = 1.8V ± 5%, I_{OH} = –2mA	V_{DDD} – 0.45		V_{DDD} + 0.3	V
V_{OL}	Output voltage low for GPIO_[4:0]	V_{DDD} = 1.8V ± 5%, I_{OL} = 2mA			0.45	V
V_{OH}	Output voltage high for GPIO_[4:0]	V_{DDD} = 2.5V ± 5%, I_{OH} = –2mA	1.7		V_{DDD} + 0.3	V
V_{OL}	Output voltage low for GPIO_[4:0]	V_{DDD} = 2.5V ± 5%, I_{OL} = 2mA			0.7	V
V_{OH}	Output voltage high for GPIO_[4:0]	V_{DDD} = 3.3V ± 5%, I_{OH} = –2mA	2.4		V_{DDD} + 0.3	V
V_{OL}	Output voltage low for GPIO_[4:0]	V_{DDD} = 3.3V ± 5%, I_{OL} = 2mA			0.4	V
$R_{pu/pd}$	Recommended external pull-up/pull-down resistor for GPI_[5:0] and GPIO_[4:0]		0		10	kΩ

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	GPI_[1:0] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDX} = 1.8V ± 5%	-32		128	µA
		Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDX} = 2.5V ± 5%	-32		142	µA
		Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDX} = 3.3V ± 5%	-32		171	µA
	GPI_[5:2] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDR} = 1.8V ± 5%	-32		128	µA
		Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDR} = 2.5V ± 5%	-32		143	µA
		Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDR} = 3.3V ± 5%	-32		171	µA
	GPIO_[4:0] input leakage current	Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDR} = 1.8V ± 5%	-37		32	µA
		Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDR} = 2.5V ± 5%	-47		43	µA
		Including pull-up/pull-down resistor. V_{IL} = 0V. V_{IH} = V_{DDR} = 3.3V ± 5%	-57		57	µA
C_{IN}	Input capacitance for GPI_[3:0]				5.5	pF
	Input capacitance for GPIO_[4:0]				3.5	pF
I2C I/O CHARACTERISTICS						
V_{IH}	Input voltage high for SCL and SDA		0.7 × V_{DDD}			V
V_{IL}	Input voltage low for SCL and SDA				0.3 × V_{DDD}	V
V_{OL}	Output voltage low for SDA	I_{OL} = 4mA			0.4	V
I_L	Input leakage current for SCL and SDA		-10		10	µA
C_{IN}	Input capacitance for SCL and SDA			1		pF

(1) PCIe test load, 15dB loss at 4GHz, f_{out} = 100MHz, trace impedance = 100Ω, high impedance load
(2) Tested with 10kΩ external pullup or pulldown resistor
(3) 0.1µF capacitor placed close to each power supply pin. Apply 50mVpp ripple (ripple is 50mV when the 0.1µF capacitor is not present) and measure the spur level at the clock output
(4) Measured using 100Ω LP-HCSL output with 100MHz output frequency. Actual V_{OH} differs based on the output frequency

5.6 I2C Characteristics

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	After this period, the first clock pulse is generated	4		0.6		µs
t_{LOW}	low period of the SCL clock		4.7		1.3		µs
t_{HIGH}	high period of the SCL clock		4		0.6		µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7		0.6		µs
$t_{HD;DAT}$	data hold time		0		0		µs

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PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
$t_{SU;DAT}$	data set-up time		250		100		ns
t_r	rise time of both SDA and SCL signals			1000	20	300	ns
t_f	fall time of both SDA and SCL signals			300	20 × (VDD / 5.5V)	300	ns
$t_{SU;STO}$	set-up time for STOP condition		4		0.6		µs
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		µs
C_b	capacitive load for each bus line			400		400	pF
$t_{VD;DAT}$	data valid time			3.45		0.9	µs
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9	µs
V_{nL}	noise margin at the low level	For each connected device, including hysteresis	0.1 × VDD		0.1 × VDD		V
V_{nH}	noise margin at the high level	For each connected device, including hysteresis	0.2 × VDD		0.2 × VDD		V

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6 Parameter Measurement Information

This section contains illustrations for the measurement of the characteristics specified under the Electrical Characteristics.

6.1 LP-HCSL Test or Simulation Loads

There are 3 test or simulation loads for LP-HCSL clock output characteristics.

- Regular LP-HCSL test load. This test load is used for all LP-HCSL output specifications unless otherwise specified in the test condition.
- LP-HCSL PCIe AC test load. This is the PCIe clock test load specified in PCI-SIG standard.
- LP-HCSL DC simulation load. This is the DC simulation load specified for CK440.

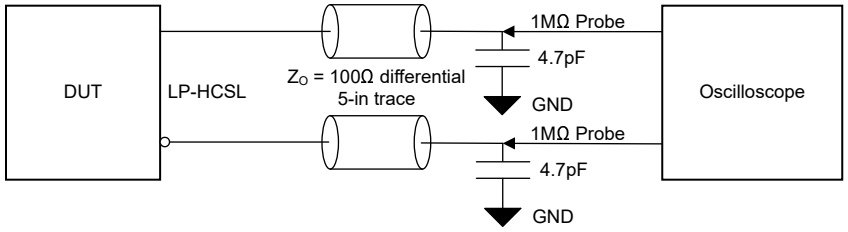


Figure 6-1. Regular LP-HCSL Test Load

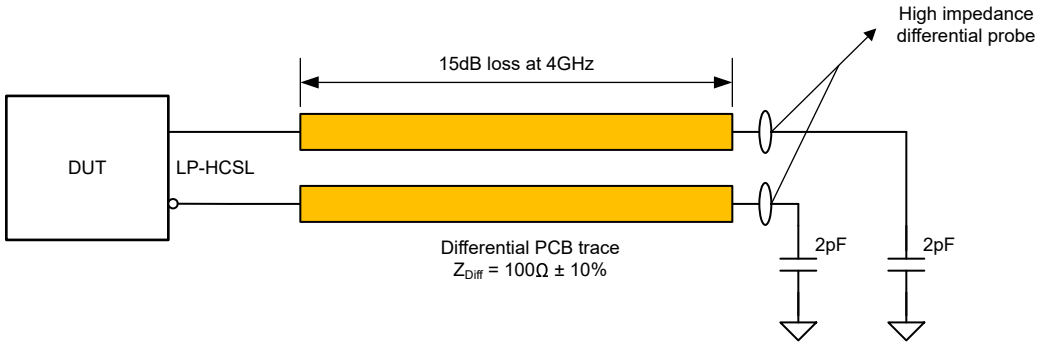


Figure 6-2. LP-HCSL PCIe AC Test Load

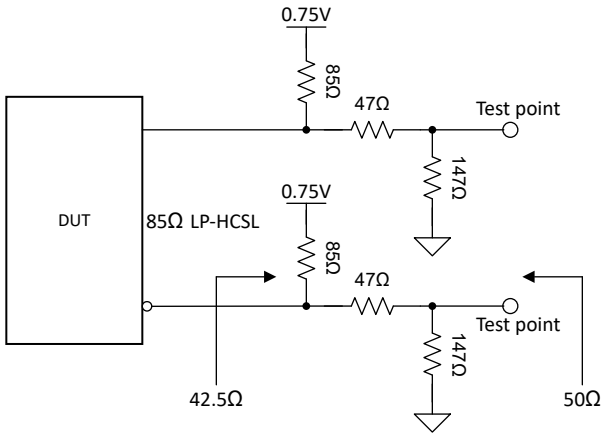


Figure 6-3. LP-HCSL DC Simulation Load

6.2 LVDS Test Load

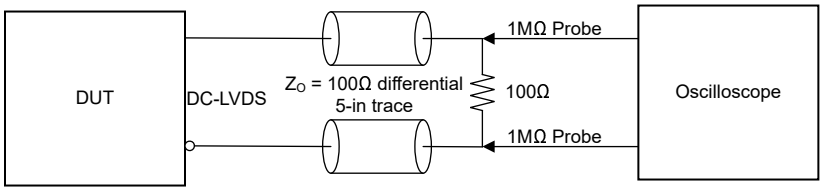


Figure 6-4. LVDS Test Load

6.3 LVCMOS Test Load

There are 3 test loads for LVCMOS clock output characteristics:

- 1.8V, 2.5V and 3.3V LVCMOS test load. 33Ω series resistor is required for a 50Ω trace, because the LVCMOS output impedance is 17Ω.
- 1.2V LVCMOS test load. No series resistor is required for a 50Ω trace, because the LVCMOS output impedance is 50Ω.
- Differential 1.2V LVCMOS test load. 1.2V LVCMOS can be used differentially which provides more flexibility in output swing and common mode. 2 types of terminations are commonly used:
  - Same with regular single-ended LVCMOS: high impedance termination or no termination. The differential LVCMOS output characteristics is the same with single-ended LVCMOS.
  - External 100Ω differential termination. The output characteristics using this termination is specified in the Electrical Characteristics.

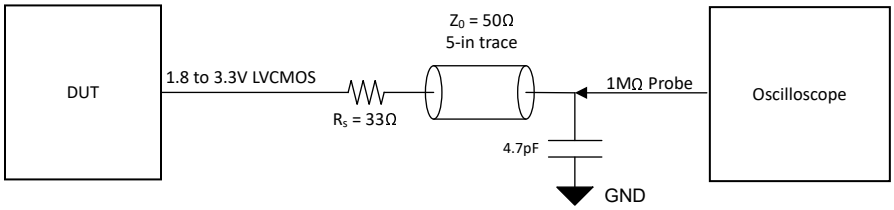


Figure 6-5. 1.8V, 2.5V and 3.3V LVCMOS Test Load

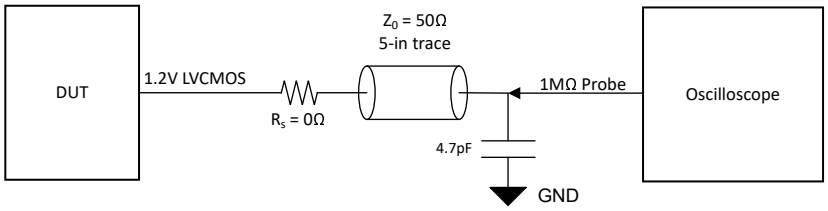


Figure 6-6. 1.2V LVCMOS Test Load

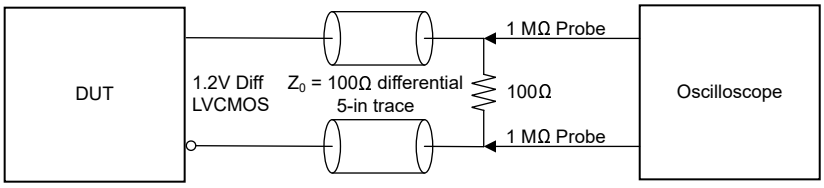


Figure 6-7. Differential 1.2V LVCMOS Test Load

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7 Detailed Description

7.1 Overview

LMK3H2104 and LMK3H2108 are clock generators, clock buffers and clock MUX. Each output bank can independently select a clock source: IN0, IN1, IN2, FOD0, FOD1 or edge combiner. Multiple GPI and GPIO pins are available to provide flexible pin controls.

7.2 Functional Block Diagram

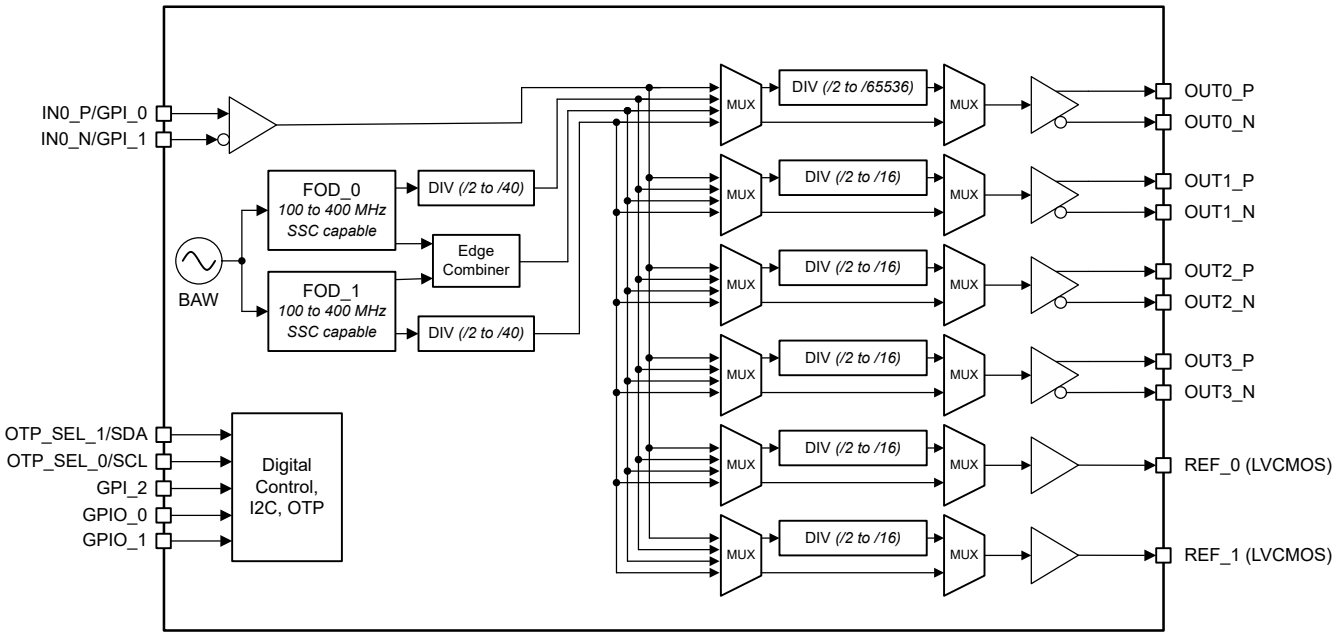


Figure 7-1. LMK3H2104 Functional Block Diagram

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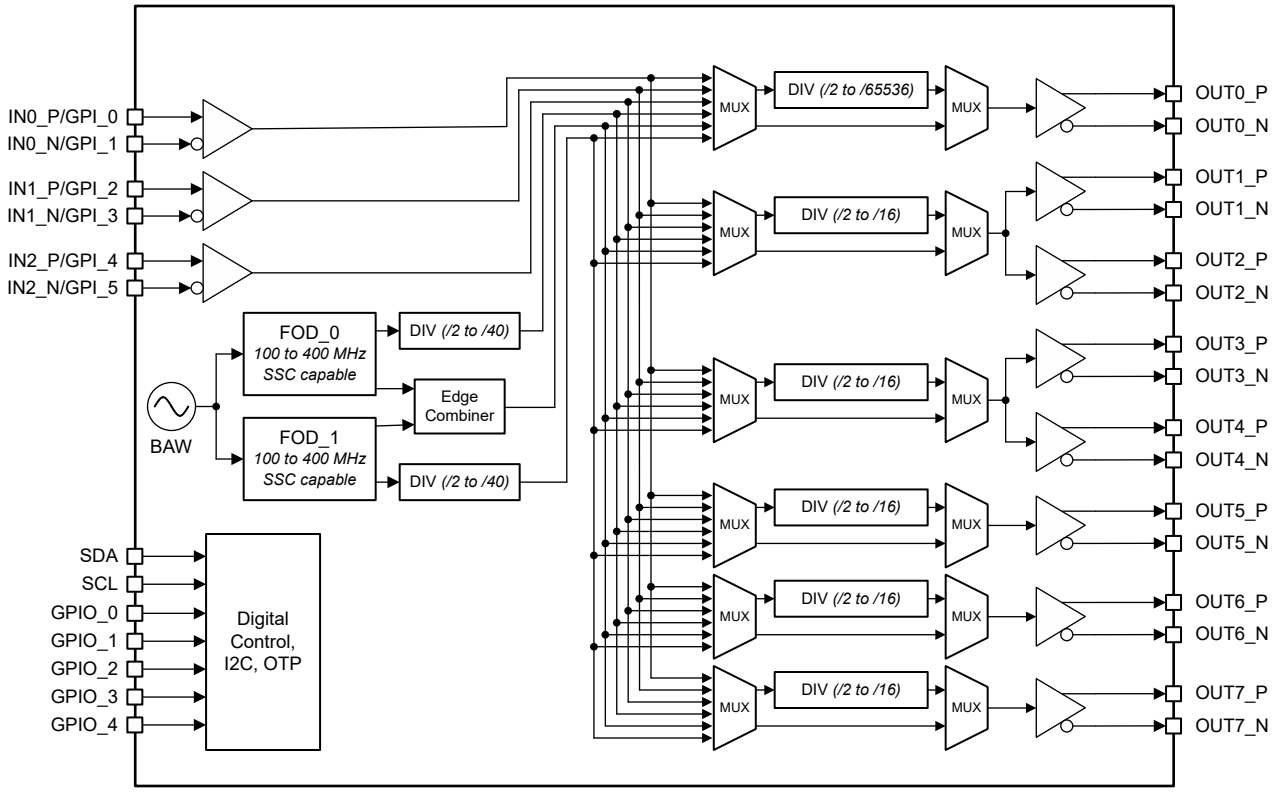


Figure 7-2. LMK3H2108 Functional Block Diagram

7.3 Feature Description

7.3.1 GPI/GPIO

7.3.1.1 GPI/GPIO Pin Functions

Table 7-1 and Table 7-2 show which functions can be assigned to which GPI or GPIO pin. PWRGD/PWRDN# assignment overrides all the other GPI/GPIO functions, except for dynamic OTP_SEL for GPIO_0, 1 and 2. See PWRGD/PWRDN# section for details.

Table 7-1. LMK3H2108 GPI/GPIO Pin Function Assignment

Pin	OE_GROUP	GOE	7-bit I2C Address	PERST#	Dynamic OTP Select	GPI	Status output	GPO
GPI_0	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	-	GPI	-	-
GPI_1	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	-	GPI	-	-
GPI_2	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	-	GPI	-	-

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Table 7-1. LMK3H2108 GPI/GPIO Pin Function Assignment (continued)

Pin	OE_GROUP	GOE	7-bit I2C Address	PERST#	Dynamic OTP Select	GPI	Status output	GPO
GPI_3	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	-	GPI	-	-
GPI_4	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	-	GPI	-	-
GPI_5	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4, OE_GROUP_5	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	-	GPI	-	-
GPIO_0	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4, OE_GROUP_6	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	Bit 0 (2 or 3 level)	GPI	DEV_INTR, CLK_READY, IN0_LOS, IN1_LOS, IN2_LOS, IN0_LOS_EVT, IN1_LOS_EVT, IN2_LOS_EVT, IN0_LOS_LMT_EVT, IN1_LOS_LMT_EVT, IN2_LOS_LMT_EVT, IN0_PERST_BUF_MODE_STAT, IN1_PERST_BUF_MODE_STAT, IN2_PERST_BUF_MODE_STAT	GPO_0
GPIO_1	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4, OE_GROUP_7	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	Bit 1 (2 or 3 level)	GPI		GPO_1
GPIO_2	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4, OE_GROUP_8	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	Bit 2 (2 or 3 level)	GPI		GPO_2
GPIO_3	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4, OE_GROUP_9	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	-	GPI		GPO_3
GPIO_4	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4, OE_GROUP_10	GOE	Bit 0, Bit 1	PERST_IN0#, PERST_IN1#, PERST_IN2#	-	GPI		GPO_4

Table 7-2. LMK3H2104 GPI/GPIO Pin Function Assignment

Pin	OE Group	Global OE	Alternative OE	7-bit I2C address	PERST#	GPI	Status output	GPO
GPI_0	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	-	Bit 0, Bit 1	PERST_IN0#	GPI	-	-

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Table 7-2. LMK3H2104 GPI/GPIO Pin Function Assignment (continued)

Pin	OE Group	Global OE	Alternative OE	7-bit I2C address	PERST#	GPI	Status output	GPO
GPI_1	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	-	Bit 0, Bit 1	PERST_IN0#	GPI	-	-
GPI_2	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	OEA	Bit 0, Bit 1	PERST_IN0#	GPI	-	-
GPIO_0	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	OEB	Bit 0, Bit 1	PERST_IN0#	GPI	DEV_INTR, CLK_READY, IN0_LOS, IN0_LOS_EVT, IN0_LOS_LMT_EVT, IN0_PERST_BUF_MODE_STAT	GPO_0
GPIO_1	OE_GROUP_0, OE_GROUP_1, OE_GROUP_2, OE_GROUP_3, OE_GROUP_4	GOE	-	Bit 0, Bit 1	PERST_IN0#	GPI		GPO_1

Output Enable Group assignment for GPI/GPIO pins is controlled by each pin's GPIx_OE_GRP_SEL/GPIOx_OE_GRP_SEL field. The function of the pin is controlled by the GPIx_FUNC/GPIOx_FUNC field. The polarity of the pin is controlled by the GPIx_POLARITY/GPIOx_POLARITY field. When a GPIO pin is configured as a status output, the corresponding status signal is selected by the field GPIO_OUT_SRC_SEL. When a GPIO is configured as a general purpose output, the output state is set by GPIO0_GPO_VAL. The output type, LVCMOS or open-drain, is set by GPIOx_OUT_SIG_TYPE.

If a GPI or GPIO pin is not used, configure the pin as a GPI. Otherwise, do not set multiple GPI/GPIO pins to share the same input function ,with the exception of dynamic OTP page selection.

Table 7-3. GPI and GPIO Input Level Read Back Registers (Normal Polarity)

Part Number	Register	Number of bits	Type	Description
LMK3H2108	GPIx_LIVE_RB (x = 0, 1, 2, 3, 4, 5)	1	RO	GPI pins input level read back • 0x0: Low • 0x1: High
LMK3H2108	GPIOx_LIVE_RB (x = 0, 1, 2)	2	RO	GPIO_0/1/2 pins input level read back • 0x0: Low (2- or 3-level) • 0x1: Mid (3-level) • 0x2: Reserved • 0x3: High (2- or 3-level)
LMK3H2108	GPIOx_LIVE_RB (x = 3, 4)	1	RO	GPIO_3/4 pins input level read back • 0x0: Low • 0x1: High
LMK3H2104	GPIx_LIVE_RB (x = 0, 1, 2)	1	RO	GPI pins input level read back • 0x0: Low • 0x1: High

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Table 7-3. GPI and GPIO Input Level Read Back Registers (Normal Polarity) (continued)

Part Number	Register	Number of bits	Type	Description
LMK3H2104	GPIO0_LIVE_RB	2	RO	GPIO_0 input level read back • 0x0: Low • 0x1: Reserved • 0x2: Reserved • 0x3: High
LMK3H2104	GPIO1_LIVE_RB	1	RO	GPIO_1 input level read back • 0x0: Low • 0x1: High

7.3.1.2 GPI/GPIO Configurations

Table 7-4. GPI Pin Configurations

Configuration	Description
GPI polarity	• 0x0: Normal polarity. Functions ending with "#" are active low, others are active high. • 0x1: Inverted polarity. Functions ending with "#" are active high, others are active low
GPI internal pull-up	• 0x0: Internal pull-up is disabled • 0x1: Internal pull-up is enabled
GPI internal pull-down	• 0x0: Internal pull-down is disabled • 0x1: Internal pull-down is enabled

Table 7-5. GPIO Pin Configurations

Configuration	Description
GPIO input type (only valid for GPIO_0, GPIO_1 and GPIO_2)	• 0x0: 2-level input • 0x1: 3-level input.
GPIO output type	• 0x0: CMOS output. No output termination is required. • 0x1: Open drain output. Requires external pull-up resistor.
GPIO polarity	• 0x0: Normal polarity. Functions with "#" are active low, others are active high. • 0x1: Inverted polarity. Functions with "#" are active high, others are active low
GPIO internal pull-up	• 0x0: Internal pull-up is disabled • 0x1: Internal pull-up is enabled
GPIO internal pull-down	• 0x0: Internal pull-down is disabled • 0x1: Internal pull-down is enabled
GPO control	Sets the output level when a GPIO pin is configured as GPO • 0x0: Output low • 0x1: Output high

The impact of GPI/GPIO polarity setting on each GPI/GPIO function is explained in the individual sections. The functions that are not described in separate sections are listed in below table.

Table 7-6. GPI/GPIO Polarity

GPIO Function	Polarity Descriptions
GPI	Polarity bit is ignored
GPO	Polarity bit is ignored

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Table 7-6. GPI/GPIO Polarity (continued)

GPIO Function	Polarity Descriptions
Bit 1 or Bit 0 of 7-bit I2C address	Normal polarity: • Low = 0 • High = 1 Inverted polarity • Low = 1 • High = 0

7.3.1.3 I2C Address Through GPI/GPIO

Bit 1 and bit 0 of the 7-bit I2C address can be set through GPI or GPIO pins. When a GPI or GPIO pin is configured to set bit 0 or bit 1 of the I2C address, the GPI or GPIO pin level overrides the bit 0 or bit 1 of the 7-bit I2C address preprogrammed in the OTP (register field I2C_TRGT_ADDR). If no GPI or GPIO pin is configured to set bit 0 or bit 1 of the I2C address, then bit 0 or bit 1 is set by I2C_TRGT_ADDR.

7.3.1.4 GPIO Pins In 3-Level Input Mode

GPIO_[2:0] can be configured to support 3-level inputs. In 3-level input mode, the mid level can be selected by floating the GPIO pin and disabling both internal pullup and internal pulldown resistors on this pin. The mid level can also be selected by forcing a mid level voltage at the pin externally. In 3-level input mode, enabling internal pullup or pulldown resistor on the GPIO pin does not select high or low, and the pin must be pulled or driven high or low externally. GPIO pins are configured as 3-level inputs by setting GPIOx_NUM_IN_LVL.

When GPIO_[2:0] are configured as 2-level inputs, the above limitations do not apply, and the internal pullup and pulldown resistors function normally.

7.3.1.5 GPI/GPIO Internal Pullup And Pulldown

For any GPI pin, when the internal pullup resistor is enabled, the pin is pulled to 1.8V regardless of GPI pin supply voltage. When the internal pullup resistor is enabled and the pin is not pulled low or driven low externally, the GPI pin is detected high. When pulling or driving GPI pins externally, user must still follow the VIH/VIL requirements specified in the Electrical Characteristics table.

For GPIO pins, when internal pullup resistor is enabled, the pin is pulled to VDDD supply voltage normally.

The internal pullup is controlled by GPIx_PULL_UP_EN/GPIOx_PULL_UP_EN, and the internal pulldown is controlled by GPIx_PULL_DN_EN/GPIOx_PULL_DN_EN.

7.3.2 OTP

7.3.2.1 OTP Overview

Both LMK3H2108 and LMK3H2104 support LMK3H2104 supports preprogrammable configurations via OTP. The OTP is divided into a 'base' section, and a 'page' section which is divided into 4 pages. Fields that are mapped to the 'base' section are always loaded from the 'base' section, while fields that are mapped to the 'page' section are loaded from one of the 4 pages. Below is a list of register categories that are mapped to the 'page' section.

- Frequency settings
- Preprogrammed SSC Modulation Depth: Custom, -0.1%, -0.25%, -0.3%, -0.5%.
- Output format settings
- Output disable states
- Individual output enable (not including global OE and single LVCMOS OE)
- Output MUX and divider settings
- Block power down bits, including the related registers for the device to operate in buffer only mode
- 7-bit I2C address
- GPIO functions, not including status output signal selection
- Selection between IN_[2:0] and GPI_[5:0] for INx/GPI pins

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- Selection between INx_P and INx_N for single-ended input clock
- GPI functions

7.3.2.2 OTP Page Selection

For LMK3H2108, each OTP page is selected using three 3-level values, PAGE_SEL_2, PAGE_SEL_1, and PAGE_SEL_0. Each of these three values is encoded as a 2-bit value, such that the full OTP page selection code for each page is represented as a 6-bit value.

Table 7-7. LMK3H2108 OTP Page Selection Mapping Code

OTP Page x PAGE_SEL	Descriptions
PAGE_SEL_2	OTP_SEL_2 level to select this OTP page • 0x0: OTP_SEL_2 must be Low • 0x1: OTP_SEL_2 must be Mid • 0x2: Don't care. OTP_SEL_2 can be any level • 0x3: OTP_SEL_2 must be High
PAGE_SEL_1	OTP_SEL_1 level to select this OTP page • 0x0: OTP_SEL_1 must be Low • 0x1: OTP_SEL_1 must be Mid • 0x2: Don't care. OTP_SEL_1 can be any level • 0x3: OTP_SEL_1 must be High
PAGE_SEL_0	OTP_SEL_0 level to select this OTP page • 0x0: OTP_SEL_0 must be Low • 0x1: OTP_SEL_0 must be Mid • 0x2: Don't care. OTP_SEL_0 can be any level • 0x3: OTP_SEL_0 must be High

Table 7-8. LMK3H2108 OTP_SEL_[2:0] Levels

OTP_SEL	Descriptions
OTP_SEL_2	If GPIO_2 is configured as dynamic OTP select, then OTP_SEL_2 is the live input level of GPIO_2. Otherwise OTP_SEL_2 = OTP_PAGE_SEL_PU_2
OTP_SEL_1	If GPIO_1 is configured as dynamic OTP select, then OTP_SEL_1 is the live input level of GPIO_1. Otherwise OTP_SEL_1 = OTP_PAGE_SEL_PU_1
OTP_SEL_0	If GPIO_0 is configured as dynamic OTP select, then OTP_SEL_0 is the live input level of GPIO_0. Otherwise OTP_SEL_0 = OTP_PAGE_SEL_PU_0

If OTP_SEL_[2:0] do not point to a valid OTP page, then the GPIO_[2:0] (if configured as dynamic OTP select) level change is ignored and OTP page is not changed.

Table 7-9. OTP Page Selection At Power-Up

Register	LMK3H2108	LMK3H2104
OTP_PAGE_SEL_PU_2	OTP_SEL_2 level at power-up • 0x0 = Low • 0x1 = Mid • 0x2 = GPIO_2 input level at power-up • 0x3 = High If GPIO_2 is configured as dynamic OTP_SEL, then OTP_PAGE_SEL_PU_2 must be set to 0x2 If OTP_PAGE_SEL_PU_2 is set to 0x2, then GPIO_2 must be configured as dynamic OTP_SEL	Reserved

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Table 7-9. OTP Page Selection At Power-Up (continued)

Register	LMK3H2108	LMK3H2104
OTP_PAGE_SEL_PU_1	OTP_SEL_1 level at power-up • 0x0 = Low • 0x1 = Mid • 0x2 = GPIO_1 input level at power-up • 0x3 = High If GPIO_1 is configured as dynamic OTP_SEL, then OTP_PAGE_SEL_PU_1 must be set to 0x2 If OTP_PAGE_SEL_PU_1 is set to 0x2, then GPIO_1 must be configured as dynamic OTP_SEL	In OTP mode (Pin 23 = High), both OTP_PAGE_SEL_PU_1 and OTP_PAGE_SEL_PU_0 must be set to 0x2 In I2C mode (Pin 23 = Low) where only one OTP page is available, OTP_PAGE_SEL_PU_[1:0] determine the available OTP page
OTP_PAGE_SEL_PU_0	OTP_SEL_0 level at power-up • 0x0 = Low • 0x1 = Mid • 0x2 = GPIO_0 input level at power-up • 0x3 = High If GPIO_0 is configured as dynamic OTP_SEL, then OTP_PAGE_SEL_PU_0 must be set to 0x2 If OTP_PAGE_SEL_PU_0 is set to 0x2, then GPIO_0 must be configured as dynamic OTP_SEL	

For LMK3H2108, not all 3 pins (GPIO_0, 1 and 2) need to be configured as dynamic OTP page selection at the same time. Dynamic OTP page selection can be done with 1, 2 or 3 pins out of GPIO_[2:0].

Table 7-10. LMK3H2104 OTP Page Selection

OTP_SEL_1 (Pin 5)	OTP_SEL_1 (Pin 4)	Selected OTP Page
Low	Low	0
Low	High	1
High	Low	2
High	High	3

7.3.2.3 OTP Page Selection Pin Polarity

Below table explains the effect of GPIO pin polarity when the GPIO is configured as dynamic OTP selection.

Table 7-11. LMK3H2108 OTP Page Selection Pin Polarity

GPIO Configuration	Polarity Description
2-level dynamic OTP select	• Normal polarity: – GPIO_x Low = OTP_SEL_x Low – GPIO_x High = OTP_SEL_x High • Inverted polarity: – GPIO_x Low = OTP_SEL_x High – GPIO_x High = OTP_SEL_x Low x = 0, 1, 2
3-level dynamic OTP select	GPIO polarity is ignored

7.3.2.4 Dynamic OTP Page Change

When OTP page is changed dynamically:

- Before switching OTP page, all outputs are disabled to the current "output disable states". The disable process can be synchronous or asynchronous depending on the output sync settings
- All outputs stay in these states throughout the OTP change process

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- After the new OTP is loaded:
  - If the output format is changed, then disable the outputs to the new disable states based on the output format and preprogrammed output disable states
  - If the output format is unchanged:
    - If the output disable states in the new OTP page are different than before, then change the output disable states according to the new OTP page, and the outputs stay muted
    - If the output disable states in the new OTP page are the same with before, then outputs stay muted to the disable states
- After the device is ready and OE is asserted, outputs are enabled synchronously or asynchronously depending on the sync settings

If the dynamic OTP select pins are level changed while the device is in low power mode via PWRDN# pin, then the new OTP configuration is loaded upon PWRDN# deassertion.

If the clock source of BANKx is different across OTP pages, then BANKx_SWITCHOVER_FRC_CLK_EN must be set to 1 for dynamic OTP page change. If the clock source of BANKx is the same across OTP pages, then BANKx_SWITCHOVER_FRC_CLK_EN can be set to 0.

If the clock source of BANKx is FOD0, FOD1 or edge combiner in OTP page A, and the clock source of BANKx is INy in OTP page B, then the clock signal at INy must be valid when the OTP page is changed from A to B dynamically, otherwise the clock source of BANKx does not switch to INy properly.

7.3.2.5 Dynamic OTP Page Change Timing

OTP page selection debounce time sets the amount of time that all dynamic OTP page selection pins must be stable before the device responds to a level change on any dynamic OTP page selection pin. Once all active dynamic OTP page selection pins have been stable for the selected amount of time, the resulting OTP Page selection code is registered and the selected page is loaded into the device registers.

Table 7-12. OTP Page Selection Debounce Time

BOOTOSC_CLK_DIS	OTP_PAGE_SEL_DYN_DEBOUNCE	OTP page selection debounce time
0x0	0x0	120ns
0x0	0x1	4.2µs
0x1	0x0	60ns
0x1	0x1	2.1µs

After the OTP page is changed, a subsequent OTP page change must not occur within 300µs.

7.3.3 PWRGD/PWRDN#

7.3.3.1 PWRGD/PWRDN# Function Assignment

- LMK3H2108: PWRGD/PWRDN# function can be assigned to GPI_2, GPI_3, GPI_4, GPI_5, GPIO_0, GPIO_1, GPIO_2, GPIO_3 or GPIO_4. If left unassigned, PWRGD/PWRDN function is disabled.
- LMK3H2104: PWRGD/PWRDN# function can be assigned to GPI_2, GPIO_0 or GPIO_1. If left unassigned, PWRGD/PWRDN function is disabled.

If PWRGD/PWRDN# function is assigned to a GPI/GPIO pin, then the VDD pin that powers this GPI/GPIO pin cannot be set to floating.

7.3.3.2 PWRGD

Device is powered up after PWRGD (Power Good) assertion. See Power Up Sequence section for details.

PWRGD polarity cannot be changed. PWRGD function is active high regardless of the GPIO polarity setting.

7.3.3.3 PWRDN#

After PWRGD assertion, PWRGD/PWRDN# pin becomes a PWRDN# (Power Down, active low) pin. Subsequent high/low transitions make the device enter or exit PWRDN# mode. There are 3 PWRDN# modes:

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- Dynamic OTP select based power-down mode (only applies to LMK3H2108). This mode is selected if both conditions are met:
  - PWRGD/PWRDN# function is assigned to GPIO_0, GPIO_1 or GPIO_2
  - PWRGD/PWRDN# pin is also configured as a 2-level dynamic OTP select pin

  When PWRDN# is asserted, device enters power-down mode by loading the OTP page selected by all dynamic OTP select pins including the PWRDN# pin. In this "power-down mode OTP page", user can power down certain blocks, disable output drivers and decide output disable states.

  When PWRDN# is deasserted, device exits power-down mode by loading the OTP page selected by all dynamic OTP select pins including the PWRDN# pin.

  In this mode, the GPIO pin with PWRDN# function must be programmed to normal polarity.
- Low power mode. In low power mode, when PWRDN# is asserted, most blocks are powered down to save power. Output banks are powered down and outputs are in tristate. Register values are unchanged. BAW is not automatically powered down in this mode and BAW_PD needs to be manually set to '1' through I2C to further save power, if needed.
- Reset mode. In reset mode, toggling PWRDN# pin is equivalent to restarting the power-up sequence. PWRDN# assertion powers down the device and disables all outputs to tristate. PWRDN# deassertion starts the power-up sequence.

PWRDN# function is always active low, regardless of GPI/GPIO polarity setting.

In dynamic OTP select based power-down mode, below blocks can be powered down through OTP registers.

Table 7-13. Power Down Controls

Part Number	Register	Description
LMK3H2108 or LMK3H2104	PDN	Power down the device. The function of this register is affected by PIN_SAMPLE_DIS and OTP_AUTOLOAD_DIS
LMK3H2108 or LMK3H2104	BAW_PD	Power down the BAW and BAW related circuits
LMK3H2108 or LMK3H2104	FOD_0_PD	Power down FOD_0.
LMK3H2108 or LMK3H2104	FOD_1_PD	Power down FOD_1
LMK3H2108 or LMK3H2104	IN0_PD	Power down IN0
LMK3H2108	IN1_PD	Power down IN1
LMK3H2108	IN2_PD	Power down IN2

To minimize the power of unused output drivers, set OUTx_DIS_STATE = 3 (Hi-Z/Hi-Z).

Besides low power mode and reset mode, more flexibility can be achieved through below registers.

Table 7-14. Power Down Mode Registers

Register	Description
PIN_RESAMPLE_DIS	Pin re-sample disable. • LMK3H2104: – 0x0: when the device exits power-down mode (the PWRDN# pin is deasserted or the PDN register field is written to 0x0), the REF_0/CTRL pin is re-sampled to determine the device operation mode. – 0x1: The pin re-sampling does not occur, and the last sampled value of the REF_0/CTRL pin is retained. • LMK3H2108: This register has no impact.

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Table 7-14. Power Down Mode Registers (continued)

Register	Description
OTP_AUTOLOAD_DIS	OTP Autoload Disable. By default, when the device exits power-down mode (the PWRDN# pin is deasserted or the PDN register field is written to 0x0), OTP data is loaded into the device registers. However, if OTP_AUTOLOAD_DIS has a value of 0x1 while exiting power-down mode, this data transfer does not occur. The OTP_AUTOLOAD_DIS register field has no effect on dynamic OTP page changes.

Table 7-15. Power Down Mode Registers And Device Behaviors

PIN_SAMPLE_DIS	OTP_AUTOLOAD_DIS	Device behaviors when PWRDN# is toggled
0x0	0x0	Reset mode, full. Toggling PWRDN# pin is equivalent to a full power cycle.
0x0	0x1	Reset mode, no OTP Autoload. Toggling PWRDN# pin resets the device, but register values are preserved.
0x1	0x0	Reset mode, no pin re-sampling. Registers are reloaded from OTP, but REF_0/CTRL pin is not re-sampled and the device operation mode of LMK3H2104 is unchanged.
0x1	0x1	Low power mode. Logic input pins are not re-sampled and no OTP content is loaded into registers. Register values are unchanged. When PWRDN# is asserted, output banks are powered down and outputs are held in tristate.

7.3.4 Power Supply

7.3.4.1 Power Supply Pin Mapping

Table 7-16. LMK3H2108 Power Supply Pin Mapping

Pin Name	Assigned Blocks	Supply Voltage	Supply Voltage Impact
VDDA	BAW, FOD_0, FOD_1	1.8, 2.5 or 3.3V	N/A
VDDD	I2C, GPIO_[4:0], OTP and other digital blocks	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	VIH and VIL of GPIO_[4:0], SCL and SDA follow VDDD voltage. See Specifications for details.
VDDR	IN1, IN2, GPI_[5:2]	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	VIH and VIL of GPI_[5:2] follow VDDR voltage. IN1 and IN2 CMOS clock input level can be 1.8, 2.5 or 3.3V regardless of VDDR voltage. See Specifications for details.
VDDX	IN0, GPI_[1:0]	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	VIH and VIL of GPI_[1:0] follow VDDX voltage. IN0 CMOS clock input level can be 1.8, 2.5 or 3.3V regardless of VDDX voltage. See Specifications for details.
VDDO_0	OUT0 driver, channel divider, MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT0 CMOS clock output level follows VDDO_0 voltage, except for 1.2V CMOS. See Specifications for details.
VDDO_1_2	OUT1 and OUT2 driver, channel divider, MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT1 and OUT2 CMOS clock output level follows VDDO_1_2 voltage, except for 1.2V CMOS. See Specifications for details.
VDDO_3_4	OUT3 and OUT4 driver, channel divider, MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT3 and OUT4 CMOS clock output level follows VDDO_3_4 voltage, except for 1.2V CMOS. See Specifications for details.
VDDO_5	OUT5 driver, channel divider, MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT5 CMOS clock output level follows VDDO_5 voltage, except for 1.2V CMOS. See Specifications for details.
VDDO_6	OUT6 driver, channel divider, MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT6 CMOS clock output level follows VDDO_6 voltage, except for 1.2V CMOS. See Specifications for details.

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Table 7-16. LMK3H2108 Power Supply Pin Mapping (continued)

Pin Name	Assigned Blocks	Supply Voltage	Supply Voltage Impact
VDDO_7	OUT7 driver, channel divider, MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT7 CMOS clock output level follows VDDO_7 voltage, except for 1.2V CMOS. See Specifications for details.

Table 7-17. LMK3H2104 Power Supply Pin Mapping

Pin Name	Assigned Block	Supply Voltage	Supply Voltage Impact
VDDA	BAW, FOD_0, FOD_1 REF1 channel divider and MUX	1.8, 2.5 or 3.3V.	N/A
VDDD	GPI_2, I2C, OTP_SEL[1:0], GPIO_[1:0], OTP and other digital blocks	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	VIH and VIL of GPI_2, OTP_SEL[1:0], SCL, SDA and GPIO_[1:0] follow VDDD voltage. See Specifications for details.
VDDO_0	OUT0 driver, channel divider and MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT0 CMOS clock output level follows VDDO_0 voltage, except for 1.2V CMOS. See Specifications for details.
VDDO_1	OUT1 driver, channel divider and MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT1 CMOS clock output level follows VDDO_1 voltage, except for 1.2V CMOS. See Specifications for details.
VDDO_2	OUT2 driver, channel divider and MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT2 CMOS clock output level follows VDDO_2 voltage, except for 1.2V CMOS. See Specifications for details.
VDDO_3	OUT3 driver, channel divider and MUX REF0 channel divider and MUX	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	OUT3 CMOS clock output level follows VDDO_3 voltage, except for 1.2V CMOS. See Specifications for details. To use REF0 for LVCMOS clock output, VDDO_3 must be connected to power.
VDD_REF	GPI_[1:0], IN0, CTRL, REF_0 and REF_1 output driver	1.8, 2.5 or 3.3V, regardless of VDDA voltage and other VDD pin voltages	VIH and VIL of GPI_[1:0] follow the VDD_REF voltage. IN0 CMOS clock input level can be 1.8, 2.5 or 3.3V regardless of VDD_REF voltage. VIH and VIL of CTRL (Pin 15) follow the VDD_REF voltage. REF_0 and REF_1 LVCMOS clock output voltage levels follow the VDD_REF voltage. See Specifications for details.

7.3.4.2 Unused Power Supply Pins

VDDD, VDDA and VDD_REF must be connected to power supply. Other VDD pins can be left floating if unused. The registers must be set through OTP for proper power-up sequence.

Table 7-18. LMK3H2108 Registers For Floating VDD Pins

Register	Description
FLOAT_VDDR	• 0x0: VDDR pin must be connected to a power rail • 0x1: GPI_[5:2] and IN[2:1] are unused. VDDR pin can be left floating
FLOAT_VDDX	• 0x0: VDDX pin must be connected to a power rail • 0x1: GPI_[1:0] and IN0 are unused. VDDX pin can be left floating
FLOAT_VDDO_0	• 0x0: VDDO_0 pin must be connected to a power rail • 0x1: OUT0 is unused. VDDO_0 pin can be left floating
FLOAT_VDDO_1_2	• 0x0: VDDO_1_2 pin must be connected to a power rail • 0x1: OUT1 and OUT2 are unused. VDDO_1_2 pin can be left floating

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Table 7-18. LMK3H2108 Registers For Floating VDD Pins (continued)

Register	Description
FLOAT_VDDO_3_4	• 0x0: VDDO_3_4 pin must be connected to a power rail • 0x1: OUT3 and OUT4 are unused. VDDO_3_4 pin can be left floating
FLOAT_VDDO_5	• 0x0: VDDO_5 pin must be connected to a power rail • 0x1: OUT5 is unused. VDDO_5 pin can be left floating
FLOAT_VDDO_6	• 0x0: VDDO_6 pin must be connected to a power rail • 0x1: OUT6 is unused. VDDO_6 pin can be left floating
FLOAT_VDDO_7	• 0x0: VDDO_7 pin must be connected to a power rail • 0x1: OUT7 is unused. VDDO_7 pin can be left floating

Table 7-19. LMK3H2104 Registers For Floating VDD Pins

Register	Description
FLOAT_VDDO_0	• 0x0: VDDO_0 pin must be connected to a power rail • 0x1: OUT0 is unused. VDDO_0 pin can be left floating
FLOAT_VDDO_1	• 0x0: VDDO_1 pin must be connected to a power rail • 0x1: OUT1 is unused. VDDO_1 pin can be left floating
FLOAT_VDDO_2	• 0x0: VDDO_2 pin must be connected to a power rail • 0x1: OUT2 is unused. VDDO_2 pin can be left floating
FLOAT_VDDO_3	• 0x0: VDDO_3 pin must be connected to a power rail • 0x1: OUT3 is unused. VDDO_3 pin can be left floating

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7.3.5 Power Up Sequence

7.3.5.1 Power Up Sequence

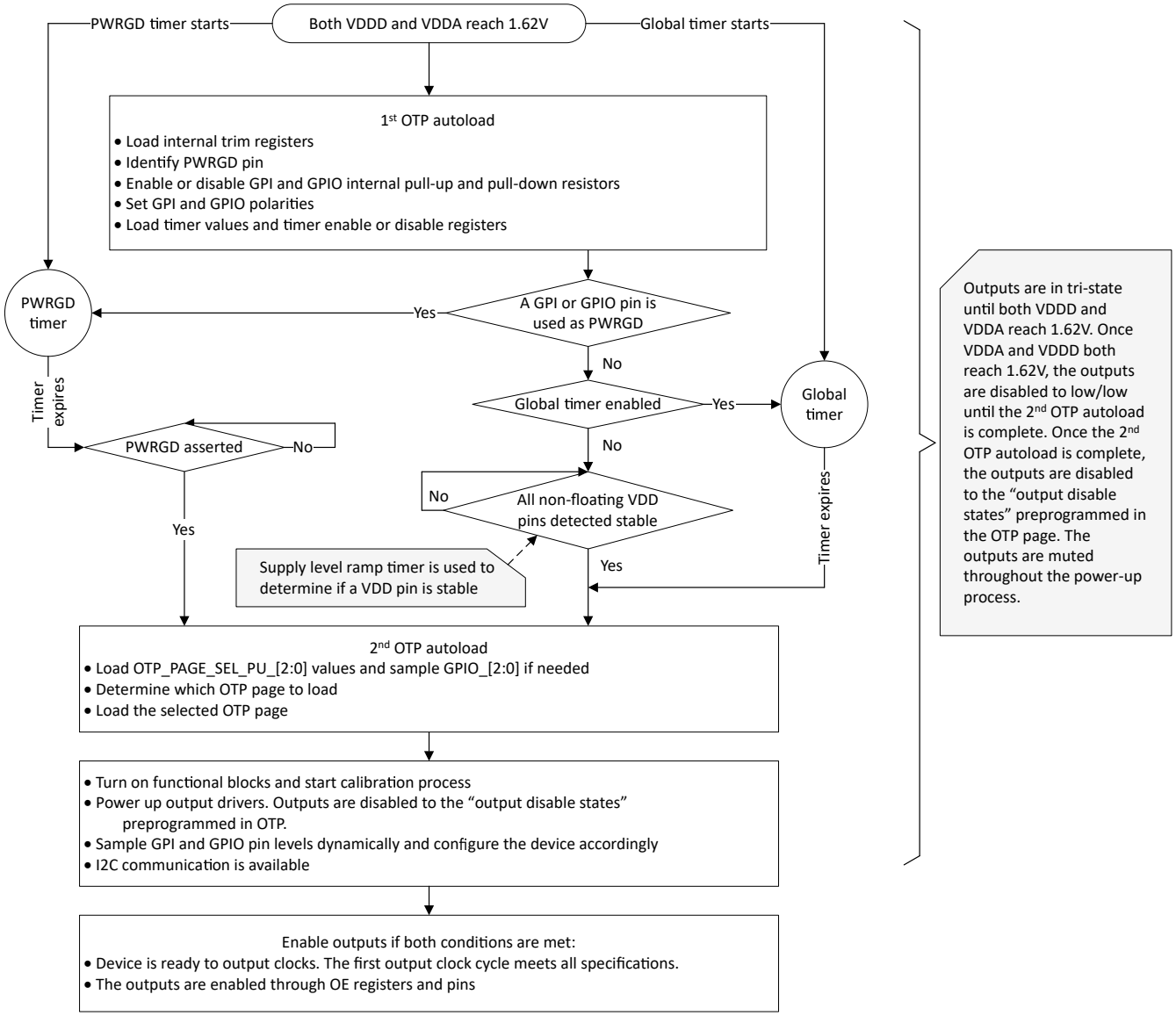


Figure 7-3. LMK3H2108 Power Up Sequence

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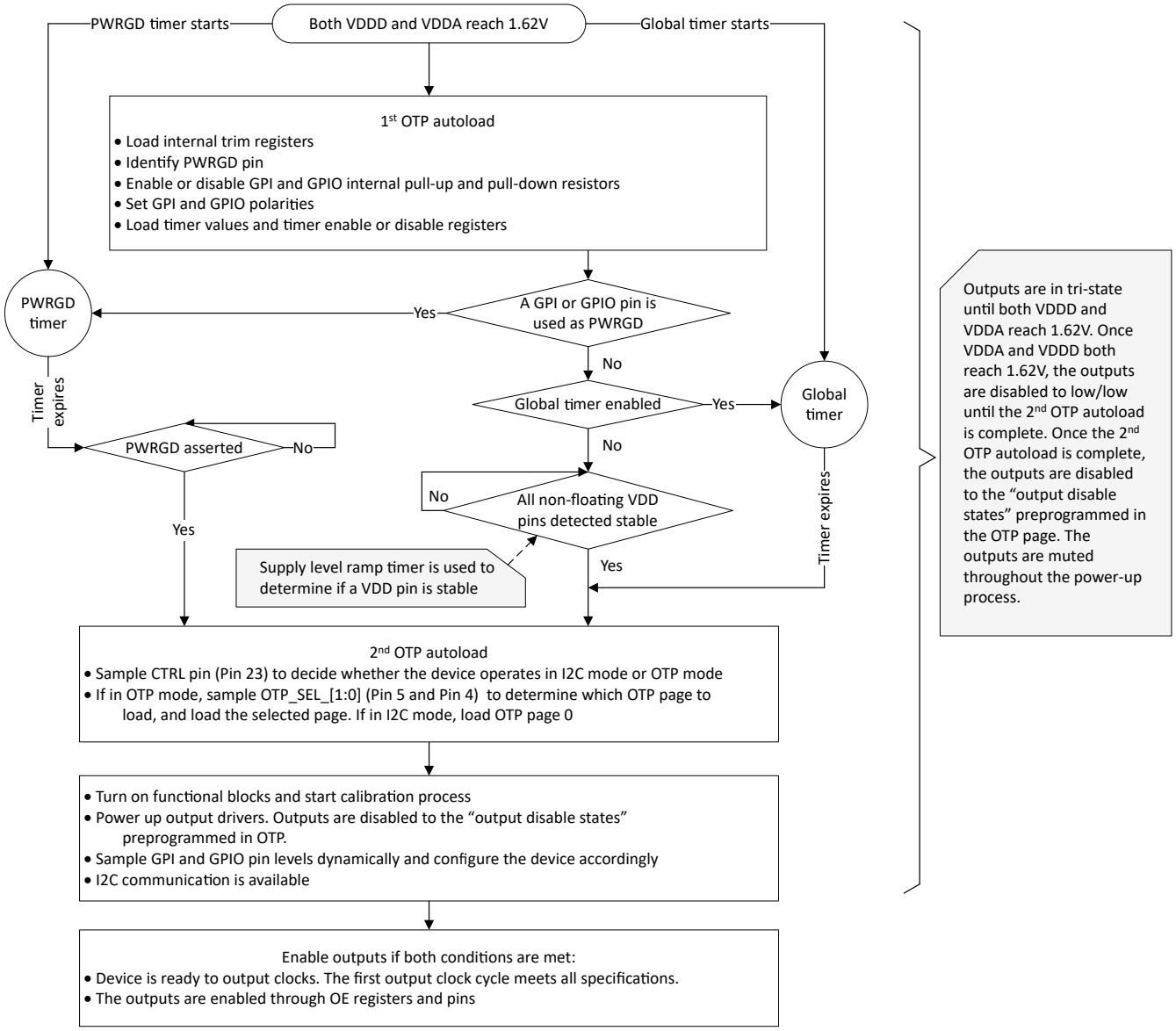


Figure 7-4. LMK3H2104 Power Up Sequence

Table 7-20. Timer descriptions

Timer	Descriptions
PWRGD timer	PWRGD timer is used to delay the sampling of PWRGD pin at power-up. This timer is useful when the PWRGD pin is tied to a power rail or control device which takes time to stabilize. User must make sure that the PWRGD input level is ready to be sampled before PWRGD timer expires.
Supply level ramp timer	The voltage level of each VDD pin is interpreted internally as 0b00 (VDDx <1.8V), 0b01 (VDDx = 1.8V), 0b10 (VDDx = 2.5V) or 0b11 (VDD = 3.3V). A VDD pin is detected stable if either of below conditions is met: • VDDx voltage level is 0b11 • VDDx voltage level is 0b01 or 0b10, and the supply level ramp timer expires. The supply level ramp timer starts when VDDx voltage reaches 1.62V. The value of the supply level ramp timer is the same for all VDD pins and must be programmed according to the longest expected power supply ramp-up time, measured from 1.62V to the final voltage

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Table 7-20. Timer descriptions (continued)

Timer	Descriptions
Global supply detect timer	Global supply detect timer exists so that if a VDD pins fails to be detected stable, the device does not wait indefinitely and still powers up when the timer expires. This timer can be enabled or disabled though OTP register. • When disabled, the device does not power up until all the non-floating VDD pins are detected stable • When enabled, the device powers up when the global timer expires, or all the non-floating VDD pins are detected stable, whichever comes first

Table 7-21. Timer range and resolution

Timer	Timer starting point	Resolution	Range
PWRGD timer	VDDA and VDDD both reach 1.62V	0.1ms	0.1ms to 25.6ms
Global timer	VDDA and VDDD both reach 1.62V	0.1ms	0.1ms to 25.6ms
Individual VDDx timer	VDDx reaches 1.62V	0.1ms	0.1ms to 6.4ms

7.3.6 Output Enable And Disable

7.3.6.1 OE Registers

Each output (including REF_0 and REF_1 for LMK3H2104) has a dedicated output disable register bit that can be accessed through I2C. OUTx is disabled when OUTx_DIS = 1; OUTx is enabled when OUTx_DIS = 0. REF_0 and REF_1 can be enabled or disabled through REFx_DIS.

There is a global OE bit to enable or disable all outputs, except for the outputs that are excluded from global OE.

7.3.6.2 OE Group Assignment

Each output can be assigned to an OE group using OUTx_OE_GRP. GPI/GPIO pins can enable or disable one or more outputs when configured as an OE group pin.

- Outputs that can be assigned to an OE group:
  - LMK3H2108: OUT0, OUT1, OUT2, OUT3, OUT4, OUT5, OUT6, OUT7
  - LMK3H2104: OUT0, OUT1, OUT2, OUT3, REF_0, REF_1
- When an output is not assigned to an OE group, the output can be either of the following:
  - Not controlled by any OE group but controlled by global OE bit and global OE pin
  - Not controlled by any OE group and excluded from global OE bit and global OE pin

Each OE group can only be controlled by one GPI or GPIO pin. Configuring 2 or more GPI/GPIO pins to control the same OE group is not allowed.

7.3.6.3 OE AND Logic

The output enable function follows AND logic. An output is enabled if all active output enable logic contributors are in the 'enabled' state. An output is disabled if any one active output enable logic contributor is in the 'disabled' state. The output enable logic contributors are:

- Individual Output Disable register field
- Global Output Enable register field (Active only if the corresponding OUTx_OE_GRP register field is not set to 'Not assigned. Not affected by global output enable controls.' Never active when the 'Alternative OE' feature is enabled.)
- Global Output Enable pin (Active only if a GPI/GPIO pin has been assigned the 'Global OE Pin' function, and the corresponding OUTx_OE_GRP register field is not set to 'Not assigned. Not affected by global output enable controls.' Never active when the 'Alternative OE' feature is enabled.)
- Output Enable Group pin (Active only if a GPI/GPIO pin has been assigned the 'OE Group' function, and the corresponding OUTx_OE_GRP register field is set to the same OE Group as that pin. Never active when the 'Alternative OE' feature is enabled.)
- Alternative OE pin (LMK3H2104 only. Active only if the Alternative OE feature is enabled (GPI2 and GPIO0 have both been assigned with the 'Alternative OE' function))

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7.3.6.4 Alternative OE

For LMK3H2104, when both GPI_2 and GPIO_0 are configured as alternative OE, the output behaviors are described in below tables.

GPI_2 = OEA, GPIO_0 = OEB

Table 7-22. Alternative OE Mapping 1 (ALTERNATE_OE_SEL = 0)

OE[B:A]	OUT0	OUT1	OUT2	OUT3	REF_0	REF_1
00	Enabled	Disabled	Enabled	Disabled	Enabled	Enabled
01	Enabled	Enabled	Disabled	Disabled	Enabled	Enabled
10	Disabled	Disabled	Enabled	Enabled	Enabled	Enabled
11	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

Table 7-23. Alternative OE Mapping 2 (ALTERNATE_OE_SEL = 1)

OE[B:A]	OUT0	OUT1	OUT2	OUT3	REF_0	REF_1
00	Enabled	Disabled	Disabled	Disabled	Enabled	Enabled
01	Enabled	Enabled	Disabled	Disabled	Enabled	Enabled
10	Enabled	Enabled	Enabled	Disabled	Enabled	Enabled
11	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

If alternative OE is enabled, the following contributors are never considered in the output enable logic:

- Global Output Enable register field
- Global Output Enable pin
- Output Enable Group pin

When alternative OE is enabled, the outputs must be configured as "No OE Group".

4.2µs debounce time is added to allow dynamically changing OEA and OEB.

7.3.6.5 OE Polarity

OE registers are always active high. OE pin polarity is decided by the GPI/GPIO pin polarity, as shown below.

Table 7-24. GPI/GPIO Polarity For OE

GPI/GPIO configuration	GPI/GPIO polarity
OE_GROUP_x	• Normal polarity: Active high – Low: Disable outputs – High: Enable outputs • Inverted polarity: Active low – Low: Enable outputs – High: Disable outputs
Global OE	
Alternative OE	GPI/GPIO polarity is ignored

7.3.6.6 Single LVCMOS OE

When an output is set to any LVCMOS format, OUTx_P and OUTx_N can be enabled or disabled separately through single LVCMOS OE bits OUTxP_OE_CMOS and OUTxN_OE_CMOS. If OUTx_P or OUTx_N is enabled or disabled through single LVCMOS OE bit, OUTx_N or OUTx_P is uninterrupted. The enable and disable process is either synchronous or asynchronous, set by SINGLE_CMOS_EN_SYNC.

For differential outputs, OUTxP_OE_CMOS and OUTxN_OE_CMOS must both be set to 1.

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7.3.6.7 LOS And Output Behaviors

When INx stops at High/Low and LOS = 1, the output clock stops at High/Low. When INx comes back and LOS = 0, the output clock briefly goes Low/High, then the programmed disable state (only if the Automatic Output Disable feature is enabled), then starts toggling again.

If LOS is disabled, then the above behaviors do not occur. When INx stops at High/Low or Low/High, the output clock also stops at High/Low or Low/High. When INx comes back, the output clock starts toggling again.

7.3.7 PERST#

7.3.7.1 PERST# Buffer Mode

PERST# (PCIe Reset Active Low) buffer mode allows user to switch between clock gen mode and bypass buffer mode based on the validness of input clocks as well as the PERST# signal provided at a GPI or GPIO pin.

To enable PERST# buffer mode, register BANKx_SWITCHOVER_FRC_CLK_EN must be set to 0

Table 7-25. PERST_INx# Polarity

GPI/GPIO function	GPI/GPIO Polarity
PERST_IN0#	Regular PERST# buffer mode: • Normal polarity – When PERST_INx# is low, the device enters buffer mode when input clock is valid, and enters clock gen mode when input clock is invalid – When PERST_INx# is high, the device operation mode does not change • Inverted polarity – When PERST_INx# is high, the device enters buffer mode when input clock is valid, and enters clock gen mode when input clock is invalid – When PERST_INx# is low, the device operation mode does not change Level triggered PERST# buffer mode: • Normal polarity: – When PERST_INx is low and INx clock is valid, the device enters buffer mode – When PERST_INx is high or INx clock is invalid, the device enters clock gen mode • Inverted polarity: – When PERST_INx is high and INx clock is valid, the device enters buffer mode – When PERST_INx is low or INx clock is invalid, the device enters clock gen mode
PERST_IN1#	
PERST_IN2#	

Table 7-26. Regular PERST# buffer mode truth table (normal polarity)

PERST#	LOS	Device operation mode
L	L	Buffer mode
L	H	Clock gen mode
H	L	Previous mode
H	H	Previous mode

Table 7-27. Regular PERST# buffer mode truth table in transition (normal polarity)

PERST#	LOS	Device operation mode
H	L to H	Previous mode
H	H to L	Previous mode
L to H	L	Buffer mode
L to H	H	Clock gen mode
L	L to H	Buffer mode to clock gen mode
L	H to L	Clock gen mode to buffer mode
H to L	L	Previous mode to buffer mode
H to L	H	Previous mode to clock gen mode

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Table 7-28. Level triggered PERST# buffer mode truth table (normal polarity)

PERST#	LOS	Device operation mode
L	L	Buffer mode
L	H	Clock gen mode
H	L	Clock gen mode
H	H	Clock gen mode

If the device operates in buffer mode but the input clock is gone, then the outputs are disabled to the programmed disable states.

With inverted polarity, the "H" and "L" of PERST# are swapped in all the truth tables.

Table 7-29. PERST# Buffer Mode Registers

Register	Type	Description
PERST_BUF_INx (x = 0, 1, 2)	RW	PERST buffer mode INx setting • 0x0: PERST# buffer mode is disabled for INx. Output banks that choose INx in PERST# buffer mode select the clock source according to output bank MUX settings instead. • 0x1: Regular PERST# buffer mode is enabled • 0x2: Level triggered PERST# buffer mode is enabled • 0x3: INx buffer mode is always enabled regardless of PERST_INx# state.
PERST_BUF_BANKx (x = 0, 1, 2, 3, 4 or 5)	RW	PERST Buffer mode BANKx setting • 0x0: Normal operation mode. BANKx selects the clocking source according to BANKx MUX setting • 0x1: BANKx selects IN0 in buffer mode • 0x2: BANKx selects IN1 in buffer mode • 0x3: BANKx selects IN2 in buffer mode
PERST_BUF_INx_STS (x = 0, 1 or 2)	RO	PERST_INx buffer mode status readback. The value of this register can also be passed to a GPIO pin • 0x0: INx is not passed to any output bank through PERST buffer mode. However, INx can be passed to output banks through normal output bank MUX settings if PERST buffer mode is disabled • 0x1: INx is passed to output banks through buffer mode.
PERST_BUF_INx_LOS_EN (x = 0, 1, 2)	RW	• 0x0: In PERST buffer mode, LOS_x status is ignored. Input clock is always assumed valid and LOS_x is "L" in all the related truth tables. • 0x1: In PERST buffer mode, LOS_x status is used.

Table 7-30. PERST_BUF_BANKx And PERST_BUF_INx Mapping

PERST_BUF_BANKx	PERST_BUF_IN0	PERST_BUF_IN1	PERST_BUF_IN2	BANKx clock source
0x0	x	x	x	Decided by BANKx_CLK_SEL
0x1	0x0	x	x	Decided by BANKx_CLK_SEL
0x1	0x1	x	x	Selects IN0 when buffer mode is active
0x1	0x2	x	x	Selects IN0 when buffer mode is active
0x1	0x3	x	x	Always selects IN0
0x2	x	0x0	x	Decided by BANKx_CLK_SEL
0x2	x	0x1	x	Selects IN1 when buffer mode is active
0x2	x	0x2	x	Selects IN1 when buffer mode is active
0x2	x	0x3	x	Always selects IN1
0x3	x	x	0x0	Decided by BANKx_CLK_SEL
0x3	x	x	0x1	Selects IN2 when buffer mode is active

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Table 7-30. PERST_BUF_BANKx And PERST_BUF_INx Mapping (continued)

PERST_BUF_BANKx	PERST_BUF_IN0	PERST_BUF_IN1	PERST_BUF_IN2	BANKx clock source
0x3	x	x	0x2	Selects IN2 when buffer mode is active
0x3	x	x	0x3	Always selects IN2

Table 7-31. PERST_BUF_INx_STS Mapping

PERST_BUF_BANKx	PERST_BUF_INx	PERST_BUF_INx_STS
0x0 for all banks	x	PERST_BUF_IN0_STS = 0x0 PERST_BUF_IN1_STS = 0x0 PERST_BUF_IN2_STS = 0x0
x	PERST_BUF_IN0 = 0x0	PERST_BUF_IN0_STS = 0x0
x	PERST_BUF_IN1 = 0x0	PERST_BUF_IN1_STS = 0x0
x	PERST_BUF_IN2 = 0x0	PERST_BUF_IN2_STS = 0x0
0x1 for at least 1 bank	PERST_BUF_IN0 = 0x1, 0x2 or 0x3	• If IN0 is not passed to output banks, then PERST_BUF_IN0_STS = 0x0 • If IN0 is passed to output banks through buffer mode, then PERST_BUF_IN0_STS = 0x1
0x2 for at least 1 bank	PERST_BUF_IN1 = 0x1, 0x2 or 0x3	• If IN1 is not passed to output banks, then PERST_BUF_IN1_STS = 0x0 • If IN1 is passed to output banks through buffer mode, then PERST_BUF_IN1_STS = 0x1
0x3 for at least 1 bank	PERST_BUF_IN2 = 0x1, 0x2 or 0x3	• If IN2 is not passed to output banks, then PERST_BUF_IN2_STS = 0x0 • If IN2 is passed to output banks through buffer mode, then PERST_BUF_IN2_STS = 0x1

7.3.7.2 PERST# Latching

After PERST# input is latched, the latch is cleared after any of below.

- PWRDN# function is set to reset mode and PWRDN# is asserted
- OTP page is changed through dynamic OTP_SEL
- PERST# buffer mode registers are changed so that:
  1. The output bank no longer selects INx
  2. Level triggered buffer mode is selected, or buffer mode is disabled
  3. Any other setting that does not enable regular PERST# buffer mode

7.3.8 Status Signals

7.3.8.1 CLK_READY

CLK_READY is asserted when the device is fully powered up and ready to output clocks. CLK_READY can be used to indicate the device readiness at power-up, when exiting power-down mode or after a hard reset. CLK_READY can be used in all operational modes including buffer only mode. Enabling or disabling outputs through OE controls does not affect the state of CLK_READY.

7.3.8.2 Input LOS

INx_LOS (loss of signal) indicates whether a valid clock signal is provided to INx. LOS is based on frequency detection. An input clock is considered valid if the frequency is higher than or equal to the detection threshold. The LOS threshold is programmable between 1MHz and 25MHz. LOS monitoring cannot be used for low frequency inputs such as 1PPS.

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7.3.8.3 Output Frequency Detection

Each output including REF0 and REF1 has a coarse frequency detector that detects if the output clock frequency is higher than or equal to the detection threshold. The detection threshold is programmable between 1MHz and 25MHz.

The output frequency detection is a useful monitoring feature. If the output clock is gone for any reason (for example, power disruption, internal circuit failure or solder joint failure), the missing output can be reported by the output frequency detector.

7.3.8.4 CRC_ERROR

CRC_ERROR indicates if the register values are correctly loaded from the preprogrammed OTP. This bit is updated every time OTP is loaded. When CRC error occurs, the OTP is loaded and the device is powered up normally. CRC_ERROR is only a status signal and does not gate the device operation.

7.3.8.5 Status Event Registers

Input LOS and output frequency detection have event registers that can record the error history. See register descriptions for details.

7.3.8.6 Device Interrupt

Table 7-32. Interrupt Registers

Register	Descriptions
DEV_INTR	Device interrupt. This register is the logic OR of all status registers that are included in the device interrupt. This signal can also be output from a GPIO pin.
INx_LOS_EVT_INTR_EN	When set to 1, LOS_x_EVT is included in the device interrupt
INx_LOS_LMT_EVT_INTR_EN	When set to 1, INx_LOS_LMT_EVT_INTR_EN is included in the device interrupt
CRC_ERROR_EVT_INTR_EN	When set to 1, CRC_ERROR_EVT is included in the device interrupt
OUTx_FREQ_ERR_EVT_INTR_EN	When set to 1, OUTx_FREQ_ERR_EVT is included in the device interrupt

7.3.8.7 Status Signals From GPIO

Status signals can also be output from GPIO pins. The polarity of a GPIO status output is determined by GPIO polarity.

- Normal polarity: Same with register polarity
- Inverted polarity: Opposite to register polarity.

7.3.9 Input Receiver

7.3.9.1 GPI Input And Clock Input

Each pair of GPI/INx pins can be configured as follows:

- If INx_RCVR_FMT = 0x0, then both INx_P and INx_N are configured as GPI pins
- If INx_RCVR_FMT = 0x1, then INx_P is LVCMOS clock input and INx_N is GPI pin
- If INx_RCVR_FMT = 0x2, then INx_P is GPI pin and INx_N is LVCMOS clock input
- If INx_RCVR_FMT = 0x3, then INx_P and INx_N are configured as differential clock input

User can connect INx_P and INx_N each to a different LVCMOS clock source, and select between the two sources dynamically by switching the value of INx_RCVR_FMT between 0x1 and 0x2.

7.3.9.2 Clock Input Configuration And Termination

Each clock input supports below terminations:

- No termination without internal bias (for LVCMOS inputs, LP-HCSL inputs and other DC-coupled inputs that do not require integrated input termination)
- No termination with internal bias (for AC-coupled inputs that do not require integrated input termination)
- 50Ω to GND on both P and N (for traditional 100Ω HCSL inputs and other DC-coupled inputs that require 50Ω to GND)

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- 50Ω to internal bias on both P and N (for AC-LVDS and other AC-coupled inputs that require 50Ω to AC-GND)
- 42.5Ω to GND on both P and N (for traditional 85Ω HCSL inputs and other DC-coupled inputs that require 42.5Ω to GND)
- 42.5Ω to internal bias on both P and N (for AC-coupled inputs that require 42.5Ω to AC-GND)
- 100Ω across P and N (for DC-coupled LVDS)
- 50Ω to DC path on both P and N. DC path is 50Ω to GND (for DC-LVPECL, depending on LVPECL termination requirements)

7.3.9.3 Differential Clock Inputs

Differential clock inputs can be AC coupled or DC coupled. When DC coupled, the input common mode can go up to 3.3V.

7.3.9.4 Fail-Safe Input

INx/GPI pins can tolerate a static high voltage when the device power is off. "Static high voltage" means no rising or falling edge. If a rising or falling edge is expected on INx/GPI pins when the device power is off, then:

- The INx pins can tolerate running differential input clocks when the device power is off, if below requirements are met:
  - The amplitude (half of differential peak-to-peak swing) is no more than 1.2V
  - The input clock can be AC or DC coupled. When DC coupled, the input common mode can go up to 3.3V.

To tolerate a running 1PPS clock with fast edge rate when the device power is off, add a 200Ω series resistor to limit the edge rate.

7.3.9.5 Input Crosstalk Mitigation

When multiple pairs of clock inputs are used, turn off the backup clock source to minimize input crosstalk. If the backup clock source cannot be turned off, power down the input driver through INx_PD to reduce input crosstalk.

However, input driver takes roughly 200µs to power up. If fast input switching is required, do not power down input drivers.

7.3.10 Input Switching

7.3.10.1 Automatic Switching

When the input clock at INx becomes invalid (LOS asserted), the output bank that select INx can automatically switch over to an FOD generated clock, if BANKy_AUTO_CLK_SWITCHOVER_EN is 1. The FOD generated clock that is automatically switched over to can be either path 0 or path 1, set by BANKy_AUTO_CLK_SWITCHOVER_CLK_SEL.

When the input clock at INx is re-validated (LOS deasserted) after BANKy undergoes an automatic clock switchover, BANKy can either switch back to INx or stay with the FOD generated clock, determined by BANKy_AUTO_CLK_SWITCHBACK_EN.

To enable the input switchover function, BANKx_SWITCHOVER_FRC_CLK_EN must be set to 0. When BANKx_SWITCHOVER_FRC_CLK_EN is set to 0, dynamic OTP page change is restricted. Set BANKx_SWITCHOVER_FRC_CLK_EN to 1 if the switchover function is unused.

7.3.10.2 Manual Switching

The clock source of each output bank can be manually switched via I2C by rewriting BANKy_CLK_SEL register. BANKy_SWITCHOVER_FRC_CLK_EN must be set to 0 to enable the manual switching.

The clock source of each output bank can also be manually switched via GPI/GPIO pins, using PERST. See PERST buffer mode for details

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7.3.11 Output MUX

7.3.11.1 Clock Output MUX Settings

For LMK3H2108, each output bank (OUT0, OUT1&2, OUT2&3, OUT4, OUT5, OUT6, OUT7) can independently select from 6 clocking sources: IN0, IN1, IN2, FOD_0, FOD_1, Edge Combiner.

For LMK3H2104, each output including REF_0 and REF_1 can independently select from 4 clocking sources: IN0, FOD_0, FOD_1, Edge combiner.

7.3.12 Output Driver

7.3.12.1 Output Formats

The device supports below output formats:

- 100Ω LP-HCSL
- 85Ω LP-HCSL
- AC-LVDS
- DC-LVDS
- LVCMOS enabled on OUTx_P, disabled on OUTx_N.
- LVCMOS disabled on OUTx_P, enabled on OUTx_N.
- LVCMOS enabled on both OUTx_P and OUTx_N. P and N are 180 degrees out of phase.
- LVCMOS enabled on both OUTx_P and OUTx_N. P and N are in phase.

7.3.12.2 1.2V LVCMOS Output

Every output except for REF0 and REF1 supports 1.2V LVCMOS. To enable 1.2V LVCMOS mode, set OUTx_CMOS_1P2V_EN to 1. When OUTx_CMOS_1P2V_EN is 0, the LVCMOS level follows the corresponding VDDO supply voltage.

Note that VDDO pins do not support 1.2V supply voltage. When the 1.2V LVCMOS driver drives a high impedance load, the corresponding VDDO must be connected to 1.8V. When the 1.2V LVCMOS driver drives an 100Ω differential load, the corresponding VDDO can be connected to 1.8V, 2.5V or 3.3V.

The 1.2V LVCMOS swing can also be factory preprogrammed to 1.1V. Contact TI for details.

7.3.12.3 LVCMOS Output Impedance

The 1.8V, 2.5V, and 3.3V LVCMOS output impedance is 17Ω. The 1.2V LVCMOS output impedance is 50Ω.

7.3.12.4 Programmable Slew Rate

LP_HCSL, LVDS and 1.2V LVCMOS clock output slew rate can be programmed through register OUTx_SLEW_RATE.

1.8/2.5/3.3V LVCMOS clock output slew rate can be programmed through register OUTx_CMOS_SLEW_RATE.

REF0 and REF1 clock output slew rate is not programmable.

7.3.12.5 Output Polarities

Output polarity can be inverted through registers OUTxP_INV_POL and OUTxN_INV_POL, for both single-ended and differential output formats. When the output driver is configured as single-ended (LVCMOS), the polarities of P and N can be inverted independently. When the output driver is configured as differential (LVDS or LP-HCSL), OUTxP_INV_POL and OUTxN_INV_POL must have the same value.

7.3.12.6 Double Terminated LP-HCSL Outputs

LP-HCSL outputs support both regular termination and double termination. With double termination, the swing is halved. For example, if the LP-HCSL swing is set to 800mV, then

- With regular termination, each single-ended output swings from 0V to 800mV
- With double termination, each single-ended output swings from 0V to 400mV

The option of double termination provides more flexibility in output swing and common mode configuration.

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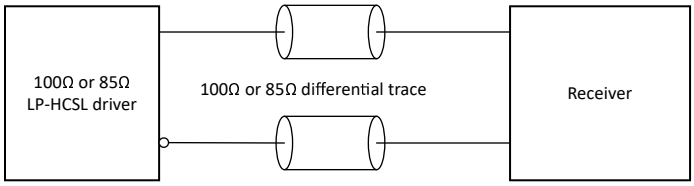


Figure 7-5. LP-HCSL Regular Termination

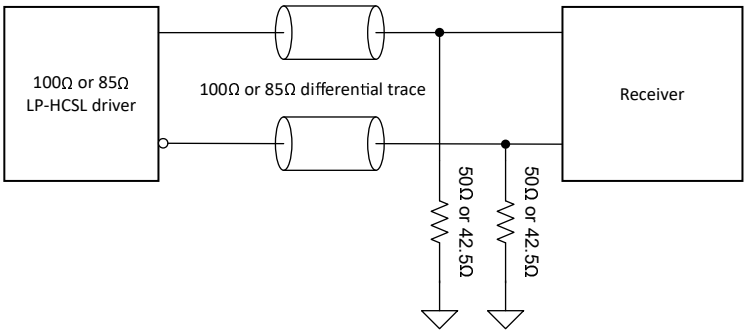


Figure 7-6. LP-HCSL Double Termination

7.3.12.7 AC- And DC-LVDS

LVDS drivers are typically DC terminated. To AC terminate an LVDS driver, either of below requirements must be met:

- If BANKx clock source is FOD or edge combiner, then the output driver can be AC-terminated
- If BANKx clock source is INy, then AC-LVDS can only be used if INy is never lost while the output is enabled via OE. If INy becomes invalid while the output is enabled via OE, then the LVDS output driver can rail out and get damaged.

In general, AC-LP-HCSL is recommended to replace AC-LVDS when applicable. Note that AC-LVDS means adding capacitors between LVDS driver and 100Ω termination. AC-coupling the DC-terminated LVDS driver and adding external bias is not considered AC-LVDS. See illustrations below.

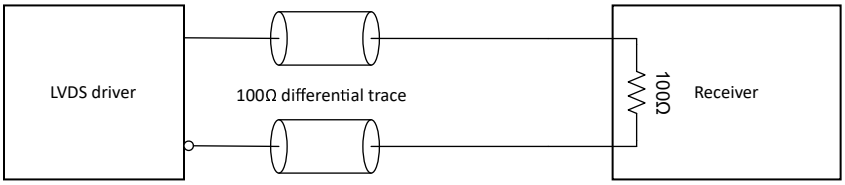


Figure 7-7. DC Terminated LVDS Output

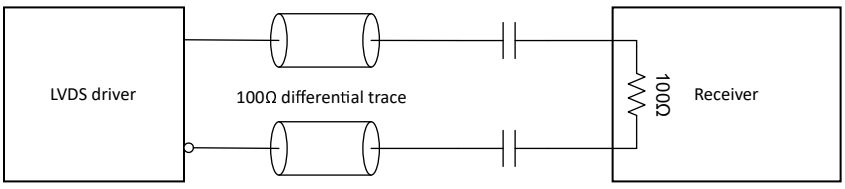


Figure 7-8. AC Terminated LVDS Output

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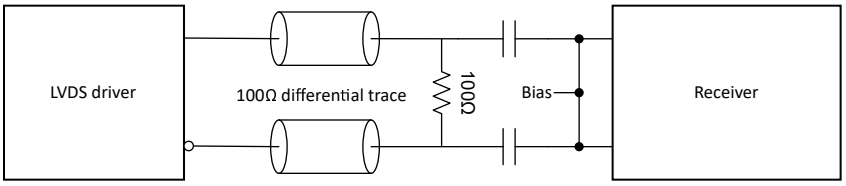


Figure 7-9. DC Terminated LVDS Output With External Bias

7.3.12.8 LVDS Output Common Mode

For 1.8V LVDS, the default common mode can be factory preprogrammed to lower levels such as 0.86V. Contact TI for details. For 2.5/3.3V LVDS, the common mode is standard 1.25V.

7.3.12.9 Output Disable States

When an output is disabled, the OUTx_P/OUTx_N can be set to High/Low, Low/High, Hi-Z/Hi-Z or Low/Low. The disable state of every output is set independently. Below table shows the output disable states for different output formats.

For AC-LVDS, Low/Low must be selected. DC-LVDS can select any disabled state. For either LVDS coupling, "Low/Low" is not descriptive of the output clock behavior and the output clock instead behaves as High/Low.

Output Format	High/Low		Low/High		Hi-Z/Hi-Z		Low/Low	
	OUTx_P	OUTx_N	OUTx_P	OUTx_N	OUTx_P	OUTx_N	OUTx_P	OUTx_N
LP-HCSL	High	Low	Low	High	Hi-Z	Hi-Z	Low	Low
DC-LVDS	High	Low	Low	High	Hi-Z	Hi-Z	High	Low
AC-LVDS	Reserved		Reserved		Reserved		High	Low
LVCMOS1	High	Low	Low	High	Hi-Z	Hi-Z	Low	Low
LVCMOS2	High	Low	Low	High	Hi-Z	Hi-Z	Low	Low
LVCMOSD	High	Low	Low	High	Hi-Z	Hi-Z	Low	Low
LVCMOSx2	High	Low	Low	High	Hi-Z	Hi-Z	Low	Low

REF_0 and REF_1 of LMK3H2104 can be disabled to Low or Hi-Z.

7.3.12.10 Output Behaviors During Change of State

Whenever the state of a clock output changes (for example, the output is enabled and disabled, the device switches between power-down mode and normal operation mode, during device power-up, during device shut-down, when clock source switches or when OTP page changes), the clock output behaves as follows :

- There is no glitch or runt pulse during the change or switch, unless asynchronous OE is selected.
- When an output is active, the output meets all electrical specifications starting from the first clock cycle.
- When an output is disabled or powered down, the output remains quiet and there is no abnormal waveform, oscillation or pulse at the output.

7.3.13 Output Synchronization

7.3.13.1 Output Synchronization

Every output bank can select between 3 sync modes:

- Full sync mode. In full sync mode, outputs that come from the same clock source are phase synchronized after:
  - Power-up, PWRDN toggling or OTP page switching
  - OE pin toggling, if the outputs are assigned to the same OE group
  - Global OE toggling

  The available clock sources are: INx, FOD_0, FOD_1, Edge Combiner. In full sync mode, OE is also synchronous.

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- Self sync mode. In self sync mode, the outputs are not phase synchronized to each other, but the OE of the outputs is synchronous.
- No sync mode. In no sync mode, the outputs are not phase synchronized to each other, and the OE of the outputs are asynchronous.

If the output dividers are bypassed, then outputs are phase aligned regardless of sync settings.

7.3.13.2 Synchronous And Asynchronous OE

With asynchronous OE, the output is immediately enabled and disabled upon OE assertion and deassertion. There is minimum delay when enabling and disabling the outputs. However, there can be glitches or runt pulses during OE.

With synchronous OE, there is no glitch or runt pulse, but there is a few cycles of delay during output enable and disable.

For high frequency (>1MHz) operations, this delay is negligible. However, for low frequency applications such as 1PPS clock buffering, such delay is typically unacceptable. The device is designed in a way so that glitchless operation and minimum power-up delay can be achieved at the same time for 1PPS input. When synchronous OE is disabled, the power-up process with 1PPS input is still glitchless, but the OE process is not glitchless.

Synchronous operation requires a constantly running reference clock source. When the clock source is FOD or edge combiner, this is not a concern. However, when the clock source is INx, then synchronous operation only works if INx clock stays valid. If INx is lost while OE is asserted, then outputs are shut down asynchronously, regardless of sync settings.

7.3.14 Output Phase Shift

Output phase shift can be achieved through FOD digital delay. Each FOD can provide up to 25ns phase delay at the outputs with 25ps step size. Therefore, the phase difference between the two FODs can be programmable from -25ns to +25ns.

7.3.15 Dynamic Frequency Change

Output frequency can be incremented or decremented glitchlessly in three ways:

- Directly change FOD frequency through FODx_CFG_UPDATE
- Directly change channel divider (coarse increment or decrement)
- DCO mode

7.3.15.1 FOD Configuration Update

Because FOD frequency configuration consists of multiple registers, FODx_CFG_UPDATE is added for clean frequency transition. The new values of FODx_N_DIV and FODx_NUM registers do not take effect until FODx_CFG_UPDATE is written with a 1.

Changing channel divider values results in an immediate change to the new frequency. The frequency changing process is glitchless. The clock cycle with new frequency starts after the last clock cycle with old frequency is completed.

7.3.15.2 Channel Divider Update

Changing BANKx_CH_DIV dynamically results in a glitchless frequency update. The clock cycle with new frequency starts after the last clock cycle with old frequency is completed.

7.3.15.3 DCO Mode

Each FOD supports independent DCO.

DCO mode consists of below registers for each FOD:

- DCO enable bit *FODx_DCO_EN* that enables or disables DCO mode. After enabling DCO mode, writing a 0 to this bit clears all the frequency increments and decrements, and brings the FOD frequency to the original value before DCO mode is enabled.

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- DCO increment and decrement step size *FODx_DCO_STEP_SIZE*
- Increment bit *FODx_DCO_INC*. Increments the frequency when written with a 1
- Decrement bit *FODx_DCO_DEC*. Decrements the frequency when written with a 1
- Read-only register *FODx_DCO_STEPS_STAT* that records the net number of increment or decrement steps
- Read-only registers *FODx_DCO_N_DIV_STAT* and *FODx_DCO_NUM_STAT* that read back the live (incremented or decremented) FOD values which can be used to calculate the live frequency

Equation 1 is the formula for setting the DCO step size based on the desired ppm step.

$$\text{FODx_DCO_STEP_SIZE} = \text{int}(2^{16} \times \left(\frac{F_{BAW}}{F_{FOD} \times \left(1 + \frac{\text{ppm}}{10^6}\right)} - \text{FODx_N_DIV} - \left(\frac{\text{FODx_NUM}}{2^{24}} \right) \right)) \quad (1)$$

where:

- F_{BAW} is the BAW frequency, 2467MHz
- F_{FOD} is the FOD frequency
- ppm is the frequency shift in parts per million
- FODx_N_DIV is the integer divider of the FOD
- FODx_NUM is the numerator of the FOD divider

7.4 SSC

Both FOD0 and FOD1 support spread-spectrum clocking (SSC). SSC can be used to reduce peak radiated emissions by modulating the output frequency. When FODx_SSC_EN = '1', SSC is enabled on FODx. FODx_SSC_MOD_TYPE selects between down-spread modulation and center-spread modulation. There are 4 predefined built-in down-spread SSC options, as well as a custom SSC option, selected by FODx_SSC_CONFIG_SEL. The predefined modulation depth is intended for use with a 200MHz FOD. If the FOD frequency is not 200MHz, then the actual modulation depth is higher or lower depending on the FOD frequency. If the edge combiner is used, SSC must be disabled.

Table 7-33. Predefined SSC Configurations

SSC_CONFIG_SEL	SSC Modulation Depth
0x0	Custom, based on SSC_STEPS and SSC_STEP_SIZE
0x1	–0.10%
0x2	–0.25%
0x3	–0.30%
0x4	–0.50%
All other values	Reserved

If Custom SSC is selected, then SSC_STEPS (register field FODx_SSC_STEPS) and SSC_STEP_SIZE (register field FODx_DCO_STEP_SIZE) must be configured to set the modulation depth.

Down-spread: SSC_STEPS = int((F_{FOD}/F_{MOD})/2) (2)

Center-spread: SSC_STEPS = int((F_{FOD}/F_{MOD})/4) (3)

where:

- F_{FOD}: FOD Frequency
- F_{MOD}: Modulation frequency, use 31.5kHz for PCIe applications

$$SSC_STEP_SIZE = floor((F_BAW/F_FOD \times (1/(1 - SSC_DEPTH) - 1))/(SSC_STEPS) \times DEN) \quad (4)$$

$$SSC_STEP_SIZE = floor((F_BAW/F_FOD \times (1/(1 - SSC_DEPTH) - 1/(1 + SSC_DEPTH)))/(2 \times SSC_STEPS) \times DEN) \quad (5)$$

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where:

- F_{BAW}: BAW frequency, 2467MHz.
- SSC_DEPTH: Modulation depth, expressed as a positive value. If –0.5% depth is used, this value is 0.005
- DEN: Fractional denominator, 2^{24}

If using a mix of SSC on one FOD and no SSC on the other FOD, there can be crosstalk between the two FODs. Contact TI to request measurement data for a specific configuration.

If SSC is only used on FOD0 and not used on FOD1, then FOD1_SSC_CONFIG_SEL must be set to non-0.

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7.5 Device Functional Modes

7.5.1 Fractional Output Divider

The device contains two fractional output dividers (FOD). If all outputs can be generated by a single FOD, use FOD0 and disable FOD1 (through FOD1_PD) to conserve power and improve performance.

7.5.1.1 FOD Operation

The internal BAW resonator is divided down by one or two FODs.

The maximum frequency that can be generated at the clock outputs by a single FOD is 200MHz, as the minimum channel divider value is a divide by two. To generate a frequency greater than 200MHz output, the edge combiner is used, bypassing the channel dividers. This requires that both FODs are enabled and have the same integer divider and fractional numerator values, and the same gain calibration values. When one of the outputs exceeds 200MHz, the other output can only select the shared FOD frequency divided by one of the channel divider values, or be the FOD frequency. Below 200MHz, the two FODs can be configured independently.

The FODs can be configured to accommodate various output frequencies through I2C programming, or in the absence of programming, the one-time programmed (OTP) settings. The FODs can be configured by setting the integer (FODx_N_DIV) and fractional (FODx_NUM) divide values.

$$FODx_N_DIV = floor(F_{BAW}/F_{FOD}) \quad (6)$$

where:

- FODx_N_DIV: Integer portion of the FOD divide value (7 bits, 6 to 24)
- F_{BAW}: BAW frequency, 2467MHz
- F_{FOD}: Desired FOD frequency (100MHz to 400MHz)

$$FODx_NUM = int(((F_{BAW}/F_{FOD}) - FODx_N_DIV) \times 2^{24}) \quad (7)$$

where FODx_NUM is the fractional portion of the FOD divide value (24 bits, that is 0 to 16777215).

The output frequency (F_{OUT}) is related to the FOD frequency as follows. If the edge combiner is disabled:

$$F_{OUT} = F_{FOD}/PATHx_DIV/BANKx_CH_DIV \quad (8)$$

If edge combiner is enabled:

$$F_{OUT} = F_{FOD}/BANKx_CH_DIV \quad (9)$$

7.5.1.2 Edge Combiner

Use the edge combiner to generate output frequencies greater than 200MHz. To use the Edge Combiner, set PATHx_EDGE_COMB_EN to '1'. When using the edge combiner, both FODs must operate at the same exact frequency (that is, the divide values must match). The device handles this by automatically loading the divider values from FOD0 into FOD1 when either CHx_EDGE_COMB_EN bit is set to a '1'. When using the edge combiner, SSC is not supported and must be disabled.

7.5.1.3 Integer Boundary Spurs

When the decimal portion of the FOD divide value is near an integer boundary, integer boundary spurs can occur. In general, this "integer boundary" is when the decimal portion is between 0.9 and 1, or 0 and 0.1. For example, if the BAW frequency is 2467MHz and an output is 122.88MHz, then the FOD must run at 245.76MHz. 2467MHz divided by 245.76MHz is approximately 10.038. The decimal portion of the divide value is 0.038, which falls between 0 and 0.1, and thus means that generating a 122.88MHz output can result in spurs in the 12kHz to 20MHz band on the output clock. In some cases, proper frequency planning can account for this by increasing the FOD frequency and the channel divider value. For any concerns about integer boundary spurs for a specific frequency plan, contact TI.

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7.5.2 Buffer Only Mode

The device can operate as a general purpose clock buffer or clock MUX. The BAW as well as both FODs can be powered down to save power and avoid crosstalk. When BAW is disabled, BOOTOSC_CLK_DIS must be set to 0.

7.6 Programming

7.6.1 I²C Serial Interface

The device supports 100kHz, 400kHz and 1MHz I²C. I²C voltage and timing parameters and can be found in I2C Characteristics.

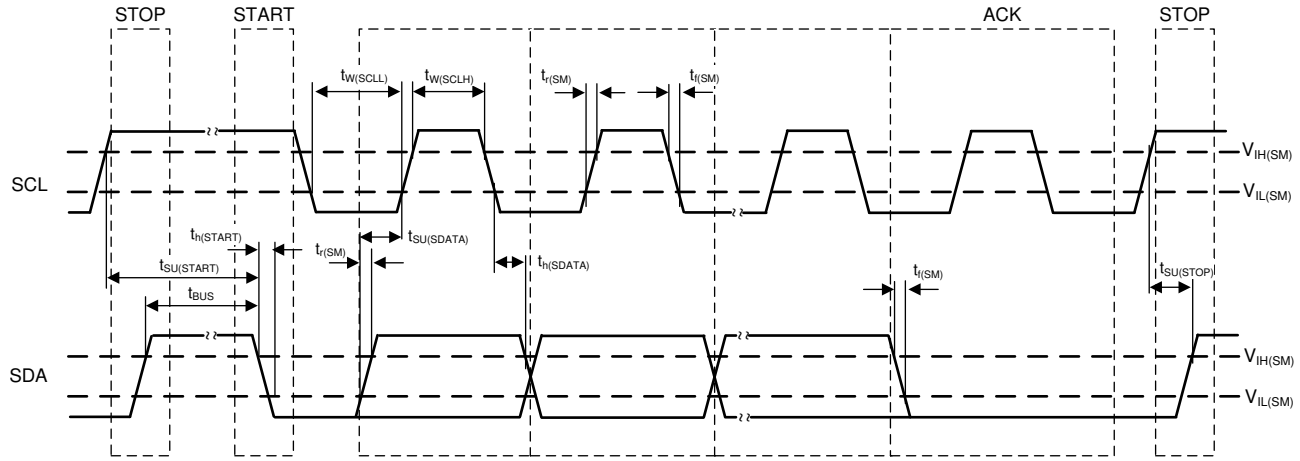


Figure 7-10. I²C Timing Diagram

Two I²C communication modes are supported: 1-byte mode and 2-byte mode.

In 1-byte mode, the upper 2 bits of a register address are accessed through 0xFD (register field PAGE_SEL). The lower 8 bits of a register address are written directly. Data words are 8-bit long for each register address.

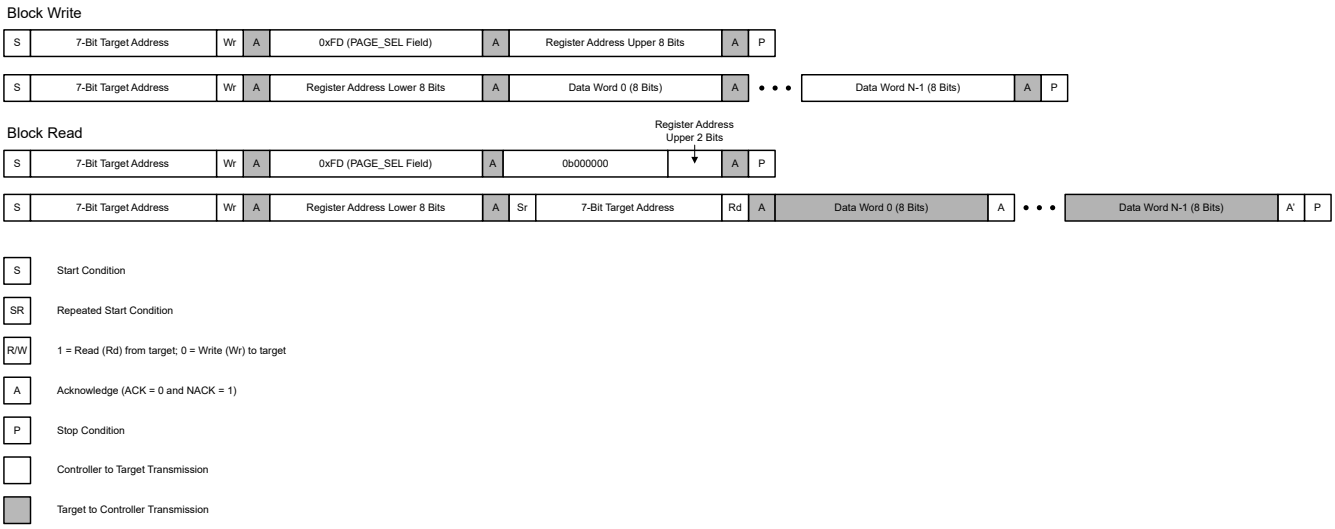


Figure 7-11. I²C 1-Byte Mode

In 2-byte mode, the 16-bit register addresses are written directly. Data words are 8-bit long for each register address.

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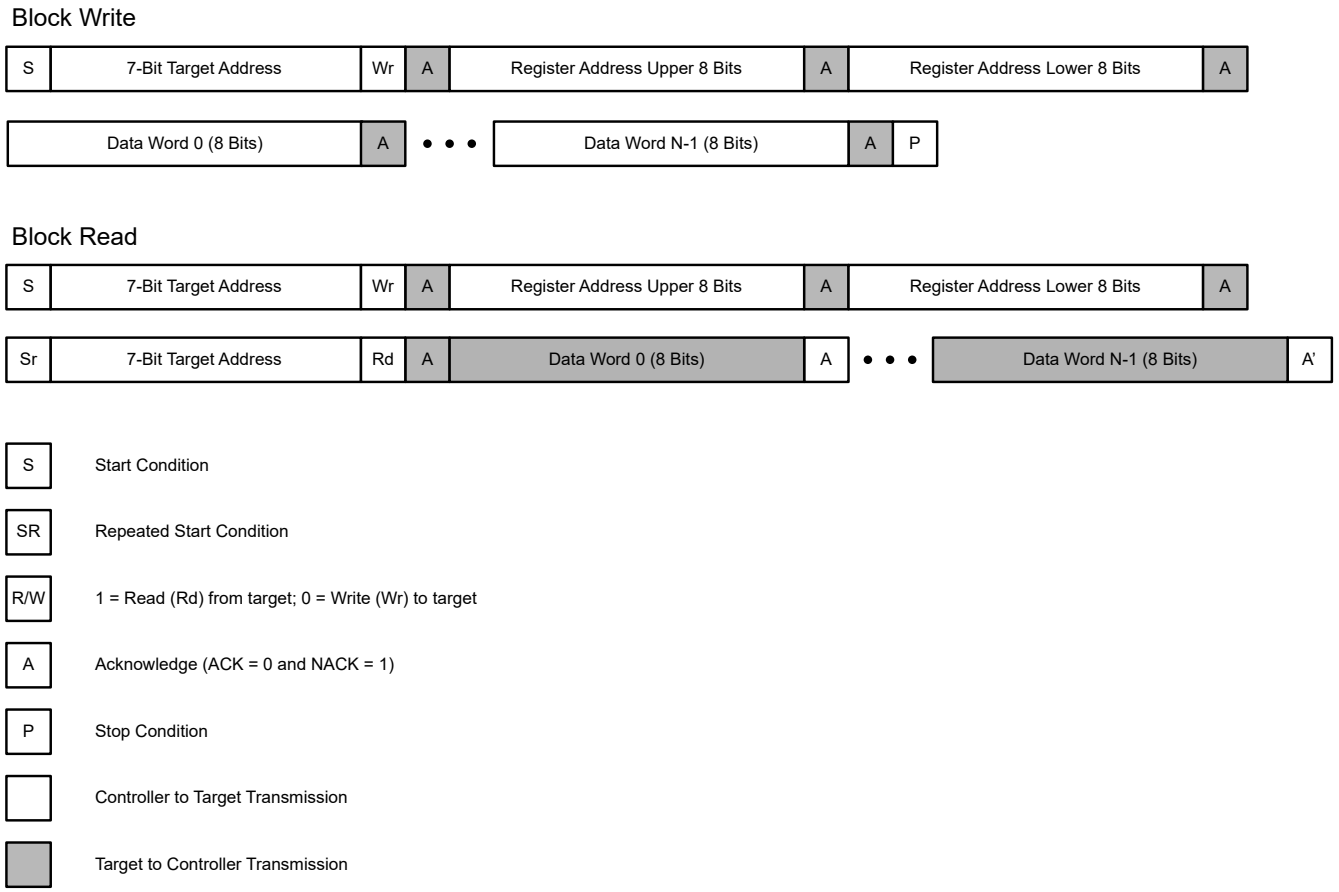


Figure 7-12. I²C 2-Byte Mode

The 7-bit I2C target address is defined by I2C_TRGT_ADDR through OTP. Bit 1 and bit 0 of the 7-bit address can be overridden through GPI/GPIO input. See I2C Address Through GPI/GPIO for details.

7.6.2 Vendor ID

The 11-bit Vendor ID (R1[2:0], R0[7:0]) is OTP programmable. R1[7:3] is read-only . (R1[7:0], R0[7:0]) = 0x038B by default.

7.6.3 OTP Programming

To create a new OTP configuration with a unique Orderable Part Number, contact TI.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMK3H2104 and LMK3H2108 are reference-less BAW-based clock generators that can provide reference clocks for various applications, including PCIe reference clocking and XTAL/XO replacement. The LMK3H2104 and LMK3H2108 support a variety of features that aids the hardware designer during the system debug and validation phase.

8.2 Typical Application

8.2.1 Application Block Diagram Example

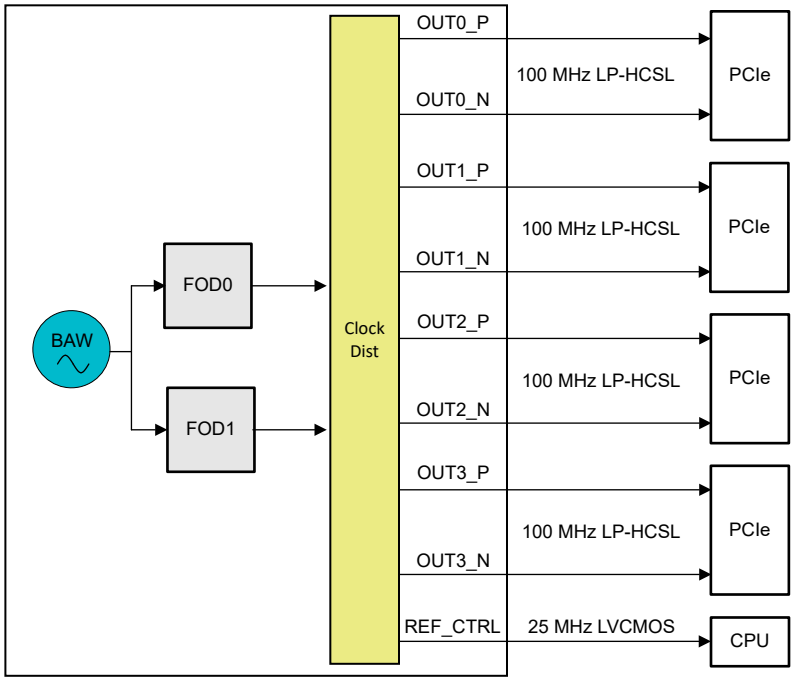


Figure 8-1. LMK3H2104 PCIe Application

8.2.2 Design Requirements

Consider a typical PCIe application as shown in Figure 8-1. In a system such as this, the clocks are expected to be available upon request without the need for any additional device-level programming. A typical output clock requirement in this application is four 100MHz LP-HCSL clocks. A 25MHz clock is added to show how to configure the REF_x output as well. The section below describes the detailed design procedure to generate the required output frequencies for the above PCIe scenario using the LMK3H2104.

8.2.3 Detailed Design Procedure

Design of all aspects of the device is straightforward, and software support is available to assist in frequency planning and part programming. This design procedure gives a straightforward outline of the process.

1. Supply Voltages

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a. Each OUTx output has a field for floating the supply voltage. When this field is set to a 1, the supply voltage pin can be either powered or floating. When this field is set to a 0, the supply voltage pin **must** be powered.

2. Input Behavior
   a. If using the LMK3H210x in buffer mode, the input buffer path must be configured. For input buffer configuration, these behaviors must be configured:
      i. INx Power Down: Controls whether the input buffer for the input clock is powered down or powered up. The corresponding register field is INx_PD.
      ii. INx Receiver Format: Sets the input clock type, either not applicable for no input clock, single-ended LVCMOS on either INx_P or INx_N, or differential. The corresponding register field is INx_RCVR_FMT.
      iii. INx Termination: Sets the input termination scheme. HCSL inputs require either a 85Ω or 100Ω differential termination setting, depending on the system requirements. Otherwise, DC-coupled inputs require no termination or biasing. AC-coupled inputs that do not require termination must use no termination with internal biasing. Otherwise, select the appropriate termination option based on the AC-coupled input format: AC-CML, AC-LVPECL, or AC-LVDS.
   b. If not using any of the LMK3H210x clock inputs, then power down the input buffers.
   c. Switching from an input clock to an FOD clock has different requirements for OTP mode and I^2C mode. Each output bank has a field that controls the switchover behavior for that bank: BANKx_SWITCHOVER_FRC_CLK_EN. When this bit is set to a 0, switchover between an input clock and the FODs is supported through I^2C, not through changing OTP pages. When this bit is set to a 1, switchover between an input clock and the FODs is supported through OTP page changing, not through I^2C. This bit can be changed to a 0 in I^2C mode for supporting switchover via I^2C.

3. Frequency Planning
   a. If not using an input clock, then the first step of designing an LMK3H210x configuration is to determine the FOD frequencies that are required to generate the required output frequencies. Key device behaviors that impact frequency planning are:
      i. If both FODs are required for generating the frequency plan, FOD1_PD must be set to a 0 for FOD1 to be powered on. In this case, PATH1_FOD_SEL must be set to a 1. This requires unlocking the device first by writing 0x5B to UNLOCK_PROTECTED_REG.
      ii. Both FODs have SSC configuration options available. If SSC is used on only FOD0, FOD1_SSC_CONFIG_SEL must be non-zero for proper SSC functionality on FOD0.
      iii. For custom SSC configuration, the FODx_DCO_STEP_SIZE field doubles as the SSC step size. Refer to Section 7.4 for details on SSC configuration. Refer to Section 7.3.15.3 for details on DCO configuration.
      iv. Each path before the output banks can select from either the FOD outputs or the Edge Combiner output. If the edge combiner is selected, then both FODs operate at the same frequency set by FOD0.
      v. When changing the FOD frequency, set the corresponding FODx_CFG_UPDATE field to a 1 to update the FOD behavior.
      vi. OUT0 has a divider range between 1 and 65536. All other outputs have a range between 1 and 16. For generating frequencies below 156.25kHz, using OUT0 is required.

4. Output Format Selection
   a. Each OUTx output has five fields that control the output behavior: OUTx_FMT, OUTxP_INV_POL, OUTxN_INV_POL, OUTxP_OE_CMOS, and OUTxN_OE_CMOS. "Inverted Phase" refers to a 180 degree phase shift of the clock signal. Table 8-1 details the combination of settings for each possible output format.
   b. Each OUTx output has the option for using 1.2V LVCMOS. For 1.2V LVCMOS, an LVCMOS output format must be selected with the corresponding OUTx_CMOS_1P2V_EN bit set to a 1.

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c. For AC-coupled LVDS, the output disable state must be set to Low/Low. Refer to Section 7.3.12.9 for a detailed explanation of the output disable state behavior.

Table 8-1. Output Format Setting Combinations

Output Format	OUTx_FMT	OUTxP_INV_POL	OUTxN_INV_POL	OUTxP_OE_CMOS	OUTxN_OE_CMOS
100Ω LP-HCSL	0	0	0	1	1
85Ω LP-HCSL	1	0	0	1	1
AC-LVDS	2	0	0	1	1
DC-LVDS	2	0	0	1	1
LVCMOS OUTx_P	3	0	0	1	0
LVCMOS OUTx_P, Inverted Phase	3	1	0	1	0
LVCMOS OUTx_N	3	0	1	0	1
LVCMOS OUTx_N, Inverted Phase	3	0	0	0	1
Differential LVCMOS	3	0	0	1	1
Differential LVCMOS, Inverted Phase	3	1	1	1	1
In-Phase LVCMOS	3	0	1	1	1
In-Phase LVCMOS, Inverted Phase	3	1	0	1	1

8.2.4 Application Performance Plots

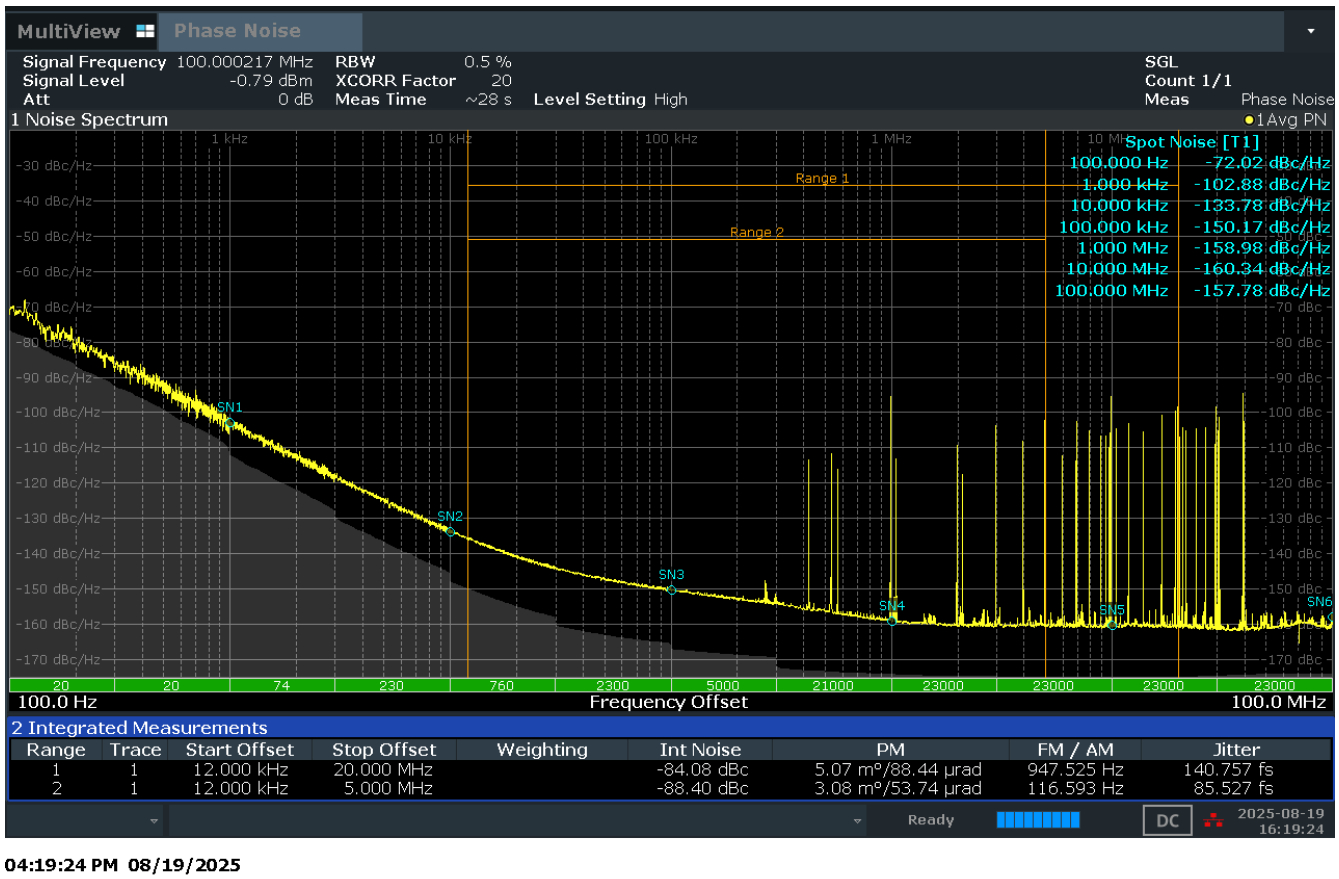


Figure 8-2. Phase Noise Plot, 100MHz LP-HCSL All Outputs, Typical Performance

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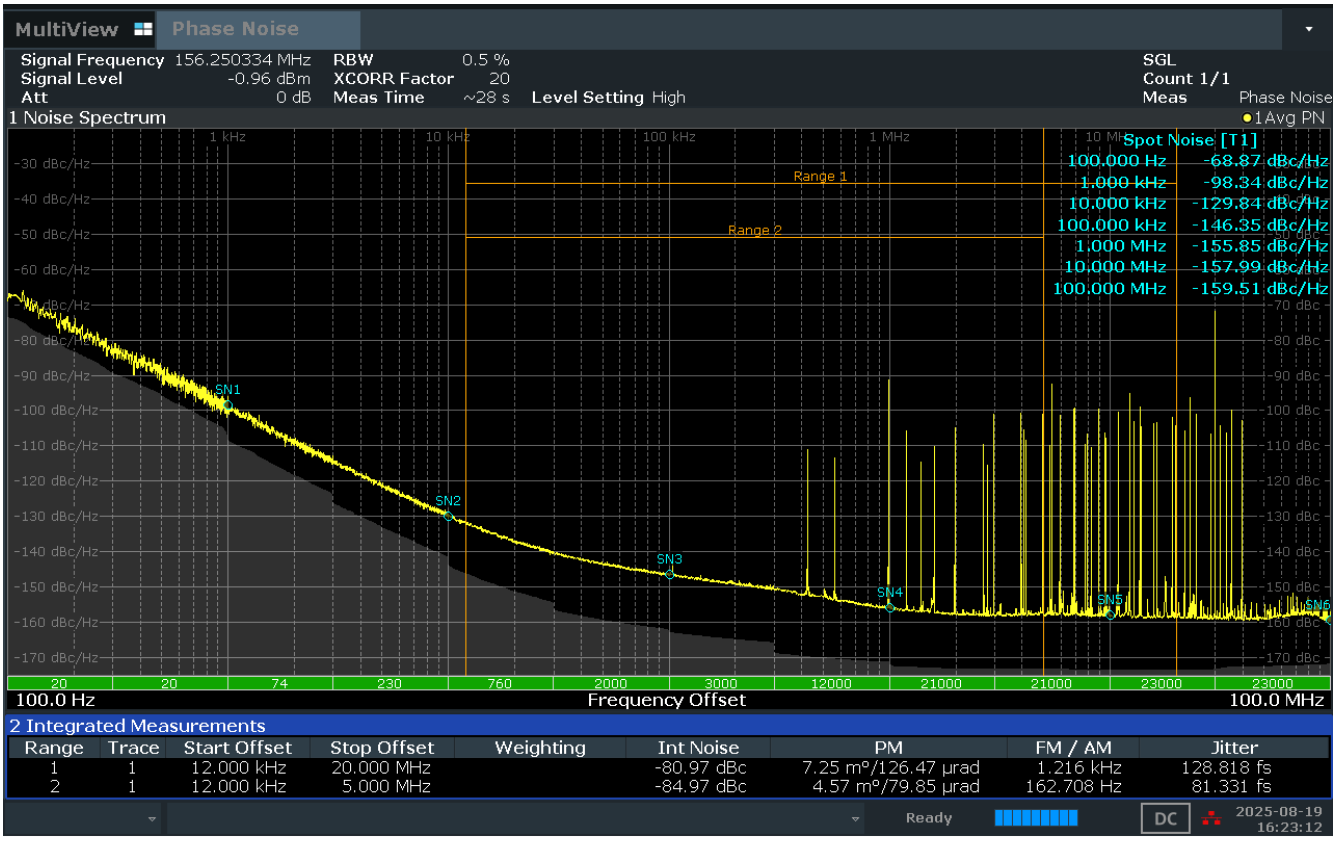


Figure 8-3. Phase Noise Plot, 156.25MHz LP-HCSL All Outputs, Typical Performance

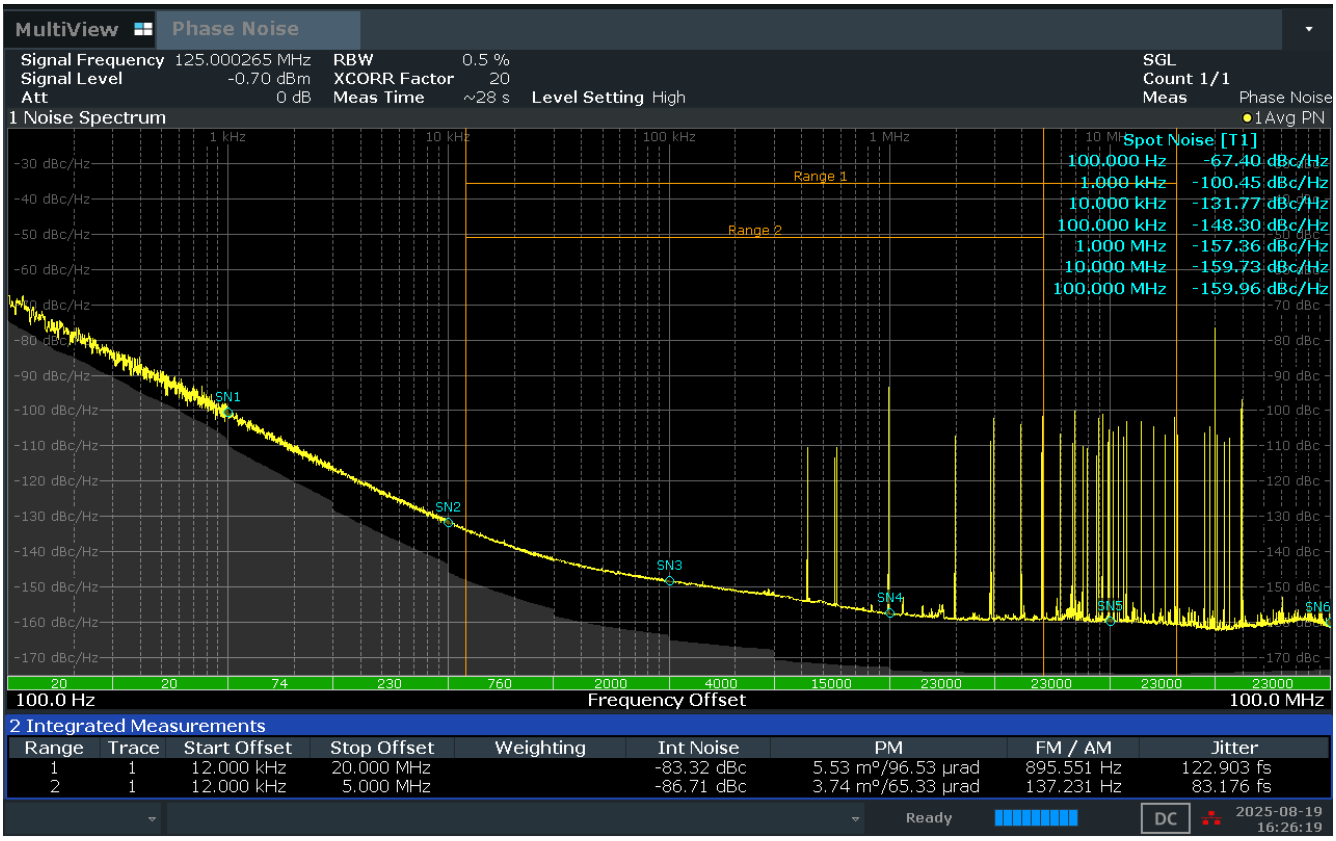


Figure 8-4. Phase Noise Plot, 125MHz LP-HCSL All Outputs, Typical Performance

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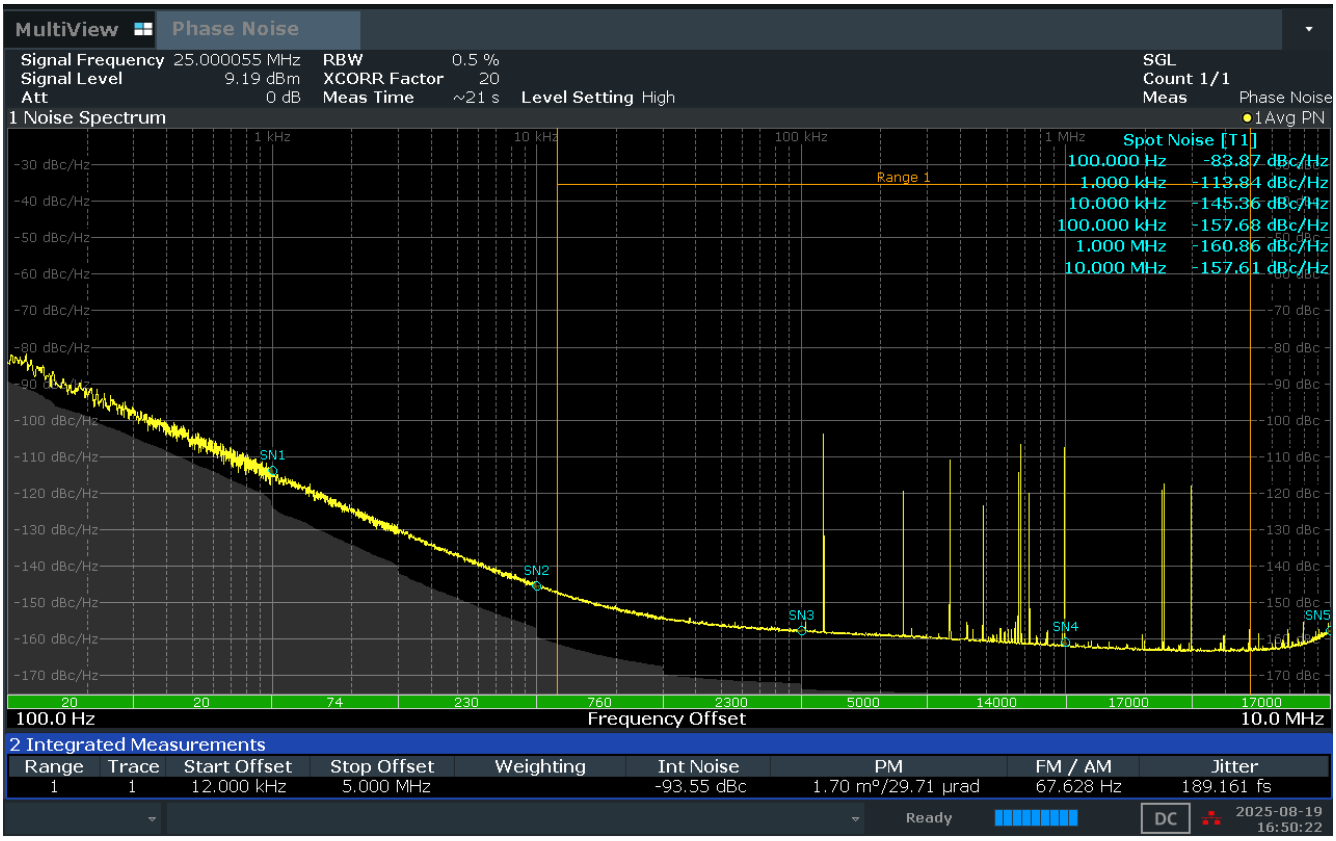


Figure 8-5. Phase Noise Plot, 25MHz LVCMOS All Outputs, Typical Performance

8.3 Power Supply Recommendations

The device provides multiple power supply pins tolerant of 1.8V, 2.5V, and 3.3V. Internal low-dropout regulators (LDO) source the internal blocks and allow each pin to be supplied with an individual supply voltage. If external pull-up resistors are used, these resistors must be connected as follows:

- LMK3H2104
  - GPI_0, GPI_1: Pull to VDD_REF voltage
  - GPI_2, GPIO_0, GPIO_1, SDA, SCL: Pull to VDDD voltage
  - REF_1: Pull to VDDA voltage
- LMK3H2108
  - GPI_0, GPI_1: Pull to VDDX voltage
  - GPI_2, GPI_3, GPI_4, GPI_5: Pull to VDDR voltage
  - GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4: Pull to VDDD voltage

TI recommends isolating all power supplies using a ferrite bead and provide decoupling for each of the supplies. TI also recommends optimizing the decoupling for the respective layout, and consider the power supply impedance to optimize for the individual frequency plan. An example for a decoupling per supply pin: 1x 4.7µF and 1x 100nF.

For detailed power sequencing requirements, refer to Section 7.3.5.1.

8.4 Layout

8.4.1 Layout Guidelines

For best device performance over the entire temperature range, follow these layout guidelines:

- Isolate inputs and outputs using a GND shield. Route all inputs and outputs as differential pairs.
- When outputs are the same frequency, the supply voltages can be connected together. When the frequencies differ, TI recommends isolating the supplies.
- If the clocks are routed to a different layer through vias, place a GND via as close as possible to the clock via.
- For LMK3H2104, use at least five vias to connect the thermal pad to a solid GND plane. For LMK3H2108, use at least nine vias to connect the thermal pad to a solid GND plane. Full-through vias are preferred. Refer to (1) in Figure 8-6 for an example.
- Place decoupling capacitors with small capacitance values very close to the supply pins. Try to place the capacitors very close on the same layer or directly on the backside layer. Larger values can be placed more far away. Refer to (2) in Figure 8-6 for an example.
- If power is routed across multiple layers, use multiple vias to connect the power traces across layers. Refer to (3) in Figure 8-6 for an example.
- For reduction of junction-to-ambient thermal resistance, use multiple PCB GND layers if possible.

8.4.2 Layout Example

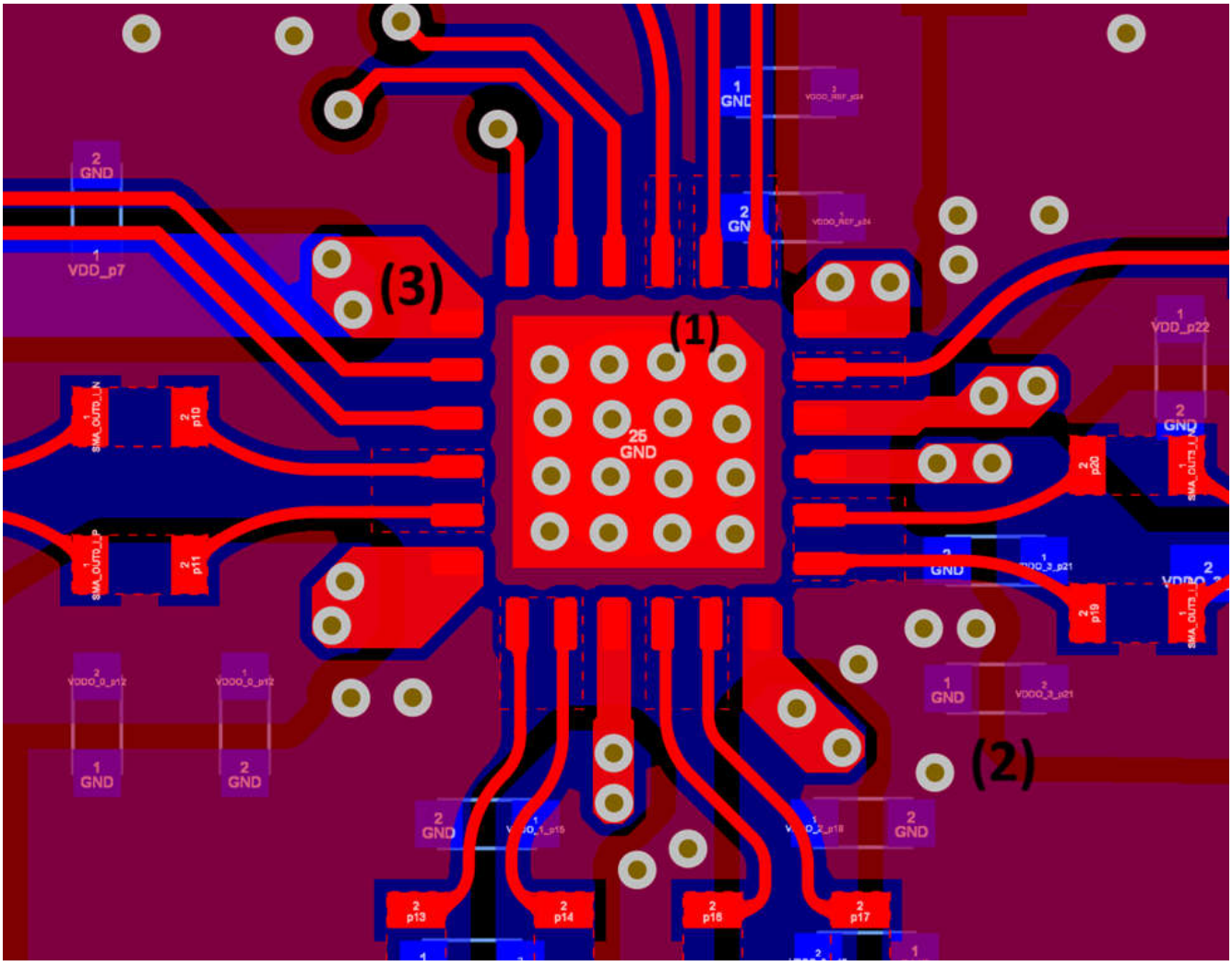


Figure 8-6. LMK3H2104 Top and Bottom Layers Example Layout

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, LMK3H2104 Evaluation Module User's Guide
- Texas Instruments, LMK3H2104 Register Map User's Guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2025) to Revision A (October 2025)	Page
• Added the LMK3H2108 device. Added LMK3H2108 related specs, diagrams and descriptions	1
• Removed the Min and Max for PSNR specs. Typical values are unchanged	7
• Changed the output enable and disable time for full sync mode and self sync mode	7
• Added the description that BANKx_SWITCHOVER_FRC_CLK_EN must be set to 0 to enable the PERST buffer mode	34

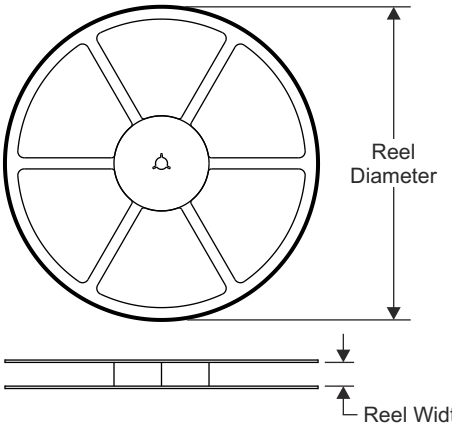
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

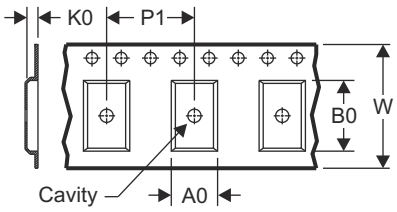
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11.1 Tape and Reel Information

REEL DIMENSIONS

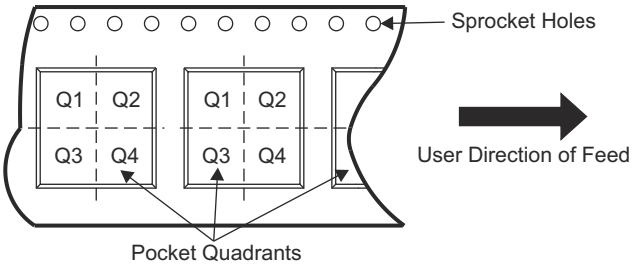


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

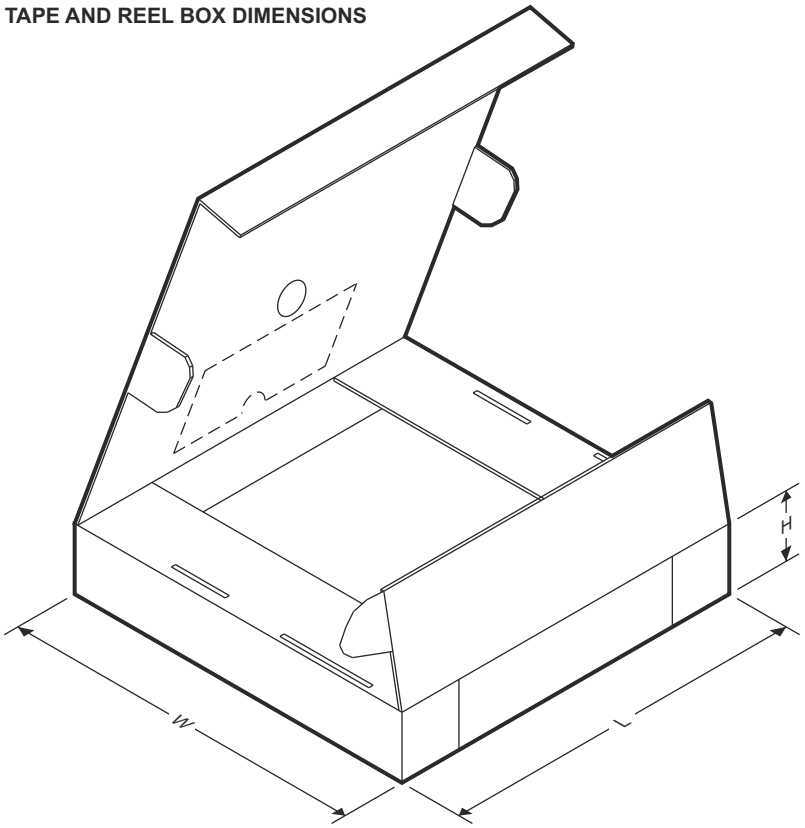
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK3H2108AxxRKPR	VQFN	RKP0040A	40	5000	330	12.4	5.3	5.3	1.1	8	12	Q2
LMK3H2104AxxLRGER	VQFN	RGE0024 AA	24	5000	330	12.4	4.25	4.25	1.15	8	12	Q2
LMK3H2104AxxRGER	VQFN	RGE0024 AB	24	5000	330	12.4	4.25	4.25	1.15	8	12	Q2

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK3H2108AxxRKPR	VQFN	RKP0040A	40	5000	346	346	33
LMK3H2104AxxLRGER	VQFN	RGE0024AA	24	5000	346	346	33
LMK3H2104AxxRGER	VQFN	RGE0024AB	24	5000	346	346	33

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK3H2104A01LRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 L A01
LMK3H2104A02LRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	3H2104 L A02
LMK3H2104A03RGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 A03
LMK3H2104A06LRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 L A06
LMK3H2104A07RGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 A07
LMK3H2104A09LRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 L A09
LMK3H2104A0DLRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 L A0D
LMK3H2104A0ELRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 L A0E
LMK3H2104A0FLRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 L A0F
LMK3H2104A10LRGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2104 L A10
LMK3H2108A01RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A01
LMK3H2108A02RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A02
LMK3H2108A03RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A03
LMK3H2108A04RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A04
LMK3H2108A05RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A05
LMK3H2108A06RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A06

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMK3H2108A07RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A07
LMK3H2108A0DRKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A0D
LMK3H2108A0ERKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A0E
LMK3H2108A0FRKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A0F
LMK3H2108A11RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A11
LMK3H2108A14RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A14
LMK3H2108A15RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A15
LMK3H2108A16RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A16
LMK3H2108A17RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A17
LMK3H2108A18RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A18
LMK3H2108A19RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A19
LMK3H2108A1ERKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A1E
LMK3H2108A22RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A22
LMK3H2108A25RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A25
LMK3H2108A26RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 105	3H2108 A26
LMK3H2108A27RKPR	Active	Production	VQFN (RKP) | 40	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	3H2108 A27

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

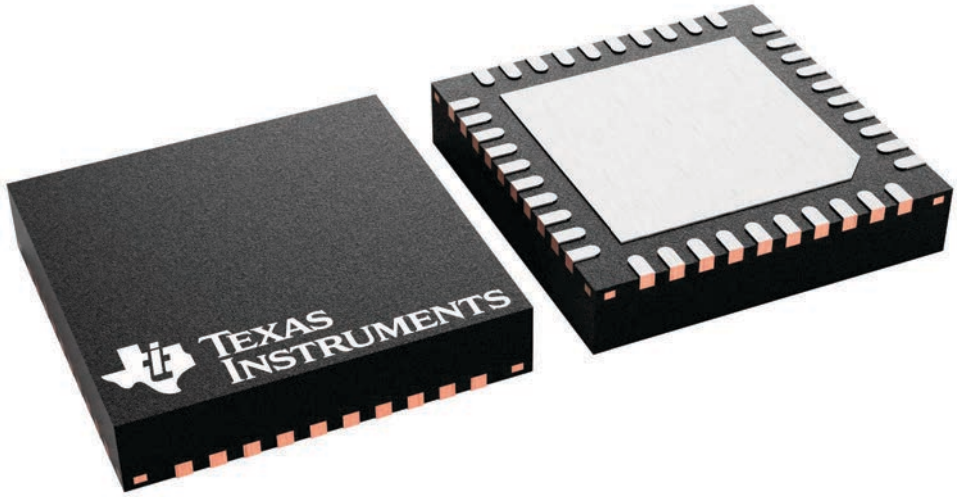
RKP 40

VQFN - 1 mm max height

5 x 5, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



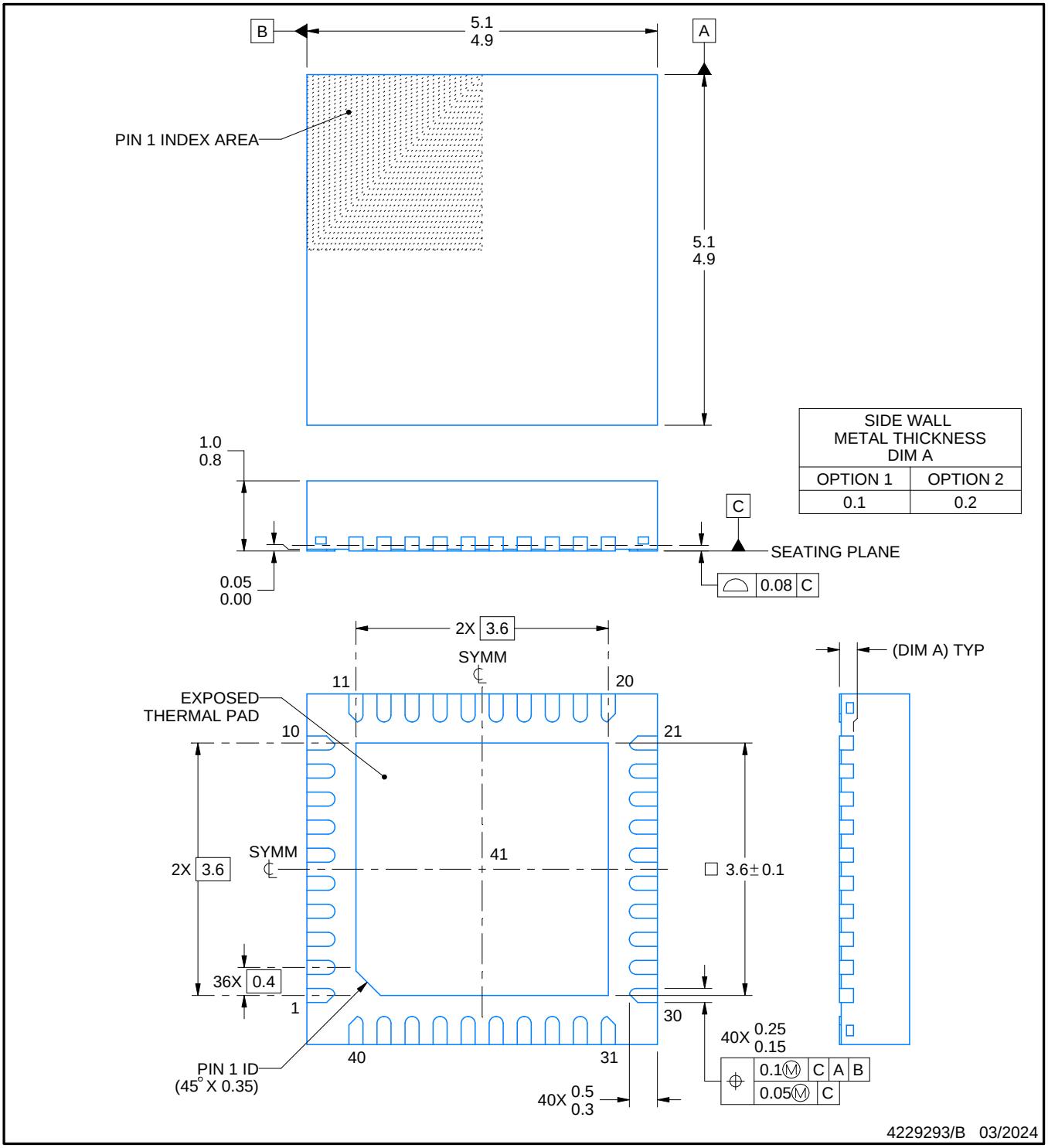
4229305/A

PACKAGE OUTLINE

RKP0040A

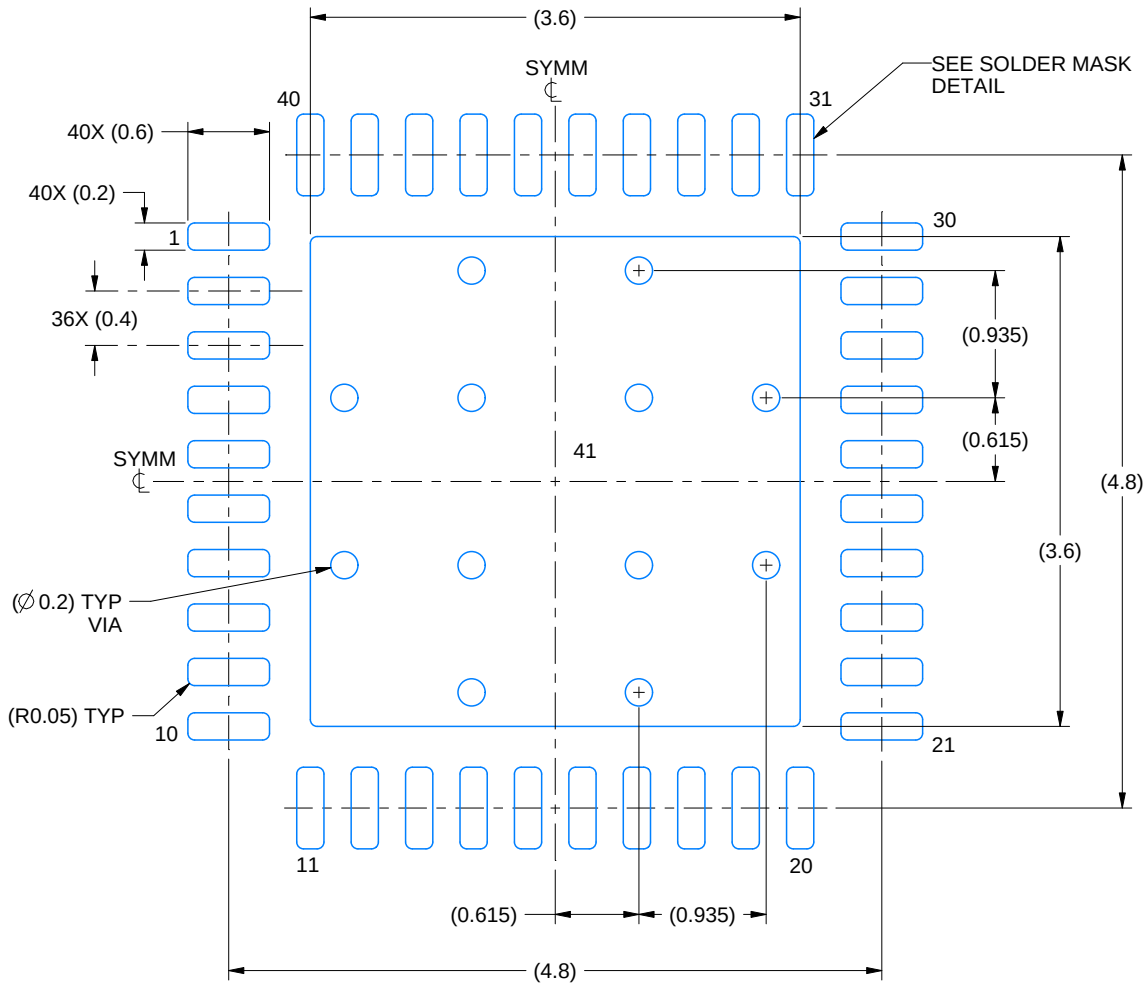
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

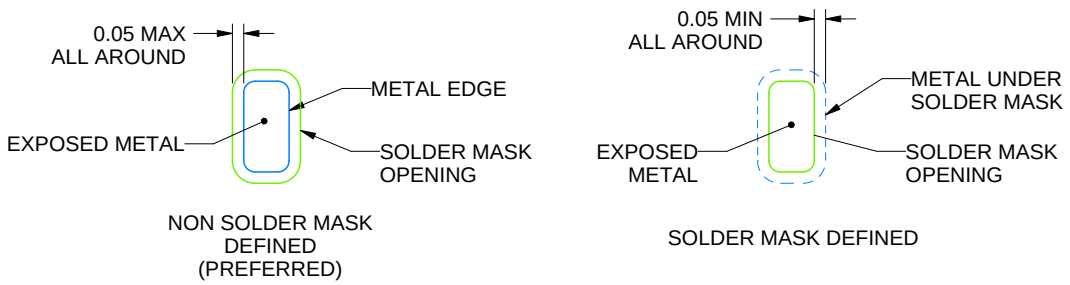


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

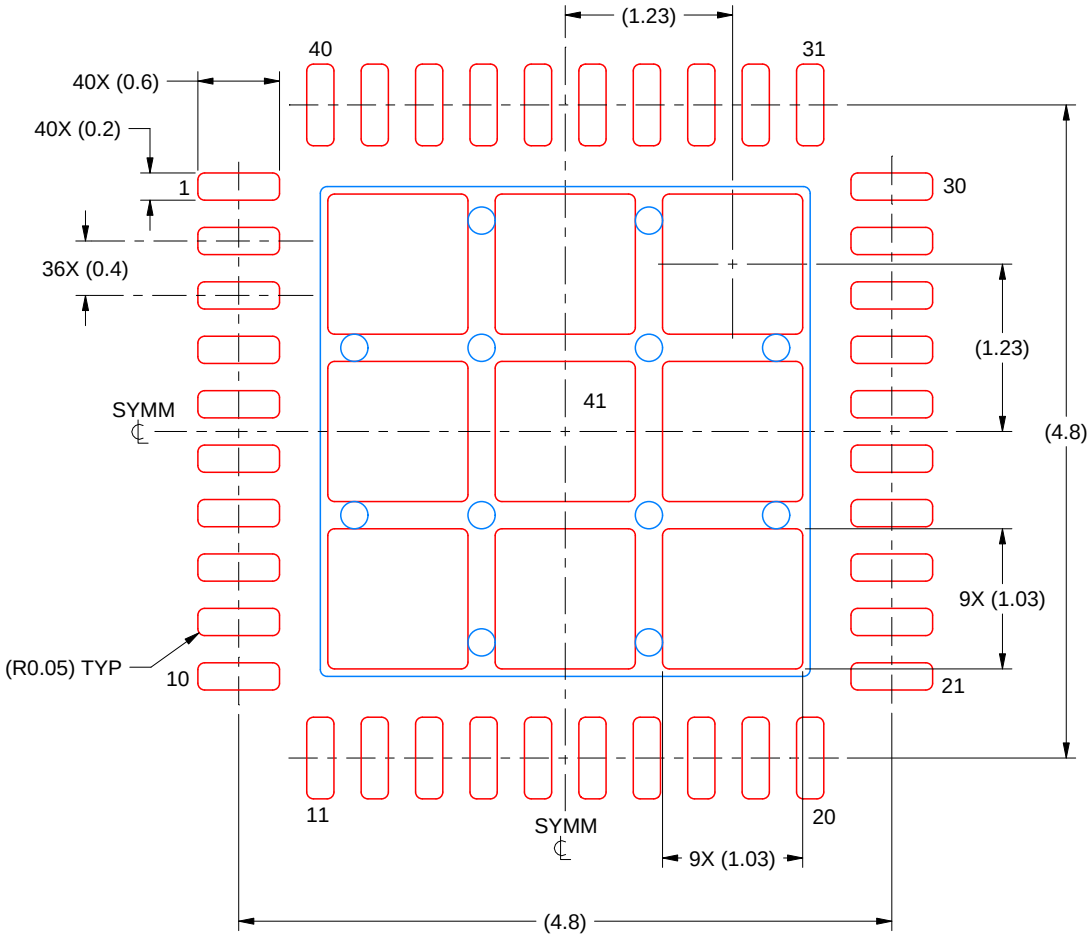


SOLDER MASK DETAILS

4229293/B 03/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 18X

EXPOSED PAD 41
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229293/B 03/2024

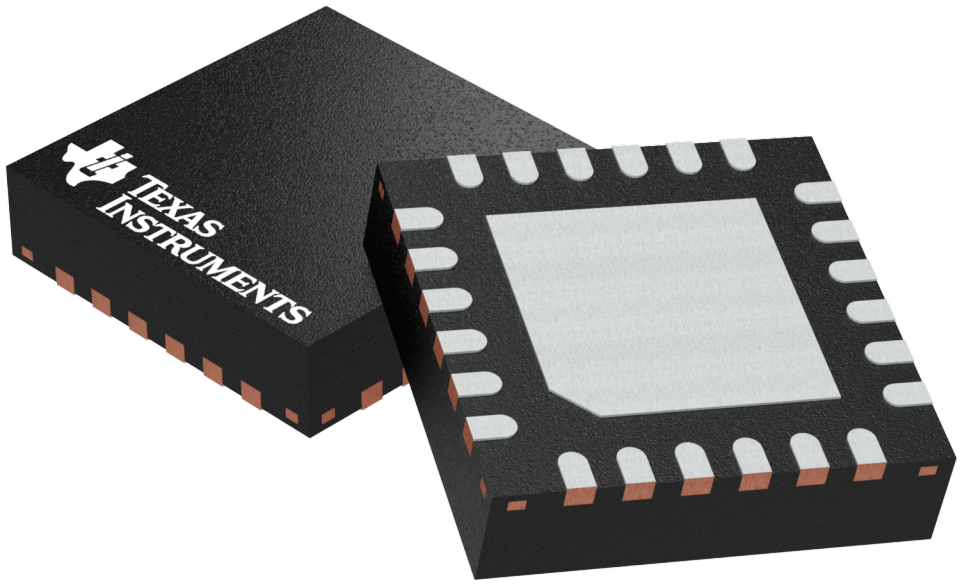
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

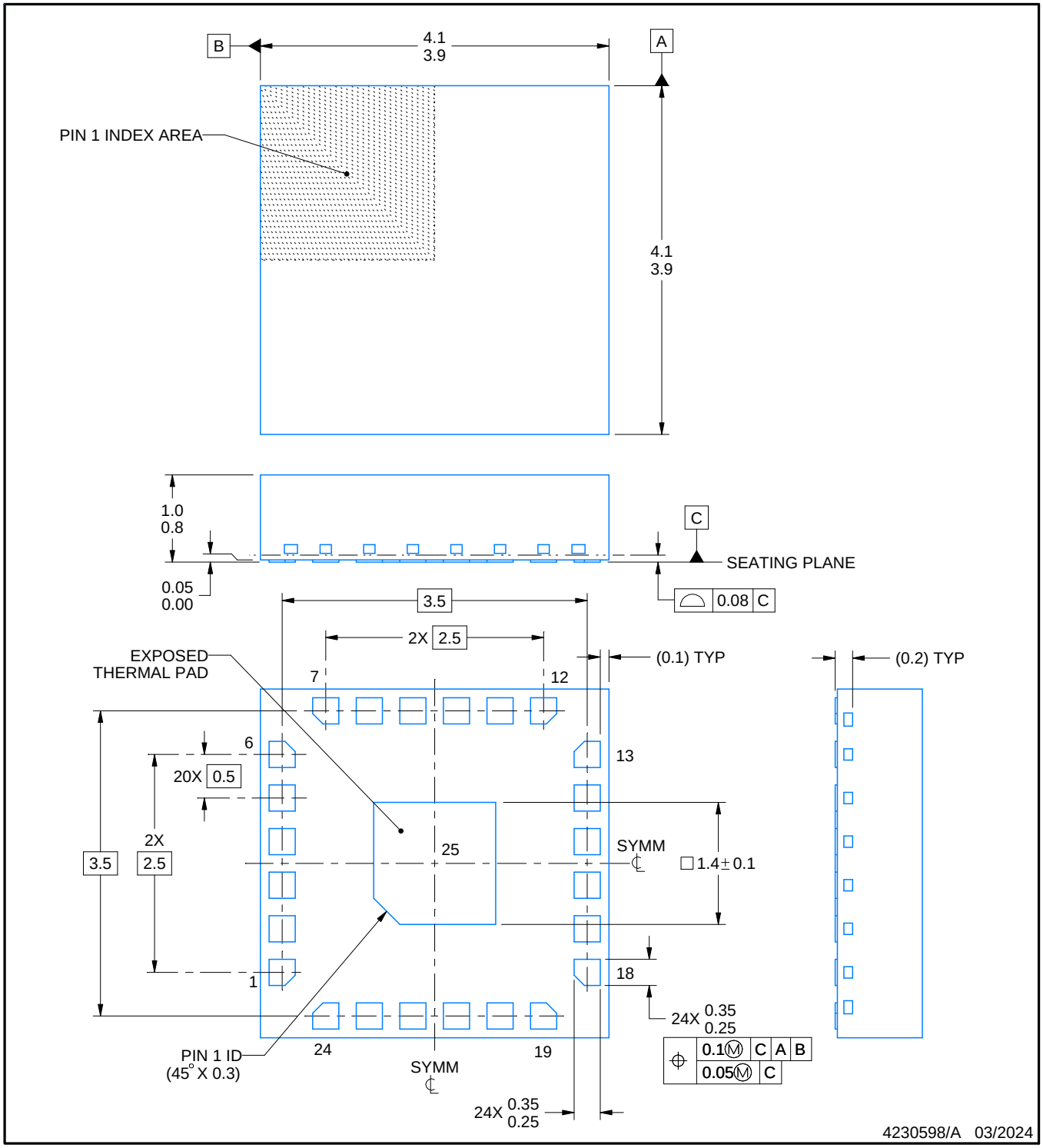
4204104/H

PACKAGE OUTLINE

RGE0024AA

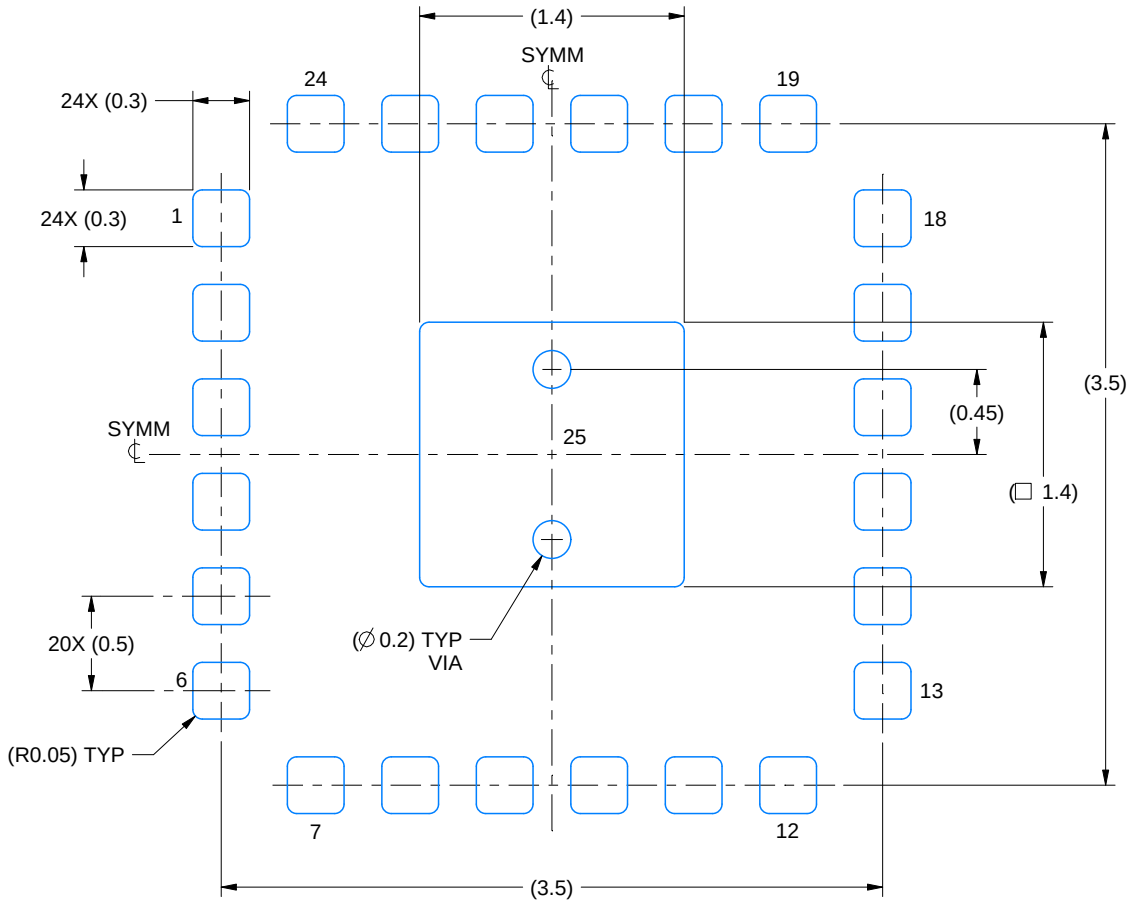
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

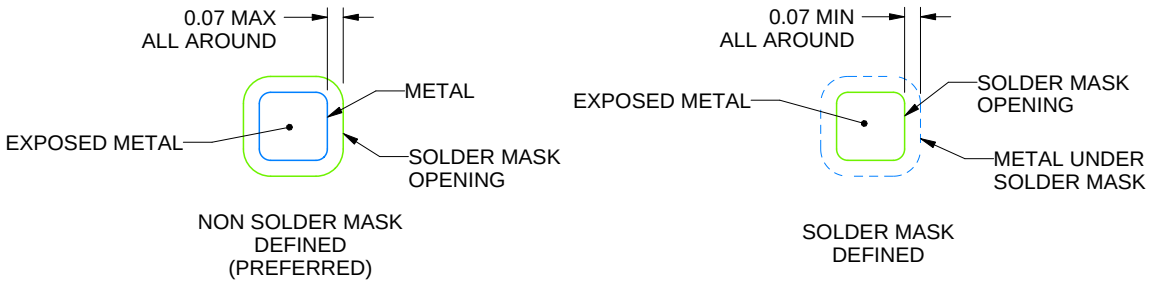


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

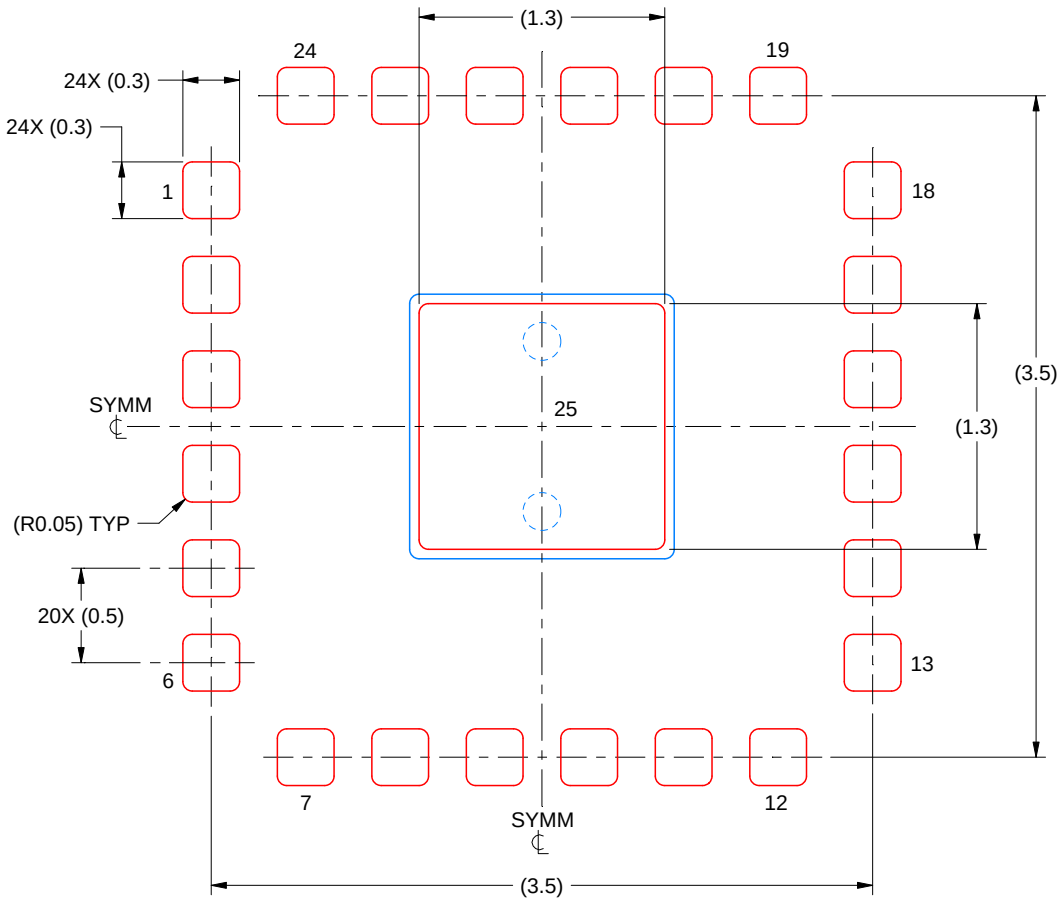


SOLDER MASK DETAILS

4230598/A 03/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 25:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4230598/A 03/2024

NOTES: (continued)

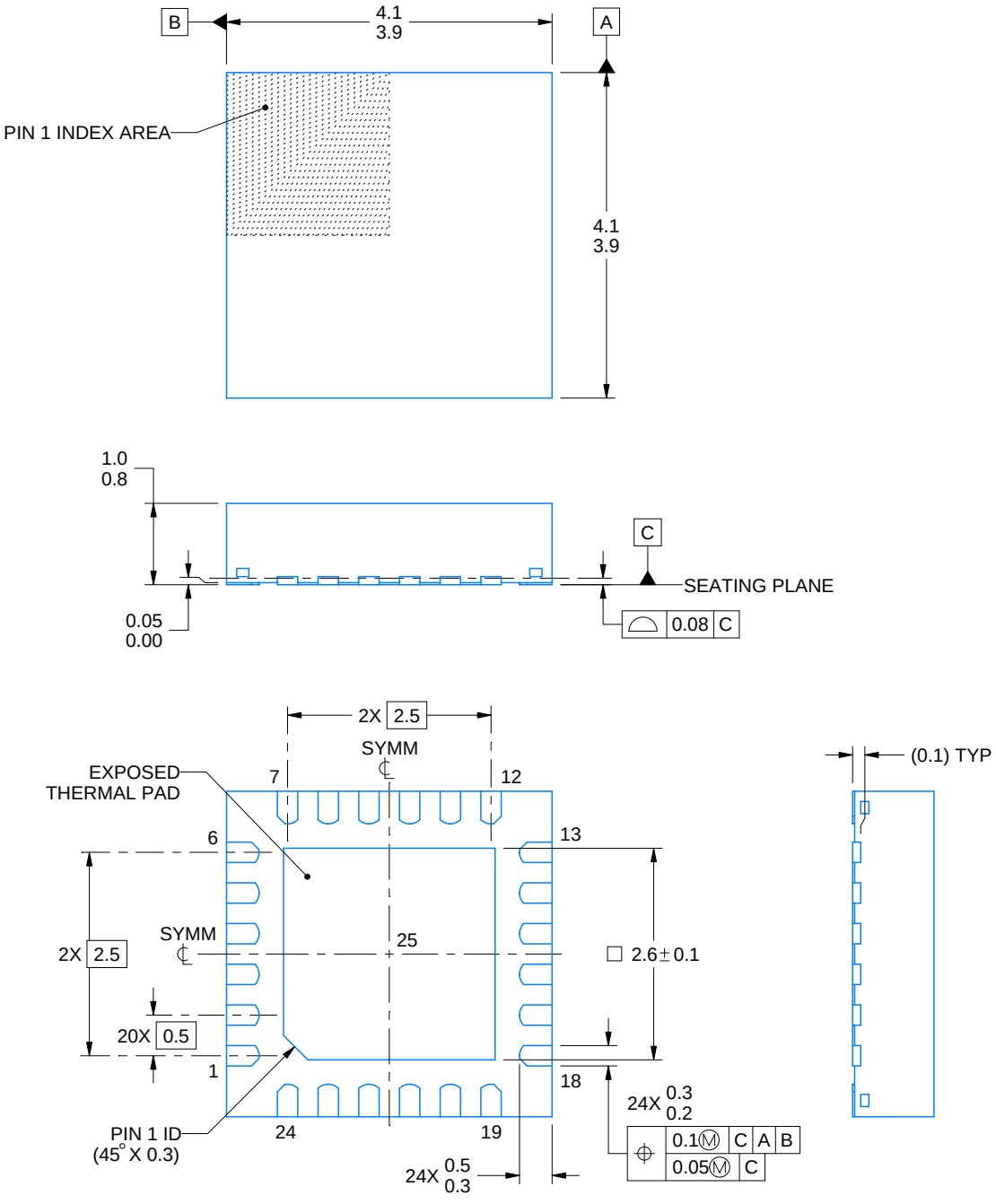
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGE0024AB

PACKAGE OUTLINE

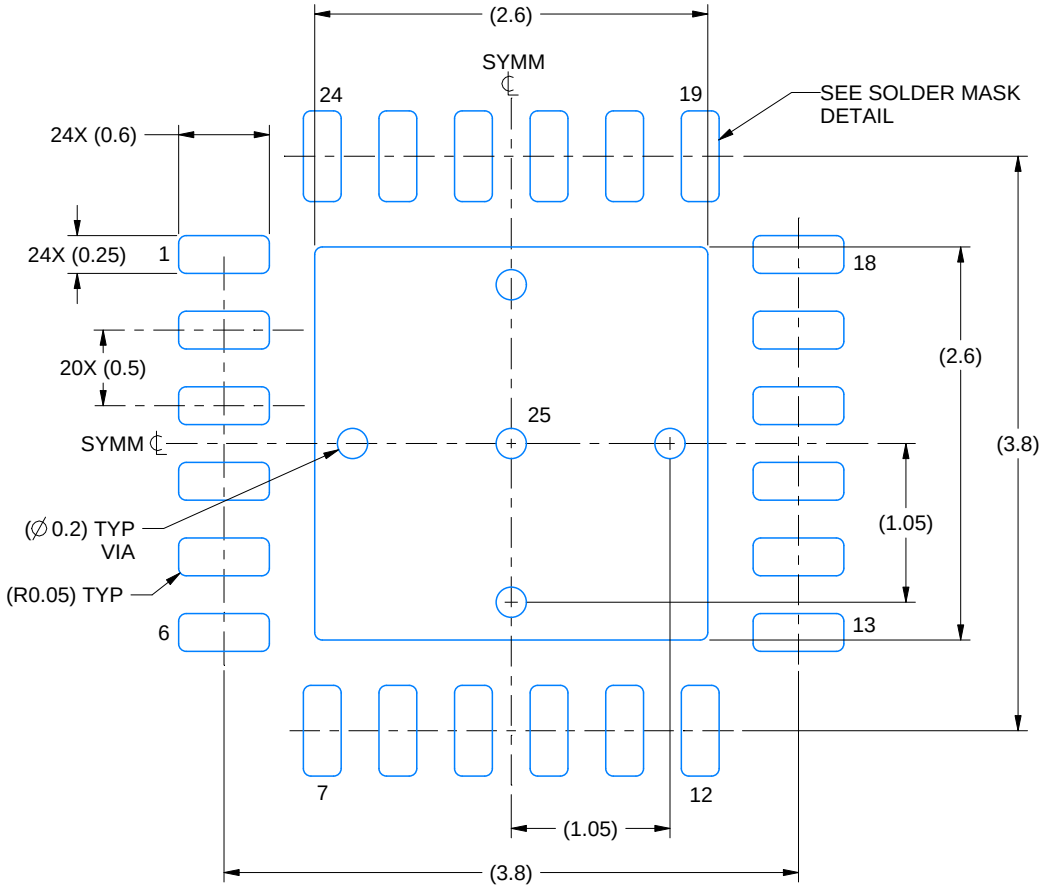
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

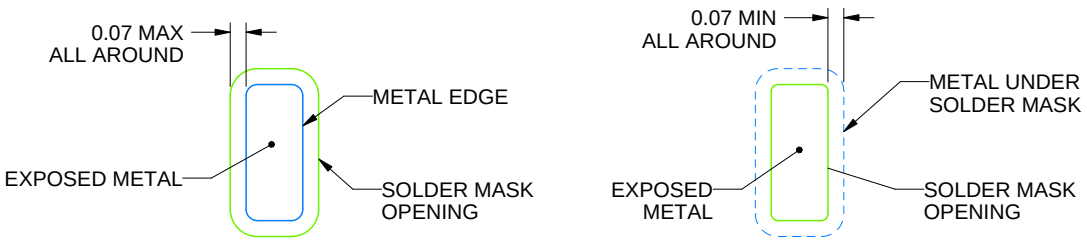


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

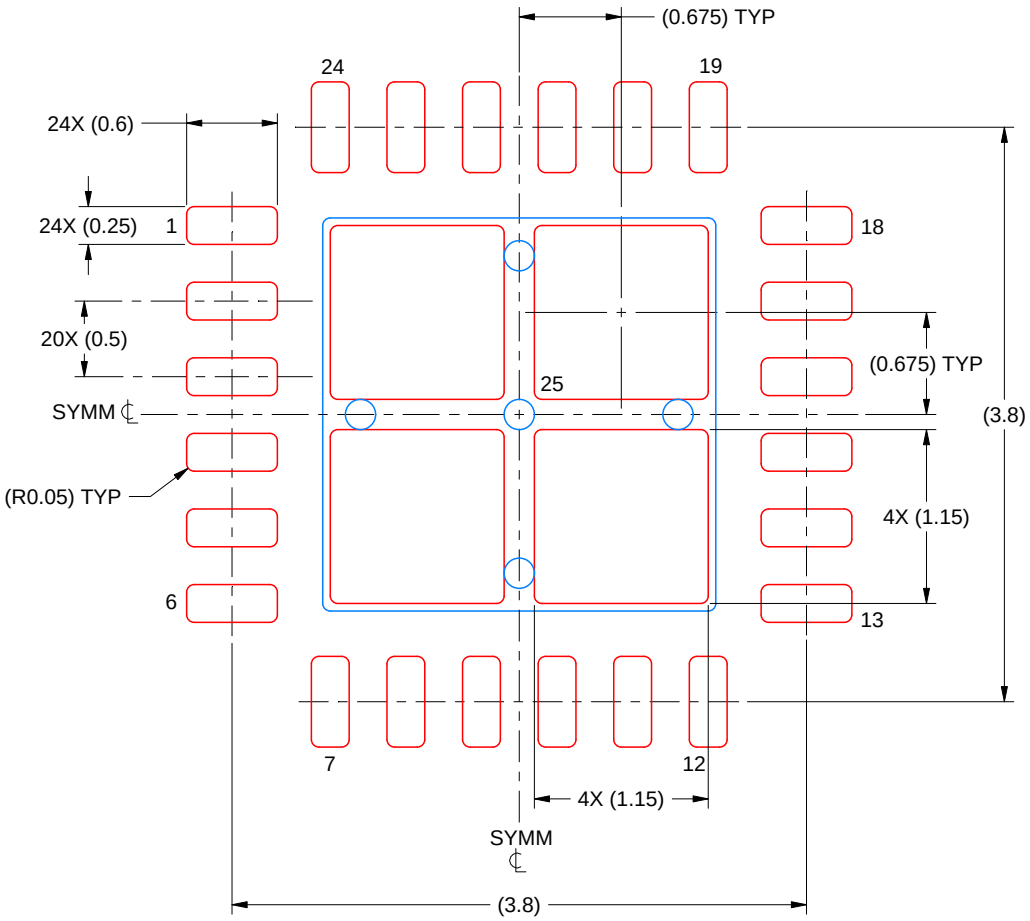
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4230599/A 03/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230599/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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