DS90UH983-Q1 4K DisplayPort/eDP to FPD-Link IV Bridge Serializer With HDCP

1 Features

- DisplayPort receiver
  - DP/eDP v1.4 compatible
  - Supports data lane swap and polarity inversion
  - HBR3/HBR2/HBR/RBR link bit rates
  - Main link: 1, 2, or 4 lanes
  - Each lane up to 8.1Gbps
  - AUX CH 1Mbps
  - Hot plug detect (HPD)
  - Multi-display (MST) and SST support
  - Supports Symmetric and Asymmetric MST
  - Daisy chaining and splitting
  - SuperFrame unpacking capability
  - Suitable for 4K at 60Hz video resolution
- FPD-Link IV interface
  - Supports 13.5/12.528/10.8/6.75/3.375Gbps per channel; Up to 27Gbps over dual channels
  - Coax/STP interconnect support
  - Port splitting to enable Y-cable interfaces
  - MST and SuperFrame based data splitting to different FPD channels
- Ultra-low latency control channel
  - Three fast-mode plus I^2C up to 1MHz (up to 3.4MHz for local bus access)
  - High speed GPIOs
- Backwards compatibility
  - IVI 94x and 92x product families
- Security and diagnostics
  - Integrated HDCP v1.4 with on-chip keys for FPD-Link III
  - Link diagnostics
  - Voltage and temperature monitoring
  - Line fault detection
  - BIST and pattern generation
  - CRC and error diagnostics
  - ECC error correction for control bits
  - Replica mode for redundancy
- Advanced link robustness and EMC control
  - Spread Spectrum Clocking (SSC) input support
  - Spread Spectrum Clocking Generation (SSCG)
  - Data scrambling
- Low power operation
  - 1.8V and 1.15V dual power supply
- AEC-Q100 qualified for automotive applications
  - AEC-Q grade-level 2, –40°C to 105°C
  - 64 pin QFN wettable flanks 9mm × 9mm
  - ISO 10605 and IEC 61000-4-2 ESD compliant

2 Applications

- Automotive displays:
  - Central Information Displays (CID)
  - Rear Seat Entertainment (RSE)
  - Digital instrument clusters
  - Head units and HMI modules
  - Head Up Display (HUD)
  - Rear view and side mirror displays

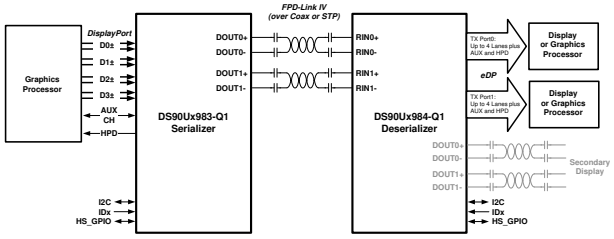
3 Description

The DS90UH983-Q1 is a DisplayPort/eDP to FPD-Link III/IV bridge device. In conjunction with an FPD-Link IV deserializer, the chipset provides a high-speed serialized interface over low-cost 50Ω coax or STP cables. The DS90UH983-Q1 is a VESA DP Standard v1.4 compatible device that supports advanced features such as MST, HBR3, and SuperFrame formats. The device is capable of supporting video resolution up to 4K resolutions with 30-bit color. 8b10b encoded DP data is serialized onto an FPD-Link IV interface output. The FPD-Link IV interface supports video and audio data transmission and full duplex control, including I^2C, and GPIO data over a single channel or dual channels. Consolidation of video data and control over FPD-Link IV lanes reduces the interconnect size and weight and simplifies system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, SSCG, and randomization. In backward compatible mode, the device supports up to 720p and 1080p resolutions with 24 bit color depth over a single/dual link as well as HDCP v1.4 support when paired with an HDCP-capable deserializer.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGING SIZE(2)
DS90UH983-Q1	RTD (VQFN, 64)	9mm × 9mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device and Documentation Support....3
4.1 Documentation Support....3
4.2 Receiving Notification of Documentation Updates....3
4.3 Support Resources....3
4.4 Trademarks....3
4.5 Electrostatic Discharge Caution....3
4.6 Glossary....3
5 Revision History....3
6 Mechanical, Packaging, and Orderable Information....4

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4 Device and Documentation Support

4.1 Documentation Support

4.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Soldering Specifications* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Leadless Leadframe Package (LLP)* application note
- Texas Instruments, *LVDS Owner's Manual*
- Texas Instruments, *I2C Communication Over FPD-Link III with Bidirectional Control Channel* application note
- Texas Instruments, *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* application note
- Texas Instruments, *I2C Bus Pullup Resistor Calculation* application note
- Texas Instruments FPD-Link Learning Center, *FPD-Link Fundamental Material* video series
- Texas Instruments, *Ten tips for successfully designing with automotive EMC/EMI requirements*
- Texas Instruments, *Serial Line-Fault Detection* (Contact TI)

4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.4 Trademarks

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4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2024	*	Initial Release

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6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UH983RTDRQ1	Active	Production	VQFN (RTD) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	UH983
DS90UH983RTDRQ1.A	Active	Production	VQFN (RTD) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	UH983
DS90UH983RTDTQ1	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	Call TI | Nipdauag	Level-3-260C-168 HR	-40 to 105	UH983
DS90UH983RTDTQ1.A	Active	Production	VQFN (RTD) | 64	250 | SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 105	UH983

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

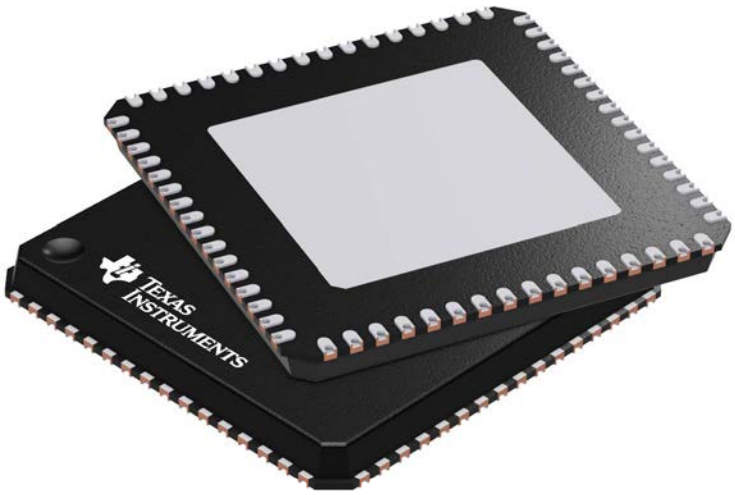
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GENERIC PACKAGE VIEW

RTD 64 VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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