

Table of Contents

1 Introduction.....	2
2 Setting Vout.....	2
3 Optional Components.....	2
4 PCB Layout Diagrams.....	4

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1 Introduction

The LM3475 evaluation board is provided as a tool for developing DC/DC converters based on the LM3475 IC. As shown in [Figure 3-1](#), the evaluation board is configured to provide an output of 2.5 V at up to 2 A from an input up to 10 V. The corresponding bill of material is given in [Table 3-1](#). Typical efficiencies are shown in [Figure 3-2](#) and [Figure 3-3](#). [Figure 4-1](#) and [Figure 4-2](#) show the board layout.

To aid in the design and evaluation of DC/DC buck converters based on the LM3475 controller, the LM3475 evaluation board can be easily re-configured for different output voltages.

2 Setting V_{out}

V_{out} can be set using R_{FB1} , as shown in [Equation 1](#):

$$V_{out} = V_{FB} \times (R_{FB1} + R_{FB2}) / R_{FB2} \quad (1)$$

where

- V_{FB} is 0.8 V typically.

See the device-specific data sheet before changing any component values since additional design adjustments can be required.

3 Optional Components

A feedforward capacitor, C_{FF} , is placed on the board, which will increase operating frequency. However, the speed up effect decreases with lower output voltage and is negligible below 1.6-V output.

A 0 Ω is used to pull up the EN pin for always on operation. The enable pin can be pulled low at the EN post to shutdown the device. If this resistor is removed, any analog level signal can be used to enable and disable the device.

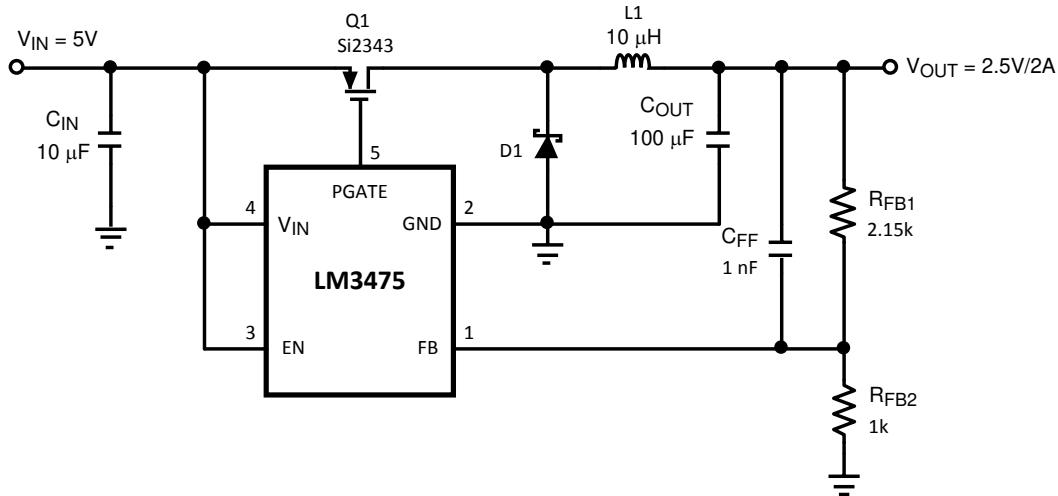


Figure 3-1. Full Demo Board Schematic

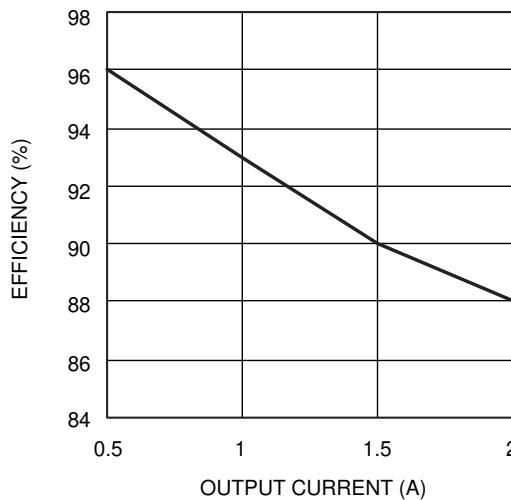


Figure 3-2. Efficiency vs Output Current ($V_{IN} = 5$ V)

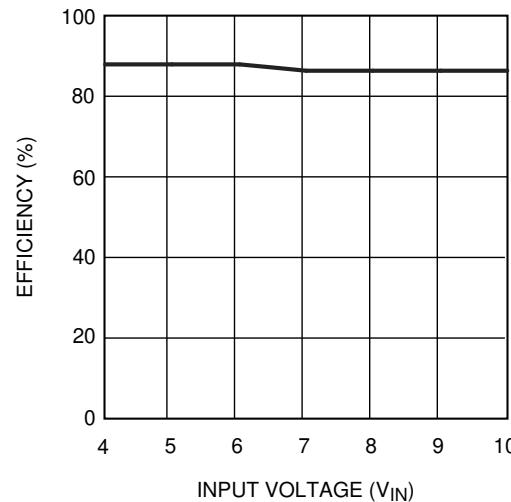


Figure 3-3. Efficiency vs Input Voltage ($I_{out} = 2$ A)

Table 3-1. Bill of Materials (BOM)

Designator	Part Description	Part Number
CIN	10 μ F, 16-V ceramic	Yuden EMK325BJ106MN
COUT	100 μ F, 6-V tantalum	AVX TPSY107M006R0100
CFF	1 nF, 25-V ceramic	VJ1206Y102KXXA
D1	Schottky 20 V, 2 A	Central CMSH2-20L
L1	10 μ H, 3.1 A	Sumida CDRH103R100
Q1	Si 2343 30 V, 2.5 A	Vishay Si2343
RFB2	1 k Ω	Vishay CRCW08051001F
RFB1	2.15 k Ω	Vishay CRCW08052151F
R2	0 Ω	Vishay CRCW08050R00F

4 PCB Layout Diagrams

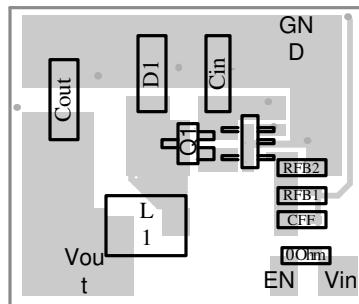


Figure 4-1. Top Side Layout

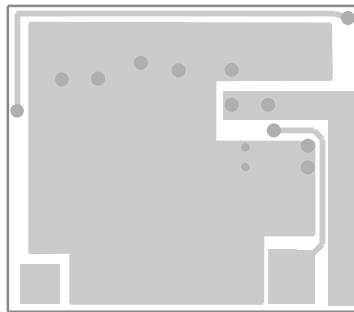


Figure 4-2. Bottom Side Layout

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