EVM User's Guide: LMG708B0-EVM12V

LMG708B0 12V_{OUT}, 20A, 400kHz, Single-Phase GaN Buck Converter Evaluation Module

Description

The LMG708B0-EVM12V evaluation module (EVM) is designed to showcase the LMG708B0 GaN synchronous buck converter. The EVM operates over a DC input voltage range of 24V to 65V to deliver a 12V regulated output at up to 20A.

Get Started

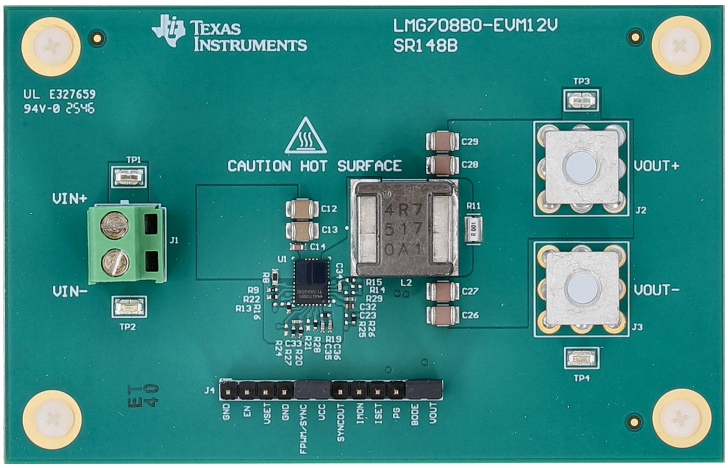
1. Order the LMG708B0-EVM12V.
2. Refer to the LMG708B0 product folder.
3. Review the Altium PCB layout source files.
4. Use the LMG708B0 quickstart calculator to assist with component selection in your design.
5. Simulate the design using PSPICE or SIMPLIS.

Features

- GaN buck converter enables ultra-high efficiency
  - 97% at 48V_{IN}, 12V_{OUT}, 20A, 400kHz
  - Low dead-time switching minimizes power loss and temperature rise
  - Bias power derived from the 12V output
- Maximum DC input of 65V, transients to 80V
  - V_{IN} UVLO thresholds set at 21V (on), 19V (off)
- Switching frequency of 400kHz synchronizable ±20% with an external clock signal
- Input π-stage EMI filter helps meet CISPR 32
  - Spread spectrum (DRSS) option for lower electromagnetic interference (EMI)
  - Electrolytic capacitor for parallel damping
- Peak current-mode control architecture provides fast line and load transient response
  - Optional constant-current (CC) loop with adjustable setpoint (ISET) and seamless transition between CV and CC modes
  - Forced PWM (FPWM) or pulsed frequency modulation (PFM) modes of operation
- Integrated protection features for robust design
  - Overcurrent protection (OCP) with low-loss shunt current sensing
  - Monotonic prebias output voltage start-up
  - Internal soft-start time set to 2.75ms, adjustable with the VSET input
  - Power-good (PG) indicator
  - Current monitor (IMON) output
- Fully assembled, tested and proven PCB layout with 3.9" × 2.5" (99mm × 63mm) total footprint

Applications

- Data center compute: power distribution board with 48V input
- Data center networking: optical module
- Industrial: test and measurement, robotics



LMG708B0 Single-Phase EVM, 99mm × 63mm

1 Evaluation Module Overview

1.1 Introduction

The LMG708B0-EVM12V evaluation module (EVM) is a synchronous buck regulator that demonstrates ultra-high conversion efficiency in a small footprint. The EVM design uses the LMG708B0 20A GaN buck converter IC, which enables high conversion efficiency and incorporates the following key features:

- Integrated GaN power FETs, buck controller and bootstrap circuit
  - High-efficiency GaN HEMT power devices
    - Low $R_{DS(on)}$ × Q_{SW} and $R_{DS(on)}$ × Q_{OSS} figures-of-merit (FoM)
    - No body diode reverse recovery effect
    - Wide V_{IN} range up to 80V maximum
  - Thermally enhanced package (TEP)
    - Optional top-side cooling (TSC) with exposed package connections (SW, PGND)
    - Low parasitic inductance for quiet switching performance
- Peak current-mode control loop architecture with low PWM minimum on-time
  - Multiphase capability
    - Stackable with intelligent SYNC clock phasing set by the CNFG resistor
    - FPWM/SYNC of the primary IC and FB of the secondary ICs set the operating mode
  - Optional constant-current (CC) regulation for battery charging and other current-source type loads
    - Dynamically adjustable current setpoint (ISET)
    - Output current monitoring (IMON)
- Optional dual-random spread spectrum (DRSS) modulation for lower measured EMI

The EVM operates over a wide input voltage range of 24V to 65V, providing a regulated output voltage of 12V. With better than 1% setpoint accuracy, the output voltage is adjustable by modifying the feedback resistor values, permitting the user to customize the output voltage up to 15V if needed.

Inherent protection features for robust design include input supply voltage UVLO, power-good (PG) indicator, current monitor (IMON) output, adjustable soft-start time, hiccup-mode overcurrent protection, and thermal shutdown with hysteresis.

The selected power-train passive components – including the 4.7µH buck inductor, 1mΩ/0508 shunt with wide aspect ratio, 10µF/100V/X7S/1210 ceramic input capacitors, and 22µF/25V/X7R/1210 ceramic output capacitors – are available from multiple component vendors. An optional 100µF/16V/12mΩ polymer-electrolytic output capacitor helps to support particularly demanding load-transient specifications.

1.2 Kit Contents

- A complete 12V_{OUT}, 20A buck regulator EVM, including the LMG708B0 GaN buck converter IC
- EVM Disclaimer Read Me

1.3 Specifications

The following table lists the EVM specifications. V_{IN} = 48V, V_{OUT} = 12V, F_{SW} = 400kHz, unless otherwise indicated.

Table 1-1. Electrical Performance Characteristics

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage, V_{IN}	DC operating		24	48	65	V
	Transient				80	V
Input UVLO turn-on threshold, V_{IN-ON}	R_{UV1} = 200kΩ, R_{UV2} = 10kΩ			21		V
Input UVLO turn-off threshold, V_{IN-OFF}				19		
Input supply current, no load, FPWM, $I_{IN-NL(FPWM)}$	I_{OUT} = 0A, FPWM/SYNC tied to VCC	V_{IN} = 24V		22		mA
		V_{IN} = 36V		25		
		V_{IN} = 48V		26		
		V_{IN} = 60V		25		
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT}	Fixed output setting (or adjustable output setting with 100kΩ and 9.09kΩ feedback divider)(1)		11.9	12	12.1	V
Output voltage adjustment range, $V_{OUT-ADJ}$	With suitable BOM changes(2)		3.3		15	V
Output current, I_{OUT}	Electrical design current (EDC)			20		A
	Thermal design current (TDC)(3), airflow = 100LFM(4)			15		A
Output voltage regulation in FPWM, ΔV_{OUT}	Load regulation	I_{OUT} = 0A to 20A		4		mV
	Line regulation	V_{IN} = 24V to 65V		4		
Output voltage ripple, V_{OUT-AC}	I_{OUT} = 10A			10		mV_{RMS}
Output overcurrent protection, $I_{OUT-OCP}$	R_S = 1mΩ, IMON tied to GND			26		A
Output average current limit, I_{OUT-CC}	R_{IMON} = 8.66kΩ			22		A
Soft-start time, t_{SS}	VSET pin open circuit			2.7		ms
Hiccup time, t_{RES}	16384 clock cycles			41		ms
SYSTEM CHARACTERISTICS						
Switching frequency, F_{SW}	R_{RT} = 54.9kΩ			400		kHz
Synchronization frequency range, F_{SYNC}			320		480	kHz
Half-load efficiency, η_{FULL} (1)	I_{OUT} = 10A	V_{IN} = 24V		98.3%		
		V_{IN} = 36V		97.7%		
		V_{IN} = 48V		97.9%		
		V_{IN} = 60V		97.2%		
Full-load efficiency, η_{FULL} (1)	I_{OUT} = 20A	V_{IN} = 24V		97.5%		
		V_{IN} = 36V		97.2%		
		V_{IN} = 48V		97.0%		
		V_{IN} = 60V		96.7%		
LMG708B0 case temperature, T_C			–40		135	°C

(1) The default output voltage of this EVM is 12V. Efficiency and other performance metrics can change based on the operating input voltage, load current, ambient temperature, externally-connected output capacitors and other parameters.
(2) See Table 4-2 and Table 4-3 for BOM changes related to 5V and 3.3V output designs, respectively.
(3) EDC and TDC can differ, for example when the application requires short-duration transients to a high-current amplitude that does not substantially increase the operating temperatures of the power-stage components.
(4) The recommended airflow is 100LFM when operating at loads above 15A at 25°C ambient temperature. Higher ambient temperatures require increased airflow or heatsinking to keep the GaN IC case temperature below 135°C. See Section 3.1.3.

1.4 Device Information

The LMG708B0 is a GaN switching DC/DC converter that features all of the functions necessary to implement a high-efficiency CC/CV synchronous buck regulator operating over a wide input voltage range from 5V to 80V. This easy-to-use converter integrates high-side and low-side GaN FETs capable of delivering 20A. Predictive dead time control is designed to minimize power dissipation during switching transitions. The LMG708B0 comes in a 4.5mm × 6mm, thermally enhanced, 22-pin eQFN package using a flip-chip routable leadframe (FCRLF) packaging technique. Leveraging high-performance GaN power FETs, thermal management and EMI mitigation features, CC/CV operation, and small design size, the LMG708B0 represents an excellent point-of-load regulator choice for applications requiring the most efficient GaN design with useable current, lifetime reliability, and cost advantages.

To optimize component selection and examine predicted efficiency performance across line and load ranges, download the LMG708B0 quickstart calculator.

1.4.1 Application Circuit Diagrams

Figure 1-1 shows an LMG708B0 synchronous buck regulator with adjustable output voltage set by feedback resistors designated as R_{FB1} and R_{FB2}. Alternatively, tying the FB pin high or low establishes fixed output settings of 12V and 5V, respectively. Defined by components R_{COMP}, C_{COMP} and C_{HF}, a type-II compensation network facilitates setting the CV loop crossover frequency and phase margin to meet a target load transient response specification.

The BIAS input derives current from the output (at voltages above the 4.6V switchover threshold) to achieve lower IC power loss and improved efficiency at light loads in particular. Resistor R_{IMON} sets the CC loop setpoint and capacitor C_{IMON} provides CC loop stability. Lastly, resistors R_{UV1} and R_{UV2} set the input UVLO turn-on and turn-off voltage thresholds. Not shown in Figure 1-1 is an EMI filter stage at the input.

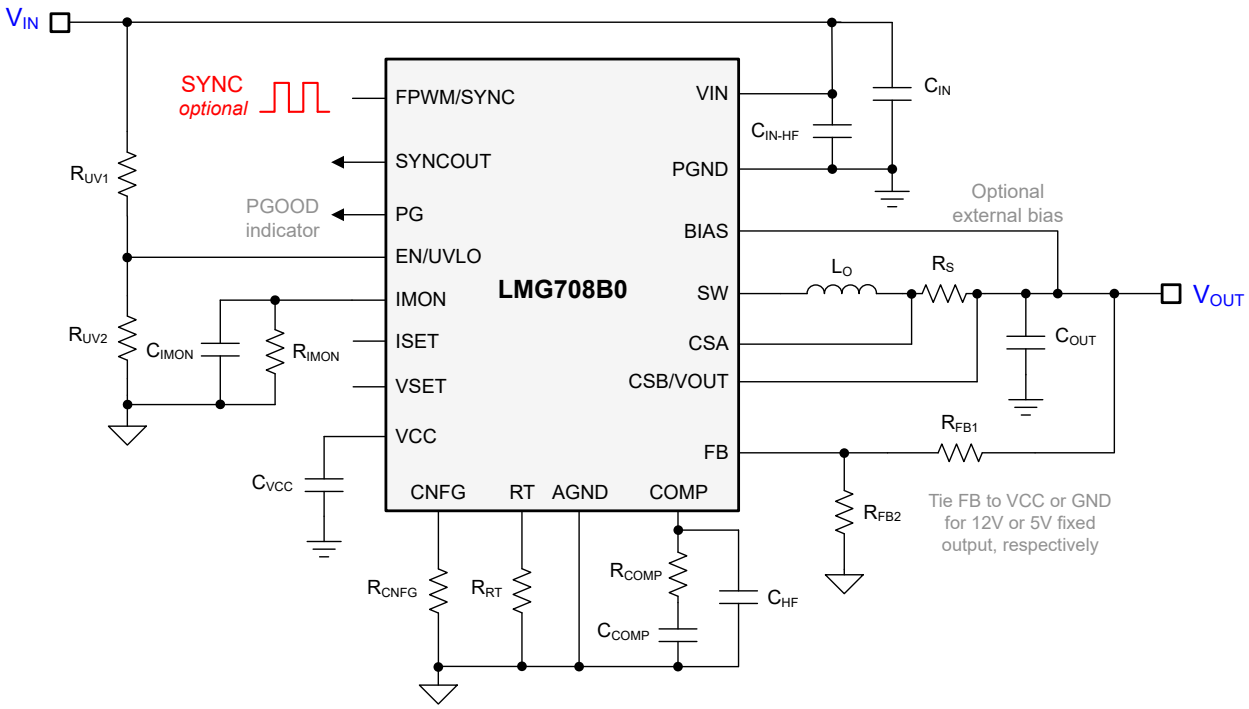


Figure 1-1. LMG708B0 GaN Synchronous Buck Regulator Simplified Schematic

For higher output current capability, as shown in Figure 1-2, the user can implement a two-phase buck regulator by connecting SYNCOUT of the primary IC to FPWM/SYNC of the secondary. Setting the CNFG resistor to 23.7kΩ on the primary IC and 0Ω (or 100kΩ) on the secondary IC establishes a two-phase setup with 180° clock synchronization. Also, tie the respective COMP, IMON, VSET, and ISET pins between each converter and revise the compensation components as needed. Tie the IMON pins to GND if CC-loop operation is not required, in

which case VSET and ISET of each IC can be left open circuit. Set FPWM or PFM operating modes by tying FPWM/SYNC of the primary IC and FB of the secondary IC high or low, respectively.

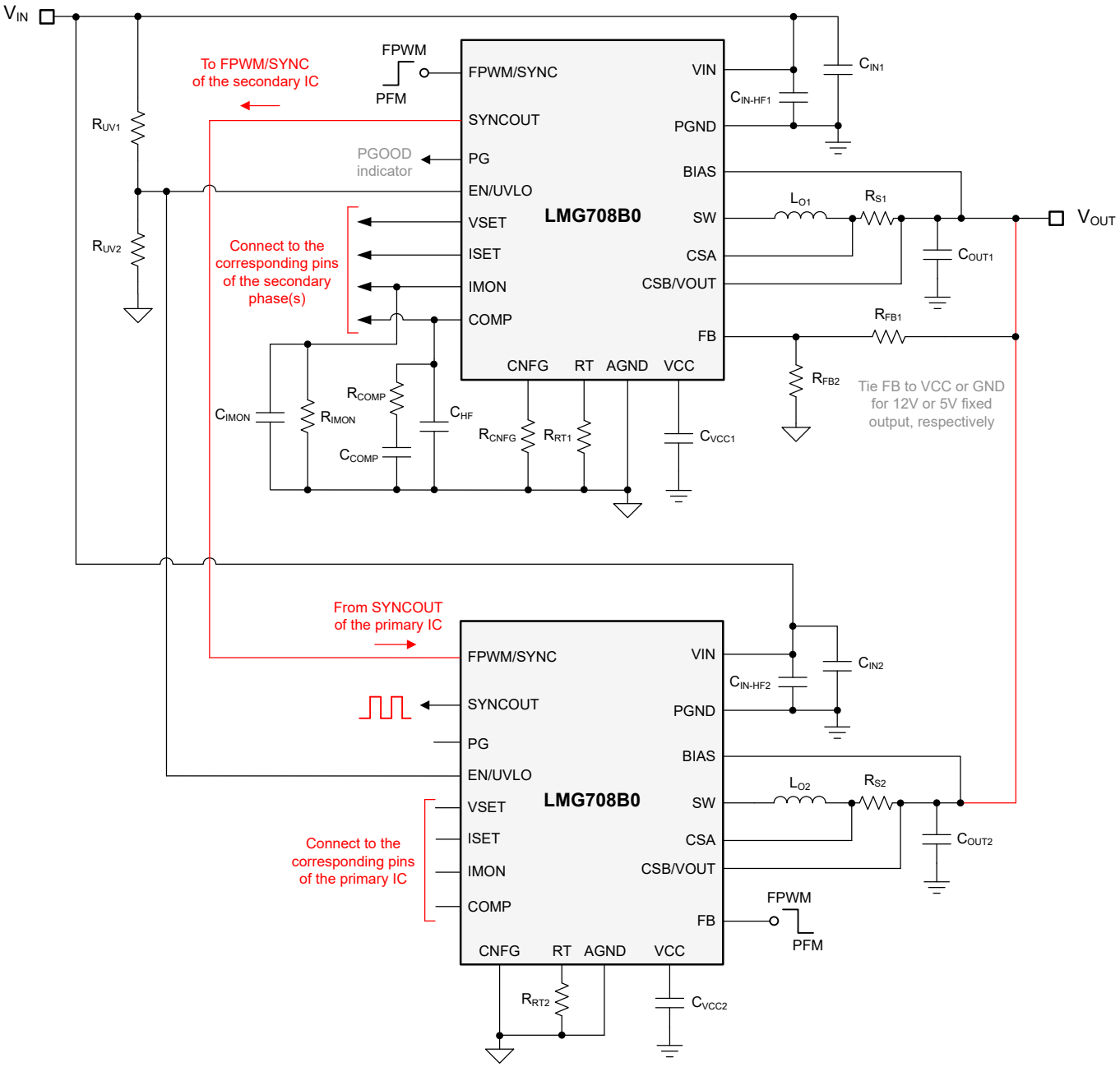


Figure 1-2. LMG708B0 Two-Phase GaN Synchronous Buck Regulator Simplified Schematic

2 Hardware

2.1 Test Setup and Procedure

2.1.1 EVM Connections

Referencing the EVM connections described in Table 2-1 and Figure 2-1 show the recommended test setup to evaluate the LMG708B0-EVM12V. Working at an ESD-protected workstation, verify that any wrist straps, boot straps, or mats are connected and referencing the user to earth ground before handling the EVM.

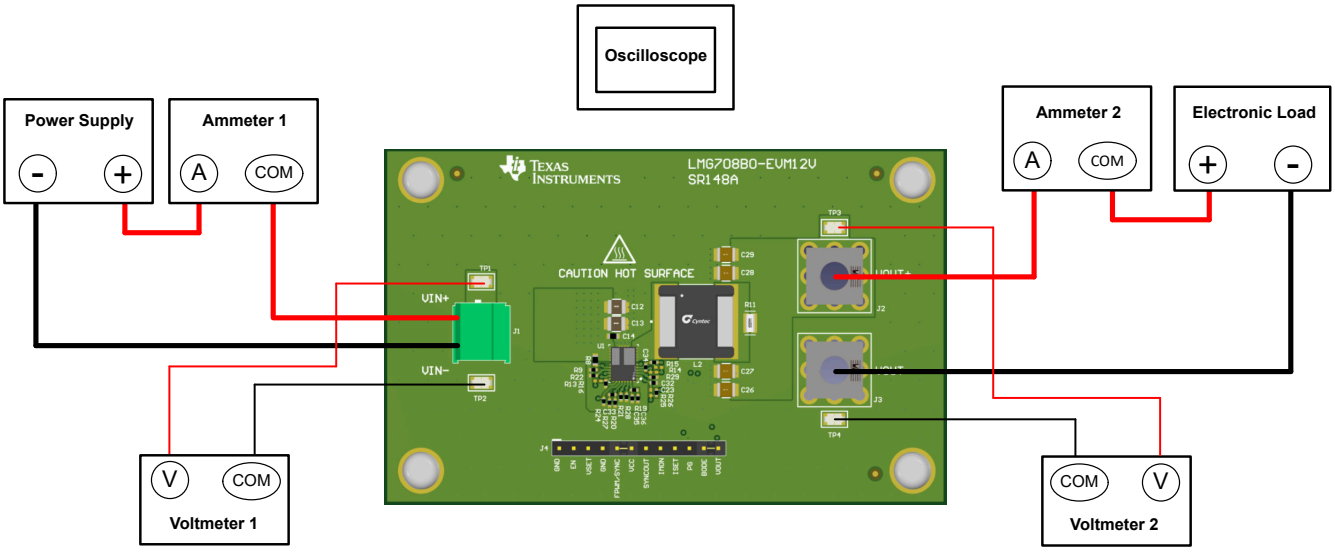


Figure 2-1. EVM Test Setup

Table 2-1. EVM Power Connections

LABEL	DESCRIPTION
VIN+	Positive input voltage power and sense connection
VIN–	Negative input voltage power and sense connection
VOUT+	Positive output voltage power and sense connection
VOUT–	Negative output voltage power and sense connection

Table 2-2. EVM Signal Connections

LABEL	DESCRIPTION
GND	Ground connection
EN	Enable input – tie to GND to disable the converter
VSET	Voltage loop setpoint adjustment
GND	Ground connection
FPWM/SYNC(1)	Mode select or synchronization input
VCC	VCC connection
SYNCOUT	Synchronization output
IMON	Current monitor output
ISET	Current loop setpoint adjustment
PG	Power-good indicator
BODE	Bode plot signal input
VOUT	

(1) A jumper on header J4 connects FPWM/SYNC to VCC.

2.1.2 Test Equipment

Voltage Source: Use an input voltage source capable of supplying 0V to 72V and 12A.

Multimeters:

- **Voltmeter 1:** Input voltage at VIN+ to VIN–. Set the voltmeter to an input impedance of 100MΩ.
- **Voltmeter 2:** Output voltage at VOUT+ to VOUT–. Set the voltmeter to an input impedance of 100MΩ.
- **Ammeter 1:** Input current. Set ammeter to a 1-second aperture time.
- **Ammeter 2:** Output current. Set ammeter to a 1-second aperture time.

Electronic Load: The load must be an electronic constant-resistance (CR) or constant-current (CC) mode load capable of 0A to 20A at 12V. For a no-load input current measurement, disconnect the electronic load (as the load can draw a residual current).

Oscilloscope: With the scope set to 20MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection, as this action can induce additional noise given a large ground loop. Adjust the oscilloscope as needed to measure other waveforms.

Safety: Always use caution when touching any circuits that can be live or energized.

2.1.3 Recommended Test Setup

2.1.3.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 0.1A maximum. Make sure the input source is initially set to 0V and connected to the VIN+ and VIN– connection points as shown in Figure 2-1. TI recommends an additional input bulk capacitor to provide damping when using long input lines.
- Connect voltmeter 1 at the VIN+ and VIN– sense points to measure the input voltage.
- Connect ammeter 1 to measure the input current and set to at least 1-second aperture time.

2.1.3.2 Output Connections

- Connect an electronic load to the output power connections. Set the load to constant-resistance mode or constant-current mode at 0A before applying input voltage.
- Connect voltmeter 2 at VOUT+ and VOUT– sense points to measure the output voltage.
- Connect ammeter 2 to measure the output current.

2.1.4 Test Procedure

2.1.4.1 Line and Load Regulation, Efficiency

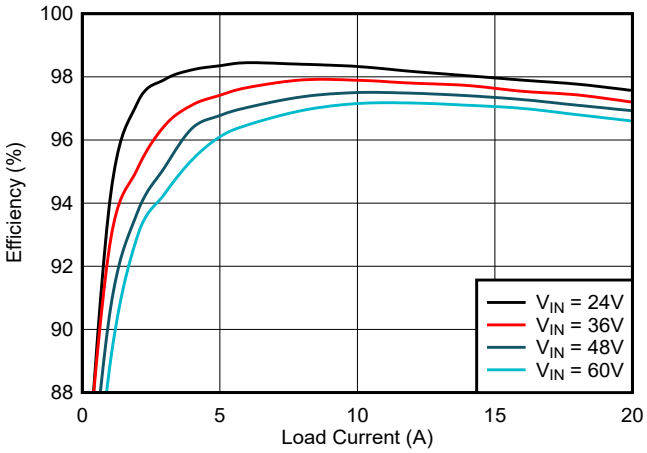
- Set up the EVM as described above.
- Set load to constant resistance or constant current mode and to sink 0A.
- Increase input source from 0V to 48V; use voltmeter 1 to measure the input voltage.
- Increase the current limit of the input supply to 10A.
- Using voltmeter 2 to measure the output voltage, V_{OUT}, vary the load current from 0A to 20A; V_{OUT} must remain within the load regulation specification.
- Set the load current to 10A (50% rated load) and vary the input source voltage from 24V to 65V; V_{OUT} must remain within the line regulation specification.
- Decrease the load to 0A. Decrease the input source voltage to 0V.

3 Implementation Results

3.1 Test Data and Performance Curves

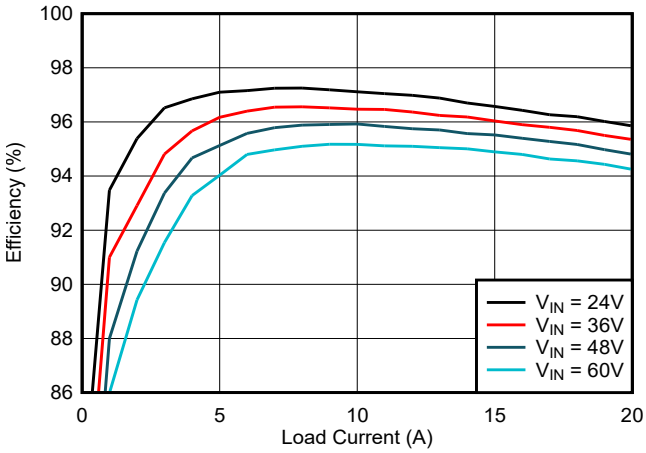
Figure 3-1 through Figure 3-10 present typical performance plots and waveforms for the LMG708B0-EVM12V. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements.

3.1.1 Efficiency



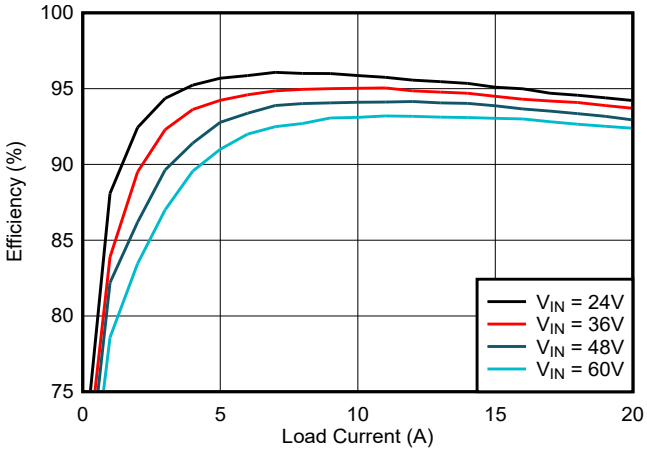
Refer to Table 4-1 for the default BOM with V_{OUT} = 12V.

Figure 3-1. Efficiency, V_{OUT} = 12V, 400kHz, FPWM



Refer to Table 4-2 for component changes to set V_{OUT} = 5V.

Figure 3-2. Efficiency, V_{OUT} = 5V, 400kHz, FPWM



Refer to Table 4-3 for component changes to set V_{OUT} = 3.3V.

Figure 3-3. Efficiency, V_{OUT} = 3.3V, 250kHz, FPWM

3.1.2 Operating Waveforms

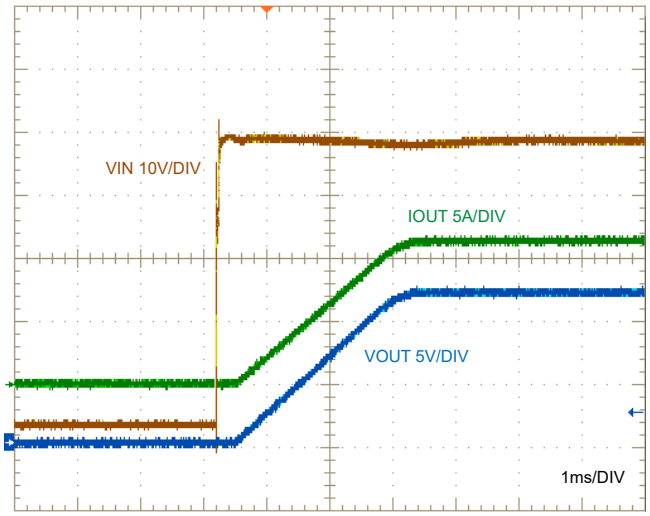


Figure 3-4. Start-Up Characteristic, V_{IN} Stepped to 48V, I_{OUT} = 12A Resistive

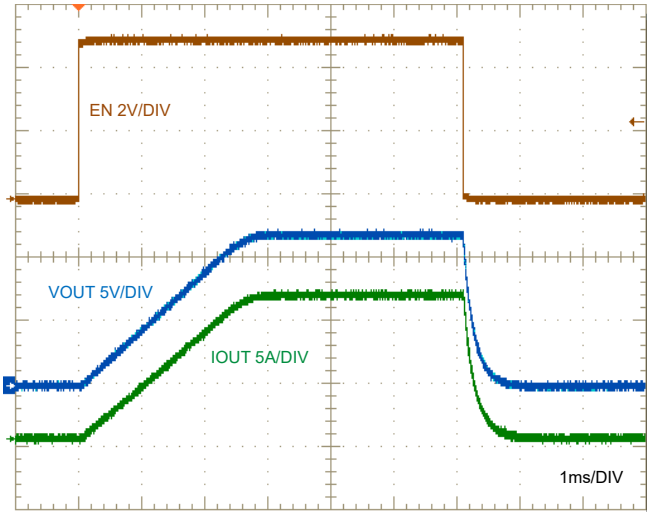


Figure 3-5. ENABLE ON and OFF, V_{IN} = 48V, I_{OUT} = 12A Resistive

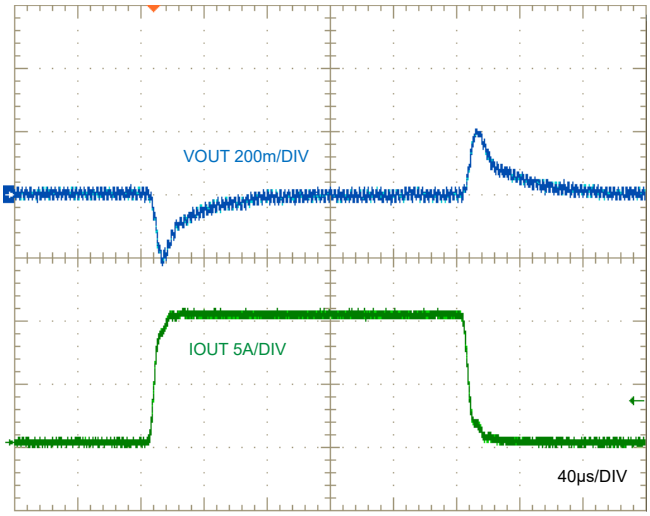


Figure 3-6. Load Transient Response, V_{IN} = 48V, FPWM, 0A to 10A at 1A/µs

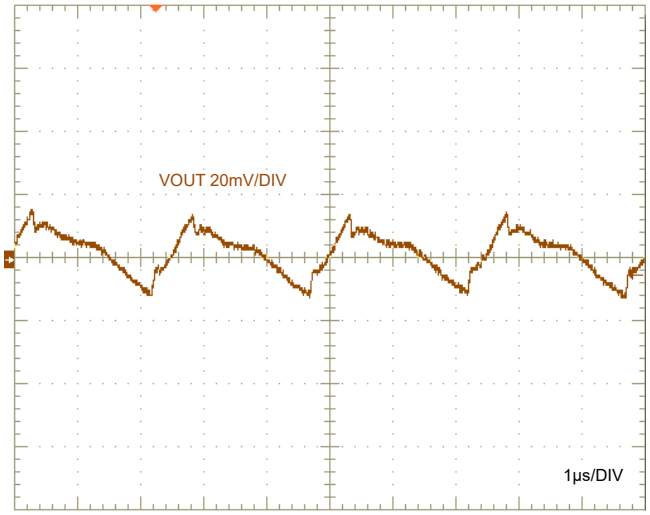


Figure 3-7. Output Voltage Ripple, V_{IN} = 48V, I_{OUT} = 10A, 20MHz Bandwidth

3.1.3 Thermal Performance

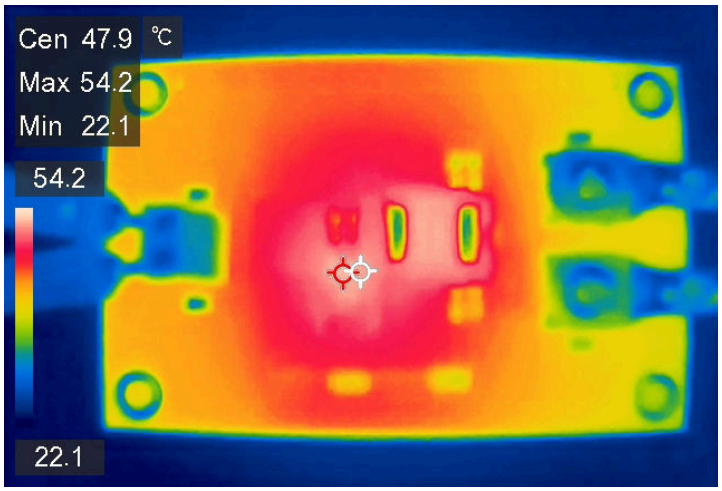


Figure 3-8. Thermal Performance, V_{IN} = 48V, I_{OUT} = 10A, Free Convection Airflow

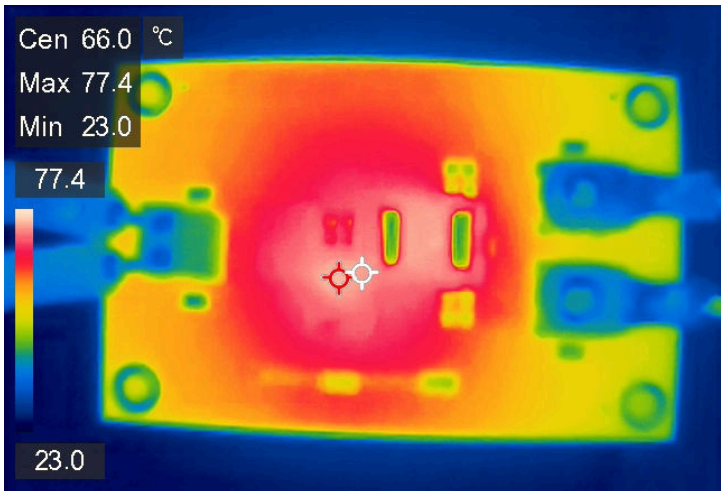


Figure 3-9. Thermal Performance, V_{IN} = 48V, I_{OUT} = 15A, Free Convection Airflow

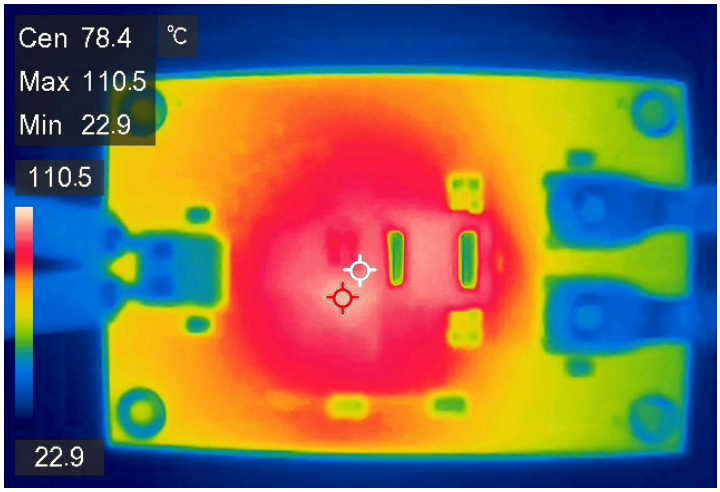


Figure 3-10. Thermal Performance, V_{IN} = 48V, I_{OUT} = 20A, Free Convection Airflow

4 Hardware Design Files

4.1 Schematic

Figure 4-1 provides the EVM schematic (with uninstalled components as indicated). If the ceramic output capacitance is deemed sufficient, remove electrolytic output capacitor C37 and adjust the COMP network to 1.5kΩ, 15nF, and 470pF.

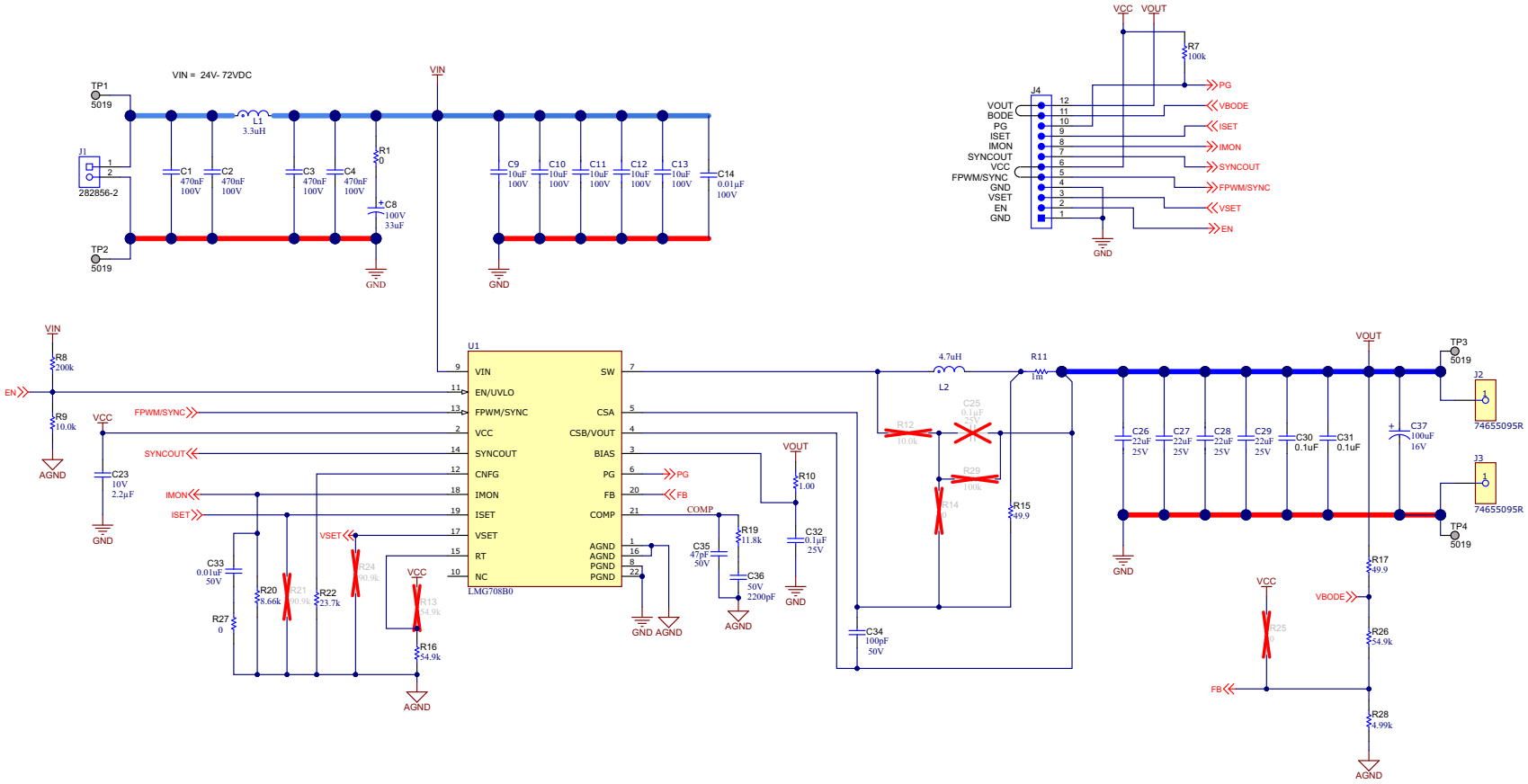


Figure 4-1. EVM Schematic

4.2 PCB Layout

Figure 4-2 through Figure 4-9 show the design of the EVM using a 6-layer PCB with 2oz copper weight (2.8mils or 70µm copper thickness). The EVM is essentially a single-sided design except for the EMI filter and some optional components located on the bottom side.

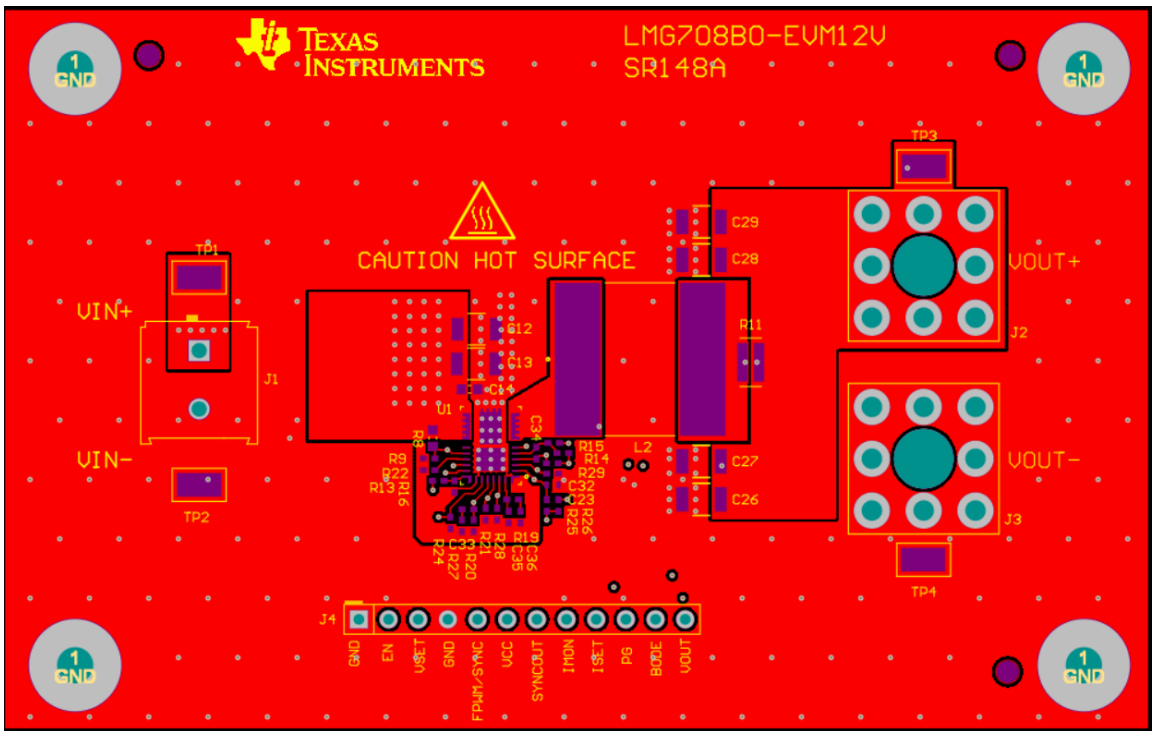


Figure 4-2. Top Copper (Top View)

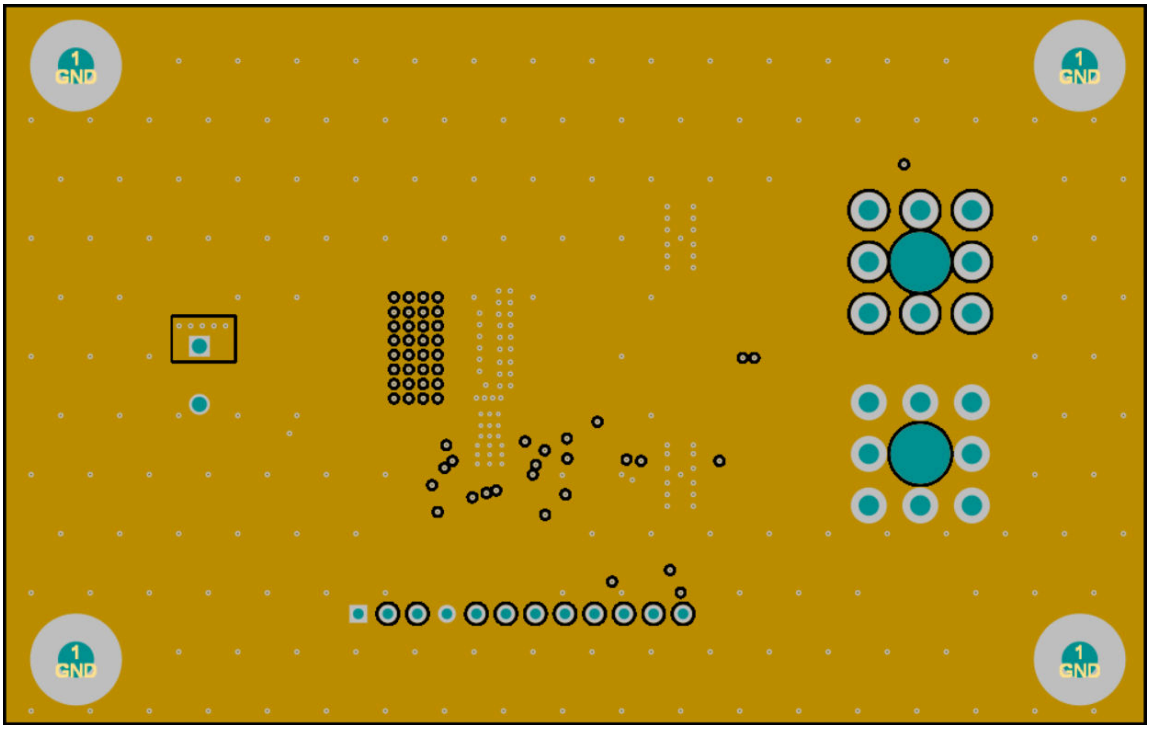


Figure 4-3. Layer 2 Copper (Top View)

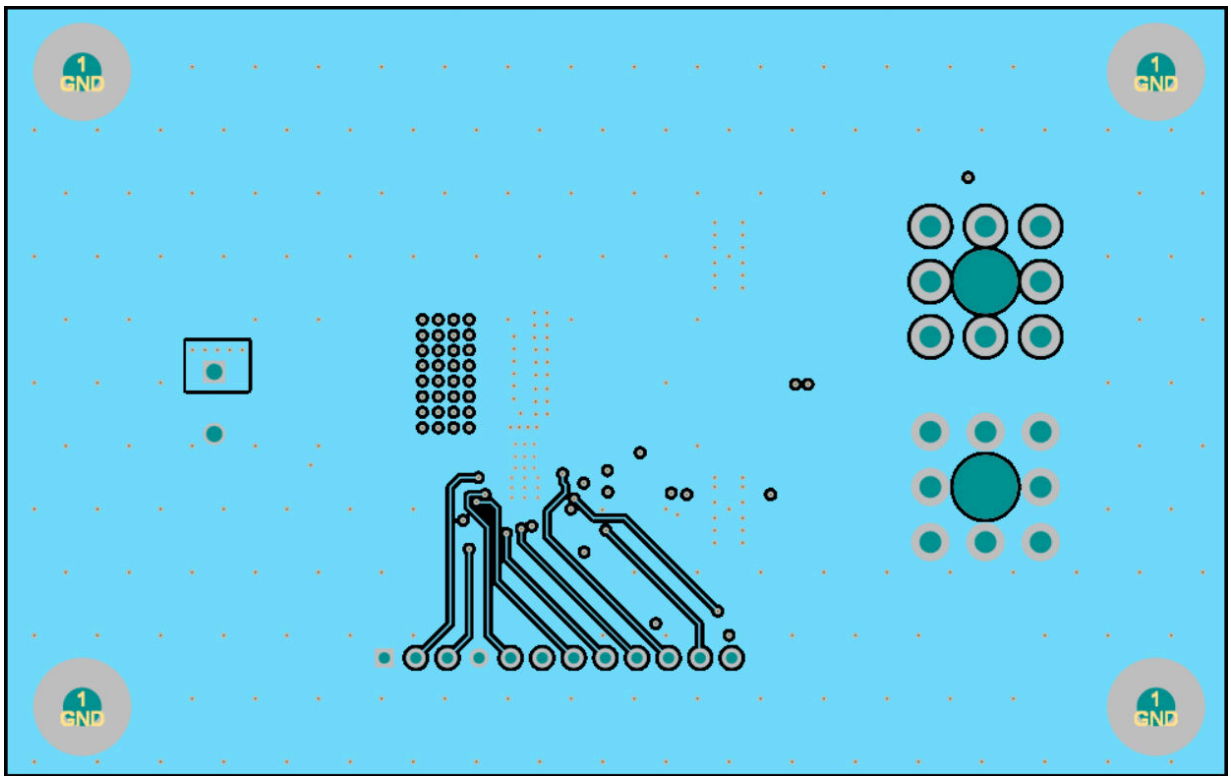


Figure 4-4. Layer 3 Copper (Top View)

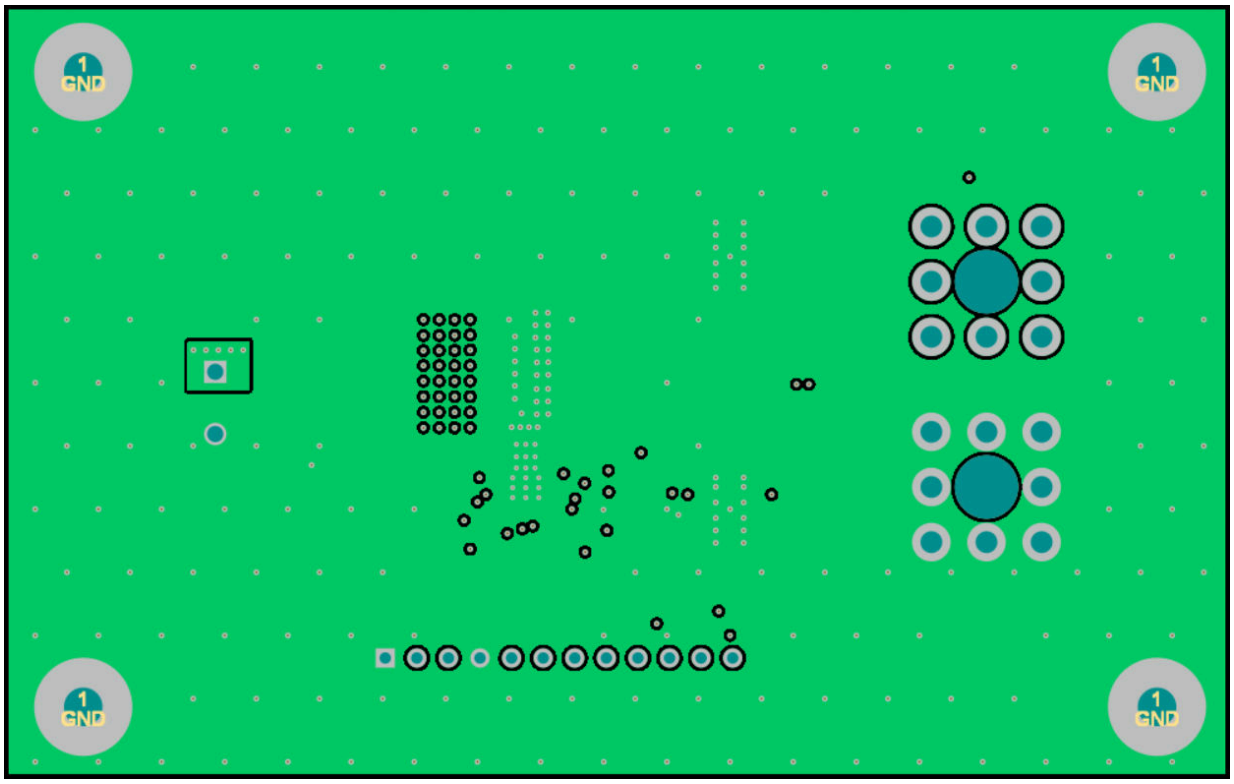


Figure 4-5. Layer 4 Copper (Top View)

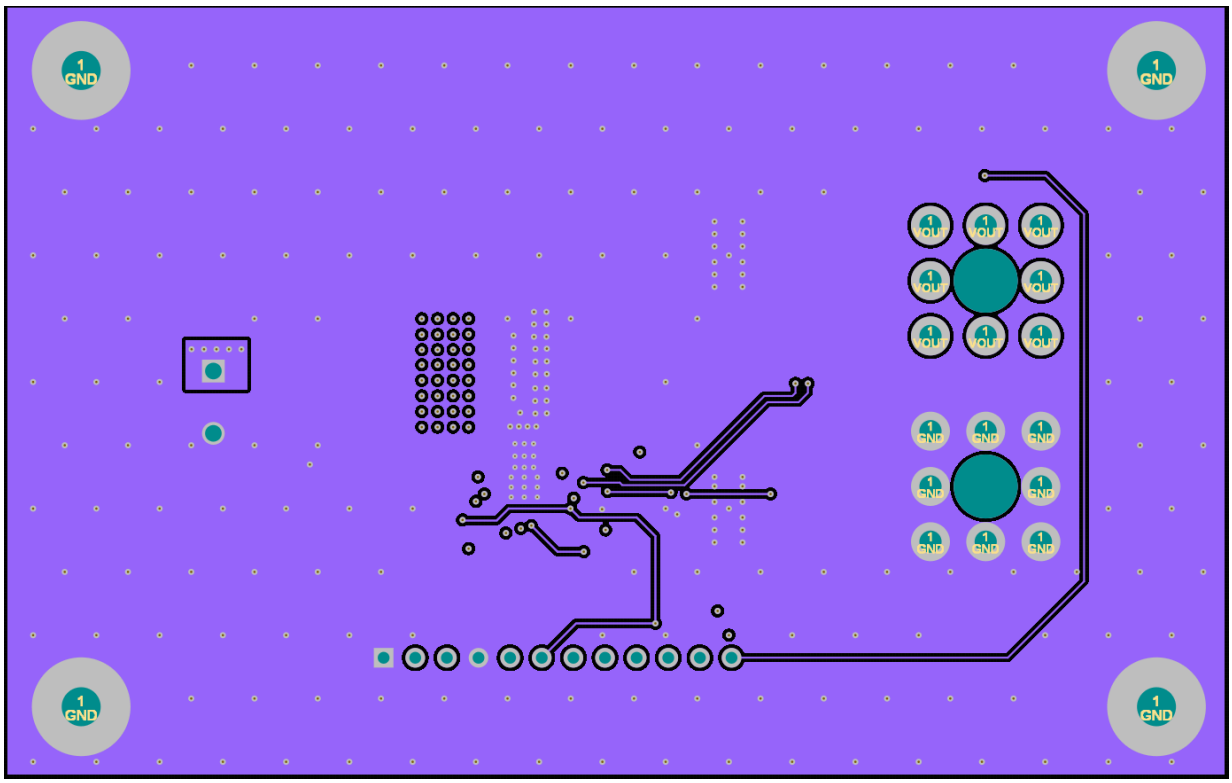


Figure 4-6. Layer 5 Copper (Top View)

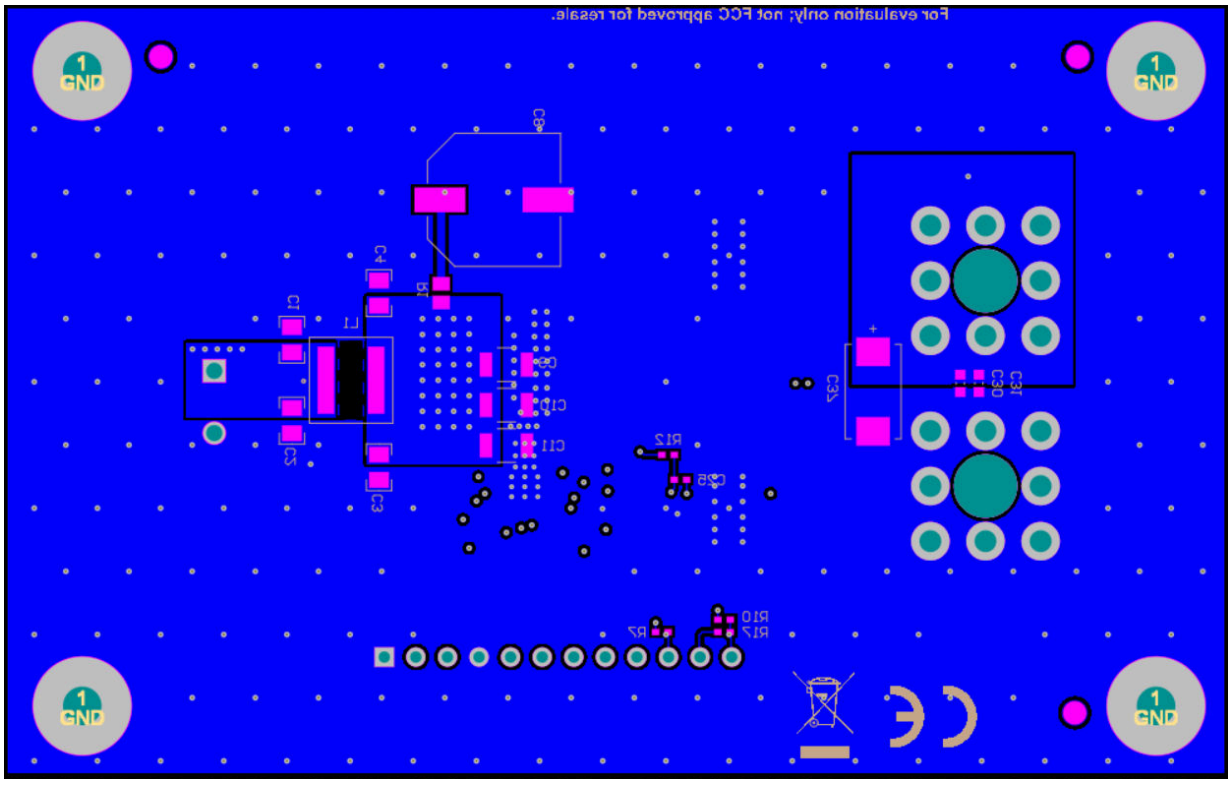


Figure 4-7. Bottom Copper (Top View)

4.2.1 Component Drawings

Figure 4-8. Top Component Drawing

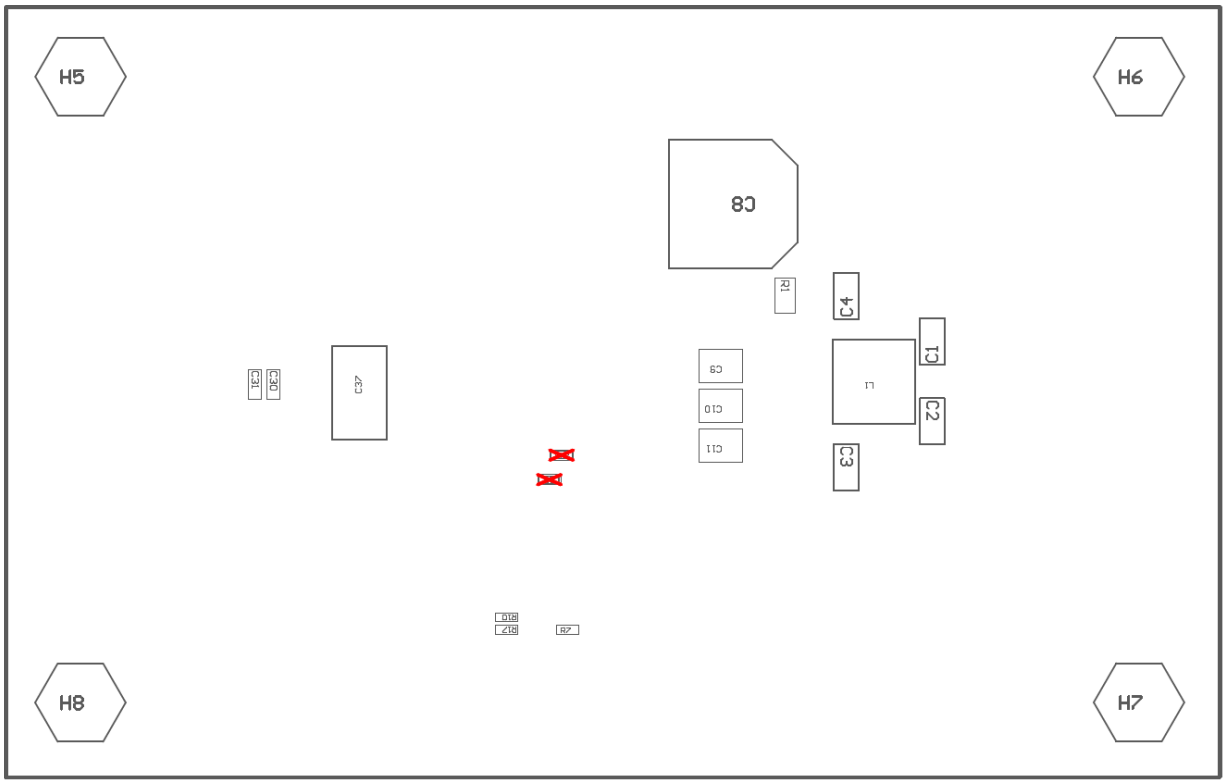


Figure 4-9. Bottom Component Drawing

4.2.2 Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuit (with high current and voltage slew rates) to achieve a robust and reliable design with low EMI signature. As expected, consider certain issues before designing a PCB layout. The high-frequency power loop of a buck regulator power stage is denoted by the shaded area in Figure 4-10. The topological architecture of a buck regulator means that particularly high di/dt current flows in this loop – and reducing the parasitic inductance of this loop by minimizing the effective loop area becomes mandatory.

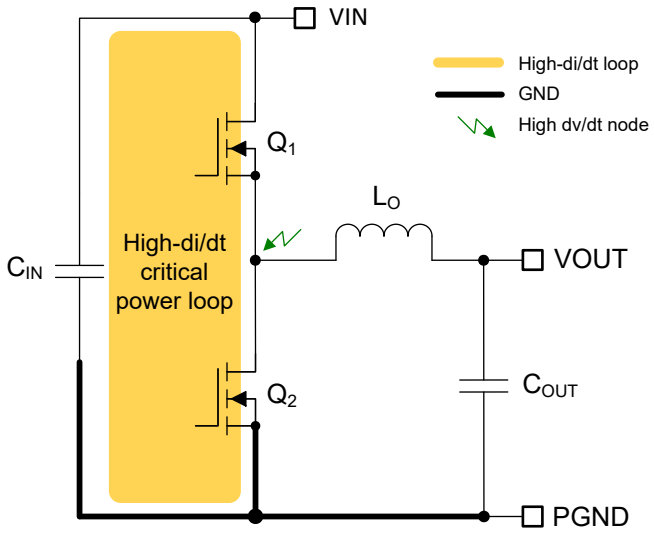


Figure 4-10. DC/DC Converter Ground System Illustrating the Power Stage Switching Loop

4.2.2.1 Power Stage Layout

- Place the components for the power stage of a buck regulator – input capacitors, output capacitors, buck inductor, shunt resistor, and the LMG708B0 power IC – on the top side of the PCB.
  - Locating the components on the top side maximizes the benefit of convective heat transfer by leveraging any system-level airflow. Use a full ground plane on layer 2 under the power stage components.
- The DC/DC regulator has one critical high-current loop: the switching power loop. Minimize the area of this loop to suppress generated switching noise, reduce parasitic inductance, and optimize switching performance.
  - **Switching power loop**: The most important loop area to minimize is the path from the input capacitors through the high- and low-side GaN FETs, and back to the capacitors through the ground (PGND) connection. Connect the negative terminals of the input capacitors close to the PGND pin, which connects to the source of the low-side GaN FET. Similarly, connect the positive terminals of the input capacitors close to the VIN pin, which connects to the drain of the high-side GaN FET.
- The PCB trace defined as switch node, which connects the SW pin of the IC to the inductor, must be short and wide. However, the SW node is a source of injected noise and thus must not be too large.
- Use a wide aspect ratio shunt that provides low ESL. See also Section 4.3 for components that are an excellent choice.
- The VCC capacitor supplies the high-di/dt current to (a) the gate driver for low-side GaN FET, and (b) to the integrated bootstrap circuit that supplies the gate driver for the high-side GaN FET. Locate the VCC capacitor as close as possible to the VCC pin of the LMG708B0 and use the GND plane on layer 2 as the return to the PGND pin.

4.2.2.2 Small-signal Component Layout

The following considers components related to the analog and feedback signals as well as current sensing:

- Place small-signal components close to the power IC. Insert at least one inner plane, connected to ground, for noise shielding. Isolate the small-signal traces from noisy power traces and polygons.
- Use a dedicated AGND island connected to the AGND pin of the IC. PGND and AGND connect internally in the IC, obviating the need for a connection on the PCB.

- Place all sensitive analog traces and components related to COMP, FB, CSA, CSB/VOUT, VSET, ISET, IMON, and RT away from the high-voltage switching node to avoid mutual coupling. Pay particular attention to shielding the feedback (FB) and current sense (CSA and CSB/VOUT) traces from power traces and components.
- Locate the upper and lower feedback resistors (if required) close to the FB pin, keeping the FB trace as short as possible. Route the trace from the upper feedback resistor to the required output voltage sense point at the load.
- Route the CSA and CSB/VOUT sense traces as a differential pair to minimize noise pickup and use Kelvin connections to the applicable shunt resistor.

4.2.2.3 Thermal Design and Layout

For a DC/DC converter to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LMG708B0 converter is available in a small 4.5mm × 6mm, 22-pin, thermally enhanced package (TEP) to cover a range of application requirements.

The useful operating temperature range of a buck converter with integrated GaN FETs, gate drivers and bias supply subregulator is greatly affected by the following:

- Thermal characteristics of the package and operating environment
- Factors affecting power FET dissipation
  - Input voltage
  - Output current
  - Switching frequency
- BIAS pin supply (from the output voltage or an available external supply)

The TEP offers a means of removing heat from the semiconductor die through the exposed thermal pads at the base and top of the package. This removal of heat allows a significant improvement in heatsinking, and the PCB designed with thermal lands, thermal vias, and one or more ground planes to complete the heat removal subsystem becomes imperative. The exposed pads at the base of the LMG708B0 are soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the IC thermal resistance to a very low value.

Preferably, use a six-layer board with 2oz copper thickness for all layers to provide low impedance, proper shielding and lower thermal resistance. Numerous vias with a 0.3mm diameter connected from the thermal lands (and from the area around the PGND pins) to the internal and solder-side ground planes are vital to facilitate heat transfer. In a multilayer PCB design, place a solid ground plane on the PCB layer below the power-stage components. This plane allows the power-stage currents to flow and also represents a thermally conductive path away from the heat-generating devices.

4.2.2.4 Ground Plane Design

TI recommends using one or more of the inner PCB layers as a solid ground plane. In particular, a full ground plane on the layer directly underneath the power-stage components is essential. Connect the exposed pads at the base of the LMG708B0 as well as the return terminals of the input and output capacitors to this ground plane. Keep PGND and AGND separate by using a dedicated island for AGND. The PGND nets contain high-frequency noise related to the high-di/dt switching currents. The power traces for VIN, PGND, and SW can be restricted to one side of the ground plane.

4.3 Bill of Materials

Table 4-1. Bill of Materials – 12V Output

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
4	C1, C2, C3, C4	Capacitor, ceramic, 470nF, 100V, X7R, 0805, AEC-Q200	GRM21BR72A474KA73L	Murata
1	C8	Capacitor, aluminum electrolytic, 33µF, 100V, AEC-Q200	EEE-FK2A330P	Panasonic
5	C9, C10, C11, C12, C13	Capacitor, ceramic, 4.7µF, 100V, X7R, 1210, AEC-Q200	CNA6P1X7R2A475K250	TDK
			C1210C475M1R2CT500	Kemet
		Capacitor, ceramic, 10µF, 100V, X7S, 1210	GRM32EC72A106KE05L	Murata
		Capacitor, ceramic, 10µF, 100V, X7R, 1210, AEC-Q200	CGA6P1X7R2A106K250	TDK
1	C14	Capacitor, ceramic, 10nF, 100V, X7R, 0603	GRM188R72A103KA01D	Murata
1	C23	Capacitor, ceramic, 2.2µF, 10V, X7S, 0402	Std	Std
4	C26, C27, C28, C29	Capacitor, ceramic, 22µF, 25V, X7S, 1210, AEC-Q200	GCM32EC71E226KE36	Murata
		Capacitor, ceramic, 22µF, 25V, X7R, 1210, AEC-Q200	CGA6P3X7R1E226M250	TDK
2	C30, C31	Capacitor, ceramic, 0.1µF, 50V, X7R, 0603	Std	Std
1	C32	Capacitor, ceramic, 0.1µF, 25V, X7R, 0402	Std	Std
1	C33	Capacitor, ceramic, 10nF, 50V, X7R, 0402	Std	Std
1	C34	Capacitor, ceramic, 100pF, 50V, X7R, 0402	Std	Std
1	C35	Capacitor, ceramic, 47pF, 50V, C0G, 5%, 0402	Std	Std
1	C36	Capacitor, ceramic, 2.2nF, 50V, X7R, 10%, 0402	Std	Std
1	C37	Capacitor, polymer electrolytic, 100µF, 16V, 12mΩ	ECASD61C107M012KA0	Murata
4	H1, H2, H3, H4	Hex standoff threaded #4-40 nylon, 1/2"	1902C	Keystone
4	H5, H6, H7, H8	#4-40 pan head machine screw Phillips drive nylon	NY PMS 440 0038 PH	Building Fasteners
2	H9, H10	WA-CLUG tubular cable lug	5580510	Würth Elektronik
2	H11, H12	M5 screw, 8mm long	MJ58MPP	Kanebridge
1	J1	Terminal block, 5mm, 2-pole, tin, TH	282856-2	TE Connectivity
2	J2, J3	8-pin PCB screw terminal connector, 85A, M5, TH	74655095	Würth Elektronik
1	J4	Header, 100mil, 12 × 1, Gold, TH	TSW-112-07-G-S	Samtec
1	L1	Inductor, 3.3µH, 13.4A, 5.9mΩ, AEC-Q200, 6.51 × 6.71 × 6.1mm	XGL6060-332MEC	Coilcraft
		Inductor, 3.3µH, 15.6A, 6mΩ, AEC-Q200, 6.4 × 6.6 × 6.1mm	744393465033	Würth Elektronik
		Inductor, 3.3µH, 22A, 6.3mΩ, 6.4 × 6.6 × 6mm	XFHCL6060HC-3R3M	XFRMS
1	L2	Inductor, 4.7µH, 27A, 3.76mΩ, AEC-Q200, 13.3 × 12.8 × 8mm	VCUD128T-4R7MS8	Cyntec
		Inductor, 4.7µH, 27.3A, 3.8mΩ, 13.3 × 12.8 × 8mm	CY1280LT150DS-4R7MC	Sumida
		Inductor, 4.7µH, 27A, 3mΩ, AEC-Q200, 13.4 × 15 × 8mm	ZG3396-AE	Coilcraft
		Inductor, 4.7µH, 28A, 3.8mΩ, AEC-Q200, 10 × 11.3 × 10mm	744393605047	Würth Elektronik
1	R1	Resistor, 0Ω, 0805	Std	Std
1	R7	Resistor, 100kΩ, 1/16W, 1%, 0402	Std	Std
1	R8	Resistor, 200kΩ, 1/10W, 1%, 0603	Std	Std
3	R9	Resistor, 10kΩ, 1/16W, 1%, 0402	Std	Std
2	R10, R27	Resistor, 0Ω, 1/16W, 1%, 0402	Std	Std
1	R11	Resistor, 1mΩ, 5%, 1.5W, 150ppm/°C, 0612, AEC-Q200	KRL3216E-C-R001-F-T5	Susumu
		Resistor, 1mΩ, 5%, 1W, 150ppm/°C, 0508, AEC-Q200	KRL2012E-C-R001-J-T5	Susumu
		Resistor, 1mΩ, 1%, 1W, 150ppm/°C, 0508, AEC-Q200	CSS0508FT1L00	Stackpole
2	R15, R17	Resistor, 49.9Ω, 1/16W, 1%, 0402	Std	Std
2	R16, R26	Resistor, 54.9kΩ, 1/16W, 1%, 0402	Std	Std
1	R19	Resistor, 11.8kΩ, 1/16W, 1%, 0402	Std	Std
1	R20	Resistor, 8.66kΩ, 1/16W, 1%, 0402	Std	Std
1	R22	Resistor, 23.7kΩ, 1/16W, 1%, 0402	Std	Std
1	R28	Resistor, 9.09kΩ, 1/16W, 1%, 0402	Std	Std
2	SH-J1, SH-J2	Open top jumper socket, 2.54mm pitch	M7582-05	Harwin
4	TP1, TP2, TP3, TP4	Test point, miniature, SMT	5019	Keystone
1	U1	LMG708B0 20A GaN buck converter, 4.5mm × 6mm	LMG708B0VBTR	TI
1	PCB1	PCB, FR4, 6 layer, 2oz, 99mm × 63mm	PCB	–

If 4 × 22µF, 25V, 1210 ceramic output capacitors are deemed sufficient, remove electrolytic output capacitor C37 and adjust the COMP network to 1.5kΩ, 15nF, and 470pF.

See Table 4-2 and Table 4-3 for recommended component changes to adjust from the default 12V output setting to 5V or 3.3V, respectively.

Table 4-2. Bill of Materials Changes – Fixed 5V Output, 300kHz

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
4	C26, C27, C28, C29	Capacitor, ceramic, 47µF, 10V, X7S, 1210, AEC-Q200	GCM32EC71A476KE02	Murata
1	C35	Capacitor, ceramic, 150pF, 50V, X7R, 10%, 0402	Std	Std
1	C36	Capacitor, ceramic, 3.3nF, 50V, X7R, 10%, 0402	Std	Std
1	C37	Capacitor, polymer electrolytic, 220µF, 6.3V, 10mΩ, AEC-Q200	ECASD40J227M010KB0	Murata
1	L2	Inductor, 2.5µH, 35A, 2.02mΩ, AEC-Q200, 13.3 × 12.8 × 8mm	VCUD128T-2R5MS8	Cyntec
		Inductor, 2.5µH, 36A, 1.9mΩ, 13.3 × 12.8 × 8mm	CY1280LT150DS-2R5MC	Sumida
		Inductor, 3.3µH, 41.5A, 2.7mΩ, AEC-Q200, 10 × 11.3 × 10mm	744393605033	Würth Elektronik
1	R16	Resistor, 73.2kΩ, 1/16W, 1%, 0402	Std	Std
1	R19	Resistor, 10kΩ, 1/16W, 1%, 0402	Std	Std
0	R26	Not assembled	–	–
1	R28	Resistor, 0Ω, 1/16W, 1%, 0402	Std	Std

Table 4-3. Bill of Materials Changes – 3.3V Output, 250kHz

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
4	C26, C27, C28, C29	Capacitor, ceramic, 47µF, 6.3V, X7R, 1210, AEC-Q200	GCM32ER70J476ME16	Murata
1	C35	Capacitor, ceramic, 270pF, 50V, X7R, 10%, 0402	Std	Std
1	C36	Capacitor, ceramic, 6.8nF, 50V, X7R, 10%, 0402	Std	Std
1	C37	Capacitor, polymer electrolytic, 220µF, 6.3V, 10mΩ, AEC-Q200	ECASD40J227M010KB0	Murata
1	L2	Inductor, 2.5µH, 35A, 2.02mΩ, AEC-Q200, 13.3 × 12.8 × 8mm	VCUD128T-2R5MS8	Cyntec
		Inductor, 2.5µH, 36A, 1.9mΩ, 13.3 × 12.8 × 8mm	CY1280LT150DS-2R5MC	Sumida
		Inductor, 2.2µH, 42.5A, 1.9mΩ, AEC-Q200, 10 × 11.3 × 10mm	744393605022	Würth Elektronik
1	R16	Resistor, 82.5kΩ, 1/16W, 1%, 0402	Std	Std
1	R19	Resistor, 5.49kΩ, 1/16W, 1%, 0402	Std	Std
1	R26	Resistor, 200kΩ, 1/16W, 1%, 0402	Std	Std
1	R28	Resistor, 86.6kΩ, 1/16W, 1%, 0402	Std	Std

5 Compliance Information

5.1 Compliance and Certifications

LMG708B0-EVM12V EU Declaration of Conformity (DoC) for Restricting the use of Hazardous Substances (RoHS) certificate

6 Additional Information

6.1 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

For development support, see the following:

- For TI's reference design library, visit TI Designs
- For TI's WEBENCH design environments, visit the WEBENCH® Design Center
- LMG708B0 GaN buck converter quickstart calculator
- LMG708B0 SIMPLIS and PSPICE simulation models
- LMG708B0-EVM12V Altium *layout* source files

7.2 Documentation Support

7.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMG708B0 5V to 80V, 20A, GaN Synchronous Buck Converter* datasheet
- Texas Instruments, *LMG5126 Wide-Input 2.5MHz Boost Converter* datasheet
- Texas Instruments, *LMG708B0 12V_{OUT}, 40A, 400kHz, Two-Phase GaN Buck Converter Evaluation Module* EVM user's guide
- Texas Instruments, GaN technologies landing page
- Texas Instruments, GaN power stages landing page
- Reference designs:
  - Texas Instruments, *48V_{IN}, 960W, four-phase buck converter with integrated GaN reference design*
  - Texas Instruments, *48V_{IN}, 5V_{OUT}, 400W, four-phase buck converter with integrated GaN reference design*
  - Texas Instruments, *48V to 24V GaN buck converter industrial power supply reference design*
- Technical articles:
  - Texas Instruments, *Four ways integrated GaN converters are redefining high-current power-supply design*
  - Texas Instruments, *Increasing power density with an integrated GaN solution*
- Application briefs:
  - Texas Instruments, *Key Parameters and Driving Requirements of GaN FETs*
  - Texas Instruments, *Nomenclature, Types, and Structure of GaN Transistors*
  - Texas Instruments, *GaN Applications*
  - Texas Instruments, *GaN Driver Schematic and Layout Recommendations*

7.2.1.1 Low-EMI Design Resources

- Texas Instruments, *Low EMI* landing page
- Texas Instruments, *Tackling the EMI challenge* company blog
- Texas Instruments, *An Engineer's Guide to Low EMI in DC/DC Regulators* e-book
- Texas Instruments, *Designing a low-EMI power supply* video series
- White papers:
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
  - Texas Instruments, *Time-Saving and Cost-Effective Innovations for EMI Reduction in Power Supplies*
  - Texas Instruments, *Valuing Wide V_{IN}, Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications*

- Texas Instruments, *Improve High-Current DC/DC Regulalor EMI for Free With Optimized Power Stage Layout* application brief
- Texas Instruments, *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* analog design journal

7.2.1.2 Thermal Design Resources

- Texas Instruments, *Improving Thermal Performance in High Ambient Temperature Environments With Thermally Enhanced Packaging* white paper
- Applications notes:
  - Texas Instruments, *Thermal Design by Insight, Not Hindsight*
  - Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
  - Texas Instruments, *Semiconductor and IC Package Thermal Metrics*
  - Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
  - Texas Instruments, *Using New Thermal Metrics*
- Texas Instruments, *PowerPAD™ Made Easy* application brief

7.2.1.3 PCB Layout Resources

- LMG708B0-EVM12V *Altium layout* source files
- LMG708B0-EVM2PH *Altium layout* source files
- Texas Instruments, *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout* application brief
- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application note
- Texas Instruments, *Constructing Your Power Supply – Layout Considerations* seminar

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (April 2026)	Page
• First public release of the EVM user's guide	1
• Updated the document title	1
• Updated the *Features*	1
• Updated the list of *Applications*	1
• Updated the hardware image	1
• Added the case temperature range, updated the input voltage, and revised the notes in *Specifications*	3
• Updated the two-phase schematic of Figure 1-2 with the FPWM/SYNC and FB inputs for mode selection	4
• Added efficiency plots for 5V and 3.3V outputs in *Efficiency*	8
• Added Figure 3-7 output voltage ripple waveform	9
• Added *Layout Guidelines*	17
• Added alternative part numbers for the input capacitor, buck inductor, and shunt in the *Bill of Materials*	19
• Added list of reference designs and tech articles to *Related Documentation*	21

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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