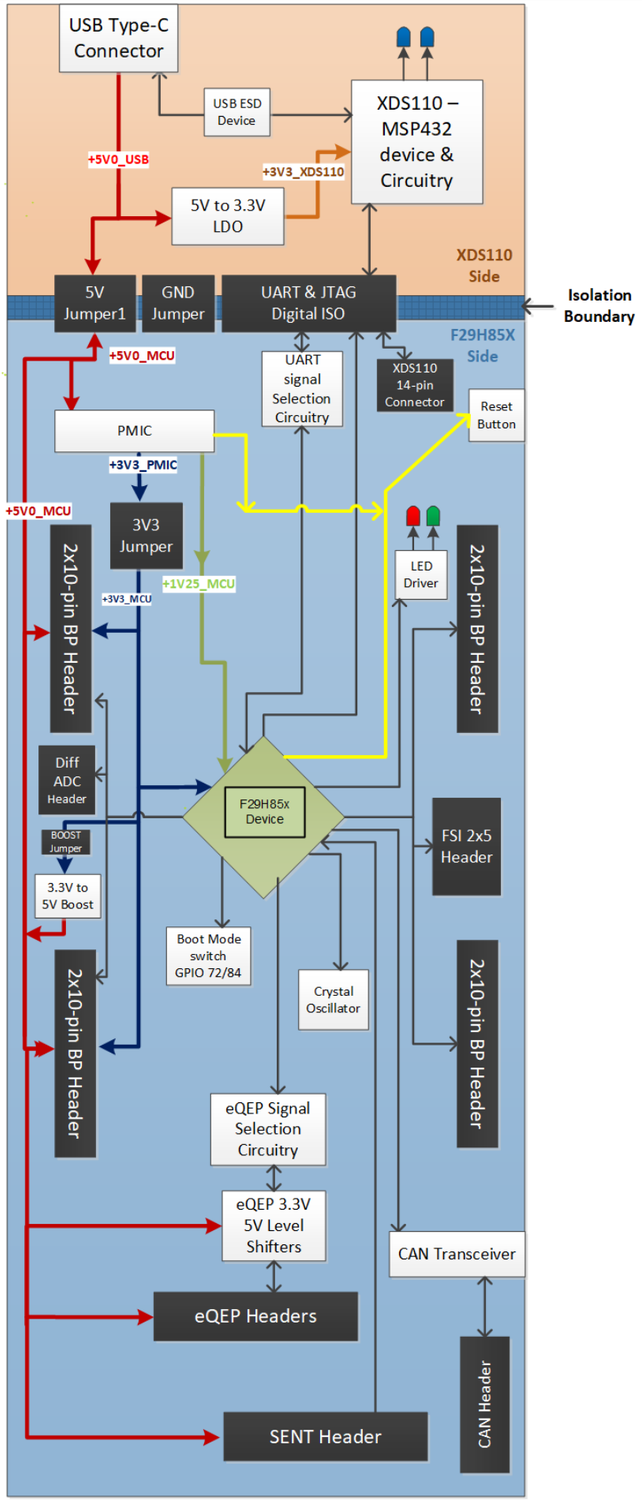
1) USB Differential Pairs - 90 Ohm
(A) USB_D_P and USB_D_N
2) ADC Differential pair Impedance Matching - 50 Ohm
(A) ADCINA4A5_P and ADCINA4A5_N
(B) ADCINB3B4_P and ADCINB3B4_N
(C) MCU_A4A5_P and MCU_A4A5_N
(D) MCU_B3B4_P and MCU_B3B4_N
3) CLK Paths - 50 Ohm
(A) X1
(B) X2



Revision History

Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	N/A	SB	Original engineering release.
A	N/A	June 20, 2025	SB	- Added C15 to U3A VOUT - Changed C28 from 0.1uF to 200pF - Changed GPIO30 connection on U10 - Changed ERRORSTS connection on U10 - Added OPN on U10 - Added R18, R26, and R27 - Added R25 and R28 - Corrected S5 and S6 silkscreen labels in PCB
A	N/A	Oct. 20, 2025	GM	Updated notes in SOM power schematic; no functional change to EVM design.
B	N/A	May 4, 2026	GM	Moved XTAL dampening resistor to X2. Updated PCB silkscreen to mention P58x and P32x support. Updated L1 part number.

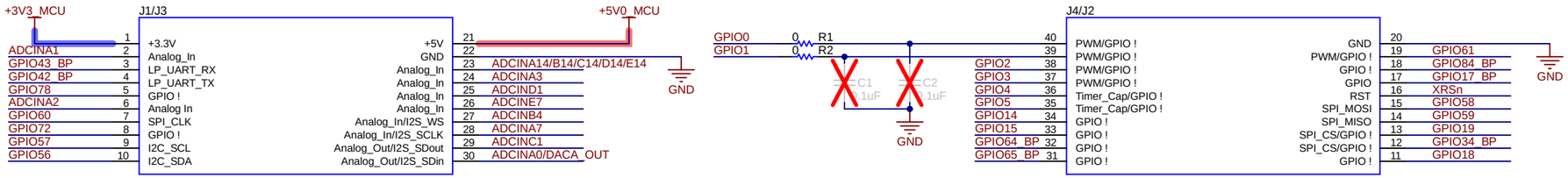
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Orderable: LAUNCHXL-F29H85X		Designed for: Public Release	Mod. Date: 11/9/2026
TID #: N/A		Project Title: LAUNCHXL-F29H85X	
Number: MCU119	Rev: B	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 002	Sheet: 1 of 8
Drawn By: Susmitha Bumadi		File: MCU119B_Block_Diagram.SchDoc	Size: B
Engineer: Susmitha Bumadi		Contact: http://www.ti.com/support	

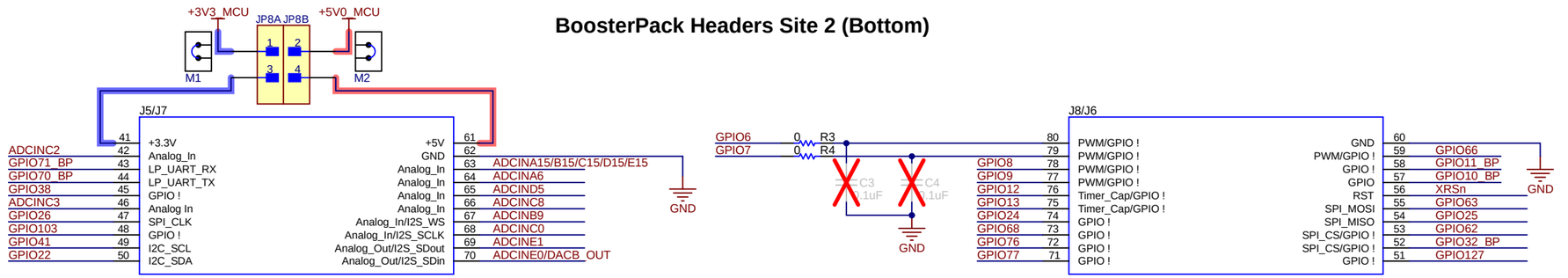
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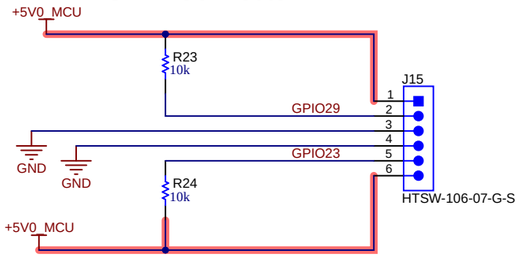
BoosterPack Headers Site 1 (Top)



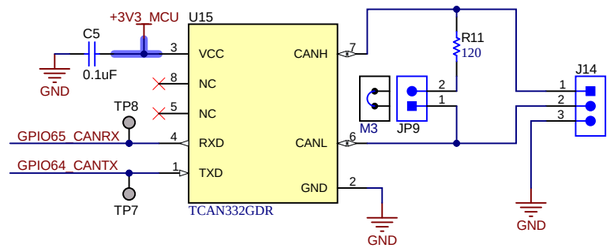
BoosterPack Headers Site 2 (Bottom)



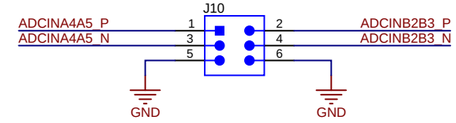
SENT Connector



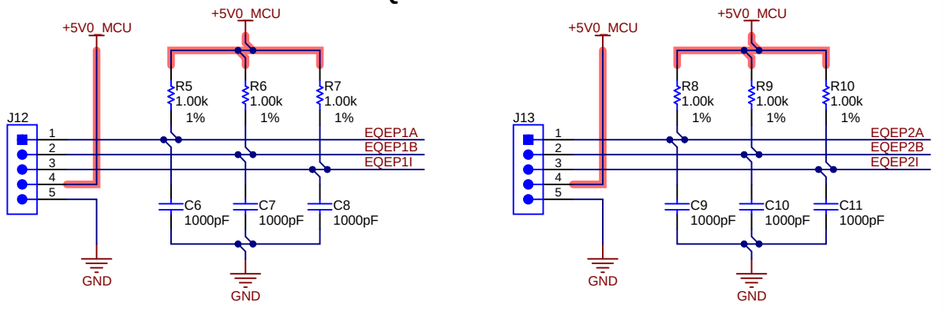
CAN Transceiver & Connector



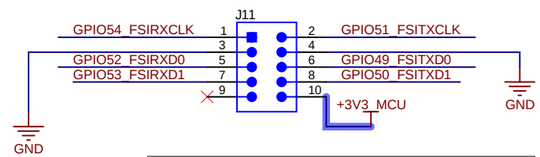
Differential ADC Connector



EQEP Connectors



FSI Connector



FSIRXCLK, FSIRXD0, and FSIRXD1 length matched to each other with 25mil tolerance.
FSITXCLK, FSITXD0, and FSITXD1 length matched to each other with 25mil tolerance.

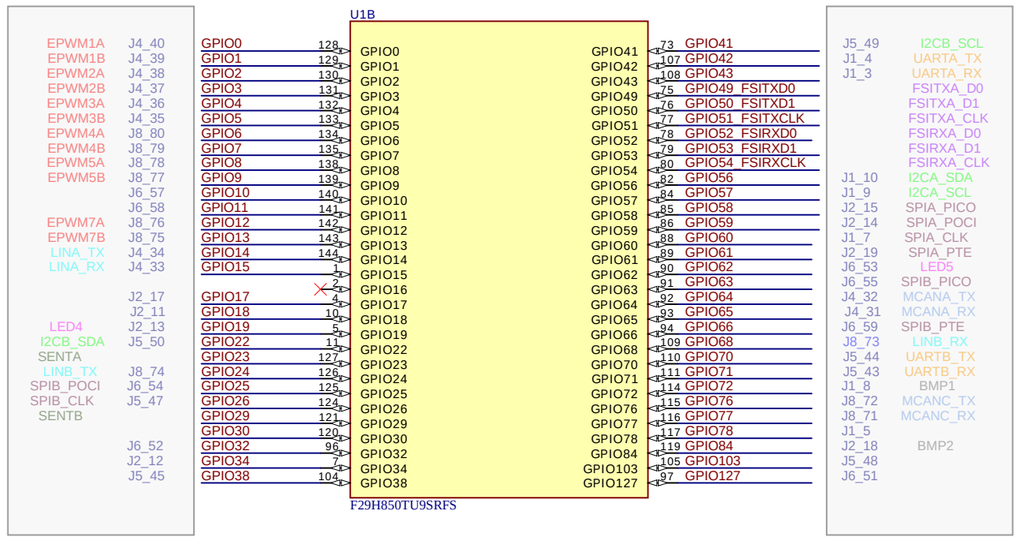
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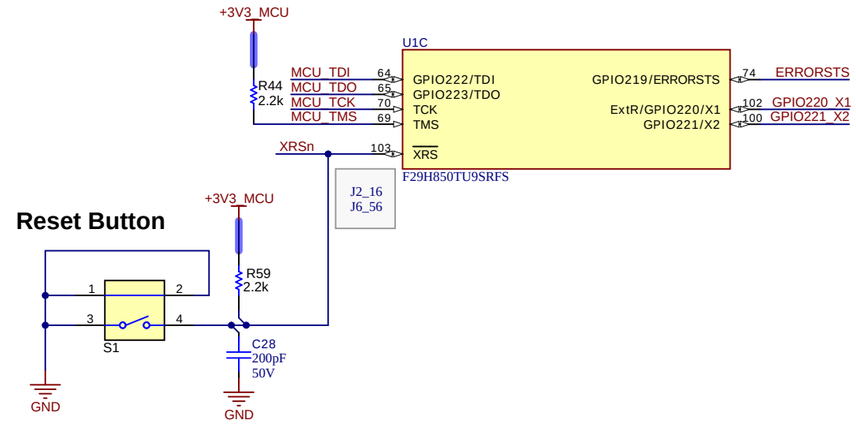
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TID #: N/A		Project Title: LAUNCHXL-F29H85X	
Number: MCU119	Rev: B	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 002	Sheet: 2 of 8
Drawn By: Susmitha Bumadi		File: MCU119B_Connectors.SchDoc	Size: B
Engineer: Susmitha Bumadi		Contact: http://www.ti.com/support	

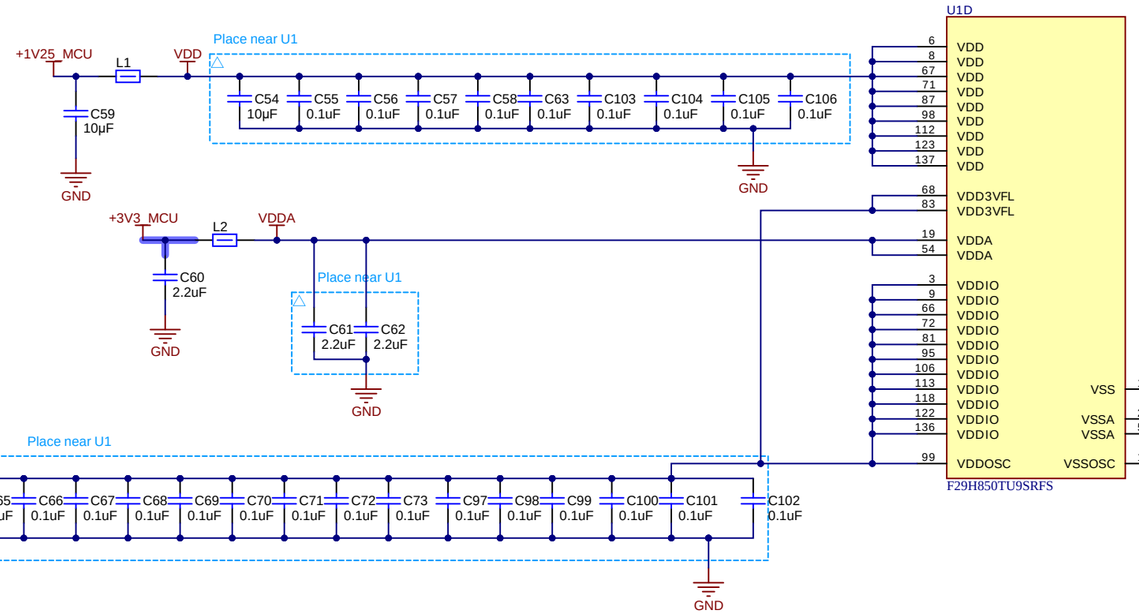
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F29H85x Device





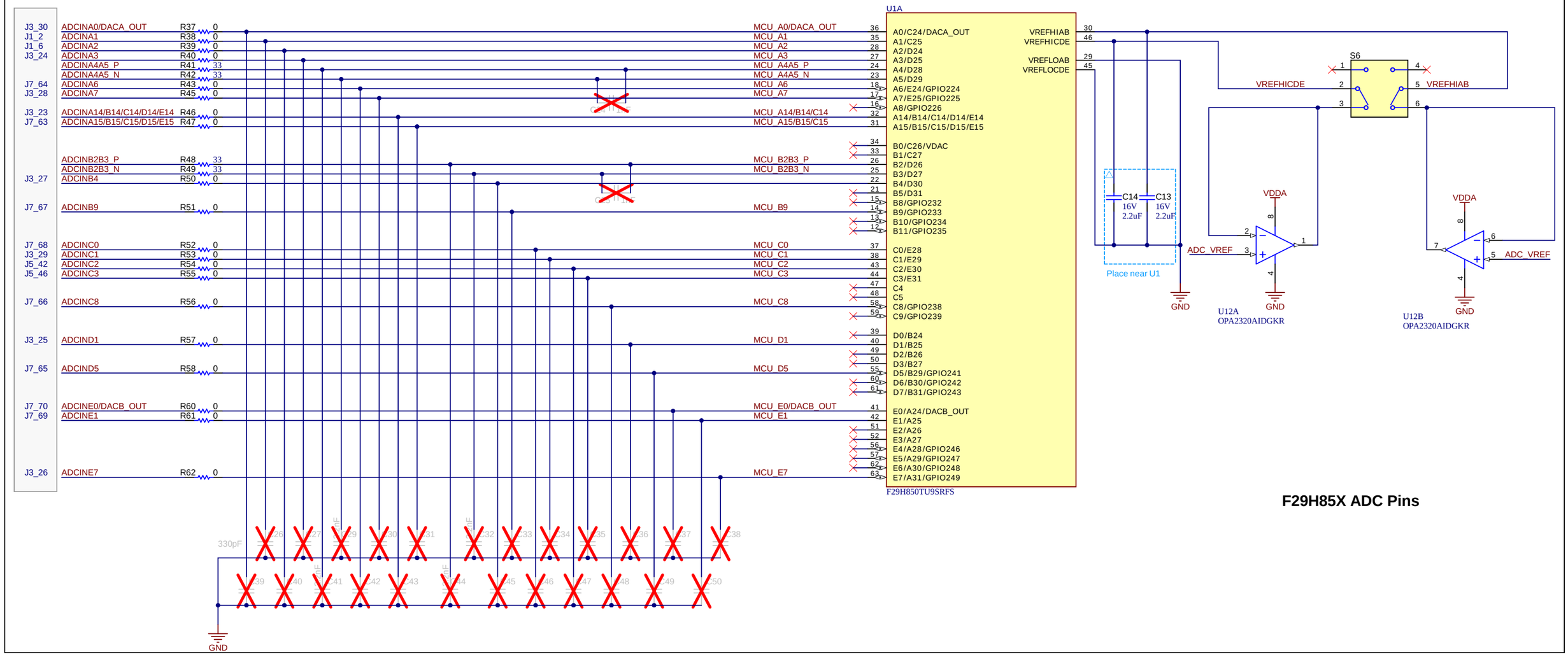


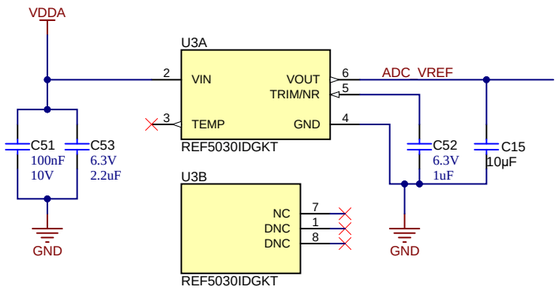
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Number: MCU119	Rev: B	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 002	Sheet: 3 of 8
Drawn By: Susmitha Bumadi		File: MCU119B_F29H85X_Device.SchDoc	Size: B
Engineer: Susmitha Bumadi		Contact: http://www.ti.com/support	

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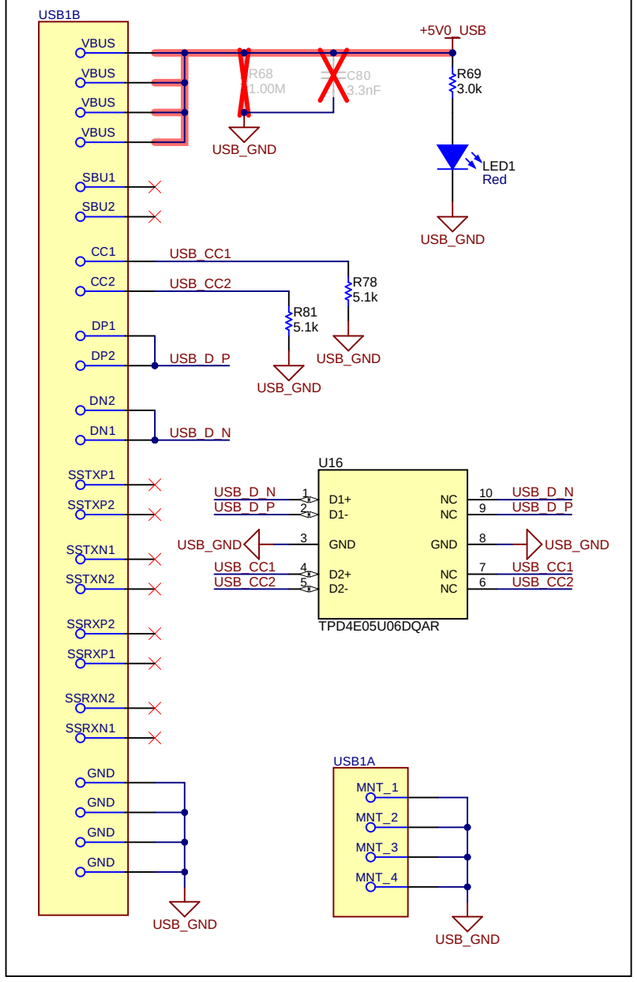
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Number: MCU119 Rev: B	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 002	Sheet: 4 of 8
Drawn By: Susmitha Bumadi	File: MCU119B_ADC.SchDoc	Size: B
Engineer: Susmitha Bumadi	Contact: http://www.ti.com/support	

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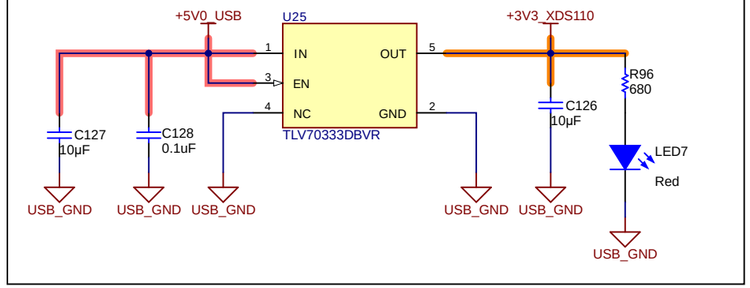
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Emulation Side

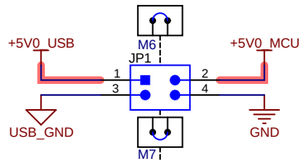
USB-C Connector



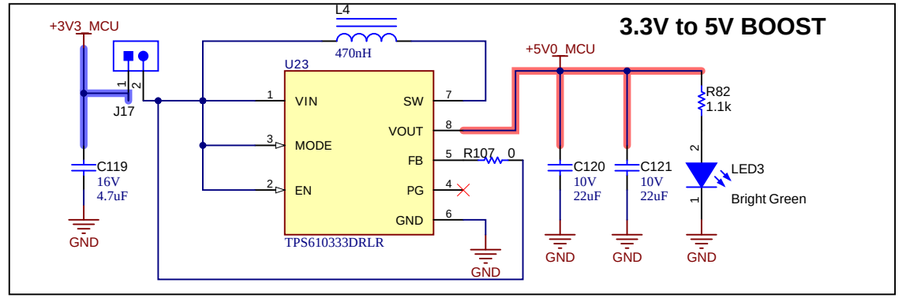
5V to 3.3V (XDS)



PWR & GND Isolation Boundary

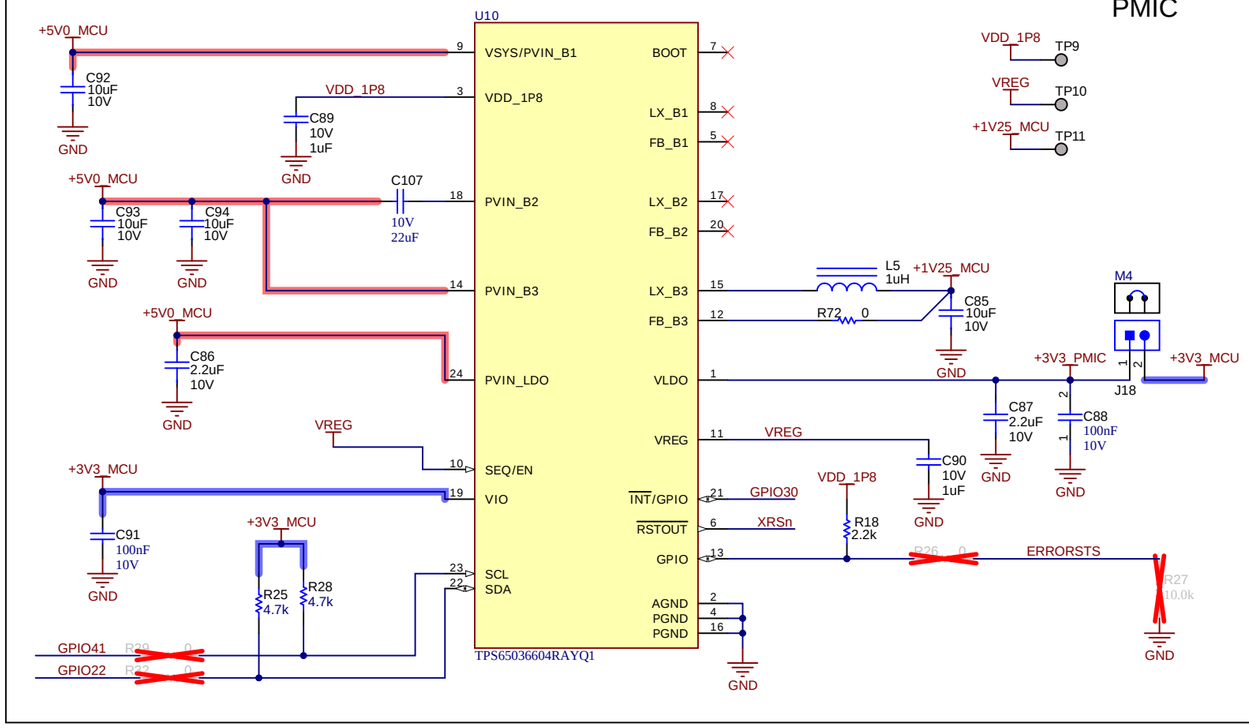


3.3V to 5V BOOST

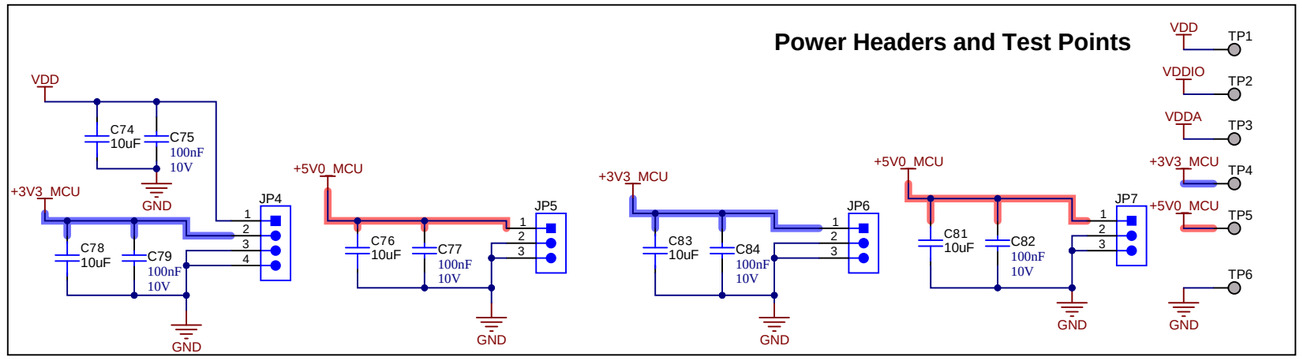


C2000 Side

PMIC



Power Headers and Test Points



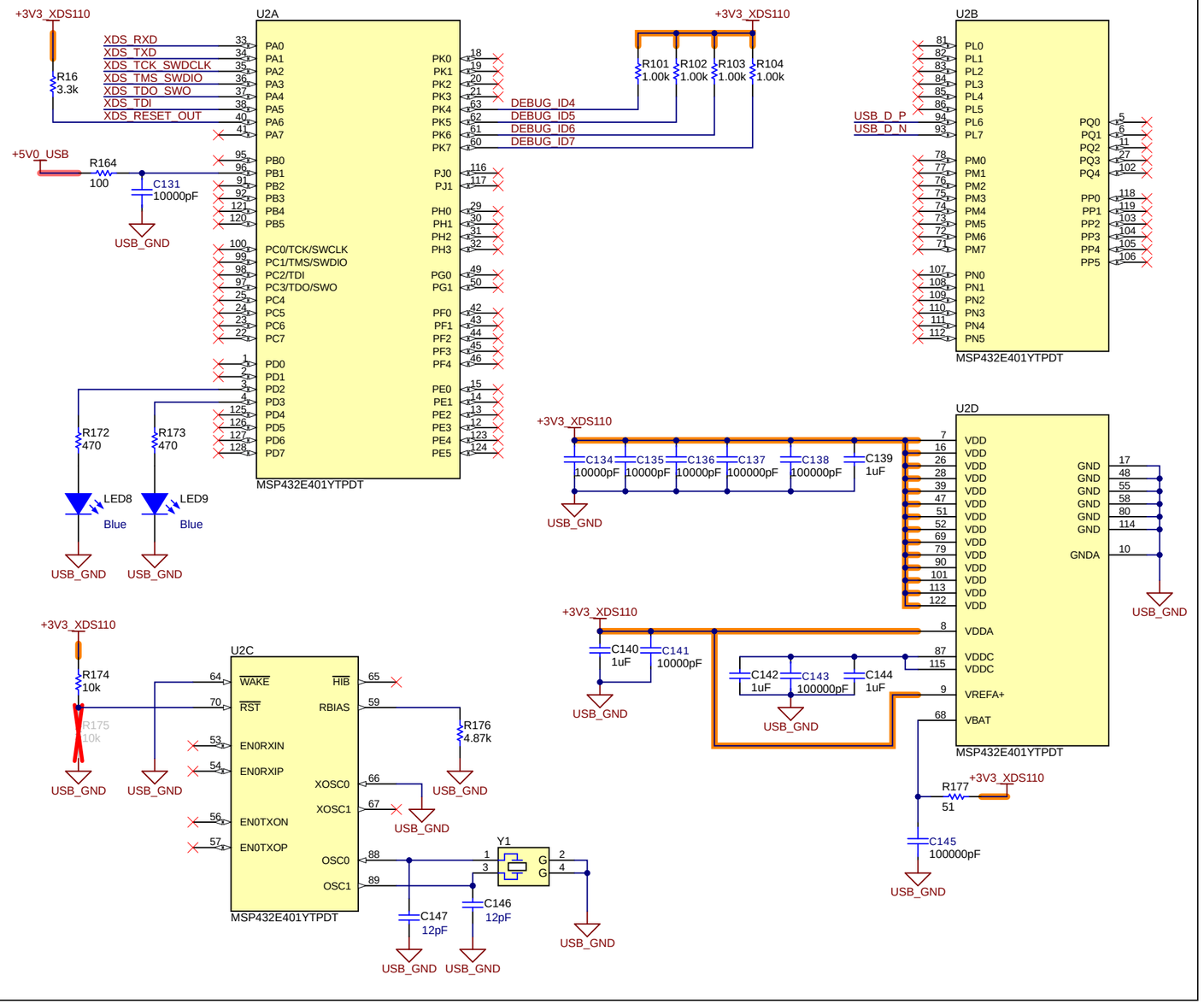
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TID #: N/A		Project Title: LAUNCHXL-F29H85X	
Number: MCU119	Rev: B	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 002	Sheet: 5 of 8
Drawn By: Susmitha Bumadi		File: MCU119B_USB_and_Power.SchDoc	Size: B
Engineer: Susmitha Bumadi		Contact: http://www.ti.com/support	

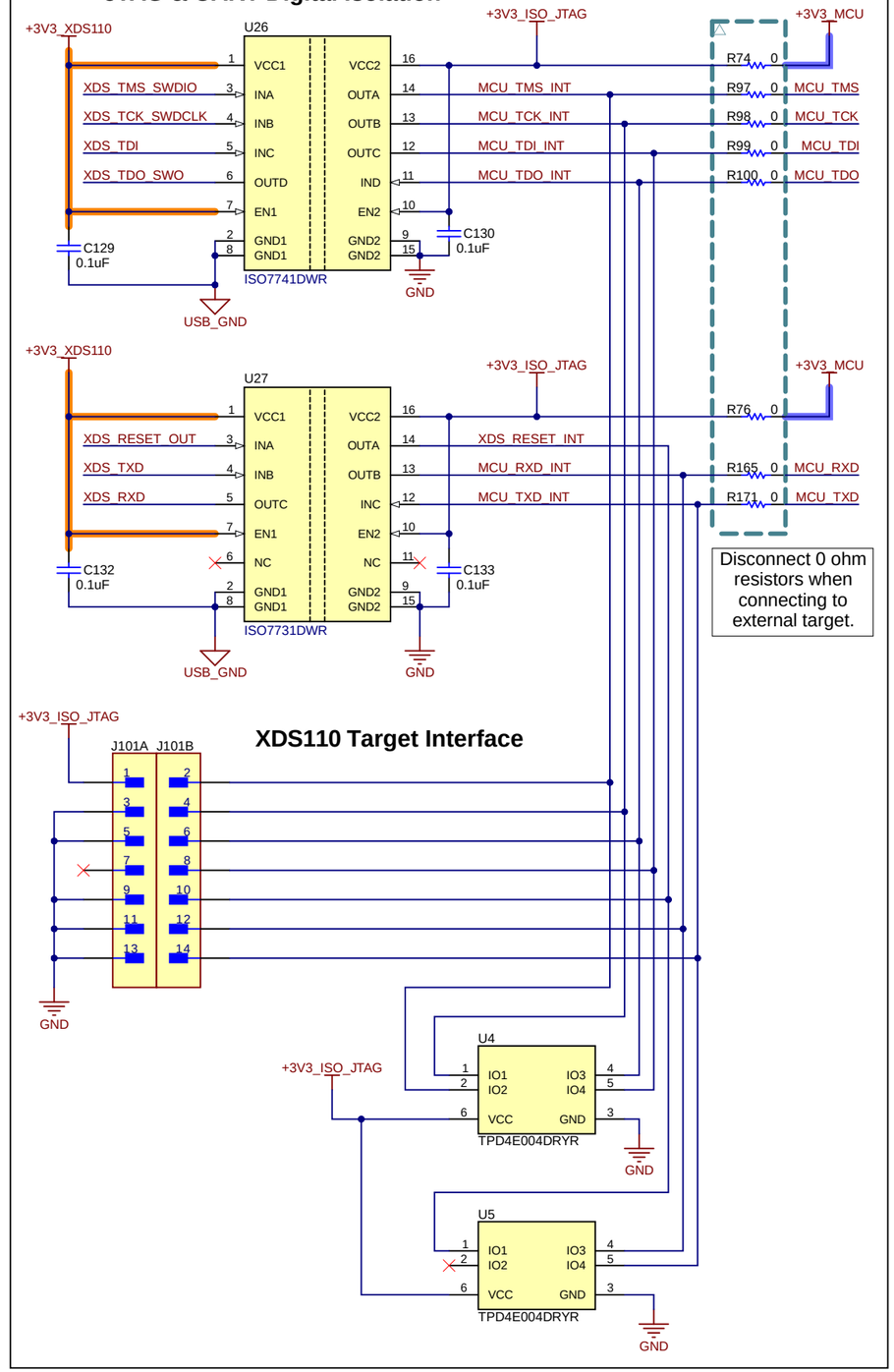
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XDS110 Device



JTAG & UART Digital Isolation



XDS110 Target Interface

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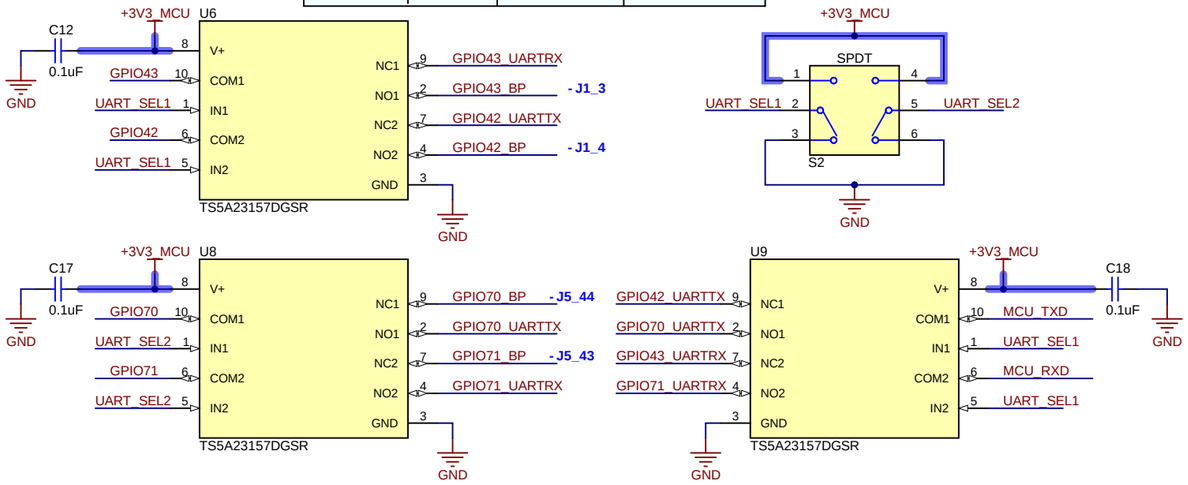
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Number: MCU119	Rev: B	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 002	Sheet: 6 of 8
Drawn By: Susmitha Bumadi		File: MCU119B_XDS110_MCU.SchDoc	Size: B
Engineer: Susmitha Bumadi		Contact: http://www.ti.com/support	

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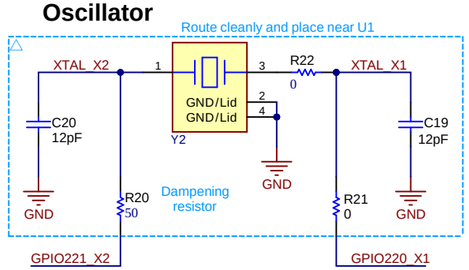
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UART Routing

UART_SEL1	UART_SEL2	GPIO42/43 Route	GPIO70/71 Route	
0	0	XDS110 COM Port	BP	- DEFAULT
0	1	XDS110 COM Port	NC	
1	0	BP	BP	
1	1	BP	XDS110 COM Port	

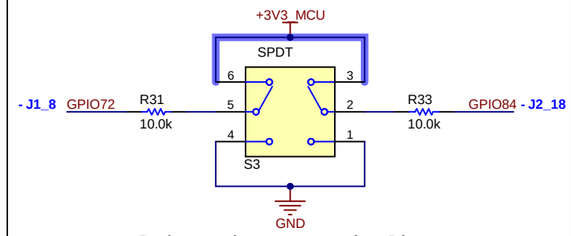


Oscillator



By default:
- Crystal Y2 is connected between GPIO221_X2 and GPIO220_X1.

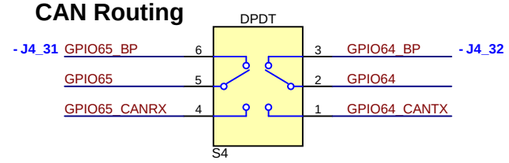
Boot Mode Select



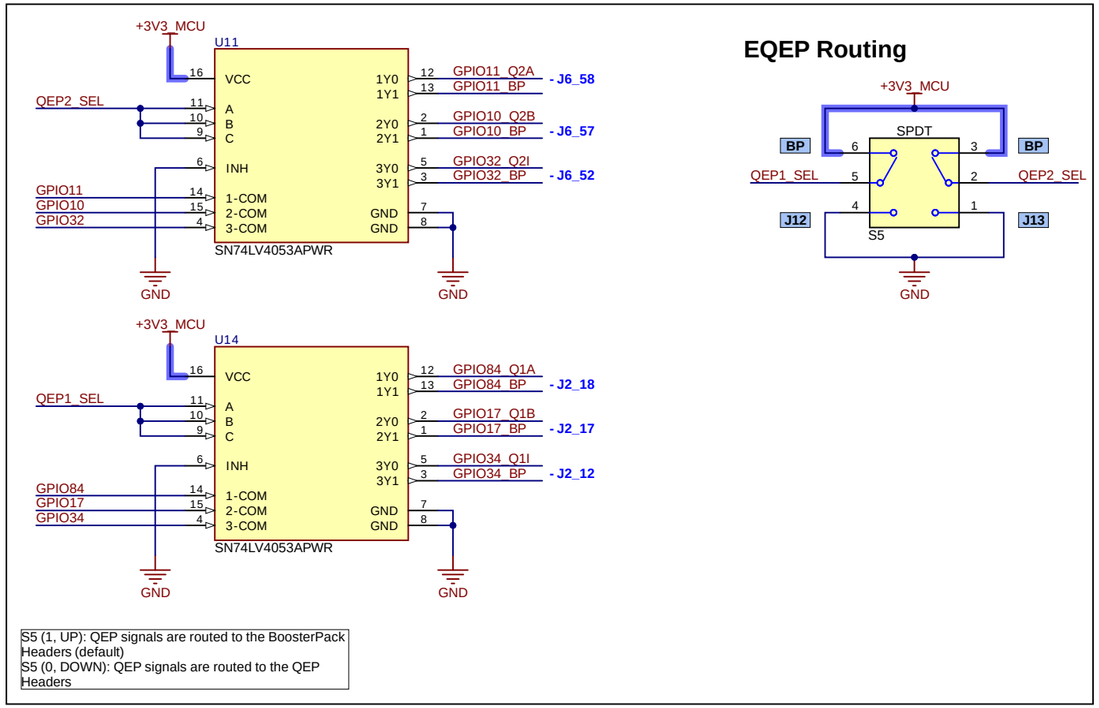
Selected Boot Mode Chart

Mode #	GPIO72	GPIO84	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

CAN Routing

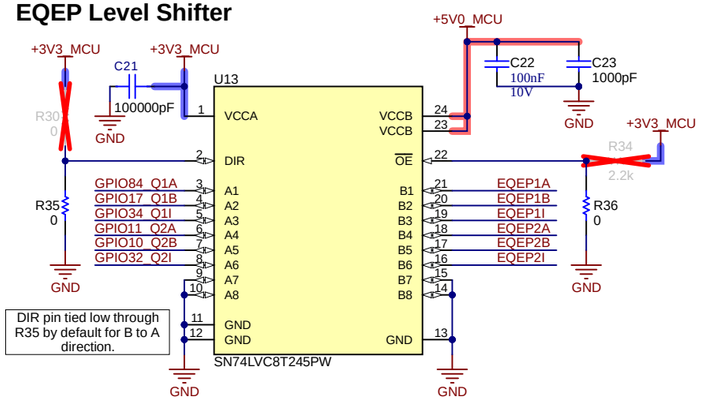


EQEP Routing



S5 (1, UP): QEP signals are routed to the BoosterPack Headers (default)
S5 (0, DOWN): QEP signals are routed to the QEP Headers

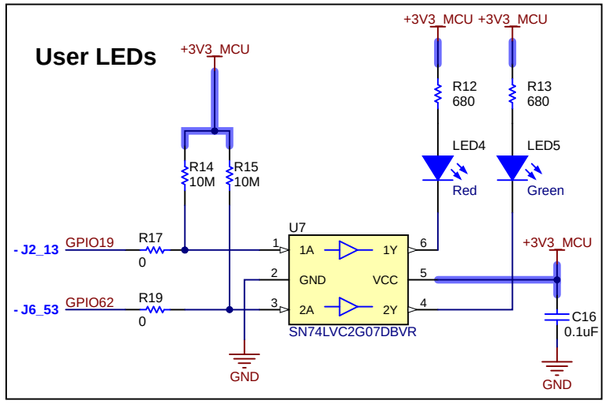
EQEP Level Shifter



DIR pin tied low through R35 by default for B to A direction.

To disable the Level Shifter:
1. De-populate R36
2. Place a 2.2k ohm resistor on R34 to pull-up OE

User LEDs



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TID #: N/A		Project Title: LAUNCHXL-F29H85X	
Number: MCU119	Rev: B	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 002	Sheet: 7 of 8
Drawn By: Susmitha Bumadi		File: MCU119B_AltRouting_Misc.SchDoc	Size: B
Engineer: Susmitha Bumadi		Contact: http://www.ti.com/support	

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FID1 FID2 FID3

FID4 FID5 FID6

MH1 MH2

MH3 MH4

PCB Number: MCU119
PCB Rev: B

Logo1
PCB
LOGO
Texas Instruments

CE Logo1

Logo3
PCB
LOGO
FCC disclaimer

Logo4
PCB
LOGO
WEEE logo

Logo5
PCB
LOGO
Texas Instruments

Logo6
PCB
LOGO
ETHERCAT LABEL

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Orderable: LAUNCHXL-F29H85X		Designed for: Public Release	Mod. Date: 11/9/2026
TID #: N/A		Project Title: LAUNCHXL-F29H85X	
Number: MCU119	Rev: B	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 002	Sheet: 8 of 8
Drawn By: Susmitha Bumadi		File: MCU119B_Hardware.SchDoc	Size: B
Engineer: Susmitha Bumadi		Contact: http://www.ti.com/support	

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