Texas Instruments

Application Report
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C2000™ Dual Sync Buck/Boost Converters

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1 Basics

Buck/Boost is a very normal topology in current power supply equipment.

Buck and Boost are very similar topologies. They have two MOSFETs and diodes and one power inductor. But the I/O ports are symmetrical.

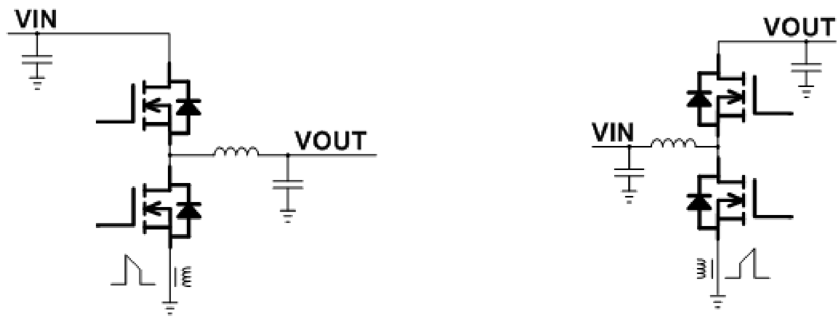


Figure 1. Buck and Boost Converter

Usually, we used a special analog controller to control the power stage before. Unfortunately, this analog controller can do very limited tasks. When this power supply is placed in a large system, it might be required to report some running information, or it might be controlled by the upper machine. A digital controller can fulfill all complex tasks and satisfy all kinds of requirements.

Table 1. Comparison of Some Methods

		Advantages	Disadvantages
Analog versus Digital	Analog Control	Widely used before	Special part for application Difficult to optimize
	Digital Control	Good platform for all kinds of topologies Less external components SCI/PMBUS interface	Need software engineer Need 3.3-V auxiliary power
Nonsync versus Sync	Nonsync Rect.	Less expensive	Lower efficiency under heavy load
	Sync Rect.	Higher efficiency and lower temperature rise, higher output ability	Expensive
Current Sensing	Current transformer	Higher efficiency	Cannot sample dc signal
	Shunt Resistor	Can sample ac or dc signal	Lower efficiency Need an expensive amplifier.

2 MCU Solution for Multiconverters

In this application note, we will show how to control a synchronous buck/boost converter and how one C2000 microcontroller unit (MCU) can handle multichannel buck/boost converters.

2.1 C2000 Piccolo A MCU Overview

The features of the C2000 Piccolo A MCU are:

- High-efficiency 32-bit CPU of 60 MIPS
- Low cost of device and system
- Enhanced pulse width modulator (ePWM) module
- High-resolution PWM (HRPWM) module
- Enhanced capture (eCAP) module
- Analog-to-digital converter (ADC); up to 13 channels and 4.6 MSPS
- On-chip temperature sensor
- Comparator supports all peripheral interrupts
- Independent 16-bit timer in each ePWM module

2.2 C2000 MCU Solution

Figure 2 shows the block diagram of the dual sync buck/boost converters.

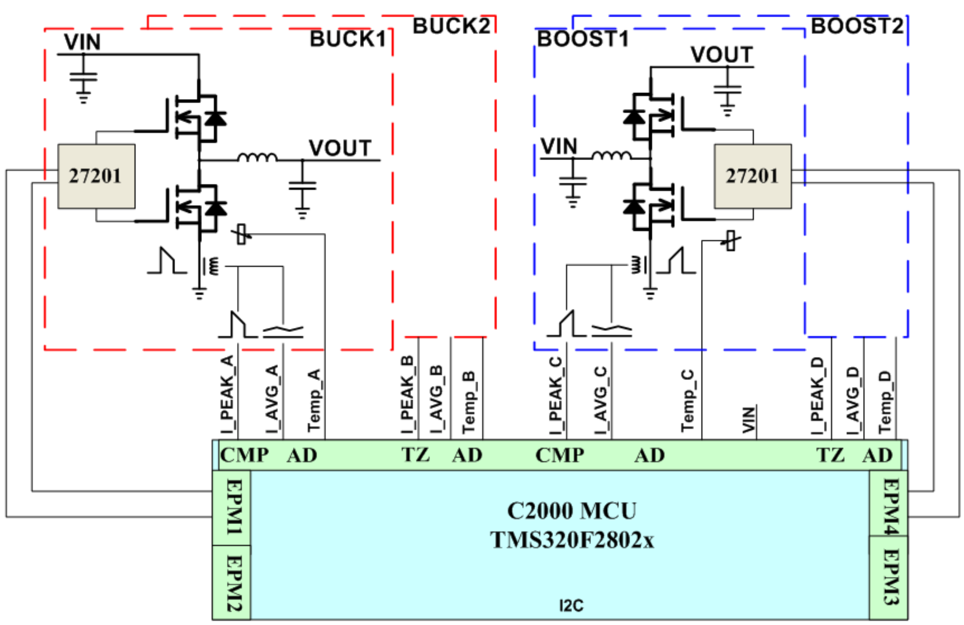


Figure 2. Block Diagram of Dual Sync Buck/Boost Converters

In our solution, we use the powerful ADC/comparator/calculation functions of C2000 Piccolo A MCU to control dual sync buck/boost converters.

3 Hardware Design

3.1 Power Stage

The power stage is standard buck/boost circuit, which would be compatible between a synchronous rectifier and a nonsynchronous rectifier.

3.2 Auxiliary Power Supply

The auxiliary power supply is connected to an input port and supplies +12 V or +3.3 V power for MOSFET drivers and MCU and other ICs.

3.3 Detection Circuits

The most important feedback is the current signal which sends the MCU an image of the current flowing through the upper and lower MOSFET. This signal is used to monitor the current amplitude and the average value, and to protect the converter from OCP damage.

Table 2. Some Pinouts of This Solution

PORT	ADC/CMP	PORT NAME	Function
A0	ADC	VAO	Buck1 output voltage sampling
A1	ADC	IAAD	Buck1 output current sampling
A2	CMP	IACMP	Buck1 peak current protection
A3	ADC	TEMPA	Buck1 and 2 temperature sampling
A4	CMP	ICCMP	Boost1 peak current protection
A6	ADC	ICAD	Boost1 output current sampling
A7	ADC	VCO	Boost1 output voltage sampling
B1	ADC	IBAD	Buck2 output current sampling
B2	ADC	VBO	Buck2 output voltage sampling
B3	ADC	IDAD	Boost2 output current sampling
B4	ADC	VDO	Boost2 output voltage sampling
B6	ADC	TEMPD	Boost1 and 2 temperature sampling
B7	ADC	VIN_R	Input voltage sampling
TZ1	Trip zone	TZB	Buck2 peak current protection
TZ2	Trip zone	TZD	Boost2 peak current protection

3.4 MCU Functions

The C2000 MCU samples the I/O voltage and current value with a 4.6-MSPS high-speed ADC converter and quickly calculates the duty ratio of each converter with 60 MIPS high-speed calculation unit and then sends out PWM signals to control all four channel converters.

PWMH (HRPWM) is for the main switch, and PWML is for the auxiliary switch.

3.5 PCB Layout Design

The four converters, shown in Figure 3, have the same 24-V input power supply.

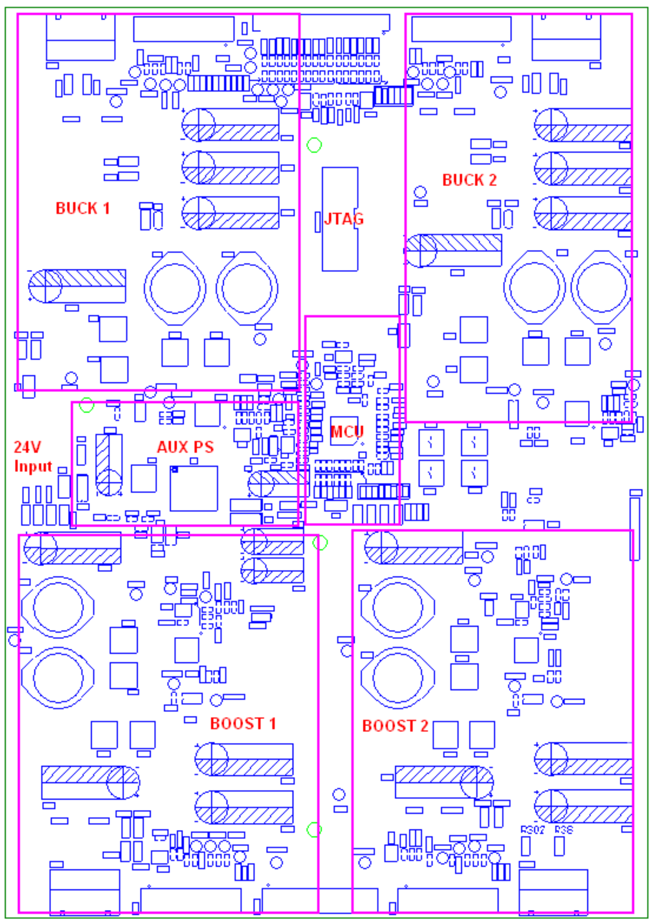


Figure 3. PCB Layout Design

4 Firmware Design

4.1 Firmware Tasks

The entire firmware system is a forward-background system. Figure 4 shows the background structure.

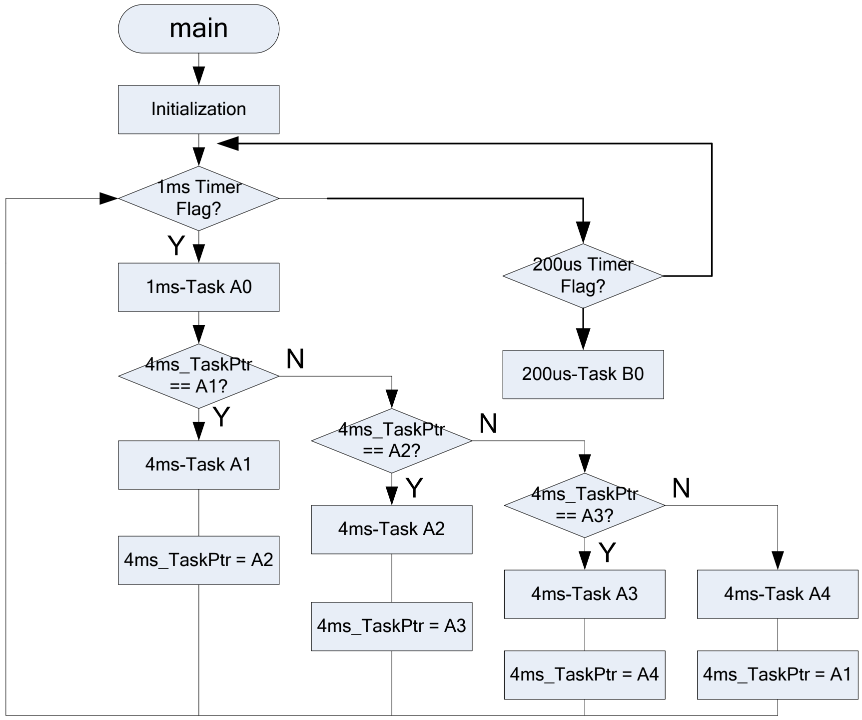


Figure 4. Background Structure

- **200μs – Task B0:** The 200-μs task deals with the protection.
- **1ms – Task A0:** The 1-ms periodical task. The soft-start process is performed in this task.
- **4ms – Task A1:** The task deals with the status machine of the system.
- **4ms – Task A2:** The task deals with the ADC calibration in the power on stage, and it also execute the SFO function periodically, which is used by the HRPWM module.
- **4ms – Task A3:** The task detects the key operation, finishes the auto-restart detection, and sends the command.
- **4ms – Task A4:** The task detects the input voltage range. When the input voltage is out of range, it generates a fault status.

4.2 The Status Machine

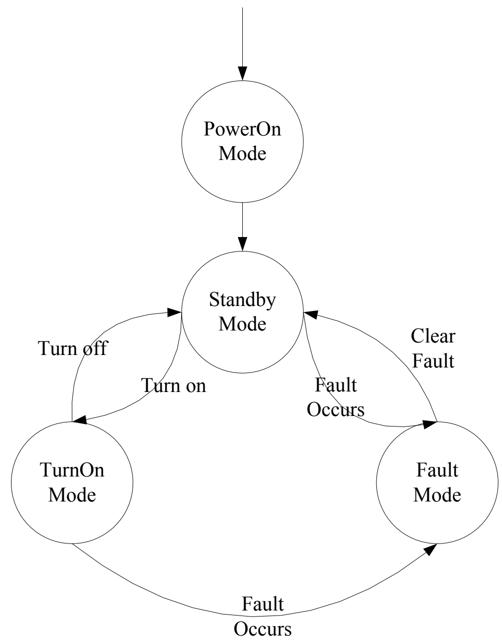


Figure 5. Status Machine Flow Chart

There are four running modes in this system:

- Power-on
- Standby
- Turn-on
- Fault

When the power is on, the MCU starts to work. First, it gets into power-on mode. In this mode, the system deals with the initializations. When the initialization is finished, the system goes automatically to standby mode.

In standby mode, the system responds to a command only when the user presses the appropriate key. When a turn-on command exists, the corresponding buck or boost converter turns on its PWM, and soft-starts the reference voltage, after which the system enters turn-on mode.

In turn-on mode, only some of the converters may be working. If a converter is not working, the converter also can be turned on by the user. If one of the converters contains a fault, the fault status of that converter is recorded while the remaining converters continue to run.

When all the converters have faults, the system goes to fault mode, and all the PWMs turn off. Fault mode can be cleared by powering on again or by pressing and holding any key for more than 1 second. When the fault is cleared, the system returns to standby mode.

4.3 The Key and LED Specification

There are four user keys on the board. Table 3 summarizes the key functions.

Table 3. Key Definition

	SW1	SW2	SW3	SW4
BUCK1	Turn ON/OFF	X	X	X
BUCK2	X	Turn ON/OFF	X	X
Boost1	X	X	Turn ON/OFF	X
Boost2	X	X	X	Turn ON/OFF

When the system is in fault mode, pressing and holding any key for more than 1 second clears the fault.

If there is an LED in this system, the LED flashes follow the rules defined in Table 4.

Table 4. LED Flashing Specification

	Power On Mode	Standby Mode	Turn On Mode	Fault Mode
LED1 flashing	Always OFF	Flashing in every 0.6 second	Flashing in every 1.2 seconds	Always ON

4.4 The Interrupt Service Routine

All the algorithms execute in the interrupt service routine (ISR), which is triggered by the EOS of the ADC. In the MCU initialization, the ADC sampling is triggered in every three switching cycles. To handle the four converters, the ISR must execute the different calculation task in a specified time slot.

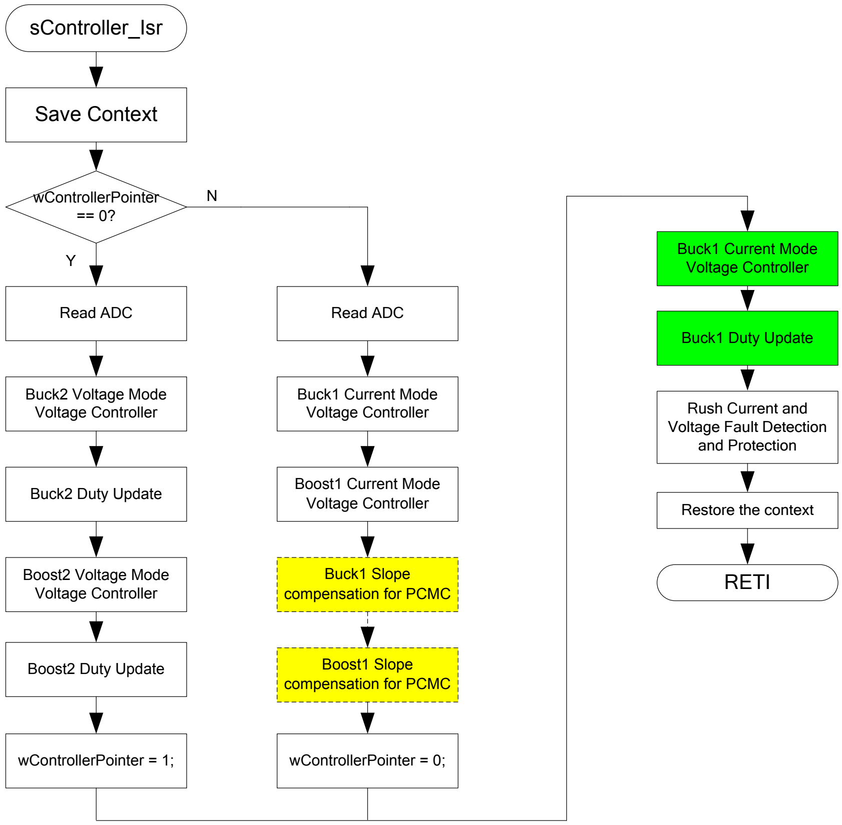


Figure 6. The ISR Flow Chart

The ISR is divided into two time slots: the first interrupt deals with the voltage mode controller calculation and the second interrupt deals with the current mode voltage loop. The duty cycle is updated in every interrupt.

4.5 The Algorithms

4.5.1 The Voltage Mode

Voltage mode control controls the output voltage by a single output voltage loop, and the controller simply regulates the duty cycle in different running conditions. For example, consider the buck topology (see Figure 7 for the voltage mode closed-loop block diagram).

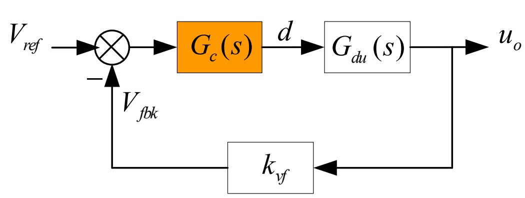


Figure 7. Voltage Mode Control Block Diagram

Equation (1) shows the open-loop transfer function:

$$G_{open} = G_c(s)G_{du}(s)k_{vf} \tag{1}$$

$G_c(s)$ is the closed- loop controller, and k_{vf} is the voltage sampling ratio.

From Equation (1), we can see that $G_{du}(s)$ has a low-frequency pole that greatly affects the frequency response of the system by slowing down the bandwidth and reducing the phase margin. To reduce the effect of this pole, we need a zero to offset the pole.

Therefore, it is better to choose a controller as shown in Equation (2):

$$G_c(s) = \frac{K(s+a)(s+b)}{s(s+c)} \tag{2}$$

$a = \frac{1}{RC}$ is an offset zero to the pole of $G_{du}(s)$.

b is a high-frequency zero to compensate the phase, and c is a high-frequency pole to reduce the high-frequency noise. Besides, we need an integral element to reduce the static difference of the controller.

For the detail controller design, see the reference documentation in Section 8, *References*.

4.5.2 The Average Current Mode

Current mode control means to regulate the output voltage by internal current loop and an external voltage loop controller. The inductor current and the output voltage are controllable in an external voltage loop controller. Figure 8 shows the current mode control block diagram.

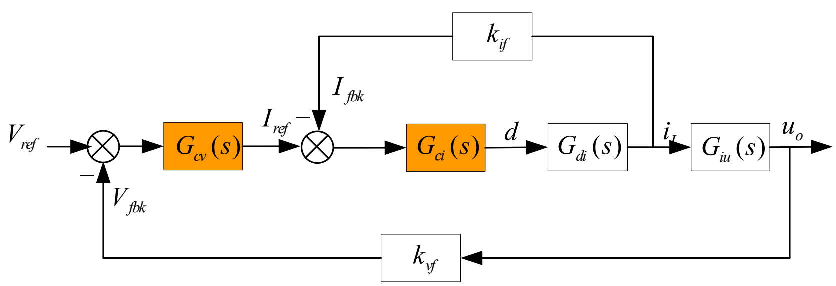


Figure 8. Current Mode Block Diagram

When designing the multiloop system, the most important factor is the design of the current loop controller for the system. Also, the internal loop must be designed first. From Figure 8, we can get the internal open-loop transfer function is:

$$G_{open\_i} = G_{ci}(s)G_{di}(s)k_{if} \tag{3}$$

The internal loop object is the transfer function from the duty cycle to the inductor current $G_{di}(s)$. From the preceding analysis, this object is integral. To regulate this kind of object, the PI controller can be used.

Equation (4) reflects a PI controller that adds a high-frequency pole, which can reduce the high-frequency noise of the system.

$$G_{ci}(s) = \frac{K(s+b)}{s(s+a)} \quad (4)$$

If the design of the internal loop is fast enough, the internal loop of the system can be considered as a gain, so the external loop object is similar to the integral, and the PI controller can be used for the external loop.

$$G_{cv}(s) = \frac{K(s+b)}{s(s+a)} \quad (5)$$

To ensure the stability of the system, the internal loop must be much faster than the external loop. Therefore, it is necessary to choose the proper bandwidth for both current loop and voltage loop. In the 300-kHz switching frequency application, a 60-MHz MCU cannot execute a 1-cycle controller algorithm because the CPU speed is not fast enough to finish the calculation for the controller in 3.3 μs. In addition, the sampling delay in the closed loop, which greatly reduces the phase margin of the system, cannot be neglected. So, we must reduce the sampling rate and the controller execution rate to reduce the CPU load and the effect of the sampling delay.

For the detail design for the controller, see the reference documentation in Section 8, *References*.

4.5.3 Peak Current Mode

The control block diagram of the peak current control is nearly the same as the block diagram of the average current control mode. The difference is that the internal comparator does the internal loop of the peak current mode.

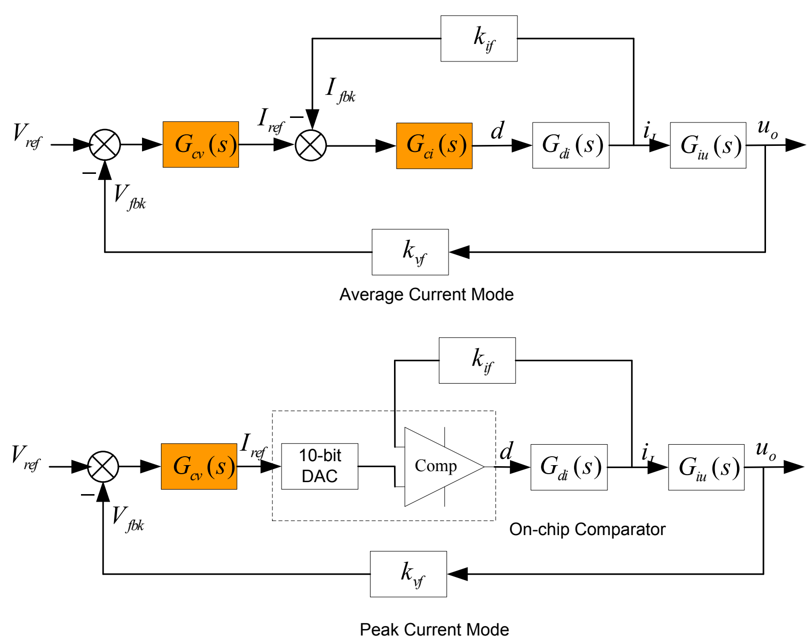


Figure 9. Control Block Diagram

For the peak current mode control, as with average current mode, only a voltage loop controller must be designed.

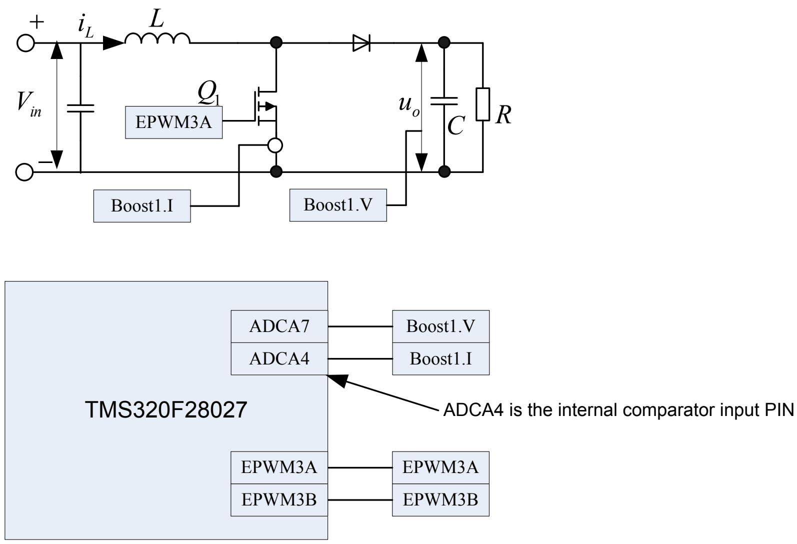


Figure 10. Block Diagram of the Implementation

Using the Piccolo A MCU as the main controller, the EPWM3A is the PWM output pin and the IGBT current is sampled as the inductor current. Also, the output voltage is sampled to design the voltage loop.

In peak current mode, software only needs to calculate the voltage loop, after which the reference current is determined. The reference current is written to the internal 10-bit DAC to let the comparator finish the current loop process. At the same time, the RAMP ratio must be updated when the reference current is changed.

The voltage loop and the slope compensation are executed every three switching cycles in the ISR.

5 How the System Works

5.1 System On

The converter is turned on by pressing the respective ON/OFF button.

5.2 Control Mode

To show the performance of our demo, the four converters run in different modes.

- Buck 1 is in average voltage mode.
- Buck 2 is in average current mode.
- Boost 1 is in peak current mode.

- Boost 2 is in average current mode.

5.3 Power Dissipations

Buck converter is an example.

The calculation for power loss in the lower MOSFET is simple, because virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($R_{ds(on)}$).

$$P_{low\_on} = {I_{out}}^2 \times R_{ds(on)} \times (1 - D) \tag{6}$$

In Equation 6, I_{out} is the average output current and D is the duty cycle (V_{out}/V_{in}).

An additional term can be added to the loss equation of the lower MOSFET to account for additional loss accrued during the dead time when inductor current is flowing through the body diode of the lower MOSFET. This term is dependent on the diode forward voltage (V_d) and the switching frequency, F_s, and the length of dead times.

$$P_{low\_off} = \frac{1}{6} \times V_d \times I_{out} \times F_s \times (t_{d1} + t_{d2}) \tag{7}$$

In addition to $R_{ds(on)}$ losses, a large portion of the upper MOSFET losses are due to currents conducted across the input voltage (VIN) during switching. Because a substantially higher portion of the upper MOSFET losses are dependent on switching frequency, the power calculation is more complex.

$$P_{up\_on} = {I_{out}}^2 \times R_{ds(on)} \times D \tag{8}$$

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. At turn on, the upper MOSFET begins to conduct and this transition occurs over a time, t_2. The approximate power loss is P_{up_off}.

$$P_{up\_off} = \frac{1}{6} \times V_{in} \times I_{out} \times F_s \times (t_1 + t_2) \tag{9}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations (8) and (9).

The output inductor is another key loss. DCR is the DC resistance of the output inductor and P_{fe} is the ferrite core loss.

$$P_l = {I_{out}}^2 \times DCR + P_{fe} \tag{10}$$

The total dissipation P_d is:

$$P_d = P_{low\_on} + P_{low\_off} + P_{up\_on} + P_{up\_off} + P_l \tag{11}$$

Because the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Also, the dead time of the two PWM signals would affect the total efficiency. It is very easy to optimize the dead time with a C2000 MCU emulator.

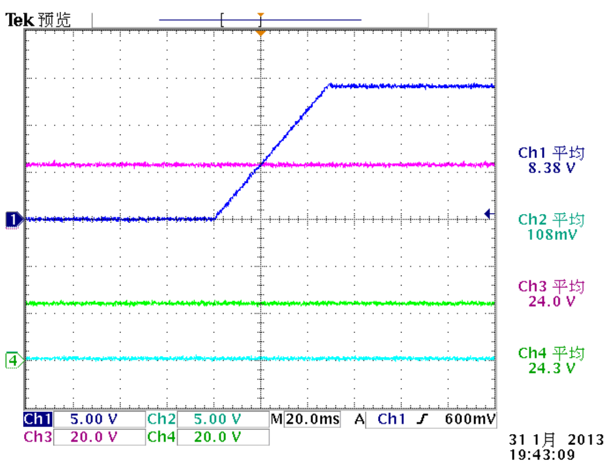
5.4 System Off

The converter is turned off by pressing the respective ON/OFF button again.

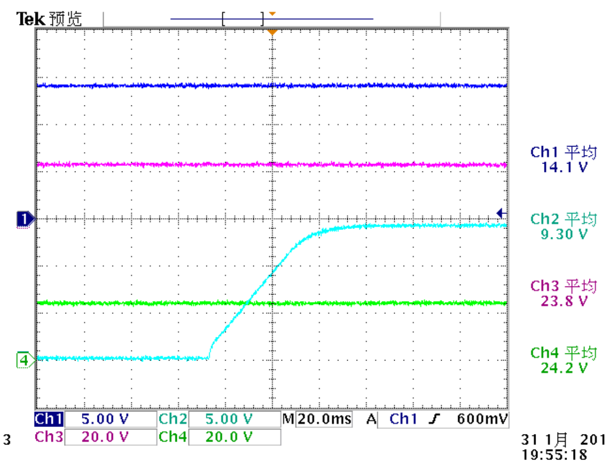
6 Measurements

6.1 Startup Waveform

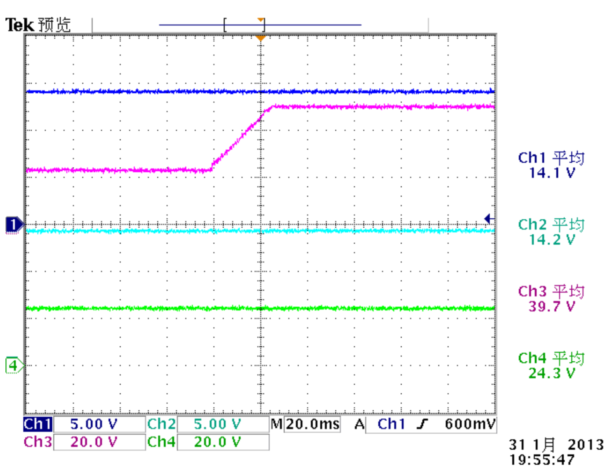
In demo board, there are four switches for four converters to power on/off them. After pressed the “ON/OFF” button, C2000 MCU would power on the respectively channel. We can see the startup waveform is very smooth and no overshoot.



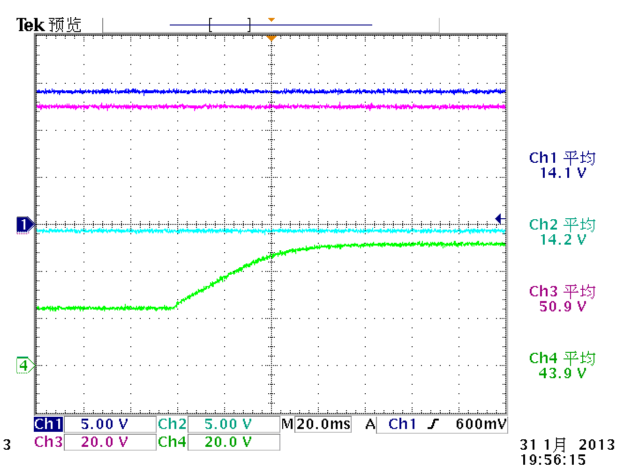
a) Buck 1 startup



b) Buck 2 startup



c) Boost 1 startup



d) Boost 2 startup

Figure 11. Startup Waveforms

6.2 Transient Load

Figures 12 through 15 show the test condition of transient load:

- 0% to 100% with approximately 0 load
- 1A/uS slew rate

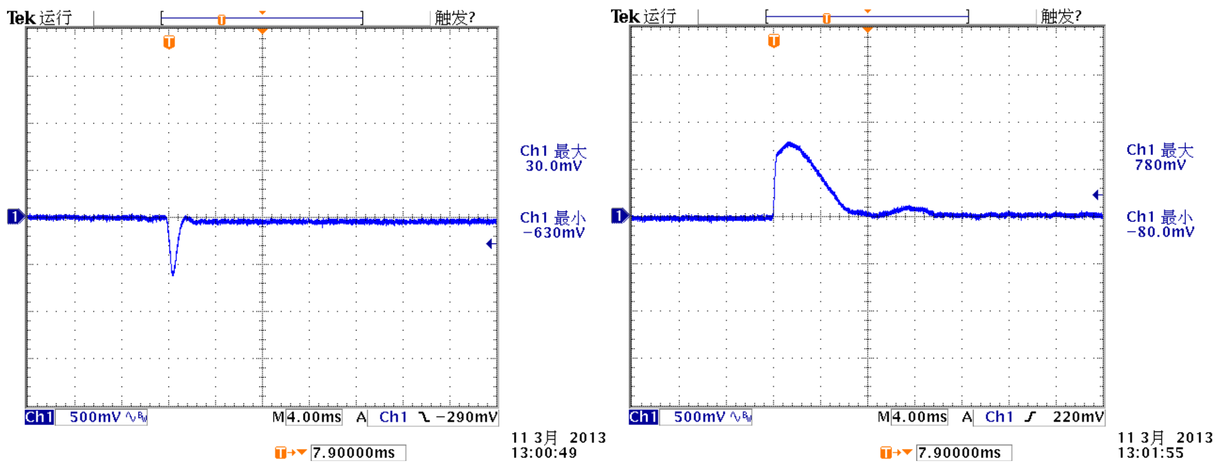


Figure 12. Buck 1 Transient Load

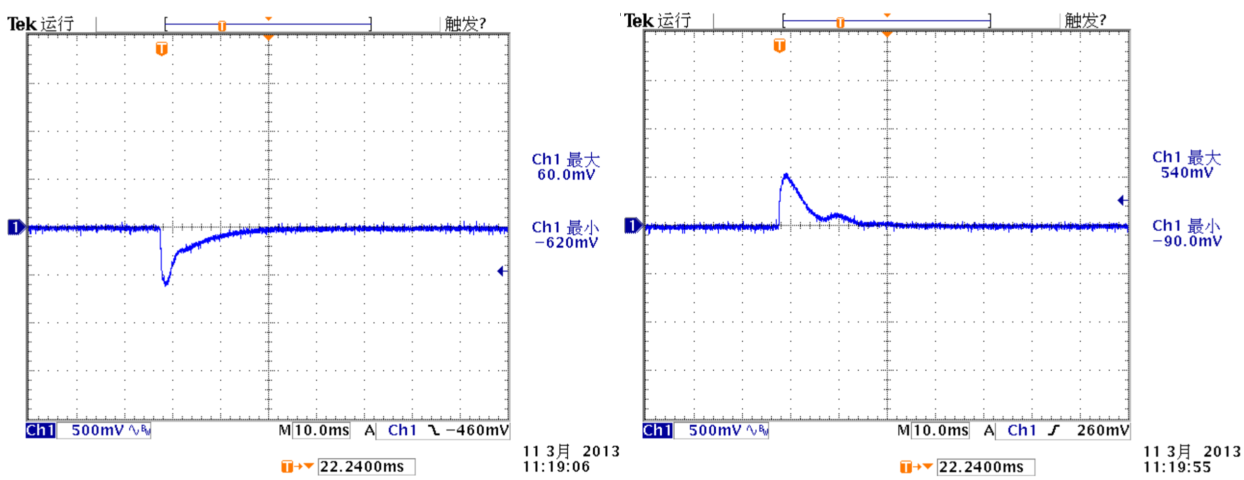


Figure 13. Buck 2 Transient Load

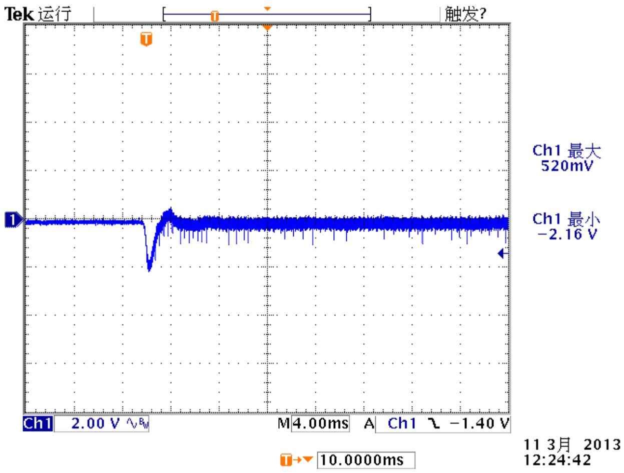


Figure 14. Boost 1 Transient Load

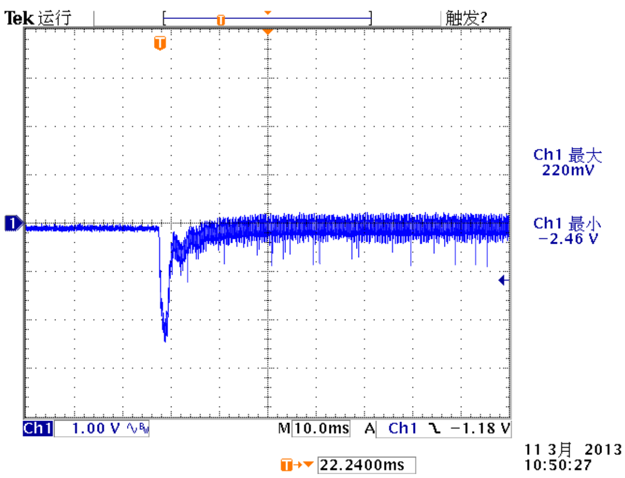
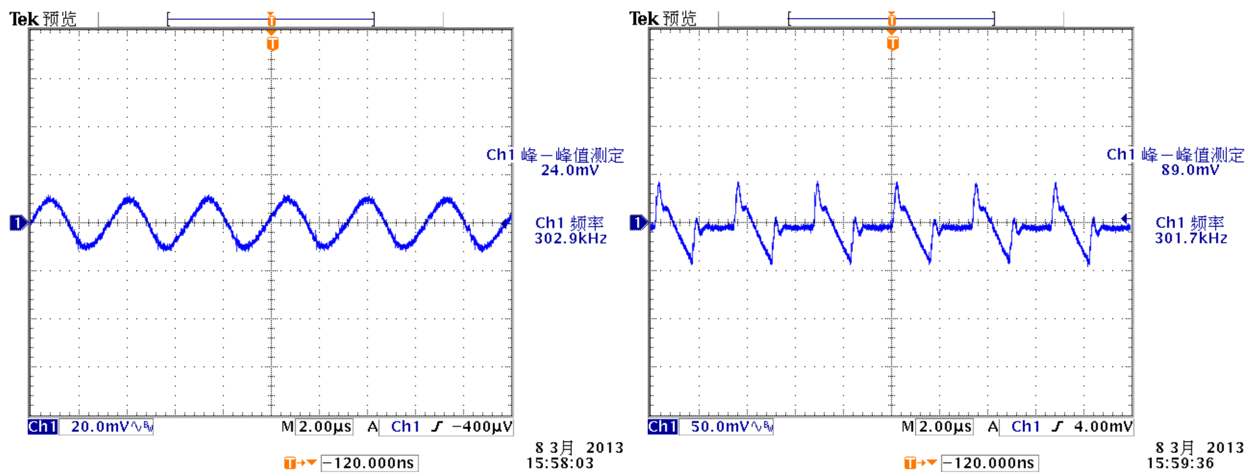


Figure 15. Boost 2 Transient Load

We received a good transient load response, which is approximately 5% to 6% of output voltage.

6.3 Output Ripple Voltage

Figure 16 shows the test results of output ripple voltage. The ripple voltage is the same because we used synchronous rectify technology.



a) Buck Converter b) Boost Converter

Figure 16. Output Ripple Voltage

7 Fault Management

When input UVP/OVP occurs, the output shuts down.

When output OVP occurs, the output latches off.

When output OCP occurs, the converter goes into hiccup mode (that is, the converter shuts off the power supply for a given time and then tries to restart the power).

8 References

1. *TMS320F28027/28026/28023/28022/28021/28020/280200 Piccolo Microcontrollers (Rev. I) Datasheet,* SPRS523I

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