Application Note

Key Design Points of F28P65x in High-Power BBU DC/DC

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ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAGA1)

This paper introduces the implementation of Peak Current Mode (PCM) control for a multiphase interleaved Boost converter suitable for BBU using the TI C2000™ F28P65x series microcontrollers. This paper elaborates on the C2000 signal processing path and configuration recommendations, and proposes configuration methods for on-chip cycle-by-cycle (CBC) current limiting and inductor negative current shutdown, while introducing the advantages of dual-CPU co-working and the non-disruptive online upgrade process, providing design guidance for high-power DC/DC in data center BBU/CBU applications.

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1 Introduction

The BBU (Battery Backup Unit) in data centers needs to quickly take over load power supply within 2~5 minutes after AC/PSU power outage to buy time windows for bus switching, load migration, and safe shutdown. As the sole power interface between the battery and the data center bus, the dynamic response capability of the DC/DC converter directly determines the availability of the BBU.

Traditional analog control schemes (such as peak current mode PWM controllers) lack flexibility in the face of requirements like multiphase paralleling, online parameter adjustment, and firmware upgrades. The F28P65x series DSP, due to its rich integrated peripherals, efficient loop control, and dual-CPU multi-Flash Bank features, can overcome the challenges of high power density, dynamic response, and non-disruptive online upgrades in BBU applications. Taking an asymmetric interleaved scheme with multiphase discharge Boost and charge Buck as an example, this paper introduces the hardware signal chain design, software configuration methods, and key points of dual-CPU co-working for F28P65x to achieve peak current mode control.

2 BBU Interleave DC/DC Topology and Control Framework

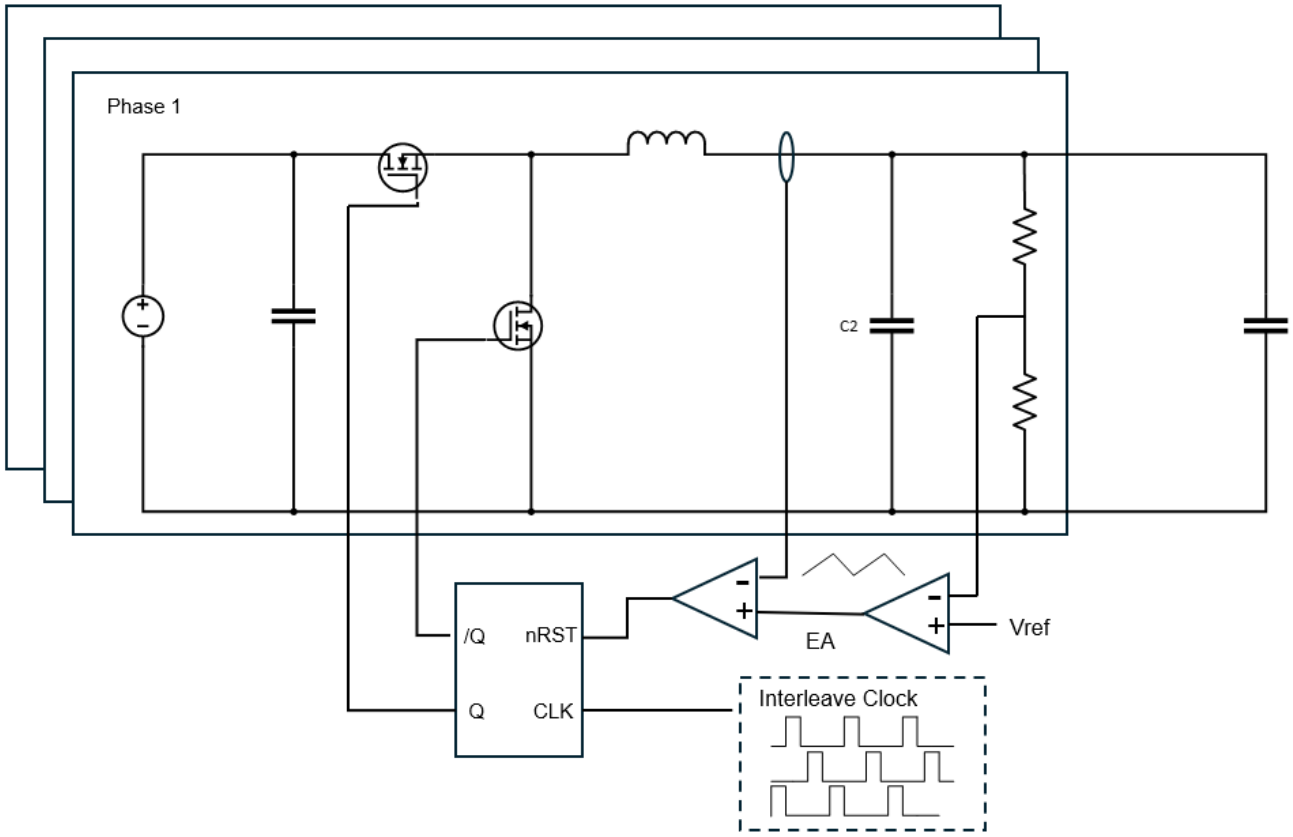


Figure 2-1. Interleaved BOOST Topology

BBU/CBU requires extremely high power density. Non-isolated interleaved Buck/Boost is widely used due to its advantages of small magnetic component volume and ripple cancellation to reduce output capacitance. Data centers generally do not require fast charging for BBU, but require it to provide massive emergency peak power within a short period (typically 2-5 minutes); therefore, the number of charging phases is generally smaller than that of discharging phases. As shown in Figure 2-1, since the charging Buck is easy to implement, this system takes the multiphase interleaved discharge Boost as an example for introduction. In certain scenarios with higher power density requirements, bidirectional Buck/Boost topology is also selected, but it also brings challenges in redundancy design and charge/discharge timing control.

The control challenges lie in the dynamic performance requirements during load empty-to-full switching and phase-to-phase current sharing. Peak current mode (PCM) control is generally used in design. Through the inner current loop, the inductor acts as a controlled current source, reducing the small-signal transfer function of the traditional Boost to a first-order single-pole system, avoiding the risk of phase deterioration caused by the right half-plane zero (RHPZ), and allowing the control bandwidth of the outer voltage loop to be significantly widened to enhance system dynamic performance. Phase-to-phase current sharing adopts an adaptive scheme sharing COMP, where PWM comparators across phases uniformly use the same voltage error signal as input to compare with peak current signals before triggering duty cycles. When an inductor inductance in a certain phase is smaller and causes a faster current rising slope, the phase current will trigger the comparator flip earlier at the same threshold, thereby producing a narrower duty cycle within that cycle and automatically suppressing average energy output. The entire current sharing process is completed at the cycle-by-cycle hardware level without occupying ADC sampling channels or main control processing resources. Compared with droop methods and democratic current sharing methods, it offers significant advantages in integration.

3 F28P65X Real-Time Control Signal Path

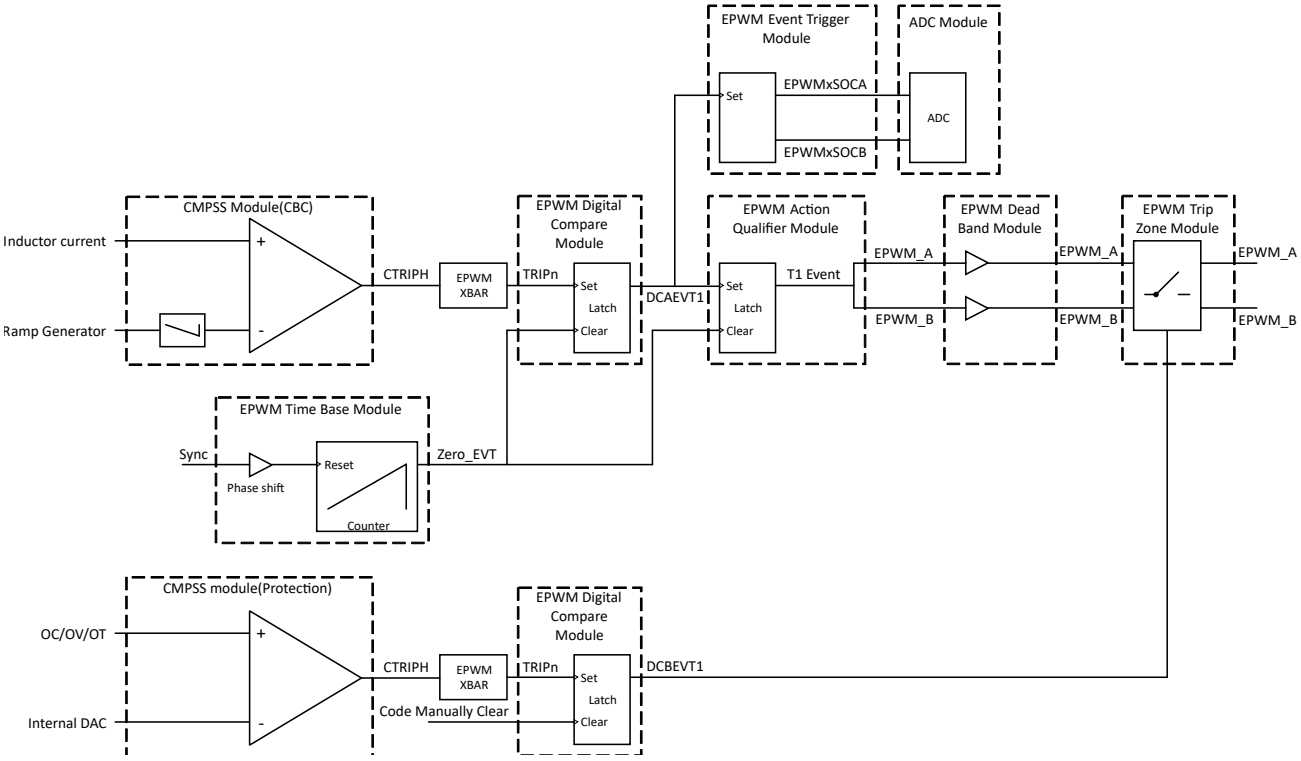


Figure 3-1. F28P65X Control Signal Path

This section introduces the design of the real-time control signal path of F28P65X. As shown in Figure 3-1, the signal path mainly consists of peripherals such as CMPSS, EPWM XBAR, EPWM, and ADC. Compared to the common method of using Trip Zone to generate CBC control, this paper uses Action Qualifier to generate CBC control signals. The advantage of this method lies in solving the challenge where the Trip Zone module in EPWM is located behind the Dead Band module and thus cannot superimpose dead-band control. Using the Action Qualifier module to generate CBC signals allows superimposing dead-band control signals because Action Qualifier precedes the Dead Band module; furthermore, the Trip Zone module can be used to generate protection signals that shut down all PWM signal outputs.

The usage and functions of each peripheral module are described in detail below.

- CMPSS: The comparator reference can be set to an internal ramp generator or DAC. The first function is using the ramp generator as a reference benchmark to compare with the inductor current to generate CBC control signals; the second function is using the internal DAC as a reference benchmark to compare with fault signals (overcurrent, overvoltage, overtemperature, etc.) to trigger a one-shot PWM shutdown protection signal when a fault occurs.
- EPWM X-BAR: Processes the CMPSS trigger event CTRIPH into a TRIP signal that can be used by the EPWM Digital Compare module.
- EPWM Digital Compare: This module processes the TRIP signal provided by EPWM X-BAR into a DCAEVT1 event for the Action Qualifier module to perform CBC control, while passing this DCAEVT1 event to the Event Trigger module to trigger ADC peak current sampling when a CBC event occurs. In addition, this module also processes the TRIP signal provided by EPWM X-BAR into a DCBEVT 1 event for the Trip Zone module to perform one-shot protection.
- EPWM Action Qualifier: This module processes the DCAEVT1 event received from the Digital Compare module into a T1 event, and defines the outputs of EPWM channels A and B at the zero point of the EPWM period and when the T1 event occurs, thereby realizing the CBC function.
- EPWM Dead Band: This module adds a dead band between the two switch tubes, avoiding potential damage caused by simultaneous conduction.

- EPWM Trip Zone: This module receives the DCBEVT 1 event passed from Digital Compare and defines the behavior of upper and lower switch tubes when the event occurs, thereby shutting down all PWM output signals to protect hardware circuitry upon fault occurrence.
- EPWM Event Trigger: This module receives the DCAEVT1 event from the Digital Compare module and uses this event to trigger ADC peak current sampling.

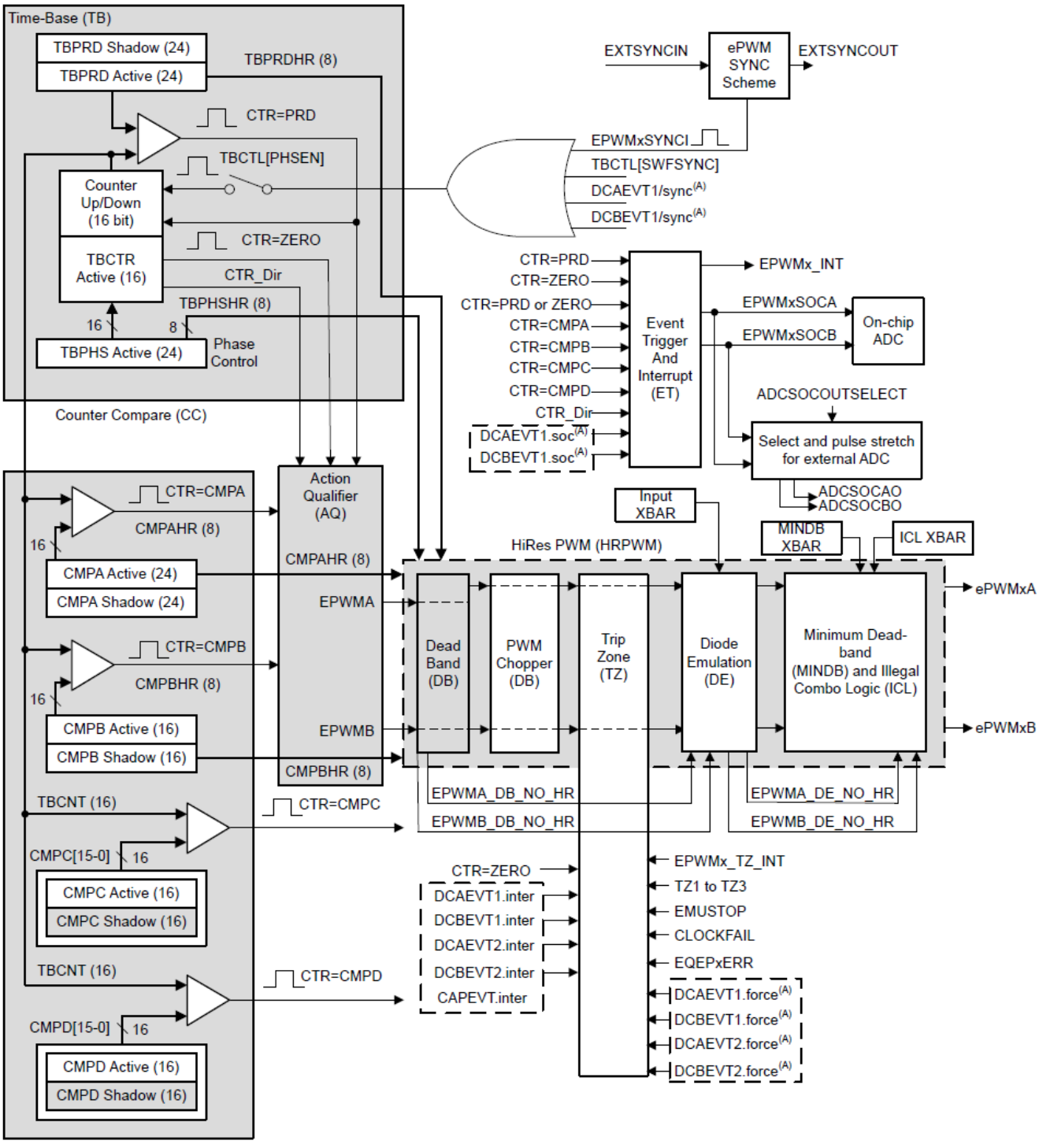


Figure 3-2. EPWM Block Diagram

4 F28P65X Hardware SysConfig Configuration and Project Implementation

4.1 CMPSS Configuration Considerations

4.1.1 CMPSS Ramp Compensation and Cycle-by-Cycle Current Limiting

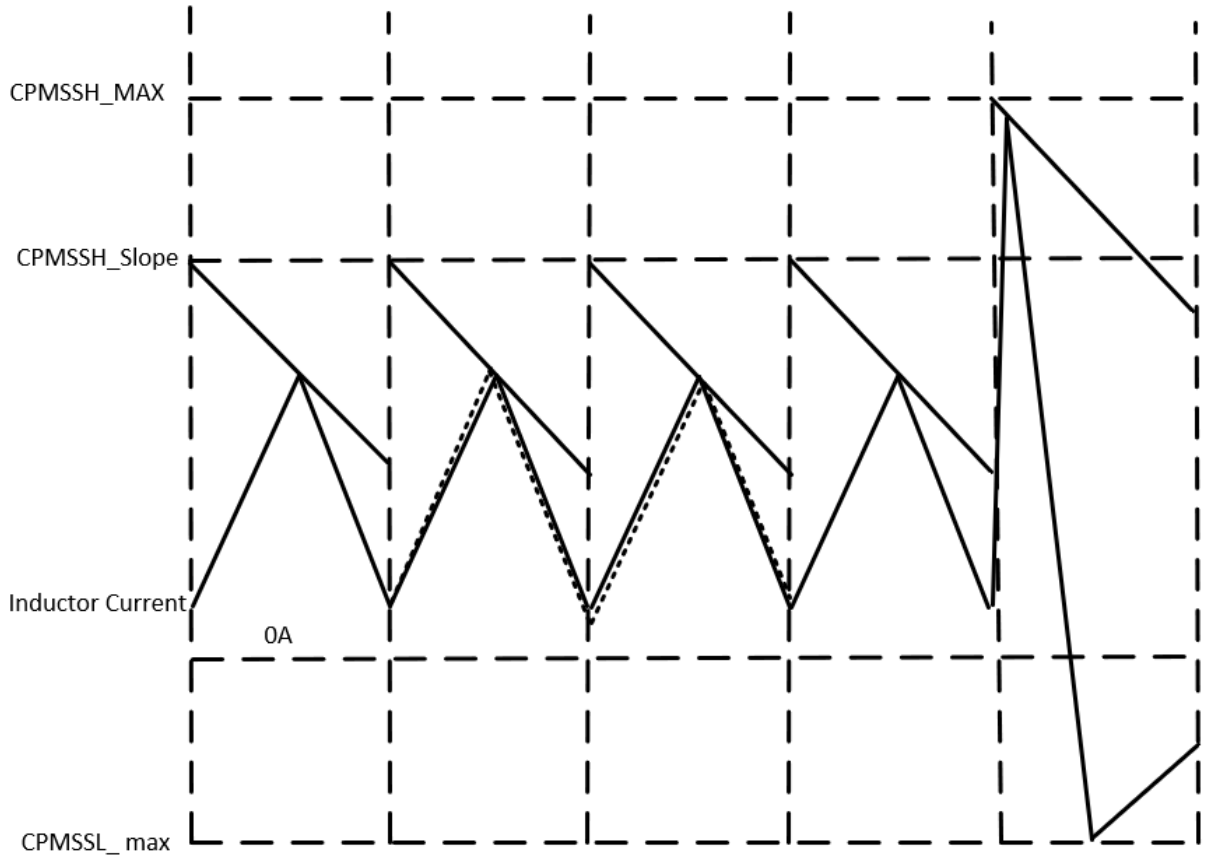


Figure 4-1. CPMSS PCM Control

In the multiphase Boost discharge circuit, we allocate a CMPSS comparison module to each Boost output phase to trigger the capture of CBC events under peak control mode. Because the input end of the BBU is a battery, it has a wide input voltage range and operates in Continuous Conduction Mode (CCM). Duty cycles exceeding 50% are common, and this operating condition can cause sub-harmonic oscillation in the inner current loop due to error non-convergence. Therefore, the design of ramp compensation is particularly important.

The CMPSS module operates in count-down mode, setting the corresponding Ramp Generator Step Value and Ramp Clock Frequency according to the falling slope of the inductor current. The synchronization source of the ramp generator is then configured as the corresponding EPWM module, so that the ramp generator resets its value to the preset maximum at the start of the EPWM period.

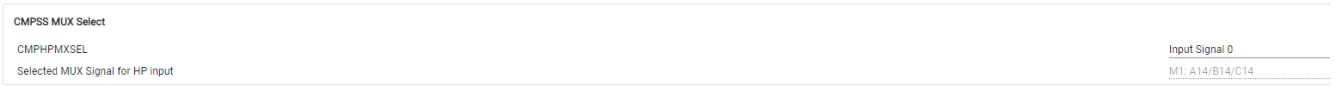
Cycle-by-cycle current limiting protection (CBC) is generally used to protect the inductor peak current within a switching period, usually implemented by external analog circuits or additional comparator circuits. CMPSS offers another possibility: by limiting the Max Ramp Generator Reference Value to the maximum allowable inductor current, CBC can be conveniently achieved through a single CMPSS without any extra external circuits, making it suitable for applications with high power density requirements such as BBUs. However, the following points also need to be noted:

1. Because there is a certain delay from CMPSS to the final PWM (typically around 50ns), design redundancy for inductors and power devices must be fully considered.
2. The setting of the maximum initial value should be fully considered during design, as RAMP decreases with continuous turn-on of the duty cycle, resulting in single-cycle energy output limitation.

Based on the above explanations, the specific configuration process of CMPSS is as follows:

1. The ramp generator configuration is as follows, with the maximum reference value range being 0-65535. Based on the step value and clock frequency, the reference voltage at maximum period can be calculated. It should be noted here that the reset time of the maximum reference value is bound to the EPWM module:

2. The CMPSS positive input pin configuration is as follows; each CMPSS has up to four selectable input pins.



3. DAC-related configurations are set as follows.

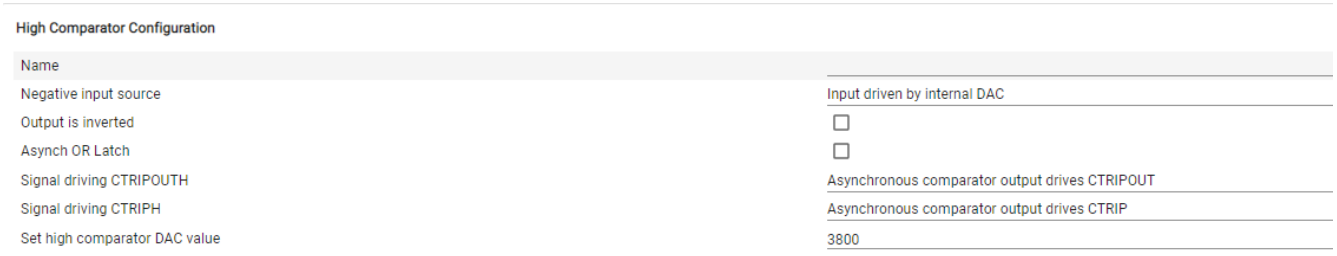
4.1.2 Application of CMPSS Negative Current Shutdown

In high-power synchronous Boost, negative inductor current in the freewheeling phase should be carefully considered. Excessive negative current leads to energy backfeeding, posing a risk of DC/DC damage. This paper proposes a concise configuration method also based on the CMPSS module: each CMPSS module features two internal comparator modules (CMPSSH/CMPSSL), where CMPSSH is responsible for duty cycle generation and CMPSSL is configured for negative current identification. Under potential negative current conditions in FCCM mode, CMPSSL triggers the negative current threshold to shut down the synchronous tube drive, thereby protecting the circuit. Similarly, this module can also be used to realize Zero Voltage Switching (ZVS).

For the CMPSS module used for negative current protection, we directly use a fixed DAC value instead of the ramp generator.

4.1.3 CMPSS Fault Protection

When fault conditions such as overvoltage and overcurrent occur, the system needs to quickly identify fault events and execute protection actions. Fault condition identification can be captured using the CMPSS module with the internal DAC as the reference benchmark.



4.2 EPWM XBAR Configuration

Comparator triggers from the CMPSS module can be converted via EPWM XBAR into TRIP signals used by the EPWM module. The specific EPWM XBAR configuration for the CMPSS module is shown below; note that this configuration can only be implemented in the CPU1 project:

Name	Boost_1_XBAR
Trip Input	TRIP4 of the ePWM X-BAR
Invert Mode	☐
Auto Enable Mux Setting From Source	☐
Mux Selection Method	
MUXes to be used	MUX 06
MUX 6 Config	CMPSS4 CTRIPH

The specific introduction of Mux Selection can be reviewed in Chapter 16.2 of the user manual TMS320F28P65x Real-Time Microcontrollers datasheet (Rev. D).

4.3 EPWM Configuration

4.3.1 Interleaved PWM Global Configuration

EPWM is the final PWM control module. In interleaved applications, the phase shift of each phase should be 360°/n to cancel output current ripple, which requires us to define the period and counting mode of the EPWM. This paper uses the Phase Shift function to configure the phase difference of each EPWM, taking one selected EPWM as a reference to configure the phase shift angle of other EPWM modules. The reference configuration is as follows:

EPWM Time Base	
Emulation Mode	Stop after next Time Base counter increment or decrement
Time Base Clock Divider	Divide clock by 2
	ⓘ For perfectly synchronized TBCLKs across multiple EPWM modules, th
High Speed Clock Divider	Divide clock by 1
Time Base Period Load Mode	PWM Period register access is through shadow register
Time Base Period Load Event	Shadow to active load occurs when time base counter reaches 0
Time Base Period	2000
Time Base Period Link	Disable Linking
Enable Time Base Period Global Load	☐
Initial Counter Value	0
Counter Mode	Up - count mode
Enable Phase Shift Load	☑
	ⓘ If the EPWMxSYNCI signal is held HIGH, the sync will NOT continously
Phase Shift Value	400
Force a Sync Pulse	☐
Sync In Pulse Source	Sync-in source is EPWM6 sync-out signal
Sync Out Pulse	Counter zero event generates EPWM sync-out pulse
One-Shot Sync Out Trigger	Trigger is OSHT sync
EPWMxSYNCPER Source Select	Counter equals zero

4.3.2 Single-Phase EPWM Module Configuration

In the Digital Compare module of EPWM, the Trip 4 event routed from EPWM X-BAR can be further processed into a DCAEVT1 event usable by the Action Qualifier module for peak control. Note that this event is also the event that triggers ADC SOC; the specific configuration reference is as follows:

EPWM Digital Compare

DCAEVT1 and DCAEVT2

Digital Compare A High	Trip 4
Combination Input Sources (Digital Compare A High)	None
Digital Compare A Low	Trip 1
Combination Input Sources (Digital Compare A Low)	None
Condition For Digital Compare output 1 A	Event when DCxH high
Condition For Digital Compare output 2 A	Event is disabled
Generate ADC SOC (DCAEVT1)	☑
Generate SYNCOUT (DCAEVT1)	☐
Synch Mode (DCAEVT1)	DC input signal is synced with TBCLK
Signal Source (DCAEVT1)	Signal source is unfiltered (DCAEVT1/2)
CBC Latch Mode (DCAEVT1)	DC cycle-by-cycle(CBC) latch is disabled
CBC Latch Clear Event (DCAEVT1)	Clear CBC latch when counter equals zero
Synch Mode (DCAEVT2)	DC input signal is synced with TBCLK
Signal Source (DCAEVT2)	Signal source is unfiltered (DCAEVT1/2)
CBC Latch Mode (DCAEVT2)	DC cycle-by-cycle(CBC) latch is disabled
CBC Latch Clear Event (DCAEVT2)	Clear CBC latch when counter equals zero

The Action Qualifier module is responsible for processing DCAEVT1 into a T1 event; the reference configuration is as follows:

EPWM Action Qualifier

Enable Continuous SW Force Global Load	☐
Continuous SW Force Shadow Mode	Shadow mode load when counter equals zero
T1 Trigger Source	Digital compare event A 1 T1/T2 selection and configuration of a trip/digital-compar submodule
T2 Trigger Source	Digital compare event A 2 T1/T2 selection and configuration of a trip/digital-compar submodule

Further define the behaviors of EPWMxA and EPWMxB channels when counter zero event and T1 event occur as follows:

ePWMxA Event Output Configuration

ePWMxA Time base counter equals zero	Set output pins to High
ePWMxA Time base counter equals period	No change in the output pins
ePWMxA Time base counter up equals COMPA	No change in the output pins
ePWMxA Time base counter down equals COMPA	No change in the output pins
ePWMxA Time base counter up equals COMPB	No change in the output pins
ePWMxA Time base counter down equals COMPB	No change in the output pins
ePWMxA T1 event on count up	Set output pins to low
ePWMxA T1 event on count down	No change in the output pins
ePWMxA T2 event on count up	No change in the output pins
ePWMxA T2 event on count down	No change in the output pins

ePWMxB Event Output Configuration

ePWMxB Time base counter equals zero	Set output pins to low
ePWMxB Time base counter equals period	No change in the output pins
ePWMxB Time base counter up equals COMPA	No change in the output pins
ePWMxB Time base counter down equals COMPA	No change in the output pins
ePWMxB Time base counter up equals COMPB	No change in the output pins
ePWMxB Time base counter down equals COMPB	No change in the output pins
ePWMxB T1 event on count up	Set output pins to High
ePWMxB T1 event on count down	No change in the output pins
ePWMxB T2 event on count up	No change in the output pins
ePWMxB T2 event on count down	No change in the output pins

At this point, channels A/B of EPWM can directly complete CBC control based on the CTRIPH flip event triggered by CMPSS.

Next, we add dead-band control for upper and lower tubes. This function can be implemented in the Dead Band module; reference configuration is as follows:

EPWM Dead-Band

Common Dead-Band Modes Mode for the Dead-Band Submodule

Rising Edge Delay Input	Input signal is ePWMA
Falling Edge Delay Input	Input signal is ePWMA
Rising Edge Delay Polarity	DB polarity is not inverted
Falling Edge Delay Polarity	DB polarity is inverted
Enable Rising Edge Delay	☑
RED Shadow Load Event	Load when counter equals zero
Enable RED Shadow Mode	☐
Rising Edge Delay Value	50
Enable Falling Edge Delay	☑
FED Shadow Load Event	Load when counter equals zero
Enable FED Shadow Mode	☐
Falling Edge Delay Value	50
Swap Output for EPWMxA	☐
Swap Output for EPWMxB	☐
Enable Deadband Control Global Load	☐
Deadband Control Shadow Load Event	Load when counter equals zero
Enable RED Global Load	☐
Enable FED Global Load	☐
Dead Band Counter Clock Rate	Dead band counter runs at TBCLK
Dead Band Rising Edge Delay Link	Disable Linking
Dead Band Falling Edge Delay Link	Disable Linking

In BBU applications, faults such as over/undervoltage, overcurrent, and overtemperature require shutdown lockouts, requiring EPWM to quickly turn off all outputs for protection. In the Digital Compare module, the routed Trip6 event can be processed into DCBEVT1; reference configuration is as follows:

DCBEVT1 and DCBEVT2

Digital Compare B High	Trip 6
Combination Input Sources (Digital Compare B High)	None
Digital Compare B Low	Trip 1
Combination Input Sources (Digital Compare B Low)	None
Condition For Digital Compare output 1 B	Event when DCxH high
Condition For Digital Compare output 2 B	Event is disabled
Generate ADC SOC (DCBEVT1)	☐
Generate SYNCOUT (DCBEVT1)	☐
Synch Mode (DCBEVT1)	DC input signal is synced with TBCLK
Signal Source (DCBEVT1)	Signal source is unfiltered (DCAEVT1/2)
CBC Latch Mode (DCBEVT1)	DC cycle-by-cycle(CBC) latch is disabled
CBC Latch Clear Event (DCBEVT1)	Clear CBC latch when counter equals zero
Synch Mode (DCBEVT2)	DC input signal is synced with TBCLK
Signal Source (DCBEVT2)	Signal source is unfiltered (DCAEVT1/2)
CBC Latch Mode (DCBEVT2)	DC cycle-by-cycle(CBC) latch is disabled
CBC Latch Clear Event (DCBEVT2)	Clear CBC latch when counter equals zero

The implementation of EPWM A/B one-shot protection action is executed in the Trip Zone module, with an interrupt registered, reference as follows.

EPWM Trip Zone

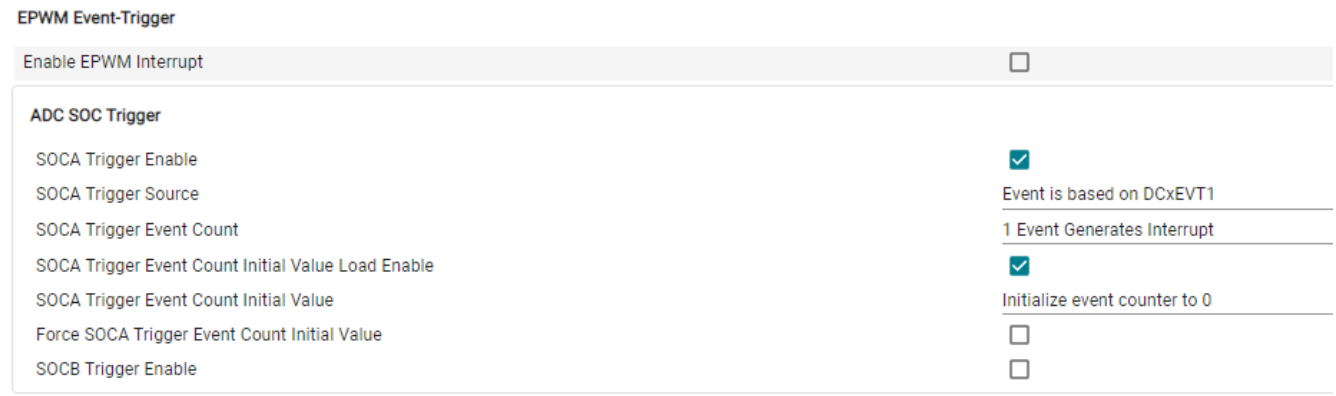
Use Advanced EPWM Trip Zone Actions	☐
TZA Event	Low voltage state Conflicting actions on the TZCTL, TZCTL2, TZCTLDC
TZB Event	Low voltage state Conflicting actions on the TZCTL, TZCTL2, TZCTLDC
DCAEVT1 Event	High impedance output
DCAEVT2 Event	High impedance output
DCBEVT1 Event	High impedance output
DCBEVT2 Event	High impedance output
One-Shot Source	One-shot DCBEVT1 For the condition to remain latched, a minimum of 3
Additional One-Shot Source	None
CBC Source	None
CBC Latch Clear Signal	Clear CBC pulse when counter equals zero
Additional CBC Source	None
TZ Interrupt Source (ORed)	Digital Compare B Event 1 interrupt
Register Interrupt Handler	☑
TRIPOUT Source	None

In the EPWM TZ Interrupt module, configure the interrupt service specifically, reference as follows:

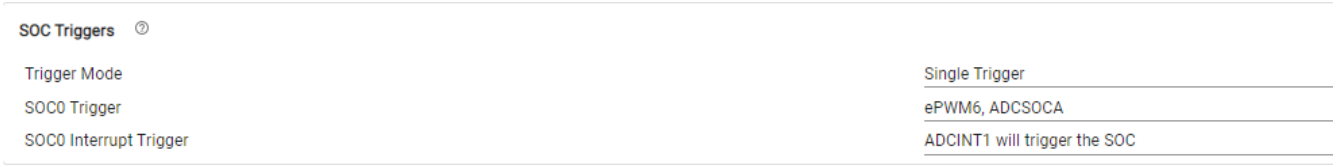
EPWM TZ Interrupt

Name	Boost_1_EPWM_TZ_INT
Interrupt Name	INT_Boost_1_EPWM_TZ
Interrupt Handler	INT_Boost_1_EPWM_TZ_ISR
Enable Interrupt in PIE	☑

Utilizing the DCAEVT1 event, the ADC SOC trigger source can be configured in the EPWM Event Trigger module, with specific configuration as follows.



In the ADC peripheral, this trigger source can be referenced, with configuration as follows:



5 F28P65x Dual-CPU Co-Working and Considerations

BBU system design generally has the following requirements:

1. Capabilities for both charging and discharging, generally with multiple Boost channels as discharge output and a single Buck channel as charge input
2. The Boost discharge circuit needs to run continuously at no load to meet dynamic requirements for instantaneous full load, while the Buck charge circuit operates only when the battery is depleted
3. As a backup power unit for data centers, the BBU requires online upgrades without stopping operation

F28P65x series DSPs offer optional dual cores, having two C28 cores and an additional CLA core to process loop calculation tasks in parallel, reducing DSP load pressure and increasing signal processing bandwidth by allocating different tasks to the two C28 cores. Meanwhile, regarding online upgrade requirements, F28P65x has 5 Flash Banks, which can meet the requirement of dual-core non-disruptive online upgrades. In summary, F28P65x is highly suitable for data center BBU applications. This paper proposes the following configuration method as a reference:

1. CPU1 + CLA provides ample computing power to handle loop calculation requirements for the multiphase Boost discharge circuit
2. CPU2 controls the single-phase Buck charge circuit and can simultaneously handle Housekeeping and online upgrade requests
3. Among 5 FLASH Banks, 1 FLASH Bank can be allocated to store the Boot program, and the remaining 4 FLASH Banks are divided into two mutually backed-up groups for CPU1 and CPU2 APP programs. As shown below:

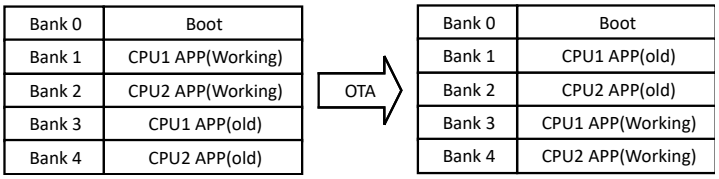


Figure 5-1. FLASH Bank Configuration Reference

Note

When a CMPSS module is assigned to CPU2 and the selected signal channel is not Input Signal, an operating condition may occur where CMPSS flipping cannot be triggered correctly even if the inductor current signal exceeds the reference value of the ramp generator, leading to abnormal duty cycle output. The reason for this anomaly is that the CMPSS input signal pin configuration can only take effect when configured in CPU1.

In dual-CPU co-working, if CPU2 is required to control the charging DC/DC, this paper proposes a synchronization method where the following code needs to be added during the initialization phase of the main function to trigger CMPSS correctly:

```
SysCtl_disablePeripheral(SYSCTL_PERIPH_CLK_TBCLKSYNC);
Board_init();
ASysCtl_selectCMPHPMux(ASYSCTL_CMPHPMUX_SELECT_9, 2U);//更改 CMPSS 的输入信号通道
ASysCtl_selectCMPHPMux(ASYSCTL_CMPHPMUX_SELECT_6, 1U);//更改 CMPSS 的输入信号通道
ASysCtl_selectCMPHPMux(ASYSCTL_CMPHPMUX_SELECT_5, 1U);//更改 CMPSS 的输入信号通道
SysCtl_enablePeripheral(SYSCTL_PERIPH_CLK_TBCLKSYNC);
```

6 Test Waveforms

Utilize the internal DAC module of F28P65 to output an upward periodic ramp, and connect this ramp to the positive input of CMPSS to verify the CBC waveform output by EPWM6:

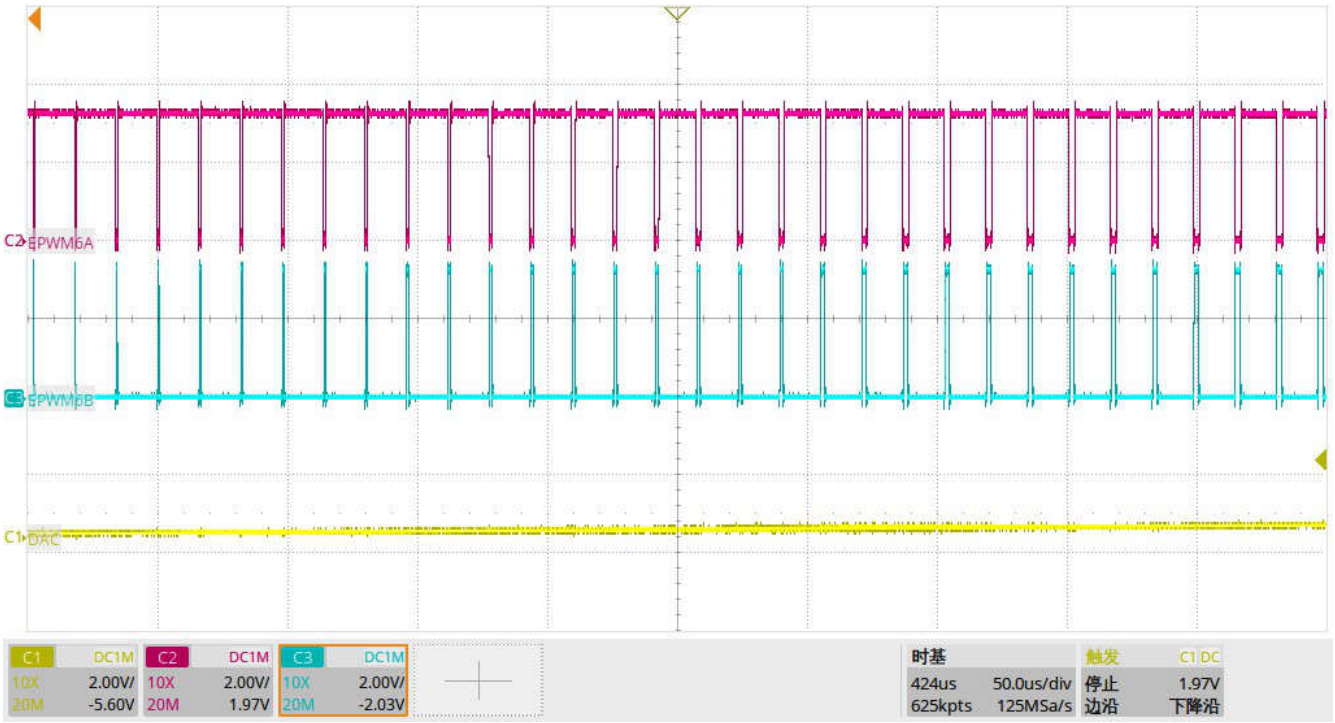


Figure 6-1. PCM CBC Duty Cycle Generation

As shown in Figure 6-1, the DAC determines the turn-on time of EPWM6B for soft start or cycle-by-cycle current protection. As shown in Figure 6-2, under both turn-on and turn-off conditions of EPWM B, there is always dead-band isolation between channels A and B. Furthermore, there is a fixed phase shift between EPWM6 and EPWM4:

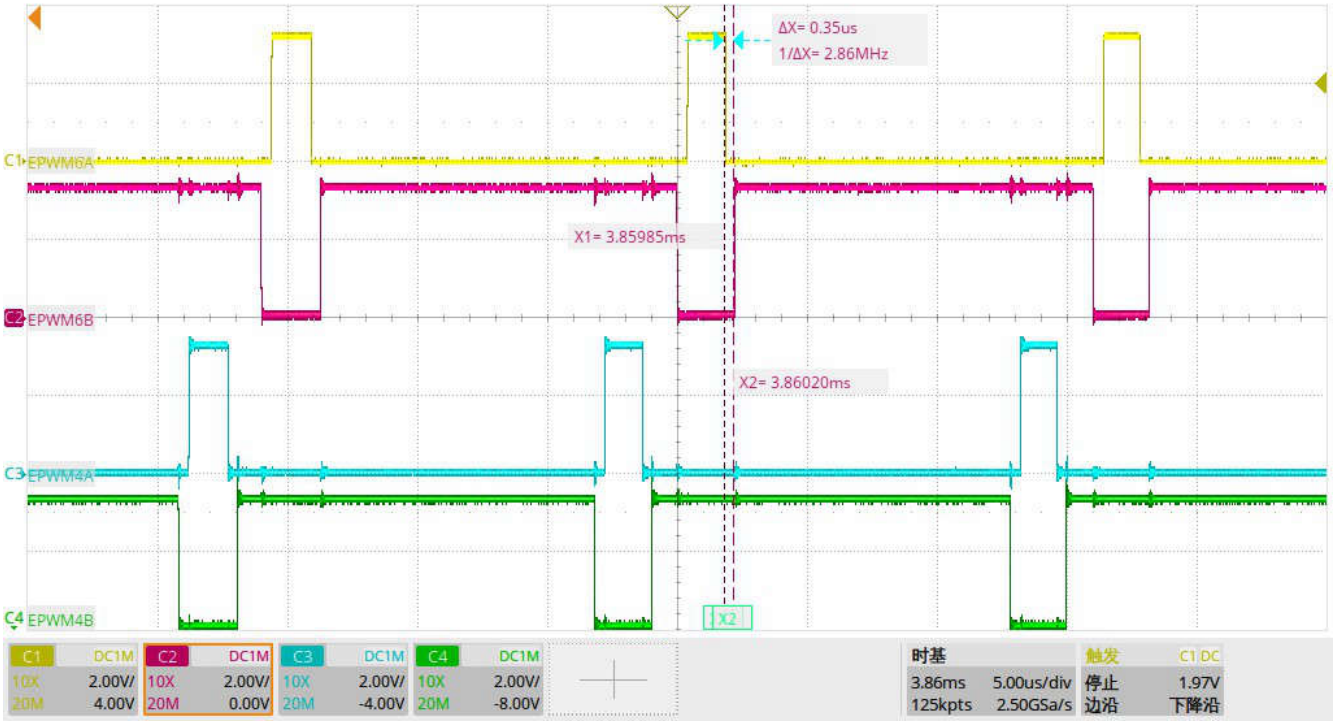


Figure 6-2. Dead-Band Waveforms of EPWM6A and EPWM6B

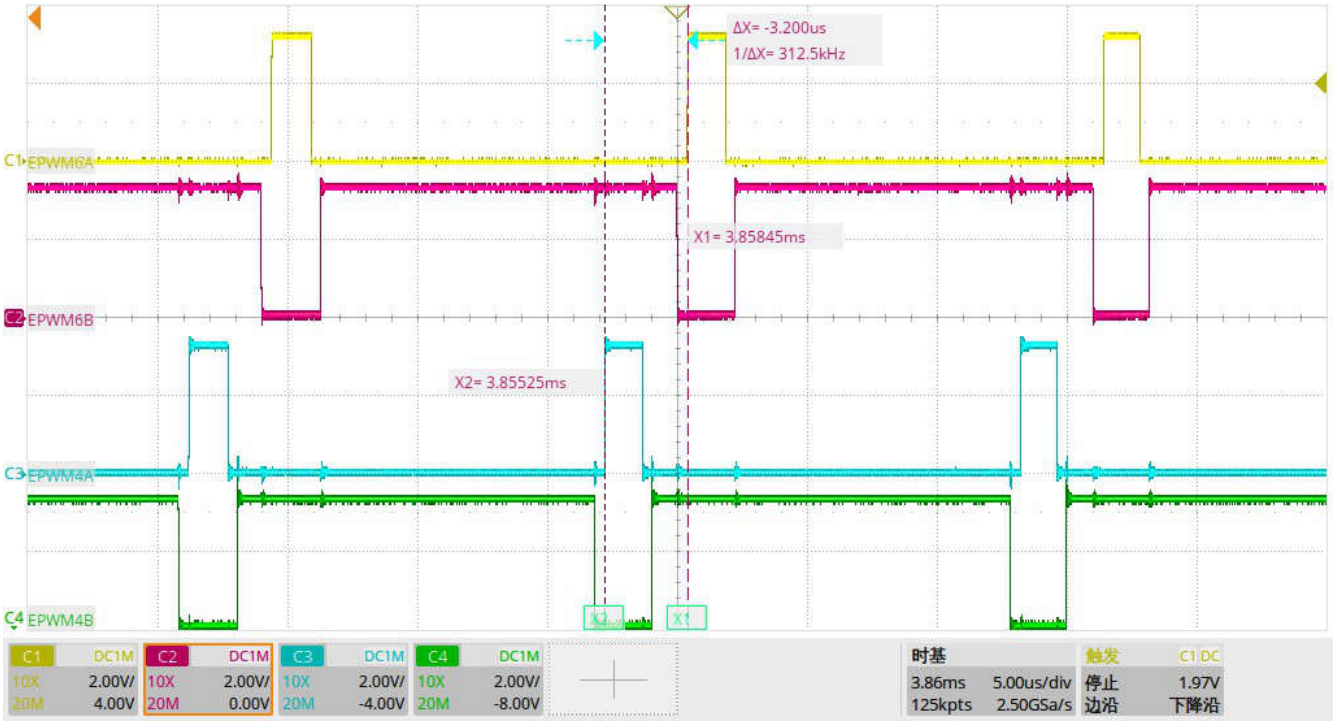


Figure 6-3. Phase Shift between EPWM6A and EPWM4A

When CBC is triggered, EPWM6 and EPWM4 each trigger an ADC SOC conversion. An interrupt service function is configured for each of these two SOCs, and an IO is toggled in each interrupt service function to

verify the ADC sampling moment as shown in the figure below. It can be seen that there is a delay compared to the turn-off moment of channel A, which is the ADC conversion time.

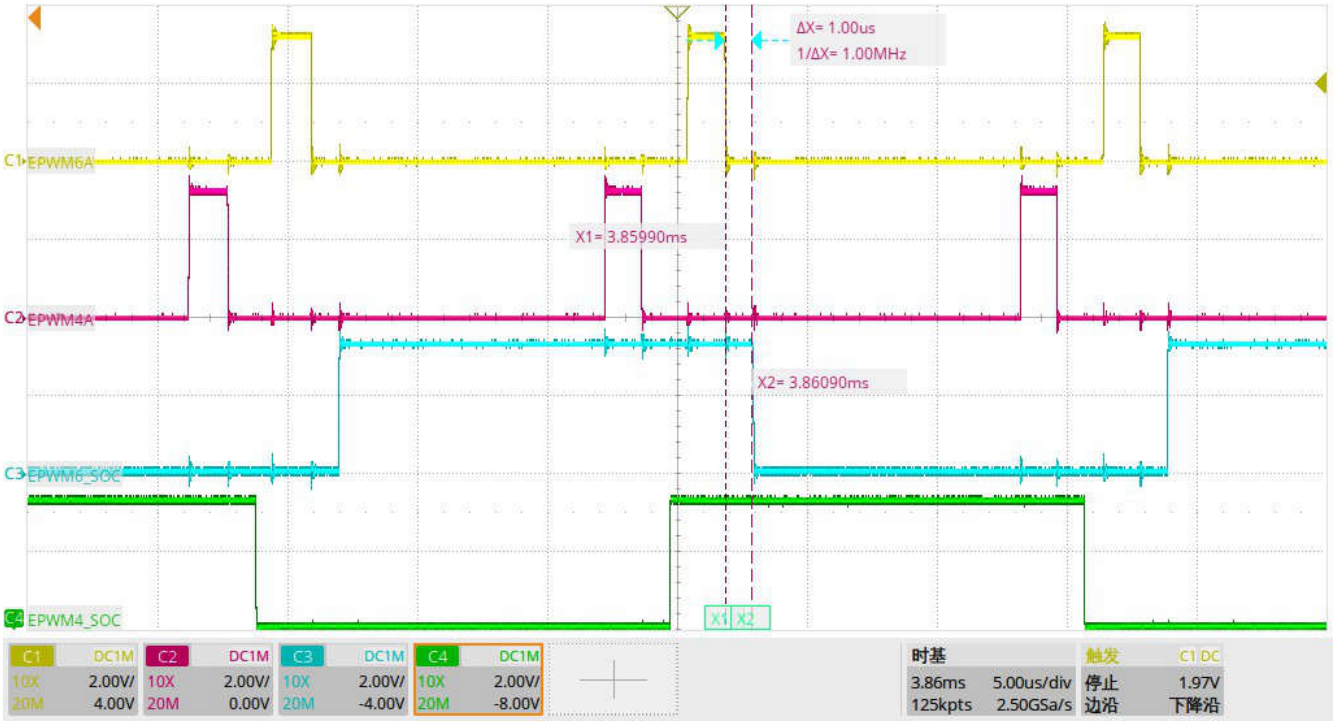


Figure 6-4. SOC Triggering of EPWM6 and EPWM4

Connect an IO to the positive input of CMPSS capturing fault conditions to simulate a fault occurrence, triggering the protection shutdown action of the EPWM6 module as shown below:

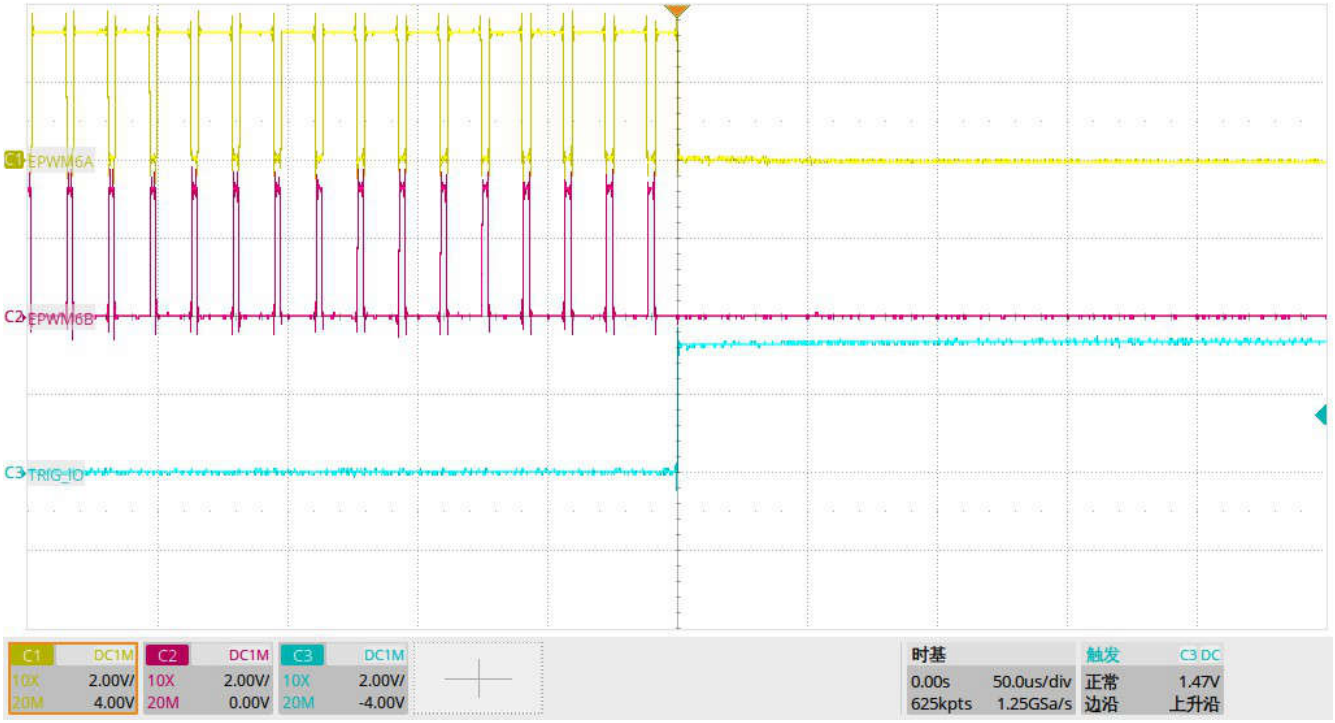


Figure 6-5. CMPSS Triggered Protection

7 References

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2. Implement three-phase interleaved LLC on C2000 Type-4 PWM
3. CRM/ZVS PFC Implementation Based on C2000 Type-4 PWM Module
4. Digital Control Implementation for Hybrid Hysteretic Control LLC Converter (Rev. A)
5. Step-by-Step Design Guide for Digital Peak Current Mode Control: A Single-Chip Solution

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