Application Note

TDA4 SoC-Driven CSI2-RX Acquisition of Raw ADC Signals From AWR2188 Radar MMIC

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ABSTRACT

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With the wider application and standardization of L2 and higher-level advanced driver assistance systems, high-performance imaging-grade 4D mmWave radar sensors and signal processing algorithms play an increasingly important role. Mainstream 4D forward mmWave radar technology is upgrading from the current 4T4R to the 8T8R, which offers longer range, higher detection speed, and a balance of ultra-high angular resolution and accuracy in both horizontal and vertical directions. However, it also raises challenges for data volume and bandwidth for the system's high-speed digital signal processing, algorithm computing performance, and software design complexity. TI has now released the AWR2188, an industry-leading, highly integrated, automotive-grade RF CMOS 76-to-81GHz mmWave RF transceiver. It allows the implementation of an 8T8R 4D imaging radar front end on a single chip. Its back end can be integrated with a high-performance automotive-grade SoC processor from TI's Jacinto TDA4 family, along with the software Processor RTOS SDK, to deploy lossless radar ADC raw data reception based on the built-in Cortex R5 MCU, achieve signal chain algorithm processing based on the integrated C7 DSP + MMA, and ultimately output dense point clouds with up to thousands of points per frame over high-speed Gigabit Ethernet ports.

This article focuses on the raw ADC data format and layout that the AWR2188 outputs over the CSI2-TX high-speed interface. TDA4VEN, a cost-effective entry-level SoC from TI's TDA4 processor family, is selected to demonstrate how to configure the CSI2-RX interface for correct capture of lossless ADC data. At the end of the article, the software driver source code is provided to help users more conveniently and quickly set up and debug this most critical link connecting the mmWave radar RF front end and high-performance signal processor SoC.

Table of Contents

List of Figures

1 Overview

TI's TDA4VEN SoC integrates an image capture flow control IP that complies with the MIPI® CSI-2 v1.3 standard and MIPI® D-PHY 1.2 physical layer standard. Within the SoC, the hardware is designed with four sets of Camera Serial Interface (CSI2) receivers (each with four lanes of D-PHY). Each data lane supports a transmission rate of up to 2.5Gbps, making the total physical bandwidth reach 10Gbps, which is fully sufficient. The CSI2-RX controller supports multiple Virtual Channels. The hardware is capable of distinguishing frame data from different inputs through distinct Virtual Channel IDs (VC-IDs). The controller is not only responsible for unpacking on the physical layer, but also directly moves and stores data into the SoC's external system memory (DDR) based on the data stream format through its integrated DMA component. The CSI2-RX controller is capable of identifying a wide range of data types, including RAW formats (RAW8, RAW10, RAW12, RAW14, and RAW16) and YUV formats (YUV422 and YUV420).

CSI2-TX on TI's AWR2188 single-chip 8T8R mmWave radar has to transmit massive raw ADC data (raw IF data) captured across eight receive channels externally in real time and without loss. The CSI2-TX controller and physical layer of the AWR2188 are compliant with the MIPI® CSI-2 v1.2 protocol standard and integrate a physical-layer high-speed waveform generator compliant with the MIPI D-PHY v1.1/v1.2 standard. The AWR2188 SR2.0 supports efficient transfer of all data across eight receive channels at a rate of up to 1.7Gbps/lane through only one CSI2-TX interface (equipped with four lanes of D-PHY). Since the output of radar ADC sampling is real or complex signals, which have a vastly different layout and format from the line and field data of ordinary video cameras, the CSI2-TX controller must disguise and package the signals at the hardware level into a standard MIPI Data Type image data format for streaming, such as RAW8/RAW12/RAW16.

2 AWR2188 + TDA4VEN System Design

2.1 Applications of AWR2188 Radar Sensor in Automotive Products

The AWR2188 has a built-in 8TX and 8RX RF transceiver and digital front end, and is equipped with a rich set of host interface peripherals, including SPI to receive the initialization firmware and real-time chirp profile parameter configuration from the back-end processor and CSI2-TX to transfer raw ADC data to the processor. Current mainstream edge radars, such as 4D mmWave forward radar, and back-end processors are typically integrated on the same PCB board. The CSI2-RX and CSI2-TX interfaces are not connected across boards over a long distance but have an intra-board connection through four lanes of MIPI high-speed differential signals. Satellite radars, however, are often integrated into the central domain controller for radar signal chain algorithm processing. Front-end radar sensors are not designed with the algorithm processing capability, thus transferring raw ADC data over the SerDes/TI FPD-Link single-ended coaxial cable.

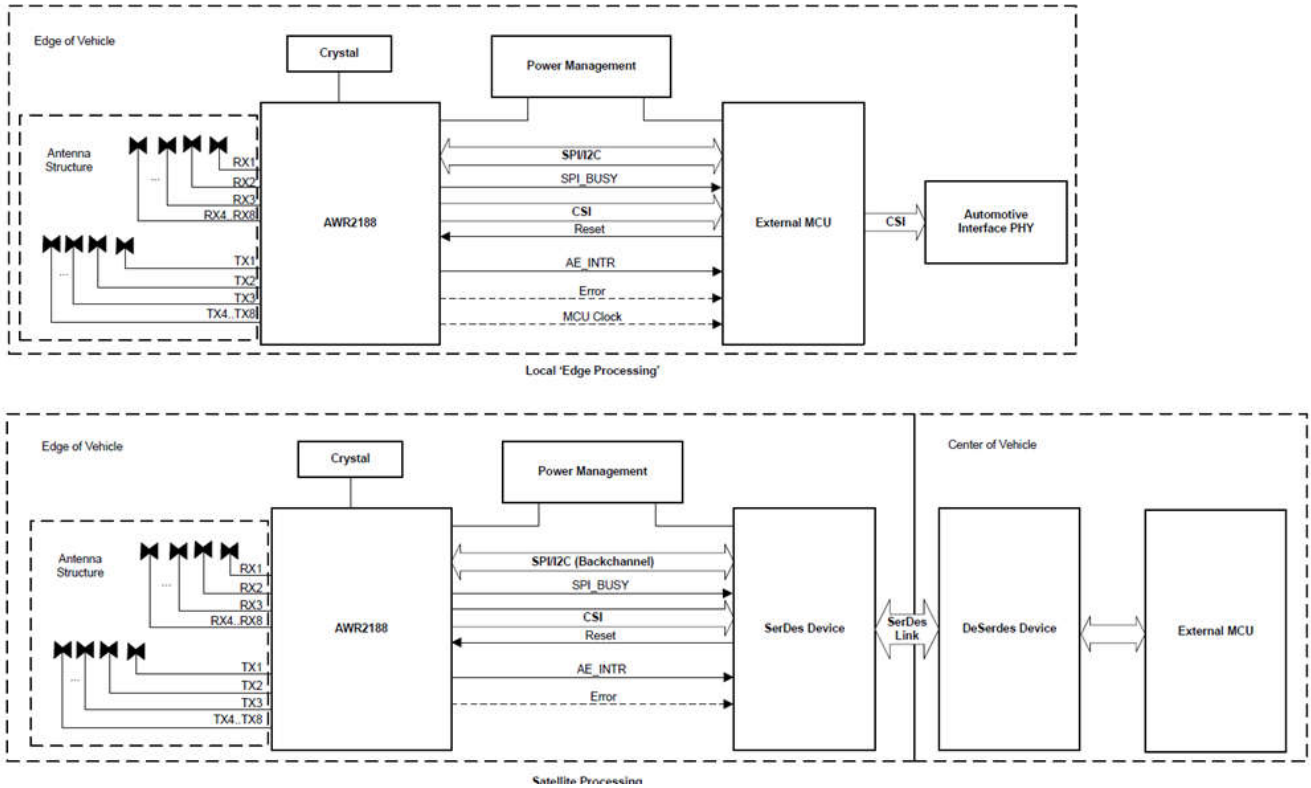

Figure 2-1. AWR2188 Edge and Satellite Processing System Block Diagram

2.2 TDA4VEN Internal Compute Resource Partitioning and Data Flow

The TDA4VEN SoC integrates three 800MHz ARM Cortex-R5 cores and two 1GHz high-performance 64+256-bit scalar-vector mixed full floating-point TI C7 DSP cores. Each DSP core is mounted with an additional 1GHz matrix multiply accelerator (MMA). As a result, a total of 80Gflops 32-bit floating-point computation and 4Tops/INT8 neural network acceleration, or range and Doppler FFT acceleration necessary for equivalent radar signal processing, are supported. One Wakeup R5 core is used for the system's SBL bootloader startup and device driver resource management, and one MCU R5 core is used for customer-specific MCU features such as AutoSar-based software protocols and tasks. The last one, the Main R5 core, is used to drive the CSI2-RX software driver on FreeRTOS, configure raw ADC data reception format, initialize and respond to TI's high-speed UDMA channels to move the received raw ADC data to the external LPDDR4 memory, and inform the C7 DSP core via the IPC for algorithm calculations. The C7 DSP core requires no frame copy. By obtaining the shared memory address from the IPC and configuring the additional UDMA channels, it moves data from the DDR to the on-chip L2 SRAM in batches for efficient operations and performs the subsequent data move-in and the move-out of the current result simultaneously in the background, achieving significant optimization and resolving the memory latency issue that particularly affects the overall system performance. Finally, the DSP core puts the

4D point-cloud data generated by the radar signal chain algorithm into the shared memory and informs the R5 core to transmit the data externally over the Ethernet interface that it drives.

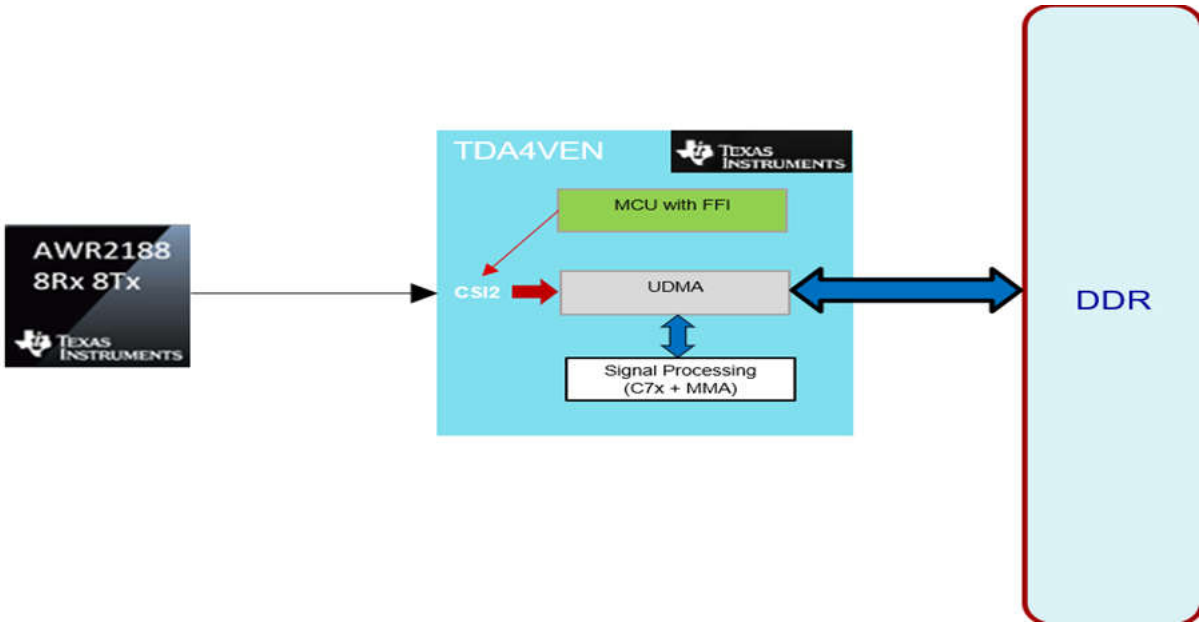

Figure 2-2. TDA4VEN Software Task Partitioning and Data Flow

2.3 Data Format and Layout and Raw ADC Data Memory Consumption

The AWR2188 SR2.0 supports transmission over a single CSI2-TX interface, with all its RX0-RX7 channels configured to output to Port 0, the data type set to the RAW8 format, and the lane speed for transmission set to 850MHz. To improve the speed resolution, the transmission profile of each RX antenna on the AWR2188 is set to 1024 Chirps. To improve the range resolution, each Chirp is configured to contain 1024 16-bit real-valued ADC sample data points (each ADC sample has two bytes). In this way, the total data amount per frame is 2 Bytes * 1024 Samples * 1024 chirps * 8 Rx = 16MB.

The CSI2-RX interface on the TDA4VEN receiver only needs to enable one receiver instance 0, receive data in the RAW8 format, and enable only Virtual Channel 0. All 1024 16-bit samples from the eight RX channels (arrange all samples first and all RX channels second) are accommodated in a large width, and the number of Chirps corresponds to the Height dimension.

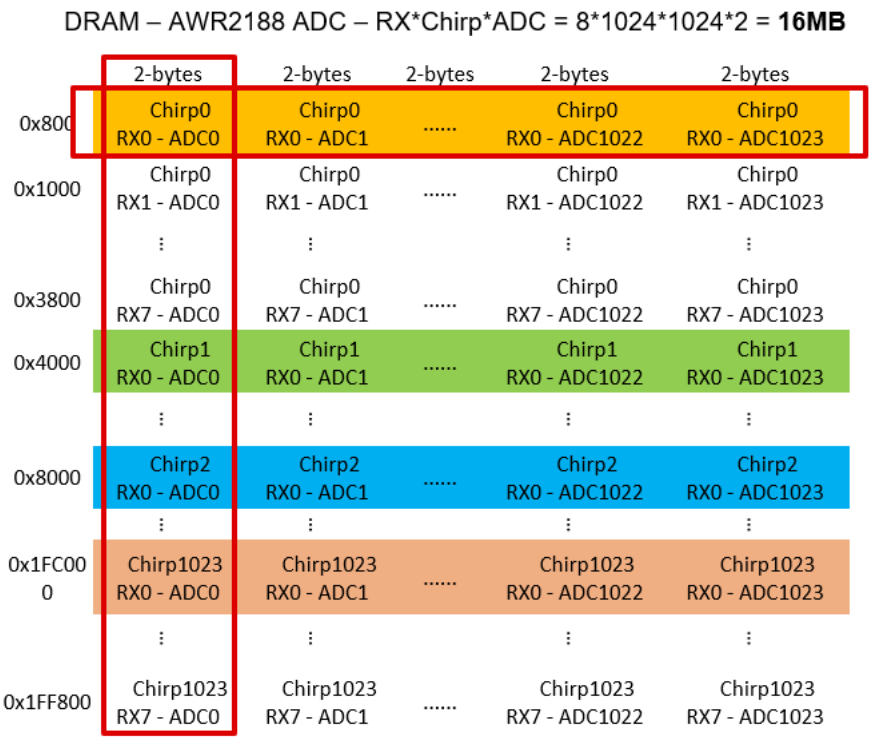

Figure 2-3. AWR2188 SR2.0 ADC Data Transmitted and Stored in Non-interleaved Mode

3 CSI2-RX Capture Software Module Driver Configuration in Processor RTOS SDK

3.1 The CSI2-RX software parameters of the TDA4VEN must match the transmission format of the AWR2188 SR2.0

```
gCsiCfgHandle[i]->chFrmCnt = 0U;
gCsiCfgHandle[i]->createPrms.chCfg.chId = 0U;
gCsiCfgHandle[i]->createPrms.chCfg.chType = 0U;
gCsiCfgHandle[i]->createPrms.chCfg.vcNum = 0U;
gCsiCfgHandle[i]->createPrms.chCfg.inCsiDataType = FVID2_CSI2_DF_RAW8;
gCsiCfgHandle[i]->createPrms.chCfg.outFmt.width = 1024(adc)*2(Bytes)*8(RX);
gCsiCfgHandle[i]->createPrms.chCfg.outFmt.height = 1024(Chirp);
gCsiCfgHandle[i]->createPrms.chCfg.outFmt.pitch[0U] = 1024(adc)*2(Bytes)*8(RX);
gCsiCfgHandle[i]->createPrms.chCfg.outFmt.dataFormat = FVID2_DF_RAW08;
gCsiCfgHandle[i]->createPrms.chCfg.outFmt.ccsFormat = FVID2_CCSF_BITS8_PACKED;
gCsiCfgHandle[i]->createPrms.instCfg.enableCsiv2p0Support = (uint32_t)TRUE;
gCsiCfgHandle[i]->createPrms.instCfg.numDataLanes = 4U;
gCsiCfgHandle[i]->createPrms.instCfg.enableErrbypass = (uint32_t)FALSE;
gCsiCfgHandle[i]->createPrms.instCfg.enableStrm[CSIRX_CAPT_STREAM_ID] = 1U;
dphyCfg->leftLaneBandSpeed  = CSIRX_LANE_BAND_SPEED_1500_TO_1750_MBPS;
dphyCfg->rightLaneBandSpeed = CSIRX_LANE_BAND_SPEED_1500_TO_1750_MBPS;
chType:表示 CSIRX 内置的 DMA 把数据搬运到 DDR 中;
vcNum:表示虚拟通道号;
inCsiDataType:表示传输格式;
Width:表示传输的宽度;
Height:表示传输的高度;
Pitch:表示传输完一行数据后开始下一行需要跳过多少数据;
DataFormat:表示输出的格式;
ccsFormat:表示输出的数据在内存里面的排列;
numDataLanes:表示按照硬件连接使用多少条 data lane;
enableErrbypass:表示是否要使能错误检查;
leftLaneBandSpeed/rightLaneBandSpeed:表示按照发送端的速度 bps;
```

CAUTION

MIPI-CSI2 is a dual-edge sampled differential signal, and the data transfer rate on the data lane is twice the frequency on the clock lane. Therefore, the frequency on AWR2188 SR2.0 CSI2-TX Port0 is configured to 850MHz, which corresponds to a data transfer rate of 1700Mbps.

CAUTION

It is important to note that the CSI2-RX controller of the TDA4VEN must be ready before the peer transmitter starts transmitting data. Timing must be strictly followed, or the CSI2-RX interface may not receive signals reliably.

3.2 How to troubleshoot the TDA4VEN SoC when CSI2-RX does not receive data correctly

Step A: The function CsirxDrv_udmaCQEventCb under SDK source\drivers\csirx\v1\src\csirx_drvUdma.c is the DMA interrupt callback function when the CSIRX receives data. You can first set a breakpoint through CCS to check in the function below whether data has been received.

```
429:
430: void CsirxDrv_udmaCQEventCb(Udma_EventHandle eventHandle,
431:                                uint32_t eventType,
432:                                void *appData)
433: {
434:     int32_t retVal = UDMA_SOK, tempVal = UDMA_SOK;
435:     CsirxDrv_ChObj *chObj;
436:     CsirxDrv_QueObj *qObj;
437:     CsirxDrv_BufManObj *bmObj;
438:     uint64_t pDesc = 0;
439:     uint32_t *pTrResp;
440:     uint32_t pTrRespVal, pTrRespStsTypeVal;
441:     uint32_t curQCnt, appCb = 0U, cookie, chIdx;
442:     uint64_t timeStamp;
443:     CSL_UdmapTR1 *pTr;
444:
445:     if(eventHandle == NULL)
446:     {
447:         /*To remove unused variable warning*/
448:     }
449:
450:     chObj = (CsirxDrv_ChObj *) appData;
451:     GT_assert(CsirxTrace, (chObj ! = NULL));
452:
453:     / * Take out completed TRPD from UDMA CQ Ring */
454:     if(eventType == UDMA_EVENT_TYPE_DMA_COMPLETION)
455:     {
456:         / * Disable HW interrupts here */
457:         cookie = HwiP_disable();
458:         bmObj = &chObj- >bufManObj;
459:         / * Response received in completion queue, empty up full CQ Ring */
460:         while (retVal == UDMA_SOK)
```

Step B: When the software interrupt is not called (no data is received), check whether the hardware CSI2-RX IP has received protocol packets from the MIPI or errors reported by the IP.

14.8.6.1.2.36.1 CSIRX_INFO_IRQS Register (Offset = 20h) [reset = 0h]

Information type Interrupt status (non-error conditions)

Return to Summary Table

Table 14-23120. Instance Table

Instance Name	Physical Address
CSI_RX_IF0	3010 1020h

Figure 14-11440. CSIRX_INFO_IRQS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED							
NONE							
0h							
15	14	13	12	11	10	9	8
RESERVED	STREAM3_ABORT_IRQ	STREAM3_STOP_IRQ	STREAM2_ABORT_IRQ	STREAM2_STOP_IRQ	STREAM1_ABORT_IRQ	STREAM1_STOP_IRQ	STREAM0_ABORT_IRQ
NONE	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
STREAM0_STOP_IRQ	SP_GENERIC_RCVD_IRQ	DESKEW_ENTRY_IRQ	ECC_SPARES_NONZERO_IRQ	WAKEUP_IRQ	SLEEP_IRQ	LP_RCVD_IRQ	SP_RCVD_IRQ
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h	0h	0h	0h	0h	0h	0h	0h

Table 14-23121. CSIRX_INFO_IRQS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DESKEW_ENTRY_IRQ	R/W1TC	0h	Either clock or any datalane has entered deskew
4	ECC_SPARES_NONZERO_IRQ	R/W1TC	0h	Bits 7:6 of the ECC byte are non-zero. Indicates non compliance with the MIPI specification although the core will continue to operate as normal.
3	WAKEUP_IRQ	R/W1TC	0h	Wake-up interrupt.
2	SLEEP_IRQ	R/W1TC	0h	Sleep interrupt.
1	LP_RCVD_IRQ	R/W1TC	0h	Long Packet received by the protocol module
0	SP_RCVD_IRQ	R/W1TC	0h	Short Packet received by the protocol module

Note: Bit0/1: Indicates that the MIPI IP protocol layer has received protocol-compliant data.

Note: Bit5: When the rate on CSIRX's data lane is greater than 1.5Gbps, the TDA4VEN requires the transmitter to do DESKEW before transmitting data. If this bit is not set, the transmission configuration of the transmitter AWR2188's CSI2-TX should be checked for inclusion of DESKEW.

Step C: Check the status register for any error. For common errors with ECC and CRC generated during the signal transfer process, check whether the configuration of the transmitter's CSI2-TX interface follows the standard timing. For FIFO overflow errors, check whether the MIPI rates on both the transmitter and receiver match each other. For data ID mismatch errors, check whether the formats configured for the transmitter and receiver are consistent. TRUNCATED_PACKET indicates that the size settings for both the transmitter and receiver are not consistent. Be sure that the length and width settings are consistent.

14.8.6.1.2.38.1 CSIRX_ERROR_IRQS Register (Offset = 28h) [reset = 0h]

Datapath error interrupt status. Provides information about data path errors. The host processor can read the interrupt status register to identify the root cause of the event, typically after that the csi2rx_err_irq interrupt line is raised

Return to Summary Table

Table 14-23124. Instance Table

Instance Name	Physical Address
CSI_RX_IF0	3010 1028h

Figure 14-11442. CSIRX_ERROR_IRQS Name Register

31	30	29	28	27	26	25	24
RESERVED							
NONE							
0h							
23	22	21	20	19	18	17	16
RESERVED				STREAM3_FIFO_OVERFLOW_IRQ	STREAM2_FIFO_OVERFLOW_IRQ	STREAM1_FIFO_OVERFLOW_IRQ	STREAM0_FIFO_OVERFLOW_IRQ
NONE				R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h				0h	0h	0h	0h
15	14	13	12	11	10	9	8
RESERVED			FRONT_TRUNC_HDR_IRQ	PROT_TRUNCATED_PACKET_IRQ	FRONT_LP_NO_PAYLOAD_IRQ	SP_INVALID_RCVD_IRQ	INVALID_ACCESS_IRQ
NONE			R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0h			0h	0h	0h	0h	0h
7	6	5	4	3	2	1	0
DATA_ID_IRQ	HEADER_CORRECTED_ECC_IRQ	HEADER_ECC_IRQ	PAYLOAD_CRC_IRQ	RESERVED			FRONT_FIFO_OVERFLOW_IRQ
R/W1TC	R/W1TC	R/W1TC	R/W1TC	NONE			R/W1TC
0h	0h	0h	0h	0h			0h

Step D: Check if the DATA ID and VC channel number of the DMA settings for CSIRX of the TDA4VEN match those of the transmitter.

14.8.6.1.2.109.1 CSI_RX_IF_CNTX_CNTL_DMACNTX_J Register (Offset = 0h) [reset = C000000h]

DMA Channel Context. Configuration for each of 32 possible channel contexts. Illegal to program 2 chanCntx with same extraction values.

Return to Summary Table

Table 14-23266. Instance Table

Instance Name	Physical Address
CSI_RX_IF0	3010 2000h + formula

Figure 14-11513. CSI_RX_IF_CNTX_CNTL_DMACNTX_J Name Register

31	30	29	28	27	26	25	24
EN_CFG	RESERVED	RSV0	RSV1	YUV422_MODE_CFG		RSV2	DUAL_PCK_CFG
R/W	NONE	R/W	R/W	R/W		R/W	R/W
0h	0h	0h	0h	3h		0h	0h
23	22	21	20	19	18	17	16
RESERVED		SIZE_CFG		RESERVED	PCK12_CFG	RESERVED	
NONE		R/W		NONE	R/W	NONE	
0h		0h		0h	0h	0h	
15	14	13	12	11	10	9	8
RESERVED						VIRTCH_CFG	
NONE						R/W	
0h						0h	
7	6	5	4	3	2	1	0
VIRTCH_CFG		DATTYP_CFG					
R/W		R/W					
0h		0h					

9:6	VIRTCH_CFG	R/W	0h	CSI virtual channel index. Supplied by MIPI CSI protocol to DPHY. For CSIver1.3 program 2MSb==0 Reset Source: main_mod_g_srst_n
5:0	DATTYP_CFG	R/W	0h	CSI data type index. Supplied by MIPI CSI protocol to DPHY Reset Source: main_mod_g_srst_n

Step E: The left and right rates must be the same. For example, if the parameter is configured to #define CSIRX_LANE_BAND_SPEED_1500_TO_1750_MBPS ((uint32_t) 0x13U) in the software SDK, then the readback value of this register should be 0x273 (0010 0111 0011).

14.8.6.2.2.5.1 K3_DPHY_RX_PCS_TX_DIG_TBIT0 Register (Offset = B00h) [reset = 0h]

PHY_BAND_CONTROL

Return to Summary Table

Table 14-23282. Instance Table

Instance Name	Physical Address
DPHY_RX0	3011 0B00h

Figure 14-11520. K3_DPHY_RX_PCS_TX_DIG_TBIT0 Name Register

31	30	29	28	27	26	25	24
UNUSED							
R							
0h							
23	22	21	20	19	18	17	16
UNUSED							
R							
0h							
15	14	13	12	11	10	9	8
UNUSED						BAND_CTL_REG_R	
R						R/W	
0h						0h	
7	6	5	4	3	2	1	0
BAND_CTL_REG_R				BAND_CTL_REG_L			
R/W				R/W			
0h				0h			

Table 14-23283. K3_DPHY_RX_PCS_TX_DIG_TBIT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31:10	UNUSED	R	0h	RESERVED
9:5	BAND_CTL_REG_R	R/W	0h	Data Rate [80_100] MHz
4:0	BAND_CTL_REG_L	R/W	0h	Data Rate [80_100] MHz

4 Test Script Tool

In a real-world project, more registers must be checked to determine whether the configuration and status of the TDA4VEN SoC are correct. A GEL script file is attached, which contains all the registers for the CSI2-RX and DHPY of the TDA4VEN. It is possible to check for inconsistent configuration and status by dumping out the complete register list directly after the CCS connection and comparing it with the registers normally receiving data on the TI EVM.

5 References

1. J722S TDA4VEN TDA4AEN AM67 Processor Silicon Revision 1.0 Technical Reference Manual (Rev. C)
2. AWR2188 Single Chip 8x8 Cascadable 76-to-81GHz Transceiver in LOP package datasheet (Rev. A)
3. Software Development Kit for TDA4VEN and TDA4AEN Jacinto processors-Download/PROCESSOR-SDK-RTOS-J722S

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