System Power Savings Using Dynamic Voltage Scaling

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What Is Dynamic Voltage Scaling?

- Dynamic voltage scaling, or DVS, is a method of reducing the average power consumption in embedded systems.

- This is accomplished by reducing the switching losses of the system by selectively reducing the frequency and voltage of the system.

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Where Is DVS Used?

- DVS is typically used in battery-operated devices where power savings and battery run times are paramount.

- DVS is also used in large systems with multiple processors/DSPs where power savings is required for thermal reasons.

- DVS is implemented extensively in:
  - Cell phones
  - PDAs
  - MP3 players
  - Microcontroller-based battery-operated devices

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Underlying Concepts for Microprocessor/Controller/DSP Systems

- Today's embedded systems use high clock frequencies to boost processing power and system performance.

- The power dissipated by an embedded system is (typically) dominated by switching losses.

- The losses from switching are due to the capacitance of what is being switched. Examples of the capacitance being switched include trace impedance, load capacitance and the gates of MOSFETs used to implement logic in the processor.

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Power Dissipation in a Capacitor

$$Power = \frac{1}{2}CV^2F$$
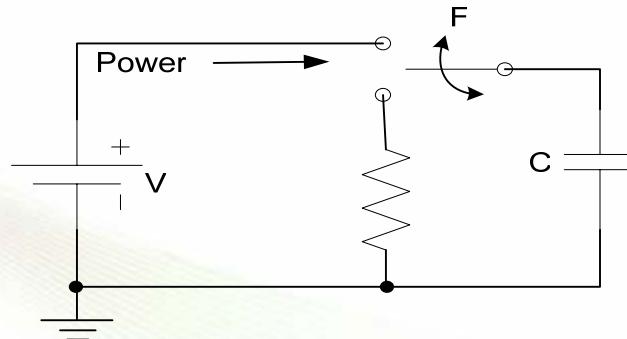
- V is the voltage the capacitor is charged to, F is the frequency that the voltage is switched across the capacitor.
- Power goes up by the square of the voltage.
- Power goes up linearly with switching frequency.

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Discreet Logic Example
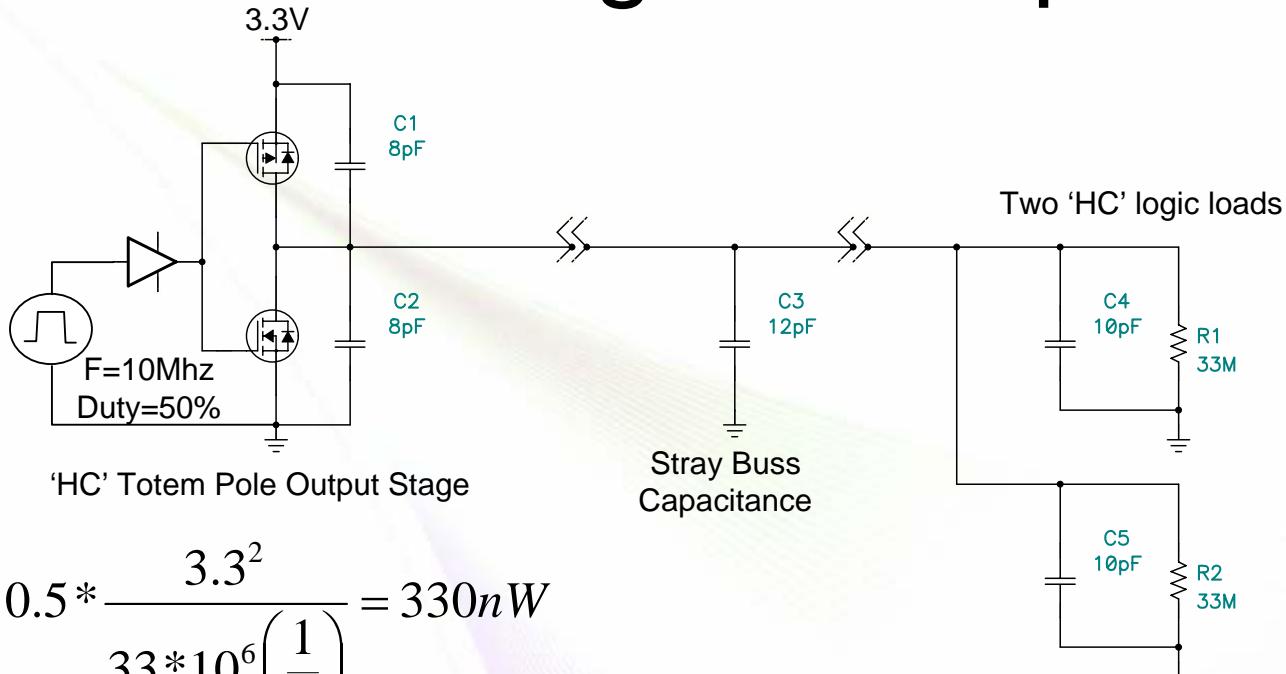
$$P_r = D * \frac{V^2}{R} = 0.5 * \frac{3.3^2}{33 * 10^6 \left(\frac{1}{2}\right)} = 330nW$$

$$P_{sw} = \frac{1}{2}CV^2F = \frac{1}{2} * (8pF + 8pF + 12pF + 10pF + 10pF) * 3.3^2 * 10^7 = 2.613mW$$

Power loss due to switching capacitors is 7,900 times higher than powering the load resistance!

Reducing Voltage and Frequency Adds Up to Power Savings

- Can reduce the switching power by a factor of **2** by reducing the switching frequency to one-half.

- Can reduce the switching power by a factor of **4** by reducing the voltage by one-half.

- Can reduce the switching power by a factor of **8** by reducing the voltage by a factor of two and the frequency by one-half.

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A DSP Example Using DVS

- Look at the TMS320VC5509A, a more complex example. This is a dual voltage rail DSP IC.

- The I/O voltage is 3.3V.

- The core voltage is between 1.2V and 1.6V.

- The maximum processor clock that can be supported is related to the core voltage.

- As in previous slides, the current consumption will go up as the core voltage goes up due to switching losses.

Maximum Clock Speed (Mhz) vs **Core Voltage (V)**

Core Voltage (V)	Maximum Clock Speed (Mhz)
1.2	108
1.35	144
1.6	200

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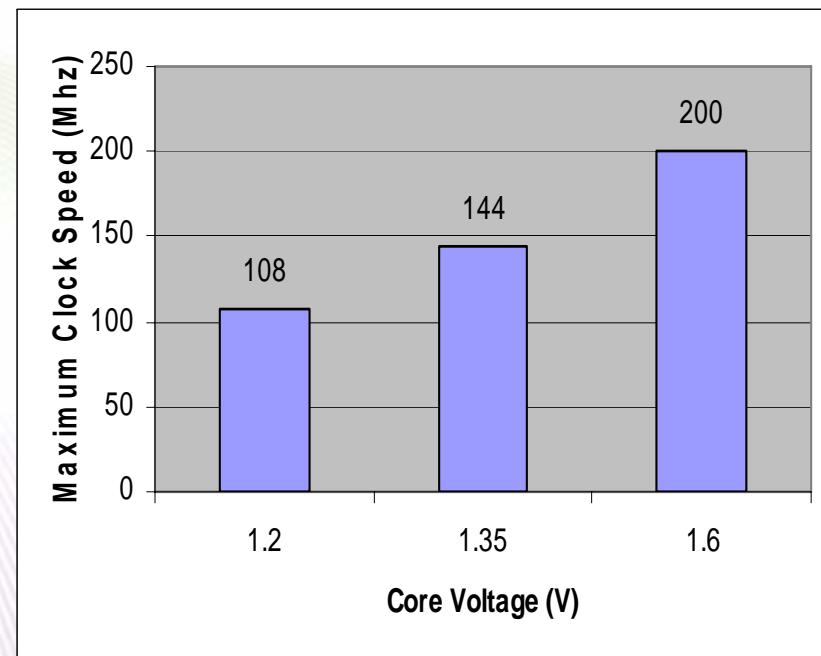
Digital Signal Processor Example
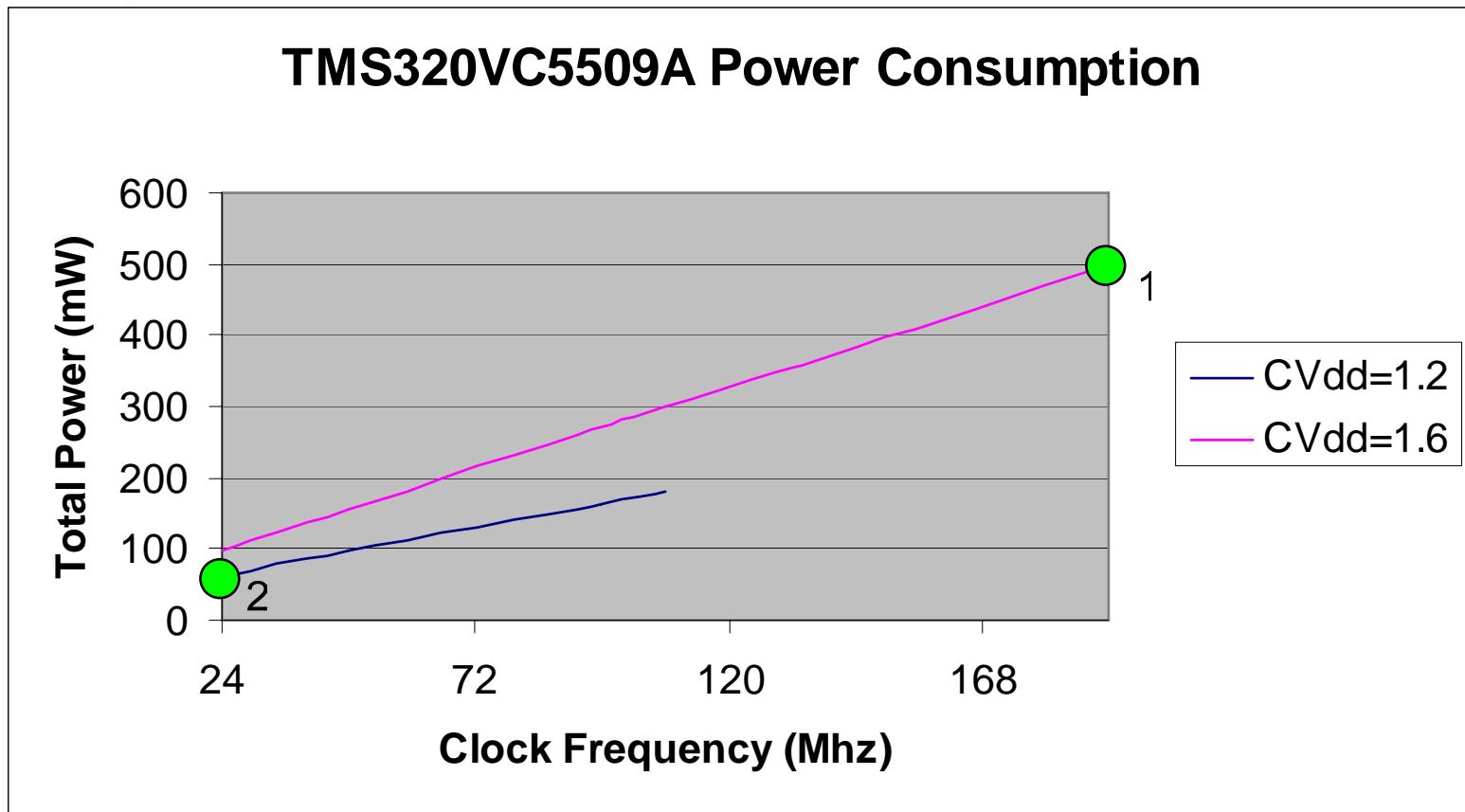
Point 1, Vcore=1.6, F=192Mhz, Power=500mW

Point 2, Vcore=1.2, F=24Mhz, Power=50mW

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Static Losses: Sidebar

- The TMS320VC5509A has very low static losses. What effect would higher static losses have?

- Static losses do not change with the frequency of operation.

- Excluding any loads, static losses are mostly due to leakage currents in transistors, which are dependent on the geometry of the silicon used to fabricate the transistors.

- The amount of leakage current is mostly linear with the voltage applied (Vcc). Looks like a resistor.

Lower Voltage Is Not Always the Lowest Power Operating Point

- Need to take into account static losses to find lowest operating power point.

- Need to look at how long the required software process will take to execute (number of clock cycles).

- At lower clock frequencies there will be lower dynamic losses but the amount of time to perform the operation is longer and static losses are incurred the entire time.

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Static and Dynamic Power Loss
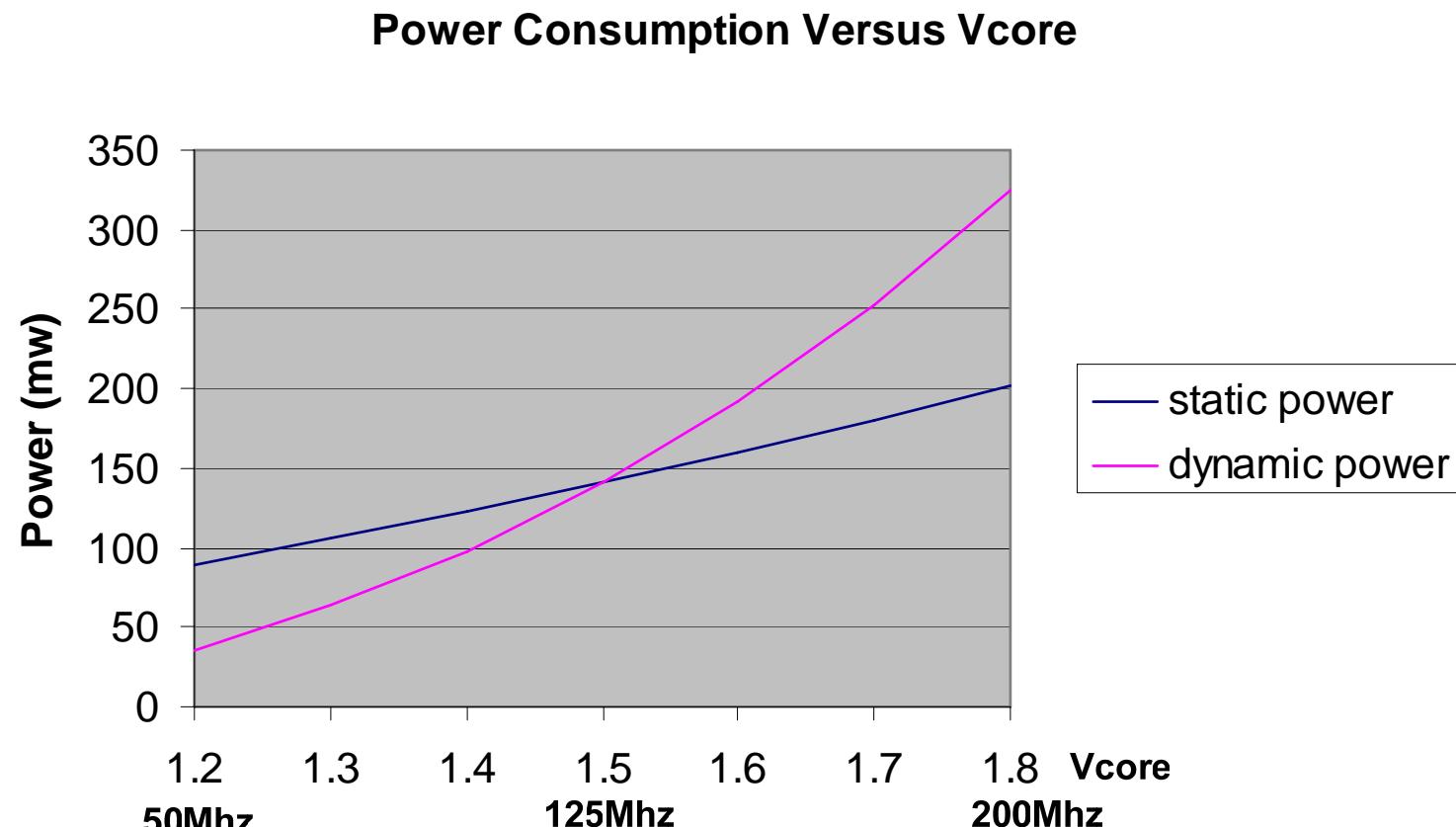
Power to Perform a Fixed-Length Process

Power Time Product to Perform 1 Million Clock Cycle Process
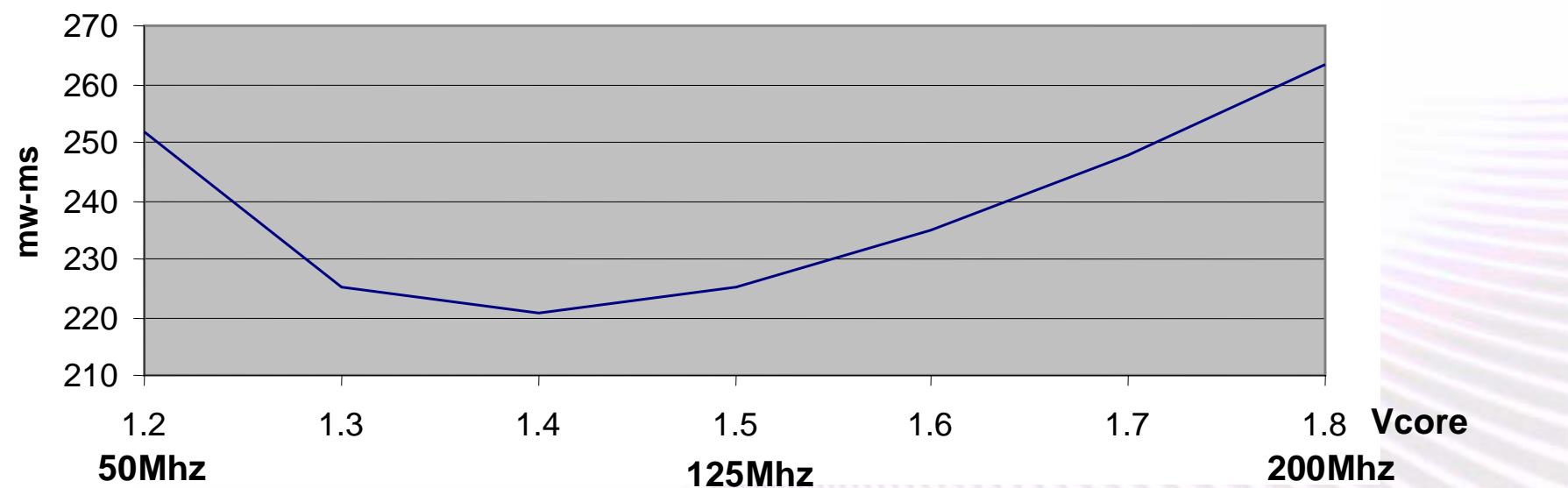
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Back to DVS: Process

- The DSP operating system predicts the immediate processing needs.

- DSP adjusts its clock frequency to match the needed processing power. This will **linearly** reduce the switching power.

- If the power supply powering the DSP supports DVS, then the DSP can adjust the voltage to what is needed to maintain the clock frequency. This will **exponentially** reduce the switching power.

Impact of DVS

Power Consumption vs Time – **NO DVS**

Pavg=Pmax=500mW

500mW —

50mW —

time ⟶

Power Consumption vs Time – **WITH DVS**

500mW —

Pavg=168mW

50mW —

time ⟶
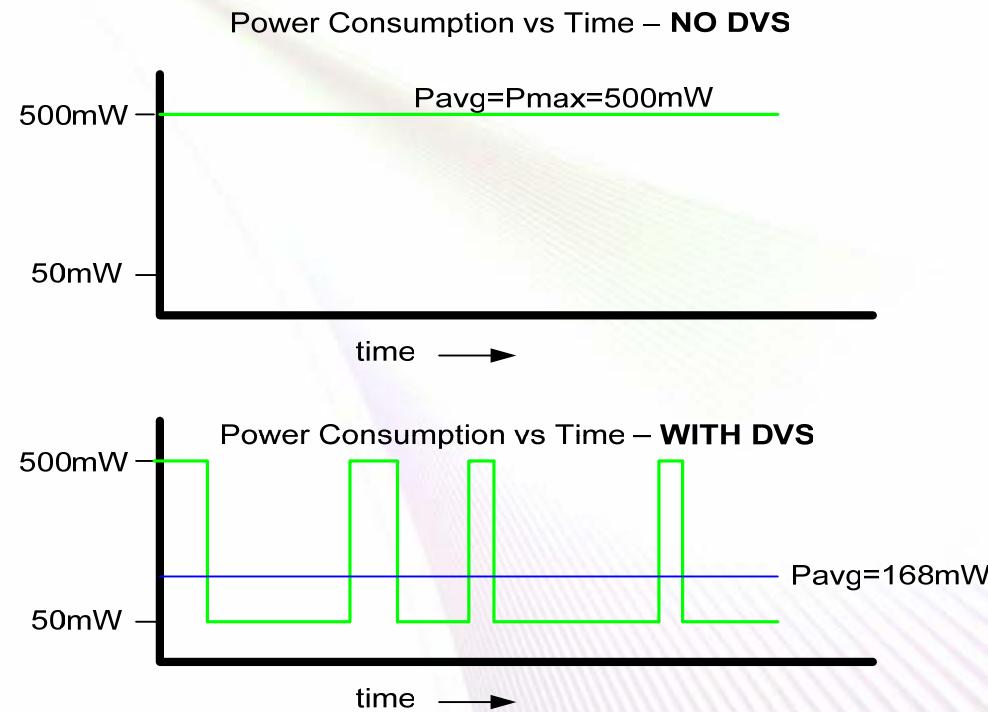
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DVS Power Supply Requirements

- Most DVS systems have dual voltage rails (core voltage and I/O voltage). A dual-channel power supply reduces parts count and cost, and it simplifies the design.
- One or both voltage outputs needs to be adjustable "on the fly" so that the supply voltage can dynamically track the needs of the processor.
- The output voltage of the power supply needs to change based on a digital input or some other communications channel.

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TPS624xx

- Some ICs that are designed to support DVS of dual-core processors, FPGAs, and digital signal processors are the TPS62400, TPS62401 and TPS62420 from TI.

- They are dual output step-down DC/DC converters.

- Output currents are 400mA/600mA or 600mA/1000mA.

- Input voltage range is 2.5 - 6.0 VDC.

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Features

- Software or pin-programmable output voltage selection to support dynamic voltage scaling applications. The output voltage can be changed "on-the-fly."

- All versions support a one-wire serial communications channel (Easyscale) to change the output voltages of either output.

- TPS62401 has digital input to select between two different output voltages for VOUT1.

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TPS62400 'Adjustable' Output

Output voltage at power-up is determined by a feedback resistor network. Output can then be changed using Easyscale interface.

$$initial\_Vout1 = 0.6\left(1 + \frac{R1}{R2}\right)$$

$$initial\_Vout2 = 0.6\left(1 + \frac{R3}{R4}\right)$$

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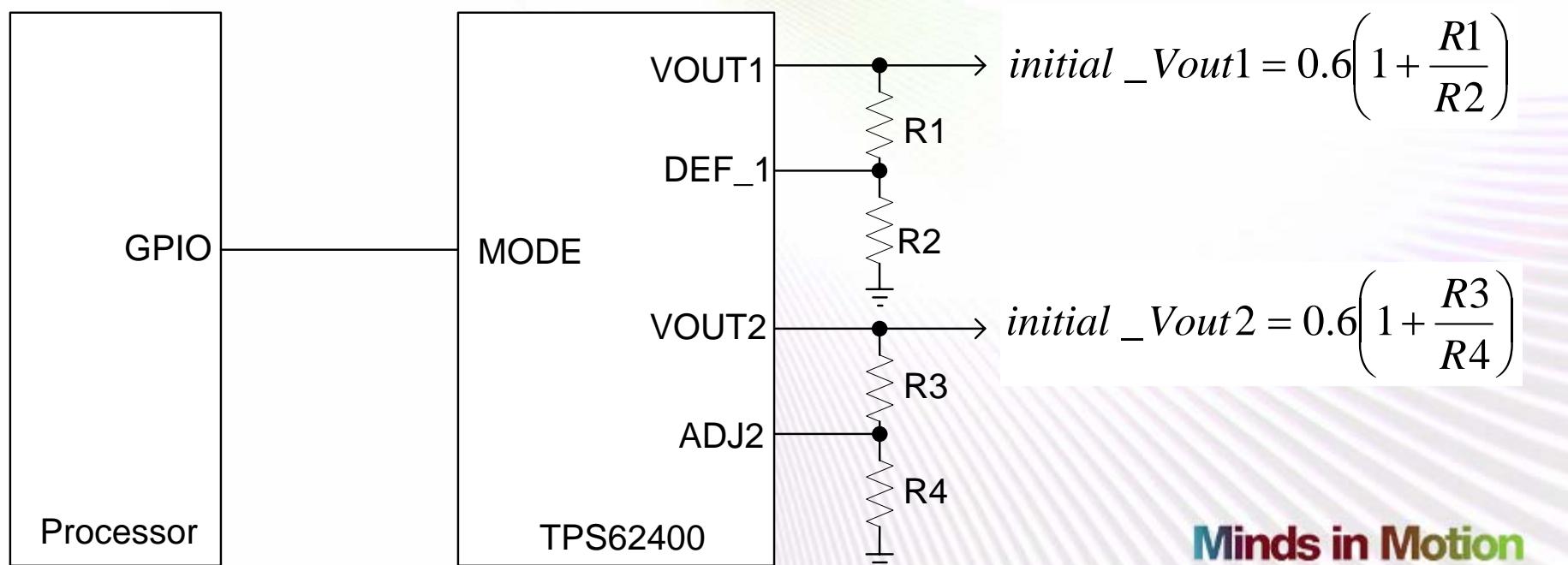
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TPS624x0 Output Voltage Selection

TPS624x0

CONVERTER #1

CONVERTER #2

ADJ2=Resistor Network

ADJ2=VOUT

Voltage at Power-up

$$Vout = 0.6\left(1 + \frac{R_1}{R_2}\right)$$

$$Vout = 0.6\left(1 + \frac{R_1}{R_2}\right)$$

Vout=0.6

Software Adjustable Output Range

Vfbk, 0.825-1.575

Any value other than 00000b in REG_2 will make Vout=Vin

0.6, 0.85-3.3
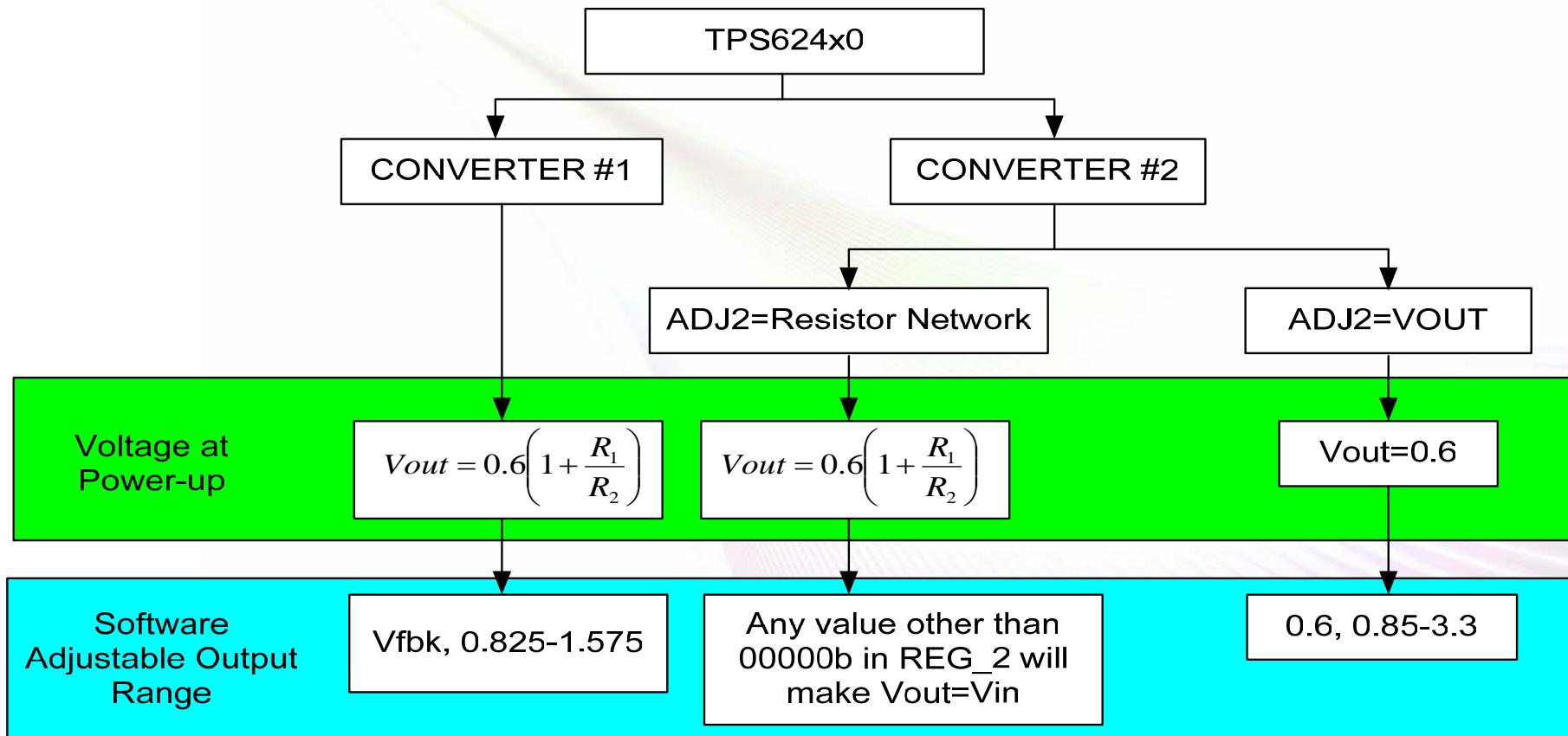
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TPS62401 'Fixed' Output

DEF_1 pin acts as digital input to switch between two factory-preset output voltages. After power-up, the voltages can be altered using Easyscale.

| Processor		TPS62401		
GPIO		DEF_1	VOUT1	VOUT1 = **1.575V** When **DEF_1 = low** VOUT1 = **1.100V** When **DEF_1 = high**
			FB	
GPIO		MODE	VOUT2	Vout2 = **1.800V**
			ADJ2	
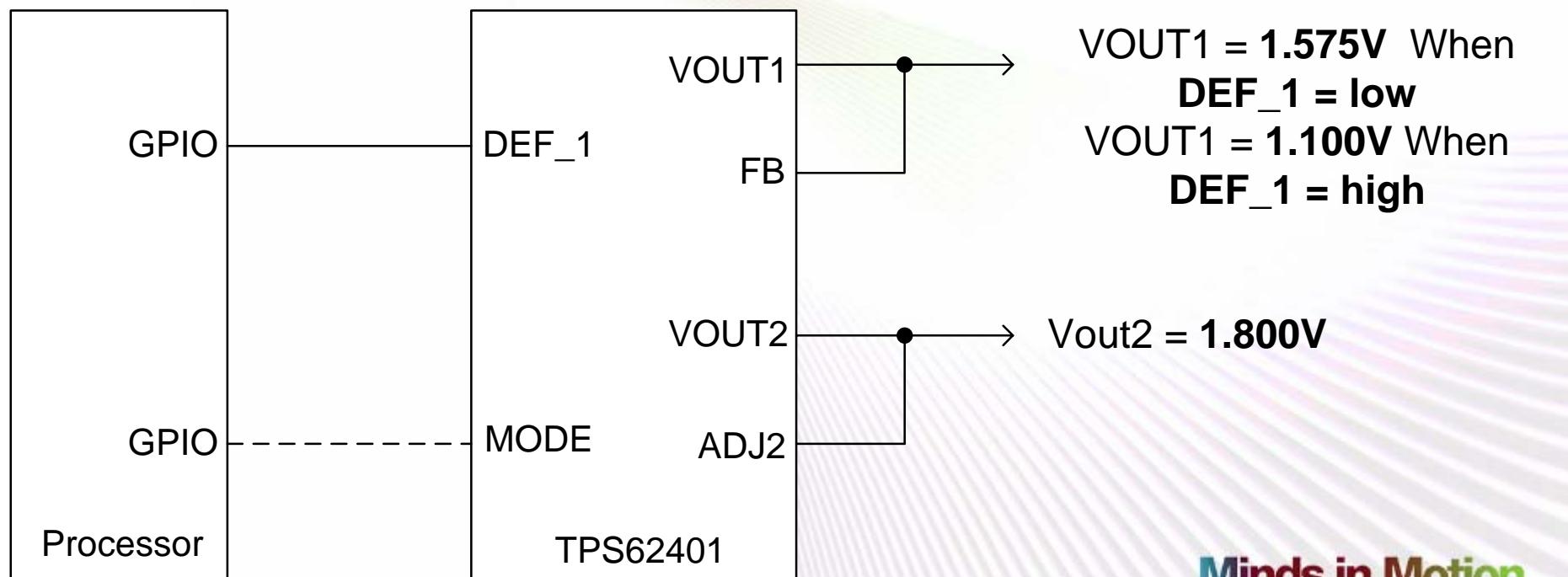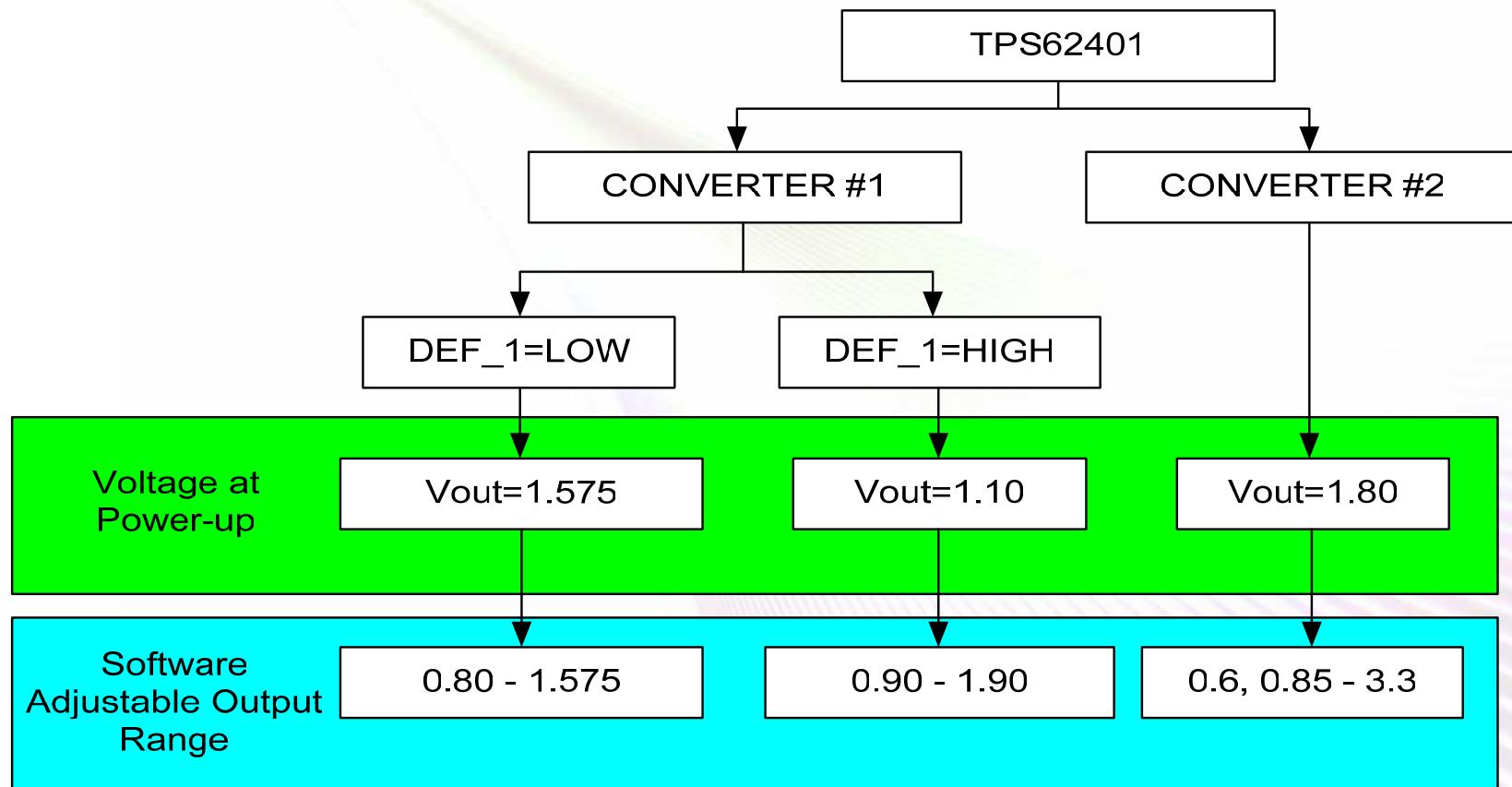
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Easyscale Protocol

START	Device Address 8 bits	EOS	START	Data Byte 8 bits	EOS

DA7 0	DA6 1	DA5 0	DA4 0	DA3 1	DA2 1	DA1 1	DA7 0

Fixed to 4E hex

| RFA	A1	A0	D4	D3	D2	D1	D0
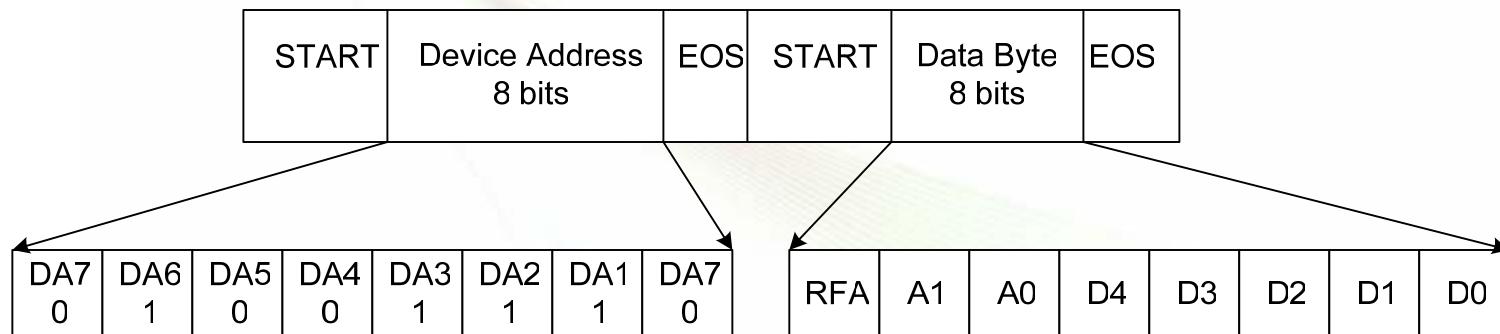
RFA: Request for Acknowledge
0=no ack

A0 & A1: Register Address
00 – DEF_1_LOW reg.
01 – DEF_1_High reg.
10 – DEF_2 reg
11 – not valid

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Easyscale Waveforms & Bit Coding
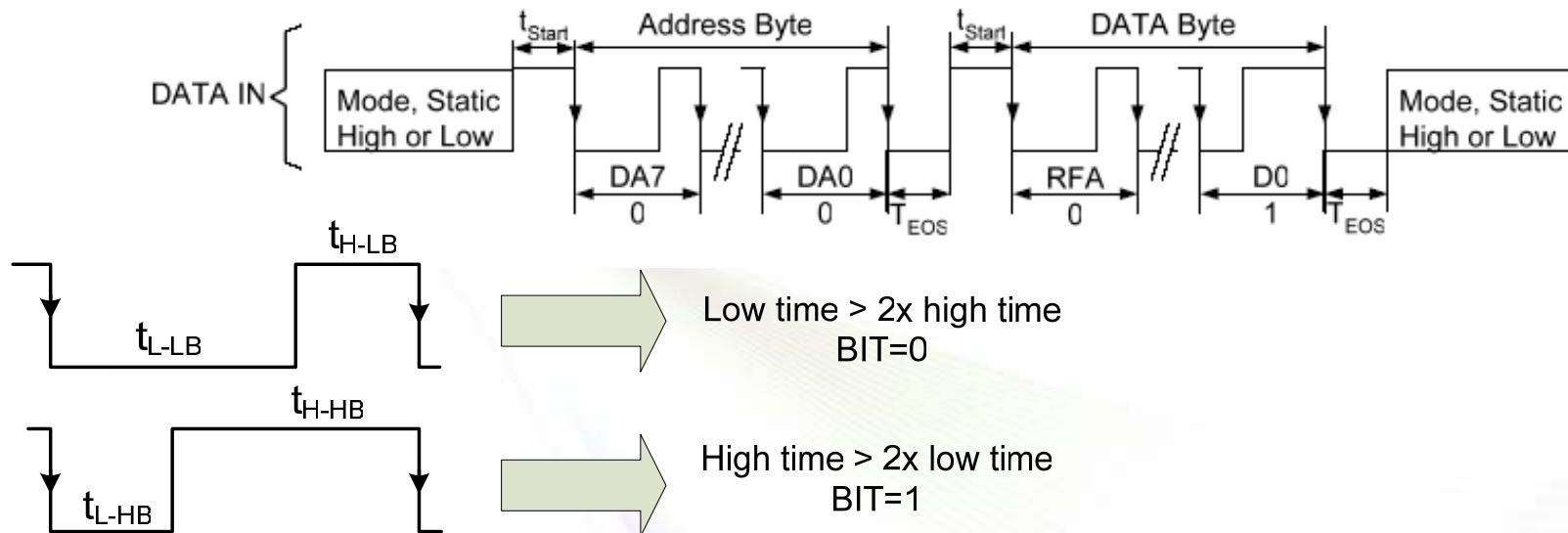
| t_{H_LB}	High Time Low Bit, logic 0 detection	signal level on MODE/DATA pin is > 1.2V	2	200	us
t_{L_LB}	Low Time Low Bit, logic 0 detection	signal level on MODE/DATA pin < 0.4V	2x t_{H_LB}	400	us
t_{L_HB}	LowTime High Bit, logic 1 detection	signal level on MODE/DATA pin < 0.4V	2	200	us
t_{H_HB}	High Time High Bit, logic 1 detection	signal level on MODE/DATA pin is > 1.2V	2x t_{L_HB}	400	us

TPS62400 DSP Application
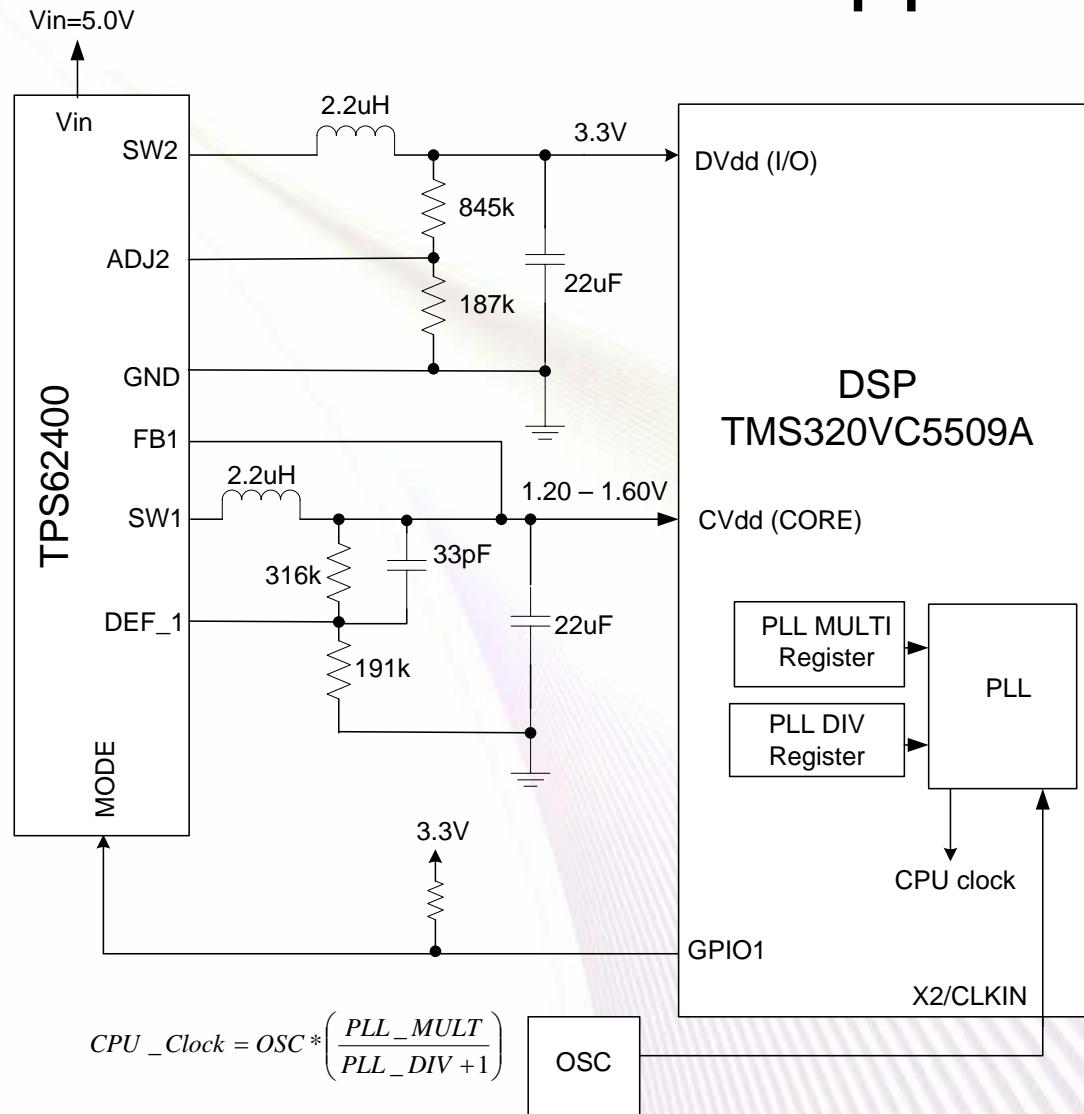
$$CPU\_Clock = OSC * \left(\frac{PLL\_MULT}{PLL\_DIV + 1} \right)$$

DSP Firmware Process

```
                    ┌─────────────────────────┐
                    │       POWER UP          │
                    │       TPS62400          │
                    │    CV_cc=1.60V          │
                    │    DV_dd=3.3            │
                    └────────────┬────────────┘
                                 │
                                 ▼
                    ┌─────────────────────────┐
                    │ 5509 Resets and initializes │
                    │   Set clock to 192Mhz   │
                    └────────────┬────────────┘
                                 │
```

POWER UP
TPS62400
$CV_{cc}=1.60V$
$DV_{dd}=3.3$

5509 Resets and initializes
Set clock to 192Mhz

LOW NEED

Write 10h to
DEF_1_LOW
CVcc=1.2V

Set clock to
24Mhz

Calculate
Processing
Needs

Write 00h to
DEF_1_LOW
CVcc=1.6V

Set clock to
192Mhz

HIGH NEED
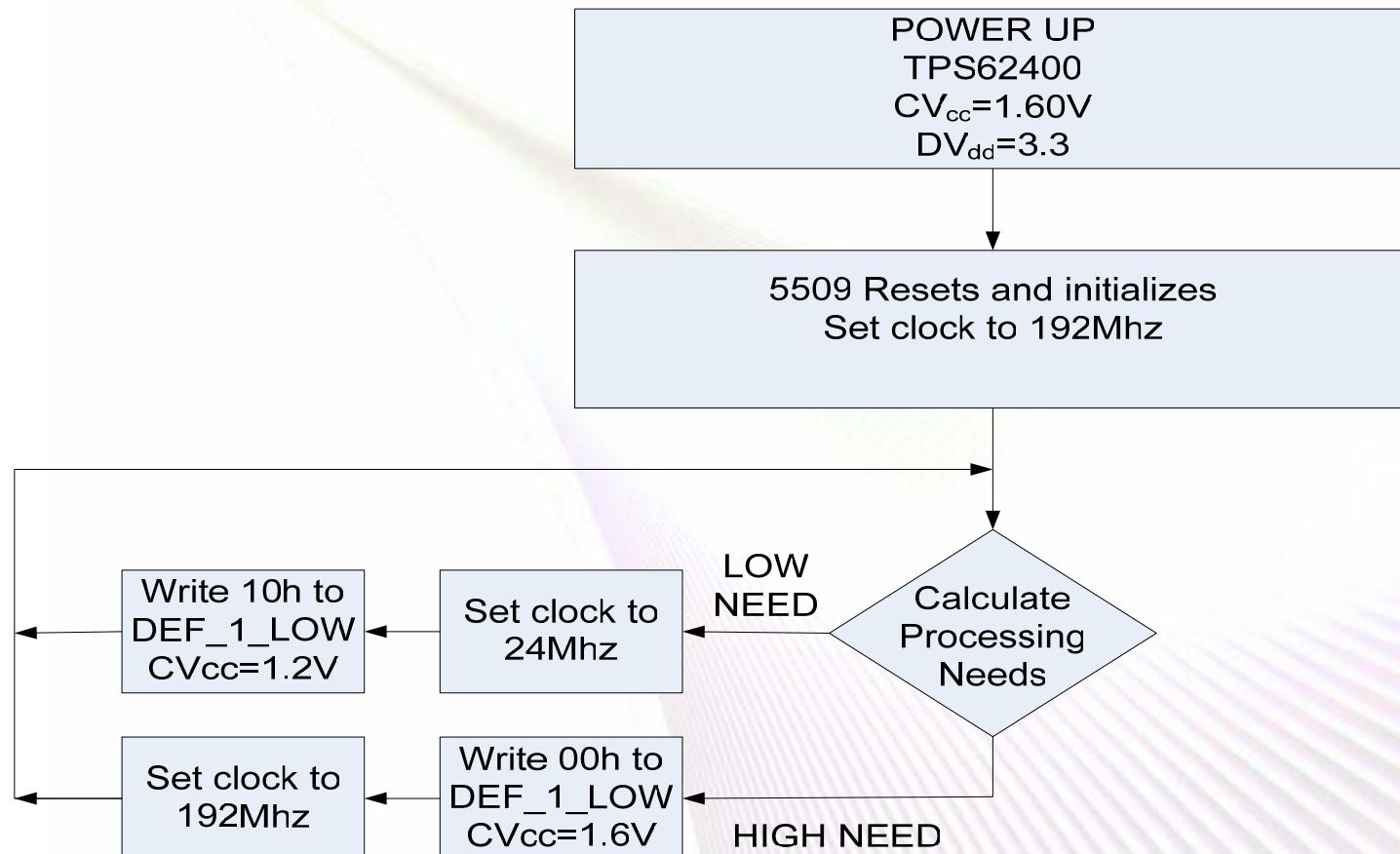
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Conclusion

- DVS can achieve significant power savings.
- DVS implementation requires a special-purpose power supply.
  - The power supply must be able to adjust the output voltage and remain stable.
  - There must be an interface between the power supply and the DSP or processor.
- TI has several power supply ICs to support dynamic voltage scaling designs.

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