

Low I_Q Low Dropout Regulators for Battery Powered Applications



1 Introduction

Modern low I_Q LDOs are designed to minimize power consumption by minimizing the quiescent current consumed, especially under light-load or no-load conditions. This focus on ultra-low I_Q enables more efficient power management and simplifies system design for products that are mostly operated in standby or idle state where power consumption must be minimized to maximize battery life (Figure 1).

Texas Instruments (TI) offers a broad range of low I_Q LDOs (Table 1) designed for multiple input voltage ranges and output current requirements to accommodate different system needs.

Table 1. Low - I_Q LDOs Voltage versus Current

LiPo Battery Pack Voltage ⁽¹⁾	$I_{OUT} < 300mA$	$300mA \leq I_{OUT} \leq 500mA$
$V_{IN} > 60V$ ($V_{IN} > 14s$)	TPS7A43	-
$40V < V_{IN} \leq 60V$ ($9s < V_{IN} \leq 14s$)	TPS7A16A	-
$30V < V_{IN} \leq 40V$ ($7s < V_{IN} \leq 9s$)	TPS7E81	TPS7E82
$18V < V_{IN} \leq 30V$ ($4s < V_{IN} \leq 7s$)	TLV709	TPS7E72
$7V \leq V_{IN} \leq 18V$ ($1s < V_{IN} \leq 4s$)	TPS7A24	TPS7A26
$V_{IN} < 7V$ ($V_{IN} = 1s$)	TPS7A02	TPS7A11

(1) $Xs = 3.7V$ times X number of cells in series

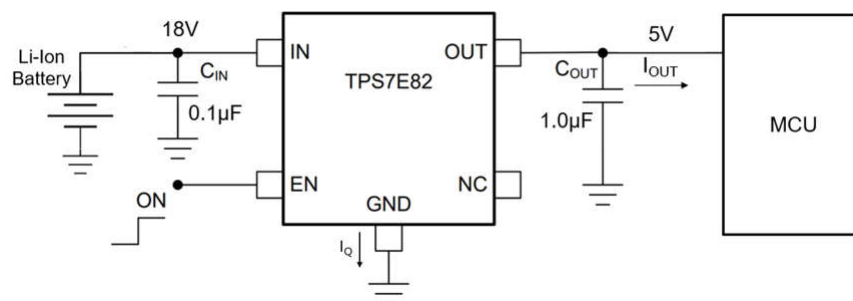


Figure 1. TPS7E82 Being Powered by a Multicell Battery

Table 2 highlights TI's latest top low I_Q LDOs sorted by maximum input voltage and provides the electrical specifications many low I_Q system designers use to select devices.

Table 2. Low I_Q LDOs Electrical Specifications

Device	Input Voltage (Max)	Output Current (Max)	Quiescent Current (I _Q)	Shutdown Current (I _{SHUTDOWN}) ⁽²⁾	Accuracy ⁽³⁾	Packages Available	Package Dimensions ⁽¹⁾	Thermal Resistance (R _{θJA})
TPS7A43	85V	50mA	5.5μA	710nA	±0.75%	HVSSOP	3mm × 4.9mm	53.7°C/W
TPS7A16A	60V	100mA	5μA	590nA	±2%	HVSSOP	3mm × 4.9mm	52.5°C/W
TPS7E82	40V	300mA	2.8μA	450nA	±1.2%	SOT-23	2.9mm × 2.8mm	190.9°C/W
						WSO	2mm × 2mm	90.2°C/W
TPS7E81	40V	150mA	2.8μA	450nA	±1.2%	SOT-23	2.9mm × 2.8mm	190.9°C/W
						WSO	2mm × 2mm	90.2°C/W
TPS7E72	30V	300mA	2.8μA	450nA	±1.2%	SOT-23	2.9mm × 2.8mm	190.9°C/W
						WSO	2mm × 2mm	90.2°C/W
TLV709	30V	150mA	3.2μA	-	±4%	SOT-89	4.5mm × 4.095mm	72.5°C/W
						SOT-23	2.9mm × 2.8mm	195.7°C/W
TPS7A26	18V	500mA	2μA	325nA	±1%	WSO	2mm × 2mm	73.3°C/W
TPS7A24	18V	200mA	2μA	325nA	±1.25%	SOT-23	2.9mm × 2.8mm	167.8°C/W
TPS7A02	6V	200mA	25nA	3nA	±1%	DSBGA	0.637mm × 0.637mm	201.1°C/W
						SOT-23	2.9mm × 2.8mm	181.9°C/W
						X2SON	1mm × 1mm	179.1°C/W
TPS7A11	3.3V	500mA	6μA	70nA ⁽⁴⁾	±1.5%	DSBGA	1.13mm × 0.78mm	169.4°C/W
						WSO	2mm × 2mm	77.3°C/W

(1) Package dimensions (length × width) is a nominal value and includes pins, where applicable.

(2) Typical values measured at 25°C.

(3) Across line, load, and temperature.

(4) Includes input and bias current.

Table 3. Low I_Q LDO Feature Comparison

	TPS7A43	TPS7E82	TPS7E81	TPS7E72	TLV709	TPS7A26	TPS7A24	TPS7A16A	TPS7A02	TPS7A11
Adjustable Version Available	✓	✓	✓	✓	✓	✓	✓	✓		
Enable Logic	✓	✓	✓	✓		✓	✓	✓	✓	✓
Internal Enable Pull Up or Pull Down	Pull Up	Pull Up	Pull Up	Pull Up					Pull Down	
Power Good	✓					✓		✓		
Operational Junction Temperature (T_J) up to 150 °C		✓	✓	✓						
Transient Performance ⁽¹⁾	★★	★★★	★★★	★★★	★	★★	★★	★	★★★★	★★★★★

(1) Rank is based on what TI considers high performance (1 ★ lowest – 5 ★ highest). Rank is determined by comparative load step response and includes line and load transients.

2 Adjustable Feedback Voltage

While adjustable LDOs offer flexibility to meet non-standard voltage requirements, the external resistor feedback network required to set the output can significantly increase the total system quiescent current (I_Q). Because the current through the divider is inversely proportional to the network's total resistance, the choice of resistors directly impacts the system's overall power dissipation. To optimize efficiency in battery-powered applications, systems must utilize high-impedance resistor networks to minimize the parasitic current drawn from the output.

However, this optimization must be balanced against the requirement for regulation accuracy. If the resistor values are excessively high, the feedback current can become comparable to the LDO internal leakage current, creating a voltage error at the feedback pin that shifts the output from the intended output. To reconcile low system-wide power consumption with high precision, a good approximation is to maintain the current flowing through the divider is at least 100 times greater than the LDO's maximum expected leakage current. This approach allows for significant reduction in total system I_Q without compromising the stability or accuracy of the voltage regulation.

3 Power Good

Devices with a Power Good feature (PG) have an integrated comparator that monitors the output voltage relative to the internal reference voltage.

Applications with an MCU can be configured to remain in a reset state or a low-power standby mode until it detects a change on the PG pin. Once the LDO output voltage exceeds the internal threshold and the PG pin asserts high, usually via an external pull-up resistor, the MCU receives a signal that the power rails are established. This maintains that the processor only begins when the electrical environment is safe and consistent (Figure 2).

Furthermore, the PG pin provides continuous monitoring that extends beyond the initial startup. If the input voltage drops significantly or if there is a sudden load change that causes the output voltage to sag below a safe level, the PG pin pulls low.

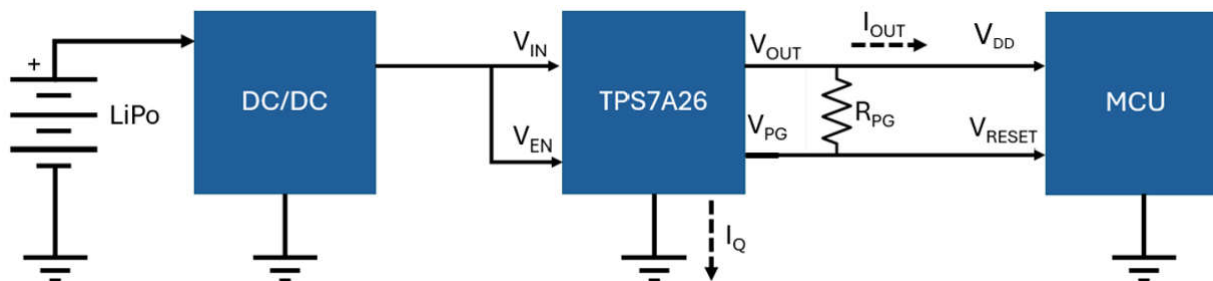


Figure 2. TPS7A26 using Power Good Functionality

4 Enable Logic

An enable (EN) pin on an LDO allows designers to dynamically turn an LDO on and off to save power by leveraging the lower shutdown current (I_{SHDN}) instead of the I_Q .

Table 4 is an example breakdown of how these two parameters impact power savings on TPS7E81.

Table 4. Dynamic Power Dissipation Enable

Enable Level	Conditions	Current seen from GND Pin		Input Voltage	Power Dissipated
		Quiescent Current (I_Q) ⁽¹⁾	Shutdown Current (I_{SHDN}) ⁽¹⁾		
$V_{EN} = 2V$ (High)	Device is ON, $I_{OUT} = 0mA$	7.6 μA	-	12V	91.2 μW
$V_{EN} = 0V$ (Low)	Device is OFF	-	1.5 μA		18 μW

(1) Max values seen across $V_{OUT} + 0.5V \leq V_{IN} \leq 40V$ for operating temperature range of TPS7E81.

LDO's enable (EN) pin sometimes has an internal pull-up or pull-down resistor where the primary consideration is the device default state and how that state affects your system power profile. An internal pull-up maintains the LDO is enabled by default as soon as an input voltage is applied to the device. This is ideal for *always-on* rails that must be active immediately to support system startup without requiring intervention from a microcontroller.

In contrast, an internal pull-down keeps the LDO in a disabled state when the EN pin is left floating. This allows the LDO to remain completely inactive until the pin is driven high.

Precision EN, like in TPS7A43, is a feature that helps enable or disable an LDO at a fixed and accurate threshold voltage. In battery applications, V_{IN} can fluctuate as the battery discharges. Precision EN allows the system to disable the LDO at a specific, predictable voltage threshold, protecting the downstream components and optimizing power usage.

5 Package Selection

A common misconception in LDO selection is the assumption that choosing a physically larger package yields better thermal performance but this is not always the case. A critical factor in LDO thermal management is the PCB layout and with a good layout, heat spread on a board often outperforms a poorly laid out design with a large package.

Table 2 makes the package-versus-thermal-resistance relationship impossible to ignore. For instance, TPS7E82 is available in two industry-standard packages: SOT-23 (190.9°C/W) for high footprint compatibility and the WSON package (90.2°C/W) for thermally conscious designs. Despite the WSON being more than 50% smaller than the SOT-23, it provides more than a 50% improvement in thermal resistance. Choosing a low $R_{\theta JA}$ package is only half the equation as the $R_{\theta JA}$ values published in datasheets are measured and defined by JEDEC standards. In a real PCB design, your actual thermal resistance can be significantly better or worse depending on how well you implement the layout around the device (see [An empirical analysis of the impact of board layout on LDO thermal performance \[Rev. A\]](#)).

For packages with an exposed thermal pad, such as the WSON or HVSSOP, the thermal pad must be soldered directly to a copper pour on the PCB, which then spreads heat laterally across the board. Maximizing this copper area, stitching it with thermal vias to inner ground planes on a multi-layer board, and avoiding thermal relief connections on the pad all dramatically reduce the effective θ_{JA} beyond what the datasheet specifies.

6 Controlled I_Q In Dropout

Controlled I_Q in an LDO refers to the regulator's ability to keep the quiescent current relatively low even when the device operates in dropout. In battery-powered applications, dropout can occur when the battery has discharged until the difference between V_{IN} and V_{OUT} , also known as headroom ($V_{HEADROOM}$), is at or below the dropout voltage (V_{DO}). When $V_{HEADROOM}$ is at or below the dropout voltage, the error amplifier struggles to drive the pass element to the required operating point and saturates, drawing more current which is shown in Figure 3.

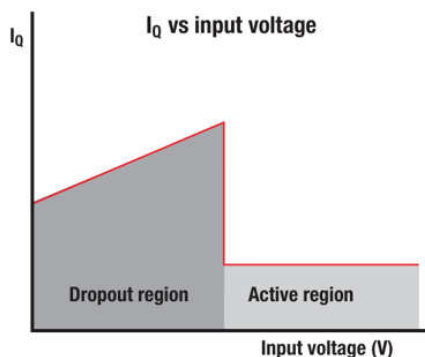


Figure 3. Typical LDO IQ Behavior in Dropout Conditions

Comparing the I_Q response in Figure 3 and Figure 5 highlights the impact of internal circuit saturation. While Figure 3 shows a stabilized I_Q profile, Figure 5 exhibits a significantly more severe I_Q spike, which may result in increased battery drain and unintended voltage sags in dropout conditions.

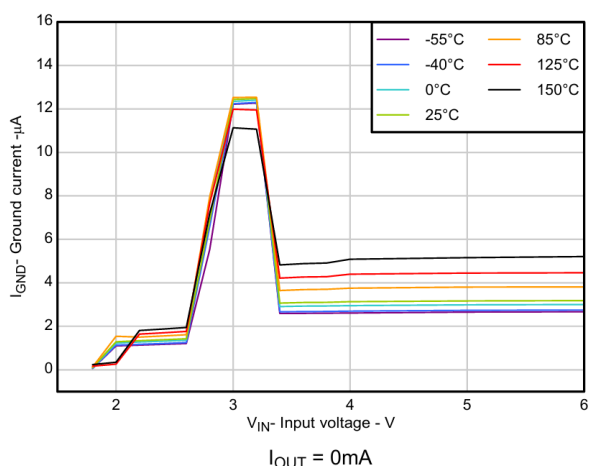


Figure 4. Comparing IQ in Dropout, Controlled I_Q

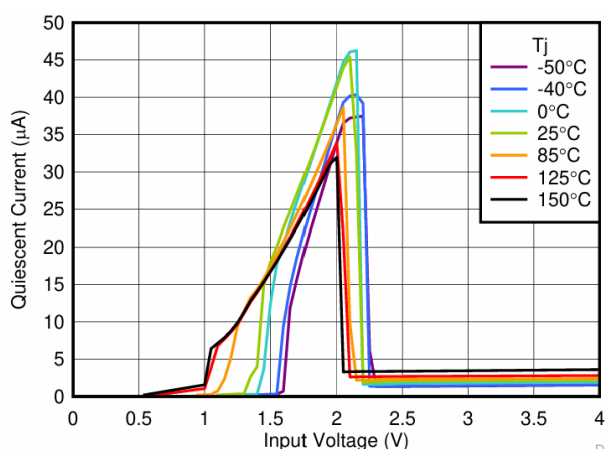
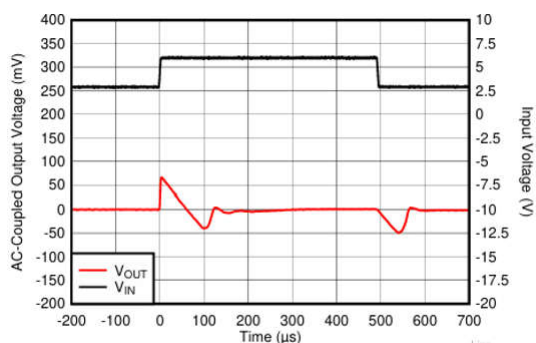


Figure 5. Comparing IQ in Dropout, Typical

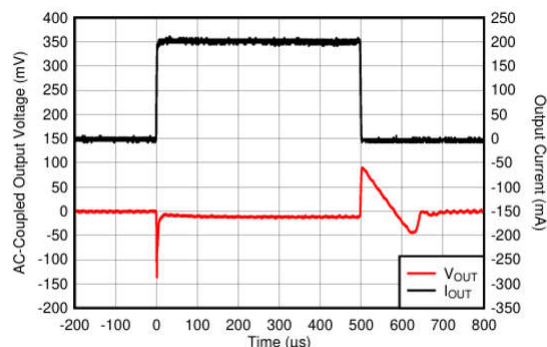
7 Transient Performance

Load transient performance describes the LDO's ability to maintain the output voltage when the load changes. The key metrics are the voltage deviation (undershoot/overshoot) during a load-step and the settling time needed for the output to settle back within spec. Minimizing this peak in an LDO's transient response can help shorten the time the regulator needs to bring its output back within the specified window, which in turn tightens the overall recovery time.



$V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 1\text{ }\mu\text{F}$, slew rate = $1\text{ V}/\mu\text{s}$

Figure 6. Example Line Transient for LDOs



$V_{OUT} = 1.8\text{ V}$, $V_{IN} = 2.8\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $t_r = t_f = 1\text{ }\mu\text{s}$

Figure 7. Example Load Transient for LDOs

A line transient occurs when the input voltage changes abruptly, for example, when a battery's voltage sags under heavy use. A load transient occurs when the current demand from the circuit changes suddenly, like when a motor kicks on or a MCU wakes up from sleep mode. In both cases, the LDO's output voltage momentarily dips or spikes before regulating back to the target voltage. In battery-operated applications like power tools or home appliances, this matters because an unexpected voltage dip can trigger false fault conditions. An LDO with good transient response recovers from these disturbances quickly and with minimal voltage deviation, maintaining reliable operation even as the battery drains and loads switch on and off throughout normal use. See [Table 3](#) for a comparison of transient performance across TI's low I_Q portfolio. Improving an LDO's transient response involves selecting the right type and value of output capacitor, as well as maintaining the error amplifier has sufficient bandwidth to react quickly to load steps.

8 Summary

This overview highlighted how TI's top low I_Q LDOs are key to maximizing battery life in standby or idle power applications because they draw a minimal amount of quiescent current. Beyond ultra-low I_Q , these modern LDOs offer integrated protection circuitry and output voltage monitoring features that allow for stable output performance and improve the overall functionality of the system.

Check out our [complete low \$I_Q\$ LDO portfolio here](#).

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