

Technical Reference Manual

J721E DRA829/TDA4VM/AM68P Processors Silicon Revision 1.1 Texas Instruments Families of Products



1 ADC Registers

1.1 ADC Configuration Registers

Table 1-2 lists the memory-mapped registers for the ADC. All register offset addresses not listed in Table 1-2 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. ADC Instances

Instance	Base Address
MCU_ADC0	4020 0000h
MCU_ADC1	4021 0000h

Table 1-2. ADC Registers

Offset	Acronym	Register Name	MCU_ADC0 Physical Address	MCU_ADC1 Physical Address
0h	ADC_REVISION	Revision Identifier Register	4020 0000h	4021 0000h
20h	ADC_EOI	End of Interrupt Register	4020 0020h	4021 0020h
24h	ADC_STATUS_RAW	Raw Interrupt Status Register	4020 0024h	4021 0024h
28h	ADC_STATUS	Interrupt Status Register	4020 0028h	4021 0028h
2Ch	ADC_ENABLE_SET	Interrupt Enable Register	4020 002Ch	4021 002Ch
30h	ADC_ENABLE_CLR	Interrupt Disable Register	4020 0030h	4021 0030h
38h	ADC_DMAENABLE_SET	DMA Request Enable Register	4020 0038h	4021 0038h
3Ch	ADC_DMAENABLE_CLR	DMA Request Disable Register	4020 003Ch	4021 003Ch
40h	ADC_CONTROL	Control Register	4020 0040h	4021 0040h
44h	ADC_SEQUENCER_STAT	Sequencer Status Register	4020 0044h	4021 0044h
48h	ADC_RANGE	Range Check Register	4020 0048h	4021 0048h
50h	ADC_MISC	AFE Input/Output Control Register	4020 0050h	4021 0050h
54h	ADC_STEPENABLE	Sequencer Step Enable Register	4020 0054h	4021 0054h
64h + formula	ADC_STEPCONFIG_j	Step Configuration Register	4020 0000h	4021 0000h
68h + formula	ADC_STEPDELAY_j	Step Delay Register	4020 0000h	4021 0000h
E4h	ADC_FIFO0WC	FIFO0 Word Count Register	4020 00E4h	4021 00E4h
E8h	ADC_FIFO0THRESHOLD	FIFO0 Threshold Level Register	4020 00E8h	4021 00E8h
ECh	ADC_FIFO0DMAREQ	FIFO0 DMA Request Level Register	4020 00ECh	4021 00ECh
F0h	ADC_FIFO1WC	FIFO1 Word Count Register	4020 00F0h	4021 00F0h
F4h	ADC_FIFO1THRESHOLD	FIFO1 Threshold Level Register	4020 00F4h	4021 00F4h
F8h	ADC_FIFO1DMAREQ	FIFO1 DMA Request Level Register	4020 00F8h	4021 00F8h
100h	ADC_FIFO0DATA	FIFO0 Read Data Register	4020 0100h	4021 0100h
200h	ADC_FIFO1DATA	FIFO1 Read Data Register	4020 0200h	4021 0200h

1.2 ADC_REVISION Register (Offset = 0h) [reset = Xh]

ADC_REVISION is shown in [Figure 1-1](#) and described in [Table 1-4](#).

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IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility.

Reset = 00452900h

Table 1-3. ADC_REVISION Instances

Instance	Physical Address
MCU_ADC0	4020 0000h
MCU_ADC1	4021 0000h

Figure 1-1. ADC_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-45h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-5h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 1-4. ADC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	45h	Module ID field
15-11	REVRTL	R	5h	RTL ADC_REVISION. Will vary depending on release.
10-8	REVMAJ	R	1h	Major ADC_REVISION
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	0h	Minor ADC_REVISION

1.3 ADC_EOI Register (Offset = 20h) [reset = 0h]

ADC_EOI is shown in [Figure 1-2](#) and described in [Table 1-6](#).

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The End of Interrupt (ADC_EOI) ADC_MISC Register allows the CPU to acknowledge completion of an interrupt by writing to the ADC_EOI for ADC_MISC interrupt sources. An eoi_write signal will be generated and another interrupt will be triggered if interrupt sources remain. This register will be reset one cycle after it has been written to.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 1-5. ADC_EOI Instances

Instance	Physical Address
MCU_ADC0	4020 0020h
MCU_ADC1	4021 0020h

Figure 1-2. ADC_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							LINENUMEIOI
R-0h							W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 1-6. ADC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	LINENUMEIOI	W	0h	Software End Of Interrupt (EOI) control. 0h = EOI for interrupt line number 0. Read returns 0.

1.4 ADC_STATUS_RAW Register (Offset = 24h) [reset = 0h]

ADC_STATUS_RAW is shown in [Figure 1-3](#) and described in [Table 1-8](#).

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The ADC_STATUS_RAW register allows the MCU_ADC0/1 interrupt sources to be manually set when writing a 1 to a specific bit. Write 0: No action Write 1: Set event Read 0: No event pending Read 1: Event pending

Table 1-7. ADC_STATUS_RAW Instances

Instance	Physical Address
MCU_ADC0	4020 0024h
MCU_ADC1	4021 0024h

Figure 1-3. ADC_STATUS_RAW Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUTOFRANGE
R-0h							R/W-0h
7	6	5	4	3	2	1	0
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUEN CE	AFE_EOC_MIS SING
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-8. ADC_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUTOFRANGE	R/W	0h	Status raw for out of range interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
7	FIFO1UNFL	R/W	0h	Status raw for FIFO1 under-flow interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
6	FIFO1OVFL	R/W	0h	Status raw for FIFO1 over-flow interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending

Table 1-8. ADC_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FIFO1THRS	R/W	0h	Status raw for FIFO1 threshold interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
4	FIFO0UNFL	R/W	0h	Status raw for FIFO0 under-flow interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
3	FIFO0OVFL	R/W	0h	Status raw for FIFO0 over-flow interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
2	FIFO0THRS	R/W	0h	Status raw for FIFO0 threshold interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
1	ENDOFSEQUENCE	R/W	0h	Status raw for end of sequence interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending
0	AFE_EOC_MISSING	R/W	0h	Status raw for missing AFE EOC interrupt. Write 0h = No action Write 1h = Set event (debug) Read 0h = No event pending Read 1h = Event pending

1.5 ADC_STATUS Register (Offset = 28h) [reset = 0h]

ADC_STATUS is shown in [Figure 1-4](#) and described in [Table 1-10](#).

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The ADC_STATUS register allows the MCU_ADC0/1 interrupt sources to be manually cleared when writing a 1 to a specific bit. Write 0: No action Write 1: Clear event Read 0: No event pending Read 1: Event pending

Table 1-9. ADC_STATUS Instances

Instance	Physical Address
MCU_ADC0	4020 0028h
MCU_ADC1	4021 0028h

Figure 1-4. ADC_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUTOFRANGE
R-0h							R/W-0h
7	6	5	4	3	2	1	0
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUEN CE	AFE_EOC_MIS SING
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-10. ADC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUTOFRANGE	R/W	0h	Enabled status for out of range interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
7	FIFO1UNFL	R/W	0h	Enabled status for FIFO1 under-flow interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
6	FIFO1OVFL	R/W	0h	Enabled status for FIFO1 over-flow interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending

Table 1-10. ADC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FIFO1THRS	R/W	0h	Enabled status for FIFO1 threshold interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
4	FIFO0UNFL	R/W	0h	Enabled status for FIFO0 under-flow interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
3	FIFO0OVFL	R/W	0h	Enabled status for FIFO0 over-flow interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
2	FIFO0THRS	R/W	0h	Enabled status for FIFO0 threshold interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
1	ENDOFSEQUENCE	R/W	0h	Enabled status for end of sequence interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending
0	AFE_EOC_MISSING	R/W	0h	Enable status for missing AFE EOC interrupt. Write 0h = No action Write 1h = Clear (raw) event Read 0h = No (enabled) event pending Read 1h = Event pending

1.6 ADC_ENABLE_SET Register (Offset = 2Ch) [reset = 0h]

ADC_ENABLE_SET is shown in [Figure 1-5](#) and described in [Table 1-12](#).

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The ADC_ENABLE_SET register allows the MCU_ADC0/1 interrupt sources to be manually enabled when writing a 1 to a specific bit. Write 0: No action Write 1: Enable event Read 0: Event is disabled Read 1: Event is enabled

Table 1-11. ADC_ENABLE_SET Instances

Instance	Physical Address
MCU_ADC0	4020 002Ch
MCU_ADC1	4021 002Ch

Figure 1-5. ADC_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUTOFRANGE
R-0h							R/W-0h
7	6	5	4	3	2	1	0
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUEN CE	AFE_EOC_MIS SING
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-12. ADC_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUTOFRANGE	R/W	0h	Out of range interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
7	FIFO1UNFL	R/W	0h	FIFO1 under-flow interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
6	FIFO1OVFL	R/W	0h	FIFO1 over-flow interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled

Table 1-12. ADC_ENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FIFO1THRS	R/W	0h	FIFO1 threshold interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
4	FIFO0UNFL	R/W	0h	FIFO0 under-flow interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
3	FIFO0OVFL	R/W	0h	FIFO0 over-flow interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
2	FIFO0THRS	R/W	0h	FIFO0 threshold interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
1	ENDOFSEQUENCE	R/W	0h	End of sequence interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
0	AFE_EOC_MISSING	R/W	0h	Missing AFE EOC interrupt enable. Write 0h = No action Write 1h = Enable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled

1.7 ADC_ENABLE_CLR Register (Offset = 30h) [reset = 0h]

ADC_ENABLE_CLR is shown in [Figure 1-6](#) and described in [Table 1-14](#).

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The ADC_ENABLE_CLR register allows the MCU_ADC0/1 interrupt sources to be manually disabled when writing a 1 to a specific bit. Write 0: No action Write 1: Disable event Read 0: Event is disabled Read 1: Event is enabled

Table 1-13. ADC_ENABLE_CLR Instances

Instance	Physical Address
MCU_ADC0	4020 0030h
MCU_ADC1	4021 0030h

Figure 1-6. ADC_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUTOFRANGE
R-0h							R/W-0h
7	6	5	4	3	2	1	0
FIFO1UNFL	FIFO1OVFL	FIFO1THRS	FIFO0UNFL	FIFO0OVFL	FIFO0THRS	ENDOFEQUEN CE	AFE_EOC_MIS SING
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-14. ADC_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUTOFRANGE	R/W	0h	Out of range interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
7	FIFO1UNFL	R/W	0h	FIFO1 under-flow interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
6	FIFO1OVFL	R/W	0h	FIFO1 over-flow interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled

Table 1-14. ADC_ENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FIFO1THRS	R/W	0h	FIFO1 threshold interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
4	FIFO0UNFL	R/W	0h	FIFO0 under-flow interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
3	FIFO0OVFL	R/W	0h	FIFO0 over-flow interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
2	FIFO0THRS	R/W	0h	FIFO0 threshold interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
1	ENDOFSEQUENCE	R/W	0h	End of sequence interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled
0	AFE_EOC_MISSING	R/W	0h	Missing AFE EOC interrupt disable. Write 0h = No action Write 1h = Disable interrupt Read 0h = Interrupt disabled (masked) Read 1h = Interrupt enabled

1.8 ADC_DMAENABLE_SET Register (Offset = 38h) [reset = X]

ADC_DMAENABLE_SET is shown in [Figure 1-7](#) and described in [Table 1-16](#).

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The ADC_DMAENABLE_SET register allows the enabling of DMA requests.

Table 1-15. ADC_DMAENABLE_SET Instances

Instance	Physical Address
MCU_ADC0	4020 0038h
MCU_ADC1	4021 0038h

Figure 1-7. ADC_DMAENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R/W-X	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						ENABLE1	ENABLE0
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-16. ADC_DMAENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	Reserved
30-2	RESERVED	R	0h	Reserved
1	ENABLE1	R/W	0h	Enable DMA event to FIFO1 Write 0h = No action Write 1h = Enable DMA event Read 0h = DMA event disabled Read 1h = DMA event enabled
0	ENABLE0	R/W	0h	Enable DMA event to FIFO0 Write 0h = No action Write 1h = Enable DMA event Read 0h = DMA event disabled Read 1h = DMA event enabled

1.9 ADC_DMAENABLE_CLR Register (Offset = 3Ch) [reset = X]

ADC_DMAENABLE_CLR is shown in [Figure 1-8](#) and described in [Table 1-18](#).

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The ADC_DMAENABLE_CLR register allows the disabling of DMA requests.

Table 1-17. ADC_DMAENABLE_CLR Instances

Instance	Physical Address
MCU_ADC0	4020 003Ch
MCU_ADC1	4021 003Ch

Figure 1-8. ADC_DMAENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						
R/W-X	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						ENABLE1	ENABLE0
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-18. ADC_DMAENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	Reserved
30-2	RESERVED	R	0h	Reserved
1	ENABLE1	R/W	0h	Clears the enable of the DMA event to FIFO1. Disable DMA event to FIFO1 Write 0h = No action Write 1h = Disable DMA event Read 0h = DMA event disabled Read 1h = DMA event enabled
0	ENABLE0	R/W	0h	Clears the enable of the DMA event to FIFO0. Disable DMA event to FIFO0 Write 0h = No action Write 1h = Disable DMA event Read 0h = DMA event disabled Read 1h = DMA event enabled

1.10 ADC_CONTROL Register (Offset = 40h) [reset = 10h]

ADC_CONTROL is shown in [Figure 1-9](#) and described in [Table 1-20](#).

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Controls various parameters of the controller state.

Table 1-19. ADC_CONTROL Instances

Instance	Physical Address
MCU_ADC0	4020 0040h
MCU_ADC1	4021 0040h

Figure 1-9. ADC_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				HI_MID_SEL	HI_MID_EN	HW_PREEMPT	HW_MAP
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			PD	RESERVED		STEP_ID_EN	MODULE_ENABLE
R-0h			R/W-1h	R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-20. ADC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	HI_MID_SEL	R/W	0h	Reference select for functional internal diagnostic debug mode. 0h = VMID 1h = REFP
10	HI_MID_EN	R/W	0h	Functional internal diagnostic debug mode. 0h = disabled 1h = enabled
9	HW_PREEMPT	R/W	0h	0h = SW steps are not preempted by HW events 1h = SW steps are preempted by HW events
8	HW_MAP	R/W	0h	0h = HW events are disabled 1h = HW events are enabled
7-5	RESERVED	R	0h	Reserved
4	PD	R/W	1h	ADC Power Down control. 0h = AFE is powered up 1h = AFE is powered down (default) At default, AFE is powered down; Software must write 0 to turn on the power and wait 4 us before starting a conversion
3-2	RESERVED	R	0h	Reserved
1	STEP_ID_EN	R/W	0h	Writing 1 to this bit will store the Step ID number with the captured ADC data in the FIFO. 0h = Write zeros 1h = Store the input (channel) ID tag

Table 1-20. ADC_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MODULE_ENABLE	R/W	0h	<p>ADC module enable bit.</p> <p>After programming all the configuration and step enable registers, write a 1 to this bit to start conversion.</p> <p>Writing a 0 will disable the module after the current conversion.</p> <p>Before turning on again, the ADC_SEQUENCER_STAT register show read back STEP_IDLE = 10h and FSM_BUSY = 0h.</p> <p>Enabling the controller will be held off until MEM_INIT_DONE = 1h.</p>

1.11 ADC_SEQUENCER_STAT Register (Offset = 44h) [reset = 20h]

ADC_SEQUENCER_STAT is shown in [Figure 1-10](#) and described in [Table 1-22](#).

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SW can read this register to find out the currently scheduled step id being converted on the ADC port. If you want to turn the controller off and then back on, the step_id bit should be checked and compared to IDLE before enabling the ADC module again. Also, before enabling the controller again, the user should wait for the FSM bit 5 to read idl.

Table 1-21. ADC_SEQUENCER_STAT Instances

Instance	Physical Address
MCU_ADC0	4020 0044h
MCU_ADC1	4021 0044h

Figure 1-10. ADC_SEQUENCER_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	MEM_INIT_DONE	FSM_BUSY	STEP_IDLE				
R-0h	R-0h	R-1h	R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 1-22. ADC_SEQUENCER_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	MEM_INIT_DONE	R	0h	ADC_STATUS of RAM initialization for ECC. 1h = RAM initialization to 0 after reset is done.
5	FSM_BUSY	R	1h	ADC_STATUS of FSM. 0h = Idle 1h = Conversion in progress
4-0	STEP_IDLE	R	0h	10h = Idle 0h - Fh = Corresponds to Step 1 - Step 16

1.12 ADC_RANGE Register (Offset = 48h) [reset = 0h]

ADC_RANGE is shown in [Figure 1-11](#) and described in [Table 1-24](#).

Return to [Summary Table](#).

This feature requires the ADC_RANGE check interrupt bit to be enabled first. The user can decide which input (channel) is compared by programming the RangeCheck bit of the ADC_STEPCONFIG_j Registers. It is up to software to sort through FIFO data to determine which input (channel) data was out of ADC_RANGE.

Table 1-23. ADC_RANGE Instances

Instance	Physical Address
MCU_ADC0	4020 0048h
MCU_ADC1	4021 0048h

Figure 1-11. ADC_RANGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HIRANGE											
R-0h				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				LOWRANGE											
R-0h				R/W-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-24. ADC_RANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-16	HIRANGE	R/W	0h	Sampled ADC data is compared to this value. If the sampled data is > HIRANGE, then interrupt is generated.
15-12	RESERVED	R	0h	Reserved
11-0	LOWRANGE	R/W	0h	Sampled ADC data is compared to this value. If the sampled data is < LOWRANGE, then interrupt is generated.

1.13 ADC_MISC Register (Offset = 50h) [reset = 0h]

ADC_MISC is shown in [Figure 1-12](#) and described in [Table 1-26](#).

Return to [Summary Table](#).

Spare inputs of the AFE are driven by this register, spare outputs from the AFE are read.

Table 1-25. ADC_MISC Instances

Instance	Physical Address
MCU_ADC0	4020 0050h
MCU_ADC1	4021 0050h

Figure 1-12. ADC_MISC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AFE_SPARE_OUT			
R-0h				R-0h			
7	6	5	4	3	2	1	0
RESERVED				AFE_SPARE_IN			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-26. ADC_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AFE_SPARE_OUT	R	0h	Connected to AFE Spare Output pins, reserved in normal operation.
7-4	RESERVED	R	0h	Reserved
3-0	AFE_SPARE_IN	R/W	0h	Connected to AFE Spare Input pins, reserved in normal operation.

1.14 ADC_STEPENABLE Register (Offset = 54h) [reset = 0h]

ADC_STEPENABLE is shown in [Figure 1-13](#) and described in [Table 1-28](#).

Return to [Summary Table](#).

Contains the enable bit for each step in the sequencer. When all steps are disabled, the FSM will stay in IDLE state.

Table 1-27. ADC_STEPENABLE Instances

Instance	Physical Address
MCU_ADC0	4020 0054h
MCU_ADC1	4021 0054h

Figure 1-13. ADC_STEPENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							STEP16
R-0h							R/W-0h
15	14	13	12	11	10	9	8
STEP15	STEP14	STEP13	STEP12	STEP11	STEP10	STEP9	STEP8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
STEP7	STEP6	STEP5	STEP4	STEP3	STEP2	STEP1	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-28. ADC_STEPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	STEP16	R/W	0h	Enable step 16
15	STEP15	R/W	0h	Enable step 15
14	STEP14	R/W	0h	Enable step 14
13	STEP13	R/W	0h	Enable step 13
12	STEP12	R/W	0h	Enable step 12
11	STEP11	R/W	0h	Enable step 11
10	STEP10	R/W	0h	Enable step 10
9	STEP9	R/W	0h	Enable step 9
8	STEP8	R/W	0h	Enable step 8
7	STEP7	R/W	0h	Enable step 7
6	STEP6	R/W	0h	Enable step 6
5	STEP5	R/W	0h	Enable step 5
4	STEP4	R/W	0h	Enable step 4
3	STEP3	R/W	0h	Enable step 3
2	STEP2	R/W	0h	Enable step 2
1	STEP1	R/W	0h	Enable step 1

Table 1-28. ADC_STEPENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0h	Reserved

1.15 ADC_STEPCONFIG_j Register (Offset = 64h + formula) [reset = 00040000h]

ADC_STEPCONFIG_j is shown in [Figure 1-14](#) and described in [Table 1-30](#).

Return to [Summary Table](#).

The user should write the appropriate value to this register that is required to configure the various functions of each step.

Offset = 64h + (j * 8h); where j = 0h to Fh

Table 1-29. ADC_STEPCONFIG_j Instances

Instance	Physical Address
MCU_ADC0	4020 0000h
MCU_ADC1	4021 0000h

Figure 1-14. ADC_STEPCONFIG_j Register

31	30	29	28	27	26	25	24
RESERVED				RANGECHECK	FIFOSEL	DIFF_CNTRL	RESERVED
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED	SEL_INP_SWC				SEL_INM_SWM		
R/W-0h	R/W-0h				R/W-8h		
15	14	13	12	11	10	9	8
SEL_INM_SW M	RESERVED						
R/W-8h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED				AVERAGING		MODE	
R/W-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-30. ADC_STEPCONFIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	RANGECHECK	R/W	0h	0h = Disable ADC_RANGE check 1h = compare ADC data with ADC_RANGE
26	FIFOSEL	R/W	0h	Sampled data will be stored in FIFO. 0h = FIFO0 1h = FIFO1
25	DIFF_CNTRL	R/W	0h	Differential ADC_CONTROL. 0h = Single ended input, SEL_INM_SWM must be 8h 1h = Differential input
24-23	RESERVED	R/W	0h	Reserved
22-19	SEL_INP_SWC	R/W	0h	Select source for positive ADC input (INP). 0h = Input (channel) 0 1h = Input (channel) 1 2h = Input (channel) 2 3h = Input (channel) 3 4h = Input (channel) 4 5h = Input (channel) 5 6h = Input (channel) 6 7h = Input (channel) 7 8h = REFN

Table 1-30. ADC_STEPCONFIG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	SEL_INM_SWM	R/W	8h	Select source for negative ADC input (INM). 0h = Input (channel) 0 1h = Input (channel) 1 2h = Input (channel) 2 3h = Input (channel) 3 4h = Input (channel) 4 5h = Input (channel) 5 6h = Input (channel) 6 7h = Input (channel) 7 8h = REFN
14-5	RESERVED	R/W	0h	Reserved
4-2	AVERAGING	R/W	0h	Number of samplings to average. 0h = no average 1h = 2 samples average 2h = 4 samples average 3h = 8 samples average 4h = 16 samples average
1-0	MODE	R/W	0h	0h = SW enabled, one-shot 1h = SW enabled, continuous 2h = HW synchronized, one-shot 3h = HW synchronized, continuous

1.16 ADC_STEPDELAY_j Register (Offset = 68h + formula) [reset = 0h]

ADC_STEPDELAY_j is shown in [Figure 1-15](#) and described in [Table 1-32](#).

Return to [Summary Table](#).

Controls number of SMPL_CLK periods to sample and delay.

Offset = 68h + (j × 8h); where j = 0h to Fh

Table 1-31. ADC_STEPDELAY_j Instances

Instance	Physical Address
MCU_ADC0	4020 0000h
MCU_ADC1	4021 0000h

Figure 1-15. ADC_STEPDELAY_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SAMPLEDELAY								RESERVED						OPENDELAY	
R/W-0h								R-0h						R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPENDELAY															
R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-32. ADC_STEPDELAY_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SAMPLEDELAY	R/W	0h	This register will control the number of SMPL_CLK cycles to sample the input signal (hold SOC high). Any value programmed here will be added to the minimum time of 2 SMPL_CLK cycles.
23-18	RESERVED	R	0h	Reserved
17-0	OPENDELAY	R/W	0h	Program the number of SMPL_CLK cycles to wait after applying the step configuration registers and before sending the start of ADC conversion.

1.17 ADC_FIFO0WC Register (Offset = E4h) [reset = 0h]

ADC_FIFO0WC is shown in [Figure 1-16](#) and described in [Table 1-34](#).

Return to [Summary Table](#).

FIFO word count ADC_STATUS

Table 1-33. ADC_FIFO0WC Instances

Instance	Physical Address
MCU_ADC0	4020 00E4h
MCU_ADC1	4021 00E4h

Figure 1-16. ADC_FIFO0WC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																							NUMWDS														
R-0h																							R-0h														

LEGEND: R = Read Only; -n = value after reset

Table 1-34. ADC_FIFO0WC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	NUMWDS	R	0h	Number of words currently in the FIFO0.

1.18 ADC_FIFO0THRESHOLD Register (Offset = E8h) [reset = 0h]

ADC_FIFO0THRESHOLD is shown in [Figure 1-17](#) and described in [Table 1-36](#).

Return to [Summary Table](#).

FIFO threshold

Table 1-35. ADC_FIFO0THRESHOLD Instances

Instance	Physical Address
MCU_ADC0	4020 00E8h
MCU_ADC1	4021 00E8h

Figure 1-17. ADC_FIFO0THRESHOLD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRESHOLD							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-36. ADC_FIFO0THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	THRESHOLD	R/W	0h	Program the desired FIFO0 data sample level minus 1 to reach before generating interrupt to CPU.

1.19 ADC_FIFO0DMAREQ Register (Offset = ECh) [reset = 0h]

ADC_FIFO0DMAREQ is shown in [Figure 1-18](#) and described in [Table 1-38](#).

Return to [Summary Table](#).

DMA request.

Table 1-37. ADC_FIFO0DMAREQ Instances

Instance	Physical Address
MCU_ADC0	4020 00ECh
MCU_ADC1	4021 00ECh

Figure 1-18. ADC_FIFO0DMAREQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DMAREQLEVEL							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-38. ADC_FIFO0DMAREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DMAREQLEVEL	R/W	0h	Number of words in FIFO0 before generating a DMA request.

1.20 ADC_FIFO1WC Register (Offset = F0h) [reset = 0h]

ADC_FIFO1WC is shown in [Figure 1-19](#) and described in [Table 1-40](#).

Return to [Summary Table](#).

FIFO word count ADC_STATUS

Table 1-39. ADC_FIFO1WC Instances

Instance	Physical Address
MCU_ADC0	4020 00F0h
MCU_ADC1	4021 00F0h

Figure 1-19. ADC_FIFO1WC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																							NUMWDS														
R-0h																							R-0h														

LEGEND: R = Read Only; -n = value after reset

Table 1-40. ADC_FIFO1WC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-0	NUMWDS	R	0h	Number of words currently in the FIFO1.

1.21 ADC_FIFO1THRESHOLD Register (Offset = F4h) [reset = 0h]

ADC_FIFO1THRESHOLD is shown in [Figure 1-20](#) and described in [Table 1-42](#).

Return to [Summary Table](#).

FIFO threshold

Table 1-41. ADC_FIFO1THRESHOLD Instances

Instance	Physical Address
MCU_ADC0	4020 00F4h
MCU_ADC1	4021 00F4h

Figure 1-20. ADC_FIFO1THRESHOLD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THRESHOLD							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-42. ADC_FIFO1THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	THRESHOLD	R/W	0h	Program the desired FIFO1 data sample level minus 1 to reach before generating interrupt to CPU.

1.22 ADC_FIFO1DMAREQ Register (Offset = F8h) [reset = 0h]

ADC_FIFO1DMAREQ is shown in [Figure 1-21](#) and described in [Table 1-44](#).

Return to [Summary Table](#).

DMA request.

Table 1-43. ADC_FIFO1DMAREQ Instances

Instance	Physical Address
MCU_ADC0	4020 00F8h
MCU_ADC1	4021 00F8h

Figure 1-21. ADC_FIFO1DMAREQ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DMAREQLEVEL							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-44. ADC_FIFO1DMAREQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DMAREQLEVEL	R/W	0h	Number of words in FIFO1 before generating a DMA request.

1.23 ADC_FIFO0DATA Register (Offset = 100h) [reset = X]

ADC_FIFO0DATA is shown in [Figure 1-22](#) and described in [Table 1-46](#).

Return to [Summary Table](#).

A read from this register will auto increment the FIFO read pointer. If you read when FIFO is empty, it will trigger an underflow interrupt.

Table 1-45. ADC_FIFO0DATA Instances

Instance	Physical Address
MCU_ADC0	4020 0100h
MCU_ADC1	4021 0100h

Figure 1-22. ADC_FIFO0DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ADCCHANLID			
R-0h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					ADCDATA										
R-X					R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 1-46. ADC_FIFO0DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	ADCCHANLID	R	0h	Optional ID tag of input (channel) that captured the data. If tag option is disabled, these bits will be 0.
15-12	RESERVED	R	X	Reserved
11-0	ADCDATA	R	0h	Sampled ADC converted data value stored in FIFO0.

1.24 ADC_FIFO1DATA Register (Offset = 200h) [reset = X]

ADC_FIFO1DATA is shown in [Figure 1-23](#) and described in [Table 1-48](#).

Return to [Summary Table](#).

A read from this register will auto increment the FIFO read pointer. If you read when FIFO is empty, it will trigger an underflow interrupt.

Table 1-47. ADC_FIFO1DATA Instances

Instance	Physical Address
MCU_ADC0	4020 0200h
MCU_ADC1	4021 0200h

Figure 1-23. ADC_FIFO1DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ADCCHANLID			
R-0h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					ADCDATA										
R-X					R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 1-48. ADC_FIFO1DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	ADCCHANLID	R	0h	Optional ID tag of input (channel) that captured the data. If tag option is disabled, these bits will be 0.
15-12	RESERVED	R	X	Reserved
11-0	ADCDATA	R	0h	Sampled ADC converted data value stored in FIFO1.

1.25 ADC FIFO and DMA Registers

Table 1-50 lists the memory-mapped registers for the MCU_ADC12_FIFO_DMA. All register offset addresses not listed in Table 1-50 should be considered as reserved locations and the register contents should not be modified.

Table 1-49. ADC FIFO and DMA Instances

Instance	Base Address
MCU_ADC0_FIFO	4020 8000h
MCU_ADC1_FIFO	4021 8000h

Table 1-50. ADC FIFO and DMA Registers

Offset	Acronym	Register Name	MCU_ADC0_FIFO Physical Address	MCU_ADC1_FIFO Physical Address
100h	ADC_FIFO0DMADATA	MCU_ADC0 Memory Register	4020 8100h	4021 8100h
200h	ADC_FIFO1DMADATA	MCU_ADC1 Memory Register	4020 8200h	4021 8200h

1.26 ADC_FIFO0DMADATA Register (Offset = 100h) [reset = X]

ADC_FIFO0DMADATA is shown in [Figure 1-24](#) and described in [Table 1-52](#).

[Return to Summary Table.](#)

DMA sample FIFO

Table 1-51. ADC_FIFO0DMADATA Instances

Instance	Physical Address
MCU_ADC0_FIFO	4020 8100h
MCU_ADC1_FIFO	4021 8100h

Figure 1-24. ADC_FIFO0DMADATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ADCCHANLID			
R-0h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					ADCDATA										
R-X					R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 1-52. ADC_FIFO0DMADATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	ADCCHANLID	R	0h	Optional ID tag of input (channel) that captured the data. If tag option is disabled, these bits will be 0.
15-12	RESERVED	R	X	Reserved
11-0	ADCDATA	R	0h	Sampled ADC converted data value stored in FIFO0.

1.27 ADC_FIFO1DMADATA Register (Offset = 200h) [reset = X]

ADC_FIFO1DMADATA is shown in [Figure 1-25](#) and described in [Table 1-54](#).

[Return to Summary Table.](#)

DMA sample FIFO

Table 1-53. ADC_FIFO1DMADATA Instances

Instance	Physical Address
MCU_ADC0_FIFO	4020 8200h
MCU_ADC1_FIFO	4021 8200h

Figure 1-25. ADC_FIFO1DMADATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ADCCHANLID			
R-0h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					ADCDATA										
R-X					R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 1-54. ADC_FIFO1DMADATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	ADCCHANLID	R	0h	Optional ID tag of input (channel) that captured the data. If tag option is disabled, these bits will be 0.
15-12	RESERVED	R	X	Reserved
11-0	ADCDATA	R	0h	Sampled ADC converted data value stored in FIFO1.

1.28 ADC ECC Registers

Table 1-56 lists the memory-mapped registers for the ADC ECC. All register offset addresses not listed in Table 1-56 should be considered as reserved locations and the register contents should not be modified.

Table 1-55. ADC ECC Instances

Instance	Base Address
MCU_ADC0_ECC	4070 7000h
MCU_ADC1_ECC	4070 8000h

Table 1-56. ADC ECC Registers

Offset	Acronym	Register Name	MCU_ADC0_ECC Physical Address	MCU_ADC1_ECC Physical Address
0h	ADC_AGGR_REVISION	Aggregator Revision Register	4070 7000h	4070 8000h
8h	ADC_ECC_VECTOR	ECC Vector Register	4070 7008h	4070 8008h
Ch	ADC_MISC_STATUS	Misc Status Register	4070 700Ch	4070 800Ch
10h	ADC_ECC_WRAP_REV	ECC Wrapper Revision Register	4070 7010h	4070 8010h
14h	ADC_ECC_CTRL	ECC Control Register	4070 7014h	4070 8014h
18h	ADC_ECC_ERR_CTRL1	ECC Error Control1 Register	4070 7018h	4070 8018h
1Ch	ADC_ECC_ERR_CTRL2	ECC Error Control2 Register	4070 701Ch	4070 801Ch
20h	ADC_ECC_ERR_STAT1	ECC Error Status1 Register	4070 7020h	4070 8020h
24h	ADC_ECC_ERR_STAT2	ECC Error Status2 Register	4070 7024h	4070 8024h
3Ch	ADC_ECC_SEC_EOI_REG	SEC End of Interrupt Register	4070 703Ch	4070 803Ch
40h	ADC_ECC_SEC_STATUS_REG0	Interrupt Status Register	4070 7040h	4070 8040h
80h	ADC_ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register	4070 7080h	4070 8080h
C0h	ADC_ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register	4070 70C0h	4070 80C0h
13Ch	ADC_ECC_DED_EOI_REG	DED End of Interrupt Register	4070 713Ch	4070 813Ch
140h	ADC_ECC_DED_STATUS_REG0	Interrupt Status Register	4070 7140h	4070 8140h
180h	ADC_ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register	4070 7180h	4070 8180h
1C0h	ADC_ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register	4070 71C0h	4070 81C0h

1.29 ADC_AGGR_REVISION Register (Offset = 0h) [reset = Xh]

ADC_AGGR_REVISION is shown in [Figure 1-26](#) and described in [Table 1-58](#).

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Revision parameters

Reset = 60060B00h

Table 1-57. ADC_AGGR_REVISION Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 7000h
MCU_ADC1_ECC	4070 8000h

Figure 1-26. ADC_AGGR_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME			BU		MODULE_ID										
R-1h			R-2h		R-6h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1h					R-3h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 1-58. ADC_AGGR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6h	Module ID
15-11	REVRTL	R	1h	RTL version
10-8	REVMAJ	R	3h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

1.30 ADC_ECC_VECTOR Register (Offset = 8h) [reset = X]

ADC_ECC_VECTOR is shown in [Figure 1-27](#) and described in [Table 1-60](#).

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ECC Vector Register

Table 1-59. ADC_ECC_VECTOR Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 7008h
MCU_ADC1_ECC	4070 8008h

Figure 1-27. ADC_ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R/W-X							R-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-60. ADC_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	Reserved
24	RD_SVBUS_DONE	R	0h	Status to indicate if read on serial VBUS is complete
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W	0h	Write 1h = Trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	Reserved
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for ADC_CONTROL or ADC_STATUS

1.31 ADC_MISC_STATUS Register (Offset = Ch) [reset = X]

ADC_MISC_STATUS is shown in [Figure 1-28](#) and described in [Table 1-62](#).

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Misc Status

Table 1-61. ADC_MISC_STATUS Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 700Ch
MCU_ADC1_ECC	4070 800Ch

Figure 1-28. ADC_MISC_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	NUM_RAMs														
R-X																	R-2h														

LEGEND: R = Read Only; -n = value after reset

Table 1-62. ADC_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	Reserved
10-0	NUM_RAMs	R	2h	Indicates the number of RAMs serviced by the ECC aggregator

1.32 ADC_ECC_WRAP_REV Register (Offset = 10h) [reset = 60060900h]

ADC_ECC_WRAP_REV is shown in [Figure 1-29](#) and described in [Table 1-64](#).

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Revision parameters

Table 1-63. ADC_ECC_WRAP_REV Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 7010h
MCU_ADC1_ECC	4070 8010h

Figure 1-29. ADC_ECC_WRAP_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 1-64. ADC_ECC_WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6h	Module ID
15-11	REVRTL	R	1h	RTL version
10-8	REVMAJ	R	1h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

1.33 ADC_ECC_CTRL Register (Offset = 14h) [reset = X]

ADC_ECC_CTRL is shown in [Figure 1-30](#) and described in [Table 1-66](#).

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ECC Control Register

Table 1-65. ADC_ECC_CTRL Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 7014h
MCU_ADC1_ECC	4070 8014h

Figure 1-30. ADC_ECC_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-66. ADC_ECC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	Reserved
6	ERROR_ONCE	R/W	0h	Force Error only once
5	FORCE_N_ROW	R/W	0h	Force Error on any RAM read
4	FORCE_DED	R/W	0h	Force Double Bit Error
3	FORCE_SEC	R/W	0h	Force Single Bit Error
2	ENABLE_RMW	R/W	1h	Enable rmw
1	ECC_CHECK	R/W	1h	Enable ECC check
0	ECC_ENABLE	R/W	1h	Enable ECC

1.34 ADC_ECC_ERR_CTRL1 Register (Offset = 18h) [reset = 0h]

ADC_ECC_ERR_CTRL1 is shown in [Figure 1-31](#) and described in [Table 1-68](#).

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ECC Error Control1 Register

Table 1-67. ADC_ECC_ERR_CTRL1 Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 7018h
MCU_ADC1_ECC	4070 8018h

Figure 1-31. ADC_ECC_ERR_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-68. ADC_ECC_ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R/W	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

1.35 ADC_ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ADC_ECC_ERR_CTRL2 is shown in [Figure 1-32](#) and described in [Table 1-70](#).

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ECC Error Control2 Register

Table 1-69. ADC_ECC_ERR_CTRL2 Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 701Ch
MCU_ADC1_ECC	4070 801Ch

Figure 1-32. ADC_ECC_ERR_CTRL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT2																ECC_BIT1															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-70. ADC_ECC_ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT2	R/W	0h	Data bit that needs to be flipped if double bit error needs to be forced
15-0	ECC_BIT1	R/W	0h	Data bit that needs to be flipped when force_sec is set

1.36 ADC_ECC_ERR_STAT1 Register (Offset = 20h) [reset = X]

ADC_ECC_ERR_STAT1 is shown in [Figure 1-33](#) and described in [Table 1-72](#).

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ECC Error Status1 Register

Table 1-71. ADC_ECC_ERR_STAT1 Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 7020h
MCU_ADC1_ECC	4070 8020h

Figure 1-33. ADC_ECC_ERR_STAT1 Register

31	30	29	28	27	26	25	24
ECC_BIT1							
R-0h							
23	22	21	20	19	18	17	16
ECC_BIT1							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					CLR_ECC_OTHER	CLR_ECC_DED	CLR_ECC_SEC
R/W-X					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED					ECC_OTHER	ECC_DED	ECC_SEC
R/W-X					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-72. ADC_ECC_ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT1	R	0h	Data bit that corresponds to the single-bit error
15-11	RESERVED	R/W	X	Reserved
10	CLR_ECC_OTHER	R/W	0h	Clear other Error Status
9	CLR_ECC_DED	R/W	0h	Clear Double Bit Error Status
8	CLR_ECC_SEC	R/W	0h	Clear Single Bit Error Status
7-3	RESERVED	R/W	X	Reserved
2	ECC_OTHER	R/W	0h	Successive single-bit errors have occurred while a writeback is still pending, Level interrupt
1	ECC_DED	R/W	0h	Level Double Bit Error Status
0	ECC_SEC	R/W	0h	Level Single Bit Error Status

1.37 ADC_ECC_ERR_STAT2 Register (Offset = 24h) [reset = 0h]

ADC_ECC_ERR_STAT2 is shown in [Figure 1-34](#) and described in [Table 1-74](#).

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ECC Error Status1 Register

Table 1-73. ADC_ECC_ERR_STAT2 Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 7024h
MCU_ADC1_ECC	4070 8024h

Figure 1-34. ADC_ECC_ERR_STAT2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 1-74. ADC_ECC_ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_ROW	R	0h	Row address where the single or double-bit error has occurred

1.38 ADC_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

ADC_ECC_SEC_EOI_REG is shown in [Figure 1-35](#) and described in [Table 1-76](#).

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ADC_EOI Register

Table 1-75. ADC_ECC_SEC_EOI_REG Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 703Ch
MCU_ADC1_ECC	4070 803Ch

Figure 1-35. ADC_ECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-76. ADC_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	Reserved
0	EOI_WR	R/W	0h	ADC_EOI Register

1.39 ADC_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

ADC_ECC_SEC_STATUS_REG0 is shown in [Figure 1-36](#) and described in [Table 1-78](#).

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Interrupt Status Register 0

**Table 1-77. ADC_ECC_SEC_STATUS_REG0
Instances**

Instance	Physical Address
MCU_ADC0_ECC	4070 7040h
MCU_ADC1_ECC	4070 8040h

Figure 1-36. ADC_ECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RAM1_PEND	RAM0_PEND
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-78. ADC_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	Reserved
1	RAM1_PEND	R/W	0h	Interrupt Pending Status for ram1_pend
0	RAM0_PEND	R/W	0h	Interrupt Pending Status for ram0_pend

1.40 ADC_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

ADC_ECC_SEC_ENABLE_SET_REG0 is shown in [Figure 1-37](#) and described in [Table 1-80](#).

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Interrupt Enable Set Register 0

**Table 1-79. ADC_ECC_SEC_ENABLE_SET_REG0
Instances**

Instance	Physical Address
MCU_ADC0_ECC	4070 7080h
MCU_ADC1_ECC	4070 8080h

Figure 1-37. ADC_ECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RAM1_ENABL E_SET	RAM0_ENABL E_SET
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-80. ADC_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	Reserved
1	RAM1_ENABLE_SET	R/W	0h	Interrupt Enable Set Register for ram1_pend
0	RAM0_ENABLE_SET	R/W	0h	Interrupt Enable Set Register for ram0_pend

1.41 ADC_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

ADC_ECC_SEC_ENABLE_CLR_REG0 is shown in [Figure 1-38](#) and described in [Table 1-82](#).

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Interrupt Enable Clear Register 0

**Table 1-81. ADC_ECC_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
MCU_ADC0_ECC	4070 70C0h
MCU_ADC1_ECC	4070 80C0h

Figure 1-38. ADC_ECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RAM1_ENABL E_CLR	RAM0_ENABL E_CLR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-82. ADC_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	Reserved
1	RAM1_ENABLE_CLR	R/W	0h	Interrupt Enable Clear Register for ram1_pend
0	RAM0_ENABLE_CLR	R/W	0h	Interrupt Enable Clear Register for ram0_pend

1.42 ADC_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

ADC_ECC_DED_EOI_REG is shown in [Figure 1-39](#) and described in [Table 1-84](#).

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ADC_EOI Register

Table 1-83. ADC_ECC_DED_EOI_REG Instances

Instance	Physical Address
MCU_ADC0_ECC	4070 713Ch
MCU_ADC1_ECC	4070 813Ch

Figure 1-39. ADC_ECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-84. ADC_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	Reserved
0	EOI_WR	R/W	0h	ADC_EOI Register

1.43 ADC_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

ADC_ECC_DED_STATUS_REG0 is shown in [Figure 1-40](#) and described in [Table 1-86](#).

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Interrupt Status Register 0

**Table 1-85. ADC_ECC_DED_STATUS_REG0
Instances**

Instance	Physical Address
MCU_ADC0_ECC	4070 7140h
MCU_ADC1_ECC	4070 8140h

Figure 1-40. ADC_ECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RAM1_PEND	RAM0_PEND
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-86. ADC_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	Reserved
1	RAM1_PEND	R/W	0h	Interrupt Pending Status for ram1_pend
0	RAM0_PEND	R/W	0h	Interrupt Pending Status for ram0_pend

1.44 ADC_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

ADC_ECC_DED_ENABLE_SET_REG0 is shown in [Figure 1-41](#) and described in [Table 1-88](#).

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Interrupt Enable Set Register 0

**Table 1-87. ADC_ECC_DED_ENABLE_SET_REG0
Instances**

Instance	Physical Address
MCU_ADC0_ECC	4070 7180h
MCU_ADC1_ECC	4070 8180h

Figure 1-41. ADC_ECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RAM1_ENABL E_SET	RAM0_ENABL E_SET
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-88. ADC_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	Reserved
1	RAM1_ENABLE_SET	R/W	0h	Interrupt Enable Set Register for ram1_pend
0	RAM0_ENABLE_SET	R/W	0h	Interrupt Enable Set Register for ram0_pend

1.45 ADC_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

ADC_ECC_DED_ENABLE_CLR_REG0 is shown in [Figure 1-42](#) and described in [Table 1-90](#).

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Interrupt Enable Clear Register 0

**Table 1-89. ADC_ECC_DED_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
MCU_ADC0_ECC	4070 71C0h
MCU_ADC1_ECC	4070 81C0h

Figure 1-42. ADC_ECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RAM1_ENABL E_CLR	RAM0_ENABL E_CLR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-90. ADC_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	Reserved
1	RAM1_ENABLE_CLR	R/W	0h	Interrupt Enable Clear Register for ram1_pend
0	RAM0_ENABLE_CLR	R/W	0h	Interrupt Enable Clear Register for ram0_pend

2 GPIO Registers

Table 2-2 lists the memory-mapped registers for the GPIO registers. All register offset addresses not listed in Table 2-2 should be considered as reserved locations and the register contents should not be modified.

Table 2-1. GPIO Instances

Instance	Base Address
GPIO0	0060 0000h
GPIO1	0060 1000h
GPIO2	0061 0000h
GPIO3	0061 1000h
GPIO4	0062 0000h
GPIO5	0062 1000h
GPIO6	0063 0000h
GPIO7	0068 0000h
WKUP_GPIO1	4210 0000h
WKUP_GPIO0	4211 0000h

Table 2-2. GPIO Registers

Offset	Acronym	Register Name	GPIO0 Physical Address	GPIO2 Physical Address
0h	GPIO_PID		0060 0000h	0061 0000h
4h	GPIO_PCR		0060 0004h	0061 0004h
8h	GPIO_BINTEN		0060 0008h	0061 0008h
10h	GPIO_DIR01		0060 0010h	0061 0010h
14h	GPIO_OUT_DATA01		0060 0014h	0061 0014h
18h	GPIO_SET_DATA01		0060 0018h	0061 0018h
1Ch	GPIO_CLR_DATA01		0060 001Ch	0061 001Ch
20h	GPIO_IN_DATA01		0060 0020h	0061 0020h
24h	GPIO_SET_RIS_TRIG01		0060 0024h	0061 0024h
28h	GPIO_CLR_RIS_TRIG01		0060 0028h	0061 0028h
2Ch	GPIO_SET_FAL_TRIG01		0060 002Ch	0061 002Ch
30h	GPIO_CLR_FAL_TRIG01		0060 0030h	0061 0030h
34h	GPIO_INTSTAT01		0060 0034h	0061 0034h
38h	GPIO_DIR23		0060 0038h	0061 0038h
3Ch	GPIO_OUT_DATA23		0060 003Ch	0061 003Ch
40h	GPIO_SET_DATA23		0060 0040h	0061 0040h
44h	GPIO_CLR_DATA23		0060 0044h	0061 0044h
48h	GPIO_IN_DATA23		0060 0048h	0061 0048h
4Ch	GPIO_SET_RIS_TRIG23		0060 004Ch	0061 004Ch
50h	GPIO_CLR_RIS_TRIG23		0060 0050h	0061 0050h
54h	GPIO_SET_FAL_TRIG23		0060 0054h	0061 0054h
58h	GPIO_CLR_FAL_TRIG23		0060 0058h	0061 0058h
5Ch	GPIO_INTSTAT23		0060 005Ch	0061 005Ch
60h	GPIO_DIR45		0060 0060h	0061 0060h
64h	GPIO_OUT_DATA45		0060 0064h	0061 0064h
68h	GPIO_SET_DATA45		0060 0068h	0061 0068h
6Ch	GPIO_CLR_DATA45		0060 006Ch	0061 006Ch
70h	GPIO_IN_DATA45		0060 0070h	0061 0070h
74h	GPIO_SET_RIS_TRIG45		0060 0074h	0061 0074h
78h	GPIO_CLR_RIS_TRIG45		0060 0078h	0061 0078h

Table 2-2. GPIO Registers (continued)

Offset	Acronym	Register Name	GPIO0 Physical Address	GPIO2 Physical Address
7Ch	GPIO_SET_FAL_TRIG45		0060 007Ch	0061 007Ch
80h	GPIO_CLR_FAL_TRIG45		0060 0080h	0061 0080h
84h	GPIO_INTSTAT45		0060 0084h	0061 0084h
88h	GPIO_DIR67		0060 0088h	0061 0088h
8Ch	GPIO_OUT_DATA67		0060 008Ch	0061 008Ch
90h	GPIO_SET_DATA67		0060 0090h	0061 0090h
94h	GPIO_CLR_DATA67		0060 0094h	0061 0094h
98h	GPIO_IN_DATA67		0060 0098h	0061 0098h
9Ch	GPIO_SET_RIS_TRIG67		0060 009Ch	0061 009Ch
A0h	GPIO_CLR_RIS_TRIG67		0060 00A0h	0061 00A0h
A4h	GPIO_SET_FAL_TRIG67		0060 00A4h	0061 00A4h
A8h	GPIO_CLR_FAL_TRIG67		0060 00A8h	0061 00A8h
ACh	GPIO_INTSTAT67		0060 00ACh	0061 00ACh
B0h	GPIO_DIR8		0060 00B0h	0061 00B0h
B4h	GPIO_OUT_DATA8		0060 00B4h	0061 00B4h
B8h	GPIO_SET_DATA8		0060 00B8h	0061 00B8h
BCh	GPIO_CLR_DATA8		0060 00BCh	0061 00BCh
C0h	GPIO_IN_DATA8		0060 00C0h	0061 00C0h
C4h	GPIO_SET_RIS_TRIG8		0060 00C4h	0061 00C4h
C8h	GPIO_CLR_RIS_TRIG8		0060 00C8h	0061 00C8h
CCh	GPIO_SET_FAL_TRIG8		0060 00CCh	0061 00CCh
D0h	GPIO_CLR_FAL_TRIG8		0060 00D0h	0061 00D0h
D4h	GPIO_INTSTAT8		0060 00D4h	0061 00D4h

Table 2-3. GPIO Registers

Offset	Acronym	Register Name	GPIO1 Physical Address	GPIO3 Physical Address
0h	GPIO_PID		0060 1000h	0061 1000h
4h	GPIO_PCR		0060 1004h	0061 1004h
8h	GPIO_BINTEN		0060 1008h	0061 1008h
10h	GPIO_DIR01		0060 1010h	0061 1010h
14h	GPIO_OUT_DATA01		0060 1014h	0061 1014h
18h	GPIO_SET_DATA01		0060 1018h	0061 1018h
1Ch	GPIO_CLR_DATA01		0060 101Ch	0061 101Ch
20h	GPIO_IN_DATA01		0060 1020h	0061 1020h
24h	GPIO_SET_RIS_TRIG01		0060 1024h	0061 1024h
28h	GPIO_CLR_RIS_TRIG01		0060 1028h	0061 1028h
2Ch	GPIO_SET_FAL_TRIG01		0060 102Ch	0061 102Ch
30h	GPIO_CLR_FAL_TRIG01		0060 1030h	0061 1030h
34h	GPIO_INTSTAT01		0060 1034h	0061 1034h
38h	GPIO_DIR23		0060 1038h	0061 1038h
3Ch	GPIO_OUT_DATA23		0060 103Ch	0061 103Ch
40h	GPIO_SET_DATA23		0060 1040h	0061 1040h
44h	GPIO_CLR_DATA23		0060 1044h	0061 1044h
48h	GPIO_IN_DATA23		0060 1048h	0061 1048h
4Ch	GPIO_SET_RIS_TRIG23		0060 104Ch	0061 104Ch
50h	GPIO_CLR_RIS_TRIG23		0060 1050h	0061 1050h
54h	GPIO_SET_FAL_TRIG23		0060 1054h	0061 1054h

Table 2-3. GPIO Registers (continued)

Offset	Acronym	Register Name	GPIO1 Physical Address	GPIO3 Physical Address
58h	GPIO_CLR_FAL_TRIG23		0060 1058h	0061 1058h
5Ch	GPIO_INTSTAT23		0060 105Ch	0061 105Ch
60h	GPIO_DIR45		0060 1060h	0061 1060h
64h	GPIO_OUT_DATA45		0060 1064h	0061 1064h
68h	GPIO_SET_DATA45		0060 1068h	0061 1068h
6Ch	GPIO_CLR_DATA45		0060 106Ch	0061 106Ch
70h	GPIO_IN_DATA45		0060 1070h	0061 1070h
74h	GPIO_SET_RIS_TRIG45		0060 1074h	0061 1074h
78h	GPIO_CLR_RIS_TRIG45		0060 1078h	0061 1078h
7Ch	GPIO_SET_FAL_TRIG45		0060 107Ch	0061 107Ch
80h	GPIO_CLR_FAL_TRIG45		0060 1080h	0061 1080h
84h	GPIO_INTSTAT45		0060 1084h	0061 1084h
88h	GPIO_DIR67		0060 1088h	0061 1088h
8Ch	GPIO_OUT_DATA67		0060 108Ch	0061 108Ch
90h	GPIO_SET_DATA67		0060 1090h	0061 1090h
94h	GPIO_CLR_DATA67		0060 1094h	0061 1094h
98h	GPIO_IN_DATA67		0060 1098h	0061 1098h
9Ch	GPIO_SET_RIS_TRIG67		0060 109Ch	0061 109Ch
A0h	GPIO_CLR_RIS_TRIG67		0060 10A0h	0061 10A0h
A4h	GPIO_SET_FAL_TRIG67		0060 10A4h	0061 10A4h
A8h	GPIO_CLR_FAL_TRIG67		0060 10A8h	0061 10A8h
ACH	GPIO_INTSTAT67		0060 10ACH	0061 10ACH
B0h	GPIO_DIR8		0060 10B0h	0061 10B0h
B4h	GPIO_OUT_DATA8		0060 10B4h	0061 10B4h
B8h	GPIO_SET_DATA8		0060 10B8h	0061 10B8h
BCh	GPIO_CLR_DATA8		0060 10BCh	0061 10BCh
C0h	GPIO_IN_DATA8		0060 10C0h	0061 10C0h
C4h	GPIO_SET_RIS_TRIG8		0060 10C4h	0061 10C4h
C8h	GPIO_CLR_RIS_TRIG8		0060 10C8h	0061 10C8h
CCh	GPIO_SET_FAL_TRIG8		0060 10CCh	0061 10CCh
D0h	GPIO_CLR_FAL_TRIG8		0060 10D0h	0061 10D0h
D4h	GPIO_INTSTAT8		0060 10D4h	0061 10D4h

Table 2-4. GPIO Registers

Offset	Acronym	Register Name	GPIO4 Physical Address	GPIO6 Physical Address
0h	GPIO_PID		0062 0000h	0063 0000h
4h	GPIO_PCR		0062 0004h	0063 0004h
8h	GPIO_BINTEN		0062 0008h	0063 0008h
10h	GPIO_DIR01		0062 0010h	0063 0010h
14h	GPIO_OUT_DATA01		0062 0014h	0063 0014h
18h	GPIO_SET_DATA01		0062 0018h	0063 0018h
1Ch	GPIO_CLR_DATA01		0062 001Ch	0063 001Ch
20h	GPIO_IN_DATA01		0062 0020h	0063 0020h
24h	GPIO_SET_RIS_TRIG01		0062 0024h	0063 0024h
28h	GPIO_CLR_RIS_TRIG01		0062 0028h	0063 0028h
2Ch	GPIO_SET_FAL_TRIG01		0062 002Ch	0063 002Ch

Table 2-4. GPIO Registers (continued)

Offset	Acronym	Register Name	GPIO4 Physical Address	GPIO6 Physical Address
30h	GPIO_CLR_FAL_TRIG01		0062 0030h	0063 0030h
34h	GPIO_INTSTAT01		0062 0034h	0063 0034h
38h	GPIO_DIR23		0062 0038h	0063 0038h
3Ch	GPIO_OUT_DATA23		0062 003Ch	0063 003Ch
40h	GPIO_SET_DATA23		0062 0040h	0063 0040h
44h	GPIO_CLR_DATA23		0062 0044h	0063 0044h
48h	GPIO_IN_DATA23		0062 0048h	0063 0048h
4Ch	GPIO_SET_RIS_TRIG23		0062 004Ch	0063 004Ch
50h	GPIO_CLR_RIS_TRIG23		0062 0050h	0063 0050h
54h	GPIO_SET_FAL_TRIG23		0062 0054h	0063 0054h
58h	GPIO_CLR_FAL_TRIG23		0062 0058h	0063 0058h
5Ch	GPIO_INTSTAT23		0062 005Ch	0063 005Ch
60h	GPIO_DIR45		0062 0060h	0063 0060h
64h	GPIO_OUT_DATA45		0062 0064h	0063 0064h
68h	GPIO_SET_DATA45		0062 0068h	0063 0068h
6Ch	GPIO_CLR_DATA45		0062 006Ch	0063 006Ch
70h	GPIO_IN_DATA45		0062 0070h	0063 0070h
74h	GPIO_SET_RIS_TRIG45		0062 0074h	0063 0074h
78h	GPIO_CLR_RIS_TRIG45		0062 0078h	0063 0078h
7Ch	GPIO_SET_FAL_TRIG45		0062 007Ch	0063 007Ch
80h	GPIO_CLR_FAL_TRIG45		0062 0080h	0063 0080h
84h	GPIO_INTSTAT45		0062 0084h	0063 0084h
88h	GPIO_DIR67		0062 0088h	0063 0088h
8Ch	GPIO_OUT_DATA67		0062 008Ch	0063 008Ch
90h	GPIO_SET_DATA67		0062 0090h	0063 0090h
94h	GPIO_CLR_DATA67		0062 0094h	0063 0094h
98h	GPIO_IN_DATA67		0062 0098h	0063 0098h
9Ch	GPIO_SET_RIS_TRIG67		0062 009Ch	0063 009Ch
A0h	GPIO_CLR_RIS_TRIG67		0062 00A0h	0063 00A0h
A4h	GPIO_SET_FAL_TRIG67		0062 00A4h	0063 00A4h
A8h	GPIO_CLR_FAL_TRIG67		0062 00A8h	0063 00A8h
ACh	GPIO_INTSTAT67		0062 00ACh	0063 00ACh
B0h	GPIO_DIR8		0062 00B0h	0063 00B0h
B4h	GPIO_OUT_DATA8		0062 00B4h	0063 00B4h
B8h	GPIO_SET_DATA8		0062 00B8h	0063 00B8h
BCh	GPIO_CLR_DATA8		0062 00BCh	0063 00BCh
C0h	GPIO_IN_DATA8		0062 00C0h	0063 00C0h
C4h	GPIO_SET_RIS_TRIG8		0062 00C4h	0063 00C4h
C8h	GPIO_CLR_RIS_TRIG8		0062 00C8h	0063 00C8h
CCh	GPIO_SET_FAL_TRIG8		0062 00CCh	0063 00CCh
D0h	GPIO_CLR_FAL_TRIG8		0062 00D0h	0063 00D0h
D4h	GPIO_INTSTAT8		0062 00D4h	0063 00D4h

Table 2-5. GPIO Registers

Offset	Acronym	Register Name	GPIO5 Physical Address	GPIO7 Physical Address
0h	GPIO_PID		0062 1000h	0068 0000h

Table 2-5. GPIO Registers (continued)

Offset	Acronym	Register Name	GPIO5 Physical Address	GPIO7 Physical Address
4h	GPIO_PCR		0062 1004h	0068 0004h
8h	GPIO_BINTEN		0062 1008h	0068 0008h
10h	GPIO_DIR01		0062 1010h	0068 0010h
14h	GPIO_OUT_DATA01		0062 1014h	0068 0014h
18h	GPIO_SET_DATA01		0062 1018h	0068 0018h
1Ch	GPIO_CLR_DATA01		0062 101Ch	0068 001Ch
20h	GPIO_IN_DATA01		0062 1020h	0068 0020h
24h	GPIO_SET_RIS_TRIG01		0062 1024h	0068 0024h
28h	GPIO_CLR_RIS_TRIG01		0062 1028h	0068 0028h
2Ch	GPIO_SET_FAL_TRIG01		0062 102Ch	0068 002Ch
30h	GPIO_CLR_FAL_TRIG01		0062 1030h	0068 0030h
34h	GPIO_INTSTAT01		0062 1034h	0068 0034h
38h	GPIO_DIR23		0062 1038h	0068 0038h
3Ch	GPIO_OUT_DATA23		0062 103Ch	0068 003Ch
40h	GPIO_SET_DATA23		0062 1040h	0068 0040h
44h	GPIO_CLR_DATA23		0062 1044h	0068 0044h
48h	GPIO_IN_DATA23		0062 1048h	0068 0048h
4Ch	GPIO_SET_RIS_TRIG23		0062 104Ch	0068 004Ch
50h	GPIO_CLR_RIS_TRIG23		0062 1050h	0068 0050h
54h	GPIO_SET_FAL_TRIG23		0062 1054h	0068 0054h
58h	GPIO_CLR_FAL_TRIG23		0062 1058h	0068 0058h
5Ch	GPIO_INTSTAT23		0062 105Ch	0068 005Ch
60h	GPIO_DIR45		0062 1060h	0068 0060h
64h	GPIO_OUT_DATA45		0062 1064h	0068 0064h
68h	GPIO_SET_DATA45		0062 1068h	0068 0068h
6Ch	GPIO_CLR_DATA45		0062 106Ch	0068 006Ch
70h	GPIO_IN_DATA45		0062 1070h	0068 0070h
74h	GPIO_SET_RIS_TRIG45		0062 1074h	0068 0074h
78h	GPIO_CLR_RIS_TRIG45		0062 1078h	0068 0078h
7Ch	GPIO_SET_FAL_TRIG45		0062 107Ch	0068 007Ch
80h	GPIO_CLR_FAL_TRIG45		0062 1080h	0068 0080h
84h	GPIO_INTSTAT45		0062 1084h	0068 0084h
88h	GPIO_DIR67		0062 1088h	0068 0088h
8Ch	GPIO_OUT_DATA67		0062 108Ch	0068 008Ch
90h	GPIO_SET_DATA67		0062 1090h	0068 0090h
94h	GPIO_CLR_DATA67		0062 1094h	0068 0094h
98h	GPIO_IN_DATA67		0062 1098h	0068 0098h
9Ch	GPIO_SET_RIS_TRIG67		0062 109Ch	0068 009Ch
A0h	GPIO_CLR_RIS_TRIG67		0062 10A0h	0068 00A0h
A4h	GPIO_SET_FAL_TRIG67		0062 10A4h	0068 00A4h
A8h	GPIO_CLR_FAL_TRIG67		0062 10A8h	0068 00A8h
ACH	GPIO_INTSTAT67		0062 10ACH	0068 00ACH
B0h	GPIO_DIR8		0062 10B0h	0068 00B0h
B4h	GPIO_OUT_DATA8		0062 10B4h	0068 00B4h
B8h	GPIO_SET_DATA8		0062 10B8h	0068 00B8h
BCh	GPIO_CLR_DATA8		0062 10BCh	0068 00BCh

Table 2-5. GPIO Registers (continued)

Offset	Acronym	Register Name	GPIO5 Physical Address	GPIO7 Physical Address
C0h	GPIO_IN_DATA8		0062 10C0h	0068 00C0h
C4h	GPIO_SET_RIS_TRIG8		0062 10C4h	0068 00C4h
C8h	GPIO_CLR_RIS_TRIG8		0062 10C8h	0068 00C8h
CCh	GPIO_SET_FAL_TRIG8		0062 10CCh	0068 00CCh
D0h	GPIO_CLR_FAL_TRIG8		0062 10D0h	0068 00D0h
D4h	GPIO_INTSTAT8		0062 10D4h	0068 00D4h

Table 2-6. GPIO Registers

Offset	Acronym	Register Name	WKUP_GPIO0 Physical Address	WKUP_GPIO1 Physical Address
0h	GPIO_PID		4211 0000h	4210 0000h
4h	GPIO_PCR		4211 0004h	4210 0004h
8h	GPIO_BINTEN		4211 0008h	4210 0008h
10h	GPIO_DIR01		4211 0010h	4210 0010h
14h	GPIO_OUT_DATA01		4211 0014h	4210 0014h
18h	GPIO_SET_DATA01		4211 0018h	4210 0018h
1Ch	GPIO_CLR_DATA01		4211 001Ch	4210 001Ch
20h	GPIO_IN_DATA01		4211 0020h	4210 0020h
24h	GPIO_SET_RIS_TRIG01		4211 0024h	4210 0024h
28h	GPIO_CLR_RIS_TRIG01		4211 0028h	4210 0028h
2Ch	GPIO_SET_FAL_TRIG01		4211 002Ch	4210 002Ch
30h	GPIO_CLR_FAL_TRIG01		4211 0030h	4210 0030h
34h	GPIO_INTSTAT01		4211 0034h	4210 0034h
38h	GPIO_DIR23		4211 0038h	4210 0038h
3Ch	GPIO_OUT_DATA23		4211 003Ch	4210 003Ch
40h	GPIO_SET_DATA23		4211 0040h	4210 0040h
44h	GPIO_CLR_DATA23		4211 0044h	4210 0044h
48h	GPIO_IN_DATA23		4211 0048h	4210 0048h
4Ch	GPIO_SET_RIS_TRIG23		4211 004Ch	4210 004Ch
50h	GPIO_CLR_RIS_TRIG23		4211 0050h	4210 0050h
54h	GPIO_SET_FAL_TRIG23		4211 0054h	4210 0054h
58h	GPIO_CLR_FAL_TRIG23		4211 0058h	4210 0058h
5Ch	GPIO_INTSTAT23		4211 005Ch	4210 005Ch
60h	GPIO_DIR45		4211 0060h	4210 0060h
64h	GPIO_OUT_DATA45		4211 0064h	4210 0064h
68h	GPIO_SET_DATA45		4211 0068h	4210 0068h
6Ch	GPIO_CLR_DATA45		4211 006Ch	4210 006Ch
70h	GPIO_IN_DATA45		4211 0070h	4210 0070h
74h	GPIO_SET_RIS_TRIG45		4211 0074h	4210 0074h
78h	GPIO_CLR_RIS_TRIG45		4211 0078h	4210 0078h
7Ch	GPIO_SET_FAL_TRIG45		4211 007Ch	4210 007Ch
80h	GPIO_CLR_FAL_TRIG45		4211 0080h	4210 0080h
84h	GPIO_INTSTAT45		4211 0084h	4210 0084h
88h	GPIO_DIR67		4211 0088h	4210 0088h
8Ch	GPIO_OUT_DATA67		4211 008Ch	4210 008Ch
90h	GPIO_SET_DATA67		4211 0090h	4210 0090h
94h	GPIO_CLR_DATA67		4211 0094h	4210 0094h

Table 2-6. GPIO Registers (continued)

Offset	Acronym	Register Name	WKUP_GPIO0 Physical Address	WKUP_GPIO1 Physical Address
98h	GPIO_IN_DATA67		4211 0098h	4210 0098h
9Ch	GPIO_SET_RIS_TRIG67		4211 009Ch	4210 009Ch
A0h	GPIO_CLR_RIS_TRIG67		4211 00A0h	4210 00A0h
A4h	GPIO_SET_FAL_TRIG67		4211 00A4h	4210 00A4h
A8h	GPIO_CLR_FAL_TRIG67		4211 00A8h	4210 00A8h
ACH	GPIO_INTSTAT67		4211 00ACH	4210 00ACH
B0h	GPIO_DIR8		4211 00B0h	4210 00B0h
B4h	GPIO_OUT_DATA8		4211 00B4h	4210 00B4h
B8h	GPIO_SET_DATA8		4211 00B8h	4210 00B8h
BCh	GPIO_CLR_DATA8		4211 00BCh	4210 00BCh
C0h	GPIO_IN_DATA8		4211 00C0h	4210 00C0h
C4h	GPIO_SET_RIS_TRIG8		4211 00C4h	4210 00C4h
C8h	GPIO_CLR_RIS_TRIG8		4211 00C8h	4210 00C8h
CCh	GPIO_SET_FAL_TRIG8		4211 00CCh	4210 00CCh
D0h	GPIO_CLR_FAL_TRIG8		4211 00D0h	4210 00D0h
D4h	GPIO_INTSTAT8		4211 00D4h	4210 00D4h

2.1 GPIO_PID Register (Offset = 0h) [reset = 44832905h]

GPIO_PID is shown in [Figure 2-1](#) and described in [Table 2-8](#).

Return to [Summary Table](#).

GPIO Peripheral ID Register

Table 2-7. GPIO_PID Instances

Instance	Physical Address
GPIO0	0060 0000h
GPIO1	0060 1000h
GPIO2	0061 0000h
GPIO3	0061 1000h
GPIO4	0062 0000h
GPIO5	0062 1000h
GPIO6	0063 0000h
GPIO7	0068 0000h
WKUP_GPIO1	4210 0000h
WKUP_GPIO0	4211 0000h

Figure 2-1. GPIO_PID Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R-1h		R-0h		R-483h			
23	22	21	20	19	18	17	16
FUNC							
R-483h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R-5h					R-1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R-0h				R-5h			

LEGEND: R = Read Only; -n = value after reset

Table 2-8. GPIO_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Current scheme
29-28	RESERVED	R	0h	RESERVED
27-16	FUNC	R	483h	Function code assigned to TCP3
15-11	RTL	R	5h	RTL Version R code
10-8	MAJOR	R	1h	Major revision X code
7-6	CUSTOM	R	0h	Custom version code
5-0	MINOR	R	5h	Minor revision Y code

2.2 GPIO_PCR Register (Offset = 4h) [reset = X]

GPIO_PCR is shown in [Figure 2-2](#) and described in [Table 2-10](#).

[Return to Summary Table.](#)

Peripheral Control Register

Table 2-9. GPIO_PCR Instances

Instance	Physical Address
GPIO0	0060 0004h
GPIO1	0060 1004h
GPIO2	0061 0004h
GPIO3	0061 1004h
GPIO4	0062 0004h
GPIO5	0062 1004h
GPIO6	0063 0004h
GPIO7	0068 0004h
WKUP_GPIO1	4210 0004h
WKUP_GPIO0	4211 0004h

Figure 2-2. GPIO_PCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R-X						R-0h	R-1h

LEGEND: R = Read Only; -n = value after reset

Table 2-10. GPIO_PCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	SOFT	R	0h	Used in conjunction with FREE bit to determine the emulation suspend mode
0	FREE	R	1h	For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend

2.3 GPIO_BINTEN Register (Offset = 8h) [reset = 0h]

GPIO_BINTEN is shown in [Figure 2-3](#) and described in [Table 2-12](#).

Return to [Summary Table](#).

Bit Interrupt Enable Register

Table 2-11. GPIO_BINTEN Instances

Instance	Physical Address
GPIO0	0060 0008h
GPIO1	0060 1008h
GPIO2	0061 0008h
GPIO3	0061 1008h
GPIO4	0062 0008h
GPIO5	0062 1008h
GPIO6	0063 0008h
GPIO7	0068 0008h
WKUP_GPIO1	4210 0008h
WKUP_GPIO0	4211 0008h

Figure 2-3. GPIO_BINTEN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EN															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-12. GPIO_BINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	RESERVED
15-0	EN	R/W	0h	Per bank interrupt enable 0 = disable, 1 = enable

2.4 GPIO_DIR01 Register (Offset = 10h) [reset = FFFFFFFFh]

GPIO_DIR01 is shown in [Figure 2-4](#) and described in [Table 2-14](#).

Return to [Summary Table](#).

Direction Register

Table 2-13. GPIO_DIR01 Instances

Instance	Physical Address
GPIO0	0060 0010h
GPIO1	0060 1010h
GPIO2	0061 0010h
GPIO3	0061 1010h
GPIO4	0062 0010h
GPIO5	0062 1010h
GPIO6	0063 0010h
GPIO7	0068 0010h
WKUP_GPIO1	4210 0010h
WKUP_GPIO0	4211 0010h

Figure 2-4. GPIO_DIR01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR1																DIR0															
R/W-FFFFh																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-14. GPIO_DIR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DIR1	R/W	FFFFh	Direction of GPIO bank 1 bits, 0 = output, 1 = input
15-0	DIR0	R/W	FFFFh	Direction of GPIO bank 0 bits, 0 = output, 1 = input

2.5 GPIO_OUT_DATA01 Register (Offset = 14h) [reset = 0h]

GPIO_OUT_DATA01 is shown in [Figure 2-5](#) and described in [Table 2-16](#).

Return to [Summary Table](#).

Output Drive State Register

Table 2-15. GPIO_OUT_DATA01 Instances

Instance	Physical Address
GPIO0	0060 0014h
GPIO1	0060 1014h
GPIO2	0061 0014h
GPIO3	0061 1014h
GPIO4	0062 0014h
GPIO5	0062 1014h
GPIO6	0063 0014h
GPIO7	0068 0014h
WKUP_GPIO1	4210 0014h
WKUP_GPIO0	4211 0014h

Figure 2-5. GPIO_OUT_DATA01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT1																OUT0															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-16. GPIO_OUT_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OUT1	R/W	0h	Output drive state of GPIO bank 1 bits, does not affect operation when it is configured as input Reading it returns the output drive state
15-0	OUT0	R/W	0h	Output drive state of GPIO bank 0 bits, does not affect operation when it is configured as input Reading it returns the output drive state

2.6 GPIO_SET_DATA01 Register (Offset = 18h) [reset = 0h]

GPIO_SET_DATA01 is shown in [Figure 2-6](#) and described in [Table 2-18](#).

Return to [Summary Table](#).

Set Output Drive State Register

Table 2-17. GPIO_SET_DATA01 Instances

Instance	Physical Address
GPIO0	0060 0018h
GPIO1	0060 1018h
GPIO2	0061 0018h
GPIO3	0061 1018h
GPIO4	0062 0018h
GPIO5	0062 1018h
GPIO6	0063 0018h
GPIO7	0068 0018h
WKUP_GPIO1	4210 0018h
WKUP_GPIO0	4211 0018h

Figure 2-6. GPIO_SET_DATA01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET1																SET0															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-18. GPIO_SET_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SET1	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 1 bits Reading it returns the output drive state
15-0	SET0	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 0 bits Reading it returns the output drive state

2.7 GPIO_CLR_DATA01 Register (Offset = 1Ch) [reset = 0h]

GPIO_CLR_DATA01 is shown in [Figure 2-7](#) and described in [Table 2-20](#).

Return to [Summary Table](#).

Clear Output Drive State Register

Table 2-19. GPIO_CLR_DATA01 Instances

Instance	Physical Address
GPIO0	0060 001Ch
GPIO1	0060 101Ch
GPIO2	0061 001Ch
GPIO3	0061 101Ch
GPIO4	0062 001Ch
GPIO5	0062 101Ch
GPIO6	0063 001Ch
GPIO7	0068 001Ch
WKUP_GPIO1	4210 001Ch
WKUP_GPIO0	4211 001Ch

Figure 2-7. GPIO_CLR_DATA01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR1																CLR0															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-20. GPIO_CLR_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLR1	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state
15-0	CLR0	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state

2.8 GPIO_IN_DATA01 Register (Offset = 20h) [reset = 0h]

GPIO_IN_DATA01 is shown in [Figure 2-8](#) and described in [Table 2-22](#).

Return to [Summary Table](#).

Bank Status Register

Table 2-21. GPIO_IN_DATA01 Instances

Instance	Physical Address
GPIO0	0060 0020h
GPIO1	0060 1020h
GPIO2	0061 0020h
GPIO3	0061 1020h
GPIO4	0062 0020h
GPIO5	0062 1020h
GPIO6	0063 0020h
GPIO7	0068 0020h
WKUP_GPIO1	4210 0020h
WKUP_GPIO0	4211 0020h

Figure 2-8. GPIO_IN_DATA01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN1																IN0															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 2-22. GPIO_IN_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	IN1	R	0h	Status of GPIO bank 1 bits
15-0	IN0	R	0h	Status of GPIO bank 0 bits

2.9 GPIO_SET_RIS_TRIG01 Register (Offset = 24h) [reset = 0h]

GPIO_SET_RIS_TRIG01 is shown in [Figure 2-9](#) and described in [Table 2-24](#).

[Return to Summary Table.](#)

Set Rising Edge Detection Register

Table 2-23. GPIO_SET_RIS_TRIG01 Instances

Instance	Physical Address
GPIO0	0060 0024h
GPIO1	0060 1024h
GPIO2	0061 0024h
GPIO3	0061 1024h
GPIO4	0062 0024h
GPIO5	0062 1024h
GPIO6	0063 0024h
GPIO7	0068 0024h
WKUP_GPIO1	4210 0024h
WKUP_GPIO0	4211 0024h

Figure 2-9. GPIO_SET_RIS_TRIG01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS1																SETRIS0															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-24. GPIO_SET_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SETRIS1	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 1 bits
15-0	SETRIS0	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 0 bits

2.10 GPIO_CLR_RIS_TRIG01 Register (Offset = 28h) [reset = 0h]

GPIO_CLR_RIS_TRIG01 is shown in [Figure 2-10](#) and described in [Table 2-26](#).

Return to [Summary Table](#).

Clear Rising Edge Detection Register

Table 2-25. GPIO_CLR_RIS_TRIG01 Instances

Instance	Physical Address
GPIO0	0060 0028h
GPIO1	0060 1028h
GPIO2	0061 0028h
GPIO3	0061 1028h
GPIO4	0062 0028h
GPIO5	0062 1028h
GPIO6	0063 0028h
GPIO7	0068 0028h
WKUP_GPIO1	4210 0028h
WKUP_GPIO0	4211 0028h

Figure 2-10. GPIO_CLR_RIS_TRIG01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS1																CLRRIS0															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-26. GPIO_CLR_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLRRIS1	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 1 bits
15-0	CLRRIS0	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 0 bits

2.11 GPIO_SET_FAL_TRIG01 Register (Offset = 2Ch) [reset = 0h]

GPIO_SET_FAL_TRIG01 is shown in [Figure 2-11](#) and described in [Table 2-28](#).

Return to [Summary Table](#).

Set Falling Edge Detection Register

Table 2-27. GPIO_SET_FAL_TRIG01 Instances

Instance	Physical Address
GPIO0	0060 002Ch
GPIO1	0060 102Ch
GPIO2	0061 002Ch
GPIO3	0061 102Ch
GPIO4	0062 002Ch
GPIO5	0062 102Ch
GPIO6	0063 002Ch
GPIO7	0068 002Ch
WKUP_GPIO1	4210 002Ch
WKUP_GPIO0	4211 002Ch

Figure 2-11. GPIO_SET_FAL_TRIG01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL1																SETFAL0															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-28. GPIO_SET_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SETFAL1	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 1 bits
15-0	SETFAL0	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 0 bits

2.12 GPIO_CLR_FAL_TRIG01 Register (Offset = 30h) [reset = 0h]

GPIO_CLR_FAL_TRIG01 is shown in [Figure 2-12](#) and described in [Table 2-30](#).

[Return to Summary Table.](#)

Clear Falling Edge Detection Register

Table 2-29. GPIO_CLR_FAL_TRIG01 Instances

Instance	Physical Address
GPIO0	0060 0030h
GPIO1	0060 1030h
GPIO2	0061 0030h
GPIO3	0061 1030h
GPIO4	0062 0030h
GPIO5	0062 1030h
GPIO6	0063 0030h
GPIO7	0068 0030h
WKUP_GPIO1	4210 0030h
WKUP_GPIO0	4211 0030h

Figure 2-12. GPIO_CLR_FAL_TRIG01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL1																CLRFAL0															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-30. GPIO_CLR_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLRFAL1	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 1 bits
15-0	CLRFAL0	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 0 bits

2.13 GPIO_INTSTAT01 Register (Offset = 34h) [reset = 0h]

GPIO_INTSTAT01 is shown in [Figure 2-13](#) and described in [Table 2-32](#).

Return to [Summary Table](#).

Bank Interrupt Status Register

Table 2-31. GPIO_INTSTAT01 Instances

Instance	Physical Address
GPIO0	0060 0034h
GPIO1	0060 1034h
GPIO2	0061 0034h
GPIO3	0061 1034h
GPIO4	0062 0034h
GPIO5	0062 1034h
GPIO6	0063 0034h
GPIO7	0068 0034h
WKUP_GPIO1	4210 0034h
WKUP_GPIO0	4211 0034h

Figure 2-13. GPIO_INTSTAT01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT1																STAT0															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-32. GPIO_INTSTAT01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	STAT1	R/W1C	0h	Status of GPIO bank 0 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status
15-0	STAT0	R/W1C	0h	Status of GPIO bank 0 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status

2.14 GPIO_DIR23 Register (Offset = 38h) [reset = FFFFFFFFh]

GPIO_DIR23 is shown in [Figure 2-14](#) and described in [Table 2-34](#).

Return to [Summary Table](#).

Direction Register

Table 2-33. GPIO_DIR23 Instances

Instance	Physical Address
GPIO0	0060 0038h
GPIO1	0060 1038h
GPIO2	0061 0038h
GPIO3	0061 1038h
GPIO4	0062 0038h
GPIO5	0062 1038h
GPIO6	0063 0038h
GPIO7	0068 0038h
WKUP_GPIO1	4210 0038h
WKUP_GPIO0	4211 0038h

Figure 2-14. GPIO_DIR23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR3																DIR2															
R/W-FFFFh																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-34. GPIO_DIR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DIR3	R/W	FFFFh	Direction of GPIO bank 3 bits, 0 = output, 1 = input
15-0	DIR2	R/W	FFFFh	Direction of GPIO bank 2 bits, 0 = output, 1 = input

2.15 GPIO_OUT_DATA23 Register (Offset = 3Ch) [reset = 0h]

GPIO_OUT_DATA23 is shown in [Figure 2-15](#) and described in [Table 2-36](#).

Return to [Summary Table](#).

Output Drive State Register

Table 2-35. GPIO_OUT_DATA23 Instances

Instance	Physical Address
GPIO0	0060 003Ch
GPIO1	0060 103Ch
GPIO2	0061 003Ch
GPIO3	0061 103Ch
GPIO4	0062 003Ch
GPIO5	0062 103Ch
GPIO6	0063 003Ch
GPIO7	0068 003Ch
WKUP_GPIO1	4210 003Ch
WKUP_GPIO0	4211 003Ch

Figure 2-15. GPIO_OUT_DATA23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT3																OUT2															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-36. GPIO_OUT_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OUT3	R/W	0h	Output drive state of GPIO bank 3 bits, does not affect operation when it is configured as input Reading it returns the output drive state
15-0	OUT2	R/W	0h	Output drive state of GPIO bank 2 bits, does not affect operation when it is configured as input Reading it returns the output drive state

2.16 GPIO_SET_DATA23 Register (Offset = 40h) [reset = 0h]

GPIO_SET_DATA23 is shown in [Figure 2-16](#) and described in [Table 2-38](#).

Return to [Summary Table](#).

Set Output Drive State Register

Table 2-37. GPIO_SET_DATA23 Instances

Instance	Physical Address
GPIO0	0060 0040h
GPIO1	0060 1040h
GPIO2	0061 0040h
GPIO3	0061 1040h
GPIO4	0062 0040h
GPIO5	0062 1040h
GPIO6	0063 0040h
GPIO7	0068 0040h
WKUP_GPIO1	4210 0040h
WKUP_GPIO0	4211 0040h

Figure 2-16. GPIO_SET_DATA23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET3																SET2															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-38. GPIO_SET_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SET3	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 3 bits Reading it returns the output drive state
15-0	SET2	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 2 bits Reading it returns the output drive state

2.17 GPIO_CLR_DATA23 Register (Offset = 44h) [reset = 0h]

GPIO_CLR_DATA23 is shown in [Figure 2-17](#) and described in [Table 2-40](#).

Return to [Summary Table](#).

Clear Output Drive State Register

Table 2-39. GPIO_CLR_DATA23 Instances

Instance	Physical Address
GPIO0	0060 0044h
GPIO1	0060 1044h
GPIO2	0061 0044h
GPIO3	0061 1044h
GPIO4	0062 0044h
GPIO5	0062 1044h
GPIO6	0063 0044h
GPIO7	0068 0044h
WKUP_GPIO1	4210 0044h
WKUP_GPIO0	4211 0044h

Figure 2-17. GPIO_CLR_DATA23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR3																CLR2															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-40. GPIO_CLR_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLR3	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state
15-0	CLR2	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state

2.18 GPIO_IN_DATA23 Register (Offset = 48h) [reset = 0h]

GPIO_IN_DATA23 is shown in [Figure 2-18](#) and described in [Table 2-42](#).

Return to [Summary Table](#).

Bank Status Register

Table 2-41. GPIO_IN_DATA23 Instances

Instance	Physical Address
GPIO0	0060 0048h
GPIO1	0060 1048h
GPIO2	0061 0048h
GPIO3	0061 1048h
GPIO4	0062 0048h
GPIO5	0062 1048h
GPIO6	0063 0048h
GPIO7	0068 0048h
WKUP_GPIO1	4210 0048h
WKUP_GPIO0	4211 0048h

Figure 2-18. GPIO_IN_DATA23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN3																IN2															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 2-42. GPIO_IN_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	IN3	R	0h	Status of GPIO bank 3 bits
15-0	IN2	R	0h	Status of GPIO bank 2 bits

2.19 GPIO_SET_RIS_TRIG23 Register (Offset = 4Ch) [reset = 0h]

GPIO_SET_RIS_TRIG23 is shown in [Figure 2-19](#) and described in [Table 2-44](#).

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Set Rising Edge Detection Register

Table 2-43. GPIO_SET_RIS_TRIG23 Instances

Instance	Physical Address
GPIO0	0060 004Ch
GPIO1	0060 104Ch
GPIO2	0061 004Ch
GPIO3	0061 104Ch
GPIO4	0062 004Ch
GPIO5	0062 104Ch
GPIO6	0063 004Ch
GPIO7	0068 004Ch
WKUP_GPIO1	4210 004Ch
WKUP_GPIO0	4211 004Ch

Figure 2-19. GPIO_SET_RIS_TRIG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS3																SETRIS2															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-44. GPIO_SET_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SETRIS3	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 3 bits
15-0	SETRIS2	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 2 bits

2.20 GPIO_CLR_RIS_TRIG23 Register (Offset = 50h) [reset = 0h]

GPIO_CLR_RIS_TRIG23 is shown in [Figure 2-20](#) and described in [Table 2-46](#).

Return to [Summary Table](#).

Clear Rising Edge Detection Register

Table 2-45. GPIO_CLR_RIS_TRIG23 Instances

Instance	Physical Address
GPIO0	0060 0050h
GPIO1	0060 1050h
GPIO2	0061 0050h
GPIO3	0061 1050h
GPIO4	0062 0050h
GPIO5	0062 1050h
GPIO6	0063 0050h
GPIO7	0068 0050h
WKUP_GPIO1	4210 0050h
WKUP_GPIO0	4211 0050h

Figure 2-20. GPIO_CLR_RIS_TRIG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS3																CLRRIS2															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-46. GPIO_CLR_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLRRIS3	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 3 bits
15-0	CLRRIS2	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 2 bits

2.21 GPIO_SET_FAL_TRIG23 Register (Offset = 54h) [reset = 0h]

GPIO_SET_FAL_TRIG23 is shown in [Figure 2-21](#) and described in [Table 2-48](#).

Return to [Summary Table](#).

Set Falling Edge Detection Register

Table 2-47. GPIO_SET_FAL_TRIG23 Instances

Instance	Physical Address
GPIO0	0060 0054h
GPIO1	0060 1054h
GPIO2	0061 0054h
GPIO3	0061 1054h
GPIO4	0062 0054h
GPIO5	0062 1054h
GPIO6	0063 0054h
GPIO7	0068 0054h
WKUP_GPIO1	4210 0054h
WKUP_GPIO0	4211 0054h

Figure 2-21. GPIO_SET_FAL_TRIG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL3																SETFAL2															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-48. GPIO_SET_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SETFAL3	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 3 bits
15-0	SETFAL2	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 2 bits

2.22 GPIO_CLR_FAL_TRIG23 Register (Offset = 58h) [reset = 0h]

GPIO_CLR_FAL_TRIG23 is shown in [Figure 2-22](#) and described in [Table 2-50](#).

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Clear Falling Edge Detection Register

Table 2-49. GPIO_CLR_FAL_TRIG23 Instances

Instance	Physical Address
GPIO0	0060 0058h
GPIO1	0060 1058h
GPIO2	0061 0058h
GPIO3	0061 1058h
GPIO4	0062 0058h
GPIO5	0062 1058h
GPIO6	0063 0058h
GPIO7	0068 0058h
WKUP_GPIO1	4210 0058h
WKUP_GPIO0	4211 0058h

Figure 2-22. GPIO_CLR_FAL_TRIG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL3																CLRFAL2															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-50. GPIO_CLR_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLRFAL3	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 3 bits
15-0	CLRFAL2	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 2 bits

2.23 GPIO_INTSTAT23 Register (Offset = 5Ch) [reset = 0h]

GPIO_INTSTAT23 is shown in [Figure 2-23](#) and described in [Table 2-52](#).

[Return to Summary Table.](#)

Bank Interrupt Status Register

Table 2-51. GPIO_INTSTAT23 Instances

Instance	Physical Address
GPIO0	0060 005Ch
GPIO1	0060 105Ch
GPIO2	0061 005Ch
GPIO3	0061 105Ch
GPIO4	0062 005Ch
GPIO5	0062 105Ch
GPIO6	0063 005Ch
GPIO7	0068 005Ch
WKUP_GPIO1	4210 005Ch
WKUP_GPIO0	4211 005Ch

Figure 2-23. GPIO_INTSTAT23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT3																STAT2															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-52. GPIO_INTSTAT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	STAT3	R/W1C	0h	Status of GPIO bank 2 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status
15-0	STAT2	R/W1C	0h	Status of GPIO bank 2 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status

2.24 GPIO_DIR45 Register (Offset = 60h) [reset = FFFFFFFFh]

GPIO_DIR45 is shown in [Figure 2-24](#) and described in [Table 2-54](#).

Return to [Summary Table](#).

Direction Register

Table 2-53. GPIO_DIR45 Instances

Instance	Physical Address
GPIO0	0060 0060h
GPIO1	0060 1060h
GPIO2	0061 0060h
GPIO3	0061 1060h
GPIO4	0062 0060h
GPIO5	0062 1060h
GPIO6	0063 0060h
GPIO7	0068 0060h
WKUP_GPIO1	4210 0060h
WKUP_GPIO0	4211 0060h

Figure 2-24. GPIO_DIR45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR5																DIR4															
R/W-FFFFh																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-54. GPIO_DIR45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DIR5	R/W	FFFFh	Direction of GPIO bank 5 bits, 0 = output, 1 = input
15-0	DIR4	R/W	FFFFh	Direction of GPIO bank 4 bits, 0 = output, 1 = input

2.25 GPIO_OUT_DATA45 Register (Offset = 64h) [reset = 0h]

GPIO_OUT_DATA45 is shown in [Figure 2-25](#) and described in [Table 2-56](#).

Return to [Summary Table](#).

Output Drive State Register

Table 2-55. GPIO_OUT_DATA45 Instances

Instance	Physical Address
GPIO0	0060 0064h
GPIO1	0060 1064h
GPIO2	0061 0064h
GPIO3	0061 1064h
GPIO4	0062 0064h
GPIO5	0062 1064h
GPIO6	0063 0064h
GPIO7	0068 0064h
WKUP_GPIO1	4210 0064h
WKUP_GPIO0	4211 0064h

Figure 2-25. GPIO_OUT_DATA45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT5																OUT4															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-56. GPIO_OUT_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OUT5	R/W	0h	Output drive state of GPIO bank 5 bits, does not affect operation when it is configured as input Reading it returns the output drive state
15-0	OUT4	R/W	0h	Output drive state of GPIO bank 4 bits, does not affect operation when it is configured as input Reading it returns the output drive state

2.26 GPIO_SET_DATA45 Register (Offset = 68h) [reset = 0h]

GPIO_SET_DATA45 is shown in [Figure 2-26](#) and described in [Table 2-58](#).

[Return to Summary Table.](#)

Set Output Drive State Register

Table 2-57. GPIO_SET_DATA45 Instances

Instance	Physical Address
GPIO0	0060 0068h
GPIO1	0060 1068h
GPIO2	0061 0068h
GPIO3	0061 1068h
GPIO4	0062 0068h
GPIO5	0062 1068h
GPIO6	0063 0068h
GPIO7	0068 0068h
WKUP_GPIO1	4210 0068h
WKUP_GPIO0	4211 0068h

Figure 2-26. GPIO_SET_DATA45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET5																SET4															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-58. GPIO_SET_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SET5	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 5 bits Reading it returns the output drive state
15-0	SET4	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 4 bits Reading it returns the output drive state

2.27 GPIO_CLR_DATA45 Register (Offset = 6Ch) [reset = 0h]

GPIO_CLR_DATA45 is shown in [Figure 2-27](#) and described in [Table 2-60](#).

[Return to Summary Table.](#)

Clear Output Drive State Register

Table 2-59. GPIO_CLR_DATA45 Instances

Instance	Physical Address
GPIO0	0060 006Ch
GPIO1	0060 106Ch
GPIO2	0061 006Ch
GPIO3	0061 106Ch
GPIO4	0062 006Ch
GPIO5	0062 106Ch
GPIO6	0063 006Ch
GPIO7	0068 006Ch
WKUP_GPIO1	4210 006Ch
WKUP_GPIO0	4211 006Ch

Figure 2-27. GPIO_CLR_DATA45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR5																CLR4															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-60. GPIO_CLR_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLR5	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state
15-0	CLR4	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state

2.28 GPIO_IN_DATA45 Register (Offset = 70h) [reset = 0h]

GPIO_IN_DATA45 is shown in [Figure 2-28](#) and described in [Table 2-62](#).

[Return to Summary Table.](#)

Bank Status Register

Table 2-61. GPIO_IN_DATA45 Instances

Instance	Physical Address
GPIO0	0060 0070h
GPIO1	0060 1070h
GPIO2	0061 0070h
GPIO3	0061 1070h
GPIO4	0062 0070h
GPIO5	0062 1070h
GPIO6	0063 0070h
GPIO7	0068 0070h
WKUP_GPIO1	4210 0070h
WKUP_GPIO0	4211 0070h

Figure 2-28. GPIO_IN_DATA45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN5																IN4															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 2-62. GPIO_IN_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	IN5	R	0h	Status of GPIO bank 5 bits
15-0	IN4	R	0h	Status of GPIO bank 4 bits

2.29 GPIO_SET_RIS_TRIG45 Register (Offset = 74h) [reset = 0h]

GPIO_SET_RIS_TRIG45 is shown in [Figure 2-29](#) and described in [Table 2-64](#).

Return to [Summary Table](#).

Set Rising Edge Detection Register

Table 2-63. GPIO_SET_RIS_TRIG45 Instances

Instance	Physical Address
GPIO0	0060 0074h
GPIO1	0060 1074h
GPIO2	0061 0074h
GPIO3	0061 1074h
GPIO4	0062 0074h
GPIO5	0062 1074h
GPIO6	0063 0074h
GPIO7	0068 0074h
WKUP_GPIO1	4210 0074h
WKUP_GPIO0	4211 0074h

Figure 2-29. GPIO_SET_RIS_TRIG45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS5																SETRIS4															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-64. GPIO_SET_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SETRIS5	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 5 bits
15-0	SETRIS4	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 4 bits

2.30 GPIO_CLR_RIS_TRIG45 Register (Offset = 78h) [reset = 0h]

GPIO_CLR_RIS_TRIG45 is shown in [Figure 2-30](#) and described in [Table 2-66](#).

Return to [Summary Table](#).

Clear Rising Edge Detection Register

Table 2-65. GPIO_CLR_RIS_TRIG45 Instances

Instance	Physical Address
GPIO0	0060 0078h
GPIO1	0060 1078h
GPIO2	0061 0078h
GPIO3	0061 1078h
GPIO4	0062 0078h
GPIO5	0062 1078h
GPIO6	0063 0078h
GPIO7	0068 0078h
WKUP_GPIO1	4210 0078h
WKUP_GPIO0	4211 0078h

Figure 2-30. GPIO_CLR_RIS_TRIG45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS5																CLRRIS4															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-66. GPIO_CLR_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLRRIS5	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 5 bits
15-0	CLRRIS4	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 4 bits

2.31 GPIO_SET_FAL_TRIG45 Register (Offset = 7Ch) [reset = 0h]

GPIO_SET_FAL_TRIG45 is shown in [Figure 2-31](#) and described in [Table 2-68](#).

[Return to Summary Table.](#)

Set Falling Edge Detection Register

Table 2-67. GPIO_SET_FAL_TRIG45 Instances

Instance	Physical Address
GPIO0	0060 007Ch
GPIO1	0060 107Ch
GPIO2	0061 007Ch
GPIO3	0061 107Ch
GPIO4	0062 007Ch
GPIO5	0062 107Ch
GPIO6	0063 007Ch
GPIO7	0068 007Ch
WKUP_GPIO1	4210 007Ch
WKUP_GPIO0	4211 007Ch

Figure 2-31. GPIO_SET_FAL_TRIG45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL5																SETFAL4															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-68. GPIO_SET_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SETFAL5	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 5 bits
15-0	SETFAL4	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 4 bits

2.32 GPIO_CLR_FAL_TRIG45 Register (Offset = 80h) [reset = 0h]

GPIO_CLR_FAL_TRIG45 is shown in [Figure 2-32](#) and described in [Table 2-70](#).

Return to [Summary Table](#).

Clear Falling Edge Detection Register

Table 2-69. GPIO_CLR_FAL_TRIG45 Instances

Instance	Physical Address
GPIO0	0060 0080h
GPIO1	0060 1080h
GPIO2	0061 0080h
GPIO3	0061 1080h
GPIO4	0062 0080h
GPIO5	0062 1080h
GPIO6	0063 0080h
GPIO7	0068 0080h
WKUP_GPIO1	4210 0080h
WKUP_GPIO0	4211 0080h

Figure 2-32. GPIO_CLR_FAL_TRIG45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL5																CLRFAL4															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-70. GPIO_CLR_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLRFAL5	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 5 bits
15-0	CLRFAL4	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 4 bits

2.33 GPIO_INTSTAT45 Register (Offset = 84h) [reset = 0h]

GPIO_INTSTAT45 is shown in [Figure 2-33](#) and described in [Table 2-72](#).

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Bank Interrupt Status Register

Table 2-71. GPIO_INTSTAT45 Instances

Instance	Physical Address
GPIO0	0060 0084h
GPIO1	0060 1084h
GPIO2	0061 0084h
GPIO3	0061 1084h
GPIO4	0062 0084h
GPIO5	0062 1084h
GPIO6	0063 0084h
GPIO7	0068 0084h
WKUP_GPIO1	4210 0084h
WKUP_GPIO0	4211 0084h

Figure 2-33. GPIO_INTSTAT45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT5																STAT4															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-72. GPIO_INTSTAT45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	STAT5	R/W1C	0h	Status of GPIO bank 4 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status
15-0	STAT4	R/W1C	0h	Status of GPIO bank 4 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status

2.34 GPIO_DIR67 Register (Offset = 88h) [reset = FFFFFFFFh]

GPIO_DIR67 is shown in [Figure 2-34](#) and described in [Table 2-74](#).

Return to [Summary Table](#).

Direction Register

Table 2-73. GPIO_DIR67 Instances

Instance	Physical Address
GPIO0	0060 0088h
GPIO1	0060 1088h
GPIO2	0061 0088h
GPIO3	0061 1088h
GPIO4	0062 0088h
GPIO5	0062 1088h
GPIO6	0063 0088h
GPIO7	0068 0088h
WKUP_GPIO1	4210 0088h
WKUP_GPIO0	4211 0088h

Figure 2-34. GPIO_DIR67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR7																DIR6															
R/W-FFFFh																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-74. GPIO_DIR67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DIR7	R/W	FFFFh	Direction of GPIO bank 7 bits, 0 = output, 1 = input
15-0	DIR6	R/W	FFFFh	Direction of GPIO bank 6 bits, 0 = output, 1 = input

2.35 GPIO_OUT_DATA67 Register (Offset = 8Ch) [reset = 0h]

GPIO_OUT_DATA67 is shown in [Figure 2-35](#) and described in [Table 2-76](#).

Return to [Summary Table](#).

Output Drive State Register

Table 2-75. GPIO_OUT_DATA67 Instances

Instance	Physical Address
GPIO0	0060 008Ch
GPIO1	0060 108Ch
GPIO2	0061 008Ch
GPIO3	0061 108Ch
GPIO4	0062 008Ch
GPIO5	0062 108Ch
GPIO6	0063 008Ch
GPIO7	0068 008Ch
WKUP_GPIO1	4210 008Ch
WKUP_GPIO0	4211 008Ch

Figure 2-35. GPIO_OUT_DATA67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT7																OUT6															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-76. GPIO_OUT_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OUT7	R/W	0h	Output drive state of GPIO bank 7 bits, does not affect operation when it is configured as input Reading it returns the output drive state
15-0	OUT6	R/W	0h	Output drive state of GPIO bank 6 bits, does not affect operation when it is configured as input Reading it returns the output drive state

2.36 GPIO_SET_DATA67 Register (Offset = 90h) [reset = 0h]

GPIO_SET_DATA67 is shown in [Figure 2-36](#) and described in [Table 2-78](#).

Return to [Summary Table](#).

Set Output Drive State Register

Table 2-77. GPIO_SET_DATA67 Instances

Instance	Physical Address
GPIO0	0060 0090h
GPIO1	0060 1090h
GPIO2	0061 0090h
GPIO3	0061 1090h
GPIO4	0062 0090h
GPIO5	0062 1090h
GPIO6	0063 0090h
GPIO7	0068 0090h
WKUP_GPIO1	4210 0090h
WKUP_GPIO0	4211 0090h

Figure 2-36. GPIO_SET_DATA67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET7																SET6															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-78. GPIO_SET_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SET7	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 7 bits Reading it returns the output drive state
15-0	SET6	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 6 bits Reading it returns the output drive state

2.37 GPIO_CLR_DATA67 Register (Offset = 94h) [reset = 0h]

GPIO_CLR_DATA67 is shown in [Figure 2-37](#) and described in [Table 2-80](#).

Return to [Summary Table](#).

Clear Output Drive State Register

Table 2-79. GPIO_CLR_DATA67 Instances

Instance	Physical Address
GPIO0	0060 0094h
GPIO1	0060 1094h
GPIO2	0061 0094h
GPIO3	0061 1094h
GPIO4	0062 0094h
GPIO5	0062 1094h
GPIO6	0063 0094h
GPIO7	0068 0094h
WKUP_GPIO1	4210 0094h
WKUP_GPIO0	4211 0094h

Figure 2-37. GPIO_CLR_DATA67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR7																CLR6															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-80. GPIO_CLR_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLR7	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state
15-0	CLR6	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state

2.38 GPIO_IN_DATA67 Register (Offset = 98h) [reset = 0h]

GPIO_IN_DATA67 is shown in [Figure 2-38](#) and described in [Table 2-82](#).

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Bank Status Register

Table 2-81. GPIO_IN_DATA67 Instances

Instance	Physical Address
GPIO0	0060 0098h
GPIO1	0060 1098h
GPIO2	0061 0098h
GPIO3	0061 1098h
GPIO4	0062 0098h
GPIO5	0062 1098h
GPIO6	0063 0098h
GPIO7	0068 0098h
WKUP_GPIO1	4210 0098h
WKUP_GPIO0	4211 0098h

Figure 2-38. GPIO_IN_DATA67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN7																IN6															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 2-82. GPIO_IN_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	IN7	R	0h	Status of GPIO bank 7 bits
15-0	IN6	R	0h	Status of GPIO bank 6 bits

2.39 GPIO_SET_RIS_TRIG67 Register (Offset = 9Ch) [reset = 0h]

GPIO_SET_RIS_TRIG67 is shown in [Figure 2-39](#) and described in [Table 2-84](#).

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Set Rising Edge Detection Register

Table 2-83. GPIO_SET_RIS_TRIG67 Instances

Instance	Physical Address
GPIO0	0060 009Ch
GPIO1	0060 109Ch
GPIO2	0061 009Ch
GPIO3	0061 109Ch
GPIO4	0062 009Ch
GPIO5	0062 109Ch
GPIO6	0063 009Ch
GPIO7	0068 009Ch
WKUP_GPIO1	4210 009Ch
WKUP_GPIO0	4211 009Ch

Figure 2-39. GPIO_SET_RIS_TRIG67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS7																SETRIS6															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-84. GPIO_SET_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SETRIS7	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 7 bits
15-0	SETRIS6	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 6 bits

2.40 GPIO_CLR_RIS_TRIG67 Register (Offset = A0h) [reset = 0h]

GPIO_CLR_RIS_TRIG67 is shown in [Figure 2-40](#) and described in [Table 2-86](#).

Return to [Summary Table](#).

Clear Rising Edge Detection Register

Table 2-85. GPIO_CLR_RIS_TRIG67 Instances

Instance	Physical Address
GPIO0	0060 00A0h
GPIO1	0060 10A0h
GPIO2	0061 00A0h
GPIO3	0061 10A0h
GPIO4	0062 00A0h
GPIO5	0062 10A0h
GPIO6	0063 00A0h
GPIO7	0068 00A0h
WKUP_GPIO1	4210 00A0h
WKUP_GPIO0	4211 00A0h

Figure 2-40. GPIO_CLR_RIS_TRIG67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS7																CLRRIS6															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-86. GPIO_CLR_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLRRIS7	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 7 bits
15-0	CLRRIS6	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 6 bits

2.41 GPIO_SET_FAL_TRIG67 Register (Offset = A4h) [reset = 0h]

GPIO_SET_FAL_TRIG67 is shown in [Figure 2-41](#) and described in [Table 2-88](#).

[Return to Summary Table.](#)

Set Falling Edge Detection Register

Table 2-87. GPIO_SET_FAL_TRIG67 Instances

Instance	Physical Address
GPIO0	0060 00A4h
GPIO1	0060 10A4h
GPIO2	0061 00A4h
GPIO3	0061 10A4h
GPIO4	0062 00A4h
GPIO5	0062 10A4h
GPIO6	0063 00A4h
GPIO7	0068 00A4h
WKUP_GPIO1	4210 00A4h
WKUP_GPIO0	4211 00A4h

Figure 2-41. GPIO_SET_FAL_TRIG67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL7																SETFAL6															
R/W1S-0h																R/W1S-0h															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-88. GPIO_SET_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SETFAL7	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 7 bits
15-0	SETFAL6	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 6 bits

2.42 GPIO_CLR_FAL_TRIG67 Register (Offset = A8h) [reset = 0h]

GPIO_CLR_FAL_TRIG67 is shown in [Figure 2-42](#) and described in [Table 2-90](#).

[Return to Summary Table.](#)

Clear Falling Edge Detection Register

Table 2-89. GPIO_CLR_FAL_TRIG67 Instances

Instance	Physical Address
GPIO0	0060 00A8h
GPIO1	0060 10A8h
GPIO2	0061 00A8h
GPIO3	0061 10A8h
GPIO4	0062 00A8h
GPIO5	0062 10A8h
GPIO6	0063 00A8h
GPIO7	0068 00A8h
WKUP_GPIO1	4210 00A8h
WKUP_GPIO0	4211 00A8h

Figure 2-42. GPIO_CLR_FAL_TRIG67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL7																CLRFAL6															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-90. GPIO_CLR_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CLRFAL7	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 7 bits
15-0	CLRFAL6	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 6 bits

2.43 GPIO_INTSTAT67 Register (Offset = ACh) [reset = 0h]

GPIO_INTSTAT67 is shown in [Figure 2-43](#) and described in [Table 2-92](#).

Return to [Summary Table](#).

Bank Interrupt Status Register

Table 2-91. GPIO_INTSTAT67 Instances

Instance	Physical Address
GPIO0	0060 00ACh
GPIO1	0060 10ACh
GPIO2	0061 00ACh
GPIO3	0061 10ACh
GPIO4	0062 00ACh
GPIO5	0062 10ACh
GPIO6	0063 00ACh
GPIO7	0068 00ACh
WKUP_GPIO1	4210 00ACh
WKUP_GPIO0	4211 00ACh

Figure 2-43. GPIO_INTSTAT67 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT7																STAT6															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-92. GPIO_INTSTAT67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	STAT7	R/W1C	0h	Status of GPIO bank 6 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status
15-0	STAT6	R/W1C	0h	Status of GPIO bank 6 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status

2.44 GPIO_DIR8 Register (Offset = B0h) [reset = FFFFFFFFh]

GPIO_DIR8 is shown in [Figure 2-44](#) and described in [Table 2-94](#).

[Return to Summary Table.](#)

Direction Register

Table 2-93. GPIO_DIR8 Instances

Instance	Physical Address
GPIO0	0060 00B0h
GPIO1	0060 10B0h
GPIO2	0061 00B0h
GPIO3	0061 10B0h
GPIO4	0062 00B0h
GPIO5	0062 10B0h
GPIO6	0063 00B0h
GPIO7	0068 00B0h
WKUP_GPIO1	4210 00B0h
WKUP_GPIO0	4211 00B0h

Figure 2-44. GPIO_DIR8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DIR8															
R-FFFFh																R/W-FFFFh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-94. GPIO_DIR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	FFFFh	RESERVED
15-0	DIR8	R/W	FFFFh	Direction of GPIO bank 8 bits, 0 = output, 1 = input

2.45 GPIO_OUT_DATA8 Register (Offset = B4h) [reset = 0h]

GPIO_OUT_DATA8 is shown in [Figure 2-45](#) and described in [Table 2-96](#).

Return to [Summary Table](#).

Output Drive State Register

Table 2-95. GPIO_OUT_DATA8 Instances

Instance	Physical Address
GPIO0	0060 00B4h
GPIO1	0060 10B4h
GPIO2	0061 00B4h
GPIO3	0061 10B4h
GPIO4	0062 00B4h
GPIO5	0062 10B4h
GPIO6	0063 00B4h
GPIO7	0068 00B4h
WKUP_GPIO1	4210 00B4h
WKUP_GPIO0	4211 00B4h

Figure 2-45. GPIO_OUT_DATA8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OUT8															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-96. GPIO_OUT_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	RESERVED
15-0	OUT8	R/W	0h	Output drive state of GPIO bank 8 bits, does not affect operation when it is configured as input Reading it returns the output drive state

2.46 GPIO_SET_DATA8 Register (Offset = B8h) [reset = 0h]

GPIO_SET_DATA8 is shown in [Figure 2-46](#) and described in [Table 2-98](#).

[Return to Summary Table.](#)

Set Output Drive State Register

Table 2-97. GPIO_SET_DATA8 Instances

Instance	Physical Address
GPIO0	0060 00B8h
GPIO1	0060 10B8h
GPIO2	0061 00B8h
GPIO3	0061 10B8h
GPIO4	0062 00B8h
GPIO5	0062 10B8h
GPIO6	0063 00B8h
GPIO7	0068 00B8h
WKUP_GPIO1	4210 00B8h
WKUP_GPIO0	4211 00B8h

Figure 2-46. GPIO_SET_DATA8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SET8															
R-0h																R/W1S-0h															

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-98. GPIO_SET_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	RESERVED
15-0	SET8	R/W1S	0h	Writing 1 sets the output drive state of GPIO bank 8 bits Reading it returns the output drive state

2.47 GPIO_CLR_DATA8 Register (Offset = BCh) [reset = 0h]

GPIO_CLR_DATA8 is shown in [Figure 2-47](#) and described in [Table 2-100](#).

Return to [Summary Table](#).

Clear Output Drive State Register

Table 2-99. GPIO_CLR_DATA8 Instances

Instance	Physical Address
GPIO0	0060 00BCh
GPIO1	0060 10BCh
GPIO2	0061 00BCh
GPIO3	0061 10BCh
GPIO4	0062 00BCh
GPIO5	0062 10BCh
GPIO6	0063 00BCh
GPIO7	0068 00BCh
WKUP_GPIO1	4210 00BCh
WKUP_GPIO0	4211 00BCh

Figure 2-47. GPIO_CLR_DATA8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLR8															
R-0h																R/W1C-0h															

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-100. GPIO_CLR_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	RESERVED
15-0	CLR8	R/W1C	0h	Writing 1 clears the output drive state of GPIO Reading it returns the output drive state

2.48 GPIO_IN_DATA8 Register (Offset = C0h) [reset = 0h]

GPIO_IN_DATA8 is shown in [Figure 2-48](#) and described in [Table 2-102](#).

Return to [Summary Table](#).

Bank Status Register

Table 2-101. GPIO_IN_DATA8 Instances

Instance	Physical Address
GPIO0	0060 00C0h
GPIO1	0060 10C0h
GPIO2	0061 00C0h
GPIO3	0061 10C0h
GPIO4	0062 00C0h
GPIO5	0062 10C0h
GPIO6	0063 00C0h
GPIO7	0068 00C0h
WKUP_GPIO1	4210 00C0h
WKUP_GPIO0	4211 00C0h

Figure 2-48. GPIO_IN_DATA8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																IN8															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 2-102. GPIO_IN_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	RESERVED
15-0	IN8	R	0h	Status of GPIO bank 8 bits

2.49 GPIO_SET_RIS_TRIG8 Register (Offset = C4h) [reset = X]

GPIO_SET_RIS_TRIG8 is shown in [Figure 2-49](#) and described in [Table 2-104](#).

[Return to Summary Table.](#)

Set Rising Edge Detection Register

Table 2-103. GPIO_SET_RIS_TRIG8 Instances

Instance	Physical Address
GPIO0	0060 00C4h
GPIO1	0060 10C4h
GPIO2	0061 00C4h
GPIO3	0061 10C4h
GPIO4	0062 00C4h
GPIO5	0062 10C4h
GPIO6	0063 00C4h
GPIO7	0068 00C4h
WKUP_GPIO1	4210 00C4h
WKUP_GPIO0	4211 00C4h

Figure 2-49. GPIO_SET_RIS_TRIG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SETRIS8															
R/W-X																R/W1S-0h															

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-104. GPIO_SET_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	SETRIS8	R/W1S	0h	Writing 1 enables rising edge detection for GPIO bank 8 bits

2.50 GPIO_CLR_RIS_TRIG8 Register (Offset = C8h) [reset = X]

GPIO_CLR_RIS_TRIG8 is shown in [Figure 2-50](#) and described in [Table 2-106](#).

[Return to Summary Table.](#)

Clear Rising Edge Detection Register

Table 2-105. GPIO_CLR_RIS_TRIG8 Instances

Instance	Physical Address
GPIO0	0060 00C8h
GPIO1	0060 10C8h
GPIO2	0061 00C8h
GPIO3	0061 10C8h
GPIO4	0062 00C8h
GPIO5	0062 10C8h
GPIO6	0063 00C8h
GPIO7	0068 00C8h
WKUP_GPIO1	4210 00C8h
WKUP_GPIO0	4211 00C8h

Figure 2-50. GPIO_CLR_RIS_TRIG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLRRIS8															
R/W-X																R/W1C-0h															

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-106. GPIO_CLR_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	CLRRIS8	R/W1C	0h	Writing 1 clears rising edge detection for GPIO bank 8 bits

2.51 GPIO_SET_FAL_TRIG8 Register (Offset = CCh) [reset = X]

GPIO_SET_FAL_TRIG8 is shown in [Figure 2-51](#) and described in [Table 2-108](#).

[Return to Summary Table.](#)

Set Falling Edge Detection Register

Table 2-107. GPIO_SET_FAL_TRIG8 Instances

Instance	Physical Address
GPIO0	0060 00CCh
GPIO1	0060 10CCh
GPIO2	0061 00CCh
GPIO3	0061 10CCh
GPIO4	0062 00CCh
GPIO5	0062 10CCh
GPIO6	0063 00CCh
GPIO7	0068 00CCh
WKUP_GPIO1	4210 00CCh
WKUP_GPIO0	4211 00CCh

Figure 2-51. GPIO_SET_FAL_TRIG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SETFAL8															
R/W-X																R/W1S-0h															

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 2-108. GPIO_SET_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	SETFAL8	R/W1S	0h	Writing 1 enables falling edge detection for for GPIO bank 8 bits

2.52 GPIO_CLR_FAL_TRIG8 Register (Offset = D0h) [reset = X]

GPIO_CLR_FAL_TRIG8 is shown in [Figure 2-52](#) and described in [Table 2-110](#).

Return to [Summary Table](#).

Clear Falling Edge Detection Register

Table 2-109. GPIO_CLR_FAL_TRIG8 Instances

Instance	Physical Address
GPIO0	0060 00D0h
GPIO1	0060 10D0h
GPIO2	0061 00D0h
GPIO3	0061 10D0h
GPIO4	0062 00D0h
GPIO5	0062 10D0h
GPIO6	0063 00D0h
GPIO7	0068 00D0h
WKUP_GPIO1	4210 00D0h
WKUP_GPIO0	4211 00D0h

Figure 2-52. GPIO_CLR_FAL_TRIG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CLR_FAL8															
R/W-X																R/W1C-0h															

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-110. GPIO_CLR_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	CLR_FAL8	R/W1C	0h	Writing 1 clears falling edge detection for for GPIO bank 8 bits

2.53 GPIO_INTSTAT8 Register (Offset = D4h) [reset = 0h]

GPIO_INTSTAT8 is shown in [Figure 2-53](#) and described in [Table 2-112](#).

Return to [Summary Table](#).

Bank Interrupt Status Register

Table 2-111. GPIO_INTSTAT8 Instances

Instance	Physical Address
GPIO0	0060 00D4h
GPIO1	0060 10D4h
GPIO2	0061 00D4h
GPIO3	0061 10D4h
GPIO4	0062 00D4h
GPIO5	0062 10D4h
GPIO6	0063 00D4h
GPIO7	0068 00D4h
WKUP_GPIO1	4210 00D4h
WKUP_GPIO0	4211 00D4h

Figure 2-53. GPIO_INTSTAT8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																STAT8															
R-0h																R/W1C-0h															

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-112. GPIO_INTSTAT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	RESERVED
15-0	STAT8	R/W1C	0h	Status of GPIO bank 8 bits interrupt Reading back 1 = interrupt occurred 0 = interrupt hasnt occurred since last cleared Writing 1 clears the corresponding interrupt status

3 I2C Registers

Table 3-2 lists the memory-mapped registers for the I2C registers. All register offset addresses not listed in Table 3-2 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. I2C Instances

Instance	Base Address
I2C0_CFG	0200 0000h
I2C1_CFG	0201 0000h
I2C2_CFG	0202 0000h
I2C3_CFG	0203 0000h
I2C4_CFG	0204 0000h
I2C5_CFG	0205 0000h
I2C6_CFG	0206 0000h
MCU_I2C0_CFG	40B0 0000h
MCU_I2C1_CFG	40B1 0000h
WKUP_I2C0_CFG	4212 0000h

Table 3-2. I2C Registers

Offset	Acronym	Register Name	I2C0_CFG Physical Address	I2C1_CFG Physical Address	I2C2_CFG Physical Address
0h	I2C_REVNB_LO		0200 0000h	0201 0000h	0202 0000h
4h	I2C_REVNB_HI		0200 0004h	0201 0004h	0202 0004h
10h	I2C_SYSC		0200 0010h	0201 0010h	0202 0010h
20h	I2C_EOI		0200 0020h	0201 0020h	0202 0020h
24h	I2C_IRQSTATUS_RAW		0200 0024h	0201 0024h	0202 0024h
28h	I2C_IRQSTATUS		0200 0028h	0201 0028h	0202 0028h
2Ch	I2C_IRQENABLE_SET		0200 002Ch	0201 002Ch	0202 002Ch
30h	I2C_IRQENABLE_CLR		0200 0030h	0201 0030h	0202 0030h
34h	I2C_WE		0200 0034h	0201 0034h	0202 0034h
38h	I2C_DMARXENABLE_SET		0200 0038h	0201 0038h	0202 0038h
3Ch	I2C_DMATXENABLE_SET		0200 003Ch	0201 003Ch	0202 003Ch
40h	I2C_DMARXENABLE_CLR		0200 0040h	0201 0040h	0202 0040h
44h	I2C_DMATXENABLE_CLR		0200 0044h	0201 0044h	0202 0044h
48h	I2C_DMARXWAKE_EN		0200 0048h	0201 0048h	0202 0048h
4Ch	I2C_DMATXWAKE_EN		0200 004Ch	0201 004Ch	0202 004Ch
84h	I2C_IE		0200 0084h	0201 0084h	0202 0084h
88h	I2C_STAT		0200 0088h	0201 0088h	0202 0088h
90h	I2C_SYSS		0200 0090h	0201 0090h	0202 0090h
94h	I2C_BUF		0200 0094h	0201 0094h	0202 0094h
98h	I2C_CNT		0200 0098h	0201 0098h	0202 0098h
9Ch	I2C_DATA		0200 009Ch	0201 009Ch	0202 009Ch
A4h	I2C_CON		0200 00A4h	0201 00A4h	0202 00A4h
A8h	I2C_OA		0200 00A8h	0201 00A8h	0202 00A8h
ACH	I2C_SA		0200 00ACH	0201 00ACH	0202 00ACH
B0h	I2C_PSC		0200 00B0h	0201 00B0h	0202 00B0h
B4h	I2C_SCLL		0200 00B4h	0201 00B4h	0202 00B4h
B8h	I2C_SCLH		0200 00B8h	0201 00B8h	0202 00B8h
BCh	I2C_SYSTEST		0200 00BCh	0201 00BCh	0202 00BCh
C0h	I2C_BUFSTAT		0200 00C0h	0201 00C0h	0202 00C0h
C4h	I2C_OA1		0200 00C4h	0201 00C4h	0202 00C4h

Table 3-2. I2C Registers (continued)

Offset	Acronym	Register Name	I2C0_CFG Physical Address	I2C1_CFG Physical Address	I2C2_CFG Physical Address
C8h	I2C_OA2		0200 00C8h	0201 00C8h	0202 00C8h
CCh	I2C_OA3		0200 00CCh	0201 00CCh	0202 00CCh
D0h	I2C_ACTOA		0200 00D0h	0201 00D0h	0202 00D0h
D4h	I2C_SBLOCK		0200 00D4h	0201 00D4h	0202 00D4h

Table 3-3. I2C Registers

Offset	Acronym	Register Name	I2C3_CFG Physical Address	I2C4_CFG Physical Address	I2C5_CFG Physical Address
0h	I2C_REVNB_LO		0203 0000h	0204 0000h	0205 0000h
4h	I2C_REVNB_HI		0203 0004h	0204 0004h	0205 0004h
10h	I2C_SYSC		0203 0010h	0204 0010h	0205 0010h
20h	I2C_EOI		0203 0020h	0204 0020h	0205 0020h
24h	I2C_IRQSTATUS_RAW		0203 0024h	0204 0024h	0205 0024h
28h	I2C_IRQSTATUS		0203 0028h	0204 0028h	0205 0028h
2Ch	I2C_IRQENABLE_SET		0203 002Ch	0204 002Ch	0205 002Ch
30h	I2C_IRQENABLE_CLR		0203 0030h	0204 0030h	0205 0030h
34h	I2C_WE		0203 0034h	0204 0034h	0205 0034h
38h	I2C_DMARXENABLE_SET		0203 0038h	0204 0038h	0205 0038h
3Ch	I2C_DMATXENABLE_SET		0203 003Ch	0204 003Ch	0205 003Ch
40h	I2C_DMARXENABLE_CLR		0203 0040h	0204 0040h	0205 0040h
44h	I2C_DMATXENABLE_CLR		0203 0044h	0204 0044h	0205 0044h
48h	I2C_DMARXWAKE_EN		0203 0048h	0204 0048h	0205 0048h
4Ch	I2C_DMATXWAKE_EN		0203 004Ch	0204 004Ch	0205 004Ch
84h	I2C_IE		0203 0084h	0204 0084h	0205 0084h
88h	I2C_STAT		0203 0088h	0204 0088h	0205 0088h
90h	I2C_SYSS		0203 0090h	0204 0090h	0205 0090h
94h	I2C_BUF		0203 0094h	0204 0094h	0205 0094h
98h	I2C_CNT		0203 0098h	0204 0098h	0205 0098h
9Ch	I2C_DATA		0203 009Ch	0204 009Ch	0205 009Ch
A4h	I2C_CON		0203 00A4h	0204 00A4h	0205 00A4h
A8h	I2C_OA		0203 00A8h	0204 00A8h	0205 00A8h
ACh	I2C_SA		0203 00ACh	0204 00ACh	0205 00ACh
B0h	I2C_PSC		0203 00B0h	0204 00B0h	0205 00B0h
B4h	I2C_SCLL		0203 00B4h	0204 00B4h	0205 00B4h
B8h	I2C_SCLH		0203 00B8h	0204 00B8h	0205 00B8h
BCh	I2C_SYSTEST		0203 00BCh	0204 00BCh	0205 00BCh
C0h	I2C_BUFSTAT		0203 00C0h	0204 00C0h	0205 00C0h
C4h	I2C_OA1		0203 00C4h	0204 00C4h	0205 00C4h
C8h	I2C_OA2		0203 00C8h	0204 00C8h	0205 00C8h
CCh	I2C_OA3		0203 00CCh	0204 00CCh	0205 00CCh
D0h	I2C_ACTOA		0203 00D0h	0204 00D0h	0205 00D0h
D4h	I2C_SBLOCK		0203 00D4h	0204 00D4h	0205 00D4h

Table 3-4. I2C Registers

Offset	Acronym	Register Name	I2C6_CFG Physical Address	MCU_I2C0_CFG Physical Address	MCU_I2C1_CFG Physical Address
0h	I2C_REVNB_LO		0206 0000h	40B0 0000h	40B1 0000h

Table 3-4. I2C Registers (continued)

Offset	Acronym	Register Name	I2C6_CFG Physical Address	MCU_I2C0_CFG Physical Address	MCU_I2C1_CFG Physical Address
4h	I2C_REVNB_HI		0206 0004h	40B0 0004h	40B1 0004h
10h	I2C_SYSC		0206 0010h	40B0 0010h	40B1 0010h
20h	I2C_EOI		0206 0020h	40B0 0020h	40B1 0020h
24h	I2C_IRQSTATUS_RAW		0206 0024h	40B0 0024h	40B1 0024h
28h	I2C_IRQSTATUS		0206 0028h	40B0 0028h	40B1 0028h
2Ch	I2C_IRQENABLE_SET		0206 002Ch	40B0 002Ch	40B1 002Ch
30h	I2C_IRQENABLE_CLR		0206 0030h	40B0 0030h	40B1 0030h
34h	I2C_WE		0206 0034h	40B0 0034h	40B1 0034h
38h	I2C_DMARXENABLE_SET		0206 0038h	40B0 0038h	40B1 0038h
3Ch	I2C_DMATXENABLE_SET		0206 003Ch	40B0 003Ch	40B1 003Ch
40h	I2C_DMARXENABLE_CLR		0206 0040h	40B0 0040h	40B1 0040h
44h	I2C_DMATXENABLE_CLR		0206 0044h	40B0 0044h	40B1 0044h
48h	I2C_DMARXWAKE_EN		0206 0048h	40B0 0048h	40B1 0048h
4Ch	I2C_DMATXWAKE_EN		0206 004Ch	40B0 004Ch	40B1 004Ch
84h	I2C_IE		0206 0084h	40B0 0084h	40B1 0084h
88h	I2C_STAT		0206 0088h	40B0 0088h	40B1 0088h
90h	I2C_SYSS		0206 0090h	40B0 0090h	40B1 0090h
94h	I2C_BUF		0206 0094h	40B0 0094h	40B1 0094h
98h	I2C_CNT		0206 0098h	40B0 0098h	40B1 0098h
9Ch	I2C_DATA		0206 009Ch	40B0 009Ch	40B1 009Ch
A4h	I2C_CON		0206 00A4h	40B0 00A4h	40B1 00A4h
A8h	I2C_OA		0206 00A8h	40B0 00A8h	40B1 00A8h
ACh	I2C_SA		0206 00ACh	40B0 00ACh	40B1 00ACh
B0h	I2C_PSC		0206 00B0h	40B0 00B0h	40B1 00B0h
B4h	I2C_SCLL		0206 00B4h	40B0 00B4h	40B1 00B4h
B8h	I2C_SCLH		0206 00B8h	40B0 00B8h	40B1 00B8h
BCh	I2C_SYSTEST		0206 00BCh	40B0 00BCh	40B1 00BCh
C0h	I2C_BUFSTAT		0206 00C0h	40B0 00C0h	40B1 00C0h
C4h	I2C_OA1		0206 00C4h	40B0 00C4h	40B1 00C4h
C8h	I2C_OA2		0206 00C8h	40B0 00C8h	40B1 00C8h
CCh	I2C_OA3		0206 00CCh	40B0 00CCh	40B1 00CCh
D0h	I2C_ACTOA		0206 00D0h	40B0 00D0h	40B1 00D0h
D4h	I2C_SBLOCK		0206 00D4h	40B0 00D4h	40B1 00D4h

Table 3-5. I2C Registers

Offset	Acronym	Register Name	WKUP_I2C0_CFG Physical Address
0h	I2C_REVNB_LO		4212 0000h
4h	I2C_REVNB_HI		4212 0004h
10h	I2C_SYSC		4212 0010h
20h	I2C_EOI		4212 0020h
24h	I2C_IRQSTATUS_RAW		4212 0024h
28h	I2C_IRQSTATUS		4212 0028h
2Ch	I2C_IRQENABLE_SET		4212 002Ch
30h	I2C_IRQENABLE_CLR		4212 0030h
34h	I2C_WE		4212 0034h
38h	I2C_DMARXENABLE_SET		4212 0038h

Table 3-5. I2C Registers (continued)

Offset	Acronym	Register Name	WKUP_I2C0_CFG Physical Address
3Ch	I2C_DMATXENABLE_SET		4212 003Ch
40h	I2C_DMARXENABLE_CLR		4212 0040h
44h	I2C_DMATXENABLE_CLR		4212 0044h
48h	I2C_DMARXWAKE_EN		4212 0048h
4Ch	I2C_DMATXWAKE_EN		4212 004Ch
84h	I2C_IE		4212 0084h
88h	I2C_STAT		4212 0088h
90h	I2C_SYSS		4212 0090h
94h	I2C_BUF		4212 0094h
98h	I2C_CNT		4212 0098h
9Ch	I2C_DATA		4212 009Ch
A4h	I2C_CON		4212 00A4h
A8h	I2C_OA		4212 00A8h
ACCh	I2C_SA		4212 00ACCh
B0h	I2C_PSC		4212 00B0h
B4h	I2C_SCLL		4212 00B4h
B8h	I2C_SCLH		4212 00B8h
BCh	I2C_SYSTEST		4212 00BCh
C0h	I2C_BUFSTAT		4212 00C0h
C4h	I2C_OA1		4212 00C4h
C8h	I2C_OA2		4212 00C8h
CCh	I2C_OA3		4212 00CCh
D0h	I2C_ACTOA		4212 00D0h
D4h	I2C_SBLOCK		4212 00D4h

3.1 I2C_REVNB_LO Register (Offset = 0h) [reset = X]

I2C_REVNB_LO is shown in [Figure 3-1](#) and described in [Table 3-7](#).

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Revision Number register (Low)

Table 3-6. I2C_REVNB_LO Instances

Instance	Physical Address
I2C0_CFG	0200 0000h
I2C1_CFG	0201 0000h
I2C2_CFG	0202 0000h
I2C3_CFG	0203 0000h
I2C4_CFG	0204 0000h
I2C5_CFG	0205 0000h
I2C6_CFG	0206 0000h
MCU_I2C0_CFG	40B0 0000h
MCU_I2C1_CFG	40B1 0000h
WKUP_I2C0_CFG	4212 0000h

Figure 3-1. I2C_REVNB_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM				MINOR			
R-1h				R-0h				R-0h				R-Ch			

LEGEND: R = Read Only; -n = value after reset

Table 3-7. I2C_REVNB_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-11	RTL	R	1h	RTL version This field changes on bug fix, and resets to
10-8	MAJOR	R	0h	Major Revision This field changes when there is a major feature change This field does not change due to bug fix, or minor feature change
7-6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers 0 if non-custom
5-0	MINOR	R	Ch	Minor Revision This field changes when features are scaled up or down This field does not change due to bug fix, or major feature change

3.2 I2C_REVNB_HI Register (Offset = 4h) [reset = X]

I2C_REVNB_HI is shown in [Figure 3-2](#) and described in [Table 3-9](#).

Return to [Summary Table](#).

Revision Number register (High)

Table 3-8. I2C_REVNB_HI Instances

Instance	Physical Address
I2C0_CFG	0200 0004h
I2C1_CFG	0201 0004h
I2C2_CFG	0202 0004h
I2C3_CFG	0203 0004h
I2C4_CFG	0204 0004h
I2C5_CFG	0205 0004h
I2C6_CFG	0206 0004h
MCU_I2C0_CFG	40B0 0004h
MCU_I2C1_CFG	40B1 0004h
WKUP_I2C0_CFG	4212 0004h

Figure 3-2. I2C_REVNB_HI Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
SCHEME		RESERVED			FUNC		
R-1h		R-1h			R-40h		
7	6	5	4	3	2	1	0
FUNC							
R-40h							

LEGEND: R = Read Only; -n = value after reset

Table 3-9. I2C_REVNB_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-14	SCHEME	R	1h	Used to distinguish between old Scheme and current Spare bit to encode future schemes
13-12	RESERVED	R	1h	Reads return 0x1
11-0	FUNC	R	40h	Function: Indicates a software compatible module family

3.3 I2C_SYSC Register (Offset = 10h) [reset = X]

I2C_SYSC is shown in [Figure 3-3](#) and described in [Table 3-11](#).

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System Configuration register

Table 3-10. I2C_SYSC Instances

Instance	Physical Address
I2C0_CFG	0200 0010h
I2C1_CFG	0201 0010h
I2C2_CFG	0202 0010h
I2C3_CFG	0203 0010h
I2C4_CFG	0204 0010h
I2C5_CFG	0205 0010h
I2C6_CFG	0206 0010h
MCU_I2C0_CFG	40B0 0010h
MCU_I2C1_CFG	40B1 0010h
WKUP_I2C0_CFG	4212 0010h

Figure 3-3. I2C_SYSC Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CLKACTIVITY	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED			IDLEMODE		ENAWAKEUP	SRST	AUTOIDLE
R-0h			R/W-0h		R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-11. I2C_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved
9-8	CLKACTIVITY	R/W	0h	Clock Activity selection bits
7-5	RESERVED	R	0h	Reads return 0
4-3	IDLEMODE	R/W	0h	Idle Mode selection bits
2	ENAWAKEUP	R/W	0h	Enable Wakeup control bit
1	SRST	R/W	0h	SoftReset bit
0	AUTOIDLE	R/W	1h	Autoidle bit

3.4 I2C_EOI Register (Offset = 20h) [reset = X]

I2C_EOI is shown in [Figure 3-4](#) and described in [Table 3-13](#).

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End Of Interrupt number specification

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 3-12. I2C_EOI Instances

Instance	Physical Address
I2C0_CFG	0200 0020h
I2C1_CFG	0201 0020h
I2C2_CFG	0202 0020h
I2C3_CFG	0203 0020h
I2C4_CFG	0204 0020h
I2C5_CFG	0205 0020h
I2C6_CFG	0206 0020h
MCU_I2C0_CFG	40B0 0020h
MCU_I2C1_CFG	40B1 0020h
WKUP_I2C0_CFG	4212 0020h

Figure 3-4. I2C_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							LINE_NUMBER
R-0h							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 3-13. I2C_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved
0	LINE_NUMBER	W	0h	Software End Of Interrupt [EOI] control Write number of interrupt output

3.5 I2C_IRQSTATUS_RAW Register (Offset = 24h) [reset = X]

I2C_IRQSTATUS_RAW is shown in [Figure 3-5](#) and described in [Table 3-15](#).

Return to [Summary Table](#).

Per-event raw interrupt status vector

Table 3-14. I2C_IRQSTATUS_RAW Instances

Instance	Physical Address
I2C0_CFG	0200 0024h
I2C1_CFG	0201 0024h
I2C2_CFG	0202 0024h
I2C3_CFG	0203 0024h
I2C4_CFG	0204 0024h
I2C5_CFG	0205 0024h
I2C6_CFG	0206 0024h
MCU_I2C0_CFG	40B0 0024h
MCU_I2C1_CFG	40B1 0024h
WKUP_I2C0_CFG	4212 0024h

Figure 3-5. I2C_IRQSTATUS_RAW Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-15. I2C_IRQSTATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ status
13	RDR	R/W	0h	Receive draining IRQ status
12	BB	R	0h	Bus busy statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as slave IRQ status
8	BF	R/W	0h	Bus Free IRQ status
7	AERR	R/W	0h	Access Error IRQ status
6	STC	R/W	0h	Start Condition IRQ status

Table 3-15. I2C_IRQSTATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GC	R/W	0h	General call IRQ status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear
4	XRDY	R/W	0h	Transmit data ready IRQ status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W	0h	Receive data ready IRQ status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W	0h	Register access ready IRQ status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W	0h	No acknowledgement IRQ status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ status This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

3.6 I2C_IRQSTATUS Register (Offset = 28h) [reset = X]

I2C_IRQSTATUS is shown in [Figure 3-6](#) and described in [Table 3-17](#).

Return to [Summary Table](#).

Per-event enabled interrupt status vector

Table 3-16. I2C_IRQSTATUS Instances

Instance	Physical Address
I2C0_CFG	0200 0028h
I2C1_CFG	0201 0028h
I2C2_CFG	0202 0028h
I2C3_CFG	0203 0028h
I2C4_CFG	0204 0028h
I2C5_CFG	0205 0028h
I2C6_CFG	0206 0028h
MCU_I2C0_CFG	40B0 0028h
MCU_I2C1_CFG	40B1 0028h
WKUP_I2C0_CFG	4212 0028h

Figure 3-6. I2C_IRQSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-17. I2C_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ enabled status
13	RDR	R/W	0h	Receive draining IRQ enabled status
12	BB	R	0h	Bus busy enabled statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun enabled statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow enabled statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as slave IRQ enabled status
8	BF	R/W	0h	Bus Free IRQ enabled status
7	AERR	R/W	0h	Access Error IRQ enabled status
6	STC	R/W	0h	Start Condition IRQ enabled status

Table 3-17. I2C_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GC	R/W	0h	General call IRQ enabled status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear
4	XRDY	R/W	0h	Transmit data ready IRQ enabled status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W	0h	Receive data ready IRQ enabled status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W	0h	Register access ready IRQ enabled status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W	0h	No acknowledgement IRQ enabled status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ enabled status This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

3.7 I2C_IRQENABLE_SET Register (Offset = 2Ch) [reset = X]

I2C_IRQENABLE_SET is shown in [Figure 3-7](#) and described in [Table 3-19](#).

Return to [Summary Table](#).

Per-event interrupt enable bit vector.

Table 3-18. I2C_IRQENABLE_SET Instances

Instance	Physical Address
I2C0_CFG	0200 002Ch
I2C1_CFG	0201 002Ch
I2C2_CFG	0202 002Ch
I2C3_CFG	0203 002Ch
I2C4_CFG	0204 002Ch
I2C5_CFG	0205 002Ch
I2C6_CFG	0206 002Ch
MCU_I2C0_CFG	40B0 002Ch
MCU_I2C1_CFG	40B1 002Ch
WKUP_I2C0_CFG	4212 002Ch

Figure 3-7. I2C_IRQENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-19. I2C_IRQENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable set
10	XUDF	R/W	0h	Transmit underflow enable set
9	ASS_IE	R/W	0h	Addressed as Slave interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]

Table 3-19. I2C_IRQENABLE_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	BF_IE	R/W	0h	Bus Free interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]
7	AERR_IE	R/W	0h	Access Error interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]
6	STC_IE	R/W	0h	Start Condition interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable set Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

3.8 I2C_IRQENABLE_CLR Register (Offset = 30h) [reset = X]

I2C_IRQENABLE_CLR is shown in [Figure 3-8](#) and described in [Table 3-21](#).

Return to [Summary Table](#).

Per-event interrupt clear bit vector.

Table 3-20. I2C_IRQENABLE_CLR Instances

Instance	Physical Address
I2C0_CFG	0200 0030h
I2C1_CFG	0201 0030h
I2C2_CFG	0202 0030h
I2C3_CFG	0203 0030h
I2C4_CFG	0204 0030h
I2C5_CFG	0205 0030h
I2C6_CFG	0206 0030h
MCU_I2C0_CFG	40B0 0030h
MCU_I2C1_CFG	40B1 0030h
WKUP_I2C0_CFG	4212 0030h

Figure 3-8. I2C_IRQENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-21. I2C_IRQENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable clear
10	XUDF	R/W	0h	Transmit underflow enable clear
9	ASS_IE	R/W	0h	Addressed as Slave interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]

Table 3-21. I2C_IRQENABLE_CLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	BF_IE	R/W	0h	Bus Free interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]
7	AERR_IE	R/W	0h	Access Error interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]
6	STC_IE	R/W	0h	Start Condition interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable clear Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

3.9 I2C_WE Register (Offset = 34h) [reset = X]

I2C_WE is shown in [Figure 3-9](#) and described in [Table 3-23](#).

Return to [Summary Table](#).

I2C wakeup enable vector (legacy).

Table 3-22. I2C_WE Instances

Instance	Physical Address
I2C0_CFG	0200 0034h
I2C1_CFG	0201 0034h
I2C2_CFG	0202 0034h
I2C3_CFG	0203 0034h
I2C4_CFG	0204 0034h
I2C5_CFG	0205 0034h
I2C6_CFG	0206 0034h
MCU_I2C0_CFG	40B0 0034h
MCU_I2C1_CFG	40B1 0034h
WKUP_I2C0_CFG	4212 0034h

Figure 3-9. I2C_WE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-23. I2C_WE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as slave IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set

Table 3-23. I2C_WE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED	R	0h	Reserved
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

3.10 I2C_DMARXENABLE_SET Register (Offset = 38h) [reset = X]

I2C_DMARXENABLE_SET is shown in [Figure 3-10](#) and described in [Table 3-25](#).

Return to [Summary Table](#).

Per-event DMA RX enable set.

Table 3-24. I2C_DMARXENABLE_SET Instances

Instance	Physical Address
I2C0_CFG	0200 0038h
I2C1_CFG	0201 0038h
I2C2_CFG	0202 0038h
I2C3_CFG	0203 0038h
I2C4_CFG	0204 0038h
I2C5_CFG	0205 0038h
I2C6_CFG	0206 0038h
MCU_I2C0_CFG	40B0 0038h
MCU_I2C1_CFG	40B1 0038h
WKUP_I2C0_CFG	4212 0038h

Figure 3-10. I2C_DMARXENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DMARX_ENABLE_SET
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-25. I2C_DMARXENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved
0	DMARX_ENABLE_SET	R/W	0h	Receive DMA channel enable set

3.11 I2C_DMATXENABLE_SET Register (Offset = 3Ch) [reset = X]

I2C_DMATXENABLE_SET is shown in [Figure 3-11](#) and described in [Table 3-27](#).

Return to [Summary Table](#).

Per-event DMA TX enable set.

Table 3-26. I2C_DMATXENABLE_SET Instances

Instance	Physical Address
I2C0_CFG	0200 003Ch
I2C1_CFG	0201 003Ch
I2C2_CFG	0202 003Ch
I2C3_CFG	0203 003Ch
I2C4_CFG	0204 003Ch
I2C5_CFG	0205 003Ch
I2C6_CFG	0206 003Ch
MCU_I2C0_CFG	40B0 003Ch
MCU_I2C1_CFG	40B1 003Ch
WKUP_I2C0_CFG	4212 003Ch

Figure 3-11. I2C_DMATXENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DMATX_ENAB LE_SET
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-27. I2C_DMATXENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved
0	DMATX_ENABLE_SET	R/W	0h	Transmit DMA channel enable set

3.12 I2C_DMARXENABLE_CLR Register (Offset = 40h) [reset = X]

I2C_DMARXENABLE_CLR is shown in [Figure 3-12](#) and described in [Table 3-29](#).

Return to [Summary Table](#).

Per-event DMA RX enable clear.

Table 3-28. I2C_DMARXENABLE_CLR Instances

Instance	Physical Address
I2C0_CFG	0200 0040h
I2C1_CFG	0201 0040h
I2C2_CFG	0202 0040h
I2C3_CFG	0203 0040h
I2C4_CFG	0204 0040h
I2C5_CFG	0205 0040h
I2C6_CFG	0206 0040h
MCU_I2C0_CFG	40B0 0040h
MCU_I2C1_CFG	40B1 0040h
WKUP_I2C0_CFG	4212 0040h

Figure 3-12. I2C_DMARXENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DMARX_ENAB LE_CLEAR
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-29. I2C_DMARXENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved
0	DMARX_ENABLE_CLEAR	R/W	0h	Receive DMA channel enable clear

3.13 I2C_DMATXENABLE_CLR Register (Offset = 44h) [reset = X]

I2C_DMATXENABLE_CLR is shown in [Figure 3-13](#) and described in [Table 3-31](#).

Return to [Summary Table](#).

Per-event DMA TX enable clear.

Table 3-30. I2C_DMATXENABLE_CLR Instances

Instance	Physical Address
I2C0_CFG	0200 0044h
I2C1_CFG	0201 0044h
I2C2_CFG	0202 0044h
I2C3_CFG	0203 0044h
I2C4_CFG	0204 0044h
I2C5_CFG	0205 0044h
I2C6_CFG	0206 0044h
MCU_I2C0_CFG	40B0 0044h
MCU_I2C1_CFG	40B1 0044h
WKUP_I2C0_CFG	4212 0044h

Figure 3-13. I2C_DMATXENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DMATX_ENABLE_CLEAR
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-31. I2C_DMATXENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	RESERVED	R	0h	Reserved
0	DMATX_ENABLE_CLEAR	R/W	0h	Transmit DMA channel enable clear

3.14 I2C_DMARXWAKE_EN Register (Offset = 48h) [reset = X]

I2C_DMARXWAKE_EN is shown in [Figure 3-14](#) and described in [Table 3-33](#).

Return to [Summary Table](#).

Per-event DMA RX wakeup enable.

Table 3-32. I2C_DMARXWAKE_EN Instances

Instance	Physical Address
I2C0_CFG	0200 0048h
I2C1_CFG	0201 0048h
I2C2_CFG	0202 0048h
I2C3_CFG	0203 0048h
I2C4_CFG	0204 0048h
I2C5_CFG	0205 0048h
I2C6_CFG	0206 0048h
MCU_I2C0_CFG	40B0 0048h
MCU_I2C1_CFG	40B1 0048h
WKUP_I2C0_CFG	4212 0048h

Figure 3-14. I2C_DMARXWAKE_EN Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-33. I2C_DMARXWAKE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as slave IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set

Table 3-33. I2C_DMARXWAKE_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED	R	0h	Reserved
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

3.15 I2C_DMATXWAKE_EN Register (Offset = 4Ch) [reset = X]

I2C_DMATXWAKE_EN is shown in [Figure 3-15](#) and described in [Table 3-35](#).

Return to [Summary Table](#).

Per-event DMA TX wakeup enable.

Table 3-34. I2C_DMATXWAKE_EN Instances

Instance	Physical Address
I2C0_CFG	0200 004Ch
I2C1_CFG	0201 004Ch
I2C2_CFG	0202 004Ch
I2C3_CFG	0203 004Ch
I2C4_CFG	0204 004Ch
I2C5_CFG	0205 004Ch
I2C6_CFG	0206 004Ch
MCU_I2C0_CFG	40B0 004Ch
MCU_I2C1_CFG	40B1 004Ch
WKUP_I2C0_CFG	4212 004Ch

Figure 3-15. I2C_DMATXWAKE_EN Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	RESERVED	ROVR	XUDF	AAS	BF
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	STC	GC	RESERVED	DRDY	ARDY	NACK	AL
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-35. I2C_DMATXWAKE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R	0h	Reserved
14	XDR	R/W	0h	Transmit Draining wakeup set
13	RDR	R/W	0h	Receive Draining wakeup set
12	RESERVED	R	0h	Reserved
11	ROVR	R/W	0h	Receive overrun wakeup set
10	XUDF	R/W	0h	Transmit underflow wakeup set
9	AAS	R/W	0h	Address as slave IRQ wakeup set
8	BF	R/W	0h	Bus Free IRQ wakeup set
7	RESERVED	R	0h	Reserved
6	STC	R/W	0h	Start Condition IRQ wakeup set

Table 3-35. I2C_DMATXWAKE_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GC	R/W	0h	General call IRQ wakeup set
4	RESERVED	R	0h	Reserved
3	DRDY	R/W	0h	Receive/Transmit data ready IRQ wakeup set
2	ARDY	R/W	0h	Register access ready IRQ wakeup set
1	NACK	R/W	0h	No acknowledgment IRQ wakeup set
0	AL	R/W	0h	Arbitration lost IRQ wakeup set

3.16 I2C_IE Register (Offset = 84h) [reset = X]

I2C_IE is shown in [Figure 3-16](#) and described in [Table 3-37](#).

Return to [Summary Table](#).

I2C interrupt enable vector (legacy).

Table 3-36. I2C_IE Instances

Instance	Physical Address
I2C0_CFG	0200 0084h
I2C1_CFG	0201 0084h
I2C2_CFG	0202 0084h
I2C3_CFG	0203 0084h
I2C4_CFG	0204 0084h
I2C5_CFG	0205 0084h
I2C6_CFG	0206 0084h
MCU_I2C0_CFG	40B0 0084h
MCU_I2C1_CFG	40B1 0084h
WKUP_I2C0_CFG	4212 0084h

Figure 3-16. I2C_IE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR_IE	RDR_IE	RESERVED	ROVR	XUDF	ASS_IE	BF_IE
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR_IE	STC_IE	GC_IE	XRDY_IE	RRDY_IE	ARDY_IE	NACK_IE	AL_IE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-37. I2C_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR_IE	R/W	0h	Transmit Draining interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[XDR]
13	RDR_IE	R/W	0h	Receive Draining interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[RDR]
12	RESERVED	R	0h	reserved
11	ROVR	R/W	0h	Receive overrun enable set
10	XUDF	R/W	0h	Transmit underflow enable set
9	ASS_IE	R/W	0h	Addressed as Slave interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AAS]

Table 3-37. I2C_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	BF_IE	R/W	0h	Bus Free interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[BF]
7	AERR_IE	R/W	0h	Access Error interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AERR]
6	STC_IE	R/W	0h	Start Condition interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[STC]
5	GC_IE	R/W	0h	General call Interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[GC]
4	XRDY_IE	R/W	0h	Transmit data ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[XRDY]
3	RRDY_IE	R/W	0h	Receive data ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[RRDY]
2	ARDY_IE	R/W	0h	Register access ready interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[ARDY]
1	NACK_IE	R/W	0h	No acknowledgement interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[NACK]
0	AL_IE	R/W	0h	Arbitration lost interrupt enable Mask or unmask the interrupt signaled by bit in I2C_STAT[AL]

3.17 I2C_STAT Register (Offset = 88h) [reset = X]

I2C_STAT is shown in [Figure 3-17](#) and described in [Table 3-39](#).

Return to [Summary Table](#).

I2C interrupt status vector (legacy).

Table 3-38. I2C_STAT Instances

Instance	Physical Address
I2C0_CFG	0200 0088h
I2C1_CFG	0201 0088h
I2C2_CFG	0202 0088h
I2C3_CFG	0203 0088h
I2C4_CFG	0204 0088h
I2C5_CFG	0205 0088h
I2C6_CFG	0206 0088h
MCU_I2C0_CFG	40B0 0088h
MCU_I2C1_CFG	40B1 0088h
WKUP_I2C0_CFG	4212 0088h

Figure 3-17. I2C_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	XDR	RDR	BB	ROVR	XUDF	AAS	BF
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AERR	STC	GC	XRDY	RRDY	ARDY	NACK	AL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-39. I2C_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RESERVED	R/W	0h	Write 0s for future compatibility Read returns 0
14	XDR	R/W	0h	Transmit draining IRQ status
13	RDR	R/W	0h	Receive draining IRQ status
12	BB	R	0h	Bus busy statusWriting into this bit has no effect
11	ROVR	R/W	0h	Receive overrun statusWriting into this bit has no effect
10	XUDF	R/W	0h	Transmit underflow statusWriting into this bit has no effect
9	AAS	R/W	0h	Address recognized as slave IRQ status
8	BF	R/W	0h	Bus Free IRQ status
7	AERR	R/W	0h	Access Error IRQ status
6	STC	R/W	0h	Start Condition IRQ status

Table 3-39. I2C_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GC	R/W	0h	General call IRQ status Set to '1' by core when General call address detected and interrupt signaled to MPUSS Write '1' to clear
4	XRDY	R/W	0h	Transmit data ready IRQ status Set to '1' by core when transmitter and when new data is requested When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
3	RRDY	R/W	0h	Receive data ready IRQ status Set to '1' by core when receiver mode, a new data is able to be read When set to '1' by core, an interrupt is signaled to MPUSS Write '1' to clear
2	ARDY	R/W	0h	Register access ready IRQ status When set to '1' it indicates that previous access has been performed and registers are ready to be accessed again An interrupt is signaled to MPUSS Write '1' to clear
1	NACK	R/W	0h	No acknowledgement IRQ status Bit is set when No Acknowledge has been received, an interrupt is signaled to MPUSS Write '1' to clear this bit
0	AL	R/W	0h	Arbitration lost IRQ status This bit is automatically set by the hardware when it loses the Arbitration in master transmit mode, an interrupt is signaled to MPUSS During reads, it always returns 0

3.18 I2C_SYSS Register (Offset = 90h) [reset = X]

I2C_SYSS is shown in [Figure 3-18](#) and described in [Table 3-41](#).

[Return to Summary Table.](#)

System Status register

Table 3-40. I2C_SYSS Instances

Instance	Physical Address
I2C0_CFG	0200 0090h
I2C1_CFG	0201 0090h
I2C2_CFG	0202 0090h
I2C3_CFG	0203 0090h
I2C4_CFG	0204 0090h
I2C5_CFG	0205 0090h
I2C6_CFG	0206 0090h
MCU_I2C0_CFG	40B0 0090h
MCU_I2C1_CFG	40B1 0090h
WKUP_I2C0_CFG	4212 0090h

Figure 3-18. I2C_SYSS Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RDONE
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 3-41. I2C_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-1	RESERVED	R	0h	Reserved
0	RDONE	R	0h	Reset done bit

3.19 I2C_BUF Register (Offset = 94h) [reset = X]

I2C_BUF is shown in [Figure 3-19](#) and described in [Table 3-43](#).

Return to [Summary Table](#).

Buffer Configuration register

Table 3-42. I2C_BUF Instances

Instance	Physical Address
I2C0_CFG	0200 0094h
I2C1_CFG	0201 0094h
I2C2_CFG	0202 0094h
I2C3_CFG	0203 0094h
I2C4_CFG	0204 0094h
I2C5_CFG	0205 0094h
I2C6_CFG	0206 0094h
MCU_I2C0_CFG	40B0 0094h
MCU_I2C1_CFG	40B1 0094h
WKUP_I2C0_CFG	4212 0094h

Figure 3-19. I2C_BUF Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RDMA_EN	RXFIFO_CLR	RXTRSH					
R/W-0h	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
XDMA_EN	TXFIFO_CLR	TXTRSH					
R/W-0h	R/W-0h	R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-43. I2C_BUF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RDMA_EN	R/W	0h	Receive DMA channel enable
14	RXFIFO_CLR	R/W	0h	Receive FIFO clear
13-8	RXTRSH	R/W	0h	Threshold value for FIFO buffer in RX mode
7	XDMA_EN	R/W	0h	Transmit DMA channel enable
6	TXFIFO_CLR	R/W	0h	Transmit FIFO clear
5-0	TXTRSH	R/W	0h	Threshold value for FIFO buffer in TX mode

3.20 I2C_CNT Register (Offset = 98h) [reset = X]

I2C_CNT is shown in [Figure 3-20](#) and described in [Table 3-45](#).

Return to [Summary Table](#).

Data counter register

Table 3-44. I2C_CNT Instances

Instance	Physical Address
I2C0_CFG	0200 0098h
I2C1_CFG	0201 0098h
I2C2_CFG	0202 0098h
I2C3_CFG	0203 0098h
I2C4_CFG	0204 0098h
I2C5_CFG	0205 0098h
I2C6_CFG	0206 0098h
MCU_I2C0_CFG	40B0 0098h
MCU_I2C1_CFG	40B1 0098h
WKUP_I2C0_CFG	4212 0098h

Figure 3-20. I2C_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DCOUNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-45. I2C_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	DCOUNT	R/W	0h	Data count

3.21 I2C_DATA Register (Offset = 9Ch) [reset = X]

I2C_DATA is shown in [Figure 3-21](#) and described in [Table 3-47](#).

Return to [Summary Table](#).

Data access register

Table 3-46. I2C_DATA Instances

Instance	Physical Address
I2C0_CFG	0200 009Ch
I2C1_CFG	0201 009Ch
I2C2_CFG	0202 009Ch
I2C3_CFG	0203 009Ch
I2C4_CFG	0204 009Ch
I2C5_CFG	0205 009Ch
I2C6_CFG	0206 009Ch
MCU_I2C0_CFG	40B0 009Ch
MCU_I2C1_CFG	40B1 009Ch
WKUP_I2C0_CFG	4212 009Ch

Figure 3-21. I2C_DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								DATA							
R/W-X																R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-47. I2C_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	RESERVED	R	0h	Reserved
7-0	DATA	R/W	0h	Transmit/Receive data FIFO endpoint

3.22 I2C_CON Register (Offset = A4h) [reset = X]

I2C_CON is shown in [Figure 3-22](#) and described in [Table 3-49](#).

Return to [Summary Table](#).

I2C configuration register.

Table 3-48. I2C_CON Instances

Instance	Physical Address
I2C0_CFG	0200 00A4h
I2C1_CFG	0201 00A4h
I2C2_CFG	0202 00A4h
I2C3_CFG	0203 00A4h
I2C4_CFG	0204 00A4h
I2C5_CFG	0205 00A4h
I2C6_CFG	0206 00A4h
MCU_I2C0_CFG	40B0 00A4h
MCU_I2C1_CFG	40B1 00A4h
WKUP_I2C0_CFG	4212 00A4h

Figure 3-22. I2C_CON Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
I2C_EN	RESERVED	OPMODE		STB	MST	TRX	XSA
R/W-0h	R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
XOA0	XOA1	XOA2	XOA3	RESERVED		STP	STT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-49. I2C_CON Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	I2C_EN	R/W	0h	I2C module enable
14	RESERVED	R	0h	Reserved
13-12	OPMODE	R/W	0h	Operation mode selection
11	STB	R/W	0h	Start byte mode [master mode only]
10	MST	R/W	0h	Master/slave mode
9	TRX	R/W	0h	Transmitter/Receiver mode [master mode only]
8	XSA	R/W	0h	Expand Slave address
7	XOA0	R/W	0h	Expand Own address 0
6	XOA1	R/W	0h	Expand Own address 1
5	XOA2	R/W	0h	Expand Own address 2

Table 3-49. I2C_CON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XOA3	R/W	0h	Expand Own address 3
3-2	RESERVED	R	0h	Reserved
1	STP	R/W	0h	Stop condition [master mode only]
0	STT	R/W	0h	Start condition [master mode only]

3.23 I2C_OA Register (Offset = A8h) [reset = X]

I2C_OA is shown in [Figure 3-23](#) and described in [Table 3-51](#).

[Return to Summary Table.](#)

Own address register

Table 3-50. I2C_OA Instances

Instance	Physical Address
I2C0_CFG	0200 00A8h
I2C1_CFG	0201 00A8h
I2C2_CFG	0202 00A8h
I2C3_CFG	0203 00A8h
I2C4_CFG	0204 00A8h
I2C5_CFG	0205 00A8h
I2C6_CFG	0206 00A8h
MCU_I2C0_CFG	40B0 00A8h
MCU_I2C1_CFG	40B1 00A8h
WKUP_I2C0_CFG	4212 00A8h

Figure 3-23. I2C_OA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCODE				RESERVED				OA							
R/W-0h				R-0h				R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-51. I2C_OA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	MCODE	R/W	0h	Master Code
12-10	RESERVED	R	0h	Reserved
9-0	OA	R/W	0h	Own address

3.24 I2C_SA Register (Offset = ACh) [reset = X]

I2C_SA is shown in [Figure 3-24](#) and described in [Table 3-53](#).

Return to [Summary Table](#).

Slave address register

Table 3-52. I2C_SA Instances

Instance	Physical Address
I2C0_CFG	0200 00ACh
I2C1_CFG	0201 00ACh
I2C2_CFG	0202 00ACh
I2C3_CFG	0203 00ACh
I2C4_CFG	0204 00ACh
I2C5_CFG	0205 00ACh
I2C6_CFG	0206 00ACh
MCU_I2C0_CFG	40B0 00ACh
MCU_I2C1_CFG	40B1 00ACh
WKUP_I2C0_CFG	4212 00ACh

Figure 3-24. I2C_SA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SA									
R-0h						R/W-3FFh									

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-53. I2C_SA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved
9-0	SA	R/W	3FFh	Slave address

3.25 I2C_PSC Register (Offset = B0h) [reset = X]

I2C_PSC is shown in [Figure 3-25](#) and described in [Table 3-55](#).

Return to [Summary Table](#).

I2C Clock Prescaler Register

Table 3-54. I2C_PSC Instances

Instance	Physical Address
I2C0_CFG	0200 00B0h
I2C1_CFG	0201 00B0h
I2C2_CFG	0202 00B0h
I2C3_CFG	0203 00B0h
I2C4_CFG	0204 00B0h
I2C5_CFG	0205 00B0h
I2C6_CFG	0206 00B0h
MCU_I2C0_CFG	40B0 00B0h
MCU_I2C1_CFG	40B1 00B0h
WKUP_I2C0_CFG	4212 00B0h

Figure 3-25. I2C_PSC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED								PSC							
R/W-X																R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-55. I2C_PSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	RESERVED	R	0h	Reserved
7-0	PSC	R/W	0h	Fast/Standard mode prescale sampling clock divider value 0x 0: Divide by 1 0x 1: Divide by 2 0xFF: Divide by 256

3.26 I2C_SCLL Register (Offset = B4h) [reset = X]

I2C_SCLL is shown in [Figure 3-26](#) and described in [Table 3-57](#).

Return to [Summary Table](#).

I2C_SCL Low Time Register.

Table 3-56. I2C_SCLL Instances

Instance	Physical Address
I2C0_CFG	0200 00B4h
I2C1_CFG	0201 00B4h
I2C2_CFG	0202 00B4h
I2C3_CFG	0203 00B4h
I2C4_CFG	0204 00B4h
I2C5_CFG	0205 00B4h
I2C6_CFG	0206 00B4h
MCU_I2C0_CFG	40B0 00B4h
MCU_I2C1_CFG	40B1 00B4h
WKUP_I2C0_CFG	4212 00B4h

Figure 3-26. I2C_SCLL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSSCLL								SCLL							
R/W-X																R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-57. I2C_SCLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	HSSCLL	R/W	0h	High Speed mode SCL low time
7-0	SCLL	R/W	0h	Fast/Standard mode SCL low time

3.27 I2C_SCLH Register (Offset = B8h) [reset = X]

I2C_SCLH is shown in [Figure 3-27](#) and described in [Table 3-59](#).

Return to [Summary Table](#).

I2C SCL High Time Register.

Table 3-58. I2C_SCLH Instances

Instance	Physical Address
I2C0_CFG	0200 00B8h
I2C1_CFG	0201 00B8h
I2C2_CFG	0202 00B8h
I2C3_CFG	0203 00B8h
I2C4_CFG	0204 00B8h
I2C5_CFG	0205 00B8h
I2C6_CFG	0206 00B8h
MCU_I2C0_CFG	40B0 00B8h
MCU_I2C1_CFG	40B1 00B8h
WKUP_I2C0_CFG	4212 00B8h

Figure 3-27. I2C_SCLH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSSCLH						SCLH									
R/W-X																R/W-0h						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-59. I2C_SCLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	HSSCLH	R/W	0h	High Speed mode SCL high time
7-0	SCLH	R/W	0h	Fast/Standard mode SCL high time

3.28 I2C_SYSTEST Register (Offset = BCh) [reset = X]

I2C_SYSTEST is shown in [Figure 3-28](#) and described in [Table 3-61](#).

Return to [Summary Table](#).

I2C System Test Register.

Table 3-60. I2C_SYSTEST Instances

Instance	Physical Address
I2C0_CFG	0200 00BCh
I2C1_CFG	0201 00BCh
I2C2_CFG	0202 00BCh
I2C3_CFG	0203 00BCh
I2C4_CFG	0204 00BCh
I2C5_CFG	0205 00BCh
I2C6_CFG	0206 00BCh
MCU_I2C0_CFG	40B0 00BCh
MCU_I2C1_CFG	40B1 00BCh
WKUP_I2C0_CFG	4212 00BCh

Figure 3-28. I2C_SYSTEST Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
ST_EN	FREE	TMODE		SSB	RESERVED		SCL_I_FUNC
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R-0h		R-1h
7	6	5	4	3	2	1	0
SCL_O_FUNC	SDA_I_FUNC	SDA_O_FUNC	SCCB_E_O	SCL_I	SCL_O	SDA_I	SDA_O
R-1h	R-1h	R-1h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-61. I2C_SYSTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	ST_EN	R/W	0h	System test enable
14	FREE	R/W	0h	Free running mode [on breakpoint]
13-12	TMODE	R/W	0h	Test mode select
11	SSB	R/W	0h	Set status bits
10-9	RESERVED	R	0h	Reserved
8	SCL_I_FUNC	R	1h	SCL line input value [functional mode]
7	SCL_O_FUNC	R	1h	SCL line output value [functional mode]
6	SDA_I_FUNC	R	1h	SDA line input value [functional mode]
5	SDA_O_FUNC	R	1h	SDA line output value [functional mode]
4	SCCB_E_O	R/W	0h	SCCB_E line sense output value

Table 3-61. I2C_SYSTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SCL_I	R	0h	SCL line sense input value
2	SCL_O	R/W	0h	SCL line drive output value
1	SDA_I	R	0h	SDA line sense input value
0	SDA_O	R/W	0h	SDA line drive output value

3.29 I2C_BUFSTAT Register (Offset = C0h) [reset = X]

I2C_BUFSTAT is shown in [Figure 3-29](#) and described in [Table 3-63](#).

Return to [Summary Table](#).

I2C Buffer Status Register.

Table 3-62. I2C_BUFSTAT Instances

Instance	Physical Address
I2C0_CFG	0200 00C0h
I2C1_CFG	0201 00C0h
I2C2_CFG	0202 00C0h
I2C3_CFG	0203 00C0h
I2C4_CFG	0204 00C0h
I2C5_CFG	0205 00C0h
I2C6_CFG	0206 00C0h
MCU_I2C0_CFG	40B0 00C0h
MCU_I2C1_CFG	40B1 00C0h
WKUP_I2C0_CFG	4212 00C0h

Figure 3-29. I2C_BUFSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
FIFODEPTH				RXSTAT			
R-2h				R-0h			
7	6	5	4	3	2	1	0
RESERVED				TXSTAT			
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 3-63. I2C_BUFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-14	FIFODEPTH	R	2h	Internal FIFO buffers depth
13-8	RXSTAT	R	0h	RX Buffer Status
7-6	RESERVED	R	0h	Reserved
5-0	TXSTAT	R	0h	TX Buffer Status

3.30 I2C_OA1 Register (Offset = C4h) [reset = X]

I2C_OA1 is shown in [Figure 3-30](#) and described in [Table 3-65](#).

Return to [Summary Table](#).

I2C Own Address 1 Register

Table 3-64. I2C_OA1 Instances

Instance	Physical Address
I2C0_CFG	0200 00C4h
I2C1_CFG	0201 00C4h
I2C2_CFG	0202 00C4h
I2C3_CFG	0203 00C4h
I2C4_CFG	0204 00C4h
I2C5_CFG	0205 00C4h
I2C6_CFG	0206 00C4h
MCU_I2C0_CFG	40B0 00C4h
MCU_I2C1_CFG	40B1 00C4h
WKUP_I2C0_CFG	4212 00C4h

Figure 3-30. I2C_OA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						OA1									
R-0h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-65. I2C_OA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved
9-0	OA1	R/W	0h	Own address 1

3.31 I2C_OA2 Register (Offset = C8h) [reset = X]

I2C_OA2 is shown in [Figure 3-31](#) and described in [Table 3-67](#).

Return to [Summary Table](#).

I2C Own Address 2 Register

Table 3-66. I2C_OA2 Instances

Instance	Physical Address
I2C0_CFG	0200 00C8h
I2C1_CFG	0201 00C8h
I2C2_CFG	0202 00C8h
I2C3_CFG	0203 00C8h
I2C4_CFG	0204 00C8h
I2C5_CFG	0205 00C8h
I2C6_CFG	0206 00C8h
MCU_I2C0_CFG	40B0 00C8h
MCU_I2C1_CFG	40B1 00C8h
WKUP_I2C0_CFG	4212 00C8h

Figure 3-31. I2C_OA2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						OA2									
R-0h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-67. I2C_OA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved
9-0	OA2	R/W	0h	Own address 2

3.32 I2C_OA3 Register (Offset = CCh) [reset = X]

I2C_OA3 is shown in [Figure 3-32](#) and described in [Table 3-69](#).

[Return to Summary Table.](#)

I2C Own Address 3 Register

Table 3-68. I2C_OA3 Instances

Instance	Physical Address
I2C0_CFG	0200 00CCh
I2C1_CFG	0201 00CCh
I2C2_CFG	0202 00CCh
I2C3_CFG	0203 00CCh
I2C4_CFG	0204 00CCh
I2C5_CFG	0205 00CCh
I2C6_CFG	0206 00CCh
MCU_I2C0_CFG	40B0 00CCh
MCU_I2C1_CFG	40B1 00CCh
WKUP_I2C0_CFG	4212 00CCh

Figure 3-32. I2C_OA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						OA3									
R-0h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-69. I2C_OA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	RESERVED	R	0h	Reserved
9-0	OA3	R/W	0h	Own address 3

3.33 I2C_ACTOA Register (Offset = D0h) [reset = X]

I2C_ACTOA is shown in [Figure 3-33](#) and described in [Table 3-71](#).

Return to [Summary Table](#).

I2C Active Own Address Register.

Table 3-70. I2C_ACTOA Instances

Instance	Physical Address
I2C0_CFG	0200 00D0h
I2C1_CFG	0201 00D0h
I2C2_CFG	0202 00D0h
I2C3_CFG	0203 00D0h
I2C4_CFG	0204 00D0h
I2C5_CFG	0205 00D0h
I2C6_CFG	0206 00D0h
MCU_I2C0_CFG	40B0 00D0h
MCU_I2C1_CFG	40B1 00D0h
WKUP_I2C0_CFG	4212 00D0h

Figure 3-33. I2C_ACTOA Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				OA3_ACT	OA2_ACT	OA1_ACT	OA0_ACT
R-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 3-71. I2C_ACTOA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-4	RESERVED	R	0h	Reserved
3	OA3_ACT	R	0h	Own Address 3 active
2	OA2_ACT	R	0h	Own Address 2 active
1	OA1_ACT	R	0h	Own Address 1 active
0	OA0_ACT	R	0h	Own Address 0 active

3.34 I2C_SBLOCK Register (Offset = D4h) [reset = X]

I2C_SBLOCK is shown in [Figure 3-34](#) and described in [Table 3-73](#).

Return to [Summary Table](#).

I2C Clock Blocking Enable Register.

Table 3-72. I2C_SBLOCK Instances

Instance	Physical Address
I2C0_CFG	0200 00D4h
I2C1_CFG	0201 00D4h
I2C2_CFG	0202 00D4h
I2C3_CFG	0203 00D4h
I2C4_CFG	0204 00D4h
I2C5_CFG	0205 00D4h
I2C6_CFG	0206 00D4h
MCU_I2C0_CFG	40B0 00D4h
MCU_I2C1_CFG	40B1 00D4h
WKUP_I2C0_CFG	4212 00D4h

Figure 3-34. I2C_SBLOCK Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				OA3_EN	OA2_EN	OA1_EN	OA0_EN
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-73. I2C_SBLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-4	RESERVED	R	0h	Reserved
3	OA3_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 3
2	OA2_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 2
1	OA1_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 1
0	OA0_EN	R/W	0h	Enable I2C Clock Blocking for Own Address 0

4 I3C Registers

4.1 I3C_WRAP_CORE_MST Registers

Table 4-2 lists the I3C_WRAP_CORE_MST registers. All register locations not listed in Table 4-2 should be considered as reserved locations and the register contents should not be modified.

I3C controller configuration and status registers

Table 4-1. I3C_WRAP_CORE_MST Instances

Instance	Base Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8000h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8000h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8000h

Table 4-2. I3C_WRAP_CORE_MST Registers

Offset	Acronym	Register Name	MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
0h	I3C_DEV_ID		40B8 8000h
4h	I3C_CONF_STATUS0		40B8 8004h
8h	I3C_CONF_STATUS1		40B8 8008h
Ch	I3C_REV_ID		40B8 800Ch
10h	I3C_CTRL		40B8 8010h
14h	I3C_PRESCL_CTRL0		40B8 8014h
18h	I3C_PRESCL_CTRL1		40B8 8018h
20h	I3C_MST_IER		40B8 8020h
24h	I3C_MST_IDR		40B8 8024h
28h	I3C_MST_IMR		40B8 8028h
2Ch	I3C_MST_ICR		40B8 802Ch
30h	I3C_MST_ISR		40B8 8030h
34h	I3C_MST_STATUS0		40B8 8034h
38h	I3C_CMDR		40B8 8038h
3Ch	I3C_IBIR		40B8 803Ch
40h	I3C_SLV_IER		40B8 8040h
44h	I3C_SLV_IDR		40B8 8044h
48h	I3C_SLV_IMR		40B8 8048h
4Ch	I3C_SLV_ICR		40B8 804Ch
50h	I3C_SLV_ISR		40B8 8050h
54h	I3C_SLV_STATUS0		40B8 8054h
58h	I3C_SLV_STATUS1		40B8 8058h
60h	I3C_CMD0_FIFO		40B8 8060h
64h	I3C_CMD1_FIFO		40B8 8064h
68h	I3C_TX_FIFO		40B8 8068h
70h	I3C_IMD_CMD0		40B8 8070h
74h	I3C_IMD_CMD1		40B8 8074h
78h	I3C_IMD_DATA		40B8 8078h
80h	I3C_RX_FIFO		40B8 8080h
84h	I3C_IBI_DATA_FIFO		40B8 8084h
88h	I3C_SLV_DDR_TX_FIFO		40B8 8088h
8Ch	I3C_SLV_DDR_RX_FIFO		40B8 808Ch
90h	I3C_CMD_IBI_THR_CTRL		40B8 8090h

Table 4-2. I3C_WRAP_CORE_MST Registers (continued)

Offset	Acronym	Register Name	MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
94h	I3C_TX_RX_THR_CTRL		40B8 8094h
98h	I3C_SLV_DDR_TX_RX_THR_CTRL		40B8 8098h
9Ch	I3C_FLUSH_CTRL		40B8 809Ch
B0h	I3C_TTO_PRESCCL_CTRL0		40B8 80B0h
B4h	I3C_TTO_PRESCCL_CTRL1		40B8 80B4h
B8h	I3C_DEVS_CTRL		40B8 80B8h
C0h	I3C_DEV_ID0_RR0		40B8 80C0h
C4h	I3C_DEV_ID0_RR1		40B8 80C4h
C8h	I3C_DEV_ID0_RR2		40B8 80C8h
D0h	I3C_DEV_ID1_RR0		40B8 80D0h
D4h	I3C_DEV_ID1_RR1		40B8 80D4h
D8h	I3C_DEV_ID1_RR2		40B8 80D8h
E0h	I3C_DEV_ID2_RR0		40B8 80E0h
E4h	I3C_DEV_ID2_RR1		40B8 80E4h
E8h	I3C_DEV_ID2_RR2		40B8 80E8h
F0h	I3C_DEV_ID3_RR0		40B8 80F0h
F4h	I3C_DEV_ID3_RR1		40B8 80F4h
F8h	I3C_DEV_ID3_RR2		40B8 80F8h
100h	I3C_DEV_ID4_RR0		40B8 8100h
104h	I3C_DEV_ID4_RR1		40B8 8104h
108h	I3C_DEV_ID4_RR2		40B8 8108h
110h	I3C_DEV_ID5_RR0		40B8 8110h
114h	I3C_DEV_ID5_RR1		40B8 8114h
118h	I3C_DEV_ID5_RR2		40B8 8118h
120h	I3C_DEV_ID6_RR0		40B8 8120h
124h	I3C_DEV_ID6_RR1		40B8 8124h
128h	I3C_DEV_ID6_RR2		40B8 8128h
130h	I3C_DEV_ID7_RR0		40B8 8130h
134h	I3C_DEV_ID7_RR1		40B8 8134h
138h	I3C_DEV_ID7_RR2		40B8 8138h
140h	I3C_DEV_ID8_RR0		40B8 8140h
144h	I3C_DEV_ID8_RR1		40B8 8144h
148h	I3C_DEV_ID8_RR2		40B8 8148h
150h	I3C_DEV_ID9_RR0		40B8 8150h
154h	I3C_DEV_ID9_RR1		40B8 8154h
158h	I3C_DEV_ID9_RR2		40B8 8158h
160h	I3C_DEV_ID10_RR0		40B8 8160h
164h	I3C_DEV_ID10_RR1		40B8 8164h
168h	I3C_DEV_ID10_RR2		40B8 8168h
170h	I3C_DEV_ID11_RR0		40B8 8170h
174h	I3C_DEV_ID11_RR1		40B8 8174h
178h	I3C_DEV_ID11_RR2		40B8 8178h
180h	I3C_SIR_MAP0		40B8 8180h
184h	I3C_SIR_MAP1		40B8 8184h
188h	I3C_SIR_MAP2		40B8 8188h
18Ch	I3C_SIR_MAP3		40B8 818Ch

Table 4-2. I3C_WRAP_CORE_MST Registers (continued)

Offset	Acronym	Register Name	MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
190h	I3C_SIR_MAP4		40B8 8190h
194h	I3C_SIR_MAP5		40B8 8194h
1A0h	I3C_GPIR_WORD0		40B8 81A0h
220h	I3C_GPOR_WORD0		40B8 8220h
300h	I3C_ASF_INT_STATUS		40B8 8300h
304h	I3C_ASF_INT_RAW_STATUS		40B8 8304h
308h	I3C_ASF_INT_MASK		40B8 8308h
30Ch	I3C_ASF_INT_TEST		40B8 830Ch
310h	I3C_ASF_FATAL_NONFATAL_SELECT		40B8 8310h
320h	I3C_ASF_SRAM_CORR_FAULT_STATUS		40B8 8320h
324h	I3C_ASF_SRAM_UNCORR_FAULT_STATUS		40B8 8324h
328h	I3C_ASF_SRAM_FAULT_STATS		40B8 8328h
330h	I3C_ASF_TRANS_TO_CTRL		40B8 8330h
334h	I3C_ASF_TRANS_TO_FAULT_MASK		40B8 8334h
338h	I3C_ASF_TRANS_TO_FAULT_STATUS		40B8 8338h
340h	I3C_ASF_PROTOCOL_FAULT_MASK		40B8 8340h
344h	I3C_ASF_PROTOCOL_FAULT_STATUS		40B8 8344h

Table 4-3. I3C_WRAP_CORE_MST Registers

Offset	Acronym	Register Name	MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
0h	I3C_DEV_ID		40B9 8000h
4h	I3C_CONF_STATUS0		40B9 8004h
8h	I3C_CONF_STATUS1		40B9 8008h
Ch	I3C_REV_ID		40B9 800Ch
10h	I3C_CTRL		40B9 8010h
14h	I3C_PRESCCL_CTRL0		40B9 8014h
18h	I3C_PRESCCL_CTRL1		40B9 8018h
20h	I3C_MST_IER		40B9 8020h
24h	I3C_MST_IDR		40B9 8024h
28h	I3C_MST_IMR		40B9 8028h
2Ch	I3C_MST_ICR		40B9 802Ch
30h	I3C_MST_ISR		40B9 8030h
34h	I3C_MST_STATUS0		40B9 8034h
38h	I3C_CMDR		40B9 8038h
3Ch	I3C_IBIR		40B9 803Ch
40h	I3C_SLV_IER		40B9 8040h
44h	I3C_SLV_IDR		40B9 8044h
48h	I3C_SLV_IMR		40B9 8048h
4Ch	I3C_SLV_ICR		40B9 804Ch
50h	I3C_SLV_ISR		40B9 8050h
54h	I3C_SLV_STATUS0		40B9 8054h
58h	I3C_SLV_STATUS1		40B9 8058h
60h	I3C_CMD0_FIFO		40B9 8060h
64h	I3C_CMD1_FIFO		40B9 8064h
68h	I3C_TX_FIFO		40B9 8068h
70h	I3C_IMD_CMD0		40B9 8070h

Table 4-3. I3C_WRAP_CORE_MST Registers (continued)

Offset	Acronym	Register Name	MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
74h	I3C_IMD_CMD1		40B9 8074h
78h	I3C_IMD_DATA		40B9 8078h
80h	I3C_RX_FIFO		40B9 8080h
84h	I3C_IBI_DATA_FIFO		40B9 8084h
88h	I3C_SLV_DDR_TX_FIFO		40B9 8088h
8Ch	I3C_SLV_DDR_RX_FIFO		40B9 808Ch
90h	I3C_CMD_IBI_THR_CTRL		40B9 8090h
94h	I3C_TX_RX_THR_CTRL		40B9 8094h
98h	I3C_SLV_DDR_TX_RX_THR_CTRL		40B9 8098h
9Ch	I3C_FLUSH_CTRL		40B9 809Ch
B0h	I3C_TTO_PRESCCL_CTRL0		40B9 80B0h
B4h	I3C_TTO_PRESCCL_CTRL1		40B9 80B4h
B8h	I3C_DEVS_CTRL		40B9 80B8h
C0h	I3C_DEV_ID0_RR0		40B9 80C0h
C4h	I3C_DEV_ID0_RR1		40B9 80C4h
C8h	I3C_DEV_ID0_RR2		40B9 80C8h
D0h	I3C_DEV_ID1_RR0		40B9 80D0h
D4h	I3C_DEV_ID1_RR1		40B9 80D4h
D8h	I3C_DEV_ID1_RR2		40B9 80D8h
E0h	I3C_DEV_ID2_RR0		40B9 80E0h
E4h	I3C_DEV_ID2_RR1		40B9 80E4h
E8h	I3C_DEV_ID2_RR2		40B9 80E8h
F0h	I3C_DEV_ID3_RR0		40B9 80F0h
F4h	I3C_DEV_ID3_RR1		40B9 80F4h
F8h	I3C_DEV_ID3_RR2		40B9 80F8h
100h	I3C_DEV_ID4_RR0		40B9 8100h
104h	I3C_DEV_ID4_RR1		40B9 8104h
108h	I3C_DEV_ID4_RR2		40B9 8108h
110h	I3C_DEV_ID5_RR0		40B9 8110h
114h	I3C_DEV_ID5_RR1		40B9 8114h
118h	I3C_DEV_ID5_RR2		40B9 8118h
120h	I3C_DEV_ID6_RR0		40B9 8120h
124h	I3C_DEV_ID6_RR1		40B9 8124h
128h	I3C_DEV_ID6_RR2		40B9 8128h
130h	I3C_DEV_ID7_RR0		40B9 8130h
134h	I3C_DEV_ID7_RR1		40B9 8134h
138h	I3C_DEV_ID7_RR2		40B9 8138h
140h	I3C_DEV_ID8_RR0		40B9 8140h
144h	I3C_DEV_ID8_RR1		40B9 8144h
148h	I3C_DEV_ID8_RR2		40B9 8148h
150h	I3C_DEV_ID9_RR0		40B9 8150h
154h	I3C_DEV_ID9_RR1		40B9 8154h
158h	I3C_DEV_ID9_RR2		40B9 8158h
160h	I3C_DEV_ID10_RR0		40B9 8160h
164h	I3C_DEV_ID10_RR1		40B9 8164h
168h	I3C_DEV_ID10_RR2		40B9 8168h

Table 4-3. I3C_WRAP_CORE_MST Registers (continued)

Offset	Acronym	Register Name	MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
170h	I3C_DEV_ID11_RR0		40B9 8170h
174h	I3C_DEV_ID11_RR1		40B9 8174h
178h	I3C_DEV_ID11_RR2		40B9 8178h
180h	I3C_SIR_MAP0		40B9 8180h
184h	I3C_SIR_MAP1		40B9 8184h
188h	I3C_SIR_MAP2		40B9 8188h
18Ch	I3C_SIR_MAP3		40B9 818Ch
190h	I3C_SIR_MAP4		40B9 8190h
194h	I3C_SIR_MAP5		40B9 8194h
1A0h	I3C_GPIR_WORD0		40B9 81A0h
220h	I3C_GPOR_WORD0		40B9 8220h
300h	I3C_ASF_INT_STATUS		40B9 8300h
304h	I3C_ASF_INT_RAW_STATUS		40B9 8304h
308h	I3C_ASF_INT_MASK		40B9 8308h
30Ch	I3C_ASF_INT_TEST		40B9 830Ch
310h	I3C_ASF_FATAL_NONFATAL_SELECT		40B9 8310h
320h	I3C_ASF_SRAM_CORR_FAULT_STATUS		40B9 8320h
324h	I3C_ASF_SRAM_UNCORR_FAULT_STATUS		40B9 8324h
328h	I3C_ASF_SRAM_FAULT_STATS		40B9 8328h
330h	I3C_ASF_TRANS_TO_CTRL		40B9 8330h
334h	I3C_ASF_TRANS_TO_FAULT_MASK		40B9 8334h
338h	I3C_ASF_TRANS_TO_FAULT_STATUS		40B9 8338h
340h	I3C_ASF_PROTOCOL_FAULT_MASK		40B9 8340h
344h	I3C_ASF_PROTOCOL_FAULT_STATUS		40B9 8344h

Table 4-4. I3C_WRAP_CORE_MST Registers

Offset	Acronym	Register Name	I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
0h	I3C_DEV_ID		020A 8000h
4h	I3C_CONF_STATUS0		020A 8004h
8h	I3C_CONF_STATUS1		020A 8008h
Ch	I3C_REV_ID		020A 800Ch
10h	I3C_CTRL		020A 8010h
14h	I3C_PRESCCL_CTRL0		020A 8014h
18h	I3C_PRESCCL_CTRL1		020A 8018h
20h	I3C_MST_IER		020A 8020h
24h	I3C_MST_IDR		020A 8024h
28h	I3C_MST_IMR		020A 8028h
2Ch	I3C_MST_ICR		020A 802Ch
30h	I3C_MST_ISR		020A 8030h
34h	I3C_MST_STATUS0		020A 8034h
38h	I3C_CMDR		020A 8038h
3Ch	I3C_IBIR		020A 803Ch
40h	I3C_SLV_IER		020A 8040h
44h	I3C_SLV_IDR		020A 8044h
48h	I3C_SLV_IMR		020A 8048h
4Ch	I3C_SLV_ICR		020A 804Ch

Table 4-4. I3C_WRAP_CORE_MST Registers (continued)

Offset	Acronym	Register Name	I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
50h	I3C_SLV_ISR		020A 8050h
54h	I3C_SLV_STATUS0		020A 8054h
58h	I3C_SLV_STATUS1		020A 8058h
60h	I3C_CMD0_FIFO		020A 8060h
64h	I3C_CMD1_FIFO		020A 8064h
68h	I3C_TX_FIFO		020A 8068h
70h	I3C_IMD_CMD0		020A 8070h
74h	I3C_IMD_CMD1		020A 8074h
78h	I3C_IMD_DATA		020A 8078h
80h	I3C_RX_FIFO		020A 8080h
84h	I3C_IBI_DATA_FIFO		020A 8084h
88h	I3C_SLV_DDR_TX_FIFO		020A 8088h
8Ch	I3C_SLV_DDR_RX_FIFO		020A 808Ch
90h	I3C_CMD_IBI_THR_CTRL		020A 8090h
94h	I3C_TX_RX_THR_CTRL		020A 8094h
98h	I3C_SLV_DDR_TX_RX_THR_CTRL		020A 8098h
9Ch	I3C_FLUSH_CTRL		020A 809Ch
B0h	I3C_TTO_PRESCCL_CTRL0		020A 80B0h
B4h	I3C_TTO_PRESCCL_CTRL1		020A 80B4h
B8h	I3C_DEVS_CTRL		020A 80B8h
C0h	I3C_DEV_ID0_RR0		020A 80C0h
C4h	I3C_DEV_ID0_RR1		020A 80C4h
C8h	I3C_DEV_ID0_RR2		020A 80C8h
D0h	I3C_DEV_ID1_RR0		020A 80D0h
D4h	I3C_DEV_ID1_RR1		020A 80D4h
D8h	I3C_DEV_ID1_RR2		020A 80D8h
E0h	I3C_DEV_ID2_RR0		020A 80E0h
E4h	I3C_DEV_ID2_RR1		020A 80E4h
E8h	I3C_DEV_ID2_RR2		020A 80E8h
F0h	I3C_DEV_ID3_RR0		020A 80F0h
F4h	I3C_DEV_ID3_RR1		020A 80F4h
F8h	I3C_DEV_ID3_RR2		020A 80F8h
100h	I3C_DEV_ID4_RR0		020A 8100h
104h	I3C_DEV_ID4_RR1		020A 8104h
108h	I3C_DEV_ID4_RR2		020A 8108h
110h	I3C_DEV_ID5_RR0		020A 8110h
114h	I3C_DEV_ID5_RR1		020A 8114h
118h	I3C_DEV_ID5_RR2		020A 8118h
120h	I3C_DEV_ID6_RR0		020A 8120h
124h	I3C_DEV_ID6_RR1		020A 8124h
128h	I3C_DEV_ID6_RR2		020A 8128h
130h	I3C_DEV_ID7_RR0		020A 8130h
134h	I3C_DEV_ID7_RR1		020A 8134h
138h	I3C_DEV_ID7_RR2		020A 8138h
140h	I3C_DEV_ID8_RR0		020A 8140h
144h	I3C_DEV_ID8_RR1		020A 8144h

Table 4-4. I3C_WRAP_CORE_MST Registers (continued)

Offset	Acronym	Register Name	I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST Physical Address
148h	I3C_DEV_ID8_RR2		020A 8148h
150h	I3C_DEV_ID9_RR0		020A 8150h
154h	I3C_DEV_ID9_RR1		020A 8154h
158h	I3C_DEV_ID9_RR2		020A 8158h
160h	I3C_DEV_ID10_RR0		020A 8160h
164h	I3C_DEV_ID10_RR1		020A 8164h
168h	I3C_DEV_ID10_RR2		020A 8168h
170h	I3C_DEV_ID11_RR0		020A 8170h
174h	I3C_DEV_ID11_RR1		020A 8174h
178h	I3C_DEV_ID11_RR2		020A 8178h
180h	I3C_SIR_MAP0		020A 8180h
184h	I3C_SIR_MAP1		020A 8184h
188h	I3C_SIR_MAP2		020A 8188h
18Ch	I3C_SIR_MAP3		020A 818Ch
190h	I3C_SIR_MAP4		020A 8190h
194h	I3C_SIR_MAP5		020A 8194h
1A0h	I3C_GPIR_WORD0		020A 81A0h
220h	I3C_GPOR_WORD0		020A 8220h
300h	I3C_ASF_INT_STATUS		020A 8300h
304h	I3C_ASF_INT_RAW_STATUS		020A 8304h
308h	I3C_ASF_INT_MASK		020A 8308h
30Ch	I3C_ASF_INT_TEST		020A 830Ch
310h	I3C_ASF_FATAL_NONFATAL_SELECT		020A 8310h
320h	I3C_ASF_SRAM_CORR_FAULT_STATUS		020A 8320h
324h	I3C_ASF_SRAM_UNCORR_FAULT_STATUS		020A 8324h
328h	I3C_ASF_SRAM_FAULT_STATS		020A 8328h
330h	I3C_ASF_TRANS_TO_CTRL		020A 8330h
334h	I3C_ASF_TRANS_TO_FAULT_MASK		020A 8334h
338h	I3C_ASF_TRANS_TO_FAULT_STATUS		020A 8338h
340h	I3C_ASF_PROTOCOL_FAULT_MASK		020A 8340h
344h	I3C_ASF_PROTOCOL_FAULT_STATUS		020A 8344h

4.2 I3C_DEV_ID Register (Offset = 0h) [reset = 5034h]

I3C_DEV_ID is shown in [Figure 4-1](#) and described in [Table 4-6](#).

Return to the [Summary Table](#).

This register holds the IP identifier.

Table 4-5. I3C_DEV_ID Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8000h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8000h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8000h

Figure 4-1. I3C_DEV_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD0																DEV_ID															
R-0h																R-5034h															

LEGEND: R = Read Only; -n = value after reset

Table 4-6. I3C_DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD0	R	0h	Reserved.
15-0	DEV_ID	R	5034h	Unique IP identifier within IP portfolio

4.3 I3C_CONF_STATUS0 Register (Offset = 4h) [reset = 7F01016Bh]

I3C_CONF_STATUS0 is shown in [Figure 4-2](#) and described in [Table 4-8](#).

Return to the [Summary Table](#).

The read-only Configuration Status Register 0 indicates the hardware configuration options chosen for implementation of the I3C-Master.

Table 4-7. I3C_CONF_STATUS0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8004h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8004h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8004h

Figure 4-2. I3C_CONF_STATUS0 Register

31	30	29	28	27	26	25	24
CMDR_MEM_DEPTH				ASF			
R-3h				R-1Fh			
23	22	21	20	19	18	17	16
GPO_NUM							
R-1h							
15	14	13	12	11	10	9	8
GPI_NUM							
R-1h							
7	6	5	4	3	2	1	0
IBIR_MEM_DEPTH		DDR	DEV_ROLE	DEVS_NUM			
R-1h		R-1h	R-0h	R-Bh			

LEGEND: R = Read Only; -n = value after reset

Table 4-8. I3C_CONF_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	CMDR_MEM_DEPTH	R	3h	CMD Resp MEM depth coded into 3 bits.
28-24	ASF	R	1Fh	Indicates supported ASF checks.
23-16	GPO_NUM	R	1h	Returns the value of User GPO [1-126].
15-8	GPI_NUM	R	1h	Returns the value of User GPI [1-126].
7-6	IBIR_MEM_DEPTH	R	1h	IBI Resp MEM depth coded into 2 bits.
5	DDR	R	1h	Indicates if DDR is supported.
4	DEV_ROLE	R	0h	Returns status of Device Role [Main/Secondary Master].
3-0	DEVS_NUM	R	Bh	Returns the number of retaining registers for I3C Slave devices [Addresses and Characteristics], the max value is 11.

4.4 I3C_CONF_STATUS1 Register (Offset = 8h) [reset = ACC61127h]

I3C_CONF_STATUS1 is shown in [Figure 4-3](#) and described in [Table 4-10](#).

Return to the [Summary Table](#).

The read-only Configuration Status Register 1 indicates the hardware configuration options chosen for implementation of the I3C-Master.

Table 4-9. I3C_CONF_STATUS1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8008h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8008h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8008h

Figure 4-3. I3C_CONF_STATUS1 Register

31	30	29	28	27	26	25	24
IBI_HW_RES				CMD_MEM_DEPTH		SLV_DDR_RX_MEM_DEPTH	
R-Ah				R-3h		R-6h	
23	22	21	20	19	18	17	16
SLV_DDR_RX_MEM_DEPTH				SLV_DDR_TX_MEM_DEPTH			
R-6h				R-6h			
15	14	13	12	11	10	9	8
RSVD0				IBI_MEM_DEPTH		RX_MEM_DEPTH	
R-0h				R-4h		R-9h	
7	6	5	4	3	2	1	0
RX_MEM_DEPTH				TX_MEM_DEPTH			
R-9h				R-7h			

LEGEND: R = Read Only; -n = value after reset

Table 4-10. I3C_CONF_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	IBI_HW_RES	R	Ah	IBI resources
27-26	CMD_MEM_DEPTH	R	3h	CMD FIFO depth coded into 3 bits.
25-21	SLV_DDR_RX_MEM_DEPTH	R	6h	SLV DDR RX FIFO depth coded into 5 bits.
20-16	SLV_DDR_TX_MEM_DEPTH	R	6h	SLV DDR TX FIFO depth coded into 5 bits.
15-13	RSVD0	R	0h	Reserved.
12-10	IBI_MEM_DEPTH	R	4h	IBI FIFO depth coded into 3 bits.
9-5	RX_MEM_DEPTH	R	9h	RX FIFO depth coded into 5 bits.
4-0	TX_MEM_DEPTH	R	7h	TX FIFO depth coded into 5 bits.

4.5 I3C_REV_ID Register (Offset = Ch) [reset = CAD13C25h]

I3C_REV_ID is shown in [Figure 4-4](#) and described in [Table 4-12](#).

Return to the [Summary Table](#).

This register gives an information about particular version of the IP.

Table 4-11. I3C_REV_ID Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 800Ch
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 800Ch
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 800Ch

Figure 4-4. I3C_REV_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VID												PID			
R-CADh												R-13Ch			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID								REV_MAJOR			REV_MINOR				
R-13Ch								R-1h			R-5h				

LEGEND: R = Read Only; -n = value after reset

Table 4-12. I3C_REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	VID	R	CADh	VENDOR_ID: IP vendor ID affected to IP [reset = 0xCAD].
19-8	PID	R	13Ch	PRODUCT_ID: unique IP identifier within CDNS IP portfolio [reset = 0x13C].
7-5	REV_MAJOR	R	1h	X: Major revision value.
4-0	REV_MINOR	R	5h	Y: Minor revision value.

4.6 I3C_CTRL Register (Offset = 10h) [reset = C0h]

I3C_CTRL is shown in [Figure 4-5](#) and described in [Table 4-14](#).

Return to the [Summary Table](#).

Control Register for I3C Master IP - register that provides main control and configuration options for the controller.

Table 4-13. I3C_CTRL Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8010h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8010h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8010h

Figure 4-5. I3C_CTRL Register

31	30	29	28	27	26	25	24
DEV_EN	HALT_EN	MCS	MCS_EN	RSVD2	I3C_11_SUPP	THD_DEL	
R/W-0h	R/W-0h	W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
RSVD1							
R-0h							
15	14	13	12	11	10	9	8
RSVD1						HJ_DISEC	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
MST_ACK	HJ_ACK	HJ_INIT	MST_INIT	AHDR_OPT	RSVD0	BUS_MODE	
R/W-1h	R/W-1h	W-0h	W-0h	R/W-0h	R-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-14. I3C_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DEV_EN	R/W	0h	<p>When set HIGH the I3C-Master is enabled and it can initiate the I3C/I2C transactions.</p> <p>Also write access to the following fields of various registers is forbidden :</p> <p>I3C_CTRL.bus_mode I3C_CTRL.ahdr_opt I3C_CTRL.halt_en I3C_PRESCAL_CTRL0.i3c I3C_PRESCAL_CTRL0.i2c I3C_PRESCAL_CTRL1.od_low I3C_PRESCAL_CTRL1.pp_low</p> <p>When set LOW the I3C-Master is disabled and access to the key control fields that listed above is available.</p> <p>If this bit is being set to 0 during ongoing transfer then it will wait until the transfer completion and then the controller will be disabled.</p> <p>I3C Master IP is returned by I3C_MST_STATUS0.idle bit of Status Register and this field should be checked before accessing key control fields.</p>
30	HALT_EN	R/W	0h	Enable halt on abort behavior.
29	MCS	W	0h	<p>Manual Command Start writing 1 starts execution of the commands currently in CMD Memories.</p> <p>Self-cleared bit.</p> <p>Relevant only if MCS_EN bit [I3C_CTRL.mcs_en] set to 1, disregarded otherwise.</p>
28	MCS_EN	R/W	0h	<p>Manual Command Start Enable if set 1 the IP will wait with starting of command execution until MCS but [I3C_CTRL.mcs] would be set 1.</p> <p>If set to 0, the IP will start execute commands automatically as soon as at least one is present in the CMD MEM and the MCS [I3C_CTRL.mcs] bit is disregarded.</p>
27	RSVD2	R	0h	Reserved.
26	I3C_11_SUPP	R/W	0h	<p>Enables support for timing parameter that has been changed in v1.1, i.e.</p> <p>tCASr_min.</p> <p>If: 1'b</p> <p>0 - then tCASr_min = tCAS_min [as per MIPI spec v1.0], 1'b</p> <p>1 - then tCASr_min = tCAS_min/2 [as per draft version of MIPI spec v1.0]</p>
25-24	THD_DEL	R/W	0h	<p>Field that provides option to add data hold delay with respect to the SCL clock on which data on SDA is launched [applied only during actual Data transfer]</p> <p>00 - adds delay of 3x sys_clock cycles, 01 - adds delay of 2x sys_clk clock cycles, 10 - adds delay of 1x sys_clk clock cycles, 11 - no delay [data is launched simultaneously with SCL clock edge].</p>
23-9	RSVD1	R	0h	Reserved.

Table 4-14. I3C_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	HJ_DISEC	R/W	0h	This bit controls the HW response for ACK'ed HJ request. When set HIGH, then the DISEC CCC is used. Otherwise, if set LOW the ENTDAACCC is used. This control bit is meaningful if hj_ack=1 and controller operates in Main Master configuration.
7	MST_ACK	R/W	1h	Specifies ACK response type for GETACCMST CCC, it can be either ACK response type [mst_ack = 1] or NACK response type [mst_ack = 0]. This control bit is meaningful in Slave Mode only.
6	HJ_ACK	R/W	1h	Specifies ACK response type for HJ request, it can be either ACK response type [hj_ack = 1] or NACK response type [hj_ack = 0]. For Secondary Master configuration, this bit tied off to 0.
5	HJ_INIT	W	0h	Initiate HJ request - applicable only for Secondary master in slave mode. Self-cleared bit.
4	MST_INIT	W	0h	Initiate Mastership request - applicable only in slave mode. When set in master mode this bit has no effect. Self-cleared bit.
3	AHDR_OPT	R/W	0h	Enable[1]/Disable[0] the Address Header optimization. If enabled, FW needs to restrict DAs to 0x03 - 0x3F range.
2	RSVD0	R	0h	Reserved
1-0	BUS_MODE	R/W	0h	Bus Mode 00 : Pure Bus Mode 01 : Invalid Config 10 : Mixed Fast Bus Mode 11 : Mixed Slow/Limited Bus Mode

4.7 I3C_PRESCL_CTRL0 Register (Offset = 14h) [reset = 007C0004h]

I3C_PRESCL_CTRL0 is shown in [Figure 4-6](#) and described in [Table 4-16](#).

Return to the [Summary Table](#).

Prescale settings for SDR/I2C modes

Table 4-15. I3C_PRESCL_CTRL0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8014h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8014h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8014h

Figure 4-6. I3C_PRESCL_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C																RSVD0				I3C											
R/W-7Ch																R-0h				R/W-4h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-16. I3C_PRESCL_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	I2C	R/W	7Ch	Prescaler value for I2C SCL clock generation. It should be generated based on sys clock freq and should be 5x w.r.t. to the slowest I2C device's SCL speed: presc_ctl_i2c [15:0] = sys_clk_freq / [i2c_freq * 5] - 1'b1 if presc_ctl_i2c [15:0] == 0 - no sys_clk division
15-10	RSVD0	R	0h	Reserved
9-0	I3C	R/W	4h	Prescaler value for I3C Push-Pull SDR Mode SCL clock generation. When the bus is configured in mixed fast mode, the resulting SCL frequency must be faster than 11MHz. It should be generated based on sys clock freq and should be 4x w.r.t. to the SDR SCL speed: presc_ctl_i3c [9:0] = [sys_clk_freq / sdr_freq * 4] - 1'b1 If sys_clk == 4*sdr_freq, presc_ctl_i3c [9:0] should be 0

4.8 I3C_PRESCL_CTRL1 Register (Offset = 18h) [reset = X]

I3C_PRESCL_CTRL1 is shown in [Figure 4-7](#) and described in [Table 4-18](#).

[Return to the Summary Table.](#)

Prescale settings related to Open Drain / Push Pull I3C timings

Table 4-17. I3C_PRESCL_CTRL1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8018h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8018h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8018h

Figure 4-7. I3C_PRESCL_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PP_LOW				OD_LOW											
R/W-X																R/W-0h				R/W-9h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-18. I3C_PRESCL_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PP_LOW	R/W	0h	Counter for low period of SCL clock for Push Pull in I3C. When particular I3C device does not support Max SCL speed, low period stretching is required for PP as well. Controller will determine that by inspecting BCR[0] bit. When BCR[0] is 0, SCL waveform will have constant asymmetric ratio in Push-Pull mode as it will be calculated by $1/4 \text{ SCL} * [\text{pp_low} + 2]$. The resolution used is 1/4 SDR SCL clock. FW need to ensure $1/4 \text{ SCL} * [\text{pp_low} + 2] \geq$ minimum low period duration for the particular device. When BCR[0] is 1, PP timings will have 50/50 DC.
7-0	OD_LOW	R/W	9h	Counter for low period of SCL clock for Open Drain in I3C. SCL waveform will have constant asymmetric ratio in OD as it will be calculated by $1/4 \text{ SCL} * [\text{od_low} + 2]$. The resolution used is 1/4 SDR SCL clock. FW need to ensure $1/4 \text{ SCL} * [\text{od_low} + 2] \geq 160\text{ns}$.

4.9 I3C_MST_IER Register (Offset = 20h) [reset = 0h]

I3C_MST_IER is shown in [Figure 4-8](#) and described in [Table 4-20](#).

Return to the [Summary Table](#).

The write only Interrupt Enable Register is used to enable interrupts by setting bits in the read only Interrupt Mask Register - Master Mode (I3C_MST_IMR).

See Interrupt Status Register - Master Mode (I3C_MST_ISR) description for details on specific interrupt conditions.

When any bit is written high, the corresponding interrupt is enabled. Writing a low to any bit has no effect.

Table 4-19. I3C_MST_IER Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8020h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8020h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8020h

Figure 4-8. I3C_MST_IER Register

31	30	29	28	27	26	25	24
RSVD1							
R-0h							
23	22	21	20	19	18	17	16
RSVD1				HALTED		MR_DONE	IMM_COMP
R-0h				W-0h		W-0h	W-0h
15	14	13	12	11	10	9	8
TX_THR	TX_OVF	RSVD0	IBID_THR	IBID_UNF	IBIR_THR	IBIR_UNF	IBIR_OVF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
RX_THR	RX_UNF	CMDD_EMP	CMDD_THR	CMDD_OVF	CMDR_THR	CMDR_UNF	CMDR_OVF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-20. I3C_MST_IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RSVD1	R	0h	Reserved.
18	HALTED	W	0h	Controller in halted state.
17	MR_DONE	W	0h	Mastership handoff done Enable.
16	IMM_COMP	W	0h	Immediate Command Completed Enable
15	TX_THR	W	0h	Tx Data Threshold Enable.
14	TX_OVF	W	0h	Tx Data MEM Underflow Enable
13	RSVD0	W	0h	Reserved.
12	IBID_THR	W	0h	IBI Data MEM threshold Enable.
11	IBID_UNF	W	0h	IBI Data MEM underflow Enable.
10	IBIR_THR	W	0h	IBI Response Queue threshold Enable
9	IBIR_UNF	W	0h	IBI Response Queue underflow Enable
8	IBIR_OVF	W	0h	IBI Response Queue onoverflow Enable.

Table 4-20. I3C_MST_IER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RX_THR	W	0h	Rx Data MEM threshold Enable.
6	RX_UNF	W	0h	Rx Data MEM underflow Enable.
5	CMDD_EMP	W	0h	Command Request Queue Empty Enable.
4	CMDD_THR	W	0h	Command Request Queue Threshold Enable.
3	CMDD_OVF	W	0h	Command Request Queue Overflow Enable.
2	CMDR_THR	W	0h	Command Response Queue Threshold Enable.
1	CMDR_UNF	W	0h	Command Response Queue Underflow Enable.
0	CMDR_OVF	W	0h	Command Response Queue Overflow Enable.

4.10 I3C_MST_IDR Register (Offset = 24h) [reset = 0h]

I3C_MST_IDR is shown in [Figure 4-9](#) and described in [Table 4-22](#).

Return to the [Summary Table](#).

The write only Interrupt Disable Register is used to disable interrupts by clearing the bits in the read only Interrupt Mask Register - Master Mode (I3C_MST_IMR).

See Interrupt Status Register - Master Mode (I3C_MST_ISR) description for details on specific interrupt conditions.

When any bit is written high, the corresponding interrupt is disabled. Writing a low to any bit has no effect.

Table 4-21. I3C_MST_IDR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8024h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8024h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8024h

Figure 4-9. I3C_MST_IDR Register

31	30	29	28	27	26	25	24
RSVD1							
R-0h							
23	22	21	20	19	18	17	16
RSVD1				HALTED		MR_DONE	IMM_COMP
R-0h				W-0h		W-0h	W-0h
15	14	13	12	11	10	9	8
TX_THR	TX_OVF	RSVD0	IBID_THR	IBID_UNF	IBIR_THR	IBIR_UNF	IBIR_OVF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
RX_THR	RX_UNF	CMDD_EMP	CMDD_THR	CMDD_OVF	CMDR_THR	CMDR_UNF	CMDR_OVF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-22. I3C_MST_IDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RSVD1	R	0h	Reserved.
18	HALTED	W	0h	Controller in halted state.
17	MR_DONE	W	0h	Mastership handoff done Disable.
16	IMM_COMP	W	0h	Immediate Command Completed Disable
15	TX_THR	W	0h	Tx Data Threshold Disable.
14	TX_OVF	W	0h	Tx Data MEM Underflow Disable
13	RSVD0	W	0h	Reserved.
12	IBID_THR	W	0h	IBI Data MEM threshold Disable.
11	IBID_UNF	W	0h	IBI Data MEM underflow Disable.
10	IBIR_THR	W	0h	IBI Response Queue threshold Disable
9	IBIR_UNF	W	0h	IBI Response Queue underflow Disable
8	IBIR_OVF	W	0h	IBI Response Queue onoverflow Disable.

Table 4-22. I3C_MST_IDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RX_THR	W	0h	Rx Data MEM threshold Disable.
6	RX_UNF	W	0h	Rx Data MEM underflow Disable.
5	CMDD_EMP	W	0h	Command Request Queue Empty Disable.
4	CMDD_THR	W	0h	Command Request Queue Threshold Disable.
3	CMDD_OVF	W	0h	Command Request Queue Overflow Disable.
2	CMDR_THR	W	0h	Command Response Queue Threshold Disable.
1	CMDR_UNF	W	0h	Command Response Queue Underflow Disable.
0	CMDR_OVF	W	0h	Command Response Queue Overflow Disable.

4.11 I3C_MST_IMR Register (Offset = 28h) [reset = 0h]

I3C_MST_IMR is shown in [Figure 4-10](#) and described in [Table 4-24](#).

Return to the [Summary Table](#).

This read only register, indicates the current state of the interrupts mask.

See Interrupt Status Register - Master Mode (I3C_MST_ISR) description for details on specific interrupt conditions.

A high value indicates the interrupt is enabled to generate an interrupt.

A low value indicates the interrupt is disabled from generating an interrupt (masked).

Table 4-23. I3C_MST_IMR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8028h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8028h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8028h

Figure 4-10. I3C_MST_IMR Register

31	30	29	28	27	26	25	24
RSVD1							
R-0h							
23	22	21	20	19	18	17	16
RSVD1				HALTED		MR_DONE	IMM_COMP
R-0h				R-0h		R-0h	R-0h
15	14	13	12	11	10	9	8
TX_THR	TX_OVF	RSVD0	IBID_THR	IBID_UNF	IBIR_THR	IBIR_UNF	IBIR_OVF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RX_THR	RX_UNF	CMDD_EMP	CMDD_THR	CMDD_OVF	CMDR_THR	CMDR_UNF	CMDR_OVF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 4-24. I3C_MST_IMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RSVD1	R	0h	Reserved.
18	HALTED	R	0h	Controller in halted state.
17	MR_DONE	R	0h	Mastership handoff done Mask.
16	IMM_COMP	R	0h	Immediate Command Completed Mask
15	TX_THR	R	0h	Tx Data Threshold Mask.
14	TX_OVF	R	0h	Tx Data MEM Underflow Mask
13	RSVD0	R	0h	Reserved.
12	IBID_THR	R	0h	IBI Data MEM threshold Mask.
11	IBID_UNF	R	0h	IBI Data MEM underflow Mask.
10	IBIR_THR	R	0h	IBI Response Queue threshold Mask
9	IBIR_UNF	R	0h	IBI Response Queue underflow Mask
8	IBIR_OVF	R	0h	IBI Response Queue onoverflow Mask.

Table 4-24. I3C_MST_IMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RX_THR	R	0h	Rx Data MEM threshold Mask.
6	RX_UNF	R	0h	Rx Data MEM underflow Mask.
5	CMDD_EMP	R	0h	Command Request Queue Empty Mask.
4	CMDD_THR	R	0h	Command Request Queue Threshold Mask.
3	CMDD_OVF	R	0h	Command Request Queue Overflow Mask.
2	CMDR_THR	R	0h	Command Response Queue Threshold Mask.
1	CMDR_UNF	R	0h	Command Response Queue Underflow Mask.
0	CMDR_OVF	R	0h	Command Response Queue Overflow Mask.

4.12 I3C_MST_ICR Register (Offset = 2Ch) [reset = 0h]

I3C_MST_ICR is shown in [Figure 4-11](#) and described in [Table 4-26](#).

Return to the [Summary Table](#).

Interrupt Clear Register for Master Mode of the cdnsi3c_master controller. Write 1 to clear (change from 1 to 0) corresponding bit in I3C_MST_ISR. Writing 0 has no effect

Table 4-25. I3C_MST_ICR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 802Ch
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 802Ch
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 802Ch

Figure 4-11. I3C_MST_ICR Register

31	30	29	28	27	26	25	24
RSVD1							
R-0h							
23	22	21	20	19	18	17	16
RSVD1				HALTED		MR_DONE	IMM_COMP
R-0h				W-0h		W-0h	W-0h
15	14	13	12	11	10	9	8
TX_THR	TX_OVF	RSVD0	IBID_THR	IBID_UNF	IBIR_THR	IBIR_UNF	IBIR_OVF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
RX_THR	RX_UNF	CMDD_EMP	CMDD_THR	CMDD_OVF	CMDR_THR	CMDR_UNF	CMDR_OVF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-26. I3C_MST_ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RSVD1	R	0h	Reserved.
18	HALTED	W	0h	Controller is in halted state.
17	MR_DONE	W	0h	Mastership handoff done Mask.
16	IMM_COMP	W	0h	Immediate Command Completed Mask
15	TX_THR	W	0h	Tx Data Threshold Mask.
14	TX_OVF	W	0h	Tx Data MEM Underflow Mask
13	RSVD0	W	0h	Reserved.
12	IBID_THR	W	0h	IBI Data MEM threshold Mask.
11	IBID_UNF	W	0h	IBI Data MEM underflow Mask.
10	IBIR_THR	W	0h	IBI Response Queue threshold Mask
9	IBIR_UNF	W	0h	IBI Response Queue underflow Mask
8	IBIR_OVF	W	0h	IBI Response Queue onoverflow Mask.
7	RX_THR	W	0h	Rx Data MEM threshold Mask.
6	RX_UNF	W	0h	Rx Data MEM underflow Mask.

Table 4-26. I3C_MST_ICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CMDD_EMP	W	0h	Command Request Queue Empty Mask.
4	CMDD_THR	W	0h	Command Request Queue Threshold Mask.
3	CMDD_OVF	W	0h	Command Request Queue Overflow Mask.
2	CMDR_THR	W	0h	Command Response Queue Threshold Mask.
1	CMDR_UNF	W	0h	Command Response Queue Underflow Mask.
0	CMDR_OVF	W	0h	Command Response Queue Overflow Mask.

4.13 I3C_MST_ISR Register (Offset = 30h) [reset = 0h]

I3C_MST_ISR is shown in [Figure 4-12](#) and described in [Table 4-28](#).

Return to the [Summary Table](#).

Interrupt Status Register for Master Mode of the cdnsi3c_master controller

Table 4-27. I3C_MST_ISR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8030h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8030h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8030h

Figure 4-12. I3C_MST_ISR Register

31	30	29	28	27	26	25	24
RSVD1							
R-0h							
23	22	21	20	19	18	17	16
RSVD1				HALTED		MR_DONE	IMM_COMP
R-0h				R-0h		R-0h	R-0h
15	14	13	12	11	10	9	8
TX_THR	TX_OVF	RSVD0	IBID_THR	IBID_UNF	IBIR_THR	IBIR_UNF	IBIR_OVF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RX_THR	RX_UNF	CMDD_EMP	CMDD_THR	CMDD_OVF	CMDR_THR	CMDR_UNF	CMDR_OVF
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 4-28. I3C_MST_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RSVD1	R	0h	Reserved.
18	HALTED	R	0h	Controller in Halted state.
17	MR_DONE	R	0h	Mastership handoff done.
16	IMM_COMP	R	0h	Immediate Command Completed
15	TX_THR	R	0h	Tx Data Threshold.
14	TX_OVF	R	0h	Tx Data MEM overflow
13	RSVD0	R	0h	Reserved.
12	IBID_THR	R	0h	IBI Data MEM threshold.
11	IBID_UNF	R	0h	IBI Data MEM underflow.
10	IBIR_THR	R	0h	IBI Response Queue threshold
9	IBIR_UNF	R	0h	IBI Response Queue underflow
8	IBIR_OVF	R	0h	IBI Response Queue onoverflow.
7	RX_THR	R	0h	Rx Data MEM threshold.
6	RX_UNF	R	0h	Rx Data MEM underflow.
5	CMDD_EMP	R	0h	Command Request Queue Empty.

Table 4-28. I3C_MST_ISR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CMDD_THR	R	0h	Command Request Queue Threshold.
3	CMDD_OVF	R	0h	Command Request Queue Overflow.
2	CMDR_THR	R	0h	Command Response Queue Threshold.
1	CMDR_UNF	R	0h	Command Response Queue Underflow.
0	CMDR_OVF	R	0h	Command Response Queue Overflow.

4.14 I3C_MST_STATUS0 Register (Offset = 34h) [reset = 0005003Fh]

I3C_MST_STATUS0 is shown in [Figure 4-13](#) and described in [Table 4-30](#).

Return to the [Summary Table](#).

Status Register for I3C Master IP, meaningful only when controller operates in Master mode.

Table 4-29. I3C_MST_STATUS0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8034h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8034h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8034h

Figure 4-13. I3C_MST_STATUS0 Register

31	30	29	28	27	26	25	24
RSVD2							
R-0h							
23	22	21	20	19	18	17	16
RSVD2				IDLE	HALTED	OP_MODE	
R-0h				R-1h	R/W1C-0h	R-1h	
15	14	13	12	11	10	9	8
RSVD1	TX_FULL	IBID_FULL	IBIR_FULL	RX_FULL	CMDD_FULL	CMDR_FULL	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	
7	6	5	4	3	2	1	0
RSVD0	TX_EMP	IBID_EMP	IBIR_EMP	RX_EMP	CMDD_EMP	CMDR_EMP	
R-0h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-30. I3C_MST_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RSVD2	R	0h	Reserved
18	IDLE	R	1h	Indicates when the core is IDLE and ready to accept new commands. When I3C_CTRL.dev_en is deasserted, FW should poll this reg in order to ensure that core completed its last command. It is advisable to use this bit in order to ensure that currently the core is IDLE and I3C_CTRL register can be changed.
17	HALTED	R/W1C	0h	Core Halted. This status bit will be asserted on the second abort has occurred during Read operation [if I3C_CTRL.halt_en=1] or in case of Rx DATA FIFO is full [regardless of I3C_CTRL.halt_en state]. Writing 1 will unhalt the controllers core.
16	OP_MODE	R	1h	Indicates current mode of the controller: 0 - Slave mode 1 - Master mode. For Main Master configuration the reset value is 1 For Secondary Master configuration the reset value is 0 Set by HW.

Table 4-30. I3C_MST_STATUS0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	RSVD1	R	0h	Reserved.
13	TX_FULL	R	0h	TX Full.
12	IBID_FULL	R	0h	IBID Full.
11	IBIR_FULL	R	0h	I3C_IBIR Full.
10	RX_FULL	R	0h	RX Full.
9	CMDD_FULL	R	0h	CMDD Full.
8	CMDR_FULL	R	0h	I3C_CMDR Full.
7-6	RSVD0	R	0h	Reserved.
5	TX_EMP	R	1h	TX Empty.
4	IBID_EMP	R	1h	IBID Empty.
3	IBIR_EMP	R	1h	I3C_IBIR Empty.
2	RX_EMP	R	1h	RX Empty.
1	CMDD_EMP	R	1h	CMDD Empty.
0	CMDR_EMP	R	1h	I3C_CMDR Empty.

4.15 I3C_CMDR Register (Offset = 38h) [reset = 0h]

I3C_CMDR is shown in [Figure 4-14](#) and described in [Table 4-32](#).

Return to the [Summary Table](#).

Stores status on completion of each command, works on FIFO-basis.

Table 4-31. I3C_CMDR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8038h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8038h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8038h

Figure 4-14. I3C_CMDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD1				ERROR				RSVD0				XFER_BYTES			
R-0h				R-0h				R-0h				R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XFER_BYTES								CMD_ID							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-32. I3C_CMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RSVD1	R	0h	Reserved.
27-24	ERROR	R	0h	This field contains the code of an error that has occurred during the last transaction.
23-20	RSVD0	R	0h	Reserved.
19-8	XFER_BYTES	R	0h	The number of transferred bytes [SDR] or transferred words [DDR] during the last command. Will be set correctly for CCC commands as well even for those without payload [to zero value].
7-0	CMD_ID	R	0h	CMD_ID - command identifier.

4.16 I3C_IBIR Register (Offset = 3Ch) [reset = 0h]

I3C_IBIR is shown in [Figure 4-15](#) and described in [Table 4-34](#).

Return to the [Summary Table](#).

Stores status of SIR on its completion, works on FIFO-basis.

Table 4-33. I3C_IBIR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 803Ch
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 803Ch
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 803Ch

Figure 4-15. I3C_IBIR Register

31	30	29	28	27	26	25	24
RSVD0							
R-0h							
23	22	21	20	19	18	17	16
RSVD0							
R-0h							
15	14	13	12	11	10	9	8
RSVD0			RESP	SLV_ID			
R-0h			R-0h	R-0h			
7	6	5	4	3	2	1	0
ERROR	XFER_BYTES					IBI_TYPE	
R-0h	R-0h					R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 4-34. I3C_IBIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RSVD0	R	0h	Reserved
12	RESP	R	0h	If HIGH IBI has been ACKed, NACK response otherwise
11-8	SLV_ID	R	0h	ID of a Slave that has issued an IBI request
7	ERROR	R	0h	Set to 1 if IBI Data FIFO overflow has occurred during the transaction.
6-2	XFER_BYTES	R	0h	Number of received DATA bytes.
1-0	IBI_TYPE	R	0h	This field contains the type of an IBI.

4.17 I3C_SLV_IER Register (Offset = 40h) [reset = X]

I3C_SLV_IER is shown in [Figure 4-16](#) and described in [Table 4-36](#).

Return to the [Summary Table](#).

The write only Interrupt Enable Register is used to enable interrupts by setting bits in the read only Interrupt Mask Register - Slave Mode (I3C_SLV_IMR).

See Interrupt Status Register - Slave Mode (I3C_SLV_ISR) description for details on specific interrupt conditions.

When any bit is written high, the corresponding interrupt is enabled. Writing a low to any bit has no effect.

Table 4-35. I3C_SLV_IER Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8040h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8040h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8040h

Figure 4-16. I3C_SLV_IER Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED		DEFSLVS	TM	ERROR	EVENT_UP	HJ_DONE	MR_DONE
W-X		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DA_UPDATE	SDR_FAIL	DDR_FAIL	M_RD_ABORT	DDR_RX_THR	DDR_TX_THR	SDR_RX_THR	SDR_TX_THR
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DDR_RX_UNF	DDR_TX_OVF	SDR_RX_UNF	SDR_TX_OVF	DDR_RD_COM_P	DDR_WR_COM_P	SDR_RD_COM_P	SDR_WR_COM_P
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 4-36. I3C_SLV_IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	W	X	
21	DEFSLVS	W	0h	DEFSLVS interrupt Enable.
20	TM	W	0h	TM interrupt Enable.
19	ERROR	W	0h	ERROR interrupt Enable.
18	EVENT_UP	W	0h	EVENT_UP interrupt Enable.
17	HJ_DONE	W	0h	HJ_DONE interrupt Enable.
16	MR_DONE	W	0h	MR_DONE interrupt Enable.
15	DA_UPDATE	W	0h	DA_UPDATE interrupt Enable
14	SDR_FAIL	W	0h	SDR_FAIL interrupt Enable
13	DDR_FAIL	W	0h	DDR_FAIL interrupt Enable
12	M_RD_ABORT	W	0h	M_RD_ABORT interrupt Enable.
11	DDR_RX_THR	W	0h	DDR_RX_THR interrupt Enable.

Table 4-36. I3C_SLV_IER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DDR_TX_THR	W	0h	DDR_TX_THR interrupt Enable.
9	SDR_RX_THR	W	0h	SDR_RX_THR interrupt Enable.
8	SDR_TX_THR	W	0h	SLV_SDR_TX_THR interrupt Enable.
7	DDR_RX_UNF	W	0h	DDR_RX_UNF interrupt Enable.
6	DDR_TX_OVF	W	0h	DDR_TX_OVF interrupt Enable.
5	SDR_RX_UNF	W	0h	SDR_RX_UNF interrupt Enable.
4	SDR_TX_OVF	W	0h	SDR_TX_OVF interrupt Enable.
3	DDR_RD_COMP	W	0h	DDR_RD_COMP interrupt Enable.
2	DDR_WR_COMP	W	0h	DDR_WR_COMP interrupt Enable.
1	SDR_RD_COMP	W	0h	SDR_RD_COMP interrupt Enable.
0	SDR_WR_COMP	W	0h	SDR_WR_COMP interrupt Enable.

4.18 I3C_SLV_IDR Register (Offset = 44h) [reset = X]

I3C_SLV_IDR is shown in [Figure 4-17](#) and described in [Table 4-38](#).

Return to the [Summary Table](#).

The write only Interrupt Disable Register is used to disable interrupts by clearing the bits in the read only Interrupt Mask Register - Slave Mode (I3C_SLV_IMR).

See Interrupt Status Register - Slave Mode (I3C_SLV_ISR) description for details on specific interrupt conditions.

When any bit is written high, the corresponding interrupt is disabled. Writing a low to any bit has no effect.

Table 4-37. I3C_SLV_IDR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8044h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8044h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8044h

Figure 4-17. I3C_SLV_IDR Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED		DEFSLVS	TM	ERROR	EVENT_UP	HJ_DONE	MR_DONE
W-X		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DA_UPDATE	SDR_FAIL	DDR_FAIL	M_RD_ABORT	DDR_RX_THR	DDR_TX_THR	SDR_RX_THR	SDR_TX_THR
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DDR_RX_UNF	DDR_TX_OVF	SDR_RX_UNF	SDR_TX_OVF	DDR_RD_COM_P	DDR_WR_COM_P	SDR_RD_COM_P	SDR_WR_COM_P
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 4-38. I3C_SLV_IDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	W	X	
21	DEFSLVS	W	0h	DEFSLVS interrupt Disable.
20	TM	W	0h	TM interrupt Disable.
19	ERROR	W	0h	ERROR interrupt Disable.
18	EVENT_UP	W	0h	EVENT_UP interrupt Disable.
17	HJ_DONE	W	0h	HJ_DONE interrupt Disable.
16	MR_DONE	W	0h	MR_DONE interrupt Disable.
15	DA_UPDATE	W	0h	DA_UPDATE interrupt Disable.
14	SDR_FAIL	W	0h	SDR_FAIL interrupt Disable
13	DDR_FAIL	W	0h	DDR_FAIL interrupt Disable
12	M_RD_ABORT	W	0h	M_RD_ABORT interrupt Disable.
11	DDR_RX_THR	W	0h	DDR_RX_THR interrupt Disable.

Table 4-38. I3C_SLV_IDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DDR_TX_THR	W	0h	DDR_TX_THR interrupt Disable.
9	SDR_RX_THR	W	0h	SDR_RX_THR interrupt Disable.
8	SDR_TX_THR	W	0h	SDR_TX_THR interrupt Disable.
7	DDR_RX_UNF	W	0h	DDR_RX_UNF interrupt Disable.
6	DDR_TX_OVF	W	0h	DDR_TX_OVF interrupt Disable.
5	SDR_RX_UNF	W	0h	SDR_RX_UNF interrupt Disable.
4	SDR_TX_OVF	W	0h	SDR_TX_OVF interrupt Disable.
3	DDR_RD_COMP	W	0h	DDR_RD_COMP interrupt Disable.
2	DDR_WR_COMP	W	0h	DDR_WR_COMP interrupt Disable.
1	SDR_RD_COMP	W	0h	SDR_RD_COMP interrupt Disable.
0	SDR_WR_COMP	W	0h	SDR_WR_COMP interrupt Disable.

4.19 I3C_SLV_IMR Register (Offset = 48h) [reset = X]

I3C_SLV_IMR is shown in [Figure 4-18](#) and described in [Table 4-40](#).

Return to the [Summary Table](#).

This read only register, indicates the current state of the interrupts mask.

See Interrupt Status Register - Slave Mode (I3C_SLV_ISR) description for details on specific interrupt conditions.

A high value indicates the interrupt is enabled to generate an interrupt.

A low value indicates the interrupt is disabled from generating an interrupt (masked).

Table 4-39. I3C_SLV_IMR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8048h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8048h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8048h

Figure 4-18. I3C_SLV_IMR Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED		DEFSLVS	TM	ERROR	EVENT_UP	HJ_DONE	MR_DONE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
DA_UPDATE	SDR_FAIL	DDR_FAIL	M_RD_ABORT	DDR_RX_THR	DDR_TX_THR	SDR_RX_THR	SDR_TX_THR
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DDR_RX_UNF	DDR_TX_OVF	SDR_RX_UNF	SDR_TX_OVF	DDR_RD_COM_P	DDR_WR_COM_P	SDR_RD_COM_P	SDR_WR_COM_P
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 4-40. I3C_SLV_IMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	X	
21	DEFSLVS	R	0h	DEFSLVS interrupt Mask.
20	TM	R	0h	TM interrupt Mask.
19	ERROR	R	0h	ERROR interrupt Mask.
18	EVENT_UP	R	0h	EVENT_UP interrupt Mask.
17	HJ_DONE	R	0h	HJ_DONE interrupt Mask.
16	MR_DONE	R	0h	MR_DONE interrupt Mask.
15	DA_UPDATE	R	0h	DA_UPDATE interrupt Mask.
14	SDR_FAIL	R	0h	SDR_FAIL interrupt Mask
13	DDR_FAIL	R	0h	DDR_FAIL interrupt Mask
12	M_RD_ABORT	R	0h	M_RD_ABORT interrupt Mask.
11	DDR_RX_THR	R	0h	DDR_RX_THR interrupt Mask.

Table 4-40. I3C_SLV_IMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	DDR_TX_THR	R	0h	DDR_TX_THR interrupt Mask.
9	SDR_RX_THR	R	0h	SDR_RX_THR interrupt Mask.
8	SDR_TX_THR	R	0h	SDR_TX_THR interrupt Mask.
7	DDR_RX_UNF	R	0h	DDR_RX_UNF interrupt Mask.
6	DDR_TX_OVF	R	0h	DDR_TX_OVF interrupt Mask.
5	SDR_RX_UNF	R	0h	SDR_RX_UNF interrupt Mask.
4	SDR_TX_OVF	R	0h	SDR_TX_OVF interrupt Mask.
3	DDR_RD_COMP	R	0h	DDR_RD_COMP interrupt Mask.
2	DDR_WR_COMP	R	0h	DDR_WR_COMP interrupt Mask.
1	SDR_RD_COMP	R	0h	SDR_RD_COMP interrupt Mask.
0	SDR_WR_COMP	R	0h	SDR_WR_COMP interrupt Mask.

4.20 I3C_SLV_ICR Register (Offset = 4Ch) [reset = X]

I3C_SLV_ICR is shown in [Figure 4-19](#) and described in [Table 4-42](#).

Return to the [Summary Table](#).

Interrupt Clear Register for Slave Mode of the cdnsi3c_master controller. Write 1 to clear (change from 1 to 0) corresponding bit in I3C_SLV_ISR. Writing 0 has no effect

Table 4-41. I3C_SLV_ICR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 804Ch
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 804Ch
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 804Ch

Figure 4-19. I3C_SLV_ICR Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED		DEFSLV	TM	ERROR	EVENT_UP	HJ_DONE	MR_DONE
W-X		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DA_UPDATE	SDR_FAIL	DDR_FAIL	M_RD_ABORT	DDR_RX_THR	DDR_TX_THR	SDR_RX_THR	SDR_TX_THR
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DDR_RX_UNF	DDR_TX_OVF	SDR_RX_UNF	SDR_TX_OVF	DDR_RD_COM_P	DDR_WR_COM_P	SDR_RD_COM_P	SDR_WR_COM_P
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 4-42. I3C_SLV_ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	W	X	
21	DEFSLV	W	0h	DEFSLV interrupt Clear.
20	TM	W	0h	TM interrupt Clear.
19	ERROR	W	0h	ERROR interrupt Clear.
18	EVENT_UP	W	0h	EVENT_UP interrupt Clear.
17	HJ_DONE	W	0h	HJ_DONE interrupt Clear.
16	MR_DONE	W	0h	MR_DONE interrupt Clear.
15	DA_UPDATE	W	0h	DA_UPDATE interrupt Clear.
14	SDR_FAIL	W	0h	SDR_FAIL interrupt Clear.
13	DDR_FAIL	W	0h	DDR_FAIL interrupt Clear.
12	M_RD_ABORT	W	0h	M_RD_ABORT interrupt Clear.
11	DDR_RX_THR	W	0h	DDR_RX_THR interrupt Clear.
10	DDR_TX_THR	W	0h	DDR_TX_THR interrupt Clear.
9	SDR_RX_THR	W	0h	SDR_RX_THR interrupt Clear.

Table 4-42. I3C_SLV_ICR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SDR_TX_THR	W	0h	SDR_TX_THR interrupt Clear.
7	DDR_RX_UNF	W	0h	DDR_RX_UNF interrupt Clear.
6	DDR_TX_OVF	W	0h	DDR_TX_OVF interrupt Clear.
5	SDR_RX_UNF	W	0h	SDR_RX_UNF interrupt Clear.
4	SDR_TX_OVF	W	0h	SDR_TX_OVF interrupt Clear.
3	DDR_RD_COMP	W	0h	DDR_RD_COMP interrupt Clear.
2	DDR_WR_COMP	W	0h	DDR_WR_COMP interrupt Clear.
1	SDR_RD_COMP	W	0h	SDR_RD_COMP interrupt Clear.
0	SDR_WR_COMP	W	0h	SDR_WR_COMP interrupt Clear.

4.21 I3C_SLV_ISR Register (Offset = 50h) [reset = X]

I3C_SLV_ISR is shown in [Figure 4-20](#) and described in [Table 4-44](#).

Return to the [Summary Table](#).

Interrupt Status Register for Slave Mode of the cdnsi3c_master controller

Table 4-43. I3C_SLV_ISR Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8050h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8050h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8050h

Figure 4-20. I3C_SLV_ISR Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED		DEFSLVs	TM	ERROR	EVENT_UP	HJ_DONE	MR_DONE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
DA_UPDATE	SDR_FAIL	DDR_FAIL	M_RD_ABORT	DDR_RX_THR	DDR_TX_THR	SDR_RX_THR	SDR_TX_THR
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
DDR_RX_UNF	DDR_TX_OVF	SDR_RX_UNF	SDR_TX_OVF	DDR_RD_COM_P	DDR_WR_COM_P	SDR_RD_COM_P	SDR_WR_COM_P
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 4-44. I3C_SLV_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	X	
21	DEFSLVs	R	0h	This interrupt is triggered whenever I3C-Slave DEFSLVs CCC command is received.
20	TM	R	0h	This interrupt is triggered whenever I3C-Slave is not in Test Mode and ENT TM CCC command with byte value of 0x01 [general Test Mode] is received.
19	ERROR	R	0h	This event is triggered whenever SDR Error is detected - applicable for S0, S1, S2, S4 and S5 Errors from MIPI spec.
18	EVENT_UP	R	0h	This event is triggered whenever DISEC CCC or ENEC CCC is received.
17	HJ_DONE	R	0h	This event is triggered whenever Hot-Join request is completed.
16	MR_DONE	R	0h	This event is triggered whenever Mastership Request is completed.
15	DA_UPDATE	R	0h	This event is triggered whenever Dynamic Address of the device has been updated.
14	SDR_FAIL	R	0h	This event is triggered whenever fail event during SDR transfer is detected [applicable for Private Write transfers only].

Table 4-44. I3C_SLV_ISR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	DDR_FAIL	R	0h	This event is triggered whenever fail event during DDR transfer is detected.
12	M_RD_ABORT	R	0h	Read Transfer Aborted by Master.
11	DDR_RX_THR	R	0h	This event is triggered whenever threshold level for DDR Rx DATA Buffer is reached.
10	DDR_TX_THR	R	0h	This event is triggered whenever threshold level for DDR Tx DATA Buffer is reached.
9	SDR_RX_THR	R	0h	Rx DATA Buffer Threshold. It is set when the number of bytes in the Rx DATA Buffer reaches value programmed in I3C_TX_RX_THR_CTRL.rx_thr field.
8	SDR_TX_THR	R	0h	Tx DATA Buffer Threshold. It is set when the number of bytes in the Tx DATA Buffer reaches value programmed in I3C_TX_RX_THR_CTRL.tx_thr field.
7	DDR_RX_UNF	R	0h	Set if the host attempts to read from the DDR_RX_FIFO register when there is no more data.
6	DDR_TX_OVF	R	0h	Set if the host attempts to write to DDR_TX_FIFO register more times than the FIFO depth.
5	SDR_RX_UNF	R	0h	Rx DATA Buffer Underflow. Set if the host attempts to read from the empty Rx DATA Buffer.
4	SDR_TX_OVF	R	0h	Tx DATA Buffer Overflow. Set if host attempts to write to Tx DATA Buffer which is already full.
3	DDR_RD_COMP	R	0h	This bit is set whenever the Slave terminates the DDR Read transfer.
2	DDR_WR_COMP	R	0h	This bit is set whenever the Master terminates the DDR Write transfer.
1	SDR_RD_COMP	R	0h	This bit is set whenever the Slave terminates the SDR Private Read transfer.
0	SDR_WR_COMP	R	0h	This bit is set whenever the Master terminates the SDR Private Write transfer.

4.22 I3C_SLV_STATUS0 Register (Offset = 54h) [reset = 0h]

I3C_SLV_STATUS0 is shown in [Figure 4-21](#) and described in [Table 4-46](#).

Return to the [Summary Table](#).

The read only Status 0 register (I3C_SLV_STATUS0) is provided to enable the continuous monitoring of the raw unmasked status information of the I3C-Master operating in Slave mode.

Table 4-45. I3C_SLV_STATUS0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8054h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8054h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8054h

Figure 4-21. I3C_SLV_STATUS0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD0								REG_ADDR								XFERRED_BYTES															
R-0h								R-0h								R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-46. I3C_SLV_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RSVD0	R	0h	Reserved
23-16	REG_ADDR	R	0h	Private Read/Write Address.
15-0	XFERRED_BYTES	R	0h	Number of transferred bytes in SDR transactions.

4.23 I3C_SLV_STATUS1 Register (Offset = 58h) [reset = 00061133h]

I3C_SLV_STATUS1 is shown in [Figure 4-22](#) and described in [Table 4-48](#).

Return to the [Summary Table](#).

The read only Status 1 register (I3C_SLV_STATUS1) is provided to enable the continuous monitoring of the raw unmasked status information of the I3C-Master operating in Slave mode.

Table 4-47. I3C_SLV_STATUS1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8058h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8058h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8058h

Figure 4-22. I3C_SLV_STATUS1 Register

31	30	29	28	27	26	25	24
RSVD1							
R-0h							
23	22	21	20	19	18	17	16
RSVD1	ENTAS		VEN_TM	HJ_DIS	MR_DIS	PROT_ERROR	
R-0h	R-0h		R-0h	R-1h	R-1h	R-0h	
15	14	13	12	11	10	9	8
DA						HAS_DA	
R-8h						R-1h	
7	6	5	4	3	2	1	0
DDRRX_FULL	DDRTX_FULL	DDRRX_EMPTY	DDRTX_EMPTY	SDRRX_FULL	SDRTX_FULL	SDRRX_EMPTY	SDRTX_EMPTY
R-0h	R-0h	R-1h	R-1h	R-0h	R-0h	R-1h	R-1h

LEGEND: R = Read Only; -n = value after reset

Table 4-48. I3C_SLV_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RSVD1	R	0h	Reserved
21-20	ENTAS	R	0h	Bits that indicate current Activity State. It is updated based on ENTASx CCC [broadcast or direct], by default is set to 2'b00.
19	VEN_TM	R	0h	Vendor Test Mode. This bit is set whenever ENTTM CCC is received with value of 0x01. It remains HIGH until reception of another ENTTM CCC with different value.
18	HJ_DIS	R	1h	Hot-Join Disabled. This bit is set whenever HJ request is disabled by Current I3C-Master using DISEC CCC.
17	MR_DIS	R	1h	This bit is set whenever MR request is disabled by Current I3C-Master using DISEC CCC.
16	PROT_ERROR	R	0h	Protocol Error Condition Indicator. This bit is set whenever SDR error condition is detected by I3C-Master operating in Slave mode. It remains High until detection of recovery pattern.

Table 4-48. I3C_SLV_STATUS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-9	DA	R	8h	Slave Dynamic Address.
8	HAS_DA	R	1h	This bit is set whenever Slave has Dynamic Address assigned.
7	DDRRX_FULL	R	0h	This bit is set whenever I3C_SLV_DDR_RX_FIFO is full.
6	DDRTX_FULL	R	0h	This bit is set whenever I3C_SLV_DDR_TX_FIFO is full.
5	DDRRX_EMPTY	R	1h	This bit is set whenever I3C_SLV_DDR_RX_FIFO is empty.
4	DDRTX_EMPTY	R	1h	This bit is set whenever I3C_SLV_DDR_TX_FIFO is empty.
3	SDRRX_FULL	R	0h	This bit is set whenever SDR_RX_FIFO is full.
2	SDRTX_FULL	R	0h	This bit is set whenever SDR_TX_FIFO is full.
1	SDRRX_EMPTY	R	1h	This bit is set whenever SDR_RX_FIFO is empty.
0	SDRTX_EMPTY	R	1h	This bit is set whenever SDR_TX_FIFO is empty.

4.24 I3C_CMD0_FIFO Register (Offset = 60h) [reset = X]

I3C_CMD0_FIFO is shown in [Figure 4-23](#) and described in [Table 4-50](#).

Return to the [Summary Table](#).

Command0 FIFO. When implemented, the commands will be executed sequentially in order of arrival from the FW.

Table 4-49. I3C_CMD0_FIFO Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8060h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8060h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8060h

Figure 4-23. I3C_CMD0_FIFO Register

31	30	29	28	27	26	25	24
IS_DDR	IS_CCC	BCH	XMIT_MODE		SBCA	RSBC	IS10B
W-0h	W-0h	W-0h	W-0h		W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
PL_LEN							
W-0h							
15	14	13	12	11	10	9	8
PL_LEN				RESERVED	DEV_ADDR_MSB		
W-0h				W-X	W-0h		
7	6	5	4	3	2	1	0
DEV_ADDR							RNW
W-0h							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 4-50. I3C_CMD0_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IS_DDR	W	0h	IS_DDR - DDR command. Enables DDR mode of transfer. 0 - SDR mode 1 - DDR mode, note that ENTHDR-DDR CCC should precede any commands with DDR mode enabled.
30	IS_CCC	W	0h	IsCCC. Denotes whether it is a CCC or generic command. 0 - generic command 1 - CCC command
29	BCH	W	0h	BCH - Broadcast Header. Defines whether command will includes broadcast address header [0x7E] or not. Implicitly set for CCC commands. 0 - broadcast header disabled 1 - broadcast header enabled

Table 4-50. I3C_CMD0_FIFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-27	XMIT_MODE	W	0h	Defines transfer modes for I3C private read/write commands [not CCC], the following options are available: 00 - single CSR address. Send one single slave CSR address followed by data bytes only. Expecting slave will make self-increment of the address for each data byte or will have payload buffer implemented. 01 - multi byte incrementing CSR address, each data byte followed by repeated start condition and the slave's CSR address incremented explicitly. 10 - multi byte static CSR address, each data byte followed by repeat start condition and the slave's CSR address unchanged. 11 - No CSR ADDR [NCA], CCC/CSR ADDR0 filed is not used. First data byte after the slave address is a payload.
26	SBCA	W	0h	SBCA - Sixteen Bits CSR Addressing. Defines the CSR addressing mode for I3C private commands only. 0 - normal CSR addressing mode [8-bit] - ADDR0_ 7 - ADDR0_ 1 - extended CSR addressing mode [16-bit] - ADDR0_ 7 - ADDR0_0 and ADDR1_ 7 - ADDR1_0
25	RSBC	W	0h	RSBC - Repeated Start Between Commands. When this bit is set then between commands he repeated start condition is issued instead stop condition. It is only applicable when there is more than one command is in the command queue and next command is for Slave device of same type. The stop condition will be generated regardless of RSCB bit value for the following scenarios: - current command is the last command in the command queue - next command has invalid DA/SA - immediate command comes through
24	IS10B	W	0h	Is10B - Normal/Extended Address. Defines the addressing mode, applicable only for legacy I2C messaging. 0 - normal addressing mode [7-bit] - ID 6-ID0 1 - extended addressing mode [10-bit] - ID10B 2-ID10B0 and ID 6-ID0
23-12	PL_LEN	W	0h	PL_LEN - Payload Length. The number of bytes to be sent for particular CCC or generic R/Q command. Supports up to 4095 bytes.
11	RESERVED	W	X	
10-8	DEV_ADDR_MSB	W	0h	DEV_ADDR_MSB - legacy I2C Extended Address. The 3 MSB bits of legacy I2C 10-bit address. Applicable only if Is_10B is set for I2C legacy transfers.

Table 4-50. I3C_CMD0_FIFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-1	DEV_ADDR	W	0h	DEV_ADDR - Static/Dynamic slave Address. Correspond to a given slave Dynamic Address and Static Address. For CCC is applicable only when it is direct CCC command. For broadcast CCC this field is ignored.
0	RNW	W	0h	RnW - Read no Write. Defines the direction of transfer, for broadcast CCC this field is ignored. 0 - Write Transfer 1 - Read Transfer

4.25 I3C_CMD1_FIFO Register (Offset = 64h) [reset = 0h]

I3C_CMD1_FIFO is shown in [Figure 4-24](#) and described in [Table 4-52](#).

Return to the [Summary Table](#).

Command 1 FIFO. When implemented, the commands will be executed sequentially in order of arrival from the FW.

Table 4-51. I3C_CMD1_FIFO Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8064h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8064h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8064h

Figure 4-24. I3C_CMD1_FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMD_ID								RSVD0							
W-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSRADDR1								CCC_CSRADDR0							
W-0h								W-0h							

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-52. I3C_CMD1_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMD_ID	W	0h	COMMAND ID - generated by the host and used by the DMA to sort incoming read data to different consumers [channelization].
23-16	RSVD0	R	0h	Reserved
15-8	CSRADDR1	W	0h	CSR ADDR 1 - second byte of the CSR address in 16-bit addressing mode. Applicable only when 16-bit addressing mode is used and for private commands [non CCC commands].
7-0	CCC_CSRADDR0	W	0h	CCC/CSR ADDR 0 - CCC or CSR Address. Meaning of this field depends on bit 30 [IsCCC] of Command Word0. - When IsCCC is set to '0' then this field holds address of slave CSR. When 16-bit addressing is used, then it is the first byte of the CSR address. - When IsCCC is set to '1' then this field holds code of CCC.

4.26 I3C_TX_FIFO Register (Offset = 68h) [reset = 0h]

I3C_TX_FIFO is shown in [Figure 4-25](#) and described in [Table 4-54](#).

Return to the [Summary Table](#).

Tx Data FIFO which stores number of bytes to be sent with particular command.
APB->I3C direction

Table 4-53. I3C_TX_FIFO Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8068h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8068h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8068h

Figure 4-25. I3C_TX_FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 4-54. I3C_TX_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	W	0h	Tx Data FIFO which stores number of bytes to be sent with particular command

4.27 I3C_IMD_CMD0 Register (Offset = 70h) [reset = X]

I3C_IMD_CMD0 is shown in [Figure 4-26](#) and described in [Table 4-56](#).

Return to the [Summary Table](#).

High priority command register. When the core currently is executing a particular command from the CMD FIFO and new immediate command is sent, the core finish the standard command and then will execute the immediate command, disregarding the CMD FIFO state.

Supposed to be used mainly for CCC commands with payload up to 4 bytes.

Table 4-55. I3C_IMD_CMD0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8070h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8070h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8070h

Figure 4-26. I3C_IMD_CMD0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED	PL_LEN			RESERVED				DEV_ADDR							RNW
W-X	W-0h			W-X				W-0h							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 4-56. I3C_IMD_CMD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	W	X	
14-12	PL_LEN	W	0h	PL_LEN - Payload Length. The number of bytes to be sent for particular CCC. Supports up to 4 bytes.
11-8	RESERVED	W	X	
7-1	DEV_ADDR	W	0h	DEV_ADDR - Static/Dynamic slave Address. Correspond to a given slave Dynamic Address and Static Address. For CCC is applicable only when it is direct CCC command. For broadcast CCC this field is ignored.
0	RNW	W	0h	RnW - Read no Write. Defines the direction of transfer, for broadcast CCC this field is ignored. 0 - Write Transfer 1 - Read Transfer

4.28 I3C_IMD_CMD1 Register (Offset = 74h) [reset = 0h]

I3C_IMD_CMD1 is shown in [Figure 4-27](#) and described in [Table 4-58](#).

Return to the [Summary Table](#).

High priority command register. When the core currently is executing a particular command from the CMD FIFO and new immediate command is sent, the core finish the standard command and then will execute the immediate command, disregarding the CMD FIFO state.

Supposed to be used mainly for CCC commands with payload up to 4 bytes.

Table 4-57. I3C_IMD_CMD1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8074h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8074h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8074h

Figure 4-27. I3C_IMD_CMD1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ID								RSVD0								CCC															
W-0h								R-0h								W-0h															

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-58. I3C_IMD_CMD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMD_ID	W	0h	COMMAND ID - generated by the host and used by the DMA to sort incoming read data to different consumers [channelization].
23-8	RSVD0	R	0h	Reserved
7-0	CCC	W	0h	CCC code

4.29 I3C_IMD_DATA Register (Offset = 78h) [reset = 0h]

I3C_IMD_DATA is shown in [Figure 4-28](#) and described in [Table 4-60](#).

Return to the [Summary Table](#).

Payload/Data for a particular immediate command.

Table 4-59. I3C_IMD_DATA Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8078h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8078h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8078h

Figure 4-28. I3C_IMD_DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-60. I3C_IMD_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Payload/Data for a particular immediate command. Supports up to 4 bytes

4.30 I3C_RX_FIFO Register (Offset = 80h) [reset = 0h]

I3C_RX_FIFO is shown in [Figure 4-29](#) and described in [Table 4-62](#).

Return to the [Summary Table](#).

Rx Data FIFO which stores number of bytes to be received with particular command.
I3C->APB direction

Table 4-61. I3C_RX_FIFO Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8080h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8080h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8080h

Figure 4-29. I3C_RX_FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-62. I3C_RX_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	Rx Data FIFO which stores number of bytes to be received with particular command.

4.31 I3C_IBI_DATA_FIFO Register (Offset = 84h) [reset = 0h]

I3C_IBI_DATA_FIFO is shown in [Figure 4-30](#) and described in [Table 4-64](#).

Return to the [Summary Table](#).

IBI Data FIFO which stores number of bytes to be received for particular IBI request when BCR[2]=1
I3C->APB direction

Table 4-63. I3C_IBI_DATA_FIFO Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8084h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8084h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8084h

Figure 4-30. I3C_IBI_DATA_FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-64. I3C_IBI_DATA_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R	0h	IBI Data FIFO which stores number of bytes to be received for particular IBI request.

4.32 I3C_SLV_DDR_TX_FIFO Register (Offset = 88h) [reset = X]

I3C_SLV_DDR_TX_FIFO is shown in [Figure 4-31](#) and described in [Table 4-66](#).

Return to the [Summary Table](#).

DDR Tx Data FIFO stores number of words to be sent with particular DDR command in slave mode.
APB->I3C direction

Table 4-65. I3C_SLV_DDR_TX_FIFO Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8088h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8088h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8088h

Figure 4-31. I3C_SLV_DDR_TX_FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												DDR_SLAVE_TX_DATA_FIFO			
W-X												W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDR_SLAVE_TX_DATA_FIFO															
W-0h															

LEGEND: W = Write Only; -n = value after reset

Table 4-66. I3C_SLV_DDR_TX_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	W	X	
19-0	DDR_SLAVE_TX_DATA_FIFO	W	0h	DDR Tx Data FIFO stores number of words to be sent with particular DDR command in slave mode

4.33 I3C_SLV_DDR_RX_FIFO Register (Offset = 8Ch) [reset = X]

I3C_SLV_DDR_RX_FIFO is shown in [Figure 4-32](#) and described in [Table 4-68](#).

Return to the [Summary Table](#).

DDR Rx Data FIFO stores number of words to be received with particular DDR command in slave mode.
APB->I3C direction

Table 4-67. I3C_SLV_DDR_RX_FIFO Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 808Ch
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 808Ch
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 808Ch

Figure 4-32. I3C_SLV_DDR_RX_FIFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												DDR_SLAVE_RX_DATA_FIFO			
R-X												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDR_SLAVE_RX_DATA_FIFO															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-68. I3C_SLV_DDR_RX_FIFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19-0	DDR_SLAVE_RX_DATA_FIFO	R	0h	DDR Rx Data FIFO stores number of words to be received with particular DDR command in slave mode

4.34 I3C_CMD_IBI_THR_CTRL Register (Offset = 90h) [reset = 01010101h]

I3C_CMD_IBI_THR_CTRL is shown in [Figure 4-33](#) and described in [Table 4-70](#).

Return to the [Summary Table](#).

Configuration register for Command and In-Band Interrupt data buffer thresholds.

Table 4-69. I3C_CMD_IBI_THR_CTRL Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8090h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8090h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8090h

Figure 4-33. I3C_CMD_IBI_THR_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD3				IBIR_THR				RSVD2				CMDR_THR			
R-0h				R/W-1h				R-0h				R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD1				IBID_THR				RSVD0				CMDD_THR			
R-0h				R/W-1h				R-0h				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-70. I3C_CMD_IBI_THR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RSVD3	R	0h	Reserved
29-24	IBIR_THR	R/W	1h	Threshold configuration value for IBI RESP memory block
23-21	RSVD2	R	0h	Reserved
20-16	CMDR_THR	R/W	1h	Threshold configuration value for Command RESP memory block
15-14	RSVD1	R	0h	Reserved
13-8	IBID_THR	R/W	1h	Threshold configuration value for IBI DATA memory block
7-5	RSVD0	R	0h	Reserved
4-0	CMDD_THR	R/W	1h	Threshold configuration value for Command REQ memory block

4.35 I3C_TX_RX_THR_CTRL Register (Offset = 94h) [reset = 00010001h]

I3C_TX_RX_THR_CTRL is shown in [Figure 4-34](#) and described in [Table 4-72](#).

Return to the [Summary Table](#).

Configuration register for Tx and Rx data buffer thresholds.

Table 4-71. I3C_TX_RX_THR_CTRL Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8094h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8094h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8094h

Figure 4-34. I3C_TX_RX_THR_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_THR																TX_THR															
R/W-1h																R/W-1h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-72. I3C_TX_RX_THR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_THR	R/W	1h	Threshold configuration value for Rx Data memory block
15-0	TX_THR	R/W	1h	Threshold configuration value for Tx Data memory block

4.36 I3C_SLV_DDR_TX_RX_THR_CTRL Register (Offset = 98h) [reset = 00010001h]

I3C_SLV_DDR_TX_RX_THR_CTRL is shown in [Figure 4-35](#) and described in [Table 4-74](#).

Return to the [Summary Table](#).

Configuration register for Tx and Rx thresholds associated with Slave Mode DDR Data memory blocks.

Table 4-73. I3C_SLV_DDR_TX_RX_THR_CTRL Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8098h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8098h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8098h

Figure 4-35. I3C_SLV_DDR_TX_RX_THR_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLV_DDR_RX_THR																SLV_DDR_TX_THR															
R/W-1h																R/W-1h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-74. I3C_SLV_DDR_TX_RX_THR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SLV_DDR_RX_THR	R/W	1h	Threshold configuration value for Slave Mode DDR Rx Data memory block
15-0	SLV_DDR_TX_THR	R/W	1h	Threshold configuration value for Slave Mode DDR Tx Data memory block

4.37 I3C_FLUSH_CTRL Register (Offset = 9Ch) [reset = X]

I3C_FLUSH_CTRL is shown in [Figure 4-36](#) and described in [Table 4-76](#).

Return to the [Summary Table](#).

Control register for FIFO soft flush control

Table 4-75. I3C_FLUSH_CTRL Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 809Ch
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 809Ch
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 809Ch

Figure 4-36. I3C_FLUSH_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							IBI_RESP_FLUSH
W-X							W-0h
23	22	21	20	19	18	17	16
CMD_RESP_FLUSH	SLV_DDR_RX_FLUSH	SLV_DDR_TX_FLUSH	IMM_CMD_FLUSH	IBI_FLUSH	RX_FLUSH	TX_FLUSH	CMD_FLUSH
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							
W-X							

LEGEND: W = Write Only; -n = value after reset

Table 4-76. I3C_FLUSH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	W	X	
24	IBI_RESP_FLUSH	W	0h	When asserted while controller is disabled, the IBI Response Queue read/write pointers will be set to 0, effectively make the FIFO empty. Self-cleared control bit.
23	CMD_RESP_FLUSH	W	0h	When asserted while controller is disabled, the Command Response Queue read/write pointers will be set to 0, effectively make the FIFO empty. Self-cleared control bit.
22	SLV_DDR_RX_FLUSH	W	0h	When asserted while controller is disabled, the SLV DDR Rx Data memory block read/write pointers will be set to 0, effectively make the FIFO empty. Self-cleared control bit.
21	SLV_DDR_TX_FLUSH	W	0h	When asserted while controller is disabled, the SLV DDR Tx Data memory block read/write pointers will be set to 0, effectively make the FIFO empty. Self-cleared control bit.

Table 4-76. I3C_FLUSH_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	IMM_CMD_FLUSH	W	0h	When asserted while controller is disabled, the immediate command/data register will be cleared. Self-cleared control bit.
19	IBI_FLUSH	W	0h	When asserted while controller is disabled, the IBI data memory block read/write pointers will be set to 0. Self-cleared control bit.
18	RX_FLUSH	W	0h	When asserted while controller is disabled, the Rx Data memory block read/write pointers will be set to 0. Self-cleared control bit.
17	TX_FLUSH	W	0h	When asserted while controller is disabled, the Tx Data memory block read/write pointers will be set to 0. Self-cleared control bit.
16	CMD_FLUSH	W	0h	When asserted while controller is disabled, the command Command memory block read/write pointers will be set to 0. Self-cleared control bit.
15-0	RESERVED	W	X	

4.38 I3C_TTO_PRESCL_CTRL0 Register (Offset = B0h) [reset = 03FF07FFh]

I3C_TTO_PRESCL_CTRL0 is shown in [Figure 4-37](#) and described in [Table 4-78](#).

[Return to the Summary Table.](#)

Prescale settings for First SCL high timeout detection

Table 4-77. I3C_TTO_PRESCL_CTRL0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 80B0h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 80B0h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 80B0h

Figure 4-37. I3C_TTO_PRESCL_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD1						DIV_B						RSVD0						DIV_A													
R-0h						R/W-3FFh						R-0h						R/W-7FFh													

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-78. I3C_TTO_PRESCL_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RSVD1	R	0h	Reserved
25-16	DIV_B	R/W	3FFh	Divider B
15-11	RSVD0	R	0h	Reserved
10-0	DIV_A	R/W	7FFh	Divider A

4.39 I3C_TTO_PRESCL_CTRL1 Register (Offset = B4h) [reset = 03FF00FFh]

I3C_TTO_PRESCL_CTRL1 is shown in [Figure 4-38](#) and described in [Table 4-80](#).

Return to the [Summary Table](#).

Prescale settings for SCL high and low timeout detection

Table 4-79. I3C_TTO_PRESCL_CTRL1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80B4h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80B4h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80B4h

Figure 4-38. I3C_TTO_PRESCL_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD1								DIV_B								RSVD0								DIV_A							
R-0h								R/W-3FFh								R-0h								R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-80. I3C_TTO_PRESCL_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RSVD1	R	0h	Reserved
25-16	DIV_B	R/W	3FFh	Divider B
15-8	RSVD0	R	0h	Reserved
7-0	DIV_A	R/W	FFh	Divider A

4.40 I3C_DEVS_CTRL Register (Offset = B8h) [reset = 1h]

I3C_DEVS_CTRL is shown in [Figure 4-39](#) and described in [Table 4-82](#).

Return to the [Summary Table](#).

Device control register

Table 4-81. I3C_DEVS_CTRL Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 80B8h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 80B8h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 80B8h

Figure 4-39. I3C_DEVS_CTRL Register

31	30	29	28	27	26	25	24
RSVD1				DEV11_CLR	DEV10_CLR	DEV9_CLR	DEV8_CLR
R-0h				W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
DEV7_CLR	DEV6_CLR	DEV5_CLR	DEV4_CLR	DEV3_CLR	DEV2_CLR	DEV1_CLR	RSVD0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R-0h
15	14	13	12	11	10	9	8
RSVD0				DEV11_ACTIVE	DEV10_ACTIVE	DEV9_ACTIVE	DEV8_ACTIVE
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DEV7_ACTIVE	DEV6_ACTIVE	DEV5_ACTIVE	DEV4_ACTIVE	DEV3_ACTIVE	DEV2_ACTIVE	DEV1_ACTIVE	DEV0_ACTIVE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-1h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-82. I3C_DEVS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RSVD1	R	0h	Reserved.
27	DEV11_CLR	W	0h	Clear DevID11 retaining registers set. Self-cleared bit.
26	DEV10_CLR	W	0h	Clear DevID10 retaining registers set. Self-cleared bit.
25	DEV9_CLR	W	0h	Clear DevID9 retaining registers set. Self-cleared bit.
24	DEV8_CLR	W	0h	Clear DevID8 retaining registers set. Self-cleared bit.
23	DEV7_CLR	W	0h	Clear DevID7 retaining registers set. Self-cleared bit.
22	DEV6_CLR	W	0h	Clear DevID6 retaining registers set. Self-cleared bit.
21	DEV5_CLR	W	0h	Clear DevID5 retaining registers set. Self-cleared bit.
20	DEV4_CLR	W	0h	Clear DevID4 retaining registers set. Self-cleared bit.

Table 4-82. I3C_DEVS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	DEV3_CLR	W	0h	Clear DevID3 retaining registers set. Self-cleared bit.
18	DEV2_CLR	W	0h	Clear DevID2 retaining registers set. Self-cleared bit.
17	DEV1_CLR	W	0h	Clear DevID1 retaining registers set. Self-cleared bit.
16-12	RSVD0	R	0h	Reserved.
11	DEV11_ACTIVE	R/W	0h	DevID11 is active - has either valid DA or SA.
10	DEV10_ACTIVE	R/W	0h	DevID10 is active - has either valid DA or SA.
9	DEV9_ACTIVE	R/W	0h	DevID9 is active - has either valid DA or SA.
8	DEV8_ACTIVE	R/W	0h	DevID8 is active - has either valid DA or SA.
7	DEV7_ACTIVE	R/W	0h	DevID7 is active - has either valid DA or SA.
6	DEV6_ACTIVE	R/W	0h	DevID6 is active - has either valid DA or SA.
5	DEV5_ACTIVE	R/W	0h	DevID5 is active - has either valid DA or SA.
4	DEV4_ACTIVE	R/W	0h	DevID4 is active - has either valid DA or SA.
3	DEV3_ACTIVE	R/W	0h	DevID3 is active - has either valid DA or SA.
2	DEV2_ACTIVE	R/W	0h	DevID2 is active - has either valid DA or SA.
1	DEV1_ACTIVE	R/W	0h	DevID1 is active - has either valid DA or SA.
0	DEV0_ACTIVE	R	1h	DevID0 is active - has either valid DA or SA.

4.41 I3C_DEV_ID0_RR0 Register (Offset = C0h) [reset = X]

I3C_DEV_ID0_RR0 is shown in [Figure 4-40](#) and described in [Table 4-84](#).

Return to the [Summary Table](#).

Device ID 0 Retaining Register 0 : Configuration Register

Table 4-83. I3C_DEV_ID0_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 80C0h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 80C0h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 80C0h

Figure 4-40. I3C_DEV_ID0_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-84. I3C_DEV_ID0_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 0 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device0_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R	1h	Device 0 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-84. I3C_DEV_ID0_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	10h	Device 0 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.42 I3C_DEV_ID0_RR1 Register (Offset = C4h) [reset = 02040000h]

I3C_DEV_ID0_RR1 is shown in [Figure 4-41](#) and described in [Table 4-86](#).

Return to the [Summary Table](#).

Device ID 0 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-85. I3C_DEV_ID0_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80C4h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80C4h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80C4h

Figure 4-41. I3C_DEV_ID0_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-02040000h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-86. I3C_DEV_ID0_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	02040000h	Device 0 48 to 16 Dev ID bits

4.43 I3C_DEV_ID0_RR2 Register (Offset = C8h) [reset = 6200h]

I3C_DEV_ID0_RR2 is shown in [Figure 4-42](#) and described in [Table 4-88](#).

Return to the [Summary Table](#).

Device ID 0 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-87. I3C_DEV_ID0_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 80C8h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 80C8h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 80C8h

Figure 4-42. I3C_DEV_ID0_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR								DCR_LVR							
R/W-0h																R/W-62h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-88. I3C_DEV_ID0_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 0 15 to 0 Dev ID bits
15-8	BCR	R/W	62h	Device 0 BCR register
7-0	DCR_LVR	R/W	0h	Device 0 DCR [if I3C device] or LVR [if I2C device] register Decoding if used as DCR: Bits [7:0]: 255 available codes for describing the type of sensor, or Device Decoding if used as LVR: Bits [7:4]: Device 0 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system Bits [3:3]: Device 0 LVR Slave operation mode: 1'b0 FM mode 1'b1 FM+ mode Bits [2:0]: Device 0 LVR Index: 3'b000 Index 0 3'b001 Index 1 3'b010 Index 2 3'b011 Index 3 [Reserved] 3'b100 Index 4 [Reserved] 3'b101 Index 5 [Reserved] 3'b110 Index 6 [Reserved] 3'b111 Index 7 [Reserved]

4.44 I3C_DEV_ID1_RR0 Register (Offset = D0h) [reset = X]

I3C_DEV_ID1_RR0 is shown in [Figure 4-43](#) and described in [Table 4-90](#).

Return to the [Summary Table](#).

Device ID 1 Retaining Register 0 : Configuration Register

Table 4-89. I3C_DEV_ID1_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80D0h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80D0h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80D0h

Figure 4-43. I3C_DEV_ID1_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-13h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-90. I3C_DEV_ID1_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 1 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device1_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 1 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-90. I3C_DEV_ID1_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	13h	Device 1 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.45 I3C_DEV_ID1_RR1 Register (Offset = D4h) [reset = 0h]

I3C_DEV_ID1_RR1 is shown in [Figure 4-44](#) and described in [Table 4-92](#).

Return to the [Summary Table](#).

Device ID 1 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-91. I3C_DEV_ID1_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80D4h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80D4h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80D4h

Figure 4-44. I3C_DEV_ID1_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-92. I3C_DEV_ID1_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 1 48 to 16 Dev ID bits

4.46 I3C_DEV_ID1_RR2 Register (Offset = D8h) [reset = 0h]

I3C_DEV_ID1_RR2 is shown in [Figure 4-45](#) and described in [Table 4-94](#).

Return to the [Summary Table](#).

Device ID 1 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-93. I3C_DEV_ID1_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80D8h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80D8h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80D8h

Figure 4-45. I3C_DEV_ID1_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-94. I3C_DEV_ID1_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 1 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 1 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 1 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 1 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 1 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 1 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.47 I3C_DEV_ID2_RR0 Register (Offset = E0h) [reset = X]

I3C_DEV_ID2_RR0 is shown in [Figure 4-46](#) and described in [Table 4-96](#).

Return to the [Summary Table](#).

Device ID 2 Retaining Register 0 : Configuration Register

Table 4-95. I3C_DEV_ID2_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80E0h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80E0h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80E0h

Figure 4-46. I3C_DEV_ID2_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-15h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-96. I3C_DEV_ID2_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 2 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device2_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 2 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-96. I3C_DEV_ID2_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	15h	Device 2 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.48 I3C_DEV_ID2_RR1 Register (Offset = E4h) [reset = 0h]

I3C_DEV_ID2_RR1 is shown in [Figure 4-47](#) and described in [Table 4-98](#).

Return to the [Summary Table](#).

Device ID 2 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-97. I3C_DEV_ID2_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80E4h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80E4h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80E4h

Figure 4-47. I3C_DEV_ID2_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-98. I3C_DEV_ID2_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 2 48 to 16 Dev ID bits

4.49 I3C_DEV_ID2_RR2 Register (Offset = E8h) [reset = 0h]

I3C_DEV_ID2_RR2 is shown in [Figure 4-48](#) and described in [Table 4-100](#).

Return to the [Summary Table](#).

Device ID 2 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-99. I3C_DEV_ID2_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 80E8h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 80E8h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 80E8h

Figure 4-48. I3C_DEV_ID2_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-100. I3C_DEV_ID2_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 2 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 2 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 2 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 2 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 2 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 2 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.50 I3C_DEV_ID3_RR0 Register (Offset = F0h) [reset = X]

I3C_DEV_ID3_RR0 is shown in [Figure 4-49](#) and described in [Table 4-102](#).

Return to the [Summary Table](#).

Device ID 3 Retaining Register 0 : Configuration Register

Table 4-101. I3C_DEV_ID3_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 80F0h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 80F0h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 80F0h

Figure 4-49. I3C_DEV_ID3_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-16h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-102. I3C_DEV_ID3_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 3 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device3_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 3 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-102. I3C_DEV_ID3_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	16h	Device 3 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.51 I3C_DEV_ID3_RR1 Register (Offset = F4h) [reset = 0h]

I3C_DEV_ID3_RR1 is shown in [Figure 4-50](#) and described in [Table 4-104](#).

Return to the [Summary Table](#).

Device ID 3 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-103. I3C_DEV_ID3_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80F4h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80F4h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80F4h

Figure 4-50. I3C_DEV_ID3_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-104. I3C_DEV_ID3_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 3 48 to 16 Dev ID bits

4.52 I3C_DEV_ID3_RR2 Register (Offset = F8h) [reset = 0h]

I3C_DEV_ID3_RR2 is shown in [Figure 4-51](#) and described in [Table 4-106](#).

Return to the [Summary Table](#).

Device ID 3 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-105. I3C_DEV_ID3_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 80F8h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 80F8h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 80F8h

Figure 4-51. I3C_DEV_ID3_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR								DCR_LVR							
R/W-0h																R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-106. I3C_DEV_ID3_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 3 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 3 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 3 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 3 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 3 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 3 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.53 I3C_DEV_ID4_RR0 Register (Offset = 100h) [reset = X]

I3C_DEV_ID4_RR0 is shown in [Figure 4-52](#) and described in [Table 4-108](#).

Return to the [Summary Table](#).

Device ID 4 Retaining Register 0 : Configuration Register

Table 4-107. I3C_DEV_ID4_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8100h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8100h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8100h

Figure 4-52. I3C_DEV_ID4_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-19h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-108. I3C_DEV_ID4_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 4 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device4_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 4 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-108. I3C_DEV_ID4_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	19h	Device 4 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.54 I3C_DEV_ID4_RR1 Register (Offset = 104h) [reset = 0h]

I3C_DEV_ID4_RR1 is shown in [Figure 4-53](#) and described in [Table 4-110](#).

Return to the [Summary Table](#).

Device ID 4 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-109. I3C_DEV_ID4_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8104h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8104h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8104h

Figure 4-53. I3C_DEV_ID4_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-110. I3C_DEV_ID4_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 4 48 to 16 Dev ID bits

4.55 I3C_DEV_ID4_RR2 Register (Offset = 108h) [reset = 0h]

I3C_DEV_ID4_RR2 is shown in [Figure 4-54](#) and described in [Table 4-112](#).

Return to the [Summary Table](#).

Device ID 4 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-111. I3C_DEV_ID4_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8108h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8108h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8108h

Figure 4-54. I3C_DEV_ID4_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-112. I3C_DEV_ID4_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 4 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 4 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 4 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 4 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 4 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 4 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.56 I3C_DEV_ID5_RR0 Register (Offset = 110h) [reset = X]

I3C_DEV_ID5_RR0 is shown in [Figure 4-55](#) and described in [Table 4-114](#).

Return to the [Summary Table](#).

Device ID 5 Retaining Register 0 : Configuration Register

Table 4-113. I3C_DEV_ID5_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8110h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8110h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8110h

Figure 4-55. I3C_DEV_ID5_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-1Ah							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-114. I3C_DEV_ID5_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 5 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device5_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 5 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-114. I3C_DEV_ID5_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	1Ah	Device 5 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.57 I3C_DEV_ID5_RR1 Register (Offset = 114h) [reset = 0h]

I3C_DEV_ID5_RR1 is shown in [Figure 4-56](#) and described in [Table 4-116](#).

Return to the [Summary Table](#).

Device ID 5 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-115. I3C_DEV_ID5_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8114h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8114h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8114h

Figure 4-56. I3C_DEV_ID5_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-116. I3C_DEV_ID5_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 5 48 to 16 Dev ID bits

4.58 I3C_DEV_ID5_RR2 Register (Offset = 118h) [reset = 0h]

I3C_DEV_ID5_RR2 is shown in [Figure 4-57](#) and described in [Table 4-118](#).

Return to the [Summary Table](#).

Device ID 5 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-117. I3C_DEV_ID5_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8118h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8118h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8118h

Figure 4-57. I3C_DEV_ID5_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-118. I3C_DEV_ID5_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 5 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 5 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 5 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 5 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 5 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 5 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.59 I3C_DEV_ID6_RR0 Register (Offset = 120h) [reset = X]

I3C_DEV_ID6_RR0 is shown in [Figure 4-58](#) and described in [Table 4-120](#).

Return to the [Summary Table](#).

Device ID 6 Retaining Register 0 : Configuration Register

Table 4-119. I3C_DEV_ID6_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8120h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8120h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8120h

Figure 4-58. I3C_DEV_ID6_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-1Ch							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-120. I3C_DEV_ID6_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 6 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device6_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 6 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-120. I3C_DEV_ID6_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	1Ch	Device 6 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.60 I3C_DEV_ID6_RR1 Register (Offset = 124h) [reset = 0h]

I3C_DEV_ID6_RR1 is shown in [Figure 4-59](#) and described in [Table 4-122](#).

Return to the [Summary Table](#).

Device ID 6 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-121. I3C_DEV_ID6_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8124h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8124h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8124h

Figure 4-59. I3C_DEV_ID6_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-122. I3C_DEV_ID6_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 6 48 to 16 Dev ID bits

4.61 I3C_DEV_ID6_RR2 Register (Offset = 128h) [reset = 0h]

I3C_DEV_ID6_RR2 is shown in [Figure 4-60](#) and described in [Table 4-124](#).

Return to the [Summary Table](#).

Device ID 6 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-123. I3C_DEV_ID6_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8128h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8128h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8128h

Figure 4-60. I3C_DEV_ID6_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-124. I3C_DEV_ID6_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 6 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 6 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 6 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 6 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 6 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 6 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.62 I3C_DEV_ID7_RR0 Register (Offset = 130h) [reset = X]

I3C_DEV_ID7_RR0 is shown in [Figure 4-61](#) and described in [Table 4-126](#).

Return to the [Summary Table](#).

Device ID 7 Retaining Register 0 : Configuration Register

Table 4-125. I3C_DEV_ID7_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8130h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8130h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8130h

Figure 4-61. I3C_DEV_ID7_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-1Fh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-126. I3C_DEV_ID7_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 7 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device7_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 7 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-126. I3C_DEV_ID7_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	1Fh	Device 7 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.63 I3C_DEV_ID7_RR1 Register (Offset = 134h) [reset = 0h]

I3C_DEV_ID7_RR1 is shown in [Figure 4-62](#) and described in [Table 4-128](#).

Return to the [Summary Table](#).

Device ID 7 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-127. I3C_DEV_ID7_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8134h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8134h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8134h

Figure 4-62. I3C_DEV_ID7_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-128. I3C_DEV_ID7_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 7 48 to 16 Dev ID bits

4.64 I3C_DEV_ID7_RR2 Register (Offset = 138h) [reset = 0h]

I3C_DEV_ID7_RR2 is shown in [Figure 4-63](#) and described in [Table 4-130](#).

Return to the [Summary Table](#).

Device ID 7 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-129. I3C_DEV_ID7_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8138h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8138h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8138h

Figure 4-63. I3C_DEV_ID7_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-130. I3C_DEV_ID7_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 7 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 7 BCR register
7-0	DCR_LVR	R/W	0h	Device 7 DCR [if I3C device] or LVR [if I2C device] register Decoding if used as DCR: Bits [7:0]: 255 available codes for describing the type of sensor, or Device Decoding if used as LVR: Bits [7:4]: Device 7 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system Bits [3:3]: Device 7 LVR Slave operation mode: 1'b0 FM mode 1'b1 FM+ mode Bits [2:0]: Device 7 LVR Index: 3'b000 Index 0 3'b001 Index 1 3'b010 Index 2 3'b011 Index 3 [Reserved] 3'b100 Index 4 [Reserved] 3'b101 Index 5 [Reserved] 3'b110 Index 6 [Reserved] 3'b111 Index 7 [Reserved]

4.65 I3C_DEV_ID8_RR0 Register (Offset = 140h) [reset = X]

I3C_DEV_ID8_RR0 is shown in [Figure 4-64](#) and described in [Table 4-132](#).

Return to the [Summary Table](#).

Device ID 8 Retaining Register 0 : Configuration Register

Table 4-131. I3C_DEV_ID8_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8140h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8140h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8140h

Figure 4-64. I3C_DEV_ID8_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-20h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-132. I3C_DEV_ID8_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 8 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device8_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 8 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-132. I3C_DEV_ID8_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	20h	Device 8 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.66 I3C_DEV_ID8_RR1 Register (Offset = 144h) [reset = 0h]

I3C_DEV_ID8_RR1 is shown in [Figure 4-65](#) and described in [Table 4-134](#).

Return to the [Summary Table](#).

Device ID 8 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-133. I3C_DEV_ID8_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8144h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8144h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8144h

Figure 4-65. I3C_DEV_ID8_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-134. I3C_DEV_ID8_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 8 48 to 16 Dev ID bits

4.67 I3C_DEV_ID8_RR2 Register (Offset = 148h) [reset = 0h]

I3C_DEV_ID8_RR2 is shown in [Figure 4-66](#) and described in [Table 4-136](#).

Return to the [Summary Table](#).

Device ID 8 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-135. I3C_DEV_ID8_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8148h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8148h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8148h

Figure 4-66. I3C_DEV_ID8_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-136. I3C_DEV_ID8_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 8 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 8 BCR register
7-0	DCR_LVR	R/W	0h	Device 8 DCR [if I3C device] or LVR [if I2C device] register Decoding if used as DCR: Bits [7:0]: 255 available codes for describing the type of sensor, or Device Decoding if used as LVR: Bits [7:4]: Device 8 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system Bits [3:3]: Device 8 LVR Slave operation mode: 1'b0 FM mode 1'b1 FM+ mode Bits [2:0]: Device 8 LVR Index: 3'b000 Index 0 3'b001 Index 1 3'b010 Index 2 3'b011 Index 3 [Reserved] 3'b100 Index 4 [Reserved] 3'b101 Index 5 [Reserved] 3'b110 Index 6 [Reserved] 3'b111 Index 7 [Reserved]

4.68 I3C_DEV_ID9_RR0 Register (Offset = 150h) [reset = X]

I3C_DEV_ID9_RR0 is shown in [Figure 4-67](#) and described in [Table 4-138](#).

Return to the [Summary Table](#).

Device ID 9 Retaining Register 0 : Configuration Register

Table 4-137. I3C_DEV_ID9_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8150h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8150h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8150h

Figure 4-67. I3C_DEV_ID9_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-23h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-138. I3C_DEV_ID9_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 9 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device9_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 9 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-138. I3C_DEV_ID9_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	23h	Device 9 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.69 I3C_DEV_ID9_RR1 Register (Offset = 154h) [reset = 0h]

I3C_DEV_ID9_RR1 is shown in [Figure 4-68](#) and described in [Table 4-140](#).

Return to the [Summary Table](#).

Device ID 9 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-139. I3C_DEV_ID9_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8154h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8154h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8154h

Figure 4-68. I3C_DEV_ID9_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-140. I3C_DEV_ID9_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 9 48 to 16 Dev ID bits

4.70 I3C_DEV_ID9_RR2 Register (Offset = 158h) [reset = 0h]

I3C_DEV_ID9_RR2 is shown in [Figure 4-69](#) and described in [Table 4-142](#).

Return to the [Summary Table](#).

Device ID 9 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-141. I3C_DEV_ID9_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8158h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8158h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8158h

Figure 4-69. I3C_DEV_ID9_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-142. I3C_DEV_ID9_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 9 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 9 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 9 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 9 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 9 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 9 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.71 I3C_DEV_ID10_RR0 Register (Offset = 160h) [reset = X]

I3C_DEV_ID10_RR0 is shown in [Figure 4-70](#) and described in [Table 4-144](#).

Return to the [Summary Table](#).

Device ID 10 Retaining Register 0 : Configuration Register

Table 4-143. I3C_DEV_ID10_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8160h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8160h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8160h

Figure 4-70. I3C_DEV_ID10_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-25h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-144. I3C_DEV_ID10_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 10 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device10_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 10 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-144. I3C_DEV_ID10_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	25h	Device 10 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.72 I3C_DEV_ID10_RR1 Register (Offset = 164h) [reset = 0h]

I3C_DEV_ID10_RR1 is shown in [Figure 4-71](#) and described in [Table 4-146](#).

Return to the [Summary Table](#).

Device ID 10 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-145. I3C_DEV_ID10_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8164h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8164h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8164h

Figure 4-71. I3C_DEV_ID10_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-146. I3C_DEV_ID10_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 10 48 to 16 Dev ID bits

4.73 I3C_DEV_ID10_RR2 Register (Offset = 168h) [reset = 0h]

I3C_DEV_ID10_RR2 is shown in [Figure 4-72](#) and described in [Table 4-148](#).

Return to the [Summary Table](#).

Device ID 10 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-147. I3C_DEV_ID10_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8168h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8168h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8168h

Figure 4-72. I3C_DEV_ID10_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-148. I3C_DEV_ID10_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 10 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 10 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 10 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 10 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 10 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 10 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.74 I3C_DEV_ID11_RR0 Register (Offset = 170h) [reset = X]

I3C_DEV_ID11_RR0 is shown in [Figure 4-73](#) and described in [Table 4-150](#).

Return to the [Summary Table](#).

Device ID 11 Retaining Register 0 : Configuration Register

Table 4-149. I3C_DEV_ID11_RR0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8170h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8170h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8170h

Figure 4-73. I3C_DEV_ID11_RR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
LVR_SA_MSB			RSVD2	LVR_EXT_ADD R	RSVD1	IS_I3C	RSVD0
R/W-0h			R-0h	R/W-0h	R-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
DEV_ADDR							
R/W-26h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-150. I3C_DEV_ID11_RR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	LVR_SA_MSB	R/W	0h	MSB bits of Legacy I2C Device with 10-bit addressing.
12	RSVD2	R	0h	Reserved
11	LVR_EXT_ADDR	R/W	0h	Device 11 Address mode used: 0 - 7-bit addressing - applicable for I3C and I2C devices. 1 - 10-bit addressing - applicable only for I2C devices with 10-bit extended address. NOTE: Invalid setting when Device11_RR0.is_i3c=1
10	RSVD1	R	0h	Reserved
9	IS_I3C	R/W	1h	Device 11 I3C mode Operation 1 Yes 0 No
8	RSVD0	R	0h	Reserved

Table 4-150. I3C_DEV_ID11_RR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DEV_ADDR	R/W	26h	Device 11 Slave Dynamic [Static/Legacy] Address bits 7:1 bit 0 - parity XOR check -> ~XOR[Slave_Addr [7:1]].

4.75 I3C_DEV_ID11_RR1 Register (Offset = 174h) [reset = 0h]

I3C_DEV_ID11_RR1 is shown in [Figure 4-74](#) and described in [Table 4-152](#).

Return to the [Summary Table](#).

Device ID 11 Retaining Register 1 : Provisional ID MSB 32-bits

Table 4-151. I3C_DEV_ID11_RR1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8174h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8174h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8174h

Figure 4-74. I3C_DEV_ID11_RR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_MSB																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-152. I3C_DEV_ID11_RR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID_MSB	R/W	0h	Device 11 48 to 16 Dev ID bits

4.76 I3C_DEV_ID11_RR2 Register (Offset = 178h) [reset = 0h]

I3C_DEV_ID11_RR2 is shown in [Figure 4-75](#) and described in [Table 4-154](#).

Return to the [Summary Table](#).

Device ID 11 Retaining Register 2 : Provisional ID LSB 16-bits, BCR, DCR or LVR (for legacy Mode)

Table 4-153. I3C_DEV_ID11_RR2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8178h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8178h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8178h

Figure 4-75. I3C_DEV_ID11_RR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID_LSB																BCR				DCR_LVR											
R/W-0h																R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-154. I3C_DEV_ID11_RR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PID_LSB	R/W	0h	Device 11 15 to 0 Dev ID bits
15-8	BCR	R/W	0h	Device 11 BCR register
7-0	DCR_LVR	R/W	0h	<p>Device 11 DCR [if I3C device] or LVR [if I2C device] register</p> <p>Decoding if used as DCR:</p> <p>Bits</p> <p>[7:0]: 255 available codes for describing the type of sensor, or Device</p> <p>Decoding if used as LVR:</p> <p>Bits</p> <p>[7:4]: Device 11 LVR Code: 15 available codes for describing the Device capabilities and function on the sensors' system</p> <p>Bits</p> <p>[3:3]: Device 11 LVR Slave operation mode:</p> <p>1'b0 FM mode</p> <p>1'b1 FM+ mode</p> <p>Bits</p> <p>[2:0]: Device 11 LVR Index:</p> <p>3'b000 Index 0</p> <p>3'b001 Index 1</p> <p>3'b010 Index 2</p> <p>3'b011 Index 3 [Reserved]</p> <p>3'b100 Index 4 [Reserved]</p> <p>3'b101 Index 5 [Reserved]</p> <p>3'b110 Index 6 [Reserved]</p> <p>3'b111 Index 7 [Reserved]</p>

4.77 I3C_SIR_MAP0 Register (Offset = 180h) [reset = 00FE00Feh]

I3C_SIR_MAP0 is shown in [Figure 4-76](#) and described in [Table 4-156](#).

Return to the [Summary Table](#).

Slave-initiated request Device ID Detection register0

Table 4-155. I3C_SIR_MAP0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8180h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8180h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8180h

Figure 4-76. I3C_SIR_MAP0 Register

31	30	29	28	27	26	25	24
DEVID1_ROLE		DEVID1_SLOW	DEVID1_PL				
R/W-0h		R/W-0h	R/W-0h				
23	22	21	20	19	18	17	16
DEVID1_DA							DEVID1_RESP
R/W-7Fh							R/W-0h
15	14	13	12	11	10	9	8
DEVID0_ROLE		DEVID0_SLOW	DEVID0_PL				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
DEVID0_DA							DEVID0_RESP
R/W-7Fh							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-156. I3C_SIR_MAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DEVID1_ROLE	R/W	0h	Slave-initiated request Device ID0 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
29	DEVID1_SLOW	R/W	0h	Slave-initiated request Device ID0 Max Data Speed Limitation 0 - No limitation 1 - Limitation
28-24	DEVID1_PL	R/W	0h	Slave-initiated request Device ID0 payload length
23-17	DEVID1_DA	R/W	7Fh	Slave-initiated request Device ID0 DA
16	DEVID1_RESP	R/W	0h	Slave-initiated request Device ID0 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

Table 4-156. I3C_SIR_MAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	DEVID0_ROLE	R/W	0h	Slave-initiated request Device ID0 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
13	DEVID0_SLOW	R/W	0h	Slave-initiated request Device ID0 Max Data Speed Limitation 0 - No limitation 1 - Limitation
12-8	DEVID0_PL	R/W	0h	Slave-initiated request Device ID0 payload length
7-1	DEVID0_DA	R/W	7Fh	Slave-initiated request Device ID0 DA
0	DEVID0_RESP	R/W	0h	Slave-initiated request Device ID0 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

4.78 I3C_SIR_MAP1 Register (Offset = 184h) [reset = 00FE00Feh]

I3C_SIR_MAP1 is shown in [Figure 4-77](#) and described in [Table 4-158](#).

Return to the [Summary Table](#).

Slave-initiated request Device ID Detection register1

Table 4-157. I3C_SIR_MAP1 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8184h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8184h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8184h

Figure 4-77. I3C_SIR_MAP1 Register

31	30	29	28	27	26	25	24
DEVID3_ROLE		DEVID3_SLOW	DEVID3_PL				
R/W-0h		R/W-0h	R/W-0h				
23	22	21	20	19	18	17	16
DEVID3_DA							DEVID3_RESP
R/W-7Fh							R/W-0h
15	14	13	12	11	10	9	8
DEVID2_ROLE		DEVID2_SLOW	DEVID2_PL				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
DEVID2_DA							DEVID2_RESP
R/W-7Fh							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-158. I3C_SIR_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DEVID3_ROLE	R/W	0h	Slave-initiated request Device ID2 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
29	DEVID3_SLOW	R/W	0h	Slave-initiated request Device ID2 Max Data Speed Limitation 0 - No limitation 1 - Limitation
28-24	DEVID3_PL	R/W	0h	Slave-initiated request Device ID2 payload length
23-17	DEVID3_DA	R/W	7Fh	Slave-initiated request Device ID2 DA
16	DEVID3_RESP	R/W	0h	Slave-initiated request Device ID2 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

Table 4-158. I3C_SIR_MAP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	DEVID2_ROLE	R/W	0h	Slave-initiated request Device ID2 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
13	DEVID2_SLOW	R/W	0h	Slave-initiated request Device ID2 Max Data Speed Limitation 0 - No limitation 1 - Limitation
12-8	DEVID2_PL	R/W	0h	Slave-initiated request Device ID2 payload length
7-1	DEVID2_DA	R/W	7Fh	Slave-initiated request Device ID2 DA
0	DEVID2_RESP	R/W	0h	Slave-initiated request Device ID2 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

4.79 I3C_SIR_MAP2 Register (Offset = 188h) [reset = 00FE00Feh]

I3C_SIR_MAP2 is shown in [Figure 4-78](#) and described in [Table 4-160](#).

Return to the [Summary Table](#).

Slave-initiated request Device ID Detection register2

Table 4-159. I3C_SIR_MAP2 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8188h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8188h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8188h

Figure 4-78. I3C_SIR_MAP2 Register

31	30	29	28	27	26	25	24
DEVID5_ROLE		DEVID5_SLOW	DEVID5_PL				
R/W-0h		R/W-0h	R/W-0h				
23	22	21	20	19	18	17	16
DEVID5_DA							DEVID5_RESP
R/W-7Fh							R/W-0h
15	14	13	12	11	10	9	8
DEVID4_ROLE		DEVID4_SLOW	DEVID4_PL				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
DEVID4_DA							DEVID4_RESP
R/W-7Fh							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-160. I3C_SIR_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DEVID5_ROLE	R/W	0h	Slave-initiated request Device ID4 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
29	DEVID5_SLOW	R/W	0h	Slave-initiated request Device ID4 Max Data Speed Limitation 0 - No limitation 1 - Limitation
28-24	DEVID5_PL	R/W	0h	Slave-initiated request Device ID4 payload length
23-17	DEVID5_DA	R/W	7Fh	Slave-initiated request Device ID4 DA
16	DEVID5_RESP	R/W	0h	Slave-initiated request Device ID4 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

Table 4-160. I3C_SIR_MAP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	DEVID4_ROLE	R/W	0h	Slave-initiated request Device ID4 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
13	DEVID4_SLOW	R/W	0h	Slave-initiated request Device ID4 Max Data Speed Limitation 0 - No limitation 1 - Limitation
12-8	DEVID4_PL	R/W	0h	Slave-initiated request Device ID4 payload length
7-1	DEVID4_DA	R/W	7Fh	Slave-initiated request Device ID4 DA
0	DEVID4_RESP	R/W	0h	Slave-initiated request Device ID4 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

4.80 I3C_SIR_MAP3 Register (Offset = 18Ch) [reset = 00FE00Feh]

I3C_SIR_MAP3 is shown in [Figure 4-79](#) and described in [Table 4-162](#).

Return to the [Summary Table](#).

Slave-initiated request Device ID Detection register3

Table 4-161. I3C_SIR_MAP3 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 818Ch
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 818Ch
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 818Ch

Figure 4-79. I3C_SIR_MAP3 Register

31	30	29	28	27	26	25	24
DEVID7_ROLE		DEVID7_SLOW	DEVID7_PL				
R/W-0h		R/W-0h	R/W-0h				
23	22	21	20	19	18	17	16
DEVID7_DA							DEVID7_RESP
R/W-7Fh							R/W-0h
15	14	13	12	11	10	9	8
DEVID6_ROLE		DEVID6_SLOW	DEVID6_PL				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
DEVID6_DA							DEVID6_RESP
R/W-7Fh							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-162. I3C_SIR_MAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DEVID7_ROLE	R/W	0h	Slave-initiated request Device ID6 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
29	DEVID7_SLOW	R/W	0h	Slave-initiated request Device ID6 Max Data Speed Limitation 0 - No limitation 1 - Limitation
28-24	DEVID7_PL	R/W	0h	Slave-initiated request Device ID6 payload length
23-17	DEVID7_DA	R/W	7Fh	Slave-initiated request Device ID6 DA
16	DEVID7_RESP	R/W	0h	Slave-initiated request Device ID6 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

Table 4-162. I3C_SIR_MAP3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	DEVID6_ROLE	R/W	0h	Slave-initiated request Device ID6 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
13	DEVID6_SLOW	R/W	0h	Slave-initiated request Device ID6 Max Data Speed Limitation 0 - No limitation 1 - Limitation
12-8	DEVID6_PL	R/W	0h	Slave-initiated request Device ID6 payload length
7-1	DEVID6_DA	R/W	7Fh	Slave-initiated request Device ID6 DA
0	DEVID6_RESP	R/W	0h	Slave-initiated request Device ID6 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

4.81 I3C_SIR_MAP4 Register (Offset = 190h) [reset = 00FE00FEh]

I3C_SIR_MAP4 is shown in [Figure 4-80](#) and described in [Table 4-164](#).

Return to the [Summary Table](#).

Slave-initiated request Device ID Detection register4

Table 4-163. I3C_SIR_MAP4 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8190h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8190h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8190h

Figure 4-80. I3C_SIR_MAP4 Register

31	30	29	28	27	26	25	24
DEVID9_ROLE		DEVID9_SLOW	DEVID9_PL				
R/W-0h		R/W-0h	R/W-0h				
23	22	21	20	19	18	17	16
DEVID9_DA							DEVID9_RESP
R/W-7Fh							R/W-0h
15	14	13	12	11	10	9	8
DEVID8_ROLE		DEVID8_SLOW	DEVID8_PL				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
DEVID8_DA							DEVID8_RESP
R/W-7Fh							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-164. I3C_SIR_MAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	DEVID9_ROLE	R/W	0h	Slave-initiated request Device ID8 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
29	DEVID9_SLOW	R/W	0h	Slave-initiated request Device ID8 Max Data Speed Limitation 0 - No limitation 1 - Limitation
28-24	DEVID9_PL	R/W	0h	Slave-initiated request Device ID8 payload length
23-17	DEVID9_DA	R/W	7Fh	Slave-initiated request Device ID8 DA
16	DEVID9_RESP	R/W	0h	Slave-initiated request Device ID8 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

Table 4-164. I3C_SIR_MAP4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	DEVID8_ROLE	R/W	0h	Slave-initiated request Device ID8 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
13	DEVID8_SLOW	R/W	0h	Slave-initiated request Device ID8 Max Data Speed Limitation 0 - No limitation 1 - Limitation
12-8	DEVID8_PL	R/W	0h	Slave-initiated request Device ID8 payload length
7-1	DEVID8_DA	R/W	7Fh	Slave-initiated request Device ID8 DA
0	DEVID8_RESP	R/W	0h	Slave-initiated request Device ID8 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

4.82 I3C_SIR_MAP5 Register (Offset = 194h) [reset = X]

I3C_SIR_MAP5 is shown in [Figure 4-81](#) and described in [Table 4-166](#).

Return to the [Summary Table](#).

Slave-initiated request Device ID Detection register5

Table 4-165. I3C_SIR_MAP5 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8194h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8194h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8194h

Figure 4-81. I3C_SIR_MAP5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
DEVID10_ROLE		DEVID10_SLOW	DEVID10_PL				
R/W-0h		R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
DEVID10_DA							DEVID10_RESP
R/W-7Fh							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-166. I3C_SIR_MAP5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	DEVID10_ROLE	R/W	0h	Slave-initiated request Device ID10 BCR role 2'b 00 - Slave 2'b 01 - Master/Secondary Master 2'b 10 - Reserved 2'b 11 - Reserved
13	DEVID10_SLOW	R/W	0h	Slave-initiated request Device ID10 Max Data Speed Limitation 0 - No limitation 1 - Limitation
12-8	DEVID10_PL	R/W	0h	Slave-initiated request Device ID10 payload length
7-1	DEVID10_DA	R/W	7Fh	Slave-initiated request Device ID10 DA

Table 4-166. I3C_SIR_MAP5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DEVID10_RESP	R/W	0h	Slave-initiated request Device ID10 Ack/Nack response 0 - NACK each request from this device. 1 - ACK each request from this device.

4.83 I3C_GPIR_WORD0 Register (Offset = 1A0h) [reset = 0h]

I3C_GPIR_WORD0 is shown in [Figure 4-82](#) and described in [Table 4-168](#).

Return to the [Summary Table](#).

User Defined GPI Word 0: four 8-bits GPI Registers

Table 4-167. I3C_GPIR_WORD0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 81A0h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 81A0h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 81A0h

Figure 4-82. I3C_GPIR_WORD0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD2								RSVD1								RSVD0								GPI0							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-168. I3C_GPIR_WORD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RSVD2	R	0h	Reserved
23-16	RSVD1	R	0h	Reserved
15-8	RSVD0	R	0h	Reserved
7-0	GPI0	R	0h	User Defined GPI Register 0

4.84 I3C_GPOR_WORD0 Register (Offset = 220h) [reset = 0h]

I3C_GPOR_WORD0 is shown in [Figure 4-83](#) and described in [Table 4-170](#).

Return to the [Summary Table](#).

User Defined GPO Word 0: four 8-bits GPO Registers

Table 4-169. I3C_GPOR_WORD0 Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8220h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8220h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8220h

Figure 4-83. I3C_GPOR_WORD0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD2								RSVD1								RSVD0								GPO0							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-170. I3C_GPOR_WORD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RSVD2	R	0h	Reserved
23-16	RSVD1	R	0h	Reserved
15-8	RSVD0	R	0h	Reserved
7-0	GPO0	R	0h	User Defined GPO Register 0

4.85 I3C_ASF_INT_STATUS Register (Offset = 300h) [reset = 0h]

I3C_ASF_INT_STATUS is shown in [Figure 4-84](#) and described in [Table 4-172](#).

Return to the [Summary Table](#).

ASF Interrupt Status Register. This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_fatal or asf_nonfatal signal will be asserted. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 4-171. I3C_ASF_INT_STATUS Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8300h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8300h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8300h

Figure 4-84. I3C_ASF_INT_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR	ASF_PROTOCOL_ERR	ASF_TRANSACTION_TIMEOUT_ERR	ASF_CSR_ERR	ASF_DAP_ERR	ASF_SRAM_UNCORRECTABLE_ERR	ASF_SRAM_CORRECTABLE_ERR
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-172. I3C_ASF_INT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved, read as 0, ignored on write.
6	ASF_INTEGRITY_ERR	R/W1C	0h	Integrity error interrupt
5	ASF_PROTOCOL_ERR	R/W1C	0h	Protocol error interrupt
4	ASF_TRANSACTION_TIMEOUT_ERR	R/W1C	0h	Transaction timeouts error interrupt
3	ASF_CSR_ERR	R/W1C	0h	Configuration and status registers error interrupt
2	ASF_DAP_ERR	R/W1C	0h	Data and address paths parity error interrupt
1	ASF_SRAM_UNCORRECTABLE_ERR	R/W1C	0h	SRAM uncorrectable error interrupt
0	ASF_SRAM_CORRECTABLE_ERR	R/W1C	0h	SRAM correctable error interrupt

4.86 I3C_ASF_INT_RAW_STATUS Register (Offset = 304h) [reset = 0h]

I3C_ASF_INT_RAW_STATUS is shown in [Figure 4-85](#) and described in [Table 4-174](#).

Return to the [Summary Table](#).

ASF Interrupt Raw Status Register. A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 4-173. I3C_ASF_INT_RAW_STATUS Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8304h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8304h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8304h

Figure 4-85. I3C_ASF_INT_RAW_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR	ASF_PROTOCOL_ERR	ASF_TRANSACTION_TIMEOUT_ERR	ASF_CSR_ERR	ASF_DAP_ERR	ASF_SRAM_UNCORRECTABLE_ERR	ASF_SRAM_CORRECTABLE_ERR
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-174. I3C_ASF_INT_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved, read as 0, ignored on write.
6	ASF_INTEGRITY_ERR	R/W1C	0h	Integrity error interrupt
5	ASF_PROTOCOL_ERR	R/W1C	0h	Protocol error interrupt
4	ASF_TRANSACTION_TIMEOUT_ERR	R/W1C	0h	Transaction timeouts error interrupt
3	ASF_CSR_ERR	R/W1C	0h	Configuration and status registers error interrupt
2	ASF_DAP_ERR	R/W1C	0h	Data and address paths parity error interrupt
1	ASF_SRAM_UNCORRECTABLE_ERR	R/W1C	0h	SRAM uncorrectable error interrupt
0	ASF_SRAM_CORRECTABLE_ERR	R/W1C	0h	SRAM correctable error interrupt

4.87 I3C_ASF_INT_MASK Register (Offset = 308h) [reset = 7Fh]

I3C_ASF_INT_MASK is shown in [Figure 4-86](#) and described in [Table 4-176](#).

Return to the [Summary Table](#).

The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt status register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt.

Table 4-175. I3C_ASF_INT_MASK Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8308h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8308h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8308h

Figure 4-86. I3C_ASF_INT_MASK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR_MASK	ASF_PROTOCOL_ERR_MASK	ASF_TRANSACTION_ERR_MASK	ASF_CSR_ERR_MASK	ASF_DAP_ERR_MASK	ASF_SRAM_UNCORRECTABLE_ERR_MASK	ASF_SRAM_CORRECTABLE_ERR_MASK
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-176. I3C_ASF_INT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved, read as 0, ignored on write.
6	ASF_INTEGRITY_ERR_MASK	R/W	1h	Mask bit for integrity error interrupt
5	ASF_PROTOCOL_ERR_MASK	R/W	1h	Mask bit for protocol error interrupt.
4	ASF_TRANSACTION_ERR_MASK	R/W	1h	Mask bit for transaction timeouts error interrupt.
3	ASF_CSR_ERR_MASK	R/W	1h	Mask bit for configuration and status registers error interrupt.
2	ASF_DAP_ERR_MASK	R/W	1h	Mask bit for data and address paths parity error interrupt.
1	ASF_SRAM_UNCORRECTABLE_ERR_MASK	R/W	1h	Mask bit for SRAM uncorrectable error interrupt.
0	ASF_SRAM_CORRECTABLE_ERR_MASK	R/W	1h	Mask bit for SRAM correctable error interrupt.

4.88 I3C_ASF_INT_TEST Register (Offset = 30Ch) [reset = 0h]

I3C_ASF_INT_TEST is shown in [Figure 4-87](#) and described in [Table 4-178](#).

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The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) status registers according to mask and will generate interrupt accordingly.

Table 4-177. I3C_ASF_INT_TEST Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 830Ch
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 830Ch
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 830Ch

Figure 4-87. I3C_ASF_INT_TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR_TEST	ASF_PROTOCOL_ERR_TEST	ASF_TRANSACTION_ERR_TEST	ASF_CSR_ERR_TEST	ASF_DAP_ERR_TEST	ASF_SRAM_UNCORRECTABLE_ERR_TEST	ASF_SRAM_CORRECTABLE_ERR_TEST
R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-178. I3C_ASF_INT_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved, read as 0, ignored on write.
6	ASF_INTEGRITY_ERR_TEST	W	0h	Test bit for integrity error interrupt
5	ASF_PROTOCOL_ERR_TEST	W	0h	Test bit for protocol error interrupt.
4	ASF_TRANSACTION_ERR_TEST	W	0h	Test bit for transaction timeouts error interrupt.
3	ASF_CSR_ERR_TEST	W	0h	Test bit for configuration and status registers error interrupt.
2	ASF_DAP_ERR_TEST	W	0h	Test bit for data and address paths parity error interrupt.
1	ASF_SRAM_UNCORRECTABLE_ERR_TEST	W	0h	Test bit for SRAM uncorrectable error interrupt.
0	ASF_SRAM_CORRECTABLE_ERR_TEST	W	0h	Test bit for SRAM correctable error interrupt.

4.89 I3C_ASF_FATAL_NONFATAL_SELECT Register (Offset = 310h) [reset = 7Fh]

I3C_ASF_FATAL_NONFATAL_SELECT is shown in [Figure 4-88](#) and described in [Table 4-180](#).

Return to the [Summary Table](#).

The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered.

Table 4-179. I3C_ASF_FATAL_NONFATAL_SELECT Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8310h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8310h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8310h

Figure 4-88. I3C_ASF_FATAL_NONFATAL_SELECT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR	ASF_PROTOCOL_ERR	ASF_TRANSACTION_TIMEOUT_ERR	ASF_CSR_ERR	ASF_DAP_ERR	ASF_SRAM_UNCORRECTABLE_ERR	ASF_SRAM_CORRECTABLE_ERR
R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-180. I3C_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved, read as 0, ignored on write.
6	ASF_INTEGRITY_ERR	R/W	1h	Enable integrity error interrupt as fatal
5	ASF_PROTOCOL_ERR	R/W	1h	Enable protocol error interrupt as fatal.
4	ASF_TRANSACTION_TIMEOUT_ERR	R/W	1h	Enable transaction timeouts error interrupt as fatal.
3	ASF_CSR_ERR	R/W	1h	Enable configuration and status registers error interrupt as fatal.
2	ASF_DAP_ERR	R/W	1h	Enable data and address paths parity error interrupt as fatal.
1	ASF_SRAM_UNCORRECTABLE_ERR	R/W	1h	Enable SRAM uncorrectable error interrupt as fatal.
0	ASF_SRAM_CORRECTABLE_ERR	R/W	1h	Enable SRAM correctable error interrupt as fatal.

4.90 I3C_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 320h) [reset = 0h]

I3C_ASF_SRAM_CORR_FAULT_STATUS is shown in [Figure 4-89](#) and described in [Table 4-182](#).

Return to the [Summary Table](#).

Status register for SRAM correctable fault. These fields are updated whenever asf_sram_corr_fault input is active.

Table 4-181.
I3C_ASF_SRAM_CORR_FAULT_STATUS Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8320h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8320h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8320h

Figure 4-89. I3C_ASF_SRAM_CORR_FAULT_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ASF_SRAM_CORR_FAULT_INST								ASF_SRAM_CORR_FAULT_ADDR							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASF_SRAM_CORR_FAULT_ADDR															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-182. I3C_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ASF_SRAM_CORR_FAULT_INST	R	0h	Last SRAM instance that generated fault.
23-0	ASF_SRAM_CORR_FAULT_ADDR	R	0h	Last SRAM address that generated fault.

4.91 I3C_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 324h) [reset = 0h]

I3C_ASF_SRAM_UNCORR_FAULT_STATUS is shown in [Figure 4-90](#) and described in [Table 4-184](#).

Return to the [Summary Table](#).

Status register for SRAM uncorrectable fault. These fields are updated whenever asf_sram_uncorr_fault input is active.

Table 4-183.
I3C_ASF_SRAM_UNCORR_FAULT_STATUS
Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B8 8324h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	40B9 8324h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPi_I3C_MST	020A 8324h

Figure 4-90. I3C_ASF_SRAM_UNCORR_FAULT_STATUS Register

31	30	29	28	27	26	25	24
ASF_SRAM_UNCORR_FAULT_INST							
R-0h							
23	22	21	20	19	18	17	16
ASF_SRAM_UNCORR_FAULT_ADDR							
R-0h							
15	14	13	12	11	10	9	8
ASF_SRAM_UNCORR_FAULT_ADDR							
R-0h							
7	6	5	4	3	2	1	0
ASF_SRAM_UNCORR_FAULT_ADDR							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-184. I3C_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ASF_SRAM_UNCORR_FAULT_INST	R	0h	Last SRAM instance that generated fault.
23-0	ASF_SRAM_UNCORR_FAULT_ADDR	R	0h	Last SRAM address that generated fault.

4.92 I3C_ASF_SRAM_FAULT_STATS Register (Offset = 328h) [reset = 0h]

I3C_ASF_SRAM_FAULT_STATS is shown in [Figure 4-91](#) and described in [Table 4-186](#).

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Statistics register for SRAM faults. Note that this register clears when software writes to any field.

Table 4-185. I3C_ASF_SRAM_FAULT_STATS Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8328h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8328h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8328h

Figure 4-91. I3C_ASF_SRAM_FAULT_STATS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ASF_SRAM_FAULT_UNCORR_STATS															
R/W1C-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASF_SRAM_FAULT_CORR_STATS															
R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-186. I3C_ASF_SRAM_FAULT_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ASF_SRAM_FAULT_UNCORR_STATS	R/W1C	0h	Count of number of uncorrectable errors if implemented. Count value will saturate at 0xffff.
15-0	ASF_SRAM_FAULT_CORR_STATS	R/W1C	0h	Count of number of correctable errors if implemented. Count value will saturate at 0xffff.

4.93 I3C_ASF_TRANS_TO_CTRL Register (Offset = 330h) [reset = 0h]

I3C_ASF_TRANS_TO_CTRL is shown in [Figure 4-92](#) and described in [Table 4-188](#).

Return to the [Summary Table](#).

Control register to configure the ASF transaction timeout monitors.

Table 4-187. I3C_ASF_TRANS_TO_CTRL Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B8 8330h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	40B9 8330h
I3C0_VBP2APB_WRAP_CORE_VBP_MIPI_I3C_MST	020A 8330h

Figure 4-92. I3C_ASF_TRANS_TO_CTRL Register

31	30	29	28	27	26	25	24
ASF_TRANS_TO_EN	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ASF_TRANS_TO_CTRL							
R/W-0h							
7	6	5	4	3	2	1	0
ASF_TRANS_TO_CTRL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-188. I3C_ASF_TRANS_TO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ASF_TRANS_TO_EN	R/W	0h	Enable transaction timeout monitoring.
30-16	RESERVED	R	0h	Reserved, read as 0, ignored on write.
15-0	ASF_TRANS_TO_CTRL	R/W	0h	Timer value to use for transaction timeout monitor.

4.94 I3C_ASF_TRANS_TO_FAULT_MASK Register (Offset = 334h) [reset = Fh]

I3C_ASF_TRANS_TO_FAULT_MASK is shown in [Figure 4-93](#) and described in [Table 4-190](#).

Return to the [Summary Table](#).

Control register to mask out ASF transaction timeout faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterizable and the bit definitions are implementation specific.

Table 4-189. I3C_ASF_TRANS_TO_FAULT_MASK Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8334h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8334h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8334h

Figure 4-93. I3C_ASF_TRANS_TO_FAULT_MASK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ASF_TRANS_TO_FAULT_3_MASK	ASF_TRANS_TO_FAULT_2_MASK	ASF_TRANS_TO_FAULT_1_MASK	ASF_TRANS_TO_FAULT_0_MASK
R-0h				R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-190. I3C_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved, read as 0, ignored on write.
3	ASF_TRANS_TO_FAULT_3_MASK	R/W	1h	Mask bit for apb transaction timeout fault.
2	ASF_TRANS_TO_FAULT_2_MASK	R/W	1h	Mask bit for I3C transaction SCL low timeout fault.
1	ASF_TRANS_TO_FAULT_1_MASK	R/W	1h	Mask bit for I3C transaction SCL high timeout fault.
0	ASF_TRANS_TO_FAULT_0_MASK	R/W	1h	Mask bit for I3C transaction first SCL high timeout fault.

4.95 I3C_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 338h) [reset = 0h]

I3C_ASF_TRANS_TO_FAULT_STATUS is shown in [Figure 4-94](#) and described in [Table 4-192](#).

Return to the [Summary Table](#).

Status register for transaction timeouts fault. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit.

Table 4-191. I3C_ASF_TRANS_TO_FAULT_STATUS Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8338h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8338h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8338h

Figure 4-94. I3C_ASF_TRANS_TO_FAULT_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ASF_TRANS_TO_FAULT_3_STATUS	ASF_TRANS_TO_FAULT_2_STATUS	ASF_TRANS_TO_FAULT_1_STATUS	ASF_TRANS_TO_FAULT_0_STATUS
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-192. I3C_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved, read as 0, ignored on write.
3	ASF_TRANS_TO_FAULT_3_STATUS	R/W1C	0h	Status bits for apb transaction timeout fault.
2	ASF_TRANS_TO_FAULT_2_STATUS	R/W1C	0h	Status bits for I3C transaction SCL low timeout fault.
1	ASF_TRANS_TO_FAULT_1_STATUS	R/W1C	0h	Status bits for I3C transaction SCL high timeout fault.
0	ASF_TRANS_TO_FAULT_0_STATUS	R/W1C	0h	Status bits for I3C transaction first SCL high timeout fault.

4.96 I3C_ASF_PROTOCOL_FAULT_MASK Register (Offset = 340h) [reset = 1FFFh]

I3C_ASF_PROTOCOL_FAULT_MASK is shown in [Figure 4-95](#) and described in [Table 4-194](#).

Return to the [Summary Table](#).

Control register to mask out ASF Protocol faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

Table 4-193. I3C_ASF_PROTOCOL_FAULT_MASK Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8340h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8340h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8340h

Figure 4-95. I3C_ASF_PROTOCOL_FAULT_MASK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			ASF_PROTOCOL_FAULT_SLV_SDR_RD_ABORT_MASK	ASF_PROTOCOL_FAULT_SLV_DDR_FAIL_MASK	ASF_PROTOCOL_FAULT_S5_MASK	ASF_PROTOCOL_FAULT_S4_MASK	ASF_PROTOCOL_FAULT_S3_MASK
R-0h			R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
ASF_PROTOCOL_FAULT_S2_MASK	ASF_PROTOCOL_FAULT_S1_MASK	ASF_PROTOCOL_FAULT_S0_MASK	ASF_PROTOCOL_FAULT_MST_SDR_RD_ABORT_MASK	ASF_PROTOCOL_FAULT_MST_DDR_FAIL_MASK	ASF_PROTOCOL_FAULT_M2_MASK	ASF_PROTOCOL_FAULT_M1_MASK	ASF_PROTOCOL_FAULT_M0_MASK
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-194. I3C_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved, read as 0, ignored on write.
12	ASF_PROTOCOL_FAULT_SLV_SDR_RD_ABORT_MASK	R/W	1h	Mask bit for slv_sdr_rd_abort protocol fault source.
11	ASF_PROTOCOL_FAULT_SLV_DDR_FAIL_MASK	R/W	1h	Mask bit for slv_ddr_fail protocol fault source.
10	ASF_PROTOCOL_FAULT_S5_MASK	R/W	1h	Mask bit for s5 protocol fault source.
9	ASF_PROTOCOL_FAULT_S4_MASK	R/W	1h	Mask bit for s4 protocol fault source.
8	ASF_PROTOCOL_FAULT_S3_MASK	R/W	1h	Mask bit for s3 protocol fault source.

Table 4-194. I3C_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ASF_PROTOCOL_FAULT_S2_MASK	R/W	1h	Mask bit for s2 protocol fault source.
6	ASF_PROTOCOL_FAULT_S1_MASK	R/W	1h	Mask bit for s1 protocol fault source.
5	ASF_PROTOCOL_FAULT_S0_MASK	R/W	1h	Mask bit for s0 protocol fault source.
4	ASF_PROTOCOL_FAULT_MST_SDR_RD_ABORT_MASK	R/W	1h	Mask bit for mst_sdr_rd_abort protocol fault source.
3	ASF_PROTOCOL_FAULT_MST_DDR_FAIL_MASK	R/W	1h	Mask bit for mst_ddr_fail protocol fault source.
2	ASF_PROTOCOL_FAULT_M2_MASK	R/W	1h	Mask bit for m2 protocol fault source.
1	ASF_PROTOCOL_FAULT_M1_MASK	R/W	1h	Mask bit for m1 protocol fault source.
0	ASF_PROTOCOL_FAULT_M0_MASK	R/W	1h	Mask bit for m0 protocol fault source.

4.97 I3C_ASF_PROTOCOL_FAULT_STATUS Register (Offset = 344h) [reset = 0h]

I3C_ASF_PROTOCOL_FAULT_STATUS is shown in [Figure 4-96](#) and described in [Table 4-196](#).

Return to the [Summary Table](#).

Status register for protocol faults. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit

Table 4-195. I3C_ASF_PROTOCOL_FAULT_STATUS Instances

Instance	Physical Address
MCU_I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B8 8344h
MCU_I3C1_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	40B9 8344h
I3C0_VBP2APB_WRAP_CORE_VBP_MIP1_I3C_MST	020A 8344h

Figure 4-96. I3C_ASF_PROTOCOL_FAULT_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			ASF_PROTOCOL_FAULT_SLV_SDR_RD_ABORT_STATUS	ASF_PROTOCOL_FAULT_SLV_DDR_FAIL_STATUS	ASF_PROTOCOL_FAULT_S5_STATUS	ASF_PROTOCOL_FAULT_S4_STATUS	ASF_PROTOCOL_FAULT_S3_STATUS
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
ASF_PROTOCOL_FAULT_S2_STATUS	ASF_PROTOCOL_FAULT_S1_STATUS	ASF_PROTOCOL_FAULT_S0_STATUS	ASF_PROTOCOL_FAULT_MST_SDR_RD_ABORT_STATUS	ASF_PROTOCOL_FAULT_MST_DDR_FAIL_STATUS	ASF_PROTOCOL_FAULT_M2_STATUS	ASF_PROTOCOL_FAULT_M1_STATUS	ASF_PROTOCOL_FAULT_M0_STATUS
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-196. I3C_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved, read as 0, ignored on write.
12	ASF_PROTOCOL_FAULT_SLV_SDR_RD_ABORT_STATUS	R/W1C	0h	Status bit for slv_sdr_rd_abort protocol fault.
11	ASF_PROTOCOL_FAULT_SLV_DDR_FAIL_STATUS	R/W1C	0h	Status bit for slv_ddr_fail protocol fault.
10	ASF_PROTOCOL_FAULT_S5_STATUS	R/W1C	0h	Status bit for s5 protocol fault.
9	ASF_PROTOCOL_FAULT_S4_STATUS	R/W1C	0h	Status bit for s4 protocol fault.
8	ASF_PROTOCOL_FAULT_S3_STATUS	R/W1C	0h	Status bit for s3 protocol fault.

Table 4-196. I3C_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ASF_PROTOCOL_FAULT_S2_STATUS	R/W1C	0h	Status bit for s2 protocol fault.
6	ASF_PROTOCOL_FAULT_S1_STATUS	R/W1C	0h	Status bit for s1 protocol fault.
5	ASF_PROTOCOL_FAULT_S0_STATUS	R/W1C	0h	Status bit for s0 protocol fault.
4	ASF_PROTOCOL_FAULT_MST_SDR_RD_ABORT_STATUS	R/W1C	0h	Status bit for mst_sdr_rd_abort protocol fault.
3	ASF_PROTOCOL_FAULT_MST_DDR_FAIL_STATUS	R/W1C	0h	Status bit for mst_ddr_fail protocol fault.
2	ASF_PROTOCOL_FAULT_M2_STATUS	R/W1C	0h	Status bit for m2 protocol fault.
1	ASF_PROTOCOL_FAULT_M1_STATUS	R/W1C	0h	Status bit for m1 protocol fault.
0	ASF_PROTOCOL_FAULT_M0_STATUS	R/W1C	0h	Status bit for m0 protocol fault.

4.98 I3C_MMR Registers

Table 4-198 lists the I3C_MMR registers. All register locations not listed in Table 4-198 should be considered as reserved locations and the register contents should not be modified.

The Global Control Registers region is accessed by setting the rsel signal to 0 during the access. The address map for the region is as follows:

Table 4-197. I3C_MMR Instances

Instance	Base Address
MCU_I3C0_MMR_MMVBVP	40B8 0000h
MCU_I3C1_MMR_MMVBVP	40B9 0000h
I3C0_MMR_MMVBVP	020A 0000h

Table 4-198. I3C_MMR Registers

Offset	Acronym	Register Name	MCU_I3C0_MMR_MMVBVP Physical Address
0h	I3C_PID	Revision Register	40B8 0000h

Table 4-199. I3C_MMR Registers

Offset	Acronym	Register Name	MCU_I3C1_MMR_MMVBVP Physical Address
0h	I3C_PID	Revision Register	40B9 0000h

Table 4-200. I3C_MMR Registers

Offset	Acronym	Register Name	I3C0_MMR_MMVBVP Physical Address
0h	I3C_PID	Revision Register	020A 0000h

4.99 I3C_PID Register (Offset = 0h) [reset = 68A06100h]

I3C_PID is shown in [Figure 4-97](#) and described in [Table 4-202](#).

Return to the [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 4-201. I3C_PID Instances

Instance	Physical Address
MCU_I3C0_MMR_MMVBVP	40B8 0000h
MCU_I3C1_MMR_MMVBVP	40B9 0000h
I3C0_MMR_MMVBVP	020A 0000h

Figure 4-97. I3C_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-8A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM			MINOR				
R-Ch					R-1h			R-0h			R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 4-202. I3C_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	I3C_PID register scheme
29-28	BU	R	2h	Business Unit: 10 = Processors
27-16	MODULE_ID	R	8A0h	Module ID
15-11	RTL	R	Ch	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

4.100 I3C_PCLK_ECC_AGGR Registers

Table 4-204 lists the I3C_PCLK_ECC_AGGR registers. All register locations not listed in Table 4-204 should be considered as reserved locations and the register contents should not be modified.

Table 4-203. I3C_PCLK_ECC_AGGR Instances

Instance	Base Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0000h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2000h
I3C0_P_ECC_AGGR_CFG	02A7 4000h

Table 4-204. I3C_PCLK_ECC_AGGR Registers

Offset	Acronym	Register Name	MCU_I3C0_P_ECC_AGGR_CFG Physical Address
0h	I3C_P_REV	Aggregator Revision Register	4072 0000h
8h	I3C_P_VECTOR	ECC Vector Register	4072 0008h
Ch	I3C_P_STAT	Misc Status	4072 000Ch
10h + formula	I3C_P_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4072 0010h + formula
3Ch	I3C_P_SEC_EOI_REG	EOI Register	4072 003Ch
40h	I3C_P_SEC_STATUS_REG0	Interrupt Status Register 0	4072 0040h
80h	I3C_P_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4072 0080h
C0h	I3C_P_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4072 00C0h
13Ch	I3C_P_DED_EOI_REG	EOI Register	4072 013Ch
140h	I3C_P_DED_STATUS_REG0	Interrupt Status Register 0	4072 0140h
180h	I3C_P_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4072 0180h
1C0h	I3C_P_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4072 01C0h
200h	I3C_P_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4072 0200h
204h	I3C_P_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4072 0204h
208h	I3C_P_AGGR_STATUS_SET	AGGR interrupt status set Register	4072 0208h
20Ch	I3C_P_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4072 020Ch

Table 4-205. I3C_PCLK_ECC_AGGR Registers

Offset	Acronym	Register Name	MCU_I3C1_P_ECC_AGGR_CFG Physical Address
0h	I3C_P_REV	Aggregator Revision Register	4072 2000h
8h	I3C_P_VECTOR	ECC Vector Register	4072 2008h
Ch	I3C_P_STAT	Misc Status	4072 200Ch
10h + formula	I3C_P_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4072 2010h + formula
3Ch	I3C_P_SEC_EOI_REG	EOI Register	4072 203Ch
40h	I3C_P_SEC_STATUS_REG0	Interrupt Status Register 0	4072 2040h
80h	I3C_P_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4072 2080h
C0h	I3C_P_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4072 20C0h
13Ch	I3C_P_DED_EOI_REG	EOI Register	4072 213Ch
140h	I3C_P_DED_STATUS_REG0	Interrupt Status Register 0	4072 2140h
180h	I3C_P_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4072 2180h
1C0h	I3C_P_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4072 21C0h
200h	I3C_P_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4072 2200h
204h	I3C_P_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4072 2204h
208h	I3C_P_AGGR_STATUS_SET	AGGR interrupt status set Register	4072 2208h
20Ch	I3C_P_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4072 220Ch

Table 4-206. I3C_PCLK_ECC_AGGR Registers

Offset	Acronym	Register Name	I3C0_P_ECC_AGGR_CFG Physical Address
0h	I3C_P_REV	Aggregator Revision Register	02A7 4000h
8h	I3C_P_VECTOR	ECC Vector Register	02A7 4008h
Ch	I3C_P_STAT	Misc Status	02A7 400Ch
10h + formula	I3C_P_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	02A7 4010h + formula
3Ch	I3C_P_SEC_EOI_REG	EOI Register	02A7 403Ch
40h	I3C_P_SEC_STATUS_REG0	Interrupt Status Register 0	02A7 4040h
80h	I3C_P_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A7 4080h
C0h	I3C_P_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A7 40C0h
13Ch	I3C_P_DED_EOI_REG	EOI Register	02A7 413Ch
140h	I3C_P_DED_STATUS_REG0	Interrupt Status Register 0	02A7 4140h
180h	I3C_P_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A7 4180h
1C0h	I3C_P_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A7 41C0h
200h	I3C_P_AGGR_ENABLE_SET	AGGR interrupt enable set Register	02A7 4200h
204h	I3C_P_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	02A7 4204h
208h	I3C_P_AGGR_STATUS_SET	AGGR interrupt status set Register	02A7 4208h
20Ch	I3C_P_AGGR_STATUS_CLR	AGGR interrupt status clear Register	02A7 420Ch

4.101 I3C_P_REV Register (Offset = 0h) [reset = 66A0EA00h]

I3C_P_REV is shown in [Figure 4-98](#) and described in [Table 4-208](#).

Return to the [Summary Table](#).

Revision parameters

Table 4-207. I3C_P_REV Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0000h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2000h
I3C0_P_ECC_AGGR_CFG	02A7 4000h

Figure 4-98. I3C_P_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 4-208. I3C_P_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

4.102 I3C_P_VECTOR Register (Offset = 8h) [reset = X]

I3C_P_VECTOR is shown in [Figure 4-99](#) and described in [Table 4-210](#).

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ECC Vector Register

Table 4-209. I3C_P_VECTOR Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0008h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2008h
I3C0_P_ECC_AGGR_CFG	02A7 4008h

Figure 4-99. I3C_P_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-210. I3C_P_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

4.103 I3C_P_STAT Register (Offset = Ch) [reset = X]

I3C_P_STAT is shown in [Figure 4-100](#) and described in [Table 4-212](#).

Return to the [Summary Table](#).

Misc Status

Table 4-211. I3C_P_STAT Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 000Ch
MCU_I3C1_P_ECC_AGGR_CFG	4072 200Ch
I3C0_P_ECC_AGGR_CFG	02A7 400Ch

Figure 4-100. I3C_P_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																					NUM_RAMs																
R-X																					R-1h																

LEGEND: R = Read Only; -n = value after reset

Table 4-212. I3C_P_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	1h	Indicates the number of RAMs serviced by the ECC aggregator

4.104 I3C_P_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

I3C_P_RESERVED_SVBUS_y is shown in [Figure 4-101](#) and described in [Table 4-214](#).

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Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

Table 4-213. I3C_P_RESERVED_SVBUS_y Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0010h + formula
MCU_I3C1_P_ECC_AGGR_CFG	4072 2010h + formula
I3C0_P_ECC_AGGR_CFG	02A7 4010h + formula

Figure 4-101. I3C_P_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-214. I3C_P_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

4.105 I3C_P_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

I3C_P_SEC_EOI_REG is shown in [Figure 4-102](#) and described in [Table 4-216](#).

Return to the [Summary Table](#).

EOI Register

Table 4-215. I3C_P_SEC_EOI_REG Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 003Ch
MCU_I3C1_P_ECC_AGGR_CFG	4072 203Ch
I3C0_P_ECC_AGGR_CFG	02A7 403Ch

Figure 4-102. I3C_P_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-216. I3C_P_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.106 I3C_P_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

I3C_P_SEC_STATUS_REG0 is shown in [Figure 4-103](#) and described in [Table 4-218](#).

Return to the [Summary Table](#).

Interrupt Status Register 0

Table 4-217. I3C_P_SEC_STATUS_REG0 Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0040h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2040h
I3C0_P_ECC_AGGR_CFG	02A7 4040h

Figure 4-103. I3C_P_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EDC_CTRL_PEND
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-218. I3C_P_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EDC_CTRL_PEND	R/W1S	0h	Interrupt Pending Status for edc_ctrl_pend

4.107 I3C_P_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

I3C_P_SEC_ENABLE_SET_REG0 is shown in [Figure 4-104](#) and described in [Table 4-220](#).

Return to the [Summary Table](#).

Interrupt Enable Set Register 0

Table 4-219. I3C_P_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0080h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2080h
I3C0_P_ECC_AGGR_CFG	02A7 4080h

Figure 4-104. I3C_P_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EDC_CTRL_ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-220. I3C_P_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EDC_CTRL_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for edc_ctrl_pend

4.108 I3C_P_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

I3C_P_SEC_ENABLE_CLR_REG0 is shown in [Figure 4-105](#) and described in [Table 4-222](#).

Return to the [Summary Table](#).

Interrupt Enable Clear Register 0

Table 4-221. I3C_P_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 00C0h
MCU_I3C1_P_ECC_AGGR_CFG	4072 20C0h
I3C0_P_ECC_AGGR_CFG	02A7 40C0h

Figure 4-105. I3C_P_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EDC_CTRL_ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-222. I3C_P_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EDC_CTRL_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for edc_ctrl_pend

4.109 I3C_P_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

I3C_P_DED_EOI_REG is shown in [Figure 4-106](#) and described in [Table 4-224](#).

Return to the [Summary Table](#).

EOI Register

Table 4-223. I3C_P_DED_EOI_REG Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 013Ch
MCU_I3C1_P_ECC_AGGR_CFG	4072 213Ch
I3C0_P_ECC_AGGR_CFG	02A7 413Ch

Figure 4-106. I3C_P_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-224. I3C_P_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.110 I3C_P_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

I3C_P_DED_STATUS_REG0 is shown in [Figure 4-107](#) and described in [Table 4-226](#).

Return to the [Summary Table](#).

Interrupt Status Register 0

Table 4-225. I3C_P_DED_STATUS_REG0 Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0140h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2140h
I3C0_P_ECC_AGGR_CFG	02A7 4140h

Figure 4-107. I3C_P_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EDC_CTRL_PEND
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-226. I3C_P_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EDC_CTRL_PEND	R/W1S	0h	Interrupt Pending Status for edc_ctrl_pend

4.111 I3C_P_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

I3C_P_DED_ENABLE_SET_REG0 is shown in [Figure 4-108](#) and described in [Table 4-228](#).

Return to the [Summary Table](#).

Interrupt Enable Set Register 0

Table 4-227. I3C_P_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0180h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2180h
I3C0_P_ECC_AGGR_CFG	02A7 4180h

Figure 4-108. I3C_P_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EDC_CTRL_ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-228. I3C_P_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EDC_CTRL_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for edc_ctrl_pend

4.112 I3C_P_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

I3C_P_DED_ENABLE_CLR_REG0 is shown in [Figure 4-109](#) and described in [Table 4-230](#).

Return to the [Summary Table](#).

Interrupt Enable Clear Register 0

Table 4-229. I3C_P_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 01C0h
MCU_I3C1_P_ECC_AGGR_CFG	4072 21C0h
I3C0_P_ECC_AGGR_CFG	02A7 41C0h

Figure 4-109. I3C_P_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EDC_CTRL_EN ABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-230. I3C_P_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EDC_CTRL_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for edc_ctrl_pend

4.113 I3C_P_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

I3C_P_AGGR_ENABLE_SET is shown in [Figure 4-110](#) and described in [Table 4-232](#).

Return to the [Summary Table](#).

AGGR interrupt enable set Register

Table 4-231. I3C_P_AGGR_ENABLE_SET Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0200h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2200h
I3C0_P_ECC_AGGR_CFG	02A7 4200h

Figure 4-110. I3C_P_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-232. I3C_P_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

4.114 I3C_P_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

I3C_P_AGGR_ENABLE_CLR is shown in [Figure 4-111](#) and described in [Table 4-234](#).

Return to the [Summary Table](#).

AGGR interrupt enable clear Register

Table 4-233. I3C_P_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0204h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2204h
I3C0_P_ECC_AGGR_CFG	02A7 4204h

Figure 4-111. I3C_P_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-234. I3C_P_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

4.115 I3C_P_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

I3C_P_AGGR_STATUS_SET is shown in [Figure 4-112](#) and described in [Table 4-236](#).

Return to the [Summary Table](#).

AGGR interrupt status set Register

Table 4-235. I3C_P_AGGR_STATUS_SET Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 0208h
MCU_I3C1_P_ECC_AGGR_CFG	4072 2208h
I3C0_P_ECC_AGGR_CFG	02A7 4208h

Figure 4-112. I3C_P_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 4-236. I3C_P_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

4.116 I3C_P_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

I3C_P_AGGR_STATUS_CLR is shown in [Figure 4-113](#) and described in [Table 4-238](#).

Return to the [Summary Table](#).

AGGR interrupt status clear Register

Table 4-237. I3C_P_AGGR_STATUS_CLR Instances

Instance	Physical Address
MCU_I3C0_P_ECC_AGGR_CFG	4072 020Ch
MCU_I3C1_P_ECC_AGGR_CFG	4072 220Ch
I3C0_P_ECC_AGGR_CFG	02A7 420Ch

Figure 4-113. I3C_P_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 4-238. I3C_P_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

4.117 I3C_SCLK_ECC_AGGR Registers

Table 4-240 lists the I3C_SCLK_ECC_AGGR registers. All register locations not listed in Table 4-240 should be considered as reserved locations and the register contents should not be modified.

Table 4-239. I3C_SCLK_ECC_AGGR Instances

Instance	Base Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1000h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3000h
I3C0_S_ECC_AGGR_CFG	02A7 5000h

Table 4-240. I3C_SCLK_ECC_AGGR Registers

Offset	Acronym	Register Name	MCU_I3C0_S_ECC_AGGR_CFG Physical Address
0h	I3C_S_REV	Aggregator Revision Register	4072 1000h
8h	I3C_S_VECTOR	ECC Vector Register	4072 1008h
Ch	I3C_S_STAT	Misc Status	4072 100Ch
10h + formula	I3C_S_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4072 1010h + formula
3Ch	I3C_S_SEC_EOI_REG	EOI Register	4072 103Ch
40h	I3C_S_SEC_STATUS_REG0	Interrupt Status Register 0	4072 1040h
80h	I3C_S_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4072 1080h
C0h	I3C_S_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4072 10C0h
13Ch	I3C_S_DED_EOI_REG	EOI Register	4072 113Ch
140h	I3C_S_DED_STATUS_REG0	Interrupt Status Register 0	4072 1140h
180h	I3C_S_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4072 1180h
1C0h	I3C_S_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4072 11C0h
200h	I3C_S_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4072 1200h
204h	I3C_S_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4072 1204h
208h	I3C_S_AGGR_STATUS_SET	AGGR interrupt status set Register	4072 1208h
20Ch	I3C_S_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4072 120Ch

Table 4-241. I3C_SCLK_ECC_AGGR Registers

Offset	Acronym	Register Name	MCU_I3C1_S_ECC_AGGR_CFG Physical Address
0h	I3C_S_REV	Aggregator Revision Register	4072 3000h
8h	I3C_S_VECTOR	ECC Vector Register	4072 3008h
Ch	I3C_S_STAT	Misc Status	4072 300Ch
10h + formula	I3C_S_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4072 3010h + formula
3Ch	I3C_S_SEC_EOI_REG	EOI Register	4072 303Ch
40h	I3C_S_SEC_STATUS_REG0	Interrupt Status Register 0	4072 3040h
80h	I3C_S_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4072 3080h
C0h	I3C_S_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4072 30C0h
13Ch	I3C_S_DED_EOI_REG	EOI Register	4072 313Ch
140h	I3C_S_DED_STATUS_REG0	Interrupt Status Register 0	4072 3140h
180h	I3C_S_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4072 3180h
1C0h	I3C_S_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4072 31C0h
200h	I3C_S_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4072 3200h
204h	I3C_S_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4072 3204h
208h	I3C_S_AGGR_STATUS_SET	AGGR interrupt status set Register	4072 3208h
20Ch	I3C_S_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4072 320Ch

Table 4-242. I3C_SCLK_ECC_AGGR Registers

Offset	Acronym	Register Name	I3C0_S_ECC_AGGR_CFG Physical Address
0h	I3C_S_REV	Aggregator Revision Register	02A7 5000h
8h	I3C_S_VECTOR	ECC Vector Register	02A7 5008h
Ch	I3C_S_STAT	Misc Status	02A7 500Ch
10h + formula	I3C_S_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	02A7 5010h + formula
3Ch	I3C_S_SEC_EOI_REG	EOI Register	02A7 503Ch
40h	I3C_S_SEC_STATUS_REG0	Interrupt Status Register 0	02A7 5040h
80h	I3C_S_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A7 5080h
C0h	I3C_S_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A7 50C0h
13Ch	I3C_S_DED_EOI_REG	EOI Register	02A7 513Ch
140h	I3C_S_DED_STATUS_REG0	Interrupt Status Register 0	02A7 5140h
180h	I3C_S_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A7 5180h
1C0h	I3C_S_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A7 51C0h
200h	I3C_S_AGGR_ENABLE_SET	AGGR interrupt enable set Register	02A7 5200h
204h	I3C_S_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	02A7 5204h
208h	I3C_S_AGGR_STATUS_SET	AGGR interrupt status set Register	02A7 5208h
20Ch	I3C_S_AGGR_STATUS_CLR	AGGR interrupt status clear Register	02A7 520Ch

4.118 I3C_S_REV Register (Offset = 0h) [reset = 66A0EA00h]

I3C_S_REV is shown in [Figure 4-114](#) and described in [Table 4-244](#).

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Revision parameters

Table 4-243. I3C_S_REV Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1000h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3000h
I3C0_S_ECC_AGGR_CFG	02A7 5000h

Figure 4-114. I3C_S_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 4-244. I3C_S_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

4.119 I3C_S_VECTOR Register (Offset = 8h) [reset = X]

I3C_S_VECTOR is shown in [Figure 4-115](#) and described in [Table 4-246](#).

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ECC Vector Register

Table 4-245. I3C_S_VECTOR Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1008h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3008h
I3C0_S_ECC_AGGR_CFG	02A7 5008h

Figure 4-115. I3C_S_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-246. I3C_S_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

4.120 I3C_S_STAT Register (Offset = Ch) [reset = X]

I3C_S_STAT is shown in [Figure 4-116](#) and described in [Table 4-248](#).

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Misc Status

Table 4-247. I3C_S_STAT Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 100Ch
MCU_I3C1_S_ECC_AGGR_CFG	4072 300Ch
I3C0_S_ECC_AGGR_CFG	02A7 500Ch

Figure 4-116. I3C_S_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																					NUM_RAMs																
R-X																					R-9h																

LEGEND: R = Read Only; -n = value after reset

Table 4-248. I3C_S_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	9h	Indicates the number of RAMs serviced by the ECC aggregator

4.121 I3C_S_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

I3C_S_RESERVED_SVBUS_y is shown in [Figure 4-117](#) and described in [Table 4-250](#).

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Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

Table 4-249. I3C_S_RESERVED_SVBUS_y Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1010h + formula
MCU_I3C1_S_ECC_AGGR_CFG	4072 3010h + formula
I3C0_S_ECC_AGGR_CFG	02A7 5010h + formula

Figure 4-117. I3C_S_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-250. I3C_S_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

4.122 I3C_S_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

I3C_S_SEC_EOI_REG is shown in [Figure 4-118](#) and described in [Table 4-252](#).

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EOI Register

Table 4-251. I3C_S_SEC_EOI_REG Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 103Ch
MCU_I3C1_S_ECC_AGGR_CFG	4072 303Ch
I3C0_S_ECC_AGGR_CFG	02A7 503Ch

Figure 4-118. I3C_S_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-252. I3C_S_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.123 I3C_S_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

I3C_S_SEC_STATUS_REG0 is shown in [Figure 4-119](#) and described in [Table 4-254](#).

Return to the [Summary Table](#).

Interrupt Status Register 0

Table 4-253. I3C_S_SEC_STATUS_REG0 Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1040h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3040h
I3C0_S_ECC_AGGR_CFG	02A7 5040h

Figure 4-119. I3C_S_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_DATA_PEND
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
CMD_WRD0_PEND	TX_DATA_PEND	CMD_WRD1_PEND	IBI_PEND	SLV_DDR_TX_PEND	CMDR_QUEUE_PEND	SLV_DDR_RX_PEND	IBIR_QUEUE_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-254. I3C_S_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_DATA_PEND	R/W1S	0h	Interrupt Pending Status for rx_data_pend
7	CMD_WRD0_PEND	R/W1S	0h	Interrupt Pending Status for cmd_wrd0_pend
6	TX_DATA_PEND	R/W1S	0h	Interrupt Pending Status for tx_data_pend
5	CMD_WRD1_PEND	R/W1S	0h	Interrupt Pending Status for cmd_wrd1_pend
4	IBI_PEND	R/W1S	0h	Interrupt Pending Status for ibi_pend
3	SLV_DDR_TX_PEND	R/W1S	0h	Interrupt Pending Status for slv_ddr_tx_pend
2	CMDR_QUEUE_PEND	R/W1S	0h	Interrupt Pending Status for cmdr_queue_pend
1	SLV_DDR_RX_PEND	R/W1S	0h	Interrupt Pending Status for slv_ddr_rx_pend
0	IBIR_QUEUE_PEND	R/W1S	0h	Interrupt Pending Status for ibir_queue_pend

4.124 I3C_S_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

I3C_S_SEC_ENABLE_SET_REG0 is shown in [Figure 4-120](#) and described in [Table 4-256](#).

Return to the [Summary Table](#).

Interrupt Enable Set Register 0

Table 4-255. I3C_S_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1080h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3080h
I3C0_S_ECC_AGGR_CFG	02A7 5080h

Figure 4-120. I3C_S_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_DATA_ENABLE_SET
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
CMD_WRD0_ENABLE_SET	TX_DATA_ENABLE_SET	CMD_WRD1_ENABLE_SET	IBI_ENABLE_SET	SLV_DDR_TX_ENABLE_SET	CMDR_QUEUE_ENABLE_SET	SLV_DDR_RX_ENABLE_SET	IBIR_QUEUE_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-256. I3C_S_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_DATA_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for rx_data_pend
7	CMD_WRD0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for cmd_wrd0_pend
6	TX_DATA_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tx_data_pend
5	CMD_WRD1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for cmd_wrd1_pend
4	IBI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ibi_pend
3	SLV_DDR_TX_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for slv_ddr_tx_pend
2	CMDR_QUEUE_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for cmdr_queue_pend
1	SLV_DDR_RX_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for slv_ddr_rx_pend
0	IBIR_QUEUE_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ibir_queue_pend

4.125 I3C_S_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

I3C_S_SEC_ENABLE_CLR_REG0 is shown in [Figure 4-121](#) and described in [Table 4-258](#).

Return to the [Summary Table](#).

Interrupt Enable Clear Register 0

**Table 4-257. I3C_S_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 10C0h
MCU_I3C1_S_ECC_AGGR_CFG	4072 30C0h
I3C0_S_ECC_AGGR_CFG	02A7 50C0h

Figure 4-121. I3C_S_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_DATA_ENA BLE_CLR
R/W-X							R/W1C-0h
7	6	5	4	3	2	1	0
CMD_WRD0_E NABLE_CLR	TX_DATA_ENA BLE_CLR	CMD_WRD1_E NABLE_CLR	IBI_ENABLE_C LR	SLV_DDR_TX ENABLE_CLR	CMDR_QUEUE _ENABLE_CLR	SLV_DDR_RX ENABLE_CLR	IBIR_QUEUE ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-258. I3C_S_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_DATA_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for rx_data_pend
7	CMD_WRD0_ENABLE_C LR	R/W1C	0h	Interrupt Enable Clear Register for cmd_wrd0_pend
6	TX_DATA_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tx_data_pend
5	CMD_WRD1_ENABLE_C LR	R/W1C	0h	Interrupt Enable Clear Register for cmd_wrd1_pend
4	IBI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ibi_pend
3	SLV_DDR_TX_ENABLE_ CLR	R/W1C	0h	Interrupt Enable Clear Register for slv_ddr_tx_pend
2	CMDR_QUEUE_ENABLE _CLR	R/W1C	0h	Interrupt Enable Clear Register for cmdr_queue_pend
1	SLV_DDR_RX_ENABLE_ CLR	R/W1C	0h	Interrupt Enable Clear Register for slv_ddr_rx_pend
0	IBIR_QUEUE_ENABLE_C LR	R/W1C	0h	Interrupt Enable Clear Register for ibir_queue_pend

4.126 I3C_S_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

I3C_S_DED_EOI_REG is shown in [Figure 4-122](#) and described in [Table 4-260](#).

Return to the [Summary Table](#).

EOI Register

Table 4-259. I3C_S_DED_EOI_REG Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 113Ch
MCU_I3C1_S_ECC_AGGR_CFG	4072 313Ch
I3C0_S_ECC_AGGR_CFG	02A7 513Ch

Figure 4-122. I3C_S_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-260. I3C_S_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.127 I3C_S_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

I3C_S_DED_STATUS_REG0 is shown in [Figure 4-123](#) and described in [Table 4-262](#).

Return to the [Summary Table](#).

Interrupt Status Register 0

Table 4-261. I3C_S_DED_STATUS_REG0 Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1140h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3140h
I3C0_S_ECC_AGGR_CFG	02A7 5140h

Figure 4-123. I3C_S_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_DATA_PEND
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
CMD_WRD0_PEND	TX_DATA_PEND	CMD_WRD1_PEND	IBI_PEND	SLV_DDR_TX_PEND	CMDR_QUEUE_PEND	SLV_DDR_RX_PEND	IBIR_QUEUE_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-262. I3C_S_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_DATA_PEND	R/W1S	0h	Interrupt Pending Status for rx_data_pend
7	CMD_WRD0_PEND	R/W1S	0h	Interrupt Pending Status for cmd_wrd0_pend
6	TX_DATA_PEND	R/W1S	0h	Interrupt Pending Status for tx_data_pend
5	CMD_WRD1_PEND	R/W1S	0h	Interrupt Pending Status for cmd_wrd1_pend
4	IBI_PEND	R/W1S	0h	Interrupt Pending Status for ibi_pend
3	SLV_DDR_TX_PEND	R/W1S	0h	Interrupt Pending Status for slv_ddr_tx_pend
2	CMDR_QUEUE_PEND	R/W1S	0h	Interrupt Pending Status for cmdr_queue_pend
1	SLV_DDR_RX_PEND	R/W1S	0h	Interrupt Pending Status for slv_ddr_rx_pend
0	IBIR_QUEUE_PEND	R/W1S	0h	Interrupt Pending Status for ibir_queue_pend

4.128 I3C_S_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

I3C_S_DED_ENABLE_SET_REG0 is shown in [Figure 4-124](#) and described in [Table 4-264](#).

Return to the [Summary Table](#).

Interrupt Enable Set Register 0

Table 4-263. I3C_S_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1180h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3180h
I3C0_S_ECC_AGGR_CFG	02A7 5180h

Figure 4-124. I3C_S_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_DATA_ENABLE_SET
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
CMD_WRD0_ENABLE_SET	TX_DATA_ENABLE_SET	CMD_WRD1_ENABLE_SET	IBI_ENABLE_SET	SLV_DDR_TX_ENABLE_SET	CMDR_QUEUE_ENABLE_SET	SLV_DDR_RX_ENABLE_SET	IBIR_QUEUE_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-264. I3C_S_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_DATA_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for rx_data_pend
7	CMD_WRD0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for cmd_wrd0_pend
6	TX_DATA_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tx_data_pend
5	CMD_WRD1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for cmd_wrd1_pend
4	IBI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ibi_pend
3	SLV_DDR_TX_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for slv_ddr_tx_pend
2	CMDR_QUEUE_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for cmdr_queue_pend
1	SLV_DDR_RX_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for slv_ddr_rx_pend
0	IBIR_QUEUE_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ibir_queue_pend

4.129 I3C_S_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

I3C_S_DED_ENABLE_CLR_REG0 is shown in [Figure 4-125](#) and described in [Table 4-266](#).

Return to the [Summary Table](#).

Interrupt Enable Clear Register 0

Table 4-265. I3C_S_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 11C0h
MCU_I3C1_S_ECC_AGGR_CFG	4072 31C0h
I3C0_S_ECC_AGGR_CFG	02A7 51C0h

Figure 4-125. I3C_S_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_DATA_ENA BLE_CLR
R/W-X							R/W1C-0h
7	6	5	4	3	2	1	0
CMD_WRD0_E NABLE_CLR	TX_DATA_ENA BLE_CLR	CMD_WRD1_E NABLE_CLR	IBI_ENABLE_C LR	SLV_DDR_TX_ ENABLE_CLR	CMDR_QUEUE_ ENABLE_CLR	SLV_DDR_RX_ ENABLE_CLR	IBIR_QUEUE_ ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-266. I3C_S_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_DATA_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for rx_data_pend
7	CMD_WRD0_ENABLE_C LR	R/W1C	0h	Interrupt Enable Clear Register for cmd_wrd0_pend
6	TX_DATA_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tx_data_pend
5	CMD_WRD1_ENABLE_C LR	R/W1C	0h	Interrupt Enable Clear Register for cmd_wrd1_pend
4	IBI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ibi_pend
3	SLV_DDR_TX_ENABLE_ CLR	R/W1C	0h	Interrupt Enable Clear Register for slv_ddr_tx_pend
2	CMDR_QUEUE_ENABLE_ CLR	R/W1C	0h	Interrupt Enable Clear Register for cmdr_queue_pend
1	SLV_DDR_RX_ENABLE_ CLR	R/W1C	0h	Interrupt Enable Clear Register for slv_ddr_rx_pend
0	IBIR_QUEUE_ENABLE_C LR	R/W1C	0h	Interrupt Enable Clear Register for ibir_queue_pend

4.130 I3C_S_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

I3C_S_AGGR_ENABLE_SET is shown in [Figure 4-126](#) and described in [Table 4-268](#).

Return to the [Summary Table](#).

AGGR interrupt enable set Register

Table 4-267. I3C_S_AGGR_ENABLE_SET Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1200h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3200h
I3C0_S_ECC_AGGR_CFG	02A7 5200h

Figure 4-126. I3C_S_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-268. I3C_S_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

4.131 I3C_S_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

I3C_S_AGGR_ENABLE_CLR is shown in [Figure 4-127](#) and described in [Table 4-270](#).

Return to the [Summary Table](#).

AGGR interrupt enable clear Register

Table 4-269. I3C_S_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1204h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3204h
I3C0_S_ECC_AGGR_CFG	02A7 5204h

Figure 4-127. I3C_S_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-270. I3C_S_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

4.132 I3C_S_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

I3C_S_AGGR_STATUS_SET is shown in [Figure 4-128](#) and described in [Table 4-272](#).

Return to the [Summary Table](#).

AGGR interrupt status set Register

Table 4-271. I3C_S_AGGR_STATUS_SET Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 1208h
MCU_I3C1_S_ECC_AGGR_CFG	4072 3208h
I3C0_S_ECC_AGGR_CFG	02A7 5208h

Figure 4-128. I3C_S_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 4-272. I3C_S_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

4.133 I3C_S_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

I3C_S_AGGR_STATUS_CLR is shown in [Figure 4-129](#) and described in [Table 4-274](#).

Return to the [Summary Table](#).

AGGR interrupt status clear Register

Table 4-273. I3C_S_AGGR_STATUS_CLR Instances

Instance	Physical Address
MCU_I3C0_S_ECC_AGGR_CFG	4072 120Ch
MCU_I3C1_S_ECC_AGGR_CFG	4072 320Ch
I3C0_S_ECC_AGGR_CFG	02A7 520Ch

Figure 4-129. I3C_S_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 4-274. I3C_S_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

5 MCSPi Registers

Table 5-2 lists the memory-mapped registers for the MCSPi. All register offset addresses not listed in Table 5-2 should be considered as reserved locations and the register contents should not be modified.

Table 5-1. MCSPi Instances

Instance	Base Address
MCSPi0_CFG	0210 0000h
MCSPi1_CFG	0211 0000h
MCSPi2_CFG	0212 0000h
MCSPi3_CFG	0213 0000h
MCSPi4_CFG	0214 0000h
MCSPi5_CFG	0215 0000h
MCSPi6_CFG	0216 0000h
MCSPi7_CFG	0217 0000h
MCU_MCSPi0_CFG	4030 0000h
MCU_MCSPi1_CFG	4031 0000h
MCU_MCSPi2_CFG	4032 0000h

Table 5-2. MCSPi Registers

Offset	Acronym	Register Name	MCSPi0_CFG Physical Address	MCSPi1_CFG Physical Address	MCSPi2_CFG Physical Address
0h	MCSPi_HL_REV	IP Revision register	0210 0000h	0211 0000h	0212 0000h
4h	MCSPi_HL_HWINFO	MCSPi hardware configuration register	0210 0004h	0211 0004h	0212 0004h
10h	MCSPi_HL_SYSCONFIG	Clock management configuration register	0210 0010h	0211 0010h	0212 0010h
100h	MCSPi_REVISION	Revision number	0210 0100h	0211 0100h	0212 0100h
110h	MCSPi_SYSCONFIG	Configuration register	0210 0110h	0211 0110h	0212 0110h
114h	MCSPi_SYSSTATUS	Status information register	0210 0114h	0211 0114h	0212 0114h
118h	MCSPi_IRQSTATUS	Interrupt status register	0210 0118h	0211 0118h	0212 0118h
11Ch	MCSPi_IRQENABLE	Interrupt enable register	0210 011Ch	0211 011Ch	0212 011Ch
120h	MCSPi_WAKEUPENABLE	Wake-up enable register	0210 0120h	0211 0120h	0212 0120h
124h	MCSPi_SYST	System interconnect check in system test mode	0210 0124h	0211 0124h	0212 0124h
128h	MCSPi_MODULCTRL	MCSPi configuration register	0210 0128h	0211 0128h	0212 0128h
12Ch	MCSPi_CHCONF_0	Configuration register of channel 0	0210 012Ch	0211 012Ch	0212 012Ch
130h	MCSPi_CHSTAT_0	Status register of channel 0	0210 0130h	0211 0130h	0212 0130h
134h	MCSPi_CHCTRL_0	Enable register of channel 0	0210 0134h	0211 0134h	0212 0134h
138h	MCSPi_TX_0	TX register of channel 0	0210 0138h	0211 0138h	0212 0138h
13Ch	MCSPi_RX_0	RX register of channel 0	0210 013Ch	0211 013Ch	0212 013Ch
140h	MCSPi_CHCONF_1	Configuration register of channel 1	0210 0140h	0211 0140h	0212 0140h
144h	MCSPi_CHSTAT_1	Status register of channel 1	0210 0144h	0211 0144h	0212 0144h
148h	MCSPi_CHCTRL_1	Enable register of channel 1	0210 0148h	0211 0148h	0212 0148h
14Ch	MCSPi_TX_1	TX register of channel 1	0210 014Ch	0211 014Ch	0212 014Ch
150h	MCSPi_RX_1	RX register of channel 1	0210 0150h	0211 0150h	0212 0150h
154h	MCSPi_CHCONF_2	Configuration register of channel 2	0210 0154h	0211 0154h	0212 0154h
158h	MCSPi_CHSTAT_2	Status register of channel 2	0210 0158h	0211 0158h	0212 0158h
15Ch	MCSPi_CHCTRL_2	Enable register of channel 2	0210 015Ch	0211 015Ch	0212 015Ch
160h	MCSPi_TX_2	TX register of channel 2	0210 0160h	0211 0160h	0212 0160h
164h	MCSPi_RX_2	RX register of channel 2	0210 0164h	0211 0164h	0212 0164h
168h	MCSPi_CHCONF_3	Configuration register of channel 3	0210 0168h	0211 0168h	0212 0168h

Table 5-2. MCSPI Registers (continued)

Offset	Acronym	Register Name	MCSPI0_CFG Physical Address	MCSPI1_CFG Physical Address	MCSPI2_CFG Physical Address
16Ch	MCSPI_CHSTAT_3	Status register of channel 3	0210 016Ch	0211 016Ch	0212 016Ch
170h	MCSPI_CHCTRL_3	Enable register of channel 3	0210 0170h	0211 0170h	0212 0170h
174h	MCSPI_TX_3	TX register of channel 3	0210 0174h	0211 0174h	0212 0174h
178h	MCSPI_RX_3	RX register of channel 3	0210 0178h	0211 0178h	0212 0178h
17Ch	MCSPI_XFERLEVEL	Transfer levels when FIFO is used	0210 017Ch	0211 017Ch	0212 017Ch
180h	MCSPI_DAFTX	MCSPI words transmitted when FIFO is used	0210 0180h	0211 0180h	0212 0180h
1A0h	MCSPI_DAFRX	MCSPI words received when FIFO is used	0210 01A0h	0211 01A0h	0212 01A0h

Table 5-3. MCSPI Registers

Offset	Acronym	Register Name	MCSPI3_CFG Physical Address	MCSPI4_CFG Physical Address
0h	MCSPI_HL_REV	IP Revision register	0213 0000h	0214 0000h
4h	MCSPI_HL_HWINFO	MCSPI hardware configuration register	0213 0004h	0214 0004h
10h	MCSPI_HL_SYSCONFIG	Clock management configuration register	0213 0010h	0214 0010h
100h	MCSPI_REVISION	Revision number	0213 0100h	0214 0100h
110h	MCSPI_SYSCONFIG	Configuration register	0213 0110h	0214 0110h
114h	MCSPI_SYSSTATUS	Status information register	0213 0114h	0214 0114h
118h	MCSPI_IRQSTATUS	Interrupt status register	0213 0118h	0214 0118h
11Ch	MCSPI_IRQENABLE	Interrupt enable register	0213 011Ch	0214 011Ch
120h	MCSPI_WAKEUPENABLE	Wake-up enable register	0213 0120h	0214 0120h
124h	MCSPI_SYST	System interconnect check in system test mode	0213 0124h	0214 0124h
128h	MCSPI_MODULCTRL	MCSPI configuration register	0213 0128h	0214 0128h
12Ch	MCSPI_CHCONF_0	Configuration register of channel 0	0213 012Ch	0214 012Ch
130h	MCSPI_CHSTAT_0	Status register of channel 0	0213 0130h	0214 0130h
134h	MCSPI_CHCTRL_0	Enable register of channel 0	0213 0134h	0214 0134h
138h	MCSPI_TX_0	TX register of channel 0	0213 0138h	0214 0138h
13Ch	MCSPI_RX_0	RX register of channel 0	0213 013Ch	0214 013Ch
140h	MCSPI_CHCONF_1	Configuration register of channel 1	0213 0140h	0214 0140h
144h	MCSPI_CHSTAT_1	Status register of channel 1	0213 0144h	0214 0144h
148h	MCSPI_CHCTRL_1	Enable register of channel 1	0213 0148h	0214 0148h
14Ch	MCSPI_TX_1	TX register of channel 1	0213 014Ch	0214 014Ch
150h	MCSPI_RX_1	RX register of channel 1	0213 0150h	0214 0150h
154h	MCSPI_CHCONF_2	Configuration register of channel 2	0213 0154h	0214 0154h
158h	MCSPI_CHSTAT_2	Status register of channel 2	0213 0158h	0214 0158h
15Ch	MCSPI_CHCTRL_2	Enable register of channel 2	0213 015Ch	0214 015Ch
160h	MCSPI_TX_2	TX register of channel 2	0213 0160h	0214 0160h
164h	MCSPI_RX_2	RX register of channel 2	0213 0164h	0214 0164h
168h	MCSPI_CHCONF_3	Configuration register of channel 3	0213 0168h	0214 0168h
16Ch	MCSPI_CHSTAT_3	Status register of channel 3	0213 016Ch	0214 016Ch
170h	MCSPI_CHCTRL_3	Enable register of channel 3	0213 0170h	0214 0170h
174h	MCSPI_TX_3	TX register of channel 3	0213 0174h	0214 0174h
178h	MCSPI_RX_3	RX register of channel 3	0213 0178h	0214 0178h
17Ch	MCSPI_XFERLEVEL	Transfer levels when FIFO is used	0213 017Ch	0214 017Ch
180h	MCSPI_DAFTX	MCSPI words transmitted when FIFO is used	0213 0180h	0214 0180h

Table 5-3. MCSPI Registers (continued)

Offset	Acronym	Register Name	MCSPI3_CFG Physical Address	MCSPI4_CFG Physical Address
1A0h	MCSPI_DAFRX	MCSPI words received when FIFO is used	0213 01A0h	0214 01A0h

Table 5-4. MCSPI Registers

Offset	Acronym	Register Name	MCSPI5_CFG Physical Address	MCSPI6_CFG Physical Address	MCSPI7_CFG Physical Address
0h	MCSPI_HL_REV	IP Revision register	0215 0000h	0216 0000h	0217 0000h
4h	MCSPI_HL_HWINFO	MCSPI hardware configuration register	0215 0004h	0216 0004h	0217 0004h
10h	MCSPI_HL_SYSCONFIG	Clock management configuration register	0215 0010h	0216 0010h	0217 0010h
100h	MCSPI_REVISION	Revision number	0215 0100h	0216 0100h	0217 0100h
110h	MCSPI_SYSCONFIG	Configuration register	0215 0110h	0216 0110h	0217 0110h
114h	MCSPI_SYSSTATUS	Status information register	0215 0114h	0216 0114h	0217 0114h
118h	MCSPI_IRQSTATUS	Interrupt status register	0215 0118h	0216 0118h	0217 0118h
11Ch	MCSPI_IRQENABLE	Interrupt enable register	0215 011Ch	0216 011Ch	0217 011Ch
120h	MCSPI_WAKEUPENABLE	Wake-up enable register	0215 0120h	0216 0120h	0217 0120h
124h	MCSPI_SYST	System interconnect check in system test mode	0215 0124h	0216 0124h	0217 0124h
128h	MCSPI_MODULCTRL	MCSPI configuration register	0215 0128h	0216 0128h	0217 0128h
12Ch	MCSPI_CHCONF_0	Configuration register of channel 0	0215 012Ch	0216 012Ch	0217 012Ch
130h	MCSPI_CHSTAT_0	Status register of channel 0	0215 0130h	0216 0130h	0217 0130h
134h	MCSPI_CHCTRL_0	Enable register of channel 0	0215 0134h	0216 0134h	0217 0134h
138h	MCSPI_TX_0	TX register of channel 0	0215 0138h	0216 0138h	0217 0138h
13Ch	MCSPI_RX_0	RX register of channel 0	0215 013Ch	0216 013Ch	0217 013Ch
140h	MCSPI_CHCONF_1	Configuration register of channel 1	0215 0140h	0216 0140h	0217 0140h
144h	MCSPI_CHSTAT_1	Status register of channel 1	0215 0144h	0216 0144h	0217 0144h
148h	MCSPI_CHCTRL_1	Enable register of channel 1	0215 0148h	0216 0148h	0217 0148h
14Ch	MCSPI_TX_1	TX register of channel 1	0215 014Ch	0216 014Ch	0217 014Ch
150h	MCSPI_RX_1	RX register of channel 1	0215 0150h	0216 0150h	0217 0150h
154h	MCSPI_CHCONF_2	Configuration register of channel 2	0215 0154h	0216 0154h	0217 0154h
158h	MCSPI_CHSTAT_2	Status register of channel 2	0215 0158h	0216 0158h	0217 0158h
15Ch	MCSPI_CHCTRL_2	Enable register of channel 2	0215 015Ch	0216 015Ch	0217 015Ch
160h	MCSPI_TX_2	TX register of channel 2	0215 0160h	0216 0160h	0217 0160h
164h	MCSPI_RX_2	RX register of channel 2	0215 0164h	0216 0164h	0217 0164h
168h	MCSPI_CHCONF_3	Configuration register of channel 3	0215 0168h	0216 0168h	0217 0168h
16Ch	MCSPI_CHSTAT_3	Status register of channel 3	0215 016Ch	0216 016Ch	0217 016Ch
170h	MCSPI_CHCTRL_3	Enable register of channel 3	0215 0170h	0216 0170h	0217 0170h
174h	MCSPI_TX_3	TX register of channel 3	0215 0174h	0216 0174h	0217 0174h
178h	MCSPI_RX_3	RX register of channel 3	0215 0178h	0216 0178h	0217 0178h
17Ch	MCSPI_XFERLEVEL	Transfer levels when FIFO is used	0215 017Ch	0216 017Ch	0217 017Ch
180h	MCSPI_DAFTX	MCSPI words transmitted when FIFO is used	0215 0180h	0216 0180h	0217 0180h
1A0h	MCSPI_DAFRX	MCSPI words received when FIFO is used	0215 01A0h	0216 01A0h	0217 01A0h

Table 5-5. MCSPI Registers

Offset	Acronym	Register Name	MCU_MCSPI0_CFG Physical Address	MCU_MCSPI1_CFG Physical Address	MCU_MCSPI2_CFG Physical Address
0h	MCSPI_HL_REV	IP Revision register	4030 0000h	4031 0000h	4032 0000h

Table 5-5. MCSPI Registers (continued)

Offset	Acronym	Register Name	MCU_MCSPI0_ CFG Physical Address	MCU_MCSPI1_ CFG Physical Address	MCU_MCSPI2_ CFG Physical Address
4h	MCSPI_HL_HWINFO	MCSPI hardware configuration register	4030 0004h	4031 0004h	4032 0004h
10h	MCSPI_HL_SYSCONFIG	Clock management configuration register	4030 0010h	4031 0010h	4032 0010h
100h	MCSPI_REVISION	Revision number	4030 0100h	4031 0100h	4032 0100h
110h	MCSPI_SYSCONFIG	Configuration register	4030 0110h	4031 0110h	4032 0110h
114h	MCSPI_SYSSTATUS	Status information register	4030 0114h	4031 0114h	4032 0114h
118h	MCSPI_IRQSTATUS	Interrupt status register	4030 0118h	4031 0118h	4032 0118h
11Ch	MCSPI_IRQENABLE	Interrupt enable register	4030 011Ch	4031 011Ch	4032 011Ch
120h	MCSPI_WAKEUPENABLE	Wake-up enable register	4030 0120h	4031 0120h	4032 0120h
124h	MCSPI_SYST	System interconnect check in system test mode	4030 0124h	4031 0124h	4032 0124h
128h	MCSPI_MODULCTRL	MCSPI configuration register	4030 0128h	4031 0128h	4032 0128h
12Ch	MCSPI_CHCONF_0	Configuration register of channel 0	4030 012Ch	4031 012Ch	4032 012Ch
130h	MCSPI_CHSTAT_0	Status register of channel 0	4030 0130h	4031 0130h	4032 0130h
134h	MCSPI_CHCTRL_0	Enable register of channel 0	4030 0134h	4031 0134h	4032 0134h
138h	MCSPI_TX_0	TX register of channel 0	4030 0138h	4031 0138h	4032 0138h
13Ch	MCSPI_RX_0	RX register of channel 0	4030 013Ch	4031 013Ch	4032 013Ch
140h	MCSPI_CHCONF_1	Configuration register of channel 1	4030 0140h	4031 0140h	4032 0140h
144h	MCSPI_CHSTAT_1	Status register of channel 1	4030 0144h	4031 0144h	4032 0144h
148h	MCSPI_CHCTRL_1	Enable register of channel 1	4030 0148h	4031 0148h	4032 0148h
14Ch	MCSPI_TX_1	TX register of channel 1	4030 014Ch	4031 014Ch	4032 014Ch
150h	MCSPI_RX_1	RX register of channel 1	4030 0150h	4031 0150h	4032 0150h
154h	MCSPI_CHCONF_2	Configuration register of channel 2	4030 0154h	4031 0154h	4032 0154h
158h	MCSPI_CHSTAT_2	Status register of channel 2	4030 0158h	4031 0158h	4032 0158h
15Ch	MCSPI_CHCTRL_2	Enable register of channel 2	4030 015Ch	4031 015Ch	4032 015Ch
160h	MCSPI_TX_2	TX register of channel 2	4030 0160h	4031 0160h	4032 0160h
164h	MCSPI_RX_2	RX register of channel 2	4030 0164h	4031 0164h	4032 0164h
168h	MCSPI_CHCONF_3	Configuration register of channel 3	4030 0168h	4031 0168h	4032 0168h
16Ch	MCSPI_CHSTAT_3	Status register of channel 3	4030 016Ch	4031 016Ch	4032 016Ch
170h	MCSPI_CHCTRL_3	Enable register of channel 3	4030 0170h	4031 0170h	4032 0170h
174h	MCSPI_TX_3	TX register of channel 3	4030 0174h	4031 0174h	4032 0174h
178h	MCSPI_RX_3	RX register of channel 3	4030 0178h	4031 0178h	4032 0178h
17Ch	MCSPI_XFERLEVEL	Transfer levels when FIFO is used	4030 017Ch	4031 017Ch	4032 017Ch
180h	MCSPI_DAFTX	MCSPI words transmitted when FIFO is used	4030 0180h	4031 0180h	4032 0180h
1A0h	MCSPI_DAFRX	MCSPI words received when FIFO is used	4030 01A0h	4031 01A0h	4032 01A0h

5.1 MCSPI_HL_REV Register (Offset = 0h) [reset = 40301A0Bh]

MCSPi_HL_REV is shown in [Figure 5-1](#) and described in [Table 5-7](#).

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IP Revision Identifier (X.Y.R)

Used by software to track features, bugs, and compatibility

Table 5-6. MCSPI_HL_REV Instances

Instance	Physical Address
MCSPi0_CFG	0210 0000h
MCSPi1_CFG	0211 0000h
MCSPi2_CFG	0212 0000h
MCSPi3_CFG	0213 0000h
MCSPi4_CFG	0214 0000h
MCSPi5_CFG	0215 0000h
MCSPi6_CFG	0216 0000h
MCSPi7_CFG	0217 0000h
MCU_MCSPi0_CFG	4030 0000h
MCU_MCSPi1_CFG	4031 0000h
MCU_MCSPi2_CFG	4032 0000h

Figure 5-1. MCSPI_HL_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-40301A0Bh																															

LEGEND: R = Read Only; -n = value after reset

Table 5-7. MCSPI_HL_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	40301A0Bh	IP Revision

5.2 MCSPI_HL_HWINFO Register (Offset = 4h) [reset = 41h]

MCSPI_HL_HWINFO is shown in [Figure 5-2](#) and described in [Table 5-9](#).

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Information about the IP module's hardware configuration, that is, typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

Table 5-8. MCSPI_HL_HWINFO Instances

Instance	Physical Address
MCSPi0_CFG	0210 0004h
MCSPi1_CFG	0211 0004h
MCSPi2_CFG	0212 0004h
MCSPi3_CFG	0213 0004h
MCSPi4_CFG	0214 0004h
MCSPi5_CFG	0215 0004h
MCSPi6_CFG	0216 0004h
MCSPi7_CFG	0217 0004h
MCU_MCSPi0_CFG	4030 0004h
MCU_MCSPi1_CFG	4031 0004h
MCU_MCSPi2_CFG	4032 0004h

Figure 5-2. MCSPI_HL_HWINFO Register

31	30	29	28	27	26	25	24
RSVD							
R-0h							
23	22	21	20	19	18	17	16
RSVD							
R-0h							
15	14	13	12	11	10	9	8
RSVD							
R-0h							
7	6	5	4	3	2	1	0
RSVD	RETMODE	FFNBYTE				USEFIFO	
R-0h	R-0h	R-4h				R-1h	

LEGEND: R = Read Only; -n = value after reset

Table 5-9. MCSPI_HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RSVD	R	0h	Reserved These bits are initialized to 0, and writes to them are ignored.
6	RETMODE	R	0h	Retention Mode generic parameter. This bit field indicates whether the retention mode is supported using the pin PIRFFRET. 0h = Retention mode disabled 1h = Retention mode enabled

Table 5-9. MCSPI_HL_HWINFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-1	FFNBYTE	R	4h	<p>FIFO number of byte generic parameter</p> <p>This field defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account.</p> <p>1h (R) = FIFO 16 bytes depth</p> <p>2h (R) = FIFO 32 bytes depth</p> <p>4h (R) = FIFO 64 bytes depth</p> <p>8h (R) = FIFO 128 bytes depth</p> <p>10h (R) = FIFO 256 bytes depth</p>
0	USEFIFO	R	1h	<p>Use of a FIFO enable:</p> <p>This bit indicates if a FIFO is integrated within controller design with its management.</p> <p>0h (R) = FIFO not implemented in design</p> <p>1h (R) = FIFO and its management implemented in design with depth defined by FFNBYTE generic</p>

5.3 MCSPI_HL_SYSCONFIG Register (Offset = 10h) [reset = 8h]

MCSPI_HL_SYSCONFIG is shown in [Figure 5-3](#) and described in [Table 5-11](#).

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Clock management configuration

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

Table 5-10. MCSPI_HL_SYSCONFIG Instances

Instance	Physical Address
MCSPi0_CFG	0210 0010h
MCSPi1_CFG	0211 0010h
MCSPi2_CFG	0212 0010h
MCSPi3_CFG	0213 0010h
MCSPi4_CFG	0214 0010h
MCSPi5_CFG	0215 0010h
MCSPi6_CFG	0216 0010h
MCSPi7_CFG	0217 0010h
MCU_MCSPi0_CFG	4030 0010h
MCU_MCSPi1_CFG	4031 0010h
MCU_MCSPi2_CFG	4032 0010h

Figure 5-3. MCSPI_HL_SYSCONFIG Register

31	30	29	28	27	26	25	24
RSVD							
R-0h							
23	22	21	20	19	18	17	16
RSVD							
R-0h							
15	14	13	12	11	10	9	8
RSVD							
R-0h							
7	6	5	4	3	2	1	0
RSVD				IDLEMODE		FREEEMU	SOFTRESET
R-0h				R/W-2h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-11. MCSPI_HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RSVD	R	0h	Reads returns 0

Table 5-11. MCSPI_HL_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	IDLEMODE	R/W	2h	<p>Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state.</p> <p>0h (R/W) = Force-idle mode: local target's IDLE state follows (acknowledges) the system's clock stop requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only.</p> <p>1h (R/W) = No-idle mode: local target never enters IDLE state. Backup mode, for debug only.</p> <p>2h (R/W) = Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events.</p> <p>3h (R/W) = Smart-idle wake-up-capable mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wake-up events when in IDLE state.</p>
1	FREEEMU	R/W	0h	<p>Sensitivity to emulation (debug) suspend input signal.</p> <p>0h (R/W) = IP module is sensitive to emulation suspend.</p> <p>1h (R/W) = IP module is not sensitive to emulation suspend.</p>
0	SOFTRESET	R/W	0h	<p>Software reset. (Optional)</p> <p>0h (R/W) = Reset done, no pending action</p> <p>1h (R/W) = Initiate software reset</p>

5.4 MCSPI_REVISION Register (Offset = 100h) [reset = 2Bh]

MCSPI_REVISION is shown in [Figure 5-4](#) and described in [Table 5-13](#).

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This register contains the revision number.

Table 5-12. MCSPI_REVISION Instances

Instance	Physical Address
MCSPi0_CFG	0210 0100h
MCSPi1_CFG	0211 0100h
MCSPi2_CFG	0212 0100h
MCSPi3_CFG	0213 0100h
MCSPi4_CFG	0214 0100h
MCSPi5_CFG	0215 0100h
MCSPi6_CFG	0216 0100h
MCSPi7_CFG	0217 0100h
MCU_MCSPi0_CFG	4030 0100h
MCU_MCSPi1_CFG	4031 0100h
MCU_MCSPi2_CFG	4032 0100h

Figure 5-4. MCSPI_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-2Bh																															

LEGEND: R = Read Only; -n = value after reset

Table 5-13. MCSPI_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	2Bh	IP revision

5.5 MCSPI_SYSCONFIG Register (Offset = 110h) [reset = 15h]

MCSPI_SYSCONFIG is shown in [Figure 5-5](#) and described in [Table 5-15](#).

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This register allows controlling various parameters of the configuration interface and is not affected by software reset.

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

Table 5-14. MCSPI_SYSCONFIG Instances

Instance	Physical Address
MCSPI0_CFG	0210 0110h
MCSPI1_CFG	0211 0110h
MCSPI2_CFG	0212 0110h
MCSPI3_CFG	0213 0110h
MCSPI4_CFG	0214 0110h
MCSPI5_CFG	0215 0110h
MCSPI6_CFG	0216 0110h
MCSPI7_CFG	0217 0110h
MCU_MCSPI0_CFG	4030 0110h
MCU_MCSPI1_CFG	4031 0110h
MCU_MCSPI2_CFG	4032 0110h

Figure 5-5. MCSPI_SYSCONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						CLOCKACTIVITY	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R-0h			R/W-2h		R/W-1h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-15. MCSPI_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reads returns 0

Table 5-15. MCSPI_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	CLOCKACTIVITY	R/W	0h	Clocks activity during wake-up mode period 0h (R/W) = Interface and functional clocks may be switched off. 1h (R/W) = Interface clock is maintained. Functional clock may be switched off. 2h (R/W) = Functional clock is maintained. Interface clock may be switched off. 3h (R/W) = Interface and functional clocks are maintained.
7-5	RESERVED	R	0h	Reads returns 0
4-3	SIDLEMODE	R/W	2h	Power management 0h (R/W) = If an IDLE request is detected, the MCSPI acknowledges it unconditionally and goes in inactive mode. Interrupt, DMA requests and wake-up lines are unconditionally deasserted and the module wake-up capability is deactivated even if the MCSPI_SYSCONFIG[2] ENAWAKEUP bit is set. 1h (R/W) = If an IDLE request is detected, the request is ignored and the module does not switch to wake-up mode, and keeps on behaving normally. 2h (R/W) = If an IDLE request is detected, the module will switch to wake-up mode based on its internal activity, and the wake-up capability can be used if the bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set. 3h (R/W) = Reserved - do not use.
2	ENAWAKEUP	R/W	1h	Wake-up feature control 0h (R/W) = Wake-up capability is disabled. 1h (R/W) = Wake-up capability is enabled.
1	SOFTRESET	R/W	0h	Software reset. During reads it always returns 0. 0h (R/W) = (write) Normal mode 1h (R/W) = (write) Set this bit to 1 to trigger a module reset. The bit is automatically reset by the hardware.
0	AUTOIDLE	R/W	1h	Internal interface clock-gating strategy 0h (R/W) = Interface clock is free-running. 1h (R/W) = Automatic interface clock gating strategy is applied, based on the configuration interface activity.

5.6 MCSPI_SYSSTATUS Register (Offset = 114h) [reset = 1h]

MCSPi_SYSSTATUS is shown in [Figure 5-6](#) and described in [Table 5-17](#).

[Return to Summary Table.](#)

This register provides status information about the module excluding the interrupt status information.

Table 5-16. MCSPI_SYSSTATUS Instances

Instance	Physical Address
MCSPi0_CFG	0210 0114h
MCSPi1_CFG	0211 0114h
MCSPi2_CFG	0212 0114h
MCSPi3_CFG	0213 0114h
MCSPi4_CFG	0214 0114h
MCSPi5_CFG	0215 0114h
MCSPi6_CFG	0216 0114h
MCSPi7_CFG	0217 0114h
MCU_MCSPi0_CFG	4030 0114h
MCU_MCSPi1_CFG	4031 0114h
MCU_MCSPi2_CFG	4032 0114h

Figure 5-6. MCSPI_SYSSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R-0h							R-1h

LEGEND: R = Read Only; -n = value after reset

Table 5-17. MCSPI_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved for module specific status information. Read returns 0.
0	RESETDONE	R	1h	Internal reset monitoring 0h (R) = Internal module reset is ongoing 1h (R) = Reset completed

5.7 MCSPI_IRQSTATUS Register (Offset = 118h) [reset = 0h]

MCSPI_IRQSTATUS is shown in [Figure 5-7](#) and described in [Table 5-19](#).

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The interrupt status regroups all the status of the module internal events that can generate an interrupt.

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

Table 5-18. MCSPI_IRQSTATUS Instances

Instance	Physical Address
MCSPi0_CFG	0210 0118h
MCSPi1_CFG	0211 0118h
MCSPi2_CFG	0212 0118h
MCSPi3_CFG	0213 0118h
MCSPi4_CFG	0214 0118h
MCSPi5_CFG	0215 0118h
MCSPi6_CFG	0216 0118h
MCSPi7_CFG	0217 0118h
MCU_MCSPi0_CFG	4030 0118h
MCU_MCSPi1_CFG	4031 0118h
MCU_MCSPi2_CFG	4032 0118h

Figure 5-7. MCSPI_IRQSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						EOW	WKS
R-0h						R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RESERVED	RX3_FULL	TX3_UNDERFL OW	TX3_EMPTY	RESERVED	RX2_FULL	TX2_UNDERFL OW	TX2_EMPTY
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RESERVED	RX1_FULL	TX1_UNDERFL OW	TX1_EMPTY	RX0_OVERFL OW	RX0_FULL	TX0_UNDERFL OW	TX0_EMPTY
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-19. MCSPI_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reads returns 0
17	EOW	R/W1C	0h	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of MCSPI word defined by MCSPI_XFERLEVEL[31-16] WCNT. 0h (R/W) = Event false 1h (R/W) = Event status bit is reset

Table 5-19. MCSPI_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	WKS	R/W1C	0h	Wake-up event in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CHCONF_0[22-21] SPIENSLV 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
15	RESERVED	R	0h	Reads returns 0
14	RX3_FULL	R/W1C	0h	Receiver register is full or almost full. Only when Channel 3 is enabled 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
13	TX3_UNDERFLOW	R/W1C	0h	Transmitter register underflow. Only when Channel 3 is enabled. The transmitter register is empty (not updated by host or DMA with new data) before its time slot assignment. Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled. 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
12	TX3_EMPTY	R/W1C	0h	Transmitter register is empty or almost empty. Note: Enabling the channel automatically rises this event. 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
11	RESERVED	R	0h	Reads returns 0.
10	RX2_FULL	R/W1C	0h	Receiver register full or almost full. Channel 2 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
9	TX2_UNDERFLOW	R/W1C	0h	Transmitter register underflow. Channel 2 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
8	TX2_EMPTY	R/W1C	0h	Transmitter register empty or almost empty. Channel 2 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
7	RESERVED	R	0h	Reads returns 0
6	RX1_FULL	R/W1C	0h	Receiver register full or almost full. Channel 1 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
5	TX1_UNDERFLOW	R/W1C	0h	Transmitter register underflow. Channel 1 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
4	TX1_EMPTY	R/W1C	0h	Transmitter register empty or almost empty. Channel 1 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
3	RX0_OVERFLOW	R/W1C	0h	Receiver register overflow (slave mode only). Channel 0 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
2	RX0_FULL	R/W1C	0h	Receiver register full or almost full. Channel 0 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending

Table 5-19. MCSPI_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TX0_UNDERFLOW	R/W1C	0h	Transmitter register underflow. Channel 0 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending
0	TX0_EMPTY	R/W1C	0h	Transmitter register empty or almost empty. Channel 0 0h (R/W) = Event status bit unchanged 1h (R/W) = Event is pending

5.8 MCSPI_IRQENABLE Register (Offset = 11Ch) [reset = 0h]

MCSPI_IRQENABLE is shown in [Figure 5-8](#) and described in [Table 5-21](#).

Return to [Summary Table](#).

This register allows enabling/disabling of the module internal sources of interrupt, on an event-by-event basis.

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

Table 5-20. MCSPI_IRQENABLE Instances

Instance	Physical Address
MCSPI0_CFG	0210 011Ch
MCSPI1_CFG	0211 011Ch
MCSPI2_CFG	0212 011Ch
MCSPI3_CFG	0213 011Ch
MCSPI4_CFG	0214 011Ch
MCSPI5_CFG	0215 011Ch
MCSPI6_CFG	0216 011Ch
MCSPI7_CFG	0217 011Ch
MCU_MCSPI0_CFG	4030 011Ch
MCU_MCSPI1_CFG	4031 011Ch
MCU_MCSPI2_CFG	4032 011Ch

Figure 5-8. MCSPI_IRQENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						EOW_ENABLE	WKE
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	RX3_FULL_EN ABLE	TX3_UNDERFL OW_ENABLE	TX3_EMPTY_E NABLE	RESERVED	RX2_FULL_EN ABLE	TX2_UNDERFL OW_ENABLE	TX2_EMPTY_E NABLE
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RX1_FULL_EN ABLE	TX1_UNDERFL OW_ENABLE	TX1_EMPTY_E NABLE	RX0_OVERFL OW_ENABLE	RX0_FULL_EN ABLE	TX0_UNDERFL OW_ENABLE	TX0_EMPTY_E NABLE
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-21. MCSPI_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reads return 0.
17	EOW_ENABLE	R/W	0h	End of Word count Interrupt Enable. 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled

Table 5-21. MCSPI_IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	WKE	R/W	0h	Wake-up event interrupt enable in slave mode when an active control signal is detected on the SPIEN line programmed in the MCSPI_CHCONF_0[22-21] SPIENSLV bit 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
15	RESERVED	R	0h	Reads returns 0.
14	RX3_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable. Channel 3 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
13	TX3_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable. Channel 3 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
12	TX3_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable. Channel 3 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
11	RESERVED	R	0h	Reads return 0.
10	RX2_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable. Channel 2 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
9	TX2_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable. Channel 2 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
8	TX2_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable. Channel 2 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
7	RESERVED	R	0h	Reads return 0.
6	RX1_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable. Channel 1 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
5	TX1_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable. Channel 1 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
4	TX1_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable. Channel 1 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
3	RX0_OVERFLOW_ENABLE	R/W	0h	Receiver register Overflow Interrupt Enable. Channel 0 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
2	RX0_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable. Channel 0 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
1	TX0_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable. Channel 0 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled
0	TX0_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable. Channel 0 0h (R/W) = Interrupt disabled 1h (R/W) = Interrupt enabled

5.9 MCSPI_WAKEUPENABLE Register (Offset = 120h) [reset = 0h]

MCSPI_WAKEUPENABLE is shown in [Figure 5-9](#) and described in [Table 5-23](#).

Return to [Summary Table](#).

The wake-up enable register allows enabling and disabling of the module internal sources of wakeup on event-by-event basis.

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see *MCSPI Not Supported Features*.

Table 5-22. MCSPI_WAKEUPENABLE Instances

Instance	Physical Address
MCSPI0_CFG	0210 0120h
MCSPI1_CFG	0211 0120h
MCSPI2_CFG	0212 0120h
MCSPI3_CFG	0213 0120h
MCSPI4_CFG	0214 0120h
MCSPI5_CFG	0215 0120h
MCSPI6_CFG	0216 0120h
MCSPI7_CFG	0217 0120h
MCU_MCSPI0_CFG	4030 0120h
MCU_MCSPI1_CFG	4031 0120h
MCU_MCSPI2_CFG	4032 0120h

Figure 5-9. MCSPI_WAKEUPENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							WKEN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-23. MCSPI_WAKEUPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reads returns 0.

Table 5-23. MCSPI_WAKEUPENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	WKEN	R/W	0h	<p>Wake-up functionality in slave mode when an active control signal is detected on the SPIEN line programmed in the MCSPI_CHCONF_0[22-21] SPIENSLV bit</p> <p>0h (R/W) = The event is not allowed to wake-up the system, even if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set.</p> <p>1h (R/W) = The event is allowed to wake-up the system if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set.</p>

5.10 MCSPI_SYST Register (Offset = 124h) [reset = 0h]

MCSPi_SYST is shown in [Figure 5-10](#) and described in [Table 5-25](#).

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This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device I/O pads, when the module is configured in system test (SYSTEST) mode.

Table 5-24. MCSPI_SYST Instances

Instance	Physical Address
MCSPi0_CFG	0210 0124h
MCSPi1_CFG	0211 0124h
MCSPi2_CFG	0212 0124h
MCSPi3_CFG	0213 0124h
MCSPi4_CFG	0214 0124h
MCSPi5_CFG	0215 0124h
MCSPi6_CFG	0216 0124h
MCSPi7_CFG	0217 0124h
MCU_MCSPi0_CFG	4030 0124h
MCU_MCSPi1_CFG	4031 0124h
MCU_MCSPi2_CFG	4032 0124h

Figure 5-10. MCSPI_SYST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-25. MCSPI_SYST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reads returns 0.
11	SSB	R/W	0h	Set status bit 0h (R/W) = No action. Writing 0 does not clear already set status bits. This bit must be cleared before trying to clear a status bit of the MCSPi_IRQSTATUS register. 1h (R/W) = Force to 1 all status bits of MCSPi_IRQSTATUS register. Writing 1 into this bit sets to 1 all status bits in the MCSPi_IRQSTATUS register.
10	SPIENDIR	R/W	0h	Set the direction of the SPIEN[3:0] lines and SPICLK line. 0h (R/W) = Output (as in master mode) 1h (R/W) = Input (as in slave mode)

Table 5-25. MCSPI_SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	SPIDATDIR1	R/W	0h	Set the direction of the SPIDAT[1]. 0h (R/W) = Output 1h (R/W) = Input
8	SPIDATDIR0	R/W	0h	Set the direction of the SPIDAT[0]. 0h (R/W) = Output 1h (R/W) = Input
7	WAKD	R/W	0h	SWAKEUP output (signal data value of internal signal to system). The signal is driven high or low according to the value written into this bit. 0h (R/W) = The pin is driven low. 1h (R/W) = The pin is driven high.
6	SPICLK	R/W	0h	SPICLK line (signal data value) If MCSPI_SYST[10] SPIENDIR = 1 (input mode direction), this bit returns the value on the CLKSPI line (high or low), and a write into this bit has no effect. If MCSPI_SYST[10] SPIENDIR = 0 (output mode direction), the CLKSPI line is driven high or low according to the value written into this bit.
5	SPIDAT_1	R/W	0h	SPIDAT[1] line (signal data value) If MCSPI_SYST[9] SPIDATDIR1 = 0 (output mode direction), the SPIDAT[1] line is driven high or low according to the value written into this bit. If MCSPI_SYST[9] SPIDATDIR1 = 1 (input mode direction), this bit returns the value on the SPIDAT[1] line (high or low), and a write into this bit has no effect.
4	SPIDAT_0	R/W	0h	SPIDAT[0] line (signal data value) If MCSPI_SYST[8] SPIDATDIR0 = 0 (output mode direction), the SPIDAT[0] line is driven high or low according to the value written into this bit. If MCSPI_SYST[8] SPIDATDIR0 = 1 (input mode direction), this bit returns the value on the SPIDAT[0] line (high or low), and a write into this bit has no effect.
3	SPIEN_3	R/W	0h	SPIEN[3] line (signal data value) If MCSPI_SYST[10] SPIENDIR = 0 (output mode direction), the SPIEN[3] line is driven high or low according to the value written into this bit. If MCSPI_SYST[10] SPIENDIR = 1 (input mode direction), this bit returns the value on the SPIEN[3] line (high or low), and a write into this bit has no effect.
2	SPIEN_2	R/W	0h	SPIEN[2] line (signal data value) If MCSPI_SYST[10] SPIENDIR = 0 (output mode direction), the SPIEN[2] line is driven high or low according to the value written into this bit. If MCSPI_SYST[10] SPIENDIR = 1 (input mode direction), this bit returns the value on the SPIEN[2] line (high or low), and a write into this bit has no effect.

Table 5-25. MCSPI_SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SPIEN_1	R/W	0h	<p>SPIEN[1] line (signal data value)</p> <p>If MCSPI_SYST[10] SPIENDIR = 0 (output mode direction), the SPIEN[1] line is driven high or low according to the value written into this bit.</p> <p>If MCSPI_SYST[10] SPIENDIR = 1 (input mode direction), this bit returns the value on the SPIEN[1] line (high or low), and a write into this bit has no effect.</p>
0	SPIEN_0	R/W	0h	<p>SPIEN[0] line (signal data value)</p> <p>If MCSPI_SYST[10] SPIENDIR = 0 (output mode direction), the SPIEN[0] line is driven high or low according to the value written into this bit.</p> <p>If MCSPI_SYST[10] SPIENDIR = 1 (input mode direction), this bit returns the value on the SPIEN[0] line (high or low), and a write into this bit has no effect.</p>

5.11 MCSPI_MODULCTRL Register (Offset = 128h) [reset = 4h]

MCSPI_MODULCTRL is shown in [Figure 5-11](#) and described in [Table 5-27](#).

Return to [Summary Table](#).

This register is dedicated to the configuration of the serial peripheral interface.

Table 5-26. MCSPI_MODULCTRL Instances

Instance	Physical Address
MCSPi0_CFG	0210 0128h
MCSPi1_CFG	0211 0128h
MCSPi2_CFG	0212 0128h
MCSPi3_CFG	0213 0128h
MCSPi4_CFG	0214 0128h
MCSPi5_CFG	0215 0128h
MCSPi6_CFG	0216 0128h
MCSPi7_CFG	0217 0128h
MCU_MCSPi0_CFG	4030 0128h
MCU_MCSPi1_CFG	4031 0128h
MCU_MCSPi2_CFG	4032 0128h

Figure 5-11. MCSPI_MODULCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							FDAA
R-0h							R/W-0h
7	6	5	4	3	2	1	0
MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE
R/W-0h	R-0h			R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-27. MCSPI_MODULCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reads returns 0.
8	FDAA	R/W	0h	FIFO DMA address 256-bit aligned This bit is used when a FIFO is managed by the module and DMA connected to the controller provides only 256-bit aligned address. If this bit is set the enabled channel which uses the FIFO has its data managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX(i) and MCSPI_RX(i) registers. 0h (R/W) = FIFO data managed by MCSPI_TX(i) and MCSPI_RX(i) registers. 1h (R/W) = FIFO data managed by MCSPI_DAFTX and MCSPI_DAFRX registers.

Table 5-27. MCSPI_MODULCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	MOA	R/W	0h	Multiple word configuration interface access: This bit can only be used when a channel is enabled using a FIFO. It allows the system to perform multiple MCSPI word access for a single 32-bit interface word access. This is possible for WL < 16. 0h (R/W) = Multiple word access disabled 1h (R/W) = Multiple word access enabled with FIFO
6-4	INITDLY	R/W	0h	Initial MCSPI delay for first transfer: This field is an option only available in SINGLE master mode. The controller waits for a delay to transmit the first MCSPI word after channel enabled and corresponding TX register filled. This delay is based on MCSPI output frequency clock. No clock output provided to the boundary and chip select is not active in 4-pin mode within this period. 0h (R/W) = No delay for first MCSPI transfer. 1h (R/W) = The controller wait 4 MCSPI bus clock 2h (R/W) = The controller wait 8 MCSPI bus clock 3h (R/W) = The controller wait 16 MCSPI bus clock 4h (R/W) = The controller wait 32 MCSPI bus clock
3	SYSTEM_TEST	R/W	0h	Enables the system test mode 0h (R/W) = Functional mode 1h (R/W) = System test mode (SYSTEST)
2	MS	R/W	1h	Master/slave 0h (R/W) = Master - The module generates the SPICLK and SPIEN[3:0]. 1h (R/W) = Slave - The module receives the SPICLK and SPIEN[3:0].
1	PIN34	R/W	0h	Pin mode selection: This bit is used in master or slave mode to configure the MCSPI pin mode (3-pin or 4-pin). If asserted the controller only uses SIMO, SOMI, and SPICLK clock pin for MCSPI transfers. 0h (R/W) = SPIEN is used as a chip-select. 1h (R/W) = SPIEN is not used. In this mode all related options to chip-select have no meaning.
0	SINGLE	R/W	0h	Single channel/Multi Channel (master mode only) 0h (R/W) = More than one channel will be used in master mode. 1h (R/W) = Only one channel will be used in master mode. This bit must be set in Force SPIEN[i] mode.

5.12 MCSPI_CHCONF_0 Register (Offset = 12Ch) [reset = 00060000h]

MCSPI_CHCONF_0 is shown in [Figure 5-12](#) and described in [Table 5-29](#).

Return to [Summary Table](#).

This register is dedicated to the configuration of the channel i.

Table 5-28. MCSPI_CHCONF_0 Instances

Instance	Physical Address
MCSPi0_CFG	0210 012Ch
MCSPi1_CFG	0211 012Ch
MCSPi2_CFG	0212 012Ch
MCSPi3_CFG	0213 012Ch
MCSPi4_CFG	0214 012Ch
MCSPi5_CFG	0215 012Ch
MCSPi6_CFG	0216 012Ch
MCSPi7_CFG	0217 012Ch
MCU_MCSPi0_CFG	4030 012Ch
MCU_MCSPi1_CFG	4031 012Ch
MCU_MCSPi2_CFG	4032 012Ch

Figure 5-12. MCSPI_CHCONF_0 Register

31	30	29	28	27	26	25	24
RESERVED		CLKG	FFER	FFEW	TCS0		SBPOL
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
23	22	21	20	19	18	17	16
SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
DMAR	DMAW	TRM		WL			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
WL	EPOL	CLKD				POL	PHA
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-29. MCSPI_CHCONF_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Read returns 0.
29	CLKG	R/W	0h	<p>Clock divider granularity</p> <p>This bit defines the granularity of channel clock divider: power of 2 or one clock cycle granularity.</p> <p>When this bit is set the register MCSPI_CHCTRL_0[15-8] EXTCLK must be configured to reach a maximum of 4096 clock divider ratio. Then the clock divider ratio is a concatenation of MCSPI_CHCONF_0[5-2] CLKD and MCSPI_CHCTRL_0[15-8] EXTCLK values</p> <p>0h (R/W) = Clock granularity of power of 2</p> <p>1h (R/W) = One clock cycle granularity</p>

Table 5-29. MCSPI_CHCONF_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	FFER	R/W	0h	FIFO enabled for receive: Only one channel can have this bit field set. 0h (R/W) = The buffer is not used to receive data. 1h (R/W) = The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for transmit: Only one channel can have this bit field set. 0h (R/W) = The buffer is not used to transmit data. 1h (R/W) = The buffer is used to transmit data.
26-25	TCS0	R/W	0h	Chip-select time control This 2-bit field defines the number of interface clock cycles between CS toggling and first or last edge of MCSPI clock. 0h (R/W) = 0.5 clock cycle 1h (R/W) = 1.5 clock cycles 2h (R/W) = 2.5 clock cycles 3h (R/W) = 3.5 clock cycles
24	SBPOL	R/W	0h	Start-bit polarity 0h (R/W) = Start-bit polarity is held to 0 during MCSPI transfer. 1h (R/W) = Start-bit polarity is held to 1 during MCSPI transfer.
23	SBE	R/W	0h	Start-bit enable for MCSPI transfer 0h (R/W) = Default MCSPI transfer length as specified by WL bit field 1h (R/W) = Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22-21	SPIENSLV	R/W	0h	Channel 0 only and slave mode only: MCSPI slave select signal detection. Reserved bits for other cases. 0h (R/W) = Detection enabled only on SPIEN[0] 1h (R/W) = Detection enabled only on SPIEN[1] 2h (R/W) = Detection enabled only on SPIEN[2] 3h (R/W) = Detection enabled only on SPIEN[3]
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between MCSPI words (single channel master mode only). 0h (R/W) = Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1h (R/W) = Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0h (R/W) = Turbo is deactivated (recommended for single MCSPI word transfer). 1h (R/W) = Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0h (R/W) = Data line 0 (SPIDAT[0]) selected for reception 1h (R/W) = Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission enable for data line 1 0h (R/W) = Data line 1 (SPIDAT[1]) selected for transmission 1h (R/W) = No transmission on Data Line1 (SPIDAT[1])

Table 5-29. MCSPI_CHCONF_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	DPE0	R/W	0h	Transmission Enable for data line 0 0h (R/W) = Data Line0 (SPIDAT[0]) selected for transmission 1h (R/W) = No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA read request The DMA read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel. The DMA read request line is deasserted on read completion of the receive register of the channel. 0h (R/W) = DMA read request disabled 1h (R/W) = DMA read request enabled
14	DMAW	R/W	0h	DMA write request. The DMA write request line is asserted when The channel is enabled and the transmitter register of the channel is empty. The DMA write request line is deasserted on load completion of the transmitter register of the channel. 0h (R/W) = DMA write request disabled 1h (R/W) = DMA write request enabled
13-12	TRM	R/W	0h	Transmit/receive modes 0h (R/W) = Transmit-and-receive mode 1h (R/W) = Receive-only mode 2h (R/W) = Transmit-only mode 3h (R/W) = Reserved

Table 5-29. MCSPI_CHCONF_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-7	WL	R/W	0h	SPI word length 0h (R/W) = Reserved 1h (R/W) = Reserved 2h (R/W) = Reserved 3h (R/W) = The MCSPI word is 4 bits long 4h (R/W) = The MCSPI word is 5 bits long 5h (R/W) = The MCSPI word is 6 bits long 6h (R/W) = The MCSPI word is 7 bits long 7h (R/W) = The MCSPI word is 8 bits long 8h (R/W) = The MCSPI word is 9 bits long 9h (R/W) = The MCSPI word is 10 bits long Ah (R/W) = The MCSPI word is 11 bits long Bh (R/W) = The MCSPI word is 12 bits long Ch (R/W) = The MCSPI word is 13 bits long Dh (R/W) = The MCSPI word is 14 bits long Eh (R/W) = The MCSPI word is 15 bits long Fh (R/W) = The MCSPI word is 16 bits long 10h (R/W) = The MCSPI word is 17 bits long 11h (R/W) = The MCSPI word is 18 bits long 12h (R/W) = The MCSPI word is 19 bits long 13h (R/W) = The MCSPI word is 20 bits long 14h (R/W) = The MCSPI word is 21 bits long 15h (R/W) = The MCSPI word is 22 bits long 16h (R/W) = The MCSPI word is 23 bits long 17h (R/W) = The MCSPI word is 24 bits long 18h (R/W) = The MCSPI word is 25 bits long 19h (R/W) = The MCSPI word is 26 bits long 1Ah (R/W) = The MCSPI word is 27 bits long 1Bh (R/W) = The MCSPI word is 28 bits long 1Ch (R/W) = The MCSPI word is 29 bits long 1Dh (R/W) = The MCSPI word is 30 bits long 1Eh (R/W) = The MCSPI word is 31 bits long 1Fh (R/W) = The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0h (R/W) = SPIEN is held high during the ACTIVE state. 1h (R/W) = SPIEN is held low during the ACTIVE state.

Table 5-29. MCSPI_CHCONF_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-2	CLKD	R/W	0h	<p>Frequency divider for SPICLK (only when the module is a Master MCSPI device). A programmable clock divider divides the MCSPI reference clock (SPICLKREF) with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data. By default the clock divider ratio has a power of 2 granularity when MCSPI_CHCONF_0/1/2/3[29] CLKG is cleared. Otherwise this field is the 4-LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL_0/1/2/3[15-8] EXTCLK register. The value description below defines the clock ratio when MCSPI_CHCONF_0/1/2/3[29] CLKG is set to 0.</p> <p>0h (R/W) = 1 1h (R/W) = 2 2h (R/W) = 4 3h (R/W) = 8 4h (R/W) = 16 5h (R/W) = 32 6h (R/W) = 64 7h (R/W) = 128 8h (R/W) = 256 9h (R/W) = 512 Ah (R/W) = 1024 Bh (R/W) = 2048 Ch (R/W) = 4096 Dh (R/W) = 8192 Eh (R/W) = 16384 Fh (R/W) = 32768</p>
1	POL	R/W	0h	<p>SPICLK polarity (see <i>Transfer Format</i>) 0h (R/W) = SPICLK is held low during the INACTIVE state 1h (R/W) = SPICLK is held high during the INACTIVE state</p>
0	PHA	R/W	0h	<p>SPICLK phase (see <i>Transfer Format</i>) 0h (R/W) = Data are latched on odd-numbered edges of SPICLK. 1h (R/W) = Data are latched on even-numbered edges of SPICLK.</p>

5.13 MCSPI_CHSTAT_0 Register (Offset = 130h) [reset = 0h]

MCSPi_CHSTAT_0 is shown in [Figure 5-13](#) and described in [Table 5-31](#).

Return to [Summary Table](#).

This register provides status information about transmitter and receiver registers of channel i.

Table 5-30. MCSPI_CHSTAT_0 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0130h
MCSPi1_CFG	0211 0130h
MCSPi2_CFG	0212 0130h
MCSPi3_CFG	0213 0130h
MCSPi4_CFG	0214 0130h
MCSPi5_CFG	0215 0130h
MCSPi6_CFG	0216 0130h
MCSPi7_CFG	0217 0130h
MCU_MCSPi0_CFG	4030 0130h
MCU_MCSPi1_CFG	4031 0130h
MCU_MCSPi2_CFG	4032 0130h

Figure 5-13. MCSPI_CHSTAT_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-31. MCSPI_CHSTAT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Read returns 0.
6	RXFFF	R	0h	Channel i FIFO receive buffer full status 0h (R) = FIFO receive buffer is not full 1h (R) = FIFO receive buffer is full
5	RXFFE	R	0h	Channel i FIFO receive buffer empty status 0h (R) = FIFO receive buffer is not empty 1h (R) = FIFO receive buffer is empty
4	TXFFF	R	0h	Channel i FIFO transmit buffer full status 0h (R) = FIFO transmit buffer is not full 1h (R) = FIFO transmit buffer is full

Table 5-31. MCSPI_CHSTAT_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TXFFE	R	0h	Channel i FIFO transmit buffer empty status 0h (R) = FIFO transmit buffer is not empty 1h (R) = FIFO transmit buffer is empty
2	EOT	R	0h	Channel i end of transfer status. The definitions of beginning and end of transfer vary with master versus slave and the transfer format (transmit/receive modes, turbo mode). See dedicated chapters for details. 0h (R) = This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1h (R) = This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel i transmitter register status 0h (R) = Register is full. 1h (R) = Register is empty.
0	RXS	R	0h	Channel i receiver register status 0h (R) = Register is empty. 1h (R) = Register is full.

5.14 MCSPI_CHCTRL_0 Register (Offset = 134h) [reset = 0h]

MCSPI_CHCTRL_0 is shown in [Figure 5-14](#) and described in [Table 5-33](#).

Return to [Summary Table](#).

This register is dedicated to enable channel i.

Table 5-32. MCSPI_CHCTRL_0 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0134h
MCSPi1_CFG	0211 0134h
MCSPi2_CFG	0212 0134h
MCSPi3_CFG	0213 0134h
MCSPi4_CFG	0214 0134h
MCSPi5_CFG	0215 0134h
MCSPi6_CFG	0216 0134h
MCSPi7_CFG	0217 0134h
MCU_MCSPi0_CFG	4030 0134h
MCU_MCSPi1_CFG	4031 0134h
MCU_MCSPi2_CFG	4032 0134h

Figure 5-14. MCSPI_CHCTRL_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W-0h								R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-33. MCSPI_CHCTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Read returns 0.
15-8	EXTCLK	R/W	0h	Clock ratio extension: This field is used to concatenate with MCSPI_CHCONF_0/1/2/3[5-2] CLKD register for clock ratio only when granularity is one clock cycle (MCSPI_CHCONF_0/1/2/3[29] CLKG set to 1). Then the maximum value reached is 4096 clock divider ratio. 0h (R/W) = Clock ratio is CLKD + 1. 1h (R/W) = Clock ratio is CLKD + 1 + 16. FFh (R/W) = Clock ratio is CLKD + 1 + 4080.
7-1	RESERVED	R	0h	Read returns 0.
0	EN	R/W	0h	Channel enable 0h (R/W) = Channel i is not active. 1h (R/W) = Channel i is active.

5.15 MCSPI_TX_0 Register (Offset = 138h) [reset = 0h]

MCSPI_TX_0 is shown in [Figure 5-15](#) and described in [Table 5-35](#).

Return to [Summary Table](#).

This register contains a single MCSPI word for channel i to transmit on the serial link, whatever MCSPI word length is.

Table 5-34. MCSPI_TX_0 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0138h
MCSPi1_CFG	0211 0138h
MCSPi2_CFG	0212 0138h
MCSPi3_CFG	0213 0138h
MCSPi4_CFG	0214 0138h
MCSPi5_CFG	0215 0138h
MCSPi6_CFG	0216 0138h
MCSPi7_CFG	0217 0138h
MCU_MCSPi0_CFG	4030 0138h
MCU_MCSPi1_CFG	4031 0138h
MCU_MCSPi2_CFG	4032 0138h

Figure 5-15. MCSPI_TX_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-35. MCSPI_TX_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDATA	R/W	0h	Channel i data to transmit

5.16 MCSPI_RX_0 Register (Offset = 13Ch) [reset = 0h]

MCSPI_RX_0 is shown in [Figure 5-16](#) and described in [Table 5-37](#).

Return to [Summary Table](#).

This register contains a single MCSPI word for channel i received through the serial link, whatever MCSPI word length is.

Table 5-36. MCSPI_RX_0 Instances

Instance	Physical Address
MCSPi0_CFG	0210 013Ch
MCSPi1_CFG	0211 013Ch
MCSPi2_CFG	0212 013Ch
MCSPi3_CFG	0213 013Ch
MCSPi4_CFG	0214 013Ch
MCSPi5_CFG	0215 013Ch
MCSPi6_CFG	0216 013Ch
MCSPi7_CFG	0217 013Ch
MCU_MCSPi0_CFG	4030 013Ch
MCU_MCSPi1_CFG	4031 013Ch
MCU_MCSPi2_CFG	4032 013Ch

Figure 5-16. MCSPI_RX_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-37. MCSPI_RX_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R	0h	Channel i received data

5.17 MCSPI_CHCONF_1 Register (Offset = 140h) [reset = 00060000h]

MCSPI_CHCONF_1 is shown in [Figure 5-17](#) and described in [Table 5-39](#).

Return to [Summary Table](#).

This register is dedicated to the configuration of the channel i.

Table 5-38. MCSPI_CHCONF_1 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0140h
MCSPi1_CFG	0211 0140h
MCSPi2_CFG	0212 0140h
MCSPi3_CFG	0213 0140h
MCSPi4_CFG	0214 0140h
MCSPi5_CFG	0215 0140h
MCSPi6_CFG	0216 0140h
MCSPi7_CFG	0217 0140h
MCU_MCSPi0_CFG	4030 0140h
MCU_MCSPi1_CFG	4031 0140h
MCU_MCSPi2_CFG	4032 0140h

Figure 5-17. MCSPI_CHCONF_1 Register

31	30	29	28	27	26	25	24
RESERVED		CLKG	FFER	FFEW	TCS0		SBPOL
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
23	22	21	20	19	18	17	16
SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
DMAR	DMAW	TRM		WL			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
WL	EPOL	CLKD				POL	PHA
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-39. MCSPI_CHCONF_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Read returns 0.
29	CLKG	R/W	0h	<p>Clock divider granularity</p> <p>This bit defines the granularity of channel clock divider: power of 2 or one clock cycle granularity.</p> <p>When this bit is set the register MCSPI_CHCTRL_0/1/2/3[15-8] EXTCLK must be configured to reach a maximum of 4096 clock divider ratio.</p> <p>Then the clock divider ratio is a concatenation of MCSPI_CHCONF_0/1/2/3[5-2] CLKD and MCSPI_CHCTRL_0/1/2/3[15-8] EXTCLK values</p> <p>0h (R/W) = Clock granularity of power of 2</p> <p>1h (R/W) = One clock cycle granularity</p>

Table 5-39. MCSPI_CHCONF_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	FFER	R/W	0h	FIFO enabled for receive: Only one channel can have this bit field set. 0h (R/W) = The buffer is not used to receive data. 1h (R/W) = The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for transmit: Only one channel can have this bit field set. 0h (R/W) = The buffer is not used to transmit data. 1h (R/W) = The buffer is used to transmit data.
26-25	TCS0	R/W	0h	Chip-select time control This 2-bit field defines the number of interface clock cycles between CS toggling and first or last edge of MCSPI clock. 0h (R/W) = 0.5 clock cycle 1h (R/W) = 1.5 clock cycles 2h (R/W) = 2.5 clock cycles 3h (R/W) = 3.5 clock cycles
24	SBPOL	R/W	0h	Start-bit polarity 0h (R/W) = Start-bit polarity is held to 0 during MCSPI transfer. 1h (R/W) = Start-bit polarity is held to 1 during MCSPI transfer.
23	SBE	R/W	0h	Start-bit enable for MCSPI transfer 0h (R/W) = Default MCSPI transfer length as specified by WL bit field 1h (R/W) = Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL
22-21	SPIENSLV	R/W	0h	Channel 0 only and slave mode only: MCSPI slave select signal detection. Reserved bits for other cases. 0h (R/W) = Detection enabled only on SPIEN[0] 1h (R/W) = Detection enabled only on SPIEN[1] 2h (R/W) = Detection enabled only on SPIEN[2] 3h (R/W) = Detection enabled only on SPIEN[3]
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between MCSPI words (single channel master mode only). 0h (R/W) = Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1h (R/W) = Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0h (R/W) = Turbo is deactivated (recommended for single MCSPI word transfer). 1h (R/W) = Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0h (R/W) = Data line 0 (SPIDAT[0]) selected for reception 1h (R/W) = Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission enable for data line 1 0h (R/W) = Data line 1 (SPIDAT[1]) selected for transmission 1h (R/W) = No transmission on Data Line1 (SPIDAT[1])

Table 5-39. MCSPI_CHCONF_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	DPE0	R/W	0h	Transmission Enable for data line 0 0h (R/W) = Data Line0 (SPIDAT[0]) selected for transmission 1h (R/W) = No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA read request The DMA read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel. The DMA read request line is deasserted on read completion of the receive register of the channel. 0h (R/W) = DMA read request disabled 1h (R/W) = DMA read request enabled
14	DMAW	R/W	0h	DMA write request. The DMA write request line is asserted when The channel is enabled and the transmitter register of the channel is empty. The DMA write request line is deasserted on load completion of the transmitter register of the channel. 0h (R/W) = DMA write request disabled 1h (R/W) = DMA write request enabled
13-12	TRM	R/W	0h	Transmit/receive modes 0h (R/W) = Transmit-and-receive mode 1h (R/W) = Receive-only mode 2h (R/W) = Transmit-only mode 3h (R/W) = Reserved

Table 5-39. MCSPI_CHCONF_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-7	WL	R/W	0h	SPI word length 0h (R/W) = Reserved 1h (R/W) = Reserved 2h (R/W) = Reserved 3h (R/W) = The MCSPI word is 4 bits long 4h (R/W) = The MCSPI word is 5 bits long 5h (R/W) = The MCSPI word is 6 bits long 6h (R/W) = The MCSPI word is 7 bits long 7h (R/W) = The MCSPI word is 8 bits long 8h (R/W) = The MCSPI word is 9 bits long 9h (R/W) = The MCSPI word is 10 bits long Ah (R/W) = The MCSPI word is 11 bits long Bh (R/W) = The MCSPI word is 12 bits long Ch (R/W) = The MCSPI word is 13 bits long Dh (R/W) = The MCSPI word is 14 bits long Eh (R/W) = The MCSPI word is 15 bits long Fh (R/W) = The MCSPI word is 16 bits long 10h (R/W) = The MCSPI word is 17 bits long 11h (R/W) = The MCSPI word is 18 bits long 12h (R/W) = The MCSPI word is 19 bits long 13h (R/W) = The MCSPI word is 20 bits long 14h (R/W) = The MCSPI word is 21 bits long 15h (R/W) = The MCSPI word is 22 bits long 16h (R/W) = The MCSPI word is 23 bits long 17h (R/W) = The MCSPI word is 24 bits long 18h (R/W) = The MCSPI word is 25 bits long 19h (R/W) = The MCSPI word is 26 bits long 1Ah (R/W) = The MCSPI word is 27 bits long 1Bh (R/W) = The MCSPI word is 28 bits long 1Ch (R/W) = The MCSPI word is 29 bits long 1Dh (R/W) = The MCSPI word is 30 bits long 1Eh (R/W) = The MCSPI word is 31 bits long 1Fh (R/W) = The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0h (R/W) = SPIEN is held high during the ACTIVE state. 1h (R/W) = SPIEN is held low during the ACTIVE state.

Table 5-39. MCSPI_CHCONF_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-2	CLKD	R/W	0h	<p>Frequency divider for SPICLK (only when the module is a Master MCSPI device). A programmable clock divider divides the MCSPI reference clock (SPICLKREF) with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data. By default the clock divider ratio has a power of 2 granularity when MCSPI_CHCONF_0/1/2/3[29] CLKG is cleared. Otherwise this field is the 4-LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL_0/1/2/3[15-8] EXTCLK register. The value description below defines the clock ratio when MCSPI_CHCONF_0/1/2/3[29] CLKG is set to 0.</p> <p>0h (R/W) = 1 1h (R/W) = 2 2h (R/W) = 4 3h (R/W) = 8 4h (R/W) = 16 5h (R/W) = 32 6h (R/W) = 64 7h (R/W) = 128 8h (R/W) = 256 9h (R/W) = 512 Ah (R/W) = 1024 Bh (R/W) = 2048 Ch (R/W) = 4096 Dh (R/W) = 8192 Eh (R/W) = 16384 Fh (R/W) = 32768</p>
1	POL	R/W	0h	<p>SPICLK polarity (see <i>Transfer Format</i>) 0h (R/W) = SPICLK is held low during the INACTIVE state 1h (R/W) = SPICLK is held high during the INACTIVE state</p>
0	PHA	R/W	0h	<p>SPICLK phase (see <i>Transfer Format</i>) 0h (R/W) = Data are latched on odd-numbered edges of SPICLK. 1h (R/W) = Data are latched on even-numbered edges of SPICLK.</p>

5.18 MCSPI_CHSTAT_1 Register (Offset = 144h) [reset = 0h]

MCSPi_CHSTAT_1 is shown in [Figure 5-18](#) and described in [Table 5-41](#).

Return to [Summary Table](#).

This register provides status information about transmitter and receiver registers of channel i.

Table 5-40. MCSPI_CHSTAT_1 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0144h
MCSPi1_CFG	0211 0144h
MCSPi2_CFG	0212 0144h
MCSPi3_CFG	0213 0144h
MCSPi4_CFG	0214 0144h
MCSPi5_CFG	0215 0144h
MCSPi6_CFG	0216 0144h
MCSPi7_CFG	0217 0144h
MCU_MCSPi0_CFG	4030 0144h
MCU_MCSPi1_CFG	4031 0144h
MCU_MCSPi2_CFG	4032 0144h

Figure 5-18. MCSPI_CHSTAT_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-41. MCSPI_CHSTAT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Read returns 0.
6	RXFFF	R	0h	Channel i FIFO receive buffer full status 0h (R) = FIFO receive buffer is not full 1h (R) = FIFO receive buffer is full
5	RXFFE	R	0h	Channel i FIFO receive buffer empty status 0h (R) = FIFO receive buffer is not empty 1h (R) = FIFO receive buffer is empty
4	TXFFF	R	0h	Channel i FIFO transmit buffer full status 0h (R) = FIFO transmit buffer is not full 1h (R) = FIFO transmit buffer is full

Table 5-41. MCSPI_CHSTAT_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TXFFE	R	0h	Channel i FIFO transmit buffer empty status 0h (R) = FIFO transmit buffer is not empty 1h (R) = FIFO transmit buffer is empty
2	EOT	R	0h	Channel i end of transfer status. The definitions of beginning and end of transfer vary with master versus slave and the transfer format (transmit/receive modes, turbo mode). See dedicated chapters for details. 0h (R) = This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1h (R) = This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel i transmitter register status 0h (R) = Register is full. 1h (R) = Register is empty.
0	RXS	R	0h	Channel i receiver register status 0h (R) = Register is empty. 1h (R) = Register is full.

5.19 MCSPI_CHCTRL_1 Register (Offset = 148h) [reset = 0h]

MCSPI_CHCTRL_1 is shown in [Figure 5-19](#) and described in [Table 5-43](#).

Return to [Summary Table](#).

This register is dedicated to enable channel i.

Table 5-42. MCSPI_CHCTRL_1 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0148h
MCSPi1_CFG	0211 0148h
MCSPi2_CFG	0212 0148h
MCSPi3_CFG	0213 0148h
MCSPi4_CFG	0214 0148h
MCSPi5_CFG	0215 0148h
MCSPi6_CFG	0216 0148h
MCSPi7_CFG	0217 0148h
MCU_MCSPi0_CFG	4030 0148h
MCU_MCSPi1_CFG	4031 0148h
MCU_MCSPi2_CFG	4032 0148h

Figure 5-19. MCSPI_CHCTRL_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W-0h								R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-43. MCSPI_CHCTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Read returns 0.
15-8	EXTCLK	R/W	0h	Clock ratio extension: This field is used to concatenate with MCSPI_CHCONF_0/1/2/3[5-2] CLKD register for clock ratio only when granularity is one clock cycle (MCSPI_CHCONF_0/1/2/3[29] CLKG set to 1). Then the maximum value reached is 4096 clock divider ratio. 0h (R/W) = Clock ratio is CLKD + 1. 1h (R/W) = Clock ratio is CLKD + 1 + 16. FFh (R/W) = Clock ratio is CLKD + 1 + 4080.
7-1	RESERVED	R	0h	Read returns 0.
0	EN	R/W	0h	Channel enable 0h (R/W) = Channel "i" is not active. 1h (R/W) = Channel "i" is active.

5.20 MCSPI_TX_1 Register (Offset = 14Ch) [reset = 0h]

MCSPI_TX_1 is shown in [Figure 5-20](#) and described in [Table 5-45](#).

Return to [Summary Table](#).

This register contains a single MCSPI word for channel i to transmit on the serial link, whatever MCSPI word length is.

Table 5-44. MCSPI_TX_1 Instances

Instance	Physical Address
MCSPi0_CFG	0210 014Ch
MCSPi1_CFG	0211 014Ch
MCSPi2_CFG	0212 014Ch
MCSPi3_CFG	0213 014Ch
MCSPi4_CFG	0214 014Ch
MCSPi5_CFG	0215 014Ch
MCSPi6_CFG	0216 014Ch
MCSPi7_CFG	0217 014Ch
MCU_MCSPi0_CFG	4030 014Ch
MCU_MCSPi1_CFG	4031 014Ch
MCU_MCSPi2_CFG	4032 014Ch

Figure 5-20. MCSPI_TX_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA																															
R/W-																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-45. MCSPI_TX_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDATA	R/W	0	Channel i data to transmit

5.21 MCSPI_RX_1 Register (Offset = 150h) [reset = 0h]

MCSPI_RX_1 is shown in [Figure 5-21](#) and described in [Table 5-47](#).

Return to [Summary Table](#).

This register contains a single MCSPI word for channel i received through the serial link, whatever MCSPI word length is.

Table 5-46. MCSPI_RX_1 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0150h
MCSPi1_CFG	0211 0150h
MCSPi2_CFG	0212 0150h
MCSPi3_CFG	0213 0150h
MCSPi4_CFG	0214 0150h
MCSPi5_CFG	0215 0150h
MCSPi6_CFG	0216 0150h
MCSPi7_CFG	0217 0150h
MCU_MCSPi0_CFG	4030 0150h
MCU_MCSPi1_CFG	4031 0150h
MCU_MCSPi2_CFG	4032 0150h

Figure 5-21. MCSPI_RX_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															
R-																															

LEGEND: R = Read Only; -n = value after reset

Table 5-47. MCSPI_RX_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R	0	Channel i received data

5.22 MCSPI_CHCONF_2 Register (Offset = 154h) [reset = 00060000h]

MCSPI_CHCONF_2 is shown in [Figure 5-22](#) and described in [Table 5-49](#).

Return to [Summary Table](#).

This register is dedicated to the configuration of the channel i

Table 5-48. MCSPI_CHCONF_2 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0154h
MCSPi1_CFG	0211 0154h
MCSPi2_CFG	0212 0154h
MCSPi3_CFG	0213 0154h
MCSPi4_CFG	0214 0154h
MCSPi5_CFG	0215 0154h
MCSPi6_CFG	0216 0154h
MCSPi7_CFG	0217 0154h
MCU_MCSPi0_CFG	4030 0154h
MCU_MCSPi1_CFG	4031 0154h
MCU_MCSPi2_CFG	4032 0154h

Figure 5-22. MCSPI_CHCONF_2 Register

31	30	29	28	27	26	25	24
RESERVED		CLKG	FFER	FFEW	TCS0		SBPOL
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
23	22	21	20	19	18	17	16
SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
DMAR	DMAW	TRM		WL			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
WL	EPOL	CLKD				POL	PHA
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-49. MCSPI_CHCONF_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Read returns 0.
29	CLKG	R/W	0h	<p>Clock divider granularity</p> <p>This bit defines the granularity of channel clock divider: power of 2 or one clock cycle granularity.</p> <p>When this bit is set the register MCSPI_CHCTRL_2[15-8] EXTCLK must be configured to reach a maximum of 4096 clock divider ratio. Then the clock divider ratio is a concatenation of MCSPI_CHCONF_2[5-2] CLKD and MCSPI_CHCTRL_2[15-8] EXTCLK values</p> <p>0h (R/W) = Clock granularity of power of 2</p> <p>1h (R/W) = One clock cycle granularity</p>

Table 5-49. MCSPI_CHCONF_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	FFER	R/W	0h	FIFO enabled for receive: Only one channel can have this bit field set. 0h (R/W) = The buffer is not used to receive data. 1h (R/W) = The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for transmit: Only one channel can have this bit field set. 0h (R/W) = The buffer is not used to transmit data. 1h (R/W) = The buffer is used to transmit data.
26-25	TCS0	R/W	0h	Chip-select time control This 2-bit field defines the number of interface clock cycles between CS toggling and first or last edge of MCSPI clock. 0h (R/W) = 0.5 clock cycle 1h (R/W) = 1.5 clock cycles 2h (R/W) = 2.5 clock cycles 3h (R/W) = 3.5 clock cycles
24	SBPOL	R/W	0h	Start-bit polarity 0h (R/W) = Start-bit polarity is held to 0 during MCSPI transfer. 1h (R/W) = Start-bit polarity is held to 1 during MCSPI transfer.
23	SBE	R/W	0h	Start-bit enable for MCSPI transfer 0h (R/W) = Default MCSPI transfer length as specified by WL bit field 1h (R/W) = Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_2[24] SBPOL
22-21	SPIENSLV	R/W	0h	Channel 0 only and slave mode only: MCSPI slave select signal detection. Reserved bits for other cases. 0h (R/W) = Detection enabled only on SPIEN[0] 1h (R/W) = Detection enabled only on SPIEN[1] 2h (R/W) = Detection enabled only on SPIEN[2] 3h (R/W) = Detection enabled only on SPIEN[3]
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between MCSPI words (single channel master mode only). 0h (R/W) = Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1h (R/W) = Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0h (R/W) = Turbo is deactivated (recommended for single MCSPI word transfer). 1h (R/W) = Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0h (R/W) = Data line 0 (SPIDAT[0]) selected for reception 1h (R/W) = Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission enable for data line 1 0h (R/W) = Data line 1 (SPIDAT[1]) selected for transmission 1h (R/W) = No transmission on Data Line1 (SPIDAT[1])

Table 5-49. MCSPI_CHCONF_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	DPE0	R/W	0h	Transmission Enable for data line 0 0h (R/W) = Data Line0 (SPIDAT[0]) selected for transmission 1h (R/W) = No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA read request The DMA read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel. The DMA read request line is deasserted on read completion of the receive register of the channel. 0h (R/W) = DMA read request disabled 1h (R/W) = DMA read request enabled
14	DMAW	R/W	0h	DMA write request. The DMA write request line is asserted when The channel is enabled and the transmitter register of the channel is empty. The DMA write request line is deasserted on load completion of the transmitter register of the channel. 0h (R/W) = DMA write request disabled 1h (R/W) = DMA write request enabled
13-12	TRM	R/W	0h	Transmit/receive modes 0h (R/W) = Transmit-and-receive mode 1h (R/W) = Receive-only mode 2h (R/W) = Transmit-only mode 3h (R/W) = Reserved

Table 5-49. MCSPI_CHCONF_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-7	WL	R/W	0h	SPI word length 0h (R/W) = Reserved 1h (R/W) = Reserved 2h (R/W) = Reserved 3h (R/W) = The MCSPI word is 4 bits long 4h (R/W) = The MCSPI word is 5 bits long 5h (R/W) = The MCSPI word is 6 bits long 6h (R/W) = The MCSPI word is 7 bits long 7h (R/W) = The MCSPI word is 8 bits long 8h (R/W) = The MCSPI word is 9 bits long 9h (R/W) = The MCSPI word is 10 bits long Ah (R/W) = The MCSPI word is 11 bits long Bh (R/W) = The MCSPI word is 12 bits long Ch (R/W) = The MCSPI word is 13 bits long Dh (R/W) = The MCSPI word is 14 bits long Eh (R/W) = The MCSPI word is 15 bits long Fh (R/W) = The MCSPI word is 16 bits long 10h (R/W) = The MCSPI word is 17 bits long 11h (R/W) = The MCSPI word is 18 bits long 12h (R/W) = The MCSPI word is 19 bits long 13h (R/W) = The MCSPI word is 20 bits long 14h (R/W) = The MCSPI word is 21 bits long 15h (R/W) = The MCSPI word is 22 bits long 16h (R/W) = The MCSPI word is 23 bits long 17h (R/W) = The MCSPI word is 24 bits long 18h (R/W) = The MCSPI word is 25 bits long 19h (R/W) = The MCSPI word is 26 bits long 1Ah (R/W) = The MCSPI word is 27 bits long 1Bh (R/W) = The MCSPI word is 28 bits long 1Ch (R/W) = The MCSPI word is 29 bits long 1Dh (R/W) = The MCSPI word is 30 bits long 1Eh (R/W) = The MCSPI word is 31 bits long 1Fh (R/W) = The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0h (R/W) = SPIEN is held high during the ACTIVE state. 1h (R/W) = SPIEN is held low during the ACTIVE state.

Table 5-49. MCSPI_CHCONF_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-2	CLKD	R/W	0h	<p>Frequency divider for SPICLK (only when the module is a Master MCSPI device). A programmable clock divider divides the MCSPI reference clock (SPICLKREF) with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data. By default the clock divider ratio has a power of 2 granularity when MCSPI_CHCONF_2[29] CLKG is cleared. Otherwise this field is the 4-LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL_2[15-8] EXTCLK register. The value description below defines the clock ratio when MCSPI_CHCONF_2[29] CLKG is set to 0.</p> <p>0h (R/W) = 1 1h (R/W) = 2 2h (R/W) = 4 3h (R/W) = 8 4h (R/W) = 16 5h (R/W) = 32 6h (R/W) = 64 7h (R/W) = 128 8h (R/W) = 256 9h (R/W) = 512 Ah (R/W) = 1024 Bh (R/W) = 2048 Ch (R/W) = 4096 Dh (R/W) = 8192 Eh (R/W) = 16384 Fh (R/W) = 32768</p>
1	POL	R/W	0h	<p>SPICLK polarity (see <i>Transfer Format</i>)</p> <p>0h (R/W) = SPICLK is held low during the INACTIVE state 1h (R/W) = SPICLK is held high during the INACTIVE state</p>
0	PHA	R/W	0h	<p>SPICLK phase (see <i>Transfer Format</i>)</p> <p>0h (R/W) = Data are latched on odd-numbered edges of SPICLK. 1h (R/W) = Data are latched on even-numbered edges of SPICLK.</p>

5.23 MCSPI_CHSTAT_2 Register (Offset = 158h) [reset = 0h]

MCSPi_CHSTAT_2 is shown in [Figure 5-23](#) and described in [Table 5-51](#).

Return to [Summary Table](#).

This register provides status information about transmitter and receiver registers of channel i.

Table 5-50. MCSPI_CHSTAT_2 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0158h
MCSPi1_CFG	0211 0158h
MCSPi2_CFG	0212 0158h
MCSPi3_CFG	0213 0158h
MCSPi4_CFG	0214 0158h
MCSPi5_CFG	0215 0158h
MCSPi6_CFG	0216 0158h
MCSPi7_CFG	0217 0158h
MCU_MCSPi0_CFG	4030 0158h
MCU_MCSPi1_CFG	4031 0158h
MCU_MCSPi2_CFG	4032 0158h

Figure 5-23. MCSPI_CHSTAT_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-51. MCSPI_CHSTAT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Read returns 0.
6	RXFFF	R	0h	Channel i FIFO receive buffer full status 0h (R) = FIFO receive buffer is not full 1h (R) = FIFO receive buffer is full
5	RXFFE	R	0h	Channel i FIFO receive buffer empty status 0h (R) = FIFO receive buffer is not empty 1h (R) = FIFO receive buffer is empty
4	TXFFF	R	0h	Channel i FIFO transmit buffer full status 0h (R) = FIFO transmit buffer is not full 1h (R) = FIFO transmit buffer is full

Table 5-51. MCSPI_CHSTAT_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TXFFE	R	0h	Channel i FIFO transmit buffer empty status 0h (R) = FIFO transmit buffer is not empty 1h (R) = FIFO transmit buffer is empty
2	EOT	R	0h	Channel i end of transfer status. The definitions of beginning and end of transfer vary with master versus slave and the transfer format (transmit/receive modes, turbo mode). See dedicated chapters for details. 0h (R) = This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1h (R) = This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel i transmitter register status 0h (R) = Register is full. 1h (R) = Register is empty.
0	RXS	R	0h	Channel i receiver register status 0h (R) = Register is empty. 1h (R) = Register is full.

5.24 MCSPI_CHCTRL_2 Register (Offset = 15Ch) [reset = 0h]

MCSPi_CHCTRL_2 is shown in [Figure 5-24](#) and described in [Table 5-53](#).

Return to [Summary Table](#).

This register is dedicated to enable channel i.

Table 5-52. MCSPI_CHCTRL_2 Instances

Instance	Physical Address
MCSPi0_CFG	0210 015Ch
MCSPi1_CFG	0211 015Ch
MCSPi2_CFG	0212 015Ch
MCSPi3_CFG	0213 015Ch
MCSPi4_CFG	0214 015Ch
MCSPi5_CFG	0215 015Ch
MCSPi6_CFG	0216 015Ch
MCSPi7_CFG	0217 015Ch
MCU_MCSPi0_CFG	4030 015Ch
MCU_MCSPi1_CFG	4031 015Ch
MCU_MCSPi2_CFG	4032 015Ch

Figure 5-24. MCSPI_CHCTRL_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W-0h								R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-53. MCSPI_CHCTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Read returns 0.
15-8	EXTCLK	R/W	0h	Clock ratio extension: This field is used to concatenate with MCSPI_CHCONF_0/1/2/3[5-2] CLKD register for clock ratio only when granularity is one clock cycle (MCSPi_CHCONF_0/1/2/3[29] CLKG set to 1). Then the maximum value reached is 4096 clock divider ratio. 0h (R/W) = Clock ratio is CLKD + 1. 1h (R/W) = Clock ratio is CLKD + 1 + 16. FFh (R/W) = Clock ratio is CLKD + 1 + 4080.
7-1	RESERVED	R	0h	Read returns 0.
0	EN	R/W	0h	Channel enable 0h (R/W) = Channel i is not active. 1h (R/W) = Channel i is active.

5.25 MCSPI_TX_2 Register (Offset = 160h) [reset = 0h]

MCSPI_TX_2 is shown in [Figure 5-25](#) and described in [Table 5-55](#).

Return to [Summary Table](#).

This register contains a single MCSPI word for channel i to transmit on the serial link, whatever MCSPI word length is.

Table 5-54. MCSPI_TX_2 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0160h
MCSPi1_CFG	0211 0160h
MCSPi2_CFG	0212 0160h
MCSPi3_CFG	0213 0160h
MCSPi4_CFG	0214 0160h
MCSPi5_CFG	0215 0160h
MCSPi6_CFG	0216 0160h
MCSPi7_CFG	0217 0160h
MCU_MCSPi0_CFG	4030 0160h
MCU_MCSPi1_CFG	4031 0160h
MCU_MCSPi2_CFG	4032 0160h

Figure 5-25. MCSPI_TX_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-55. MCSPI_TX_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDATA	R/W	0h	Channel i data to transmit

5.26 MCSPI_RX_2 Register (Offset = 164h) [reset = 0h]

MCSPi_RX_2 is shown in [Figure 5-26](#) and described in [Table 5-57](#).

Return to [Summary Table](#).

This register contains a single MCSPI word for channel i received through the serial link, whatever MCSPI word length is.

Table 5-56. MCSPI_RX_2 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0164h
MCSPi1_CFG	0211 0164h
MCSPi2_CFG	0212 0164h
MCSPi3_CFG	0213 0164h
MCSPi4_CFG	0214 0164h
MCSPi5_CFG	0215 0164h
MCSPi6_CFG	0216 0164h
MCSPi7_CFG	0217 0164h
MCU_MCSPi0_CFG	4030 0164h
MCU_MCSPi1_CFG	4031 0164h
MCU_MCSPi2_CFG	4032 0164h

Figure 5-26. MCSPI_RX_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-57. MCSPI_RX_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R	0h	Channel i received data

5.27 MCSPI_CHCONF_3 Register (Offset = 168h) [reset = 00060000h]

MCSPI_CHCONF_3 is shown in [Figure 5-27](#) and described in [Table 5-59](#).

Return to [Summary Table](#).

This register is dedicated to the configuration of the channel i

Table 5-58. MCSPI_CHCONF_3 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0168h
MCSPi1_CFG	0211 0168h
MCSPi2_CFG	0212 0168h
MCSPi3_CFG	0213 0168h
MCSPi4_CFG	0214 0168h
MCSPi5_CFG	0215 0168h
MCSPi6_CFG	0216 0168h
MCSPi7_CFG	0217 0168h
MCU_MCSPi0_CFG	4030 0168h
MCU_MCSPi1_CFG	4031 0168h
MCU_MCSPi2_CFG	4032 0168h

Figure 5-27. MCSPI_CHCONF_3 Register

31	30	29	28	27	26	25	24
RESERVED		CLKG	FFER	FFEW	TCS0		SBPOL
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h
23	22	21	20	19	18	17	16
SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
DMAR	DMAW	TRM		WL			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
WL	EPOL	CLKD				POL	PHA
R/W-0h	R/W-0h	R/W-0h				R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-59. MCSPI_CHCONF_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Read returns 0.
29	CLKG	R/W	0h	<p>Clock divider granularity</p> <p>This bit defines the granularity of channel clock divider: power of 2 or one clock cycle granularity.</p> <p>When this bit is set the register MCSPI_CHCTRL_3[15-8] EXTCLK must be configured to reach a maximum of 4096 clock divider ratio. Then the clock divider ratio is a concatenation of MCSPI_CHCONF_3[5-2] CLKD and MCSPI_CHCTRL_3[15-8] EXTCLK values</p> <p>0h (R/W) = Clock granularity of power of 2</p> <p>1h (R/W) = One clock cycle granularity</p>

Table 5-59. MCSPI_CHCONF_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	FFER	R/W	0h	FIFO enabled for receive: Only one channel can have this bit field set. 0h (R/W) = The buffer is not used to receive data. 1h (R/W) = The buffer is used to receive data.
27	FFEW	R/W	0h	FIFO enabled for transmit: Only one channel can have this bit field set. 0h (R/W) = The buffer is not used to transmit data. 1h (R/W) = The buffer is used to transmit data.
26-25	TCS0	R/W	0h	Chip-select time control This 2-bit field defines the number of interface clock cycles between CS toggling and first or last edge of MCSPI clock. 0h (R/W) = 0.5 clock cycle 1h (R/W) = 1.5 clock cycles 2h (R/W) = 2.5 clock cycles 3h (R/W) = 3.5 clock cycles
24	SBPOL	R/W	0h	Start-bit polarity 0h (R/W) = Start-bit polarity is held to 0 during MCSPI transfer. 1h (R/W) = Start-bit polarity is held to 1 during MCSPI transfer.
23	SBE	R/W	0h	Start-bit enable for MCSPI transfer 0h (R/W) = Default MCSPI transfer length as specified by WL bit field 1h (R/W) = Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_3[24] SBPOL
22-21	SPIENSLV	R/W	0h	Channel 0 only and slave mode only: MCSPI slave select signal detection. Reserved bits for other cases. 0h (R/W) = Detection enabled only on SPIEN[0] 1h (R/W) = Detection enabled only on SPIEN[1] 2h (R/W) = Detection enabled only on SPIEN[2] 3h (R/W) = Detection enabled only on SPIEN[3]
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between MCSPI words (single channel master mode only). 0h (R/W) = Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it high when MCSPI_CHCONF_0/1/2/3[6] EPOL=1. 1h (R/W) = Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0/1/2/3[6] EPOL=0, and drives it low when MCSPI_CHCONF_0/1/2/3[6] EPOL=1.
19	TURBO	R/W	0h	Turbo mode 0h (R/W) = Turbo is deactivated (recommended for single MCSPI word transfer). 1h (R/W) = Turbo is activated to maximize the throughput for multiple MCSPI words transfer.
18	IS	R/W	1h	Input Select 0h (R/W) = Data line 0 (SPIDAT[0]) selected for reception 1h (R/W) = Data line 1 (SPIDAT[1]) selected for reception
17	DPE1	R/W	1h	Transmission enable for data line 1 0h (R/W) = Data line 1 (SPIDAT[1]) selected for transmission 1h (R/W) = No transmission on Data Line1 (SPIDAT[1])

Table 5-59. MCSPI_CHCONF_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	DPE0	R/W	0h	Transmission Enable for data line 0 0h (R/W) = Data Line0 (SPIDAT[0]) selected for transmission 1h (R/W) = No transmission on data line 0 (SPIDAT[0])
15	DMAR	R/W	0h	DMA read request The DMA read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel. The DMA read request line is deasserted on read completion of the receive register of the channel. 0h (R/W) = DMA read request disabled 1h (R/W) = DMA read request enabled
14	DMAW	R/W	0h	DMA write request. The DMA write request line is asserted when The channel is enabled and the transmitter register of the channel is empty. The DMA write request line is deasserted on load completion of the transmitter register of the channel. 0h (R/W) = DMA write request disabled 1h (R/W) = DMA write request enabled
13-12	TRM	R/W	0h	Transmit/receive modes 0h (R/W) = Transmit-and-receive mode 1h (R/W) = Receive-only mode 2h (R/W) = Transmit-only mode 3h (R/W) = Reserved

Table 5-59. MCSPI_CHCONF_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-7	WL	R/W	0h	SPI word length 0h (R/W) = Reserved 1h (R/W) = Reserved 2h (R/W) = Reserved 3h (R/W) = The MCSPI word is 4 bits long 4h (R/W) = The MCSPI word is 5 bits long 5h (R/W) = The MCSPI word is 6 bits long 6h (R/W) = The MCSPI word is 7 bits long 7h (R/W) = The MCSPI word is 8 bits long 8h (R/W) = The MCSPI word is 9 bits long 9h (R/W) = The MCSPI word is 10 bits long Ah (R/W) = The MCSPI word is 11 bits long Bh (R/W) = The MCSPI word is 12 bits long Ch (R/W) = The MCSPI word is 13 bits long Dh (R/W) = The MCSPI word is 14 bits long Eh (R/W) = The MCSPI word is 15 bits long Fh (R/W) = The MCSPI word is 16 bits long 10h (R/W) = The MCSPI word is 17 bits long 11h (R/W) = The MCSPI word is 18 bits long 12h (R/W) = The MCSPI word is 19 bits long 13h (R/W) = The MCSPI word is 20 bits long 14h (R/W) = The MCSPI word is 21 bits long 15h (R/W) = The MCSPI word is 22 bits long 16h (R/W) = The MCSPI word is 23 bits long 17h (R/W) = The MCSPI word is 24 bits long 18h (R/W) = The MCSPI word is 25 bits long 19h (R/W) = The MCSPI word is 26 bits long 1Ah (R/W) = The MCSPI word is 27 bits long 1Bh (R/W) = The MCSPI word is 28 bits long 1Ch (R/W) = The MCSPI word is 29 bits long 1Dh (R/W) = The MCSPI word is 30 bits long 1Eh (R/W) = The MCSPI word is 31 bits long 1Fh (R/W) = The MCSPI word is 32 bits long
6	EPOL	R/W	0h	SPIEN polarity 0h (R/W) = SPIEN is held high during the ACTIVE state. 1h (R/W) = SPIEN is held low during the ACTIVE state.

Table 5-59. MCSPI_CHCONF_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-2	CLKD	R/W	0h	<p>Frequency divider for SPICLK (only when the module is a Master MCSPI device). A programmable clock divider divides the MCSPI reference clock (SPICLKREF) with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data. By default the clock divider ratio has a power of 2 granularity when MCSPI_CHCONF_0/1/2/3[29] CLKG is cleared. Otherwise this field is the 4-LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL_3[15-8] EXTCLK register. The value description below defines the clock ratio when MCSPI_CHCONF_3[29] CLKG is set to 0.</p> <p>0h (R/W) = 1 1h (R/W) = 2 2h (R/W) = 4 3h (R/W) = 8 4h (R/W) = 16 5h (R/W) = 32 6h (R/W) = 64 7h (R/W) = 128 8h (R/W) = 256 9h (R/W) = 512 Ah (R/W) = 1024 Bh (R/W) = 2048 Ch (R/W) = 4096 Dh (R/W) = 8192 Eh (R/W) = 16384 Fh (R/W) = 32768</p>
1	POL	R/W	0h	<p>SPICLK polarity (see <i>Transfer Format</i>) 0h (R/W) = SPICLK is held low during the INACTIVE state 1h (R/W) = SPICLK is held high during the INACTIVE state</p>
0	PHA	R/W	0h	<p>SPICLK phase (see <i>Transfer Format</i>) 0h (R/W) = Data are latched on odd-numbered edges of SPICLK. 1h (R/W) = Data are latched on even-numbered edges of SPICLK.</p>

5.28 MCSPI_CHSTAT_3 Register (Offset = 16Ch) [reset = 0h]

MCSPi_CHSTAT_3 is shown in [Figure 5-28](#) and described in [Table 5-61](#).

Return to [Summary Table](#).

This register provides status information about transmitter and receiver registers of channel i.

Table 5-60. MCSPI_CHSTAT_3 Instances

Instance	Physical Address
MCSPi0_CFG	0210 016Ch
MCSPi1_CFG	0211 016Ch
MCSPi2_CFG	0212 016Ch
MCSPi3_CFG	0213 016Ch
MCSPi4_CFG	0214 016Ch
MCSPi5_CFG	0215 016Ch
MCSPi6_CFG	0216 016Ch
MCSPi7_CFG	0217 016Ch
MCU_MCSPi0_CFG	4030 016Ch
MCU_MCSPi1_CFG	4031 016Ch
MCU_MCSPi2_CFG	4032 016Ch

Figure 5-28. MCSPI_CHSTAT_3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-61. MCSPI_CHSTAT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Read returns 0.
6	RXFFF	R	0h	Channel i FIFO receive buffer full status 0h (R) = FIFO receive buffer is not full 1h (R) = FIFO receive buffer is full
5	RXFFE	R	0h	Channel i FIFO receive buffer empty status 0h (R) = FIFO receive buffer is not empty 1h (R) = FIFO receive buffer is empty
4	TXFFF	R	0h	Channel i FIFO transmit buffer full status 0h (R) = FIFO transmit buffer is not full 1h (R) = FIFO transmit buffer is full

Table 5-61. MCSPI_CHSTAT_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TXFFE	R	0h	Channel i FIFO transmit buffer empty status 0h (R) = FIFO transmit buffer is not empty 1h (R) = FIFO transmit buffer is empty
2	EOT	R	0h	Channel i end of transfer status. The definitions of beginning and end of transfer vary with master versus slave and the transfer format (transmit/receive modes, turbo mode). See dedicated chapters for details. 0h (R) = This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer). 1h (R) = This flag is automatically set to one at the end of an MCSPI transfer.
1	TXS	R	0h	Channel i transmitter register status 0h (R) = Register is full. 1h (R) = Register is empty.
0	RXS	R	0h	Channel i receiver register status 0h (R) = Register is empty. 1h (R) = Register is full.

5.29 MCSPI_CHCTRL_3 Register (Offset = 170h) [reset = 0h]

MCSPI_CHCTRL_3 is shown in [Figure 5-29](#) and described in [Table 5-63](#).

Return to [Summary Table](#).

This register is dedicated to enable channel i.

Table 5-62. MCSPI_CHCTRL_3 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0170h
MCSPi1_CFG	0211 0170h
MCSPi2_CFG	0212 0170h
MCSPi3_CFG	0213 0170h
MCSPi4_CFG	0214 0170h
MCSPi5_CFG	0215 0170h
MCSPi6_CFG	0216 0170h
MCSPi7_CFG	0217 0170h
MCU_MCSPi0_CFG	4030 0170h
MCU_MCSPi1_CFG	4031 0170h
MCU_MCSPi2_CFG	4032 0170h

Figure 5-29. MCSPI_CHCTRL_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W-0h								R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-63. MCSPI_CHCTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Read returns 0.
15-8	EXTCLK	R/W	0h	Clock ratio extension: This field is used to concatenate with MCSPI_CHCONF_0/1/2/3[5-2] CLKD register for clock ratio only when granularity is one clock cycle (MCSPI_CHCONF_0/1/2/3[29] CLKG set to 1). Then the maximum value reached is 4096 clock divider ratio. 0h (R/W) = Clock ratio is CLKD + 1. 1h (R/W) = Clock ratio is CLKD + 1 + 16. FFh (R/W) = Clock ratio is CLKD + 1 + 4080.
7-1	RESERVED	R	0h	Read returns 0.
0	EN	R/W	0h	Channel enable 0h (R/W) = Channel "i" is not active. 1h (R/W) = Channel "i" is active.

5.30 MCSPI_TX_3 Register (Offset = 174h) [reset = 0h]

MCSPI_TX_3 is shown in [Figure 5-30](#) and described in [Table 5-65](#).

Return to [Summary Table](#).

This register contains a single MCSPI word for channel i to transmit on the serial link, whatever MCSPI word length is.

Table 5-64. MCSPI_TX_3 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0174h
MCSPi1_CFG	0211 0174h
MCSPi2_CFG	0212 0174h
MCSPi3_CFG	0213 0174h
MCSPi4_CFG	0214 0174h
MCSPi5_CFG	0215 0174h
MCSPi6_CFG	0216 0174h
MCSPi7_CFG	0217 0174h
MCU_MCSPi0_CFG	4030 0174h
MCU_MCSPi1_CFG	4031 0174h
MCU_MCSPi2_CFG	4032 0174h

Figure 5-30. MCSPI_TX_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-65. MCSPI_TX_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDATA	R/W	0h	Channel i data to transmit

5.31 MCSPI_RX_3 Register (Offset = 178h) [reset = 0h]

MCSPI_RX_3 is shown in [Figure 5-31](#) and described in [Table 5-67](#).

Return to [Summary Table](#).

This register contains a single MCSPI word for channel i received through the serial link, whatever MCSPI word length is.

Table 5-66. MCSPI_RX_3 Instances

Instance	Physical Address
MCSPi0_CFG	0210 0178h
MCSPi1_CFG	0211 0178h
MCSPi2_CFG	0212 0178h
MCSPi3_CFG	0213 0178h
MCSPi4_CFG	0214 0178h
MCSPi5_CFG	0215 0178h
MCSPi6_CFG	0216 0178h
MCSPi7_CFG	0217 0178h
MCU_MCSPi0_CFG	4030 0178h
MCU_MCSPi1_CFG	4031 0178h
MCU_MCSPi2_CFG	4032 0178h

Figure 5-31. MCSPI_RX_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-67. MCSPI_RX_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R	0h	Channel i received data

5.32 MCSPI_XFERLEVEL Register (Offset = 17Ch) [reset = 0h]

MCSPI_XFERLEVEL is shown in [Figure 5-32](#) and described in [Table 5-69](#).

Return to [Summary Table](#).

This register provides transfer levels needed while using FIFO buffer during transfer.

Table 5-68. MCSPI_XFERLEVEL Instances

Instance	Physical Address
MCSPi0_CFG	0210 017Ch
MCSPi1_CFG	0211 017Ch
MCSPi2_CFG	0212 017Ch
MCSPi3_CFG	0213 017Ch
MCSPi4_CFG	0214 017Ch
MCSPi5_CFG	0215 017Ch
MCSPi6_CFG	0216 017Ch
MCSPi7_CFG	0217 017Ch
MCU_MCSPi0_CFG	4030 017Ch
MCU_MCSPi1_CFG	4031 017Ch
MCU_MCSPi2_CFG	4032 017Ch

Figure 5-32. MCSPI_XFERLEVEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WCNT																AFL								AEL							
R/W-0h																R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-69. MCSPI_XFERLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WCNT	R/W	0h	<p>SPI word counter.</p> <p>This field holds the programmable value of number of MCSPI word to be transferred on channel which is using the FIFO buffer. When transfer had started, a read back in this field returns the current MCSPI word transfer index.</p> <p>0h (R/W) = Counter not used</p> <p>1h (R/W) = One word</p> <p>FFFEh (R/W) = 65534 MCSPI word</p> <p>FFFFh (R/W) = 65535 MCSPI word</p>
15-8	AFL	R/W	0h	<p>Buffer almost full</p> <p>This field holds the programmable almost full level value used to determine almost full buffer condition. If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_XFERLEVEL[15-8] AFL must be set with n-1. The size of this field is defined by the generic parameter FFBYTE.</p> <p>0h (R/W) = 1 byte</p> <p>1h (R/W) = 2 bytes</p> <p>FEh (R/W) = 255bytes</p> <p>FFh (R/W) = 256bytes</p>

Table 5-69. MCSPI_XFERLEVEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	AEL	R/W	0h	<p>Buffer almost empty.</p> <p>This field holds the programmable almost empty level value used to determine almost empty buffer condition. If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_XFERLEVEL[7-0] AEL must be set with – 1.</p> <p>0h (R/W) = 1 byte 1h (R/W) = 2 bytes FEh (R/W) = 255 bytes FFh (R/W) = 256bytes</p>

5.33 MCSPI_DAFTX Register (Offset = 180h) [reset = 0h]

MCSPI_DAFTX is shown in [Figure 5-33](#) and described in [Table 5-71](#).

Return to [Summary Table](#).

This register contains the MCSPI words to be transmitted on the MCSPI bus when FIFO is used and DMA address is aligned on 256 bit.

This register is an image of one of the MCSPI_TX registers corresponding to the channel which has its FIFO enabled.

Table 5-70. MCSPI_DAFTX Instances

Instance	Physical Address
MCSPi0_CFG	0210 0180h
MCSPi1_CFG	0211 0180h
MCSPi2_CFG	0212 0180h
MCSPi3_CFG	0213 0180h
MCSPi4_CFG	0214 0180h
MCSPi5_CFG	0215 0180h
MCSPi6_CFG	0216 0180h
MCSPi7_CFG	0217 0180h
MCU_MCSPi0_CFG	4030 0180h
MCU_MCSPi1_CFG	4031 0180h
MCU_MCSPi2_CFG	4032 0180h

Figure 5-33. MCSPI_DAFTX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAFTDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-71. MCSPI_DAFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DAFTDATA	R/W	0h	FIFO data to transmit with DMA 256 bit aligned address. This field is only used when MCSPI_MODULCTRL[8] FDAA is set to 1h and only one of the enabled channels has the MCSPI_CHCONF_0/1/2/3[27] FFEW bit set to 1h. If these conditions are not met any access to this field returns a null value.

5.34 MCSPI_DAFRX Register (Offset = 1A0h) [reset = 0h]

MCSPI_DAFRX is shown in [Figure 5-34](#) and described in [Table 5-73](#).

Return to [Summary Table](#).

This register contains the MCSPI words received from the MCSPI bus when FIFO is used and DMA address is aligned on 256 bit.

This register is an image of one of the MCSPI_RX registers corresponding to the channel which has its FIFO enabled.

Table 5-72. MCSPI_DAFRX Instances

Instance	Physical Address
MCSPI0_CFG	0210 01A0h
MCSPI1_CFG	0211 01A0h
MCSPI2_CFG	0212 01A0h
MCSPI3_CFG	0213 01A0h
MCSPI4_CFG	0214 01A0h
MCSPI5_CFG	0215 01A0h
MCSPI6_CFG	0216 01A0h
MCSPI7_CFG	0217 01A0h
MCU_MCSPI0_CFG	4030 01A0h
MCU_MCSPI1_CFG	4031 01A0h
MCU_MCSPI2_CFG	4032 01A0h

Figure 5-34. MCSPI_DAFRX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAFRDATA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-73. MCSPI_DAFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DAFRDATA	R	0h	FIFO data received with DMA 256 bit aligned address. This field is only used when MCSPI_MODULCTRL[8] FDAA is set to 1h and only one of the enabled channels has the MCSPI_CHCONF_0/1/2/3[28] FFER bit set to 1h. If these conditions are not met any access to this field returns a null value.

6 UART Registers

Table 6-2 lists the memory-mapped registers for the UART. All register offset addresses not listed in Table 6-2 should be considered as reserved locations and the register contents should not be modified.

Table 6-1. UART Instances

Instance	Base Address
UART0	0280 0000h
UART1	0281 0000h
UART2	0282 0000h
UART3	0283 0000h
UART4	0284 0000h
UART5	0285 0000h
UART6	0286 0000h
UART7	0287 0000h
UART8	0288 0000h
UART9	0289 0000h
UART0	04A0 0000h
WKUP_UART0	4230 0000h

Table 6-2. UART Registers

Offset	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
0h	UART_THR	Transmit holding register	0280 0000h	0281 0000h	0282 0000h
0h	UART_RHR	Receiver holding register	0280 0000h	0281 0000h	0282 0000h
0h	UART_DLL	Baud clock divisor LSB value register	0280 0000h	0281 0000h	0282 0000h
4h	UART_IER_UART	UART mode interrupt enable register	0280 0004h	0281 0004h	0282 0004h
4h	UART_IER_IRDA	IrDA mode interrupt enable register	0280 0004h	0281 0004h	0282 0004h
4h	UART_IER_CIR	CIR mode interrupt enable register	0280 0004h	0281 0004h	0282 0004h
4h	UART_DLH	Baud clock divisor MSB value register	0280 0004h	0281 0004h	0282 0004h
8h	UART_IIR_UART	UART mode interrupt identification register	0280 0008h	0281 0008h	0282 0008h
8h	UART_IIR_IRDA	IrDA mode interrupt identification register	0280 0008h	0281 0008h	0282 0008h
8h	UART_IIR_CIR	CIR mode interrupt identification register	0280 0008h	0281 0008h	0282 0008h
8h	UART_FCR	FIFO control register	0280 0008h	0281 0008h	0282 0008h
8h	UART_EFR	Enhanced feature register	0280 0008h	0281 0008h	0282 0008h
Ch	UART_LCR	Line control register	0280 000Ch	0281 000Ch	0282 000Ch
10h	UART_MCR	Modem control register	0280 0010h	0281 0010h	0282 0010h
10h	UART_XON1_ADDR1	UART mode XON1 character, IrDA mode ADDR1 address register	0280 0010h	0281 0010h	0282 0010h
14h	UART_LSR_UART	UART mode line status register	0280 0014h	0281 0014h	0282 0014h
14h	UART_LSR_IRDA	IrDA mode line status register	0280 0014h	0281 0014h	0282 0014h
14h	UART_LSR_CIR	CIR mode line status register	0280 0014h	0281 0014h	0282 0014h
14h	UART_XON2_ADDR2	UART mode XON2 character, IrDA mode ADDR2 address register	0280 0014h	0281 0014h	0282 0014h
18h	UART_MSR	Modem status register	0280 0018h	0281 0018h	0282 0018h
18h	UART_XOFF1	UART mode XOFF1 character	0280 0018h	0281 0018h	0282 0018h
18h	UART_TCR	Transmission control register	0280 0018h	0281 0018h	0282 0018h
1Ch	UART_SPR	Scratchpad register	0280 001Ch	0281 001Ch	0282 001Ch
1Ch	UART_XOFF2	UART mode XOFF2 character	0280 001Ch	0281 001Ch	0282 001Ch
1Ch	UART_TLR	Trigger level register	0280 001Ch	0281 001Ch	0282 001Ch
20h	UART_MDR1	Mode definition register 1	0280 0020h	0281 0020h	0282 0020h

Table 6-2. UART Registers (continued)

Offset	Acronym	Register Name	UART0 Physical Address	UART1 Physical Address	UART2 Physical Address
24h	UART_MDR2	Mode definition register 2	0280 0024h	0281 0024h	0282 0024h
28h	UART_SFLSR	Status FIFO line status register	0280 0028h	0281 0028h	0282 0028h
28h	UART_TXFL	Transmit frame length register low	0280 0028h	0281 0028h	0282 0028h
2Ch	UART_RESUME	Resume halted operation register	0280 002Ch	0281 002Ch	0282 002Ch
2Ch	UART_TXFLH	Transmit frame length register high	0280 002Ch	0281 002Ch	0282 002Ch
30h	UART_SFREGL	Status FIFO register low	0280 0030h	0281 0030h	0282 0030h
30h	UART_RXFL	Received frame length register low	0280 0030h	0281 0030h	0282 0030h
34h	UART_SFREGH	Status FIFO register high	0280 0034h	0281 0034h	0282 0034h
34h	UART_RXFLH	Received frame length register high	0280 0034h	0281 0034h	0282 0034h
38h	UART_BLR	BOF control register	0280 0038h	0281 0038h	0282 0038h
38h	UART_UASR	UART autobauding status register	0280 0038h	0281 0038h	0282 0038h
3Ch	UART_ACREG	Auxiliary control register	0280 003Ch	0281 003Ch	0282 003Ch
40h	UART_SCR	Supplementary control register	0280 0040h	0281 0040h	0282 0040h
44h	UART_SSR	Supplementary status register	0280 0044h	0281 0044h	0282 0044h
48h	UART_EBLR	BOF length register	0280 0048h	0281 0048h	0282 0048h
50h	UART_MVR	Module version register	0280 0050h	0281 0050h	0282 0050h
54h	UART_SYSC	System configuration register	0280 0054h	0281 0054h	0282 0054h
58h	UART_SYSS	System status register	0280 0058h	0281 0058h	0282 0058h
5Ch	UART_WER	Wake-up enable register	0280 005Ch	0281 005Ch	0282 005Ch
60h	UART_CFPS	Carrier frequency prescaler register	0280 0060h	0281 0060h	0282 0060h
64h	UART_RXFIFO_LVL	RX FIFO level register	0280 0064h	0281 0064h	0282 0064h
68h	UART_TXFIFO_LVL	TX FIFO level register	0280 0068h	0281 0068h	0282 0068h
6Ch	UART_IER2	Interrupt enable register 2	0280 006Ch	0281 006Ch	0282 006Ch
70h	UART_ISR2	Interrupt status register 2	0280 0070h	0281 0070h	0282 0070h
74h	UART_FREQ_SEL	Sample per bit selector register	0280 0074h	0281 0074h	0282 0074h
78h	UART_ABAUD_1ST_CHAR		0280 0078h	0281 0078h	0282 0078h
7Ch	UART_BAUD_2ND_CHAR		0280 007Ch	0281 007Ch	0282 007Ch
80h	UART_MDR3	Mode definition register 3	0280 0080h	0281 0080h	0282 0080h
84h	UART_TX_DMA_THRESHOLD	TX DMA threshold level register	0280 0084h	0281 0084h	0282 0084h
88h	UART_MDR4	Mode definition register 4	0280 0088h	0281 0088h	0282 0088h
8Ch	UART_EFR2	Enhanced features register 2	0280 008Ch	0281 008Ch	0282 008Ch
90h	UART_ECR	Enhanced control register	0280 0090h	0281 0090h	0282 0090h
94h	UART_TIMEGUARD	Timeguard register	0280 0094h	0281 0094h	0282 0094h
98h	UART_TIMEOUTL	Timeout lower byte register	0280 0098h	0281 0098h	0282 0098h
9Ch	UART_TIMEOUTH	Timeout higher byte register	0280 009Ch	0281 009Ch	0282 009Ch
A0h	UART_SCCR	Smartcard mode control register	0280 00A0h	0281 00A0h	0282 00A0h
A4h	UART_ERHR	Extended receive holding register	0280 00A4h	0281 00A4h	0282 00A4h
A4h	UART_ETHR	Extended transmit holding register	0280 00A4h	0281 00A4h	0282 00A4h
A8h	UART_MAR	Multidrop address register	0280 00A8h	0281 00A8h	0282 00A8h
ACH	UART_MMR	Multidrop mask register	0280 00ACH	0281 00ACH	0282 00ACH
B0h	UART_MBR	Multidrop broadcast address register	0280 00B0h	0281 00B0h	0282 00B0h

Table 6-3. UART Registers

Offset	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
0h	UART_THR	Transmit holding register	0283 0000h	0284 0000h	0285 0000h
0h	UART_RHR	Receiver holding register	0283 0000h	0284 0000h	0285 0000h
0h	UART_DLL	Baud clock divisor LSB value register	0283 0000h	0284 0000h	0285 0000h
4h	UART_IER_UART	UART mode interrupt enable register	0283 0004h	0284 0004h	0285 0004h
4h	UART_IER_IRDA	IrDA mode interrupt enable register	0283 0004h	0284 0004h	0285 0004h
4h	UART_IER_CIR	CIR mode interrupt enable register	0283 0004h	0284 0004h	0285 0004h
4h	UART_DLH	Baud clock divisor MSB value register	0283 0004h	0284 0004h	0285 0004h
8h	UART_IIR_UART	UART mode interrupt identification register	0283 0008h	0284 0008h	0285 0008h
8h	UART_IIR_IRDA	IrDA mode interrupt identification register	0283 0008h	0284 0008h	0285 0008h
8h	UART_IIR_CIR	CIR mode interrupt identification register	0283 0008h	0284 0008h	0285 0008h
8h	UART_FCR	FIFO control register	0283 0008h	0284 0008h	0285 0008h
8h	UART_EFR	Enhanced feature register	0283 0008h	0284 0008h	0285 0008h
Ch	UART_LCR	Line control register	0283 000Ch	0284 000Ch	0285 000Ch
10h	UART_MCR	Modem control register	0283 0010h	0284 0010h	0285 0010h
10h	UART_XON1_ADDR1	UART mode XON1 character, IrDA mode ADDR1 address register	0283 0010h	0284 0010h	0285 0010h
14h	UART_LSR_UART	UART mode line status register	0283 0014h	0284 0014h	0285 0014h
14h	UART_LSR_IRDA	IrDA mode line status register	0283 0014h	0284 0014h	0285 0014h
14h	UART_LSR_CIR	CIR mode line status register	0283 0014h	0284 0014h	0285 0014h
14h	UART_XON2_ADDR2	UART mode XON2 character, IrDA mode ADDR2 address register	0283 0014h	0284 0014h	0285 0014h
18h	UART_MSR	Modem status register	0283 0018h	0284 0018h	0285 0018h
18h	UART_XOFF1	UART mode XOFF1 character	0283 0018h	0284 0018h	0285 0018h
18h	UART_TCR	Transmission control register	0283 0018h	0284 0018h	0285 0018h
1Ch	UART_SPR	Scratchpad register	0283 001Ch	0284 001Ch	0285 001Ch
1Ch	UART_XOFF2	UART mode XOFF2 character	0283 001Ch	0284 001Ch	0285 001Ch
1Ch	UART_TLR	Trigger level register	0283 001Ch	0284 001Ch	0285 001Ch
20h	UART_MDR1	Mode definition register 1	0283 0020h	0284 0020h	0285 0020h
24h	UART_MDR2	Mode definition register 2	0283 0024h	0284 0024h	0285 0024h
28h	UART_SFLSR	Status FIFO line status register	0283 0028h	0284 0028h	0285 0028h
28h	UART_TXFLL	Transmit frame length register low	0283 0028h	0284 0028h	0285 0028h
2Ch	UART_RESUME	Resume halted operation register	0283 002Ch	0284 002Ch	0285 002Ch
2Ch	UART_TXFLH	Transmit frame length register high	0283 002Ch	0284 002Ch	0285 002Ch
30h	UART_SFREGL	Status FIFO register low	0283 0030h	0284 0030h	0285 0030h
30h	UART_RXFLL	Received frame length register low	0283 0030h	0284 0030h	0285 0030h
34h	UART_SFREGH	Status FIFO register high	0283 0034h	0284 0034h	0285 0034h
34h	UART_RXFLH	Received frame length register high	0283 0034h	0284 0034h	0285 0034h
38h	UART_BLR	BOF control register	0283 0038h	0284 0038h	0285 0038h
38h	UART_UASR	UART autobauding status register	0283 0038h	0284 0038h	0285 0038h
3Ch	UART_ACREG	Auxiliary control register	0283 003Ch	0284 003Ch	0285 003Ch
40h	UART_SCR	Supplementary control register	0283 0040h	0284 0040h	0285 0040h
44h	UART_SSR	Supplementary status register	0283 0044h	0284 0044h	0285 0044h
48h	UART_EBLR	BOF length register	0283 0048h	0284 0048h	0285 0048h
50h	UART_MVR	Module version register	0283 0050h	0284 0050h	0285 0050h
54h	UART_SYSC	System configuration register	0283 0054h	0284 0054h	0285 0054h
58h	UART_SYSS	System status register	0283 0058h	0284 0058h	0285 0058h

Table 6-3. UART Registers (continued)

Offset	Acronym	Register Name	UART3 Physical Address	UART4 Physical Address	UART5 Physical Address
5Ch	UART_WER	Wake-up enable register	0283 005Ch	0284 005Ch	0285 005Ch
60h	UART_CFPS	Carrier frequency prescaler register	0283 0060h	0284 0060h	0285 0060h
64h	UART_RXFIFO_LVL	RX FIFO level register	0283 0064h	0284 0064h	0285 0064h
68h	UART_TXFIFO_LVL	TX FIFO level register	0283 0068h	0284 0068h	0285 0068h
6Ch	UART_IER2	Interrupt enable register 2	0283 006Ch	0284 006Ch	0285 006Ch
70h	UART_ISR2	Interrupt status register 2	0283 0070h	0284 0070h	0285 0070h
74h	UART_FREQ_SEL	Sample per bit selector register	0283 0074h	0284 0074h	0285 0074h
78h	UART_ABAUD_1ST_CHAR		0283 0078h	0284 0078h	0285 0078h
7Ch	UART_BAUD_2ND_CHAR		0283 007Ch	0284 007Ch	0285 007Ch
80h	UART_MDR3	Mode definition register 3	0283 0080h	0284 0080h	0285 0080h
84h	UART_TX_DMA_THRESHOLD	TX DMA threshold level register	0283 0084h	0284 0084h	0285 0084h
88h	UART_MDR4	Mode definition register 4	0283 0088h	0284 0088h	0285 0088h
8Ch	UART_EFR2	Enhanced features register 2	0283 008Ch	0284 008Ch	0285 008Ch
90h	UART_ECR	Enhanced control register	0283 0090h	0284 0090h	0285 0090h
94h	UART_TIMEGUARD	Timeguard register	0283 0094h	0284 0094h	0285 0094h
98h	UART_TIMEOUTL	Timeout lower byte register	0283 0098h	0284 0098h	0285 0098h
9Ch	UART_TIMEOUTH	Timeout higher byte register	0283 009Ch	0284 009Ch	0285 009Ch
A0h	UART_SCCR	Smartcard mode control register	0283 00A0h	0284 00A0h	0285 00A0h
A4h	UART_ERHR	Extended receive holding register	0283 00A4h	0284 00A4h	0285 00A4h
A4h	UART_ETHR	Extended transmit holding register	0283 00A4h	0284 00A4h	0285 00A4h
A8h	UART_MAR	Multidrop address register	0283 00A8h	0284 00A8h	0285 00A8h
ACH	UART_MMR	Multidrop mask register	0283 00ACH	0284 00ACH	0285 00ACH
B0h	UART_MBR	Multidrop broadcast address register	0283 00B0h	0284 00B0h	0285 00B0h

Table 6-4. UART Registers

Offset	Acronym	Register Name	UART6 Physical Address	UART7 Physical Address
0h	UART_THR	Transmit holding register	0286 0000h	0287 0000h
0h	UART_RHR	Receiver holding register	0286 0000h	0287 0000h
0h	UART_DLL	Baud clock divisor LSB value register	0286 0000h	0287 0000h
4h	UART_IER_UART	UART mode interrupt enable register	0286 0004h	0287 0004h
4h	UART_IER_IRDA	IrDA mode interrupt enable register	0286 0004h	0287 0004h
4h	UART_IER_CIR	CIR mode interrupt enable register	0286 0004h	0287 0004h
4h	UART_DLH	Baud clock divisor MSB value register	0286 0004h	0287 0004h
8h	UART_IIR_UART	UART mode interrupt identification register	0286 0008h	0287 0008h
8h	UART_IIR_IRDA	IrDA mode interrupt identification register	0286 0008h	0287 0008h
8h	UART_IIR_CIR	CIR mode interrupt identification register	0286 0008h	0287 0008h
8h	UART_FCR	FIFO control register	0286 0008h	0287 0008h
8h	UART_EFR	Enhanced feature register	0286 0008h	0287 0008h
Ch	UART_LCR	Line control register	0286 000Ch	0287 000Ch
10h	UART_MCR	Modem control register	0286 0010h	0287 0010h
10h	UART_XON1_ADDR1	UART mode XON1 character, IrDA mode ADDR1 address register	0286 0010h	0287 0010h
14h	UART_LSR_UART	UART mode line status register	0286 0014h	0287 0014h
14h	UART_LSR_IRDA	IrDA mode line status register	0286 0014h	0287 0014h
14h	UART_LSR_CIR	CIR mode line status register	0286 0014h	0287 0014h

Table 6-4. UART Registers (continued)

Offset	Acronym	Register Name	UART6 Physical Address	UART7 Physical Address
14h	UART_XON2_ADDR2	UART mode XON2 character, IrDA mode ADDR2 address register	0286 0014h	0287 0014h
18h	UART_MSR	Modem status register	0286 0018h	0287 0018h
18h	UART_XOFF1	UART mode XOFF1 character	0286 0018h	0287 0018h
18h	UART_TCR	Transmission control register	0286 0018h	0287 0018h
1Ch	UART_SPR	Scratchpad register	0286 001Ch	0287 001Ch
1Ch	UART_XOFF2	UART mode XOFF2 character	0286 001Ch	0287 001Ch
1Ch	UART_TLR	Trigger level register	0286 001Ch	0287 001Ch
20h	UART_MDR1	Mode definition register 1	0286 0020h	0287 0020h
24h	UART_MDR2	Mode definition register 2	0286 0024h	0287 0024h
28h	UART_SFLSR	Status FIFO line status register	0286 0028h	0287 0028h
28h	UART_TXFLL	Transmit frame length register low	0286 0028h	0287 0028h
2Ch	UART_RESUME	Resume halted operation register	0286 002Ch	0287 002Ch
2Ch	UART_TXFLH	Transmit frame length register high	0286 002Ch	0287 002Ch
30h	UART_SFREGL	Status FIFO register low	0286 0030h	0287 0030h
30h	UART_RXFLL	Received frame length register low	0286 0030h	0287 0030h
34h	UART_SFREGH	Status FIFO register high	0286 0034h	0287 0034h
34h	UART_RXFLH	Received frame length register high	0286 0034h	0287 0034h
38h	UART_BLR	BOF control register	0286 0038h	0287 0038h
38h	UART_UASR	UART autobauding status register	0286 0038h	0287 0038h
3Ch	UART_ACREG	Auxiliary control register	0286 003Ch	0287 003Ch
40h	UART_SCR	Supplementary control register	0286 0040h	0287 0040h
44h	UART_SSR	Supplementary status register	0286 0044h	0287 0044h
48h	UART_EBLR	BOF length register	0286 0048h	0287 0048h
50h	UART_MVR	Module version register	0286 0050h	0287 0050h
54h	UART_SYSC	System configuration register	0286 0054h	0287 0054h
58h	UART_SYSS	System status register	0286 0058h	0287 0058h
5Ch	UART_WER	Wake-up enable register	0286 005Ch	0287 005Ch
60h	UART_CFPS	Carrier frequency prescaler register	0286 0060h	0287 0060h
64h	UART_RXFIFO_LVL	RX FIFO level register	0286 0064h	0287 0064h
68h	UART_TXFIFO_LVL	TX FIFO level register	0286 0068h	0287 0068h
6Ch	UART_IER2	Interrupt enable register 2	0286 006Ch	0287 006Ch
70h	UART_ISR2	Interrupt status register 2	0286 0070h	0287 0070h
74h	UART_FREQ_SEL	Sample per bit selector register	0286 0074h	0287 0074h
78h	UART_ABAUD_1ST_CHAR		0286 0078h	0287 0078h
7Ch	UART_BAUD_2ND_CHAR		0286 007Ch	0287 007Ch
80h	UART_MDR3	Mode definition register 3	0286 0080h	0287 0080h
84h	UART_TX_DMA_THRESHOLD	TX DMA threshold level register	0286 0084h	0287 0084h
88h	UART_MDR4	Mode definition register 4	0286 0088h	0287 0088h
8Ch	UART_EFR2	Enhanced features register 2	0286 008Ch	0287 008Ch
90h	UART_ECR	Enhanced control register	0286 0090h	0287 0090h
94h	UART_TIMEGUARD	Timeguard register	0286 0094h	0287 0094h
98h	UART_TIMEOUTL	Timeout lower byte register	0286 0098h	0287 0098h
9Ch	UART_TIMEOUTH	Timeout higher byte register	0286 009Ch	0287 009Ch
A0h	UART_SCCR	Smartcard mode control register	0286 00A0h	0287 00A0h
A4h	UART_ERHR	Extended receive holding register	0286 00A4h	0287 00A4h

Table 6-4. UART Registers (continued)

Offset	Acronym	Register Name	UART6 Physical Address	UART7 Physical Address
A4h	UART_ETHR	Extended transmit holding register	0286 00A4h	0287 00A4h
A8h	UART_MAR	Multidrop address register	0286 00A8h	0287 00A8h
ACh	UART_MMR	Multidrop mask register	0286 00ACh	0287 00ACh
B0h	UART_MBR	Multidrop broadcast address register	0286 00B0h	0287 00B0h

Table 6-5. UART Registers

Offset	Acronym	Register Name	UART8 Physical Address	UART9 Physical Address
0h	UART_THR	Transmit holding register	0288 0000h	0289 0000h
0h	UART_RHR	Receiver holding register	0288 0000h	0289 0000h
0h	UART_DLL	Baud clock divisor LSB value register	0288 0000h	0289 0000h
4h	UART_IER_UART	UART mode interrupt enable register	0288 0004h	0289 0004h
4h	UART_IER_IRDA	IrDA mode interrupt enable register	0288 0004h	0289 0004h
4h	UART_IER_CIR	CIR mode interrupt enable register	0288 0004h	0289 0004h
4h	UART_DLH	Baud clock divisor MSB value register	0288 0004h	0289 0004h
8h	UART_IIR_UART	UART mode interrupt identification register	0288 0008h	0289 0008h
8h	UART_IIR_IRDA	IrDA mode interrupt identification register	0288 0008h	0289 0008h
8h	UART_IIR_CIR	CIR mode interrupt identification register	0288 0008h	0289 0008h
8h	UART_FCR	FIFO control register	0288 0008h	0289 0008h
8h	UART_EFR	Enhanced feature register	0288 0008h	0289 0008h
Ch	UART_LCR	Line control register	0288 000Ch	0289 000Ch
10h	UART_MCR	Modem control register	0288 0010h	0289 0010h
10h	UART_XON1_ADDR1	UART mode XON1 character, IrDA mode ADDR1 address register	0288 0010h	0289 0010h
14h	UART_LSR_UART	UART mode line status register	0288 0014h	0289 0014h
14h	UART_LSR_IRDA	IrDA mode line status register	0288 0014h	0289 0014h
14h	UART_LSR_CIR	CIR mode line status register	0288 0014h	0289 0014h
14h	UART_XON2_ADDR2	UART mode XON2 character, IrDA mode ADDR2 address register	0288 0014h	0289 0014h
18h	UART_MSR	Modem status register	0288 0018h	0289 0018h
18h	UART_XOFF1	UART mode XOFF1 character	0288 0018h	0289 0018h
18h	UART_TCR	Transmission control register	0288 0018h	0289 0018h
1Ch	UART_SPR	Scratchpad register	0288 001Ch	0289 001Ch
1Ch	UART_XOFF2	UART mode XOFF2 character	0288 001Ch	0289 001Ch
1Ch	UART_TLR	Trigger level register	0288 001Ch	0289 001Ch
20h	UART_MDR1	Mode definition register 1	0288 0020h	0289 0020h
24h	UART_MDR2	Mode definition register 2	0288 0024h	0289 0024h
28h	UART_SFSLR	Status FIFO line status register	0288 0028h	0289 0028h
28h	UART_TXFLL	Transmit frame length register low	0288 0028h	0289 0028h
2Ch	UART_RESUME	Resume halted operation register	0288 002Ch	0289 002Ch
2Ch	UART_TXFLH	Transmit frame length register high	0288 002Ch	0289 002Ch
30h	UART_SFREGL	Status FIFO register low	0288 0030h	0289 0030h
30h	UART_RXFLL	Received frame length register low	0288 0030h	0289 0030h
34h	UART_SFREGH	Status FIFO register high	0288 0034h	0289 0034h
34h	UART_RXFLH	Received frame length register high	0288 0034h	0289 0034h
38h	UART_BLR	BOF control register	0288 0038h	0289 0038h

Table 6-5. UART Registers (continued)

Offset	Acronym	Register Name	UART8 Physical Address	UART9 Physical Address
38h	UART_UASR	UART autobauding status register	0288 0038h	0289 0038h
3Ch	UART_ACREG	Auxiliary control register	0288 003Ch	0289 003Ch
40h	UART_SCR	Supplementary control register	0288 0040h	0289 0040h
44h	UART_SSR	Supplementary status register	0288 0044h	0289 0044h
48h	UART_EBLR	BOF length register	0288 0048h	0289 0048h
50h	UART_MVR	Module version register	0288 0050h	0289 0050h
54h	UART_SYSC	System configuration register	0288 0054h	0289 0054h
58h	UART_SYSS	System status register	0288 0058h	0289 0058h
5Ch	UART_WER	Wake-up enable register	0288 005Ch	0289 005Ch
60h	UART_CFPS	Carrier frequency prescaler register	0288 0060h	0289 0060h
64h	UART_RXFIFO_LVL	RX FIFO level register	0288 0064h	0289 0064h
68h	UART_TXFIFO_LVL	TX FIFO level register	0288 0068h	0289 0068h
6Ch	UART_IER2	Interrupt enable register 2	0288 006Ch	0289 006Ch
70h	UART_ISR2	Interrupt status register 2	0288 0070h	0289 0070h
74h	UART_FREQ_SEL	Sample per bit selector register	0288 0074h	0289 0074h
78h	UART_ABAUD_1ST_CHAR		0288 0078h	0289 0078h
7Ch	UART_BAUD_2ND_CHAR		0288 007Ch	0289 007Ch
80h	UART_MDR3	Mode definition register 3	0288 0080h	0289 0080h
84h	UART_TX_DMA_THRESHOLD	TX DMA threshold level register	0288 0084h	0289 0084h
88h	UART_MDR4	Mode definition register 4	0288 0088h	0289 0088h
8Ch	UART_EFR2	Enhanced features register 2	0288 008Ch	0289 008Ch
90h	UART_ECR	Enhanced control register	0288 0090h	0289 0090h
94h	UART_TIMEGUARD	Timeguard register	0288 0094h	0289 0094h
98h	UART_TIMEOUTL	Timeout lower byte register	0288 0098h	0289 0098h
9Ch	UART_TIMEOUTH	Timeout higher byte register	0288 009Ch	0289 009Ch
A0h	UART_SCCR	Smartcard mode control register	0288 00A0h	0289 00A0h
A4h	UART_ERHR	Extended receive holding register	0288 00A4h	0289 00A4h
A4h	UART_ETHR	Extended transmit holding register	0288 00A4h	0289 00A4h
A8h	UART_MAR	Multidrop address register	0288 00A8h	0289 00A8h
ACh	UART_MMR	Multidrop mask register	0288 00ACh	0289 00ACh
B0h	UART_MBR	Multidrop broadcast address register	0288 00B0h	0289 00B0h

Table 6-6. UART Registers

Offset	Acronym	Register Name	MCU_UART0 Physical Address	WKUP_UART 0 Physical Address
0h	UART_THR	Transmit holding register	40A0 0000h	4230 0000h
0h	UART_RHR	Receiver holding register	40A0 0000h	4230 0000h
0h	UART_DLL	Baud clock divisor LSB value register	40A0 0000h	4230 0000h
4h	UART_IER_UART	UART mode interrupt enable register	40A0 0004h	4230 0004h
4h	UART_IER_IRDA	IrDA mode interrupt enable register	40A0 0004h	4230 0004h
4h	UART_IER_CIR	CIR mode interrupt enable register	40A0 0004h	4230 0004h
4h	UART_DLH	Baud clock divisor MSB value register	40A0 0004h	4230 0004h
8h	UART_IIR_UART	UART mode interrupt identification register	40A0 0008h	4230 0008h
8h	UART_IIR_IRDA	IrDA mode interrupt identification register	40A0 0008h	4230 0008h
8h	UART_IIR_CIR	CIR mode interrupt identification register	40A0 0008h	4230 0008h

Table 6-6. UART Registers (continued)

Offset	Acronym	Register Name	MCU_UART0 Physical Address	WKUP_UART 0 Physical Address
8h	UART_FCR	FIFO control register	40A0 0008h	4230 0008h
8h	UART_EFR	Enhanced feature register	40A0 0008h	4230 0008h
Ch	UART_LCR	Line control register	40A0 000Ch	4230 000Ch
10h	UART_MCR	Modem control register	40A0 0010h	4230 0010h
10h	UART_XON1_ADDR1	UART mode XON1 character, IrDA mode ADDR1 address register	40A0 0010h	4230 0010h
14h	UART_LSR_UART	UART mode line status register	40A0 0014h	4230 0014h
14h	UART_LSR_IRDA	IrDA mode line status register	40A0 0014h	4230 0014h
14h	UART_LSR_CIR	CIR mode line status register	40A0 0014h	4230 0014h
14h	UART_XON2_ADDR2	UART mode XON2 character, IrDA mode ADDR2 address register	40A0 0014h	4230 0014h
18h	UART_MSR	Modem status register	40A0 0018h	4230 0018h
18h	UART_XOFF1	UART mode XOFF1 character	40A0 0018h	4230 0018h
18h	UART_TCR	Transmission control register	40A0 0018h	4230 0018h
1Ch	UART_SPR	Scratchpad register	40A0 001Ch	4230 001Ch
1Ch	UART_XOFF2	UART mode XOFF2 character	40A0 001Ch	4230 001Ch
1Ch	UART_TLR	Trigger level register	40A0 001Ch	4230 001Ch
20h	UART_MDR1	Mode definition register 1	40A0 0020h	4230 0020h
24h	UART_MDR2	Mode definition register 2	40A0 0024h	4230 0024h
28h	UART_SFLSR	Status FIFO line status register	40A0 0028h	4230 0028h
28h	UART_TXFLL	Transmit frame length register low	40A0 0028h	4230 0028h
2Ch	UART_RESUME	Resume halted operation register	40A0 002Ch	4230 002Ch
2Ch	UART_TXFLH	Transmit frame length register high	40A0 002Ch	4230 002Ch
30h	UART_SFREGL	Status FIFO register low	40A0 0030h	4230 0030h
30h	UART_RXFLL	Received frame length register low	40A0 0030h	4230 0030h
34h	UART_SFREGH	Status FIFO register high	40A0 0034h	4230 0034h
34h	UART_RXFLH	Received frame length register high	40A0 0034h	4230 0034h
38h	UART_BLR	BOF control register	40A0 0038h	4230 0038h
38h	UART_UASR	UART autobauding status register	40A0 0038h	4230 0038h
3Ch	UART_ACREG	Auxiliary control register	40A0 003Ch	4230 003Ch
40h	UART_SCR	Supplementary control register	40A0 0040h	4230 0040h
44h	UART_SSR	Supplementary status register	40A0 0044h	4230 0044h
48h	UART_EBLR	BOF length register	40A0 0048h	4230 0048h
50h	UART_MVR	Module version register	40A0 0050h	4230 0050h
54h	UART_SYSC	System configuration register	40A0 0054h	4230 0054h
58h	UART_SYSS	System status register	40A0 0058h	4230 0058h
5Ch	UART_WER	Wake-up enable register	40A0 005Ch	4230 005Ch
60h	UART_CFPS	Carrier frequency prescaler register	40A0 0060h	4230 0060h
64h	UART_RXFIFO_LVL	RX FIFO level register	40A0 0064h	4230 0064h
68h	UART_TXFIFO_LVL	TX FIFO level register	40A0 0068h	4230 0068h
6Ch	UART_IER2	Interrupt enable register 2	40A0 006Ch	4230 006Ch
70h	UART_ISR2	Interrupt status register 2	40A0 0070h	4230 0070h
74h	UART_FREQ_SEL	Sample per bit selector register	40A0 0074h	4230 0074h
78h	UART_ABAUD_1ST_CHAR		40A0 0078h	4230 0078h
7Ch	UART_BAUD_2ND_CHAR		40A0 007Ch	4230 007Ch
80h	UART_MDR3	Mode definition register 3	40A0 0080h	4230 0080h

Table 6-6. UART Registers (continued)

Offset	Acronym	Register Name	MCU_UART0 Physical Address	WKUP_UART 0 Physical Address
84h	UART_TX_DMA_THRESHOLD	TX DMA threshold level register	40A0 0084h	4230 0084h
88h	UART_MDR4	Mode definition register 4	40A0 0088h	4230 0088h
8Ch	UART_EFR2	Enhanced features register 2	40A0 008Ch	4230 008Ch
90h	UART_ECR	Enhanced control register	40A0 0090h	4230 0090h
94h	UART_TIMEGUARD	Timeguard register	40A0 0094h	4230 0094h
98h	UART_TIMEOUTL	Timeout lower byte register	40A0 0098h	4230 0098h
9Ch	UART_TIMEOUTH	Timeout higher byte register	40A0 009Ch	4230 009Ch
A0h	UART_SCCR	Smartcard mode control register	40A0 00A0h	4230 00A0h
A4h	UART_ERHR	Extended receive holding register	40A0 00A4h	4230 00A4h
A4h	UART_ETHR	Extended transmit holding register	40A0 00A4h	4230 00A4h
A8h	UART_MAR	Multidrop address register	40A0 00A8h	4230 00A8h
ACH	UART_MMR	Multidrop mask register	40A0 00ACH	4230 00ACH
B0h	UART_MBR	Multidrop broadcast address register	40A0 00B0h	4230 00B0h

6.1 UART_THR Register (Offset = 0h) [reset = 0h]

UART_THR is shown in [Figure 6-1](#) and described in [Table 6-8](#).

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The transmitter section consists of the transmit holding register (UART_THR) and the transmit shift register. The UART_THR is a 64-byte FIFO. The local host (LH) writes data to the UART_THR. The data is placed in the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled, location 0 of the FIFO stores the data.

Table 6-7. UART_THR Instances

Instance	Physical Address
UART0	0280 0000h
UART1	0281 0000h
UART2	0282 0000h
UART3	0283 0000h
UART4	0284 0000h
UART5	0285 0000h
UART6	0286 0000h
UART7	0287 0000h
UART8	0288 0000h
UART9	0289 0000h
MCU_UART0	40A0 0000h
WKUP_UART0	4230 0000h

Figure 6-1. UART_THR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								THR							
R-0h																								W-0h							

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 6-8. UART_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	THR	W	0h	Transmit holding register

6.2 UART_RHR Register (Offset = 0h) [reset = 0h]

UART_RHR is shown in [Figure 6-2](#) and described in [Table 6-10](#).

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The receiver section consists of the receiver holding register (UART_RHR) and the receiver shift register. The UART_RHR is a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the UART_RHR. If the FIFO is disabled, location 0 of the FIFO stores the single data character. Note: If an overflow occurs, the data in the UART_RHR is not overwritten.

Table 6-9. UART_RHR Instances

Instance	Physical Address
UART0	0280 0000h
UART1	0281 0000h
UART2	0282 0000h
UART3	0283 0000h
UART4	0284 0000h
UART5	0285 0000h
UART6	0286 0000h
UART7	0287 0000h
UART8	0288 0000h
UART9	0289 0000h
MCU_UART0	40A0 0000h
WKUP_UART0	4230 0000h

Figure 6-2. UART_RHR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RHR							
R-0h																								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 6-10. UART_RHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RHR	R	0h	Receive holding register

6.3 UART_DLL Register (Offset = 0h) [reset = 0h]

UART_DLL is shown in [Figure 6-3](#) and described in [Table 6-12](#).

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This register, with UART_DLH, stores the 14-bit divisor for generation of the baud clock in the baud rate generator. UART_DLH stores the most-significant part of the divisor. UART_DLL stores the least-significant part of the divisor.

Table 6-11. UART_DLL Instances

Instance	Physical Address
UART0	0280 0000h
UART1	0281 0000h
UART2	0282 0000h
UART3	0283 0000h
UART4	0284 0000h
UART5	0285 0000h
UART6	0286 0000h
UART7	0287 0000h
UART8	0288 0000h
UART9	0289 0000h
MCU_UART0	40A0 0000h
WKUP_UART0	4230 0000h

Figure 6-3. UART_DLL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLOCK_LSB							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-12. UART_DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	CLOCK_LSB	R/W	0h	Stores the 8-bit LSB divisor value

6.4 UART_IER_UART Register (Offset = 4h) [reset = 0h]

UART_IER_UART is shown in [Figure 6-4](#) and described in [Table 6-14](#).

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Interrupt enable register

The interrupt enable register (UART_IER_UART) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, UART_RHR interrupt, UART_THR interrupt, XOFF received and CTS*/RTS* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.

Table 6-13. UART_IER_UART Instances

Instance	Physical Address
UART0	0280 0004h
UART1	0281 0004h
UART2	0282 0004h
UART3	0283 0004h
UART4	0284 0004h
UART5	0285 0004h
UART6	0286 0004h
UART7	0287 0004h
UART8	0288 0004h
UART9	0289 0004h
MCU_UART0	40A0 0004h
WKUP_UART0	4230 0004h

Figure 6-4. UART_IER_UART Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_I T	LINE_STS_IT	THR_IT	RHR_IT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-14. UART_IER_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	CTS_IT	R/W	0h	0h = Disables the CTS* interrupt 1h = Enables the CTS* interrupt
6	RTS_IT	R/W	0h	0h = Disables the RTS* interrupt 1h = Enables the RTS* interrupt

Table 6-14. UART_IER_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	XOFF_IT	R/W	0h	0h = Disables the XOFF interrupt 1h = Enables the XOFF interrupt
4	SLEEP_MODE	R/W	0h	0h = Disables sleep mode 1h = Enables sleep mode (stop baud rate clock when the module is inactive)
3	MODEM_STS_IT	R/W	0h	0h = Disables the modem status register interrupt 1h = Enables the modem status register interrupt
2	LINE_STS_IT	R/W	0h	0h = Disables the receiver line status interrupt 1h = Enables the receiver line status interrupt
1	THR_IT	R/W	0h	0h = Disables the THR interrupt 1h = Enables the THR interrupt
0	RHR_IT	R/W	0h	0h = Disables the RHR interrupt and time-out interrupt 1h = Enables the RHR interrupt and time-out interrupt

6.5 UART_IER_IRDA Register (Offset = 4h) [reset = 0h]

UART_IER_IRDA is shown in [Figure 6-5](#) and described in [Table 6-16](#).

Return to [Summary Table](#).

There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually. Note: The TX_STATUS_IT interrupt reflects two possible conditions. The UART_MDR2[0] should be read to determine the status in the event of this interrupt.

Table 6-15. UART_IER_IRDA Instances

Instance	Physical Address
UART0	0280 0004h
UART1	0281 0004h
UART2	0282 0004h
UART3	0283 0004h
UART4	0284 0004h
UART5	0285 0004h
UART6	0286 0004h
UART7	0287 0004h
UART8	0288 0004h
UART9	0289 0004h
MCU_UART0	40A0 0004h
WKUP_UART0	4230 0004h

Figure 6-5. UART_IER_IRDA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRI G_IT	RX_OVERRUN _IT	LAST_RX_BYT E_IT	THR_IT	RHR_IT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-16. UART_IER_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	EOF_IT	R/W	0h	0h = Disables the received EOF interrupt 1h = Enables the received EOF interrupt
6	LINE_STS_IT	R/W	0h	0h = Disables the receiver line status interrupt 1h = Enables the receiver line status interrupt
5	TX_STATUS_IT	R/W	0h	0h = Disables the TX status interrupt 1h = Enables the TX status interrupt

Table 6-16. UART_IER_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	STS_FIFO_TRIG_IT	R/W	0h	0h = Disables status FIFO trigger level interrupt 1h = Enables status FIFO trigger level interrupt
3	RX_OVERRUN_IT	R/W	0h	0h = Disables the RX overrun interrupt 1h = Enables the RX overrun interrupt
2	LAST_RX_BYTE_IT	R/W	0h	0h = Disables the last byte of frame in RX FIFO interrupt 1h = Enables the last byte of frame in RX FIFO interrupt
1	THR_IT	R/W	0h	0h = Disables the THR interrupt 1h = Enables the THR interrupt
0	RHR_IT	R/W	0h	0h = Disables the RHR interrupt and time-out interrupt 1h = Enables the RHR interrupt and time-out interrupt

6.6 UART_IER_CIR Register (Offset = 4h) [reset = X]

UART_IER_CIR is shown in [Figure 6-6](#) and described in [Table 6-18](#).

Return to [Summary Table](#).

There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually. Notes: The RX_STOP_IT interrupt is generated based on the value set in the BOF Length register (UART_EBLR). In IR-CIR mode, contrary to the IR-IRDA mode, the TX_STATUS_IT has only one meaning corresponding to the case UART_MDR2[0] = 0.

Table 6-17. UART_IER_CIR Instances

Instance	Physical Address
UART0	0280 0004h
UART1	0281 0004h
UART2	0282 0004h
UART3	0283 0004h
UART4	0284 0004h
UART5	0285 0004h
UART6	0286 0004h
UART7	0287 0004h
UART8	0288 0004h
UART9	0289 0004h
MCU_UART0	40A0 0004h
WKUP_UART0	4230 0004h

Figure 6-6. UART_IER_CIR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
NOT_USED	TX_STATUS_IT	RESERVED	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT	
R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-18. UART_IER_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-6	NOT_USED	R/W	0h	
5	TX_STATUS_IT	R/W	0h	0h = Disables the TX status interrupt 1h = Enables the TX status interrupt
4	RESERVED	R/W	X	
3	RX_OVERRUN_IT	R/W	0h	0h = Disables the RX overrun interrupt 1h = Enables the RX overrun interrupt

Table 6-18. UART_IER_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RX_STOP_IT	R/W	0h	0h = Disables the receive stop interrupt 1h = Enables the receive stop interrupt
1	THR_IT	R/W	0h	0h = Disables the THR interrupt 1h = Enables the THR interrupt
0	RHR_IT	R/W	0h	0h = Disables the RHR interrupt 1h = Enables the RHR interrupt

6.7 UART_DLH Register (Offset = 4h) [reset = 0h]

UART_DLH is shown in [Figure 6-7](#) and described in [Table 6-20](#).

Return to [Summary Table](#).

This register, with UART_DLL, stores the 14-bit divisor for generating the baud clock in the baud rate generator. DLH stores the most-significant part of the divisor. DLL stores the least-significant part of the divisor.

Table 6-19. UART_DLH Instances

Instance	Physical Address
UART0	0280 0004h
UART1	0281 0004h
UART2	0282 0004h
UART3	0283 0004h
UART4	0284 0004h
UART5	0285 0004h
UART6	0286 0004h
UART7	0287 0004h
UART8	0288 0004h
UART9	0289 0004h
MCU_UART0	40A0 0004h
WKUP_UART0	4230 0004h

Figure 6-7. UART_DLH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										CLOCK_MSB					
R-0h										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-20. UART_DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	CLOCK_MSB	R/W	0h	Stores the 6-bit MSB divisor value

6.8 UART_IIR_UART Register (Offset = 8h) [reset = 1h]

UART_IIR_UART is shown in [Figure 6-8](#) and described in [Table 6-22](#).

Return to [Summary Table](#).

Interrupt identification register.

The UART_IIR_UART is a read-only register that provides the source of the interrupt in a prioritized manner.

Table 6-21. UART_IIR_UART Instances

Instance	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
UART7	0287 0008h
UART8	0288 0008h
UART9	0289 0008h
MCU_UART0	40A0 0008h
WKUP_UART0	4230 0008h

Figure 6-8. UART_IIR_UART Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
FCR_MIRROR		IT_TYPE					IT_PENDING
R-0h		R-0h					R-1h

LEGEND: R = Read Only; -n = value after reset

Table 6-22. UART_IIR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-6	FCR_MIRROR	R	0h	Mirror the contents of UART_FCR[0] on both bits.
5-1	IT_TYPE	R	0h	Read 0h = Modem interrupt. Priority = 4 Read 1h = THR interrupt. Priority = 3 Read 2h = RHR interrupt. Priority = 2 Read 3h = Receiver line status error. Priority = 3 Read 6h = Rx time-out. Priority = 2 Read 8h = XOFF/special character. Priority = 5 Read 10h = CTS, RTS, DSR change state from active (low) to inactive (high) Priority = 6

Table 6-22. UART_IIR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IT_PENDING	R	1h	Read 0h = An interrupt is pending. Read 1h = No interrupt is pending.

6.9 UART_IIR_IRDA Register (Offset = 8h) [reset = 0h]

UART_IIR_IRDA is shown in [Figure 6-9](#) and described in [Table 6-24](#).

Return to [Summary Table](#).

The interrupt line is activated whenever one of the 8 interrupts is active.

Table 6-23. UART_IIR_IRDA Instances

Instance	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
UART7	0287 0008h
UART8	0288 0008h
UART9	0289 0008h
MCU_UART0	40A0 0008h
WKUP_UART0	4230 0008h

Figure 6-9. UART_IIR_IRDA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAS T_BYTE_IT	THR_IT	RHR_IT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 6-24. UART_IIR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	EOF_IT	R	0h	Read 0h = Receive EOF interrupt inactive Read 1h = Received EOF interrupt active
6	LINE_STS_IT	R	0h	Read 0h = Receiver line status interrupt inactive Read 1h = Receiver line status interrupt active
5	TX_STATUS_IT	R	0h	Read 0h = TX status interrupt inactive Read 1h = TX status interrupt active
4	STS_FIFO_IT	R	0h	Read 0h = Status FIFO trigger level interrupt inactive Read 1h = Status FIFO trigger level interrupt active

Table 6-24. UART_IIR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RX_OE_IT	R	0h	Read 0h = RX overrun interrupt inactive Read 1h = RX overrun interrupt active
2	RX_FIFO_LAST_BYTE_IT	R	0h	Read 0h = Last byte of frame in RX FIFO interrupt inactive Read 1h = Last byte of frame in RX FIFO interrupt active
1	THR_IT	R	0h	Read 0h = THR interrupt inactive Read 1h = THR interrupt active
0	RHR_IT	R	0h	Read 0h = RHR interrupt inactive Read 1h = RHR interrupt active

6.10 UART_IIR_CIR Register (Offset = 8h) [reset = X]

UART_IIR_CIR is shown in [Figure 6-10](#) and described in [Table 6-26](#).

Return to [Summary Table](#).

The interrupt line is activated whenever one of the 6 interrupts is active.

Table 6-25. UART_IIR_CIR Instances

Instance	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
UART7	0287 0008h
UART8	0288 0008h
UART9	0289 0008h
MCU_UART0	40A0 0008h
WKUP_UART0	4230 0008h

Figure 6-10. UART_IIR_CIR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT
R-X		R-0h	R-X	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 6-26. UART_IIR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-6	RESERVED	R	X	
5	TX_STATUS_IT	R	0h	Read 0h = TX status interrupt inactive Read 1h = TX status interrupt active
4	RESERVED	R	X	
3	RX_OE_IT	R	0h	Read 0h = RX overrun interrupt inactive Read 1h = RX overrun interrupt active
2	RX_STOP_IT	R	0h	Read 0h = Receive stop interrupt inactive Read 1h = Receive stop interrupt active
1	THR_IT	R	0h	Read 0h = THR interrupt inactive Read 1h = THR interrupt active

Table 6-26. UART_IIR_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RHR_IT	R	0h	Read 0h = RHR interrupt inactive Read 1h = RHR interrupt active

6.11 UART_FCR Register (Offset = 8h) [reset = 0h]

UART_FCR is shown in [Figure 6-11](#) and described in [Table 6-28](#).

Return to [Summary Table](#).

FIFO control register

Notes: Bits 4 and 5 can only be written to when UART_EFR[4] = 1. Bits 0 and 3 can be changed only when the baud clock is not running (DLL and DLH set to 0). See for UART_FCR[5:4] setting restriction when UART_SCR[6] = 1. See for UART_FCR[7:6] setting restriction when UART_SCR[7] = 1.

Table 6-27. UART_FCR Instances

Instance	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
UART7	0287 0008h
UART8	0288 0008h
UART9	0289 0008h
MCU_UART0	40A0 0008h
WKUP_UART0	4230 0008h

Figure 6-11. UART_FCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLE AR	RX_FIFO_CLE AR	FIFO_EN
W-0h		W-0h		W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 6-28. UART_FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	

Table 6-28. UART_FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RX_FIFO_TRIG	W	0h	Sets the trigger level for the RX FIFO: If UART_SCR[7] = 0 and UART_TLR[7:4] = 0000: 0h = 8 characters 1h = 16 characters 2h = 56 characters 3h = 60 characters If UART_SCR[7] = 0 and UART_TLR[7:4] != 0000, RX_FIFO_TRIG is not considered. If UART_SCR[7] = 1, RX_FIFO_TRIG is 2 LSBs of the trigger level (1-63 on 6 bits) with the granularity 1.
5-4	TX_FIFO_TRIG	W	0h	Sets the trigger level for the TX FIFO: If UART_SCR[6] = 0 and UART_TLR[3:0] = 0000: 0h = 8 spaces 1h = 16 spaces 2h = 32 spaces 3h = 56 spaces If UART_SCR[6] = 0 and UART_TLR[3:0] != 0000, TX_FIFO_TRIG is not considered. If UART_SCR[6] = 1, TX_FIFO_TRIG is 2 LSBs of the trigger level (1-63 on 6 bits) with the granularity 1
3	DMA_MODE	W	0h	This register is considered if UART_SCR[0] = 0. Write 0h = DMA_MODE 0 (No DMA) Write 1h = DMA_MODE 1 (UART_nDMA_REQ[0] in TX (UARTi_DREQ_TX), UART_nDMA_REQ[1] in RX (UARTi_DREQ_RX))
2	TX_FIFO_CLEAR	W	0h	Write 0h = No change Write 1h = Clears the TX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO.
1	RX_FIFO_CLEAR	W	0h	Write 0h = No change Write 1h = Clears the RX FIFO and resets its counter logic to 0. Returns to 0 after clearing FIFO.
0	FIFO_EN	W	0h	Write 0h = Disables the transmit and RX FIFOs. The transmit and receive holding registers are 1-byte FIFOs. Write 1h = Enables the transmit and RX FIFOs. The transmit and receive holding registers are 64-byte FIFOs.

6.12 UART_EFR Register (Offset = 8h) [reset = 0h]

UART_EFR is shown in [Figure 6-12](#) and described in [Table 6-30](#).

Return to [Summary Table](#).

Enhanced feature register

This register enables or disables enhanced features. Most of the enhanced functions apply only to UART modes, but UART_EFR[4] enables write accesses to UART_FCR[5:4], the TX trigger level, which is also used in IrDA modes.

Table 6-29. UART_EFR Instances

Instance	Physical Address
UART0	0280 0008h
UART1	0281 0008h
UART2	0282 0008h
UART3	0283 0008h
UART4	0284 0008h
UART5	0285 0008h
UART6	0286 0008h
UART7	0287 0008h
UART8	0288 0008h
UART9	0289 0008h
MCU_UART0	40A0 0008h
WKUP_UART0	4230 0008h

Figure 6-12. UART_EFR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHARACTER_DETECT	ENHANCED_ENABLE	SW_FLOW_CONTROL			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-30. UART_EFR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	AUTO_CTS_EN	R/W	0h	Auto-CTS enable bit 0h = Normal operation 1h = Auto-CTS flow control is enabled. Transmission is halted when the CTS* pin is high (inactive).

Table 6-30. UART_EFR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AUTO_RTS_EN	R/W	0h	Auto-RTS enable bit 0h = Normal operation 1h = Auto-RTS flow control is enabled. RTS* pin goes high (inactive) when the RX FIFO HALT trigger level, UART_TCR[3:0], is reached, and goes low (active) when the RX FIFO RESTORE transmission trigger level is reached.
5	SPECIAL_CHAR_DETECT	R/W	0h	0h = Normal operation 1h = Special character detect enable. Received data is compared with XOFF2 data. If a match occurs, the received data is transferred to the RX FIFO and the UART_IIR[4] bit is set to 1 to indicate that a special character was detected.
4	ENHANCED_EN	R/W	0h	Enhanced functions write enable bit 0h = Disables writing to IER bits 4-7, UART_FCR bits 4-5, and UART_MCR bits 5-7. 1h = Enables writing to IER bits 4-7, UART_FCR bits 4-5, and UART_MCR bits 5-7.
3-0	SW_FLOW_CONTROL	R/W	0h	Combinations of software flow control can be selected by programming bit 3 - bit 0. See <i>UART_EFR[3:0] Software Flow Control Options</i> .

6.13 UART_LCR Register (Offset = Ch) [reset = 0h]

UART_LCR is shown in [Figure 6-13](#) and described in [Table 6-32](#).

Return to [Summary Table](#).

Line control register UART_LCR[6:0] define transmission and reception parameters. Note: When UART_LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as UART_LCR[6] = 1.

Table 6-31. UART_LCR Instances

Instance	Physical Address
UART0	0280 000Ch
UART1	0281 000Ch
UART2	0282 000Ch
UART3	0283 000Ch
UART4	0284 000Ch
UART5	0285 000Ch
UART6	0286 000Ch
UART7	0287 000Ch
UART8	0288 000Ch
UART9	0289 000Ch
MCU_UART0	40A0 000Ch
WKUP_UART0	4230 000Ch

Figure 6-13. UART_LCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DIV_EN	BREAK_EN	PARITY_TYPE 2	PARITY_TYPE 1	PARITY_EN	NB_STOP	CHAR_LENGTH	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-32. UART_LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	DIV_EN	R/W	0h	0h = Normal operating condition 1h = Divisor latch enable. Allows access to UART_DLL, UART_DLH, and other registers (see <i>UART Register Access Mode Programming (Using UART_LCR)</i>).
6	BREAK_EN	R/W	0h	Break control bit 0h = Normal operating condition 1h = Forces the transmitter output to go low to alert the communication terminal

Table 6-32. UART_LCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PARITY_TYPE2	R/W	0h	Selects the forced parity format (if UART_LCR[3] = 1). If UART_LCR[5] = 1 and UART_LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If UART_LCR[5] = 1 and UART_LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data.
4	PARITY_TYPE1	R/W	0h	0h = Odd parity is generated (if UART_LCR[3] = 1). 1h = Even parity is generated (if UART_LCR[3] = 1).
3	PARITY_EN	R/W	0h	0h = No parity 1h = A parity bit is generated during transmission and the receiver checks for received parity.
2	NB_STOP	R/W	0h	Specifies the number of stop-bits 0h = 1 stop-bit (word length = 5, 6, 7, 8) 1h = 1.5 stop-bits (word length = 5) 2 stop-bits (word length = 6, 7, 8)
1-0	CHAR_LENGTH	R/W	0h	Specifies the word length to be transmitted or received 0h = 5 bits 1h = 6 bits 2h = 7 bits 3h = 8 bits

6.14 UART_MCR Register (Offset = 10h) [reset = 0h]

UART_MCR is shown in [Figure 6-14](#) and described in [Table 6-34](#).

Return to [Summary Table](#).

Modem control register UART_MCR[3:0] controls the interface with the modem, data set, or peripheral device that emulates the modem.

Table 6-33. UART_MCR Instances

Instance	Physical Address
UART0	0280 0010h
UART1	0281 0010h
UART2	0282 0010h
UART3	0283 0010h
UART4	0284 0010h
UART5	0285 0010h
UART6	0286 0010h
UART7	0287 0010h
UART8	0288 0010h
UART9	0289 0010h
MCU_UART0	40A0 0010h
WKUP_UART0	4230 0010h

Figure 6-14. UART_MCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	TCR_TLR	XON_EN	LOOPBACK_EN	CD_STS_CH	RI_STS_CH	RTS	DTR
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-34. UART_MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	TCR_TLR	R/W	0h	0h = No action 1h = Enables access to the UART_TCR and UART_TLR registers
5	XON_EN	R/W	0h	0h = Disable XON any function. 1h = Enable XON any function.
4	LOOPBACK_EN	R/W	0h	0h = Normal operating mode 1h = Enable local loopback mode (internal). In this mode, the MCR[3:0] signals are looped back into the UART_MSR[7:4] bit field. The transmit output is looped back to the receive input internally.

Table 6-34. UART_MCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CD_STS_CH	R/W	0h	0h = In loopback, forces DCD* input high and IRQ outputs to inactive state 1h = In loopback, forces DCD* input low and IRQ outputs to inactive state
2	RI_STS_CH	R/W	0h	0h = In loopback, forces RI* input high 1h = In loopback, forces RI* input low
1	RTS	R/W	0h	In loopback, controls the UART_MSR[4] bit. If auto-RTS is enabled, the RTS* output is controlled by hardware flow control. 0h = Force RTS* output to inactive (high). 1h = Force RTS* output to active (low).
0	DTR	R/W	0h	0h = Force DTR* output to inactive (high). 1h = Force DTR* output to active (low).

6.15 UART_XON1_ADDR1 Register (Offset = 10h) [reset = 0h]

UART_XON1_ADDR1 is shown in [Figure 6-15](#) and described in [Table 6-36](#).

Return to [Summary Table](#).

UART mode: XON1 character, IrDA mode: ADDR1 address

Table 6-35. UART_XON1_ADDR1 Instances

Instance	Physical Address
UART0	0280 0010h
UART1	0281 0010h
UART2	0282 0010h
UART3	0283 0010h
UART4	0284 0010h
UART5	0285 0010h
UART6	0286 0010h
UART7	0287 0010h
UART8	0288 0010h
UART9	0289 0010h
MCU_UART0	40A0 0010h
WKUP_UART0	4230 0010h

Figure 6-15. UART_XON1_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XON_WORD1							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-36. UART_XON1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	XON_WORD1	R/W	0h	Stores the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes

6.16 UART_LSR_UART Register (Offset = 14h) [reset = 60h]

UART_LSR_UART is shown in [Figure 6-16](#) and described in [Table 6-38](#).

[Return to Summary Table.](#)

Line status register

Table 6-37. UART_LSR_UART Instances

Instance	Physical Address
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
UART7	0287 0014h
UART8	0288 0014h
UART9	0289 0014h
MCU_UART0	40A0 0014h
WKUP_UART0	4230 0014h

Figure 6-16. UART_LSR_UART Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E
R-0h	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 6-38. UART_LSR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	RX_FIFO_STS	R	0h	Read 0h = Normal operation Read 1h = At least one parity error, framing error, or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.
6	TX_SR_E	R	1h	Read 0h = Transmitter hold (TX FIFO) and shift registers are not empty. Read 1h = Transmitter hold (TX FIFO) and shift registers are empty.
5	TX_FIFO_E	R	1h	Read 0h = Transmit hold register (TX FIFO) is not empty. Read 1h = Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.

Table 6-38. UART_LSR_UART Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RX_BI	R	0h	Read 0h = No break condition Read 1h = A break was detected while the data from the RX FIFO was received (for example, RX input was low for one character + 1 bit time frame).
3	RX_FE	R	0h	Read 0h = No framing error in data RX FIFO Read 1h = Framing error occurred in data from RX FIFO (received data did not have a valid stop-bit).
2	RX_PE	R	0h	Read 0h = No parity error in data from RX FIFO Read 1h = Parity error in data from RX FIFO
1	RX_OE	R	0h	Read 0h = No overrun error Read 1h = Overrun error occurred. Set when the character in the receive shift register is not transferred to the RX FIFO. This occurs only when the RX FIFO is full.
0	RX_FIFO_E	R	0h	Read 0h = No data in the RX FIFO Read 1h = At least one data character in the RX FIFO

6.17 UART_LSR_IRDA Register (Offset = 14h) [reset = 83h]

UART_LSR_IRDA is shown in [Figure 6-17](#) and described in [Table 6-40](#).

Return to [Summary Table](#).

When the LSR is read, LSR[4:2] reflect the error bits [FL, CRC, ABORT] of the frame at the top of the STATUS FIFO (next frame status to be read).

Table 6-39. UART_LSR_IRDA Instances

Instance	Physical Address
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
UART7	0287 0014h
UART8	0288 0014h
UART9	0289 0014h
MCU_UART0	40A0 0014h
WKUP_UART0	4230 0014h

Figure 6-17. UART_LSR_IRDA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E
R-1h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h

LEGEND: R = Read Only; -n = value after reset

Table 6-40. UART_LSR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	THR_EMPTY	R	1h	Read 0h = Transmit holding register (TX FIFO) is not empty. Read 1h = Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.
6	STS_FIFO_FULL	R	0h	Read 0h = Status FIFO not full Read 1h = Status FIFO full

Table 6-40. UART_LSR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RX_LAST_BYTE	R	0h	Read 0h = The RX FIFO (RHR) does not contain the last byte of the frame to be read. Read 1h = The RX FIFO (RHR) contains the last byte of the frame to be read. This bit is set only when the last byte of a frame is available to be read. It determines the frame boundary. It is cleared on a single read of the LSR register.
4	FRAME_TOO_LONG	R	0h	Read 0h = No frame-too-long error in frame Read 1h = Frame-too-long error in the frame at the top of the STATUS FIFO, (next character to be read). This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) is received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected.
3	ABORT	R	0h	Read 0h = No abort pattern error in frame Read 1h = Abort pattern is received. SIR and MIR: Abort pattern FIR: Illegal symbol
2	CRC	R	0h	Read 0h = No CRC error in frame Read 1h = CRC error in the frame at the top of the STATUS FIFO (next character to be read)
1	STS_FIFO_E	R	1h	Read 0h = Status FIFO not empty Read 1h = Status FIFO empty
0	RX_FIFO_E	R	1h	Read 0h = No data in the RX FIFO Read 1h = At least one data character in the RX FIFO

6.18 UART_LSR_CIR Register (Offset = 14h) [reset = X]

UART_LSR_CIR is shown in [Figure 6-18](#) and described in [Table 6-42](#).

Return to [Summary Table](#).

Line status register in CIR mode

Table 6-41. UART_LSR_CIR Instances

Instance	Physical Address
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
UART7	0287 0014h
UART8	0288 0014h
UART9	0289 0014h
MCU_UART0	40A0 0014h
WKUP_UART0	4230 0014h

Figure 6-18. UART_LSR_CIR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E
R-1h	R-0h	R-0h	R-X				R-1h

LEGEND: R = Read Only; -n = value after reset

Table 6-42. UART_LSR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	THR_EMPTY	R	1h	Read 0h = Transmit holding register (TX FIFO) is not empty. Read 1h = Transmit hold register (TX FIFO) is empty. The transmission is not necessarily complete.
6	RESERVED	R	0h	
5	RX_STOP	R	0h	The RX_STOP is generated based on the value set in the BOF Length register (UART_EBLR). It is cleared on a single read of the UART_LSR register. Read 0h = Reception is ongoing or waiting for a new frame. Read 1h = Reception is complete.
4-1	RESERVED	R	X	

Table 6-42. UART_LSR_CIR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RX_FIFO_E	R	1h	Read 0h = At least one data character in the RX FIFO Read 1h = No data in the RX FIFO

6.19 UART_XON2_ADDR2 Register (Offset = 14h) [reset = 0h]

UART_XON2_ADDR2 is shown in [Figure 6-19](#) and described in [Table 6-44](#).

Return to [Summary Table](#).

Stores the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes

Table 6-43. UART_XON2_ADDR2 Instances

Instance	Physical Address
UART0	0280 0014h
UART1	0281 0014h
UART2	0282 0014h
UART3	0283 0014h
UART4	0284 0014h
UART5	0285 0014h
UART6	0286 0014h
UART7	0287 0014h
UART8	0288 0014h
UART9	0289 0014h
MCU_UART0	40A0 0014h
WKUP_UART0	4230 0014h

Figure 6-19. UART_XON2_ADDR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XON_WORD2							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-44. UART_XON2_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	XON_WORD2	R/W	0h	Stores the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes

6.20 UART_MSR Register (Offset = 18h) [reset = 0h]

UART_MSR is shown in [Figure 6-20](#) and described in [Table 6-46](#).

Return to [Summary Table](#).

Modem status register. UART mode only.

This register provides information about the current state of the control lines from the modem, data set, or peripheral device to the LH. It also indicates when a control input from the modem changes state.

Table 6-45. UART_MSR Instances

Instance	Physical Address
UART0	0280 0018h
UART1	0281 0018h
UART2	0282 0018h
UART3	0283 0018h
UART4	0284 0018h
UART5	0285 0018h
UART6	0286 0018h
UART7	0287 0018h
UART8	0288 0018h
UART9	0289 0018h
MCU_UART0	40A0 0018h
WKUP_UART0	4230 0018h

Figure 6-20. UART_MSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 6-46. UART_MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	NCD_STS	R	0h	This bit is the complement of the DCD* input. In loopback mode, it is equivalent to UART_MCR[3].
6	NRI_STS	R	0h	This bit is the complement of the RI* input. In loopback mode, it is equivalent to UART_MCR[2].
5	NDSR_STS	R	0h	This bit is the complement of the DSR* input. In loopback mode, it is equivalent to UART_MCR[0].
4	NCTS_STS	R	0h	This bit is the complement of the CTS* input. In loopback mode, it is equivalent to UART_MCR[1].

Table 6-46. UART_MSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	DCD_STS	R	0h	Indicates that DCD* input (or UART_MCR[3] in loopback) changed. Cleared on a read.
2	RI_STS	R	0h	Indicates that RI* input (or UART_MCR[2] in loopback) changed state from low to high. Cleared on a read.
1	DSR_STS	R	0h	Read 1h = Indicates that DSR* input (or UART_MCR[0] in loopback) changed state. Cleared on a read.
0	CTS_STS	R	0h	Read 1h = Indicates that CTS* input (or UART_MCR[1] in loopback) changed state. Cleared on a read.

6.21 UART_XOFF1 Register (Offset = 18h) [reset = 0h]

UART_XOFF1 is shown in [Figure 6-21](#) and described in [Table 6-48](#).

[Return to Summary Table.](#)

UART mode XOFF1 character

Table 6-47. UART_XOFF1 Instances

Instance	Physical Address
UART0	0280 0018h
UART1	0281 0018h
UART2	0282 0018h
UART3	0283 0018h
UART4	0284 0018h
UART5	0285 0018h
UART6	0286 0018h
UART7	0287 0018h
UART8	0288 0018h
UART9	0289 0018h
MCU_UART0	40A0 0018h
WKUP_UART0	4230 0018h

Figure 6-21. UART_XOFF1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XOFF_WORD1							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-48. UART_XOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	XOFF_WORD1	R/W	0h	Stores the 8-bit XOFF1 character used in UART modes

6.22 UART_TCR Register (Offset = 18h) [reset = Fh]

UART_TCR is shown in [Figure 6-22](#) and described in [Table 6-50](#).

Return to [Summary Table](#).

Transmission control register

This register stores the RX FIFO threshold levels to start/stop transmission during hardware/software flow control. Notes: Trigger levels from 0 to 60 bytes are available with a granularity of 4. (Trigger level = 4 x [4-bit register value]) The programmer must ensure that UART_TCR[3:0] > UART_TCR[7:4] when auto-RTS or software flow control is enabled to avoid a mis-operation of the device. In FIFO interrupt mode with flow control, the programmer must ensure that the trigger level to halt transmission is greater than or equal to the RX FIFO trigger level (UART_TLR[7:4] or UART_FCR[7:6]); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist because a DMA request is sent each time a byte is received.

Table 6-49. UART_TCR Instances

Instance	Physical Address
UART0	0280 0018h
UART1	0281 0018h
UART2	0282 0018h
UART3	0283 0018h
UART4	0284 0018h
UART5	0285 0018h
UART6	0286 0018h
UART7	0287 0018h
UART8	0288 0018h
UART9	0289 0018h
MCU_UART0	40A0 0018h
WKUP_UART0	4230 0018h

Figure 6-22. UART_TCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			
R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-50. UART_TCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-4	RX_FIFO_TRIG_START	R/W	0h	RX FIFO trigger level to RESTORE transmission (0 - 60)
3-0	RX_FIFO_TRIG_HALT	R/W	Fh	RX FIFO trigger level to HALT transmission (0 - 60)

6.23 UART_SPR Register (Offset = 1Ch) [reset = 0h]

UART_SPR is shown in [Figure 6-23](#) and described in [Table 6-52](#).

Return to [Summary Table](#).

Scratchpad register

This read/write register does not control the module. It is a scratchpad register to be used by the programmer to hold temporary data.

Table 6-51. UART_SPR Instances

Instance	Physical Address
UART0	0280 001Ch
UART1	0281 001Ch
UART2	0282 001Ch
UART3	0283 001Ch
UART4	0284 001Ch
UART5	0285 001Ch
UART6	0286 001Ch
UART7	0287 001Ch
UART8	0288 001Ch
UART9	0289 001Ch
MCU_UART0	40A0 001Ch
WKUP_UART0	4230 001Ch

Figure 6-23. UART_SPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SPR_WORD															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-52. UART_SPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	SPR_WORD	R/W	0h	Scratchpad register

6.24 UART_XOFF2 Register (Offset = 1Ch) [reset = 0h]

UART_XOFF2 is shown in [Figure 6-24](#) and described in [Table 6-54](#).

Return to [Summary Table](#).

UART mode XOFF2 character

Table 6-53. UART_XOFF2 Instances

Instance	Physical Address
UART0	0280 001Ch
UART1	0281 001Ch
UART2	0282 001Ch
UART3	0283 001Ch
UART4	0284 001Ch
UART5	0285 001Ch
UART6	0286 001Ch
UART7	0287 001Ch
UART8	0288 001Ch
UART9	0289 001Ch
MCU_UART0	40A0 001Ch
WKUP_UART0	4230 001Ch

Figure 6-24. UART_XOFF2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XOFF_WORD2							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-54. UART_XOFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	XOFF_WORD2	R/W	0h	Stores the 8-bit XOFF2 character used in UART modes.

6.25 UART_TLR Register (Offset = 1Ch) [reset = 0h]

UART_TLR is shown in [Figure 6-25](#) and described in [Table 6-56](#).

Return to [Summary Table](#).

Trigger level register

This register stores the programmable transmit and RX FIFO trigger levels for DMA and IRQ generation.

Table 6-55. UART_TLR Instances

Instance	Physical Address
UART0	0280 001Ch
UART1	0281 001Ch
UART2	0282 001Ch
UART3	0283 001Ch
UART4	0284 001Ch
UART5	0285 001Ch
UART6	0286 001Ch
UART7	0287 001Ch
UART8	0288 001Ch
UART9	0289 001Ch
MCU_UART0	40A0 001Ch
WKUP_UART0	4230 001Ch

Figure 6-25. UART_TLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-56. UART_TLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-4	RX_FIFO_TRIG_DMA	R/W	0h	Receive FIFO trigger level
3-0	TX_FIFO_TRIG_DMA	R/W	0h	Transmit FIFO trigger level

6.26 UART_MDR1 Register (Offset = 20h) [reset = 7h]

UART_MDR1 is shown in [Figure 6-26](#) and described in [Table 6-58](#).

[Return to Summary Table.](#)

Mode definition register 1

The mode of operation can be programmed by writing to MDR1[2:0] and therefore the UART_MDR1 must be programmed on startup after configuration of the configuration registers (UART_DLL, UART_DLH, and UART_LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to 111, interrupt requests can still be generated unless disabled through the interrupt enable register (UART_IER). In this case, UART mode interrupts are visible. Reading the interrupt identification register (UART_IIR) shows UART mode interrupt flags.

Table 6-57. UART_MDR1 Instances

Instance	Physical Address
UART0	0280 0020h
UART1	0281 0020h
UART2	0282 0020h
UART3	0283 0020h
UART4	0284 0020h
UART5	0285 0020h
UART6	0286 0020h
UART7	0287 0020h
UART8	0288 0020h
UART9	0289 0020h
MCU_UART0	40A0 0020h
WKUP_UART0	4230 0020h

Figure 6-26. UART_MDR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-7h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-58. UART_MDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	FRAME_END_MODE	R/W	0h	IrDA mode only 0h = Frame-length method 1h = Set EOT bit method

Table 6-58. UART_MDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SIP_MODE	R/W	0h	MIR/FIR modes only 0h = Manual SIP mode: SIP is generated with the control of UART_ACREG[3]. 1h = Automatic SIP mode: SIP is generated after each transmission.
5	SCT	R/W	0h	Store and control the transmission. 0h = Starts the infrared transmission when a value is written to UART_THR 1h = Starts the infrared transmission with the control of UART_ACREG[2]. Note: Before starting any transmission, there must be no reception ongoing.
4	SET_TXIR	R/W	0h	Used to configure the infrared transceiver 0h = a) No action if UART_MDR2[7] = 0 b) TXIR pin output is forced low if UART_MDR2[7] = 1. 1h = IRTX pin output is forced high (not dependent on UART_MDR2[7] value).
3	IR_SLEEP	R/W	0h	0h = IrDA/CIR sleep mode disabled 1h = IrDA/CIR sleep mode enabled
2-0	MODE_SELECT	R/W	7h	0h = UART 16x mode 1h = SIR mode 2h = UART 16x auto-baud 3h = UART 13x mode 4h = MIR mode 5h = FIR mode 6h = CIR mode 7h = Disable (default state)

6.27 UART_MDR2 Register (Offset = 24h) [reset = 0h]

UART_MDR2 is shown in [Figure 6-27](#) and described in [Table 6-60](#).

Return to [Summary Table](#).

Mode definition register 2

IR-IrDA and IR-CIR modes only. UART_MDR2[0] describes the status of the interrupt in UART_IIR[5]. The IRTX_UNDERRUN bit should be read after an UART_IIR[5] TX_STATUS_IT interrupt. The bits [2:1] of this register set the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in UART_MDR1[2:0].

Note: The UART_MDR2[6] gives the flexibility to invert the RX pin in the UART to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most transceivers invert the IR receive pin.

Table 6-59. UART_MDR2 Instances

Instance	Physical Address
UART0	0280 0024h
UART1	0281 0024h
UART2	0282 0024h
UART3	0283 0024h
UART4	0284 0024h
UART5	0285 0024h
UART6	0286 0024h
UART7	0287 0024h
UART8	0288 0024h
UART9	0289 0024h
MCU_UART0	40A0 0024h
WKUP_UART0	4230 0024h

Figure 6-27. UART_MDR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-60. UART_MDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	SET_TXIR_ALT	R/W	0h	Provide alternate function for UART_MDR1[4] (SET_TXIR). 0h = Normal mode 1h = Alternate mode for SET_TXIR

Table 6-60. UART_MDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	IRRXINVERT	R/W	0h	IR mode only (IrDA and CIR). Invert RX pin in the module before the voting or sampling system logic of the infrared block. This does not affect the RX path in UART modem modes. 0h = Inversion is performed. 1h = No inversion is performed.
5-4	CIR_PULSE_MODE	R/W	0h	CIR pulse modulation definition. Defines high level of the pulse width associated with a digit: 0h = Pulse width of 3 from 12 cycles 1h = Pulse width of 4 from 12 cycles 2h = Pulse width of 5 from 12 cycles 3h = Pulse width of 6 from 12 cycles
3	UART_PULSE	R/W	0h	UART mode only. Allows pulse shaping in UART mode. 0h = Normal UART mode 1h = UART mode with a pulse shaping
2-1	STS_FIFO_TRIG	R/W	0h	IR-IrDA mode only. Frame status FIFO threshold select: 0h = 1 entry 1h = 4 entries 2h = 7 entries 3h = 8 entries
0	IRTX_UNDERRUN	R	0h	IrDA transmission status interrupt. When the UART_IIR[5] interrupt occurs, the meaning of the interrupt is: Read 0h = The last bit of the frame transmitted successfully without error. Read 1h = An underrun occurred. The last bit of the frame was transmitted but with an underrun error. The bit is reset to 0 when the UART_RESUME register is read.

6.28 UART_SFLSR Register (Offset = 28h) [reset = 0h]

UART_SFLSR is shown in [Figure 6-28](#) and described in [Table 6-62](#).

Return to [Summary Table](#).

Status FIFO line status register

IrDA modes only. Reading this register effectively reads frame status information from the status FIFO (this register does not physically exist). Reading this register increments the status FIFO read pointer (UART_SFREGL and UART_SFREGH must be read first).

Table 6-61. UART_SFLSR Instances

Instance	Physical Address
UART0	0280 0028h
UART1	0281 0028h
UART2	0282 0028h
UART3	0283 0028h
UART4	0284 0028h
UART5	0285 0028h
UART6	0286 0028h
UART7	0287 0028h
UART8	0288 0028h
UART9	0289 0028h
MCU_UART0	40A0 0028h
WKUP_UART0	4230 0028h

Figure 6-28. UART_SFLSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 6-62. UART_SFLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-5	RESERVED	R	0h	
4	OE_ERROR	R	0h	Read 1h = Overrun error in RX FIFO when frame at top of RX FIFO was received Note: Top of RX FIFO = Next frame to be read from RX FIFO
3	FRAME_TOO_LONG_ERROR	R	0h	Read 1h = Frame-length too long error in frame at top of RX FIFO
2	ABORT_DETECT	R	0h	Read 1h = Abort pattern detected in frame at top of RX FIFO

Table 6-62. UART_SFLSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CRC_ERROR	R	0h	Read 1h = CRC error in frame at top of RX FIFO
0	RESERVED	R	0h	

6.29 UART_TXFLL Register (Offset = 28h) [reset = 0h]

UART_TXFLL is shown in [Figure 6-29](#) and described in [Table 6-64](#).

Return to [Summary Table](#).

Transmit frame length register low

IrDA modes only. The UART_TXFLL and UART_TXFLH registers hold the 13-bit transmit frame length (expressed in bytes). UART_TXFLL holds the LSBs and UART_TXFLH holds the MSBs. The frame length value is used if the frame length method of frame closing is used.

Table 6-63. UART_TXFLL Instances

Instance	Physical Address
UART0	0280 0028h
UART1	0281 0028h
UART2	0282 0028h
UART3	0283 0028h
UART4	0284 0028h
UART5	0285 0028h
UART6	0286 0028h
UART7	0287 0028h
UART8	0288 0028h
UART9	0289 0028h
MCU_UART0	40A0 0028h
WKUP_UART0	4230 0028h

Figure 6-29. UART_TXFLL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								TXFLL							
R-0h																								W-0h							

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 6-64. UART_TXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TXFLL	W	0h	LSB register used to specify the frame length

6.30 UART_RESUME Register (Offset = 2Ch) [reset = 0h]

UART_RESUME is shown in [Figure 6-30](#) and described in [Table 6-66](#).

Return to [Summary Table](#).

IR-IrDA and IR-CIR modes only. This register is used to clear internal flags, which halt transmission/reception when an underrun/overflow error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

Table 6-65. UART_RESUME Instances

Instance	Physical Address
UART0	0280 002Ch
UART1	0281 002Ch
UART2	0282 002Ch
UART3	0283 002Ch
UART4	0284 002Ch
UART5	0285 002Ch
UART6	0286 002Ch
UART7	0287 002Ch
UART8	0288 002Ch
UART9	0289 002Ch
MCU_UART0	40A0 002Ch
WKUP_UART0	4230 002Ch

Figure 6-30. UART_RESUME Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESUME															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 6-66. UART_RESUME Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RESUME	R	0h	Dummy read to restart the TX or RX

6.31 UART_TXFLH Register (Offset = 2Ch) [reset = 0h]

UART_TXFLH is shown in [Figure 6-31](#) and described in [Table 6-68](#).

Return to [Summary Table](#).

Transmit frame length register high

IrDA modes only. The UART_TXFLL and UART_TXFLH registers hold the 13-bit transmit frame length (expressed in bytes). UART_TXFLL holds the LSBs and UART_TXFLH holds the MSBs. The frame length value is used if the frame length method of frame closing is used.

Table 6-67. UART_TXFLH Instances

Instance	Physical Address
UART0	0280 002Ch
UART1	0281 002Ch
UART2	0282 002Ch
UART3	0283 002Ch
UART4	0284 002Ch
UART5	0285 002Ch
UART6	0286 002Ch
UART7	0287 002Ch
UART8	0288 002Ch
UART9	0289 002Ch
MCU_UART0	40A0 002Ch
WKUP_UART0	4230 002Ch

Figure 6-31. UART_TXFLH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED				TXFLH			
R-0h								R-0h				W-0h			

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 6-68. UART_TXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-5	RESERVED	R	0h	
4-0	TXFLH	W	0h	MSB register used to specify the frame length

6.32 UART_SFREGL Register (Offset = 30h) [reset = 0h]

UART_SFREGL is shown in [Figure 6-32](#) and described in [Table 6-70](#).

[Return to Summary Table.](#)

Status FIFO register low

IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the UART_SFREGL and UART_SFREGH registers (these registers do not physically exist). The LSBs are read from UART_SFREGL and the MSBs are read from UART_SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the UART_SFLSR register.

Table 6-69. UART_SFREGL Instances

Instance	Physical Address
UART0	0280 0030h
UART1	0281 0030h
UART2	0282 0030h
UART3	0283 0030h
UART4	0284 0030h
UART5	0285 0030h
UART6	0286 0030h
UART7	0287 0030h
UART8	0288 0030h
UART9	0289 0030h
MCU_UART0	40A0 0030h
WKUP_UART0	4230 0030h

Figure 6-32. UART_SFREGL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SFREGL							
R-0h																								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 6-70. UART_SFREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	SFREGL	R	0h	LSB part of the frame length

6.33 UART_RXFLL Register (Offset = 30h) [reset = 0h]

UART_RXFLL is shown in [Figure 6-33](#) and described in [Table 6-72](#).

Return to [Summary Table](#).

Received frame length register low

IrDA modes only. The UART_RXFLL and UART_RXFLH registers hold the 12-bit receive maximum frame length. UART_RXFLL holds the LSBs and UART_RXFLH holds the MSBs. If the intended maximum receive frame length is n bytes, program the UART_RXFLL and UART_RXFLH registers to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are the result of frame format with CRC and stop flag; 2 bytes are associated with the FIR stop flag).

Table 6-71. UART_RXFLL Instances

Instance	Physical Address
UART0	0280 0030h
UART1	0281 0030h
UART2	0282 0030h
UART3	0283 0030h
UART4	0284 0030h
UART5	0285 0030h
UART6	0286 0030h
UART7	0287 0030h
UART8	0288 0030h
UART9	0289 0030h
MCU_UART0	40A0 0030h
WKUP_UART0	4230 0030h

Figure 6-33. UART_RXFLL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								RXFLL							
R-0h																								W-0h							

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 6-72. UART_RXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RXFLL	W	0h	LSB register used to specify the frame length in reception

6.34 UART_SFREGH Register (Offset = 34h) [reset = 0h]

UART_SFREGH is shown in [Figure 6-34](#) and described in [Table 6-74](#).

Return to [Summary Table](#).

Status FIFO register high

IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the UART_SFREGL and UART_SFREGH registers (these registers do not physically exist). The LSBs are read from UART_SFREGL and the MSBs are read from UART_SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the UART_SFLSR register.

Table 6-73. UART_SFREGH Instances

Instance	Physical Address
UART0	0280 0034h
UART1	0281 0034h
UART2	0282 0034h
UART3	0283 0034h
UART4	0284 0034h
UART5	0285 0034h
UART6	0286 0034h
UART7	0287 0034h
UART8	0288 0034h
UART9	0289 0034h
MCU_UART0	40A0 0034h
WKUP_UART0	4230 0034h

Figure 6-34. UART_SFREGH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED				SFREGH			
R-0h								R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 6-74. UART_SFREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-4	RESERVED	R	0h	
3-0	SFREGH	R	0h	MSB part of the frame length

6.35 UART_RXFLH Register (Offset = 34h) [reset = 0h]

UART_RXFLH is shown in [Figure 6-35](#) and described in [Table 6-76](#).

Return to [Summary Table](#).

Received frame length register high

IrDA modes only. The UART_RXFLH and UART_RXFLH registers hold the 12-bit receive maximum frame length. UART_RXFLH holds the LSBs and UART_RXFLH holds the MSBs. If the intended maximum receive frame length is n bytes, program the UART_RXFLH and UART_RXFLH to be $n + 3$ in SIR or MIR modes and $n + 6$ in FIR mode (+3 and +6 are the result of frame format with CRC and stop flag; 2 bytes are associated with the FIR stop flag).

Table 6-75. UART_RXFLH Instances

Instance	Physical Address
UART0	0280 0034h
UART1	0281 0034h
UART2	0282 0034h
UART3	0283 0034h
UART4	0284 0034h
UART5	0285 0034h
UART6	0286 0034h
UART7	0287 0034h
UART8	0288 0034h
UART9	0289 0034h
MCU_UART0	40A0 0034h
WKUP_UART0	4230 0034h

Figure 6-35. UART_RXFLH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED				RXFLH			
R-0h								R-0h				W-0h			

LEGEND: R = Read Only; W = Write Only; - n = value after reset

Table 6-76. UART_RXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-4	RESERVED	R	0h	
3-0	RXFLH	W	0h	MSB register used to specify the frame length in reception

6.36 UART_BLR Register (Offset = 38h) [reset = 40h]

UART_BLR is shown in [Figure 6-36](#) and described in [Table 6-78](#).

Return to [Summary Table](#).

BOF control register

IrDA modes only. The UART_BLR[6] bit selects whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR mode. If only one start flag is required, this is always 0xC0. If n start flags are required, (-1) 0xC0 or (-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

Table 6-77. UART_BLR Instances

Instance	Physical Address
UART0	0280 0038h
UART1	0281 0038h
UART2	0282 0038h
UART3	0283 0038h
UART4	0284 0038h
UART5	0285 0038h
UART6	0286 0038h
UART7	0287 0038h
UART8	0288 0038h
UART9	0289 0038h
MCU_UART0	40A0 0038h
WKUP_UART0	4230 0038h

Figure 6-36. UART_BLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
STS_FIFO_RE SET	XBOF_TYPE	RESERVED					
R/W1S-0h	R/W-1h	R-0h					

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 6-78. UART_BLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	STS_FIFO_RESET	R/W1S	0h	Status FIFO reset. This bit is self-clearing.
6	XBOF_TYPE	R/W	1h	SIR xBOF select 0h = 0xFF 1h = 0xC0
5-0	RESERVED	R	0h	

6.37 UART_UASR Register (Offset = 38h) [reset = 0h]

UART_UASR is shown in [Figure 6-37](#) and described in [Table 6-80](#).

Return to [Summary Table](#).

UART autobauding status register

UART autobauding mode only. This status register returns the speed, the number of bits by characters, and the type of the parity in UART autobauding mode. In autobauding mode, the input frequency of the UART modem must be fixed to 48 MHz. Any other module clock frequency results in incorrect baud rate recognition.

Note: When the UART is in autobauding mode, this register, instead of the UART_LCR, UART_DLL, and UART_DLH registers, is used to set up transmission according to the characteristics of the previous reception.

To reset the autobauding hardware (to start a new AT detection), set UART_MDR1[2:0] to 111 (reset value), then set UART_MDR1[2:1] to 010 (UART in autobaud mode).

To set the UART to standard mode (no autobaud), set UART_MDR1[2:1] to 000.

Table 6-79. UART_UASR Instances

Instance	Physical Address
UART0	0280 0038h
UART1	0281 0038h
UART2	0282 0038h
UART3	0283 0038h
UART4	0284 0038h
UART5	0285 0038h
UART6	0286 0038h
UART7	0287 0038h
UART8	0288 0038h
UART9	0289 0038h
MCU_UART0	40A0 0038h
WKUP_UART0	4230 0038h

Figure 6-37. UART_UASR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
PARITY_TYPE		BIT_BY_CHAR		SPEED			
R-0h		R-0h		R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 6-80. UART_UASR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	

Table 6-80. UART_UASR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	PARITY_TYPE	R	0h	Read 0h = No parity identified Read 1h = Parity space Read 2h = Even parity Read 3h = Odd parity
5	BIT_BY_CHAR	R	0h	Read 0h = 7-bit character identified Read 1h = 8-bit character identified
4-0	SPEED	R	0h	Used to report the speed identified Read 0h = No speed identified Read 1h = 115,200 baud Read 2h = 57,600 baud Read 3h = 38,400 baud Read 4h = 28,800 baud Read 5h = 19,200 baud Read 6h = 14,400 baud Read 7h = 9,600 baud Read 8h = 4,800 baud Read 9h = 2,400 baud Read Ah = 1,200 baud

6.38 UART_ACREG Register (Offset = 3Ch) [reset = 0h]

UART_ACREG is shown in [Figure 6-38](#) and described in [Table 6-82](#).

[Return to Summary Table.](#)

Auxiliary control register. IR-IrDA and IR-CIR modes only.

Table 6-81. UART_ACREG Instances

Instance	Physical Address
UART0	0280 003Ch
UART1	0281 003Ch
UART2	0282 003Ch
UART3	0283 003Ch
UART4	0284 003Ch
UART5	0285 003Ch
UART6	0286 003Ch
UART7	0287 003Ch
UART8	0288 003Ch
UART9	0289 003Ch
MCU_UART0	40A0 003Ch
WKUP_UART0	4230 003Ch

Figure 6-38. UART_ACREG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDE RRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W1S-0h	R/W1S-0h	R/W-0h	R/W1S-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 6-82. UART_ACREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	PULSE_TYPE	R/W	0h	SIR pulse width select 0h = 3/16 of baud-rate pulse width 1h = 1.6 μ s
6	SD_MOD	R/W	0h	Primary output used to configure transceivers. Connected to the SD/ MODE input pin of IrDA transceivers. 0h = SD pin is set to high. 1h = SD pin is set to low.
5	DIS_IR_RX	R/W	0h	0h = Normal operation (RX input automatically disabled during transmit but enabled outside of transmit operation) 1h = Disables RX input (permanent state - independent of transmit)

Table 6-82. UART_ACREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DIS_TX_UNDERRUN	R/W	0h	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting UART_ACREG[4] = 1, garbage data is sent over TX line. 0h = Long stop-bits cannot be transmitted; TX underrun is enabled. 1h = Long stop-bits can be transmitted; TX underrun is disabled.
3	SEND_SIP	R/W1S	0h	MIR/FIR modes only. Send serial infrared interaction pulse (SIP). If this bit is set during an MIR/FIR transmission, the SIP is sent at the end of it. This bit is cleared automatically at the end of the SIP transmission. 0h = No action 1h = Send SIP pulse.
2	SCTX_EN	R/W1S	0h	Store and controlled TX start. When UART_MDR1[5] = 1 and the LH writes 1 to this bit, the TX state-machine starts frame transmission. This bit is self-clearing.
1	ABORT_EN	R/W	0h	Frame abort. The LH can intentionally abort transmission of a frame by writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If TX FIFO is not empty and UART_MDR1[5] = 1, UART IrDA starts a new transfer with data of the previous frame when the abort frame is sent. Therefore, TX FIFO must be reset before sending an abort frame.
0	EOT_EN	R/W1S	0h	EOT (end of transmission) bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit is cleared automatically when the LH writes to the THR (TX FIFO).

6.39 UART_SCR Register (Offset = 40h) [reset = 0h]

UART_SCR is shown in [Figure 6-39](#) and described in [Table 6-84](#).

[Return to Summary Table.](#)

Supplementary control register

Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the UART_IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the UART_IIR register, the UART_SSR[1] bit must be checked. To clear the wake-up interrupt, bit UART_SCR[4] must be reset to 0.

Table 6-83. UART_SCR Instances

Instance	Physical Address
UART0	0280 0040h
UART1	0281 0040h
UART2	0282 0040h
UART3	0283 0040h
UART4	0284 0040h
UART5	0285 0040h
UART6	0286 0040h
UART7	0287 0040h
UART8	0288 0040h
UART9	0289 0040h
MCU_UART0	40A0 0040h
WKUP_UART0	4230 0040h

Figure 6-39. UART_SCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RX_TRIG_GRA NU1	TX_TRIG_GRA NU1	DSR_IT	RX_CTS_DSR_ WAKE_UP_EN ABLE	TX_EMPTY_CT L_IT	DMA_MODE_2		DMA_MODE_C TL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-84. UART_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	RX_TRIG_GRANU1	R/W	0h	0h = Disables the granularity of 1 for trigger RX level 1h = Enables the granularity of 1 for trigger RX level
6	TX_TRIG_GRANU1	R/W	0h	0h = Disables the granularity of 1 for trigger TX level 1h = Enables the granularity of 1 for trigger TX level
5	DSR_IT	R/W	0h	0h = Disables DSR* interrupt 1h = Enables DSR* interrupt

Table 6-84. UART_SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RX_CTS_DSR_WAKE_UP_ENABLE	R/W	0h	0h = Disables the wake-up interrupt and clears SSR[1] 1h = Waits for a falling edge of pins RX, CTS*, or DSR* to generate an interrupt
3	TX_EMPTY_CTL_IT	R/W	0h	0h = Normal mode for THR interrupt 1h = The THR interrupt is generated when TX FIFO and TX shift register are empty.
2-1	DMA_MODE_2	R/W	0h	Used to specify the DMA mode valid if the UART_SCR[0] bit = 1 0h = DMA mode 0 (no DMA) 1h = DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX) 2h = DMA mode 2 (UART_nDMA_REQ[0] in RX) 3h = DMA mode 3 (UART_nDMA_REQ[0] in TX)
0	DMA_MODE_CTL	R/W	0h	0h = The DMA_MODE is set with UART_FCR[3]. 1h = The DMA_MODE is set with UART_SCR[2:1].

6.40 UART_SSR Register (Offset = 44h) [reset = 4h]

UART_SSR is shown in [Figure 6-40](#) and described in [Table 6-86](#).

Return to [Summary Table](#).

Supplementary status register

Note: Bit 1 is reset only when UART_SCR[4] is reset to 0.

Table 6-85. UART_SSR Instances

Instance	Physical Address
UART0	0280 0044h
UART1	0281 0044h
UART2	0282 0044h
UART3	0283 0044h
UART4	0284 0044h
UART5	0285 0044h
UART6	0286 0044h
UART7	0287 0044h
UART8	0288 0044h
UART9	0289 0044h
MCU_UART0	40A0 0044h
WKUP_UART0	4230 0044h

Figure 6-40. UART_SSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL
R-0h					R/W-1h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-86. UART_SSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-3	RESERVED	R	0h	
2	DMA_COUNTER_RST	R/W	1h	0h = The DMA counter will not be reset if the corresponding FIFO is reset (through UART_FCR[1] or UART_FCR[2]). 1h = The DMA counter will be reset if corresponding FIFO is reset (through UART_FCR[1] or UART_FCR[2]).
1	RX_CTS_DSR_WAKE_UP_STS	R	0h	Read 0h = No falling edge event on RX, CTS*, and DSR* Read 1h = A falling edge occurred on RX, CTS*, or DSR*.

Table 6-86. UART_SSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TX_FIFO_FULL	R	0h	Read 0h = TX FIFO is not full. Read 1h = TX FIFO is full.

6.41 UART_EBLR Register (Offset = 48h) [reset = 0h]

UART_EBLR is shown in [Figure 6-41](#) and described in [Table 6-88](#).

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BOF length register

IR-IrDA and IR-CIR modes only. In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must account for the BOF character; therefore, to send only one BOF with no XBOF, this register must be set to 1. To send one BOF with N XBOF, this register must be set to N + 1. The value 0 sends 1 BOF plus 255 XBOF. In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags). In IR-CIR mode, this register specifies the number of consecutive 0s to be received before generating the RX_STOP interrupt (UART_IIR[2]). All received 0s are stored in the RX FIFO. When the register is set to 0, this feature is deactivated and always in reception state, which can be disabled by setting the UART_ACREG[5] to 1.

Note: If the RX_STOP interrupt occurs before a byte boundary, the remaining bits of the last byte are filled with 0s and passed into the RX FIFO.

Table 6-87. UART_EBLR Instances

Instance	Physical Address
UART0	0280 0048h
UART1	0281 0048h
UART2	0282 0048h
UART3	0283 0048h
UART4	0284 0048h
UART5	0285 0048h
UART6	0286 0048h
UART7	0287 0048h
UART8	0288 0048h
UART9	0289 0048h
MCU_UART0	40A0 0048h
WKUP_UART0	4230 0048h

Figure 6-41. UART_EBLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EBLR							
R-0h																								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-88. UART_EBLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	EBLR	R/W	0h	IR-IrDA mode: This register allows definition of up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive 0s to be received before generating the RX_STOP interrupt (UART_IIR[2]). 00h = Feature disabled 01h = Generate RX_STOP interrupt after receiving one zero bit. ... FFh = Generate RX_STOP interrupt after receiving 255 zero bits.

6.42 UART_MVR Register (Offset = 50h) [reset = 47423E03h]

UART_MVR is shown in [Figure 6-42](#) and described in [Table 6-90](#).

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Module version register

The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned.

Table 6-89. UART_MVR Instances

Instance	Physical Address
UART0	0280 0050h
UART1	0281 0050h
UART2	0282 0050h
UART3	0283 0050h
UART4	0284 0050h
UART5	0285 0050h
UART6	0286 0050h
UART7	0287 0050h
UART8	0288 0050h
UART9	0289 0050h
MCU_UART0	40A0 0050h
WKUP_UART0	4230 0050h

Figure 6-42. UART_MVR Register

31	30	29	28	27	26	25	24
SCHEME		RESERVED		FUNC			
R-1h		R-0h		R-742h			
23	22	21	20	19	18	17	16
FUNC							
R-742h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
7h					R-6h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R-0h		R-3h					

LEGEND: R = Read Only; -n = value after reset

Table 6-90. UART_MVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme revision number of module
29-28	RESERVED	R	0h	
27-16	FUNC	R	742h	Function revision number of module
15-11	RTL	R	7h	Rtl revision number of module
10-8	MAJOR	R	6h	Major revision number of the module
7-6	CUSTOM	R	0h	Custom revision number of the module
5-0	MINOR	R	3h	Minor revision number of the module

6.43 UART_SYSC Register (Offset = 54h) [reset = 0h]

UART_SYSC is shown in [Figure 6-43](#) and described in [Table 6-92](#).

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System configuration register

The AUTOIDLE bit controls a power-saving technique to reduce the logic power consumption of the open-core protocol (OCP) interface. When the feature is enabled, the clock is gated off until an OCP command for this device is detected. When the software reset bit is set high, it causes a full device reset.

Table 6-91. UART_SYSC Instances

Instance	Physical Address
UART0	0280 0054h
UART1	0281 0054h
UART2	0282 0054h
UART3	0283 0054h
UART4	0284 0054h
UART5	0285 0054h
UART6	0286 0054h
UART7	0287 0054h
UART8	0288 0054h
UART9	0289 0054h
MCU_UART0	40A0 0054h
WKUP_UART0	4230 0054h

Figure 6-43. UART_SYSC Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R-0h			R/W-0h		R/W-0h	W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 6-92. UART_SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-5	RESERVED	R	0h	

Table 6-92. UART_SYSC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	IDLEMODE	R/W	0h	Power management req/ack control ref: OCP Design Guidelines Version 1.1 0h = Force-idle: Idle request is acknowledged unconditionally. 1h = No-idle: Idle request is never acknowledged. 2h = Smart-idle: Idle request is acknowledged based in module internal activity. 3h = Smart-idle Wake-up: Acknowledgement to an idle request is given based in the internal activity of the module. The module is allowed to generate wake-up request.
2	ENAWAKEUP	R/W	0h	Wake-up feature control 0h = Wakeup is disabled. 1h = Wake-up capability is enabled.
1	SOFTRESET	W	0h	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. Read returns 0. 0h = Normal mode 1h = The module is reset.
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy 0h = Clock is running. 1h = Automatic OCP clock gating strategy is applied, based on OCP interface activity

6.44 UART_SYSS Register (Offset = 58h) [reset = 0h]

UART_SYSS is shown in [Figure 6-44](#) and described in [Table 6-94](#).

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System status register

Table 6-93. UART_SYSS Instances

Instance	Physical Address
UART0	0280 0058h
UART1	0281 0058h
UART2	0282 0058h
UART3	0283 0058h
UART4	0284 0058h
UART5	0285 0058h
UART6	0286 0058h
UART7	0287 0058h
UART8	0288 0058h
UART9	0289 0058h
MCU_UART0	40A0 0058h
WKUP_UART0	4230 0058h

Figure 6-44. UART_SYSS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 6-94. UART_SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-1	RESERVED	R	0h	
0	RESETDONE	R	0h	Internal reset monitoring Read 0h = Internal module reset is ongoing. Read 1h = Reset complete

6.45 UART_WER Register (Offset = 5Ch) [reset = FFh]

UART_WER is shown in [Figure 6-45](#) and described in [Table 6-96](#).

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Wake-up enable register

The UART wake-up enable register is used to mask and unmask a UART event that would subsequently notify the system. An event is any activity in the logic that could cause an interrupt and/or an activity that would require the system to wake up. Even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, the UART registers the interrupt.

Table 6-95. UART_WER Instances

Instance	Physical Address
UART0	0280 005Ch
UART1	0281 005Ch
UART2	0282 005Ch
UART3	0283 005Ch
UART4	0284 005Ch
UART5	0285 005Ch
UART6	0286 005Ch
UART7	0287 005Ch
UART8	0288 005Ch
UART9	0289 005Ch
MCU_UART0	40A0 005Ch
WKUP_UART0	4230 005Ch

Figure 6-45. UART_WER Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
EVENT_7_TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RIACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-96. UART_WER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	EVENT_7_TX_WAKEUP_EN	R/W	1h	0h = Event is not allowed to wake up the system. 1h = Event can wake up the system: it can be THR_IT or TX_DMA request and/or TX_STATUS_IT.

Table 6-96. UART_WER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	R/W	1h	0h = Event is not allowed to wake up the system. 1h = Event can wake up the system.
5	EVENT_5_RHR_INTERRUPT	R/W	1h	0h = Event is not allowed to wake up the system. 1h = Event can wake up the system.
4	EVENT_4_RX_ACTIVITY	R/W	1h	0h = Event is not allowed to wake up the system. 1h = Event can wake up the system.
3	EVENT_3_DCD_CD_ACTIVITY	R/W	1h	0h = Event is not allowed to wake up the system 1h = Event can wake up the system
2	EVENT_2_RI_ACTIVITY	R/W	1h	0h = Event is not allowed to wake up the system. 1h = Event can wake up the system.
1	EVENT_1_DSR_ACTIVITY	R/W	1h	0h = Event is not allowed to wake up the system. 1h = Event can wake up the system.
0	EVENT_0_CTS_ACTIVITY	R/W	1h	0h = Event is not allowed to wake up the system. 1h = Event can wake up the system.

6.46 UART_CFPS Register (Offset = 60h) [reset = 69h]

UART_CFPS is shown in [Figure 6-46](#) and described in [Table 6-98](#).

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Carrier frequency prescaler

Because the consumer IR works at modulation rates of 30 to 56.8 kHz, the 48-MHz clock must be prescaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote-control requirements in baud multiples of 12x. The value of the CFPS at reset is 0105 decimal, which equals 38.1 kHz output from starting conditions. The 48-MHz carrier is prescaled by the CFPS, which is then divided by the 12x baud multiple.

Table 6-97. UART_CFPS Instances

Instance	Physical Address
UART0	0280 0060h
UART1	0281 0060h
UART2	0282 0060h
UART3	0283 0060h
UART4	0284 0060h
UART5	0285 0060h
UART6	0286 0060h
UART7	0287 0060h
UART8	0288 0060h
UART9	0289 0060h
MCU_UART0	40A0 0060h
WKUP_UART0	4230 0060h

Figure 6-46. UART_CFPS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CFPS							
R-0h																								R/W-69h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-98. UART_CFPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	CFPS	R/W	69h	System clock frequency prescaler at (12x multiple). Examples for CFPS values: 85h = 30 kHz Target Freq; 30.08 kHz Actual Freq 7Ah = 32.75 kHz Target Freq; 32.79 kHz Actual Freq 6Fh = 36 kHz Target Freq; 36.04 kHz Actual Freq 6Dh = 36.7 kHz Target Freq; 36.69 kHz Actual Freq 69h = 38 kHz Target Freq; 38.1 kHz Actual Freq 64h = 40 kHz Target Freq; 40 kHz Actual Freq 46h = 56.8 kHz Target Freq; 57.14 kHz Actual Freq Note: CFPS = 0 is not supported.

6.47 UART_RXFIFO_LVL Register (Offset = 64h) [reset = 0h]

UART_RXFIFO_LVL is shown in [Figure 6-47](#) and described in [Table 6-100](#).

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Level of the RX FIFO

Table 6-99. UART_RXFIFO_LVL Instances

Instance	Physical Address
UART0	0280 0064h
UART1	0281 0064h
UART2	0282 0064h
UART3	0283 0064h
UART4	0284 0064h
UART5	0285 0064h
UART6	0286 0064h
UART7	0287 0064h
UART8	0288 0064h
UART9	0289 0064h
MCU_UART0	40A0 0064h
WKUP_UART0	4230 0064h

Figure 6-47. UART_RXFIFO_LVL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RXFIFO_LVL							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 6-100. UART_RXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	RXFIFO_LVL	R	0h	Shows the number of received bytes in the RX FIFO

6.48 UART_TXFIFO_LVL Register (Offset = 68h) [reset = 0h]

UART_TXFIFO_LVL is shown in [Figure 6-48](#) and described in [Table 6-102](#).

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Level of the TX FIFO

Table 6-101. UART_TXFIFO_LVL Instances

Instance	Physical Address
UART0	0280 0068h
UART1	0281 0068h
UART2	0282 0068h
UART3	0283 0068h
UART4	0284 0068h
UART5	0285 0068h
UART6	0286 0068h
UART7	0287 0068h
UART8	0288 0068h
UART9	0289 0068h
MCU_UART0	40A0 0068h
WKUP_UART0	4230 0068h

Figure 6-48. UART_TXFIFO_LVL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TXFIFO_LVL							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 6-102. UART_TXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TXFIFO_LVL	R	0h	Shows the number of written bytes in the TX FIFO

6.49 UART_IER2 Register (Offset = 6Ch) [reset = 0h]

UART_IER2 is shown in [Figure 6-49](#) and described in [Table 6-104](#).

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Enables RX/TX FIFOs empty corresponding interrupts

Table 6-103. UART_IER2 Instances

Instance	Physical Address
UART0	0280 006Ch
UART1	0281 006Ch
UART2	0282 006Ch
UART3	0283 006Ch
UART4	0284 006Ch
UART5	0285 006Ch
UART6	0286 006Ch
UART7	0287 006Ch
UART8	0288 006Ch
UART9	0289 006Ch
MCU_UART0	40A0 006Ch
WKUP_UART0	4230 006Ch

Figure 6-49. UART_IER2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-104. UART_IER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-2	RESERVED	R	0h	
2	RHR_IT_DIS	R/W	0h	0h = Enables the RHR interrupt. 1h = Disables the RHR interrupt.
1	EN_TXFIFO_EMPTY	R/W	0h	Enables TX FIFO empty corresponding interrupt 0h = Disables EN_TXFIFO_EMPTY interrupt 1h = Enables EN_TXFIFO_EMPTY interrupt

Table 6-104. UART_IER2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EN_RXFIFO_EMPTY	R/W	0h	Enables RX FIFO empty corresponding interrupt 0h = Disables EN_RXFIFO_EMPTY interrupt 1h = Enables EN_RXFIFO_EMPTY interrupt

6.50 UART_ISR2 Register (Offset = 70h) [reset = 3h]

UART_ISR2 is shown in [Figure 6-50](#) and described in [Table 6-106](#).

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Status of RX/TX FIFOs empty corresponding interrupts

Table 6-105. UART_ISR2 Instances

Instance	Physical Address
UART0	0280 0070h
UART1	0281 0070h
UART2	0282 0070h
UART3	0283 0070h
UART4	0284 0070h
UART5	0285 0070h
UART6	0286 0070h
UART7	0287 0070h
UART8	0288 0070h
UART9	0289 0070h
MCU_UART0	40A0 0070h
WKUP_UART0	4230 0070h

Figure 6-50. UART_ISR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TXFIFO_EMPTY_STS	RXFIFO_EMPTY_STS
R-0h						R/W1C-1h	R/W1C-1h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 6-106. UART_ISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-2	RESERVED	R	0h	
1	TXFIFO_EMPTY_STS	R/W1C	1h	Used to generate interrupt if the TX_FIFO is empty (software flow control) 0h = TXFIFO_EMPTY interrupt not pending. 1h = TXFIFO_EMPTY interrupt pending.
0	RXFIFO_EMPTY_STS	R/W1C	1h	Used to generate interrupt if the RX_FIFO is empty (software flow control) 0h = RXFIFO_EMPTY interrupt not pending. 1h = RXFIFO_EMPTY interrupt pending.

6.51 UART_FREQ_SEL Register (Offset = 74h) [reset = 1Ah]

UART_FREQ_SEL is shown in [Figure 6-51](#) and described in [Table 6-108](#).

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Sample per bit selector

Table 6-107. UART_FREQ_SEL Instances

Instance	Physical Address
UART0	0280 0074h
UART1	0281 0074h
UART2	0282 0074h
UART3	0283 0074h
UART4	0284 0074h
UART5	0285 0074h
UART6	0286 0074h
UART7	0287 0074h
UART8	0288 0074h
UART9	0289 0074h
MCU_UART0	40A0 0074h
WKUP_UART0	4230 0074h

Figure 6-51. UART_FREQ_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								FREQ_SEL							
R-0h																								R/W-1Ah							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-108. UART_FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	RESERVED
7-0	FREQ_SEL	R/W	1Ah	Sets the sample per bit if nondefault frequency is used. UART_MDR3[1] must be set to 1 after this value is set. Must be equal to or higher than 6.

6.52 UART_ABAUD_1ST_CHAR Register (Offset = 78h) [reset = 0h]

UART_ABAUD_1ST_CHAR is shown in [Figure 6-52](#) and described in [Table 6-110](#).

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Unused

Table 6-109. UART_ABAUD_1ST_CHAR Instances

Instance	Physical Address
UART0	0280 0078h
UART1	0281 0078h
UART2	0282 0078h
UART3	0283 0078h
UART4	0284 0078h
UART5	0285 0078h
UART6	0286 0078h
UART7	0287 0078h
UART8	0288 0078h
UART9	0289 0078h
MCU_UART0	40A0 0078h
WKUP_UART0	4230 0078h

Figure 6-52. UART_ABAUD_1ST_CHAR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 6-110. UART_ABAUD_1ST_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	

6.53 UART_BAUD_2ND_CHAR Register (Offset = 7Ch) [reset = 0h]

UART_BAUD_2ND_CHAR is shown in [Figure 6-53](#) and described in [Table 6-112](#).

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Unused

Table 6-111. UART_BAUD_2ND_CHAR Instances

Instance	Physical Address
UART0	0280 007Ch
UART1	0281 007Ch
UART2	0282 007Ch
UART3	0283 007Ch
UART4	0284 007Ch
UART5	0285 007Ch
UART6	0286 007Ch
UART7	0287 007Ch
UART8	0288 007Ch
UART9	0289 007Ch
MCU_UART0	40A0 007Ch
WKUP_UART0	4230 007Ch

Figure 6-53. UART_BAUD_2ND_CHAR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 6-112. UART_BAUD_2ND_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	

6.54 UART_MDR3 Register (Offset = 80h) [reset = 0h]

UART_MDR3 is shown in [Figure 6-54](#) and described in [Table 6-114](#).

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Mode definition register 3

Table 6-113. UART_MDR3 Instances

Instance	Physical Address
UART0	0280 0080h
UART1	0281 0080h
UART2	0282 0080h
UART3	0283 0080h
UART4	0284 0080h
UART5	0285 0080h
UART6	0286 0080h
UART7	0287 0080h
UART8	0288 0080h
UART9	0289 0080h
MCU_UART0	40A0 0080h
WKUP_UART0	4230 0080h

Figure 6-54. UART_MDR3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			DIR_EN	DIR_POL	SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-114. UART_MDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-5	RESERVED	R	0h	Reserved
4	DIR_EN	R/W	0h	RS-485 External Transceiver Direction Enable
3	DIR_POL	R/W	0h	RS-485 External Transceiver Direction Polarity. 0h = TX: RTS=0, RX: RTS=1. 1h = TX: RTS=1, RX: RTS=0
2	SET_DMA_TX_THRESHOLD	R/W	0h	Enable to set different TXDMA threshold in UART_TX_DMA_THRESHOLD register.

Table 6-114. UART_MDR3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	NONDEFAULT_FREQ	R/W	0h	Used to enable the NONDEFAULT fclk frequencies. 0h = Disables using NONDEFAULT fclk frequencies. 1h = Enables using NONDEFAULT fclk frequencies (set UART_FREQ_SEL and UART_DLH/UART_DLL).
0	DISABLE_CIR_RX_DEMOD	R/W	0h	Used to enable CIR RX demodulation. 0h = Enables CIR RX demodulation. 1h = Disables CIR RX demodulation.

6.55 UART_TX_DMA_THRESHOLD Register (Offset = 84h) [reset = 0h]

UART_TX_DMA_THRESHOLD is shown in [Figure 6-55](#) and described in [Table 6-116](#).

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Use to manually set the TX DMA threshold level. UART_MDR3[2] SET_TX_DMA_THRESHOLD must be 1 and must be value + tx_trigger_level = 64 (TX FIFO size). If not, 64-tx_trigger_level will be used without modifying the value of this register.

**Table 6-115. UART_TX_DMA_THRESHOLD
Instances**

Instance	Physical Address
UART0	0280 0084h
UART1	0281 0084h
UART2	0282 0084h
UART3	0283 0084h
UART4	0284 0084h
UART5	0285 0084h
UART6	0286 0084h
UART7	0287 0084h
UART8	0288 0084h
UART9	0289 0084h
MCU_UART0	40A0 0084h
WKUP_UART0	4230 0084h

Figure 6-55. UART_TX_DMA_THRESHOLD Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		TX_DMA_THRESHOLD					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-116. UART_TX_DMA_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-6	RESERVED	R	0h	
5-0	TX_DMA_THRESHOLD	R/W	0h	Used to manually set the TX DMA threshold level

6.56 UART_MDR4 Register (Offset = 88h) [reset = 0h]

UART_MDR4 is shown in [Figure 6-56](#) and described in [Table 6-118](#).

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Mode definition register 4

Table 6-117. UART_MDR4 Instances

Instance	Physical Address
UART0	0280 0088h
UART1	0281 0088h
UART2	0282 0088h
UART3	0283 0088h
UART4	0284 0088h
UART5	0285 0088h
UART6	0286 0088h
UART7	0287 0088h
UART8	0288 0088h
UART9	0289 0088h
MCU_UART0	40A0 0088h
WKUP_UART0	4230 0088h

Figure 6-56. UART_MDR4 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	MODE9	FREQ_SEL_H			MODE		
R-0h	R/W-0h	R/W-0h			R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-118. UART_MDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	MODE9	R/W	0h	9-bit character length When '1', overrides character length setting in UART_LCR
5-3	FREQ_SEL_H	R/W	0h	Upper 3 bits of UART_FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode

Table 6-118. UART_MDR4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MODE	R/W	0h	<p>New modes [when set, overrides UART_MDR1 modes]</p> <p>0h = Disabled (no override)</p> <p>1h = Reserved</p> <p>2h = Synchronous mode with external clock</p> <p>3h = Synchronous mode with generated clock</p> <p>4h = ISO 7816 mode T=0</p> <p>5h = ISO 7816 mode T=1</p> <p>6h = Reserved</p> <p>7h = Reserved</p>

6.57 UART_EFR2 Register (Offset = 8Ch) [reset = 0h]

UART_EFR2 is shown in [Figure 6-57](#) and described in [Table 6-120](#).

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Enhanced Features Register 2

Table 6-119. UART_EFR2 Instances

Instance	Physical Address
UART0	0280 008Ch
UART1	0281 008Ch
UART2	0282 008Ch
UART3	0283 008Ch
UART4	0284 008Ch
UART5	0285 008Ch
UART6	0286 008Ch
UART7	0287 008Ch
UART8	0288 008Ch
UART9	0289 008Ch
MCU_UART0	40A0 008Ch
WKUP_UART0	4230 008Ch

Figure 6-57. UART_EFR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
BROADCAST	TIMEOUT_BEH AVE	C8	C4	C2	MULTIDROP	RHR_OVERRU N	ENDIAN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-120. UART_EFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	BROADCAST	R/W	0h	Enables broadcast address matching in multi-drop address match mode
6	TIMEOUT_BEHAVE	R/W	0h	Specifies how timeout is measured 0h = Timeout after at least one character has been received 1h = Periodic timeout even when no character has been received
5	C8	R/W	0h	Value for ISO 7816 C8 pin for software control
4	C4	R/W	0h	Value for ISO 7816 C4 pin for software control
3	C2	R/W	0h	Value for ISO 7816 reset pin [software controllable]
2	MULTIDROP	R/W	0h	Enables parity Multi-drop mode [overrides UART_LCR[5..3]] when '1'

Table 6-120. UART_EFR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RHR_OVERRUN	R/W	0h	UART_RHR Overrun behavior when buffer full 0h = Data in RHR is not overwritten (standard) 1h = Data in RHR is overwritten when buffer full (and FIFO disabled)
0	ENDIAN	R/W	0h	Endianness 0h = Little Endian (LSB First) 1h = Big Endian (MSB First)

6.58 UART_ECR Register (Offset = 90h) [reset = 18h]

UART_ECR is shown in [Figure 6-58](#) and described in [Table 6-122](#).

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Enhanced Control register

Table 6-121. UART_ECR Instances

Instance	Physical Address
UART0	0280 0090h
UART1	0281 0090h
UART2	0282 0090h
UART3	0283 0090h
UART4	0284 0090h
UART5	0285 0090h
UART6	0286 0090h
UART7	0287 0090h
UART8	0288 0090h
UART9	0289 0090h
MCU_UART0	40A0 0090h
WKUP_UART0	4230 0090h

Figure 6-58. UART_ECR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	CLEAR_TX_PE	TX_EN	RX_EN	TX_RST	RX_RST	A_MULTIDROP	
R-0h	W-0h	R/W-1h	R/W-1h	W-0h	W-0h	W-0h	

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 6-122. UART_ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-6	RESERVED	R	0h	
5	CLEAR_TX_PE	W	0h	Write 1h = to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only]
4	TX_EN	R/W	1h	Enables/Disables the transmitter 0h = DISABLED (Transmitter is shut down) 1h = ENABLED (Transmitter is working)
3	RX_EN	R/W	1h	Enables/Disables the receiver 0h = DISABLED (Receiver is shut down) 1h = ENABLED (Receiver is operating)
2	TX_RST	W	0h	Writing 1h = resets the transmitter

Table 6-122. UART_ECR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RX_RST	W	0h	Writing 1h = resets the receiver
0	A_MULTIDROP	W	0h	In multi-drop mode, when written with the value '1' causes the next byte written into UART_THR to be transmitted with the parity bit set, signaling an address

6.59 UART_TIMEGUARD Register (Offset = 94h) [reset = 0h]

UART_TIMEGUARD is shown in [Figure 6-59](#) and described in [Table 6-124](#).

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Timeguard

Table 6-123. UART_TIMEGUARD Instances

Instance	Physical Address
UART0	0280 0094h
UART1	0281 0094h
UART2	0282 0094h
UART3	0283 0094h
UART4	0284 0094h
UART5	0285 0094h
UART6	0286 0094h
UART7	0287 0094h
UART8	0288 0094h
UART9	0289 0094h
MCU_UART0	40A0 0094h
WKUP_UART0	4230 0094h

Figure 6-59. UART_TIMEGUARD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEGUARD							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-124. UART_TIMEGUARD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TIMEGUARD	R/W	0h	Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when communicating with slower devices

6.60 UART_TIMEOUTL Register (Offset = 98h) [reset = 0h]

UART_TIMEOUTL is shown in [Figure 6-60](#) and described in [Table 6-126](#).

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Timeout lower byte

Table 6-125. UART_TIMEOUTL Instances

Instance	Physical Address
UART0	0280 0098h
UART1	0281 0098h
UART2	0282 0098h
UART3	0283 0098h
UART4	0284 0098h
UART5	0285 0098h
UART6	0286 0098h
UART7	0287 0098h
UART8	0288 0098h
UART9	0289 0098h
MCU_UART0	40A0 0098h
WKUP_UART0	4230 0098h

Figure 6-60. UART_TIMEOUTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEOUT_L							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-126. UART_TIMEOUTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TIMEOUT_L	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0 [Lower byte of the 16 bit value]

6.61 UART_TIMEOUT Register (Offset = 9Ch) [reset = 0h]

UART_TIMEOUT is shown in [Figure 6-61](#) and described in [Table 6-128](#).

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Timeout higher byte

Table 6-127. UART_TIMEOUT Instances

Instance	Physical Address
UART0	0280 009Ch
UART1	0281 009Ch
UART2	0282 009Ch
UART3	0283 009Ch
UART4	0284 009Ch
UART5	0285 009Ch
UART6	0286 009Ch
UART7	0287 009Ch
UART8	0288 009Ch
UART9	0289 009Ch
MCU_UART0	40A0 009Ch
WKUP_UART0	4230 009Ch

Figure 6-61. UART_TIMEOUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEOUT_H							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-128. UART_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	TIMEOUT_H	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0 [Higher byte of the 16 bit value]

6.62 UART_SCCR Register (Offset = A0h) [reset = 7h]

UART_SCCR is shown in [Figure 6-62](#) and described in [Table 6-130](#).

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Smartcard (ISO7816) mode Control Register

Table 6-129. UART_SCCR Instances

Instance	Physical Address
UART0	0280 00A0h
UART1	0281 00A0h
UART2	0282 00A0h
UART3	0283 00A0h
UART4	0284 00A0h
UART5	0285 00A0h
UART6	0286 00A0h
UART7	0287 00A0h
UART8	0288 00A0h
UART9	0289 00A0h
MCU_UART0	40A0 00A0h
WKUP_UART0	4230 00A0h

Figure 6-62. UART_SCCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DSNACK	INACK	RESERVED			MAX_ITERATION		
R/W-0h	R/W-0h	R-0h			R/W-7h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-130. UART_SCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7	DSNACK	R/W	0h	Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error The data will be loaded into the receiver FIFO and PE will be set when reading it
6	INACK	R/W	0h	Inhibit NACK when receiving, even if an error is received The data will be loaded into the receiver FIFO and PE will be set when reading it
5-3	RESERVED	R	0h	

Table 6-130. UART_SCCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	MAX_ITERATION	R/W	7h	Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the UART transmitter will set parity error, stop and not continue until it is cleared.

6.63 UART_ERHR Register (Offset = A4h) [reset = 0h]

UART_ERHR is shown in [Figure 6-63](#) and described in [Table 6-132](#).

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Extended Receive Holding Register

Table 6-131. UART_ERHR Instances

Instance	Physical Address
UART0	0280 00A4h
UART1	0281 00A4h
UART2	0282 00A4h
UART3	0283 00A4h
UART4	0284 00A4h
UART5	0285 00A4h
UART6	0286 00A4h
UART7	0287 00A4h
UART8	0288 00A4h
UART9	0289 00A4h
MCU_UART0	40A0 00A4h
WKUP_UART0	4230 00A4h

Figure 6-63. UART_ERHR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERHR															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 6-132. UART_ERHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8-0	ERHR	R	0h	Extended Receive Holding Register - allows accessing the full 9bit UART_RHR

6.64 UART_ETHR Register (Offset = A4h) [reset = 0h]

UART_ETHR is shown in [Figure 6-64](#) and described in [Table 6-134](#).

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Extended Transmit Holding Register

Table 6-133. UART_ETHR Instances

Instance	Physical Address
UART0	0280 00A4h
UART1	0281 00A4h
UART2	0282 00A4h
UART3	0283 00A4h
UART4	0284 00A4h
UART5	0285 00A4h
UART6	0286 00A4h
UART7	0287 00A4h
UART8	0288 00A4h
UART9	0289 00A4h
MCU_UART0	40A0 00A4h
WKUP_UART0	4230 00A4h

Figure 6-64. UART_ETHR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ETHR															
R-0h																W-0h															

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 6-134. UART_ETHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	
8-0	ETHR	W	0h	Extended Transmit Holding Register - allows writing the full 9bit UART_RHR

6.65 UART_MAR Register (Offset = A8h) [reset = 0h]

UART_MAR is shown in [Figure 6-65](#) and described in [Table 6-136](#).

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Multidrop Address Register

Table 6-135. UART_MAR Instances

Instance	Physical Address
UART0	0280 00A8h
UART1	0281 00A8h
UART2	0282 00A8h
UART3	0283 00A8h
UART4	0284 00A8h
UART5	0285 00A8h
UART6	0286 00A8h
UART7	0287 00A8h
UART8	0288 00A8h
UART9	0289 00A8h
MCU_UART0	40A0 00A8h
WKUP_UART0	4230 00A8h

Figure 6-65. UART_MAR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								ADDRESS							
R-0h																								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-136. UART_MAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	ADDRESS	R/W	0h	Multidrop match address value

6.66 UART_MMR Register (Offset = ACh) [reset = 0h]

UART_MMR is shown in [Figure 6-66](#) and described in [Table 6-138](#).

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Multidrop Mask Register

Table 6-137. UART_MMR Instances

Instance	Physical Address
UART0	0280 00ACh
UART1	0281 00ACh
UART2	0282 00ACh
UART3	0283 00ACh
UART4	0284 00ACh
UART5	0285 00ACh
UART6	0286 00ACh
UART7	0287 00ACh
UART8	0288 00ACh
UART9	0289 00ACh
MCU_UART0	40A0 00ACh
WKUP_UART0	4230 00ACh

Figure 6-66. UART_MMR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MASK															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-138. UART_MMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	MASK	R/W	0h	Address match masking value ? writing a 0 to a bit means that the corresponding address bit will be ignored in matching

6.67 UART_MBR Register (Offset = B0h) [reset = 0h]

UART_MBR is shown in [Figure 6-67](#) and described in [Table 6-140](#).

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Multidrop Broadcast Address Register

Table 6-139. UART_MBR Instances

Instance	Physical Address
UART0	0280 00B0h
UART1	0281 00B0h
UART2	0282 00B0h
UART3	0283 00B0h
UART4	0284 00B0h
UART5	0285 00B0h
UART6	0286 00B0h
UART7	0287 00B0h
UART8	0288 00B0h
UART9	0289 00B0h
MCU_UART0	40A0 00B0h
WKUP_UART0	4230 00B0h

Figure 6-67. UART_MBR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BROADCAST_ADDRESS							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-140. UART_MBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	
7-0	BROADCAST_ADDRESS	R/W	0h	Broadcast address for address matching

7 MCU_CPSW0 Registers

7.1 MCU_CPSW0_ALE Registers

Table 7-2 lists the memory-mapped registers for the MCU_CPSW0_ALE. All register offset addresses not listed in Table 7-2 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. MCU_CPSW0_ALE Instances

Instance	Base Address
MCU_CPSW0_NUSS_ALE	4600 0000h

Table 7-2. MCU_CPSW0_ALE Registers

Offset	Acronym	Register Name	MCU_CPSW0_N USS_ALE Physical Address
0003E000h	CPSW_ALE_MOD_VER	ALE Module and Version Register	4603 E000h
0003E004h	CPSW_ALE_STATUS	ALE Status Register	4603 E004h
0003E008h	CPSW_ALE_CONTROL	ALE Control Register	4603 E008h
0003E00Ch	CPSW_ALE_CTRL2	ALE Control 2 Register	4603 E00Ch
0003E010h	CPSW_ALE_PRESCALE	ALE Prescale Register	4603 E010h
0003E014h	CPSW_ALE_AGING_CTRL	ALE Aging Control Register	4603 E014h
0003E01Ch	CPSW_ALE_NXT_HDR	ALE Next Header Register	4603 E01Ch
0003E020h	CPSW_ALE_TBLCTL	ALE Table Control Register	4603 E020h
0003E034h	CPSW_ALE_TBLW2	ALE LUT Table Word 2 Register	4603 E034h
0003E038h	CPSW_ALE_TBLW1	ALE LUT Table Word 1 Register	4603 E038h
0003E03Ch	CPSW_ALE_TBLW0	ALE LUT Table Word 0 Register	4603 E03Ch
0003E040h + formula	CPSW_ly_ALE_PORTCTL0_y	ALE Port Control 0 to 1 Registers	4603 E040h + formula
0003E090h	CPSW_ALE_UVLAN_MEMBER	ALE Unknown VLAN Member Mask Register	4603 E090h
0003E094h	CPSW_ALE_UVLAN_URCAST	ALE Unknown VLAN Unregistered Multicast Flood Mask Register	4603 E094h
0003E098h	CPSW_ALE_UVLAN_RMCAST	ALE Unknown VLAN Registered Multicast Flood Mask Register	4603 E098h
0003E09Ch	CPSW_ALE_UVLAN_UNTAG	ALE Unknown VLAN force Untagged Egress Mask Register	4603 E09Ch
0003E0B8h	CPSW_ALE_STAT_DIAG	ALE Statistic Output Diagnostic Register	4603 E0B8h
0003E0BCh	CPSW_ALE_OAM_LB_CTRL	ALE OAM Loopback Control Register	4603 E0BCh
0003E0C0h	CPSW_ALE_MSK_MUX0	ALE Mask Mux 0 Register	4603 E0C0h
0003E0C4h + formula	CPSW_ix_ALE_MSK_MUXx	ALE Mask Mux 1 to 3 Registers	4603 E0C4h + formula
0003E0FCh	CPSW_ALE_EGRESSOP	ALE Egress Operation Register	4603 E0FCh
0003E100h	CPSW_ALE_POLICECFG0	ALE Policing Configuration 0 Register	4603 E100h
0003E104h	CPSW_ALE_POLICECFG1	ALE Policing Configuration 1 Register	4603 E104h
0003E108h	CPSW_ALE_POLICECFG2	ALE Policing Configuration 2 Register	4603 E108h
0003E10Ch	CPSW_ALE_POLICECFG3	ALE Policing Configuration 3 Register	4603 E10Ch
0003E110h	CPSW_ALE_POLICECFG4	ALE Policing Configuration 4 Register	4603 E110h
0003E118h	CPSW_ALE_POLICECFG6	ALE Policing Configuration 6 Register	4603 E118h
0003E11Ch	CPSW_ALE_POLICECFG7	ALE Policing Configuration 7 Register	4603 E11Ch
0003E120h	CPSW_ALE_POLICETBLCTL	ALE Policing Table Control Register	4603 E120h
0003E124h	CPSW_ALE_POLICECONTROL	ALE Policing Control Register	4603 E124h
0003E128h	CPSW_ALE_POLICETESTCTL	ALE Policing Test Control Register	4603 E128h
0003E12Ch	CPSW_ALE_POLICEHSTAT	ALE Policing Hit Status Register	4603 E12Ch
0003E134h	CPSW_ALE_THREADMAPDEF	ALE THREAD Mapping Default Value Register	4603 E134h
0003E138h	CPSW_ALE_THREADMAPCTL	ALE THREAD Mapping Control Register	4603 E138h

Table 7-2. MCU_CPSW0_ALE Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_N USS_ALE Physical Address
0003E13Ch	CPSW_ALE_THREADMAPVAL	ALE THREAD Mapping Value Register	4603 E13Ch

7.1.1 CPSW_ALE_MOD_VER Register (Offset = 0003E000h) [reset = 00293904h]

CPSW_ALE_MOD_VER is shown in [Figure 7-1](#) and described in [Table 7-4](#).

Return to [Summary Table](#).

The Module and Version Register identifies the module identifier of the ALE_2g64i module.

Table 7-3. CPSW_ALE_MOD_VER Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E000h

Figure 7-1. CPSW_ALE_MOD_VER Register

31	30	29	28	27	26	25	24
MODULE_ID							
R-29h							
23	22	21	20	19	18	17	16
MODULE_ID							
R-29h							
15	14	13	12	11	10	9	8
RTL_VERSION				MAJOR_REVISION			
R-7h				R-1h			
7	6	5	4	3	2	1	0
CUSTOM_REVISION		MINOR_REVISION					
R-0h		R-4h					

LEGEND: R = Read Only; -n = value after reset

Table 7-4. CPSW_ALE_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULE_ID	R	29h	ALE module ID.
15-11	RTL_VERSION	R	7h	RTL Version.
10-8	MAJOR_REVISION	R	1h	Major Revision.
7-6	CUSTOM_REVISION	R	0h	Custom Revision.
5-0	MINOR_REVISION	R	4h	Minor Revision.

7.1.2 CPSW_ALE_STATUS Register (Offset = 0003E004h) [reset = X]

CPSW_ALE_STATUS is shown in Figure 7-2 and described in Table 7-6.

Return to [Summary Table](#).

The ALE status provides information on the ALE configuration and state. The RAMDEPTH is used to determine how IPv6 entries are stored in the table. IPv6 entries are stored in two entries where IPv6 Entry Hi is designated by the odd slice index and Lo is designated by the even slice index. The slice index is above the ram depth like {SlixelIndex,RamIndex}. So for a 64 deep RAM index of 0x005, the Hi portion of the IPv6 entry is located at 0x005|0x040 and the Lo portion is located at 0x005&(~0x040).

Table 7-5. CPSW_ALE_STATUS Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E004h

Figure 7-2. CPSW_ALE_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
POLCNTDIV8							
R-1h							
7	6	5	4	3	2	1	0
RAMDEPTH12 8	RAMDEPTH32	RESERVED	KLUENTRIES				
R-0h	R-1h	R-X	R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 7-6. CPSW_ALE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	
15-8	POLCNTDIV8	R	1h	This is the number of policer engines the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.
7	RAMDEPTH128	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both RAMDEPTH128 and RAMDEPTH32 are zero the depth is 64.
6	RAMDEPTH32	R	1h	The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both RAMDEPTH128 and RAMDEPTH32 are zero the depth is 64.
5	RESERVED	R	0h	
4-0	KLUENTRIES	R	0h	This is the number of table entries total divided by 1024. A value of 1h indicates 1024 table entries. A value of 8h indicates 8192 table entries.

7.1.3 CPSW_ALE_CONTROL Register (Offset = 0003E008h) [reset = X]

CPSW_ALE_CONTROL is shown in [Figure 7-3](#) and described in [Table 7-8](#).

Return to [Summary Table](#).

The ALE Control Register is used to set the ALE modes used for all ports.

Table 7-7. CPSW_ALE_CONTROL Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E008h

Figure 7-3. CPSW_ALE_CONTROL Register

31	30	29	28	27	26	25	24
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NOW	RESERVED				MIRROR_DP
R/W-0h	R/W-0h	R/W-0h	R/W-X				R/W-0h
23	22	21	20	19	18	17	16
UPD_BW_CTRL			RESERVED				MIRROR_TOP
R/W-0h			R/W-X				R/W-0h
15	14	13	12	11	10	9	8
UPD_STATIC	RESERVED	UVLAN_NO_LEARN	MIRROR_MEN	MIRROR_DEN	MIRROR_SEN	RESERVED	EN_HOST_UNI_FLOOD
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h
7	6	5	4	3	2	1	0
LEARN_NO_VLANID	ENABLE_VID0_MODE	ENABLE_OUI_DENY	ENABLE_BYPASS	BCAST_MCAS_T_CTL	ALE_VLAN_AWARE	ENABLE_AUTH_MODE	ENABLE_RATE_LIMIT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-8. CPSW_ALE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_ALE	R/W	0h	Enable ALE. 0h = Drop all packets 1h = Enable ALE packet processing
30	CLEAR_TABLE	R/W	0h	Clear ALE address table. Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.
29	AGE_OUT_NOW	R/W	0h	Age Out Address Table Now. Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.
28-25	RESERVED	R/W	0h	

Table 7-8. CPSW_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	MIRROR_DP	R/W	0h	Mirror Destination Port. This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the MIRROR_TOP port.
23-21	UPD_BW_CTRL	R/W	0h	The UPD_BW_CTRL field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the UPD_BW_CTRL can be programmed more aggressive. If the UPD_BW_CTRL is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. 0h = 350Mhz, 5M 1h = 359Mhz, 11M 2h = 367Mhz, 16M 3h = 375Mhz, 22M 4h = 384Mhz, 28M 5h = 392Mhz, 34M 6h = 400Mhz, 39M 7h = 409Mhz, 45M
20-17	RESERVED	R/W	0h	
16	MIRROR_TOP	R/W	0h	Mirror To Port. This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.
15	UPD_STATIC	R/W	0h	Update Static Entries - A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be 0h for most switch configurations.
14	RESERVED	R/W	0h	
13	UVLAN_NO_LEARN	R/W	0h	Unknown VLAN No Learn. This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.
12	MIRROR_MEN	R/W	0h	Mirror Match Entry Enable. This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the ~imirror_midx entry index will have that traffic also sent to the ~imirror_top port.
11	MIRROR_DEN	R/W	0h	Mirror Destination Port Enable - This field enables the destination port mirror option. When this bit is set any traffic destined for the ~imirror_dp port will have its transmit traffic also sent to the ~imirror_top port.
10	MIRROR_SEN	R/W	0h	Mirror Source Port Enable - This field enables the source port mirror option. When this bit is set any port with the ly_REG_P0_MIRROR_SP set in the CPSW_ly_ALE_PORTCTL0_y registers set will have its received traffic also sent to the MIRROR_TOP port.
9	RESERVED	R/W	X	
8	EN_HOST_UNI_FLOOD	R/W	0h	Unknown unicast packets flood to host. 0h = Unknown unicast packets are not sent to the host. 1h = Unknown unicast packets flood to host port as well as other ports.
7	LEARN_NO_VLANID	R/W	0h	Learn No VID. 0h = VID is learned with the source address. 1h = VID is not learned with the source address (source address is not tied to VID). Determines the entry type.

Table 7-8. CPSW_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	ENABLE_VID0_MODE	R/W	0h	Enable VLAN ID = 0 Mode 0h = Process the priority tagged packet with VID = PORT_VLAN[11:0]. 1h = Process the priority tagged packet with VID = 0h.
5	ENABLE_OUI_DENY	R/W	0h	Enable OUI Deny Mode. 0h = Any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry. 1h = Any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry.
4	ENABLE_BYPASS	R/W	0h	ALE Bypass. When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port. 0h = No bypass 1h = Bypass the ALE
3	BCAST_MCAST_CTL	R/W	0h	Rate Limit Transmit mode. 0h = Broadcast and multicast rate limit counters are received port based. 1h = Broadcast and multicast rate limit counters are transmit port based.
2	ALE_VLAN_AWARE	R/W	0h	ALE VLAN Aware. Determines how traffic is forwarded using VLAN rules. 0h = Simple switch rules, packets forwarded to all ports for unknown destinations. 1h = VLAN Aware rules, packets forwarded based on VLAN members
1	ENABLE_AUTH_MODE	R/W	0h	Enable MAC Authorization Mode. Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set). 0h = The ALE is not in MAC authorization mode 1h = The ALE is in MAC authorization mode
0	ENABLE_RATE_LIMIT	R/W	0h	Enable Broadcast and Multicast Rate Limit 0h = Broadcast/Multicast rates not limited 1h = Broadcast/Multicast packet reception limited to the port control register rate limit fields.

7.1.4 CPSW_ALE_CTRL2 Register (Offset = 0003E00Ch) [reset = X]

CPSW_ALE_CTRL2 is shown in [Figure 7-4](#) and described in [Table 7-10](#).

Return to [Summary Table](#).

The ALE Control 2 Register is used to set the extended features used for all ports.

Table 7-9. CPSW_ALE_CTRL2 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E00Ch

Figure 7-4. CPSW_ALE_CTRL2 Register

31	30	29	28	27	26	25	24
TRK_EN_DST	TRK_EN_SRC	TRK_EN_PRI	RESERVED	TRK_EN_IVLAN	RESERVED	TRK_EN_SIP	TRK_EN_DIP
R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-X	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DROP_BADLEN	NODROP_SRCMCST	DEFNOFRAG	DEFLMTNXTHDR	RESERVED	TRK_BASE		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		MIRROR_MIDX					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-10. CPSW_ALE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK_EN_DST	R/W	0h	Trunk Enable Destination Address. This field enables the destination MAC address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.
30	TRK_EN_SRC	R/W	0h	Trunk Enable Source Address. This field enables the source MAC address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.
29	TRK_EN_PRI	R/W	0h	Trunk Enable Priority. This field enables the VLAN Priority bits to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used.
28	RESERVED	R/W	0h	
27	TRK_EN_IVLAN	R/W	0h	Trunk Enable Inner VLAN. This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.
26	RESERVED	R/W	0h	

Table 7-10. CPSW_ALE_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	TRK_EN_SIP	R/W	0h	Trunk Enable Source IP Address. This field enables the source IP address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
24	TRK_EN_DIP	R/W	0h	Trunk Enable Destination IP Address. This field enables the destination IP address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
23	DROP_BADLEN	R/W	0h	Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.
22	NODROP_SRCMCST	R/W	0h	No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.
21	DEFNOFRAG	R/W	0h	Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.
20	DEFLMTNXTHDR	R/W	0h	Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the CPSW_ALE_NXT_HDR register values.
19	RESERVED	R/W	X	
18-16	TRK_BASE	R/W	0h	Trunk Base. This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the [31]TRK_EN_DST, [30]TRK_EN_SRC, [29]TRK_EN_PRI and [27]TRK_EN_VLAN bits are cleared (value: 0h), this value is used as the distribution index. That is a 0h will select the 1st bit of an 'N' link trunk, a 1h will select the second, etc. Below is the distribution across the trunk links. The first number in the sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0h will go to the base port (0), hash result 1h will go to the highest port of the trunk group (2), hash result 2h will go to the middle port (1), etc. 1h = 00000000 2h = 01010101 3h = 02102102 4h = 03210321
15-6	RESERVED	R/W	0h	
5-0	MIRROR_MIDX	R/W	0h	Mirror Index. This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the MIRROR_TOP port. That is any VLAN, ONU or address with or without VLAN can be selected for traffic mirroring.

7.1.5 CPSW_ALE_PRESCALE Register (Offset = 0003E010h) [reset = X]

CPSW_ALE_PRESCALE is shown in [Figure 7-5](#) and described in [Table 7-12](#).

Return to [Summary Table](#).

The ALE Prescale Register is used to set the Broadcast and Multicast rate limiting prescaler value.

Table 7-11. CPSW_ALE_PRESCALE Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E010h

Figure 7-5. CPSW_ALE_PRESCALE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ALE_PRESCALE																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-12. CPSW_ALE_PRESCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	ALE_PRESCALE	R/W	0h	ALE Prescale. The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 10h. The prescaler is off when the value is zero.

7.1.6 CPSW_ALE_AGING_CTRL Register (Offset = 0003E014h) [reset = X]

CPSW_ALE_AGING_CTRL is shown in [Figure 7-6](#) and described in [Table 7-14](#).

Return to [Summary Table](#).

The ALE Aging Control sets the aging interval which will cause periodic aging to occur. This value specifies the minimum time between aging starts.

Table 7-13. CPSW_ALE_AGING_CTRL Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E014h

Figure 7-6. CPSW_ALE_AGING_CTRL Register

31	30	29	28	27	26	25	24
PRESALE_2_DISABLE	PRESALE_1_DISABLE	RESERVED					
R/W-0h	R/W-0h	R/W-X					
23	22	21	20	19	18	17	16
ALE_AGING_TIMER							
R/W-0h							
15	14	13	12	11	10	9	8
ALE_AGING_TIMER							
R/W-0h							
7	6	5	4	3	2	1	0
ALE_AGING_TIMER							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-14. CPSW_ALE_AGING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESALE_2_DISABLE	R/W	0h	ALE Prescaler 2 Disable. When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
30	PRESALE_1_DISABLE	R/W	0h	ALE Prescaler 1 Disable. When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
29-24	RESERVED	R/W	X	
23-0	ALE_AGING_TIMER	R/W	0h	ALE Aging Timer. This field specifies the number of clock cycles times 1,000,000 between aging operations.

7.1.7 CPSW_ALE_NXT_HDR Register (Offset = 0003E01Ch) [reset = 0h]

CPSW_ALE_NXT_HDR is shown in [Figure 7-7](#) and described in [Table 7-16](#).

Return to [Summary Table](#).

The ALE Next Header is used to limit the IPv6 Next header or IPv4 Protocol values found in the IP header. It is enabled via the DEFLMTNXTHDR bit in the VLAN entry. All four IP_NXT_HDR0 to IP_NXT_HDR3 bits are compared when enabled, so if only one is required, set them all to the one value to be tested.

Table 7-15. CPSW_ALE_NXT_HDR Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E01Ch

Figure 7-7. CPSW_ALE_NXT_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP_NXT_HDR3								IP_NXT_HDR2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_NXT_HDR1								IP_NXT_HDR0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-16. CPSW_ALE_NXT_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	IP_NXT_HDR3	R/W	0h	The IP_NXT_HDR3 is the forth protocol or next header compared when enabled.
23-16	IP_NXT_HDR2	R/W	0h	The IP_NXT_HDR2 is the third protocol or next header compared when enabled.
15-8	IP_NXT_HDR1	R/W	0h	The IP_NXT_HDR1 is the second protocol or next header compared when enabled.
7-0	IP_NXT_HDR0	R/W	0h	The IP_NXT_HDR0 is the first protocol or next header compared when enabled.

7.1.8 CPSW_ALE_TBLCTL Register (Offset = 0003E020h) [reset = X]

CPSW_ALE_TBLCTL is shown in [Figure 7-8](#) and described in [Table 7-18](#).

Return to [Summary Table](#).

The ALE table control register is used to read or write that ALE table entries. After writing to this register any read or write to any ALE register will be stalled until the read or write operation completes.

Table 7-17. CPSW_ALE_TBLCTL Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E020h

Figure 7-8. CPSW_ALE_TBLCTL Register

31	30	29	28	27	26	25	24
TABLEWR	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		TABLEIDX					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-18. CPSW_ALE_TBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TABLEWR	R/W	0h	Table Write. This bit is used to write the table words to the lookup table. 0h = Table Read Operation is performed. The contents of the TABLEIDX bit will be read into the CPSW_ALE_TBLWx registers (where x = 0 to 2). 1h = Table write operation is performed. This will take the current contents from the CPSW_ALE_TBLWx registers and write them to the table at the specified TABLEIDX.
30-6	RESERVED	R/W	X	
5-0	TABLEIDX	R/W	0h	The table index is used to determine which lookup table entry is read or written.

7.1.9 CPSW_ALE_TBLW2 Register (Offset = 0003E034h) [reset = X]

CPSW_ALE_TBLW2 is shown in [Figure 7-9](#) and described in [Table 7-20](#).

Return to [Summary Table](#).

The ALE Table Word 2 is the most significant word of an ALE table entry.

Table 7-19. CPSW_ALE_TBLW2 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E034h

Figure 7-9. CPSW_ALE_TBLW2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TABLEWRD2						
R/W-X									R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-20. CPSW_ALE_TBLW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6-0	TABLEWRD2	R/W	0h	Table Entry bits [71-64]

7.1.10 CPSW_ALE_TBLW1 Register (Offset = 0003E038h) [reset = 0h]

CPSW_ALE_TBLW1 is shown in [Figure 7-10](#) and described in [Table 7-22](#).

Return to [Summary Table](#).

The ALE Table Word 1 is the middle word of an ALE table entry.

Table 7-21. CPSW_ALE_TBLW1 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E038h

Figure 7-10. CPSW_ALE_TBLW1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEWRD1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-22. CPSW_ALE_TBLW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TABLEWRD1	R/W	0h	Table Entry bits [63-32]

7.1.11 CPSW_ALE_TBLW0 Register (Offset = 0003E03Ch) [reset = 0h]

CPSW_ALE_TBLW0 is shown in [Figure 7-11](#) and described in [Table 7-24](#).

Return to [Summary Table](#).

The ALE Table Word 0 is the least significant word of an ALE table entry.

Table 7-23. CPSW_ALE_TBLW0 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E03Ch

Figure 7-11. CPSW_ALE_TBLW0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEWRD0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-24. CPSW_ALE_TBLW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TABLEWRD0	R/W	0h	Table Entry bits [31-0]

7.1.12 CPSW_ly_ALE_PORTCTL0_y Register (Offset = 0003E040h + formula) [reset = X]

CPSW_ly_ALE_PORTCTL0_y is shown in [Figure 7-12](#) and described in [Table 7-26](#).

Return to [Summary Table](#).

The ALE Port Control Register sets the port specific modes of operation.

Offset = 0003E040h + (y * 4h); where y = 0 to 1

Table 7-25. CPSW_ly_ALE_PORTCTL0_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E040h + formula

Figure 7-12. CPSW_ly_ALE_PORTCTL0_y Register

31	30	29	28	27	26	25	24
ly_REG_Py_BCAST_LIMIT							
R/W-0h							
23	22	21	20	19	18	17	16
ly_REG_Py_MCAST_LIMIT							
R/W-0h							
15	14	13	12	11	10	9	8
ly_REG_Py_DR OP_DOUBLE_ VLAN	ly_REG_Py_DR OP_DUAL_VLA N	ly_REG_Py_M ACONLY_CAF	ly_REG_Py_DI S_PAUTHMOD	ly_REG_Py_M ACONLY	ly_REG_Py_TR UNKEN	ly_REG_Py_TRUNKNUM	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
ly_REG_Py_MI RROR_SP	RESERVED	ly_REG_Py_N O_SA_UPDATE	ly_REG_Py_N O_LEARN	ly_REG_Py_VI D_INGRESS_C HECK	ly_REG_Py_DR OP_UN_TAGG ED	ly_REG_Py_PORTSTATE	
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-26. CPSW_ly_ALE_PORTCTL0_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ly_REG_P0_BCAST_LIMI T	R/W	0h	Broadcast Packet Rate Limit - Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23-16	ly_REG_P0_MCAST_LIMI T	R/W	0h	Multicast Packet Rate Limit - Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field. The ly_REG_P0_MCAST_LIMIT bit field is the number of Multicast packets that will be forwarded per CPSW_ALE_PRESCALE time.
15	ly_REG_P0_DROP_DOU BLE_VLAN	R/W	0h	Drop Double VLAN. When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.
14	ly_REG_P0_DROP_DUA L_VLAN	R/W	0h	Drop Dual VLAN. When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.

Table 7-26. CPSW_ly_ALE_PORTCTL0_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ly_REG_P0_MACONLY_CAF	R/W	0h	Mac Only Copy All Frames. When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with ly_REG_P0_MACONLY set.
12	ly_REG_P0_DIS_PAUTH_MOD	R/W	0h	Disable Port authorization. When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.
11	ly_REG_P0_MACONLY	R/W	0h	MAC Only. When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the ly_REG_P0_MACONLY bit set and the ly_REG_P0_NO_LEARN also set. If ly_REG_P0_MACONLY bit is set and the ly_REG_P0_NO_LEARN is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that the host can broadcast to all ports including MacOnly ports in this mode.
10	ly_REG_P0_TRUNKEN	R/W	0h	Trunk Enable. This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the ly_REG_P0_TRUNKEN bit is set and having the same ly_REG_P0_TRUNKNUM will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never transmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry.
9-8	ly_REG_P0_TRUNKNUM	R/W	0h	Trunk Number. This field is used as the trunk number when the ly_REG_P0_TRUNKEN bit is also set. Ports with the same trunk number that have the ly_REG_P0_TRUNKEN bit is also set will have traffic distributed within the trunk based on the result of the hash function described above.
7	ly_REG_P0_MIRROR_SP	R/W	0h	Mirror Source Port - This field enables the source port mirror option. When this bit is set any traffic received on the port with the ly_REG_P0_MIRROR_SP bit set will have its received traffic also sent to the MIRROR_TOP port.
6	RESERVED	R/W	X	
5	ly_REG_P0_NO_SA_UPD_ATE	R/W	0h	No Source Address Update. When set will not update the source addresses for this port.
4	ly_REG_P0_NO_LEARN	R/W	0h	No Learn. When set will not learn the source addresses for this port.
3	ly_REG_P0_VID_INGRESS_CHECK	R/W	0h	VLAN Ingress Check. When set if a packet received is not a member of the VLAN, the packet will be dropped.
2	ly_REG_P0_DROP_UNTAGGED	R/W	0h	If Drop Untagged. When set will drop packets without a VLAN tag.
1-0	ly_REG_P0_PORTSTATE	R/W	0h	Port State. Defines the current port state used for lookup operations. 0h = Disabled 1h = Blocked 2h = Learning 3h = Forwarding

7.1.13 CPSW_ALE_UVLAN_MEMBER Register (Offset = 0003E090h) [reset = X]

CPSW_ALE_UVLAN_MEMBER is shown in [Figure 7-13](#) and described in [Table 7-28](#).

Return to [Summary Table](#).

The ALE Unknown VLAN Member Mask Register is used to specify the member list for unknown VLAN ID.

Table 7-27. CPSW_ALE_UVLAN_MEMBER Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E090h

Figure 7-13. CPSW_ALE_UVLAN_MEMBER Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						UVLAN_MEMBER_LIST	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-28. CPSW_ALE_UVLAN_MEMBER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	UVLAN_MEMBER_LIST	R/W	0h	Unknown VLAN Member List. Each bit represents the port member status for unknown VLANs.

7.1.14 CPSW_ALE_UVLAN_URCAST Register (Offset = 0003E094h) [reset = X]

CPSW_ALE_UVLAN_URCAST is shown in [Figure 7-14](#) and described in [Table 7-30](#).

Return to [Summary Table](#).

The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is used to specify which egress ports unregistered multicast addresses egress for the unregistered VLAN ID.

Table 7-29. CPSW_ALE_UVLAN_URCAST Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E094h

Figure 7-14. CPSW_ALE_UVLAN_URCAST Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						UVLAN_UNREG_MCAST_FLOOD_MASK	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-30. CPSW_ALE_UVLAN_URCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	UVLAN_UNREG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Unregister Multicast Flood Mask. Each bit represents the port to which unregistered multicast are sent for unregistered VLANs.

7.1.15 CPSW_ALE_UVLAN_RMCAST Register (Offset = 0003E098h) [reset = X]

CPSW_ALE_UVLAN_RMCAST is shown in [Figure 7-15](#) and described in [Table 7-32](#).

Return to [Summary Table](#).

The ALE Unknown VLAN Registered Multicast Flood Mask Register is used to specify which egress ports registered multicast addresses egress for the unregistered VLAN ID.

Table 7-31. CPSW_ALE_UVLAN_RMCAST Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E098h

Figure 7-15. CPSW_ALE_UVLAN_RMCAST Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						UVLAN_REG_MCAST_FLOOD_MASK	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-32. CPSW_ALE_UVLAN_RMCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	UVLAN_REG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Register Multicast Flood Mask. Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs.

7.1.16 CPSW_ALE_UVLAN_UNTAG Register (Offset = 0003E09Ch) [reset = X]

CPSW_ALE_UVLAN_UNTAG is shown in [Figure 7-16](#) and described in [Table 7-34](#).

Return to [Summary Table](#).

The ALE Unknown VLAN force Untagged Egress Mask Register is used to specify which egress ports the VLAN ID will be removed.

Table 7-33. CPSW_ALE_UVLAN_UNTAG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E09Ch

Figure 7-16. CPSW_ALE_UVLAN_UNTAG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						UVLAN_FORCE_UNTAGGED_EGRESS	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-34. CPSW_ALE_UVLAN_UNTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	0h	
1-0	UVLAN_FORCE_UNTAGGED_EGRESS	R/W	0h	Unknown VLAN Force Untagged Egress Mask. Each bit represents the port where the VLAN will be removed for unregistered VLANs.

7.1.17 CPSW_ALE_STAT_DIAG Register (Offset = 0003E0B8h) [reset = X]

CPSW_ALE_STAT_DIAG is shown in [Figure 7-17](#) and described in [Table 7-36](#).

Return to [Summary Table](#).

The ALE Statistic Output Diagnostic Register allows the output statistics to diagnose the SW counters. This register is for diagnostic only.

Table 7-35. CPSW_ALE_STAT_DIAG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E0B8h

Figure 7-17. CPSW_ALE_STAT_DIAG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PBCAST_DIAG	RESERVED						PORT_DIAG
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED				STAT_DIAG			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-36. CPSW_ALE_STAT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	
15	PBCAST_DIAG	R/W	0h	When set and the PORT_DIAG is set to zero, will allow all ports to see the same stat diagnostic increment.
14-9	RESERVED	R/W	X	
8	PORT_DIAG	R/W	0h	The port selected that a received packet will cause the selected error to increment
7-4	RESERVED	R/W	0h	
3-0	STAT_DIAG	R/W	0h	When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port. 0h = Disabled 1h = Destination Equal Source Drop Stat will count 2h = VLAN Ingress Check Drop Stat will count 3h = Source Multicast Drop Stat will count 4h = Dual VLAN Drop Stat will count 5h = Ether Type length error Drop Stat will count 6h = Next Hop Limit Drop Stat will count 7h = IPv4 Fragment Drop Stat will count 8h = Classifier Hit Stat will count 9h = Classifier Red Drop Stat will count 10h = Classifier Yellow Drop Stat will count 11h = ALE Overflow Drop Stat will count 12h = Rate Limit Drop Stat will count 13h = Blocked Address Drop Stat will count 14h = Secure Address Drop Stat will count 15h = Authorization Drop Stat will count

7.1.18 CPSW_ALE_OAM_LB_CTRL Register (Offset = 0003E0BCh) [reset = X]

CPSW_ALE_OAM_LB_CTRL is shown in Figure 7-18 and described in Table 7-38.

Return to [Summary Table](#).

The ALE OAM Control allows ports to be put into OAM Loopback, only non-supervisor packet are looped back to the source port.

Table 7-37. CPSW_ALE_OAM_LB_CTRL Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E0BCh

Figure 7-18. CPSW_ALE_OAM_LB_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						OAM_LB_CTRL	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-38. CPSW_ALE_OAM_LB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	OAM_LB_CTRL	R/W	0h	The OAM_LB_CTRL bit field allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an CPSW_ALE_EGRESSOP [31-24] EGRESS_OP of 0xFF which swaps the source (SA) and destination address (DA). BPDUs will still flow through as normal so that OAM can be remotely requested and disabled.

7.1.19 CPSW_ALE_MSK_MUX0 Register (Offset = 0003E0C0h) [reset = X]

CPSW_ALE_MSK_MUX0 is shown in [Figure 7-19](#) and described in [Table 7-40](#).

Return to [Summary Table](#).

VLAN Mask Mux 0. The ALE Mask Mux 0 register is used along with the VLAN registered/unregistered index selectors from the Lookup Table to determine the value for VLAN registered and unregister mask respectively.

Table 7-39. CPSW_ALE_MSK_MUX0 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E0C0h

Figure 7-19. CPSW_ALE_MSK_MUX0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						VLAN_MASK_MUX_0	
R-X						R-3h	

LEGEND: R = Read Only; -n = value after reset

Table 7-40. CPSW_ALE_MSK_MUX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1-0	VLAN_MASK_MUX_0	R	3h	VLAN Mask Mux 0. When selected by the VLAN lookup table entry FwdUnRegIdx or FwdAllRegIdx is used as the FwdUnRegMask or FwdUnRegMask values anded with the member list to determine the forwarding of packets. The Value of VLAN_MASK_MUX_0 is read only and set to all ones for all ports.

7.1.20 CPSW_Ix_ALE_MSK_MUXx Register (Offset = 0003E0C4h + formula) [reset = X]

CPSW_Ix_ALE_MSK_MUXx is shown in [Figure 7-20](#) and described in [Table 7-42](#).

Return to [Summary Table](#).

VLAN Mask Mux x (where x = 1 to 3). The ALE Mask Mux registers are used along with the VLAN registered/unregistered index selectors from the Lookup Table to determine the value for VLAN registered and unregistered mask respectively.

Offset = 0003E0C4h + (x * 4h); where x = 1 to 3

Table 7-41. CPSW_Ix_ALE_MSK_MUXx Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E0C4h + formula

Figure 7-20. CPSW_Ix_ALE_MSK_MUXx Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						I1_REG_VLAN_MASK_MUX_1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-42. CPSW_Ix_ALE_MSK_MUXx Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	Ix_REG_VLAN_MASK_MUX_x	R/W	0h	<p>VLAN Mask Mux x (where x = 1 to 3).</p> <p>When selected by the VLAN lookup table entry FwdUnRegIdx or FwdAllRegIdx is used as the FwdUnRegMask or FwdUnRegMask values anded with the member list to determine the forwarding of packets.</p> <p>The Value of CPSW_ALE_MSK_MUX0[1-0] VLAN_MASK_MUX_0 is read only and set to all ones for all ports.</p>

7.1.21 CPSW_ALE_EGRESSOP Register (Offset = 0003E0FCh) [reset = X]

CPSW_ALE_EGRESSOP is shown in [Figure 7-21](#) and described in [Table 7-44](#).

Return to [Summary Table](#).

The Egress Operation register allows enabled classifiers with IPSA or IPDA match to use the CPSW Egress Packet Operations Inter VLAN Routing sub functions. If the packet was destined for the host, but matches a classifier that has a programmed egress opcode, it will be forwarded to the destination ports where the destination ports will use the thier egress opcode entry to modify the packet. InterVLAN Routing and mirroring need to be understood, they are orthogonal functions.

Table 7-43. CPSW_ALE_EGRESSOP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E0FCh

Figure 7-21. CPSW_ALE_EGRESSOP Register

31	30	29	28	27	26	25	24
EGRESS_OP							
R/W-0h							
23	22	21	20	19	18	17	16
EGRESS_TRK			TTL_CHECK	RESERVED			
R/W-0h			R/W-0h	R/W-X			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DEST_PORTS	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-44. CPSW_ALE_EGRESSOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	EGRESS_OP	R/W	0h	The Egress Operation defines the operation performed by the CPSW Egress Packet Operations 0h = NOP : 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load. FFh: Swaps source address (SA) and destination address (DA) of packet, this is intended to allow OAM diagnostics for a link.
23-21	EGRESS_TRK	R/W	0h	The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.
20	TTL_CHECK	R/W	0h	The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.
19-2	RESERVED	R/W	X	
1-0	DEST_PORTS	R/W	0h	The Destination Ports is a list of the ports the classified packet will be set to. If a destination is a Trunk, all the port bits for that trunk must be set.

7.1.22 CPSW_ALE_POLICECFG0 Register (Offset = 0003E100h) [reset = X]

CPSW_ALE_POLICECFG0 is shown in [Figure 7-22](#) and described in [Table 7-46](#).

Return to [Summary Table](#).

The Policing Config 0 holds the port, frame priority and ONU address index as well as match enables for port, frame priority and ONU address matching.

Table 7-45. CPSW_ALE_POLICECFG0 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E100h

Figure 7-22. CPSW_ALE_POLICECFG0 Register

31	30	29	28	27	26	25	24
PORT_MEN	TRUNKID	RESERVED				PORT_NUM	RESERVED
R/W-0h	R/W-0h	R/W-X				R/W-0h	R/W-X
23	22	21	20	19	18	17	16
RESERVED				PRI_MEN	PRI_VAL		
R/W-X				R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
ONU_MEN	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED		ONU_INDEX					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-46. CPSW_ALE_POLICECFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PORT_MEN	R/W	0h	Port Match Enable. Enabled port match for the selected policing/ classifier entry
30	TRUNKID	R/W	0h	Trunk ID. When set indicates the port number is a trunk group.
29-26	RESERVED	R/W	0h	
25	PORT_NUM	R/W	0h	Port Number. Specifies the port address to match for the selected policing/ classifier entry
24-20	RESERVED	R/W	0h	
19	PRI_MEN	R/W	0h	Priority Match Enable. Enables frame priority match for the selected policing/ classifier entry
18-16	PRI_VAL	R/W	0h	Priority Value. Specifies the frame priority to match for the selected policing/ classifier entry
15	ONU_MEN	R/W	0h	OUI Match Enable. Enables frame ONU address match for the selected policing/ classifier entry
14-6	RESERVED	R/W	0h	

Table 7-46. CPSW_ALE_POLICECFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	ONU_INDEX	R/W	0h	OUI Table Entry Index. Specifies the ALE ONU address lookup table index to match for the selected policing/ classifier entry

7.1.23 CPSW_ALE_POLICECFG1 Register (Offset = 0003E104h) [reset = X]

CPSW_ALE_POLICECFG1 is shown in [Figure 7-23](#) and described in [Table 7-48](#).

Return to [Summary Table](#).

The Policing Config 1 holds the match enable/match index for the L2 Destination and L2 source addresses.

Table 7-47. CPSW_ALE_POLICECFG1 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E104h

Figure 7-23. CPSW_ALE_POLICECFG1 Register

31	30	29	28	27	26	25	24
DST_MEN	RESERVED						
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED			DST_INDEX				
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
SRC_MEN	RESERVED						
R/W-0h				R/W-X			
7	6	5	4	3	2	1	0
RESERVED			SRC_INDEX				
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-48. CPSW_ALE_POLICECFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DST_MEN	R/W	0h	Destination Address Match Enable. Enables frame L2 destination address match for the selected policing/ classifier entry
30-22	RESERVED	R/W	X	
21-16	DST_INDEX	R/W	0h	Destination Address Table Entry Index. Specifies the ALE L2 destination address lookup table index to match for the selected policing/ classifier entry
15	SRC_MEN	R/W	0h	Source Address Match Enable. Enables frame L2 source address match for the selected policing/ classifier entry
14-6	RESERVED	R/W	X	
5-0	SRC_INDEX	R/W	0h	Source Address Table Entry Index. Specifies the ALE L2 source address lookup table index to match for the selected policing/ classifier entry

7.1.24 CPSW_ALE_POLICECFG2 Register (Offset = 0003E108h) [reset = X]

CPSW_ALE_POLICECFG2 is shown in [Figure 7-24](#) and described in [Table 7-50](#).

Return to [Summary Table](#).

The Policing Config 2 holds the match enable/match index for the Outer VLAN and Inner VLAN addresses.

Table 7-49. CPSW_ALE_POLICECFG2 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E108h

Figure 7-24. CPSW_ALE_POLICECFG2 Register

31	30	29	28	27	26	25	24
OVLAN_MEN	RESERVED						
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED		OVLAN_INDEX					
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
IVLAN_MEN	RESERVED						
R/W-0h				R/W-X			
7	6	5	4	3	2	1	0
RESERVED		IVLAN_INDEX					
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-50. CPSW_ALE_POLICECFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVLAN_MEN	R/W	0h	Outer VLAN Match Enable. Enables frame Outer VLAN address match for the selected policing/ classifier entry
30-22	RESERVED	R/W	0h	
21-16	OVLAN_INDEX	R/W	0h	Outer VLAN Table Entry Index. Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/ classifier entry
15	IVLAN_MEN	R/W	0h	Inner VLAN Match Enable. Enables frame Inner VLAN address match for the selected policing/ classifier entry
14-6	RESERVED	R/W	0h	
5-0	IVLAN_INDEX	R/W	0h	Inner VLAN Table Entry Index. Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/ classifier entry

7.1.25 CPSW_ALE_POLICECFG3 Register (Offset = 0003E10Ch) [reset = X]

CPSW_ALE_POLICECFG3 is shown in [Figure 7-25](#) and described in [Table 7-52](#).

Return to [Summary Table](#).

The Policing Config 3 holds the match enable/match index for the Ether Type and IP Source address.

Table 7-51. CPSW_ALE_POLICECFG3 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E10Ch

Figure 7-25. CPSW_ALE_POLICECFG3 Register

31	30	29	28	27	26	25	24
ETHERTYPE_MEN	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED		ETHERTYPE_INDEX					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
IPSRC_MEN	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED		IPSRC_INDEX					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-52. CPSW_ALE_POLICECFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ETHERTYPE_MEN	R/W	0h	EtherType Match Enable. Enables frame Ether Type match for the selected policing/ classifier entry
30-22	RESERVED	R/W	X	
21-16	ETHERTYPE_INDEX	R/W	0h	EtherType Table Entry Index. Specifies the ALE Ether Type lookup table index to match for the selected policing/ classifier entry
15	IPSRC_MEN	R/W	0h	IP Source Address Match Enable. Enables frame IP Source address match for the selected policing/ classifier entry
14-6	RESERVED	R/W	X	
5-0	IPSRC_INDEX	R/W	0h	IP Source Address Table Entry Index. Specifies the ALE IP Source address lookup table index to match for the selected policing/ classifier entry

7.1.26 CPSW_ALE_POLICECFG4 Register (Offset = 0003E110h) [reset = X]

CPSW_ALE_POLICECFG4 is shown in [Figure 7-26](#) and described in [Table 7-54](#).

Return to [Summary Table](#).

The Policing Config 4 holds the match enable/match index for the IP Destination address

Table 7-53. CPSW_ALE_POLICECFG4 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E110h

Figure 7-26. CPSW_ALE_POLICECFG4 Register

31	30	29	28	27	26	25	24
IPDST_MEN	RESERVED						
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED		IPDST_INDEX					
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-54. CPSW_ALE_POLICECFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPDST_MEN	R/W	0h	IP Destination Address Match Enable. Enables frame IP Destination address match for the selected policing/ classifier entry
30-22	RESERVED	R/W	X	
21-16	IPDST_INDEX	R/W	0h	IP Destination Address Table Entry Index. Specifies the ALE IP Destination address lookup table index to match for the selected policing/ classifier entry
15-0	RESERVED	R/W	X	

7.1.27 CPSW_ALE_POLICECFG6 Register (Offset = 0003E118h) [reset = 0h]

CPSW_ALE_POLICECFG6 is shown in [Figure 7-27](#) and described in [Table 7-56](#).

Return to [Summary Table](#).

The PIR counter is a 37 bit internal counter where PIR_IDLE_INC_VAL is added every clock and the frame size << 18 is subtracted at EOF if not RED at LUT time. If the counter is negative the packet will be marked RED, else it can be YELLOW or GREEN based on the CIR counter. If only this counter is used (CIR_IDLE_INC_VAL = 0h), then packets are marked RED or GREEN based on PIR counter only.

Table 7-55. CPSW_ALE_POLICECFG6 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E118h

Figure 7-27. CPSW_ALE_POLICECFG6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIR_IDLE_INC_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-56. CPSW_ALE_POLICECFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PIR_IDLE_INC_VAL	R/W	0h	Peak Information Rate Idle Increment Value. The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED.

7.1.28 CPSW_ALE_POLICECFG7 Register (Offset = 0003E11Ch) [reset = 0h]

CPSW_ALE_POLICECFG7 is shown in [Figure 7-28](#) and described in [Table 7-58](#).

Return to [Summary Table](#).

The CIR counter is a 37 bit internal counter where CIR_IDLE_INC_VAL is added every clock and the frame size << 18 is subtracted at EOF if not RED or YELLOW at LUT time. If the counter is positive the packet will be marked GREEN, else it can be YELLOW or RED based on the PIR counter. If only this counter is used (PIR_IDLE_INC_VAL= 0h), then packets are marked YELLOW or GREEN based on CIR counter only.

Table 7-57. CPSW_ALE_POLICECFG7 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E11Ch

Figure 7-28. CPSW_ALE_POLICECFG7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CIR_IDLE_INC_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-58. CPSW_ALE_POLICECFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CIR_IDLE_INC_VAL	R/W	0h	Committed Information Idle Increment Value - The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW.

7.1.29 CPSW_ALE_POLICETBLCTL Register (Offset = 0003E120h) [reset = X]

CPSW_ALE_POLICETBLCTL is shown in [Figure 7-29](#) and described in [Table 7-60](#).

Return to [Summary Table](#).

The Policing Table Control is used to read or write the selected policing/classifier entry. The selected policing/classifier entry is only read or written after this register is written based on the value of the WRITE_ENABLE bit.

Table 7-59. CPSW_ALE_POLICETBLCTL Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E120h

Figure 7-29. CPSW_ALE_POLICETBLCTL Register

31	30	29	28	27	26	25	24
WRITE_ENABLE	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					POL_TBL_IDX		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-60. CPSW_ALE_POLICETBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRITE_ENABLE	R/W	0h	Write Enable. Setting this bit will write the POLICECFG0-7 to the [2-0] POL_TBL_IDX selected policing/ classifier entry. Clearing this bit will read the [2-0] POL_TBL_IDX selected policing/ classifier entry into the POLICECFG0-7 registers.
30-3	RESERVED	R/W	X	
2-0	POL_TBL_IDX	R/W	0h	Policer Entry Index. This field specifies the policing/classifier entry to be read or written. When writing to this field without setting the [31] WRITE_ENABLE=1h will cause the selected policing/classifier entry to be loaded into the POLICECFG0-7 registers. When writing to this field with setting the [31] WRITE_ENABLE=1h will cause the selected policing/classifier entry to be updated from the POLICECFG0-7 registers.

7.1.30 CPSW_ALE_POLICECONTROL Register (Offset = 0003E124h) [reset = X]

CPSW_ALE_POLICECONTROL is shown in [Figure 7-30](#) and described in [Table 7-62](#).

Return to [Summary Table](#).

The Control Enables color marking as well as internal ALE packet dropping rules.

**Table 7-61. CPSW_ALE_POLICECONTROL
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E124h

Figure 7-30. CPSW_ALE_POLICECONTROL Register

31	30	29	28	27	26	25	24
POLICING_EN	RESERVED	RED_DROP_EN	YELLOW_DROP_EN	RESERVED	YELLOWTHRESH		
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
POLMCHMODE		PRIORITY_TH_READ_EN	MAC_ONLY_DEF_DIS	RESERVED			
R/W-0h		R/W-0h	R/W-0h	R/W-X			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-62. CPSW_ALE_POLICECONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLICING_EN	R/W	0h	Policing Enable - Enables the policing to color the packets, this also enables red or yellow drop capabilities.
30	RESERVED	R/W	X	
29	RED_DROP_EN	R/W	0h	RED Drop Enable - Enables the ALE to drop the red colored packets.
28	YELLOW_DROP_EN	R/W	0h	YELLOW Drop Enable - Enables the ALE to drop yellow packets based on the YELLOWTHRESH bit value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature.
27	RESERVED	R/W	0h	
26-24	YELLOWTHRESH	R/W	0h	Yellow Threshold - When set enables a portion of the yellow packets to be dropped based on the YELLOW_DROP_EN bit enable. 0h = 100% 1h = 50% 2h = 33% 3h = 25% 4h = 20% 5h = 17% 6h = 14% 7h = 13%

Table 7-62. CPSW_ALE_POLICECONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-22	POLMCHMODE	R/W	0h	Policing Match Mode - This field determines what happens to packets that fail to hit any policing/classifier entry. 0h = No Hit packets are marked GREEN 1h = No Hit packets are marked YELLOW 2h = No Hit packets are marked RED 3h = No Hit packets are marked based on policing/classifier entry=0 state.
21	PRIORITY_THREAD_EN	R/W	0h	Priority Thread Enable - This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.
20	MAC_ONLY_DEF_DIS	R/W	0h	MAC Only Default Disable - This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}. If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.
19-0	RESERVED	R/W	X	

7.1.31 CPSW_ALE_POLICETESTCTL Register (Offset = 0003E128h) [reset = X]

CPSW_ALE_POLICETESTCTL is shown in [Figure 7-31](#) and described in [Table 7-64](#).

Return to [Summary Table](#).

The Policing Test Control enables the ability to determine which policing entry has been hit and whether they reported a red or yellow rate condition.

Table 7-63. CPSW_ALE_POLICETESTCTL Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E128h

Figure 7-31. CPSW_ALE_POLICETESTCTL Register

31	30	29	28	27	26	25	24
POL_CLRALL_HIT	POL_CLRALL_REDHIT	POL_CLRALL_YELLOWHIT	POL_CLRSEL_ALL	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X			
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					POL_TEST_IDX		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-64. CPSW_ALE_POLICETESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_CLRALL_HIT	R/W	0h	Policer Clear - This bit clears all the policing/classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit.
30	POL_CLRALL_REDHIT	R/W	0h	Policer Clear RED - This bit clears all the policing/classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.
29	POL_CLRALL_YELLOWHIT	R/W	0h	Policer Clear YELLOW - This bit clears all the policing/classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition.
28	POL_CLRSEL_ALL	R/W	0h	Police Clear Selected - This bit clears the selected policing/classifier hit, redhit and yellowhit bits. This bit is self clearing.
27-3	RESERVED	R/W	X	
2-0	POL_TEST_IDX	R/W	0h	Policer Test Index - This field selects which policing/classifier hit bits will be read or written.

7.1.32 CPSW_ALE_POLICEHSTAT Register (Offset = 0003E12Ch) [reset = X]

CPSW_ALE_POLICEHSTAT is shown in Figure 7-32 and described in Table 7-66.

Return to [Summary Table](#).

The policing hit status is a read only register that reads the hit bits of the selected policing/classifier.

Table 7-65. CPSW_ALE_POLICEHSTAT Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E12Ch

Figure 7-32. CPSW_ALE_POLICEHSTAT Register

31	30	29	28	27	26	25	24
POL_HIT	POL_REDHIT	POL_YELLOW HIT	RESERVED				
R-0h	R-0h	R-0h	R-X				
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							
R-X							

LEGEND: R = Read Only; -n = value after reset

Table 7-66. CPSW_ALE_POLICEHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_HIT	R	0h	<p>Policer Hit.</p> <p>This indicates that the selected policing/ classifier via the CPSW_ALE_POLICETESTCTL[2-0] POL_TEST_IDX field has been hit by a packet seen on any port that matches the policing/ classifier entry match.</p>
30	POL_REDHIT	R	0h	<p>Policer Hit RED.</p> <p>This indicates that the selected policing/ classifier via the CPSW_ALE_POLICETESTCTL[2-0] POL_TEST_IDX field has been hit during a RED condition by a packet seen on any port that matches the policing/ classifier entry match.</p>
29	POL_YELLOWHIT	R	0h	<p>Policer Hit YELLOW.</p> <p>This indicates that the selected policing/ classifier via the CPSW_ALE_POLICETESTCTL[2-0] POL_TEST_IDX field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/ classifier entry match.</p>
28-0	RESERVED	R	X	

7.1.33 CPSW_ALE_THREADMAPDEF Register (Offset = 0003E134h) [reset = X]

CPSW_ALE_THREADMAPDEF is shown in [Figure 7-33](#) and described in [Table 7-68](#).

Return to [Summary Table](#).

The THREAD Mapping Default Value register is used to set the default thread ID when no classifier is matched.

Table 7-67. CPSW_ALE_THREADMAPDEF Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E134h

Figure 7-33. CPSW_ALE_THREADMAPDEF Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
DEFTHREAD_EN	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED		DEFTHREADVAL					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-68. CPSW_ALE_THREADMAPDEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	DEFTHREAD_EN	R/W	0h	Default Tread Enable. 0h = The switch will generate its own thread ID based on port and priority if there is no classifier match. 1h = The switch will use the default thread value (DEFTHREADVAL) for the host interface thread ID if no classifier is matched.
14-6	RESERVED	R/W	X	
5-0	DEFTHREADVAL	R/W	0h	Default Thread Value. This field specifies the default thread ID value.

7.1.34 CPSW_ALE_THREADMAPCTL Register (Offset = 0003E138h) [reset = X]

CPSW_ALE_THREADMAPCTL is shown in [Figure 7-34](#) and described in [Table 7-70](#).

Return to [Summary Table](#).

The THREAD Mapping Control register allows the highest matched classifier to return a particular thread ID for traffic sent to the host. This allows particular classifier matched traffic to be placed on a particular host's queue.

Table 7-69. CPSW_ALE_THREADMAPCTL Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E138h

Figure 7-34. CPSW_ALE_THREADMAPCTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					CLASSINDEX		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-70. CPSW_ALE_THREADMAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	CLASSINDEX	R/W	0h	Classifier Index. This is the classifier index entry that the thread enable and thread value will be read or written by the CPSW_ALE_THREADMAPVAL[5-0] THREADVAL register.

7.1.35 CPSW_ALE_THREADMAPVAL Register (Offset = 0003E13Ch) [reset = X]

CPSW_ALE_THREADMAPVAL is shown in [Figure 7-35](#) and described in [Table 7-72](#).

Return to [Summary Table](#).

The THREAD Mapping Value register is used to set the thread ID for a particular classifier entry.

Table 7-71. CPSW_ALE_THREADMAPVAL Instances

Instance	Physical Address
MCU_CPSW0_NUSS_ALE	4603 E13Ch

Figure 7-35. CPSW_ALE_THREADMAPVAL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
THREAD_EN	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED		THREADVAL					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-72. CPSW_ALE_THREADMAPVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	THREAD_EN	R/W	0h	Thread Enable. 0h = The the thread ID will be determined by the CPSW_ALE_THREADMAPDEF register settings. 1h = The switch will use the [5-0] THREADVAL for the selected classifier match.
14-6	RESERVED	R/W	X	
5-0	THREADVAL	R/W	0h	Thread Value. This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.

7.2 MCU_CPSW0_CONTROL Registers

Table 7-74 lists the memory-mapped registers for the MCU_CPSW0_CONTROL. All register offset addresses not listed in Table 7-74 should be considered as reserved locations and the register contents should not be modified.

Table 7-73. MCU_CPSW0_CONTROL Instances

Instance	Base Address
MCU_CPSW0_NUSS_CONTROL	4600 0000h

Table 7-74. MCU_CPSW0_CONTROL Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_CON TROL Physical Address
00020000h	CPSW_CPSW_ID_VER_REG	ID Version Register	4602 0000h
00020004h	CPSW_CONTROL_REG	Control Register	4602 0004h
00020010h	CPSW_EM_CONTROL_REG	Emulation Control Register	4602 0010h
00020014h	CPSW_STAT_PORT_EN_REG	Statistics Port Enable Register	4602 0014h
00020018h	CPSW_PTYPE_REG	Transmit Priority Type Register	4602 0018h
0002001Ch	CPSW_SOFT_IDLE_REG	Software Idle Register	4602 001Ch
00020020h	CPSW_THRU_RATE_REG	Thru Rate Register	4602 0020h
00020024h	CPSW_GAP_THRESH_REG	Transmit FIFO Short Gap Threshold Register	4602 0024h
00020028h	CPSW_TX_START_WDS_REG	Transmit FIFO Start Words Register	4602 0028h
0002002Ch	CPSW_EEE_PRESCALE_REG	Energy Efficient Ethernet Prescale Value Register	4602 002Ch
00020030h	CPSW_TX_G_OFLOW_THRESH_SET_REG	PFC Tx Global Out Flow Threshold Set Register	4602 0030h
00020034h	CPSW_TX_G_OFLOW_THRESH_CLR_REG	PFC Tx Global Out Flow Threshold Clear Register	4602 0034h
00020038h	CPSW_TX_G_BUF_THRESH_SET_L_REG	PFC Global Tx Buffer Threshold Set Low Register	4602 0038h
0002003Ch	CPSW_TX_G_BUF_THRESH_SET_H_REG	PFC Global Tx Buffer Threshold Set High Register	4602 003Ch
00020040h	CPSW_TX_G_BUF_THRESH_CLR_L_REG	PFC Global Tx Buffer Threshold Clear Low Register	4602 0040h
00020044h	CPSW_TX_G_BUF_THRESH_CLR_H_REG	PFC Global Tx Buffer Threshold Clear High Register	4602 0044h
00020050h	CPSW_VLAN_LTYPE_REG	VLAN LTYPE Outer and Inner Register	4602 0050h
00020054h	CPSW_EST_TS_DOMAIN_REG	EST Timestamp Domain Register	4602 0054h
00020100h	CPSW_TX_PRI0_MAXLEN_REG	Priority 0 Maximum Transmit Packet Length Register	4602 0100h
00020104h	CPSW_TX_PRI1_MAXLEN_REG	Priority 1 Maximum Transmit Packet Length Register	4602 0104h
00020108h	CPSW_TX_PRI2_MAXLEN_REG	Priority 2 Maximum Transmit Packet Length Register	4602 0108h
0002010Ch	CPSW_TX_PRI3_MAXLEN_REG	Priority 3 Maximum Transmit Packet Length Register	4602 010Ch
00020110h	CPSW_TX_PRI4_MAXLEN_REG	Priority 4 Maximum Transmit Packet Length Register	4602 0110h
00020114h	CPSW_TX_PRI5_MAXLEN_REG	Priority 5 Maximum Transmit Packet Length Register	4602 0114h
00020118h	CPSW_TX_PRI6_MAXLEN_REG	Priority 6 Maximum Transmit Packet Length Register	4602 0118h
0002011Ch	CPSW_TX_PRI7_MAXLEN_REG	Priority 7 Maximum Transmit Packet Length Register	4602 011Ch

Table 7-74. MCU_CPSW0_CONTROL Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_CON TROL Physical Address
00021004h	CPSW_P0_CONTROL_REG	CPPI Port 0 Control Register	4602 1004h
00021008h	CPSW_P0_FLOW_ID_OFFSET_REG	CPPI Port 0 Transmit FLOW ID Offset Register	4602 1008h
00021010h	CPSW_P0_BLK_CNT_REG	CPPI Port 0 FIFO Block Usage Count Register	4602 1010h
00021014h	CPSW_P0_PORT_VLAN_REG	CPPI Port 0 VLAN Register	4602 1014h
00021018h	CPSW_P0_TX_PRI_MAP_REG	CPPI Port 0 Tx Header Priority to Switch Priority Map Register	4602 1018h
0002101Ch	CPSW_P0_PRI_CTL_REG	CPPI Port 0 Priority Control Register	4602 101Ch
00021020h	CPSW_P0_RX_PRI_MAP_REG	CPPI Port 0 RX Paket Priority to Header Priority Map Register	4602 1020h
00021024h	CPSW_P0_RX_MAXLEN_REG	CPPI Port 0 Receive Frame Max Length Register	4602 1024h
00021028h	CPSW_P0_TX_BLKs_PRI_REG	CPPI Port 0 Transmit Block Sub Per Priority Register	4602 1028h
00021030h	CPSW_P0_IDLE2LPI_REG	CPPI Port 0 EEE Idle to LPI Count Register	4602 1030h
00021034h	CPSW_P0_LPI2WAKE_REG	CPPI Port 0 EEE LPI to Wakeup Count Register	4602 1034h
00021038h	CPSW_P0_EEE_STATUS_REG	CPPI Port 0 EEE Port Status Register	4602 1038h
0002103Ch	CPSW_P0_RX_PKTS_PRI_REG	CPPI Port 0 Receive Packets Per Priority Register	4602 103Ch
0002104Ch	CPSW_P0_RX_GAP_REG	CPPI Port 0 Receive Gap Register	4602 104Ch
00021050h	CPSW_P0_FIFO_STATUS_REG	CPPI Port 0 FIFO Status Register	4602 1050h
00021120h + formula	CPSW_P0_RX_DSCP_MAP_REG_y	CPPI Port 0 Receive IPV4/IPV6 DSCP Map 0 to Map 7 Registers	4602 1120h + formula
00021140h + formula	CPSW_P0_PRI_CIR_REG_y	CPPI Port 0 Rx Priority 0 to Priority 7 Committed Information Rate Registers	4602 1140h + formula
00021160h + formula	CPSW_P0_PRI_EIR_REG_y	CPPI Port 0 Rx Priority 0 to Priority 7 Excess Information Rate Registers	4602 1160h + formula
00021180h	CPSW_P0_TX_D_THRESH_SET_L_REG	CPPI Port 0 Tx PFC Destination Threshold Set Low Register	4602 1180h
00021184h	CPSW_P0_TX_D_THRESH_SET_H_REG	CPPI Port 0 Tx PFC Destination Threshold Set High Register	4602 1184h
00021188h	CPSW_P0_TX_D_THRESH_CLR_L_REG	CPPI Port 0 Tx PFC Destination Threshold Clear Low Register	4602 1188h
0002118Ch	CPSW_P0_TX_D_THRESH_CLR_H_REG	CPPI Port 0 Tx PFC Destination Threshold Clear High Register	4602 118Ch
00021190h	CPSW_P0_TX_G_BUF_THRESH_SET_L_REG	CPPI Port 0 Tx PFC Global Buffer Threshold Set Low Register	4602 1190h
00021194h	CPSW_P0_TX_G_BUF_THRESH_SET_H_REG	CPPI Port 0 Tx PFC Global Buffer Threshold Set High Register	4602 1194h
00021198h	CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG	CPPI Port 0 Tx PFC Global Buffer Threshold Clear Low Register	4602 1198h
0002119Ch	CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG	CPPI Port 0 Tx PFC Global Buffer Threshold Clear High Register	4602 119Ch
00021300h	CPSW_P0_SRC_ID_A_REG	CPPI Port 0 CPPI Source ID A Register	4602 1300h
00021304h	RESERVED	Reserved	4602 1304h

Table 7-74. MCU_CPSW0_CONTROL Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_CON TROL Physical Address
00021320h	CPSW_P0_HOST_BLKs_PRI_REG	CPPI Port 0 Host Blocks Priority Register	4602 1320h
00022000h	CPSW_PN_RESERVED_REG	Reserved Register	4602 2000h
00022004h	CPSW_PN_CONTROL_REG	Ethernet Port N Control Register	4602 2004h
00022008h	CPSW_PN_MAX_BLKs_REG	Ethernet Port N Maximum Blocks Register	4602 2008h
00022010h	CPSW_PN_BLK_CNT_REG	Ethernet Port N FIFO Block Usage Count Register	4602 2010h
00022014h	CPSW_PN_PORT_VLAN_REG	Ethernet Port N VLAN Register	4602 2014h
00022018h	CPSW_PN_TX_PRI_MAP_REG	Ethernet Port N Tx Header Priority to Switch Priority Mapping Register	4602 2018h
0002201Ch	CPSW_PN_PRI_CTL_REG	Ethernet Port N Priority Control Register	4602 201Ch
00022020h	CPSW_PN_RX_PRI_MAP_REG	Ethernet Port N RX Paket Priority to Header Priority Map	4602 2020h
00022024h	CPSW_PN_RX_MAXLEN_REG	Ethernet Port N Receive Frame Maximum Length Register	4602 2024h
00022028h	CPSW_PN_TX_BLKs_PRI_REG	Ethernet Port N Transmit Block Sub Per Priority Register	4602 2028h
0002202Ch	CPSW_PN_RX_FLOW_THRESH_REG	Ethernet Port N Receive Flow Threshold Register	4602 202Ch
00022030h	CPSW_PN_IDLE2LPI_REG	Ethernet Port N EEE Idle to LPI Count Register	4602 2030h
00022034h	CPSW_PN_LPI2WAKE_REG	Ethernet Port N EEE LPI to Wake Count Register	4602 2034h
00022038h	CPSW_PN_EEE_STATUS_REG	Ethernet Port N EEE Status Register	4602 2038h
00022040h	CPSW_PN_IET_CONTROL_REG	Ethernet Port N FIFO Status Register	4602 2040h
00022044h	CPSW_PN_IET_STATUS_REG	Ethernet Port N Enhanced Scheduled Traffic (EST) Control Register	4602 2044h
00022048h	CPSW_PN_IET_VERIFY_REG	Ethernet Port N Receive IPV4/IPV6 DSCP Map 0 to Map 7 Registers	4602 2048h
00022050h	CPSW_PN_FIFO_STATUS_REG	Ethernet Port N Rx Priority 0 to Priority 7 Committed Information Rate Registers	4602 2050h
00022060h	CPSW_PN_EST_CONTROL_REG	Ethernet Port N Rx Priority 0 to Priority 7 Excess Information Rate Registers	4602 2060h
00022120h + formula	CPSW_PN_RX_DSCP_MAP_REG_y	Ethernet Port N Tx PFC Destination Threshold Set Low Register	4602 2120h + formula
00022140h + formula	CPSW_PN_PRI_CIR_REG_y	Ethernet Port N Tx PFC Destination Threshold Set High Register	4602 2140h + formula
00022160h + formula	CPSW_PN_PRI_EIR_REG_y	Ethernet Port N Tx PFC Destination Threshold Clear Low Register	4602 2160h + formula
00022180h	CPSW_PN_TX_D_THRESH_SET_L_REG	Ethernet Port N Tx PFC Destination Threshold Clear High Register	4602 2180h
00022184h	CPSW_PN_TX_D_THRESH_SET_H_REG	Ethernet Port N Tx PFC Global Buffer Threshold Set Low Register	4602 2184h
00022188h	CPSW_PN_TX_D_THRESH_CLR_L_REG	Ethernet Port N Tx PFC Global Buffer Threshold Set High Register	4602 2188h

Table 7-74. MCU_CPSW0_CONTROL Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_CON TROL Physical Address
0002218Ch	CPSW_PN_TX_D_THRESH_CLR_H_REG	Ethernet Port N Tx PFC Global Buffer Threshold Clear Low Register	4602 218Ch
00022190h	CPSW_PN_TX_G_BUF_THRESH_SET_L_REG	Ethernet Port N Tx PFC Global Buffer Threshold Clear High Register	4602 2190h
00022194h	CPSW_PN_TX_G_BUF_THRESH_SET_H_REG	Ethernet Port N Tx Destination Out Flow Add Values Low Register	4602 2194h
00022198h	CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG	Ethernet Port N Tx Destination Out Flow Add Values High Register	4602 2198h
0002219Ch	CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG	Ethernet Port N Tx Pause Frame Source Address Low Register	4602 219Ch
00022300h	CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG	Ethernet Port N Tx Pause Frame Source Address High Register	4602 2300h
00022304h	CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG	Ethernet Port N Time Sync Control Register	4602 2304h
00022308h	CPSW_PN_SA_L_REG	Ethernet Port N Time Sync LTYPE Register (and SEQ_ID_OFFSET)	4602 2308h
0002230Ch	CPSW_PN_SA_H_REG	Ethernet Port N Time Sync VLAN2 and VLAN2 Register	4602 230Ch
00022310h	CPSW_PN_TS_CTL_REG	Ethernet Port N Time Sync Control and LTYPE 2 Register	4602 2310h
00022314h	CPSW_PN_TS_SEQ_LTYPE_REG	Ethernet Port N Time Sync Control 2 Register	4602 2314h
00022318h	CPSW_PN_TS_VLAN_LTYPE_REG	Ethernet Port N Mac Control Register	4602 2318h
0002231Ch	CPSW_PN_TS_CTL_LTYPE2_REG	Ethernet Port N Mac Status Register	4602 231Ch
00022320h	CPSW_PN_TS_CTL2_REG	Ethernet Port N Mac Software Reset Register	4602 2320h
00022330h	CPSW_PN_MAC_CONTROL_REG	Ethernet Port N Mac Backoff Test Register	4602 2330h
00022334h	CPSW_PN_MAC_STATUS_REG	Ethernet Port N 802.3 Receive Pause Timer Register	4602 2334h
00022338h	CPSW_PN_MAC_SOFT_RESET_REG	Ethernet Port N PFC Priority 0 to Priority 7 Rx Pause Timer Registers	4602 2338h
0002233Ch	CPSW_PN_MAC_BOFFTEST_REG	Ethernet Port N 802.3 Tx Pause Timer Registers	4602 233Ch
00022340h	CPSW_PN_MAC_RX_PAUSETIMER_REG	Ethernet Port N PFC Priority 0 to Priority 7 Tx Pause Timer Registers	4602 2340h
00022350h + formula ⁽¹⁾	CPSW_PN_MAC_RXN_PAUSETIMER_REG_y	Ethernet Port N Emulation Control Register	4602 2350h + formula
00022370h	CPSW_PN_MAC_TX_PAUSETIMER_REG	Ethernet Port N Tx Inter Packet Gap Register	4602 2370h
00022380h + formula	CPSW_PN_MAC_TXN_PAUSETIMER_REG_y		4602 2380h + formula
000223A0h	CPSW_PN_MAC_EMCONTROL_REG		4602 23A0h
000223A4h	CPSW_PN_MAC_TX_GAP_REG		4602 23A4h
000223ACh	CPSW_PN_INTERVLAN_OPX_POINTER_REG		4602 23ACh
000223B0h	CPSW_PN_INTERVLAN_OPX_A_REG		4602 23B0h
000223B4h	CPSW_PN_INTERVLAN_OPX_B_REG		4602 23B4h
000223B8h	CPSW_PN_INTERVLAN_OPX_C_REG		4602 23B8h

Table 7-74. MCU_CPSW0_CONTROL Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_CON TROL Physical Address
000223BCh	CPSW_PN_INTERVLAN_OPX_D_REG		4602 23BCh

(1) y = 0 to 7

7.2.1 CPSW_CPSW_ID_VER_REG Register (Offset = 00020000h) [reset = 6BA80100h]

CPSW_CPSW_ID_VER_REG is shown in [Figure 7-36](#) and described in [Table 7-76](#).

Return to [Summary Table](#).

CPSW ID Version Register.

Table 7-75. CPSW_CPSW_ID_VER_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0000h

Figure 7-36. CPSW_CPSW_ID_VER_REG Register

31	30	29	28	27	26	25	24
IDENT							
R-6BA8h							
23	22	21	20	19	18	17	16
IDENT							
R-6BA8h							
15	14	13	12	11	10	9	8
RTL_VER				MAJOR_VER			
R-0h				R-1h			
7	6	5	4	3	2	1	0
CUSTOM_VER		MINOR_VER					
R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 7-76. CPSW_CPSW_ID_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	IDENT	R	6BA8h	Identification Value
15-11	RTL_VER	R	Eh	RTL Version Value
10-8	MAJOR_VER	R	1h	Major Version Value
7-6	CUSTOM_VER	R	0h	Custom Version Value
5-0	MINOR_VER	R	0h	Minor Version Value

7.2.2 CPSW_CONTROL_REG Register (Offset = 00020004h) [reset = X]

CPSW_CONTROL_REG is shown in Figure 7-37 and described in Table 7-78.

Return to [Summary Table](#).

CPSW Switch Control Register.

Table 7-77. CPSW_CONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0004h

Figure 7-37. CPSW_CONTROL_REG Register

31	30	29	28	27	26	25	24
ECC_CRC_MODE	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED					EST_ENABLE	IET_ENABLE	EEE_ENABLE
R/W-X					R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
P0_RX_PASS_CRC_ERR	P0_RX_PAD	P0_TX_CRC_REMOVE	RESERVED	P8_PASS_PRI_TAGGED	P7_PASS_PRI_TAGGED	P6_PASS_PRI_TAGGED	P5_PASS_PRI_TAGGED
R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
P4_PASS_PRI_TAGGED	P3_PASS_PRI_TAGGED	P2_PASS_PRI_TAGGED	P1_PASS_PRI_TAGGED	P0_PASS_PRI_TAGGED	P0_ENABLE	VLAN_AWARE	S_CN_SWITCH
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-78. CPSW_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_CRC_MODE	R/W	0h	ECC CRC Mode. 0h = ECC errors induced through the ECC aggregator flip bits in the packet headers (not in packet data). 1h = ECC errors induced through the ECC aggregator flip bits in the packet data (not in the packet headers).
30-19	RESERVED	R/W	X	
18	EST_ENABLE	R/W	0h	Enhanced Scheduled Traffic enable (EST) 0h = EST is disabled 1h = EST is enabled
17	IET_ENABLE	R/W	0h	Interspersed Express Traffic enable (IET) 0h = IET is disabled 1h = IET is enabled
16	EEE_ENABLE	R/W	0h	Energy Efficient Ethernet enable 0h = Energy Efficient Ethernet is disabled 1h = Energy Efficient Ethernet is enabled
15	P0_RX_PASS_CRC_ERR	R/W	0h	Port 0 Pass Received CRC errors 0h = Packets received with CRC errors on Port 0 are dropped. 1h = Packets received with CRC errors on Port 0 are transferred to the destination ports.

Table 7-78. CPSW_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	P0_RX_PAD	R/W	0h	Port 0 Receive Short Packet Pad 0h = Short packets are dropped. 1h = Short packets are padded to 64-bytes (with pad and added CRC) if the CRC is not passed in. Short packets are dropped if the CRC is passed (in the Info0 word).
13	P0_TX_CRC_REMOVE	R/W	0h	Port 0 Transmit CRC remove. 0h = Do not remove the CRC on Port 0 transmit (egress) packets. 1h = Remove the CRC on all Port 0 transmit (egress) packets.
12	RESERVED	R/W	X	
11	P8_PASS_PRI_TAGGED	R/W	0h	Port 8 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P8_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
10	P7_PASS_PRI_TAGGED	R/W	0h	Port 7 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P7_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
9	P6_PASS_PRI_TAGGED	R/W	0h	Port 6 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P6_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
8	P5_PASS_PRI_TAGGED	R/W	0h	Port 5 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P5_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
7	P4_PASS_PRI_TAGGED	R/W	0h	Port 4 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P4_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
6	P3_PASS_PRI_TAGGED	R/W	0h	Port 3 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P3_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
5	P2_PASS_PRI_TAGGED	R/W	0h	Port 2 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P2_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
4	P1_PASS_PRI_TAGGED	R/W	0h	Port 1 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P1_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
3	P0_PASS_PRI_TAGGED	R/W	0h	Port 0 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port P0_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
2	P0_ENABLE	R/W	0h	Port 0 Enable 0h = CPPI port (port 0) packet operations are disabled 1h = CPPI port (port 0) packet operations are enabled

Table 7-78. CPSW_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VLAN_AWARE	R/W	0h	VLAN Aware Mode: 0h = CPSW_NU is in the VLAN unaware mode. 1h = CPSW_NU is in the VLAN aware mode.
0	S_CN_SWITCH	R/W	0h	Service or Customer VLAN switch. 0h = Customer switch. VLAN processing uses the inner_vlan_ltype. 1h = Service switch. VLAN processing uses the outer_vlan_ltype.

7.2.3 CPSW_EM_CONTROL_REG Register (Offset = 00020010h) [reset = X]

CPSW_EM_CONTROL_REG is shown in [Figure 7-38](#) and described in [Table 7-80](#).

Return to [Summary Table](#).

CPSW Emulation Control Register.

Table 7-79. CPSW_EM_CONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0010h

Figure 7-38. CPSW_EM_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-80. CPSW_EM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

7.2.4 CPSW_STAT_PORT_EN_REG Register (Offset = 00020014h) [reset = X]

CPSW_STAT_PORT_EN_REG is shown in [Figure 7-39](#) and described in [Table 7-82](#).

Return to [Summary Table](#).

CPSW Statistics Port Enable Register.

Table 7-81. CPSW_STAT_PORT_EN_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0014h

Figure 7-39. CPSW_STAT_PORT_EN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							P8_STAT_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-82. CPSW_STAT_PORT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	P8_STAT_EN	R/W	0h	Port 8 Statistics Enable (if N > 8) 0h = Port 8 statistics are not enabled 1h = Port 8 statistics are enabled.
7	P7_STAT_EN	R/W	0h	Port 7 Statistics Enable (if N > 7) 0h = Port 7 statistics are not enabled 1h = Port 7 statistics are enabled.
6	P6_STAT_EN	R/W	0h	Port 6 Statistics Enable (if N > 6) 0h = Port 6 statistics are not enabled 1h = Port 6 statistics are enabled.
5	P5_STAT_EN	R/W	0h	Port 5 Statistics Enable (if N > 5) 0h = Port 5 statistics are not enabled 1h = Port 5 statistics are enabled.
4	P4_STAT_EN	R/W	0h	Port 4 Statistics Enable (if N > 4) 0h = Port 4 statistics are not enabled 1h = Port 4 statistics are enabled.
3	P3_STAT_EN	R/W	0h	Port 3 Statistics Enable (if N > 3) 0h = Port 3 statistics are not enabled 1h = Port 3 statistics are enabled.
2	P2_STAT_EN	R/W	0h	Port 2 Statistics Enable (if N > 2) 0h = Port 2 statistics are not enabled 1h = Port 2 statistics are enabled.

Table 7-82. CPSW_STAT_PORT_EN_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	P1_STAT_EN	R/W	0h	Port 1 Statistics Enable 0h = Port 1 statistics are not enabled 1h = Port 1 statistics are enabled.
0	P0_STAT_EN	R/W	0h	Port 0 Statistics Enable 0h = Port 0 statistics are not enabled 1h = Port 0 statistics are enabled.

7.2.5 CPSW_PTYPE_REG Register (Offset = 00020018h) [reset = X]

CPSW_PTYPE_REG is shown in Figure 7-40 and described in Table 7-84.

Return to [Summary Table](#).

CPSW Transmit Priority Type Register.

Table 7-83. CPSW_PTYPE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0018h

Figure 7-40. CPSW_PTYPE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							P8_PTYPE_ESC
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC	P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				ESC_PRI_LD_VAL			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-84. CPSW_PTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	P8_PTYPE_ESC	R/W	0h	Port 8 Priority Type Escalate (if N > 8) 0h = Port 8 priority type fixed 1h = Port 8 priority type escalate
15	P7_PTYPE_ESC	R/W	0h	Port 7 Priority Type Escalate (if N > 7) 0h = Port 7 priority type fixed 1h = Port 7 priority type escalate
14	P6_PTYPE_ESC	R/W	0h	Port 6 Priority Type Escalate (if N > 6) 0h = Port 6 priority type fixed 1h = Port 6 priority type escalate
13	P5_PTYPE_ESC	R/W	0h	Port 5 Priority Type Escalate (if N > 5) 0h = Port 5 priority type fixed 1h = Port 5 priority type escalate
12	P4_PTYPE_ESC	R/W	0h	Port 4 Priority Type Escalate (if N > 4) 0h = Port 4 priority type fixed 1h = Port 4 priority type escalate
11	P3_PTYPE_ESC	R/W	0h	Port 3 Priority Type Escalate (if N > 3) 0h = Port 3 priority type fixed 1h = Port 3 priority type escalate

Table 7-84. CPSW_PTYPE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	P2_PTYPE_ESC	R/W	0h	Port 2 Priority Type Escalate (if N > 2) 0h = Port 2 priority type fixed 1h = Port 2 priority type escalate
9	P1_PTYPE_ESC	R/W	0h	Port 1 Priority Type Escalate 0h = Port 1 priority type fixed 1h = Port 1 priority type escalate
8	P0_PTYPE_ESC	R/W	0h	Port 0 Priority Type Escalate 0h = Port 0 priority type fixed 1h = Port 0 priority type escalate
7-5	RESERVED	R/W	X	
4-0	ESC_PRI_LD_VAL	R/W	0h	Escalate Priority Load Value When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority. The min value of ESC_PRI_LD_VAL = 2h.

7.2.6 CPSW_SOFT_IDLE_REG Register (Offset = 0002001Ch) [reset = X]

CPSW_SOFT_IDLE_REG is shown in [Figure 7-41](#) and described in [Table 7-86](#).

Return to [Summary Table](#).

CPSW Software Idle

Table 7-85. CPSW_SOFT_IDLE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 001Ch

Figure 7-41. CPSW_SOFT_IDLE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							SOFT_IDLE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-86. CPSW_SOFT_IDLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	SOFT_IDLE	R/W	0h	Software Idle. 0h = Not in Idle. 1h = Command a MCU_CPSW0 software Idle. When set, no packets will be started to be unloaded from ports 0 through 4 receive unload. Packets that are currently being unloaded are unaffected.

7.2.7 CPSW_THRU_RATE_REG Register (Offset = 00020020h) [reset = X]

CPSW_THRU_RATE_REG is shown in [Figure 7-42](#) and described in [Table 7-88](#).

Return to [Summary Table](#).

CPSW Thru Rate Register.

Table 7-87. CPSW_THRU_RATE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0020h

Figure 7-42. CPSW_THRU_RATE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
SL_RX_THRU_RATE				RESERVED			
R/W-3h				R/W-X			
7	6	5	4	3	2	1	0
RESERVED				P0_RX_THRU_RATE			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-88. CPSW_THRU_RATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-12	SL_RX_THRU_RATE	R/W	3h	Ethernet Port Switch FIFO receive through rate. This register value is the maximum throughput of the Ethernet ports to the crossbar SCR. The default is one 8-byte word for every 3 VBUSP_GCLK periods maximum. The minimum value is 2. This is not a field that is intended to be changed by a user.
11-4	RESERVED	R/W	X	
3-0	P0_RX_THRU_RATE	R/W	1h	CPPI FIFO (port 0) receive through rate. This register value is the maximum throughput of the CPPI FIFO (port 0) into the MCU_CPSW0. The minimum value is 1. This field is not intended to be changed by the user.

7.2.8 CPSW_GAP_THRESH_REG Register (Offset = 00020024h) [reset = X]

CPSW_GAP_THRESH_REG is shown in [Figure 7-43](#) and described in [Table 7-90](#).

Return to [Summary Table](#).

CPSW Transmit FIFO Short Gap Threshold Register.

Table 7-89. CPSW_GAP_THRESH_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0024h

Figure 7-43. CPSW_GAP_THRESH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												GAP_THRESH			
R/W-X												R/W-Bh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-90. CPSW_GAP_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	GAP_THRESH	R/W	Bh	Ethernet Port Short Gap Threshold. This is the Ethernet port associated FIFO transmit block usage value for triggering transmit short gap (when short gap is enabled).

7.2.9 CPSW_TX_START_WDS_REG Register (Offset = 00020028h) [reset = X]

CPSW_TX_START_WDS_REG is shown in [Figure 7-44](#) and described in [Table 7-92](#).

Return to [Summary Table](#).

CPSW Transmit FIFO Start Words Register.

Table 7-91. CPSW_TX_START_WDS_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0028h

Figure 7-44. CPSW_TX_START_WDS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TX_START_WDS									
R/W-X						R/W-8h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-92. CPSW_TX_START_WDS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	TX_START_WDS	R/W	8h	FIFO Packet Transmit (egress) Start Words. This value is the number of required 32-byte packet words in an Ethernet transmit FIFO before the packet egress will begin. This value is non-zero to preclude Ethernet transmit underrun. Decimal 8 is the recommended value. It should not be increased unnecessarily to prevent adding to the switch latency.

7.2.10 CPSW_EEE_PRESCALE_REG Register (Offset = 0002002Ch) [reset = X]

CPSW_EEE_PRESCALE_REG is shown in [Figure 7-45](#) and described in [Table 7-94](#).

Return to [Summary Table](#).

CPSW Energy Efficient Ethernet Prescale Value Register.

Table 7-93. CPSW_EEE_PRESCALE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 002Ch

Figure 7-45. CPSW_EEE_PRESCALE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EEE_PRESCALE															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-94. CPSW_EEE_PRESCALE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	EEE_PRESCALE	R/W	0h	Energy Efficient Ethernet Pre-scale count load value.

7.2.11 CPSW_TX_G_OFLOW_THRESH_SET_REG Register (Offset = 00020030h) [reset = FFFFFFFh]

CPSW_TX_G_OFLOW_THRESH_SET_REG is shown in [Figure 7-46](#) and described in [Table 7-96](#).

Return to [Summary Table](#).

CPSW PFC Tx Global Out Flow Threshold Set

Table 7-95.
CPSW_TX_G_OFLOW_THRESH_SET_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0030h

Figure 7-46. CPSW_TX_G_OFLOW_THRESH_SET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-96. CPSW_TX_G_OFLOW_THRESH_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27-24	PRI6	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23-20	PRI5	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19-16	PRI4	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15-12	PRI3	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11-8	PRI2	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7-4	PRI1	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3-0	PRI0	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

7.2.12 CPSW_TX_G_OFLOW_THRESH_CLR_REG Register (Offset = 00020034h) [reset = 0h]

CPSW_TX_G_OFLOW_THRESH_CLR_REG is shown in Figure 7-47 and described in Table 7-98.

Return to [Summary Table](#).

CPSW PFC Tx Global Out Flow Threshold Clear Register.

Table 7-97.
CPSW_TX_G_OFLOW_THRESH_CLR_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0034h

Figure 7-47. CPSW_TX_G_OFLOW_THRESH_CLR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-98. CPSW_TX_G_OFLOW_THRESH_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27-24	PRI6	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23-20	PRI5	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19-16	PRI4	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15-12	PRI3	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11-8	PRI2	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7-4	PRI1	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3-0	PRI0	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

7.2.13 CPSW_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 00020038h) [reset = FFFFFFFFh]

CPSW_TX_G_BUF_THRESH_SET_L_REG is shown in [Figure 7-48](#) and described in [Table 7-100](#).

Return to [Summary Table](#).

CPSW PFC Global Tx Buffer Threshold Set Low Register.

Table 7-99.
CPSW_TX_G_BUF_THRESH_SET_L_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0038h

Figure 7-48. CPSW_TX_G_BUF_THRESH_SET_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3								PRI2								PRI1								PRI0							
R/W-FFh								R/W-FFh								R/W-FFh								R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-100. CPSW_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI3	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23-16	PRI2	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15-8	PRI1	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7-0	PRI0	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

7.2.14 CPSW_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 0002003Ch) [reset = FFFFFFFFh]

CPSW_TX_G_BUF_THRESH_SET_H_REG is shown in [Figure 7-49](#) and described in [Table 7-102](#).

Return to [Summary Table](#).

CPSW PFC Global Tx Buffer Threshold Set High Register.

Table 7-101.
CPSW_TX_G_BUF_THRESH_SET_H_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 003Ch

Figure 7-49. CPSW_TX_G_BUF_THRESH_SET_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7								PRI6								PRI5								PRI4							
R/W-FFh								R/W-FFh								R/W-FFh								R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-102. CPSW_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI7	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23-16	PRI6	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15-8	PRI5	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7-0	PRI4	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

7.2.15 CPSW_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 00020040h) [reset = 0h]

CPSW_TX_G_BUF_THRESH_CLR_L_REG is shown in [Figure 7-50](#) and described in [Table 7-104](#).

Return to [Summary Table](#).

CPSW PFC Global Tx Buffer Threshold Clear Low Register.

Table 7-103.
CPSW_TX_G_BUF_THRESH_CLR_L_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0040h

Figure 7-50. CPSW_TX_G_BUF_THRESH_CLR_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3								PRI2								PRI1								PRI0							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-104. CPSW_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI3	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23-16	PRI2	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15-8	PRI1	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7-0	PRI0	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

7.2.16 CPSW_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 00020044h) [reset = 0h]

CPSW_TX_G_BUF_THRESH_CLR_H_REG is shown in [Figure 7-51](#) and described in [Table 7-106](#).

Return to [Summary Table](#).

CPSW PFC Global Tx Buffer Threshold Clear High Register.

Table 7-105.
CPSW_TX_G_BUF_THRESH_CLR_H_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0044h

Figure 7-51. CPSW_TX_G_BUF_THRESH_CLR_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7								PRI6								PRI5								PRI4							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-106. CPSW_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI7	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23-16	PRI6	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15-8	PRI5	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7-0	PRI4	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

7.2.17 CPSW_VLAN_LTYPE_REG Register (Offset = 00020050h) [reset = 88A88100h]

CPSW_VLAN_LTYPE_REG is shown in [Figure 7-52](#) and described in [Table 7-108](#).

Return to [Summary Table](#).

VLAN LTYPE Outer and Inner Register.

Table 7-107. CPSW_VLAN_LTYPE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0050h

Figure 7-52. CPSW_VLAN_LTYPE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLAN_LTYPE_OUTER																VLAN_LTYPE_INNER															
R/W-88A8h																R/W-8100h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-108. CPSW_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VLAN_LTYPE_OUTER	R/W	88A8h	Outer VLAN LTYPE
15-0	VLAN_LTYPE_INNER	R/W	8100h	Inner VLAN LTYPE

7.2.18 CPSW_EST_TS_DOMAIN_REG Register (Offset = 00020054h) [reset = X]

CPSW_EST_TS_DOMAIN_REG is shown in [Figure 7-53](#) and described in [Table 7-110](#).

Return to [Summary Table](#).

Enhanced Scheduled Traffic Host Event Domain Register.

Table 7-109. CPSW_EST_TS_DOMAIN_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0054h

Figure 7-53. CPSW_EST_TS_DOMAIN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EST_TS_DOMAIN							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-110. CPSW_EST_TS_DOMAIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	EST_TS_DOMAIN	R/W	0h	Enhanced Scheduled Traffic Host Event Domain. This value is used as the domain in the CPTS event to indicate that the event came from EST.

7.2.19 CPSW_TX_PRI0_MAXLEN_REG Register (Offset = 00020100h) [reset = X]

CPSW_TX_PRI0_MAXLEN_REG is shown in [Figure 7-54](#) and described in [Table 7-112](#).

Return to [Summary Table](#).

Priority 0 Maximum Transmit Packet Length Register.

**Table 7-111. CPSW_TX_PRI0_MAXLEN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0100h

Figure 7-54. CPSW_TX_PRI0_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI0_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-112. CPSW_TX_PRI0_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI0_MAXLEN	R/W	7E8h	Transmit Priority 0 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

7.2.20 CPSW_TX_PRI1_MAXLEN_REG Register (Offset = 00020104h) [reset = X]

CPSW_TX_PRI1_MAXLEN_REG is shown in [Figure 7-55](#) and described in [Table 7-114](#).

Return to [Summary Table](#).

Priority 1 Maximum Transmit Packet Length Register.

Table 7-113. CPSW_TX_PRI1_MAXLEN_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0104h

Figure 7-55. CPSW_TX_PRI1_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI1_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-114. CPSW_TX_PRI1_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI1_MAXLEN	R/W	7E8h	Transmit Priority 1 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

7.2.21 CPSW_TX_PRI2_MAXLEN_REG Register (Offset = 00020108h) [reset = X]

CPSW_TX_PRI2_MAXLEN_REG is shown in [Figure 7-56](#) and described in [Table 7-116](#).

Return to [Summary Table](#).

Priority 2 Maximum Transmit Packet Length Register.

**Table 7-115. CPSW_TX_PRI2_MAXLEN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0108h

Figure 7-56. CPSW_TX_PRI2_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI2_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-116. CPSW_TX_PRI2_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI2_MAXLEN	R/W	7E8h	Transmit Priority 2 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

7.2.22 CPSW_TX_PRI3_MAXLEN_REG Register (Offset = 0002010Ch) [reset = X]

CPSW_TX_PRI3_MAXLEN_REG is shown in [Figure 7-57](#) and described in [Table 7-118](#).

Return to [Summary Table](#).

Priority 3 Maximum Transmit Packet Length Register.

Table 7-117. CPSW_TX_PRI3_MAXLEN_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 010Ch

Figure 7-57. CPSW_TX_PRI3_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI3_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-118. CPSW_TX_PRI3_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI3_MAXLEN	R/W	7E8h	Transmit Priority 3 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

7.2.23 CPSW_TX_PRI4_MAXLEN_REG Register (Offset = 00020110h) [reset = X]

CPSW_TX_PRI4_MAXLEN_REG is shown in [Figure 7-58](#) and described in [Table 7-120](#).

Return to [Summary Table](#).

Priority 4 Maximum Transmit Packet Length Register.

**Table 7-119. CPSW_TX_PRI4_MAXLEN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0110h

Figure 7-58. CPSW_TX_PRI4_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI4_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-120. CPSW_TX_PRI4_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI4_MAXLEN	R/W	7E8h	Transmit Priority 4 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

7.2.24 CPSW_TX_PRI5_MAXLEN_REG Register (Offset = 00020114h) [reset = X]

CPSW_TX_PRI5_MAXLEN_REG is shown in [Figure 7-59](#) and described in [Table 7-122](#).

Return to [Summary Table](#).

Priority 5 Maximum Transmit Packet Length Register.

Transmit Priority 5 Maximum Length

**Table 7-121. CPSW_TX_PRI5_MAXLEN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0114h

Figure 7-59. CPSW_TX_PRI5_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI5_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-122. CPSW_TX_PRI5_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI5_MAXLEN	R/W	7E8h	Transmit Priority 5 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

7.2.25 CPSW_TX_PRI6_MAXLEN_REG Register (Offset = 00020118h) [reset = X]

CPSW_TX_PRI6_MAXLEN_REG is shown in [Figure 7-60](#) and described in [Table 7-124](#).

Return to [Summary Table](#).

Priority 6 Maximum Transmit Packet Length Register.

**Table 7-123. CPSW_TX_PRI6_MAXLEN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 0118h

Figure 7-60. CPSW_TX_PRI6_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI6_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-124. CPSW_TX_PRI6_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI6_MAXLEN	R/W	7E8h	Transmit Priority 6 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

7.2.26 CPSW_TX_PRI7_MAXLEN_REG Register (Offset = 0002011Ch) [reset = X]

CPSW_TX_PRI7_MAXLEN_REG is shown in [Figure 7-61](#) and described in [Table 7-126](#).

Return to [Summary Table](#).

Priority 7 Maximum Transmit Packet Length Register.

Table 7-125. CPSW_TX_PRI7_MAXLEN_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 011Ch

Figure 7-61. CPSW_TX_PRI7_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI7_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-126. CPSW_TX_PRI7_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI7_MAXLEN	R/W	7E8h	Transmit Priority 7 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

7.2.27 CPSW_P0_CONTROL_REG Register (Offset = 00021004h) [reset = X]

CPSW_P0_CONTROL_REG is shown in Figure 7-62 and described in Table 7-128.

Return to [Summary Table](#).

CPPI Port 0 Control Register.

Table 7-127. CPSW_P0_CONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1004h

Figure 7-62. CPSW_P0_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					RX_REMAP_D SCP_V6	RX_REMAP_D SCP_V4	RX_REMAP_V LAN
R/W-X					R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_ECC_ERR _EN	TX_ECC_ERR _EN	RESERVED					
R/W-0h	R/W-0h	R/W-X					
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_E N	DSCP_IPV4_E N	RX_CHECKSU M_EN
R/W-X					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-128. CPSW_P0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18	RX_REMAP_DSCP_V6	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
17	RX_REMAP_DSCP_V4	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
16	RX_REMAP_VLAN	R/W	0h	Port 0 receive remap thread to VLAN.
15	RX_ECC_ERR_EN	R/W	0h	Port 0 receive ECC Error Enable This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port 0 transmit ECC Error Enable This bit must be set to enable transmit ECC error operations
13-3	RESERVED	R/W	X	
2	DSCP_IPV6_EN	R/W	0h	Port 0 IPv6 DSCP enable 0h = IPV6 DSCP priority mapping is disabled 1h = IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	Port 0 IPV4 DSCP enable 0h = IPV4 DSCP priority mapping is disabled 1h = IPV4 DSCP priority mapping is enabled
0	RX_CHECKSUM_EN	R/W	0h	Port 0 Receive (port 0 ingress) Checksum Enable 0h = Port 0 receive checksum is disabled 1h = Port 0 receive checksum is enabled

7.2.28 CPSW_P0_FLOW_ID_OFFSET_REG Register (Offset = 00021008h) [reset = X]

CPSW_P0_FLOW_ID_OFFSET_REG is shown in [Figure 7-63](#) and described in [Table 7-130](#).

Return to [Summary Table](#).

CPPI Port 0 Transmit FLOW ID Offset Register.

Table 7-129. CPSW_P0_FLOW_ID_OFFSET_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1008h

Figure 7-63. CPSW_P0_FLOW_ID_OFFSET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		VALUE													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-130. CPSW_P0_FLOW_ID_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	VALUE	R/W	0h	This value is added to the thread/Flow_ID in CPPI transmit PSI Info Word 0

7.2.29 CPSW_P0_BLK_CNT_REG Register (Offset = 00021010h) [reset = X]

CPSW_P0_BLK_CNT_REG is shown in [Figure 7-64](#) and described in [Table 7-132](#).

Return to [Summary Table](#).

CPPI Port 0 FIFO Block Usage Count Register.

Table 7-131. CPSW_P0_BLK_CNT_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1010h

Figure 7-64. CPSW_P0_BLK_CNT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED				TX_BLK_CNT			
R-X				R-0h			
7	6	5	4	3	2	1	0
RESERVED			RX_BLK_CNT				
R-X			R-1h				

LEGEND: R = Read Only; -n = value after reset

Table 7-132. CPSW_P0_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	X	
12-8	TX_BLK_CNT	R	0h	Port 0 Transmit Block Count Usage. This value is the number of blocks allocated to the FIFO logical transmit queues. Note: For N=2 this field is always zero (no transmit FIFO).
7-6	RESERVED	R	X	
5-0	RX_BLK_CNT	R	1h	Port 0 Receive Block Count Usage. This value is the number of blocks allocated in the receive FIFO.

7.2.30 CPSW_P0_PORT_VLAN_REG Register (Offset = 00021014h) [reset = X]

CPSW_P0_PORT_VLAN_REG is shown in [Figure 7-65](#) and described in [Table 7-134](#).

Return to [Summary Table](#).

CPPI Port 0 VLAN Register.

**Table 7-133. CPSW_P0_PORT_VLAN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1014h

Figure 7-65. CPSW_P0_PORT_VLAN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W-0h			R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-134. CPSW_P0_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11-0	PORT_VID	R/W	0h	Port VLAN ID

7.2.31 CPSW_P0_TX_PRI_MAP_REG Register (Offset = 00021018h) [reset = X]

CPSW_P0_TX_PRI_MAP_REG is shown in Figure 7-66 and described in Table 7-136.

Return to [Summary Table](#).

CPPI Port 0 Tx Header Pri to Switch Pri Mapping

**Table 7-135. CPSW_P0_TX_PRI_MAP_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1018h

Figure 7-66. CPSW_P0_TX_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED		PRI7		RESERVED		PRI6	
R/W-X		R/W-7h		R/W-X		R/W-6h	
23	22	21	20	19	18	17	16
RESERVED		PRI5		RESERVED		PRI4	
R/W-X		R/W-5h		R/W-X		R/W-4h	
15	14	13	12	11	10	9	8
RESERVED		PRI3		RESERVED		PRI2	
R/W-X		R/W-3h		R/W-X		R/W-2h	
7	6	5	4	3	2	1	0
RESERVED		PRI1		RESERVED		PRI0	
R/W-X		R/W-1h		R/W-X		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-136. CPSW_P0_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	R/W	X	
26-24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	R/W	X	
22-20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	R/W	X	
18-16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	R/W	X	
14-12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	R/W	X	
10-8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	R/W	X	
6-4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.

Table 7-136. CPSW_P0_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

7.2.32 CPSW_P0_PRI_CTL_REG Register (Offset = 0002101Ch) [reset = X]

CPSW_P0_PRI_CTL_REG is shown in [Figure 7-67](#) and described in [Table 7-138](#).

Return to [Summary Table](#).

CPPI Port 0 Priority Control Register.

Table 7-137. CPSW_P0_PRI_CTL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 101Ch

Figure 7-67. CPSW_P0_PRI_CTL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RX_FLOW_PRI							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							RX_PTYPE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-138. CPSW_P0_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority). Note: Priority Based Flow Control feature is not supported for 2-port CPSW module. This field should remain zero.
15-9	RESERVED	R/W	X	
8	RX_PTYPE	R/W	0h	Receive Priority Type 0h = Fixed priority 1h = Round Robin priority
7-0	RESERVED	R/W	X	

7.2.33 CPSW_P0_RX_PRI_MAP_REG Register (Offset = 00021020h) [reset = X]

CPSW_P0_RX_PRI_MAP_REG is shown in Figure 7-68 and described in Table 7-140.

Return to [Summary Table](#).

CPPI Port 0 RX Pkt Pri to Header Pri Map.

Table 7-139. CPSW_P0_RX_PRI_MAP_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1020h

Figure 7-68. CPSW_P0_RX_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED		PRI7		RESERVED		PRI6	
R/W-X		R/W-7h		R/W-X		R/W-6h	
23	22	21	20	19	18	17	16
RESERVED		PRI5		RESERVED		PRI4	
R/W-X		R/W-5h		R/W-X		R/W-4h	
15	14	13	12	11	10	9	8
RESERVED		PRI3		RESERVED		PRI2	
R/W-X		R/W-3h		R/W-X		R/W-2h	
7	6	5	4	3	2	1	0
RESERVED		PRI1		RESERVED		PRI0	
R/W-X		R/W-1h		R/W-X		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-140. CPSW_P0_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	R/W	X	
26-24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	R/W	X	
22-20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	R/W	X	
18-16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	R/W	X	
14-12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	R/W	X	
10-8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	R/W	X	
6-4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.

Table 7-140. CPSW_P0_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

7.2.34 CPSW_P0_RX_MAXLEN_REG Register (Offset = 00021024h) [reset = X]

CPSW_P0_RX_MAXLEN_REG is shown in [Figure 7-69](#) and described in [Table 7-142](#).

Return to [Summary Table](#).

CPPI Port 0 Receive Frame Max Length.

Table 7-141. CPSW_P0_RX_MAXLEN_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1024h

Figure 7-69. CPSW_P0_RX_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		RX_MAXLEN													
R/W-X																		R/W-5EEh													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-142. CPSW_P0_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_MAXLEN	R/W	5EEh	<p>RX Maximum Frame Length.</p> <p>This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_P0_RX_MAXLEN_REG are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN) when fifo_blk_size = 4.</p> <p>When fifo_blk_size = 1 the maximum value is 2024 (including VLAN).</p>

7.2.35 CPSW_P0_TX_BLKs_PRI_REG Register (Offset = 00021028h) [reset = 01245678h]

CPSW_P0_TX_BLKs_PRI_REG is shown in [Figure 7-70](#) and described in [Table 7-144](#).

Return to [Summary Table](#).

CPPI Port 0 Transmit Block Sub Per Priority Register.

**Table 7-143. CPSW_P0_TX_BLKs_PRI_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1028h

Figure 7-70. CPSW_P0_TX_BLKs_PRI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-1h				R/W-2h				R/W-4h				R/W-5h				R/W-6h				R/W-7h				R/W-8h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-144. CPSW_P0_TX_BLKs_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Port Transmit Blocks Priority 7
27-24	PRI6	R/W	1h	Port Transmit Blocks Priority 6
23-20	PRI5	R/W	2h	Port Transmit Blocks Priority 5
19-16	PRI4	R/W	4h	Port Transmit Blocks Priority 4
15-12	PRI3	R/W	5h	Port Transmit Blocks Priority 3
11-8	PRI2	R/W	6h	Port Transmit Blocks Priority 2
7-4	PRI1	R/W	7h	Port Transmit Blocks Priority 1
3-0	PRI0	R/W	8h	Port Transmit Blocks Priority 0

7.2.36 CPSW_P0_IDLE2LPI_REG Register (Offset = 00021030h) [reset = X]

CPSW_P0_IDLE2LPI_REG is shown in [Figure 7-71](#) and described in [Table 7-146](#).

Return to [Summary Table](#).

CPPI Port 0 EEE Idle to LPI Count Register.

Table 7-145. CPSW_P0_IDLE2LPI_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1030h

Figure 7-71. CPSW_P0_IDLE2LPI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-146. CPSW_P0_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	COUNT	R/W	0h	Port 0 EEE Idle to LPI counter load value.

7.2.37 CPSW_P0_LPI2WAKE_REG Register (Offset = 00021034h) [reset = X]

CPSW_P0_LPI2WAKE_REG is shown in [Figure 7-72](#) and described in [Table 7-148](#).

Return to [Summary Table](#).

CPPI Port 0 EEE LPI to Wakeup Count Register.

Table 7-147. CPSW_P0_LPI2WAKE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1034h

Figure 7-72. CPSW_P0_LPI2WAKE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-148. CPSW_P0_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	COUNT	R/W	0h	Port 0 EEE LPI to wake counter load value.

7.2.38 CPSW_P0_EEE_STATUS_REG Register (Offset = 00021038h) [reset = X]

CPSW_P0_EEE_STATUS_REG is shown in Figure 7-73 and described in Table 7-150.

Return to [Summary Table](#).

CPPI Port 0 EEE Port Status Register.

Table 7-149. CPSW_P0_EEE_STATUS_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1038h

Figure 7-73. CPSW_P0_EEE_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
R-X	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-150. CPSW_P0_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	X	
6	TX_FIFO_EMPTY	R	1h	Port 0 Transmit FIFO packet count zero. This bit is set when there are no packets in the transmit FIFO. Note: for N=2 this bit is always set (there is no p0 transmit FIFO).
5	RX_FIFO_EMPTY	R	1h	Port 0 Receive FIFO packet count zero. This bit is set when there are no packets in the receive FIFO.
4	TX_FIFO_HOLD	R	0h	Port 0 Transmit FIFO hold. This bit is set during LPI and Wake time.
3	TX_WAKE	R	0h	Port 0 Receive Wake Time. This bit is set when the IDLE to Wake time is being counted.
2	TX_LPI	R	0h	Port 0 LPI. This bit is set when the CPPI streaming interface is in the LPI state. Transmit LPI and receive LPI are not separate for the CPPI port
1	RX_LPI	R	0h	Port 0 LPI. This bit is set when the CPPI streaming interface is in the LPI state. Transmit LPI and receive LPI are not separate for the CPPI port.
0	WAIT_IDLE2LPI	R	0h	Transmit Wait Idle to LPI. This bit is set when the port is counting the IDLE to LPI time.

7.2.39 CPSW_P0_RX_PKTS_PRI_REG Register (Offset = 0002103Ch) [reset = 0h]

CPSW_P0_RX_PKTS_PRI_REG is shown in [Figure 7-74](#) and described in [Table 7-152](#).

Return to [Summary Table](#).

CPPI Port 0 Receive Packets Per Priority Register.

**Table 7-151. CPSW_P0_RX_PKTS_PRI_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 103Ch

Figure 7-74. CPSW_P0_RX_PKTS_PRI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-152. CPSW_P0_RX_PKTS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Port 0 Receive (same as Port 1 Transmit) Packets Per Priority 7
27-24	PRI6	R/W	0h	Port 0 Receive (same as Port 1 Transmit) Packets Per Priority 6
23-20	PRI5	R/W	0h	Port 0 Receive (same as Port 1 Transmit) Packets Per Priority 5
19-16	PRI4	R/W	0h	Port 0 Receive (same as Port 1 Transmit) Packets Per Priority 4
15-12	PRI3	R/W	0h	Port 0 Receive (same as Port 1 Transmit) Packets Per Priority 3
11-8	PRI2	R/W	0h	Port 0 Receive (same as Port 1 Transmit) Packets Per Priority 2
7-4	PRI1	R/W	0h	Port 0 Receive (same as Port 1 Transmit) Packets Per Priority 1
3-0	PRI0	R/W	0h	Port 0 Receive (same as Port 1 Transmit) Packets Per Priority 0

7.2.40 CPSW_P0_RX_GAP_REG Register (Offset = 0002104Ch) [reset = X]

CPSW_P0_RX_GAP_REG is shown in [Figure 7-75](#) and described in [Table 7-154](#).

Return to [Summary Table](#).

CPPI Port 0 Receive Gap Register.

Table 7-153. CPSW_P0_RX_GAP_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 104Ch

Figure 7-75. CPSW_P0_RX_GAP_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						RX_GAP_CNT									
R/W-X						R/W-100h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_GAP_EN							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-154. CPSW_P0_RX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	RX_GAP_CNT	R/W	100h	Receive Gap Count. This is the number of clocks that will in the gap between received packet on port 0 when a priority has CPSW_P0_RX_GAP_REG[7-0] RX_GAP_EN bit field set.
15-8	RESERVED	R/W	X	
7-0	RX_GAP_EN	R/W	0h	Port 0 Receive Gap Enable

7.2.41 CPSW_P0_FIFO_STATUS_REG Register (Offset = 00021050h) [reset = X]

CPSW_P0_FIFO_STATUS_REG is shown in [Figure 7-76](#) and described in [Table 7-156](#).

Return to [Summary Table](#).

Port 0 FIFO Status

**Table 7-155. CPSW_P0_FIFO_STATUS_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1050h

Figure 7-76. CPSW_P0_FIFO_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_PRI_ACTIVE							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 7-156. CPSW_P0_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	TX_PRI_ACTIVE	R	0h	Port 0 Transmit FIFO Priority Active. Each bit indicates whether the corresponding FIFO priority has one or more queued packets on it or not. Note: For N=2 this field is always zero (there is no transmit FIFO).

7.2.42 CPSW_P0_RX_DSCP_MAP_REG_y Register (Offset = 00021120h + formula) [reset = X]

CPSW_P0_RX_DSCP_MAP_REG_y is shown in Figure 7-77 and described in Table 7-158.

Return to [Summary Table](#).

CPPI Port 0 Receive IPV4/IPV6 DSCP Map 0 to Map 7 Registers.

Offset = 00021120h + (y * 4h); where y = 0h to 7h

**Table 7-157. CPSW_P0_RX_DSCP_MAP_REG_y
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1120h + formula

Figure 7-77. CPSW_P0_RX_DSCP_MAP_REG_y Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
R/W-X	R/W-0h			R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
R/W-X	R/W-0h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-158. CPSW_P0_RX_DSCP_MAP_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	R/W	X	
26-24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	R/W	X	
22-20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	R/W	X	
18-16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	R/W	X	
14-12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	R/W	X	
10-8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	R/W	X	

Table 7-158. CPSW_P0_RX_DSCP_MAP_REG_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

7.2.43 CPSW_P0_PRI_CIR_REG_y Register (Offset = 00021140h + formula) [reset = X]

CPSW_P0_PRI_CIR_REG_y is shown in [Figure 7-78](#) and described in [Table 7-160](#).

Return to [Summary Table](#).

CPPI Port 0 Rx Priority 0 to Priority 7 Committed Information Rate Registers.

Offset = 00021140h + (y * 4h); where y = 0h to 7h

Table 7-159. CPSW_P0_PRI_CIR_REG_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1140h + formula

Figure 7-78. CPSW_P0_PRI_CIR_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI_CIR																											
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-160. CPSW_P0_PRI_CIR_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PRI_CIR	R/W	0h	Priority “y” Committed Information Rate Count Value

7.2.44 CPSW_P0_PRI_EIR_REG_y Register (Offset = 00021160h + formula) [reset = X]

CPSW_P0_PRI_EIR_REG_y is shown in [Figure 7-79](#) and described in [Table 7-162](#).

Return to [Summary Table](#).

CPPI Port 0 Rx Priority 0 to Priority 7 Excess Information Rate Registers.

Offset = 00021160h + (y * 4h); where y = 0h to 7h

Table 7-161. CPSW_P0_PRI_EIR_REG_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1160h + formula

Figure 7-79. CPSW_P0_PRI_EIR_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRI_EIR																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-162. CPSW_P0_PRI_EIR_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PRI_EIR	R/W	0h	Priority “y” Excess Information Rate Count Value

7.2.45 CPSW_P0_TX_D_THRESH_SET_L_REG Register (Offset = 00021180h) [reset = X]

CPSW_P0_TX_D_THRESH_SET_L_REG is shown in [Figure 7-80](#) and described in [Table 7-164](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Destination Threshold Set Low

Table 7-163. CPSW_P0_TX_D_THRESH_SET_L_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1180h

Figure 7-80. CPSW_P0_TX_D_THRESH_SET_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-164. CPSW_P0_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

7.2.46 CPSW_P0_TX_D_THRESH_SET_H_REG Register (Offset = 00021184h) [reset = X]

CPSW_P0_TX_D_THRESH_SET_H_REG is shown in [Figure 7-81](#) and described in [Table 7-166](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Destination Threshold Set High

Table 7-165.
CPSW_P0_TX_D_THRESH_SET_H_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1184h

Figure 7-81. CPSW_P0_TX_D_THRESH_SET_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-166. CPSW_P0_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

7.2.47 CPSW_P0_TX_D_THRESH_CLR_L_REG Register (Offset = 00021188h) [reset = X]

CPSW_P0_TX_D_THRESH_CLR_L_REG is shown in [Figure 7-82](#) and described in [Table 7-168](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Destination Threshold Clr Low

Table 7-167.
CPSW_P0_TX_D_THRESH_CLR_L_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1188h

Figure 7-82. CPSW_P0_TX_D_THRESH_CLR_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-168. CPSW_P0_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

7.2.48 CPSW_P0_TX_D_THRESH_CLR_H_REG Register (Offset = 0002118Ch) [reset = X]

CPSW_P0_TX_D_THRESH_CLR_H_REG is shown in [Figure 7-83](#) and described in [Table 7-170](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Destination Threshold Clr High

Table 7-169.
CPSW_P0_TX_D_THRESH_CLR_H_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 118Ch

Figure 7-83. CPSW_P0_TX_D_THRESH_CLR_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-170. CPSW_P0_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

7.2.49 CPSW_P0_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 00021190h) [reset = X]

CPSW_P0_TX_G_BUF_THRESH_SET_L_REG is shown in [Figure 7-84](#) and described in [Table 7-172](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Global Buffer Threshold Set Low

Table 7-171.
CPSW_P0_TX_G_BUF_THRESH_SET_L_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1190h

Figure 7-84. CPSW_P0_TX_G_BUF_THRESH_SET_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-172. CPSW_P0_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

7.2.50 CPSW_P0_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 00021194h) [reset = X]

CPSW_P0_TX_G_BUF_THRESH_SET_H_REG is shown in [Figure 7-85](#) and described in [Table 7-174](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Global Buffer Threshold Set High

Table 7-173.
CPSW_P0_TX_G_BUF_THRESH_SET_H_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1194h

Figure 7-85. CPSW_P0_TX_G_BUF_THRESH_SET_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-174. CPSW_P0_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

7.2.51 CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 00021198h) [reset = X]

CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG is shown in Figure 7-86 and described in Table 7-176.

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Global Buffer Threshold Clr Low

Table 7-175.
CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1198h

Figure 7-86. CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-176. CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

7.2.52 CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 0002119Ch) [reset = X]

CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG is shown in [Figure 7-87](#) and described in [Table 7-178](#).

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CPPI Port 0 Tx PFC Global Buffer Threshold Clr High

Table 7-177.
CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 119Ch

Figure 7-87. CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-178. CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

7.2.53 CPSW_P0_SRC_ID_A_REG Register (Offset = 00021300h) [reset = 04030201h]

CPSW_P0_SRC_ID_A_REG is shown in [Figure 7-88](#) and described in [Table 7-180](#).

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CPPI Port 0 CPPI Source ID A

Table 7-179. CPSW_P0_SRC_ID_A_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1300h

Figure 7-88. CPSW_P0_SRC_ID_A_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PORT1															
R-0h																R/W-1h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-180. CPSW_P0_SRC_ID_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved.
7-0	PORT1	R/W	1h	Port 1 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 1.

7.2.54 CPSW_P0_HOST_BLKs_PRI_REG Register (Offset = 00021320h) [reset = 0h]

CPSW_P0_HOST_BLKs_PRI_REG is shown in [Figure 7-89](#) and described in [Table 7-182](#).

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CPPI Port 0 Host Blocks Priority

**Table 7-181. CPSW_P0_HOST_BLKs_PRI_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 1320h

Figure 7-89. CPSW_P0_HOST_BLKs_PRI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-182. CPSW_P0_HOST_BLKs_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Host Blocks Per Priority 7
27-24	PRI6	R/W	0h	Host Blocks Per Priority 6
23-20	PRI5	R/W	0h	Host Blocks Per Priority 5
19-16	PRI4	R/W	0h	Host Blocks Per Priority 4
15-12	PRI3	R/W	0h	Host Blocks Per Priority 3
11-8	PRI2	R/W	0h	Host Blocks Per Priority 2
7-4	PRI1	R/W	0h	Host Blocks Per Priority 1
3-0	PRI0	R/W	0h	Host Blocks Per Priority 0

7.2.55 CPSW_PN_RESERVED_REG Register (Offset = 00022000h) [reset = 0h]

CPSW_PN_RESERVED_REG is shown in [Figure 7-90](#) and described in [Table 7-184](#).

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Reserved

Table 7-183. CPSW_PN_RESERVED_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2000h

Figure 7-90. CPSW_PN_RESERVED_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 7-184. CPSW_PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved register for memory map alignment

7.2.56 CPSW_PN_CONTROL_REG Register (Offset = 00022004h) [reset = X]

CPSW_PN_CONTROL_REG is shown in [Figure 7-91](#) and described in [Table 7-186](#).

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Enet Port N Control

Table 7-185. CPSW_PN_CONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2004h

Figure 7-91. CPSW_PN_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						EST_PORT_EN	IET_PORT_EN
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED	TX_LPI_CLKST_OP_EN	RESERVED			
R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-X			
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
R/W-X					R/W-0h	R/W-0h	R/W-X

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-186. CPSW_PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	EST_PORT_EN	R/W	0h	EST Port Enable. 0h = EST is disabled on the port 1h = EST is enabled on the port – Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
16	IET_PORT_EN	R/W	0h	Interspersed Express Traffic (IET) Port Enable. 0h = IET is disabled on the port 1h = IET is enabled on the port – Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
15	RX_ECC_ERR_EN	R/W	0h	Port N receive ECC Error Enable This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port N transmit ECC Error Enable This bit must be set to enable transmit ECC error operations
13	RESERVED	R/W	X	
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable. When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11-3	RESERVED	R/W	X	

Table 7-186. CPSW_PN_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DSCP_IPV6_EN	R/W	0h	IPV6 DSCP enable 0h = IPV6 DSCP priority mapping is disabled 1h = IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	IPV4 DSCP enable 0h = IPV4 DSCP priority mapping is disabled 1h = IPV4 DSCP priority mapping is enabled
0	RESERVED	R/W	X	

7.2.57 CPSW_PN_MAX_BLKs_REG Register (Offset = 00022008h) [reset = X]

CPSW_PN_MAX_BLKs_REG is shown in [Figure 7-92](#) and described in [Table 7-188](#).

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Enet Port N FIFO Max Blocks

Table 7-187. CPSW_PN_MAX_BLKs_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2008h

Figure 7-92. CPSW_PN_MAX_BLKs_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MAX_BLKs								RX_MAX_BLKs							
R/W-10h								R/W-4h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-188. CPSW_PN_MAX_BLKs_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	TX_MAX_BLKs	R/W	10h	Transmit Max Blocks. The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive when Fullduplex (CPSW_PN_MAC_CONTROL_REG[0] FULLDUPLEX = 1h) flow control is enabled to allow for flow control runout.
7-0	RX_MAX_BLKs	R/W	4h	Receive Max Blocks. The maximum number of blocks allowed on the express and preempt receive FIFOs (transmit and receive FIFO's combined when fifo_oneram = 1)

7.2.58 CPSW_PN_BLK_CNT_REG Register (Offset = 00022010h) [reset = X]

CPSW_PN_BLK_CNT_REG is shown in [Figure 7-93](#) and described in [Table 7-190](#).

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Enet Port N FIFO Block Usage Count

Table 7-189. CPSW_PN_BLK_CNT_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2010h

Figure 7-93. CPSW_PN_BLK_CNT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED		RX_BLK_CNT_P					
R-X		R-0h					
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
R-X			R-0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT_E					
R-X		R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 7-190. CPSW_PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	X	
21-16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO preempt receive queue. No blocks are allocated until the CPSW_CONTROL_REG[17] IET_ENABLE is set.
15-13	RESERVED	R	X	
12-8	TX_BLK_CNT	R	0h	Transmit Block Count Usage. This value is the number of blocks allocated to the port's FIFO logical transmit queues.
7-6	RESERVED	R	X	
5-0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO express receive queue.

7.2.59 CPSW_PN_PORT_VLAN_REG Register (Offset = 00022014h) [reset = X]

CPSW_PN_PORT_VLAN_REG is shown in [Figure 7-94](#) and described in [Table 7-192](#).

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Enet Port N VLAN

**Table 7-191. CPSW_PN_PORT_VLAN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2014h

Figure 7-94. CPSW_PN_PORT_VLAN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W-0h			R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-192. CPSW_PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11-0	PORT_VID	R/W	0h	Port VLAN ID

7.2.60 CPSW_PN_TX_PRI_MAP_REG Register (Offset = 00022018h) [reset = X]

CPSW_PN_TX_PRI_MAP_REG is shown in Figure 7-95 and described in Table 7-194.

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Enet Port N Tx Header Pri to Switch Pri Mapping

Table 7-193. CPSW_PN_TX_PRI_MAP_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2018h

Figure 7-95. CPSW_PN_TX_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
R/W-X	R/W-7h			R/W-X	R/W-6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
R/W-X	R/W-5h			R/W-X	R/W-4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
R/W-X	R/W-3h			R/W-X	R/W-2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
R/W-X	R/W-1h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-194. CPSW_PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	R/W	X	
26-24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	R/W	X	
22-20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	R/W	X	
18-16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	R/W	X	
14-12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	R/W	X	
10-8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	R/W	X	
6-4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.

Table 7-194. CPSW_PN_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

7.2.61 CPSW_PN_PRI_CTL_REG Register (Offset = 0002201Ch) [reset = X]

CPSW_PN_PRI_CTL_REG is shown in [Figure 7-96](#) and described in [Table 7-196](#).

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Enet Port N Priority Control

Table 7-195. CPSW_PN_PRI_CTL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 201Ch

Figure 7-96. CPSW_PN_PRI_CTL_REG Register

31	30	29	28	27	26	25	24
TX_FLOW_PRI							
R/W-0h							
23	22	21	20	19	18	17	16
RX_FLOW_PRI							
R/W-0h							
15	14	13	12	11	10	9	8
TX_HOST_BLKs_REM				RESERVED			
R/W-9h				R/W-X			
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-196. CPSW_PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23-16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15-12	TX_HOST_BLKs_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11-0	RESERVED	R/W	X	

7.2.62 CPSW_PN_RX_PRI_MAP_REG Register (Offset = 00022020h) [reset = X]

CPSW_PN_RX_PRI_MAP_REG is shown in [Figure 7-97](#) and described in [Table 7-198](#).

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Enet Port N RX Pkt Pri to Header Pri Map

**Table 7-197. CPSW_PN_RX_PRI_MAP_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2020h

Figure 7-97. CPSW_PN_RX_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED		PRI7		RESERVED		PRI6	
R/W-X		R/W-7h		R/W-X		R/W-6h	
23	22	21	20	19	18	17	16
RESERVED		PRI5		RESERVED		PRI4	
R/W-X		R/W-5h		R/W-X		R/W-4h	
15	14	13	12	11	10	9	8
RESERVED		PRI3		RESERVED		PRI2	
R/W-X		R/W-3h		R/W-X		R/W-2h	
7	6	5	4	3	2	1	0
RESERVED		PRI1		RESERVED		PRI0	
R/W-X		R/W-1h		R/W-X		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-198. CPSW_PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	R/W	X	
26-24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	R/W	X	
22-20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	R/W	X	
18-16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	R/W	X	
14-12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	R/W	X	
10-8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	R/W	X	
6-4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.

Table 7-198. CPSW_PN_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

7.2.63 CPSW_PN_RX_MAXLEN_REG Register (Offset = 00022024h) [reset = X]

CPSW_PN_RX_MAXLEN_REG is shown in [Figure 7-98](#) and described in [Table 7-200](#).

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Enet Port N Receive Frame Max Length

**Table 7-199. CPSW_PN_RX_MAXLEN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2024h

Figure 7-98. CPSW_PN_RX_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		RX_MAXLEN													
R/W-X																		R/W-5EEh													

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-200. CPSW_PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_MAXLEN	R/W	5EEh	<p>RX Maximum Frame Length.</p> <p>This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_PN_RX_MAXLEN_REG[13-0] RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).</p>

7.2.64 CPSW_PN_TX_BLKs_PRI_REG Register (Offset = 00022028h) [reset = 01245678h]

CPSW_PN_TX_BLKs_PRI_REG is shown in [Figure 7-99](#) and described in [Table 7-202](#).

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Enet Port N Transmit Block Sub Per Priority

**Table 7-201. CPSW_PN_TX_BLKs_PRI_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2028h

Figure 7-99. CPSW_PN_TX_BLKs_PRI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-1h				R/W-2h				R/W-4h				R/W-5h				R/W-6h				R/W-7h				R/W-8h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-202. CPSW_PN_TX_BLKs_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Transmit Blocks Per Priority (subtract value) 7
27-24	PRI6	R/W	1h	Transmit Blocks Per Priority (subtract value) 6
23-20	PRI5	R/W	2h	Transmit Blocks Per Priority (subtract value) 5
19-16	PRI4	R/W	4h	Transmit Blocks Per Priority (subtract value) 4
15-12	PRI3	R/W	5h	Transmit Blocks Per Priority (subtract value) 3
11-8	PRI2	R/W	6h	Transmit Blocks Per Priority (subtract value) 2
7-4	PRI1	R/W	7h	Transmit Blocks Per Priority (subtract value) 1
3-0	PRI0	R/W	8h	Transmit Blocks Per Priority (subtract value) 0

7.2.65 CPSW_PN_RX_FLOW_THRESH_REG Register (Offset = 0002202Ch) [reset = X]

CPSW_PN_RX_FLOW_THRESH_REG is shown in [Figure 7-100](#) and described in [Table 7-204](#).

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Enet MAC Receive Flow Threshold in Receive Buffer Words

Table 7-203. CPSW_PN_RX_FLOW_THRESH_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 202Ch

Figure 7-100. CPSW_PN_RX_FLOW_THRESH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								COUNT							
R/W-X																								R/W-40h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-204. CPSW_PN_RX_FLOW_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	COUNT	R/W	40h	Receive Flow Control Threshold in Words. This register contains the receive flow control threshold value. Receive flow control will be triggered (when enabled) when there are 32-byte words in the receive fifo. This register is only present when N=2.

7.2.66 CPSW_PN_IDLE2LPI_REG Register (Offset = 00022030h) [reset = X]

CPSW_PN_IDLE2LPI_REG is shown in [Figure 7-101](#) and described in [Table 7-206](#).

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Enet Port N EEE Idle to LPI counter

Table 7-205. CPSW_PN_IDLE2LPI_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2030h

Figure 7-101. CPSW_PN_IDLE2LPI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-206. CPSW_PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	COUNT	R/W	0h	EEE Idle to LPI counter load value.

7.2.67 CPSW_PN_LPI2WAKE_REG Register (Offset = 00022034h) [reset = X]

CPSW_PN_LPI2WAKE_REG is shown in [Figure 7-102](#) and described in [Table 7-208](#).

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Enet Port N EEE LPI to wake counter

Table 7-207. CPSW_PN_LPI2WAKE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2034h

Figure 7-102. CPSW_PN_LPI2WAKE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-208. CPSW_PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	COUNT	R/W	0h	EEE LPI to wake counter load value.

7.2.68 CPSW_PN_EEE_STATUS_REG Register (Offset = 00022038h) [reset = X]

CPSW_PN_EEE_STATUS_REG is shown in [Figure 7-103](#) and described in [Table 7-210](#).

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Enet Port N EEE status

Table 7-209. CPSW_PN_EEE_STATUS_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2038h

Figure 7-103. CPSW_PN_EEE_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
R-X	R-1h	R-1h	R-0h	R-0h	R-0h	R-1h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-210. CPSW_PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	X	
6	TX_FIFO_EMPTY	R	1h	Port N Transmit FIFO packet count zero. This bit is set when there are no packets in the transmit FIFO.
5	RX_FIFO_EMPTY	R	1h	Port N Receive FIFO packet count zero. This bit is set when there are no packets in the receive FIFO.
4	TX_FIFO_HOLD	R	0h	Port N Transmit FIFO hold. This bit is set during LPI and Wake time.
3	TX_WAKE	R	0h	Port N Receive Wake Time. This bit is set when the IDLE to Wake time is being counted.
2	TX_LPI	R	0h	Port N Transmit LPI. This bit is set when the Ethernet transmit is in the LPI state.
1	RX_LPI	R	1h	Port N Receive LPI. This bit is set when the Ethernet receive is in the LPI state. The LPI state is indicated after reset because the port is disabled (CPSW_PN_MAC_CONTROL_REG [5] GMII_EN = 0h).
0	WAIT_IDLE2LPI	R	0h	Transmit Wait Idle to LPI. This bit is set when the port is counting the IDLE to LPI time.

7.2.69 CPSW_PN_IET_CONTROL_REG Register (Offset = 00022040h) [reset = 8h]

CPSW_PN_IET_CONTROL_REG is shown in [Figure 7-104](#) and described in [Table 7-212](#).

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Enet Port N IET Control

**Table 7-211. CPSW_PN_IET_CONTROL_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2040h

Figure 7-104. CPSW_PN_IET_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
MAC_PREMPT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				MAC_ADDFRAGSIZE			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				MAC_LINKFAIL	MAC_DISABLE VERIFY	MAC_HOLD	MAC_PENABL E
R/W-0h				R/W-1h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-212. CPSW_PN_IET_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	Reserved
23-16	MAC_PREMPT	R/W	0h	Mac Preempt Queue – Indicates which transmit FIFO queues are sent to the preempt MAC. Bit 0 indicates queue zero, bit 1 queue 1 and so on. Packets will be sent to the preempt MAC only when MAC_PENABLE is set, and when MAC_VERIFIED (from CPSW_PN_IET_STATUS_REG) or MAC_DISABLEVERIFY is set, and when IET_PORT_EN is set.
15-11	RESERVED	R/W	0h	Reserved
10-8	MAC_ADDFRAGSIZE	R/W	0h	Mac Fragment Size – An integer in the range 0:7 indicating, as a multiple of 64, the minimum additional length for nonfinal mPackets. 0 = 64 1 = 128 2 = 192 3 = 256 4 = 320 5 = 384 6 = 448 7 = 512
7-4	RESERVED	R/W	0h	Reserved
3	MAC_LINKFAIL	R/W	1h	Mac Link Fail – Link Fail Indicator to reset the verify state machine. This bit is reset high. Verify and response frames will be sent/allowed when this bit is cleared.

Table 7-212. CPSW_PN_IET_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MAC_DISABLEVERIFY	R/W	0h	Mac Disable Verify – Disables verification on the port when set. If this bit is set then packets will be sent to the preempt Mac when MAC_PENABLE is set (This is a forced mode with no IET verification).
1	MAC_HOLD	R/W	0h	Mac Hold – Hold Preemption on the port.
0	MAC_PENABLE	R/W	0h	Mac Preemption Enable – Port Preemption Enable. This takes effect only when IET_PORT_EN is set.

7.2.70 CPSW_PN_IET_STATUS_REG Register (Offset = 00022044h) [reset = 0h]

CPSW_PN_IET_STATUS_REG is shown in [Figure 7-105](#) and described in [Table 7-214](#).

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Enet Port N IET Status

**Table 7-213. CPSW_PN_IET_STATUS_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2044h

Figure 7-105. CPSW_PN_IET_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				MAC_VERIFY_	MAC_RESPON	MAC_VERIFY_	MAC_VERIFIE
				ERR	D_ERR	FAIL	D
R-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-214. CPSW_PN_IET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MAC_VERIFY_ERR	R	0h	Mac Received Verify Packet with Errors – Set when a verify packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
2	MAC_RESPOND_ERR	R	0h	Mac Received Respond Packet with Errors – Set when a respond packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
1	MAC_VERIFY_FAIL	R	0h	Mac Verification Failed – Indication that verification was unsuccessful.
0	MAC_VERIFIED	R	0h	Mac Verified – Indication that verification was successful.

7.2.71 CPSW_PN_IET_VERIFY_REG Register (Offset = 00022048h) [reset = 1312D0h]

CPSW_PN_IET_VERIFY_REG is shown in [Figure 7-106](#) and described in [Table 7-216](#).

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Enet Port N IET VERIFY

Table 7-215. CPSW_PN_IET_VERIFY_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2048h

Figure 7-106. CPSW_PN_IET_VERIFY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAC_VERIFY_CNT																							
R/W-0h								R/W-001312D0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-216. CPSW_PN_IET_VERIFY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	Reserved
23-0	MAC_VERIFY_CNT	R/W	001312D0h	Mac Verify Timeout Count – The number of wireside clocks contained in the verify timeout counter. The default is 0x1312D0 (10ms at 125MHz in gig mode).

7.2.72 CPSW_PN_FIFO_STATUS_REG Register (Offset = 00022050h) [reset = X]

CPSW_PN_FIFO_STATUS_REG is shown in [Figure 7-107](#) and described in [Table 7-218](#).

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Enet Port N FIFO STATUS

**Table 7-217. CPSW_PN_FIFO_STATUS_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2050h

Figure 7-107. CPSW_PN_FIFO_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED					EST_BUFACT	EST_ADD_ER R	EST_CNT_ERR
R-X					R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
TX_E_MAC_ALLOW							
R-FFh							
7	6	5	4	3	2	1	0
TX_PRI_ACTIVE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 7-218. CPSW_PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	X	
18	EST_BUFACT	R	0h	EST RAM active buffer. Indicates the active 64-word fetch buffer when CPSW_PN_EST_CONTROL_REG[0] EST_ONEBUF is cleared to zero. Indicates the fetch RAM address MSB when bit [0] EST_ONEBUF is set to one.
17	EST_ADD_ERR	R	0h	EST Address Error. Indicates that the fetch RAM was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error. Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15-8	TX_E_MAC_ALLOW	R	FFh	EST transmit MAC allow. Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the preempt queue).
7-0	TX_PRI_ACTIVE	R	0h	EST Transmit Priority Active. Bus that indicates which priorities have packets (non-empty) at the time of the register read.

7.2.73 CPSW_PN_EST_CONTROL_REG Register (Offset = 00022060h) [reset = X]

CPSW_PN_EST_CONTROL_REG is shown in [Figure 7-108](#) and described in [Table 7-220](#).

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Enet Port N EST CONTROL

Table 7-219. CPSW_PN_EST_CONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2060h

Figure 7-108. CPSW_PN_EST_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED						EST_FILL_MARGIN	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
EST_FILL_MARGIN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						EST_FILL_EN	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-220. CPSW_PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin. Sets the fill margin required to ensure that the Ethernet wire is clear (including IPG) so that the timed EST express packet can egress at the required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended.
15-9	RESERVED	R/W	X	
8	EST_FILL_EN	R/W	0h	EST Fill Enable. Enable EST fill mode.
7-5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority. Selects the express priority that timestamp(s) will be generated on when CPSW_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI bit is set.
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority. When set, timestamp only enabled packets on the express priority selected by CPSW_PN_EST_CONTROL_REG[7-5] ST_TS_PRI bit field. When cleared to zero, express packet selection for timestamp is independent of priority.

Table 7-220. CPSW_PN_EST_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only. Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If CPSW_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is also set then the timestamp is generated only on the first packet on CPSW_PN_EST_CONTROL_REG[7-5] ST_TS_PRI).
2	EST_TS_EN	R/W	0h	EST Timestamp Enable. Enable express timestamps (when CPSW_CONTROL_REG[18] EST_ENABLE and CPSW_PN_CONTROL_REG[17] EST_PORT_EN bits are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select. If CPSW_PN_EST_CONTROL_REG[0] EST_ONEBUF is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the CPSW_PN_FIFO_STATUS_REG register, bit [18] EST_BUFACT.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer. When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The CPSW_PN_EST_CONTROL_REG[1] EST_BUFSEL bit selects the buffer to be used when bit [0] EST_ONEBUF is cleared to zero.

7.2.74 CPSW_PN_RX_DSCP_MAP_REG_y Register (Offset = 00022120h + formula) [reset = X]

CPSW_PN_RX_DSCP_MAP_REG_y is shown in Figure 7-109 and described in Table 7-222.

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Enet Port N Receive IPV4/IPV6 DSCP Map 0 to Map 7 Registers.

Offset = 00022120h + (y * 4h); where y = 0h to 7h

Table 7-221. CPSW_PN_RX_DSCP_MAP_REG_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2120h + formula

Figure 7-109. CPSW_PN_RX_DSCP_MAP_REG_y Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
R/W-X	R/W-0h			R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
R/W-X	R/W-0h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-222. CPSW_PN_RX_DSCP_MAP_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	R/W	X	
26-24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	R/W	X	
22-20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	R/W	X	
18-16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	R/W	X	
14-12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	R/W	X	
10-8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	R/W	X	

Table 7-222. CPSW_PN_RX_DSCP_MAP_REG_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

7.2.75 CPSW_PN_PRI_CIR_REG_y Register (Offset = 00022140h + formula) [reset = X]

CPSW_PN_PRI_CIR_REG_y is shown in [Figure 7-110](#) and described in [Table 7-224](#).

Return to [Summary Table](#).

Ethernet Port N Rx Priority 0 to Priority 7 Committed Information Rate Registers.

Offset = 00022140h + (y * 4h); where y = 0h to 7h

Table 7-223. CPSW_PN_PRI_CIR_REG_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2140h + formula

Figure 7-110. CPSW_PN_PRI_CIR_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRI_CIR																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-224. CPSW_PN_PRI_CIR_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PRI_CIR	R/W	0h	Priority “y” Committed Information Rate Count Value

7.2.76 CPSW_PN_PRI_EIR_REG_y Register (Offset = 00022160h + formula) [reset = X]

CPSW_PN_PRI_EIR_REG_y is shown in [Figure 7-111](#) and described in [Table 7-226](#).

Return to [Summary Table](#).

Ethernet Port N Rx Priority 0 to Priority 7 Excess Information Rate Registers

Offset = 00022160h + (y * 4h); where y = 0h to 7h

Table 7-225. CPSW_PN_PRI_EIR_REG_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2160h + formula

Figure 7-111. CPSW_PN_PRI_EIR_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI_EIR																											
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-226. CPSW_PN_PRI_EIR_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PRI_EIR	R/W	0h	Priority “y” Excess Information Rate Count Value

7.2.77 CPSW_PN_TX_D_THRESH_SET_L_REG Register (Offset = 00022180h) [reset = X]

CPSW_PN_TX_D_THRESH_SET_L_REG is shown in [Figure 7-112](#) and described in [Table 7-228](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Destination Threshold Set Low

Table 7-227.
CPSW_PN_TX_D_THRESH_SET_L_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2180h

Figure 7-112. CPSW_PN_TX_D_THRESH_SET_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-228. CPSW_PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

7.2.78 CPSW_PN_TX_D_THRESH_SET_H_REG Register (Offset = 00022184h) [reset = X]

CPSW_PN_TX_D_THRESH_SET_H_REG is shown in [Figure 7-113](#) and described in [Table 7-230](#).

[Return to Summary Table.](#)

Enet Port N Tx PFC Destination Threshold Set High

Table 7-229.
CPSW_PN_TX_D_THRESH_SET_H_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2184h

Figure 7-113. CPSW_PN_TX_D_THRESH_SET_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-230. CPSW_PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

7.2.79 CPSW_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 00022188h) [reset = X]

CPSW_PN_TX_D_THRESH_CLR_L_REG is shown in [Figure 7-114](#) and described in [Table 7-232](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Destination Threshold Clr Low

Table 7-231.
CPSW_PN_TX_D_THRESH_CLR_L_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2188h

Figure 7-114. CPSW_PN_TX_D_THRESH_CLR_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-232. CPSW_PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

7.2.80 CPSW_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 0002218Ch) [reset = X]

CPSW_PN_TX_D_THRESH_CLR_H_REG is shown in [Figure 7-115](#) and described in [Table 7-234](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Destination Threshold Clr High

Table 7-233.
CPSW_PN_TX_D_THRESH_CLR_H_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 218Ch

Figure 7-115. CPSW_PN_TX_D_THRESH_CLR_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-234. CPSW_PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

7.2.81 CPSW_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 00022190h) [reset = X]

CPSW_PN_TX_G_BUF_THRESH_SET_L_REG is shown in [Figure 7-116](#) and described in [Table 7-236](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Global Buffer Threshold Set Low

Table 7-235.
CPSW_PN_TX_G_BUF_THRESH_SET_L_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2190h

Figure 7-116. CPSW_PN_TX_G_BUF_THRESH_SET_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-236. CPSW_PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

7.2.82 CPSW_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 00022194h) [reset = X]

CPSW_PN_TX_G_BUF_THRESH_SET_H_REG is shown in [Figure 7-117](#) and described in [Table 7-238](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Global Buffer Threshold Set High

Table 7-237.
CPSW_PN_TX_G_BUF_THRESH_SET_H_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2194h

Figure 7-117. CPSW_PN_TX_G_BUF_THRESH_SET_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-238. CPSW_PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

7.2.83 CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 00022198h) [reset = X]

CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG is shown in [Figure 7-118](#) and described in [Table 7-240](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Global Buffer Threshold Clr Low

Table 7-239.
CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2198h

Figure 7-118. CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-240. CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

7.2.84 CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 0002219Ch) [reset = X]

CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG is shown in [Figure 7-119](#) and described in [Table 7-242](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Global Buffer Threshold Clr High

Table 7-241.
CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 219Ch

Figure 7-119. CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-242. CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

7.2.85 CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 00022300h) [reset = X]

CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG is shown in [Figure 7-120](#) and described in [Table 7-244](#).

Return to [Summary Table](#).

Enet Port N Tx Destination Out Flow Add Values Low

Table 7-243.
CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2300h

Figure 7-120. CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-244. CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

7.2.86 CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 00022304h) [reset = X]

CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG is shown in [Figure 7-121](#) and described in [Table 7-246](#).

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Enet Port N Tx Destination Out Flow Add Values High

Table 7-245.
CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2304h

Figure 7-121. CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-246. CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

7.2.87 CPSW_PN_SA_L_REG Register (Offset = 00022308h) [reset = X]

CPSW_PN_SA_L_REG is shown in [Figure 7-122](#) and described in [Table 7-248](#).

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Enet Port N Tx Pause Frame Source Address Low

Table 7-247. CPSW_PN_SA_L_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2308h

Figure 7-122. CPSW_PN_SA_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_7_0								MACSRCADDR_15_8							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-248. CPSW_PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits (byte 0)
7-0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15-8 (byte 1)

7.2.88 CPSW_PN_SA_H_REG Register (Offset = 0002230Ch) [reset = 0h]

CPSW_PN_SA_H_REG is shown in [Figure 7-123](#) and described in [Table 7-250](#).

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Enet Port N Tx Pause Frame Source Address High

Table 7-249. CPSW_PN_SA_H_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 230Ch

Figure 7-123. CPSW_PN_SA_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACSRCADDR_23_16								MACSRCADDR_31_24							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_39_32								MACSRCADDR_47_40							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-250. CPSW_PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23-16 (byte 2)
23-16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31-24 (byte 3)
15-8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39-32 (byte 4)
7-0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47-40 (byte 5)

7.2.89 CPSW_PN_TS_CTL_REG Register (Offset = 00022310h) [reset = X]

CPSW_PN_TS_CTL_REG is shown in Figure 7-124 and described in Table 7-252.

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Enet Port N Time Sync Control

Table 7-251. CPSW_PN_TS_CTL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2310h

Figure 7-124. CPSW_PN_TS_CTL_REG Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W-0h							
23	22	21	20	19	18	17	16
TS_MSG_TYPE_EN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-252. CPSW_PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable. Each bit in this field enables the corresponding message type in receive and transmit time sync messages (bit 0 enables message type 0 etc.).
15-12	RESERVED	R/W	X	
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable.
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Sync Transmit Annex E enable.
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Sync Receive Annex E enable.
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable (transmit and receive).
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Sync Transmit Annex D enable.
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable.
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable.
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Sync Transmit Annex F enable.
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Sync Receive Annex D enable.
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable.
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable.

Table 7-252. CPSW_PN_TS_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Sync Receive Annex F Enable.

7.2.90 CPSW_PN_TS_SEQ_LTYPE_REG Register (Offset = 00022314h) [reset = X]

CPSW_PN_TS_SEQ_LTYPE_REG is shown in [Figure 7-125](#) and described in [Table 7-254](#).

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Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET)

Table 7-253. CPSW_PN_TS_SEQ_LTYPE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2314h

Figure 7-125. CPSW_PN_TS_SEQ_LTYPE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_SEQ_ID_OFFSET					
R/W-X										R/W-1Eh					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LTYPE1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-254. CPSW_PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6h.
15-0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1 This is the port's time sync LTYPE1 value.

7.2.91 CPSW_PN_TS_VLAN_LTYPE_REG Register (Offset = 00022318h) [reset = 0h]

CPSW_PN_TS_VLAN_LTYPE_REG is shown in [Figure 7-126](#) and described in [Table 7-256](#).

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Enet Port N Time Sync VLAN2 and VLAN2

**Table 7-255. CPSW_PN_TS_VLAN_LTYPE_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2318h

Figure 7-126. CPSW_PN_TS_VLAN_LTYPE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_VLAN_LTYPE2																TS_VLAN_LTYPE1															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-256. CPSW_PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2 This VLAN LTYPE value is used for the port TX and RX time sync decode.
15-0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1 This VLAN LTYPE value is used for the port TX and RX time sync decode.

7.2.92 CPSW_PN_TS_CTL_LTYPE2_REG Register (Offset = 0002231Ch) [reset = X]

CPSW_PN_TS_CTL_LTYPE2_REG is shown in [Figure 7-127](#) and described in [Table 7-258](#).

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Enet Port N Time Sync Control and LTYPE 2

Table 7-257. CPSW_PN_TS_CTL_LTYPE2_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 231Ch

Figure 7-127. CPSW_PN_TS_CTL_LTYPE2_REG Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TS_LTYPE2							
R/W-0h							
7	6	5	4	3	2	1	0
TS_LTYPE2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-258. CPSW_PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable 0h = Unicast disabled 1h = Unicast enabled
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable 0h = TTL must be 1h 1h = TTL may be any value
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable 0h = Disabled 1h = Destination port number (decimal) 320 is enabled
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable 0h = Disabled 1h = Destination port number (decimal) 319 is enabled
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.1.132 is enabled
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.1.131 is enabled

Table 7-258. CPSW_PN_TS_CTL_LTYPE2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.1.130 is enabled
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.1.129 is enabled
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.0.107 is enabled
15-0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2 This is the time sync LTYPE1 value for port 1.

7.2.93 CPSW_PN_TS_CTL2_REG Register (Offset = 00022320h) [reset = X]

CPSW_PN_TS_CTL2_REG is shown in [Figure 7-128](#) and described in [Table 7-260](#).

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Enet Port N Time Sync Control 2

Table 7-259. CPSW_PN_TS_CTL2_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2320h

Figure 7-128. CPSW_PN_TS_CTL2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_DOMAIN_OFFSET					
R/W-X										R/W-4h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_MCAST_TYPE_EN															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-260. CPSW_PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset.
15-0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable.

7.2.94 CPSW_PN_MAC_CONTROL_REG Register (Offset = 00022330h) [reset = X]

CPSW_PN_MAC_CONTROL_REG is shown in [Figure 7-129](#) and described in [Table 7-262](#).

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Enet Port N Mac Control

**Table 7-261. CPSW_PN_MAC_CONTROL_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2330h

Figure 7-129. CPSW_PN_MAC_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							RX_CMF_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RX_CSF_EN	RX_CEF_EN	TX_SHORT_G AP_LIM_EN	EXT_TX_FLOW _EN	EXT_RX_FLO W_EN	CTL_EN	GIG_FORCE	IFCTL_B
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_G AP_ENABLE	RESERVED	
R/W-0h	R/W-X		R/W-0h	R/W-0h	R/W-0h	R/W-X	
7	6	5	4	3	2	1	0
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-262. CPSW_PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the CPSW_PN_MAC_CONTROL_REG register, regardless of the value of [24] RX_CMF_EN bit. Frames transferred to memory due to [24] RX_CMF_EN will have the control bit set in their EOP buffer descriptor. 0h = MAC control frames are filtered (but acted upon if enabled). 1h = MAC control frames are transferred to memory.
23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable. Enables frames or fragments shorter than 64 bytes to be copied to memory. Frames transferred to memory due to CPSW_PN_MAC_CONTROL_REG [23] RX_CSF_EN will have the fragment or undersized bit set in their receive footer. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors. 0h = Short frames are filtered. 1h = Short frames are transferred to memory.

Table 7-262. CPSW_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable. Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when CPSW_PN_MAC_CONTROL_REG[22] RX_CEF_EN is not set. 0h = Frames containing errors are filtered. 1h = Frames containing errors are transferred to memory.
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable When set this bit limits the number of short gap packets transmitted to 100ppm. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable. Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the [4] TX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG register.
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable. Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the CPSW_PN_MAC_CONTROL_REG[3] RX_FLOW_EN bit in this register.
18	CTL_EN	R/W	0h	External Control Enable. Enables the full duplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the [0] FULLDUPLEX and [7] GIG bits in the CPSW_PN_MAC_CONTROL_REG register. The [0] FULLDUPLEX bit reflects the actual full duplex mode selected.
17	GIG_FORCE	R/W	0h	Gigabit Mode Force. This bit is used to force the Ethernet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.
16	IFCTL_B	R/W	0h	Interface Control B - Not used.
15	IFCTL_A	R/W	0h	Interface Control A - Determines the RMII link speed 0h = 10Mbps 1h = 100Mbps
14-13	RESERVED	R/W	X	
12	CRC_TYPE	R/W	0h	Port CRC Type 0h = Ethernet CRC 1h = Castagnoli CRC
11	CMD_IDLE	R/W	0h	Command Idle 0h = Idle not commanded 1h = Idle Commanded (read bit [31] IDLE in CPSW_PN_MAC_STATUS_REG register)

Table 7-262. CPSW_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable 0h = Transmit with a short IPG is disabled 1h = Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.
9-8	RESERVED	R/W	X	
7	GIG	R/W	0h	Gigabit Mode. 0h = 10/100 mode 1h = Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit.
6	TX_PACE	R/W	0h	Transmit Pacing Enable 0h = Transmit Pacing Disabled 1h = Transmit Pacing Enabled
5	GMII_EN	R/W	0h	GMII Enable. 0h = GMII RX and TX held in reset. 1h = GMII RX and TX released from reset.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0h = Transmit Flow Control Disabled. Full-duplex mode – Incoming pause frames are not acted upon. 1h = Transmit Flow Control Enabled. Full-duplex mode – Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable. 0h = Receive Flow Control Disabled Half-duplex mode – No flow control generated collisions are sent. Full-duplex mode – No outgoing pause frames are sent. 1h = Receive Flow Control Enabled Half-duplex mode – Collisions are initiated when receive flow control is triggered. Full-duplex mode – Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode. This bit must be set to allow writes to the CPSW_PN_MAC_BOFFTEST_REG and CPSW_PN_MAC_RX_PAUSETIMER_REG registers.
1	LOOPBACK	R/W	0h	Loop Back Mode. Loopback mode forces internal full duplex mode regardless of whether the CPSW_PN_MAC_CONTROL_REG[0] FULLDUPLEX bit is set or not. The [1] LOOPBACK bit should be changed only when [5] GMII_EN is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS). 0h = Not looped back mode 1h = Loop Back mode enabled

Table 7-262. CPSW_PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FULLDUPLEX	R/W	0h	<p>Full Duplex mode.</p> <p>Gigabit mode forces fullduplex mode regardless of whether the [0] FULLDUPLEX bit is set or not.</p> <p>The FULLDUPLEX_OUT output is the value of this register bit</p> <p>0h = Half duplex mode</p> <p>1h = Full duplex mode</p>

7.2.95 CPSW_PN_MAC_STATUS_REG Register (Offset = 00022334h) [reset = X]

CPSW_PN_MAC_STATUS_REG is shown in [Figure 7-130](#) and described in [Table 7-264](#).

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Enet Port N Mac Status

**Table 7-263. CPSW_PN_MAC_STATUS_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2334h

Figure 7-130. CPSW_PN_MAC_STATUS_REG Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	P_IDLE	TX_IDLE	TORF	TORF_PRI		
R-1h	R-1h	R-1h	R-1h	R-0h	R-0h		
23	22	21	20	19	18	17	16
TX_PFC_FLOW_ACT							
R-0h							
15	14	13	12	11	10	9	8
RX_PFC_FLOW_ACT							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
R-X	R-0h	R-0h	R-0h	R-0h	R-X	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-264. CPSW_PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	Enet IDLE. The Ethernet port (express and preempt) are in the Idle state (valid after an Idle command) 0h = The port is not in the Idle state. 1h = The port is in the Idle state.
30	E_IDLE	R	1h	Express MAC is Idle.
29	P_IDLE	R	1h	Preempt MAC is Idle.
28	TX_IDLE	R	1h	Mac Transmit Idle. Both Preempt and Express MAC Transmit are in Idle state.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26-24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 7h to clear.
23-16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15-8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	R	X	
6	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG [19] EXT_RX_FLOW_EN input bit.

Table 7-264. CPSW_PN_MAC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG [20] EXT_TX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG. This is the value of the [4] EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Fullduplex. This is the value of the [3] EXT_FULLDUPLEX input bit.
2	RESERVED	R	X	
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

7.2.96 CPSW_PN_MAC_SOFT_RESET_REG Register (Offset = 00022338h) [reset = X]

CPSW_PN_MAC_SOFT_RESET_REG is shown in [Figure 7-131](#) and described in [Table 7-266](#).

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Enet Port N Mac Soft Reset

Table 7-265. CPSW_PN_MAC_SOFT_RESET_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2338h

Figure 7-131. CPSW_PN_MAC_SOFT_RESET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-266. CPSW_PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	SOFT_RESET	R/W	0h	<p>Software reset.</p> <p>Writing a 1h to this bit causes the Ethernet Mac logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a 1h is read, the reset has not yet occurred. If a 0h is read then reset has occurred.</p> <p>NOTE: If this bit is set CPSW_PN_RX_MAXLEN_REG, CPSW_PN_RX_PRI_MAP_REG, CPSW_PN_MAC_TX_GAP_REG, CPSW_PN_INTERVLAN_OPX_POINTER_REG, CPSW_PN_INTERVLAN_OPX_A_REG, CPSW_PN_INTERVLAN_OPX_B_REG, CPSW_PN_INTERVLAN_OPX_C_REG, CPSW_PN_INTERVLAN_OPX_D_REG will be reset to default value.</p>

7.2.97 CPSW_PN_MAC_BOFFTEST_REG Register (Offset = 0002233Ch) [reset = X]

CPSW_PN_MAC_BOFFTEST_REG is shown in Figure 7-132 and described in Table 7-268.

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Enet Port N Mac Backoff Test

Table 7-267. CPSW_PN_MAC_BOFFTEST_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 233Ch

Figure 7-132. CPSW_PN_MAC_BOFFTEST_REG Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
R/W-X	R/W-0h					R/W-0h	
23	22	21	20	19	18	17	16
RNDNUM							
R/W-0h							
15	14	13	12	11	10	9	8
COLL_COUNT				RESERVED		TX_BACKOFF	
R-0h				R/W-X		R-0h	
7	6	5	4	3	2	1	0
TX_BACKOFF							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 7-268. CPSW_PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-26	PACEVAL	R/W	0h	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce "capture" effects improving overall network bandwidth.
25-16	RNDNUM	R/W	0h	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when CPSW_PN_MAC_CONTROL_REG[2] MTEST bit has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15-12	COLL_COUNT	R	0h	Collision Count.
11-10	RESERVED	R/W	X	

Table 7-268. CPSW_PN_MAC_BOFFTEST_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	TX_BACKOFF	R	0h	<p>Backoff Count.</p> <p>This field allows the current value of the backoff counter to be observed for test purposes.</p> <p>This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.</p>

7.2.98 CPSW_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 00022340h) [reset = X]

CPSW_PN_MAC_RX_PAUSETIMER_REG is shown in [Figure 7-133](#) and described in [Table 7-270](#).

[Return to Summary Table.](#)

Enet Port N 802.3 Receive Pause Timer

Table 7-269.
CPSW_PN_MAC_RX_PAUSETIMER_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2340h

Figure 7-133. CPSW_PN_MAC_RX_PAUSETIMER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_PAUSETIMER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-270. CPSW_PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_PAUSETIMER	R/W	0h	<p>RX Pause Timer Value.</p> <p>This field allows the contents of the receive pause timer to be observed (and written in test mode).</p> <p>The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh).</p> <p>The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).</p>

7.2.99 CPSW_PN_MAC_RXN_PAUSETIMER_REG_y Register (Offset = 00022350h + formula) [reset = X]

CPSW_PN_MAC_RXN_PAUSETIMER_REG_y is shown in [Figure 7-134](#) and described in [Table 7-272](#).

Return to [Summary Table](#).

Ethernet Port N PFC Priority 0 to Priority 7 Rx Pause Timer Registers.

Offset = 00022350h + (y * 4h); where y = 0h to 7h

Table 7-271.
CPSW_PN_MAC_RXN_PAUSETIMER_REG_y
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2350h + formula

Figure 7-134. CPSW_PN_MAC_RXN_PAUSETIMER_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_PAUSETIMER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-272. CPSW_PN_MAC_RXN_PAUSETIMER_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_PAUSETIMER	R/W	0h	Rx "y" Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

7.2.100 CPSW_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 00022370h) [reset = X]

CPSW_PN_MAC_TX_PAUSETIMER_REG is shown in [Figure 7-135](#) and described in [Table 7-274](#).

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Enet Port N 802.3 Tx Pause Timer

Table 7-273.
CPSW_PN_MAC_TX_PAUSETIMER_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2370h

Figure 7-135. CPSW_PN_MAC_TX_PAUSETIMER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_PAUSETIMER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-274. CPSW_PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

7.2.101 CPSW_PN_MAC_TXN_PAUSETIMER_REG_y Register (Offset = 00022380h + formula) [reset = X]

CPSW_PN_MAC_TXN_PAUSETIMER_REG_y is shown in [Figure 7-136](#) and described in [Table 7-276](#).

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Ethernet Port N PFC Priority 0 to Priority 7 Tx Pause Timer Registers.

Offset = 00022380h + (y * 4h); where y = 0h to 7h

Table 7-275.
CPSW_PN_MAC_TXN_PAUSETIMER_REG_y
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 2380h + formula

Figure 7-136. CPSW_PN_MAC_TXN_PAUSETIMER_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_PAUSETIMER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-276. CPSW_PN_MAC_TXN_PAUSETIMER_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_PAUSETIMER	R/W	0h	PFC Tx "y" Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

7.2.102 CPSW_PN_MAC_EMCONTROL_REG Register (Offset = 000223A0h) [reset = X]

CPSW_PN_MAC_EMCONTROL_REG is shown in [Figure 7-137](#) and described in [Table 7-278](#).

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Enet Port N Emulation Control

Table 7-277. CPSW_PN_MAC_EMCONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 23A0h

Figure 7-137. CPSW_PN_MAC_EMCONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-278. CPSW_PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

7.2.103 CPSW_PN_MAC_TX_GAP_REG Register (Offset = 000223A4h) [reset = X]

CPSW_PN_MAC_TX_GAP_REG is shown in [Figure 7-138](#) and described in [Table 7-280](#).

[Return to Summary Table.](#)

Enet Port N Tx Inter Packet Gap

**Table 7-279. CPSW_PN_MAC_TX_GAP_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 23A4h

Figure 7-138. CPSW_PN_MAC_TX_GAP_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_GAP															
R/W-X																R/W-Ch															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-280. CPSW_PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap GMII modes – This is the default gap value and only bits [8-0] are used. This can be increased from 12 to increase the gap between packets. XGMII mode – In 10 Gigabit mode this is the short gap rate and should be changed to 5000 (1388h) to get approximately 200ppm faster when short gap is triggered and enabled.

7.2.104 CPSW_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 000223ACh) [reset = X]

CPSW_PN_INTERVLAN_OPX_POINTER_REG is shown in Figure 7-139 and described in Table 7-282.

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Enet Port N Tx Egress InterVLAN Operation Pointer

Table 7-281.
CPSW_PN_INTERVLAN_OPX_POINTER_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 23ACh

Figure 7-139. CPSW_PN_INTERVLAN_OPX_POINTER_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					INTERVLAN_OPX_POINTER		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-282. CPSW_PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	INTERVLAN_OPX_POINTER	R/W	0h	Egress InterVLAN Operation Pointer

7.2.105 CPSW_PN_INTERVLAN_OPX_A_REG Register (Offset = 000223B0h) [reset = 0h]

CPSW_PN_INTERVLAN_OPX_A_REG is shown in [Figure 7-140](#) and described in [Table 7-284](#).

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Enet Port N Tx Egress InterVLAN A

Table 7-283. CPSW_PN_INTERVLAN_OPX_A_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 23B0h

Figure 7-140. CPSW_PN_INTERVLAN_OPX_A_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERVLAN_OPX_A																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-284. CPSW_PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DA[23:16]	R/W	0h	Destination Address bits 23-16 – DA byte 4 on wire.
23-16	DA[31:24]	R/W	0h	Destination Address bits 31-24 – DA byte 3 on wire.
15-8	DA[39:32]	R/W	0h	Destination Address bits 39-32 – DA byte 2 on wire.
7-0	DA[47:40]	R/W	0h	Destination Address bits 47-40 – DA byte 1 on wire.

7.2.106 CPSW_PN_INTERVLAN_OPX_B_REG Register (Offset = 000223B4h) [reset = 0h]

CPSW_PN_INTERVLAN_OPX_B_REG is shown in [Figure 7-141](#) and described in [Table 7-286](#).

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Enet Port N Tx Egress InterVLAN B

Table 7-285. CPSW_PN_INTERVLAN_OPX_B_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 23B4h

Figure 7-141. CPSW_PN_INTERVLAN_OPX_B_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERVLAN_OPX_B																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-286. CPSW_PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SA[39:32]	R/W	0h	Source Address bits 39-32 – SA byte 2 on wire.
23-16	SA[47:40]	R/W	0h	Source Address bits 47-40 – SA byte 1 on wire.
15-8	DA[7:0]	R/W	0h	Destination Address bits 7-0 – DA byte 6 on wire.
7-0	DA[15:8]	R/W	0h	Destination Address bits 15-8 – DA byte 5 on wire.

7.2.107 CPSW_PN_INTERVLAN_OPX_C_REG Register (Offset = 000223B8h) [reset = 0h]

CPSW_PN_INTERVLAN_OPX_C_REG is shown in [Figure 7-142](#) and described in [Table 7-288](#).

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Enet Port N Tx Egress InterVLAN C

Table 7-287. CPSW_PN_INTERVLAN_OPX_C_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 23B8h

Figure 7-142. CPSW_PN_INTERVLAN_OPX_C_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERVLAN_OPX_C																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-288. CPSW_PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SA[7:0]	R/W	0h	Source Address bits 7-0 – SA byte 6 on wire.
23-16	SA[15:8]	R/W	0h	Source Address bits 15-8 – SA byte 5 on wire.
15-8	SA[23:16]	R/W	0h	Source Address bits 23-16 – SA byte 4 on wire.
7-0	SA[31:24]	R/W	0h	Source Address bits 31-24 – SA byte 3 on wire.

7.2.108 CPSW_PN_INTERVLAN_OPX_D_REG Register (Offset = 000223BCh) [reset = X]

CPSW_PN_INTERVLAN_OPX_D_REG is shown in [Figure 7-143](#) and described in [Table 7-290](#).

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Enet Port N Tx Egress InterVLAN D

Table 7-289. CPSW_PN_INTERVLAN_OPX_D_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CONTROL	4602 23BCh

Figure 7-143. CPSW_PN_INTERVLAN_OPX_D_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																INTERVLAN_OPX_D															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-290. CPSW_PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	INTERVLAN_OPX_D	R/W	0h	Egress InterVLAN D

7.3 MCU_CPSW0_CPINT Registers

Table 7-292 lists the memory-mapped registers for the MCU_CPSW0_CPINT. All register offset addresses not listed in Table 7-292 should be considered as reserved locations and the register contents should not be modified.

Table 7-291. MCU_CPSW0_CPINT Instances

Instance	Base Address
MCU_CPSW0_NUSS_CPINT	4600 0000h

Table 7-292. MCU_CPSW0_CPINT Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_CPINT Physical Address
1000h	CPSW_INT_REVISION	Revision Register	4600 1000h
1010h	CPSW_INT_EOI_REG	End of Interrupt Register	4600 1010h
1014h	CPSW_INT_INTR_VECTOR_REG	Interrupt Vector Register	4600 1014h
1100h	CPSW_INT_ENABLE_REG_OUT_PULSE_0	Enable Register 0	4600 1100h
1300h	CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0	Enable Clear Register 0	4600 1300h
1500h	CPSW_INT_STATUS_REG_OUT_PULSE_0	Status Register 0	4600 1500h
1A80h	CPSW_INT_INTR_VECTOR_REG_OUT_PULSE	Interrupt Vector for out_pulse	4600 1A80h

7.3.1 CPSW_INT_REVISION Register (Offset = 1000h) [reset = 6690A200h]

CPSW_INT_REVISION is shown in [Figure 7-144](#) and described in [Table 7-294](#).

Return to [Summary Table](#).

Revision Register

Table 7-293. CPSW_INT_REVISION Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPINT	4600 1000h

Figure 7-144. CPSW_INT_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R-1h		R-2h		R-690h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER					MAJREV			CUSTOM		MINREV					
R-14h					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 7-294. CPSW_INT_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	BU
27-16	FUNCTION	R	690h	Module ID
15-11	RTLVER	R	14h	RTL revisions
10-8	MAJREV	R	2h	Major CPSW_INT_REVISION
7-6	CUSTOM	R	0h	Custom CPSW_INT_REVISION
5-0	MINREV	R	0h	Minor CPSW_INT_REVISION

7.3.2 CPSW_INT_EOI_REG Register (Offset = 1010h) [reset = X]

CPSW_INT_EOI_REG is shown in [Figure 7-145](#) and described in [Table 7-296](#).

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End of Interrupt Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 7-295. CPSW_INT_EOI_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPINT	4600 1010h

Figure 7-145. CPSW_INT_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-296. CPSW_INT_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	EOI_VECTOR	R/W	0h	End of Interrupt Vector

7.3.3 CPSW_INT_INTR_VECTOR_REG Register (Offset = 1014h) [reset = 0h]

CPSW_INT_INTR_VECTOR_REG is shown in [Figure 7-146](#) and described in [Table 7-298](#).

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Interrupt Vector Register

Table 7-297. CPSW_INT_INTR_VECTOR_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPINT	4600 1014h

Figure 7-146. CPSW_INT_INTR_VECTOR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VECTOR																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 7-298. CPSW_INT_INTR_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INTR_VECTOR	R	0h	Interrupt Vector Register

7.3.4 CPSW_INT_ENABLE_REG_OUT_PULSE_0 Register (Offset = 1100h) [reset = X]

CPSW_INT_ENABLE_REG_OUT_PULSE_0 is shown in [Figure 7-147](#) and described in [Table 7-300](#).

Return to [Summary Table](#).

Enable Register 0

Table 7-299.
CPSW_INT_ENABLE_REG_OUT_PULSE_0
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPINT	4600 1100h

Figure 7-147. CPSW_INT_ENABLE_REG_OUT_PULSE_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA	ENABLE_OUT_PULSE_EN_MDIO_PENDA	ENABLE_OUT_PULSE_EN_EVT_PENDA
R/W-X					R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-300. CPSW_INT_ENABLE_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	ENABLE_OUT_PULSE_EN_STAT_PENDA	R/W1S	0h	Enable Set for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA	R/W1S	0h	Enable Set for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVT_PENDA	R/W1S	0h	Enable Set for out_pulse_en_evt_penda

7.3.5 CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 Register (Offset = 1300h) [reset = X]

CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 is shown in Figure 7-148 and described in Table 7-302.

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Enable Clear Register 0

Table 7-301.
CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPINT	4600 1300h

Figure 7-148. CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	ENABLE_OUT_PULSE_EN_EVT_PENDA_CLR
R/W-X					R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-302. CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	R/W1C	0h	Enable Clear for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	R/W1C	0h	Enable Clear for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVT_PENDA_CLR	R/W1C	0h	Enable Clear for out_pulse_en_evt_penda

7.3.6 CPSW_INT_STATUS_REG_OUT_PULSE_0 Register (Offset = 1500h) [reset = X]

CPSW_INT_STATUS_REG_OUT_PULSE_0 is shown in Figure 7-149 and described in Table 7-304.

Return to [Summary Table](#).

Status Register 0

Table 7-303.
CPSW_INT_STATUS_REG_OUT_PULSE_0 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPINT	4600 1500h

Figure 7-149. CPSW_INT_STATUS_REG_OUT_PULSE_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED					STATUS_OUT_PULSE_STAT_PENDA	STATUS_OUT_PULSE_MDIO_PENDA	STATUS_OUT_PULSE_EVTNT_PENDA
R-X					R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-304. CPSW_INT_STATUS_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	X	
2	STATUS_OUT_PULSE_STAT_PENDA	R	0h	Status for out_pulse_en_stat_penda
1	STATUS_OUT_PULSE_MDIO_PENDA	R	0h	Status for out_pulse_en_mdio_penda
0	STATUS_OUT_PULSE_EVTNT_PENDA	R	0h	Status for out_pulse_en_evtnt_penda

7.3.7 CPSW_INT_INTR_VECTOR_REG_OUT_PULSE Register (Offset = 1A80h) [reset = 0h]

CPSW_INT_INTR_VECTOR_REG_OUT_PULSE is shown in [Figure 7-150](#) and described in [Table 7-306](#).

Return to [Summary Table](#).

Interrupt Vector for out_pulse

Table 7-305.
CPSW_INT_INTR_VECTOR_REG_OUT_PULSE
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPINT	4600 1A80h

Figure 7-150. CPSW_INT_INTR_VECTOR_REG_OUT_PULSE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VECTOR_OUT_PULSE																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 7-306. CPSW_INT_INTR_VECTOR_REG_OUT_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INTR_VECTOR_OUT_PULSE	R	0h	Interrupt Vector

7.4 MCU_CPSW0_CPTS Registers

Table 7-308 lists the memory-mapped registers for the MCU_CPSW0_CPTS. All register offset addresses not listed in Table 7-308 should be considered as reserved locations and the register contents should not be modified.

Table 7-307. MCU_CPSW0_CPTS Instances

Instance	Base Address
MCU_CPSW0_NUSS_CPTS	4600 0000h

Table 7-308. MCU_CPSW0_CPTS Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_CPTS Physical Address
0003D000h	CPSW_CPTS_IDVER_REG	MCU_CPSW0_NUSS CPTS Identification and Version Register	4603 D000h
0003D004h	CPSW_CPTS_CONTROL_REG	Time Sync Control Register	4603 D004h
0003D008h	CPSW_CPTS_RFTCLK_SEL_REG	Reference Clock Select Register	4603 D008h
0003D00Ch	CPSW_CPTS_TS_PUSH_REG	Time Stamp Event Push Register	4603 D00Ch
0003D010h	CPSW_CPTS_TS_LOAD_VAL_REG	Time Stamp Load Low Value (lower 32-bits) Register	4603 D010h
0003D014h	CPSW_CPTS_TS_LOAD_EN_REG	Time Stamp Load Enable Register	4603 D014h
0003D018h	CPSW_CPTS_TS_COMP_VAL_REG	Time Stamp Comparison Low Value (lower 32-bits) Register	4603 D018h
0003D01Ch	CPSW_CPTS_TS_COMP_LEN_REG	Time Stamp Comparison Length Register	4603 D01Ch
0003D020h	CPSW_CPTS_INTSTAT_RAW_REG	Interrupt Status Raw Register	4603 D020h
0003D024h	CPSW_CPTS_INTSTAT_MASKED_REG	Interrupt Status Masked Register	4603 D024h
0003D028h	CPSW_CPTS_INT_ENABLE_REG	Interrupt Enable Register Register	4603 D028h
0003D02Ch	CPSW_CPTS_TS_COMP_NUDGE_REG	Time Stamp Comparison Nudge Value Register	4603 D02Ch
0003D030h	CPSW_CPTS_EVENT_POP_REG	Event Interrupt Pop Register	4603 D030h
0003D034h	CPSW_CPTS_EVENT_0_REG	Lower 32-bits of the Event Value Register	4603 D034h
0003D038h	CPSW_CPTS_EVENT_1_REG	Lower Middle 32-bits of the Event Value Register	4603 D038h
0003D03Ch	CPSW_CPTS_EVENT_2_REG	Upper Middle 32-bits of the Event Value Register	4603 D03Ch
0003D040h	CPSW_CPTS_EVENT_3_REG	Upper 32-bits of the Event Value Register	4603 D040h
0003D044h	CPSW_CPTS_TS_LOAD_HIGH_VAL_REG	Time Stamp Load High Value (upper 32-bits) Register	4603 D044h
0003D048h	CPSW_CPTS_TS_COMP_HIGH_VAL_REG	Time Stamp Comparison High Value (upper 32-bits) Register	4603 D048h
0003D04Ch	CPSW_CPTS_TS_ADD_VAL_REG	Time Stamp Add Value Register	4603 D04Ch
0003D050h	CPSW_CPTS_TS_PPM_LOW_VAL_REG	Time Stamp PPM Load Low Value (lower 32-bits) Register	4603 D050h
0003D054h	CPSW_CPTS_TS_PPM_HIGH_VAL_REG	Time Stamp PPM Load High Value (upper 32-bits) Register	4603 D054h
0003D058h	CPSW_CPTS_TS_NUDGE_VAL_REG	Time Stamp Nudge Value Register	4603 D058h
0003D0E0h	CPSW_GENF0_COMP_LOW_REG_L	GENF0 time stamp Comparison Value Lower 32-bits Registers	4603 D0E0h
0003D0E4h	CPSW_GENF0_COMP_HIGH_REG_L	GENF0 time stamp Comparison Value Upper 32-bits Registers	4603 D0E4h
0003D0E8h	CPSW_GENF0_TS_GENF_CONTROL_REG	GENF0 Control Register Registers	4603 D0E8h
0003D0ECh	CPSW_GENF0_LENGTH_REG_L	GENF0 Length Value Registers	4603 D0ECh
0003D0F0h	CPSW_GENF0_PPM_LOW_REG_L	GENF0 PPM Value Lower 32-bits Registers	4603 D0F0h
0003D0F4h	CPSW_GENF0_PPM_HIGH_REG_L	GENF0 PPM Value Upper 32-bits Registers	4603 D0F4h

Table 7-308. MCU_CPSW0_CPTS Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_NUS S_CPTS Physical Address
0003D0F8h	CPSW_GENF0_NUDGE_REG_L	GENF0 Nudge Value Registers	4603 D0F8h
0003D100h	CPSW_GENF1_COMP_LOW_REG	GENF1 time stamp Comparison Value Lower 32-bits Register	4603 D100h
0003D104h	CPSW_GENF1_COMP_HIGH_REG	GENF1 time stamp Comparison Value Upper 32-bits Register	4603 D104h
0003D108h	CPSW_GENF1_CONTROL_REG	GENF1 Control Register	4603 D108h
0003D10Ch	CPSW_GENF1_LENGTH_REG	GENF1 Length Value Register	4603 D10Ch
0003D110h	CPSW_GENF1_PPM_LOW_REG	GENF1 PPM Value Lower 32-bits Register	4603 D110h
0003D114h	CPSW_GENF1_PPM_HIGH_REG	GENF1 PPM Value Upper 32-bits Register	4603 D114h
0003D118h	CPSW_GENF1_NUDGE_REG	GENF1 Nudge Value Register	4603 D118h
0003D200h	CPSW_ESTF1_COMP_LOW_REG	ESTF1 time stamp Comparison Value Lower 32-bits Register	4603 D200h
0003D204h	CPSW_ESTF1_COMP_HIGH_REG	ESTF1 time stamp Comparison Value Upper 32-bits Register	4603 D204h
0003D208h	CPSW_ESTF1_CONTROL_REG	ESTF1 Control Register	4603 D208h
0003D20Ch	CPSW_ESTF1_LENGTH_REG	ESTF1 Length Value Register	4603 D20Ch
0003D210h	CPSW_ESTF1_PPM_LOW_REG	ESTF1 PPM Value Lower 32-bits Register	4603 D210h
0003D214h	CPSW_ESTF1_PPM_HIGH_REG	ESTF1 PPM Value Upper 32-bits Register	4603 D214h
0003D218h	CPSW_ESTF1_NUDGE_REG	ESTF1 Nudge Value Register	4603 D218h

7.4.1 CPSW_CPTS_IDVER_REG Register (Offset = 0003D000h) [reset = 4E8A010Ah]

CPSW_CPTS_IDVER_REG is shown in Figure 7-151 and described in Table 7-310.

Return to [Summary Table](#).

MCU_CPSW0_NUSS CPTS Identification and Version Register

Table 7-309. CPSW_CPTS_IDVER_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D000h

Figure 7-151. CPSW_CPTS_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R-4E8Ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER				MAJOR_VER				MINOR_VER							
R-0h				R-1h				R-Ah							

LEGEND: R = Read Only; -n = value after reset

Table 7-310. CPSW_CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_IDENT	R	4E8Ah	TX Identification Value
15-11	RTL_VER	R	0h	RTL version value
10-8	MAJOR_VER	R	1h	Major Version Value
7-0	MINOR_VER	R	Ah	Minor Version Value

7.4.2 CPSW_CPTS_CONTROL_REG Register (Offset = 0003D004h) [reset = X]

CPSW_CPTS_CONTROL_REG is shown in Figure 7-152 and described in Table 7-312.

Return to [Summary Table](#).

Time Sync Control Register

**Table 7-311. CPSW_CPTS_CONTROL_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D004h

Figure 7-152. CPSW_CPTS_CONTROL_REG Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED						TX_GENF_CLR_EN	TS_RX_NO_EVENT
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
HW8_TS_PUS H_EN	HW7_TS_PUS H_EN	HW6_TS_PUS H_EN	HW5_TS_PUS H_EN	HW4_TS_PUS H_EN	HW3_TS_PUS H_EN	HW2_TS_PUS H_EN	HW1_TS_PUS H_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TS_PPM_DIR	TS_COMP_TO G	MODE	SEQUENCE_E N	TSTAMP_EN	TS_COMP_PO LARITY	INT_TEST	CPTS_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-312. CPSW_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TS_SYNC_SEL	R/W	0h	TS_SYNC output time stamp counter bit select 0h = TS_SYNC disabled 1h to Fh = TS_SYNC is time stamp counter bits 31 (Fh) down to 17 (1h)
27-18	RESERVED	R/W	0h	
17	TX_GENF_CLR_EN	R/W	0h	GENF (and ESTF) Clear Enable. 0h = A CPTS_GENFn output is not cleared when the associated CPSW_GENF0_LENGTH_REG/ CPSW_GENF1_LENGTH_REG[31:0] is cleared to zero. 1h = A CPTS_GENFn output is cleared when the associated CPSW_GENF0_LENGTH_REG/ CPSW_GENF1_LENGTH_REG[31:0] is cleared to zero.
16	TS_RX_NO_EVENT	R/W	0h	Timestamp Ethernet Receive produces no events. 0h = Ethernet receive TimeSync events enabled 1h = Ethernet receive TimeSync events disabled
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable

Table 7-312. CPSW_CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable
7	TS_PPM_DIR	R/W	0h	PPM Correction Direction 0h = Increase the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG) by the PPM value 1h = Decrease the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG and) by the PPM value
6	TS_COMP_TOG	R/W	0h	Time stamp Compare Toggle mode 0h = TS_COMP is in non-toggle mode 1h = TS_COMP is in toggle mode
5	MODE	R/W	0h	64-Bit Mode. 0h = The time stamp is 32-bits with the upper 32-bits forced to zero. 1h = The time stamp is 64-bits.
4	SEQUENCE_EN	R/W	0h	Sequence Enable. 0h = The time stamp value increments with the selected RFTCLK 1h = The time stamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc).
3	TSTAMP_EN	R/W	0h	Host Receive time stamp Enable 0h = Time stamps are disabled on received packets to host 1h = Time stamps enabled on received packets to host (PCIE_CPTS_CONTROL_REG[0] CPTS_EN must be set)
2	TS_COMP_POLARITY	R/W	1h	TS_COMP Polarity 0h = TS_COMP is asserted low 1h = TS_COMP is asserted high
1	INT_TEST	R/W	0h	Interrupt Test. When set, this bit allows the raw interrupt to be written to facilitate interrupt test.
0	CPTS_EN	R/W	0h	Time Sync Enable. When disabled (cleared to zero), the RCLK domain is held in reset.

7.4.3 CPSW_CPTS_RFTCLK_SEL_REG Register (Offset = 0003D008h) [reset = X]

CPSW_CPTS_RFTCLK_SEL_REG is shown in [Figure 7-153](#) and described in [Table 7-314](#).

Return to [Summary Table](#).

RFTCLK Select Register

Table 7-313. CPSW_CPTS_RFTCLK_SEL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D008h

Figure 7-153. CPSW_CPTS_RFTCLK_SEL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											RFTCLK_SEL				
R/W-X											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-314. CPSW_CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	RFTCLK_SEL	R/W	0h	<p>Reference clock select.</p> <p>This bit field is used to control an external multiplexer that selects one out of 8 clocks for time sync reference.</p> <p>0h = Selects CPSWHSDIV_CLKOUT2 clock</p> <p>1h = Selects MAINHSDIV_CLKOUT3 clock</p> <p>2h = Selects MCU_CPTS0_RFT_CLK I/O pin</p> <p>3h = Selects CPTS0_RFT_CLK I/O pin</p> <p>4h = Selects MCU_EXT_REFCLK0 I/O pin</p> <p>5h = Selects EXT_REFCLK1 I/O pin</p> <p>6h = Selects PCIE0_TXIO_CLK clock</p> <p>7h = Selects PCIE1_TXIO_CLK clock</p> <p>The RFTCLK_SEL value can be written only when the [0] CPTS_EN and [3] TSTAMP_EN bits are cleared to zero in the CPSW_CPTS_CONTROL_REG register.</p>

7.4.4 CPSW_CPTS_TS_PUSH_REG Register (Offset = 0003D00Ch) [reset = X]

CPSW_CPTS_TS_PUSH_REG is shown in [Figure 7-154](#) and described in [Table 7-316](#).

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Time Stamp Event Push Register

**Table 7-315. CPSW_CPTS_TS_PUSH_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D00Ch

Figure 7-154. CPSW_CPTS_TS_PUSH_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 7-316. CPSW_CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_PUSH	W	0h	Time stamp event push. When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads zero.

7.4.5 CPSW_CPTS_TS_LOAD_VAL_REG Register (Offset = 0003D010h) [reset = 0h]

CPSW_CPTS_TS_LOAD_VAL_REG is shown in [Figure 7-155](#) and described in [Table 7-318](#).

Return to [Summary Table](#).

Time Stamp Load Low Value Register

Table 7-317. CPSW_CPTS_TS_LOAD_VAL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D010h

Figure 7-155. CPSW_CPTS_TS_LOAD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-318. CPSW_CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	Time stamp load low value

7.4.6 CPSW_CPTS_TS_LOAD_EN_REG Register (Offset = 0003D014h) [reset = X]

CPSW_CPTS_TS_LOAD_EN_REG is shown in [Figure 7-156](#) and described in [Table 7-320](#).

Return to [Summary Table](#).

Time Stamp Load Enable Register

**Table 7-319. CPSW_CPTS_TS_LOAD_EN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D014h

Figure 7-156. CPSW_CPTS_TS_LOAD_EN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 7-320. CPSW_CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_LOAD_EN	W	0h	Time Stamp Load Enable. Writing a one to this bit enables the time stamp value to be written with the value in CPSW_CPTS_TS_LOAD_VAL_REG / CPSW_CPTS_TS_LOAD_HIGH_VAL_REG . This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the time stamp (CPSW_CPTS_TS_LOAD_HIGH_VAL_REG) are forced to zero in 32-bit mode.

7.4.7 CPSW_CPTS_TS_COMP_VAL_REG Register (Offset = 0003D018h) [reset = 0h]

[CPSW_CPTS_TS_COMP_VAL_REG](#) is shown in [Figure 7-157](#) and described in [Table 7-322](#).

Return to [Summary Table](#).

Time Stamp Comparison Low Value (lower 32-bits) Register.

Table 7-321. CPSW_CPTS_TS_COMP_VAL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D018h

Figure 7-157. CPSW_CPTS_TS_COMP_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-322. CPSW_CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_VAL	R/W	0h	Time Stamp Comparison Low Value. Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG [31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG [31-0] TS_COMP_VAL.

7.4.8 CPSW_CPTS_TS_COMP_LEN_REG Register (Offset = 0003D01Ch) [reset = 0h]

CPSW_CPTS_TS_COMP_LEN_REG is shown in [Figure 7-158](#) and described in [Table 7-324](#).

Return to [Summary Table](#).

Time Stamp Comparison Length Register.

**Table 7-323. CPSW_CPTS_TS_COMP_LEN_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D01Ch

Figure 7-158. CPSW_CPTS_TS_COMP_LEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-324. CPSW_CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_LENGTH	R/W	0h	Time Stamp Comparison Length. Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the CPSW_GENF0_COMP_LOW_REG_L[31-0] COMP_LOW and CPSW_GENF0_COMP_HIGH_REG_L[31-0] COMP_HIGH registers are written.

7.4.9 CPSW_CPTS_INTSTAT_RAW_REG Register (Offset = 0003D020h) [reset = X]

CPSW_CPTS_INTSTAT_RAW_REG is shown in [Figure 7-159](#) and described in [Table 7-326](#).

Return to [Summary Table](#).

Interrupt Status Register Raw

Table 7-325. CPSW_CPTS_INTSTAT_RAW_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D020h

Figure 7-159. CPSW_CPTS_INTSTAT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_RAW
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-326. CPSW_CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable). Writable when CPSW_CPTS_CONTROL_REG [1] INT_TEST = 1h A one in this bit indicates that there are one or more events in the event FIFO.

7.4.10 CPSW_CPTS_INTSTAT_MASKED_REG Register (Offset = 0003D024h) [reset = X]

CPSW_CPTS_INTSTAT_MASKED_REG is shown in [Figure 7-160](#) and described in [Table 7-328](#).

Return to [Summary Table](#).

Interrupt Status Register Masked

**Table 7-327. CPSW_CPTS_INTSTAT_MASKED_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D024h

Figure 7-160. CPSW_CPTS_INTSTAT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-328. CPSW_CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable).

7.4.11 CPSW_CPTS_INT_ENABLE_REG Register (Offset = 0003D028h) [reset = X]

CPSW_CPTS_INT_ENABLE_REG is shown in [Figure 7-161](#) and described in [Table 7-330](#).

Return to [Summary Table](#).

Interrupt Enable Register

**Table 7-329. CPSW_CPTS_INT_ENABLE_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D028h

Figure 7-161. CPSW_CPTS_INT_ENABLE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-330. CPSW_CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable.

7.4.12 CPSW_CPTS_TS_COMP_NUDGE_REG Register (Offset = 0003D02Ch) [reset = X]

CPSW_CPTS_TS_COMP_NUDGE_REG is shown in [Figure 7-162](#) and described in [Table 7-332](#).

Return to [Summary Table](#).

Time Stamp Comparison Nudge Value Register.

**Table 7-331. CPSW_CPTS_TS_COMP_NUDGE_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D02Ch

Figure 7-162. CPSW_CPTS_TS_COMP_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-332. CPSW_CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time stamp Comparison Nudge Value. This two's complement number is added to the CPSW_CPTS_TS_COMP_LEN_REG [31-0] TS_COMP_LENGTH value to increase or decrease the TS_COMP length by the CPSW_CPTS_TS_COMP_NUDGE_REG [7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_CPTS_TS_COMP_NUDGE_REG value is cleared to zero when the nudge has occurred.

7.4.13 CPSW_CPTS_EVENT_POP_REG Register (Offset = 0003D030h) [reset = X]

CPSW_CPTS_EVENT_POP_REG is shown in [Figure 7-163](#) and described in [Table 7-334](#).

Return to [Summary Table](#).

Event Interrupt Pop Register.

Table 7-333. CPSW_CPTS_EVENT_POP_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D030h

Figure 7-163. CPSW_CPTS_EVENT_POP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 7-334. CPSW_CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	EVENT_POP	W	0h	Event Pop. When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read from the CPSW_CPTS_EVENT_0_REG to CPSW_CPTS_EVENT_3_REG registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.

7.4.14 CPSW_CPTS_EVENT_0_REG Register (Offset = 0003D034h) [reset = 0h]

CPSW_CPTS_EVENT_0_REG is shown in [Figure 7-164](#) and described in [Table 7-336](#).

Return to [Summary Table](#).

Lower 32-bits of the Event Value Register.

Table 7-335. CPSW_CPTS_EVENT_0_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D034h

Figure 7-164. CPSW_CPTS_EVENT_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 7-336. CPSW_CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp. The time stamp is valid for transmit, receive, and time stamp push event types. The time stamp value is not valid for counter roll event types.

7.4.15 CPSW_CPTS_EVENT_1_REG Register (Offset = 0003D038h) [reset = X]

CPSW_CPTS_EVENT_1_REG is shown in [Figure 7-165](#) and described in [Table 7-338](#).

Return to [Summary Table](#).

Lower Middle 32-bits of the Event Value Register.

Table 7-337. CPSW_CPTS_EVENT_1_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D038h

Figure 7-165. CPSW_CPTS_EVENT_1_REG Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
R-X		R-0h	R-0h				
23	22	21	20	19	18	17	16
EVENT_TYPE				MESSAGE_TYPE			
R-0h				R-0h			
15	14	13	12	11	10	9	8
SEQUENCE_ID							
R-0h							
7	6	5	4	3	2	1	0
SEQUENCE_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 7-338. CPSW_CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29	PREMPT_QUEUE	R	0h	Prempt QUEUE
28-24	PORT_NUMBER	R	0h	Port Number. Indicates the port number (encoded) of an Ethernet event or the encoded hardware time stamp number.
23-20	EVENT_TYPE	R	0h	Time Sync Event Type 0h = Time Stamp Push Event 1h = Time Stamp Rollover Event 2h = Time Stamp Half Rollover Event 3h = Hardware Time Stamp Push Event 4h = Ethernet Receive Event 5h = Ethernet Transmit Event 6h = Time Stamp Compare Event 7h = Host Transmit Event 8H to Fh = Reserved
19-16	MESSAGE_TYPE	R	0h	Message type. The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

Table 7-338. CPSW_CPTS_EVENT_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	SEQUENCE_ID	R	0h	<p>Sequence ID.</p> <p>The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet.</p> <p>This field is valid only for Ethernet transmit or receive events.</p>

7.4.16 CPSW_CPTS_EVENT_2_REG Register (Offset = 0003D03Ch) [reset = X]

CPSW_CPTS_EVENT_2_REG is shown in [Figure 7-166](#) and described in [Table 7-340](#).

Return to [Summary Table](#).

Upper Middle 32-bits of the Event Value Register.

Table 7-339. CPSW_CPTS_EVENT_2_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D03Ch

Figure 7-166. CPSW_CPTS_EVENT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DOMAIN							
R-X																								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 7-340. CPSW_CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	DOMAIN	R	0h	Domain. The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

7.4.17 CPSW_CPTS_EVENT_3_REG Register (Offset = 0003D040h) [reset = 0h]

CPSW_CPTS_EVENT_3_REG is shown in [Figure 7-167](#) and described in [Table 7-342](#).

Return to [Summary Table](#).

Upper 32-bits of the Event Value Register

Table 7-341. CPSW_CPTS_EVENT_3_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D040h

Figure 7-167. CPSW_CPTS_EVENT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 7-342. CPSW_CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp. The time stamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode.

7.4.18 CPSW_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 0003D044h) [reset = 0h]

CPSW_CPTS_TS_LOAD_HIGH_VAL_REG is shown in [Figure 7-168](#) and described in [Table 7-344](#).

Return to [Summary Table](#).

Time Stamp Load High Value (upper 32-bits) Register

Table 7-343.
CPSW_CPTS_TS_LOAD_HIGH_VAL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D044h

Figure 7-168. CPSW_CPTS_TS_LOAD_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-344. CPSW_CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	<p>Time Stamp Load high Value.</p> <p>Writing the CPSW_CPTS_TS_LOAD_EN_REG[0] TS_LOAD_EN bit causes the value contained in this register to be written into the time stamp.</p> <p>The time stamp value is read by initiating a time stamp push event, not by reading this register.</p> <p>When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode</p>

7.4.19 CPSW_CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 0003D048h) [reset = 0h]

CPSW_CPTS_TS_COMP_HIGH_VAL_REG is shown in [Figure 7-169](#) and described in [Table 7-346](#).

Return to [Summary Table](#).

Time Stamp Comparison High Value (upper 32-bits) Register.

Table 7-345.
CPSW_CPTS_TS_COMP_HIGH_VAL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D048h

Figure 7-169. CPSW_CPTS_TS_COMP_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-346. CPSW_CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_HIGH_VAL	R/W	0h	<p>Time Stamp Comparison High Value.</p> <p>Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the [31-0]TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL and CPSW_CPTS_TS_COMP_HIGH_VAL_REG[31-0] TS_COMP_HIGH_VAL.</p> <p>This value is unused in 32-bit mode. The upper 32-bits in CPSW_CPTS_TS_COMP_HIGH_VAL_REG register should be written before the lower 32-bits in the CPSW_CPTS_TS_COMP_VAL_REG register.</p>

7.4.20 CPSW_CPTS_TS_ADD_VAL_REG Register (Offset = 0003D04Ch) [reset = X]

CPSW_CPTS_TS_ADD_VAL_REG is shown in [Figure 7-170](#) and described in [Table 7-348](#).

Return to [Summary Table](#).

TS Add Value Register

Table 7-347. CPSW_CPTS_TS_ADD_VAL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D04Ch

Figure 7-170. CPSW_CPTS_TS_ADD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ADD_VAL			
R/W-X												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-348. CPSW_CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	ADD_VAL	R/W	0h	<p>The ts_add_value[2:0] is added to 1 to comprise the time stamp increment value.</p> <p>The time stamp increment value is added to the current time stamp (time_stamp[63:0]) on each RCLK. The time stamp increment value can be adjusted by nudge and ppm also. The CPSW_CPTS_TS_ADD_VAL_REG[2:0] ADD_VAL value may be non-zero in 64-bit mode only.</p>

7.4.21 CPSW_CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 0003D050h) [reset = 0h]

CPSW_CPTS_TS_PPM_LOW_VAL_REG is shown in [Figure 7-171](#) and described in [Table 7-350](#).

Return to [Summary Table](#).

Time Stamp PPM Load Low Value (lower 32-bits) Register.

Table 7-349. CPSW_CPTS_TS_PPM_LOW_VAL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D050h

Figure 7-171. CPSW_CPTS_TS_PPM_LOW_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-350. CPSW_CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_PPM_LOW_VAL	R/W	0h	Time Stamp PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen.

7.4.22 CPSW_CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 0003D054h) [reset = X]

CPSW_CPTS_TS_PPM_HIGH_VAL_REG is shown in [Figure 7-172](#) and described in [Table 7-352](#).

Return to [Summary Table](#).

Time Stamp PPM Load High Value (upper 32-bits) Register.

Table 7-351.
CPSW_CPTS_TS_PPM_HIGH_VAL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D054h

Figure 7-172. CPSW_CPTS_TS_PPM_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_PPM_HIGH_VAL							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-352. CPSW_CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TS_PPM_HIGH_VAL	R/W	0h	Time Stamp PPM High Value. This value should be written first (before the low value is written). The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG [31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG [9-0] TS_PPM_HIGH_VAL).

7.4.23 CPSW_CPTS_TS_NUDGE_VAL_REG Register (Offset = 0003D058h) [reset = X]

CPSW_CPTS_TS_NUDGE_VAL_REG is shown in [Figure 7-173](#) and described in [Table 7-354](#).

Return to [Summary Table](#).

Time Stamp Nudge Value Register

Table 7-353. CPSW_CPTS_TS_NUDGE_VAL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D058h

Figure 7-173. CPSW_CPTS_TS_NUDGE_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_NUDGE_VAL							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-354. CPSW_CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS_NUDGE_VAL	R/W	0h	<p>Time stamp Nudge Value.</p> <p>This two's complement number is added to the CPSW_CPTS_EVENT_0_REG[31-0] TIME_STAMP and CPSW_CPTS_EVENT_3_REG[[31-0] TIME_STAMP value to increase or decrease the time stamp value by the CPSW_CPTS_TS_NUDGE_VAL_REG[7-0] TS_NUDGE_VAL amount. The TS_NUDGE_VAL value is cleared to zero when the nudge has occurred.</p> <p>The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).</p>

7.4.24 CPSW_GENF0_COMP_LOW_REG_L Register (Offset = 0003D0E0h) [reset = 0h]

CPSW_GENF0_COMP_LOW_REG_L is shown in Figure 7-174 and described in Table 7-356.

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Comparison Low Value (lower 32-bits).

Offset = 0003D0E0h + (I * 20h); where I = 0 to 1

Table 7-355. CPSW_GENF0_COMP_LOW_REG_L Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D0E0h

Figure 7-174. CPSW_GENF0_COMP_LOW_REG_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-356. CPSW_GENF0_COMP_LOW_REG_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_GENF0_COMP_HIGH_REG_L and CPSW_GENF0_COMP_LOW_REG_L should only be written when the CPSW_GENF0_LENGTH_REG_L [31-0] LENGTH value is zero.

7.4.25 CPSW_GENF0_COMP_HIGH_REG_L Register (Offset = 0003D0E4h) [reset = 0h]

CPSW_GENF0_COMP_HIGH_REG_L is shown in [Figure 7-175](#) and described in [Table 7-358](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Comparison high Value (upper 32-bits).

Offset = 0003D0E4h + (I * 20h); where I = 0 to 1

**Table 7-357. CPSW_GENF0_COMP_HIGH_REG_L
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D0E4h

Figure 7-175. CPSW_GENF0_COMP_HIGH_REG_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-358. CPSW_GENF0_COMP_HIGH_REG_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits. The CPSW_GENF0_COMP_HIGH_REG_L and CPSW_GENF0_COMP_LOW_REG_L should only be written when the CPSW_GENF0_LENGTH_REG_L [31-0] LENGTH value is zero.

7.4.26 CPSW_GENF0_TS_GENF_CONTROL_REG Register (Offset = 0003D0E8h) [reset = X]

CPSW_GENF0_TS_GENF_CONTROL_REG is shown in Figure 7-176 and described in Table 7-360.

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Control Registers.

Offset = 0003D0E8h + (I * 20h); where I = 0 to 1

Table 7-359.
CPSW_GENF0_TS_GENF_CONTROL_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D0E8h

Figure 7-176. CPSW_GENF0_TS_GENF_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-360. CPSW_GENF0_TS_GENF_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert 0h = The output TS_GENFn signal asserts low 1h = The output TS_GENFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction. 0h = A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h = A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

7.4.27 CPSW_GENF0_LENGTH_REG_L Register (Offset = 0003D0ECh) [reset = 0h]

CPSW_GENF0_LENGTH_REG_L is shown in [Figure 7-177](#) and described in [Table 7-362](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Length Value.

Offset = 0003D0ECh + (I * 20h); where I = 0 to 1

**Table 7-361. CPSW_GENF0_LENGTH_REG_L
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D0ECh

Figure 7-177. CPSW_GENF0_LENGTH_REG_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-362. CPSW_GENF0_LENGTH_REG_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value

7.4.28 CPSW_GENF0_PPM_LOW_REG_L Register (Offset = 0003D0F0h) [reset = 0h]

CPSW_GENF0_PPM_LOW_REG_L is shown in [Figure 7-178](#) and described in [Table 7-364](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) PPM Low Value (lower 32-bits).

Offset = 0003D0F0h + (I * 20h); where I = 0 to 1

**Table 7-363. CPSW_GENF0_PPM_LOW_REG_L
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D0F0h

Figure 7-178. CPSW_GENF0_PPM_LOW_REG_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-364. CPSW_GENF0_PPM_LOW_REG_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

7.4.29 CPSW_GENF0_PPM_HIGH_REG_L Register (Offset = 0003D0F4h) [reset = X]

CPSW_GENF0_PPM_HIGH_REG_L is shown in [Figure 7-179](#) and described in [Table 7-366](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) PPM High Value (upper 32-bits).

Offset = 0003D0F4h + (I * 20h); where I = 0 to 1

**Table 7-365. CPSW_GENF0_PPM_HIGH_REG_L
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D0F4h

Figure 7-179. CPSW_GENF0_PPM_HIGH_REG_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-366. CPSW_GENF0_PPM_HIGH_REG_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value. This value should be written first (before the low value is written).

7.4.30 CPSW_GENF0_NUDGE_REG_L Register (Offset = 0003D0F8h) [reset = X]

CPSW_GENF0_NUDGE_REG_L is shown in Figure 7-180 and described in Table 7-368.

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Nudge Value Registers.

Offset = 0003D0F8h + (I * 20h); where I = 0 to 1

**Table 7-367. CPSW_GENF0_NUDGE_REG_L
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D0F8h

Figure 7-180. CPSW_GENF0_NUDGE_REG_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
RESERVED																								NUDGE															
R/W-X																								R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-368. CPSW_GENF0_NUDGE_REG_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_GENF0_NUDGE_REG_L[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_GENF0_NUDGE_REG_L value is cleared to zero when the nudge has occurred.

7.4.31 CPSW_GENF1_COMP_LOW_REG Register (Offset = 0003D100h) [reset = 0h]

CPSW_GENF1_COMP_LOW_REG is shown in [Figure 7-181](#) and described in [Table 7-370](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Comparison Low Value.

**Table 7-369. CPSW_GENF1_COMP_LOW_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D200h

Figure 7-181. CPSW_GENF1_COMP_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-370. CPSW_GENF1_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function (GENF1) Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_GENF1_COMP_HIGH_REG_L and CPSW_GENF1_COMP_LOW_REG should only be written when the CPSW_GENF1_LENGTH_REG_L[31-0] LENGTH value is zero.

7.4.32 CPSW_GENF1_COMP_HIGH_REG Register (Offset = 0003D104h) [reset = 0h]

CPSW_GENF1_COMP_HIGH_REG is shown in [Figure 7-182](#) and described in [Table 7-372](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Comparison high Value (upper 32-bits).

Table 7-371. CPSW_GENF1_COMP_HIGH_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D204h

Figure 7-182. CPSW_GENF1_COMP_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-372. CPSW_GENF1_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function (GENF1) Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits are written. The CPSW_GENF1_COMP_HIGH_REG and CPSW_GENF1_COMP_LOW_REG should only be written when the CPSW_GENF0_LENGTH_REG_L[31-0] LENGTH value is zero.

7.4.33 CPSW_GENF1_CONTROL_REG Register (Offset = 0003D108h) [reset = X]

CPSW_GENF1_CONTROL_REG is shown in [Figure 7-183](#) and described in [Table 7-374](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Control Register.

**Table 7-373. CPSW_GENF1_CONTROL_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D208h

Figure 7-183. CPSW_GENF1_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-374. CPSW_GENF1_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function (GENF1) Polarity Invert. 0h = The output TS_GENFn signal asserts low 1h = The output TS_GENFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function (GENF1) PPM Direction. 0h = A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h = A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

7.4.34 CPSW_GENF1_LENGTH_REG Register (Offset = 0003D10Ch) [reset = 0h]

CPSW_GENF1_LENGTH_REG is shown in [Figure 7-184](#) and described in [Table 7-376](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Length Value

Table 7-375. CPSW_GENF1_LENGTH_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D20Ch

Figure 7-184. CPSW_GENF1_LENGTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-376. CPSW_GENF1_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp Generate Function (GENF1) Length Value

7.4.35 CPSW_GENF1_PPM_LOW_REG Register (Offset = 0003D110h) [reset = 0h]

CPSW_GENF1_PPM_LOW_REG is shown in [Figure 7-185](#) and described in [Table 7-378](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) PPM Low Value (lower 32-bits).

**Table 7-377. CPSW_GENF1_PPM_LOW_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D210h

Figure 7-185. CPSW_GENF1_PPM_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-378. CPSW_GENF1_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp Generate Function (GENF1) PPM Low Value The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

7.4.36 CPSW_GENF1_PPM_HIGH_REG Register (Offset = 0003D114h) [reset = X]

CPSW_GENF1_PPM_HIGH_REG is shown in [Figure 7-186](#) and described in [Table 7-380](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) PPM High Value (upper 32-bits).

Table 7-379. CPSW_GENF1_PPM_HIGH_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D214h

Figure 7-186. CPSW_GENF1_PPM_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-380. CPSW_GENF1_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp Generate Function (GENF1) PPM High Value. This value should be written first (before the low value is written).

7.4.37 CPSW_GENF1_NUDGE_REG Register (Offset = 0003D118h) [reset = X]

CPSW_GENF1_NUDGE_REG is shown in [Figure 7-187](#) and described in [Table 7-382](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Nudge Value.

Table 7-381. CPSW_GENF1_NUDGE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D218h

Figure 7-187. CPSW_GENF1_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-382. CPSW_GENF1_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp Generate Function (GENF1) Nudge Value . This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_GENF1_NUDGE_REG[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_GENF1_NUDGE_REG value is cleared to zero when the nudge has occurred.

7.4.38 CPSW_ESTF1_COMP_LOW_REG Register (Offset = 0003D200h) [reset = 0h]

CPSW_ESTF1_COMP_LOW_REG is shown in [Figure 7-188](#) and described in [Table 7-384](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTF1) Comparison Low Value.

Table 7-383. CPSW_ESTF1_COMP_LOW_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D200h

Figure 7-188. CPSW_ESTF1_COMP_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-384. CPSW_ESTF1_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function (ESTF1) Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_ESTF1_COMP_HIGH_REG_L and CPSW_ESTF1_COMP_LOW_REG should only be written when the CPSW_ESTF1_LENGTH_REG_L[31-0] LENGTH value is zero.

7.4.39 CPSW_ESTF1_COMP_HIGH_REG Register (Offset = 0003D204h) [reset = 0h]

CPSW_ESTF1_COMP_HIGH_REG is shown in [Figure 7-189](#) and described in [Table 7-386](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTF1) Comparison high Value (upper 32-bits).

Table 7-385. CPSW_ESTF1_COMP_HIGH_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D204h

Figure 7-189. CPSW_ESTF1_COMP_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-386. CPSW_ESTF1_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function (ESTF1) Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits are written. The CPSW_ESTF1_COMP_HIGH_REG and CPSW_ESTF1_COMP_LOW_REG should only be written when the CPSW_ESTF1_LENGTH_REG_L[31-0] LENGTH value is zero.

7.4.40 CPSW_ESTF1_CONTROL_REG Register (Offset = 0003D208h) [reset = X]

CPSW_ESTF1_CONTROL_REG is shown in Figure 7-190 and described in Table 7-388.

Return to [Summary Table](#).

Time Stamp Generate Function (ESTF1) Control Register.

Table 7-387. CPSW_ESTF1_CONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D208h

Figure 7-190. CPSW_ESTF1_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-388. CPSW_ESTF1_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function (ESTF1) Polarity Invert. 0h = The output TS_ESTFn signal asserts low 1h = The output TS_ESTFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function (ESTF1) PPM Direction. 0h = A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h = A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

7.4.41 CPSW_ESTF1_LENGTH_REG Register (Offset = 0003D20Ch) [reset = 0h]

CPSW_ESTF1_LENGTH_REG is shown in [Figure 7-191](#) and described in [Table 7-390](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTF1) Length Value

Table 7-389. CPSW_ESTF1_LENGTH_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D20Ch

Figure 7-191. CPSW_ESTF1_LENGTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-390. CPSW_ESTF1_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp Generate Function (ESTF1) Length Value

7.4.42 CPSW_ESTF1_PPM_LOW_REG Register (Offset = 0003D210h) [reset = 0h]

CPSW_ESTF1_PPM_LOW_REG is shown in [Figure 7-192](#) and described in [Table 7-392](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTF1) PPM Low Value (lower 32-bits).

Table 7-391. CPSW_ESTF1_PPM_LOW_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D210h

Figure 7-192. CPSW_ESTF1_PPM_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-392. CPSW_ESTF1_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp Generate Function (ESTF1) PPM Low Value The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

7.4.43 CPSW_ESTF1_PPM_HIGH_REG Register (Offset = 0003D214h) [reset = X]

CPSW_ESTF1_PPM_HIGH_REG is shown in [Figure 7-193](#) and described in [Table 7-394](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTF1) PPM High Value (upper 32-bits).

**Table 7-393. CPSW_ESTF1_PPM_HIGH_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D214h

Figure 7-193. CPSW_ESTF1_PPM_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-394. CPSW_ESTF1_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp Generate Function (ESTF1) PPM High Value. This value should be written first (before the low value is written).

7.4.44 CPSW_ESTF1_NUDGE_REG Register (Offset = 0003D218h) [reset = X]

CPSW_ESTF1_NUDGE_REG is shown in [Figure 7-194](#) and described in [Table 7-396](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTF1) Nudge Value.

Table 7-395. CPSW_ESTF1_NUDGE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_CPTS	4603 D218h

Figure 7-194. CPSW_ESTF1_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-396. CPSW_ESTF1_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp Generate Function (ESTF1) Nudge Value . This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_ESTF1_NUDGE_REG[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_ESTF1_NUDGE_REG value is cleared to zero when the nudge has occurred.

7.5 MCU_CPSW0_ECC Registers

Table 7-398 lists the memory-mapped registers for the MCU_CPSW0_ECC. All register offset addresses not listed in Table 7-398 should be considered as reserved locations and the register contents should not be modified.

Table 7-397. MCU_CPSW0_ECC Instances

Instance	Base Address
MCU_CPSW0_ECC	4070 9000h

Table 7-398. MCU_CPSW0_ECC Registers

Offset	Acronym	Register Name	MCU_CPSW0_ECC Physical Address	Section
0h	CPSW_ECC_REV	Aggregator Revision Register	4070 9000h	Section 7.5.1
8h	CPSW_ECC_VECTOR	ECC Vector Register	4070 9008h	Section 7.5.2
Ch	CPSW_ECC_STAT	Misc Status	4070 900Ch	Section 7.5.3
10h + formula	CPSW_ECC_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4070 9010h + formula	Section 7.5.4
3Ch	CPSW_ECC_SEC_EOI_REG	EOI Register	4070 903Ch	Section 7.5.5
40h	CPSW_ECC_SEC_STATUS_REG0	Interrupt Status Register 0	4070 9040h	Section 7.5.6
80h	CPSW_ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4070 9080h	Section 7.5.7
C0h	CPSW_ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4070 90C0h	Section 7.5.8
13Ch	CPSW_ECC_DED_EOI_REG	EOI Register	4070 913Ch	Section 7.5.9
140h	CPSW_ECC_DED_STATUS_REG0	Interrupt Status Register 0	4070 9140h	Section 7.5.10
180h	CPSW_ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4070 9180h	Section 7.5.11
1C0h	CPSW_ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4070 91C0h	Section 7.5.12
200h	CPSW_ECC_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4070 9200h	Section 7.5.13
204h	CPSW_ECC_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4070 9204h	Section 7.5.14
208h	CPSW_ECC_AGGR_STATUS_SET	AGGR interrupt status set Register	4070 9208h	Section 7.5.15
20Ch	CPSW_ECC_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4070 920Ch	Section 7.5.16

7.5.1 CPSW_ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

CPSW_ECC_REV is shown in [Figure 7-195](#) and described in [Table 7-400](#).

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Table 7-399. CPSW_ECC_REV Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 9000h

Figure 7-195. CPSW_ECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVM AJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 7-400. CPSW_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVM AJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

7.5.2 CPSW_ECC_VECTOR Register (Offset = 8h) [reset = X]

CPSW_ECC_VECTOR is shown in [Figure 7-196](#) and described in [Table 7-402](#).

Return to [Summary Table](#).

ECC Vector Register

Table 7-401. CPSW_ECC_VECTOR Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 9008h

Figure 7-196. CPSW_ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-402. CPSW_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

7.5.3 CPSW_ECC_STAT Register (Offset = Ch) [reset = X]

CPSW_ECC_STAT is shown in [Figure 7-197](#) and described in [Table 7-404](#).

Return to [Summary Table](#).

Misc Status

Table 7-403. CPSW_ECC_STAT Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 900Ch

Figure 7-197. CPSW_ECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMs										
R-X																					R-14h										

LEGEND: R = Read Only; -n = value after reset

Table 7-404. CPSW_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	14h	Indicates the number of RAMs serviced by the ECC aggregator

7.5.4 CPSW_ECC_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

CPSW_ECC_RESERVED_SVBUS_y is shown in [Figure 7-198](#) and described in [Table 7-406](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 7-405. CPSW_ECC_RESERVED_SVBUS_y
Instances**

Instance	Physical Address
MCU_CPSW0_ECC	4070 9010h + formula

Figure 7-198. CPSW_ECC_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-406. CPSW_ECC_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

7.5.5 CPSW_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

CPSW_ECC_SEC_EOI_REG is shown in [Figure 7-199](#) and described in [Table 7-408](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 7-407. CPSW_ECC_SEC_EOI_REG Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 903Ch

Figure 7-199. CPSW_ECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-408. CPSW_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

7.5.6 CPSW_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

CPSW_ECC_SEC_STATUS_REG0 is shown in [Figure 7-200](#) and described in [Table 7-410](#).

[Return to Summary Table.](#)

Interrupt Status Register 0

**Table 7-409. CPSW_ECC_SEC_STATUS_REG0
Instances**

Instance	Physical Address
MCU_CPSW0_ECC	4070 9040h

Figure 7-200. CPSW_ECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_P END	RAMECC18_P END	RAMECC17_P END	RAMECC16_P END
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RAMECC15_P END	RAMECC14_P END	RAMECC13_P END	RAMECC12_P END	RAMECC11_P END	RAMECC10_P END	RAMECC9_P END	RAMECC8_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RAMECC7_P END	RAMECC6_P END	RAMECC5_P END	RAMECC4_P END	RAMECC3_P END	RAMECC2_P END	RAMECC1_P END	RAMECC0_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-410. CPSW_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_PEND	R/W1S	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1S	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1S	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1S	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1S	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1S	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1S	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1S	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1S	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1S	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1S	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1S	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1S	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1S	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1S	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1S	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1S	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1S	0h	Interrupt Pending Status for ramecc2_pend

Table 7-410. CPSW_ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RAMECC1_PEND	R/W1S	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1S	0h	Interrupt Pending Status for ramecc0_pend

7.5.7 CPSW_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

CPSW_ECC_SEC_ENABLE_SET_REG0 is shown in Figure 7-201 and described in Table 7-412.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

**Table 7-411. CPSW_ECC_SEC_ENABLE_SET_REG0
Instances**

Instance	Physical Address
MCU_CPSW0_ECC	4070 9080h

Figure 7-201. CPSW_ECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_E NABLE_SET	RAMECC18_E NABLE_SET	RAMECC17_E NABLE_SET	RAMECC16_E NABLE_SET
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RAMECC15_E NABLE_SET	RAMECC14_E NABLE_SET	RAMECC13_E NABLE_SET	RAMECC12_E NABLE_SET	RAMECC11_E NABLE_SET	RAMECC10_E NABLE_SET	RAMECC9_EN ABLE_SET	RAMECC8_EN ABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RAMECC7_EN ABLE_SET	RAMECC6_EN ABLE_SET	RAMECC5_EN ABLE_SET	RAMECC4_EN ABLE_SET	RAMECC3_EN ABLE_SET	RAMECC2_EN ABLE_SET	RAMECC1_EN ABLE_SET	RAMECC0_EN ABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-412. CPSW_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc10_pend
9	RAMECC9_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc9_pend

Table 7-412. CPSW_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RAMECC8_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc0_pend

7.5.8 CPSW_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

CPSW_ECC_SEC_ENABLE_CLR_REG0 is shown in Figure 7-202 and described in Table 7-414.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

**Table 7-413. CPSW_ECC_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
MCU_CPSW0_ECC	4070 90C0h

Figure 7-202. CPSW_ECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_E NABLE_CLR	RAMECC18_E NABLE_CLR	RAMECC17_E NABLE_CLR	RAMECC16_E NABLE_CLR
R/W-X				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RAMECC15_E NABLE_CLR	RAMECC14_E NABLE_CLR	RAMECC13_E NABLE_CLR	RAMECC12_E NABLE_CLR	RAMECC11_E NABLE_CLR	RAMECC10_E NABLE_CLR	RAMECC9_EN ABLE_CLR	RAMECC8_EN ABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RAMECC7_EN ABLE_CLR	RAMECC6_EN ABLE_CLR	RAMECC5_EN ABLE_CLR	RAMECC4_EN ABLE_CLR	RAMECC3_EN ABLE_CLR	RAMECC2_EN ABLE_CLR	RAMECC1_EN ABLE_CLR	RAMECC0_EN ABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-414. CPSW_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc10_pend

Table 7-414. CPSW_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc0_pend

7.5.9 CPSW_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

CPSW_ECC_DED_EOI_REG is shown in [Figure 7-203](#) and described in [Table 7-416](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 7-415. CPSW_ECC_DED_EOI_REG Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 913Ch

Figure 7-203. CPSW_ECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-416. CPSW_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

7.5.10 CPSW_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

CPSW_ECC_DED_STATUS_REG0 is shown in Figure 7-204 and described in Table 7-418.

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 7-417. CPSW_ECC_DED_STATUS_REG0
Instances**

Instance	Physical Address
MCU_CPSW0_ECC	4070 9140h

Figure 7-204. CPSW_ECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_P END	RAMECC18_P END	RAMECC17_P END	RAMECC16_P END
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RAMECC15_P END	RAMECC14_P END	RAMECC13_P END	RAMECC12_P END	RAMECC11_P END	RAMECC10_P END	RAMECC9_P END	RAMECC8_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RAMECC7_P END	RAMECC6_P END	RAMECC5_P END	RAMECC4_P END	RAMECC3_P END	RAMECC2_P END	RAMECC1_P END	RAMECC0_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-418. CPSW_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_PEND	R/W1S	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1S	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1S	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1S	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1S	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1S	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1S	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1S	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1S	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1S	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1S	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1S	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1S	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1S	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1S	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1S	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1S	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1S	0h	Interrupt Pending Status for ramecc2_pend

Table 7-418. CPSW_ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RAMECC1_PEND	R/W1S	0h	Interrupt Pending Status for ramecc1_pend
0	RAMECC0_PEND	R/W1S	0h	Interrupt Pending Status for ramecc0_pend

7.5.11 CPSW_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

CPSW_ECC_DED_ENABLE_SET_REG0 is shown in Figure 7-205 and described in Table 7-420.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 7-419. CPSW_ECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 9180h

Figure 7-205. CPSW_ECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-420. CPSW_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc10_pend
9	RAMECC9_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc9_pend

Table 7-420. CPSW_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RAMECC8_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc0_pend

7.5.12 CPSW_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

CPSW_ECC_DED_ENABLE_CLR_REG0 is shown in Figure 7-206 and described in Table 7-422.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 7-421. CPSW_ECC_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 91C0h

Figure 7-206. CPSW_ECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
R/W-X				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-422. CPSW_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc10_pend

Table 7-422. CPSW_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc0_pend

7.5.13 CPSW_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

CPSW_ECC_AGGR_ENABLE_SET is shown in Figure 7-207 and described in Table 7-424.

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 7-423. CPSW_ECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 9200h

Figure 7-207. CPSW_ECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-424. CPSW_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

7.5.14 CPSW_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

CPSW_ECC_AGGR_ENABLE_CLR is shown in [Figure 7-208](#) and described in [Table 7-426](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

**Table 7-425. CPSW_ECC_AGGR_ENABLE_CLR
Instances**

Instance	Physical Address
MCU_CPSW0_ECC	4070 9204h

Figure 7-208. CPSW_ECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-426. CPSW_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

7.5.15 CPSW_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

CPSW_ECC_AGGR_STATUS_SET is shown in [Figure 7-209](#) and described in [Table 7-428](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

Table 7-427. CPSW_ECC_AGGR_STATUS_SET Instances

Instance	Physical Address
MCU_CPSW0_ECC	4070 9208h

Figure 7-209. CPSW_ECC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 7-428. CPSW_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

7.5.16 CPSW_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

CPSW_ECC_AGGR_STATUS_CLR is shown in [Figure 7-210](#) and described in [Table 7-430](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

**Table 7-429. CPSW_ECC_AGGR_STATUS_CLR
Instances**

Instance	Physical Address
MCU_CPSW0_ECC	4070 920Ch

Figure 7-210. CPSW_ECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 7-430. CPSW_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

7.6 MCU_CPSW0_MDIO Registers

Table 7-432 lists the memory-mapped registers for the MCU_CPSW0_MDIO. All register offset addresses not listed in Table 7-432 should be considered as reserved locations and the register contents should not be modified.

Table 7-431. MCU_CPSW0_MDIO Instances

Instance	Base Address
MCU_CPSW0_NUSS_MDIO	4600 0000h

Table 7-432. MCU_CPSW0_MDIO Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_MDIO Physical Address
F00h	CPSW_MDIO_VERSION_REG	MDIO Version Register	4600 0F00h
F04h	CPSW_MDIO_CONTROL_REG	MDIO Control Register	4600 0F04h
F08h	CPSW_MDIO_ALIVE_REG	MDIO Alive Register	4600 0F08h
F0Ch	CPSW_MDIO_LINK_REG	MDIO Link Register	4600 0F0Ch
F10h	CPSW_MDIO_LINK_INT_RAW_REG	MDIO Link Interrupt Raw Register	4600 0F10h
F14h	CPSW_MDIO_LINK_INT_MASKED_REG	MDIO Link Interrupt Masked Register	4600 0F14h
F18h	CPSW_MDIO_LINK_INT_MASK_SET_REG	MDIO Link Interrupt Mask Set Register	4600 0F18h
F1Ch	CPSW_MDIO_LINK_INT_MASK_CLEAR_REG	MDIO Link Interrupt Mask Clear Register	4600 0F1Ch
F20h	CPSW_MDIO_USER_INT_RAW_REG	MDIO User Interrupt Raw Register	4600 0F20h
F24h	CPSW_MDIO_USER_INT_MASKED_REG	MDIO User Interrupt Masked Register	4600 0F24h
F28h	CPSW_MDIO_USER_INT_MASK_SET_REG	MDIO User Interrupt Mask Set Register	4600 0F28h
F2Ch	CPSW_MDIO_USER_INT_MASK_CLEAR_REG	MDIO User Interrupt Mask Clear Register	4600 0F2Ch
F30h	CPSW_MDIO_MANUAL_IF_REG	MDIO Manual Interface Register	4600 0F30h
F34h	CPSW_MDIO_POLL_REG	MDIO Poll Inter Register	4600 0F34h
F38h	CPSW_MDIO_POLL_EN_REG	MDIO Poll Enable Register	4600 0F38h
F3Ch	CPSW_MDIO_CLAUS45_REG	Clause 45 Enable Register	4600 0F3Ch
F40h	CPSW_MDIO_USER_ADDR0_REG	MDIO User Address 0 Register	4600 0F40h
F44h	CPSW_MDIO_USER_ADDR1_REG	MDIO User Address 1 Register	4600 0F44h
F80h + formula	CPSW_MDIO_USER_ACCESS_REG_k	MDIO User Access k Register	4600 0F80h + formula
F84h + formula	CPSW_MDIO_USER_PHY_SEL_REG_k	MDIO User PHY Select k Register	4600 0F84h + formula

7.6.1 CPSW_MDIO_VERSION_REG Register (Offset = F00h) [reset = 00070907h]

CPSW_MDIO_VERSION_REG is shown in [Figure 7-211](#) and described in [Table 7-434](#).

[Return to Summary Table.](#)

MDIO Version Register

Table 7-433. CPSW_MDIO_VERSION_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F00h

Figure 7-211. CPSW_MDIO_VERSION_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-0h		R-0h		R-7h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMaj			CUSTOM		REVMIN					
R-1h					R-1h			R-0h		R-7h					

LEGEND: R = Read Only; -n = value after reset

Table 7-434. CPSW_MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	0h	Scheme
29-28	BU	R	0h	bu
27-16	MODULE_ID	R	7h	Module ID
15-11	REVRTL	R	1h	RTL version
10-8	REVMaj	R	1h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	7h	Minor version

7.6.2 CPSW_MDIO_CONTROL_REG Register (Offset = F04h) [reset = X]

MCU_CPSW0_CONTROL_REG is shown in [Figure 7-212](#) and described in [Table 7-436](#).

Return to [Summary Table](#).

MDIO Control Register

Table 7-435. CPSW_MDIO_CONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F04h

Figure 7-212. MCU_CPSW0_CONTROL_REG Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R-1h	R/W-0h	R/W-X	R-1h				
23	22	21	20	19	18	17	16
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
R/W-X			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X
15	14	13	12	11	10	9	8
CLKDIV							
R/W-FFh							
7	6	5	4	3	2	1	0
CLKDIV							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 7-436. CPSW_MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1h when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1h to this bit enables the MDIO state machine, writing a 0h disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	R/W	X	
28-24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest user access channel that is available in the module and is currently set to 1h. This implies that MDIOUserAccess1 is the highest available user access channel.
23-21	RESERVED	R/W	X	
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1h to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.

Table 7-436. CPSW_MDIO_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	FAULT	R/W	0h	Fault indicator. This bit is set to 1h if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1h to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1h to enable the physical layer fault detection.
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1h to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	R/W	X	
15-0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. MDCLK is disabled when clkdiv is set to 0h. $\text{MDCLK frequency} = \text{clk frequency} / (\text{clkdiv} + 1)$.

7.6.3 CPSW_MDIO_ALIVE_REG Register (Offset = F08h) [reset = 0h]

CPSW_MDIO_ALIVE_REG is shown in [Figure 7-213](#) and described in [Table 7-438](#).

Return to [Summary Table](#).

MDIO Alive Register

Table 7-437. CPSW_MDIO_ALIVE_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F08h

Figure 7-213. CPSW_MDIO_ALIVE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIVE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-438. CPSW_MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ALIVE	R/W	0h	<p>MDIO Alive.</p> <p>Each of the 32-bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address.</p> <p>Writing a 1h to any bit will clear it, writing a 0h has no effect.</p>

7.6.4 CPSW_MDIO_LINK_REG Register (Offset = F0Ch) [reset = 0h]

CPSW_MDIO_LINK_REG is shown in [Figure 7-214](#) and described in [Table 7-440](#).

Return to [Summary Table](#).

MDIO Link Register

Table 7-439. CPSW_MDIO_LINK_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F0Ch

Figure 7-214. CPSW_MDIO_LINK_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 7-440. CPSW_MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LINK	R	0h	<p>MDIO Link state.</p> <p>This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to 0h if the PHY indicates it does not have link or fails to acknowledge the read transaction.</p> <p>Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIOUserPhySel registers can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIOUserPhySel register. In State Change Mode the MLINK input pins are unused.</p>

7.6.5 CPSW_MDIO_LINK_INT_RAW_REG Register (Offset = F10h) [reset = X]

CPSW_MDIO_LINK_INT_RAW_REG is shown in [Figure 7-215](#) and described in [Table 7-442](#).

Return to [Summary Table](#).

MDIO Link Interrupt Raw Register

Table 7-441. CPSW_MDIO_LINK_INT_RAW_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F10h

Figure 7-215. CPSW_MDIO_LINK_INT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-442. CPSW_MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	LINKINTRAW	R/W	0h	<p>MDIO link change event raw value.</p> <p>Normal mode operation:</p> <p>When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register. [0]LINKINTRAW and [1]LINKINTRAW correspond to MDIOUserPhySel0 and MDIOUserPhySel1, respectively. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set LINKINTRAW bits to a 1h which may be used for test purposes.</p> <p>MDIO link change event raw value. State Change Mode operation:</p> <p>The [0]LINKINTRAW bit will be asserted '1' when any bit (for any PHY) in the MDIOAlive or MDIOLink registers changes due to MDIO operations. The [1]LINKINTRAW bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the [0]LINKINTRAW bit to a 1h which may be used for test purposes.</p>

7.6.6 CPSW_MDIO_LINK_INT_MASKED_REG Register (Offset = F14h) [reset = X]

CPSW_MDIO_LINK_INT_MASKED_REG is shown in [Figure 7-216](#) and described in [Table 7-444](#).

Return to [Summary Table](#).

MDIO Link Interrupt Masked Register

Table 7-443. CPSW_MDIO_LINK_INT_MASKED_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F14h

Figure 7-216. CPSW_MDIO_LINK_INT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-444. CPSW_MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	LINKINTMASKED	R/W	0h	MDIO link change interrupt masked value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding CPSW_MDIO_USER_PHY_SEL_REG_k[6] LINKINT_ENABLE bit was set. CPSW_MDIO_LINK_INT_MASKED_REG[0] LINKINTMASKED and [1] LINKINTMASKED correspond to MDIOUserPhySel0 and MDIOUserPhySel1, respectively. Writing a 1h will clear the interrupt and writing 0h has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values. MDIO link change interrupt masked value. State Change Mode operation: The [0] LINKINTMASKED bit will be asserted '1' when CPSW_MDIO_LINK_INT_RAW_REG[0] LINKINTRAW is asserted '1' and when the CPSW_MDIO_LINK_INT_MASK_SET_REG[0] LINKINTMASKSET bit is set to 1h. Writing a 1h will clear [0] LINKINTMASKED (and the MDIO_LINKINT[0] output) and writing 0h has no effect. The [1] LINKINTMASKED bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode).

7.6.7 CPSW_MDIO_LINK_INT_MASK_SET_REG Register (Offset = F18h) [reset = X]

CPSW_MDIO_LINK_INT_MASK_SET_REG is shown in [Figure 7-217](#) and described in [Table 7-446](#).

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MDIO Link Interrupt Mask Set Register

Table 7-445.
CPSW_MDIO_LINK_INT_MASK_SET_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F18h

Figure 7-217. CPSW_MDIO_LINK_INT_MASK_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK SET
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-446. CPSW_MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINKINTMASKSET	R/W	0h	MDIO link interrupt mask set. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask set. State Change Mode Operation: Writing this bit to 1h will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when [0] LINKINTRAW is asserted.

7.6.8 CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = F1Ch) [reset = X]

CPSW_MDIO_LINK_INT_MASK_CLEAR_REG is shown in [Figure 7-218](#) and described in [Table 7-448](#).

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MDIO Link Interrupt Mask Clear Register

Table 7-447.
CPSW_MDIO_LINK_INT_MASK_CLEAR_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F1Ch

Figure 7-218. CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK CLR
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-448. CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINKINTMASKCLR	R/W	0h	MDIO link interrupt mask clear. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask clear. State Change Mode Operation: Writing this bit to 1h will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the [0] LINKINTRAW bit value.

7.6.9 CPSW_MDIO_USER_INT_RAW_REG Register (Offset = F20h) [reset = X]

CPSW_MDIO_USER_INT_RAW_REG is shown in [Figure 7-219](#) and described in [Table 7-450](#).

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MDIO User Interrupt Raw Register

Table 7-449. CPSW_MDIO_USER_INT_RAW_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F20h

Figure 7-219. CPSW_MDIO_USER_INT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-450. CPSW_MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTRAW	R/W	0h	Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the userintraw bits to a 1h. This mode may be used for test purposes.

7.6.10 CPSW_MDIO_USER_INT_MASKED_REG Register (Offset = F24h) [reset = X]

CPSW_MDIO_USER_INT_MASKED_REG is shown in Figure 7-220 and described in Table 7-452.

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MDIO User Interrupt Masked Register

Table 7-451.
CPSW_MDIO_USER_INT_MASKED_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F24h

Figure 7-220. CPSW_MDIO_USER_INT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-452. CPSW_MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKED	R/W	0h	Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1h. Writing a 1h will clear the interrupt and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the CPSW_MDIO_USER_INT_MASKED_REG [1-0] USERINTMASKED bits to a 1h. This mode may be used for test purposes.

7.6.11 CPSW_MDIO_USER_INT_MASK_SET_REG Register (Offset = F28h) [reset = X]

CPSW_MDIO_USER_INT_MASK_SET_REG is shown in [Figure 7-221](#) and described in [Table 7-454](#).

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MDIO User Interrupt Mask Set Register

Table 7-453.
CPSW_MDIO_USER_INT_MASK_SET_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F28h

Figure 7-221. CPSW_MDIO_USER_INT_MASK_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKSET	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-454. CPSW_MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKSET	R/W	0h	MDIO user interrupt mask set for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0h. Writing a 0h to this register has no effect.

7.6.12 CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = F2Ch) [reset = X]

CPSW_MDIO_USER_INT_MASK_CLEAR_REG is shown in [Figure 7-222](#) and described in [Table 7-456](#).

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MDIO User Interrupt Mask Clear Register

Table 7-455.
CPSW_MDIO_USER_INT_MASK_CLEAR_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F2Ch

Figure 7-222. CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-456. CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKCLR	R/W	0h	MDIO user command complete interrupt mask clear for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0h to this register has no effect.

7.6.13 CPSW_MDIO_MANUAL_IF_REG Register (Offset = F30h) [reset = X]

CPSW_MDIO_MANUAL_IF_REG is shown in [Figure 7-223](#) and described in [Table 7-458](#).

Return to [Summary Table](#).

MDIO Manual Interface Register

Table 7-457. CPSW_MDIO_MANUAL_IF_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F30h

Figure 7-223. CPSW_MDIO_MANUAL_IF_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
R/W-X					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-458. CPSW_MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output. This value is the MDCLK_O output value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
1	MDIO_OE	R/W	0h	MDIO Output Enable. This value is inverted and output on the MDIO_OE_N output when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
0	MDIO_PIN	R/W	0h	MDIO_Pin Value. This is the external MDIO data pin value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted '1'. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted '1' and MDIO_PIN is written with a 1h then MDIO_PIN should read a 1h if there are no external devices pulling the MDIO data line low.

7.6.14 CPSW_MDIO_POLL_REG Register (Offset = F34h) [reset = X]

CPSW_MDIO_POLL_REG is shown in Figure 7-224 and described in Table 7-460.

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MDIO Poll Register

Table 7-459. CPSW_MDIO_POLL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F34h

Figure 7-224. CPSW_MDIO_POLL_REG Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANG EMODE	RESERVED					
R/W-0h	R/W-0h	R/W-X					
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
IPG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-460. CPSW_MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	MDIO Manual Mode. When set 1h, the MDIO pins are directly controlled by software through the bits in the CPSW_MDIO_MANUAL_IF_REG register
30	STATECHANGEMODE	R/W	0h	MDIO State Change Mode. When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations.
29-8	RESERVED	R/W	X	
7-0	IPG	R/W	0h	Polling Inter Packet Gap Value. This value is the number of MDCLK_O clocks between each poll when polling is enabled.

7.6.15 CPSW_MDIO_POLL_EN_REG Register (Offset = F38h) [reset = FFFFFFFFh]

CPSW_MDIO_POLL_EN_REG is shown in [Figure 7-225](#) and described in [Table 7-462](#).

Return to [Summary Table](#).

MDIO Poll Enable Register

Table 7-461. CPSW_MDIO_POLL_EN_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F38h

Figure 7-225. CPSW_MDIO_POLL_EN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLL_EN																															
R/W-FFFFFFFh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-462. CPSW_MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	POLL_EN	R/W	FFFFFFFh	MDIO Poll Enable. When set, the bit indicates that the associated PHY will be included in polling operations. When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set (regardless of the value of the preamble disable bit ([20] PREAMBLE) in the CPSW_MDIO_CONTROL_REG register. However, there does not have to be a PHY at address 31.

7.6.16 CPSW_MDIO_CLAUS45_REG Register (Offset = F3Ch) [reset = 0h]

CPSW_MDIO_CLAUS45_REG is shown in [Figure 7-226](#) and described in [Table 7-464](#).

Return to [Summary Table](#).

MDIO Clause45 Enable Register

Table 7-463. CPSW_MDIO_CLAUS45_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F3Ch

Figure 7-226. CPSW_MDIO_CLAUS45_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAUSE45																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-464. CPSW_MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAUSE45	R/W	0h	MDIO clause 45 mode. When a clause45 bit is cleared 0h, the PHY associated with the clause45 bit is operating in the clause 22 mode. When set 1h, the PHY associated with the clause45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on.

7.6.17 CPSW_MDIO_USER_ADDR0_REG Register (Offset = F40h) [reset = X]

CPSW_MDIO_USER_ADDR0_REG is shown in [Figure 7-227](#) and described in [Table 7-466](#).

Return to [Summary Table](#).

MDIO Address 0 Register

Table 7-465. CPSW_MDIO_USER_ADDR0_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F40h

Figure 7-227. CPSW_MDIO_USER_ADDR0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																USER_ADDR0															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-466. CPSW_MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	USER_ADDR0	R/W	0h	MDIO User Address 0. In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIOUserAccess0 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess0 access.

7.6.18 CPSW_MDIO_USER_ADDR1_REG Register (Offset = F44h) [reset = X]

CPSW_MDIO_USER_ADDR1_REG is shown in Figure 7-228 and described in Table 7-468.

Return to [Summary Table](#).

MDIO Address 1 Register

Table 7-467. CPSW_MDIO_USER_ADDR1_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F44h

Figure 7-228. CPSW_MDIO_USER_ADDR1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																USER_ADDR1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-468. CPSW_MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	USER_ADDR1	R/W	0h	MDIO User Address 1. In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIOUserAccess1 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess1 access.

7.6.19 CPSW_MDIO_USER_ACCESS_REG_k Register (Offset = F80h + formula) [reset = X]

CPSW_MDIO_USER_ACCESS_REG_k is shown in Figure 7-229 and described in Table 7-470.

Return to [Summary Table](#).

MDIO User Access Register

Offset = F80h + (k * 8h); where k = 0h to 1h

Table 7-469. CPSW_MDIO_USER_ACCESS_REG_k Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F80h

Figure 7-229. CPSW_MDIO_USER_ACCESS_REG_k Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W-0h	R/W-0h	R/W-0h	R/W-X			R/W-0h	
23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
DATA							
R/W-0h							
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-470. CPSW_MDIO_USER_ACCESS_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go. Writing a 1h to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0h to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1h. If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1h causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28-26	RESERVED	R/W	X	
25-21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.
20-16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.

Table 7-470. CPSW_MDIO_USER_ACCESS_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

7.6.20 CPSW_MDIO_USER_PHY_SEL_REG_k Register (Offset = F84h + formula) [reset = X]

CPSW_MDIO_USER_PHY_SEL_REG_k is shown in Figure 7-230 and described in Table 7-472.

Return to [Summary Table](#).

MDIO User PHY Select Register

Offset = F84h + (k * 8h); where k = 0h to 1h

Table 7-471. CPSW_MDIO_USER_PHY_SEL_REG_k Instances

Instance	Physical Address
MCU_CPSW0_NUSS_MDIO	4600 0F84h

Figure 7-230. CPSW_MDIO_USER_PHY_SEL_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W-0h	R/W-0h	R/W-X	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-472. CPSW_MDIO_USER_PHY_SEL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7	LINKSEL	R/W	0h	Link status determination select. Set to 1h to determine link status using the MLINK pin. Default value is 0h which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1h to enable link change status interrupts for PHY address specified in [4-0] PHYADR_MON. Link change interrupts are disabled if this bit is set to 0h.
5	RESERVED	R/W	X	
4-0	PHYADR_MON	R/W	0h	PHY address whose link status is monitored.

7.7 MCU_CPSW0_NUSS Subsystem (SS) Registers

Table 7-474 lists the memory-mapped registers for the MCU_CPSW0_NUSS SS registers. All register offset addresses not listed in Table 7-474 should be considered as reserved locations and the register contents should not be modified.

Table 7-473. MCU_CPSW0_NUSS SS Instances

Instance	Base Address
MCU_CPSW0_NUSS_SS	4600 0000h

Table 7-474. MCU_CPSW0_NUSS SS Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_SS Physical Address
0h	CPSW_SS_CPSW_NUSS_IDVER_REG	ID Version Register	4600 0000h
4h	CPSW_SS_SYNC_COUNT_REG	SyncE Count Register	4600 0004h
8h	CPSW_SS_SYNC_MUX_REG	SyncE Mux Select Register	4600 0008h
Ch	CPSW_SS_CONTROL_REG	Subsystem Control Register	4600 000Ch
30h	CPSW_SS_RGMII_STATUS_REG	RGMII Port 1 Register	4600 0018h
1Ch	CPSW_SS_SUBSYSTEM_STATUS_REG	Subsystem Status Register	4600 001Ch

7.7.1 CPSW_SS_CPSW_NUSS_IDVER_REG Register (Offset = 0h) [reset = 6BA00101h]

CPSW_SS_CPSW_NUSS_IDVER_REG is shown in [Figure 7-231](#) and described in [Table 7-476](#).

Return to [Summary Table](#).

CPSW_NUSS ID Version Register

Table 7-475. CPSW_SS_CPSW_NUSS_IDVER_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SS	4600 0000h

Figure 7-231. CPSW_SS_CPSW_NUSS_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDENT															
R-6BA0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER					MINOR_VER					
R-0h					R-1h					R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 7-476. CPSW_SS_CPSW_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	IDENT	R	6BA0h	Identification value
15-11	RTL_VER	R	0h	RTL version value
10-8	MAJOR_VER	R	1h	Major version value
7-0	MINOR_VER	R	1h	Minor version value

7.7.2 CPSW_SS_SYNCE_COUNT_REG Register (Offset = 4h) [reset = 0h]

CPSW_SS_SYNCE_COUNT_REG is shown in [Figure 7-232](#) and described in [Table 7-478](#).

Return to [Summary Table](#).

CPSW_NUSS SYNCE Count Register

**Table 7-477. CPSW_SS_SYNCE_COUNT_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SS	4600 0004h

Figure 7-232. CPSW_SS_SYNCE_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNCE_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-478. CPSW_SS_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNCE_CNT	R/W	0h	Sync E Count Value

7.7.3 CPSW_SS_SYNCE_MUX_REG Register (Offset = 8h) [reset = X]

CPSW_SS_SYNCE_MUX_REG is shown in [Figure 7-233](#) and described in [Table 7-480](#).

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CPSW_NUSS Synce Mux Register

**Table 7-479. CPSW_SS_SYNCE_MUX_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SS	4600 0008h

Figure 7-233. CPSW_SS_SYNCE_MUX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SYNCE_SEL					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-480. CPSW_SS_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	SYNCE_SEL	R/W	0h	Sync E Select Value

7.7.4 CPSW_SS_CONTROL_REG Register (Offset = Ch) [reset = X]

CPSW_SS_CONTROL_REG is shown in [Figure 7-234](#) and described in [Table 7-482](#).

Return to [Summary Table](#).

CPSW_NUSS Control Register

Table 7-481. CPSW_SS_CONTROL_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SS	4600 000Ch

Figure 7-234. CPSW_SS_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						EEE_PHY_ONL Y	EEE_EN
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-482. CPSW_SS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	EEE_PHY_ONLY	R/W	0h	Energy Efficient Enable Phy Only Mode: 0=The low power indicate state includes gating off the CPPI_GCLK to the CPSW, 1=The low power indicate state does not gate the clock to the CPSW
0	EEE_EN	R/W	0h	Energy Efficient Ethernet Enable: 0=EEE is disabled, 1=EEE is enabled

7.7.5 CPSW_SS_RGMII_STATUS_REG Register (Offset = 30h) [reset = X]

CPSW_SS_RGMII_STATUS_REG is shown in [Figure 7-235](#) and described in [Table 7-484](#).

Return to [Summary Table](#).

CPSW_NUSS RGMII Status Register

**Table 7-483. CPSW_SS_RGMII_STATUS_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SS	4600 0018h

Figure 7-235. CPSW_SS_RGMII_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-484. CPSW_SS_RGMII_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	Rgmii full duplex: 0=Half-duplex, 1=Full-duplex
2-1	SPEED	R	0h	Rgmii speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	R	0h	Rgmii link indicator: 0=Link is down, 1=Link is up

7.7.6 CPSW_SS_SUBSYSTEM_STATUS_REG Register (Offset = 1Ch) [reset = X]

CPSW_SS_SUBSYSTEM_STATUS_REG is shown in [Figure 7-236](#) and described in [Table 7-486](#).

Return to [Summary Table](#).

CPSW_NUSS Status Register

Table 7-485.
CPSW_SS_SUBSYSTEM_STATUS_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SS	4600 001Ch

Figure 7-236. CPSW_SS_SUBSYSTEM_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							EEE_CLKSTOP_ACK
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-486. CPSW_SS_SUBSYSTEM_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	EEE_CLKSTOP_ACK	R	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

7.8 MCU_CPSW0_RAM Registers

Table 7-488 lists the memory-mapped registers for the MCU_CPSW0_RAM. All register offset addresses not listed in Table 7-488 should be considered as reserved locations and the register contents should not be modified.

Table 7-487. MCU_CPSW0_RAM Instances

Instance	Base Address
MCU_CPSW0_NUSS_RAM	4600 0000h

Table 7-488. MCU_CPSW0_RAM Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_RAM Physical Address
00032000h + formula	CPSW_FETCH_LOC_y	RAM Location Register	4603 2000h + formula

7.8.1 CPSW_FETCH_LOC_y Register (Offset = 00032000h + formula) [reset = X]

CPSW_FETCH_LOC_y is shown in [Figure 7-237](#) and described in [Table 7-490](#).

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These are the RAM locations for one Ethernet port.

Offset = 00032000h + (y * 4h); where y = 0h to 7Fh

Table 7-489. CPSW_FETCH_LOC_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_RAM	4603 2000h + formula

Figure 7-237. FETCH_LOC_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											LOC																				
R/W-X											R/W-0h																				

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-490. CPSW_FETCH_LOC_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-0	LOC	R/W	0h	RAM Location

7.9 MCU_CPSW0_SGMII Registers

Table 7-492 lists the memory-mapped registers for the MCU_CPSW0_SGMII. All register offset addresses not listed in Table 7-492 should be considered as reserved locations and the register contents should not be modified.

Note

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-491. MCU_CPSW0_SGMII Instances

Instance	Base Address
MCU_CPSW0_NUSS_SGMII	4600 0000h

Table 7-492. MCU_CPSW0_SGMII Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_SGMII Physical Address
100h	CPSW_SGMII_IDVER_REG	Identification and Version Register	4600 0100h
104h	CPSW_SGMII_SOFT_RESET_REG	Software Reset Register	4600 0104h
110h	CPSW_SGMII_CONTROL_REG	Control Register	4600 0110h
114h	CPSW_SGMII_STATUS_REG	Status Register	4600 0114h
118h	CPSW_SGMII_MR_ADV_ABILITY_REG	Advertised Ability Register	4600 0118h
11Ch	CPSW_SGMII_MR_NP_TX_REG	Next Page Transmit Register	4600 011Ch
120h	CPSW_SGMII_MR_LP_ADV_ABILITY_REG	Link Partner Advertised Ability Register	4600 0120h
124h	CPSW_SGMII_MR_LP_NP_RX_REG	Link Partner Next Page Received Register	4600 0124h
130h	CPSW_SGMII_TX_CFG_REG	CPSSGMII Transmit Config Register	4600 0130h
134h	CPSW_SGMII_RX_CFG_REG	CPSSGMII Receive Config Register	4600 0134h
138h	CPSW_SGMII_AUX_CFG_REG	CPSSGMII Auxiliary Configuration Register	4600 0138h
140h	CPSW_SGMII_DIAG_CLEAR_REG	Diagnostics Clear Register	4600 0140h
144h	CPSW_SGMII_DIAG_CONTROL_REG	Diagnostics Control Register	4600 0144h
148h	CPSW_SGMII_DIAG_STATUS_REG	Diagnostics Status Register	4600 0148h

7.9.1 CPSW_SGMII_IDVER_REG Register (Offset = 100h) [reset = 4EC21102h]

CPSW_SGMII_IDVER_REG is shown in [Figure 7-238](#) and described in [Table 7-494](#).

Return to [Summary Table](#).

SGMII IDVER register

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-493. CPSW_SGMII_IDVER_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0100h

Figure 7-238. CPSW_SGMII_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R-4EC2h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER					MINOR_VER					
R-2h					R-1h					R-2h					

LEGEND: R = Read Only; -n = value after reset

Table 7-494. CPSW_SGMII_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_IDENT	R	4EC2h	Module value
15-11	RTL_VER	R	2h	RTL version value
10-8	MAJOR_VER	R	1h	Major version value
7-0	MINOR_VER	R	2h	Minor version value

7.9.2 CPSW_SGMII_SOFT_RESET_REG Register (Offset = 104h) [reset = X]

CPSW_SGMII_SOFT_RESET_REG is shown in [Figure 7-239](#) and described in [Table 7-496](#).

Return to [Summary Table](#).

SGMII Soft Reset Register

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-495. CPSW_SGMII_SOFT_RESET_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0104h

Figure 7-239. CPSW_SGMII_SOFT_RESET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RT_SOFT_RESET	SOFT_RESET
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-496. CPSW_SGMII_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	RT_SOFT_RESET	R/W	0h	Transmit and Receive Software Reset. Write 0h = The reset condition is removed. Write 1h = Causes the CPSGMII transmit and receive logic to be in the reset condition (the VBUSP_CLK domain is not reset). This bit is intended to be used when changing between loopback mode and normal mode of operation.
0	SOFT_RESET	R/W	0h	Software Reset. Write 1h = Causes the CPSGMII logic to be reset. Software reset occurs immediately. This bit reads as a zero.

7.9.3 CPSW_SGMII_CONTROL_REG Register (Offset = 110h) [reset = X]

CPSW_SGMII_CONTROL_REG is shown in [Figure 7-240](#) and described in [Table 7-498](#).

Return to [Summary Table](#).

SGMII Control Register

Note: SGMII mode is not supported on the 2-port CPSW module.

**Table 7-497. CPSW_SGMII_CONTROL_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0110h

Figure 7-240. CPSW_SGMII_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	TEST_PAT N_EN	MASTER	LOOPBACK	MR_NP_LOAD ED	FAST_LINK_TI MER	MR_AN_REST ART	MR_AN_ENAB LE
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-498. CPSW_SGMII_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	TEST_PATTERN_EN	R/W	0h	Test Pattern Enable. Force the output of K28.5 on TX_ENC for test purposes. 0h = Operation 1h = Forced K28.5 on transmit output
5	MASTER	R/W	0h	Master Mode. 0h = Slave Mode 1h = Master mode – Set to one for one side of a direct connection. When this bit is set, the control logic uses the CPSW_SGMII_MR_ADV_ABILITY_REG register to determine speed and duplexity instead of the CPSW_SGMII_MR_LP_ADV_ABILITY_REG register. Master mode allows a CPSPGMII direct connection with auto-negotiation or with a forced link.
4	LOOPBACK	R/W	0h	Loopback mode. 0h = Not in internal loopback mode 1h = Internal loopback mode. The transmit clock (TX_CLK) is used for transmit and receive.

Table 7-498. CPSW_SGMII_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MR_NP_LOADED	R/W	0h	Next Page Loaded. Writing 1h to this bit informs the auto-negotiation process that the next page register has been loaded. This bit is cleared by the auto-negotiation state machine before the CPSW_SGMII_STATUS_REG [3] MR_PAGE_RX status bit is set. This bit is not used when the SGMII_MODE input is asserted.
2	FAST_LINK_TIMER	R/W	0h	Fast Link Timer. 0h = The link timer value is 10ms in FIBER mode and 1.6ms in SGMII mode. 1h = The link timer value is 2μs in FIBER and SGMII mode. This is included for test purposes.
1	MR_AN_RESTART	R/W	0h	Auto Negotiation Restart. Writing 1h and then 0h to this bit causes the auto-negotiation process to be restarted.
0	MR_AN_ENABLE	R/W	0h	Auto Negotiation Enable. Writing 1h to this bit enables the auto-negotiation process.

7.9.4 CPSW_SGMII_STATUS_REG Register (Offset = 114h) [reset = X]

CPSW_SGMII_STATUS_REG is shown in [Figure 7-241](#) and described in [Table 7-500](#).

Return to [Summary Table](#).

SGMII Status Register

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-499. CPSW_SGMII_STATUS_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0114h

Figure 7-241. CPSW_SGMII_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED		FIB_SIG_DETE CT	LOCK	MR_PAGE_RX	MR_AN_COMP LETE	AN_ERROR	LINK
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 7-500. CPSW_SGMII_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5	FIB_SIG_DETECT	R	0h	Fiber Signal Detect. This is the FIB_SIG_DETECT input pin.
4	LOCK	R	0h	Lock. This is the LOCK input pin. Indicates that the SERDES PLL is locked.
3	MR_PAGE_RX	R	0h	Next Page Received. This bit is set to one by the auto-negotiation state machine when the next page has been received. This bit is cleared to 0h by a host write of 1h to the [3]MR_NP_LOADED bit in the CPSW_SGMII_CONTROL_REG register. This value is not valid until the lock status bit is ([4] LOCK) asserted.
2	MR_AN_COMPLETE	R	0h	Auto negotiation complete. This value is not valid until the lock status bit is asserted. 0h = Auto-negotiation is not complete 1h = Auto-negotiation is completed.

Table 7-500. CPSW_SGMII_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AN_ERROR	R	0h	Auto negotiation error. For SGMII mode, an auto-negotiation error occurs when halfduplex Gigabit is commanded. For FIBER mode, an auto-negotiation error occurs if both sides cannot be full duplex. This value is not valid until the lock status bit is asserted. 0h = No auto-negotiation error 1h = Auto-negotiation error
0	LINK	R	0h	Link indicator. This value is not valid until the lock status bit is asserted. 0h = Link is not up. 1h = Link is up.

7.9.5 CPSW_SGMII_MR_ADV_ABILITY_REG Register (Offset = 118h) [reset = X]

CPSW_SGMII_MR_ADV_ABILITY_REG is shown in [Figure 7-242](#) and described in [Table 7-502](#).

Return to [Summary Table](#).

SGMII MR Advertized Ability Register

Note: SGMII mode is not supported on the 2-port CPSW module.

**Table 7-501. CPSW_SGMII_MR_ADV_ABILITY_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0118h

Figure 7-242. CPSW_SGMII_MR_ADV_ABILITY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_ADV_ABILITY															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-502. CPSW_SGMII_MR_ADV_ABILITY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MR_ADV_ABILITY	R/W	0h	Advertised Ability. When in FIBER mode, this value corresponds to the [16-1] MR_ADV_ABILITY in the IEEE specification and is loaded into the IEEE specification TX_CONFIG_REG[15:0]. When in SGMII mode, this value corresponds to the TX_CONFIG_REG[15:0] register value in the Serial-GMII specification.

7.9.6 CPSW_SGMII_MR_NP_TX_REG Register (Offset = 11Ch) [reset = X]

CPSW_SGMII_MR_NP_TX_REG is shown in [Figure 7-243](#) and described in [Table 7-504](#).

Return to [Summary Table](#).

SGMII Next Page Transmit Register

Note: SGMII mode is not supported on the 2-port CPSW module.

**Table 7-503. CPSW_SGMII_MR_NP_TX_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 011Ch

Figure 7-243. CPSW_SGMII_MR_NP_TX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_NP_TX															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-504. CPSW_SGMII_MR_NP_TX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MR_NP_TX	R/W	0h	Next Page Transmit. This value corresponds to the [16-1]MR_NP_TX value in the IEEE specification. Next page is used only in FIBER mode.

7.9.7 CPSW_SGMII_MR_LP_ADV_ABILITY_REG Register (Offset = 120h) [reset = X]

CPSW_SGMII_MR_LP_ADV_ABILITY_REG is shown in [Figure 7-244](#) and described in [Table 7-506](#).

Return to [Summary Table](#).

SGMII Link Partner Advertized Ability Register

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-505.
CPSW_SGMII_MR_LP_ADV_ABILITY_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0120h

Figure 7-244. CPSW_SGMII_MR_LP_ADV_ABILITY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR_LP_ADV_ABILITY															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 7-506. CPSW_SGMII_MR_LP_ADV_ABILITY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MR_LP_ADV_ABILITY	R	0h	Link Partner Advertised Ability. Readable when auto-negotiation is complete. When in FIBER mode, this value corresponds to the [16-1] MR_LP_ADV_ABILITY value in the IEEE. When in SGMII mode, this value corresponds to the TX_CONFIG_REG[15-0] register value in the Serial-GMII specification.

7.9.8 CPSW_SGMII_MR_LP_NP_RX_REG Register (Offset = 124h) [reset = X]

CPSW_SGMII_MR_LP_NP_RX_REG is shown in [Figure 7-245](#) and described in [Table 7-508](#).

Return to [Summary Table](#).

SGMII Link Partner Next Page Receive Register

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-507. CPSW_SGMII_MR_LP_NP_RX_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0124h

Figure 7-245. CPSW_SGMII_MR_LP_NP_RX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_LP_NP_RX															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 7-508. CPSW_SGMII_MR_LP_NP_RX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MR_LP_NP_RX	R	0h	Link Partner Next Page Received. Readable when the next page is received. These bits are as defined in the IEEE 802.3 standard. Next page is used only in FIBER mode.

7.9.9 CPSW_SGMII_TX_CFG_REG Register (Offset = 130h) [reset = 0h]

CPSW_SGMII_TX_CFG_REG is shown in [Figure 7-246](#) and described in [Table 7-510](#).

Return to [Summary Table](#).

SGMII Transmit Configuration Register

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-509. CPSW_SGMII_TX_CFG_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0130h

Figure 7-246. CPSW_SGMII_TX_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CFG																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-510. CPSW_SGMII_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CFG	R/W	0h	Transmit configuration register output

7.9.10 CPSW_SGMII_RX_CFG_REG Register (Offset = 134h) [reset = 0h]

CPSW_SGMII_RX_CFG_REG is shown in [Figure 7-247](#) and described in [Table 7-512](#).

Return to [Summary Table](#).

SGMII Receive Configuration Register

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-511. CPSW_SGMII_RX_CFG_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0134h

Figure 7-247. CPSW_SGMII_RX_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CFG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-512. CPSW_SGMII_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CFG	R/W	0h	Receive configuration register output

7.9.11 CPSW_SGMII_AUX_CFG_REG Register (Offset = 138h) [reset = 0h]

CPSW_SGMII_RX_CFG_REG is shown in [Figure 7-248](#) and described in [Table 7-514](#).

Return to [Summary Table](#).

SGMII Auxiliary Configuration Register

Note: SGMII mode is not supported on the 2-port CPSW module.

**Table 7-513. CPSW_SGMII_AUX_CFG_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0138h

Figure 7-248. CPSW_SGMII_AUX_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_CFG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-514. CPSW_SGMII_AUX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	AUX_CFG	R/W	0h	Auxiliary configuration register output

7.9.12 CPSW_SGMII_DIAG_CLEAR_REG Register (Offset = 140h) [reset = X]

CPSW_SGMII_DIAG_CLEAR_REG is shown in Figure 7-249 and described in Table 7-516.

Return to [Summary Table](#).

SGMII Diagnostics Clear Register

Note: SGMII mode is not supported on the 2-port CPSW module.

Table 7-515. CPSW_SGMII_DIAG_CLEAR_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0140h

Figure 7-249. CPSW_SGMII_DIAG_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							DIAG_CLEAR
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-516. CPSW_SGMII_DIAG_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	DIAG_CLEAR	R/W	0h	Diagnostics Clear. Clears all diagnostic status bits when set to one. Some bits may be set back to one immediately following reset. The reset requires several clocks due to synchronizers.

7.9.13 CPSW_SGMII_DIAG_CONTROL_REG Register (Offset = 144h) [reset = X]

CPSW_SGMII_DIAG_CONTROL_REG is shown in [Figure 7-250](#) and described in [Table 7-518](#).

Return to [Summary Table](#).

SGMII Diagnostics Control Register

Note: SGMII mode is not supported on the 2-port CPSW module.

**Table 7-517. CPSW_SGMII_DIAG_CONTROL_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0144h

Figure 7-250. CPSW_SGMII_DIAG_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DIAG_SM_SEL			RESERVED	DIAG_EDGE_SEL		
R/W-X	R/W-0h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-518. CPSW_SGMII_DIAG_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6-4	DIAG_SM_SEL	R/W	0h	Diagnostic Select. Determines which internal diagnostic bits are muxed onto CPSW_SGMII_DIAG_STATUS_REG[15-0] DIAG_STATUS. 0h = Reserved 1h = Diagnostic Hold Signals 2h = Diagnostic Sync Status (sync_sm state machine) 3h = Diagnostic AN Status (amsm state machine) 4h = Diagnostic TXOS Status (txos state machine) 5h = Diagnostic TXCG Status (txcg state machine) 6h = Diagnostic RXSM Status (rxsm state machine lower bits) 7h = Diagnostic RXSM Status (rxsm state machine upper bits)
3-2	RESERVED	R/W	X	
1-0	DIAG_EDGE_SEL	R/W	0h	Diagnostic Hold Signals Edge Select 0h = Diagnostic Hold Signals Level 1h = Diagnostic Hold Signals rising edge detected 2h = Diagnostic Hold Signals falling edge detected 3h = Diagnostic Hold Signals ether (both) edge detected

7.9.14 CPSW_SGMII_DIAG_STATUS_REG Register (Offset = 148h) [reset = X]

CPSW_SGMII_DIAG_STATUS_REG is shown in [Figure 7-251](#) and described in [Table 7-520](#).

Return to [Summary Table](#).

SGMII Diagnostics Status Register

Note: SGMII mode is not supported on the 2-port CPSW module.

**Table 7-519. CPSW_SGMII_DIAG_STATUS_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_SGMII	4600 0148h

Figure 7-251. CPSW_SGMII_DIAG_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DIAG_STATUS															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 7-520. CPSW_SGMII_DIAG_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	DIAG_STATUS	R	0h	Diagnostics status

7.10 MCU_CPSW0_STAT0 Registers

Table 7-522 lists the memory-mapped registers for the MCU_CPSW0_STAT0 (Port 0). All register offset addresses not listed in Table 7-522 should be considered as reserved locations and the register contents should not be modified.

Table 7-521. MCU_CPSW0_STAT0 Instances

Instance	Base Address
MCU_CPSW0_NUSS_STAT0	4600 0000h

Table 7-522. MCU_CPSW0_STAT0 Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_STAT0 Physical Address
0003A000h	CPSW_STAT0_RXGOODFRAMES	Ethernet Port N Total Number of Good Frames Received	4603 A000h
0003A004h	CPSW_STAT0_RXBROADCASTFRAMES	Ethernet Port N Total Number of Good Broadcast Frames Received	4603 A004h
0003A008h	CPSW_STAT0_RXMULTICASTFRAMES	Ethernet Port N Total Number of Good Multicast Frames Received	4603 A008h
0003A010h	CPSW_STAT0_RXCRCERRORS	Ethernet Port N Total Number of CRC Errors Frames Received	4603 A010h
0003A018h	CPSW_STAT0_RXOVERSIZEDFRAMES	Ethernet Port N Total Number of Oversized Frames Received	4603 A018h
0003A020h	CPSW_STAT0_RXUNDERSIZEDFRAMES	Ethernet Port N Total Number of Undersized Frames Received	4603 A020h
0003A024h	CPSW_STAT0_RXFRAGMENTS	Ethernet Port N Fragments Received Register	4603 A024h
0003A028h	CPSW_STAT0_ALE_DROP	Ethernet Port N ALE Drop Register	4603 A028h
0003A02Ch	CPSW_STAT0_ALE_OVERRUN_DROP	Ethernet Port N ALE Overrun Drop Register	4603 A02Ch
0003A030h	CPSW_STAT0_RXOCTETS	Ethernet Port N Total Number of Received Bytes in Good Frames	4603 A030h
0003A034h	CPSW_STAT0_TXGOODFRAMES	Ethernet Port N Good Transmit Frames Register	4603 A034h
0003A038h	CPSW_STAT0_TXBROADCASTFRAMES	Ethernet Port N Broadcast Transmit Frames Register	4603 A038h
0003A03Ch	CPSW_STAT0_TXMULTICASTFRAMES	Ethernet Port N Multicast Transmit Frames Register	4603 A03Ch
0003A064h	CPSW_STAT0_TXOCTETS	Ethernet Port N Tx Octets Register	4603 A064h
0003A068h	CPSW_STAT0_OCTETFRAMES64	Ethernet Port N 64 Octet Frames Register	4603 A068h
0003A06Ch	CPSW_STAT0_OCTETFRAMES65T127	Ethernet Port N 65 to 127 Octet Frames Register	4603 A06Ch
0003A070h	CPSW_STAT0_OCTETFRAMES128T255	Ethernet Port N 128 to 255 Octet Frames Register	4603 A070h
0003A074h	CPSW_STAT0_OCTETFRAMES256T511	Ethernet Port N 256 to 511 Octet Frames Register	4603 A074h
0003A078h	CPSW_STAT0_OCTETFRAMES512T1023	Ethernet Port N 512-pn_rx_maxlen Octet Frames Register	4603 A078h
0003A07Ch	CPSW_STAT0_OCTETFRAMES1024TUP	Ethernet Port N 1023-1518 Octet Frames Register	4603 A07Ch
0003A080h	CPSW_STAT0_NETOCTETS	Ethernet Port N Net Octets Register	4603 A080h
0003A084h	CPSW_STAT0_RX_BOTTOM_OF_FIFO_DROP	Ethernet Port N Receive Bottom of FIFO Drop Register	4603 A084h
0003A088h	CPSW_STAT0_PORTMASK_DROP	Ethernet Port N Portmask Drop Register	4603 A088h
0003A08Ch	CPSW_STAT0_RX_TOP_OF_FIFO_DROP	Ethernet Port N Receive Top of FIFO Drop Register	4603 A08Ch

Table 7-522. MCU_CPSW0_STAT0 Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_NU SS_STAT0 Physical Address
0003A090h	CPSW_STAT0_ALE_RATE_LIMIT_DROP	Ethernet Port N ALE Rate Limit Drop Register	4603 A090h
0003A094h	CPSW_STAT0_ALE_VID_INGRESS_DROP	Ethernet Port N ALE VID Ingress Drop Register	4603 A094h
0003A098h	CPSW_STAT0_ALE_DA_EQ_SA_DROP	Ethernet Port N ALE DA equal SA Drop Register	4603 A098h
0003A09Ch	CPSW_STAT0_ALE_BLOCK_DROP	Ethernet Port N ALE Block Drop Register	4603 A09Ch
0003A0A0h	CPSW_STAT0_ALE_SECURE_DROP	Ethernet Port N ALE Secure Drop Register	4603 A0A0h
0003A0A4h	CPSW_STAT0_ALE_AUTH_DROP	Ethernet Port N ALE Authentication Drop Register	4603 A0A4h
0003A0A8h	CPSW_STAT0_ALE_UNKN_UNI	Ethernet Port N ALE Receive Unknown Unicast Register	4603 A0A8h
0003A0ACh	CPSW_STAT0_ALE_UNKN_UNI_BCNT	Ethernet Port N ALE Receive Unknown Unicast Bytecount Register	4603 A0ACh
0003A0B0h	CPSW_STAT0_ALE_UNKN_MLT	Ethernet Port N ALE Receive Unknown Multicast Register	4603 A0B0h
0003A0B4h	CPSW_STAT0_ALE_UNKN_MLT_BCNT	Ethernet Port N ALE Receive Unknown Multicast Bytecount Register	4603 A0B4h
0003A0B8h	CPSW_STAT0_ALE_UNKN_BRD	Ethernet Port N ALE Receive Unknown Broadcast Register	4603 A0B8h
0003A0BCh	CPSW_STAT0_ALE_UNKN_BRD_BCNT	Ethernet Port N ALE Receive Unknown Broadcast Bytecount Register	4603 A0BCh
0003A0C0h	CPSW_STAT0_ALE_POL_MATCH	Ethernet Port N ALE Policer Matched Register	4603 A0C0h
0003A0C4h	CPSW_STAT0_ALE_POL_MATCH_RED	Ethernet Port N ALE Policer Matched and Condition Red Register	4603 A0C4h
0003A0C8h	CPSW_STAT0_ALE_POL_MATCH_YELLOW	Ethernet Port N ALE Policer Matched and Condition Yellow Register	4603 A0C8h
0003A0CCh	CPSW_STAT0_ALE_MULT_SA_DROP	Enet Port N ALE Multicast Source Address Drop	4603 A0CCh
0003A0D0h	CPSW_STAT0_ALE_DUAL_VLAN_DROP	Enet Port N ALE Dual VLAN Drop	4603 A0D0h
0003A0D4h	CPSW_STAT0_ALE_LEN_ERROR_DROP	Enet Port N ALE IEEE 802.3 Length Error Drop	4603 A0D4h
0003A0D8h	CPSW_STAT0_ALE_IP_NEXT_HDR_DROP	Enet Port N ALE IP Next Header Limit Drop	4603 A0D8h
0003A0DCh	CPSW_STAT0_ALE_IPV4_FRAG_DROP	Enet Port N ALE IPv4 Fragment Drop	4603 A0DCh
0003A140h	CPSW_STAT0_IET_RX_ASSEMBLY_ERROR_REG	Enet Port N IET Received Assembly Error	4603 A140h
0003A144h	CPSW_STAT0_IET_RX_ASSEMBLY_OK_REG	Enet Port N IET Received Assembly OK	4603 A144h
0003A148h	CPSW_STAT0_IET_RX_SMD_ERROR_REG	Enet Port N IET Received SMD Error	4603 A148h
0003A14Ch	CPSW_STAT0_IET_RX_FRAG_REG	Enet Port N IET Received Fragment (IET fragment)	4603 A14Ch
0003A150h	CPSW_STAT0_IET_TX_HOLD_REG	Enet Port N IET Transmit Hold	4603 A150h
0003A154h	CPSW_STAT0_IET_TX_FRAG_REG	Enet Port N IET Transmit Fragment (IET fragment)	4603 A154h
0003A17Ch	CPSW_STAT0_TX_MEMORY_PROTECT_ERROR	Ethernet Port N Transmit Memory Protect CRC Error Register	4603 A17Ch

7.10.1 CPSW_STAT0_RXGOODFRAMES Register (Offset = 0003A000h) [reset = 0h]

CPSW_STAT0_RXGOODFRAMES is shown in [Figure 7-252](#) and described in [Table 7-524](#).

Return to [Summary Table](#).

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Had a length of 64 to SL_RX_MAXLEN[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the RX_ALIGN_CODE_ERRORS and [CPSW_STAT0_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

**Table 7-523. CPSW_STAT0_RXGOODFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A000h

Figure 7-252. CPSW_STAT0_RXGOODFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-524. CPSW_STAT0_RXGOODFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good frames received.

7.10.2 CPSW_STAT0_RXBROADCASTFRAMES Register (Offset = 0003A004h) [reset = 0h]

CPSW_STAT0_RXBROADCASTFRAMES is shown in [Figure 7-253](#) and described in [Table 7-526](#).

Return to [Summary Table](#).

The total number of good broadcast frames received on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address 0xFFFFFFFF
- Had a length of CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the CPSW_STAT0_RXCRCERRORS statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Table 7-525.
CPSW_STAT0_RXBROADCASTFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A004h

Figure 7-253. CPSW_STAT0_RXBROADCASTFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-526. CPSW_STAT0_RXBROADCASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good broadcast frames received.

7.10.3 CPSW_STAT0_RXMULTICASTFRAMES Register (Offset = 0003A008h) [reset = 0h]

CPSW_STAT0_RXMULTICASTFRAMES is shown in [Figure 7-254](#) and described in [Table 7-528](#).

Return to [Summary Table](#).

The total number of good multicast frames received on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than 0xFFFFFFFF
- Had a length of CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the [CPSW_STAT0_RXCRCERRORS](#) statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

**Table 7-527. CPSW_STAT0_RXMULTICASTFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A008h

Figure 7-254. CPSW_STAT0_RXMULTICASTFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-528. CPSW_STAT0_RXMULTICASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good multicast frames received.

7.10.4 CPSW_STAT0_RXCRCERRORS Register (Offset = 0003A010h) [reset = 0h]

CPSW_STAT0_RXCRCERRORS is shown in [Figure 7-255](#) and described in [Table 7-530](#).

Return to [Summary Table](#).

The total number of frames received on the port that experienced a CRC error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to CPSW0_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no code/align error,
- Had a CRC error Overruns have no effect upon this statistic.

A CRC error is defined to be:

- A frame containing an even number of nibbles
- Failing the Frame Check Sequence test.

**Table 7-529. CPSW_STAT0_RXCRCERRORS
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A010h

Figure 7-255. CPSW_STAT0_RXCRCERRORS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-530. CPSW_STAT0_RXCRCERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of CRC errors frames received.

7.10.5 CPSW_STAT0_RXOVERSIZEDFRAMES Register (Offset = 0003A018h) [reset = 0h]

CPSW_STAT0_RXOVERSIZEDFRAMES is shown in [Figure 7-256](#) and described in [Table 7-532](#).

Return to [Summary Table](#).

The total number of oversized frames received on the port. An oversized frame is defined to be:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than [CPSW_P0_RX_MAXLEN_REG](#)[13-0] RX_MAXLEN in bytes
- Had no CRC error, alignment error or code error

See the [CPSW_STAT0_RXCRCERRORS](#) statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

**Table 7-531. CPSW_STAT0_RXOVERSIZEDFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A018h

Figure 7-256. CPSW_STAT0_RXOVERSIZEDFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-532. CPSW_STAT0_RXOVERSIZEDFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of oversized frames received.

7.10.6 CPSW_STAT0_RXUNDERSIZEDFRAMES Register (Offset = 0003A020h) [reset = 0h]

CPSW_STAT0_RXUNDERSIZEDFRAMES is shown in [Figure 7-257](#) and described in [Table 7-534](#).

Return to [Summary Table](#).

The total number of undersized frames received on the port. An undersized frame is defined to be:

- Was any data frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was less than 64 octets long
- Had no CRC error, alignment error or code error

See the [CPSW_STAT0_RXCRCERRORS](#) statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Table 7-533.
CPSW_STAT0_RXUNDERSIZEDFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A020h

Figure 7-257. CPSW_STAT0_RXUNDERSIZEDFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-534. CPSW_STAT0_RXUNDERSIZEDFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of undersized frames received.

7.10.7 CPSW_STAT0_RXFRAGMENTS Register (Offset = 0003A024h) [reset = 0h]

CPSW_STAT0_RXFRAGMENTS is shown in [Figure 7-258](#) and described in [Table 7-536](#).

Return to [Summary Table](#).

The total number of frame fragments received on the port. A frame fragment is defined to be:

- Any data frame (address matching does not matter)
- Less than 64 bytes long
- Having a CRC error, an alignment error, or a code error
- Not the result of a collision caused by half duplex, collision based flow control

See the [CPSW_STAT0_RXCRCERRORS](#) statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

**Table 7-535. CPSW_STAT0_RXFRAGMENTS
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A024h

Figure 7-258. CPSW_STAT0_RXFRAGMENTS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-536. CPSW_STAT0_RXFRAGMENTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of fragmented frames received.

7.10.8 CPSW_STAT0_ALE_DROP Register (Offset = 0003A028h) [reset = 0h]

CPSW_STAT0_ALE_DROP is shown in [Figure 7-259](#) and described in [Table 7-538](#).

Return to [Summary Table](#).

Total number of frames dropped by the ALE.

Table 7-537. CPSW_STAT0_ALE_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A028h

Figure 7-259. CPSW_STAT0_ALE_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-538. CPSW_STAT0_ALE_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames dropped by the ALE.

7.10.9 CPSW_STAT0_ALE_OVERRUN_DROP Register (Offset = 0003A02Ch) [reset = 0h]

CPSW_STAT0_ALE_OVERRUN_DROP is shown in [Figure 7-260](#) and described in [Table 7-540](#).

Return to [Summary Table](#).

Total number of overrun frames dropped by the ALE.

Table 7-539. CPSW_STAT0_ALE_OVERRUN_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A02Ch

Figure 7-260. CPSW_STAT0_ALE_OVERRUN_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-540. CPSW_STAT0_ALE_OVERRUN_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE.

7.10.10 CPSW_STAT0_RXOCTETS Register (Offset = 0003A030h) [reset = 0h]

CPSW_STAT0_RXOCTETS is shown in [Figure 7-261](#) and described in [Table 7-542](#).

Return to [Summary Table](#).

The total number of bytes in all good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Of length 64 to [CPSW_P0_RX_MAXLEN_REG](#)[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the [CPSW_STAT0_RXCRCERRORS](#) statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Table 7-541. CPSW_STAT0_RXOCTETS Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A030h

Figure 7-261. CPSW_STAT0_RXOCTETS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-542. CPSW_STAT0_RXOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of received bytes in good frames

7.10.11 CPSW_STAT0_TXGOODFRAMES Register (Offset = 0003A034h) [reset = 0h]

CPSW_STAT0_TXGOODFRAMES is shown in Figure 7-262 and described in Table 7-544.

Return to [Summary Table](#).

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

**Table 7-543. CPSW_STAT0_TXGOODFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A034h

Figure 7-262. CPSW_STAT0_TXGOODFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-544. CPSW_STAT0_TXGOODFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good frames transmitted

7.10.12 CPSW_STAT0_TXBROADCASTFRAMES Register (Offset = 0003A038h) [reset = 0h]

CPSW_STAT0_TXBROADCASTFRAMES is shown in [Figure 7-263](#) and described in [Table 7-546](#).

Return to [Summary Table](#).

The total number of good broadcast frames received on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address 0xFFFFFFFF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

Table 7-545.
CPSW_STAT0_TXBROADCASTFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A038h

Figure 7-263. CPSW_STAT0_TXBROADCASTFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-546. CPSW_STAT0_TXBROADCASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good broadcast frames transmitted.

7.10.13 CPSW_STAT0_TXMULTICASTFRAMES Register (Offset = 0003A03Ch) [reset = 0h]

CPSW_STAT0_TXMULTICASTFRAMES is shown in [Figure 7-264](#) and described in [Table 7-548](#).

Return to [Summary Table](#).

The total number of good multicast frames received on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than 0xFFFFFFFF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

**Table 7-547. CPSW_STAT0_TXMULTICASTFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A03Ch

Figure 7-264. CPSW_STAT0_TXMULTICASTFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-548. CPSW_STAT0_TXMULTICASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good multicast frames transmitted.

7.10.14 CPSW_STAT0_TXOCTETS Register (Offset = 0003A064h) [reset = 0h]

CPSW_STAT0_TXOCTETS is shown in Figure 7-265 and described in Table 7-550.

Return to [Summary Table](#).

The total number of bytes in all good frames transmitted on the port. A good frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Was any size
- Had no late or excessive collisions, no carrier loss and no underrun.

Table 7-549. CPSW_STAT0_TXOCTETS Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A064h

Figure 7-265. CPSW_STAT0_TXOCTETS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-550. CPSW_STAT0_TXOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

7.10.15 CPSW_STAT0_OCTETFRAMES64 Register (Offset = 0003A068h) [reset = 0h]

CPSW_STAT0_OCTETFRAMES64 is shown in [Figure 7-266](#) and described in [Table 7-552](#).

Return to [Summary Table](#).

The total number of 64-byte frames received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was exactly 64 bytes long. (If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic).

CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

**Table 7-551. CPSW_STAT0_OCTETFRAMES64
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A068h

Figure 7-266. CPSW_STAT0_OCTETFRAMES64 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-552. CPSW_STAT0_OCTETFRAMES64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

7.10.16 CPSW_STAT0_OCTETFRAMES65T127 Register (Offset = 0003A06Ch) [reset = 0h]

CPSW_STAT0_OCTETFRAMES65T127 is shown in [Figure 7-267](#) and described in [Table 7-554](#).

Return to [Summary Table](#).

The total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 65 to 127 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

**Table 7-553. CPSW_STAT0_OCTETFRAMES65T127
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A06Ch

Figure 7-267. CPSW_STAT0_OCTETFRAMES65T127 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-554. CPSW_STAT0_OCTETFRAMES65T127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

7.10.17 CPSW_STAT0_OCTETFRAMES128T255 Register (Offset = 0003A070h) [reset = 0h]

CPSW_STAT0_OCTETFRAMES128T255 is shown in [Figure 7-268](#) and described in [Table 7-556](#).

Return to [Summary Table](#).

The total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 128 to 255 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

**Table 7-555. CPSW_STAT0_OCTETFRAMES128T255
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A070h

Figure 7-268. CPSW_STAT0_OCTETFRAMES128T255 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-556. CPSW_STAT0_OCTETFRAMES128T255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

7.10.18 CPSW_STAT0_OCTETFRAMES256T511 Register (Offset = 0003A074h) [reset = 0h]

CPSW_STAT0_OCTETFRAMES256T511 is shown in [Figure 7-269](#) and described in [Table 7-558](#).

Return to [Summary Table](#).

The total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 256 to 511 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Table 7-557. CPSW_STAT0_OCTETFRAMES256T511 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A074h

Figure 7-269. CPSW_STAT0_OCTETFRAMES256T511 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-558. CPSW_STAT0_OCTETFRAMES256T511 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted.

7.10.19 CPSW_STAT0_OCTETFRAMES512T1023 Register (Offset = 0003A078h) [reset = 0h]

CPSW_STAT0_OCTETFRAMES512T1023 is shown in [Figure 7-270](#) and described in [Table 7-560](#).

Return to [Summary Table](#).

The total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 512 to 1023 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Table 7-559.

CPSW_STAT0_OCTETFRAMES512T1023 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A078h

Figure 7-270. CPSW_STAT0_OCTETFRAMES512T1023 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-560. CPSW_STAT0_OCTETFRAMES512T1023 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted.

7.10.20 CPSW_STAT0_OCTETFRAMES1024TUP Register (Offset = 0003A07Ch) [reset = 0h]

CPSW_STAT0_OCTETFRAMES1024TUP is shown in [Figure 7-271](#) and described in [Table 7-562](#).

Return to [Summary Table](#).

The total number of frames of size 1024 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes for receive or 1024 up for transmit on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
 - Did not experience late collisions, excessive collisions, or carrier sense error
 - Was 1024 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes long on receive, or any size on transmit
- CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

**Table 7-561. CPSW_STAT0_OCTETFRAMES1024TUP
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A07Ch

Figure 7-271. CPSW_STAT0_OCTETFRAMES1024TUP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-562. CPSW_STAT0_OCTETFRAMES1024TUP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 1024 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes received and 1024 bytes or greater transmitted.

7.10.21 CPSW_STAT0_NETOCTETS Register (Offset = 0003A080h) [reset = 0h]

CPSW_STAT0_NETOCTETS is shown in Figure 7-272 and described in Table 7-564.

Return to [Summary Table](#).

The total number of bytes of frame data received and transmitted on the port. Each frame counted:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address (address match does not matter)
- Any length (including less than 64 bytes and greater than CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes)

Also counted in this statistic is:

- Every byte transmitted before a carrier- loss was experienced
- Every byte transmitted before each collision was experienced, (i.e. multiple retries are counted each time)
- Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting)

Error conditions such as alignment errors, CRC errors, code errors, overruns and underruns do not affect the recording of bytes by this statistic. The objective of this statistic is to give a reasonable indication of ethernet utilization

Table 7-563. CPSW_STAT0_NETOCTETS Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A080h

Figure 7-272. CPSW_STAT0_NETOCTETS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-564. CPSW_STAT0_NETOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of bytes received and transmitted

7.10.22 CPSW_STAT0_RX_BOTTOM_OF_FIFO_DROP Register (Offset = 0003A084h) [reset = 0h]

CPSW_STAT0_RX_BOTTOM_OF_FIFO_DROP is shown in [Figure 7-273](#) and described in [Table 7-566](#).

Return to [Summary Table](#).

Receive Bottom of FIFO Drop.

Table 7-565.
CPSW_STAT0_RX_BOTTOM_OF_FIFO_DROP
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A084h

Figure 7-273. CPSW_STAT0_RX_BOTTOM_OF_FIFO_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-566. CPSW_STAT0_RX_BOTTOM_OF_FIFO_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Receive Bottom of FIFO Drop.

7.10.23 CPSW_STAT0_PORTMASK_DROP Register (Offset = 0003A088h) [reset = 0h]

CPSW_STAT0_PORTMASK_DROP is shown in [Figure 7-274](#) and described in [Table 7-568](#).

Return to [Summary Table](#).

Total number of dropped frames received due to portmask.

Table 7-567. CPSW_STAT0_PORTMASK_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A088h

Figure 7-274. CPSW_STAT0_PORTMASK_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-568. CPSW_STAT0_PORTMASK_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames received due to portmask.

7.10.24 CPSW_STAT0_RX_TOP_OF_FIFO_DROP Register (Offset = 0003A08Ch) [reset = 0h]

CPSW_STAT0_RX_TOP_OF_FIFO_DROP is shown in [Figure 7-275](#) and described in [Table 7-570](#).

Return to [Summary Table](#).

Receive Top of FIFO Drop.

Table 7-569.
CPSW_STAT0_RX_TOP_OF_FIFO_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A08Ch

Figure 7-275. CPSW_STAT0_RX_TOP_OF_FIFO_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-570. CPSW_STAT0_RX_TOP_OF_FIFO_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Receive Top of FIFO Drop.

7.10.25 CPSW_STAT0_ALE_RATE_LIMIT_DROP Register (Offset = 0003A090h) [reset = 0h]

CPSW_STAT0_ALE_RATE_LIMIT_DROP is shown in [Figure 7-276](#) and described in [Table 7-572](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Rate Limiting.

Table 7-571. CPSW_STAT0_ALE_RATE_LIMIT_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A090h

Figure 7-276. CPSW_STAT0_ALE_RATE_LIMIT_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-572. CPSW_STAT0_ALE_RATE_LIMIT_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting.

7.10.26 CPSW_STAT0_ALE_VID_INGRESS_DROP Register (Offset = 0003A094h) [reset = 0h]

CPSW_STAT0_ALE_VID_INGRESS_DROP is shown in [Figure 7-277](#) and described in [Table 7-574](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE VID Ingress.

Table 7-573.
CPSW_STAT0_ALE_VID_INGRESS_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A094h

Figure 7-277. CPSW_STAT0_ALE_VID_INGRESS_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-574. CPSW_STAT0_ALE_VID_INGRESS_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress.

7.10.27 CPSW_STAT0_ALE_DA_EQ_SA_DROP Register (Offset = 0003A098h) [reset = 0h]

CPSW_STAT0_ALE_DA_EQ_SA_DROP is shown in [Figure 7-278](#) and described in [Table 7-576](#).

Return to [Summary Table](#).

Total number of dropped frames due to DA=SA.

Table 7-575. CPSW_STAT0_ALE_DA_EQ_SA_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A098h

Figure 7-278. CPSW_STAT0_ALE_DA_EQ_SA_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-576. CPSW_STAT0_ALE_DA_EQ_SA_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA.

7.10.28 CPSW_STAT0_ALE_BLOCK_DROP Register (Offset = 0003A09Ch) [reset = 0h]

CPSW_STAT0_ALE_BLOCK_DROP is shown in [Figure 7-279](#) and described in [Table 7-578](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Block Mode.

Table 7-577. CPSW_STAT0_ALE_BLOCK_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A09Ch

Figure 7-279. CPSW_STAT0_ALE_BLOCK_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-578. CPSW_STAT0_ALE_BLOCK_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode.

7.10.29 CPSW_STAT0_ALE_SECURE_DROP Register (Offset = 0003A0A0h) [reset = 0h]

CPSW_STAT0_ALE_SECURE_DROP is shown in [Figure 7-280](#) and described in [Table 7-580](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Secure Mode.

**Table 7-579. CPSW_STAT0_ALE_SECURE_DROP
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0A0h

Figure 7-280. CPSW_STAT0_ALE_SECURE_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-580. CPSW_STAT0_ALE_SECURE_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode.

7.10.30 CPSW_STAT0_ALE_AUTH_DROP Register (Offset = 0003A0A4h) [reset = 0h]

CPSW_STAT0_ALE_AUTH_DROP is shown in [Figure 7-281](#) and described in [Table 7-582](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Authentication.

Table 7-581. CPSW_STAT0_ALE_AUTH_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0A4h

Figure 7-281. CPSW_STAT0_ALE_AUTH_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-582. CPSW_STAT0_ALE_AUTH_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication.

7.10.31 CPSW_STAT0_ALE_UNKN_UNI Register (Offset = 0003A0A8h) [reset = 0h]

CPSW_STAT0_ALE_UNKN_UNI is shown in [Figure 7-282](#) and described in [Table 7-584](#).

Return to [Summary Table](#).

ALE Receive Unknown Unicast.

**Table 7-583. CPSW_STAT0_ALE_UNKN_UNI
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0A8h

Figure 7-282. CPSW_STAT0_ALE_UNKN_UNI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-584. CPSW_STAT0_ALE_UNKN_UNI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Unicast.

7.10.32 CPSW_STAT0_ALE_UNKN_UNI_BCNT Register (Offset = 0003A0ACh) [reset = 0h]

CPSW_STAT0_ALE_UNKN_UNI_BCNT is shown in Figure 7-283 and described in Table 7-586.

Return to [Summary Table](#).

ALE Receive Unknown Unicast Bytecount.

Table 7-585. CPSW_STAT0_ALE_UNKN_UNI_BCNT Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0ACh

Figure 7-283. CPSW_STAT0_ALE_UNKN_UNI_BCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-586. CPSW_STAT0_ALE_UNKN_UNI_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount.

7.10.33 CPSW_STAT0_ALE_UNKN_MLT Register (Offset = 0003A0B0h) [reset = 0h]

CPSW_STAT0_ALE_UNKN_MLT is shown in [Figure 7-284](#) and described in [Table 7-588](#).

Return to [Summary Table](#).

ALE Receive Unknown Multicast.

**Table 7-587. CPSW_STAT0_ALE_UNKN_MLT
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0B0h

Figure 7-284. CPSW_STAT0_ALE_UNKN_MLT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-588. CPSW_STAT0_ALE_UNKN_MLT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Multicast.

7.10.34 CPSW_STAT0_ALE_UNKN_MLT_BCNT Register (Offset = 0003A0B4h) [reset = 0h]

CPSW_STAT0_ALE_UNKN_MLT_BCNT is shown in [Figure 7-285](#) and described in [Table 7-590](#).

[Return to Summary Table.](#)

ALE Receive Unknown Multicast Bytecount.

Table 7-589. CPSW_STAT0_ALE_UNKN_MLT_BCNT Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0B4h

Figure 7-285. CPSW_STAT0_ALE_UNKN_MLT_BCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-590. CPSW_STAT0_ALE_UNKN_MLT_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount.

7.10.35 CPSW_STAT0_ALE_UNKN_BRD Register (Offset = 0003A0B8h) [reset = 0h]

CPSW_STAT0_ALE_UNKN_BRD is shown in [Figure 7-286](#) and described in [Table 7-592](#).

Return to [Summary Table](#).

ALE Receive Unknown Broadcast.

**Table 7-591. CPSW_STAT0_ALE_UNKN_BRD
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0B8h

Figure 7-286. CPSW_STAT0_ALE_UNKN_BRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-592. CPSW_STAT0_ALE_UNKN_BRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Broadcast.

7.10.36 CPSW_STAT0_ALE_UNKN_BRD_BCNT Register (Offset = 0003A0BCh) [reset = 0h]

CPSW_STAT0_ALE_UNKN_BRD_BCNT is shown in [Figure 7-287](#) and described in [Table 7-594](#).

Return to [Summary Table](#).

ALE Receive Unknown Broadcast Bytecount.

Table 7-593. CPSW_STAT0_ALE_UNKN_BRD_BCNT Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0BCh

Figure 7-287. CPSW_STAT0_ALE_UNKN_BRD_BCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-594. CPSW_STAT0_ALE_UNKN_BRD_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount.

7.10.37 CPSW_STAT0_ALE_POL_MATCH Register (Offset = 0003A0C0h) [reset = 0h]

CPSW_STAT0_ALE_POL_MATCH is shown in [Figure 7-288](#) and described in [Table 7-596](#).

Return to [Summary Table](#).

ALE Policer Matched.

**Table 7-595. CPSW_STAT0_ALE_POL_MATCH
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0C0h

Figure 7-288. CPSW_STAT0_ALE_POL_MATCH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-596. CPSW_STAT0_ALE_POL_MATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched.

7.10.38 CPSW_STAT0_ALE_POL_MATCH_RED Register (Offset = 0003A0C4h) [reset = 0h]

CPSW_STAT0_ALE_POL_MATCH_RED is shown in [Figure 7-289](#) and described in [Table 7-598](#).

Return to [Summary Table](#).

ALE Policer Matched and Condition Red.

Table 7-597. CPSW_STAT0_ALE_POL_MATCH_RED Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0C4h

Figure 7-289. CPSW_STAT0_ALE_POL_MATCH_RED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-598. CPSW_STAT0_ALE_POL_MATCH_RED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched and Condition Red.

7.10.39 CPSW_STAT0_ALE_POL_MATCH_YELLOW Register (Offset = 0003A0C8h) [reset = 0h]

CPSW_STAT0_ALE_POL_MATCH_YELLOW is shown in Figure 7-290 and described in Table 7-600.

Return to [Summary Table](#).

ALE Policer Matched and Condition Yellow.

Table 7-599.
CPSW_STAT0_ALE_POL_MATCH_YELLOW
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0C8h

Figure 7-290. CPSW_STAT0_ALE_POL_MATCH_YELLOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-600. CPSW_STAT0_ALE_POL_MATCH_YELLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow.

7.10.40 CPSW_STAT0_ALE_MULT_SA_DROP Register (Offset = 0003A0CCh) [reset = 0h]

CPSW_STAT0_ALE_MULT_SA_DROP is shown in [Figure 7-291](#) and described in [Table 7-602](#).

Return to [Summary Table](#).

ALE Multicast Source Address Drop.

Table 7-601. CPSW_STAT0_ALE_MULT_SA_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0CCh

Figure 7-291. CPSW_STAT0_ALE_MULT_SA_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-602. CPSW_STAT0_ALE_MULT_SA_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Multicast Source Address drop.

7.10.41 CPSW_STAT0_ALE_DUAL_VLAN_DROP Register (Offset = 0003A0D0h) [reset = 0h]

CPSW_STAT0_ALE_DUAL_VLAN_DROP is shown in [Figure 7-292](#) and described in [Table 7-604](#).

Return to [Summary Table](#).

ALE Dual VLAN Drop.

Table 7-603.
CPSW_STAT0_ALE_DUAL_VLAN_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0D0h

Figure 7-292. CPSW_STAT0_ALE_DUAL_VLAN_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-604. CPSW_STAT0_ALE_DUAL_VLAN_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Dual VLAN drop.

7.10.42 CPSW_STAT0_ALE_LEN_ERROR_DROP Register (Offset = 0003A0D4h) [reset = 0h]

CPSW_STAT0_ALE_LEN_ERROR_DROP is shown in [Figure 7-293](#) and described in [Table 7-606](#).

Return to [Summary Table](#).

ALE Length Error Drop.

Table 7-605.
CPSW_STAT0_ALE_LEN_ERROR_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0D4h

Figure 7-293. CPSW_STAT0_ALE_LEN_ERROR_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-606. CPSW_STAT0_ALE_LEN_ERROR_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Length Error drop.

7.10.43 CPSW_STAT0_ALE_IP_NEXT_HDR_DROP Register (Offset = 0003A0D8h) [reset = 0h]

CPSW_STAT0_ALE_IP_NEXT_HDR_DROP is shown in [Figure 7-294](#) and described in [Table 7-608](#).

[Return to Summary Table.](#)

ALE IP Next Header Drop.

Table 7-607.
CPSW_STAT0_ALE_IP_NEXT_HDR_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0D8h

Figure 7-294. CPSW_STAT0_ALE_IP_NEXT_HDR_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-608. CPSW_STAT0_ALE_IP_NEXT_HDR_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Next Header drop.

7.10.44 CPSW_STAT0_ALE_IPV4_FRAG_DROP Register (Offset = 0003A0DCh) [reset = 0h]

CPSW_STAT0_ALE_IPV4_FRAG_DROP is shown in [Figure 7-295](#) and described in [Table 7-610](#).

Return to [Summary Table](#).

ALE IPV4 Frag Drop.

Table 7-609. CPSW_STAT0_ALE_IPV4_FRAG_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A0DCh

Figure 7-295. CPSW_STAT0_ALE_IPV4_FRAG_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-610. CPSW_STAT0_ALE_IPV4_FRAG_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE IPV4 Fragment drop.

7.10.45 CPSW_STAT0_IET_RX_ASSEMBLY_ERROR_REG Register (Offset = 0003A140h) [reset = 0h]

CPSW_STAT0_IET_RX_ASSEMBLY_ERROR_REG is shown in [Figure 7-296](#) and described in [Table 7-612](#).

Return to [Summary Table](#).

IET Receive Assembly Error.

Note: IET functionality is not supported for MCU_CPSW0 Port 0.

Table 7-611.
CPSW_STAT0_IET_RX_ASSEMBLY_ERROR_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A140h

Figure 7-296. CPSW_STAT0_IET_RX_ASSEMBLY_ERROR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_ERROR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-612. CPSW_STAT0_IET_RX_ASSEMBLY_ERROR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_ASSEMBLY_ER ROR	R/W	0h	IET Receive Assembly Error Note: IET functionality is not supported for MCU_CPSW0 Port 0.

7.10.46 CPSW_STAT0_IET_RX_ASSEMBLY_OK_REG Register (Offset = 0003A144h) [reset = 0h]

CPSW_STAT0_IET_RX_ASSEMBLY_OK_REG is shown in [Figure 7-297](#) and described in [Table 7-614](#).

Return to [Summary Table](#).

IET Receive Assembly Ok.

Note: IET functionality is not supported for MCU_CPSW0 Port 0.

Table 7-613.
CPSW_STAT0_IET_RX_ASSEMBLY_OK_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A144h

Figure 7-297. CPSW_STAT0_IET_RX_ASSEMBLY_OK_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_OK																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-614. CPSW_STAT0_IET_RX_ASSEMBLY_OK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_ASSEMBLY_OK	R/W	0h	IET Receive Assembly Ok. Note: IET functionality is not supported for MCU_CPSW0 Port 0.

7.10.47 CPSW_STAT0_IET_RX_SMD_ERROR_REG Register (Offset = 0003A148h) [reset = 0h]

CPSW_STAT0_IET_RX_SMD_ERROR_REG is shown in [Figure 7-298](#) and described in [Table 7-616](#).

Return to [Summary Table](#).

IET Receive Smd Error.

Note: IET functionality is not supported for MCU_CPSW0 Port 0.

Table 7-615.
CPSW_STAT0_IET_RX_SMD_ERROR_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A148h

Figure 7-298. CPSW_STAT0_IET_RX_SMD_ERROR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_SMD_ERROR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-616. CPSW_STAT0_IET_RX_SMD_ERROR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_SMD_ERROR	R/W	0h	IET Receive Smd Error. Note: IET functionality is not supported for MCU_CPSW0 Port 0.

7.10.48 CPSW_STAT0_IET_RX_FRAG_REG Register (Offset = 0003A14Ch) [reset = 0h]

CPSW_STAT0_IET_RX_FRAG_REG is shown in [Figure 7-299](#) and described in [Table 7-618](#).

Return to [Summary Table](#).

IET Receive Frag.

Note: IET functionality is not supported for MCU_CPSW0 Port 0.

**Table 7-617. CPSW_STAT0_IET_RX_FRAG_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A14Ch

Figure 7-299. CPSW_STAT0_IET_RX_FRAG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_FRAG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-618. CPSW_STAT0_IET_RX_FRAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_FRAG	R/W	0h	IET Receive Frag. Note: IET functionality is not supported for MCU_CPSW0 Port 0.

7.10.49 CPSW_STAT0_IET_TX_HOLD_REG Register (Offset = 0003A150h) [reset = 0h]

CPSW_STAT0_IET_TX_HOLD_REG is shown in [Figure 7-300](#) and described in [Table 7-620](#).

Return to [Summary Table](#).

IET Transmit Hold.

Note: IET functionality is not supported for MCU_CPSW0 Port 0.

**Table 7-619. CPSW_STAT0_IET_TX_HOLD_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A150h

Figure 7-300. CPSW_STAT0_IET_TX_HOLD_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_TX_HOLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-620. CPSW_STAT0_IET_TX_HOLD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_TX_HOLD	R/W	0h	IET Transmit Hold. Note: IET functionality is not supported for MCU_CPSW0 Port 0.

7.10.50 CPSW_STAT0_IET_TX_FRAG_REG Register (Offset = 0003A154h) [reset = 0h]

CPSW_STAT0_IET_TX_FRAG_REG is shown in [Figure 7-301](#) and described in [Table 7-622](#).

Return to [Summary Table](#).

IET Transmit Frag.

Note: IET functionality is not supported for MCU_CPSW0 Port 0.

**Table 7-621. CPSW_STAT0_IET_TX_FRAG_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A154h

Figure 7-301. CPSW_STAT0_IET_TX_FRAG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_TX_FRAG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-622. CPSW_STAT0_IET_TX_FRAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_TX_FRAG	R/W	0h	IET Transmit Frag. Note: IET functionality is not supported for MCU_CPSW0 Port 0.

7.10.51 CPSW_STAT0_TX_MEMORY_PROTECT_ERROR Register (Offset = 0003A17Ch) [reset = X]

CPSW_STAT0_TX_MEMORY_PROTECT_ERROR is shown in [Figure 7-302](#) and described in [Table 7-624](#).

Return to [Summary Table](#).

Transmit Memory Protect CRC Error.

Table 7-623.
CPSW_STAT0_TX_MEMORY_PROTECT_ERROR
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT0	4603 A17Ch

Figure 7-302. CPSW_STAT0_TX_MEMORY_PROTECT_ERROR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								COUNT							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-624. CPSW_STAT0_TX_MEMORY_PROTECT_ERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	COUNT	R/W	0h	Transmit Memory Protect CRC Error. Note: If there is a memory protect error, then this COUNT value will increment and issue a STAT_PEND0 interrupt, when this bit field is non-zero. That is different from the other stats which only issue an interrupt when their values are greater than 0xFFFF.

7.11 MCU_CPSW0_STAT1 Registers

Table 7-626 lists the memory-mapped registers for the MCU_CPSW0_STAT1 (Port 1). All register offset addresses not listed in Table 7-626 should be considered as reserved locations and the register contents should not be modified.

Table 7-625. MCU_CPSW0_STAT1 Instances

Instance	Base Address
MCU_CPSW0_NUSS_STAT1	4600 0000h

Table 7-626. MCU_CPSW0_STAT1 Registers

Offset	Acronym	Register Name	MCU_CPSW0_NUSS_STAT1 Physical Address
0003A200h	CPSW_STAT1_RXGOODFRAMES	Ethernet Port N Total Number of Good Frames Received	4603 A200h
0003A204h	CPSW_STAT1_RXBROADCASTFRAMES	Ethernet Port N Total Number of Good Broadcast Frames Received	4603 A204h
0003A208h	CPSW_STAT1_RXMULTICASTFRAMES	Ethernet Port N Total Number of Good Multicast Frames Received	4603 A208h
0003A20Ch	CPSW_STAT1_RXPAUSEFRAMES	Ethernet Port N PauseRxFrames	4603 A20Ch
0003A210h	CPSW_STAT1_RXCRCERRORS	Ethernet Port N Total Number of CRC Errors Frames Received	4603 A210h
0003A214h	CPSW_STAT1_RXALIGNCODEERRORS	Ethernet Port N Total Number of Align/Code Errors Received	4603 A214h
0003A218h	CPSW_STAT1_RXOVERSIZEDFRAMES	Ethernet Port N Total Number of Oversized Frames Received	4603 A218h
0003A21Ch	CPSW_STAT1_RXJABBERFRAMES	Ethernet Port N Total Number of Jabber Frames Received	4603 A21Ch
0003A220h	CPSW_STAT1_RXUNDERSIZEDFRAMES	Ethernet Port N Total Number of Undersized Frames Received	4603 A220h
0003A224h	CPSW_STAT1_RXFRAGMENTS	Ethernet Port N Fragments Received Register	4603 A224h
0003A228h	CPSW_STAT1_ALE_DROP	Ethernet Port N ALE Drop Register	4603 A228h
0003A22Ch	CPSW_STAT1_ALE_OVERRUN_DROP	Ethernet Port N ALE Overrun Drop Register	4603 A22Ch
0003A230h	CPSW_STAT1_RXOCTETS	Ethernet Port N Total Number of Received Bytes in Good Frames	4603 A230h
0003A234h	CPSW_STAT1_TXGOODFRAMES	Ethernet Port N Good Transmit Frames Register	4603 A234h
0003A238h	CPSW_STAT1_TXBROADCASTFRAMES	Ethernet Port N Broadcast Transmit Frames Register	4603 A238h
0003A23Ch	CPSW_STAT1_TXMULTICASTFRAMES	Ethernet Port N Multicast Transmit Frames Register	4603 A23Ch
0003A240h	CPSW_STAT1_TXPAUSEFRAMES	Ethernet Port N Pause Transmit Frames Register	4603 A240h
0003A244h	CPSW_STAT1_TXDEFERREDFRAMES	Ethernet Port N Deferred Frames Register	4603 A244h
0003A248h	CPSW_STAT1_TXCOLLISIONFRAMES	Ethernet Port N Collisions Register	4603 A248h
0003A24Ch	CPSW_STAT1_TXSINGLECOLLFRAMES	Ethernet Port N Collision Transmit Frames Register	4603 A24Ch
0003A250h	CPSW_STAT1_TXMULTCOLLFRAMES	Ethernet Port N Multiple Collision Transmit Frames Register	4603 A250h
0003A254h	CPSW_STAT1_TXEXCESSIVECOLLISIONS	Ethernet Port N Excessive Collision Transmit Frames Register	4603 A254h
0003A258h	CPSW_STAT1_TXLATECOLLISIONS	Ethernet Port N Late Collisions Register	4603 A258h
0003A25Ch	CPSW_STAT1_RXIPGERROR	Ethernet Port N Receive Inter Packet Gap Error (10G only) Register	4603 A25Ch
0003A260h	CPSW_STAT1_TXCARRIERSENSEERRORS	Ethernet Port N Carrier Sense Errors Register	4603 A260h

Table 7-626. MCU_CPSW0_STAT1 Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_NU SS_STAT1 Physical Address
0003A264h	CPSW_STAT1_TXOCTETS	Ethernet Port N Tx Octets Register	4603 A264h
0003A268h	CPSW_STAT1_OCTETFRAMES64	Ethernet Port N 64 Octet Frames Register	4603 A268h
0003A26Ch	CPSW_STAT1_OCTETFRAMES65T127	Ethernet Port N 65-127 Octet Frames Register	4603 A26Ch
0003A270h	CPSW_STAT1_OCTETFRAMES128T255	Ethernet Port N 128-255 Octet Frames Register	4603 A270h
0003A274h	CPSW_STAT1_OCTETFRAMES256T511	Ethernet Port N 256-511 Octet Frames Register	4603 A274h
0003A278h	CPSW_STAT1_OCTETFRAMES512T1023	Ethernet Port N 512-pn_rx_maxlen Octet Frames Register	4603 A278h
0003A27Ch	CPSW_STAT1_OCTETFRAMES1024TUP	Ethernet Port N 1023-1518 Octet Frames Register	4603 A27Ch
0003A280h	CPSW_STAT1_NETOCTETS	Ethernet Port N Net Octets Register	4603 A280h
0003A284h	CPSW_STAT1_RX_BOTTOM_OF_FIFO_DROP	Ethernet Port N Receive Bottom of FIFO Drop Register	4603 A284h
0003A288h	CPSW_STAT1_PORTMASK_DROP	Ethernet Port N Portmask Drop Register	4603 A288h
0003A28Ch	CPSW_STAT1_RX_TOP_OF_FIFO_DROP	Ethernet Port N Receive Top of FIFO Drop Register	4603 A28Ch
0003A290h	CPSW_STAT1_ALE_RATE_LIMIT_DROP	Ethernet Port N ALE Rate Limit Drop Register	4603 A290h
0003A294h	CPSW_STAT1_ALE_VID_INGRESS_DROP	Ethernet Port N ALE VID Ingress Drop Register	4603 A294h
0003A298h	CPSW_STAT1_ALE_DA_EQ_SA_DROP	Ethernet Port N ALE DA equal SA Drop Register	4603 A298h
0003A29Ch	CPSW_STAT1_ALE_BLOCK_DROP	Ethernet Port N ALE Block Drop Register	4603 A29Ch
0003A2A0h	CPSW_STAT1_ALE_SECURE_DROP	Ethernet Port N ALE Secure Drop Register	4603 A2A0h
0003A2A4h	CPSW_STAT1_ALE_AUTH_DROP	Ethernet Port N ALE Authentication Drop Register	4603 A2A4h
0003A2A8h	CPSW_STAT1_ALE_UNKN_UNI	Ethernet Port N ALE Receive Unknown Unicast Register	4603 A2A8h
0003A2ACh	CPSW_STAT1_ALE_UNKN_UNI_BCNT	Ethernet Port N Receive Unknown Unicast Bytecount Register	4603 A2ACh
0003A2B0h	CPSW_STAT1_ALE_UNKN_MLT	Ethernet Port N ALE Receive Unknown Multicast Register	4603 A2B0h
0003A2B4h	CPSW_STAT1_ALE_UNKN_MLT_BCNT	Ethernet Port N ALE Receive Unknown Multicast Bytecount Register	4603 A2B4h
0003A2B8h	CPSW_STAT1_ALE_UNKN_BRD	Ethernet Port N ALE Receive Unknown Broadcast Register	4603 A2B8h
0003A2BCh	CPSW_STAT1_ALE_UNKN_BRD_BCNT	Ethernet Port N ALE Receive Unknown Broadcast Bytecount Register	4603 A2BCh
0003A2C0h	CPSW_STAT1_ALE_POL_MATCH	Ethernet Port N ALE Policer Matched Register	4603 A2C0h
0003A2C4h	CPSW_STAT1_ALE_POL_MATCH_RED	Ethernet Port N ALE Policer Matched and Condition Red Register	4603 A2C4h
0003A2C8h	CPSW_STAT1_ALE_POL_MATCH_YELLOW	Ethernet Port N ALE Policer Matched and Condition Yellow Register	4603 A2C8h
0003A2CCh	CPSW_STAT1_ALE_MULT_SA_DROP	Enet Port N ALE Multicast Source Address Drop	4603 A2CCh
0003A2D0h	CPSW_STAT1_ALE_DUAL_VLAN_DROP	Enet Port N ALE Dual VLAN Drop	4603 A2D0h
0003A2D4h	CPSW_STAT1_ALE_LEN_ERROR_DROP	Enet Port N ALE IEEE 802.3 Length Error Drop	4603 A2D4h
0003A2D8h	CPSW_STAT1_ALE_IP_NEXT_HDR_DROP	Enet Port N ALE IP Next Header Limit Drop	4603 A2D8h
0003A2DCh	CPSW_STAT1_ALE_IPV4_FRAG_DROP	Enet Port N ALE IPv4 Fragment Drop	4603 A2DCh
0003A340h	CPSW_STAT1_IET_RX_ASSEMBLY_ERROR_REG	Enet Port N IET Received Assembly Error	4603 A340h
0003A344h	CPSW_STAT1_IET_RX_ASSEMBLY_OK_REG	Enet Port N IET Received Assembly OK	4603 A344h
0003A348h	CPSW_STAT1_IET_RX_SMD_ERROR_REG	Enet Port N IET Received SMD Error	4603 A348h

Table 7-626. MCU_CPSW0_STAT1 Registers (continued)

Offset	Acronym	Register Name	MCU_CPSW0_NU SS_STAT1 Physical Address
0003A34Ch	CPSW_STAT1_IET_RX_FRAG_REG	Enet Port N IET Received Fragment (IET fragment)	4603 A34Ch
0003A350h	CPSW_STAT1_IET_TX_HOLD_REG	Enet Port N IET Transmit Hold	4603 A350h
0003A354h	CPSW_STAT1_IET_TX_FRAG_REG	Enet Port N IET Transmit Fragment (IET fragment)	4603 A354h
0003A37Ch	CPSW_STAT1_TX_MEMORY_PROTECT_ERROR	Ethernet Port N Transmit Memory Protect CRC Error Register	4603 A37Ch
0003A380h + formula	CPSW_STAT1_ENET_PN_TX_PRI_REG_y	Ethernet Port N Tx Priority 0 to Priority 7 Packet Count Registers	4603 A380h + formula
0003A3A0h + formula	CPSW_STAT1_ENET_PN_TX_PRI_BCNT_REG_y	Ethernet Port N Tx Priority 0 to Priority 7 Packet Byte Count Register	4603 A3A0h + formula
0003A3C0h + formula	CPSW_STAT1_ENET_PN_TX_PRI_DROP_REG_y	Ethernet Port N Tx Priority 0 to Priority 7 Packet Drop Count Register	4603 A3C0h + formula
0003A3E0h + formula	CPSW_STAT1_ENET_PN_TX_PRI_DROP_BCNT_REG_y	Ethernet Port N Tx Priority 0 to Priority 7 Packet Drop Byte Count Register	4603 A3E0h + formula

7.11.1 CPSW_STAT1_RXGOODFRAMES Register (Offset = 0003A200h) [reset = 0h]

CPSW_STAT1_RXGOODFRAMES is shown in [Figure 7-303](#) and described in [Table 7-628](#).

Return to [Summary Table](#).

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Had a length of 64 to [CPSW_P0_RX_MAXLEN_REG](#)[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the [CPSW_STAT1_RXALIGNCODEERRORS](#) and [CPSW_STAT1_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

**Table 7-627. CPSW_STAT1_RXGOODFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A200h

Figure 7-303. CPSW_STAT1_RXGOODFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-628. CPSW_STAT1_RXGOODFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good frames received

7.11.2 CPSW_STAT1_RXBROADCASTFRAMES Register (Offset = 0003A204h) [reset = 0h]

CPSW_STAT1_RXBROADCASTFRAMES is shown in [Figure 7-304](#) and described in [Table 7-630](#).

Return to [Summary Table](#).

The total number of good broadcast frames received on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address 0xFFFFFFFF
- Had a length of CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the [CPSW_STAT1_RXALIGNCODEERRORS](#) and [CPSW_STAT1_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

Table 7-629.

CPSW_STAT1_RXBROADCASTFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A204h

Figure 7-304. CPSW_STAT1_RXBROADCASTFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-630. CPSW_STAT1_RXBROADCASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good broadcast frames received

7.11.3 CPSW_STAT1_RXMULTICASTFRAMES Register (Offset = 0003A208h) [reset = 0h]

CPSW_STAT1_RXMULTICASTFRAMES is shown in [Figure 7-305](#) and described in [Table 7-632](#).

Return to [Summary Table](#).

The total number of good multicast frames received on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than 0xFFFFFFFF
- Had a length of CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the [CPSW_STAT1_RXALIGNCODEERRORS](#) and [CPSW_STAT1_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

**Table 7-631. CPSW_STAT1_RXMULTICASTFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A208h

Figure 7-305. CPSW_STAT1_RXMULTICASTFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-632. CPSW_STAT1_RXMULTICASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good multicast frames received

7.11.4 CPSW_STAT1_RXPAUSEFRAMES Register (Offset = 0003A20Ch) [reset = 0h]

CPSW_STAT1_RXPAUSEFRAMES is shown in Figure 7-306 and described in Table 7-634.

Return to [Summary Table](#).

The total number of IEEE 802.3X pause frames received by the port (whether acted upon or not). Such a frame:

- Contained any unicast, broadcast, or multicast address
- Contained the length/type field value 88.08 (hex) and the opcode 0x0001
- Was of length 64 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error
- Pause-frames had been enabled on the port (CPSW_PN_MAC_CONTROL_REG[4] TX_FLOW_EN = 1h). The port could have been in either half or full-duplex mode.

See the CPSW_STAT1_RXALIGNCODEERRORS and CPSW_STAT1_RXCRCERRORS statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

**Table 7-633. CPSW_STAT1_RXPAUSEFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A20Ch

Figure 7-306. CPSW_STAT1_RXPAUSEFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-634. CPSW_STAT1_RXPAUSEFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of pause frames received

7.11.5 CPSW_STAT1_RXCRCERRORS Register (Offset = 0003A210h) [reset = 0h]

CPSW_STAT1_RXCRCERRORS is shown in [Figure 7-307](#) and described in [Table 7-636](#).

Return to [Summary Table](#).

The total number of frames received on the port that experienced a CRC error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no code/align error,
- Had a CRC error Overruns have no effect upon this statistic.

A CRC error is defined to be:

- A frame containing an even number of nibbles
- Failing the Frame Check Sequence test

**Table 7-635. CPSW_STAT1_RXCRCERRORS
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A210h

Figure 7-307. CPSW_STAT1_RXCRCERRORS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-636. CPSW_STAT1_RXCRCERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of CRC errors frames received.

7.11.6 CPSW_STAT1_RXALIGNCODEERRORS Register (Offset = 0003A214h) [reset = 0h]

CPSW_STAT1_RXALIGNCODEERRORS is shown in [Figure 7-308](#) and described in [Table 7-638](#).

Return to [Summary Table](#).

The total number of frames received on the port that experienced an alignment error or code error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had either an alignment error or a code error Overruns have no effect upon this statistic. An alignment error is defined to be:
 - A frame containing an odd number of nibbles
 - Failing the Frame Check Sequence test if the final nibble is ignored

A code error is defined to be a frame which has been discarded because the port's MRXER pin driven with a one for at least one bit-time's duration at any point during the frame's reception.

Note: RFC 1757 etherStatsCRCAlignErrors Ref. 1.5 can be calculated by summing

CPSW_STAT1_RXALIGNCODEERRORS and CPSW_STAT1_RXCRCERRORS.

Table 7-637. CPSW_STAT1_RXALIGNCODEERRORS Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A214h

Figure 7-308. CPSW_STAT1_RXALIGNCODEERRORS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-638. CPSW_STAT1_RXALIGNCODEERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of alignment/code errors received

7.11.7 CPSW_STAT1_RXOVERSIZEDFRAMES Register (Offset = 0003A218h) [reset = 0h]

CPSW_STAT1_RXOVERSIZEDFRAMES is shown in [Figure 7-309](#) and described in [Table 7-640](#).

Return to [Summary Table](#).

The total number of oversized frames received on the port. An oversized frame is defined to be:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than [CPSW_P0_RX_MAXLEN_REG](#)[13-0] RX_MAXLEN in bytes
- Had no CRC error, alignment error or code error

See the [CPSW_STAT1_RXALIGNCODEERRORS](#) and [CPSW_STAT1_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

**Table 7-639. CPSW_STAT1_RXOVERSIZEDFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A218h

Figure 7-309. CPSW_STAT1_RXOVERSIZEDFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-640. CPSW_STAT1_RXOVERSIZEDFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of oversized frames received

7.11.8 CPSW_STAT1_RXJABBERFRAMES Register (Offset = 0003A21Ch) [reset = 0h]

CPSW_STAT1_RXJABBERFRAMES is shown in [Figure 7-310](#) and described in [Table 7-642](#).

Return to [Summary Table](#).

The total number of jabber frames received on the port. A jabber frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN in bytes
- Had no CRC error, alignment error or code error

See the [CPSW_STAT1_RXALIGNCODEERRORS](#) and [CPSW_STAT1_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

**Table 7-641. CPSW_STAT1_RXJABBERFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A21Ch

Figure 7-310. CPSW_STAT1_RXJABBERFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-642. CPSW_STAT1_RXJABBERFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of jabber frames received.

7.11.9 CPSW_STAT1_RXUNDERSIZEDFRAMES Register (Offset = 0003A220h) [reset = 0h]

CPSW_STAT1_RXUNDERSIZEDFRAMES is shown in [Figure 7-311](#) and described in [Table 7-644](#).

Return to [Summary Table](#).

The total number of undersized frames received on the port. An undersized frame is defined to be:

- Was any data frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was less than 64 octets long
- Had no CRC error, alignment error or code error

See the [CPSW_STAT1_RXALIGNCODEERRORS](#) and [CPSW_STAT1_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

Table 7-643.

CPSW_STAT1_RXUNDERSIZEDFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A220h

Figure 7-311. CPSW_STAT1_RXUNDERSIZEDFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-644. CPSW_STAT1_RXUNDERSIZEDFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of undersized frames received

7.11.10 CPSW_STAT1_RXFRAGMENTS Register (Offset = 0003A224h) [reset = 0h]

CPSW_STAT1_RXFRAGMENTS is shown in Figure 7-312 and described in Table 7-646.

Return to [Summary Table](#).

The total number of frame fragments received on the port. A frame fragment is defined to be:

- Any data frame (address matching does not matter)
- Less than 64 bytes long
- Having a CRC error, an alignment error, or a code error
- Not the result of a collision caused by half duplex, collision based flow control

See the [CPSW_STAT1_RXALIGNCODEERRORS](#) and [CPSW_STAT1_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

**Table 7-645. CPSW_STAT1_RXFRAGMENTS
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A224h

Figure 7-312. CPSW_STAT1_RXFRAGMENTS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-646. CPSW_STAT1_RXFRAGMENTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of fragmented frames received.

7.11.11 CPSW_STAT1_ALE_DROP Register (Offset = 0003A228h) [reset = 0h]

CPSW_STAT1_ALE_DROP is shown in [Figure 7-313](#) and described in [Table 7-648](#).

Return to [Summary Table](#).

Total number of frames dropped by the ALE.

Table 7-647. CPSW_STAT1_ALE_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A228h

Figure 7-313. CPSW_STAT1_ALE_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-648. CPSW_STAT1_ALE_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames dropped by the ALE.

7.11.12 CPSW_STAT1_ALE_OVERRUN_DROP Register (Offset = 0003A22Ch) [reset = 0h]

CPSW_STAT1_ALE_OVERRUN_DROP is shown in Figure 7-314 and described in Table 7-650.

Return to [Summary Table](#).

Total number of overrun frames dropped by the ALE.

Table 7-649. CPSW_STAT1_ALE_OVERRUN_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A22Ch

Figure 7-314. CPSW_STAT1_ALE_OVERRUN_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-650. CPSW_STAT1_ALE_OVERRUN_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE

7.11.13 CPSW_STAT1_RXOCTETS Register (Offset = 0003A230h) [reset = 0h]

CPSW_STAT1_RXOCTETS is shown in [Figure 7-315](#) and described in [Table 7-652](#).

Return to [Summary Table](#).

The total number of bytes in all good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Of length 64 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the [CPSW_STAT1_RXALIGNCODEERRORS](#) and [CPSW_STAT1_RXCRCERRORS](#) statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

Table 7-651. CPSW_STAT1_RXOCTETS Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A230h

Figure 7-315. CPSW_STAT1_RXOCTETS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-652. CPSW_STAT1_RXOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of received bytes in good frames

7.11.14 CPSW_STAT1_TXGOODFRAMES Register (Offset = 0003A234h) [reset = 0h]

CPSW_STAT1_TXGOODFRAMES is shown in Figure 7-316 and described in Table 7-654.

Return to [Summary Table](#).

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun.

**Table 7-653. CPSW_STAT1_TXGOODFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A234h

Figure 7-316. CPSW_STAT1_TXGOODFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-654. CPSW_STAT1_TXGOODFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good frames transmitted

7.11.15 CPSW_STAT1_TXBROADCASTFRAMES Register (Offset = 0003A238h) [reset = 0h]

CPSW_STAT1_TXBROADCASTFRAMES is shown in [Figure 7-317](#) and described in [Table 7-656](#).

Return to [Summary Table](#).

The total number of good broadcast frames received on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address 0xFFFFFFFF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

Table 7-655.

CPSW_STAT1_TXBROADCASTFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A238h

Figure 7-317. CPSW_STAT1_TXBROADCASTFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-656. CPSW_STAT1_TXBROADCASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good broadcast frames transmitted

7.11.16 CPSW_STAT1_TXMULTICASTFRAMES Register (Offset = 0003A23Ch) [reset = 0h]

CPSW_STAT1_TXMULTICASTFRAMES is shown in [Figure 7-318](#) and described in [Table 7-658](#).

Return to [Summary Table](#).

The total number of good multicast frames received on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than 0xFFFFFFFF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun.

Table 7-657. CPSW_STAT1_TXMULTICASTFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A23Ch

Figure 7-318. CPSW_STAT1_TXMULTICASTFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-658. CPSW_STAT1_TXMULTICASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good multicast frames transmitted

7.11.17 CPSW_STAT1_TXPAUSEFRAMES Register (Offset = 0003A240h) [reset = 0h]

CPSW_STAT1_TXPAUSEFRAMES is shown in [Figure 7-319](#) and described in [Table 7-660](#).

Return to [Summary Table](#).

This statistic indicates the number of IEEE 802.3X pause frames transmitted by the port. Pause frames cannot underrun or contain a CRC error because they are created in the transmitting MAC, so these error conditions have no effect upon the statistic. Pause frames sent by software will not be included in this count. Since pause frames are only transmitted in full duplex carrier loss and collisions have no effect upon this statistic. Transmitted pause frames are always 64 byte multicast frames so will appear in the [CPSW_STAT1_TXMULTICASTFRAMES](#) and [CPSW_STAT1_OCTETFRAMES64](#) statistics.

**Table 7-659. CPSW_STAT1_TXPAUSEFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A240h

Figure 7-319. CPSW_STAT1_TXPAUSEFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-660. CPSW_STAT1_TXPAUSEFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of pause frames transmitted

7.11.18 CPSW_STAT1_TXDEFERREDFRAMES Register (Offset = 0003A244h) [reset = 0h]

CPSW_STAT1_TXDEFERREDFRAMES is shown in Figure 7-320 and described in Table 7-662.

Return to [Summary Table](#).

The total number of frames transmitted on the port that first experienced deferment. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced no collisions before being successfully transmitted
- Found the medium busy when transmission was first attempted, so had to wait. CRC errors have no effect upon this statistic.

Table 7-661. CPSW_STAT1_TXDEFERREDFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A244h

Figure 7-320. CPSW_STAT1_TXDEFERREDFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-662. CPSW_STAT1_TXDEFERREDFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of deferred frames transmitted

7.11.19 CPSW_STAT1_TXCOLLISIONFRAMES Register (Offset = 0003A248h) [reset = 0h]

CPSW_STAT1_TXCOLLISIONFRAMES is shown in [Figure 7-321](#) and described in [Table 7-664](#).

Return to [Summary Table](#).

This statistic records the total number of times that the port experienced a collision. Collisions occur under two circumstances.

1. When a transmit data or MAC control frame:
 - Was destined for any unicast, broadcast or multicast address
 - Was any size
 - Had no carrier loss and no underrun
 - Experienced a collision. A jam sequence is sent for every non-late collision, so this statistic will increment on each occasion if a frame experiences multiple collisions (and increments on late collisions) CRC errors have no effect upon this statistic.
2. When the port is in half-duplex mode, flow control is active, and a frame reception begins.

**Table 7-663. CPSW_STAT1_TXCOLLISIONFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A248h

Figure 7-321. CPSW_STAT1_TXCOLLISIONFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-664. CPSW_STAT1_TXCOLLISIONFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames experiencing a collision

7.11.20 CPSW_STAT1_TXSINGLECOLLFRAMES Register (Offset = 0003A24Ch) [reset = 0h]

CPSW_STAT1_TXSINGLECOLLFRAMES is shown in [Figure 7-322](#) and described in [Table 7-666](#).

Return to [Summary Table](#).

The total number of frames transmitted on the port that experienced exactly one collision. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced one collision before successful transmission. The collision was not late.

CRC errors have no effect upon this statistic.

Table 7-665.

CPSW_STAT1_TXSINGLECOLLFRAMES Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A24Ch

Figure 7-322. CPSW_STAT1_TXSINGLECOLLFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-666. CPSW_STAT1_TXSINGLECOLLFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames experiencing a single collision

7.11.21 CPSW_STAT1_TXMULTCOLLFRAMES Register (Offset = 0003A250h) [reset = 0h]

CPSW_STAT1_TXMULTCOLLFRAMES is shown in [Figure 7-323](#) and described in [Table 7-668](#).

Return to [Summary Table](#).

The total number of frames transmitted on the port that experienced multiple collisions. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 2 to 15 collisions before being successfully transmitted. None of the collisions were late.

CRC errors have no effect upon this statistic.

**Table 7-667. CPSW_STAT1_TXMULTCOLLFRAMES
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A250h

Figure 7-323. CPSW_STAT1_TXMULTCOLLFRAMES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-668. CPSW_STAT1_TXMULTCOLLFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames experiencing multiple collisions

7.11.22 CPSW_STAT1_TXEXCESSIVECOLLISIONS Register (Offset = 0003A254h) [reset = 0h]

CPSW_STAT1_TXEXCESSIVECOLLISIONS is shown in [Figure 7-324](#) and described in [Table 7-670](#).

Return to [Summary Table](#).

The total number of frames for which transmission was abandoned due to excessive collisions. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- Had no carrier loss and no underrun
- Experienced 16 collisions before abandoning all attempts at transmitting the frame. None of the collisions were late.

CRC errors have no effect upon this statistic.

Table 7-669.
CPSW_STAT1_TXEXCESSIVECOLLISIONS
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A254h

Figure 7-324. CPSW_STAT1_TXEXCESSIVECOLLISIONS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-670. CPSW_STAT1_TXEXCESSIVECOLLISIONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to excessive collisions

7.11.23 CPSW_STAT1_TXLATECOLLISIONS Register (Offset = 0003A258h) [reset = 0h]

CPSW_STAT1_TXLATECOLLISIONS is shown in Figure 7-325 and described in Table 7-672.

Return to [Summary Table](#).

The total number of frames on the port for which transmission was abandoned because they experienced a late collision. Such a frame:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
 - Was any size
 - Experienced a collision later than 512 bit-times into the transmission. There may have been up to 15 previous (non-late) collisions which had previously required the transmission to be re-attempted. The Late Collisions statistic dominates over the single, multiple and excessive Collisions statistics - if a late collision occurs the frame will not be counted in any of these other three statistics.
- CRC errors have no effect upon this statistic.

**Table 7-671. CPSW_STAT1_TXLATECOLLISIONS
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A258h

Figure 7-325. CPSW_STAT1_TXLATECOLLISIONS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-672. CPSW_STAT1_TXLATECOLLISIONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to a late collision

7.11.24 CPSW_STAT1_RXIPGERROR Register (Offset = 0003A25Ch) [reset = 0h]

CPSW_STAT1_RXIPGERROR is shown in [Figure 7-326](#) and described in [Table 7-674](#).

Return to [Summary Table](#).

Total number of receive inter-packet gap errors (10G only).

Table 7-673. CPSW_STAT1_RXIPGERROR Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A25Ch

Figure 7-326. CPSW_STAT1_RXIPGERROR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-674. CPSW_STAT1_RXIPGERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of receive inter-packet gap errors (10G only)

7.11.25 CPSW_STAT1_TXCARRIERSENSEERRORS Register (Offset = 0003A260h) [reset = 0h]

CPSW_STAT1_TXCARRIERSENSEERRORS is shown in [Figure 7-327](#) and described in [Table 7-676](#).

Return to [Summary Table](#).

The total number of frames received on the port that had a middle of frame (MOF) overrun. MOF overrun frame is defined to be:

- Was any data or MAC control frame destined for any unicast, broadcast or multicast address
- Was any size
- The carrier sense condition was lost or never asserted when transmitting the frame (the frame is not retransmitted). This is a transmit only statistic. Carrier Sense is a don't care for received frames. Transmit frames with carrier sense errors are sent until completion and are not aborted.

CRC errors have no effect upon this statistic.

Table 7-675.
CPSW_STAT1_TXCARRIERSENSEERRORS
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A260h

Figure 7-327. CPSW_STAT1_TXCARRIERSENSEERRORS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-676. CPSW_STAT1_TXCARRIERSENSEERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames that experienced a carrier loss

7.11.26 CPSW_STAT1_TXOCTETS Register (Offset = 0003A264h) [reset = 0h]

CPSW_STAT1_TXOCTETS is shown in [Figure 7-328](#) and described in [Table 7-678](#).

Return to [Summary Table](#).

The total number of bytes in all good frames transmitted on the port. A good frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Was any size
- Had no late or excessive collisions, no carrier loss and no underrun.

Table 7-677. CPSW_STAT1_TXOCTETS Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A264h

Figure 7-328. CPSW_STAT1_TXOCTETS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-678. CPSW_STAT1_TXOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

7.11.27 CPSW_STAT1_OCTETFRAMES64 Register (Offset = 0003A268h) [reset = 0h]

CPSW_STAT1_OCTETFRAMES64 is shown in [Figure 7-329](#) and described in [Table 7-680](#).

Return to [Summary Table](#).

The total number of 64-byte frames received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was exactly 64 bytes long. (If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic).

CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

**Table 7-679. CPSW_STAT1_OCTETFRAMES64
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A268h

Figure 7-329. CPSW_STAT1_OCTETFRAMES64 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-680. CPSW_STAT1_OCTETFRAMES64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

7.11.28 CPSW_STAT1_OCTETFRAMES65T127 Register (Offset = 0003A26Ch) [reset = 0h]

CPSW_STAT1_OCTETFRAMES65T127 is shown in Figure 7-330 and described in Table 7-682.

Return to [Summary Table](#).

The total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 65 to 127 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

**Table 7-681. CPSW_STAT1_OCTETFRAMES65T127
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A26Ch

Figure 7-330. CPSW_STAT1_OCTETFRAMES65T127 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-682. CPSW_STAT1_OCTETFRAMES65T127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

7.11.29 CPSW_STAT1_OCTETFRAMES128T255 Register (Offset = 0003A270h) [reset = 0h]

CPSW_STAT1_OCTETFRAMES128T255 is shown in [Figure 7-331](#) and described in [Table 7-684](#).

Return to [Summary Table](#).

The total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 128 to 255 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

**Table 7-683. CPSW_STAT1_OCTETFRAMES128T255
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A270h

Figure 7-331. CPSW_STAT1_OCTETFRAMES128T255 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-684. CPSW_STAT1_OCTETFRAMES128T255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

7.11.30 CPSW_STAT1_OCTETFRAMES256T511 Register (Offset = 0003A274h) [reset = 0h]

CPSW_STAT1_OCTETFRAMES256T511 is shown in [Figure 7-332](#) and described in [Table 7-686](#).

Return to [Summary Table](#).

The total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 256 to 511 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

**Table 7-685. CPSW_STAT1_OCTETFRAMES256T511
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A274h

Figure 7-332. CPSW_STAT1_OCTETFRAMES256T511 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-686. CPSW_STAT1_OCTETFRAMES256T511 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted

7.11.31 CPSW_STAT1_OCTETFRAMES512T1023 Register (Offset = 0003A278h) [reset = 0h]

CPSW_STAT1_OCTETFRAMES512T1023 is shown in [Figure 7-333](#) and described in [Table 7-688](#).

Return to [Summary Table](#).

The total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 512 to 1023 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Table 7-687.

CPSW_STAT1_OCTETFRAMES512T1023 Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A278h

Figure 7-333. CPSW_STAT1_OCTETFRAMES512T1023 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-688. CPSW_STAT1_OCTETFRAMES512T1023 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted

7.11.32 CPSW_STAT1_OCTETFRAMES1024TUP Register (Offset = 0003A27Ch) [reset = 0h]

CPSW_STAT1_OCTETFRAMES1024TUP is shown in [Figure 7-334](#) and described in [Table 7-690](#).

Return to [Summary Table](#).

The total number of frames of size 1024 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes for receive or 1024 up for transmit on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
 - Did not experience late collisions, excessive collisions, or carrier sense error
 - Was 1024 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes long on receive, or any size on transmit
- CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Table 7-689. CPSW_STAT1_OCTETFRAMES1024TUP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A27Ch

Figure 7-334. CPSW_STAT1_OCTETFRAMES1024TUP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-690. CPSW_STAT1_OCTETFRAMES1024TUP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

7.11.33 CPSW_STAT1_NETOCTETS Register (Offset = 0003A280h) [reset = 0h]

CPSW_STAT1_NETOCTETS is shown in [Figure 7-335](#) and described in [Table 7-692](#).

Return to [Summary Table](#).

The total number of bytes of frame data received and transmitted on the port. Each frame counted:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address (address match does not matter)
- Any length (including less than 64 bytes and greater than CPSW0_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes)

Also counted in this statistic is:

- Every byte transmitted before a carrier- loss was experienced
- Every byte transmitted before each collision was experienced, (i.e. multiple retries are counted each time)
- Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting)

Error conditions such as alignment errors, CRC errors, code errors, overruns and underruns do not affect the recording of bytes by this statistic. The objective of this statistic is to give a reasonable indication of ethernet utilization

Table 7-691. CPSW_STAT1_NETOCTETS Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A280h

Figure 7-335. CPSW_STAT1_NETOCTETS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-692. CPSW_STAT1_NETOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of bytes received and transmitted

7.11.34 CPSW_STAT1_RX_BOTTOM_OF_FIFO_DROP Register (Offset = 0003A284h) [reset = 0h]

CPSW_STAT1_RX_BOTTOM_OF_FIFO_DROP is shown in [Figure 7-336](#) and described in [Table 7-694](#).

Return to [Summary Table](#).

Receive Bottom of FIFO Drop.

Table 7-693.
CPSW_STAT1_RX_BOTTOM_OF_FIFO_DROP
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A284h

Figure 7-336. CPSW_STAT1_RX_BOTTOM_OF_FIFO_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-694. CPSW_STAT1_RX_BOTTOM_OF_FIFO_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Receive Bottom of FIFO Drop.

7.11.35 CPSW_STAT1_PORTMASK_DROP Register (Offset = 0003A288h) [reset = 0h]

CPSW_STAT1_PORTMASK_DROP is shown in [Figure 7-337](#) and described in [Table 7-696](#).

Return to [Summary Table](#).

Total number of dropped frames received due to portmask.

**Table 7-695. CPSW_STAT1_PORTMASK_DROP
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A288h

Figure 7-337. CPSW_STAT1_PORTMASK_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-696. CPSW_STAT1_PORTMASK_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames received due to portmask.

7.11.36 CPSW_STAT1_RX_TOP_OF_FIFO_DROP Register (Offset = 0003A28Ch) [reset = 0h]

CPSW_STAT1_RX_TOP_OF_FIFO_DROP is shown in [Figure 7-338](#) and described in [Table 7-698](#).

Return to [Summary Table](#).

Receive Top of FIFO Drop.

Table 7-697.
CPSW_STAT1_RX_TOP_OF_FIFO_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A28Ch

Figure 7-338. CPSW_STAT1_RX_TOP_OF_FIFO_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-698. CPSW_STAT1_RX_TOP_OF_FIFO_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Receive Top of FIFO Drop.

7.11.37 CPSW_STAT1_ALE_RATE_LIMIT_DROP Register (Offset = 0003A290h) [reset = 0h]

CPSW_STAT1_ALE_RATE_LIMIT_DROP is shown in [Figure 7-339](#) and described in [Table 7-700](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Rate Limiting.

Table 7-699. CPSW_STAT1_ALE_RATE_LIMIT_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A290h

Figure 7-339. CPSW_STAT1_ALE_RATE_LIMIT_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-700. CPSW_STAT1_ALE_RATE_LIMIT_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting.

7.11.38 CPSW_STAT1_ALE_VID_INGRESS_DROP Register (Offset = 0003A294h) [reset = 0h]

CPSW_STAT1_ALE_VID_INGRESS_DROP is shown in [Figure 7-340](#) and described in [Table 7-702](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE VID Ingress.

Table 7-701.
CPSW_STAT1_ALE_VID_INGRESS_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A294h

Figure 7-340. CPSW_STAT1_ALE_VID_INGRESS_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-702. CPSW_STAT1_ALE_VID_INGRESS_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress.

7.11.39 CPSW_STAT1_ALE_DA_EQ_SA_DROP Register (Offset = 0003A298h) [reset = 0h]

CPSW_STAT1_ALE_DA_EQ_SA_DROP is shown in [Figure 7-341](#) and described in [Table 7-704](#).

Return to [Summary Table](#).

Total number of dropped frames due to DA=SA.

Table 7-703. CPSW_STAT1_ALE_DA_EQ_SA_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A298h

Figure 7-341. CPSW_STAT1_ALE_DA_EQ_SA_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-704. CPSW_STAT1_ALE_DA_EQ_SA_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA.

7.11.40 CPSW_STAT1_ALE_BLOCK_DROP Register (Offset = 0003A29Ch) [reset = 0h]

CPSW_STAT1_ALE_BLOCK_DROP is shown in [Figure 7-342](#) and described in [Table 7-706](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Block Mode.

Table 7-705. CPSW_STAT1_ALE_BLOCK_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A29Ch

Figure 7-342. CPSW_STAT1_ALE_BLOCK_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-706. CPSW_STAT1_ALE_BLOCK_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode.

7.11.41 CPSW_STAT1_ALE_SECURE_DROP Register (Offset = 0003A2A0h) [reset = 0h]

CPSW_STAT1_ALE_SECURE_DROP is shown in [Figure 7-343](#) and described in [Table 7-708](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Secure Mode.

**Table 7-707. CPSW_STAT1_ALE_SECURE_DROP
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2A0h

Figure 7-343. CPSW_STAT1_ALE_SECURE_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-708. CPSW_STAT1_ALE_SECURE_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode.

7.11.42 CPSW_STAT1_ALE_AUTH_DROP Register (Offset = 0003A2A4h) [reset = 0h]

CPSW_STAT1_ALE_AUTH_DROP is shown in [Figure 7-344](#) and described in [Table 7-710](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Authentication.

Table 7-709. CPSW_STAT1_ALE_AUTH_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2A4h

Figure 7-344. CPSW_STAT1_ALE_AUTH_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-710. CPSW_STAT1_ALE_AUTH_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication.

7.11.43 CPSW_STAT1_ALE_UNKN_UNI Register (Offset = 0003A2A8h) [reset = 0h]

CPSW_STAT1_ALE_UNKN_UNI is shown in [Figure 7-345](#) and described in [Table 7-712](#).

Return to [Summary Table](#).

ALE Receive Unknown Unicast.

**Table 7-711. CPSW_STAT1_ALE_UNKN_UNI
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2A8h

Figure 7-345. CPSW_STAT1_ALE_UNKN_UNI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-712. CPSW_STAT1_ALE_UNKN_UNI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Unicast.

7.11.44 CPSW_STAT1_ALE_UNKN_UNI_BCNT Register (Offset = 0003A2ACh) [reset = 0h]

CPSW_STAT1_ALE_UNKN_UNI_BCNT is shown in Figure 7-346 and described in Table 7-714.

Return to [Summary Table](#).

ALE Receive Unknown Unicast Bytecount.

Table 7-713. CPSW_STAT1_ALE_UNKN_UNI_BCNT Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2ACh

Figure 7-346. CPSW_STAT1_ALE_UNKN_UNI_BCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-714. CPSW_STAT1_ALE_UNKN_UNI_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount.

7.11.45 CPSW_STAT1_ALE_UNKN_MLT Register (Offset = 0003A2B0h) [reset = 0h]

CPSW_STAT1_ALE_UNKN_MLT is shown in [Figure 7-347](#) and described in [Table 7-716](#).

Return to [Summary Table](#).

ALE Receive Unknown Multicast.

**Table 7-715. CPSW_STAT1_ALE_UNKN_MLT
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2B0h

Figure 7-347. CPSW_STAT1_ALE_UNKN_MLT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-716. CPSW_STAT1_ALE_UNKN_MLT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Multicast.

7.11.46 CPSW_STAT1_ALE_UNKN_MLT_BCNT Register (Offset = 0003A2B4h) [reset = 0h]

CPSW_STAT1_ALE_UNKN_MLT_BCNT is shown in [Figure 7-348](#) and described in [Table 7-718](#).

[Return to Summary Table.](#)

ALE Receive Unknown Multicast Bytecount.

Table 7-717. CPSW_STAT1_ALE_UNKN_MLT_BCNT Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2B4h

Figure 7-348. CPSW_STAT1_ALE_UNKN_MLT_BCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-718. CPSW_STAT1_ALE_UNKN_MLT_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount.

7.11.47 CPSW_STAT1_ALE_UNKN_BRD Register (Offset = 0003A2B8h) [reset = 0h]

CPSW_STAT1_ALE_UNKN_BRD is shown in [Figure 7-349](#) and described in [Table 7-720](#).

Return to [Summary Table](#).

ALE Receive Unknown Broadcast.

**Table 7-719. CPSW_STAT1_ALE_UNKN_BRD
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2B8h

Figure 7-349. CPSW_STAT1_ALE_UNKN_BRD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-720. CPSW_STAT1_ALE_UNKN_BRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Broadcast.

7.11.48 CPSW_STAT1_ALE_UNKN_BRD_BCNT Register (Offset = 0003A2BCh) [reset = 0h]

CPSW_STAT1_ALE_UNKN_BRD_BCNT is shown in [Figure 7-350](#) and described in [Table 7-722](#).

Return to [Summary Table](#).

ALE Receive Unknown Broadcast Bytecount.

Table 7-721. CPSW_STAT1_ALE_UNKN_BRD_BCNT Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2BCh

Figure 7-350. CPSW_STAT1_ALE_UNKN_BRD_BCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-722. CPSW_STAT1_ALE_UNKN_BRD_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount.

7.11.49 CPSW_STAT1_ALE_POL_MATCH Register (Offset = 0003A2C0h) [reset = 0h]

CPSW_STAT1_ALE_POL_MATCH is shown in [Figure 7-351](#) and described in [Table 7-724](#).

Return to [Summary Table](#).

ALE Policer Matched.

**Table 7-723. CPSW_STAT1_ALE_POL_MATCH
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2C0h

Figure 7-351. CPSW_STAT1_ALE_POL_MATCH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-724. CPSW_STAT1_ALE_POL_MATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched.

7.11.50 CPSW_STAT1_ALE_POL_MATCH_RED Register (Offset = 0003A2C4h) [reset = 0h]

CPSW_STAT1_ALE_POL_MATCH_RED is shown in Figure 7-352 and described in Table 7-726.

Return to [Summary Table](#).

ALE Policer Matched and Condition Red.

Table 7-725. CPSW_STAT1_ALE_POL_MATCH_RED Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2C4h

Figure 7-352. CPSW_STAT1_ALE_POL_MATCH_RED Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-726. CPSW_STAT1_ALE_POL_MATCH_RED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched and Condition Red.

7.11.51 CPSW_STAT1_ALE_POL_MATCH_YELLOW Register (Offset = 0003A2C8h) [reset = 0h]

CPSW_STAT1_ALE_POL_MATCH_YELLOW is shown in [Figure 7-353](#) and described in [Table 7-728](#).

Return to [Summary Table](#).

ALE Policer Matched and Condition Yellow.

Table 7-727.
CPSW_STAT1_ALE_POL_MATCH_YELLOW
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2C8h

Figure 7-353. CPSW_STAT1_ALE_POL_MATCH_YELLOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-728. CPSW_STAT1_ALE_POL_MATCH_YELLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow.

7.11.52 CPSW_STAT1_ALE_MULT_SA_DROP Register (Offset = 0003A2CCh) [reset = 0h]

CPSW_STAT1_ALE_MULT_SA_DROP is shown in [Figure 7-354](#) and described in [Table 7-730](#).

Return to [Summary Table](#).

ALE Multicast Source Address Drop

Table 7-729. CPSW_STAT1_ALE_MULT_SA_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2CCh

Figure 7-354. CPSW_STAT1_ALE_MULT_SA_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-730. CPSW_STAT1_ALE_MULT_SA_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Multicast Source Address drop

7.11.53 CPSW_STAT1_ALE_DUAL_VLAN_DROP Register (Offset = 0003A2D0h) [reset = 0h]

CPSW_STAT1_ALE_DUAL_VLAN_DROP is shown in [Figure 7-355](#) and described in [Table 7-732](#).

Return to [Summary Table](#).

ALE Dual VLAN Drop

Table 7-731.
CPSW_STAT1_ALE_DUAL_VLAN_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2D0h

Figure 7-355. CPSW_STAT1_ALE_DUAL_VLAN_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-732. CPSW_STAT1_ALE_DUAL_VLAN_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Dual VLAN drop

7.11.54 CPSW_STAT1_ALE_LEN_ERROR_DROP Register (Offset = 0003A2D4h) [reset = 0h]

CPSW_STAT1_ALE_LEN_ERROR_DROP is shown in [Figure 7-356](#) and described in [Table 7-734](#).

Return to [Summary Table](#).

ALE Length Error Drop

Table 7-733.
CPSW_STAT1_ALE_LEN_ERROR_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2D4h

Figure 7-356. CPSW_STAT1_ALE_LEN_ERROR_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-734. CPSW_STAT1_ALE_LEN_ERROR_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Length Error drop

7.11.55 CPSW_STAT1_ALE_IP_NEXT_HDR_DROP Register (Offset = 0003A2D8h) [reset = 0h]

CPSW_STAT1_ALE_IP_NEXT_HDR_DROP is shown in [Figure 7-357](#) and described in [Table 7-736](#).

[Return to Summary Table.](#)

ALE IP Next Header Drop

Table 7-735.
CPSW_STAT1_ALE_IP_NEXT_HDR_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2D8h

Figure 7-357. CPSW_STAT1_ALE_IP_NEXT_HDR_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-736. CPSW_STAT1_ALE_IP_NEXT_HDR_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Next Header drop

7.11.56 CPSW_STAT1_ALE_IPV4_FRAG_DROP Register (Offset = 0003A2DCh) [reset = 0h]

CPSW_STAT1_ALE_IPV4_FRAG_DROP is shown in [Figure 7-358](#) and described in [Table 7-738](#).

Return to [Summary Table](#).

ALE IPV4 Frag Drop

Table 7-737. CPSW_STAT1_ALE_IPV4_FRAG_DROP Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A2DCh

Figure 7-358. CPSW_STAT1_ALE_IPV4_FRAG_DROP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-738. CPSW_STAT1_ALE_IPV4_FRAG_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE IPV4 Fragment drop

7.11.57 CPSW_STAT1_IET_RX_ASSEMBLY_ERROR_REG Register (Offset = 0003A340h) [reset = 0h]

CPSW_STAT1_IET_RX_ASSEMBLY_ERROR_REG is shown in [Figure 7-359](#) and described in [Table 7-740](#).

Return to [Summary Table](#).

IET Receive Assembly Error

Table 7-739.
CPSW_STAT1_IET_RX_ASSEMBLY_ERROR_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A340h

Figure 7-359. CPSW_STAT1_IET_RX_ASSEMBLY_ERROR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_ERROR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-740. CPSW_STAT1_IET_RX_ASSEMBLY_ERROR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_ASSEMBLY_ER ROR	R/W	0h	IET Receive Assembly Error

7.11.58 CPSW_STAT1_IET_RX_ASSEMBLY_OK_REG Register (Offset = 0003A344h) [reset = 0h]

CPSW_STAT1_IET_RX_ASSEMBLY_OK_REG is shown in [Figure 7-360](#) and described in [Table 7-742](#).

Return to [Summary Table](#).

IET Receive Assembly Ok

Table 7-741.
CPSW_STAT1_IET_RX_ASSEMBLY_OK_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A344h

Figure 7-360. CPSW_STAT1_IET_RX_ASSEMBLY_OK_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_OK																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-742. CPSW_STAT1_IET_RX_ASSEMBLY_OK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_ASSEMBLY_OK	R/W	0h	IET Receive Assembly Ok

7.11.59 CPSW_STAT1_IET_RX_SMD_ERROR_REG Register (Offset = 0003A348h) [reset = 0h]

CPSW_STAT1_IET_RX_SMD_ERROR_REG is shown in [Figure 7-361](#) and described in [Table 7-744](#).

[Return to Summary Table.](#)

IET Receive Smd Error

Table 7-743.
CPSW_STAT1_IET_RX_SMD_ERROR_REG
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A348h

Figure 7-361. CPSW_STAT1_IET_RX_SMD_ERROR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_SMD_ERROR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-744. CPSW_STAT1_IET_RX_SMD_ERROR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_SMD_ERROR	R/W	0h	IET Receive Smd Error

7.11.60 CPSW_STAT1_IET_RX_FRAG_REG Register (Offset = 0003A34Ch) [reset = 0h]

CPSW_STAT1_IET_RX_FRAG_REG is shown in [Figure 7-362](#) and described in [Table 7-746](#).

Return to [Summary Table](#).

IET Receive Frag

Table 7-745. CPSW_STAT1_IET_RX_FRAG_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A34Ch

Figure 7-362. CPSW_STAT1_IET_RX_FRAG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_FRAG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-746. CPSW_STAT1_IET_RX_FRAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_FRAG	R/W	0h	IET Receive Frag

7.11.61 CPSW_STAT1_IET_TX_HOLD_REG Register (Offset = 0003A350h) [reset = 0h]

CPSW_STAT1_IET_TX_HOLD_REG is shown in [Figure 7-363](#) and described in [Table 7-748](#).

Return to [Summary Table](#).

IET Transmit Hold

**Table 7-747. CPSW_STAT1_IET_TX_HOLD_REG
Instances**

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A350h

Figure 7-363. CPSW_STAT1_IET_TX_HOLD_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_TX_HOLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-748. CPSW_STAT1_IET_TX_HOLD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_TX_HOLD	R/W	0h	IET Transmit Hold

7.11.62 CPSW_STAT1_IET_TX_FRAG_REG Register (Offset = 0003A354h) [reset = 0h]

CPSW_STAT1_IET_TX_FRAG_REG is shown in [Figure 7-364](#) and described in [Table 7-750](#).

Return to [Summary Table](#).

IET Transmit Frag

Table 7-749. CPSW_STAT1_IET_TX_FRAG_REG Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A354h

Figure 7-364. CPSW_STAT1_IET_TX_FRAG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_TX_FRAG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-750. CPSW_STAT1_IET_TX_FRAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_TX_FRAG	R/W	0h	IET Transmit Frag

7.11.63 CPSW_STAT1_TX_MEMORY_PROTECT_ERROR Register (Offset = 0003A37Ch) [reset = X]

CPSW_STAT1_TX_MEMORY_PROTECT_ERROR is shown in [Figure 7-365](#) and described in [Table 7-752](#).

Return to [Summary Table](#).

Transmit Memory Protect CRC Error.

Table 7-751.
CPSW_STAT1_TX_MEMORY_PROTECT_ERROR
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1	4603 A37Ch

Figure 7-365. CPSW_STAT1_TX_MEMORY_PROTECT_ERROR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								COUNT							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-752. CPSW_STAT1_TX_MEMORY_PROTECT_ERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	COUNT	R/W	0h	Transmit Memory Protect CRC Error.

7.11.64 CPSW_STAT1_ENET_PN_TX_PRI_REG_y Register (Offset = 0003A380h + formula) [reset = 0h]

CPSW_STAT1_ENET_PN_TX_PRI_REG_y is shown in Figure 7-366 and described in Table 7-754.

Return to [Summary Table](#).

ENET Port n PRIORITY N Packet Count.

Offset = 0003A380h + (y * 4h); where y = 0h to 7h.

Table 7-753.
CPSW_STAT1_ENET_PN_TX_PRI_REG_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1_STAT0	4603 A380h + formula

Figure 7-366. CPSW_STAT1_ENET_PN_TX_PRI_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-754. CPSW_STAT1_ENET_PN_TX_PRI_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PN_TX_PRIN	R/W	0h	Enet Port n Priority N Packet Count.

7.11.65 CPSW_STAT1_ENET_PN_TX_PRI_BCNT_REG_y Register (Offset = 0003A3A0h + formula) [reset = 0h]

CPSW_STAT1_ENET_PN_TX_PRI_BCNT_REG_y is shown in [Figure 7-367](#) and described in [Table 7-756](#).

Return to [Summary Table](#).

ENET Port n PRIORITY N Packet Byte Count.

Offset = 0003A3A0h + (y * 4h); where y = 0h to 7h.

Table 7-755.
CPSW_STAT1_ENET_PN_TX_PRI_BCNT_REG_y
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1 STAT0	4603 A3A0h + formula

Figure 7-367. CPSW_STAT1_ENET_PN_TX_PRI_BCNT_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_BCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-756. CPSW_STAT1_ENET_PN_TX_PRI_BCNT_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PN_TX_PRIN_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Byte Count.

7.11.66 CPSW_STAT1_ENET_PN_TX_PRI_DROP_REG_y Register (Offset = 0003A3C0h + formula) [reset = 0h]

CPSW_STAT1_ENET_PN_TX_PRI_DROP_REG_y is shown in [Figure 7-368](#) and described in [Table 7-758](#).

Return to [Summary Table](#).

ENET Port n PRIORITY N Packet Drop Count.

Offset = 0003A3C0h + (y * 4h); where y = 0h to 7h.

Table 7-757.
CPSW_STAT1_ENET_PN_TX_PRI_DROP_REG_y
Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1_STAT0	4603 A3C0h + formula

Figure 7-368. CPSW_STAT1_ENET_PN_TX_PRI_DROP_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-758. CPSW_STAT1_ENET_PN_TX_PRI_DROP_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PN_TX_PRIN_DROP	R/W	0h	ENET Port n PRIORITY N Packet Drop Count.

7.11.67 CPSW_STAT1_ENET_PN_TX_PRI_DROP_BCNT_REG_y Register (Offset = 0003A3E0h + formula) [reset = 0h]

CPSW_STAT1_ENET_PN_TX_PRI_DROP_BCNT_REG_y is shown in [Figure 7-369](#) and described in [Table 7-760](#).

Return to [Summary Table](#).

ENET Port n PRIORITY N Packet Drop Byte Count.

Offset = 0003A3E0h + (y * 4h); where y = 0h to 7h.

Table 7-759.
CPSW_STAT1_ENET_PN_TX_PRI_DROP_BCNT_REG_y Instances

Instance	Physical Address
MCU_CPSW0_NUSS_STAT1_STAT0	4603 A3E0h + formula

Figure 7-369. CPSW_STAT1_ENET_PN_TX_PRI_DROP_BCNT_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP_BCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-760. CPSW_STAT1_ENET_PN_TX_PRI_DROP_BCNT_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PN_TX_PRIN_DROP_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Drop Byte Count.

8 CPSW0 Registers

8.1 CPSW0_ALE Registers

Table 8-2 lists the memory-mapped registers for the CPSW0_ALE. All register offset addresses not listed in Table 8-2 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. CPSW0_ALE Instances

Instance	Base Address
CPSW0_NUSS_ALE	0C00 0000h

Table 8-2. CPSW0_ALE Registers

Offset	Acronym	Register Name	CPSW0_NUSS_ALE Physical Address
0003E000h	CPSW_ALE_MOD_VER	ALE Module and Version Register	0C03 E000h
0003E004h	CPSW_ALE_STATUS	ALE Status Register	0C03 E004h
0003E008h	CPSW_ALE_CONTROL	ALE Control Register	0C03 E008h
0003E00Ch	CPSW_ALE_CTRL2	ALE Control 2 Register	0C03 E00Ch
0003E010h	CPSW_ALE_PRESCALE	ALE Prescale Register	0C03 E010h
0003E014h	CPSW_ALE_AGING_CTRL	ALE Aging Control Register	0C03 E014h
0003E01Ch	CPSW_ALE_NXT_HDR	ALE Next Header Register	0C03 E01Ch
0003E020h	CPSW_ALE_TBLCTL	ALE Table Control Register	0C03 E020h
0003E034h	CPSW_ALE_TBLW2	ALE LUT Table Word 2 Register	0C03 E034h
0003E038h	CPSW_ALE_TBLW1	ALE LUT Table Word 1 Register	0C03 E038h
0003E03Ch	CPSW_ALE_TBLW0	ALE LUT Table Word 0 Register	0C03 E03Ch
0003E040h + formula	CPSW_ly_ALE_PORTCTL0_y	ALE Port Control 0 to 8 Registers	0C03 E040h + formula
0003E090h	CPSW_ALE_UVLAN_MEMBER	ALE Unknown VLAN Member Mask Register	0C03 E090h
0003E094h	CPSW_ALE_UVLAN_URCAST	ALE Unknown VLAN Unregistered Multicast Flood Mask Register	0C03 E094h
0003E098h	CPSW_ALE_UVLAN_RMCAST	ALE Unknown VLAN Registered Multicast Flood Mask Register	0C03 E098h
0003E09Ch	CPSW_ALE_UVLAN_UNTAG	ALE Unknown VLAN Force Untagged Egress Mask Register	0C03 E09Ch
0003E0B8h	CPSW_ALE_STAT_DIAG	ALE Statistic Output Diagnostic Register	0C03 E0B8h
0003E0BCh	CPSW_ALE_OAM_LB_CTRL	ALE OAM Loopback Control Register	0C03 E0BCh
0003E0FCh	CPSW_ALE_EGRESSOP	ALE Egress Operation Register	0C03 E0FCh
0003E100h	CPSW_ALE_POLICECFG0	ALE Policing Config 0 Register	0C03 E100h
0003E104h	CPSW_ALE_POLICECFG1	ALE Policing Config 1 Register	0C03 E104h
0003E108h	CPSW_ALE_POLICECFG2	ALE Policing Config 2 Register	0C03 E108h
0003E10Ch	CPSW_ALE_POLICECFG3	ALE Policing Config 3 Register	0C03 E10Ch
0003E110h	CPSW_ALE_POLICECFG4	ALE Policing Config 4 Register	0C03 E110h
0003E118h	CPSW_ALE_POLICECFG6	ALE Policing Config 6 Register	0C03 E118h
0003E11Ch	CPSW_ALE_POLICECFG7	ALE Policing Config 7 Register	0C03 E11Ch
0003E120h	CPSW_ALE_POLICETBLCTL	Policing Table Control Register	0C03 E120h
0003E124h	CPSW_ALE_POLICECONTROL	ALE Policing Control Register	0C03 E124h
0003E128h	CPSW_ALE_POLICETESTCTL	ALE Policing Test Control Register	0C03 E128h
0003E12Ch	CPSW_ALE_POLICEHSTAT	ALE Policing Hit Status Register	0C03 E12Ch
0003E134h	CPSW_ALE_THREADMAPDEF	ALE THREAD Mapping Default Value Register	0C03 E134h
0003E138h	CPSW_ALE_THREADMAPCTL	ALE THREAD Mapping Control Register	0C03 E138h

Table 8-2. CPSW0_ALE Registers (continued)

Offset	Acronym	Register Name	CPSW0_NUSS_ALE Physical Address
0003E13Ch	CPSW_ALE_THREADMAPVAL	ALE THREAD Mapping Value Register	0C03 E13Ch

8.1.1 CPSW_ALE_MOD_VER Register (Offset = 0003E000h) [reset = 00294104h]

CPSW_ALE_MOD_VER is shown in [Figure 8-1](#) and described in [Table 8-4](#).

Return to [Summary Table](#).

The Module and Version Register identifies the module identifier and revision of the ALE module.

Table 8-3. CPSW_ALE_MOD_VER Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E000h

Figure 8-1. CPSW_ALE_MOD_VER Register

31	30	29	28	27	26	25	24
MODULE_ID							
R-29h							
23	22	21	20	19	18	17	16
MODULE_ID							
R-29h							
15	14	13	12	11	10	9	8
RTL_VERSION				MAJOR_REVISION			
R-8h				R-1h			
7	6	5	4	3	2	1	0
CUSTOM_REVISION		MINOR_REVISION					
R-0h		R-4h					

LEGEND: R = Read Only; -n = value after reset

Table 8-4. CPSW_ALE_MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODULE_ID	R	29h	ALE module ID.
15-11	RTL_VERSION	R	8h	RTL Version.
10-8	MAJOR_REVISION	R	1h	Major Revision.
7-6	CUSTOM_REVISION	R	0h	Custom Revision.
5-0	MINOR_REVISION	R	4h	Minor Revision.

8.1.2 CPSW_ALE_STATUS Register (Offset = 0003E004h) [reset = X]

CPSW_ALE_STATUS is shown in [Figure 8-2](#) and described in [Table 8-6](#).

Return to [Summary Table](#).

The ALE status provides information on the ALE configuration and state. The RAMDEPTH is used to determine how IPv6 entries are stored in the table. IPv6 entries are stored in two entries where IPv6 Entry Hi is designated by the odd slice index and Lo is designated by the even slice index. The slice index is above the ram depth like {SlixelIndex,RamIndex}. So for a 64 deep RAM index of 0x005, the Hi portion of the IPv6 entry is located at 0x005|0x040 and the Lo portion is located at 0x005&(~0x040).

Table 8-5. CPSW_ALE_STATUS Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E004h

Figure 8-2. CPSW_ALE_STATUS Register

31	30	29	28	27	26	25	24
UREGANDREG MSK12	UREGANDREG MSK08	RESERVED					
R-1h	R-0h	R-X					
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
POLCNTDIV8							
R-Ch							
7	6	5	4	3	2	1	0
RAMDEPTH12 8	RAMDEPTH32	RESERVED	KLUENTRIES				
R-0h	R-0h	R-X	R-1h				

LEGEND: R = Read Only; -n = value after reset

Table 8-6. CPSW_ALE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UREGANDREGMSK12	R	1h	When set, the unregistered multicast field is a mask versus an index on 12 bit boundary in the ALE table.
30	UREGANDREGMSK08	R	0h	When set, the unregistered multicast field is a mask versus an index on 8 bit boundary in the ALE table.
29-16	RESERVED	R	X	
15-8	POLCNTDIV8	R	Ch	This is the number of policer engines the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.
7	RAMDEPTH128	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both ramdepth128 and ramdepth32 are zero the depth is 64.
6	RAMDEPTH32	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both ramdepth128 and ramdepth32 are zero the depth is 64.
5	RESERVED	R	X	

Table 8-6. CPSW_ALE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	KLUENTRIES	R	1h	<p>This is the number of table entries total divided by 1024.</p> <p>A value of 1 indicates 1024 table entries.</p> <p>A value of 8 indicates 8192 table entries.</p>

8.1.3 CPSW_ALE_CONTROL Register (Offset = 0003E008h) [reset = X]

CPSW_ALE_CONTROL is shown in [Figure 8-3](#) and described in [Table 8-8](#).

Return to [Summary Table](#).

The ALE Control Register is used to set the ALE modes used for all ports.

Table 8-7. CPSW_ALE_CONTROL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E008h

Figure 8-3. CPSW_ALE_CONTROL Register

31	30	29	28	27	26	25	24
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NO W	RESERVED	MIRROR_DP			
R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h			
23	22	21	20	19	18	17	16
UPD_BW_CTRL			RESERVED	MIRROR_TOP			
R/W-0h			R/W-X	R/W-0h			
15	14	13	12	11	10	9	8
UPD_STATIC	RESERVED	UVLAN_NO_LE ARN	MIRROR_MEN	MIRROR_DEN	MIRROR_SEN	RESERVED	EN_HOST_UNI _FLOOD
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h
7	6	5	4	3	2	1	0
LEARN_NO_VL ANID	ENABLE_VID0 _MODE	ENABLE_OUI_ DENY	ENABLE_BYPA SS	BCAST_MCAS T_CTL	ALE_VLAN_AW ARE	ENABLE_AUTH _MODE	ENABLE_RATE _LIMIT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-8. CPSW_ALE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_ALE	R/W	0h	Enable ALE. 0h = Drop all packets 1h = Enable ALE packet processing
30	CLEAR_TABLE	R/W	0h	Clear ALE address table. Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.

Table 8-8. CPSW_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	AGE_OUT_NOW	R/W	0h	Age Out Address Table Now. Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.
28	RESERVED	R/W	X	
27-24	MIRROR_DP	R/W	0h	Mirror Destination Port. This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the MIRROR_TOP port.
23-21	UPD_BW_CTRL	R/W	0h	The UPD_BW_CTRL field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the UPD_BW_CTRL can be programmed more aggressive. If the UPD_BW_CTRL is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. 0h = 350Mhz, 5M 1h = 359Mhz, 11M 2h = 367Mhz, 16M 3h = 375Mhz, 22M 4h = 384Mhz, 28M 5h = 392Mhz, 34M 6h = 400Mhz, 39M 7h = 409Mhz, 45M
20	RESERVED	R/W	X	
19-16	MIRROR_TOP	R/W	0h	Mirror To Port. This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.
15	UPD_STATIC	R/W	0h	Update Static Entries. A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be 0h for most switch configurations.
14	RESERVED	R/W	X	
13	UVLAN_NO_LEARN	R/W	0h	Unknown VLAN No Learn. This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.

Table 8-8. CPSW_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	MIRROR_MEN	R/W	0h	Mirror Match Entry Enable. This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the MIRROR_MIDX entry index will have that traffic also sent to the MIRROR_TOP port.
11	MIRROR_DEN	R/W	0h	Mirror Destination Port Enable. This field enables the destination port mirror option. When this bit is set any traffic destined for the MIRROR_DP port will have its transmit traffic also sent to the MIRROR_TOP port.
10	MIRROR_SEN	R/W	0h	Mirror Source Port Enable. This field enables the source port mirror option. When this bit is set any port with the ly_REG_P0_MIRROR_SP set in the CPSW_ly_ALE_PORTCTL0_y registers set will have its received traffic also sent to the MIRROR_TOP port.
9	RESERVED	R/W	X	
8	EN_HOST_UNI_FLOOD	R/W	0h	Unknown unicast packets flood to host. 0h = Unknown unicast packets are not sent to the host 1h = Unknown unicast packets flood to host port as well as other ports
7	LEARN_NO_VLANID	R/W	0h	Learn No VID. 0h = VID is learned with the source address 1h = VID is not learned with the source address (source address is not tied to VID). Determines the entry type.
6	ENABLE_VID0_MODE	R/W	0h	Enable VLAN ID = 0 Mode. 0h = Process the priority tagged packet with VID = PORT_VLAN[11:0]. 1h = Process the priority tagged packet with VID = 0h.
5	ENABLE_OUI_DENY	R/W	0h	Enable OUI Deny Mode. When set, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.
4	ENABLE_BYPASS	R/W	0h	ALE Bypass. When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port. 0h = No bypass 1h = Bypass the ALE
3	BCAST_MCAST_CTL	R/W	0h	Rate Limit Transmit mode. 0h = Broadcast and multicast rate limit counters are received port based 1h = Broadcast and multicast rate limit counters are transmit port based

Table 8-8. CPSW_ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ALE_VLAN_AWARE	R/W	0h	ALE VLAN Aware. Determines how traffic is forwarded using VLAN rules. 0h = Simple switch rules, packets forwarded to all ports for unknown destinations. 1h = VLAN Aware rules, packets forwarded based on VLAN members
1	ENABLE_AUTH_MODE	R/W	0h	Enable MAC Authorization Mode. Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set). 0h = The ALE is not in MAC authorization mode 1h = The ALE is in MAC authorization mode
0	ENABLE_RATE_LIMIT	R/W	0h	Enable Broadcast and Multicast Rate Limit 0h = Broadcast/Multicast rates not limited 1h = Broadcast/Multicast packet reception limited to the port control register rate limit fields.

8.1.4 CPSW_ALE_CTRL2 Register (Offset = 0003E00Ch) [reset = X]

CPSW_ALE_CTRL2 is shown in [Figure 8-4](#) and described in [Table 8-10](#).

Return to [Summary Table](#).

The ALE Control 2 Register is used to set the extended features used for all ports.

Table 8-9. CPSW_ALE_CTRL2 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E00Ch

Figure 8-4. CPSW_ALE_CTRL2 Register

31	30	29	28	27	26	25	24
TRK_EN_DST	TRK_EN_SRC	TRK_EN_PRI	RESERVED	TRK_EN_IVLAN	RESERVED	TRK_EN_SIP	TRK_EN_DIP
R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-X	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DROP_BADLEN	NODROP_SRCMCST	DEFNOFRAG	DEFLMTNXTHDR	RESERVED	TRK_BASE		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						MIRROR_MIDX	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
MIRROR_MIDX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-10. CPSW_ALE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK_EN_DST	R/W	0h	Trunk Enable Destination Address. This field enables the destination MAC address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.
30	TRK_EN_SRC	R/W	0h	Trunk Enable Source Address. This field enables the source MAC address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.
29	TRK_EN_PRI	R/W	0h	Trunk Enable Priority. This field enables the VLAN Priority bits to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used.
28	RESERVED	R/W	X	
27	TRK_EN_IVLAN	R/W	0h	Trunk Enable Inner VLAN. This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.
26	RESERVED	R/W	X	

Table 8-10. CPSW_ALE_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	TRK_EN_SIP	R/W	0h	Trunk Enable Source IP Address. This field enables the source IP address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
24	TRK_EN_DIP	R/W	0h	Trunk Enable Destination IP Address. This field enables the destination IP address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
23	DROP_BADLEN	R/W	0h	Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.
22	NODROP_SRCMCST	R/W	0h	No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.
21	DEFNOFRAG	R/W	0h	Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.
20	DEFLMTNXTHDR	R/W	0h	Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the CPSW_ALE_NXT_HDR register values.
19	RESERVED	R/W	X	
18-16	TRK_BASE	R/W	0h	Trunk Base - This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the [31]TRK_EN_DST, [30]TRK_EN_SRC, [29]TRK_EN_PRI and [27]TRK_EN_IVLAN are cleared (value: 0h), this value is used as the distribution index. That is a 0h will select the 1st bit of an 'N' link trunk, a 1h will select the second, etc. Below is the distribution across the trunk links. The first number in the sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0h will go to the base port (0), hash result 1h will go to the highest port of the trunk group (2), hash result 2h will go to the middle port (1), etc. 1h = 00000000 2h = 01010101 3h = 02102102 4h = 03210321
15-10	RESERVED	R/W	X	
9-0	MIRROR_MIDX	R/W	0h	Mirror Index. This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the MIRROR_TOP port. That is any VLAN, ONU or address with or without VLAN can be selected for traffic mirroring.

8.1.5 CPSW_ALE_PRESCALE Register (Offset = 0003E010h) [reset = X]

CPSW_ALE_PRESCALE is shown in [Figure 8-5](#) and described in [Table 8-12](#).

Return to [Summary Table](#).

The ALE Prescale Register is used to set the Broadcast and Multicast rate limiting prescaler value.

Table 8-11. CPSW_ALE_PRESCALE Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E010h

Figure 8-5. CPSW_ALE_PRESCALE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ALE_PRESCALE																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-12. CPSW_ALE_PRESCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	ALE_PRESCALE	R/W	0h	ALE Prescale. The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 10h. The prescaler is off when the value is zero.

8.1.6 CPSW_ALE_AGING_CTRL Register (Offset = 0003E014h) [reset = X]

CPSW_ALE_AGING_CTRL is shown in [Figure 8-6](#) and described in [Table 8-14](#).

Return to [Summary Table](#).

The ALE Aging Control sets the aging interval which will cause periodic aging to occur. This value specifies the minimum time between aging starts.

Table 8-13. CPSW_ALE_AGING_CTRL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E014h

Figure 8-6. CPSW_ALE_AGING_CTRL Register

31	30	29	28	27	26	25	24
PRESALE_2_DISABLE	PRESALE_1_DISABLE	RESERVED					
R/W-0h	R/W-0h	R/W-X					
23	22	21	20	19	18	17	16
ALE_AGING_TIMER							
R/W-0h							
15	14	13	12	11	10	9	8
ALE_AGING_TIMER							
R/W-0h							
7	6	5	4	3	2	1	0
ALE_AGING_TIMER							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-14. CPSW_ALE_AGING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESALE_2_DISABLE	R/W	0h	ALE Prescaler 2 Disable. When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
30	PRESALE_1_DISABLE	R/W	0h	ALE Prescaler 1 Disable. When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
29-24	RESERVED	R/W	X	
23-0	ALE_AGING_TIMER	R/W	0h	ALE Aging Timer. This field specifies the number of clock cycles times 1,000,000 between aging operations.

8.1.7 CPSW_ALE_NXT_HDR Register (Offset = 0003E01Ch) [reset = 0h]

CPSW_ALE_NXT_HDR is shown in [Figure 8-7](#) and described in [Table 8-16](#).

Return to [Summary Table](#).

The ALE Next Header is used to limit the IPv6 Next header or IPv4 Protocol values found in the IP header. It is enabled via the DEFLMTNXTHDR bit in the VLAN entry. All four IP_NXT_HDR0 to IP_NXT_HDR3 bits are compared when enabled, so if only one is required, set them all to the one value to be tested.

Table 8-15. CPSW_ALE_NXT_HDR Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E01Ch

Figure 8-7. CPSW_ALE_NXT_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP_NXT_HDR3								IP_NXT_HDR2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_NXT_HDR1								IP_NXT_HDR0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-16. CPSW_ALE_NXT_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	IP_NXT_HDR3	R/W	0h	The IP_NXT_HDR3 is the forth protocol or next header compared when enabled.
23-16	IP_NXT_HDR2	R/W	0h	The IP_NXT_HDR2 is the third protocol or next header compared when enabled.
15-8	IP_NXT_HDR1	R/W	0h	The IP_NXT_HDR1 is the second protocol or next header compared when enabled.
7-0	IP_NXT_HDR0	R/W	0h	The IP_NXT_HDR0 is the first protocol or next header compared when enabled.

8.1.8 CPSW_ALE_TBLCTL Register (Offset = 0003E020h) [reset = X]

CPSW_ALE_TBLCTL is shown in [Figure 8-8](#) and described in [Table 8-18](#).

Return to [Summary Table](#).

The ALE table control register is used to read or write that ALE table entries. After writing to this register any read or write to any ALE register will be stalled until the read or write operation completes.

Table 8-17. CPSW_ALE_TBLCTL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E020h

Figure 8-8. CPSW_ALE_TBLCTL Register

31	30	29	28	27	26	25	24
TABLEWR	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						TABLEIDX	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
TABLEIDX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-18. CPSW_ALE_TBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TABLEWR	R/W	0h	Table Write. This bit is used to write the table words to the lookup table. 0h = Table Read Operation is performed. The contents of the TABLEIDX bit will be read into the CPSW_ALE_TBLWx registers (where x = 0 to 2). 1h = Table write operation is performed. This will take the current contents from the CPSW_ALE_TBLWx registers and write them to the table at the specified TABLEIDX.
30-10	RESERVED	R/W	X	
9-0	TABLEIDX	R/W	0h	The table index is used to determine which lookup table entry is read or written.

8.1.9 CPSW_ALE_TBLW2 Register (Offset = 0003E034h) [reset = X]

CPSW_ALE_TBLW2 is shown in [Figure 8-9](#) and described in [Table 8-20](#).

Return to [Summary Table](#).

The ALE Table Word 2 is the most significant word of an ALE table entry.

Table 8-19. CPSW_ALE_TBLW2 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E034h

Figure 8-9. CPSW_ALE_TBLW2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TABLEWRD2													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-20. CPSW_ALE_TBLW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	TABLEWRD2	R/W	0h	Table Entry bits [75:64].

8.1.10 CPSW_ALE_TBLW1 Register (Offset = 0003E038h) [reset = 0h]

CPSW_ALE_TBLW1 is shown in [Figure 8-10](#) and described in [Table 8-22](#).

Return to [Summary Table](#).

The ALE Table Word 1 is the middle word of an ALE table entry.

Table 8-21. CPSW_ALE_TBLW1 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E038h

Figure 8-10. CPSW_ALE_TBLW1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEWRD1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-22. CPSW_ALE_TBLW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TABLEWRD1	R/W	0h	Table Entry bits [63:32].

8.1.11 CPSW_ALE_TBLW0 Register (Offset = 0003E03Ch) [reset = 0h]

CPSW_ALE_TBLW0 is shown in [Figure 8-11](#) and described in [Table 8-24](#).

Return to [Summary Table](#).

The ALE Table Word 0 is the least significant word of an ALE table entry.

Table 8-23. CPSW_ALE_TBLW0 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E03Ch

Figure 8-11. CPSW_ALE_TBLW0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEWRD0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-24. CPSW_ALE_TBLW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TABLEWRD0	R/W	0h	Table Entry bits [31:0].

8.1.12 CPSW_ly_ALE_PORTCTL0_y Register (Offset = 0003E040h + formula) [reset = X]

CPSW_ly_ALE_PORTCTL0_y is shown in [Figure 8-12](#) and described in [Table 8-26](#).

Return to [Summary Table](#).

The ALE Port Control Register sets the port specific modes of operation.

Offset = 0003E040h + (y * 4h); where y = 0h to 8h

Table 8-25. CPSW_ly_ALE_PORTCTL0_y Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E040h + formula

Figure 8-12. CPSW_ly_ALE_PORTCTL0_y Register

31	30	29	28	27	26	25	24
ly_REG_Py_BCAST_LIMIT							
R/W-0h							
23	22	21	20	19	18	17	16
ly_REG_Py_MCAST_LIMIT							
R/W-0h							
15	14	13	12	11	10	9	8
ly_REG_Py_DR OP_DOUBLE_ VLAN	ly_REG_Py_DR OP_DUAL_VLA N	ly_REG_Py_M ACONLY_CAF	ly_REG_Py_DI S_PAUTHMOD	ly_REG_Py_M ACONLY	ly_REG_Py_TR UNKEN	ly_REG_Py_TRUNKNUM	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
ly_REG_Py_MI RROR_SP	RESERVED	ly_REG_Py_N O_SA_UPDATE	ly_REG_Py_N O_LEARN	ly_REG_Py_VI D_INGRESS_C HECK	ly_REG_Py_DR OP_UN_TAGG ED	ly_REG_Py_PORTSTATE	
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-26. CPSW_ly_ALE_PORTCTL0_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ly_REG_Py_BCAST_LIMI T	R/W	0h	Broadcast Packet Rate Limit. Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23-16	ly_REG_Py_MCAST_LIMI T	R/W	0h	Multicast Packet Rate Limit. Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field. The ly_REG_Py_MCAST_LIMIT bit field is the number of Multicast packets that will be forwarded per CPSW_ALE_PRESCALE time.

Table 8-26. CPSW_Iy_ALE_PORTCTL0_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	Iy_REG_Py_DROP_DOUBLE_VLAN	R/W	0h	Drop Double VLAN. When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.
14	Iy_REG_Py_DROP_DUAL_VLAN	R/W	0h	Drop Dual VLAN. When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.
13	Iy_REG_Py_MACONLY_CAF	R/W	0h	Mac Only Copy All Frames. When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with Iy_REG_Py_MACONLY set.
12	Iy_REG_Py_DIS_PAUTH_MOD	R/W	0h	Disable Port authorization. When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.
11	Iy_REG_Py_MACONLY	R/W	0h	MAC Only. When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the Iy_REG_Py_MACONLY bit set and the Iy_REG_Py_NO_LEARN also set. If Iy_REG_Py_MACONLY bit is set and the Iy_REG_Py_NO_LEARN is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that The host can broadcast to all ports including MacOnly ports in this mode.
10	Iy_REG_Py_TRUNKEN	R/W	0h	Trunk Enable. This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the Iy_REG_Py_TRUNKEN its set and having the same Iy_REG_Py_TRUNKNUM will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never trasnmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry.
9-8	Iy_REG_Py_TRUNKNUM	R/W	0h	Trunk Number. This field is used as the trunk number when the Iy_REG_Py_TRUNKEN is also set. Ports with the same trunk number that have the Iy_REG_Py_TRUNKEN also set will have traffic distributed within the trunk based on the result of the hash function described above.
7	Iy_REG_Py_MIRROR_SP	R/W	0h	Mirror Source Port. This field enables the source port mirror option. When this bit is set any traffic received on the port with the Iy_REG_Py_MIRROR_SP bit set will have its received traffic also sent to the MIRROR_TOP port.
6	RESERVED	R/W	X	
5	Iy_REG_Py_NO_SA_UPD_ATE	R/W	0h	No Source Address Update. When set will not update the source addresses for this port.
4	Iy_REG_Py_NO_LEARN	R/W	0h	No Learn. When set will not learn the source addresses for this port.

Table 8-26. CPSW_ly_ALE_PORTCTL0_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	ly_REG_Py_VID_INGRES S_CHECK	R/W	0h	VLAN Ingress Check. When set if a packet received is not a member of the VLAN, the packet will be dropped.
2	ly_REG_Py_DROP_UN_T AGGED	R/W	0h	If Drop Untagged. When set will drop packets without a VLAN tag.
1-0	ly_REG_Py_PORTSTATE	R/W	0h	Port State. Defines the current port state used for lookup operations. 0h = Disabled 1h = Blocked 2h = Learning 3h = Forwarding

8.1.13 CPSW_ALE_UVLAN_MEMBER Register (Offset = 0003E090h) [reset = X]

CPSW_ALE_UVLAN_MEMBER is shown in [Figure 8-13](#) and described in [Table 8-28](#).

Return to [Summary Table](#).

The ALE Unknown VLAN Member Mask Register is used to specify the member list for unknown VLAN ID.

Table 8-27. CPSW_ALE_UVLAN_MEMBER Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E090h

Figure 8-13. CPSW_ALE_UVLAN_MEMBER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								UVLAN_MEMBER_LIST							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-28. CPSW_ALE_UVLAN_MEMBER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	UVLAN_MEMBER_LIST	R/W	0h	Unknown VLAN Member List. Each bit represents the port member status for unknown VLANs.

8.1.14 CPSW_ALE_UVLAN_URCAST Register (Offset = 0003E094h) [reset = X]

CPSW_ALE_UVLAN_URCAST is shown in [Figure 8-14](#) and described in [Table 8-30](#).

Return to [Summary Table](#).

The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is used to specify which egress ports unregistered multicast addresses egress for the unregistered VLAN ID.

Table 8-29. CPSW_ALE_UVLAN_URCAST Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E094h

Figure 8-14. CPSW_ALE_UVLAN_URCAST Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							UVLAN_UNREG_MCAST_FLOOD_MASK
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
UVLAN_UNREG_MCAST_FLOOD_MASK							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-30. CPSW_ALE_UVLAN_URCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	UVLAN_UNREG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Unregister Multicast Flood Mask. Each bit represents the port to which unregistered multicast are sent for unregistered VLANs.

8.1.15 CPSW_ALE_UVLAN_RMCAST Register (Offset = 0003E098h) [reset = X]

CPSW_ALE_UVLAN_RMCAST is shown in [Figure 8-15](#) and described in [Table 8-32](#).

Return to [Summary Table](#).

The ALE Unknown VLAN Registered Multicast Flood Mask Register is used to specify which egress ports registered multicast addresses egress for the unregistered VLAN ID.

Table 8-31. CPSW_ALE_UVLAN_RMCAST Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E098h

Figure 8-15. CPSW_ALE_UVLAN_RMCAST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								UVLAN_REG_MCAST_FLOOD_MASK							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-32. CPSW_ALE_UVLAN_RMCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	UVLAN_REG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Register Multicast Flood Mask. Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs.

8.1.16 CPSW_ALE_UVLAN_UNTAG Register (Offset = 0003E09Ch) [reset = X]

CPSW_ALE_UVLAN_UNTAG is shown in [Figure 8-16](#) and described in [Table 8-34](#).

Return to [Summary Table](#).

The ALE Unknown VLAN force Untagged Egress Mask Register is used to specify which egress ports the VLAN ID will be removed.

Table 8-33. CPSW_ALE_UVLAN_UNTAG Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E09Ch

Figure 8-16. CPSW_ALE_UVLAN_UNTAG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								UVLAN_FORCE_UNTAGGED_EGRESS							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-34. CPSW_ALE_UVLAN_UNTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	UVLAN_FORCE_UNTAGGED_EGRESS	R/W	0h	Unknown VLAN Force Untagged Egress Mask. Each bit represents the port where the VLAN will be removed for unregistered VLANs.

8.1.17 CPSW_ALE_STAT_DIAG Register (Offset = 0003E0B8h) [reset = X]

CPSW_ALE_STAT_DIAG is shown in [Figure 8-17](#) and described in [Table 8-36](#).

Return to [Summary Table](#).

The ALE Statistic Output Diagnostic Register allows the output statistics to diagnose the SW counters. This register is for diagnostic only.

Table 8-35. CPSW_ALE_STAT_DIAG Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E0B8h

Figure 8-17. CPSW_ALE_STAT_DIAG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PBCAST_DIAG	RESERVED			PORT_DIAG			
R/W-0h	R/W-X			R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				STAT_DIAG			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-36. CPSW_ALE_STAT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	PBCAST_DIAG	R/W	0h	When set and the PORT_DIAG is set to zero, will allow all ports to see the same stat diagnostic increment.
14-12	RESERVED	R/W	X	
11-8	PORT_DIAG	R/W	0h	The port selected that a received packet will cause the selected error to increment.
7-4	RESERVED	R/W	X	

Table 8-36. CPSW_ALE_STAT_DIAG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	STAT_DIAG	R/W	0h	<p>When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port.</p> <p>0h = Disabled 1h = Destination Equal Source Drop Stat will count 2h = VLAN Ingress Check Drop Stat will count 3h = Source Multicast Drop Stat will count 4h = Dual VLAN Drop Stat will count 5h = Ether Type length error Drop Stat will count 6h = Next Hop Limit Drop Stat will count 7h = IPv4 Fragment Drop Stat will count 8h = Classifier Hit Stat will count 9h = Classifier Red Drop Stat will count 10h = Classifier Yellow Drop Stat will count 11h = ALE Overflow Drop Stat will count 12h = Rate Limit Drop Stat will count 13h = Blocked Address Drop Stat will count 14h = Secure Address Drop Stat will count 15h = Authorization Drop Stat will count</p>

8.1.18 CPSW_ALE_OAM_LB_CTRL Register (Offset = 0003E0BCh) [reset = X]

CPSW_ALE_OAM_LB_CTRL is shown in [Figure 8-18](#) and described in [Table 8-38](#).

Return to [Summary Table](#).

The ALE OAM Control allows ports to be put into OAM Loopback, only non-supervisor packet are looped back to the source port.

Table 8-37. CPSW_ALE_OAM_LB_CTRL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E0BCh

Figure 8-18. CPSW_ALE_OAM_LB_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								OAM_LB_CTRL							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-38. CPSW_ALE_OAM_LB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	OAM_LB_CTRL	R/W	0h	The OAM_LB_CTRL bit field allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an CPSW_ALE_EGRESSOP of 0xFF which swaps the source and destination address. BPDUs will still flow through as normal so that OAM can be remotely requested and disabled.

8.1.19 CPSW_ALE_EGRESSOP Register (Offset = 0003E0FCh) [reset = X]

CPSW_ALE_EGRESSOP is shown in [Figure 8-19](#) and described in [Table 8-40](#).

Return to [Summary Table](#).

The Egress Operation register allows enabled classifiers with IPSA or IPDA match to use the CPSW Egress Packet Operations Inter VLAN Routing sub functions. If the packet was destined for the host, but matches a classifier that has a programmed egress opcode, it will be forwarded to the destination ports where the destination ports will use the thier egress opcode entry to modify the packet. InterVLAN Routing and mirroring need to be understood, they are orthogonal functions.

Table 8-39. CPSW_ALE_EGRESSOP Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E0FCh

Figure 8-19. CPSW_ALE_EGRESSOP Register

31	30	29	28	27	26	25	24
EGRESS_OP							
R/W-0h							
23	22	21	20	19	18	17	16
EGRESS_TRK			TTL_CHECK	RESERVED			
R/W-0h			R/W-0h	R/W-X			
15	14	13	12	11	10	9	8
RESERVED							DEST_PORTS
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
DEST_PORTS							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-40. CPSW_ALE_EGRESSOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	EGRESS_OP	R/W	0h	The Egress Operation defines the operation performed by the CPSW Egress Packet Operations 0h = NOP : 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load. FFh: Swaps source address (SA) and destination address (DA) of packet, this is intended to allow OAM diagnostics for a link.
23-21	EGRESS_TRK	R/W	0h	The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.
20	TTL_CHECK	R/W	0h	The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.
19-9	RESERVED	R/W	X	

Table 8-40. CPSW_ALE_EGRESSOP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-0	DEST_PORTS	R/W	0h	<p>The Destination Ports is a list of the ports the classified packet will be set to.</p> <p>If a destination is a Trunk, all the port bits for that trunk must be set.</p>

8.1.20 CPSW_ALE_POLICECFG0 Register (Offset = 0003E100h) [reset = X]

CPSW_ALE_POLICECFG0 is shown in [Figure 8-20](#) and described in [Table 8-42](#).

Return to [Summary Table](#).

The Policing Config 0 holds the port, frame priority and ONU address index as well as match enables for port, frame priority and ONU address matching.

Table 8-41. CPSW_ALE_POLICECFG0 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E100h

Figure 8-20. CPSW_ALE_POLICECFG0 Register

31	30	29	28	27	26	25	24
PORT_MEN	TRUNKID	RESERVED	PORT_NUM			RESERVED	
R/W-0h	R/W-0h	R/W-X	R/W-0h			R/W-X	
23	22	21	20	19	18	17	16
RESERVED				PRI_MEN	PRI_VAL		
R/W-X				R/W-0h	R/W-0h		
15	14	13	12	11	10	9	8
ONU_MEN	RESERVED					ONU_INDEX	
R/W-0h	R/W-X					R/W-0h	
7	6	5	4	3	2	1	0
ONU_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-42. CPSW_ALE_POLICECFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PORT_MEN	R/W	0h	Port Match Enable. Enabled port match for the selected policing/classifier entry.
30	TRUNKID	R/W	0h	Trunk ID. When set indicates the port number is a trunk group.
29	RESERVED	R/W	X	
28-25	PORT_NUM	R/W	0h	Port Number. Specifies the port address to match for the selected policing/classifier entry.
24-20	RESERVED	R/W	X	
19	PRI_MEN	R/W	0h	Priority Match Enable. Enables frame priority match for the selected policing/classifier entry.
18-16	PRI_VAL	R/W	0h	Priority Value. Specifies the frame priority to match for the selected policing/classifier entry.
15	ONU_MEN	R/W	0h	OUI Match Enable. Enables frame ONU address match for the selected policing/classifier entry.
14-10	RESERVED	R/W	X	

Table 8-42. CPSW_ALE_POLICECFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	ONU_INDEX	R/W	0h	OUI Table Entry Index. Specifies the ALE ONU address lookup table index to match for the selected policing/classifier entry

8.1.21 CPSW_ALE_POLICECFG1 Register (Offset = 0003E104h) [reset = X]

CPSW_ALE_POLICECFG1 is shown in [Figure 8-21](#) and described in [Table 8-44](#).

Return to [Summary Table](#).

The Policing Config 1 holds the match enable/match index for the L2 Destination and L2 source addresses.

Table 8-43. CPSW_ALE_POLICECFG1 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E104h

Figure 8-21. CPSW_ALE_POLICECFG1 Register

31	30	29	28	27	26	25	24
DST_MEN	RESERVED					DST_INDEX	
R/W-0h	R/W-X					R/W-0h	
23	22	21	20	19	18	17	16
DST_INDEX							
R/W-0h							
15	14	13	12	11	10	9	8
SRC_MEN	RESERVED					SRC_INDEX	
R/W-0h	R/W-X					R/W-0h	
7	6	5	4	3	2	1	0
SRC_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-44. CPSW_ALE_POLICECFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DST_MEN	R/W	0h	Destination Address Match Enable - Enables frame L2 destination address match for the selected policing/classifier entry
30-26	RESERVED	R/W	X	
25-16	DST_INDEX	R/W	0h	Destination Address Table Entry Index - Specifies the ALE L2 destination address lookup table index to match for the selected policing/classifier entry
15	SRC_MEN	R/W	0h	Source Address Match Enable - Enables frame L2 source address match for the selected policing/classifier entry
14-10	RESERVED	R/W	X	
9-0	SRC_INDEX	R/W	0h	Source Address Table Entry Index - Specifies the ALE L2 source address lookup table index to match for the selected policing/classifier entry

8.1.22 CPSW_ALE_POLICECFG2 Register (Offset = 0003E108h) [reset = X]

CPSW_ALE_POLICECFG2 is shown in [Figure 8-22](#) and described in [Table 8-46](#).

Return to [Summary Table](#).

The Policing Config 2 holds the match enable/match index for the Outer VLAN and Inner VLAN addresses.

Note: VLAN ID must be tagged inside the ethernet packet for this function to work.

Table 8-45. CPSW_ALE_POLICECFG2 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E108h

Figure 8-22. CPSW_ALE_POLICECFG2 Register

31	30	29	28	27	26	25	24
OVLAN_MEN	RESERVED					OVLAN_INDEX	
R/W-0h	R/W-X					R/W-0h	
23	22	21	20	19	18	17	16
OVLAN_INDEX							
R/W-0h							
15	14	13	12	11	10	9	8
IVLAN_MEN	RESERVED					IVLAN_INDEX	
R/W-0h	R/W-X					R/W-0h	
7	6	5	4	3	2	1	0
IVLAN_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-46. CPSW_ALE_POLICECFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVLAN_MEN	R/W	0h	Outer VLAN Match Enable. Enables frame Outer VLAN address match for the selected policing/ classifier entry. Note: VLAN ID must be tagged inside the ethernet packet for this function to work.
30-26	RESERVED	R/W	X	
25-16	OVLAN_INDEX	R/W	0h	Outer VLAN Table Entry Index. Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/ classifier entry.
15	IVLAN_MEN	R/W	0h	Inner VLAN Match Enable. Enables frame Inner VLAN address match for the selected policing/ classifier entry. Note: VLAN ID must be tagged inside the ethernet packet for this function to work.
14-10	RESERVED	R/W	X	
9-0	IVLAN_INDEX	R/W	0h	Inner VLAN Table Entry Index. Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/ classifier entry.

8.1.23 CPSW_ALE_POLICECFG3 Register (Offset = 0003E10Ch) [reset = X]

CPSW_ALE_POLICECFG3 is shown in [Figure 8-23](#) and described in [Table 8-48](#).

Return to [Summary Table](#).

The Policing Config 3 holds the match enable/match index for the Ether Type and IP Source address.

Table 8-47. CPSW_ALE_POLICECFG3 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E10Ch

Figure 8-23. CPSW_ALE_POLICECFG3 Register

31	30	29	28	27	26	25	24
ETHERTYPE_MEN	RESERVED					ETHERTYPE_INDEX	
R/W-0h	R/W-X					R/W-0h	
23	22	21	20	19	18	17	16
ETHERTYPE_INDEX							
R/W-0h							
15	14	13	12	11	10	9	8
IPSRC_MEN	RESERVED					IPSRC_INDEX	
R/W-0h	R/W-X					R/W-0h	
7	6	5	4	3	2	1	0
IPSRC_INDEX							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-48. CPSW_ALE_POLICECFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ETHERTYPE_MEN	R/W	0h	EtherType Match Enable. Enables frame Ether Type match for the selected policing/ classifier entry.
30-26	RESERVED	R/W	X	
25-16	ETHERTYPE_INDEX	R/W	0h	EtherType Table Entry Index. Specifies the ALE Ether Type lookup table index to match for the selected policing/ classifier entry.
15	IPSRC_MEN	R/W	0h	IP Source Address Match Enable. Enables frame IP Source address match for the selected policing/ classifier entry.
14-10	RESERVED	R/W	X	
9-0	IPSRC_INDEX	R/W	0h	IP Source Address Table Entry Index. Specifies the ALE IP Source address lookup table index to match for the selected policing/ classifier entry.

8.1.24 CPSW_ALE_POLICECFG4 Register (Offset = 0003E110h) [reset = X]

CPSW_ALE_POLICECFG4 is shown in [Figure 8-24](#) and described in [Table 8-50](#).

Return to [Summary Table](#).

The Policing Config 4 holds the match enable/match index for the IP Destination address.

Table 8-49. CPSW_ALE_POLICECFG4 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E110h

Figure 8-24. CPSW_ALE_POLICECFG4 Register

31	30	29	28	27	26	25	24
IPDST_MEN	RESERVED					IPDST_INDEX	
R/W-0h	R/W-X					R/W-0h	
23	22	21	20	19	18	17	16
IPDST_INDEX							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-50. CPSW_ALE_POLICECFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPDST_MEN	R/W	0h	IP Destination Address Match Enable. Enables frame IP Destination address match for the selected policing/ classifier entry.
30-26	RESERVED	R/W	X	
25-16	IPDST_INDEX	R/W	0h	IP Destination Address Table Entry Index. Specifies the ALE IP Destination address lookup table index to match for the selected policing/ classifier entry.
15-0	RESERVED	R/W	X	

8.1.25 CPSW_ALE_POLICECFG6 Register (Offset = 0003E118h) [reset = 0h]

CPSW_ALE_POLICECFG6 is shown in [Figure 8-25](#) and described in [Table 8-52](#).

Return to [Summary Table](#).

The PIR counter is a 37-bit internal counter where PIR_IDLE_INC_VAL is added every clock and the frame size << 18 is subtracted at EOF if not RED at LUT time. If the counter is negative the packet will be marked RED, else it can be YELLOW or GREEN based on the CIR counter. If only this counter is used (CIR_IDLE_INC_VAL = 0h), then packets are marked RED or GREEN based on PIR counter only.

Table 8-51. CPSW_ALE_POLICECFG6 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E118h

Figure 8-25. CPSW_ALE_POLICECFG6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIR_IDLE_INC_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-52. CPSW_ALE_POLICECFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PIR_IDLE_INC_VAL	R/W	0h	Peak Information Rate Idle Increment Value. The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED.

8.1.26 CPSW_ALE_POLICECFG7 Register (Offset = 0003E11Ch) [reset = 0h]

CPSW_ALE_POLICECFG7 is shown in [Figure 8-26](#) and described in [Table 8-54](#).

Return to [Summary Table](#).

The CIR counter is a 37-bit internal counter where CIR_IDLE_INC_VAL is added every clock and the frame size << 18 is subtracted at EOF if not RED or YELLOW at LUT time. If the counter is positive the packet will be marked GREEN, else it can be YELLOW or RED based on the PIR counter. If only this counter is used (PIR_IDLE_INC_VAL= 0h), then packets are marked YELLOW or GREEN based on CIR counter only.

Table 8-53. CPSW_ALE_POLICECFG7 Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E11Ch

Figure 8-26. CPSW_ALE_POLICECFG7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CIR_IDLE_INC_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-54. CPSW_ALE_POLICECFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CIR_IDLE_INC_VAL	R/W	0h	Committed Information Idle Increment Value. The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW.

8.1.27 CPSW_ALE_POLICETBLCTL Register (Offset = 0003E120h) [reset = X]

CPSW_ALE_POLICETBLCTL is shown in [Figure 8-27](#) and described in [Table 8-56](#).

Return to [Summary Table](#).

The Policing Table Control is used to read or write the selected policing/classifier entry. The selected policing/classifier entry is only read or written after this register is written based on the value of the ~iwrite_enable bit.

Table 8-55. CPSW_ALE_POLICETBLCTL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E120h

Figure 8-27. CPSW_ALE_POLICETBLCTL Register

31	30	29	28	27	26	25	24
WRITE_ENABL E	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	POL_TBL_IDX						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-56. CPSW_ALE_POLICETBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRITE_ENABLE	R/W	0h	Write Enable - Setting this bit will write the POLICECFG 0-7 to the ~ipol_tbl_idx selected policing/classifier entry. Clearing this bit will read the ~ipol_tbl_idx selected policing/classifier entry into the POLICECFG 0-7 registers.
30-7	RESERVED	R/W	X	
6-0	POL_TBL_IDX	R/W	0h	<p>Policer Entry Index - This field specifies the policing/classifier entry to be read or written.</p> <p>When writing to this field without setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be loaded into the POLICECFG 0-7 registers.</p> <p>When writing to this field with setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be updated from the POLICECFG 0-7 registers.</p>

8.1.28 CPSW_ALE_POLICECONTROL Register (Offset = 0003E124h) [reset = X]

CPSW_ALE_POLICECONTROL is shown in [Figure 8-28](#) and described in [Table 8-58](#).

Return to [Summary Table](#).

The Control Enables color marking as well as internal ALE packet dropping rules.

Table 8-57. CPSW_ALE_POLICECONTROL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E124h

Figure 8-28. CPSW_ALE_POLICECONTROL Register

31	30	29	28	27	26	25	24
POLICING_EN	RESERVED	RED_DROP_EN	YELLOW_DROP_EN	RESERVED	YELLOWTHRESH		
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
POLMCHMODE		PRIORITY_THRESHOLD_READ_EN	MAC_ONLY_DEF_DIS	RESERVED			
R/W-0h		R/W-0h	R/W-0h	R/W-X			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-58. CPSW_ALE_POLICECONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLICING_EN	R/W	0h	Policing Enable. Enables the policing to color the packets, this also enables red or yellow drop capabilities.
30	RESERVED	R/W	X	
29	RED_DROP_EN	R/W	0h	RED Drop Enable. Enables the ALE to drop the red colored packets.
28	YELLOW_DROP_EN	R/W	0h	YELLOW Drop Enable. Enables the ALE to drop yellow packets based on the YELLOWTHRESH value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature.
27	RESERVED	R/W	X	

Table 8-58. CPSW_ALE_POLICECONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-24	YELLOWTHRESH	R/W	0h	<p>Yellow Threshold.</p> <p>When set enables a portion of the yellow packets to be dropped based on the YELLOW_DROP_EN bit enable.</p> <p>0h = 100% 1h = 50% 2h = 33% 3h = 25% 4h = 20% 5h = 17% 6h = 14% 7h = 13%</p>
23-22	POLMCHMODE	R/W	0h	<p>Policing Match Mode.</p> <p>This field determines what happens to packets that fail to hit any policing/classifier entry.</p> <p>0h = No Hit packets are marked GREEN 1h = No Hit packets are marked YELLOW 2h = No Hit packets are marked RED 3h = No Hit packets are marked based on policing/ classifier entry=0 state.</p>
21	PRIORITY_THREAD_EN	R/W	0h	<p>Priority Thread Enable.</p> <p>This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.</p>
20	MAC_ONLY_DEF_DIS	R/W	0h	<p>MAC Only Default Disable.</p> <p>This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}.</p> <p>If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.</p>
19-0	RESERVED	R/W	X	

8.1.29 CPSW_ALE_POLICETESTCTL Register (Offset = 0003E128h) [reset = X]

CPSW_ALE_POLICETESTCTL is shown in [Figure 8-29](#) and described in [Table 8-60](#).

Return to [Summary Table](#).

The Policing Test Control enables the ability to determine which policing entry has been hit and whether they reported a red or yellow rate condition.

Table 8-59. CPSW_ALE_POLICETESTCTL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E128h

Figure 8-29. CPSW_ALE_POLICETESTCTL Register

31	30	29	28	27	26	25	24
POL_CLRALL_HIT	POL_CLRALL_REDHIT	POL_CLRALL_YELLOWHIT	POL_CLRSEL_ALL	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X			
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	POL_TEST_IDX						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-60. CPSW_ALE_POLICETESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_CLRALL_HIT	R/W	0h	Policer Clear. This bit clears all the policing/ classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit.
30	POL_CLRALL_REDHIT	R/W	0h	Policer Clear RED. This bit clears all the policing/ classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.
29	POL_CLRALL_YELLOWHIT	R/W	0h	Policer Clear YELLOW. This bit clears all the policing/ classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition.
28	POL_CLRSEL_ALL	R/W	0h	Police Clear Selected. This bit clears the selected policing/ classifier hit, redhit and yellowhit bits. This bit is self clearing.
27-7	RESERVED	R/W	X	
6-0	POL_TEST_IDX	R/W	0h	Policer Test Index. This field selects which policing/ classifier hit bits will be read or written.

8.1.30 CPSW_ALE_POLICEHSTAT Register (Offset = 0003E12Ch) [reset = X]

CPSW_ALE_POLICEHSTAT is shown in [Figure 8-30](#) and described in [Table 8-62](#).

Return to [Summary Table](#).

The policing hit status is a read only register that reads the hit bits of the selected policing/classifier.

Table 8-61. CPSW_ALE_POLICEHSTAT Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E12Ch

Figure 8-30. CPSW_ALE_POLICEHSTAT Register

31	30	29	28	27	26	25	24
POL_HIT	POL_REDHIT	POL_YELLOW HIT	RESERVED				
R-0h	R-0h	R-0h	R-X				
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							
R-X							

LEGEND: R = Read Only; -n = value after reset

Table 8-62. CPSW_ALE_POLICEHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_HIT	R	0h	<p>Policer Hit.</p> <p>This bit indicates that the selected policing/ classifier via the CPSW_ALE_POLICETESTCTL[2-0] POL_TEST_IDX field has been hit by a packet seen on any port that matches the policing/ classifier entry match.</p>
30	POL_REDHIT	R	0h	<p>Policer Hit RED.</p> <p>This bit indicates that the selected policing/ classifier via the CPSW_ALE_POLICETESTCTL[2-0] POL_TEST_IDX field has been hit during a RED condition by a packet seen on any port that matches the policing/ classifier entry match.</p>
29	POL_YELLOWHIT	R	0h	<p>Policer Hit YELLOW.</p> <p>This bit indicates that the selected policing/ classifier via the CPSW_ALE_POLICETESTCTL[2-0] POL_TEST_IDX field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/ classifier entry match.</p>
28-0	RESERVED	R	X	

8.1.31 CPSW_ALE_THREADMAPDEF Register (Offset = 0003E134h) [reset = X]

CPSW_ALE_THREADMAPDEF is shown in [Figure 8-31](#) and described in [Table 8-64](#).

Return to [Summary Table](#).

The THREAD Mapping Default Value register is used to set the default thread ID when no classifier is matched.

Table 8-63. CPSW_ALE_THREADMAPDEF Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E134h

Figure 8-31. CPSW_ALE_THREADMAPDEF Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
DEFTHREAD_EN	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED		DEFTHREADVAL					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-64. CPSW_ALE_THREADMAPDEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	DEFTHREAD_EN	R/W	0h	Default Tread Enable. 0h = The switch will generate its own thread ID based on port and priority if there is no classifier match. 1h = The switch will use the default thread value (DEFTHREADVAL) for the host interface thread ID if no classifier is matched.
14-6	RESERVED	R/W	X	
5-0	DEFTHREADVAL	R/W	0h	Default Thread Value. This field specifies the default thread ID value.

8.1.32 CPSW_ALE_THREADMAPCTL Register (Offset = 0003E138h) [reset = X]

CPSW_ALE_THREADMAPCTL is shown in [Figure 8-32](#) and described in [Table 8-66](#).

Return to [Summary Table](#).

The THREAD Mapping Control register allows the highest matched classifier to return a particular thread ID for traffic sent to the host. This allows particular classifier matched traffic to be placed on a particular host's queue.

Table 8-65. CPSW_ALE_THREADMAPCTL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E138h

Figure 8-32. CPSW_ALE_THREADMAPCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLASSINDEX							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-66. CPSW_ALE_THREADMAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6-0	CLASSINDEX	R/W	0h	Classifier Index - This is the classifier index entry that the thread enable and thread value will be read or written by the CPSW_ALE_THREADMAPVAL register. Classifier Index. This is the classifier index entry that the thread enable and thread value will be read or written by the CPSW_ALE_THREADMAPVAL[5-0] THREADVAL register.

8.1.33 CPSW_ALE_THREADMAPVAL Register (Offset = 0003E13Ch) [reset = X]

CPSW_ALE_THREADMAPVAL is shown in [Figure 8-33](#) and described in [Table 8-68](#).

Return to [Summary Table](#).

The THREAD Mapping Value register is used to set the thread ID for a particular classifier entry.

Table 8-67. CPSW_ALE_THREADMAPVAL Instances

Instance	Physical Address
CPSW0_NUSS_ALE	0C03 E13Ch

Figure 8-33. CPSW_ALE_THREADMAPVAL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
THREAD_EN	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED		THREADVAL					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-68. CPSW_ALE_THREADMAPVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	THREAD_EN	R/W	0h	Thread Enable. 0h = The the thread ID will be determined by the CPSW_ALE_THREADMAPDEF register settings. 1h = The switch will use the [5-0] THREADVAL for the selected classifier match.
14-6	RESERVED	R/W	X	
5-0	THREADVAL	R/W	0h	Thread Value. This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.

8.2 CPSW0_CONTROL Registers

Table 8-70 lists the memory-mapped registers for the CPSW0_CONTROL. All register offset addresses not listed in Table 8-70 should be considered as reserved locations and the register contents should not be modified.

Table 8-69. CPSW0_CONTROL Instances

Instance	Base Address
CPSW0_NUSS_CONTROL	0C00 0000h

Table 8-70. CPSW0_CONTROL Registers5

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_CO NTROL Physical Address
00020000h	CPSW_ID_VER_REG	ID Version Register	0C02 0000h
00020004h	CPSW_CONTROL_REG	Control Register	0C02 0004h
00020010h	CPSW_EM_CONTROL_REG	Emulation Control Register	0C02 0010h
00020014h	CPSW_STAT_PORT_EN_REG	Statistics Port Enable Register	0C02 0014h
00020018h	CPSW_PTYPE_REG	Transmit Priority Type Register	0C02 0018h
0002001Ch	CPSW_SOFT_IDLE_REG	Software Idle Register	0C02 001Ch
00020020h	CPSW_THRU_RATE_REG	Thru Rate Register	0C02 0020h
00020024h	CPSW_GAP_THRESH_REG	Transmit FIFO Short Gap Threshold Register	0C02 0024h
00020028h	CPSW_TX_START_WDS_REG	Transmit FIFO Start Words Register	0C02 0028h
0002002Ch	CPSW_EEE_PRESCALE_REG	Energy Efficient Ethernet Prescale Value Register	0C02 002Ch
00020030h	CPSW_TX_G_OFLOW_THRESH_SET_REG	PFC Tx Global Out Flow Threshold Set Register	0C02 0030h
00020034h	CPSW_TX_G_OFLOW_THRESH_CLR_REG	PFC Tx Global Out Flow Threshold Clear Register	0C02 0034h
00020038h	CPSW_TX_G_BUF_THRESH_SET_L_REG	PFC Global Tx Buffer Threshold Set Low Register	0C02 0038h
0002003Ch	CPSW_TX_G_BUF_THRESH_SET_H_REG	PFC Global Tx Buffer Threshold Set High Register	0C02 003Ch
00020040h	CPSW_TX_G_BUF_THRESH_CLR_L_REG	PFC Global Tx Buffer Threshold Clear Low Register	0C02 0040h
00020044h	CPSW_TX_G_BUF_THRESH_CLR_H_REG	PFC Global Tx Buffer Threshold Clear High Register	0C02 0044h
00020050h	CPSW_VLAN_LTYPE_REG	VLAN LTYPE Outer and Inner Register	0C02 0050h
00020054h	CPSW_EST_TS_DOMAIN_REG	EST Timestamp Domain Register	0C02 0054h
00020100h	CPSW_TX_PRI0_MAXLEN_REG	Priority 0 Maximum Transmit Packet Length Register	0C02 0100h
00020104h	CPSW_TX_PRI1_MAXLEN_REG	Priority 1 Maximum Transmit Packet Length Register	0C02 0104h
00020108h	CPSW_TX_PRI2_MAXLEN_REG	Priority 2 Maximum Transmit Packet Length Register	0C02 0108h
0002010Ch	CPSW_TX_PRI3_MAXLEN_REG	Priority 3 Maximum Transmit Packet Length Register	0C02 010Ch
00020110h	CPSW_TX_PRI4_MAXLEN_REG	Priority 4 Maximum Transmit Packet Length Register	0C02 0110h
00020114h	CPSW_TX_PRI5_MAXLEN_REG	Priority 5 Maximum Transmit Packet Length Register	0C02 0114h
00020118h	CPSW_TX_PRI6_MAXLEN_REG	Priority 6 Maximum Transmit Packet Length Register	0C02 0118h
0002011Ch	CPSW_TX_PRI7_MAXLEN_REG	Priority 7 Maximum Transmit Packet Length Register	0C02 011Ch

Table 8-70. CPSW0_CONTROL Registers5 (continued)

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_CO NTROL Physical Address
00021004h	CPSW_P0_CONTROL_REG	CPPI Port 0 Control Register	0C02 1004h
00021008h	CPSW_P0_FLOW_ID_OFFSET_REG	CPPI Port 0 Transmit FLOW ID Offset Register	0C02 1008h
00021010h	CPSW_P0_BLK_CNT_REG	CPPI Port 0 FIFO Block Usage Count Register	0C02 1010h
00021014h	CPSW_P0_PORT_VLAN_REG	CPPI Port 0 VLAN Register	0C02 1014h
00021018h	CPSW_P0_TX_PRI_MAP_REG	CPPI Port 0 Tx Header Priority to Switch Priority Map Register	0C02 1018h
0002101Ch	CPSW_P0_PRI_CTL_REG	CPPI Port 0 Priority Control Register	0C02 101Ch
00021020h	CPSW_P0_RX_PRI_MAP_REG	CPPI Port 0 RX Paket Priority to Header Priority Map Register	0C02 1020h
00021024h	CPSW_P0_RX_MAXLEN_REG	CPPI Port 0 Receive Frame Max Length Register	0C02 1024h
00021028h	CPSW_P0_TX_BLKs_PRI_REG	CPPI Port 0 Transmit Block Sub Per Priority Register	0C02 1028h
00021030h	CPSW_P0_IDLE2LPI_REG	CPPI Port 0 EEE Idle to LPI Count Register	0C02 1030h
00021034h	CPSW_P0_LPI2WAKE_REG	CPPI Port 0 EEE LPI to Wakeup Count Register	0C02 1034h
00021038h	CPSW_P0_EEE_STATUS_REG	CPPI Port 0 EEE Port Status Register	0C02 1038h
00021050h	CPSW_P0_FIFO_STATUS_REG	CPPI Port 0 FIFO Status Register	0C02 1050h
00021120h + formula	CPSW_P0_RX_DSCP_MAP_REG_y	CPPI Port 0 Receive IPV4/IPV6 DSCP Map 0 to Map 7 Registers	0C02 1120h + formula
00021140h + formula	CPSW_P0_PRI_CIR_REG_y	CPPI Port 0 Rx Priority 0 to Priority 7 Committed Information Rate Registers	0C02 1140h + formula
00021160h + formula	CPSW_P0_PRI_EIR_REG_y	CPPI Port 0 Rx Priority 0 to Priority 7 Excess Information Rate Registers	0C02 1160h + formula
00021180h	CPSW_P0_TX_D_THRESH_SET_L_REG	CPPI Port 0 Tx PFC Destination Threshold Set Low Register	0C02 1180h
00021184h	CPSW_P0_TX_D_THRESH_SET_H_REG	CPPI Port 0 Tx PFC Destination Threshold Set High Register	0C02 1184h
00021188h	CPSW_P0_TX_D_THRESH_CLR_L_REG	CPPI Port 0 Tx PFC Destination Threshold Clear Low Register	0C02 1188h
0002118Ch	CPSW_P0_TX_D_THRESH_CLR_H_REG	CPPI Port 0 Tx PFC Destination Threshold Clear High Register	0C02 118Ch
00021190h	CPSW_P0_TX_G_BUF_THRESH_SET_L_REG	CPPI Port 0 Tx PFC Global Buffer Threshold Set Low Register	0C02 1190h
00021194h	CPSW_P0_TX_G_BUF_THRESH_SET_H_REG	CPPI Port 0 Tx PFC Global Buffer Threshold Set High Register	0C02 1194h
00021198h	CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG	CPPI Port 0 Tx PFC Global Buffer Threshold Clear Low Register	0C02 1198h
0002119Ch	CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG	CPPI Port 0 Tx PFC Global Buffer Threshold Clear High Register	0C02 119Ch
00021300h	CPSW_P0_SRC_ID_A_REG	CPPI Port 0 CPPI Source ID A Register	0C02 1300h
00021304h	CPSW_P0_SRC_ID_B_REG	CPPI Port 0 CPPI Source ID B Register	0C02 1304h
00021320h	CPSW_P0_HOST_BLKs_PRI_REG	CPPI Port 0 Host Blocks Priority Register	0C02 1320h

Table 8-70. CPSW0_CONTROL Registers5 (continued)

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_CO NTROL Physical Address
00022000h ⁽²⁾	CPSW_PN_RESERVED_REG_k	Reserved Register	0C02 2000h
00022004h	CPSW_PN_CONTROL_REG_k	Ethernet Port N Control Register	0C02 2004h
00022008h + formula	CPSW_PN_MAX_BLKs_REG	Ethernet Port N Maximum Blocks Register	0C02 2008h + formula
00022010h + formula	CPSW_PN_BLK_CNT_REG_k	Ethernet Port N FIFO Block Usage Count Register	0C02 2010h + formula
00022014h + formula	CPSW_PN_PORT_VLAN_REG_k	Ethernet Port N VLAN Register	0C02 2014h + formula
00022018h + formula	CPSW_PN_TX_PRI_MAP_REG_k	Ethernet Port N Tx Header Priority to Switch Priority Mapping Register	0C02 2018h + formula
0002201Ch + formula	CPSW_PN_PRI_CTL_REG_k	Ethernet Port N Priority Control Register	0C02 201Ch + formula
00022020h + formula	CPSW_PN_RX_PRI_MAP_REG_k	Ethernet Port N RX Paket Priority to Header Priority Map	0C02 2020h + formula
00022024h + formula	CPSW_PN_RX_MAXLEN_REG_k	Ethernet Port N Receive Frame Maximum Length Register	0C02 2024h + formula
00022028h + formula	CPSW_PN_TX_BLKs_PRI_REG_k	Ethernet Port N Transmit Block Sub Per Priority Register	0C02 2028h + formula
00022030h + formula	CPSW_PN_IDLE2LPI_REG_k	Ethernet Port N EEE Idle to LPI Count Register	0C02 2030h + formula
00022034h + formula	CPSW_PN_LPI2WAKE_REG_k	Ethernet Port N EEE LPI to Wake Count Register	0C02 2034h + formula
00022038h + formula	CPSW_PN_EEE_STATUS_REG_k	Ethernet Port N EEE Status Register	0C02 2038h + formula
00022040h + formula	CPSW_PN_IET_CONTROL_REG_k	Ethernet Port N IET Control Register	0C02 2040h + formula
00022044h + formula	CPSW_PN_IET_STATUS_REG_k	Ethernet Port N IET Status Register	0C02 2044h + formula
00022048h + formula	CPSW_PN_IET_VERIFY_REG_k	Ethernet Port N IET Verify Register	0C02 2048h + formula
00022050h + formula	CPSW_PN_FIFO_STATUS_REG_k	Ethernet Port N FIFO Status Register	0C02 2050h + formula
00022060h + formula	CPSW_PN_EST_CONTROL_REG_k	Ethernet Port N Enhanced Scheduled Traffic (EST) Control Register	0C02 2060h + formula
00022120h + formula	CPSW_PN_RX_DSCP_MAP_REG_k_y	Ethernet Port N Receive IPV4/IPV6 DSCP Map 0 to Map 7 Registers	0C02 2120h + formula
00022140h + formula	CPSW_PN_PRI_CIR_REG_k_y	Ethernet Port N Rx Priority 0 to Priority 7 Committed Information Rate Registers	0C02 2140h + formula
00022160h + formula	CPSW_PN_PRI_EIR_REG_k	Ethernet Port N Rx Priority 0 to Priority 7 Excess Information Rate Registers	0C02 2160h + formula
00022180h + formula	CPSW_PN_TX_D_THRESH_SET_L_REG_k	Ethernet Port N Tx PFC Destination Threshold Set Low Register	0C02 2180h + formula
00022184h + formula	CPSW_PN_TX_D_THRESH_SET_H_REG_k	Ethernet Port N Tx PFC Destination Threshold Set High Register	0C02 2184h + formula
00022188h + formula	CPSW_PN_TX_D_THRESH_CLR_L_REG_k	Ethernet Port N Tx PFC Destination Threshold Clear Low Register	0C02 2188h + formula
0002218Ch + formula	CPSW_PN_TX_D_THRESH_CLR_H_REG_k	Ethernet Port N Tx PFC Destination Threshold Clear High Register	0C02 218Ch + formula
00022190h + formula	CPSW_PN_TX_G_BUF_THRESH_SET_L_REG_k	Ethernet Port N Tx PFC Global Buffer Threshold Set Low Register	0C02 2190h + formula

Table 8-70. CPSW0_CONTROL Registers5 (continued)

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_CO NTROL Physical Address
00022194h + formula	CPSW_PN_TX_G_BUF_THRESH_SET_H_REG_k	Ethernet Port N Tx PFC Global Buffer Threshold Set High Register	0C02 2194h + formula
00022198h + formula	CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG_k	Ethernet Port N Tx PFC Global Buffer Threshold Clear Low Register	0C02 2198h + formula
0002219Ch + formula	CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG_k	Ethernet Port N Tx PFC Global Buffer Threshold Clear High Register	0C02 219Ch + formula
00022300h + formula	CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG_k	Ethernet Port N Tx Destination Out Flow Add Values Low Register	0C02 2300h + formula
00022304h + formula	CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG_k	Ethernet Port N Tx Destination Out Flow Add Values High Register	0C02 2304h + formula
00022308h + formula	CPSW_PN_SA_L_REG_k	Ethernet Port N Tx Pause Frame Source Address Low Register	0C02 2308h + formula
0002230Ch + formula	CPSW_PN_SA_H_REG_k	Ethernet Port N Tx Pause Frame Source Address High Register	0C02 230Ch + formula
00022310h + formula	CPSW_PN_TS_CTL_REG_k	Ethernet Port N Time Sync Control Register	0C02 2310h + formula
00022314h + formula	CPSW_PN_TS_SEQ_LTYPE_REG_k	Ethernet Port N Time Sync LTYPE Register (and SEQ_ID_OFFSET)	0C02 2314h + formula
00022318h + formula	CPSW_PN_TS_VLAN_LTYPE_REG_k	Ethernet Port N Time Sync VLAN2 and VLAN2 Register	0C02 2318h + formula
0002231Ch + formula	CPSW_PN_TS_CTL_LTYPE2_REG_k	Ethernet Port N Time Sync Control and LTYPE 2 Register	0C02 231Ch + formula
00022320h + formula	CPSW_PN_TS_CTL2_REG_k	Ethernet Port N Time Sync Control 2 Register	0C02 2320h + formula
00022330h + formula	CPSW_PN_MAC_CONTROL_REG_k	Ethernet Port N Mac Control Register	0C02 2330h + formula
00022334h + formula	CPSW_PN_MAC_STATUS_REG_k	Ethernet Port N Mac Status Register	0C02 2334h + formula
00022338h + formula	CPSW_PN_MAC_SOFT_RESET_REG_k	Ethernet Port N Mac Software Reset Register	0C02 2338h + formula
0002233Ch + formula	CPSW_PN_MAC_BOFFTEST_REG_k	Ethernet Port N Mac Backoff Test Register	0C02 233Ch + formula
00022340h + formula	CPSW_PN_MAC_RX_PAUSETIMER_REG_k	Ethernet Port N 802.3 Receive Pause Timer Register	0C02 2340h + formula
00022350h + formula	CPSW_PN_MAC_RXN_PAUSETIMER_REG_k_y	Ethernet Port N PFC Priority 0 to Priority 7 Rx Pause Timer Registers	0C02 2350h + formula
00022370h + formula	CPSW_PN_MAC_TX_PAUSETIMER_REG_k	Ethernet Port N 802.3 Tx Pause Timer Registers	0C02 2370h + formula
00022380h + formula	CPSW_PN_MAC_TXN_PAUSETIMER_REG_k	Ethernet Port N PFC Priority 0 to Priority 7 Tx Pause Timer Registers	0C02 2380h + formula
000223A0h + formula	CPSW_PN_MAC_EMCONTROL_REG_k	Ethernet Port N Emulation Control Register	0C02 23A0h + formula
000223A4h + formula	CPSW_PN_MAC_TX_GAP_REG_k	Ethernet Port N Tx Inter Packet Gap Register	0C02 23A4h + formula
000223ACh + formula	CPSW_PN_INTERVLAN_OPX_POINTER_REG_k	Ethernet Port N Pointer to InterVLANx (x = 1 to 4)	0C02 23ACh + formula
000223B0h + formula	CPSW_PN_INTERVLAN_OPX_A_REG_k	Ethernet Port N Pointer to InterVLANx[31:0]	0C02 23B0h + formula
000223B4h + formula	CPSW_PN_INTERVLAN_OPX_B_REG_k	Ethernet Port N Pointer to InterVLANx[63:32]	0C02 23B4h + formula
000223B8h + formula	CPSW_PN_INTERVLAN_OPX_C_REG_k	Ethernet Port N Pointer to InterVLANx[95:64]	0C02 23B8h + formula

Table 8-70. CPSW0_CONTROL Registers5 (continued)

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_CO NTROL Physical Address
000223BCh + formula	CPSW_PN_INTERVLAN_OPX_D_REG_k	Ethernet Port N Pointer to InterVLANx[129:96]	0C02 23BCh + formula

- (1) y = 0 to 7
 (2) N = 1 to 8

8.2.1 CPSW_ID_VER_REG Register (Offset = 00020000h) [reset = 6BA80101h]

CPSW_ID_VER_REG is shown in [Figure 8-34](#) and described in [Table 8-72](#).

Return to [Summary Table](#).

CPSW ID Version Register.

Table 8-71. CPSW_ID_VER_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0000h

Figure 8-34. CPSW_ID_VER_REG Register

31	30	29	28	27	26	25	24
IDENT							
R-6BA8h							
23	22	21	20	19	18	17	16
IDENT							
R-6BA8h							
15	14	13	12	11	10	9	8
RTL_VER				MAJOR_VER			
R-0h				R-1h			
7	6	5	4	3	2	1	0
CUSTOM_VER		MINOR_VER					
R-0h		R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 8-72. CPSW_ID_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	IDENT	R	6BA8h	Identification Value
15-11	RTL_VER	R	Eh	RTL Version Value
10-8	MAJOR_VER	R	1h	Major Version Value
7-6	CUSTOM_VER	R	0h	Custom Version Value
5-0	MINOR_VER	R	1h	Minor Version Value

8.2.2 CPSW_CONTROL_REG Register (Offset = 00020004h) [reset = X]

CPSW_CONTROL_REG is shown in [Figure 8-35](#) and described in [Table 8-74](#).

Return to [Summary Table](#).

CPSW Switch Control

Table 8-73. CPSW_CONTROL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0004h

Figure 8-35. CPSW_CONTROL_REG Register

31	30	29	28	27	26	25	24
ECC_CRC_MODE	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED					EST_ENABLE	IET_ENABLE	EEE_ENABLE
R/W-X					R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
P0_RX_PASS_CRC_ERR	P0_RX_PAD	P0_TX_CRC_REMOVE	P0_TX_CRC_TYPE	P8_PASS_PRI_TAGGED	P7_PASS_PRI_TAGGED	P6_PASS_PRI_TAGGED	P5_PASS_PRI_TAGGED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
P4_PASS_PRI_TAGGED	P3_PASS_PRI_TAGGED	P2_PASS_PRI_TAGGED	P1_PASS_PRI_TAGGED	P0_PASS_PRI_TAGGED	P0_ENABLE	VLAN_AWARE	S_CN_SWITCH
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-74. CPSW_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_CRC_MODE	R/W	0h	ECC CRC Mode. 0h = ECC errors induced through the ECC aggregator flip bits in the packet headers (not in packet data). 1h = ECC errors induced through the ECC aggregator flip bits in the packet data (not in the packet headers).
30-19	RESERVED	R/W	X	
18	EST_ENABLE	R/W	0h	Enhanced Scheduled Traffic enable (EST) 0h = EST is disabled 1h = EST is enabled
17	IET_ENABLE	R/W	0h	Interspersed Express Traffic enable (IET) 0h = IET is disabled 1h = IET is enabled
16	EEE_ENABLE	R/W	0h	Energy Efficient Ethernet enable 0h = Energy Efficient Ethernet is disabled 1h = Energy Efficient Ethernet is enabled
15	P0_RX_PASS_CRC_ERR	R/W	0h	Port 0 Pass Received CRC errors 0h = Packets received with CRC errors on Port 0 are dropped. 1h = Packets received with CRC errors on Port 0 are transferred to the destination ports.

Table 8-74. CPSW_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	P0_RX_PAD	R/W	0h	Port 0 Receive Short Packet Pad 0h = Short packets are dropped. 1h = Short packets are padded to 64-bytes (with pad and added CRC) if the CRC is not passed in. Short packets are dropped if the CRC is passed (in the Info0 word).
13	P0_TX_CRC_REMOVE	R/W	0h	Port 0 Transmit CRC remove. 0h = Do not remove the CRC on Port 0 transmit (egress) packets. 1h = Remove the CRC on all Port 0 transmit (egress) packets.
12	P0_TX_CRC_TYPE	R/W	0h	
11	P8_PASS_PRI_TAGGED	R/W	0h	Port 8 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P8_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
10	P7_PASS_PRI_TAGGED	R/W	0h	Port 7 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P7_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
9	P6_PASS_PRI_TAGGED	R/W	0h	Port 6 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P6_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
8	P5_PASS_PRI_TAGGED	R/W	0h	Port 5 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P5_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
7	P4_PASS_PRI_TAGGED	R/W	0h	Port 4 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P4_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
6	P3_PASS_PRI_TAGGED	R/W	0h	Port 3 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P3_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
5	P2_PASS_PRI_TAGGED	R/W	0h	Port 2 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P2_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
4	P1_PASS_PRI_TAGGED	R/W	0h	Port 1 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port Enet_P1_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
3	P0_PASS_PRI_TAGGED	R/W	0h	Port 0 Pass Priority Tagged 0h = Priority tagged packets have the zero VID replaced with the input port P0_PORT_VLAN[11:0] on ingress. 1h = Priority tagged packets are processed unchanged.
2	P0_ENABLE	R/W	0h	Port 0 Enable 0h = CPPI port (port 0) packet operations are disabled 1h = CPPI port (port 0) packet operations are enabled

Table 8-74. CPSW_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VLAN_AWARE	R/W	0h	VLAN Aware Mode: 0h = CPSW_NU is in the VLAN unaware mode. 1h = CPSW_NU is in the VLAN aware mode.
0	S_CN_SWITCH	R/W	0h	Service or Customer VLAN switch. 0h = Customer switch. VLAN processing uses the inner_vlan_ltype. 1h = Service switch. VLAN processing uses the outer_vlan_ltype.

8.2.3 CPSW_EM_CONTROL_REG Register (Offset = 00020010h) [reset = X]

CPSW_EM_CONTROL_REG is shown in [Figure 8-36](#) and described in [Table 8-76](#).

Return to [Summary Table](#).

CPSW Emulation Control Register.

Table 8-75. CPSW_EM_CONTROL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0010h

Figure 8-36. CPSW_EM_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-76. CPSW_EM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

8.2.4 CPSW_STAT_PORT_EN_REG Register (Offset = 00020014h) [reset = X]

CPSW_STAT_PORT_EN_REG is shown in [Figure 8-37](#) and described in [Table 8-78](#).

Return to [Summary Table](#).

CPSW Statistics Port Enable Register.

Table 8-77. CPSW_STAT_PORT_EN_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0014h

Figure 8-37. CPSW_STAT_PORT_EN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							P8_STAT_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-78. CPSW_STAT_PORT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	P8_STAT_EN	R/W	0h	Port 8 Statistics Enable (if N > 8) 0h = Port 8 statistics are not enabled 1h = Port 8 statistics are enabled.
7	P7_STAT_EN	R/W	0h	Port 7 Statistics Enable (if N > 7) 0h = Port 7 statistics are not enabled 1h = Port 7 statistics are enabled.
6	P6_STAT_EN	R/W	0h	Port 6 Statistics Enable (if N > 6) 0h = Port 6 statistics are not enabled 1h = Port 6 statistics are enabled.
5	P5_STAT_EN	R/W	0h	Port 5 Statistics Enable (if N > 5) 0h = Port 5 statistics are not enabled 1h = Port 5 statistics are enabled.
4	P4_STAT_EN	R/W	0h	Port 4 Statistics Enable (if N > 4) 0h = Port 4 statistics are not enabled 1h = Port 4 statistics are enabled.
3	P3_STAT_EN	R/W	0h	Port 3 Statistics Enable (if N > 3) 0h = Port 3 statistics are not enabled 1h = Port 3 statistics are enabled.
2	P2_STAT_EN	R/W	0h	Port 2 Statistics Enable (if N > 2) 0h = Port 2 statistics are not enabled 1h = Port 2 statistics are enabled.

Table 8-78. CPSW_STAT_PORT_EN_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	P1_STAT_EN	R/W	0h	Port 1 Statistics Enable 0h = Port 1 statistics are not enabled 1h = Port 1 statistics are enabled.
0	P0_STAT_EN	R/W	0h	Port 0 Statistics Enable 0h = Port 0 statistics are not enabled 1h = Port 0 statistics are enabled.

8.2.5 CPSW_PTYPE_REG Register (Offset = 00020018h) [reset = X]

CPSW_PTYPE_REG is shown in [Figure 8-38](#) and described in [Table 8-80](#).

Return to [Summary Table](#).

CPSW Transmit Priority Type.

Table 8-79. CPSW_PTYPE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0018h

Figure 8-38. CPSW_PTYPE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							P8_PTYPE_ESC
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC	P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				ESC_PRI_LD_VAL			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-80. CPSW_PTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	P8_PTYPE_ESC	R/W	0h	Port 8 Priority Type Escalate (if N > 8) 0h = Port 8 priority type fixed 1h = Port 8 priority type escalate
15	P7_PTYPE_ESC	R/W	0h	Port 7 Priority Type Escalate (if N > 7) 0h = Port 7 priority type fixed 1h = Port 7 priority type escalate
14	P6_PTYPE_ESC	R/W	0h	Port 6 Priority Type Escalate (if N > 6) 0h = Port 6 priority type fixed 1h = Port 6 priority type escalate
13	P5_PTYPE_ESC	R/W	0h	Port 5 Priority Type Escalate (if N > 5) 0h = Port 5 priority type fixed 1h = Port 5 priority type escalate
12	P4_PTYPE_ESC	R/W	0h	Port 4 Priority Type Escalate (if N > 4) 0h = Port 4 priority type fixed 1h = Port 4 priority type escalate
11	P3_PTYPE_ESC	R/W	0h	Port 3 Priority Type Escalate (if N > 3) 0h = Port 3 priority type fixed 1h = Port 3 priority type escalate

Table 8-80. CPSW_PTYPE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	P2_PTYPE_ESC	R/W	0h	Port 2 Priority Type Escalate (if N > 2) 0h = Port 2 priority type fixed 1h = Port 2 priority type escalate
9	P1_PTYPE_ESC	R/W	0h	Port 1 Priority Type Escalate 0h = Port 1 priority type fixed 1h = Port 1 priority type escalate
8	P0_PTYPE_ESC	R/W	0h	Port 0 Priority Type Escalate 0h = Port 0 priority type fixed 1h = Port 0 priority type escalate
7-5	RESERVED	R/W	X	
4-0	ESC_PRI_LD_VAL	R/W	0h	Escalate Priority Load Value When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority. The min value of ESC_PRI_LD_VAL = 2h.

8.2.6 CPSW_SOFT_IDLE_REG Register (Offset = 0002001Ch) [reset = X]

CPSW_SOFT_IDLE_REG is shown in [Figure 8-39](#) and described in [Table 8-82](#).

Return to [Summary Table](#).

CPSW Software Idle Register.

Table 8-81. CPSW_SOFT_IDLE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 001Ch

Figure 8-39. CPSW_SOFT_IDLE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							SOFT_IDLE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-82. CPSW_SOFT_IDLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	SOFT_IDLE	R/W	0h	Software Idle. 0h = Not in Idle. 1h = Command a MCU_CPSW0 software Idle. When set, no packets will be started to be unloaded from ports 0 through 4 receive unload. Packets that are currently being unloaded are unaffected.

8.2.7 CPSW_THRU_RATE_REG Register (Offset = 00020020h) [reset = X]

CPSW_THRU_RATE_REG is shown in [Figure 8-40](#) and described in [Table 8-84](#).

Return to [Summary Table](#).

CPSW Thru Rate Register.

Table 8-83. CPSW_THRU_RATE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0020h

Figure 8-40. CPSW_THRU_RATE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
SL_RX_THRU_RATE				RESERVED			
R/W-3h				R/W-X			
7	6	5	4	3	2	1	0
RESERVED				P0_RX_THRU_RATE			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-84. CPSW_THRU_RATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-12	SL_RX_THRU_RATE	R/W	3h	Ethernet Port Switch FIFO receive through rate. This register value is the maximum throughput of the Ethernet ports to the crossbar SCR. The default is one 8-byte word for every 3 VBUSP_GCLK periods maximum. The minimum value is 2. This is not a field that is intended to be changed by a user.
11-4	RESERVED	R/W	X	
3-0	P0_RX_THRU_RATE	R/W	1h	CPPI FIFO (port 0) receive through rate. This register value is the maximum throughput of the CPPI FIFO (port 0) into the MCU_CPSW0. The minimum value is 1. This field is not intended to be changed by the user.

8.2.8 CPSW_GAP_THRESH_REG Register (Offset = 00020024h) [reset = X]

CPSW_GAP_THRESH_REG is shown in [Figure 8-41](#) and described in [Table 8-86](#).

Return to [Summary Table](#).

CPSW Transmit FIFO Short Gap Threshold Register.

Table 8-85. CPSW_GAP_THRESH_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0024h

Figure 8-41. CPSW_GAP_THRESH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											GAP_THRESH				
R/W-X											R/W-Bh				

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-86. CPSW_GAP_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	GAP_THRESH	R/W	Bh	Ethernet Port Short Gap Threshold. This is the Ethernet port associated FIFO transmit block usage value for triggering transmit short gap (when short gap is enabled).

8.2.9 CPSW_TX_START_WDS_REG Register (Offset = 00020028h) [reset = X]

CPSW_TX_START_WDS_REG is shown in [Figure 8-42](#) and described in [Table 8-88](#).

Return to [Summary Table](#).

CPSW Transmit FIFO Start Words Register

Table 8-87. CPSW_TX_START_WDS_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0028h

Figure 8-42. CPSW_TX_START_WDS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TX_START_WDS									
R/W-X						R/W-8h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-88. CPSW_TX_START_WDS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	TX_START_WDS	R/W	8h	FIFO Packet Transmit (egress) Start Words. This value is the number of required 32-byte packet words in an Ethernet transmit FIFO before the packet egress will begin. This value is non-zero to preclude Ethernet transmit underrun. Decimal 8 is the recommended value. It should not be increased unnecessarily to prevent adding to the switch latency.

8.2.10 CPSW_EEE_PRESCALE_REG Register (Offset = 0002002Ch) [reset = X]

CPSW_EEE_PRESCALE_REG is shown in [Figure 8-43](#) and described in [Table 8-90](#).

Return to [Summary Table](#).

CPSW Energy Efficient Ethernet Prescale Value Register.

Table 8-89. CPSW_EEE_PRESCALE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 002Ch

Figure 8-43. CPSW_EEE_PRESCALE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EEE_PRESCALE															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-90. CPSW_EEE_PRESCALE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	EEE_PRESCALE	R/W	0h	Energy Efficient Ethernet Pre-scale count load value

8.2.11 CPSW_TX_G_OFLOW_THRESH_SET_REG Register (Offset = 00020030h) [reset = FFFFFFFFh]

CPSW_TX_G_OFLOW_THRESH_SET_REG is shown in [Figure 8-44](#) and described in [Table 8-92](#).

Return to [Summary Table](#).

CPSW PFC Tx Global Out Flow Threshold Set

Table 8-91.
CPSW_TX_G_OFLOW_THRESH_SET_REG
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0030h

Figure 8-44. CPSW_TX_G_OFLOW_THRESH_SET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-92. CPSW_TX_G_OFLOW_THRESH_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27-24	PRI6	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23-20	PRI5	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19-16	PRI4	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15-12	PRI3	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11-8	PRI2	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7-4	PRI1	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3-0	PRI0	R/W	Fh	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

8.2.12 CPSW_TX_G_OFLOW_THRESH_CLR_REG Register (Offset = 00020034h) [reset = 0h]

CPSW_TX_G_OFLOW_THRESH_CLR_REG is shown in [Figure 8-45](#) and described in [Table 8-94](#).

Return to [Summary Table](#).

CPSW PFC Tx Global Out Flow Threshold Clear Register.

Table 8-93.
CPSW_TX_G_OFLOW_THRESH_CLR_REG
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0034h

Figure 8-45. CPSW_TX_G_OFLOW_THRESH_CLR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-94. CPSW_TX_G_OFLOW_THRESH_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27-24	PRI6	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23-20	PRI5	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19-16	PRI4	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15-12	PRI3	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11-8	PRI2	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7-4	PRI1	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3-0	PRI0	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

8.2.13 CPSW_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 00020038h) [reset = FFFFFFFFh]

CPSW_TX_G_BUF_THRESH_SET_L_REG is shown in [Figure 8-46](#) and described in [Table 8-96](#).

Return to [Summary Table](#).

CPSW PFC Global Tx Buffer Threshold Set Low Register.

Table 8-95.
CPSW_TX_G_BUF_THRESH_SET_L_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0038h

Figure 8-46. CPSW_TX_G_BUF_THRESH_SET_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3								PRI2								PRI1								PRI0							
R/W-FFh								R/W-FFh								R/W-FFh								R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-96. CPSW_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI3	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23-16	PRI2	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15-8	PRI1	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7-0	PRI0	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

8.2.14 CPSW_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 0002003Ch) [reset = FFFFFFFFh]

CPSW_TX_G_BUF_THRESH_SET_H_REG is shown in [Figure 8-47](#) and described in [Table 8-98](#).

Return to [Summary Table](#).

CPSW PFC Global Tx Buffer Threshold Set High Register.

Table 8-97.
CPSW_TX_G_BUF_THRESH_SET_H_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 003Ch

Figure 8-47. CPSW_TX_G_BUF_THRESH_SET_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7								PRI6								PRI5								PRI4							
R/W-FFh								R/W-FFh								R/W-FFh								R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-98. CPSW_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI7	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23-16	PRI6	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15-8	PRI5	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7-0	PRI4	R/W	FFh	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

8.2.15 CPSW_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 00020040h) [reset = 0h]

CPSW_TX_G_BUF_THRESH_CLR_L_REG is shown in [Figure 8-48](#) and described in [Table 8-100](#).

Return to [Summary Table](#).

CPSW PFC Global Tx Buffer Threshold Clear Low Register.

Table 8-99.
CPSW_TX_G_BUF_THRESH_CLR_L_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0040h

Figure 8-48. CPSW_TX_G_BUF_THRESH_CLR_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3								PRI2								PRI1								PRI0							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-100. CPSW_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI3	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23-16	PRI2	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15-8	PRI1	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7-0	PRI0	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

8.2.16 CPSW_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 00020044h) [reset = 0h]

CPSW_TX_G_BUF_THRESH_CLR_H_REG is shown in [Figure 8-49](#) and described in [Table 8-102](#).

Return to [Summary Table](#).

CPSW PFC Global Tx Buffer Threshold Clear High Register.

Table 8-101.
CPSW_TX_G_BUF_THRESH_CLR_H_REG
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0044h

Figure 8-49. CPSW_TX_G_BUF_THRESH_CLR_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7								PRI6								PRI5								PRI4							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-102. CPSW_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PRI7	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23-16	PRI6	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15-8	PRI5	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7-0	PRI4	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

8.2.17 CPSW_VLAN_LTYPE_REG Register (Offset = 00020050h) [reset = 88A88100h]

CPSW_VLAN_LTYPE_REG is shown in [Figure 8-50](#) and described in [Table 8-104](#).

Return to [Summary Table](#).

VLAN LTYPE Outer and Inner Register.

Table 8-103. CPSW_VLAN_LTYPE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0050h

Figure 8-50. CPSW_VLAN_LTYPE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLAN_LTYPE_OUTER																VLAN_LTYPE_INNER															
R/W-88A8h																R/W-8100h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-104. CPSW_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VLAN_LTYPE_OUTER	R/W	88A8h	Outer VLAN LType
15-0	VLAN_LTYPE_INNER	R/W	8100h	Inner VLAN LType

8.2.18 CPSW_EST_TS_DOMAIN_REG Register (Offset = 00020054h) [reset = X]

CPSW_EST_TS_DOMAIN_REG is shown in [Figure 8-51](#) and described in [Table 8-106](#).

Return to [Summary Table](#).

Enhanced Scheduled Traffic Host Event Domain Register.

**Table 8-105. CPSW_EST_TS_DOMAIN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0054h

Figure 8-51. CPSW_EST_TS_DOMAIN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EST_TS_DOMAIN							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-106. CPSW_EST_TS_DOMAIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	EST_TS_DOMAIN	R/W	0h	Enhanced Scheduled Traffic Host Event Domain. This value is used as the domain in the CPTS event to indicate that the event came from EST.

8.2.19 CPSW_TX_PRI0_MAXLEN_REG Register (Offset = 00020100h) [reset = X]

CPSW_TX_PRI0_MAXLEN_REG is shown in [Figure 8-52](#) and described in [Table 8-108](#).

Return to [Summary Table](#).

Priority 0 Maximum Transmit Packet Length Register.

Table 8-107. CPSW_TX_PRI0_MAXLEN_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0100h

Figure 8-52. CPSW_TX_PRI0_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI0_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-108. CPSW_TX_PRI0_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI0_MAXLEN	R/W	7E8h	<p>Transmit Priority 0 Maximum Packet Length</p> <p>This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.</p>

8.2.20 CPSW_TX_PRI1_MAXLEN_REG Register (Offset = 00020104h) [reset = X]

CPSW_TX_PRI1_MAXLEN_REG is shown in [Figure 8-53](#) and described in [Table 8-110](#).

Return to [Summary Table](#).

Priority 1 Maximum Transmit Packet Length Register.

**Table 8-109. CPSW_TX_PRI1_MAXLEN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0104h

Figure 8-53. CPSW_TX_PRI1_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI1_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-110. CPSW_TX_PRI1_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI1_MAXLEN	R/W	7E8h	Transmit Priority 1 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

8.2.21 CPSW_TX_PRI2_MAXLEN_REG Register (Offset = 00020108h) [reset = X]

CPSW_TX_PRI2_MAXLEN_REG is shown in [Figure 8-54](#) and described in [Table 8-112](#).

Return to [Summary Table](#).

Priority 2 Maximum Transmit Packet Length Register.

Table 8-111. CPSW_TX_PRI2_MAXLEN_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0108h

Figure 8-54. CPSW_TX_PRI2_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI2_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-112. CPSW_TX_PRI2_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI2_MAXLEN	R/W	7E8h	<p>Transmit Priority 2 Maximum Packet Length</p> <p>This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI2_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.</p>

8.2.22 CPSW_TX_PRI3_MAXLEN_REG Register (Offset = 0002010Ch) [reset = X]

CPSW_TX_PRI3_MAXLEN_REG is shown in [Figure 8-55](#) and described in [Table 8-114](#).

Return to [Summary Table](#).

Priority 3 Maximum Transmit Packet Length Register.

**Table 8-113. CPSW_TX_PRI3_MAXLEN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 010Ch

Figure 8-55. CPSW_TX_PRI3_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI3_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-114. CPSW_TX_PRI3_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI3_MAXLEN	R/W	7E8h	Transmit Priority 3 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

8.2.23 CPSW_TX_PRI4_MAXLEN_REG Register (Offset = 00020110h) [reset = X]

CPSW_TX_PRI4_MAXLEN_REG is shown in [Figure 8-56](#) and described in [Table 8-116](#).

Return to [Summary Table](#).

Priority 4 Maximum Transmit Packet Length Register.

Table 8-115. CPSW_TX_PRI4_MAXLEN_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0110h

Figure 8-56. CPSW_TX_PRI4_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI4_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-116. CPSW_TX_PRI4_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI4_MAXLEN	R/W	7E8h	Transmit Priority 4 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

8.2.24 CPSW_TX_PRI5_MAXLEN_REG Register (Offset = 00020114h) [reset = X]

CPSW_TX_PRI5_MAXLEN_REG is shown in [Figure 8-57](#) and described in [Table 8-118](#).

Return to [Summary Table](#).

Priority 5 Maximum Transmit Packet Length Register.

**Table 8-117. CPSW_TX_PRI5_MAXLEN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0114h

Figure 8-57. CPSW_TX_PRI5_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI5_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-118. CPSW_TX_PRI5_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI5_MAXLEN	R/W	7E8h	Transmit Priority 5 Maximum Packet Length This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

8.2.25 CPSW_TX_PRI6_MAXLEN_REG Register (Offset = 00020118h) [reset = X]

CPSW_TX_PRI6_MAXLEN_REG is shown in [Figure 8-58](#) and described in [Table 8-120](#).

Return to [Summary Table](#).

Priority 6 Maximum Transmit Packet Length Register.

Table 8-119. CPSW_TX_PRI6_MAXLEN_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 0118h

Figure 8-58. CPSW_TX_PRI6_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI6_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-120. CPSW_TX_PRI6_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI6_MAXLEN	R/W	7E8h	<p>Transmit Priority 6 Maximum Packet Length</p> <p>This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.</p>

8.2.26 CPSW_TX_PRI7_MAXLEN_REG Register (Offset = 0002011Ch) [reset = X]

CPSW_TX_PRI7_MAXLEN_REG is shown in [Figure 8-59](#) and described in [Table 8-122](#).

Return to [Summary Table](#).

Priority 7 Maximum Transmit Packet Length Register.

**Table 8-121. CPSW_TX_PRI7_MAXLEN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 011Ch

Figure 8-59. CPSW_TX_PRI7_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TX_PRI7_MAXLEN													
R/W-X																		R/W-7E8h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-122. CPSW_TX_PRI7_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	TX_PRI7_MAXLEN	R/W	7E8h	Transmit Priority 7 Maximum Packet Length. This value determines the maximum packet length that will be transmitted on Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal). Packets on a priority that are larger than the CPSW_TX_PRI0_MAXLEN_REG to CPSW_TX_PRI7_MAXLEN_REG value are dropped. The reset value is decimal 2024 when fifo_blk_size=1 and 9604 when fifo_blk_size=4.

8.2.27 CPSW_P0_CONTROL_REG Register (Offset = 00021004h) [reset = X]

CPSW_P0_CONTROL_REG is shown in [Figure 8-60](#) and described in [Table 8-124](#).

Return to [Summary Table](#).

CPPI Port 0 Control Register.

Table 8-123. CPSW_P0_CONTROL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1004h

Figure 8-60. CPSW_P0_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					RX_REMAP_D SCP_V6	RX_REMAP_D SCP_V4	RX_REMAP_V LAN
R/W-X					R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_ECC_ERR _EN	TX_ECC_ERR _EN	RESERVED					
R/W-0h	R/W-0h	R/W-X					
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_E N	DSCP_IPV4_E N	RX_CHECKSU M_EN
R/W-X					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-124. CPSW_P0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18	RX_REMAP_DSCP_V6	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
17	RX_REMAP_DSCP_V4	R/W	0h	Port 0 receive remap thread to DSCP IPV6 priority.
16	RX_REMAP_VLAN	R/W	0h	Port 0 receive remap thread to VLAN.
15	RX_ECC_ERR_EN	R/W	0h	Port 0 receive ECC Error Enable This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port 0 transmit ECC Error Enable This bit must be set to enable transmit ECC error operations
13-3	RESERVED	R/W	X	
2	DSCP_IPV6_EN	R/W	0h	Port 0 IPv6 DSCP enable 0h = IPV6 DSCP priority mapping is disabled 1h = IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	Port 0 IPV4 DSCP enable 0h = IPV4 DSCP priority mapping is disabled 1h = IPV4 DSCP priority mapping is enabled
0	RX_CHECKSUM_EN	R/W	0h	Port 0 Receive (port 0 ingress) Checksum Enable 0h = Port 0 receive checksum is disabled 1h = Port 0 receive checksum is enabled

8.2.28 CPSW_P0_FLOW_ID_OFFSET_REG Register (Offset = 00021008h) [reset = X]

CPSW_P0_FLOW_ID_OFFSET_REG is shown in [Figure 8-61](#) and described in [Table 8-126](#).

Return to [Summary Table](#).

CPPI Port 0 Flow ID Offset Register.

Table 8-125. CPSW_P0_FLOW_ID_OFFSET_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1008h

Figure 8-61. CPSW_P0_FLOW_ID_OFFSET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		VALUE													
R/W-X																		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-126. CPSW_P0_FLOW_ID_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	VALUE	R/W	0h	This value is added to the thread/Flow_ID in CPPI transmit PSI Info Word 0

8.2.29 CPSW_P0_BLK_CNT_REG Register (Offset = 00021010h) [reset = X]

CPSW_P0_BLK_CNT_REG is shown in [Figure 8-62](#) and described in [Table 8-128](#).

Return to [Summary Table](#).

CPPI Port 0 FIFO Block Usage Count Register.

Table 8-127. CPSW_P0_BLK_CNT_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1010h

Figure 8-62. CPSW_P0_BLK_CNT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED				TX_BLK_CNT			
R-X				R-0h			
7	6	5	4	3	2	1	0
RESERVED			RX_BLK_CNT				
R-X			R-1h				

LEGEND: R = Read Only; -n = value after reset

Table 8-128. CPSW_P0_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	X	
12-8	TX_BLK_CNT	R	0h	Port 0 Transmit Block Count Usage. This value is the number of blocks allocated to the FIFO logical transmit queues.
7-6	RESERVED	R	X	
5-0	RX_BLK_CNT	R	1h	Port 0 Receive Block Count Usage. This value is the number of blocks allocated in the receive FIFO.

8.2.30 CPSW_P0_PORT_VLAN_REG Register (Offset = 00021014h) [reset = X]

CPSW_P0_PORT_VLAN_REG is shown in [Figure 8-63](#) and described in [Table 8-130](#).

Return to [Summary Table](#).

CPPI Port 0 VLAN

**Table 8-129. CPSW_P0_PORT_VLAN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1014h

Figure 8-63. CPSW_P0_PORT_VLAN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W-0h			R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-130. CPSW_P0_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11-0	PORT_VID	R/W	0h	Port VLAN ID

8.2.31 CPSW_P0_TX_PRI_MAP_REG Register (Offset = 00021018h) [reset = X]

CPSW_P0_TX_PRI_MAP_REG is shown in [Figure 8-64](#) and described in [Table 8-132](#).

Return to [Summary Table](#).

CPPI Port 0 Tx Header Pri to Switch Pri Mapping.

Table 8-131. CPSW_P0_TX_PRI_MAP_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1018h

Figure 8-64. CPSW_P0_TX_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
R/W-X	R/W-7h			R/W-X	R/W-6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
R/W-X	R/W-5h			R/W-X	R/W-4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
R/W-X	R/W-3h			R/W-X	R/W-2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
R/W-X	R/W-1h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-132. CPSW_P0_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	R/W	X	
26-24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	R/W	X	
22-20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	R/W	X	
18-16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	R/W	X	
14-12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	R/W	X	
10-8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	R/W	X	
6-4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.

Table 8-132. CPSW_P0_TX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

8.2.32 CPSW_P0_PRI_CTL_REG Register (Offset = 0002101Ch) [reset = X]

CPSW_P0_PRI_CTL_REG is shown in [Figure 8-65](#) and described in [Table 8-134](#).

Return to [Summary Table](#).

CPPI Port 0 Priority Control.

Table 8-133. CPSW_P0_PRI_CTL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 101Ch

Figure 8-65. CPSW_P0_PRI_CTL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RX_FLOW_PRI							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							RX_PTYPE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-134. CPSW_P0_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority).
15-9	RESERVED	R/W	X	
8	RX_PTYPE	R/W	0h	Receive Priority Type 0h = Fixed priority 1h = Round Robin priority
7-0	RESERVED	R/W	X	

8.2.33 CPSW_P0_RX_PRI_MAP_REG Register (Offset = 00021020h) [reset = X]

CPSW_P0_RX_PRI_MAP_REG is shown in [Figure 8-66](#) and described in [Table 8-136](#).

Return to [Summary Table](#).

CPPI Port 0 RX Pkt Pri to Header Pri Map

**Table 8-135. CPSW_P0_RX_PRI_MAP_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1020h

Figure 8-66. CPSW_P0_RX_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED		PRI7		RESERVED		PRI6	
R/W-X		R/W-7h		R/W-X		R/W-6h	
23	22	21	20	19	18	17	16
RESERVED		PRI5		RESERVED		PRI4	
R/W-X		R/W-5h		R/W-X		R/W-4h	
15	14	13	12	11	10	9	8
RESERVED		PRI3		RESERVED		PRI2	
R/W-X		R/W-3h		R/W-X		R/W-2h	
7	6	5	4	3	2	1	0
RESERVED		PRI1		RESERVED		PRI0	
R/W-X		R/W-1h		R/W-X		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-136. CPSW_P0_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	R/W	X	
26-24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	R/W	X	
22-20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	R/W	X	
18-16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	R/W	X	
14-12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	R/W	X	
10-8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	R/W	X	
6-4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.

Table 8-136. CPSW_P0_RX_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

8.2.34 CPSW_P0_RX_MAXLEN_REG Register (Offset = 00021024h) [reset = X]

CPSW_P0_RX_MAXLEN_REG is shown in [Figure 8-67](#) and described in [Table 8-138](#).

Return to [Summary Table](#).

CPPI Port 0 Receive Frame Max Length.

**Table 8-137. CPSW_P0_RX_MAXLEN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1024h

Figure 8-67. CPSW_P0_RX_MAXLEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		RX_MAXLEN													
R/W-X																		R/W-5EEh													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-138. CPSW_P0_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_MAXLEN	R/W	5EEh	<p>RX Maximum Frame Length.</p> <p>This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_P0_RX_MAXLEN_REG are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN) when fifo_blk_size = 4.</p> <p>When fifo_blk_size = 1 the maximum value is 2024 (including VLAN).</p>

8.2.35 CPSW_P0_TX_BLKs_PRI_REG Register (Offset = 00021028h) [reset = 01245678h]

CPSW_P0_TX_BLKs_PRI_REG is shown in [Figure 8-68](#) and described in [Table 8-140](#).

Return to [Summary Table](#).

CPPI Port 0 Transmit Block Sub Per Priority Register.

Table 8-139. CPSW_P0_TX_BLKs_PRI_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1028h

Figure 8-68. CPSW_P0_TX_BLKs_PRI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-1h				R/W-2h				R/W-4h				R/W-5h				R/W-6h				R/W-7h				R/W-8h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-140. CPSW_P0_TX_BLKs_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27-24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23-20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19-16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15-12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11-8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7-4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3-0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

8.2.36 CPSW_P0_IDLE2LPI_REG Register (Offset = 00021030h) [reset = X]

CPSW_P0_IDLE2LPI_REG is shown in [Figure 8-69](#) and described in [Table 8-142](#).

Return to [Summary Table](#).

Port 0 EEE LPI to wake counter load value.

Table 8-141. CPSW_P0_IDLE2LPI_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1030h

Figure 8-69. CPSW_P0_IDLE2LPI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-142. CPSW_P0_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	COUNT	R/W	0h	Port 0 EEE Idle to LPI counter load value

8.2.37 CPSW_P0_LPI2WAKE_REG Register (Offset = 00021034h) [reset = X]

CPSW_P0_LPI2WAKE_REG is shown in [Figure 8-70](#) and described in [Table 8-144](#).

Return to [Summary Table](#).

Port 0 EEE LPI to wake counter

Table 8-143. CPSW_P0_LPI2WAKE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1034h

Figure 8-70. CPSW_P0_LPI2WAKE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-144. CPSW_P0_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	COUNT	R/W	0h	Port 0 EEE LPI to wake counter load value

8.2.38 CPSW_P0_EEE_STATUS_REG Register (Offset = 00021038h) [reset = X]

CPSW_P0_EEE_STATUS_REG is shown in [Figure 8-71](#) and described in [Table 8-146](#).

Return to [Summary Table](#).

Port 0 EEE status.

**Table 8-145. CPSW_P0_EEE_STATUS_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1038h

Figure 8-71. CPSW_P0_EEE_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
R-X	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-146. CPSW_P0_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	X	
6	TX_FIFO_EMPTY	R	1h	CPPI (Port 0) Transmit FIFO packet count zero. This bit is set when there are no packets in the transmit FIFO.
5	RX_FIFO_EMPTY	R	1h	CPPI (Port 0) Receive FIFO packet count zero. This bit is set when there are no packets in the receive FIFO.
4	TX_FIFO_HOLD	R	0h	CPPI (Port 0) Transmit FIFO hold. This bit is set during LPI and Wake time.
3	TX_WAKE	R	0h	CPPI (Port 0) Receive Wake Time. This bit is set when the IDLE to Wake time is being counted.
2	TX_LPI	R	0h	CPPI (Port 0) transmit LPI state. This bit is set when the CPPI streaming interface is in the LPI state. Transmit LPI and receive LPI are not separate for the CPPI port
1	RX_LPI	R	0h	CPPI (Port 0) receive LPI state. This bit is set when the CPPI streaming interface is in the LPI state. Transmit LPI and receive LPI are not separate for the CPPI port.
0	WAIT_IDLE2LPI	R	0h	CPPI (Port 0) Transmit Wait Idle to LPI. This bit is set when the port is counting the IDLE to LPI time.

8.2.39 CPSW_P0_FIFO_STATUS_REG Register (Offset = 00021050h) [reset = X]

CPSW_P0_FIFO_STATUS_REG is shown in [Figure 8-72](#) and described in [Table 8-148](#).

Return to [Summary Table](#).

Port 0 FIFO Status

**Table 8-147. CPSW_P0_FIFO_STATUS_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1050h

Figure 8-72. CPSW_P0_FIFO_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_PRI_ACTIVE							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 8-148. CPSW_P0_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	TX_PRI_ACTIVE	R	0h	Port 0 Transmit FIFO Priority Active. Each bit indicates whether the corresponding FIFO priority has one or more queued packets on it or not. Note: For N=2 this field is always zero (there is no transmit FIFO).

8.2.40 CPSW_P0_RX_DSCP_MAP_REG_y Register (Offset = 00021120h + formula) [reset = X]

CPSW_P0_RX_DSCP_MAP_REG_y is shown in [Figure 8-73](#) and described in [Table 8-150](#).

Return to [Summary Table](#).

CPPI Port 0 Receive IPV4/IPV6 DSCP Map 0 to Map 7 Registers.

Offset = 00021120h + (y * 4h); where y = 0h to 7h

**Table 8-149. CPSW_P0_RX_DSCP_MAP_REG_y
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1120h + formula

Figure 8-73. CPSW_P0_RX_DSCP_MAP_REG_y Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
R/W-X	R/W-0h			R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
R/W-X	R/W-0h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-150. CPSW_P0_RX_DSCP_MAP_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	R/W	X	
26-24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	R/W	X	
22-20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	R/W	X	
18-16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	R/W	X	
14-12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	R/W	X	
10-8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	R/W	X	

Table 8-150. CPSW_P0_RX_DSCP_MAP_REG_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

8.2.41 CPSW_P0_PRI_CIR_REG_y Register (Offset = 00021140h + formula) [reset = X]

CPSW_P0_PRI_CIR_REG_y is shown in [Figure 8-74](#) and described in [Table 8-152](#).

Return to [Summary Table](#).

CPPI Port 0 Rx Priority 0 to Priority 7 Committed Information Rate Registers.

Offset = 00021140h + (y * 4h); where y = 0h to 7h

Table 8-151. CPSW_P0_PRI_CIR_REG_y Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1140h + formula

Figure 8-74. CPSW_P0_PRI_CIR_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI_CIR																											
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-152. CPSW_P0_PRI_CIR_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PRI_CIR	R/W	0h	Priority "y" Committed Information Rate Count Value

8.2.42 CPSW_P0_PRI_EIR_REG_y Register (Offset = 00021160h + formula) [reset = X]

CPSW_P0_PRI_EIR_REG_y is shown in [Figure 8-75](#) and described in [Table 8-154](#).

Return to [Summary Table](#).

CPPI Port 0 Rx Priority 0 to Priority 7 Excess Information Rate.

Offset = 00021160h + (y * 4h); where y = 0h to 7h

Table 8-153. CPSW_P0_PRI_EIR_REG_y Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1160h + formula

Figure 8-75. CPSW_P0_PRI_EIR_REG_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRI_EIR																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-154. CPSW_P0_PRI_EIR_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PRI_EIR	R/W	0h	Priority N EIR

8.2.43 CPSW_P0_TX_D_THRESH_SET_L_REG Register (Offset = 00021180h) [reset = X]

CPSW_P0_TX_D_THRESH_SET_L_REG is shown in [Figure 8-76](#) and described in [Table 8-156](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Destination Threshold Set Low

**Table 8-155. CPSW_P0_TX_D_THRESH_SET_L_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1180h

Figure 8-76. CPSW_P0_TX_D_THRESH_SET_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-156. CPSW_P0_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

8.2.44 CPSW_P0_TX_D_THRESH_SET_H_REG Register (Offset = 00021184h) [reset = X]

CPSW_P0_TX_D_THRESH_SET_H_REG is shown in [Figure 8-77](#) and described in [Table 8-158](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Destination Threshold Set High

Table 8-157.
CPSW_P0_TX_D_THRESH_SET_H_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1184h

Figure 8-77. CPSW_P0_TX_D_THRESH_SET_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-158. CPSW_P0_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

8.2.45 CPSW_P0_TX_D_THRESH_CLR_L_REG Register (Offset = 00021188h) [reset = X]

CPSW_P0_TX_D_THRESH_CLR_L_REG is shown in [Figure 8-78](#) and described in [Table 8-160](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Destination Threshold Clr Low

Table 8-159.
CPSW_P0_TX_D_THRESH_CLR_L_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1188h

Figure 8-78. CPSW_P0_TX_D_THRESH_CLR_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-160. CPSW_P0_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

8.2.46 CPSW_P0_TX_D_THRESH_CLR_H_REG Register (Offset = 0002118Ch) [reset = X]

CPSW_P0_TX_D_THRESH_CLR_H_REG is shown in [Figure 8-79](#) and described in [Table 8-162](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Destination Threshold Clr High

Table 8-161.
CPSW_P0_TX_D_THRESH_CLR_H_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 118Ch

Figure 8-79. CPSW_P0_TX_D_THRESH_CLR_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-162. CPSW_P0_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

8.2.47 CPSW_P0_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 00021190h) [reset = X]

CPSW_P0_TX_G_BUF_THRESH_SET_L_REG is shown in [Figure 8-80](#) and described in [Table 8-164](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Global Buffer Threshold Set Low

Table 8-163.
CPSW_P0_TX_G_BUF_THRESH_SET_L_REG
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1190h

Figure 8-80. CPSW_P0_TX_G_BUF_THRESH_SET_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-164. CPSW_P0_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

8.2.48 CPSW_P0_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 00021194h) [reset = X]

CPSW_P0_TX_G_BUF_THRESH_SET_H_REG is shown in [Figure 8-81](#) and described in [Table 8-166](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Global Buffer Threshold Set High

Table 8-165.
CPSW_P0_TX_G_BUF_THRESH_SET_H_REG
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1194h

Figure 8-81. CPSW_P0_TX_G_BUF_THRESH_SET_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-166. CPSW_P0_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

8.2.49 CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 00021198h) [reset = X]

CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG is shown in [Figure 8-82](#) and described in [Table 8-168](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Global Buffer Threshold Clr Low

Table 8-167.
CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1198h

Figure 8-82. CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-168. CPSW_P0_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

8.2.50 CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 0002119Ch) [reset = X]

CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG is shown in [Figure 8-83](#) and described in [Table 8-170](#).

Return to [Summary Table](#).

CPPI Port 0 Tx PFC Global Buffer Threshold Clr High

Table 8-169.
CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 119Ch

Figure 8-83. CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-170. CPSW_P0_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

8.2.51 CPSW_P0_SRC_ID_A_REG Register (Offset = 00021300h) [reset = 04030201h]

CPSW_P0_SRC_ID_A_REG is shown in [Figure 8-84](#) and described in [Table 8-172](#).

Return to [Summary Table](#).

CPPI Port 0 CPPI Source ID A.

Table 8-171. CPSW_P0_SRC_ID_A_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1300h

Figure 8-84. CPSW_P0_SRC_ID_A_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT4								PORT3								PORT2								PORT1							
R/W-4h								R/W-3h								R/W-2h								R/W-1h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-172. CPSW_P0_SRC_ID_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PORT4	R/W	4h	Port 4 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 4.
23-16	PORT3	R/W	3h	Port 3 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 3.
15-8	PORT2	R/W	2h	Port 2 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 2.
7-0	PORT1	R/W	1h	Port 1 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 1.

8.2.52 CPSW_P0_SRC_ID_B_REG Register (Offset = 00021304h) [reset = 08070605h]

CPSW_P0_SRC_ID_B_REG is shown in [Figure 8-85](#) and described in [Table 8-174](#).

Return to [Summary Table](#).

CPPI Port 0 CPPI Source ID B.

Table 8-173. CPSW_P0_SRC_ID_B_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1304h

Figure 8-85. CPSW_P0_SRC_ID_B_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT8								PORT7								PORT6								PORT5							
R/W-8h								R/W-7h								R/W-6h								R/W-5h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-174. CPSW_P0_SRC_ID_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PORT8	R/W	8h	Port 8 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 8.
23-16	PORT7	R/W	7h	Port 7 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 7.
15-8	PORT6	R/W	6h	Port 6 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 6.
7-0	PORT5	R/W	5h	Port 5 CPPI Info Word0 Source ID Value. This value is contained in the CPPI Info Word 0 SRC_ID field for packets received on port 5.

8.2.53 CPSW_P0_HOST_BLKs_PRI_REG Register (Offset = 00021320h) [reset = 0h]

CPSW_P0_HOST_BLKs_PRI_REG is shown in [Figure 8-86](#) and described in [Table 8-176](#).

Return to [Summary Table](#).

CPPI Port 0 Host Blocks Priority

**Table 8-175. CPSW_P0_HOST_BLKs_PRI_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 1320h

Figure 8-86. CPSW_P0_HOST_BLKs_PRI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-176. CPSW_P0_HOST_BLKs_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Priority 7 Host Blocks
27-24	PRI6	R/W	0h	Priority 6 Host Blocks
23-20	PRI5	R/W	0h	Priority 5 Host Blocks
19-16	PRI4	R/W	0h	Priority 4 Host Blocks
15-12	PRI3	R/W	0h	Priority 3 Host Blocks
11-8	PRI2	R/W	0h	Priority 2 Host Blocks
7-4	PRI1	R/W	0h	Priority 1 Host Blocks
3-0	PRI0	R/W	0h	Priority 0 Host Blocks

8.2.54 CPSW_PN_RESERVED_REG_k Register (Offset = 00022000h) [reset = 0h]

CPSW_PN_RESERVED_REG_k is shown in [Figure 8-87](#) and described in [Table 8-178](#).

Return to [Summary Table](#).

Reserved.

**Table 8-177. CPSW_PN_RESERVED_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2000h + formula

Figure 8-87. CPSW_PN_RESERVED_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 8-178. CPSW_PN_RESERVED_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved register for memory map alignment

8.2.55 CPSW_PN_CONTROL_REG_k Register (Offset = 00022004h + formula) [reset = X]

CPSW_PN_CONTROL_REG_k is shown in [Figure 8-88](#) and described in [Table 8-180](#).

Return to [Summary Table](#).

Enet Port N Control.

Offset = 00022004h + (k * 1000h); where k = 0h to 1h

**Table 8-179. CPSW_PN_CONTROL_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2004h + formula

Figure 8-88. CPSW_PN_CONTROL_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						EST_PORT_EN	IET_PORT_EN
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED	TX_LPI_CLKST_OP_EN	RESERVED			
R/W-0h	R/W-0h	R/W-X	R/W-0h	R/W-X			
7	6	5	4	3	2	1	0
RESERVED					DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
R/W-X					R/W-0h	R/W-0h	R/W-X

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-180. CPSW_PN_CONTROL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	EST_PORT_EN	R/W	0h	EST Port Enable. 0h = EST is disabled on the port 1h = EST is enabled on the port – Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
16	IET_PORT_EN	R/W	0h	Intersperced Express Traffic (IET) Port Enable. 0h = IET is disabled on the port 1h = IET is enabled on the port – Does not take effect until CPSW_CONTROL_REG[18] EST_ENABLE is set.
15	RX_ECC_ERR_EN	R/W	0h	Port N receive ECC Error Enable This bit must be set to enable receive ECC error operations
14	TX_ECC_ERR_EN	R/W	0h	Port N transmit ECC Error Enable This bit must be set to enable transmit ECC error operations
13	RESERVED	R/W	X	
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI Clock Stop Enable. When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled.
11-3	RESERVED	R/W	X	

Table 8-180. CPSW_PN_CONTROL_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DSCP_IPV6_EN	R/W	0h	IPV6 DSCP enable 0h = IPV6 DSCP priority mapping is disabled 1h = IPV6 DSCP priority mapping is enabled
1	DSCP_IPV4_EN	R/W	0h	IPV4 DSCP enable 0h = IPV4 DSCP priority mapping is disabled 1h = IPV4 DSCP priority mapping is enabled
0	RESERVED	R/W	X	

8.2.56 CPSW_PN_MAX_BLKs_REG Register (Offset = 00022008h) [reset = X]

CPSW_PN_MAX_BLKs_REG is shown in [Figure 8-89](#) and described in [Table 8-182](#).

Return to [Summary Table](#).

Enet Port N FIFO Max Blocks.

Table 8-181. CPSW_PN_MAX_BLKs_REG Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2008h + formula

Figure 8-89. CPSW_PN_MAX_BLKs_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MAX_BLKs								RX_MAX_BLKs							
R/W-10h								R/W-4h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-182. CPSW_PN_MAX_BLKs_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	TX_MAX_BLKs	R/W	10h	Transmit Max Blocks. The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive, when Full duplex flow control is enabled (CPSW_PN_MAC_CONTROL_REG_k[0] FULLDUPLEX = 1h) to allow for flow control runout.
7-0	RX_MAX_BLKs	R/W	4h	Receive Max Blocks. The maximum number of blocks allowed on the express and preempt receive FIFOs (transmit and receive FIFO's combined when fifo_oneram = 1)

8.2.57 CPSW_PN_BLK_CNT_REG_k Register (Offset = 00022010h + formula) [reset = X]

CPSW_PN_BLK_CNT_REG_k is shown in [Figure 8-90](#) and described in [Table 8-184](#).

Return to [Summary Table](#).

Enet Port N FIFO Block Usage Count

Offset = 00022010h + (N * 1000h); where k = 0h to 1h

Table 8-183. CPSW_PN_BLK_CNT_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2010h + formula

Figure 8-90. CPSW_PN_BLK_CNT_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED		RX_BLK_CNT_P					
R-X		R-0h					
15	14	13	12	11	10	9	8
RESERVED			TX_BLK_CNT				
R-X			R-0h				
7	6	5	4	3	2	1	0
RESERVED		RX_BLK_CNT_E					
R-X		R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 8-184. CPSW_PN_BLK_CNT_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	X	
21-16	RX_BLK_CNT_P	R	0h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO preempt receive queue. No blocks are allocated until the CPSW_CONTROL_REG[17] IET_ENABLE is set.
15-13	RESERVED	R	X	
12-8	TX_BLK_CNT	R	0h	Transmit Block Count Usage. This value is the number of blocks allocated to the port's FIFO logical transmit queues.
7-6	RESERVED	R	X	
5-0	RX_BLK_CNT_E	R	1h	Receive Express Block Count Usage. This value is the number of blocks allocated to the port's FIFO express receive queue.

8.2.58 CPSW_PN_PORT_VLAN_REG_k Register (Offset = 00022014h + formula) [reset = X]

CPSW_PN_PORT_VLAN_REG_k is shown in [Figure 8-91](#) and described in [Table 8-186](#).

Return to [Summary Table](#).

Enet Port N VLAN

Offset = 00022014h + (k * 1000h); where k = 0h to 1h

**Table 8-185. CPSW_PN_PORT_VLAN_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2014h + formula

Figure 8-91. CPSW_PN_PORT_VLAN_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PORT_PRI			PORT_CFI	PORT_VID			
R/W-0h			R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
PORT_VID							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-186. CPSW_PN_PORT_VLAN_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11-0	PORT_VID	R/W	0h	Port VLAN ID

8.2.59 CPSW_PN_TX_PRI_MAP_REG_k Register (Offset = 00022018h + formula) [reset = X]

CPSW_PN_TX_PRI_MAP_REG_k is shown in [Figure 8-92](#) and described in [Table 8-188](#).

Return to [Summary Table](#).

Enet Port N Tx Header Pri to Switch Pri Mapping

Offset = 00022018h + (k * 1000h); where k = 0h to 1h

**Table 8-187. CPSW_PN_TX_PRI_MAP_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2018h + formula

Figure 8-92. CPSW_PN_TX_PRI_MAP_REG_k Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
R/W-X	R/W-7h			R/W-X	R/W-6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
R/W-X	R/W-5h			R/W-X	R/W-4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
R/W-X	R/W-3h			R/W-X	R/W-2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
R/W-X	R/W-1h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-188. CPSW_PN_TX_PRI_MAP_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	7h	Priority 7. A packet header priority of 7h is given this switch queue pri.
27	RESERVED	R/W	X	
26-24	PRI6	R/W	6h	Priority 6. A packet header priority of 6h is given this switch queue pri.
23	RESERVED	R/W	X	
22-20	PRI5	R/W	5h	Priority 5. A packet header priority of 5h is given this switch queue pri.
19	RESERVED	R/W	X	
18-16	PRI4	R/W	4h	Priority 4. A packet header priority of 4h is given this switch queue pri.
15	RESERVED	R/W	X	
14-12	PRI3	R/W	3h	Priority 3. A packet header priority of 3h is given this switch queue pri.
11	RESERVED	R/W	X	
10-8	PRI2	R/W	2h	Priority 2. A packet header priority of 2h is given this switch queue pri.
7	RESERVED	R/W	X	

Table 8-188. CPSW_PN_TX_PRI_MAP_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	PRI1	R/W	1h	Priority 1. A packet header priority of 1h is given this switch queue pri.
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	Priority 0. A packet header priority of 0h is given this switch queue pri.

8.2.60 CPSW_PN_PRI_CTL_REG_k Register (Offset = 0002201Ch + formula) [reset = X]

CPSW_PN_PRI_CTL_REG_k is shown in [Figure 8-93](#) and described in [Table 8-190](#).

Return to [Summary Table](#).

Enet Port N Priority Control

Offset = 0002201Ch + (k * 1000h); where k = 0h to 1h

Table 8-189. CPSW_PN_PRI_CTL_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 201Ch + formula

Figure 8-93. CPSW_PN_PRI_CTL_REG_k Register

31	30	29	28	27	26	25	24
TX_FLOW_PRI							
R/W-0h							
23	22	21	20	19	18	17	16
RX_FLOW_PRI							
R/W-0h							
15	14	13	12	11	10	9	8
TX_HOST_BLKs_REM				RESERVED			
R/W-9h				R/W-X			
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-190. CPSW_PN_PRI_CTL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23-16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15-12	TX_HOST_BLKs_REM	R/W	9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
11-0	RESERVED	R/W	X	

8.2.61 CPSW_PN_RX_PRI_MAP_REG_k Register (Offset = 00022020h + formula) [reset = X]

CPSW_PN_RX_PRI_MAP_REG_k is shown in [Figure 8-94](#) and described in [Table 8-192](#).

Return to [Summary Table](#).

Enet Port N RX Pkt Pri to Header Pri Map

Offset = 00022020h + (k * 1000h); where k = 0h to 1h

**Table 8-191. CPSW_PN_RX_PRI_MAP_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2020h + formula

Figure 8-94. CPSW_PN_RX_PRI_MAP_REG_k Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
R/W-X	R/W-7h			R/W-X	R/W-6h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
R/W-X	R/W-5h			R/W-X	R/W-4h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
R/W-X	R/W-3h			R/W-X	R/W-2h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
R/W-X	R/W-1h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-192. CPSW_PN_RX_PRI_MAP_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	7h	Priority 7. A packet pri of 7h is mapped (changed) to this header packet pri.
27	RESERVED	R/W	X	
26-24	PRI6	R/W	6h	Priority 6. A packet pri of 6h is mapped (changed) to this header packet pri.
23	RESERVED	R/W	X	
22-20	PRI5	R/W	5h	Priority 5. A packet pri of 5h is mapped (changed) to this header packet pri.
19	RESERVED	R/W	X	
18-16	PRI4	R/W	4h	Priority 4. A packet pri of 4h is mapped (changed) to this header packet pri.
15	RESERVED	R/W	X	
14-12	PRI3	R/W	3h	Priority 3. A packet pri of 3h is mapped (changed) to this header packet pri.
11	RESERVED	R/W	X	
10-8	PRI2	R/W	2h	Priority 2. A packet pri of 2h is mapped (changed) to this header packet pri.
7	RESERVED	R/W	X	

Table 8-192. CPSW_PN_RX_PRI_MAP_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	PRI1	R/W	1h	Priority 1. A packet pri of 1h is mapped (changed) to this header packet pri.
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	Priority 0. A packet pri of 0h is mapped (changed) to this header packet pri.

8.2.62 CPSW_PN_RX_MAXLEN_REG_k Register (Offset = 00022024h + formula) [reset = X]

CPSW_PN_RX_MAXLEN_REG_k is shown in [Figure 8-95](#) and described in [Table 8-194](#).

Return to [Summary Table](#).

Enet Port N Receive Frame Max Length.

Offset = 00022024h + (k * 1000h); where k = 0h to 1h

**Table 8-193. CPSW_PN_RX_MAXLEN_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2024h + formula

Figure 8-95. CPSW_PN_RX_MAXLEN_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		RX_MAXLEN													
R/W-X																		R/W-5EEh													

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-194. CPSW_PN_RX_MAXLEN_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	RX_MAXLEN	R/W	5EEh	<p>RX Maximum Frame Length.</p> <p>This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than the value in CPSW_PN_RX_MAXLEN_REG[13-0] RX_MAXLEN are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN).</p>

8.2.63 CPSW_PN_TX_BLKs_PRI_REG_k Register (Offset = 00022028h + formula) [reset = 01245678h]

CPSW_PN_TX_BLKs_PRI_REG_k is shown in [Figure 8-96](#) and described in [Table 8-196](#).

Return to [Summary Table](#).

Enet Port N Transmit Block Sub Per Priority

Offset = 00022028h + (k * 1000h); where k = 0h to 1h

**Table 8-195. CPSW_PN_TX_BLKs_PRI_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2028h + formula

Figure 8-96. CPSW_PN_TX_BLKs_PRI_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI7				PRI6				PRI5				PRI4				PRI3				PRI2				PRI1				PRI0			
R/W-0h				R/W-1h				R/W-2h				R/W-4h				R/W-5h				R/W-6h				R/W-7h				R/W-8h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-196. CPSW_PN_TX_BLKs_PRI_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27-24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23-20	PRI5	R/W	2h	Priority 5 Port Transmit Blocks
19-16	PRI4	R/W	4h	Priority 4 Port Transmit Blocks
15-12	PRI3	R/W	5h	Priority 3 Port Transmit Blocks
11-8	PRI2	R/W	6h	Priority 2 Port Transmit Blocks
7-4	PRI1	R/W	7h	Priority 1 Port Transmit Blocks
3-0	PRI0	R/W	8h	Priority 0 Port Transmit Blocks

8.2.64 CPSW_PN_IDLE2LPI_REG_k Register (Offset = 00022030h + formula) [reset = X]

CPSW_PN_IDLE2LPI_REG_k is shown in [Figure 8-97](#) and described in [Table 8-198](#).

Return to [Summary Table](#).

Enet Port N EEE Idle to LPI counter

Offset = 00022030h + (k * 1000h); where k = 0h to 1h

Table 8-197. CPSW_PN_IDLE2LPI_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2030h + formula

Figure 8-97. CPSW_PN_IDLE2LPI_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-198. CPSW_PN_IDLE2LPI_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	COUNT	R/W	0h	EEE Idle to LPI counter load value

8.2.65 CPSW_PN_LPI2WAKE_REG_k Register (Offset = 00022034h + formula) [reset = X]

CPSW_PN_LPI2WAKE_REG_k is shown in [Figure 8-98](#) and described in [Table 8-200](#).

Return to [Summary Table](#).

Enet Port N EEE LPI to wake counter

Offset = 00022034h + (k * 1000h); where k = 0h to 1h

**Table 8-199. CPSW_PN_LPI2WAKE_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2034h + formula

Figure 8-98. CPSW_PN_LPI2WAKE_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-200. CPSW_PN_LPI2WAKE_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	COUNT	R/W	0h	EEE LPI to wake counter load value

8.2.66 CPSW_PN_EEE_STATUS_REG_k Register (Offset = 00022038h + formula) [reset = X]

CPSW_PN_EEE_STATUS_REG_k is shown in [Figure 8-99](#) and described in [Table 8-202](#).

Return to [Summary Table](#).

Enet Port N EEE status

Offset = 00022038h + (k * 1000h); where k = 0h to 1h

**Table 8-201. CPSW_PN_EEE_STATUS_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2038h + formula

Figure 8-99. CPSW_PN_EEE_STATUS_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
R-X	R-1h	R-1h	R-0h	R-0h	R-0h	R-1h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-202. CPSW_PN_EEE_STATUS_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	X	
6	TX_FIFO_EMPTY	R	1h	Port N Transmit FIFO packet count zero. This bit is set when there are no packets in the transmit FIFO.
5	RX_FIFO_EMPTY	R	1h	Port N Receive FIFO packet count zero. This bit is set when there are no packets in the receive FIFO.
4	TX_FIFO_HOLD	R	0h	Port N Transmit FIFO hold. This bit is set during LPI and Wake time.
3	TX_WAKE	R	0h	Port N Receive Wake Time. This bit is set when the IDLE to Wake time is being counted.
2	TX_LPI	R	0h	Port N Transmit LPI. This bit is set when the Ethernet transmit is in the LPI state.
1	RX_LPI	R	1h	Port N Receive LPI. This bit is set when the Ethernet receive is in the LPI state. The LPI state is indicated after reset because the port is disabled (CPSW_PN_MAC_CONTROL_REG[5] GMII_EN = 0h).
0	WAIT_IDLE2LPI	R	0h	Transmit Wait Idle to LPI. This bit is set when the port is counting the IDLE to LPI time.

8.2.67 CPSW_PN_IET_CONTROL_REG_k Register (Offset = 00022040h + formula) [reset = 8h]

CPSW_PN_IET_CONTROL_REG_k is shown in [Figure 8-100](#) and described in [Table 8-204](#).

Return to [Summary Table](#).

Enet Port N IET Control

Offset = 00022040h + (k * 1000h); where k = 0h to 1h

**Table 8-203. CPSW_PN_IET_CONTROL_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2040h + formula

Figure 8-100. CPSW_PN_IET_CONTROL_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
MAC_PREMPT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					MAC_ADDFRAGSIZE		
R/W-0h					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED				MAC_LINKFAIL	MAC_DISABLE VERIFY	MAC_HOLD	MAC_PENABL E
R/W-0h				R/W-1h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-204. CPSW_PN_IET_CONTROL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	Reserved
23-16	MAC_PREMPT	R/W	0h	Mac Preempt Queue – Indicates which transmit FIFO queues are sent to the preempt MAC. Bit 0 indicates queue zero, bit 1 queue 1 and so on. Packets will be sent to the preempt MAC only when MAC_PENABLE is set, and when MAC_VERIFIED (from CPSW_PN_IET_STATUS_REG_k) or MAC_DISABLEVERIFY is set, and when IET_PORT_EN is set.
15-11	RESERVED	R/W	0h	Reserved
10-8	MAC_ADDFRAGSIZE	R/W	0h	Mac Fragment Size – An integer in the range 0:7 indicating, as a multiple of 64, the minimum additional length for nonfinal mPackets. 0 = 64 1 = 128 2 = 192 3 = 256 4 = 320 5 = 384 6 = 448 7 = 512
7-4	RESERVED	R/W	0h	Reserved
3	MAC_LINKFAIL	R/W	1h	Mac Link Fail – Link Fail Indicator to reset the verify state machine. This bit is reset high. Verify and response frames will be sent/allowed when this bit is cleared.

Table 8-204. CPSW_PN_IET_CONTROL_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MAC_DISABLEVERIFY	R/W	0h	Mac Disable Verify – Disables verification on the port when set. If this bit is set then packets will be sent to the preempt Mac when MAC_PENABLE is set (This is a forced mode with no IET verification).
1	MAC_HOLD	R/W	0h	Mac Hold – Hold Preemption on the port.
0	MAC_PENABLE	R/W	0h	Mac Preemption Enable – Port Preemption Enable. This takes effect only when IET_PORT_EN is set.

8.2.68 CPSW_PN_IET_STATUS_REG_k Register (Offset = 00022044h + formula) [reset = 0h]

CPSW_PN_IET_STATUS_REG_k is shown in [Figure 8-101](#) and described in [Table 8-206](#).

Return to [Summary Table](#).

Enet Port N IET Status

Offset = 00022044h + (k * 1000h); where k = 0h to 1h

**Table 8-205. CPSW_PN_IET_STATUS_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2044h + formula

Figure 8-101. CPSW_PN_IET_STATUS_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				MAC_VERIFY_ERR	MAC_RESPOND_ERR	MAC_VERIFY_FAIL	MAC_VERIFIED
R-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-206. CPSW_PN_IET_STATUS_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	MAC_VERIFY_ERR	R	0h	Mac Received Verify Packet with Errors – Set when a verify packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
2	MAC_RESPOND_ERR	R	0h	Mac Received Respond Packet with Errors – Set when a respond packet with errors is received. Cleared when MAC_PENABLE is cleared to zero.
1	MAC_VERIFY_FAIL	R	0h	Mac Verification Failed – Indication that verification was unsuccessful.
0	MAC_VERIFIED	R	0h	Mac Verified – Indication that verification was successful.

8.2.69 CPSW_PN_IET_VERIFY_REG_k Register (Offset = 00022048h + formula) [reset = 1312D0h]

CPSW_PN_IET_VERIFY_REG_k is shown in [Figure 8-102](#) and described in [Table 8-208](#).

Return to [Summary Table](#).

Enet Port N IET VERIFY

Offset = 00022048h + (k * 1000h); where k = 0h to 1h

**Table 8-207. CPSW_PN_IET_VERIFY_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2048h + formula

Figure 8-102. CPSW_PN_IET_VERIFY_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAC_VERIFY_CNT																							
R/W-0h								R/W-001312D0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-208. CPSW_PN_IET_VERIFY_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	0h	Reserved
23-0	MAC_VERIFY_CNT	R/W	001312D0h	Mac Verify Timeout Count – The number of wireside clocks contained in the verify timeout counter. The default is 0x1312D0 (10ms at 125MHz in gig mode).

8.2.70 CPSW_PN_FIFO_STATUS_REG_k Register (Offset = 00022050h + formula) [reset = X]

CPSW_PN_FIFO_STATUS_REG_k is shown in [Figure 8-103](#) and described in [Table 8-210](#).

Return to [Summary Table](#).

Enet Port N FIFO STATUS

Offset = 00022050h + (k * 1000h); where k = 0h to 1h

**Table 8-209. CPSW_PN_FIFO_STATUS_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2050h + formula

Figure 8-103. CPSW_PN_FIFO_STATUS_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED					EST_BUFACT	EST_ADD_ER R	EST_CNT_ERR
R-X					R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
TX_E_MAC_ALLOW							
R-FFh							
7	6	5	4	3	2	1	0
TX_PRI_ACTIVE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 8-210. CPSW_PN_FIFO_STATUS_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	X	
18	EST_BUFACT	R	0h	EST RAM active buffer. Indicates the active 64-word fetch buffer when CPSW_PN_EST_CONTROL_REG[0] EST_ONEBUF is cleared to zero. Indicates the fetch RAM address MSB when bit [0] EST_ONEBUF is set to one.
17	EST_ADD_ERR	R	0h	EST Address Error. Indicates that the fetch RAM was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).
16	EST_CNT_ERR	R	0h	EST Fetch Count Error. Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.
15-8	TX_E_MAC_ALLOW	R	FFh	EST transmit MAC allow. Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the preempt queue).

Table 8-210. CPSW_PN_FIFO_STATUS_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	TX_PRI_ACTIVE	R	0h	EST Transmit Priority Active. Bus that indicates which priorities have packets (non-empty) at the time of the register read.

8.2.71 CPSW_PN_EST_CONTROL_REG_k Register (Offset = 00022060h + formula) [reset = X]

CPSW_PN_EST_CONTROL_REG_k is shown in [Figure 8-104](#) and described in [Table 8-212](#).

Return to [Summary Table](#).

Enet Port N EST CONTROL

Offset = 00022060h + (k * 1000h); where k = 0h to 1h

**Table 8-211. CPSW_PN_EST_CONTROL_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2060h + formula

Figure 8-104. CPSW_PN_EST_CONTROL_REG_k Register

31	30	29	28	27	26	25	24
RESERVED						EST_FILL_MARGIN	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
EST_FILL_MARGIN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						EST_FILL_EN	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-212. CPSW_PN_EST_CONTROL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	EST_FILL_MARGIN	R/W	0h	EST Fill Margin. Sets the fill margin required to ensure that the Ethernet wire is clear (including IPG) so that the timed EST express packet can egress at the required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended.
15-9	RESERVED	R/W	X	
8	EST_FILL_EN	R/W	0h	EST Fill Enable. Enable EST fill mode.
7-5	EST_TS_PRI	R/W	0h	EST Timestamp Express Priority. Selects the express priority that timestamp(s) will be generated on when CPSW_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI bit is set.

Table 8-212. CPSW_PN_EST_CONTROL_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	EST_TS_ONEPRI	R/W	0h	EST Timestamp One Express Priority. When set, timestamp only enabled packets on the express priority selected by CPSW_PN_EST_CONTROL_REG[7-5] ST_TS_PRI bit field. When cleared to zero, express packet selection for timestamp is independent of priority.
3	EST_TS_FIRST	R/W	0h	EST Timestamp First Express Packet only. Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If CPSW_PN_EST_CONTROL_REG[4] EST_TS_ONEPRI is also set then the timestamp is generated only on the first packet on CPSW_PN_EST_CONTROL_REG[7-5] ST_TS_PRI).
2	EST_TS_EN	R/W	0h	EST Timestamp Enable. Enable express timestamps (when CPSW_CONTROL_REG[18] EST_ENABLE and CPSW_PN_CONTROL_REG[17] EST_PORT_EN bits are set).
1	EST_BUFSEL	R/W	0h	EST Buffer Select. If CPSW_PN_EST_CONTROL_REG[0] EST_ONEBUF is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the CPSW_PN_FIFO_STATUS_REG register, bit [18] EST_BUFACT.
0	EST_ONEBUF	R/W	0h	EST One Fetch Buffer. When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The CPSW_PN_EST_CONTROL_REG[1] EST_BUFSEL bit selects the buffer to be used when bit [0] EST_ONEBUF is cleared to zero.

8.2.72 CPSW_PN_RX_DSCP_MAP_REG_k_y Register (Offset = 00022120h + formula) [reset = X]

CPSW_PN_RX_DSCP_MAP_REG_k_y is shown in [Figure 8-105](#) and described in [Table 8-214](#).

Return to [Summary Table](#).

Enet Port N Receive IPV4/IPV6 DSCP Map M

Offset = 00022120h + (k * 1000h) + (y * 4h); where k = 0h to 1h, y = 0h to 7h

**Table 8-213. CPSW_PN_RX_DSCP_MAP_REG_k_y
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2120h + formula

Figure 8-105. CPSW_PN_RX_DSCP_MAP_REG_k_y Register

31	30	29	28	27	26	25	24
RESERVED	PRI7			RESERVED	PRI6		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	PRI5			RESERVED	PRI4		
R/W-X	R/W-0h			R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED	PRI3			RESERVED	PRI2		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	PRI1			RESERVED	PRI0		
R/W-X	R/W-0h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-214. CPSW_PN_RX_DSCP_MAP_REG_k_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
27	RESERVED	R/W	X	
26-24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
23	RESERVED	R/W	X	
22-20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
19	RESERVED	R/W	X	
18-16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
15	RESERVED	R/W	X	
14-12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
11	RESERVED	R/W	X	
10-8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
7	RESERVED	R/W	X	

Table 8-214. CPSW_PN_RX_DSCP_MAP_REG_k_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
3	RESERVED	R/W	X	
2-0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

8.2.73 CPSW_PN_PRI_CIR_REG_k_y Register (Offset = 00022140h + formula) [reset = X]

CPSW_PN_PRI_CIR_REG_k_y is shown in [Figure 8-106](#) and described in [Table 8-216](#).

Return to [Summary Table](#).

Enet Port N Rx Priority P Committed Information Rate Value

Offset = 00022140h + (k * 1000h) + (y * 4h); where k = 0h to 1h, y = 0h to 7h

**Table 8-215. CPSW_PN_PRI_CIR_REG_k_y
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2140h + formula

Figure 8-106. CPSW_PN_PRI_CIR_REG_k_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI_CIR																											
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-216. CPSW_PN_PRI_CIR_REG_k_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PRI_CIR	R/W	0h	Priority N committed information rate

8.2.74 CPSW_PN_PRI_EIR_REG_k Register (Offset = 00022160h + formula) [reset = X]

CPSW_PN_PRI_EIR_REG_k is shown in [Figure 8-107](#) and described in [Table 8-218](#).

Return to [Summary Table](#).

Enet Port N Rx Priority P Excess Informatoin Rate Value.

Offset = 00022160h + (k * 1000h) + (y * 4h); where k = 0h to 1h, y = 0h to 7h

Table 8-217. CPSW_PN_PRI_EIR_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2160h + formula

Figure 8-107. CPSW_PN_PRI_EIR_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PRI_EIR																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-218. CPSW_PN_PRI_EIR_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

8.2.75 CPSW_PN_TX_D_THRESH_SET_L_REG_k Register (Offset = 00022180h + formula) [reset = X]

CPSW_PN_TX_D_THRESH_SET_L_REG_k is shown in [Figure 8-108](#) and described in [Table 8-220](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Destination Threshold Set Low.

Offset = 00022180h + (k * 1000h); where k = 0h to 1h

Table 8-219.
CPSW_PN_TX_D_THRESH_SET_L_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2180h + formula

Figure 8-108. CPSW_PN_TX_D_THRESH_SET_L_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-220. CPSW_PN_TX_D_THRESH_SET_L_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

8.2.76 CPSW_PN_TX_D_THRESH_SET_H_REG_k Register (Offset = 00022184h + formula) [reset = X]

CPSW_PN_TX_D_THRESH_SET_H_REG_k is shown in [Figure 8-109](#) and described in [Table 8-222](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Destination Threshold Set High.

Offset = 00022184h + (k * 1000h); where k = 0h to 1h

Table 8-221.
CPSW_PN_TX_D_THRESH_SET_H_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2184h + formula

Figure 8-109. CPSW_PN_TX_D_THRESH_SET_H_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-222. CPSW_PN_TX_D_THRESH_SET_H_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

8.2.77 CPSW_PN_TX_D_THRESH_CLR_L_REG_k Register (Offset = 00022188h + formula) [reset = X]

CPSW_PN_TX_D_THRESH_CLR_L_REG_k is shown in [Figure 8-110](#) and described in [Table 8-224](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Destination Threshold Clr Low.

Offset = 00022188h + (k * 1000h); where k = 0h to 1h

Table 8-223.
CPSW_PN_TX_D_THRESH_CLR_L_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2188h + formula

Figure 8-110. CPSW_PN_TX_D_THRESH_CLR_L_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-224. CPSW_PN_TX_D_THRESH_CLR_L_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

8.2.78 CPSW_PN_TX_D_THRESH_CLR_H_REG_k Register (Offset = 0002218Ch + formula) [reset = X]

CPSW_PN_TX_D_THRESH_CLR_H_REG_k is shown in [Figure 8-111](#) and described in [Table 8-226](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Destination Threshold Clr High.

Offset = 0002218Ch + (k * 1000h); where k = 0h to 1h

Table 8-225.
CPSW_PN_TX_D_THRESH_CLR_H_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 218Ch + formula

Figure 8-111. CPSW_PN_TX_D_THRESH_CLR_H_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-226. CPSW_PN_TX_D_THRESH_CLR_H_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

8.2.79 CPSW_PN_TX_G_BUF_THRESH_SET_L_REG_k Register (Offset = 00022190h + formula) [reset = X]

CPSW_PN_TX_G_BUF_THRESH_SET_L_REG_k is shown in [Figure 8-112](#) and described in [Table 8-228](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Global Buffer Threshold Set Low.

Offset = 00022190h + (k * 1000h); where k = 0h to 1h

Table 8-227.
CPSW_PN_TX_G_BUF_THRESH_SET_L_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2190h + formula

Figure 8-112. CPSW_PN_TX_G_BUF_THRESH_SET_L_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-228. CPSW_PN_TX_G_BUF_THRESH_SET_L_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 0

8.2.80 CPSW_PN_TX_G_BUF_THRESH_SET_H_REG_k Register (Offset = 00022194h + formula) [reset = X]

CPSW_PN_TX_G_BUF_THRESH_SET_H_REG_k is shown in [Figure 8-113](#) and described in [Table 8-230](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Global Buffer Threshold Set High.

Offset = 00022194h + (k * 1000h); where k = 0h to 1h

Table 8-229.
CPSW_PN_TX_G_BUF_THRESH_SET_H_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2194h + formula

Figure 8-113. CPSW_PN_TX_G_BUF_THRESH_SET_H_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-1Fh				R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-230. CPSW_PN_TX_G_BUF_THRESH_SET_H_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	1Fh	Port Priority Based Flow Control Threshold Set Value for Priority 4

8.2.81 CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG_k Register (Offset = 00022198h + formula) [reset = X]

CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG_k is shown in [Figure 8-114](#) and described in [Table 8-232](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Global Buffer Threshold Clr Low

Offset = 00022198h + (k * 1000h); where k = 0h to 1h

Table 8-231.
CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2198h + formula

Figure 8-114. CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3				RESERVED			PRI2					
R/W-X			R/W-0h				R/W-X			R/W-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1				RESERVED			PRI0					
R/W-X			R/W-0h				R/W-X			R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-232. CPSW_PN_TX_G_BUF_THRESH_CLR_L_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

8.2.82 CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG_k Register (Offset = 0002219Ch + formula) [reset = X]

CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG_k is shown in [Figure 8-115](#) and described in [Table 8-234](#).

Return to [Summary Table](#).

Enet Port N Tx PFC Global Buffer Threshold Clr High

Offset = 0002219Ch + (k * 1000h); where k = 0h to 1h

Table 8-233.
CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 219Ch + formula

Figure 8-115. CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-234. CPSW_PN_TX_G_BUF_THRESH_CLR_H_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

8.2.83 CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG_k Register (Offset = 00022300h + formula) [reset = X]

CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG_k is shown in [Figure 8-116](#) and described in [Table 8-236](#).

Return to [Summary Table](#).

Enet Port N Tx Destination Out Flow Add Values Low.

Offset = 00022300h + (k * 1000h); where k = 0h to 1h

Table 8-235.
CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2300h + formula

Figure 8-116. CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI3				RESERVED				PRI2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI1				RESERVED				PRI0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-236. CPSW_PN_TX_D_OFLOW_ADDVAL_L_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
23-21	RESERVED	R/W	X	
20-16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
15-13	RESERVED	R/W	X	
12-8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
7-5	RESERVED	R/W	X	
4-0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

8.2.84 CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG_k Register (Offset = 00022304h + formula) [reset = X]

CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG_k is shown in [Figure 8-117](#) and described in [Table 8-238](#).

Return to [Summary Table](#).

Enet Port N Tx Destination Out Flow Add Values High.

Offset = 00022304h + (k * 1000h); where k = 0h to 1h

Table 8-237.
CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2304h + formula

Figure 8-117. CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI7				RESERVED				PRI6			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PRI5				RESERVED				PRI4			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-238. CPSW_PN_TX_D_OFLOW_ADDVAL_H_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
23-21	RESERVED	R/W	X	
20-16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
15-13	RESERVED	R/W	X	
12-8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
7-5	RESERVED	R/W	X	
4-0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

8.2.85 CPSW_PN_SA_L_REG_k Register (Offset = 00022308h + formula) [reset = X]

CPSW_PN_SA_L_REG_k is shown in [Figure 8-118](#) and described in [Table 8-240](#).

Return to [Summary Table](#).

Enet Port N Tx Pause Frame Source Address Low

Offset = 00022308h + (k * 1000h); where k = 0h to 1h

Table 8-239. CPSW_PN_SA_L_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2308h + formula

Figure 8-118. CPSW_PN_SA_L_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_7_0								MACSRCADDR_15_8							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-240. CPSW_PN_SA_L_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits (byte 0)
7-0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15-8 (byte 1)

8.2.86 CPSW_PN_SA_H_REG_k Register (Offset = 0002230Ch + formula) [reset = 0h]

CPSW_PN_SA_H_REG_k is shown in [Figure 8-119](#) and described in [Table 8-242](#).

Return to [Summary Table](#).

Enet Port N Tx Pause Frame Source Address High.

Offset = 0002230Ch + (k * 1000h); where k = 0h to 1h

Table 8-241. CPSW_PN_SA_H_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 230Ch + formula

Figure 8-119. CPSW_PN_SA_H_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACSRCADDR_23_16								MACSRCADDR_31_24							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_39_32								MACSRCADDR_47_40							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-242. CPSW_PN_SA_H_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23-16 (byte 2)
23-16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31-24 (byte 3)
15-8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39-32 (byte 4)
7-0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47-40 (byte 5)

8.2.87 CPSW_PN_TS_CTL_REG_k Register (Offset = 00022310h + formula) [reset = X]

CPSW_PN_TS_CTL_REG_k is shown in [Figure 8-120](#) and described in [Table 8-244](#).

Return to [Summary Table](#).

Enet Port N Time Sync Control

Offset = 00022310h + (k * 1000h); where k = 0h to 1h

Table 8-243. CPSW_PN_TS_CTL_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2310h + formula

Figure 8-120. CPSW_PN_TS_CTL_REG_k Register

31	30	29	28	27	26	25	24
TS_MSG_TYPE_EN							
R/W-0h							
23	22	21	20	19	18	17	16
TS_MSG_TYPE_EN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-244. CPSW_PN_TS_CTL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable. Each bit in this field enables the corresponding message type in receive and transmit time sync messages (bit 0 enables message type 0 etc.).
15-12	RESERVED	R/W	X	
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable.
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Sync Transmit Annex E enable.
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Sync Receive Annex E enable.
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable (transmit and receive).
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Sync Transmit Annex D enable.
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable.
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable.
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Sync Transmit Annex F enable.
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Sync Receive Annex D enable.
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable.

Table 8-244. CPSW_PN_TS_CTL_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable.
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Sync Receive Annex F Enable.

8.2.88 CPSW_PN_TS_SEQ_LTYPE_REG_k Register (Offset = 00022314h + formula) [reset = X]

CPSW_PN_TS_SEQ_LTYPE_REG_k is shown in [Figure 8-121](#) and described in [Table 8-246](#).

Return to [Summary Table](#).

Enet Port N Time Sync LTYPE (and SEQ_ID_OFFSET).

Offset = 00022314h + (k * 1000h); where k = 0h to 1h

**Table 8-245. CPSW_PN_TS_SEQ_LTYPE_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2314h + formula

Figure 8-121. CPSW_PN_TS_SEQ_LTYPE_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_SEQ_ID_OFFSET					
R/W-X										R/W-1Eh					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LTYPE1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-246. CPSW_PN_TS_SEQ_LTYPE_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	TS_SEQ_ID_OFFSET	R/W	1Eh	Time Sync Sequence ID Offset This is the number of octets that the sequence ID is offset in the TX and RX time sync message header. The minimum value is 6h.
15-0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1 This is the port's time sync LTYPE1 value.

8.2.89 CPSW_PN_TS_VLAN_LTYPE_REG_k Register (Offset = 00022318h + formula) [reset = 0h]

CPSW_PN_TS_VLAN_LTYPE_REG_k is shown in [Figure 8-122](#) and described in [Table 8-248](#).

Return to [Summary Table](#).

Enet Port N Time Sync VLAN2 and VLAN1.

Offset = 00022318h + (k * 1000h); where k = 0h to 1h

**Table 8-247. CPSW_PN_TS_VLAN_LTYPE_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2318h + formula

Figure 8-122. CPSW_PN_TS_VLAN_LTYPE_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_VLAN_LTYPE2																TS_VLAN_LTYPE1															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-248. CPSW_PN_TS_VLAN_LTYPE_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2 This VLAN LTYPE value is used for the port TX and RX time sync decode.
15-0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1 This VLAN LTYPE value is used for the port TX and RX time sync decode.

8.2.90 CPSW_PN_TS_CTL_LTYPE2_REG_k Register (Offset = 0002231Ch + formula) [reset = X]

CPSW_PN_TS_CTL_LTYPE2_REG_k is shown in [Figure 8-123](#) and described in [Table 8-250](#).

Return to [Summary Table](#).

Enet Port N Time Sync Control and LTYPE 2.

Offset = 0002231Ch + (k * 1000h); where k = 0h to 1h

Table 8-249. CPSW_PN_TS_CTL_LTYPE2_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 231Ch + formula

Figure 8-123. CPSW_PN_TS_CTL_LTYPE2_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							TS_UNI_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TS_LTYPE2							
R/W-0h							
7	6	5	4	3	2	1	0
TS_LTYPE2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-250. CPSW_PN_TS_CTL_LTYPE2_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable 0h = Unicast disabled 1h = Unicast enabled
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable 0h = TTL must be 1h 1h = TTL may be any value
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable 0h = Disabled 1h = Destination port number (decimal) 320 is enabled
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable 0h = Disabled 1h = Destination port number (decimal) 319 is enabled
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.1.132 is enabled
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.1.131 is enabled

Table 8-250. CPSW_PN_TS_CTL_LTYPE2_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.1.130 is enabled
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.1.129 is enabled
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable 0h = Disabled 1h = Destination port number (decimal) 224.0.0.107 is enabled
15-0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2 This is the time sync LTYPE1 value for port 1.

8.2.91 CPSW_PN_TS_CTL2_REG_k Register (Offset = 00022320h + formula) [reset = X]

CPSW_PN_TS_CTL2_REG_k is shown in [Figure 8-124](#) and described in [Table 8-252](#).

Return to [Summary Table](#).

Enet Port N Time Sync Control 2.

Offset = 00022320h + (k * 1000h); where k = 0h to 1h

Table 8-251. CPSW_PN_TS_CTL2_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2320h + formula

Figure 8-124. CPSW_PN_TS_CTL2_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_DOMAIN_OFFSET					
R/W-X										R/W-4h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_MCAST_TYPE_EN															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-252. CPSW_PN_TS_CTL2_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	TS_DOMAIN_OFFSET	R/W	4h	Time Sync Domain Offset
15-0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

8.2.92 CPSW_PN_MAC_CONTROL_REG_k Register (Offset = 00022330h + formula) [reset = X]

CPSW_PN_MAC_CONTROL_REG_k is shown in [Figure 8-125](#) and described in [Table 8-254](#).

Return to [Summary Table](#).

Enet Port N Mac Control.

Offset = 00022330h + (k * 1000h); where k = 0h to 1h

**Table 8-253. CPSW_PN_MAC_CONTROL_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2330h + formula

Figure 8-125. CPSW_PN_MAC_CONTROL_REG_k Register

31	30	29	28	27	26	25	24
RESERVED						EXT_EN_XGIG	RX_CMF_EN
R/W-X						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RX_CSF_EN	RX_CEF_EN	TX_SHORT_G AP_LIM_EN	EXT_TX_FLOW _EN	EXT_RX_FLO W_EN	EXT_EN	GIG_FORCE	IFCTL_B
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
IFCTL_A	RESERVED	XGMII_EN	CRC_TYPE	CMD_IDLE	TX_SHORT_G AP_ENABLE	RESERVED	XGIG
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h
7	6	5	4	3	2	1	0
GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-254. CPSW_PN_MAC_CONTROL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25	EXT_EN_XGIG	R/W	0h	10G External Enable
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable. Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied to memory. MAC control frames that are pause frames will be acted upon if enabled in the CPSW_PN_MAC_CONTROL_REG register, regardless of the value of [24] RX_CMF_EN bit. Frames transferred to memory due to [24] RX_CMF_EN will have the control bit set in their EOP buffer descriptor. 0h = MAC control frames are filtered (but acted upon if enabled). 1h = MAC control frames are transferred to memory.

Table 8-254. CPSW_PN_MAC_CONTROL_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	RX_CSF_EN	R/W	0h	<p>RX Copy Short Frames Enable.</p> <p>Enables frames or fragments shorter than 64 bytes to be copied to memory.</p> <p>Frames transferred to memory due to CPSW_PN_MAC_CONTROL_REG[23] RX_CSF_EN will have the fragment or undersized bit set in their receive footer. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors.</p> <p>0h = Short frames are filtered.</p> <p>1h = Short frames are transferred to memory.</p>
22	RX_CEF_EN	R/W	0h	<p>RX Copy Error Frames Enable.</p> <p>Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive footer. Frames containing errors will be filtered when CPSW_PN_MAC_CONTROL_REG[22] RX_CEF_EN is not set.</p> <p>0h = Frames containing errors are filtered.</p> <p>1h = Frames containing errors are transferred to memory.</p>
21	TX_SHORT_GAP_LIM_EN	R/W	0h	<p>Transmit Short Gap Limit Enable</p> <p>When set this bit limits the number of short gap packets transmitted to 100ppm. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII).</p>
20	EXT_TX_FLOW_EN	R/W	0h	<p>External Transmit Flow Control Enable.</p> <p>Enables the TX_FLOW_EN to be selected from the EXT_TX_FLOW_EN input signal and not from the [4] TX_FLOW_EN bit in CPSW_PN_MAC_CONTROL_REG register.</p>
19	EXT_RX_FLOW_EN	R/W	0h	<p>External Receive Flow Control Enable.</p> <p>Enables the RX_FLOW_EN to be selected from the EXT_RX_FLOW_EN input signal and not from the CPSW_PN_MAC_CONTROL_REG[3] RX_FLOW_EN bit in this register.</p>
18	EXT_EN	R/W	0h	<p>External Control Enable.</p> <p>Enables the fullduplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the [0] FULLDUPLEX and [7] GIG bits in the CPSW_PN_MAC_CONTROL_REG register.</p> <p>The [0] FULLDUPLEX bit reflects the actual fullduplex mode selected.</p>
17	GIG_FORCE	R/W	0h	<p>Gigabit Mode Force.</p> <p>This bit is used to force the Ethernet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.</p>
16	IFCTL_B	R/W	0h	Interface Control B - Not used.
15	IFCTL_A	R/W	0h	<p>Interface Control A - Determines the RMII link speed</p> <p>0h = 10Mbps</p> <p>1h = 100Mbps</p>
14	RESERVED	R/W	X	

Table 8-254. CPSW_PN_MAC_CONTROL_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	XGMII_EN	R/W	0h	XGMII Enable. 0h = XGMII RX and TX held in reset. 1h = XGMII RX and TX released from reset.
12	CRC_TYPE	R/W	0h	Port CRC Type. 0h = Ethernet CRC 1h = Castagnoli CRC
11	CMD_IDLE	R/W	0h	Command Idle. 0h = Idle not commanded 1h = Idle Commanded (read bit [31] IDLE in CPSW_PN_MAC_STATUS_REG register)
10	TX_SHORT_GAP_ENAB LE	R/W	0h	Transmit Short Gap Enable. 0h = Transmit with a short IPG is disabled 1h = Transmit with a short IPG (when TX_SHORT_GAP input is asserted) is enabled.
9	RESERVED	R/W	X	
8	XGIG	R	0h	10 Gigabit Mode. Note: 10 Gigabit Mode is not supported for this device.
7	GIG	R/W	0h	Gigabit Mode. 0h = 10/100 mode 1h = Gigabit mode (full duplex only) The GIG_OUT output is the value of this bit.
6	TX_PACE	R/W	0h	Transmit Pacing Enable 0h = Transmit Pacing Disabled 1h = Transmit Pacing Enabled
5	GMII_EN	R/W	0h	GMII Enable. 0h = GMII RX and TX held in reset. 1h = GMII RX and TX released from reset.
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable. Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_ENABLE bits determine whether or not received pause frames are transferred to memory. 0h = Transmit Flow Control Disabled. Full-duplex mode – Incoming pause frames are not acted upon. 1h = Transmit Flow Control Enabled. Full-duplex mode – Incoming pause frames are acted upon.
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable. 0h = Receive Flow Control Disabled Half-duplex mode – No flow control generated collisions are sent. Full-duplex mode – No outgoing pause frames are sent. 1h = Receive Flow Control Enabled Half-duplex mode – Collisions are initiated when receive flow control is triggered. Full-duplex mode – Outgoing pause frames are sent when receive flow control is triggered.
2	MTEST	R/W	0h	Manufacturing Test mode. This bit must be set to allow writes to the CPSW_PN_MAC_BOFFTEST_REG and CPSW_PN_MAC_RX_PAUSETIMER_REG registers.

Table 8-254. CPSW_PN_MAC_CONTROL_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LOOPBACK	R/W	0h	<p>Loop Back Mode.</p> <p>Loopback mode forces internal full duplex mode regardless of whether the CPSW_PN_MAC_CONTROL_REG[0] FULLDUPLEX bit is set or not.</p> <p>The [1] LOOPBACK bit should be changed only when [5] GMII_EN is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS).</p> <p>0h = Not looped back mode 1h = Loop Back mode enabled</p>
0	FULLDUPLEX	R/W	0h	<p>Full Duplex mode.</p> <p>Gigabit mode forces full duplex mode regardless of whether the [0] FULLDUPLEX bit is set or not.</p> <p>The FULLDUPLEX_OUT output is the value of this register bit</p> <p>0h = Half duplex mode 1h = Full duplex mode</p>

8.2.93 CPSW_PN_MAC_STATUS_REG_k Register (Offset = 00022334h + formula) [reset = X]

CPSW_PN_MAC_STATUS_REG_k is shown in [Figure 8-126](#) and described in [Table 8-256](#).

Return to [Summary Table](#).

Enet Port N Mac Status

Offset = 00022334h + (k * 1000h); where k = 0h to 1h

**Table 8-255. CPSW_PN_MAC_STATUS_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2334h + formula

Figure 8-126. CPSW_PN_MAC_STATUS_REG_k Register

31	30	29	28	27	26	25	24
IDLE	E_IDLE	P_IDLE	MAC_TX_IDLE	TORF	TORF_PRI		
R-1h	R-1h	R-1h	R-1h	R-0h	R-0h		
23	22	21	20	19	18	17	16
TX_PFC_FLOW_ACT							
R-0h							
15	14	13	12	11	10	9	8
RX_PFC_FLOW_ACT							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
R-X	R-0h	R-0h	R-0h	R-0h	R-X	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-256. CPSW_PN_MAC_STATUS_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	Enet IDLE. The Ethernet port (express and preempt) are in the Idle state (valid after an Idle command) 0h = The port is not in the Idle state. 1h = The port is in the Idle state.
30	E_IDLE	R	1h	Express MAC is Idle.
29	P_IDLE	R	1h	Preempt MAC is Idle.
28	MAC_TX_IDLE	R	1h	Mac Transmit Idle. Both Preempt and Express MAC Transmit are in Idle state.
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26-24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 7h to clear.
23-16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15-8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
7	RESERVED	R	X	

Table 8-256. CPSW_PN_MAC_STATUS_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	EXT_RX_FLOW_EN	R	0h	External Receive Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG[19] EXT_RX_FLOW_EN input bit.
5	EXT_TX_FLOW_EN	R	0h	External Transmit Flow Control Enable. This is the value of the CPSW_PN_MAC_CONTROL_REG[20] EXT_TX_FLOW_EN input bit.
4	EXT_GIG	R	0h	External GIG. This is the value of the [4] EXT_GIG input bit.
3	EXT_FULLDUPLEX	R	0h	External Full duplex. This is the value of the [3] EXT_FULLDUPLEX input bit.
2	RESERVED	R	X	
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active. When asserted, indicates that receive flow control is enabled and triggered.
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active. When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete.

8.2.94 CPSW_PN_MAC_SOFT_RESET_REG_k Register (Offset = 00022338h + formula) [reset = X]

CPSW_PN_MAC_SOFT_RESET_REG_k is shown in [Figure 8-127](#) and described in [Table 8-258](#).

Return to [Summary Table](#).

Enet Port N Mac Soft Reset.

Offset = 00022338h + (k * 1000h); where k = 0h to 1h

Table 8-257. CPSW_PN_MAC_SOFT_RESET_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2338h + formula

Figure 8-127. CPSW_PN_MAC_SOFT_RESET_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-258. CPSW_PN_MAC_SOFT_RESET_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	SOFT_RESET	R/W	0h	Software reset. Writing a 1h to this bit causes the Ethernet Mac logic to be reset. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a 1h is read, the reset has not yet occurred. If a 0h is read then reset has occurred.

8.2.95 CPSW_PN_MAC_BOFFTEST_REG_k Register (Offset = 0002233Ch + formula) [reset = X]

CPSW_PN_MAC_BOFFTEST_REG_k is shown in [Figure 8-128](#) and described in [Table 8-260](#).

Return to [Summary Table](#).

Enet Port N Mac Backoff Test

Offset = 0002233Ch + (k * 1000h); where k = 0h to 1h

Table 8-259. CPSW_PN_MAC_BOFFTEST_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 233Ch + formula

Figure 8-128. CPSW_PN_MAC_BOFFTEST_REG_k Register

31	30	29	28	27	26	25	24
RESERVED	PACEVAL					RNDNUM	
R/W-X	R/W-0h					R/W-0h	
23	22	21	20	19	18	17	16
RNDNUM							
R/W-0h							
15	14	13	12	11	10	9	8
COLL_COUNT				RESERVED		TX_BACKOFF	
R-0h				R/W-X		R-0h	
7	6	5	4	3	2	1	0
TX_BACKOFF							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-260. CPSW_PN_MAC_BOFFTEST_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-26	PACEVAL	R/W	0h	Pacing Current Value. A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce "capture" effects improving overall network bandwidth.
25-16	RNDNUM	R/W	0h	Backoff Random Number Generator. This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when CPSW_PN_MAC_CONTROL_REG[2] MTEST bit has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.
15-12	COLL_COUNT	R	0h	Collision Count.
11-10	RESERVED	R/W	X	

Table 8-260. CPSW_PN_MAC_BOFFTEST_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	TX_BACKOFF	R	0h	<p>Backoff Count.</p> <p>This field allows the current value of the backoff counter to be observed for test purposes.</p> <p>This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision.</p>

8.2.96 CPSW_PN_MAC_RX_PAUSETIMER_REG_k Register (Offset = 00022340h + formula) [reset = X]

CPSW_PN_MAC_RX_PAUSETIMER_REG_k is shown in [Figure 8-129](#) and described in [Table 8-262](#).

Return to [Summary Table](#).

Enet Port N 802.3 Receive Pause Timer

Offset = 00022340h + (k * 1000h); where k = 0h to 1h

Table 8-261.
CPSW_PN_MAC_RX_PAUSETIMER_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2340h + formula

Figure 8-129. CPSW_PN_MAC_RX_PAUSETIMER_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_PAUSETIMER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-262. CPSW_PN_MAC_RX_PAUSETIMER_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_PAUSETIMER	R/W	0h	<p>RX Pause Timer Value.</p> <p>This field allows the contents of the receive pause timer to be observed (and written in test mode).</p> <p>The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).</p>

8.2.97 CPSW_PN_MAC_RXN_PAUSETIMER_REG_k_y Register (Offset = 00022350h + formula) [reset = X]

CPSW_PN_MAC_RXN_PAUSETIMER_REG_k_y is shown in [Figure 8-130](#) and described in [Table 8-264](#).

Return to [Summary Table](#).

Ethernet Port N PFC Priority 0 to Priority 7 Rx Pause Timer Registers.

Offset = 00022350h + (k * 1000h) + (y * 4h); where k = 0h to 1h, y = 0h to 7h

Table 8-263.
CPSW_PN_MAC_RXN_PAUSETIMER_REG_k_y
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2350h + formula

Figure 8-130. CPSW_PN_MAC_RXN_PAUSETIMER_REG_k_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RX_PAUSETIMER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-264. CPSW_PN_MAC_RXN_PAUSETIMER_REG_k_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_PAUSETIMER	R/W	0h	Rx "y" Pause Timer Value. This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with FF00h when the Ethernet port sends an outgoing pause frame (with pause time of FFFFh). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC)

8.2.98 CPSW_PN_MAC_TX_PAUSETIMER_REG_k Register (Offset = 00022370h + formula) [reset = X]

CPSW_PN_MAC_TX_PAUSETIMER_REG_k is shown in [Figure 8-131](#) and described in [Table 8-266](#).

Return to [Summary Table](#).

Enet Port N 802.3 Tx Pause Timer.

Offset = 00022370h + (k * 1000h); where k = 0h to 1h

Table 8-265.
CPSW_PN_MAC_TX_PAUSETIMER_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2370h + formula

Figure 8-131. CPSW_PN_MAC_TX_PAUSETIMER_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_PAUSETIMER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-266. CPSW_PN_MAC_TX_PAUSETIMER_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_PAUSETIMER	R/W	0h	802.3 Tx Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC).

8.2.99 CPSW_PN_MAC_TXN_PAUSETIMER_REG_k Register (Offset = 00022380h + formula) [reset = X]

CPSW_PN_MAC_TXN_PAUSETIMER_REG_k is shown in [Figure 8-132](#) and described in [Table 8-268](#).

Return to [Summary Table](#).

Ethernet Port N PFC Priority 0 to Priority 7 Tx Pause Timer Registers.

Offset = 00022380h + (k * 1000h) + (y * 4h); where k = 0h to 1h, y = 0h to 7h

Table 8-267.
CPSW_PN_MAC_TXN_PAUSETIMER_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 2380h + formula

Figure 8-132. CPSW_PN_MAC_TXN_PAUSETIMER_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_PAUSETIMER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-268. CPSW_PN_MAC_TXN_PAUSETIMER_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_PAUSETIMER	R/W	0h	PFC Tx "y" Pause Timer Value. This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC)

8.2.100 CPSW_PN_MAC_EMCONTROL_REG_k Register (Offset = 000223A0h + formula) [reset = X]

CPSW_PN_MAC_EMCONTROL_REG_k is shown in [Figure 8-133](#) and described in [Table 8-270](#).

Return to [Summary Table](#).

Enet Port N Emulation Control.

Offset = 000223A0h + (k * 1000h); where k = 0h to 1h

Table 8-269. CPSW_PN_MAC_EMCONTROL_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 23A0h + formula

Figure 8-133. CPSW_PN_MAC_EMCONTROL_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-270. CPSW_PN_MAC_EMCONTROL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

8.2.101 CPSW_PN_MAC_TX_GAP_REG_k Register (Offset = 000223A4h + formula) [reset = X]

CPSW_PN_MAC_TX_GAP_REG_k is shown in [Figure 8-134](#) and described in [Table 8-272](#).

Return to [Summary Table](#).

Enet Port N Tx Inter Packet Gap.

Offset = 000223A4h + (k * 1000h); where k = 0h to 1h

**Table 8-271. CPSW_PN_MAC_TX_GAP_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 23A4h + formula

Figure 8-134. CPSW_PN_MAC_TX_GAP_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TX_GAP															
R/W-X																R/W-Ch															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-272. CPSW_PN_MAC_TX_GAP_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TX_GAP	R/W	Ch	Transmit Inter-Packet Gap GMII modes – This is the default gap value and only bits [8-0] are used. This can be increased from 12 to increase the gap between packets. XGMII mode – In 10 Gigabit mode this is the short gap rate and should be changed to 5000 (1388h) to get approximately 200ppm faster when short gap is triggered and enabled.

8.2.102 CPSW_PN_INTERVLAN_OPX_POINTER_REG_k Register (Offset = 000223ACh + formula) [reset = X]

CPSW_PN_INTERVLAN_OPX_POINTER_REG_k is shown in [Figure 8-135](#) and described in [Table 8-274](#).

Return to [Summary Table](#).

Enet Port N Tx Egress InterVLAN Operation Pointer

Offset = 000223ACh + (k * 1000h); where k = 0h to 1h

Table 8-273.
CPSW_PN_INTERVLAN_OPX_POINTER_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 23ACh + formula

Figure 8-135. CPSW_PN_INTERVLAN_OPX_POINTER_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					INTERVLAN_OPX_POINTER		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-274. CPSW_PN_INTERVLAN_OPX_POINTER_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	INTERVLAN_OPX_POINTER	R/W	0h	Egress InterVLAN Operation Pointer

8.2.103 CPSW_PN_INTERVLAN_OPX_A_REG_k Register (Offset = 000223B0h + formula) [reset = 0h]

CPSW_PN_INTERVLAN_OPX_A_REG_k is shown in [Figure 8-136](#) and described in [Table 8-276](#).

Return to [Summary Table](#).

Enet Port N Tx Egress InterVLAN A

Offset = 000223B0h + (k * 1000h); where k = 0h to 1h

**Table 8-275. CPSW_PN_INTERVLAN_OPX_A_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 23B0h + formula

Figure 8-136. CPSW_PN_INTERVLAN_OPX_A_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERVLAN_OPX_A																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-276. CPSW_PN_INTERVLAN_OPX_A_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DA[23:16]	R/W	0h	Destination Address bits 23-16 – DA byte 4 on wire.
23-16	DA[31:24]	R/W	0h	Destination Address bits 31-24 – DA byte 3 on wire.
15-8	DA[39:32]	R/W	0h	Destination Address bits 39-32 – DA byte 2 on wire.
7-0	DA[47:40]	R/W	0h	Destination Address bits 47-40 – DA byte 1 on wire.

8.2.104 CPSW_PN_INTERVLAN_OPX_B_REG_k Register (Offset = 000223B4h + formula) [reset = 0h]

CPSW_PN_INTERVLAN_OPX_B_REG_k is shown in [Figure 8-137](#) and described in [Table 8-278](#).

Return to [Summary Table](#).

Enet Port N Tx Egress InterVLAN B

Offset = 000223B4h + (k * 1000h); where k = 0h to 1h

Table 8-277. CPSW_PN_INTERVLAN_OPX_B_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 23B4h + formula

Figure 8-137. CPSW_PN_INTERVLAN_OPX_B_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERVLAN_OPX_B																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-278. CPSW_PN_INTERVLAN_OPX_B_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SA[39:32]	R/W	0h	Source Address bits 39-32 – SA byte 2 on wire.
23-16	SA[47:40]	R/W	0h	Source Address bits 47-40 – SA byte 1 on wire.
15-8	DA[7:0]	R/W	0h	Destination Address bits 7-0 – DA byte 6 on wire.
7-0	DA[15:8]	R/W	0h	Destination Address bits 15-8 – DA byte 5 on wire.

8.2.105 CPSW_PN_INTERVLAN_OPX_C_REG_k Register (Offset = 000223B8h + formula) [reset = 0h]

CPSW_PN_INTERVLAN_OPX_C_REG_k is shown in [Figure 8-138](#) and described in [Table 8-280](#).

Return to [Summary Table](#).

Enet Port N Tx Egress InterVLAN C

Offset = 000223B8h + (k * 1000h); where k = 0h to 1h

**Table 8-279. CPSW_PN_INTERVLAN_OPX_C_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 23B8h + formula

Figure 8-138. CPSW_PN_INTERVLAN_OPX_C_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTERVLAN_OPX_C																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-280. CPSW_PN_INTERVLAN_OPX_C_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SA[7:0]	R/W	0h	Source Address bits 7-0 – SA byte 6 on wire.
23-16	SA[15:8]	R/W	0h	Source Address bits 15-8 – SA byte 5 on wire.
15-8	SA[23:16]	R/W	0h	Source Address bits 23-16 – SA byte 4 on wire.
7-0	SA[31:24]	R/W	0h	Source Address bits 31-24 – SA byte 3 on wire.

8.2.106 CPSW_PN_INTERVLAN_OPX_D_REG_k Register (Offset = 000223BCh + formula) [reset = X]

CPSW_PN_INTERVLAN_OPX_D_REG_k is shown in [Figure 8-139](#) and described in [Table 8-282](#).

Return to [Summary Table](#).

Enet Port N Tx Egress InterVLAN D.

Offset = 000223BCh + (k * 1000h); where k = 0h to 1h

Table 8-281. CPSW_PN_INTERVLAN_OPX_D_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_CONTROL	0C02 23BCh + formula

Figure 8-139. CPSW_PN_INTERVLAN_OPX_D_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																INTERVLAN_OPX_D															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-282. CPSW_PN_INTERVLAN_OPX_D_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	INTERVLAN_OPX_D	R/W	0h	Egress InterVLAN D

8.3 CPSW0_CPINT Registers

Table 8-284 lists the memory-mapped registers for the CPSW0_CPINT. All register offset addresses not listed in Table 8-284 should be considered as reserved locations and the register contents should not be modified.

Table 8-283. CPSW0_CPINT Instances

Instance	Base Address
CPSW0_NUSS_CPINT	0C00 0000h

Table 8-284. CPSW0_CPINT Registers

Offset	Acronym	Register Name	CPSW0_NUSS_CP INT Physical Address
1000h	CPSW_INT_REVISION	Revision Register	0C00 1000h
1010h	CPSW_INT_EOI_REG	End of Interrupt Register	0C00 1010h
1014h	CPSW_INT_INTR_VECTOR_REG	Interrupt Vector Register	0C00 1014h
1100h	CPSW_INT_ENABLE_REG_OUT_PULSE_0	Enable Register 0	0C00 1100h
1300h	CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0	Enable Clear Register 0	0C00 1300h
1500h	CPSW_INT_STATUS_REG_OUT_PULSE_0	Status Register 0	0C00 1500h
1A80h	CPSW_INT_INTR_VECTOR_REG_OUT_PULSE	Interrupt Vector for out_pulse	0C00 1A80h

8.3.1 CPSW_INT_REVISION Register (Offset = 1000h) [reset = 6690A200h]

CPSW_INT_REVISION is shown in [Figure 8-140](#) and described in [Table 8-286](#).

Return to [Summary Table](#).

CPSW_INT_REVISION Register.

Table 8-285. CPSW_INT_REVISION Instances

Instance	Physical Address
CPSW0_NUSS_CPINT	0C00 1000h

Figure 8-140. CPSW_INT_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R-1h		R-2h		R-690h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER					MAJREV			CUSTOM		MINREV					
R-14h					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 8-286. CPSW_INT_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	BU
27-16	FUNCTION	R	690h	Module ID
15-11	RTLVER	R	14h	RTL revisions
10-8	MAJREV	R	2h	Major revision
7-6	CUSTOM	R	0h	Custom revision
5-0	MINREV	R	0h	Minor revision

Table 8-287. Register Call Summary for CPSW_INT_REVISION

CPSW0_CPINT Registers

- [CPSW_INT_REVISION Register \(Offset = 1000h\) \[reset = 6690A200h\]: \[0\] \[1\]](#)
- [CPSW0_CPINT Registers: \[0\]](#)

8.3.2 CPSW_INT_EOI_REG Register (Offset = 1010h) [reset = X]

CPSW_INT_EOI_REG is shown in [Figure 8-141](#) and described in [Table 8-289](#).

Return to [Summary Table](#).

End of Interrupt Register.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 8-288. CPSW_INT_EOI_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPINT	0C00 1010h

Figure 8-141. CPSW_INT_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-289. CPSW_INT_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	EOI_VECTOR	R/W	0h	End of Interrupt Vector.

Table 8-290. Register Call Summary for CPSW_INT_EOI_REG

CPSW0_CPINT Registers

- [CPSW0_CPINT Registers: \[0\]](#)
- [CPSW_INT_EOI_REG Register \(Offset = 1010h\) \[reset = X\]: \[0\]](#)

8.3.3 CPSW_INT_INTR_VECTOR_REG Register (Offset = 1014h) [reset = 0h]

CPSW_INT_INTR_VECTOR_REG is shown in [Figure 8-142](#) and described in [Table 8-292](#).

Return to [Summary Table](#).

Interrupt Vector Register.

Table 8-291. CPSW_INT_INTR_VECTOR_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPINT	0C00 1014h

Figure 8-142. CPSW_INT_INTR_VECTOR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VECTOR																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 8-292. CPSW_INT_INTR_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INTR_VECTOR	R	0h	Interrupt Vector Register

Table 8-293. Register Call Summary for CPSW_INT_INTR_VECTOR_REG

CPSW0_CPINT Registers

- [CPSW0_CPINT Registers](#): [0]
- [CPSW_INT_INTR_VECTOR_REG Register \(Offset = 1014h\) \[reset = 0h\]](#): [0]

8.3.4 CPSW_INT_ENABLE_REG_OUT_PULSE_0 Register (Offset = 1100h) [reset = X]

CPSW_INT_ENABLE_REG_OUT_PULSE_0 is shown in [Figure 8-143](#) and described in [Table 8-295](#).

Return to [Summary Table](#).

Enable Register 0.

Table 8-294.
CPSW_INT_ENABLE_REG_OUT_PULSE_0
Instances

Instance	Physical Address
CPSW0_NUSS_CPINT	0C00 1100h

Figure 8-143. CPSW_INT_ENABLE_REG_OUT_PULSE_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDA	ENABLE_OUT_PULSE_EN_MDIO_PENDA	ENABLE_OUT_PULSE_EN_EVTNT_PENDA
R/W-X					R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-295. CPSW_INT_ENABLE_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	ENABLE_OUT_PULSE_EN_STAT_PENDA	R/W1S	0h	Enable Set for out_pulse_en_stat_penda.
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA	R/W1S	0h	Enable Set for out_pulse_en_mdio_penda.
0	ENABLE_OUT_PULSE_EN_EVTNT_PENDA	R/W1S	0h	Enable Set for out_pulse_en_evtnt_penda.

Table 8-296. Register Call Summary for CPSW_INT_ENABLE_REG_OUT_PULSE_0

CPSW0_CPINT Registers

- [CPSW0_CPINT Registers: \[0\]](#)
- [CPSW_INT_ENABLE_REG_OUT_PULSE_0 Register \(Offset = 1100h\) \[reset = X\]: \[0\]](#)

8.3.5 CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 Register (Offset = 1300h) [reset = X]

CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 is shown in [Figure 8-144](#) and described in [Table 8-298](#).

Return to [Summary Table](#).

Enable Clear Register 0.

Table 8-297.
CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0
Instances

Instance	Physical Address
CPSW0_NUSS_CPINT	0C00 1300h

Figure 8-144. CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					ENABLE_OUT_PULSE_EN_STAT_PENDACL_R	ENABLE_OUT_PULSE_EN_MDIO_PENDACL_R	ENABLE_OUT_PULSE_EN_EVT_PENDACL_R
R/W-X					R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-298. CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	ENABLE_OUT_PULSE_EN_STAT_PENDACL_R	R/W1C	0h	Enable Clear for out_pulse_en_stat_penda.
1	ENABLE_OUT_PULSE_EN_MDIO_PENDACL_R	R/W1C	0h	Enable Clear for out_pulse_en_mdio_penda.
0	ENABLE_OUT_PULSE_EN_EVT_PENDACL_R	R/W1C	0h	Enable Clear for out_pulse_en_evt_penda.

Table 8-299. Register Call Summary for CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0

CPSW0_CPINT Registers

- [CPSW_INT_ENABLE_CLR_REG_OUT_PULSE_0 Register \(Offset = 1300h\) \[reset = X\]: \[0\]](#)
- [CPSW0_CPINT Registers: \[0\]](#)

8.3.6 CPSW_INT_STATUS_REG_OUT_PULSE_0 Register (Offset = 1500h) [reset = X]

CPSW_INT_STATUS_REG_OUT_PULSE_0 is shown in [Figure 8-145](#) and described in [Table 8-301](#).

Return to [Summary Table](#).

Status Register 0.

Table 8-300.
CPSW_INT_STATUS_REG_OUT_PULSE_0 Instances

Instance	Physical Address
CPSW0_NUSS_CPINT	0C00 1500h

Figure 8-145. CPSW_INT_STATUS_REG_OUT_PULSE_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED					STATUS_OUT_PULSE_STAT_PENDA	STATUS_OUT_PULSE_MDIO_PENDA	STATUS_OUT_PULSE_EVTNT_PENDA
R-X					R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-301. CPSW_INT_STATUS_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	X	
2	STATUS_OUT_PULSE_STAT_PENDA	R	0h	Status for out_pulse_en_stat_penda.
1	STATUS_OUT_PULSE_MDIO_PENDA	R	0h	Status for out_pulse_en_mdio_penda.
0	STATUS_OUT_PULSE_EVTNT_PENDA	R	0h	Status for out_pulse_en_evtnt_penda.

Table 8-302. Register Call Summary for CPSW_INT_STATUS_REG_OUT_PULSE_0

CPSW0_CPINT Registers

- [CPSW_INT_STATUS_REG_OUT_PULSE_0 Register \(Offset = 1500h\) \[reset = X\]: \[0\]](#)
- [CPSW0_CPINT Registers: \[0\]](#)

8.3.7 CPSW_INT_INTR_VECTOR_REG_OUT_PULSE Register (Offset = 1A80h) [reset = 0h]

CPSW_INT_INTR_VECTOR_REG_OUT_PULSE is shown in [Figure 8-146](#) and described in [Table 8-304](#).

Return to [Summary Table](#).

Interrupt Vector for out_pulse.

Table 8-303.
CPSW_INT_INTR_VECTOR_REG_OUT_PULSE
Instances

Instance	Physical Address
CPSW0_NUSS_CPINT	0C00 1A80h

Figure 8-146. CPSW_INT_INTR_VECTOR_REG_OUT_PULSE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VECTOR_OUT_PULSE																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 8-304. CPSW_INT_INTR_VECTOR_REG_OUT_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INTR_VECTOR_OUT_PULSE	R	0h	Interrupt Vector.

Table 8-305. Register Call Summary for CPSW_INT_INTR_VECTOR_REG_OUT_PULSE

CPSW0_CPINT Registers

- [CPSW0_CPINT Registers: \[0\]](#)
- [CPSW_INT_INTR_VECTOR_REG_OUT_PULSE Register \(Offset = 1A80h\) \[reset = 0h\]: \[0\]](#)

8.4 CPSW0_CPTS Registers

Table 8-307 lists the memory-mapped registers for the CPSW0_CPTS. All register offset addresses not listed in Table 8-307 should be considered as reserved locations and the register contents should not be modified.

Table 8-306. CPSW0_CPTS Instances

Instance	Base Address
CPSW0_NUSS_CPTS	0C00 0000h

Table 8-307. CPSW0_CPTS Registers

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_CPTS .Physical Address
0003D000h	CPSW_CPTS_IDVER_REG	CPSW0 CPTS Identification and Version Register	0C03 D000h
0003D004h	CPSW_CPTS_CONTROL_REG	Time Sync Control Register	0C03 D004h
0003D008h	CPSW_CPTS_RFTCLK_SEL_REG	Reference Clock Select Register	0C03 D008h
0003D00Ch	CPSW_CPTS_TS_PUSH_REG	Time Stamp Event Push Register	0C03 D00Ch
0003D010h	CPSW_CPTS_TS_LOAD_VAL_REG	Time Stamp Load Low Value (lower 32-bits) Register	0C03 D010h
0003D014h	CPSW_CPTS_TS_LOAD_EN_REG	Time Stamp Load Enable Register	0C03 D014h
0003D018h	CPSW_CPTS_TS_COMP_VAL_REG	Time Stamp Comparison Low Value (lower 32-bits) Register	0C03 D018h
0003D01Ch	CPSW_CPTS_TS_COMP_LEN_REG	Time Stamp Comparison Length Register	0C03 D01Ch
0003D020h	CPSW_CPTS_INTSTAT_RAW_REG	Interrupt Status Raw Register	0C03 D020h
0003D024h	CPSW_CPTS_INTSTAT_MASKED_REG	Interrupt Status Masked Register	0C03 D024h
0003D028h	CPSW_CPTS_INT_ENABLE_REG	Interrupt Enable Register Register	0C03 D028h
0003D02Ch	CPSW_CPTS_TS_COMP_NUDGE_REG	Time Stamp Comparison Nudge Value Register	0C03 D02Ch
0003D030h	CPSW_CPTS_EVENT_POP_REG	Event Interrupt Pop Register	0C03 D030h
0003D034h	CPSW_CPTS_EVENT_0_REG	Lower 32-bits of the Event Value Register	0C03 D034h
0003D038h	CPSW_CPTS_EVENT_1_REG	Lower Middle 32-bits of the Event Value Register	0C03 D038h
0003D03Ch	CPSW_CPTS_EVENT_2_REG	Upper Middle 32-bits of the Event Value Register	0C03 D03Ch
0003D040h	CPSW_CPTS_EVENT_3_REG	Upper 32-bits of the Event Value Register	0C03 D040h
0003D044h	CPSW_CPTS_TS_LOAD_HIGH_VAL_REG	Time Stamp Load High Value (upper 32-bits) Register	0C03 D044h
0003D048h	CPSW_CPTS_TS_COMP_HIGH_VAL_REG	Time Stamp Comparison High Value (upper 32-bits) Register	0C03 D048h
0003D04Ch	CPSW_CPTS_TS_ADD_VAL_REG	Time Stamp Add Value Register	0C03 D04Ch
0003D050h	CPSW_CPTS_TS_PPM_LOW_VAL_REG	Time Stamp PPM Load Low Value (lower 32-bits) Register	0C03 D050h
0003D054h	CPSW_CPTS_TS_PPM_HIGH_VAL_REG	Time Stamp PPM Load High Value (upper 32-bits) Register	0C03 D054h
0003D058h	CPSW_CPTS_TS_NUDGE_VAL_REG	Time Stamp Nudge Value Register	0C03 D058h
0003D0E0h	CPSW_GENF0_COMP_LOW_REG	GENF0 Time Stamp Comparison Value Lower 32-bits Registers	0C03 D0E0h
0003D0E4h	CPSW_GENF0_COMP_HIGH_REG	GENF0 Time Stamp Comparison Value Upper 32-bits Registers	0C03 D0E4h
0003D0E8h	CPSW_GENF0_CONTROL_REG	GENF0 Control Register Registers	0C03 D0E8h
0003D0ECh	CPSW_GENF0_LENGTH_REG	GENF0 Length Value Registers	0C03 D0ECh

Table 8-307. CPSW0_CPTS Registers (continued)

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_CPTS .Physical Address
0003D0F0h	CPSW_GENF0_PPM_LOW_REG	GENF0 PPM Value Lower 32-bits Registers	0C03 D0F0h
0003D0F4h	CPSW_GENF0_PPM_HIGH_REG	GENF0 PPM Value Upper 32-bits Registers	0C03 D0F4h
0003D0F8h	CPSW_GENF0_NUDGE_REG	GENF0 Nudge Value Registers	0C03 D0F8h
0003D100h	CPSW_GENF1_COMP_LOW_REG	GENF1 time stamp Comparison Value Lower 32-bits Register	0C03 D100h
0003D104h	CPSW_GENF1_COMP_HIGH_REG	GENF1 time stamp Comparison Value Upper 32-bits Register	0C03 D104h
0003D108h	CPSW_GENF1_CONTROL_REG	GENF1 Control Register	0C03 D108h
0003D10Ch	CPSW_GENF1_LENGTH_REG	GENF1 Length Value Register	0C03 D10Ch
0003D110h	CPSW_GENF1_PPM_LOW_REG	GENF1 PPM Value Lower 32-bits Register	0C03 D110h
0003D114h	CPSW_GENF1_PPM_HIGH_REG	GENF1 PPM Value Upper 32-bits Register	0C03 D114h
0003D118h	CPSW_GENF1_NUDGE_REG	GENF1 Nudge Value Register	0C03 D118h
0003D200h + formula	CPSW_ESTF_COMP_LOW_REG_I	ESTFn (n = 1 to 8) Time Stamp Comparison Value Lower 32-bits Register	0C03 D200h + formula
0003D204h + formula	CPSW_ESTF_COMP_HIGH_REG_I	ESTFn (n = 1 to 8) Time Stamp Comparison Value Upper 32-bits Register	0C03 D204h + formula
0003D208h + formula	CPSW_ESTF_CONTROL_REG_I	ESTFn (n = 1 to 8) Control Register	0C03 D208h + formula
0003D20Ch + formula	CPSW_ESTF_LENGTH_REG_I	ESTFn (n = 1 to 8) Length Value Register	0C03 D20Ch + formula
0003D210h + formula	CPSW_ESTF_PPM_LOW_REG_I	ESTFn (n = 1 to 8) PPM Value Lower 32-bits Register	0C03 D210h + formula
0003D214h + formula	CPSW_ESTF_PPM_HIGH_REG_I	ESTFn (n = 1 to 8) PPM Value Upper 32-bits Register	0C03 D214h + formula
0003D218h + formula	CPSW_ESTF_NUDGE_REG_I	ESTFn (n = 1 to 8) Nudge Value Register	0C03 D218h + formula

(1) I = 0 to 7

8.4.1 CPSW_CPTS_IDVER_REG Register (Offset = 0003D000h) [reset = 4E8A010Ah]

CPSW_CPTS_IDVER_REG is shown in [Figure 8-147](#) and described in [Table 8-309](#).

Return to [Summary Table](#).

CPSW0_NUSS CPTS Identification and Version Register.

Table 8-308. CPSW_CPTS_IDVER_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D000h

Figure 8-147. CPSW_CPTS_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R-4E8Ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER				MAJOR_VER				MINOR_VER							
R-0h				R-1h				R-Ah							

LEGEND: R = Read Only; -n = value after reset

Table 8-309. CPSW_CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_IDENT	R	4E8Ah	Identification value.
15-11	RTL_VER	R	0h	RTL version value.
10-8	MAJOR_VER	R	1h	Major version value.
7-0	MINOR_VER	R	Ah	Minor version value.

8.4.2 CPSW_CPTS_CONTROL_REG Register (Offset = 0003D004h) [reset = X]

CPSW_CPTS_CONTROL_REG is shown in [Figure 8-148](#) and described in [Table 8-311](#).

Return to [Summary Table](#).

Time Sync Control Register.

**Table 8-310. CPSW_CPTS_CONTROL_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D004h

Figure 8-148. CPSW_CPTS_CONTROL_REG Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED						TX_GENF_CLR_EN	TS_RX_NO_EVENT
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
HW8_TS_PUSH_EN	HW7_TS_PUSH_EN	HW6_TS_PUSH_EN	HW5_TS_PUSH_EN	HW4_TS_PUSH_EN	HW3_TS_PUSH_EN	HW2_TS_PUSH_EN	HW1_TS_PUSH_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TS_PPM_DIR	TS_COMP_TOGGLE	MODE	SEQUENCE_EN	TSTAMP_EN	TS_COMP_POLARITY	INT_TEST	CPTS_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-311. CPSW_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TS_SYNC_SEL	R/W	0h	TS_SYNC output time stamp counter bit select. 0h = TS_SYNC disabled. 1h to Fh = TS_SYNC is time stamp counter bits 31 (Fh) down to 17 (1h).
27-18	RESERVED	R/W	0h	
17	TX_GENF_CLR_EN	R/W	0h	GENF (and ESTF) Clear Enable. 0h = A CPTS_GENFn output is not cleared when the associated CPSW_GENF0_LENGTH_REG/ CPSW_GENF1_LENGTH_REG[31:0] is cleared to zero. 1h = A CPTS_GENFn output is cleared when the associated CPSW_GENF0_LENGTH_REG/ CPSW_GENF1_LENGTH_REG[31:0] is cleared to zero.
16	TS_RX_NO_EVENT	R/W	0h	Timestamp Ethernet Receive produces no events. 0h = Ethernet receive timesync events enabled. 1h = Ethernet receive timesync events disabled.
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable.
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable.
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable.
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable.
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable.

Table 8-311. CPSW_CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable.
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable.
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable.
7	TS_PPM_DIR	R/W	0h	PPM Correction Direction. 0h = Increase the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG) by the PPM value. 1h = Decrease the TIME_STAMP[63:0] value (CPSW_CPTS_EVENT_0_REG and CPSW_CPTS_EVENT_3_REG and) by the PPM value.
6	TS_COMP_TOG	R/W	0h	Time Stamp Compare Toggle mode. 0h = TS_COMP is in non-toggle mode. 1h = TS_COMP is in toggle mode.
5	MODE	R/W	0h	64-Bit Mode. 0h = The time stamp is 32-bits with the upper 32-bits forced to zero. 1h = The time stamp is 64-bits.
4	SEQUENCE_EN	R/W	0h	Sequence Enable. 0h = The time stamp value increments with the selected RFTCLK 1h = The time stamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc).
3	TSTAMP_EN	R/W	0h	Host Receive Time Stamp Enable. 0h = Time stamps are disabled on received packets to host. 1h = Time stamps enabled on received packets to host (PCIE_CPTS_CONTROL_REG[0] CPTS_EN must be set).
2	TS_COMP_POLARITY	R/W	1h	TS_COMP Polarity. 0h = TS_COMP is asserted low. 1h = TS_COMP is asserted high.
1	INT_TEST	R/W	0h	Interrupt Test. When set, this bit allows the raw interrupt to be written to facilitate interrupt test.
0	CPTS_EN	R/W	0h	Time Sync Enable. When disabled (cleared to zero), the RCLK domain is held in reset.

8.4.3 CPSW_CPTS_RFTCLK_SEL_REG Register (Offset = 0003D008h) [reset = X]

CPSW_CPTS_RFTCLK_SEL_REG is shown in [Figure 8-149](#) and described in [Table 8-313](#).

Return to [Summary Table](#).

RFTCLK Select Register.

**Table 8-312. CPSW_CPTS_RFTCLK_SEL_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D008h

Figure 8-149. CPSW_CPTS_RFTCLK_SEL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											RFTCLK_SEL				
R/W-X											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-313. CPSW_CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	RFTCLK_SEL	R/W	0h	<p>Reference clock select.</p> <p>This bit field is used to control an external multiplexer that selects one out of 8 clocks for time sync reference.</p> <p>0h = Selects CPSWHSDIV_CLKOUT2 clock</p> <p>1h = Selects MAINHSDIV_CLKOUT3 clock</p> <p>2h = Selects MCU_CPTS0_RFT_CLK I/O pin</p> <p>3h = Selects CPTS0_RFT_CLK I/O pin</p> <p>4h = Selects MCU_EXT_REFCLK0 I/O pin</p> <p>5h = Selects EXT_REFCLK1 I/O pin</p> <p>6h = Selects PCIE0_TXIO_CLK clock</p> <p>7h = Selects PCIE1_TXIO_CLK clock</p> <p>The RFTCLK_SEL value can be written only when the [0] CPTS_EN and [3] TSTAMP_EN bits are cleared to zero in the CPSW_CPTS_CONTROL_REG register.</p>

8.4.4 CPSW_CPTS_TS_PUSH_REG Register (Offset = 0003D00Ch) [reset = X]

CPSW_CPTS_TS_PUSH_REG is shown in [Figure 8-150](#) and described in [Table 8-315](#).

Return to [Summary Table](#).

Time Stamp Event Push Register.

**Table 8-314. CPSW_CPTS_TS_PUSH_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D00Ch

Figure 8-150. CPSW_CPTS_TS_PUSH_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 8-315. CPSW_CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_PUSH	W	0h	Time stamp event push. When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads zero.

8.4.5 CPSW_CPTS_TS_LOAD_VAL_REG Register (Offset = 0003D010h) [reset = 0h]

CPSW_CPTS_TS_LOAD_VAL_REG is shown in [Figure 8-151](#) and described in [Table 8-317](#).

Return to [Summary Table](#).

Time Stamp Load Low Value Register.

Table 8-316. CPSW_CPTS_TS_LOAD_VAL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D010h

Figure 8-151. CPSW_CPTS_TS_LOAD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-317. CPSW_CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	Time stamp load low value.

8.4.6 CPSW_CPTS_TS_LOAD_EN_REG Register (Offset = 0003D014h) [reset = X]

CPSW_CPTS_TS_LOAD_EN_REG is shown in [Figure 8-152](#) and described in [Table 8-319](#).

Return to [Summary Table](#).

Time Stamp Load Enable Register.

**Table 8-318. CPSW_CPTS_TS_LOAD_EN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D014h

Figure 8-152. CPSW_CPTS_TS_LOAD_EN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 8-319. CPSW_CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_LOAD_EN	W	0h	Time Stamp Load Enable. Writing a one to this bit enables the time stamp value to be written with the value in CPSW_CPTS_TS_LOAD_VAL_REG/ CPSW_CPTS_TS_LOAD_HIGH_VAL_REG. This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the time stamp (CPSW_CPTS_TS_LOAD_HIGH_VAL_REG) are forced to zero in 32-bit mode.

8.4.7 CPSW_CPTS_TS_COMP_VAL_REG Register (Offset = 0003D018h) [reset = 0h]

CPSW_CPTS_TS_COMP_VAL_REG is shown in [Figure 8-153](#) and described in [Table 8-321](#).

Return to [Summary Table](#).

Time Stamp Comparison Low Value (lower 32-bits) Register.

Table 8-320. CPSW_CPTS_TS_COMP_VAL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D018h

Figure 8-153. CPSW_CPTS_TS_COMP_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-321. CPSW_CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_VAL	R/W	0h	Time Stamp Comparison Low Value. Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL.

8.4.8 CPSW_CPTS_TS_COMP_LEN_REG Register (Offset = 0003D01Ch) [reset = 0h]

CPSW_CPTS_TS_COMP_LEN_REG is shown in [Figure 8-154](#) and described in [Table 8-323](#).

Return to [Summary Table](#).

Time Stamp Comparison Length Register.

**Table 8-322. CPSW_CPTS_TS_COMP_LEN_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D01Ch

Figure 8-154. CPSW_CPTS_TS_COMP_LEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-323. CPSW_CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_LENGTH	R/W	0h	Time Stamp Comparison Length. Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the CPSW_GENF0_COMP_LOW_REG_L[31-0] COMP_LOW and CPSW_GENF0_COMP_HIGH_REG_L[31-0] COMP_HIGH registers are written.

8.4.9 CPSW_CPTS_INTSTAT_RAW_REG Register (Offset = 0003D020h) [reset = X]

CPSW_CPTS_INTSTAT_RAW_REG is shown in [Figure 8-155](#) and described in [Table 8-325](#).

Return to [Summary Table](#).

Interrupt Status Register Raw.

Table 8-324. CPSW_CPTS_INTSTAT_RAW_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D020h

Figure 8-155. CPSW_CPTS_INTSTAT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_RAW
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-325. CPSW_CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable). Writable when CPSW_CPTS_CONTROL_REG[1] INT_TEST = 1h A one in this bit indicates that there are one or more events in the event FIFO.

8.4.10 CPSW_CPTS_INTSTAT_MASKED_REG Register (Offset = 0003D024h) [reset = X]

CPSW_CPTS_INTSTAT_MASKED_REG is shown in [Figure 8-156](#) and described in [Table 8-327](#).

Return to [Summary Table](#).

Interrupt Status Register Masked.

**Table 8-326. CPSW_CPTS_INTSTAT_MASKED_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D024h

Figure 8-156. CPSW_CPTS_INTSTAT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-327. CPSW_CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable).

8.4.11 CPSW_CPTS_INT_ENABLE_REG Register (Offset = 0003D028h) [reset = X]

CPSW_CPTS_INT_ENABLE_REG is shown in [Figure 8-157](#) and described in [Table 8-329](#).

Return to [Summary Table](#).

Interrupt Enable Register.

**Table 8-328. CPSW_CPTS_INT_ENABLE_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D028h

Figure 8-157. CPSW_CPTS_INT_ENABLE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-329. CPSW_CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable.

8.4.12 CPSW_CPTS_TS_COMP_NUDGE_REG Register (Offset = 0003D02Ch) [reset = X]

CPSW_CPTS_TS_COMP_NUDGE_REG is shown in [Figure 8-158](#) and described in [Table 8-331](#).

Return to [Summary Table](#).

Time Stamp Comparison Nudge Value Register.

Table 8-330. CPSW_CPTS_TS_COMP_NUDGE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D02Ch

Figure 8-158. CPSW_CPTS_TS_COMP_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-331. CPSW_CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time stamp Comparison Nudge Value. This two's complement number is added to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH value to increase or decrease the TS_COMP length by the CPSW_CPTS_TS_COMP_NUDGE_REG[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_CPTS_TS_COMP_NUDGE_REG value is cleared to zero when the nudge has occurred.

8.4.13 CPSW_CPTS_EVENT_POP_REG Register (Offset = 0003D030h) [reset = X]

CPSW_CPTS_EVENT_POP_REG is shown in [Figure 8-159](#) and described in [Table 8-333](#).

Return to [Summary Table](#).

Event Interrupt Pop Register.

Table 8-332. CPSW_CPTS_EVENT_POP_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D030h

Figure 8-159. CPSW_CPTS_EVENT_POP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 8-333. CPSW_CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	EVENT_POP	W	0h	<p>Event Pop.</p> <p>When a logic high is written to this bit an event is popped off the event FIFO.</p> <p>The event FIFO pop occurs as part of the interrupt process after the event has been read from the CPSW_CPTS_EVENT_0_REG to CPSW_CPTS_EVENT_3_REG registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.</p>

8.4.14 CPSW_CPTS_EVENT_0_REG Register (Offset = 0003D034h) [reset = 0h]

CPSW_CPTS_EVENT_0_REG is shown in [Figure 8-160](#) and described in [Table 8-335](#).

Return to [Summary Table](#).

Lower 32-bits of the Event Value Register.

Table 8-334. CPSW_CPTS_EVENT_0_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D034h

Figure 8-160. CPSW_CPTS_EVENT_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 8-335. CPSW_CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp. The time stamp is valid for transmit, receive, and time stamp push event types. The time stamp value is not valid for counter roll event types.

8.4.15 CPSW_CPTS_EVENT_1_REG Register (Offset = 0003D038h) [reset = X]

CPSW_CPTS_EVENT_1_REG is shown in [Figure 8-161](#) and described in [Table 8-337](#).

Return to [Summary Table](#).

Lower Middle 32-bits of the Event Value Register.

Table 8-336. CPSW_CPTS_EVENT_1_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D038h

Figure 8-161. CPSW_CPTS_EVENT_1_REG Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
R-X		R-0h	R-0h				
23	22	21	20	19	18	17	16
EVENT_TYPE				MESSAGE_TYPE			
R-0h				R-0h			
15	14	13	12	11	10	9	8
SEQUENCE_ID							
R-0h							
7	6	5	4	3	2	1	0
SEQUENCE_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 8-337. CPSW_CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29	PREMPT_QUEUE	R	0h	Prempt QUEUE
28-24	PORT_NUMBER	R	0h	Port Number. Indicates the port number (encoded) of an Ethernet event or the encoded hardware time stamp number.
23-20	EVENT_TYPE	R	0h	Time Sync Event Type 0h = Time Stamp Push Event 1h = Time Stamp Rollover Event 2h = Time Stamp Half Rollover Event 3h = Hardware Time Stamp Push Event 4h = Ethernet Receive Event 5h = Ethernet Transmit Event 6h = Time Stamp Compare Event 7h = Host Transmit Event 8H to Fh = Reserved
19-16	MESSAGE_TYPE	R	0h	Message type. The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

Table 8-337. CPSW_CPTS_EVENT_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	SEQUENCE_ID	R	0h	<p>Sequence ID.</p> <p>The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet.</p> <p>This field is valid only for Ethernet transmit or receive events.</p>

8.4.16 CPSW_CPTS_EVENT_2_REG Register (Offset = 0003D03Ch) [reset = X]

CPSW_CPTS_EVENT_2_REG is shown in [Figure 8-162](#) and described in [Table 8-339](#).

Return to [Summary Table](#).

Upper Middle 32-bits of the Event Value Register.

Table 8-338. CPSW_CPTS_EVENT_2_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D03Ch

Figure 8-162. CPSW_CPTS_EVENT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DOMAIN							
R-X																								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 8-339. CPSW_CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	DOMAIN	R	0h	Domain. The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

8.4.17 CPSW_CPTS_EVENT_3_REG Register (Offset = 0003D040h) [reset = 0h]

CPSW_CPTS_EVENT_3_REG is shown in [Figure 8-163](#) and described in [Table 8-341](#).

Return to [Summary Table](#).

Upper 32-bits of the Event Value Register.

Table 8-340. CPSW_CPTS_EVENT_3_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D040h

Figure 8-163. CPSW_CPTS_EVENT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 8-341. CPSW_CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp. The time stamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode.

8.4.18 CPSW_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 0003D044h) [reset = 0h]

CPSW_CPTS_TS_LOAD_HIGH_VAL_REG is shown in [Figure 8-164](#) and described in [Table 8-343](#).

Return to [Summary Table](#).

Time Stamp Load High Value (upper 32-bits) Register

Table 8-342.
CPSW_CPTS_TS_LOAD_HIGH_VAL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D044h

Figure 8-164. CPSW_CPTS_TS_LOAD_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-343. CPSW_CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	<p>Time Stamp Load high Value.</p> <p>Writing the CPSW_CPTS_TS_LOAD_EN_REG[0] TS_LOAD_EN bit causes the value contained in this register to be written into the time stamp.</p> <p>The time stamp value is read by initiating a time stamp push event, not by reading this register.</p> <p>When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode</p>

8.4.19 CPSW_CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 0003D048h) [reset = 0h]

CPSW_CPTS_TS_COMP_HIGH_VAL_REG is shown in [Figure 8-165](#) and described in [Table 8-345](#).

Return to [Summary Table](#).

Time Stamp Comparison High Value (upper 32-bits) Register.

Table 8-344.
CPSW_CPTS_TS_COMP_HIGH_VAL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D048h

Figure 8-165. CPSW_CPTS_TS_COMP_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-345. CPSW_CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_HIGH_VAL	R/W	0h	<p>Time Stamp Comparison High Value.</p> <p>Writing a non-zero value to the CPSW_CPTS_TS_COMP_LEN_REG[31-0] TS_COMP_LENGTH register causes a pulse of TS_COMP_LENGTH RCLK periods on the TS_COMP output and a comparison event when the [31-0]TIME_STAMP counter value is equivalent to CPSW_CPTS_TS_COMP_VAL_REG[31-0] TS_COMP_VAL and CPSW_CPTS_TS_COMP_HIGH_VAL_REG[31-0] TS_COMP_HIGH_VAL.</p> <p>This value is unused in 32-bit mode. The upper 32-bits in CPSW_CPTS_TS_COMP_HIGH_VAL_REG register should be written before the lower 32-bits in the CPSW_CPTS_TS_COMP_VAL_REG register.</p>

8.4.20 CPSW_CPTS_TS_ADD_VAL_REG Register (Offset = 0003D04Ch) [reset = X]

CPSW_CPTS_TS_ADD_VAL_REG is shown in [Figure 8-166](#) and described in [Table 8-347](#).

Return to [Summary Table](#).

TS Add Value Register.

**Table 8-346. CPSW_CPTS_TS_ADD_VAL_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D04Ch

Figure 8-166. CPSW_CPTS_TS_ADD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADD_VAL		
R/W-X													R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-347. CPSW_CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	ADD_VAL	R/W	0h	<p>The ts_add_value[2:0] is added to 1 to comprise the time stamp increment value.</p> <p>The time stamp increment value is added to the current time stamp (time_stamp[63:0]) on each RCLK. The time stamp increment value can be adjusted by nudge and ppm also. The CPSW_CPTS_TS_ADD_VAL_REG[2-0] ADD_VAL value may be non-zero in 64-bit mode only.</p>

8.4.21 CPSW_CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 0003D050h) [reset = 0h]

CPSW_CPTS_TS_PPM_LOW_VAL_REG is shown in [Figure 8-167](#) and described in [Table 8-349](#).

Return to [Summary Table](#).

Time Stamp PPM Load Low Value (lower 32-bits) Register.

Table 8-348. CPSW_CPTS_TS_PPM_LOW_VAL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D050h

Figure 8-167. CPSW_CPTS_TS_PPM_LOW_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-349. CPSW_CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_PPM_LOW_VAL	R/W	0h	Time Stamp PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen.

8.4.22 CPSW_CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 0003D054h) [reset = X]

CPSW_CPTS_TS_PPM_HIGH_VAL_REG is shown in [Figure 8-168](#) and described in [Table 8-351](#).

Return to [Summary Table](#).

Time Stamp PPM Load High Value (upper 32-bits) Register.

Table 8-350.
CPSW_CPTS_TS_PPM_HIGH_VAL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D054h

Figure 8-168. CPSW_CPTS_TS_PPM_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_PPM_HIGH_VAL							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-351. CPSW_CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TS_PPM_HIGH_VAL	R/W	0h	Time Stamp PPM High Value. This value should be written first (before the low value is written). The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).

8.4.23 CPSW_CPTS_TS_NUDGE_VAL_REG Register (Offset = 0003D058h) [reset = X]

CPSW_CPTS_TS_NUDGE_VAL_REG is shown in [Figure 8-169](#) and described in [Table 8-353](#).

Return to [Summary Table](#).

Time Stamp Nudge Value Register.

Table 8-352. CPSW_CPTS_TS_NUDGE_VAL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D058h

Figure 8-169. CPSW_CPTS_TS_NUDGE_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_NUDGE_VAL							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-353. CPSW_CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS_NUDGE_VAL	R/W	0h	<p>Time stamp Nudge Value.</p> <p>This two's complement number is added to the CPSW_CPTS_EVENT_0_REG[31-0] TIME_STAMP and CPSW_CPTS_EVENT_3_REG[[31-0] TIME_STAMP value to increase or decrease the time stamp value by the CPSW_CPTS_TS_NUDGE_VAL_REG[7-0] TS_NUDGE_VAL amount. The TS_NUDGE_VAL value is cleared to zero when the nudge has occurred.</p> <p>The minimum value of the Time Stamp PPM is 0x400 (all 42 bits: CPSW_CPTS_TS_PPM_LOW_VAL_REG[31-0] TS_PPM_LOW_VAL and CPSW_CPTS_TS_PPM_HIGH_VAL_REG[9-0] TS_PPM_HIGH_VAL).</p>

8.4.24 CPSW_GENF0_COMP_LOW_REG Register (Offset = 0003D0E0h) [reset = 0h]

CPSW_GENF0_COMP_LOW_REG is shown in [Figure 8-170](#) and described in [Table 8-355](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Comparison Low Value (lower 32-bits).

Table 8-354. CPSW_GENF0_COMP_LOW_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D0E0h

Figure 8-170. CPSW_GENF0_COMP_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-355. CPSW_GENF0_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_GENF0_COMP_HIGH_REG_L and CPSW_GENF0_COMP_LOW_REG_L should only be written when the CPSW_GENF0_LENGTH_REG[31-0] LENGTH value is zero.

8.4.25 CPSW_GENF0_COMP_HIGH_REG Register (Offset = 0003D0E4h) [reset = 0h]

CPSW_GENF0_COMP_HIGH_REG is shown in [Figure 8-171](#) and described in [Table 8-357](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Comparison high Value (upper 32-bits).

Table 8-356. CPSW_GENF0_COMP_HIGH_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D0E4h

Figure 8-171. CPSW_GENF0_COMP_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-357. CPSW_GENF0_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits. The CPSW_GENF0_COMP_HIGH_REG_L and CPSW_GENF0_COMP_LOW_REG_L should only be written when the CPSW_GENF0_LENGTH_REG[31-0] LENGTH value is zero.

8.4.26 CPSW_GENF0_CONTROL_REG Register (Offset = 0003D0E8h) [reset = X]

CPSW_GENF0_CONTROL_REG is shown in [Figure 8-172](#) and described in [Table 8-359](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Control Registers.

Table 8-358. CPSW_GENF0_CONTROL_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D0E8h

Figure 8-172. CPSW_GENF0_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-359. CPSW_GENF0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert 0h = The output TS_GENFn signal asserts low 1h = The output TS_GENFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction. 0h = A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h = A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

8.4.27 CPSW_GENF0_LENGTH_REG Register (Offset = 0003D0ECh) [reset = 0h]

CPSW_GENF0_LENGTH_REG is shown in [Figure 8-173](#) and described in [Table 8-361](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Length Value.

**Table 8-360. CPSW_GENF0_LENGTH_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D0ECh

Figure 8-173. CPSW_GENF0_LENGTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-361. CPSW_GENF0_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value.

8.4.28 CPSW_GENF0_PPM_LOW_REG Register (Offset = 0003D0F0h) [reset = 0h]

CPSW_GENF0_PPM_LOW_REG is shown in [Figure 8-174](#) and described in [Table 8-363](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) PPM Low Value (lower 32-bits).

Table 8-362. CPSW_GENF0_PPM_LOW_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D0F0h

Figure 8-174. CPSW_GENF0_PPM_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-363. CPSW_GENF0_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

8.4.29 CPSW_GENF0_PPM_HIGH_REG Register (Offset = 0003D0F4h) [reset = X]

CPSW_GENF0_PPM_HIGH_REG is shown in [Figure 8-175](#) and described in [Table 8-365](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) PPM High Value (upper 32-bits).

**Table 8-364. CPSW_GENF0_PPM_HIGH_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D0F4h

Figure 8-175. CPSW_GENF0_PPM_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-365. CPSW_GENF0_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value. This value should be written first (before the low value is written).

8.4.30 CPSW_GENF0_NUDGE_REG Register (Offset = 0003D0F8h) [reset = X]

CPSW_GENF0_NUDGE_REG is shown in [Figure 8-176](#) and described in [Table 8-367](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF0) Nudge Value Registers.

Table 8-366. CPSW_GENF0_NUDGE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D0F8h

Figure 8-176. CPSW_GENF0_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-367. CPSW_GENF0_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_GENF0_NUDGE_REG_L[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_GENF0_NUDGE_REG_L value is cleared to zero when the nudge has occurred.

8.4.31 CPSW_GENF1_COMP_LOW_REG Register (Offset = 0003D100h) [reset = 0h]

CPSW_GENF1_COMP_LOW_REG is shown in [Figure 8-177](#) and described in [Table 8-369](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Comparison Low Value.

**Table 8-368. CPSW_GENF1_COMP_LOW_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D100h

Figure 8-177. CPSW_GENF1_COMP_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-369. CPSW_GENF1_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function (GENF1) Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_GENF1_COMP_HIGH_REG_L and CPSW_GENF1_COMP_LOW_REG should only be written when the CPSW_GENF1_LENGTH_REG_L[31-0] LENGTH value is zero.

8.4.32 CPSW_GENF1_COMP_HIGH_REG Register (Offset = 0003D104h) [reset = 0h]

CPSW_GENF1_COMP_HIGH_REG is shown in [Figure 8-178](#) and described in [Table 8-371](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Comparison high Value (upper 32-bits).

Table 8-370. CPSW_GENF1_COMP_HIGH_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D104h

Figure 8-178. CPSW_GENF1_COMP_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-371. CPSW_GENF1_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function (GENF1) Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits are written. The CPSW_GENF1_COMP_HIGH_REG and CPSW_GENF1_COMP_LOW_REG should only be written when the CPSW_GENF0_LENGTH_REG[31-0] LENGTH value is zero.

8.4.33 CPSW_GENF1_CONTROL_REG Register (Offset = 0003D108h) [reset = X]

CPSW_GENF1_CONTROL_REG is shown in [Figure 8-179](#) and described in [Table 8-373](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Control Register.

**Table 8-372. CPSW_GENF1_CONTROL_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D108h

Figure 8-179. CPSW_GENF1_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-373. CPSW_GENF1_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function (GENF1) Polarity Invert. 0h = The output TS_GENFn signal asserts low 1h = The output TS_GENFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function (GENF1) PPM Direction. 0h = A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h = A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

8.4.34 CPSW_GENF1_LENGTH_REG Register (Offset = 0003D10Ch) [reset = 0h]

CPSW_GENF1_LENGTH_REG is shown in [Figure 8-180](#) and described in [Table 8-375](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Length Value.

**Table 8-374. CPSW_GENF1_LENGTH_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D10Ch

Figure 8-180. CPSW_GENF1_LENGTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-375. CPSW_GENF1_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp Generate Function (GENF1) Length Value.

8.4.35 CPSW_GENF1_PPM_LOW_REG Register (Offset = 0003D110h) [reset = 0h]

CPSW_GENF1_PPM_LOW_REG is shown in [Figure 8-181](#) and described in [Table 8-377](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) PPM Low Value (lower 32-bits).

**Table 8-376. CPSW_GENF1_PPM_LOW_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D110h

Figure 8-181. CPSW_GENF1_PPM_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-377. CPSW_GENF1_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp Generate Function (GENF1) PPM Low Value The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

8.4.36 CPSW_GENF1_PPM_HIGH_REG Register (Offset = 0003D114h) [reset = X]

CPSW_GENF1_PPM_HIGH_REG is shown in [Figure 8-182](#) and described in [Table 8-379](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) PPM High Value (upper 32-bits).

Table 8-378. CPSW_GENF1_PPM_HIGH_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D114h

Figure 8-182. CPSW_GENF1_PPM_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-379. CPSW_GENF1_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp Generate Function (GENF1) PPM High Value. This value should be written first (before the low value is written).

8.4.37 CPSW_GENF1_NUDGE_REG Register (Offset = 0003D118h) [reset = X]

CPSW_GENF1_NUDGE_REG is shown in [Figure 8-183](#) and described in [Table 8-381](#).

Return to [Summary Table](#).

Time Stamp Generate Function (GENF1) Nudge Value.

Table 8-380. CPSW_GENF1_NUDGE_REG Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D118h

Figure 8-183. CPSW_GENF1_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-381. CPSW_GENF1_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp Generate Function (GENF1) Nudge Value . This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_GENF_NUDGE_REG[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_GENF_NUDGE_REG value is cleared to zero when the nudge has occurred.

8.4.38 CPSW_ESTF_COMP_LOW_REG_I Register (Offset = 0003D200h + formula) [reset = 0h]

CPSW_ESTF_COMP_LOW_REG_I is shown in [Figure 8-184](#) and described in [Table 8-383](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTF_n, where n = 1 to 8) Comparison Low Value.

Offset = 0003D200h + (I * 20h); where I = 0h to 7h.

**Table 8-382. CPSW_ESTF_COMP_LOW_REG_I
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D200h + formula

Figure 8-184. CPSW_ESTF_COMP_LOW_REG_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-383. CPSW_ESTF_COMP_LOW_REG_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function (ESTF _n , where n = 1 to 8) Comparison Low Value (lower 32-bits). This value should be written after the upper 32-bits. The CPSW_ESTF_COMP_HIGH_REG_L and CPSW_ESTF_COMP_LOW_REG should only be written when the CPSW_ESTF_LENGTH_REG_L[31-0] LENGTH value is zero.

8.4.39 CPSW_ESTF_COMP_HIGH_REG_I Register (Offset = 0003D204h + formula) [reset = 0h]

CPSW_ESTF_COMP_HIGH_REG_I is shown in [Figure 8-185](#) and described in [Table 8-385](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTFn, where n = 1 to 8) Comparison high Value (upper 32-bits).

Offset = 0003D204h + (I * 20h); where I = 0h to 7h.

**Table 8-384. CPSW_ESTF_COMP_HIGH_REG_I
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D204h + formula

Figure 8-185. CPSW_ESTF_COMP_HIGH_REG_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-385. CPSW_ESTF_COMP_HIGH_REG_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 8) Comparison High Value (upper 32-bits). This value should be written before the lower 32-bits are written. The CPSW_ESTF_COMP_HIGH_REG and CPSW_ESTF_COMP_LOW_REG should only be written when the CPSW_ESTF_LENGTH_REG_L[31-0] LENGTH value is zero.

8.4.40 CPSW_ESTF_CONTROL_REG_I Register (Offset = 0003D208h + formula) [reset = X]

CPSW_ESTF_CONTROL_REG_I is shown in [Figure 8-186](#) and described in [Table 8-387](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTFn, where n = 1 to 8) Control Register.

Offset = 0003D208h + (I * 20h); where I = 0h to 7h.

**Table 8-386. CPSW_ESTF_CONTROL_REG_I
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D208h + formula

Figure 8-186. CPSW_ESTF_CONTROL_REG_I Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-387. CPSW_ESTF_CONTROL_REG_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 8) Polarity Invert. 0h = The output TS_ESTFn signal asserts low 1h = The output TS_ESTFn signal asserts high
0	PPM_DIR	R/W	0h	Time Stamp Generate Function (ESTFn, where n = 1 to 8) PPM Direction. 0h = A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1h = A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.

8.4.41 CPSW_ESTF_LENGTH_REG_I Register (Offset = 0003D20Ch + formula) [reset = 0h]

CPSW_ESTF_LENGTH_REG_I is shown in [Figure 8-187](#) and described in [Table 8-389](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTFn, where n = 1 to 8) Length Value.

Offset = 0003D20Ch + (I * 20h); where I = 0h to 7h.

**Table 8-388. CPSW_ESTF_LENGTH_REG_I
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D20Ch + formula

Figure 8-187. CPSW_ESTF_LENGTH_REG_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-389. CPSW_ESTF_LENGTH_REG_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp ESTFn (n = 1 to 8) Generate Function Length Value.

8.4.42 CPSW_ESTF_PPM_LOW_REG_I Register (Offset = 0003D210h + formula) [reset = 0h]

CPSW_ESTF_PPM_LOW_REG_I is shown in [Figure 8-188](#) and described in [Table 8-391](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTFn, where n = 1 to 8) PPM Low Value (lower 32-bits).

Offset = 0003D210h + (I * 20h); where I = 0h to 7h.

**Table 8-390. CPSW_ESTF_PPM_LOW_REG_I
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D210h + formula

Figure 8-188. CPSW_ESTF_PPM_LOW_REG_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-391. CPSW_ESTF_PPM_LOW_REG_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp ESTFn (n = 1 to 8) Generate Function PPM Low Value. The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

8.4.43 CPSW_ESTF_PPM_HIGH_REG_I Register (Offset = 0003D214h + formula) [reset = X]

CPSW_ESTF_PPM_HIGH_REG_I is shown in [Figure 8-189](#) and described in [Table 8-393](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTFn, where n = 1 to 8) PPM High Value (upper 32-bits).

Offset = 0003D214h + (I * 20h); where I = 0h to 7h.

**Table 8-392. CPSW_ESTF_PPM_HIGH_REG_I
Instances**

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D214h + formula

Figure 8-189. CPSW_ESTF_PPM_HIGH_REG_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-393. CPSW_ESTF_PPM_HIGH_REG_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp ESTFn (n = 1 to 8) Generate Function PPM High Value. This value should be written first (before the low value is written).

8.4.44 CPSW_ESTF_NUDGE_REG_I Register (Offset = 0003D218h + formula) [reset = X]

CPSW_ESTF_NUDGE_REG_I is shown in [Figure 8-190](#) and described in [Table 8-395](#).

Return to [Summary Table](#).

Time Stamp Generate Function (ESTFn, where n = 1 to 8) Nudge Value.

Offset = 0003D218h + (I * 20h); where I = 0h to 7h.

Table 8-394. CPSW_ESTF_NUDGE_REG_I Instances

Instance	Physical Address
CPSW0_NUSS_CPTS	0C03 D218h + formula

Figure 8-190. CPSW_ESTF_NUDGE_REG_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RESERVED																								NUDGE											
R/W-X																								R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-395. CPSW_ESTF_NUDGE_REG_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp ESTFn (n = 1 to 8) Generate Function Nudge Value. This two's complement number is added to the generate counter value to increase or decrease the length by the CPSW_ESTF_NUDGE_REG[7-0] NUDGE amount. Only a single high or low time is adjusted and the CPSW_ESTF_NUDGE_REG value is cleared to zero when the nudge has occurred.

8.5 CPSW0_ECC Registers

Table 8-397 lists the memory-mapped registers for the CPSW0_ECC registers. All register offset addresses not listed in Table 8-397 should be considered as reserved locations and the register contents should not be modified.

Table 8-396. CPSW0_ECC Instances

Instance	Base Address
CPSW0_ECC	02A2 1000h

Table 8-397. CPSW0_ECC Registers

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_ECC Physical Address
0h	CPSW_ECC_REV	Aggregator Revision Register	02A2 1000h
8h	CPSW_ECC_VECTOR	ECC Vector Register	02A2 1008h
Ch	CPSW_ECC_STAT	Misc Status	02A2 100Ch
10h + formula	CPSW_ECC_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	02A2 1010h + formula
3Ch	CPSW_ECC_SEC_EOI_REG	EOI Register	02A2 103Ch
40h	CPSW_ECC_SEC_STATUS_REG0	Interrupt Status Register 0	02A2 1040h
80h	CPSW_ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A2 1080h
C0h	CPSW_ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A2 10C0h
13Ch	CPSW_ECC_DED_EOI_REG	EOI Register	02A2 113Ch
140h	CPSW_ECC_DED_STATUS_REG0	Interrupt Status Register 0	02A2 1140h
180h	CPSW_ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A2 1180h
1C0h	CPSW_ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A2 11C0h
200h	CPSW_ECC_AGGR_ENABLE_SET	AGGR interrupt enable set Register	02A2 1200h
204h	CPSW_ECC_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	02A2 1204h
208h	CPSW_ECC_AGGR_STATUS_SET	AGGR interrupt status set Register	02A2 1208h
20Ch	CPSW_ECC_AGGR_STATUS_CLR	AGGR interrupt status clear Register	02A2 120Ch

(1) y = 0 to 7

8.5.1 CPSW_ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

CPSW_ECC_REV is shown in [Figure 8-191](#) and described in [Table 8-399](#).

Return to [Summary Table](#).

Revision parameters.

Table 8-398. CPSW_ECC_REV Instances

Instance	Physical Address
CPSW0_ECC	02A2 1000h

Figure 8-191. CPSW_ECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 8-399. CPSW_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

8.5.2 CPSW_ECC_VECTOR Register (Offset = 8h) [reset = X]

CPSW_ECC_VECTOR is shown in [Figure 8-192](#) and described in [Table 8-401](#).

Return to [Summary Table](#).

ECC Vector Register.

Table 8-400. CPSW_ECC_VECTOR Instances

Instance	Physical Address
CPSW0_ECC	02A2 1008h

Figure 8-192. CPSW_ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-401. CPSW_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address.
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS.
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status.

8.5.3 CPSW_ECC_STAT Register (Offset = Ch) [reset = X]

CPSW_ECC_STAT is shown in [Figure 8-193](#) and described in [Table 8-403](#).

Return to [Summary Table](#).

Misc Status.

Table 8-402. CPSW_ECC_STAT Instances

Instance	Physical Address
CPSW0_ECC	02A2 100Ch

Figure 8-193. CPSW_ECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RESERVED																					NUM_RAMs															
R-X																					R-14h															

LEGEND: R = Read Only; -n = value after reset

Table 8-403. CPSW_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	14h	Indicates the number of RAMs serviced by the ECC aggregator.

8.5.4 CPSW_ECC_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

CPSW_ECC_RESERVED_SVBUS_y is shown in [Figure 8-194](#) and described in [Table 8-405](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 8-404. CPSW_ECC_RESERVED_SVBUS_y
Instances**

Instance	Physical Address
CPSW0_ECC	02A2 1010h + formula

Figure 8-194. CPSW_ECC_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-405. CPSW_ECC_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data.

8.5.5 CPSW_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

CPSW_ECC_SEC_EOI_REG is shown in [Figure 8-195](#) and described in [Table 8-407](#).

Return to [Summary Table](#).

EOI Register.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 8-406. CPSW_ECC_SEC_EOI_REG Instances

Instance	Physical Address
CPSW0_ECC	02A2 103Ch

Figure 8-195. CPSW_ECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-407. CPSW_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register.

8.5.6 CPSW_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

CPSW_ECC_SEC_STATUS_REG0 is shown in [Figure 8-196](#) and described in [Table 8-409](#).

Return to [Summary Table](#).

Interrupt Status Register 0.

**Table 8-408. CPSW_ECC_SEC_STATUS_REG0
Instances**

Instance	Physical Address
CPSW0_ECC	02A2 1040h

Figure 8-196. CPSW_ECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_P END	RAMECC18_P END	RAMECC17_P END	RAMECC16_P END
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RAMECC15_P END	RAMECC14_P END	RAMECC13_P END	RAMECC12_P END	RAMECC11_P END	RAMECC10_P END	RAMECC9_P END	RAMECC8_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RAMECC7_P END	RAMECC6_P END	RAMECC5_P END	RAMECC4_P END	RAMECC3_P END	RAMECC2_P END	RAMECC1_P END	RAMECC0_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-409. CPSW_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_PEND	R/W1S	0h	Interrupt Pending Status for ramecc19_pend.
18	RAMECC18_PEND	R/W1S	0h	Interrupt Pending Status for ramecc18_pend.
17	RAMECC17_PEND	R/W1S	0h	Interrupt Pending Status for ramecc17_pend.
16	RAMECC16_PEND	R/W1S	0h	Interrupt Pending Status for ramecc16_pend.
15	RAMECC15_PEND	R/W1S	0h	Interrupt Pending Status for ramecc15_pend.
14	RAMECC14_PEND	R/W1S	0h	Interrupt Pending Status for ramecc14_pend.
13	RAMECC13_PEND	R/W1S	0h	Interrupt Pending Status for ramecc13_pend.
12	RAMECC12_PEND	R/W1S	0h	Interrupt Pending Status for ramecc12_pend.
11	RAMECC11_PEND	R/W1S	0h	Interrupt Pending Status for ramecc11_pend.
10	RAMECC10_PEND	R/W1S	0h	Interrupt Pending Status for ramecc10_pend.
9	RAMECC9_PEND	R/W1S	0h	Interrupt Pending Status for ramecc9_pend.
8	RAMECC8_PEND	R/W1S	0h	Interrupt Pending Status for ramecc8_pend.
7	RAMECC7_PEND	R/W1S	0h	Interrupt Pending Status for ramecc7_pend.
6	RAMECC6_PEND	R/W1S	0h	Interrupt Pending Status for ramecc6_pend.
5	RAMECC5_PEND	R/W1S	0h	Interrupt Pending Status for ramecc5_pend.

Table 8-409. CPSW_ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RAMECC4_PEND	R/W1S	0h	Interrupt Pending Status for ramecc4_pend.
3	RAMECC3_PEND	R/W1S	0h	Interrupt Pending Status for ramecc3_pend.
2	RAMECC2_PEND	R/W1S	0h	Interrupt Pending Status for ramecc2_pend.
1	RAMECC1_PEND	R/W1S	0h	Interrupt Pending Status for ramecc1_pend.
0	RAMECC0_PEND	R/W1S	0h	Interrupt Pending Status for ramecc0_pend.

8.5.7 CPSW_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

CPSW_ECC_SEC_ENABLE_SET_REG0 is shown in [Figure 8-197](#) and described in [Table 8-411](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0.

**Table 8-410. CPSW_ECC_SEC_ENABLE_SET_REG0
Instances**

Instance	Physical Address
CPSW0_ECC	02A2 1080h

Figure 8-197. CPSW_ECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_E NABLE_SET	RAMECC18_E NABLE_SET	RAMECC17_E NABLE_SET	RAMECC16_E NABLE_SET
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RAMECC15_E NABLE_SET	RAMECC14_E NABLE_SET	RAMECC13_E NABLE_SET	RAMECC12_E NABLE_SET	RAMECC11_E NABLE_SET	RAMECC10_E NABLE_SET	RAMECC9_EN ABLE_SET	RAMECC8_EN ABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RAMECC7_EN ABLE_SET	RAMECC6_EN ABLE_SET	RAMECC5_EN ABLE_SET	RAMECC4_EN ABLE_SET	RAMECC3_EN ABLE_SET	RAMECC2_EN ABLE_SET	RAMECC1_EN ABLE_SET	RAMECC0_EN ABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-411. CPSW_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc19_pend.
18	RAMECC18_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc18_pend.
17	RAMECC17_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc17_pend.
16	RAMECC16_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc16_pend.
15	RAMECC15_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc15_pend.
14	RAMECC14_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc14_pend.
13	RAMECC13_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc13_pend.
12	RAMECC12_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc12_pend.
11	RAMECC11_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc11_pend.
10	RAMECC10_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for ramecc10_pend.
9	RAMECC9_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc9_pend.

Table 8-411. CPSW_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RAMECC8_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc8_pend.
7	RAMECC7_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc7_pend.
6	RAMECC6_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc6_pend.
5	RAMECC5_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc5_pend.
4	RAMECC4_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc4_pend.
3	RAMECC3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc3_pend.
2	RAMECC2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc2_pend.
1	RAMECC1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc1_pend.
0	RAMECC0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc0_pend.

8.5.8 CPSW_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

CPSW_ECC_SEC_ENABLE_CLR_REG0 is shown in [Figure 8-198](#) and described in [Table 8-413](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0.

**Table 8-412. CPSW_ECC_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
CPSW0_ECC	02A2 10C0h

Figure 8-198. CPSW_ECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_E NABLE_CLR	RAMECC18_E NABLE_CLR	RAMECC17_E NABLE_CLR	RAMECC16_E NABLE_CLR
R/W-X				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RAMECC15_E NABLE_CLR	RAMECC14_E NABLE_CLR	RAMECC13_E NABLE_CLR	RAMECC12_E NABLE_CLR	RAMECC11_E NABLE_CLR	RAMECC10_E NABLE_CLR	RAMECC9_EN ABLE_CLR	RAMECC8_EN ABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RAMECC7_EN ABLE_CLR	RAMECC6_EN ABLE_CLR	RAMECC5_EN ABLE_CLR	RAMECC4_EN ABLE_CLR	RAMECC3_EN ABLE_CLR	RAMECC2_EN ABLE_CLR	RAMECC1_EN ABLE_CLR	RAMECC0_EN ABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-413. CPSW_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc19_pend.
18	RAMECC18_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc18_pend.
17	RAMECC17_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc17_pend.
16	RAMECC16_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc16_pend.
15	RAMECC15_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc15_pend.
14	RAMECC14_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc14_pend.
13	RAMECC13_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc13_pend.
12	RAMECC12_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc12_pend.
11	RAMECC11_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc11_pend.
10	RAMECC10_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc10_pend.

Table 8-413. CPSW_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc9_pend.
8	RAMECC8_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc8_pend.
7	RAMECC7_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc7_pend.
6	RAMECC6_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc6_pend.
5	RAMECC5_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc5_pend.
4	RAMECC4_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc4_pend.
3	RAMECC3_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc3_pend.
2	RAMECC2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc2_pend.
1	RAMECC1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc1_pend.
0	RAMECC0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc0_pend.

8.5.9 CPSW_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

CPSW_ECC_DED_EOI_REG is shown in [Figure 8-199](#) and described in [Table 8-415](#).

Return to [Summary Table](#).

EOI Register.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 8-414. CPSW_ECC_DED_EOI_REG Instances

Instance	Physical Address
CPSW0_ECC	02A2 113Ch

Figure 8-199. CPSW_ECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-415. CPSW_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register.

8.5.10 CPSW_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

CPSW_ECC_DED_STATUS_REG0 is shown in [Figure 8-200](#) and described in [Table 8-417](#).

Return to [Summary Table](#).

Interrupt Status Register 0.

**Table 8-416. CPSW_ECC_DED_STATUS_REG0
Instances**

Instance	Physical Address
CPSW0_ECC	02A2 1140h

Figure 8-200. CPSW_ECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_P END	RAMECC18_P END	RAMECC17_P END	RAMECC16_P END
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RAMECC15_P END	RAMECC14_P END	RAMECC13_P END	RAMECC12_P END	RAMECC11_P END	RAMECC10_P END	RAMECC9_P END	RAMECC8_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RAMECC7_P END	RAMECC6_P END	RAMECC5_P END	RAMECC4_P END	RAMECC3_P END	RAMECC2_P END	RAMECC1_P END	RAMECC0_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-417. CPSW_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_PEND	R/W1S	0h	Interrupt Pending Status for ramecc19_pend.
18	RAMECC18_PEND	R/W1S	0h	Interrupt Pending Status for ramecc18_pend.
17	RAMECC17_PEND	R/W1S	0h	Interrupt Pending Status for ramecc17_pend.
16	RAMECC16_PEND	R/W1S	0h	Interrupt Pending Status for ramecc16_pend.
15	RAMECC15_PEND	R/W1S	0h	Interrupt Pending Status for ramecc15_pend.
14	RAMECC14_PEND	R/W1S	0h	Interrupt Pending Status for ramecc14_pend.
13	RAMECC13_PEND	R/W1S	0h	Interrupt Pending Status for ramecc13_pend.
12	RAMECC12_PEND	R/W1S	0h	Interrupt Pending Status for ramecc12_pend.
11	RAMECC11_PEND	R/W1S	0h	Interrupt Pending Status for ramecc11_pend.
10	RAMECC10_PEND	R/W1S	0h	Interrupt Pending Status for ramecc10_pend.
9	RAMECC9_PEND	R/W1S	0h	Interrupt Pending Status for ramecc9_pend.
8	RAMECC8_PEND	R/W1S	0h	Interrupt Pending Status for ramecc8_pend.
7	RAMECC7_PEND	R/W1S	0h	Interrupt Pending Status for ramecc7_pend.
6	RAMECC6_PEND	R/W1S	0h	Interrupt Pending Status for ramecc6_pend.
5	RAMECC5_PEND	R/W1S	0h	Interrupt Pending Status for ramecc5_pend.

Table 8-417. CPSW_ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RAMECC4_PEND	R/W1S	0h	Interrupt Pending Status for ramecc4_pend.
3	RAMECC3_PEND	R/W1S	0h	Interrupt Pending Status for ramecc3_pend.
2	RAMECC2_PEND	R/W1S	0h	Interrupt Pending Status for ramecc2_pend.
1	RAMECC1_PEND	R/W1S	0h	Interrupt Pending Status for ramecc1_pend.
0	RAMECC0_PEND	R/W1S	0h	Interrupt Pending Status for ramecc0_pend.

8.5.11 CPSW_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

CPSW_ECC_DED_ENABLE_SET_REG0 is shown in [Figure 8-201](#) and described in [Table 8-419](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0.

Table 8-418. CPSW_ECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
CPSW0_ECC	02A2 1180h

Figure 8-201. CPSW_ECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-419. CPSW_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc19_pend.
18	RAMECC18_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc18_pend.
17	RAMECC17_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc17_pend.
16	RAMECC16_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc16_pend.
15	RAMECC15_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc15_pend.
14	RAMECC14_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc14_pend.
13	RAMECC13_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc13_pend.
12	RAMECC12_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc12_pend.
11	RAMECC11_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc11_pend.
10	RAMECC10_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc10_pend.
9	RAMECC9_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc9_pend.

Table 8-419. CPSW_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RAMECC8_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc8_pend.
7	RAMECC7_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc7_pend.
6	RAMECC6_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc6_pend.
5	RAMECC5_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc5_pend.
4	RAMECC4_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc4_pend.
3	RAMECC3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc3_pend.
2	RAMECC2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc2_pend.
1	RAMECC1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc1_pend.
0	RAMECC0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc0_pend.

8.5.12 CPSW_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

CPSW_ECC_DED_ENABLE_CLR_REG0 is shown in [Figure 8-202](#) and described in [Table 8-421](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0.

Table 8-420. CPSW_ECC_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
CPSW0_ECC	02A2 11C0h

Figure 8-202. CPSW_ECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
R/W-X				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-421. CPSW_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19	RAMECC19_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc19_pend.
18	RAMECC18_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc18_pend.
17	RAMECC17_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc17_pend.
16	RAMECC16_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc16_pend.
15	RAMECC15_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc15_pend.
14	RAMECC14_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc14_pend.
13	RAMECC13_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc13_pend.
12	RAMECC12_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc12_pend.
11	RAMECC11_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc11_pend.
10	RAMECC10_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc10_pend.

Table 8-421. CPSW_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc9_pend.
8	RAMECC8_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc8_pend.
7	RAMECC7_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc7_pend.
6	RAMECC6_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc6_pend.
5	RAMECC5_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc5_pend.
4	RAMECC4_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc4_pend.
3	RAMECC3_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc3_pend.
2	RAMECC2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc2_pend.
1	RAMECC1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc1_pend.
0	RAMECC0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc0_pend.

8.5.13 CPSW_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

CPSW_ECC_AGGR_ENABLE_SET is shown in [Figure 8-203](#) and described in [Table 8-423](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register.

Table 8-422. CPSW_ECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
CPSW0_ECC	02A2 1200h

Figure 8-203. CPSW_ECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-423. CPSW_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	Interrupt enable set for SVBUS timeout errors.
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors.

8.5.14 CPSW_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

CPSW_ECC_AGGR_ENABLE_CLR is shown in [Figure 8-204](#) and described in [Table 8-425](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register.

**Table 8-424. CPSW_ECC_AGGR_ENABLE_CLR
Instances**

Instance	Physical Address
CPSW0_ECC	02A2 1204h

Figure 8-204. CPSW_ECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-425. CPSW_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for SVBUS timeout errors.
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors.

8.5.15 CPSW_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

CPSW_ECC_AGGR_STATUS_SET is shown in [Figure 8-205](#) and described in [Table 8-427](#).

Return to [Summary Table](#).

AGGR interrupt status set Register.

Table 8-426. CPSW_ECC_AGGR_STATUS_SET Instances

Instance	Physical Address
CPSW0_ECC	02A2 1208h

Figure 8-205. CPSW_ECC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 8-427. CPSW_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for SVBUS timeout errors.
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors.

8.5.16 CPSW_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

CPSW_ECC_AGGR_STATUS_CLR is shown in [Figure 8-206](#) and described in [Table 8-429](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register.

**Table 8-428. CPSW_ECC_AGGR_STATUS_CLR
Instances**

Instance	Physical Address
CPSW0_ECC	02A2 120Ch

Figure 8-206. CPSW_ECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 8-429. CPSW_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for SVBUS timeout errors.
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors.

8.6 CPSW0_MDIO Registers

Table 8-431 lists the memory-mapped registers for the CPSW0_MDIO. All register offset addresses not listed in Table 8-431 should be considered as reserved locations and the register contents should not be modified.

Table 8-430. CPSW0_MDIO Instances

Instance	Base Address
CPSW0_NUSS_MDIO	0C00 0000h

Table 8-431. CPSW0_MDIO Registers

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_MDIO Physical Address
F00h	CPSW_MDIO_VERSION_REG	MDIO Version Register	0C00 0F00h
F04h	CPSW_MDIO_CONTROL_REG	MDIO Control Register	0C00 0F04h
F08h	CPSW_MDIO_ALIVE_REG	MDIO Alive Register	0C00 0F08h
F0Ch	CPSW_MDIO_LINK_REG	MDIO Link Register	0C00 0F0Ch
F10h	CPSW_MDIO_LINK_INT_RAW_REG	MDIO Link Interrupt Raw Register	0C00 0F10h
F14h	CPSW_MDIO_LINK_INT_MASKED_REG	MDIO Link Interrupt Masked Register	0C00 0F14h
F18h	CPSW_MDIO_LINK_INT_MASK_SET_REG	MDIO Link Interrupt Mask Set Register	0C00 0F18h
F1Ch	CPSW_MDIO_LINK_INT_MASK_CLEAR_REG	MDIO Link Interrupt Mask Clear Register	0C00 0F1Ch
F20h	CPSW_MDIO_USER_INT_RAW_REG	MDIO User Interrupt Raw Register	0C00 0F20h
F24h	CPSW_MDIO_USER_INT_MASKED_REG	MDIO User Interrupt Masked Register	0C00 0F24h
F28h	CPSW_MDIO_USER_INT_MASK_SET_REG	MDIO User Interrupt Mask Set Register	0C00 0F28h
F2Ch	CPSW_MDIO_USER_INT_MASK_CLEAR_REG	MDIO User Interrupt Mask Clear Register	0C00 0F2Ch
F30h	CPSW_MDIO_MANUAL_IF_REG	MDIO Manual Interface Register	0C00 0F30h
F34h	CPSW_MDIO_POLL_REG	MDIO Poll Interrupt Register	0C00 0F34h
F38h	CPSW_MDIO_POLL_EN_REG	MDIO Poll Enable Register	0C00 0F38h
F3Ch	CPSW_MDIO_CLAUS45_REG	Clause 45 Enable Register	0C00 0F3Ch
F40h	CPSW_MDIO_USER_ADDR0_REG	MDIO User Address 0 Register	0C00 0F40h
F44h	CPSW_MDIO_USER_ADDR1_REG	MDIO User Address 1 Register	0C00 0F44h
F80h + formula	CPSW_MDIO_USER_ACCESS_REG_k	MDIO User Access k Register	0C00 0F80h + formula
F84h + formula	CPSW_MDIO_USER_PHY_SEL_REG_k	MDIO User PHY Select k Register	0C00 0F84h + formula

(1) k = 0 to 1

8.6.1 CPSW_MDIO_VERSION_REG Register (Offset = F00h) [reset = 00070907h]

CPSW_MDIO_VERSION_REG is shown in [Figure 8-207](#) and described in [Table 8-433](#).

Return to [Summary Table](#).

MDIO Version Register.

Table 8-432. CPSW_MDIO_VERSION_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F00h

Figure 8-207. CPSW_MDIO_VERSION_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-0h		R-0h		R-7h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1h					R-1h			R-0h		R-7h					

LEGEND: R = Read Only; -n = value after reset

Table 8-433. CPSW_MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	0h	Scheme
29-28	BU	R	0h	bu
27-16	MODULE_ID	R	7h	Module ID
15-11	REVRTL	R	1h	RTL version
10-8	REVMAJ	R	1h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	7h	Minor version

8.6.2 CPSW_MDIO_CONTROL_REG Register (Offset = F04h) [reset = X]

CPSW_MDIO_CONTROL_REG is shown in [Figure 8-208](#) and described in [Table 8-435](#).

Return to [Summary Table](#).

MDIO Control Register

**Table 8-434. CPSW_MDIO_CONTROL_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F04h

Figure 8-208. CPSW_MDIO_CONTROL_REG Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R-1h	R/W-0h	R/W-X	R-1h				
23	22	21	20	19	18	17	16
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
R/W-X			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X
15	14	13	12	11	10	9	8
CLKDIV							
R/W-FFh							
7	6	5	4	3	2	1	0
CLKDIV							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-435. CPSW_MDIO_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1h when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1h to this bit enables the MDIO state machine, writing a 0h disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	R/W	X	
28-24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest user access channel that is available in the module and is currently set to 1h. This implies that MDIOUserAccess1 is the highest available user access channel.
23-21	RESERVED	R/W	X	
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1h to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.

Table 8-435. CPSW_MDIO_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	FAULT	R/W	0h	Fault indicator. This bit is set to 1h if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1h to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1h to enable the physical layer fault detection.
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1h to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	R/W	X	
15-0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. MDCLK is disabled when clkdiv is set to 0h. $\text{MDCLK frequency} = \text{clk frequency} / (\text{clkdiv} + 1)$.

8.6.3 CPSW_MDIO_ALIVE_REG Register (Offset = F08h) [reset = 0h]

CPSW_MDIO_ALIVE_REG is shown in [Figure 8-209](#) and described in [Table 8-437](#).

Return to [Summary Table](#).

MDIO Alive Register.

Table 8-436. CPSW_MDIO_ALIVE_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F08h

Figure 8-209. CPSW_MDIO_ALIVE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIVE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-437. CPSW_MDIO_ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ALIVE	R/W	0h	<p>MDIO Alive.</p> <p>Each of the 32-bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address.</p> <p>Writing a 1h to any bit will clear it, writing a 0h has no effect.</p>

8.6.4 CPSW_MDIO_LINK_REG Register (Offset = F0Ch) [reset = 0h]

CPSW_MDIO_LINK_REG is shown in [Figure 8-210](#) and described in [Table 8-439](#).

Return to [Summary Table](#).

MDIO Link Register.

Table 8-438. CPSW_MDIO_LINK_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F0Ch

Figure 8-210. CPSW_MDIO_LINK_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 8-439. CPSW_MDIO_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LINK	R	0h	<p>MDIO Link state.</p> <p>This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to 0h if the PHY indicates it does not have link or fails to acknowledge the read transaction.</p> <p>Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIOUserPhySel registers can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIOUserPhySel register. In State Change Mode the MLINK input pins are unused.</p>

8.6.5 CPSW_MDIO_LINK_INT_RAW_REG Register (Offset = F10h) [reset = X]

CPSW_MDIO_LINK_INT_RAW_REG is shown in [Figure 8-211](#) and described in [Table 8-441](#).

Return to [Summary Table](#).

MDIO Link Interrupt Raw Register.

Table 8-440. CPSW_MDIO_LINK_INT_RAW_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F10h

Figure 8-211. CPSW_MDIO_LINK_INT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-441. CPSW_MDIO_LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	LINKINTRAW	R/W	0h	<p>MDIO link change event raw value.</p> <p>Normal mode operation:</p> <p>When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register. [0]LINKINTRAW and [1]LINKINTRAW correspond to MDIOUserPhySel0 and MDIOUserPhySel1, respectively. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set LINKINTRAW bits to a 1h which may be used for test purposes.</p> <p>MDIO link change event raw value. State Change Mode operation:</p> <p>The [0]LINKINTRAW bit will be asserted '1' when any bit (for any PHY) in the MDIOAlive or MDIOLink registers changes due to MDIO operations. The [1]LINKINTRAW bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the [0]LINKINTRAW bit to a 1h which may be used for test purposes.</p>

8.6.6 CPSW_MDIO_LINK_INT_MASKED_REG Register (Offset = F14h) [reset = X]

CPSW_MDIO_LINK_INT_MASKED_REG is shown in [Figure 8-212](#) and described in [Table 8-443](#).

Return to [Summary Table](#).

MDIO Link Interrupt Masked Register.

Table 8-442. CPSW_MDIO_LINK_INT_MASKED_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F14h

Figure 8-212. CPSW_MDIO_LINK_INT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-443. CPSW_MDIO_LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	LINKINTMASKED	R/W	0h	MDIO link change interrupt masked value. Normal mode operation: When asserted '1', a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding CPSW_MDIO_USER_PHY_SEL_REG_k[6] LINKINT_ENABLE bit was set. CPSW_MDIO_LINK_INT_MASKED_REG[0] LINKINTMASKED and [1] LINKINTMASKED correspond to MDIOUserPhySel0 and MDIOUserPhySel1, respectively. Writing a 1h will clear the interrupt and writing 0h has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values. MDIO link change interrupt masked value. State Change Mode operation: The [0] LINKINTMASKED bit will be asserted '1' when CPSW_MDIO_LINK_INT_RAW_REG[0] LINKINTRAW is asserted '1' and when the CPSW_MDIO_LINK_INT_MASK_SET_REG[0] LINKINTMASKSET bit is set to 1h. Writing a 1h will clear [0] LINKINTMASKED (and the MDIO_LINKINT[0] output) and writing 0h has no effect. The [1] LINKINTMASKED bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode).

8.6.7 CPSW_MDIO_LINK_INT_MASK_SET_REG Register (Offset = F18h) [reset = X]

CPSW_MDIO_LINK_INT_MASK_SET_REG is shown in [Figure 8-213](#) and described in [Table 8-445](#).

Return to [Summary Table](#).

MDIO Link Interrupt Mask Set Register.

Table 8-444.
CPSW_MDIO_LINK_INT_MASK_SET_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F18h

Figure 8-213. CPSW_MDIO_LINK_INT_MASK_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK SET
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-445. CPSW_MDIO_LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINKINTMASKSET	R/W	0h	MDIO link interrupt mask set. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask set. State Change Mode Operation: Writing this bit to 1h will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when [0] LINKINTRAW is asserted.

8.6.8 CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register (Offset = F1Ch) [reset = X]

CPSW_MDIO_LINK_INT_MASK_CLEAR_REG is shown in [Figure 8-214](#) and described in [Table 8-447](#).

Return to [Summary Table](#).

MDIO Link Interrupt Mask Clear Register.

Table 8-446.
CPSW_MDIO_LINK_INT_MASK_CLEAR_REG
Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F1Ch

Figure 8-214. CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							LINKINTMASK CLR
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-447. CPSW_MDIO_LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINKINTMASKCLR	R/W	0h	MDIO link interrupt mask clear. Normal Mode Operation: This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register. MDIO link interrupt mask clear. State Change Mode Operation: Writing this bit to 1h will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the [0] LINKINTRAW bit value.

8.6.9 CPSW_MDIO_USER_INT_RAW_REG Register (Offset = F20h) [reset = X]

CPSW_MDIO_USER_INT_RAW_REG is shown in [Figure 8-215](#) and described in [Table 8-449](#).

Return to [Summary Table](#).

MDIO User Interrupt Raw Register.

Table 8-448. CPSW_MDIO_USER_INT_RAW_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F20h

Figure 8-215. CPSW_MDIO_USER_INT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-449. CPSW_MDIO_USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTRAW	R/W	0h	Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1h will clear the event and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the userintraw bits to a 1h. This mode may be used for test purposes.

8.6.10 CPSW_MDIO_USER_INT_MASKED_REG Register (Offset = F24h) [reset = X]

CPSW_MDIO_USER_INT_MASKED_REG is shown in [Figure 8-216](#) and described in [Table 8-451](#).

Return to [Summary Table](#).

MDIO User Interrupt Masked Register.

Table 8-450.
CPSW_MDIO_USER_INT_MASKED_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F24h

Figure 8-216. CPSW_MDIO_USER_INT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-451. CPSW_MDIO_USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKED	R/W	0h	Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted '1', a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1h. Writing a 1h will clear the interrupt and writing 0h has no effect. If the [17] INT_TEST_ENABLE bit in the CPSW_MDIO_CONTROL_REG register is set, the host may set the CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED bits to a 1h. This mode may be used for test purposes.

8.6.11 CPSW_MDIO_USER_INT_MASK_SET_REG Register (Offset = F28h) [reset = X]

CPSW_MDIO_USER_INT_MASK_SET_REG is shown in [Figure 8-217](#) and described in [Table 8-453](#).

Return to [Summary Table](#).

MDIO User Interrupt Mask Set Register.

Table 8-452.
CPSW_MDIO_USER_INT_MASK_SET_REG
Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F28h

Figure 8-217. CPSW_MDIO_USER_INT_MASK_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKSET	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-453. CPSW_MDIO_USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKSET	R/W	0h	MDIO user interrupt mask set for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0h. Writing a 0h to this register has no effect.

8.6.12 CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register (Offset = F2Ch) [reset = X]

CPSW_MDIO_USER_INT_MASK_CLEAR_REG is shown in [Figure 8-218](#) and described in [Table 8-455](#).

Return to [Summary Table](#).

MDIO User Interrupt Mask Clear Register

Table 8-454.
CPSW_MDIO_USER_INT_MASK_CLEAR_REG
Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F2Ch

Figure 8-218. CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKCLR	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-455. CPSW_MDIO_USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	USERINTMASKCLR	R/W	0h	MDIO user command complete interrupt mask clear for CPSW_MDIO_USER_INT_MASKED_REG[1-0] USERINTMASKED, respectively. Writing a bit to 1h will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0h to this register has no effect.

8.6.13 CPSW_MDIO_MANUAL_IF_REG Register (Offset = F30h) [reset = X]

CPSW_MDIO_MANUAL_IF_REG is shown in [Figure 8-219](#) and described in [Table 8-457](#).

Return to [Summary Table](#).

MDIO Manual Interface Register.

Table 8-456. CPSW_MDIO_MANUAL_IF_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F30h

Figure 8-219. CPSW_MDIO_MANUAL_IF_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
R/W-X					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-457. CPSW_MDIO_MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output. This value is the MDCLK_O output value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
1	MDIO_OE	R/W	0h	MDIO Output Enable. This value is inverted and output on the MDIO_OE_N output when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register.
0	MDIO_PIN	R/W	0h	MDIO Pin Value. This is the external MDIO data pin value when the [31] MANUALMODE bit is set in the CPSW_MDIO_POLL_REG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted '1'. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted '1' and MDIO_PIN is written with a 1h then MDIO_PIN should read a 1h if there are no external devices pulling the MDIO data line low.

8.6.14 CPSW_MDIO_POLL_REG Register (Offset = F34h) [reset = X]

CPSW_MDIO_POLL_REG is shown in [Figure 8-220](#) and described in [Table 8-459](#).

Return to [Summary Table](#).

MDIO Poll Register.

Table 8-458. CPSW_MDIO_POLL_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F34h

Figure 8-220. CPSW_MDIO_POLL_REG Register

31	30	29	28	27	26	25	24
MANUALMODE	STATECHANG EMODE	RESERVED					
R/W-0h	R/W-0h	R/W-X					
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
IPG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-459. CPSW_MDIO_POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	MDIO Manual Mode. When set 1h, the MDIO pins are directly controlled by software through the bits in the CPSW_MDIO_MANUAL_IF_REG register
30	STATECHANGEMODE	R/W	0h	MDIO State Change Mode. When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations.
29-8	RESERVED	R/W	X	
7-0	IPG	R/W	0h	Polling Inter Packet Gap Value. This value is the number of MDCLK_O clocks between each poll when polling is enabled.

8.6.15 CPSW_MDIO_POLL_EN_REG Register (Offset = F38h) [reset = FFFFFFFFh]

CPSW_MDIO_POLL_EN_REG is shown in [Figure 8-221](#) and described in [Table 8-461](#).

Return to [Summary Table](#).

MDIO Poll Enable Register.

Table 8-460. CPSW_MDIO_POLL_EN_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F38h

Figure 8-221. CPSW_MDIO_POLL_EN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLL_EN																															
R/W-FFFFFFFh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-461. CPSW_MDIO_POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	POLL_EN	R/W	FFFFFFFh	<p>MDIO Poll Enable.</p> <p>When set, the bit indicates that the associated PHY will be included in polling operations.</p> <p>When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set (regardless of the value of the preamble disable bit ([20] PREAMBLE) in the CPSW_MDIO_CONTROL_REG register. However, there does not have to be a PHY at address 31.</p>

8.6.16 CPSW_MDIO_CLAUS45_REG Register (Offset = F3Ch) [reset = 0h]

CPSW_MDIO_CLAUS45_REG is shown in [Figure 8-222](#) and described in [Table 8-463](#).

Return to [Summary Table](#).

MDIO Clause45 Enable Register.

Table 8-462. CPSW_MDIO_CLAUS45_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F3Ch

Figure 8-222. CPSW_MDIO_CLAUS45_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAUSE45																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-463. CPSW_MDIO_CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CLAUSE45	R/W	0h	MDIO clause 45 mode. When a clause45 bit is cleared 0h, the PHY associated with the clause45 bit is operating in the clause 22 mode. When set 1h, the PHY associated with the clause45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on.

8.6.17 CPSW_MDIO_USER_ADDR0_REG Register (Offset = F40h) [reset = X]

CPSW_MDIO_USER_ADDR0_REG is shown in [Figure 8-223](#) and described in [Table 8-465](#).

Return to [Summary Table](#).

MDIO Address 0 Register.

Table 8-464. CPSW_MDIO_USER_ADDR0_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F40h

Figure 8-223. CPSW_MDIO_USER_ADDR0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																USER_ADDR0															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-465. CPSW_MDIO_USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	USER_ADDR0	R/W	0h	MDIO User Address 0. In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIOUserAccess0 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess0 access.

8.6.18 CPSW_MDIO_USER_ADDR1_REG Register (Offset = F44h) [reset = X]

CPSW_MDIO_USER_ADDR1_REG is shown in [Figure 8-224](#) and described in [Table 8-467](#).

Return to [Summary Table](#).

MDIO Address 1 Register.

Table 8-466. CPSW_MDIO_USER_ADDR1_REG Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F44h

Figure 8-224. CPSW_MDIO_USER_ADDR1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																USER_ADDR1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-467. CPSW_MDIO_USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	USER_ADDR1	R/W	0h	MDIO User Address 1. In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIOUserAccess1 access. This is not used for PHY's operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess1 access.

8.6.19 CPSW_MDIO_USER_ACCESS_REG_k Register (Offset = F80h + formula) [reset = X]

CPSW_MDIO_USER_ACCESS_REG_k is shown in [Figure 8-225](#) and described in [Table 8-469](#).

Return to [Summary Table](#).

MDIO User Access Register.

Offset = F80h + (k * 8h); where k = 0h to 1h

Table 8-468. CPSW_MDIO_USER_ACCESS_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F80h + formula

Figure 8-225. CPSW_MDIO_USER_ACCESS_REG_k Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W-0h	R/W-0h	R/W-0h	R/W-X			R/W-0h	
23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
DATA							
R/W-0h							
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-469. CPSW_MDIO_USER_ACCESS_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go. Writing a 1h to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0h to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1h. If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1h causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28-26	RESERVED	R/W	X	
25-21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.
20-16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.

Table 8-469. CPSW_MDIO_USER_ACCESS_REG_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

8.6.20 CPSW_MDIO_USER_PHY_SEL_REG_k Register (Offset = F84h + formula) [reset = X]

CPSW_MDIO_USER_PHY_SEL_REG_k is shown in [Figure 8-226](#) and described in [Table 8-471](#).

Return to [Summary Table](#).

MDIO User PHY Select Register

Offset = F84h + (k * 8h); where k = 0h to 1h

Table 8-470. CPSW_MDIO_USER_PHY_SEL_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_MDIO	0C00 0F84h + formula

Figure 8-226. CPSW_MDIO_USER_PHY_SEL_REG_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W-0h	R/W-0h	R/W-X	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-471. CPSW_MDIO_USER_PHY_SEL_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7	LINKSEL	R/W	0h	Link status determination select. Set to 1h to determine link status using the MLINK pin. Default value is 0h which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1h to enable link change status interrupts for PHY address specified in [4-0] PHYADR_MON. Link change interrupts are disabled if this bit is set to 0h.
5	RESERVED	R/W	X	
4-0	PHYADR_MON	R/W	0h	PHY address whose link status is monitored.

8.7 CPSW0_NUSS Subsystem (SS) Registers

Table 8-473 lists the memory-mapped registers for the CPSW0_NUSS SS registers. All register offset addresses not listed in Table 8-473 should be considered as reserved locations and the register contents should not be modified.

Table 8-472. CPSW0_NUSS SS Instances

Instance	Base Address
CPSW0_NUSS_SS	0C00 0000h

Table 8-473. CPSW0_NUSS SS Registers

Offset	Acronym	Register Name	CPSW0_NUSS_SS Physical Address
0h	CPSW_SS_CPSW_NUSS_IDVER_REG	ID Version Register	0C00 0000h
4h	CPSW_SS_SYNCE_COUNT_REG	SyncE Count Register	0C00 0004h
8h	CPSW_SS_SYNCE_MUX_REG	SyncE Mux Select Register	0C00 0008h
Ch	CPSW_SS_CONTROL_REG	Subsystem Control Register	0C00 000Ch
10h	CPSW_SS_SGMII_NON_FIBER_MODE_REG	SGMII NON FIBER Mode Register	0C00 0010h
14h	CPSW_SS_SERDES_RESET_ISO_REG	SyncE Mux Register	0C00 0014h
1Ch	CPSW_SS_SUBSYSTEM_STATUS_REG	Subsystem Status Register	0C00 001Ch
30h	CPSW_SS_RGMII1_STATUS_REG	RGMII Port 1 Status Register	0C00 0030h
34h	CPSW_SS_RGMII2_STATUS_REG	RGMII Port 2 Status Register	0C00 0034h
38h	CPSW_SS_RGMII3_STATUS_REG	RGMII Port 3 Status Register	0C00 0038h
3Ch	CPSW_SS_RGMII4_STATUS_REG	RGMII Port 4 Status Register	0C00 003Ch
40h	CPSW_SS_RGMII5_STATUS_REG	RGMII Port 5 Status Register	0C00 0040h
44h	CPSW_SS_RGMII6_STATUS_REG	RGMII Port 6 Status Register	0C00 0044h
48h	CPSW_SS_RGMII7_STATUS_REG	RGMII Port 7 Status Register	0C00 0048h
4Ch	CPSW_SS_RGMII8_STATUS_REG	RGMII Port 8 Status Register	0C00 004Ch
60h	CPSW_SS_QSGMII_CONTROL_REG	QSGMII Control Register	0C00 0060h
64h	CPSW_SS_QSGMII_STATUS_REG	QSGMII Status Register	0C00 0064h
74h	CPSW_SS_STATUS_XGMII_LINK_REG	XGMII Link Status Register	0C00 0074h
78h	CPSW_SS_STATUS_SGMII_LINK_REG	SGMII Link Status Register	0C00 0078h

8.7.1 CPSW_SS_CPSW_NUSS_IDVER_REG Register (Offset = 0h) [reset = 6BA01101h]

CPSW_SS_CPSW_NUSS_IDVER_REG is shown in [Figure 8-227](#) and described in [Table 8-475](#).

Return to [Summary Table](#).

ID Version Register.

Table 8-474. CPSW_SS_CPSW_NUSS_IDVER_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0000h

Figure 8-227. CPSW_SS_CPSW_NUSS_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDENT															
R-6BA0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER					MINOR_VER					
R-2h					R-1h					R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 8-475. CPSW_SS_CPSW_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	IDENT	R	6BA0h	Identification value
15-11	RTL_VER	R	2h	RTL version value
10-8	MAJOR_VER	R	1h	Major version value
7-0	MINOR_VER	R	1h	Minor version value

8.7.2 CPSW_SS_SYNCE_COUNT_REG Register (Offset = 4h) [reset = 0h]

CPSW_SS_SYNCE_COUNT_REG is shown in [Figure 8-228](#) and described in [Table 8-477](#).

Return to [Summary Table](#).

SyncE Count Register

**Table 8-476. CPSW_SS_SYNCE_COUNT_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0004h

Figure 8-228. CPSW_SS_SYNCE_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNCE_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-477. CPSW_SS_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNCE_CNT	R/W	0h	Sync E Count Value

8.7.3 CPSW_SS_SYNCE_MUX_REG Register (Offset = 8h) [reset = X]

CPSW_SS_SYNCE_MUX_REG is shown in [Figure 8-229](#) and described in [Table 8-479](#).

Return to [Summary Table](#).

SyncE Mux Register

**Table 8-478. CPSW_SS_SYNCE_MUX_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0008h

Figure 8-229. CPSW_SS_SYNCE_MUX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SYNCE_SEL					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-479. CPSW_SS_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	SYNCE_SEL	R/W	0h	Sync E Select Value

8.7.4 CPSW_SS_CONTROL_REG Register (Offset = Ch) [reset = X]

CPSW_SS_CONTROL_REG is shown in [Figure 8-230](#) and described in [Table 8-481](#).

Return to [Summary Table](#).

Control Register

Table 8-480. CPSW_SS_CONTROL_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 000Ch

Figure 8-230. CPSW_SS_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						EEE_PHY_ONL Y	EEE_EN
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-481. CPSW_SS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	EEE_PHY_ONLY	R/W	0h	Energy Efficient Enable Phy Only Mode: 0h =The low power indicate state includes gating off the CPPI_GCLK to the CPSW. 1h =The low power indicate state does not gate the clock to the CPSW.
0	EEE_EN	R/W	0h	Energy Efficient Ethernet Enable: 0h =EEE is disabled 1h =EEE is enabled

8.7.5 CPSW_SS_SGMII_NON_FIBER_MODE_REG Register (Offset = 10h) [reset = X]

CPSW_SS_SGMII_NON_FIBER_MODE_REG is shown in [Figure 8-231](#) and described in [Table 8-483](#).

Return to [Summary Table](#).

SGMII NON FIBER Mode Register

Table 8-482.
CPSW_SS_SGMII_NON_FIBER_MODE_REG
Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0010h

Figure 8-231. CPSW_SS_SGMII_NON_FIBER_MODE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SGMII_NON_FIBER_MODE							
R/W-X								R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-483. CPSW_SS_SGMII_NON_FIBER_MODE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	SGMII_NON_FIBER_MODE	R/W	FFh	This register bit goes to the CPSGMII mode input only.

8.7.6 CPSW_SS_SERDES_RESET_ISO_REG Register (Offset = 14h) [reset = X]

CPSW_SS_SERDES_RESET_ISO_REG is shown in [Figure 8-232](#) and described in [Table 8-485](#).

Return to [Summary Table](#).

SyncE Mux Register.

**Table 8-484. CPSW_SS_SERDES_RESET_ISO_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0014h

Figure 8-232. CPSW_SS_SERDES_RESET_ISO_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SERDES_RESET_ISO							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-485. CPSW_SS_SERDES_RESET_ISO_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	SERDES_RESET_ISO	R/W	0h	These bits control whether the SERDES ignores the hard reset for isolation or not.

8.7.7 CPSW_SS_SUBSYSTEM_STATUS_REG Register (Offset = 1Ch) [reset = X]

CPSW_SS_SUBSYSTEM_STATUS_REG is shown in [Figure 8-233](#) and described in [Table 8-487](#).

Return to [Summary Table](#).

Subsystem Status Register.

Table 8-486.
CPSW_SS_SUBSYSTEM_STATUS_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 001Ch

Figure 8-233. CPSW_SS_SUBSYSTEM_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							EEE_CLKSTOP_ACK
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-487. CPSW_SS_SUBSYSTEM_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	EEE_CLKSTOP_ACK	R	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW.

8.7.8 CPSW_SS_RGMII1_STATUS_REG Register (Offset = 30h) [reset = X]

CPSW_SS_RGMII1_STATUS_REG is shown in [Figure 8-234](#) and described in [Table 8-489](#).

Return to [Summary Table](#).

RGMII Port 1 Status Register.

**Table 8-488. CPSW_SS_RGMII1_STATUS_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0030h

Figure 8-234. CPSW_SS_RGMII1_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-489. CPSW_SS_RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	RGMII Port 1 full duplex: 0h = Half-duplex 1h = Full-duplex
2-1	SPEED	R	0h	RGMII Port 1 speed: 0h = 10Mbps 1h = 100Mbps 2h = 1000Mbps 3h = Reserved
0	LINK	R	0h	RGMII Port 1 link indicator: 0h = Link is down, 1h = Link is up

8.7.9 CPSW_SS_RGMII2_STATUS_REG Register (Offset = 34h) [reset = X]

CPSW_SS_RGMII2_STATUS_REG is shown in [Figure 8-235](#) and described in [Table 8-491](#).

Return to [Summary Table](#).

RGMII Port 2 Status Register.

Table 8-490. CPSW_SS_RGMII2_STATUS_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0034h

Figure 8-235. CPSW_SS_RGMII2_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-491. CPSW_SS_RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	RGMII Port 2 full duplex: 0h = Half-duplex 1h = Full-duplex
2-1	SPEED	R	0h	RGMII Port 2 speed: 0h = 10Mbps 1h = 100Mbps 2h = 1000Mbps 3h = Reserved
0	LINK	R	0h	RGMII Port 2 link indicator: 0h = Link is down 1h = Link is up

8.7.10 CPSW_SS_RGMII3_STATUS_REG Register (Offset = 38h) [reset = X]

CPSW_SS_RGMII3_STATUS_REG is shown in [Figure 8-236](#) and described in [Table 8-493](#).

Return to [Summary Table](#).

RGMII 3 Port Status Register.

**Table 8-492. CPSW_SS_RGMII3_STATUS_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0038h

Figure 8-236. CPSW_SS_RGMII3_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-493. CPSW_SS_RGMII3_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	RGMII Port 3 full duplex: 0h = Half-duplex 1h = Full-duplex
2-1	SPEED	R	0h	RGMII Port 3 speed: 0h = 10Mbps 1h = 100Mbps 2h = 1000Mbps 3h = Reserved
0	LINK	R	0h	RGMII Port 3 link indicator: 0h = Link is down 1h = Link is up

8.7.11 CPSW_SS_RGMII4_STATUS_REG Register (Offset = 3Ch) [reset = X]

CPSW_SS_RGMII4_STATUS_REG is shown in [Figure 8-237](#) and described in [Table 8-495](#).

Return to [Summary Table](#).

RGMII Port 4 Status Register.

Table 8-494. CPSW_SS_RGMII4_STATUS_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 003Ch

Figure 8-237. CPSW_SS_RGMII4_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-495. CPSW_SS_RGMII4_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	RGMII Port 4 full duplex: 0h = Half-duplex 1h = Full-duplex
2-1	SPEED	R	0h	RGMII Port 4 speed: 0h = 10Mbps 1h = 100Mbps 2h = 1000Mbps 3h = Reserved
0	LINK	R	0h	RGMII Port 4 link indicator: 0h = Link is down 1h = Link is up

8.7.12 CPSW_SS_RGMII5_STATUS_REG Register (Offset = 40h) [reset = X]

CPSW_SS_RGMII5_STATUS_REG is shown in [Figure 8-238](#) and described in [Table 8-497](#).

Return to [Summary Table](#).

RGMII Port 5 Status Register.

**Table 8-496. CPSW_SS_RGMII5_STATUS_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0040h

Figure 8-238. CPSW_SS_RGMII5_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-497. CPSW_SS_RGMII5_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	RGMII Port 5 full duplex: 0h = Half-duplex 1h = Full-duplex
2-1	SPEED	R	0h	RGMII Port 5 speed: 0h = 10Mbps 1h = 100Mbps 2h = 1000Mbps 3h = Reserved
0	LINK	R	0h	RGMII Port 5 link indicator: 0h = Link is down 1h = Link is up

8.7.13 CPSW_SS_RGMII6_STATUS_REG Register (Offset = 44h) [reset = X]

CPSW_SS_RGMII6_STATUS_REG is shown in [Figure 8-239](#) and described in [Table 8-499](#).

Return to [Summary Table](#).

RGMII Port 6 Status Register.

Table 8-498. CPSW_SS_RGMII6_STATUS_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0044h

Figure 8-239. CPSW_SS_RGMII6_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-499. CPSW_SS_RGMII6_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	RGMII Port 6 full duplex: 0h = Half-duplex 1h = Full-duplex
2-1	SPEED	R	0h	RGMII Port 6 speed: 0h = 10Mbps 1h = 100Mbps 2h = 1000Mbps 3h = Reserved
0	LINK	R	0h	RGMII Port 6 link indicator: 0h = Link is down 1h = Link is up

8.7.14 CPSW_SS_RGMII7_STATUS_REG Register (Offset = 48h) [reset = X]

CPSW_SS_RGMII7_STATUS_REG is shown in [Figure 8-240](#) and described in [Table 8-501](#).

Return to [Summary Table](#).

RGMII Port 7 Status Register.

**Table 8-500. CPSW_SS_RGMII7_STATUS_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0048h

Figure 8-240. CPSW_SS_RGMII7_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-501. CPSW_SS_RGMII7_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	RGMII Port 7 full duplex: 0h = Half-duplex 1h = Full-duplex
2-1	SPEED	R	0h	RGMII Port 7 speed: 0h = 10Mbps 1h = 100Mbps 2h = 1000Mbps 3h = Reserved
0	LINK	R	0h	RGMII Port 7 link indicator: 0h = Link is down 1h = Link is up

8.7.15 CPSW_SS_RGMII8_STATUS_REG Register (Offset = 4Ch) [reset = X]

CPSW_SS_RGMII8_STATUS_REG is shown in [Figure 8-241](#) and described in [Table 8-503](#).

Return to [Summary Table](#).

RGMII Port 8 Status Register.

Table 8-502. CPSW_SS_RGMII8_STATUS_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 004Ch

Figure 8-241. CPSW_SS_RGMII8_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				FULLDUPLEX	SPEED		LINK
R-X				R-0h	R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-503. CPSW_SS_RGMII8_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	FULLDUPLEX	R	0h	RGMII Port 8 full duplex: 0h = Half-duplex 1h = Full-duplex
2-1	SPEED	R	0h	RGMII Port 8 speed: 0h = 10Mbps 1h = 100Mbps 2h = 1000Mbps 3h = Reserved
0	LINK	R	0h	RGMII Port 8 link indicator: 0h = Link is down 1h = Link is up

8.7.16 CPSW_SS_QSGMII_CONTROL_REG Register (Offset = 60h) [reset = X]

CPSW_SS_QSGMII_CONTROL_REG is shown in [Figure 8-242](#) and described in [Table 8-505](#).

Return to [Summary Table](#).

QSGMII Control Register.

**Table 8-504. CPSW_SS_QSGMII_CONTROL_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0060h

Figure 8-242. CPSW_SS_QSGMII_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						Q1_RDCD	Q0_RDCD
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-505. CPSW_SS_QSGMII_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	Q1_RDCD	R/W	0h	QSGMII1 Running Disparity Check Disable.
0	Q0_RDCD	R/W	0h	QSGMII0 Running Disparity Check Disable.

8.7.17 CPSW_SS_QSGMII_STATUS_REG Register (Offset = 64h) [reset = X]

CPSW_SS_QSGMII_STATUS_REG is shown in [Figure 8-243](#) and described in [Table 8-507](#).

Return to [Summary Table](#).

QSGMII Status Register.

Table 8-506. CPSW_SS_QSGMII_STATUS_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0064h

Figure 8-243. CPSW_SS_QSGMII_STATUS_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						Q1_RDCD	Q0_RDCD
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-507. CPSW_SS_QSGMII_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	Q1_RDCD	R	0h	QSGMII1 RX Sync Detected.
0	Q0_RDCD	R	0h	QSGMII0 RX Sync Detected.

8.7.18 CPSW_SS_STATUS_XGMII_LINK_REG Register (Offset = 74h) [reset = X]

CPSW_SS_STATUS_XGMII_LINK_REG is shown in [Figure 8-244](#) and described in [Table 8-509](#).

Return to [Summary Table](#).

XGMII Link Status Register.

**Table 8-508. CPSW_SS_STATUS_XGMII_LINK_REG
Instances**

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0074h

Figure 8-244. CPSW_SS_STATUS_XGMII_LINK_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						XGMII2_LINK	XGMII1_LINK
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-509. CPSW_SS_STATUS_XGMII_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	XGMII2_LINK	R	0h	Port 2 XGMII Link Indicator.
0	XGMII1_LINK	R	0h	Port 1 XGMII Link Indicator.

8.7.19 CPSW_SS_STATUS_SGMII_LINK_REG Register (Offset = 78h) [reset = X]

CPSW_SS_STATUS_SGMII_LINK_REG is shown in [Figure 8-245](#) and described in [Table 8-511](#).

Return to [Summary Table](#).

SGMII Link Status Register.

Table 8-510. CPSW_SS_STATUS_SGMII_LINK_REG Instances

Instance	Physical Address
CPSW0_NUSS_SS	0C00 0078h

Figure 8-245. CPSW_SS_STATUS_SGMII_LINK_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						SGMII2_LINK	SGMII1_LINK
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-511. CPSW_SS_STATUS_SGMII_LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	SGMII2_LINK	R	0h	Port 2 SGMII Link Indicator.
0	SGMII1_LINK	R	0h	Port 1 SGMII Link Indicator.

8.8 CPSW0_PCSR Registers

Table 8-513 lists the memory-mapped registers for the CPSW0_PCSR. All register offset addresses not listed in Table 8-513 should be considered as reserved locations and the register contents should not be modified.

Table 8-512. CPSW0_PCSR Instances

Instance	Base Address
CPSW0_NUSS_PCSR	0C00 0000h

Table 8-513. CPSW0_PCSR Registers

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_PCSR Physical Address
2100h + formula	CPSW_PCSR_TX_CTL_REG_j	PCSR Transmit Control Register	0C00 2100h + formula
2104h + formula	CPSW_PCSR_TX_STATUS_REG_j	PCSR Transmit Status Register	0C00 2104h + formula
2108h + formula	CPSW_PCSR_RX_CTL_REG_j	PCSR Receive Control Register	0C00 2108h + formula
210Ch + formula	CPSW_PCSR_RX_STATUS_REG_j	PCSR Receive Status Register	0C00 210Ch + formula
2110h + formula	CPSW_PCSR_SEED_A_LO_REG_j	PCSR Seed A Low Register	0C00 2110h + formula
2114h + formula	CPSW_PCSR_SEED_A_HI_REG_j	PCSR SEED A High Register	0C00 2114h + formula
2118h + formula	CPSW_PCSR_SEED_B_LO_REG_j	PCSR Seed B Low Register	0C00 2118h + formula
211Ch + formula	CPSW_PCSR_SEED_B_HI_REG_j	PCSR SEED B High Register	0C00 211Ch + formula
2120h + formula	CPSW_PCSR_FEC_REG_j	PCSR FEC Register	0C00 2120h + formula
2124h + formula	CPSW_PCSR_CTL_REG_j	PCSR CTL Register	0C00 2124h + formula
2128h + formula	CPSW_PCSR_FEC_CNT_REG_j	PCSR FEC Count Register	0C00 2128h + formula
212Ch + formula	CPSW_PCSR_ERROR_FIFO_REG_j	PCSR Error FIFO Register	0C00 212Ch + formula

(1) j = 0 to 1

8.8.1 CPSW_PCSR_TX_CTL_REG_j Register (Offset = 2100h + formula) [reset = X]

CPSW_PCSR_TX_CTL_REG_j is shown in [Figure 8-246](#) and described in [Table 8-515](#).

Return to [Summary Table](#).

PCSR Transmit Control Register.

Offset = 2100h + (j * 100h); where j = 0h to 1h.

**Table 8-514. CPSW_PCSR_TX_CTL_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2100h + formula

Figure 8-246. CPSW_PCSR_TX_CTL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							TX_DATAPATH_EN
R/W-X							R/W-1h
7	6	5	4	3	2	1	0
TX_SCR_BPYASS	TX_TEST_EN	TX_TEST_SEL	TX_TEST_DAT_SEL	TX_PRBS31_EN	TX_PRBS9_EN	TX_LOOPBACK_EN	TX_SCR_LOOPBK_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-515. CPSW_PCSR_TX_CTL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	TX_DATAPATH_EN	R/W	1h	PCSR Transmit Datapath Enable.
7	TX_SCR_BPYASS	R/W	0h	PCSR Transmit SCR Bypass.
6	TX_TEST_EN	R/W	0h	PCSR Transmit Test Enable.
5	TX_TEST_SEL	R/W	0h	PCSR Transmit Test Select.
4	TX_TEST_DAT_SEL	R/W	0h	PCSR Transmit Test Data Select.
3	TX_PRBS31_EN	R/W	0h	PCSR Transmit PRBS31 Enable.
2	TX_PRBS9_EN	R/W	0h	PCSR Transmit PRBS9 Enable.
1	TX_LOOPBACK_EN	R/W	0h	PCSR Transmit Loopback Enable.
0	TX_SCR_LOOPBK_EN	R/W	0h	PCSR Transmit SCR Loopback Enable.

Table 8-516. Register Call Summary for CPSW_PCSR_TX_CTL_REG_j

CPSW0_PCSR Registers

- [CPSW_PCSR_TX_CTL_REG_j Register \(Offset = 2100h + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_PCSR Registers: \[0\]](#)

8.8.2 CPSW_PCSR_TX_STATUS_REG_j Register (Offset = 2104h + formula) [reset = X]

CPSW_PCSR_TX_STATUS_REG_j is shown in Figure 8-247 and described in Table 8-518.

Return to [Summary Table](#).

PCSR Transmit Status Register.

Offset = 2104h + (j * 100h); where j = 0h to 1h.

**Table 8-517. CPSW_PCSR_TX_STATUS_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2104h + formula

Figure 8-247. CPSW_PCSR_TX_STATUS_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							TX_FAULT
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-518. CPSW_PCSR_TX_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	TX_FAULT	R/W	0h	PCSR Transmit Fault Hold Register - write 1 to clear.
7-0	RESERVED	R/W	X	

Table 8-519. Register Call Summary for CPSW_PCSR_TX_STATUS_REG_j

CPSW0_PCSR Registers

- [CPSW_PCSR_TX_STATUS_REG_j Register \(Offset = 2104h + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_PCSR Registers: \[0\]](#)

8.8.3 CPSW_PCSR_RX_CTL_REG_j Register (Offset = 2108h + formula) [reset = X]

CPSW_PCSR_RX_CTL_REG_j is shown in Figure 8-248 and described in Table 8-521.

Return to [Summary Table](#).

PCSR Receive Control Register.

Offset = 2108h + (j * 100h); where j = 0h to 1h.

**Table 8-520. CPSW_PCSR_RX_CTL_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2108h + formula

Figure 8-248. CPSW_PCSR_RX_CTL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							RX_PRBS9_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RX_TEST_EN	RX_TEST_DAT_SEL	RX_PRBS31_EN	RX_ERR_BLK_CNT_RST	RX_BER_CNT_RST	RX_TEST_CNT_PRE	RX_TEST_CNT_125US	RX_TPTEP_CNT_RST
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-521. CPSW_PCSR_RX_CTL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	RX_PRBS9_EN	R/W	0h	PCSR Receive PRBS9 Enable.
7	RX_TEST_EN	R/W	0h	PCSR Receive Test Enable.
6	RX_TEST_DAT_SEL	R/W	0h	PCSR Receive Test Data Select.
5	RX_PRBS31_EN	R/W	0h	PCSR Receive PRBS31 Enable.
4	RX_ERR_BLK_CNT_RST	R/W	0h	PCSR Receive Error Block Count Reset.
3	RX_BER_CNT_RST	R/W	0h	PCSR Receive BER Count Reset.
2	RX_TEST_CNT_PRE	R/W	0h	PCSR Receive Test Count Pre.
1	RX_TEST_CNT_125US	R/W	0h	PCSR Receive Test Count 125us.
0	RX_TPTEP_CNT_RST	R/W	0h	PCSR Receive TPTEP Count Reset

Table 8-522. Register Call Summary for CPSW_PCSR_RX_CTL_REG_j

CPSW0_PCSR Registers

- [CPSW_PCSR_RX_CTL_REG_j Register \(Offset = 2108h + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_PCSR Registers: \[0\]](#)

8.8.4 CPSW_PCSR_RX_STATUS_REG_j Register (Offset = 210Ch + formula) [reset = 0h]

CPSW_PCSR_RX_STATUS_REG_j is shown in Figure 8-249 and described in Table 8-524.

Return to [Summary Table](#).

PCSR Receive Status Register.

Offset = 210Ch + (j * 100h); where j = 0h to 1h

**Table 8-523. CPSW_PCSR_RX_STATUS_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 210Ch + formula

Figure 8-249. CPSW_PCSR_RX_STATUS_REG_j Register

31	30	29	28	27	26	25	24
RX_HI_BER	RX_BLOCK_LOCK	RX_BER_COUNT					
R-0h	R-0h	R-0h					
23	22	21	20	19	18	17	16
RX_ERR_BLK_CNT							
R-0h							
15	14	13	12	11	10	9	8
RX_TPT_ERR_CNT							
R-0h							
7	6	5	4	3	2	1	0
RX_TPT_ERR_CNT							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 8-524. CPSW_PCSR_RX_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_HI_BER	R	0h	PCSR Receive High BER.
30	RX_BLOCK_LOCK	R	0h	PCSR Receive Block Lock.
29-24	RX_BER_COUNT	R	0h	PCSR Receive BER Count.
23-16	RX_ERR_BLK_CNT	R	0h	PCSR Error Block Count.
15-0	RX_TPT_ERR_CNT	R	0h	PCSR TPT Error Count.

Table 8-525. Register Call Summary for CPSW_PCSR_RX_STATUS_REG_j

CPSW0_PCSR Registers

- [CPSW0_PCSR Registers: \[0\]](#)
- [CPSW_PCSR_RX_STATUS_REG_j Register \(Offset = 210Ch + formula\) \[reset = 0h\]: \[0\]](#)

8.8.5 CPSW_PCSR_SEED_A_LO_REG_J Register (Offset = 2110h + formula) [reset = 0h]

CPSW_PCSR_SEED_A_LO_REG_J is shown in [Figure 8-250](#) and described in [Table 8-527](#).

Return to [Summary Table](#).

PCSR Seed A Low Register.

Offset = 2110h + (j * 100h); where j = 0h to 1h

**Table 8-526. CPSW_PCSR_SEED_A_LO_REG_J
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2110h + formula

Figure 8-250. CPSW_PCSR_SEED_A_LO_REG_J Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEED_A_LO																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-527. CPSW_PCSR_SEED_A_LO_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SEED_A_LO	R/W	0h	PCSR Seed A Low.

Table 8-528. Register Call Summary for CPSW_PCSR_SEED_A_LO_REG_J

CPSW0_PCSR Registers

- [CPSW0_PCSR Registers: \[0\]](#)
- [CPSW_PCSR_SEED_A_LO_REG_J Register \(Offset = 2110h + formula\) \[reset = 0h\]: \[0\]](#)

8.8.6 CPSW_PCSR_SEED_A_HI_REG_j Register (Offset = 2114h + formula) [reset = X]

CPSW_PCSR_SEED_A_HI_REG_j is shown in [Figure 8-251](#) and described in [Table 8-530](#).

Return to [Summary Table](#).

PCSR Seed A High Register.

Offset = 2114h + (j * 100h); where j = 0h to 1h

**Table 8-529. CPSW_PCSR_SEED_A_HI_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2114h + formula

Figure 8-251. CPSW_PCSR_SEED_A_HI_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SEED_A_HI																									
R/W-X						R/W-0h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-530. CPSW_PCSR_SEED_A_HI_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-0	SEED_A_HI	R/W	0h	PCSR Seed A High.

Table 8-531. Register Call Summary for CPSW_PCSR_SEED_A_HI_REG_j

CPSW0_PCSR Registers

- [CPSW_PCSR_SEED_A_HI_REG_j Register \(Offset = 2114h + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_PCSR Registers: \[0\]](#)

8.8.7 CPSW_PCSR_SEED_B_LO_REG_J Register (Offset = 2118h + formula) [reset = 0h]

CPSW_PCSR_SEED_B_LO_REG_J is shown in [Figure 8-252](#) and described in [Table 8-533](#).

Return to [Summary Table](#).

PCSR Seed B Low Register.

Offset = 2118h + (j * 100h); where j = 0h to 1h.

**Table 8-532. CPSW_PCSR_SEED_B_LO_REG_J
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2118h + formula

Figure 8-252. CPSW_PCSR_SEED_B_LO_REG_J Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEED_B_LO																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-533. CPSW_PCSR_SEED_B_LO_REG_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SEED_B_LO	R/W	0h	PCSR Seed B Low.

Table 8-534. Register Call Summary for CPSW_PCSR_SEED_B_LO_REG_J

CPSW0_PCSR Registers

- [CPSW0_PCSR Registers: \[0\]](#)
- [CPSW_PCSR_SEED_B_LO_REG_J Register \(Offset = 2118h + formula\) \[reset = 0h\]: \[0\]](#)

8.8.8 CPSW_PCSR_SEED_B_HI_REG_j Register (Offset = 211Ch + formula) [reset = X]

CPSW_PCSR_SEED_B_HI_REG_j is shown in [Figure 8-253](#) and described in [Table 8-536](#).

Return to [Summary Table](#).

PCSR Seed B High Register.

Offset = 211Ch + (j * 100h); where j = 0h to 1h.

**Table 8-535. CPSW_PCSR_SEED_B_HI_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 211Ch + formula

Figure 8-253. CPSW_PCSR_SEED_B_HI_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SEED_B_HI																									
R/W-X						R/W-0h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-536. CPSW_PCSR_SEED_B_HI_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-0	SEED_B_HI	R/W	0h	PCSR Seed B High.

Table 8-537. Register Call Summary for CPSW_PCSR_SEED_B_HI_REG_j

CPSW0_PCSR Registers

- [CPSW_PCSR_SEED_B_HI_REG_j Register \(Offset = 211Ch + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_PCSR Registers: \[0\]](#)

8.8.9 CPSW_PCSR_FEC_REG_j Register (Offset = 2120h + formula) [reset = X]

CPSW_PCSR_FEC_REG_j is shown in Figure 8-254 and described in Table 8-539.

Return to [Summary Table](#).

PCSR FEC Register.

Offset = 2120h + (j * 100h); where j = 0h to 1h.

Table 8-538. CPSW_PCSR_FEC_REG_j Instances

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2120h + formula

Figure 8-254. CPSW_PCSR_FEC_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						FEC_ENA_ER R_IND	FEC_ENABLE
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-539. CPSW_PCSR_FEC_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	FEC_ENA_ERR_IND	R/W	0h	PCSR FEC ENA Error Ind.
0	FEC_ENABLE	R/W	0h	PCSR FEC Enable.

Table 8-540. Register Call Summary for CPSW_PCSR_FEC_REG_j

CPSW0_PCSR Registers

- [CPSW0_PCSR Registers: \[0\]](#)
- [CPSW_PCSR_FEC_REG_j Register \(Offset = 2120h + formula\) \[reset = X\]: \[0\]](#)

8.8.10 CPSW_PCSR_CTL_REG_j Register (Offset = 2124h + formula) [reset = X]

CPSW_PCSR_CTL_REG_j is shown in [Figure 8-255](#) and described in [Table 8-542](#).

Return to [Summary Table](#).

PCSR Control Register.

Offset = 2124h + (j * 100h); where j = 0h to 1h.

Table 8-541. CPSW_PCSR_CTL_REG_j Instances

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2124h + formula

Figure 8-255. CPSW_PCSR_CTL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						SIGNAL_OK_EN	SIGNAL_OK
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-542. CPSW_PCSR_CTL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	SIGNAL_OK_EN	R/W	0h	PCSR Signal OK Enable.
0	SIGNAL_OK	R/W	0h	PCSR Signal OK.

Table 8-543. Register Call Summary for CPSW_PCSR_CTL_REG_j

CPSW0_PCSR Registers

- [CPSW_PCSR_CTL_REG_j Register \(Offset = 2124h + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_PCSR Registers: \[0\]](#)

8.8.11 CPSW_PCSR_FEC_CNT_REG_j Register (Offset = 2128h + formula) [reset = 0h]

CPSW_PCSR_FEC_CNT_REG_j is shown in [Figure 8-256](#) and described in [Table 8-545](#).

Return to [Summary Table](#).

PCSR FEC Count Register.

Offset = 2128h + (j * 100h); where j = 0h to 1h.

**Table 8-544. CPSW_PCSR_FEC_CNT_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 2128h + formula

Figure 8-256. CPSW_PCSR_FEC_CNT_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEC_CORR_CNT																FEC_UNCORRCNT															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-545. CPSW_PCSR_FEC_CNT_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FEC_CORR_CNT	R/W	0h	PCSR FEC Corrected Error Count.
15-0	FEC_UNCORRCNT	R/W	0h	PCSR FEC Uncorrected Error Count.

Table 8-546. Register Call Summary for CPSW_PCSR_FEC_CNT_REG_j

CPSW0_PCSR Registers

- [CPSW0_PCSR Registers](#): [0]
- [CPSW_PCSR_FEC_CNT_REG_j Register \(Offset = 2128h + formula\) \[reset = 0h\]](#): [0]

8.8.12 CPSW_PCSR_ERROR_FIFO_REG_j Register (Offset = 212Ch + formula) [reset = X]

CPSW_PCSR_ERROR_FIFO_REG_j is shown in Figure 8-257 and described in Table 8-548.

Return to [Summary Table](#).

PCSR Error FIFO Register.

Offset = 212Ch + (j * 100h); where j = 0h to 1h.

**Table 8-547. CPSW_PCSR_ERROR_FIFO_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_PCSR	0C00 212Ch + formula

Figure 8-257. CPSW_PCSR_ERROR_FIFO_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ERROR_FIFO_CTC
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-548. CPSW_PCSR_ERROR_FIFO_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ERROR_FIFO_CTC	R/W	0h	PCSR Error FIFO CTC.

Table 8-549. Register Call Summary for CPSW_PCSR_ERROR_FIFO_REG_j

CPSW0_PCSR Registers

- [CPSW_PCSR_ERROR_FIFO_REG_j Register \(Offset = 212Ch + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_PCSR Registers: \[0\]](#)

8.9 CPSW0_RAM Registers

[Table 8-551](#) lists the memory-mapped registers for the CPSW0_RAM. All register offset addresses not listed in [Table 8-551](#) should be considered as reserved locations and the register contents should not be modified.

Table 8-550. CPSW0_RAM Instances

Instance	Base Address
CPSW0_NUSS_RAM	0C00 0000h

Table 8-551. CPSW0_RAM Registers

Offset	Acronym	Register Name	CPSW0_NUSS_RAM Physical Address
00032000h + formula	CPSW_FETCH_LOC_y	RAM Location Register	0C03 2000h + formula

8.9.1 CPSW_FETCH_LOC_y Register (Offset = 00032000h + formula) [reset = X]

CPSW_FETCH_LOC_y is shown in [Figure 8-258](#) and described in [Table 8-553](#).

Return to [Summary Table](#).

These are the RAM locations for one Ethernet port.

Offset = 00032000h + (y * 4h); where y = 0h to 3FFh

Table 8-552. CPSW_FETCH_LOC_y Instances

Instance	Physical Address
CPSW0_NUSS_RAM	0C03 2000h + formula

Figure 8-258. CPSW_FETCH_LOC_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											LOC																				
R/W-X											R/W-0h																				

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-553. CPSW_FETCH_LOC_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-0	LOC	R/W	0h	RAM Location.

Table 8-554. Register Call Summary for CPSW_FETCH_LOC_y

CPSW0_RAM Registers

- [CPSW_FETCH_LOC_y Register \(Offset = 00032000h + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_RAM Registers: \[0\]](#)

8.10 CPSW0_SGMII Registers

Table 8-556 lists the memory-mapped registers for the CPSW0_SGMII. All register offset addresses not listed in Table 8-556 should be considered as reserved locations and the register contents should not be modified.

Table 8-555. CPSW0_SGMII Instances

Instance	Base Address
CPSW0_NUSS_SGMII	0C00 0000h

Table 8-556. CPSW0_SGMII Registers

Offset	Acronym	Register Name	CPSW0_NUSS_SGMII Physical Address
100h + formula (1)	CPSW_SGMII_IDVER_REG_j	Identification and Version Register	0C00 0100h + formula
104h + formula	CPSW_SGMII_SOFT_RESET_REG_j	SGMII Software Reset Register	0C00 0104h + formula
110h + formula	CPSW_SGMII_CONTROL_REG_j	SGMII Control Register	0C00 0110h + formula
114h + formula	CPSW_SGMII_STATUS_REG_j	SGMII Status Register	0C00 0114h + formula
118h + formula	CPSW_SGMII_MR_ADV_ABILITY_REG_j	Advertised Ability Register	0C00 0118h + formula
11Ch + formula	CPSW_SGMII_MR_NP_TX_REG_j	Next Page Transmit Register	0C00 011Ch + formula
120h + formula	CPSW_SGMII_MR_LP_ADV_ABILITY_REG_j	Link Partner Advertised Ability Register	0C00 0120h + formula
124h + formula	CPSW_SGMII_MR_LP_NP_RX_REG_j	Link Partner Next Page Received Register	0C00 0124h + formula
130h + formula	CPSW_SGMII_TX_CFG_REG_j	SGMII Transmit Config Register	0C00 0130h + formula
134h + formula	CPSW_SGMII_RX_CFG_REG_j	SGMII Receive Config Register	0C00 0134h + formula
138h + formula	CPSW_SGMII_AUX_CFG_REG_j	SGMII Auxiliary Configuration Register	0C00 0138h + formula
140h + formula	CPSW_SGMII_DIAG_CLEAR_REG_j	Diagnostics Clear Register	0C00 0140h + formula
144h + formula	CPSW_SGMII_DIAG_CONTROL_REG_j	Diagnostics Control Register	0C00 0144h + formula
148h + formula	CPSW_SGMII_DIAG_STATUS_REG_j	Diagnostics Status Register	0C00 0148h + formula

(1) j = 0 to 7

8.10.1 CPSW_SGMII_IDVER_REG_j Register (Offset = 100h + formula) [reset = 4EC21102h]

CPSW_SGMII_IDVER_REG_j is shown in [Figure 8-259](#) and described in [Table 8-558](#).

Return to [Summary Table](#).

SGMII IDVER register.

Offset = 100h + (j * 100h); where j = 0h to 7h.

Table 8-557. CPSW_SGMII_IDVER_REG_j Instances

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0100h + formula

Figure 8-259. CPSW_SGMII_IDVER_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R-4EC2h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER					MINOR_VER					
R-2h					R-1h					R-2h					

LEGEND: R = Read Only; -n = value after reset

Table 8-558. CPSW_SGMII_IDVER_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_IDENT	R	4EC2h	MODULE value
15-11	RTL_VER	R	2h	RTL version value
10-8	MAJOR_VER	R	1h	Major version value
7-0	MINOR_VER	R	2h	Minor version value

Table 8-559. Register Call Summary for CPSW_SGMII_IDVER_REG_j

CPSW0_SGMII Registers

- [CPSW0_SGMII Registers: \[0\]](#)
- [CPSW_SGMII_IDVER_REG_j Register \(Offset = 100h + formula\) \[reset = 4EC21102h\]: \[0\]](#)

8.10.2 CPSW_SGMII_SOFT_RESET_REG_j Register (Offset = 104h + formula) [reset = X]

CPSW_SGMII_SOFT_RESET_REG_j is shown in [Figure 8-260](#) and described in [Table 8-561](#).

Return to [Summary Table](#).

SGMII Soft Reset Register.

Offset = 104h + (j * 100h); where j = 0h to 7h.

**Table 8-560. CPSW_SGMII_SOFT_RESET_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0104h + formula

Figure 8-260. CPSW_SGMII_SOFT_RESET_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RT_SOFT_RESET	SOFT_RESET
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-561. CPSW_SGMII_SOFT_RESET_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	RT_SOFT_RESET	R/W	0h	Transmit and Receive Software Reset. Write 0h = The reset condition is removed. Write 1h = Causes the SGMII transmit and receive logic to be in the reset condition (the VBUSP_CLK domain is not reset). This bit is intended to be used when changing between loopback mode and normal mode of operation.
0	SOFT_RESET	R/W	0h	Software Reset. Write 1h = Causes the SGMII logic to be reset. Software reset occurs immediately. This bit reads as a zero.

Table 8-562. Register Call Summary for CPSW_SGMII_SOFT_RESET_REG_j

CPSW0_SGMII Registers

- [CPSW0_SGMII Registers: \[0\]](#)
- [CPSW_SGMII_SOFT_RESET_REG_j Register \(Offset = 104h + formula\) \[reset = X\]: \[0\]](#)

8.10.3 CPSW_SGMII_CONTROL_REG_j Register (Offset = 110h + formula) [reset = X]

CPSW_SGMII_CONTROL_REG_j is shown in Figure 8-261 and described in Table 8-564.

Return to [Summary Table](#).

SGMII Control Register

Offset = 110h + (j * 100h); where j = 0h to 7h.

**Table 8-563. CPSW_SGMII_CONTROL_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0110h + formula

Figure 8-261. CPSW_SGMII_CONTROL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	TEST_PAT T_N_EN	MASTER	LOOPBACK	MR_NP_LOAD ED	FAST_LINK_TI MER	MR_AN_REST ART	MR_AN_ENAB LE
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-564. CPSW_SGMII_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	TEST_PATTERN_EN	R/W	0h	Test Pattern Enable. Force the output of K28.5 on TX_ENC for test purposes. 0h = Operation 1h = Forced K28.5 on transmit output
5	MASTER	R/W	0h	Master Mode. 0h = Slave Mode 1h = Master mode – Set to one for one side of a direct connection. When this bit is set, the control logic uses the CPSW_SGMII_MR_ADV_ABILITY_REG register to determine speed and duplexity instead of the CPSW_SGMII_MR_LP_ADV_ABILITY_REG register. Master mode allows a CPSPGMII direct connection with auto-negotiation or with a forced link.
4	LOOPBACK	R/W	0h	Loopback mode. 0h = Not in internal loopback mode 1h = Internal loopback mode. The transmit clock (TX_CLK) is used for transmit and receive.

Table 8-564. CPSW_SGMII_CONTROL_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MR_NP_LOADED	R/W	0h	Next Page Loaded. Writing 1h to this bit informs the auto-negotiation process that the next page register has been loaded. This bit is cleared by the auto-negotiation state machine before the CPSW_SGMII_STATUS_REG[3] MR_PAGE_RX status bit is set. This bit is not used when the SGMII_MODE input is asserted.
2	FAST_LINK_TIMER	R/W	0h	Fast Link Timer. 0h = The link timer value is 10ms in FIBER mode and 1.6ms in SGMII mode. 1h = The link timer value is 2μs in FIBER and SGMII mode. This is included for test purposes.
1	MR_AN_RESTART	R/W	0h	Auto Negotiation Restart. Writing 1h and then 0h to this bit causes the auto-negotiation process to be restarted.
0	MR_AN_ENABLE	R/W	0h	Auto Negotiation Enable. Writing 1h to this bit enables the auto-negotiation process.

Table 8-565. Register Call Summary for CPSW_SGMII_CONTROL_REG_j

CPSW0_SGMII Registers

- [CPSW0_SGMII Registers: \[0\]](#)
- [CPSW_SGMII_CONTROL_REG_j Register \(Offset = 110h + formula\) \[reset = X\]: \[0\]](#)

8.10.4 CPSW_SGMII_STATUS_REG_j Register (Offset = 114h + formula) [reset = X]

CPSW_SGMII_STATUS_REG_j is shown in Figure 8-262 and described in Table 8-567.

Return to [Summary Table](#).

SGMII Status Register

Offset = 114h + (j * 100h); where j = 0h to 7h.

**Table 8-566. CPSW_SGMII_STATUS_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0114h + formula

Figure 8-262. CPSW_SGMII_STATUS_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED		FIB_SIG_DETE CT	LOCK	MR_PAGE_RX	MR_AN_COMP LETE	AN_ERROR	LINK
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 8-567. CPSW_SGMII_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5	FIB_SIG_DETECT	R	0h	Fiber Signal Detect. This is the FIB_SIG_DETECT input pin.
4	LOCK	R	0h	Lock. This is the LOCK input pin. Indicates that the SERDES PLL is locked.
3	MR_PAGE_RX	R	0h	Next Page Received. This bit is set to one by the auto-negotiation state machine when the next page has been received. This bit is cleared to 0h by a host write of 1h to the [3]MR_NP_LOADED bit in the CPSW_SGMII_CONTROL_REG register. This value is not valid until the lock status bit is ([4] LOCK) asserted.
2	MR_AN_COMPLETE	R	0h	Auto negotiation complete. This value is not valid until the lock status bit is asserted. 0h = Auto-negotiation is not complete 1h = Auto-negotiation is completed.

Table 8-567. CPSW_SGMII_STATUS_REG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AN_ERROR	R	0h	Auto negotiation error. For SGMII mode, an auto-negotiation error occurs when halfduplex Gigabit is commanded. For FIBER mode, an auto-negotiation error occurs if both sides cannot be full duplex. This value is not valid until the lock status bit is asserted. 0h = No auto-negotiation error 1h = Auto-negotiation error
0	LINK	R	0h	Link indicator. This value is not valid until the lock status bit is asserted. 0h = Link is not up. 1h = Link is up.

Table 8-568. Register Call Summary for CPSW_SGMII_STATUS_REG_j

CPSW0_SGMII Registers

- [CPSW0_SGMII Registers: \[0\]](#)
- [CPSW_SGMII_STATUS_REG_j Register \(Offset = 114h + formula\) \[reset = X\]: \[0\]](#)

8.10.5 CPSW_SGMII_MR_ADV_ABILITY_REG_j Register (Offset = 118h + formula) [reset = X]

CPSW_SGMII_MR_ADV_ABILITY_REG_j is shown in [Figure 8-263](#) and described in [Table 8-570](#).

Return to [Summary Table](#).

SGMII MR Advertized Ability Register.

Offset = 118h + (j * 100h); where j = 0h to 7h.

Table 8-569.
CPSW_SGMII_MR_ADV_ABILITY_REG_j Instances

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0118h + formula

Figure 8-263. CPSW_SGMII_MR_ADV_ABILITY_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_ADV_ABILITY															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-570. CPSW_SGMII_MR_ADV_ABILITY_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MR_ADV_ABILITY	R/W	0h	Advertised Ability. When in FIBER mode, this value corresponds to the [16-1] MR_ADV_ABILITY in the IEEE specification and is loaded into the IEEE specification TX_CONFIG_REG[15:0]. When in SGMII mode, this value corresponds to the TX_CONFIG_REG[15:0] register value in the Serial-GMII specification.

Table 8-571. Register Call Summary for CPSW_SGMII_MR_ADV_ABILITY_REG_j

CPSW0_SGMII Registers

- [CPSW0_SGMII Registers: \[0\]](#)
- [CPSW_SGMII_MR_ADV_ABILITY_REG_j Register \(Offset = 118h + formula\) \[reset = X\]: \[0\]](#)

8.10.6 CPSW_SGMII_MR_NP_TX_REG_j Register (Offset = 11Ch + formula) [reset = X]

CPSW_SGMII_MR_NP_TX_REG_j is shown in [Figure 8-264](#) and described in [Table 8-573](#).

Return to [Summary Table](#).

SGMII Next Page Transmit Register.

Offset = 11Ch + (j * 100h); where j = 0h to 7h.

**Table 8-572. CPSW_SGMII_MR_NP_TX_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 011Ch + formula

Figure 8-264. CPSW_SGMII_MR_NP_TX_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_NP_TX															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-573. CPSW_SGMII_MR_NP_TX_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	MR_NP_TX	R/W	0h	Next Page Transmit. This value corresponds to the [16-1]MR_NP_TX value in the IEEE specification. Next page is used only in FIBER mode.

Table 8-574. Register Call Summary for CPSW_SGMII_MR_NP_TX_REG_j

CPSW0_SGMII Registers

- [CPSW_SGMII_MR_NP_TX_REG_j Register \(Offset = 11Ch + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_SGMII Registers: \[0\]](#)

8.10.7 CPSW_SGMII_MR_LP_ADV_ABILITY_REG_j Register (Offset = 120h + formula) [reset = X]

CPSW_SGMII_MR_LP_ADV_ABILITY_REG_j is shown in Figure 8-265 and described in Table 8-576.

Return to [Summary Table](#).

SGMII Link Partner Advertized Ability Register.

Offset = 120h + (j * 100h); where j = 0h to 7h.

Table 8-575.
CPSW_SGMII_MR_LP_ADV_ABILITY_REG_j
Instances

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0120h + formula

Figure 8-265. CPSW_SGMII_MR_LP_ADV_ABILITY_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR_LP_ADV_ABILITY															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 8-576. CPSW_SGMII_MR_LP_ADV_ABILITY_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MR_LP_ADV_ABILITY	R	0h	Link Partner Advertised Ability. Readable when auto-negotiation is complete. When in FIBER mode, this value corresponds to the [16-1] MR_LP_ADV_ABILITY value in the IEEE. When in SGMII mode, this value corresponds to the TX_CONFIG_REG[15-0] register value in the Serial-GMII specification.

Table 8-577. Register Call Summary for CPSW_SGMII_MR_LP_ADV_ABILITY_REG_j

CPSW0_SGMII Registers

- [CPSW_SGMII_MR_LP_ADV_ABILITY_REG_j Register \(Offset = 120h + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_SGMII Registers: \[0\]](#)

8.10.8 CPSW_SGMII_MR_LP_NP_RX_REG_j Register (Offset = 124h + formula) [reset = X]

CPSW_SGMII_MR_LP_NP_RX_REG_j is shown in [Figure 8-266](#) and described in [Table 8-579](#).

Return to [Summary Table](#).

SGMII Link Partner Next Page Receive Register

Offset = 124h + (j * 100h); where j = 0h to 7h.

**Table 8-578. CPSW_SGMII_MR_LP_NP_RX_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0124h + formula

Figure 8-266. CPSW_SGMII_MR_LP_NP_RX_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MR_LP_NP_RX															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 8-579. CPSW_SGMII_MR_LP_NP_RX_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MR_LP_NP_RX	R	0h	Link Partner Next Page Received. Readable when the next page is received. These bits are as defined in the IEEE 802.3 standard. Next page is used only in FIBER mode.

Table 8-580. Register Call Summary for CPSW_SGMII_MR_LP_NP_RX_REG_j

CPSW0_SGMII Registers

- [CPSW_SGMII_MR_LP_NP_RX_REG_j Register \(Offset = 124h + formula\) \[reset = X\]: \[0\]](#)
- [CPSW0_SGMII Registers: \[0\]](#)

8.10.9 CPSW_SGMII_TX_CFG_REG_j Register (Offset = 130h + formula) [reset = 0h]

CPSW_SGMII_TX_CFG_REG_j is shown in [Figure 8-267](#) and described in [Table 8-582](#).

Return to [Summary Table](#).

SGMII Transmit Configuration Register

Offset = 130h + (j * 100h); where j = 0h to 7h.

**Table 8-581. CPSW_SGMII_TX_CFG_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0130h + formula

Figure 8-267. CPSW_SGMII_TX_CFG_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CFG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-582. CPSW_SGMII_TX_CFG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CFG	R/W	0h	Transmit configuration register output

Table 8-583. Register Call Summary for CPSW_SGMII_TX_CFG_REG_j

CPSW0_SGMII Registers

- [CPSW0_SGMII Registers: \[0\]](#)
- [CPSW_SGMII_TX_CFG_REG_j Register \(Offset = 130h + formula\) \[reset = 0h\]: \[0\]](#)

8.10.10 CPSW_SGMII_RX_CFG_REG_j Register (Offset = 134h + formula) [reset = 0h]

CPSW_SGMII_RX_CFG_REG_j is shown in [Figure 8-268](#) and described in [Table 8-585](#).

Return to [Summary Table](#).

SGMII Receive Configuration Register

Offset = 134h + (j * 100h); where j = 0h to 7h.

**Table 8-584. CPSW_SGMII_RX_CFG_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0134h + formula

Figure 8-268. CPSW_SGMII_RX_CFG_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CFG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-585. CPSW_SGMII_RX_CFG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RX_CFG	R/W	0h	Receive configuration register output

Table 8-586. Register Call Summary for CPSW_SGMII_RX_CFG_REG_j

CPSW0_SGMII Registers

- [CPSW_SGMII_RX_CFG_REG_j Register \(Offset = 134h + formula\) \[reset = 0h\]: \[0\]](#)
- [CPSW0_SGMII Registers: \[0\]](#)

8.10.11 CPSW_SGMII_AUX_CFG_REG_j Register (Offset = 138h + formula) [reset = 0h]

CPSW_SGMII_AUX_CFG_REG_j is shown in [Figure 8-269](#) and described in [Table 8-588](#).

Return to [Summary Table](#).

SGMII Auxiliary Configuration Register.

Offset = 138h + (j * 100h); where j = 0h to 7h.

**Table 8-587. CPSW_SGMII_AUX_CFG_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0138h + formula

Figure 8-269. CPSW_SGMII_AUX_CFG_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_CFG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-588. CPSW_SGMII_AUX_CFG_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	AUX_CFG	R/W	0h	Auxiliary configuration register output

Table 8-589. Register Call Summary for CPSW_SGMII_AUX_CFG_REG_j

CPSW0_SGMII Registers

- [CPSW_SGMII_AUX_CFG_REG_j Register \(Offset = 138h + formula\) \[reset = 0h\]: \[0\]](#)
- [CPSW0_SGMII Registers: \[0\]](#)

8.10.12 CPSW_SGMII_DIAG_CLEAR_REG_j Register (Offset = 140h + formula) [reset = X]

CPSW_SGMII_DIAG_CLEAR_REG_j is shown in Figure 8-270 and described in Table 8-591.

Return to [Summary Table](#).

SGMII Diagnostics Clear Register

Offset = 140h + (j * 100h); where j = 0h to 7h

**Table 8-590. CPSW_SGMII_DIAG_CLEAR_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0140h + formula

Figure 8-270. CPSW_SGMII_DIAG_CLEAR_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							DIAG_CLEAR
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-591. CPSW_SGMII_DIAG_CLEAR_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	DIAG_CLEAR	R/W	0h	Diagnostics Clear. Clears all diagnostic status bits when set to one. Some bits may be set back to one immediately following reset. The reset requires several clocks due to synchronizers.

Table 8-592. Register Call Summary for CPSW_SGMII_DIAG_CLEAR_REG_j

CPSW0_SGMII Registers

- [CPSW0_SGMII Registers: \[0\]](#)
- [CPSW_SGMII_DIAG_CLEAR_REG_j Register \(Offset = 140h + formula\) \[reset = X\]: \[0\]](#)

8.10.13 CPSW_SGMII_DIAG_CONTROL_REG_j Register (Offset = 144h + formula) [reset = X]

CPSW_SGMII_DIAG_CONTROL_REG_j is shown in Figure 8-271 and described in Table 8-594.

Return to [Summary Table](#).

SGMII Diagnostics Control Register

Offset = 144h + (j * 100h); where j = 0h to 7h.

**Table 8-593. CPSW_SGMII_DIAG_CONTROL_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0144h + formula

Figure 8-271. CPSW_SGMII_DIAG_CONTROL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DIAG_SM_SEL			RESERVED	DIAG_EDGE_SEL		
R/W-X	R/W-0h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-594. CPSW_SGMII_DIAG_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6-4	DIAG_SM_SEL	R/W	0h	Diagnostic Select. Determines which internal diagnostic bits are muxed onto CPSW_SGMII_DIAG_STATUS_REG[15-0] DIAG_STATUS. 0h = Reserved 1h = Diagnostic Hold Signals 2h = Diagnostic Sync Status (sync_sm state machine) 3h = Diagnostic AN Status (amsm state machine) 4h = Diagnostic TXOS Status (txos state machine) 5h = Diagnostic TXCG Status (txcg state machine) 6h = Diagnostic RXSM Status (rxsm state machine lower bits) 7h = Diagnostic RXSM Status (rxsm state machine upper bits)
3-2	RESERVED	R/W	X	
1-0	DIAG_EDGE_SEL	R/W	0h	Diagnostic Hold Signals Edge Select 0h = Diagnostic Hold Signals Level 1h = Diagnostic Hold Signals rising edge detected 2h = Diagnostic Hold Signals falling edge detected 3h = Diagnostic Hold Signals ether (both) edge detected

Table 8-595. Register Call Summary for CPSW_SGMII_DIAG_CONTROL_REG_j

CPSW0_SGMII Registers

- [CPSW_SGMII_DIAG_CONTROL_REG_j](#) Register (Offset = 144h + formula) [reset = X]: [0]
- [CPSW0_SGMII Registers](#): [0]

8.10.14 CPSW_SGMII_DIAG_STATUS_REG_j Register (Offset = 148h + formula) [reset = X]

CPSW_SGMII_DIAG_STATUS_REG_j is shown in Figure 8-272 and described in Table 8-597.

Return to [Summary Table](#).

SGMII Diagnostics Status Register

Offset = 148h + (j * 100h); where j = 0h to 7h.

**Table 8-596. CPSW_SGMII_DIAG_STATUS_REG_j
Instances**

Instance	Physical Address
CPSW0_NUSS_SGMII	0C00 0148h + formula

Figure 8-272. CPSW_SGMII_DIAG_STATUS_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DIAG_STATUS															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 8-597. CPSW_SGMII_DIAG_STATUS_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	DIAG_STATUS	R	0h	Diagnostics status.

Table 8-598. Register Call Summary for CPSW_SGMII_DIAG_STATUS_REG_j

CPSW0_SGMII Registers

- [CPSW0_SGMII Registers: \[0\]](#)
- [CPSW_SGMII_DIAG_STATUS_REG_j Register \(Offset = 148h + formula\) \[reset = X\]: \[0\]](#)

8.11 CPSW0_STAT Registers

Table 8-600 lists the memory-mapped registers for the CPSW0_STAT. All register offset addresses not listed in Table 8-600 should be considered as reserved locations and the register contents should not be modified.

Table 8-599. CPSW0_STAT Instances

Instance	Base Address
CPSW0_NUSS_STAT	0C00 0000h

Table 8-600. CPSW0_STAT Registers

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_STAT Physical Address
0003A000h + formula	CPSW_STAT_RXGOODFRAMES_k	Ethernet Port N Total Number of Good Frames Received	0C03 A000h + formula
0003A004h + formula	CPSW_STAT_RXBROADCASTFRAMES_k	Ethernet Port N Total Number of Good Broadcast Frames Received	0C03 A004h + formula
0003A008h + formula	CPSW_STAT_RXMULTICASTFRAMES_k	Ethernet Port N Total Number of Good Multicast Frames Received	0C03 A008h + formula
0003A00Ch + formula	CPSW_STAT_RXPAUSEFRAMES_k	Ethernet Port N Total Number of Good Pause Frames Received	0C03 A00Ch + formula
0003A010h + formula	CPSW_STAT_RXCRCERRORS_k	Ethernet Port N Total Number of CRC Errors Frames Received	0C03 A010h + formula
0003A014h + formula	CPSW_STAT_RXALIGNCODEERRORS_k	Ethernet Port N Total Number of Aligned Code Errors Frames Received	0C03 A014h + formula
0003A018h + formula	CPSW_STAT_RXOVERSIZEDFRAMES_k	Ethernet Port N Total Number of Oversized Frames Received	0C03 A018h + formula
0003A01Ch + formula	CPSW_STAT_RXJABBERFRAMES_k	Ethernet Port N Total Number of Jabber Frames Received	0C03 A01Ch + formula
0003A020h + formula	CPSW_STAT_RXUNDERSIZEDFRAMES_k	Ethernet Port N Total Number of Undersized Frames Received	0C03 A020h + formula
0003A024h + formula	CPSW_STAT_RXFRAGMENTS_k	Ethernet Port N Fragments Received Register	0C03 A024h + formula
0003A028h + formula	CPSW_STAT_ALE_DROP_k	Ethernet Port N ALE Drop Register	0C03 A028h + formula
0003A02Ch + formula	CPSW_STAT_ALE_OVERRUN_DROP_k	Ethernet Port N ALE Overrun Drop Register	0C03 A02Ch + formula
0003A030h + formula	CPSW_STAT_RXOCTETS_k	Ethernet Port N Total Number of Received Bytes in Good Frames	0C03 A030h + formula
0003A034h + formula	CPSW_STAT_TXGOODFRAMES_k	Ethernet Port N Good Transmit Frames Register	0C03 A034h + formula
0003A038h + formula	CPSW_STAT_TXBROADCASTFRAMES_k	Ethernet Port N Broadcast Transmit Frames Register	0C03 A038h + formula
0003A03Ch + formula	CPSW_STAT_TXMULTICASTFRAMES_k	Ethernet Port N Multicast Transmit Frames Register	0C03 A03Ch + formula
0003A040h + formula	CPSW_STAT_TXPAUSEFRAMES_k	Ethernet Port N Transmit Pause Frames Register	0C03 A040h + formula
0003A044h + formula	CPSW_STAT_TXDEFERREDFRAMES_k	Ethernet Port N Transmit Deferred Frames Register	0C03 A044h + formula
0003A048h + formula	CPSW_STAT_TXCOLLISIONFRAMES_k	Ethernet Port N Transmit Frames Experiencing a Collision	0C03 A048h + formula
0003A04Ch + formula	CPSW_STAT_TXSINGLECOLLFRAMES_k	Ethernet Port N Transmit Frames Experiencing a Single Collision	0C03 A04Ch + formula
0003A050h + formula	CPSW_STAT_TXMULTICOLLFRAMES_k	Ethernet Port N Transmit Frames Experiencing a Multiple Collision	0C03 A050h + formula
0003A054h + formula	CPSW_STAT_TXEXCESSIVECOLLISIONS_k	Ethernet Port N Transmit Frames Abandoned due to Excessive Collisions	0C03 A054h + formula

Table 8-600. CPSW0_STAT Registers (continued)

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_STAT Physical Address
0003A058h + formula	CPSW_STAT_TXLATECOLLISIONS_k	Ethernet Port N Transmit Frames Abandoned due to a Late Collision	0C03 A058h + formula
0003A05Ch + formula	CPSW_STAT_RXIPGERROR_k	Ethernet Port N Total Number of Inter-Packet Gap Errors Received	0C03 A05Ch + formula
0003A060h + formula	CPSW_STAT_TXCARRIERSENSEERRORS_k	Ethernet Port N Total Number of Transmitted Frames that Experienced a Carrier Loss	0C03 A060h + formula
0003A064h + formula	CPSW_STAT_TXOCTETS_k	Ethernet Port N Tx Octets Register	0C03 A064h + formula
0003A068h + formula	CPSW_STAT_OCTETFRAMES64_k	Ethernet Port N 64 Octet Frames Register	0C03 A068h + formula
0003A06Ch + formula	CPSW_STAT_OCTETFRAMES65T127_k	Ethernet Port N 65 to 127 Octet Frames Register	0C03 A06Ch + formula
0003A070h + formula	CPSW_STAT_OCTETFRAMES128T255_k	Ethernet Port N 128 to 255 Octet Frames Register	0C03 A070h + formula
0003A074h + formula	CPSW_STAT_OCTETFRAMES256T511_k	Ethernet Port N 256 to 511 Octet Frames Register	0C03 A074h + formula
0003A078h + formula	CPSW_STAT_OCTETFRAMES512T1023_k	Ethernet Port N 512-pn_rx_maxlen Octet Frames Register	0C03 A078h + formula
0003A07Ch + formula	CPSW_STAT_OCTETFRAMES1024TUP_k	Ethernet Port N 1023-1518 Octet Frames Register	0C03 A07Ch + formula
0003A080h + formula	CPSW_STAT_NETOCTETS_k	Ethernet Port N Net Octets Register	0C03 A080h + formula
0003A084h + formula	CPSW_STAT_RX_BOTTOM_OF_FIFO_DROP_k	Ethernet Port N Receive Bottom of FIFO Drop Register	0C03 A084h + formula
0003A088h + formula	CPSW_STAT_PORTMASK_DROP_k	Ethernet Port N Portmask Drop Register	0C03 A088h + formula
0003A08Ch + formula	CPSW_STAT_RX_TOP_OF_FIFO_DROP_k	Ethernet Port N Receive Top of FIFO Drop Register	0C03 A08Ch + formula
0003A090h + formula	CPSW_STAT_ALE_RATE_LIMIT_DROP_k	Ethernet Port N ALE Rate Limit Drop Register	0C03 A090h + formula
0003A094h + formula	CPSW_STAT_ALE_VID_INGRESS_DROP_k	Ethernet Port N ALE VID Ingress Drop Register	0C03 A094h + formula
0003A098h + formula	CPSW_STAT_ALE_DA_EQ_SA_DROP_k	Ethernet Port N ALE DA equal SA Drop Register	0C03 A098h + formula
0003A09Ch + formula	CPSW_STAT_ALE_BLOCK_DROP_k	Ethernet Port N ALE Block Drop Register	0C03 A09Ch + formula
0003A0A0h + formula	CPSW_STAT_ALE_SECURE_DROP_k	Ethernet Port N ALE Secure Drop Register	0C03 A0A0h + formula
0003A0A4h + formula	CPSW_STAT_ALE_AUTH_DROP_k	Ethernet Port N ALE Authentication Drop Register	0C03 A0A4h + formula
0003A0A8h + formula	CPSW_STAT_ALE_UNKN_UNI_k	Ethernet Port N ALE Receive Unknown Unicast Register	0C03 A0A8h + formula
0003A0ACh + formula	CPSW_STAT_ALE_UNKN_UNI_BCNT_k	Ethernet Port N ALE Receive Unknown Unicast Bytecount Register	0C03 A0ACh + formula
0003A0B0h + formula	CPSW_STAT_ALE_UNKN_MLT_K	Ethernet Port N ALE Receive Unknown Multicast Register	0C03 A0B0h + formula
0003A0B4h + formula	CPSW_STAT_ALE_UNKN_MLT_BCNT_k	Ethernet Port N ALE Receive Unknown Multicast Bytecount Register	0C03 A0B4h + formula
0003A0B8h + formula	CPSW_STAT_ALE_UNKN_BRD_k	Ethernet Port N ALE Receive Unknown Broadcast Register	0C03 A0B8h + formula
0003A0BCh + formula	CPSW_STAT_ALE_UNKN_BRD_BCNT_k	Ethernet Port N ALE Receive Unknown Broadcast Bytecount Register	0C03 A0BCh + formula

Table 8-600. CPSW0_STAT Registers (continued)

Offset ⁽¹⁾	Acronym	Register Name	CPSW0_NUSS_STAT Physical Address
0003A0C0h + formula	CPSW_STAT_ALE_POL_MATCH_k	Ethernet Port N ALE Policer Matched Register	0C03 A0C0h + formula
0003A0C4h + formula	CPSW_STAT_ALE_POL_MATCH_RED_k	Ethernet Port N ALE Policer Matched and Condition Red Register	0C03 A0C4h + formula
0003A0C8h + formula	CPSW_STAT_ALE_POL_MATCH_YELLOW_k	Ethernet Port N ALE Policer Matched and Condition Yellow Register	0C03 A0C8h + formula
0003A0CCh + formula	CPSW_STAT_ALE_MULT_SA_DROP_k	Enet Port N ALE Multicast Source Address Drop	0C03 A0CCh + formula
0003A0D0h + formula	CPSW_STAT_ALE_DUAL_VLAN_DROP_k	Enet Port N ALE Dual VLAN Drop	0C03 A0D0h + formula
0003A0D4h + formula	CPSW_STAT_ALE_LEN_ERROR_DROP_k	Enet Port N ALE IEEE 802.3 Length Error Drop	0C03 A0D4h + formula
0003A0D8h + formula	CPSW_STAT_ALE_IP_NEXT_HDR_DROP_k	Enet Port N ALE IP Next Header Limit Drop	0C03 A0D8h + formula
0003A0DCh + formula	CPSW_STAT_ALE_IPV4_FRAG_DROP_k	Enet Port N ALE IPv4 Fragment Drop	0C03 A0DCh + formula
0003A140h + formula	CPSW_STAT_IET_RX_ASSEMBLY_ERROR_REG_k	Enet Port N IET Received Assembly Error	0C03 A140h + formula
0003A144h + formula	CPSW_STAT_IET_RX_ASSEMBLY_OK_REG_k	Enet Port N IET Received Assembly OK	0C03 A144h + formula
0003A148h + formula	CPSW_STAT_IET_RX_SMD_ERROR_REG_k	Enet Port N IET Received SMD Error	0C03 A148h + formula
0003A14Ch + formula	CPSW_STAT_IET_RX_FRAG_REG_k	Enet Port N IET Received Fragment (IET fragment)	0C03 A14Ch + formula
0003A150h + formula	CPSW_STAT_IET_TX_HOLD_REG_k	Enet Port N IET Transmit Hold	0C03 A150h + formula
0003A154h + formula	CPSW_STAT_IET_TX_FRAG_REG_k	Enet Port N IET Transmit Fragment (IET fragment)	0C03 A154h + formula
0003A17Ch + formula	CPSW_STAT_TX_MEMORY_PROTECT_ERROR_k	Ethernet Port N Transmit Memory Protect CRC Error Register	0C03 A17Ch + formula
0003A180h + formula	CPSW_STAT_ENET_PN_TX_PRI_REG_k_y	Ethernet Port N Tx Priority 0 to Priority 7 Packet Count Register	0C03 A180h + formula
0003A1A0h + formula	CPSW_STAT_ENET_PN_TX_PRI_BCNT_REG_k_y	Ethernet Port N Tx Priority 0 to Priority 7 Packet Byte Count Register	0C03 A1A0h + formula
0003A1C0h + formula	CPSW_STAT_ENET_PN_TX_PRI_DROP_REG_k_y	Ethernet Port N Tx Priority 0 to Priority 7 Packet Drop Count Register	0C03 A1C0h + formula
0003A1E0h + formula	CPSW_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_k_y	Ethernet Port N Tx Priority 0 to Priority 7 Packet Drop Byte Count Register	0C03 A1E0h + formula

(1) k = 0 to 8

8.11.1 CPSW_STAT_RXGOODFRAMES_k Register (Offset = 0003A000h + formula) [reset = 0h]

CPSW_STAT_RXGOODFRAMES_k is shown in [Figure 8-273](#) and described in [Table 8-602](#).

Return to [Summary Table](#).

The total number of good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Had a length of 64 to SL_RX_MAXLEN[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the RX_ALIGN_CODE_ERRORS and CPSW_STAT0_RXCRCERRORS statistic descriptions for definitions of alignment, code and CRC errors. Overruns have no effect upon this statistic.

Offset = 0003A000h + (k * 200h); where k = 0h to 8h

**Table 8-601. CPSW_STAT_RXGOODFRAMES_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A000h + formula

Figure 8-273. CPSW_STAT_RXGOODFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-602. CPSW_STAT_RXGOODFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good frames received.

8.11.2 CPSW_STAT_RXBROADCASTFRAMES_k Register (Offset = 0003A004h + formula) [reset = 0h]

CPSW_STAT_RXBROADCASTFRAMES_k is shown in [Figure 8-274](#) and described in [Table 8-604](#).

Return to [Summary Table](#).

The total number of good broadcast frames received on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address 0xFFFFFFFF
- Had a length of CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the CPSW_STAT0_RXCRCERRORS statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Offset = 0003A004h + (k * 200h); where k = 0h to 8h

Table 8-603.
CPSW_STAT_RXBROADCASTFRAMES_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A004h + formula

Figure 8-274. CPSW_STAT_RXBROADCASTFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-604. CPSW_STAT_RXBROADCASTFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good broadcast frames received.

8.11.3 CPSW_STAT_RXMULTICASTFRAMES_k Register (Offset = 0003A008h + formula) [reset = 0h]

CPSW_STAT_RXMULTICASTFRAMES_k is shown in [Figure 8-275](#) and described in [Table 8-606](#).

Return to [Summary Table](#).

The total number of good multicast frames received on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than 0xFFFFFFFF
- Had a length of CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error.

See the CPSW_STAT0_RXCRCERRORS statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Offset = 0003A008h + (k * 200h); where k = 0h to 8h

**Table 8-605. CPSW_STAT_RXMULTICASTFRAMES_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A008h + formula

Figure 8-275. CPSW_STAT_RXMULTICASTFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-606. CPSW_STAT_RXMULTICASTFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good multicast frames received.

8.11.4 CPSW_STAT_RXPAUSEFRAMES_k Register (Offset = 0003A00Ch + formula) [reset = 0h]

CPSW_STAT_RXPAUSEFRAMES_k is shown in [Figure 8-276](#) and described in [Table 8-608](#).

Return to [Summary Table](#).

Total number of pause frames received

Offset = 0003A00Ch + (k * 200h); where k = 0h to 8h

**Table 8-607. CPSW_STAT_RXPAUSEFRAMES_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A00Ch + formula

Figure 8-276. CPSW_STAT_RXPAUSEFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-608. CPSW_STAT_RXPAUSEFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of pause frames received.

8.11.5 CPSW_STAT_RXCRCERRORS_k Register (Offset = 0003A010h + formula) [reset = 0h]

CPSW_STAT_RXCRCERRORS_k is shown in [Figure 8-277](#) and described in [Table 8-610](#).

Return to [Summary Table](#).

The total number of frames received on the port that experienced a CRC error. Such a frame:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was of length 64 to CPSW0_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no code/align error,
- Had a CRC error Overruns have no effect upon this statistic.

A CRC error is defined to be:

- A frame containing an even number of nibbles
- Failing the Frame Check Sequence test.

Offset = 0003A010h + (k * 200h); where k = 0h to 8h

**Table 8-609. CPSW_STAT_RXCRCERRORS_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A010h + formula

Figure 8-277. CPSW_STAT_RXCRCERRORS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-610. CPSW_STAT_RXCRCERRORS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of CRC errors frames received

8.11.6 CPSW_STAT_RXALIGNCODEERRORS_k Register (Offset = 0003A014h + formula) [reset = 0h]

CPSW_STAT_RXALIGNCODEERRORS_k is shown in [Figure 8-278](#) and described in [Table 8-612](#).

Return to [Summary Table](#).

Total number of alignment/code errors received

Offset = 0003A014h + (k * 200h); where k = 0h to 8h

Table 8-611.
CPSW_STAT_RXALIGNCODEERRORS_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A014h + formula

Figure 8-278. CPSW_STAT_RXALIGNCODEERRORS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-612. CPSW_STAT_RXALIGNCODEERRORS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of alignment/code errors received

8.11.7 CPSW_STAT_RXOVERSIZEDFRAMES_k Register (Offset = 0003A018h + formula) [reset = 0h]

CPSW_STAT_RXOVERSIZEDFRAMES_k is shown in [Figure 8-279](#) and described in [Table 8-614](#).

Return to [Summary Table](#).

The total number of oversized frames received on the port. An oversized frame is defined to be:

- Was any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was greater than CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN in bytes
- Had no CRC error, alignment error or code error

See the CPSW_STAT0_RXCRCERRORS statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Offset = 0003A018h + (k * 200h); where k = 0h to 8h

Table 8-613.
CPSW_STAT_RXOVERSIZEDFRAMES_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A018h + formula

Figure 8-279. CPSW_STAT_RXOVERSIZEDFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-614. CPSW_STAT_RXOVERSIZEDFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of oversized frames received.

8.11.8 CPSW_STAT_RXJABBERFRAMES_k Register (Offset = 0003A01Ch + formula) [reset = 0h]

CPSW_STAT_RXJABBERFRAMES_k is shown in [Figure 8-280](#) and described in [Table 8-616](#).

Return to [Summary Table](#).

Total number of jabber frames received

Offset = 0003A01Ch + (k * 200h); where k = 0h to 8h

**Table 8-615. CPSW_STAT_RXJABBERFRAMES_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A01Ch + formula

Figure 8-280. CPSW_STAT_RXJABBERFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-616. CPSW_STAT_RXJABBERFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of jabber frames received

8.11.9 CPSW_STAT_RXUNDERSIZEDFRAMES_k Register (Offset = 0003A020h + formula) [reset = 0h]

CPSW_STAT_RXUNDERSIZEDFRAMES_k is shown in [Figure 8-281](#) and described in [Table 8-618](#).

Return to [Summary Table](#).

The total number of undersized frames received on the port. An undersized frame is defined to be:

- Was any data frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Was less than 64 octets long
- Had no CRC error, alignment error or code error

See the CPSW_STAT0_RXCRCERRORS statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Offset = 0003A020h + (k * 200h); where k = 0h to 8h

Table 8-617.
CPSW_STAT_RXUNDERSIZEDFRAMES_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A020h + formula

Figure 8-281. CPSW_STAT_RXUNDERSIZEDFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-618. CPSW_STAT_RXUNDERSIZEDFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of undersized frames received

8.11.10 CPSW_STAT_RXFRAGMENTS_k Register (Offset = 0003A024h + formula) [reset = 0h]

CPSW_STAT_RXFRAGMENTS_k is shown in [Figure 8-282](#) and described in [Table 8-620](#).

Return to [Summary Table](#).

The total number of frame fragments received on the port. A frame fragment is defined to be:

- Any data frame (address matching does not matter)
- Less than 64 bytes long
- Having a CRC error, an alignment error, or a code error
- Not the result of a collision caused by half duplex, collision based flow control

See the CPSW_STAT0_RXCRCERRORS statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Offset = 0003A024h + (k * 200h); where k = 0h to 8h

**Table 8-619. CPSW_STAT_RXFRAGMENTS_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A024h + formula

Figure 8-282. CPSW_STAT_RXFRAGMENTS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-620. CPSW_STAT_RXFRAGMENTS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of fragmented frames received.

8.11.11 CPSW_STAT_ALE_DROP_k Register (Offset = 0003A028h + formula) [reset = 0h]

CPSW_STAT_ALE_DROP_k is shown in [Figure 8-283](#) and described in [Table 8-622](#).

Return to [Summary Table](#).

Total number of frames dropped by the ALE.

Offset = 0003A028h + (k * 200h); where k = 0h to 8h

Table 8-621. CPSW_STAT_ALE_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A028h + formula

Figure 8-283. CPSW_STAT_ALE_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-622. CPSW_STAT_ALE_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames dropped by the ALE.

8.11.12 CPSW_STAT_ALE_OVERRUN_DROP_k Register (Offset = 0003A02Ch + formula) [reset = 0h]

CPSW_STAT_ALE_OVERRUN_DROP_k is shown in [Figure 8-284](#) and described in [Table 8-624](#).

Return to [Summary Table](#).

Total number of overrun frames dropped by the ALE.

Offset = 0003A02Ch + (k * 200h); where k = 0h to 8h

Table 8-623. CPSW_STAT_ALE_OVERRUN_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A02Ch + formula

Figure 8-284. CPSW_STAT_ALE_OVERRUN_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-624. CPSW_STAT_ALE_OVERRUN_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE.

8.11.13 CPSW_STAT_RXOCTETS_k Register (Offset = 0003A030h + formula) [reset = 0h]

CPSW_STAT_RXOCTETS_k is shown in [Figure 8-285](#) and described in [Table 8-626](#).

Return to [Summary Table](#).

The total number of bytes in all good frames received on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Of length 64 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes inclusive
- Had no CRC error, alignment error or code error

See the CPSW_STAT0_RXCRCERRORS statistic descriptions for total number of CRC errors. Overruns have no effect upon this statistic.

Offset = 0003A030h + (k * 200h); where k = 0h to 8h

Table 8-625. CPSW_STAT_RXOCTETS_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A030h + formula

Figure 8-285. CPSW_STAT_RXOCTETS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-626. CPSW_STAT_RXOCTETS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of received bytes in good frames

8.11.14 CPSW_STAT_TXGOODFRAMES_k Register (Offset = 0003A034h + formula) [reset = 0h]

CPSW_STAT_TXGOODFRAMES_k is shown in [Figure 8-286](#) and described in [Table 8-628](#).

Return to [Summary Table](#).

The total number of good frames transmitted on the port. A good frame is defined to be:

- Any data or MAC control frame which matched a unicast, broadcast or multicast address, or matched due to promiscuous mode
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

Offset = 0003A034h + (k * 200h); where k = 0h to 8h

**Table 8-627. CPSW_STAT_TXGOODFRAMES_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A034h + formula

Figure 8-286. CPSW_STAT_TXGOODFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-628. CPSW_STAT_TXGOODFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good frames transmitted

8.11.15 CPSW_STAT_TXBROADCASTFRAMES_k Register (Offset = 0003A038h + formula) [reset = 0h]

CPSW_STAT_TXBROADCASTFRAMES_k is shown in [Figure 8-287](#) and described in [Table 8-630](#).

Return to [Summary Table](#).

The total number of good broadcast frames transmitted on the port. A good broadcast frame is defined to be:

- Any data or MAC control frame which was destined for only address 0xFFFFFFFF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

Offset = 0003A038h + (k * 200h); where k = 0h to 8h

Table 8-629.
CPSW_STAT_TXBROADCASTFRAMES_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A038h + formula

Figure 8-287. CPSW_STAT_TXBROADCASTFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-630. CPSW_STAT_TXBROADCASTFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good broadcast frames transmitted

8.11.16 CPSW_STAT_TXMULTICASTFRAMES_k Register (Offset = 0003A03Ch + formula) [reset = 0h]

CPSW_STAT_TXMULTICASTFRAMES_k is shown in [Figure 8-288](#) and described in [Table 8-632](#).

Return to [Summary Table](#).

The total number of good multicast frames transmitted on the port. A good multicast frame is defined to be:

- Any data or MAC control frame which was destined for any multicast address other than 0xFFFFFFFF
- Any length
- Had no late or excessive collisions, no carrier loss and no underrun

Offset = 0003A03Ch + (k * 200h); where k = 0h to 8h

Table 8-631. CPSW_STAT_TXMULTICASTFRAMES_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A03Ch + formula

Figure 8-288. CPSW_STAT_TXMULTICASTFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-632. CPSW_STAT_TXMULTICASTFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of good multicast frames transmitted

8.11.17 CPSW_STAT_TXPAUSEFRAMES_k Register (Offset = 0003A040h + formula) [reset = 0h]

CPSW_STAT_TXPAUSEFRAMES_k is shown in [Figure 8-289](#) and described in [Table 8-634](#).

Return to [Summary Table](#).

Total number of pause frames transmitted

Offset = 0003A040h + (k * 200h); where k = 0h to 8h

**Table 8-633. CPSW_STAT_TXPAUSEFRAMES_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A040h + formula

Figure 8-289. CPSW_STAT_TXPAUSEFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-634. CPSW_STAT_TXPAUSEFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of pause frames transmitted

8.11.18 CPSW_STAT_TXDEFERREDFRAMES_k Register (Offset = 0003A044h + formula) [reset = 0h]

CPSW_STAT_TXDEFERREDFRAMES_k is shown in [Figure 8-290](#) and described in [Table 8-636](#).

Return to [Summary Table](#).

Total number of deferred frames transmitted

Offset = 0003A044h + (k * 200h); where k = 0h to 8h

Table 8-635. CPSW_STAT_TXDEFERREDFRAMES_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A044h + formula

Figure 8-290. CPSW_STAT_TXDEFERREDFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-636. CPSW_STAT_TXDEFERREDFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of deferred frames transmitted

8.11.19 CPSW_STAT_TXCOLLISIONFRAMES_k Register (Offset = 0003A048h + formula) [reset = 0h]

CPSW_STAT_TXCOLLISIONFRAMES_k is shown in [Figure 8-291](#) and described in [Table 8-638](#).

Return to [Summary Table](#).

Total number of transmitted frames experiencing a collision

Offset = 0003A048h + (k * 200h); where k = 0h to 8h

**Table 8-637. CPSW_STAT_TXCOLLISIONFRAMES_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A048h + formula

Figure 8-291. CPSW_STAT_TXCOLLISIONFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-638. CPSW_STAT_TXCOLLISIONFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames experiencing a collision

8.11.20 CPSW_STAT_TXSINGLECOLLFRAMES_k Register (Offset = 0003A04Ch + formula) [reset = 0h]

CPSW_STAT_TXSINGLECOLLFRAMES_k is shown in [Figure 8-292](#) and described in [Table 8-640](#).

Return to [Summary Table](#).

Total number of transmitted frames experiencing a single collision

Offset = 0003A04Ch + (k * 200h); where k = 0h to 8h

Table 8-639.
CPSW_STAT_TXSINGLECOLLFRAMES_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A04Ch + formula

Figure 8-292. CPSW_STAT_TXSINGLECOLLFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-640. CPSW_STAT_TXSINGLECOLLFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames experiencing a single collision

8.11.21 CPSW_STAT_TXMULTCOLLFRAMES_k Register (Offset = 0003A050h + formula) [reset = 0h]

CPSW_STAT_TXMULTCOLLFRAMES_k is shown in [Figure 8-293](#) and described in [Table 8-642](#).

Return to [Summary Table](#).

Total number of transmitted frames experiencing multiple collisions

Offset = 0003A050h + (k * 200h); where k = 0h to 8h

**Table 8-641. CPSW_STAT_TXMULTCOLLFRAMES_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A050h + formula

Figure 8-293. CPSW_STAT_TXMULTCOLLFRAMES_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-642. CPSW_STAT_TXMULTCOLLFRAMES_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames experiencing multiple collisions

8.11.22 CPSW_STAT_TXEXCESSIVECOLLISIONS_k Register (Offset = 0003A054h + formula) [reset = 0h]

CPSW_STAT_TXEXCESSIVECOLLISIONS_k is shown in [Figure 8-294](#) and described in [Table 8-644](#).

Return to [Summary Table](#).

Total number of transmitted frames abandoned due to excessive collisions

Offset = 0003A054h + (k * 200h); where k = 0h to 8h

Table 8-643.
CPSW_STAT_TXEXCESSIVECOLLISIONS_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A054h + formula

Figure 8-294. CPSW_STAT_TXEXCESSIVECOLLISIONS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-644. CPSW_STAT_TXEXCESSIVECOLLISIONS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to excessive collisions

8.11.23 CPSW_STAT_TXLATECOLLISIONS_k Register (Offset = 0003A058h + formula) [reset = 0h]

CPSW_STAT_TXLATECOLLISIONS_k is shown in [Figure 8-295](#) and described in [Table 8-646](#).

Return to [Summary Table](#).

Total number of transmitted frames abandoned due to a late collision

Offset = 0003A058h + (k * 200h); where k = 0h to 8h

**Table 8-645. CPSW_STAT_TXLATECOLLISIONS_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A058h + formula

Figure 8-295. CPSW_STAT_TXLATECOLLISIONS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-646. CPSW_STAT_TXLATECOLLISIONS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to a late collision

8.11.24 CPSW_STAT_RXIPGERROR_k Register (Offset = 0003A05Ch + formula) [reset = 0h]

CPSW_STAT_RXIPGERROR_k is shown in [Figure 8-296](#) and described in [Table 8-648](#).

Return to [Summary Table](#).

Total number of receive inter-packet gap errors (10G only)

Offset = 0003A05Ch + (k * 200h); where k = 0h to 8h

**Table 8-647. CPSW_STAT_RXIPGERROR_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A05Ch + formula

Figure 8-296. CPSW_STAT_RXIPGERROR_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-648. CPSW_STAT_RXIPGERROR_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of receive inter-packet gap errors (10G only)

8.11.25 CPSW_STAT_TXCARRIERSENSEERRORS_k Register (Offset = 0003A060h + formula) [reset = 0h]

CPSW_STAT_TXCARRIERSENSEERRORS_k is shown in [Figure 8-297](#) and described in [Table 8-650](#).

Return to [Summary Table](#).

Total number of transmitted frames that experienced a carrier loss

Offset = 0003A060h + (k * 200h); where k = 0h to 8h

Table 8-649.
CPSW_STAT_TXCARRIERSENSEERRORS_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A060h + formula

Figure 8-297. CPSW_STAT_TXCARRIERSENSEERRORS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-650. CPSW_STAT_TXCARRIERSENSEERRORS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of transmitted frames that experienced a carrier loss

8.11.26 CPSW_STAT_TXOCTETS_k Register (Offset = 0003A064h + formula) [reset = 0h]

CPSW_STAT_TXOCTETS_k is shown in [Figure 8-298](#) and described in [Table 8-652](#).

Return to [Summary Table](#).

The total number of bytes in all good frames transmitted on the port. A good frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Was any size
- Had no late or excessive collisions, no carrier loss and no underrun.

Offset = 0003A064h + (k * 200h); where k = 0h to 8h

Table 8-651. CPSW_STAT_TXOCTETS_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A064h + formula

Figure 8-298. CPSW_STAT_TXOCTETS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-652. CPSW_STAT_TXOCTETS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

8.11.27 CPSW_STAT_OCTETFRAMES64_k Register (Offset = 0003A068h + formula) [reset = 0h]

CPSW_STAT_OCTETFRAMES64_k is shown in [Figure 8-299](#) and described in [Table 8-654](#).

Return to [Summary Table](#).

The total number of 64-byte frames received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was exactly 64 bytes long. (If the frame was being transmitted and experienced carrier loss that resulted in a frame of this size being transmitted, then the frame will be recorded in this statistic).

CRC errors, code/align errors and overruns do not affect the recording of frames in this statistic.

Offset = 0003A068h + (k * 200h); where k = 0h to 8h

**Table 8-653. CPSW_STAT_OCTETFRAMES64_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A068h + formula

Figure 8-299. CPSW_STAT_OCTETFRAMES64_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-654. CPSW_STAT_OCTETFRAMES64_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

8.11.28 CPSW_STAT_OCTETFRAMES65T127_k Register (Offset = 0003A06Ch + formula) [reset = 0h]

CPSW_STAT_OCTETFRAMES65T127_k is shown in [Figure 8-300](#) and described in [Table 8-656](#).

Return to [Summary Table](#).

The total number of frames of size 65 to 127 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 65 to 127 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Offset = 0003A06Ch + (k * 200h); where k = 0h to 8h

Table 8-655. CPSW_STAT_OCTETFRAMES65T127_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A06Ch + formula

Figure 8-300. CPSW_STAT_OCTETFRAMES65T127_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-656. CPSW_STAT_OCTETFRAMES65T127_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

8.11.29 CPSW_STAT_OCTETFRAMES128T255_k Register (Offset = 0003A070h + formula) [reset = 0h]

CPSW_STAT_OCTETFRAMES128T255_k is shown in [Figure 8-301](#) and described in [Table 8-658](#).

Return to [Summary Table](#).

The total number of frames of size 128 to 255 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 128 to 255 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Offset = 0003A070h + (k * 200h); where k = 0h to 8h

Table 8-657.
CPSW_STAT_OCTETFRAMES128T255_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A070h + formula

Figure 8-301. CPSW_STAT_OCTETFRAMES128T255_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-658. CPSW_STAT_OCTETFRAMES128T255_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

8.11.30 CPSW_STAT_OCTETFRAMES256T511_k Register (Offset = 0003A074h + formula) [reset = 0h]

CPSW_STAT_OCTETFRAMES256T511_k is shown in [Figure 8-302](#) and described in [Table 8-660](#).

Return to [Summary Table](#).

The total number of frames of size 256 to 511 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 256 to 511 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Offset = 0003A074h + (k * 200h); where k = 0h to 8h

Table 8-659.
CPSW_STAT_OCTETFRAMES256T511_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A074h + formula

Figure 8-302. CPSW_STAT_OCTETFRAMES256T511_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-660. CPSW_STAT_OCTETFRAMES256T511_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted

8.11.31 CPSW_STAT_OCTETFRAMES512T1023_k Register (Offset = 0003A078h + formula) [reset = 0h]

CPSW_STAT_OCTETFRAMES512T1023_k is shown in [Figure 8-303](#) and described in [Table 8-662](#).

Return to [Summary Table](#).

The total number of frames of size 512 to 1023 bytes received and transmitted on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
- Did not experience late collisions, excessive collisions, or carrier sense error
- Was 512 to 1023 bytes long

CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Offset = 0003A078h + (k * 200h); where k = 0h to 8h

Table 8-661.
CPSW_STAT_OCTETFRAMES512T1023_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A078h + formula

Figure 8-303. CPSW_STAT_OCTETFRAMES512T1023_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-662. CPSW_STAT_OCTETFRAMES512T1023_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted

8.11.32 CPSW_STAT_OCTETFRAMES1024TUP_k Register (Offset = 0003A07Ch + formula) [reset = 0h]

CPSW_STAT_OCTETFRAMES1024TUP_k is shown in [Figure 8-304](#) and described in [Table 8-664](#).

Return to [Summary Table](#).

The total number of frames of size 1024 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes for receive or 1024 up for transmit on the port. Such a frame is defined to be:

- Any data or MAC control frame which was destined for any unicast, broadcast or multicast address
 - Did not experience late collisions, excessive collisions, or carrier sense error
 - Was 1024 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes long on receive, or any size on transmit
- CRC errors, code/align errors, underruns and overruns do not affect the recording of frames in this statistic.

Offset = 0003A07Ch + (k * 200h); where k = 0h to 8h

Table 8-663.
CPSW_STAT_OCTETFRAMES1024TUP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A07Ch + formula

Figure 8-304. CPSW_STAT_OCTETFRAMES1024TUP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-664. CPSW_STAT_OCTETFRAMES1024TUP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of frames of size 1024 to CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes received and 1024 bytes or greater transmitted.

8.11.33 CPSW_STAT_NETOCTETS_k Register (Offset = 0003A080h + formula) [reset = 0h]

CPSW_STAT_NETOCTETS_k is shown in [Figure 8-305](#) and described in [Table 8-666](#).

Return to [Summary Table](#).

The total number of bytes of frame data received and transmitted on the port. Each frame counted:

- was any data or MAC control frame destined for any unicast, broadcast or multicast address (address match does not matter)
- Any length (including less than 64 bytes and greater than CPSW_P0_RX_MAXLEN_REG[13-0] RX_MAXLEN bytes)

Also counted in this statistic is:

- Every byte transmitted before a carrier- loss was experienced
- Every byte transmitted before each collision was experienced, (i.e. multiple retries are counted each time)
- Every byte received if the port is in half-duplex mode until a jam sequence was transmitted to initiate flow control. (The jam sequence was not counted to prevent double-counting)

Error conditions such as alignment errors, CRC errors, code errors, overruns and underruns do not affect the recording of bytes by this statistic. The objective of this statistic is to give a reasonable indication of ethernet utilization

Offset = 0003A080h + (k * 200h); where k = 0h to 8h

Table 8-665. CPSW_STAT_NETOCTETS_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A080h + formula

Figure 8-305. CPSW_STAT_NETOCTETS_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-666. CPSW_STAT_NETOCTETS_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of bytes received and transmitted

8.11.34 CPSW_STAT_RX_BOTTOM_OF_FIFO_DROP_k Register (Offset = 0003A084h + formula) [reset = 0h]

CPSW_STAT_RX_BOTTOM_OF_FIFO_DROP_k is shown in [Figure 8-306](#) and described in [Table 8-668](#).

Return to [Summary Table](#).

Receive Bottom of FIFO Drop.

Offset = 0003A084h + (k * 200h); where k = 0h to 8h

Table 8-667.
CPSW_STAT_RX_BOTTOM_OF_FIFO_DROP_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A084h + formula

Figure 8-306. CPSW_STAT_RX_BOTTOM_OF_FIFO_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-668. CPSW_STAT_RX_BOTTOM_OF_FIFO_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Receive Bottom of FIFO Drop.

8.11.35 CPSW_STAT_PORTMASK_DROP_k Register (Offset = 0003A088h + formula) [reset = 0h]

CPSW_STAT_PORTMASK_DROP_k is shown in [Figure 8-307](#) and described in [Table 8-670](#).

Return to [Summary Table](#).

Total number of dropped frames received due to portmask.

Offset = 0003A088h + (k * 200h); where k = 0h to 8h

**Table 8-669. CPSW_STAT_PORTMASK_DROP_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A088h + formula

Figure 8-307. CPSW_STAT_PORTMASK_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-670. CPSW_STAT_PORTMASK_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames received due to portmask.

8.11.36 CPSW_STAT_RX_TOP_OF_FIFO_DROP_k Register (Offset = 0003A08Ch + formula) [reset = 0h]

CPSW_STAT_RX_TOP_OF_FIFO_DROP_k is shown in [Figure 8-308](#) and described in [Table 8-672](#).

Return to [Summary Table](#).

Receive Top of FIFO Drop.

Offset = 0003A08Ch + (k * 200h); where k = 0h to 8h

Table 8-671.
CPSW_STAT_RX_TOP_OF_FIFO_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A08Ch + formula

Figure 8-308. CPSW_STAT_RX_TOP_OF_FIFO_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-672. CPSW_STAT_RX_TOP_OF_FIFO_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Receive Top of FIFO Drop.

8.11.37 CPSW_STAT_ALE_RATE_LIMIT_DROP_k Register (Offset = 0003A090h + formula) [reset = 0h]

CPSW_STAT_ALE_RATE_LIMIT_DROP_k is shown in [Figure 8-309](#) and described in [Table 8-674](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Rate Limiting.

Offset = 0003A090h + (k * 200h); where k = 0h to 8h

Table 8-673.
CPSW_STAT_ALE_RATE_LIMIT_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A090h + formula

Figure 8-309. CPSW_STAT_ALE_RATE_LIMIT_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-674. CPSW_STAT_ALE_RATE_LIMIT_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting.

8.11.38 CPSW_STAT_ALE_VID_INGRESS_DROP_k Register (Offset = 0003A094h + formula) [reset = 0h]

CPSW_STAT_ALE_VID_INGRESS_DROP_k is shown in [Figure 8-310](#) and described in [Table 8-676](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE VID Ingress.

Offset = 0003A094h + (k * 200h); where k = 0h to 8h

Table 8-675.
CPSW_STAT_ALE_VID_INGRESS_DROP_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A094h + formula

Figure 8-310. CPSW_STAT_ALE_VID_INGRESS_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-676. CPSW_STAT_ALE_VID_INGRESS_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress.

8.11.39 CPSW_STAT_ALE_DA_EQ_SA_DROP_k Register (Offset = 0003A098h + formula) [reset = 0h]

CPSW_STAT_ALE_DA_EQ_SA_DROP_k is shown in [Figure 8-311](#) and described in [Table 8-678](#).

Return to [Summary Table](#).

Total number of dropped frames due to DA=SA.

Offset = 0003A098h + (k * 200h); where k = 0h to 8h

Table 8-677.
CPSW_STAT_ALE_DA_EQ_SA_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A098h + formula

Figure 8-311. CPSW_STAT_ALE_DA_EQ_SA_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-678. CPSW_STAT_ALE_DA_EQ_SA_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA.

8.11.40 CPSW_STAT_ALE_BLOCK_DROP_k Register (Offset = 0003A09Ch + formula) [reset = 0h]

CPSW_STAT_ALE_BLOCK_DROP_k is shown in [Figure 8-312](#) and described in [Table 8-680](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Block Mode.

Offset = 0003A09Ch + (k * 200h); where k = 0h to 8h

Table 8-679. CPSW_STAT_ALE_BLOCK_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A09Ch + formula

Figure 8-312. CPSW_STAT_ALE_BLOCK_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-680. CPSW_STAT_ALE_BLOCK_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode.

8.11.41 CPSW_STAT_ALE_SECURE_DROP_k Register (Offset = 0003A0A0h + formula) [reset = 0h]

CPSW_STAT_ALE_SECURE_DROP_k is shown in [Figure 8-313](#) and described in [Table 8-682](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Secure Mode.

Offset = 0003A0A0h + (k * 200h); where k = 0h to 8h

**Table 8-681. CPSW_STAT_ALE_SECURE_DROP_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0A0h + formula

Figure 8-313. CPSW_STAT_ALE_SECURE_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-682. CPSW_STAT_ALE_SECURE_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode.

8.11.42 CPSW_STAT_ALE_AUTH_DROP_k Register (Offset = 0003A0A4h + formula) [reset = 0h]

CPSW_STAT_ALE_AUTH_DROP_k is shown in [Figure 8-314](#) and described in [Table 8-684](#).

Return to [Summary Table](#).

Total number of dropped frames due to ALE Authentication.

Offset = 0003A0A4h + (k * 200h); where k = 0h to 8h

**Table 8-683. CPSW_STAT_ALE_AUTH_DROP_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0A4h + formula

Figure 8-314. CPSW_STAT_ALE_AUTH_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-684. CPSW_STAT_ALE_AUTH_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication.

8.11.43 CPSW_STAT_ALE_UNKN_UNI_k Register (Offset = 0003A0A8h + formula) [reset = 0h]

CPSW_STAT_ALE_UNKN_UNI_k is shown in [Figure 8-315](#) and described in [Table 8-686](#).

Return to [Summary Table](#).

ALE Receive Unknown Unicast.

Offset = 0003A0A8h + (k * 200h); where k = 0h to 8h

**Table 8-685. CPSW_STAT_ALE_UNKN_UNI_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0A8h + formula

Figure 8-315. CPSW_STAT_ALE_UNKN_UNI_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-686. CPSW_STAT_ALE_UNKN_UNI_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Unicast.

8.11.44 CPSW_STAT_ALE_UNKN_UNI_BCNT_k Register (Offset = 0003A0ACh + formula) [reset = 0h]

CPSW_STAT_ALE_UNKN_UNI_BCNT_k is shown in [Figure 8-316](#) and described in [Table 8-688](#).

Return to [Summary Table](#).

ALE Receive Unknown Unicast Bytecount.

Offset = 0003A0ACh + (k * 200h); where k = 0h to 8h

Table 8-687. CPSW_STAT_ALE_UNKN_UNI_BCNT_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0ACh + formula

Figure 8-316. CPSW_STAT_ALE_UNKN_UNI_BCNT_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-688. CPSW_STAT_ALE_UNKN_UNI_BCNT_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount.

8.11.45 CPSW_STAT_ALE_UNKN_MLT_K Register (Offset = 0003A0B0h + formula) [reset = 0h]

CPSW_STAT_ALE_UNKN_MLT_K is shown in [Figure 8-317](#) and described in [Table 8-690](#).

Return to [Summary Table](#).

ALE Receive Unknown Multicast.

Offset = 0003A0B0h + (k * 200h); where k = 0h to 8h

**Table 8-689. CPSW_STAT_ALE_UNKN_MLT_K
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0B0h + formula

Figure 8-317. CPSW_STAT_ALE_UNKN_MLT_K Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-690. CPSW_STAT_ALE_UNKN_MLT_K Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Multicast.

8.11.46 CPSW_STAT_ALE_UNKN_MLT_BCNT_k Register (Offset = 0003A0B4h + formula) [reset = 0h]

CPSW_STAT_ALE_UNKN_MLT_BCNT_k is shown in [Figure 8-318](#) and described in [Table 8-692](#).

Return to [Summary Table](#).

ALE Receive Unknown Multicast Bytecount.

Offset = 0003A0B4h + (k * 200h); where k = 0h to 8h

Table 8-691. CPSW_STAT_ALE_UNKN_MLT_BCNT_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0B4h + formula

Figure 8-318. CPSW_STAT_ALE_UNKN_MLT_BCNT_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-692. CPSW_STAT_ALE_UNKN_MLT_BCNT_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount.

8.11.47 CPSW_STAT_ALE_UNKN_BRD_k Register (Offset = 0003A0B8h + formula) [reset = 0h]

CPSW_STAT_ALE_UNKN_BRD_k is shown in [Figure 8-319](#) and described in [Table 8-694](#).

Return to [Summary Table](#).

ALE Receive Unknown Broadcast.

Offset = 0003A0B8h + (k * 200h); where k = 0h to 8h

**Table 8-693. CPSW_STAT_ALE_UNKN_BRD_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0B8h + formula

Figure 8-319. CPSW_STAT_ALE_UNKN_BRD_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-694. CPSW_STAT_ALE_UNKN_BRD_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Broadcast.

8.11.48 CPSW_STAT_ALE_UNKN_BRD_BCNT_k Register (Offset = 0003A0BCh + formula) [reset = 0h]

CPSW_STAT_ALE_UNKN_BRD_BCNT_k is shown in [Figure 8-320](#) and described in [Table 8-696](#).

Return to [Summary Table](#).

ALE Receive Unknown Broadcast Bytecount.

Offset = 0003A0BCh + (k * 200h); where k = 0h to 8h

Table 8-695.
CPSW_STAT_ALE_UNKN_BRD_BCNT_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0BCh + formula

Figure 8-320. CPSW_STAT_ALE_UNKN_BRD_BCNT_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-696. CPSW_STAT_ALE_UNKN_BRD_BCNT_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount.

8.11.49 CPSW_STAT_ALE_POL_MATCH_k Register (Offset = 0003A0C0h + formula) [reset = 0h]

CPSW_STAT_ALE_POL_MATCH_k is shown in [Figure 8-321](#) and described in [Table 8-698](#).

Return to [Summary Table](#).

ALE Policer Matched.

Offset = 0003A0C0h + (k * 200h); where k = 0h to 8h

**Table 8-697. CPSW_STAT_ALE_POL_MATCH_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0C0h + formula

Figure 8-321. CPSW_STAT_ALE_POL_MATCH_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-698. CPSW_STAT_ALE_POL_MATCH_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched.

8.11.50 CPSW_STAT_ALE_POL_MATCH_RED_k Register (Offset = 0003A0C4h + formula) [reset = 0h]

CPSW_STAT_ALE_POL_MATCH_RED_k is shown in [Figure 8-322](#) and described in [Table 8-700](#).

Return to [Summary Table](#).

ALE Policer Matched and Condition Red.

Offset = 0003A0C4h + (k * 200h); where k = 0h to 8h

Table 8-699.
CPSW_STAT_ALE_POL_MATCH_RED_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0C4h + formula

Figure 8-322. CPSW_STAT_ALE_POL_MATCH_RED_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-700. CPSW_STAT_ALE_POL_MATCH_RED_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched and Condition Red.

8.11.51 CPSW_STAT_ALE_POL_MATCH_YELLOW_k Register (Offset = 0003A0C8h + formula) [reset = 0h]

CPSW_STAT_ALE_POL_MATCH_YELLOW_k is shown in [Figure 8-323](#) and described in [Table 8-702](#).

Return to [Summary Table](#).

ALE Policer Matched and Condition Yellow.

Offset = 0003A0C8h + (k * 200h); where k = 0h to 8h

Table 8-701.
CPSW_STAT_ALE_POL_MATCH_YELLOW_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0C8h + formula

Figure 8-323. CPSW_STAT_ALE_POL_MATCH_YELLOW_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-702. CPSW_STAT_ALE_POL_MATCH_YELLOW_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow.

8.11.52 CPSW_STAT_ALE_MULT_SA_DROP_k Register (Offset = 0003A0CCh + formula) [reset = 0h]

CPSW_STAT_ALE_MULT_SA_DROP_k is shown in [Figure 8-324](#) and described in [Table 8-704](#).

Return to [Summary Table](#).

ALE Multicast Source Address Drop.

Offset = 0003A0CCh + (k * 200h); where k = 0h to 8h

Table 8-703. CPSW_STAT_ALE_MULT_SA_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0CCh + formula

Figure 8-324. CPSW_STAT_ALE_MULT_SA_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-704. CPSW_STAT_ALE_MULT_SA_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Multicast Source Address drop.

8.11.53 CPSW_STAT_ALE_DUAL_VLAN_DROP_k Register (Offset = 0003A0D0h + formula) [reset = 0h]

CPSW_STAT_ALE_DUAL_VLAN_DROP_k is shown in [Figure 8-325](#) and described in [Table 8-706](#).

Return to [Summary Table](#).

ALE Dual VLAN Drop.

Offset = 0003A0D0h + (k * 200h); where k = 0h to 8h

Table 8-705.
CPSW_STAT_ALE_DUAL_VLAN_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0D0h + formula

Figure 8-325. CPSW_STAT_ALE_DUAL_VLAN_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-706. CPSW_STAT_ALE_DUAL_VLAN_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Dual VLAN drop.

8.11.54 CPSW_STAT_ALE_LEN_ERROR_DROP_k Register (Offset = 0003A0D4h + formula) [reset = 0h]

CPSW_STAT_ALE_LEN_ERROR_DROP_k is shown in [Figure 8-326](#) and described in [Table 8-708](#).

Return to [Summary Table](#).

ALE Length Error Drop.

Offset = 0003A0D4h + (k * 200h); where k = 0h to 8h

Table 8-707.
CPSW_STAT_ALE_LEN_ERROR_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0D4h + formula

Figure 8-326. CPSW_STAT_ALE_LEN_ERROR_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-708. CPSW_STAT_ALE_LEN_ERROR_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Length Error drop.

8.11.55 CPSW_STAT_ALE_IP_NEXT_HDR_DROP_k Register (Offset = 0003A0D8h + formula) [reset = 0h]

CPSW_STAT_ALE_IP_NEXT_HDR_DROP_k is shown in [Figure 8-327](#) and described in [Table 8-710](#).

Return to [Summary Table](#).

ALE IP Next Header Drop.

Offset = 0003A0D8h + (k * 200h); where k = 0h to 8h

Table 8-709.
CPSW_STAT_ALE_IP_NEXT_HDR_DROP_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0D8h + formula

Figure 8-327. CPSW_STAT_ALE_IP_NEXT_HDR_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-710. CPSW_STAT_ALE_IP_NEXT_HDR_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE Next Header drop.

8.11.56 CPSW_STAT_ALE_IPV4_FRAG_DROP_k Register (Offset = 0003A0DCh + formula) [reset = 0h]

CPSW_STAT_ALE_IPV4_FRAG_DROP_k is shown in [Figure 8-328](#) and described in [Table 8-712](#).

Return to [Summary Table](#).

ALE IPV4 Frag Drop.

Offset = 0003A0DCh + (k * 200h); where k = 0h to 8h

Table 8-711.
CPSW_STAT_ALE_IPV4_FRAG_DROP_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A0DCh + formula

Figure 8-328. CPSW_STAT_ALE_IPV4_FRAG_DROP_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-712. CPSW_STAT_ALE_IPV4_FRAG_DROP_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	ALE IPV4 Fragment drop.

8.11.57 CPSW_STAT_IET_RX_ASSEMBLY_ERROR_REG_k Register (Offset = 0003A140h + formula) [reset = 0h]

CPSW_STAT_IET_RX_ASSEMBLY_ERROR_REG_k is shown in [Figure 8-329](#) and described in [Table 8-714](#).

Return to [Summary Table](#).

IET Receive Assembly Error.

Offset = 0003A140h + (k * 200h); where k = 0h to 8h

Note: IET functionality is not supported for CPSW0 Port 0.

Table 8-713.
CPSW_STAT_IET_RX_ASSEMBLY_ERROR_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A140h + formula

Figure 8-329. CPSW_STAT_IET_RX_ASSEMBLY_ERROR_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_ERROR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-714. CPSW_STAT_IET_RX_ASSEMBLY_ERROR_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_ASSEMBLY_ERROR	R/W	0h	IET Receive Assembly Error. Note: IET functionality is not supported for CPSW0 Port 0.

8.11.58 CPSW_STAT_IET_RX_ASSEMBLY_OK_REG_k Register (Offset = 0003A144h + formula) [reset = 0h]

CPSW_STAT_IET_RX_ASSEMBLY_OK_REG_k is shown in [Figure 8-330](#) and described in [Table 8-716](#).

Return to [Summary Table](#).

IET Receive Assembly Ok.

Offset = 0003A144h + (k * 200h); where k = 0h to 8h

Note: IET functionality is not supported for CPSW0 Port 0.

Table 8-715.
CPSW_STAT_IET_RX_ASSEMBLY_OK_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A144h + formula

Figure 8-330. CPSW_STAT_IET_RX_ASSEMBLY_OK_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_OK																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-716. CPSW_STAT_IET_RX_ASSEMBLY_OK_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_ASSEMBLY_OK	R/W	0h	IET Receive Assembly Ok. Note: IET functionality is not supported for CPSW0 Port 0.

8.11.59 CPSW_STAT_IET_RX_SMD_ERROR_REG_k Register (Offset = 0003A148h + formula) [reset = 0h]

CPSW_STAT_IET_RX_SMD_ERROR_REG_k is shown in [Figure 8-331](#) and described in [Table 8-718](#).

Return to [Summary Table](#).

IET Receive Smd Error.

Offset = 0003A148h + (k * 200h); where k = 0h to 8h

Note: IET functionality is not supported for CPSW0 Port 0.

Table 8-717.
CPSW_STAT_IET_RX_SMD_ERROR_REG_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A148h + formula

Figure 8-331. CPSW_STAT_IET_RX_SMD_ERROR_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_SMD_ERROR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-718. CPSW_STAT_IET_RX_SMD_ERROR_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_SMD_ERROR	R/W	0h	IET Receive Smd Error. Note: IET functionality is not supported for CPSW0 Port 0.

8.11.60 CPSW_STAT_IET_RX_FRAG_REG_k Register (Offset = 0003A14Ch + formula) [reset = 0h]

CPSW_STAT_IET_RX_FRAG_REG_k is shown in [Figure 8-332](#) and described in [Table 8-720](#).

Return to [Summary Table](#).

IET Receive Frag.

Offset = 0003A14Ch + (k * 200h); where k = 0h to 8h

Note: IET functionality is not supported for CPSW0 Port 0.

Table 8-719. CPSW_STAT_IET_RX_FRAG_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A14Ch + formula

Figure 8-332. CPSW_STAT_IET_RX_FRAG_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_FRAG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-720. CPSW_STAT_IET_RX_FRAG_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_RX_FRAG	R/W	0h	IET Receive Frag. Note: IET functionality is not supported for CPSW0 Port 0.

8.11.61 CPSW_STAT_IET_TX_HOLD_REG_k Register (Offset = 0003A150h + formula) [reset = 0h]

CPSW_STAT_IET_TX_HOLD_REG_k is shown in [Figure 8-333](#) and described in [Table 8-722](#).

Return to [Summary Table](#).

IET Transmit Hold.

Offset = 0003A150h + (k * 200h); where k = 0h to 8h

Note: IET functionality is not supported for CPSW0 Port 0.

**Table 8-721. CPSW_STAT_IET_TX_HOLD_REG_k
Instances**

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A150h + formula

Figure 8-333. CPSW_STAT_IET_TX_HOLD_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_TX_HOLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-722. CPSW_STAT_IET_TX_HOLD_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_TX_HOLD	R/W	0h	IET Transmit Hold. Note: IET functionality is not supported for CPSW0 Port 0.

8.11.62 CPSW_STAT_IET_TX_FRAG_REG_k Register (Offset = 0003A154h + formula) [reset = 0h]

CPSW_STAT_IET_TX_FRAG_REG_k is shown in [Figure 8-334](#) and described in [Table 8-724](#).

Return to [Summary Table](#).

IET Transmit Frag.

Offset = 0003A154h + (k * 200h); where k = 0h to 8h

Note: IET functionality is not supported for CPSW0 Port 0.

Table 8-723. CPSW_STAT_IET_TX_FRAG_REG_k Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A154h + formula

Figure 8-334. CPSW_STAT_IET_TX_FRAG_REG_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_TX_FRAG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-724. CPSW_STAT_IET_TX_FRAG_REG_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IET_TX_FRAG	R/W	0h	IET Transmit Frag. Note: IET functionality is not supported for CPSW0 Port 0.

8.11.63 CPSW_STAT_TX_MEMORY_PROTECT_ERROR_k Register (Offset = 0003A17Ch + formula) [reset = X]

CPSW_STAT_TX_MEMORY_PROTECT_ERROR_k is shown in [Figure 8-335](#) and described in [Table 8-726](#).

Return to [Summary Table](#).

Transmit Memory Protect CRC Error.

Offset = 0003A17Ch + (k * 200h); where k = 0h to 8h

Table 8-725.
CPSW_STAT_TX_MEMORY_PROTECT_ERROR_k
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A17Ch + formula

Figure 8-335. CPSW_STAT_TX_MEMORY_PROTECT_ERROR_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								COUNT							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-726. CPSW_STAT_TX_MEMORY_PROTECT_ERROR_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	COUNT	R/W	0h	Transmit Memory Protect CRC Error. Note: If there is a memory protect error, then this COUNT value will increment and issue a STAT_PEND0 interrupt, when this bit field is non-zero. That is different from the other stats which only issue an interrupt when their values are greater than 0xFFFF.

8.11.64 CPSW_STAT_ENET_PN_TX_PRI_REG_k_y Register (Offset = 0003A180h + formula) [reset = 0h]

CPSW_STAT_ENET_PN_TX_PRI_REG_k_y is shown in [Figure 8-336](#) and described in [Table 8-728](#).

Return to [Summary Table](#).

ENET Port n PRIORITY N Packet Count.

Offset = 0003A180h + (k * 200h) + (y * 4h); where k = 0h to 8h, y = 0h to 7h

Table 8-727.
CPSW_STAT_ENET_PN_TX_PRI_REG_k_y
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A180h + formula

Figure 8-336. CPSW_STAT_ENET_PN_TX_PRI_REG_k_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-728. CPSW_STAT_ENET_PN_TX_PRI_REG_k_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PN_TX_PRIN	R/W	0h	ENET TX Priority Packet Count.

8.11.65 CPSW_STAT_ENET_PN_TX_PRI_BCNT_REG_k_y Register (Offset = 0003A1A0h + formula) [reset = 0h]

CPSW_STAT_ENET_PN_TX_PRI_BCNT_REG_k_y is shown in [Figure 8-337](#) and described in [Table 8-730](#).

Return to [Summary Table](#).

ENET Port n PRIORITY N Packet Byte Count.

Offset = 0003A1A0h + (k * 200h) + (y * 4h); where k = 0h to 8h, y = 0h to 7h

Table 8-729.
CPSW_STAT_ENET_PN_TX_PRI_BCNT_REG_k_y
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A1A0h + formula

Figure 8-337. CPSW_STAT_ENET_PN_TX_PRI_BCNT_REG_k_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_BCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-730. CPSW_STAT_ENET_PN_TX_PRI_BCNT_REG_k_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PN_TX_PRIN_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Byte Count.

8.11.66 CPSW_STAT_ENET_PN_TX_PRI_DROP_REG_k_y Register (Offset = 0003A1C0h + formula) [reset = 0h]

CPSW_STAT_ENET_PN_TX_PRI_DROP_REG_k_y is shown in [Figure 8-338](#) and described in [Table 8-732](#).

Return to [Summary Table](#).

ENET Port n PRIORITY N Packet Drop Count.

Offset = 0003A1C0h + (k * 200h) + (y * 4h); where k = 0h to 8h, y = 0h to 7h

Table 8-731.
CPSW_STAT_ENET_PN_TX_PRI_DROP_REG_k_y
Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A1C0h + formula

Figure 8-338. CPSW_STAT_ENET_PN_TX_PRI_DROP_REG_k_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-732. CPSW_STAT_ENET_PN_TX_PRI_DROP_REG_k_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PN_TX_PRIN_DROP	R/W	0h	ENET Port n PRIORITY N Packet Drop Count.

8.11.67 CPSW_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_k_y Register (Offset = 0003A1E0h + formula) [reset = 0h]

CPSW_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_k_y is shown in [Figure 8-339](#) and described in [Table 8-734](#).

Return to [Summary Table](#).

ENET Port n PRIORITY N Packet Drop Byte Count.

Offset = 0003A1E0h + (k * 200h) + (y * 4h); where k = 0h to 8h, y = 0h to 7h

Table 8-733.
CPSW_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG
_k_y Instances

Instance	Physical Address
CPSW0_NUSS_STAT	0C03 A1E0h + formula

Figure 8-339. CPSW_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_k_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP_BCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-734. CPSW_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_k_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PN_TX_PRIN_DROP_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Drop Byte Count.

9 PCIe Subsystem Registers

This section describes the PCIe Subsystem registers.

9.1 PCIE_CORE_AXI Registers

Table 9-2 lists the PCIE_CORE_AXI registers. All register offset addresses not listed in Table 9-2 should be considered as reserved locations and the register contents should not be modified.

PCIE core AXI configuration registers

Table 9-1. PCIE_CORE_AXI Instances

Instance	Base Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0000h

Table 9-2. PCIE_CORE_AXI Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE1_CORE_DBN_CFG_PCIE_CORE Physical Address
00400000h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0		0D40 0000h + formula	0DC0 0000h + formula
00400004h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1		0D40 0004h + formula	0DC0 0004h + formula
00400008h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_DESC0		0D40 0008h + formula	0DC0 0008h + formula
0040000Ch + formula	PCIE_CORE_ATU_WRAPPER_OB_i_DESC1		0D40 000Ch + formula	0DC0 000Ch + formula
00400014h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_DESC3		0D40 0014h + formula	0DC0 0014h + formula
00400018h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0		0D40 0018h + formula	0DC0 0018h + formula
0040001Ch + formula	PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1		0D40 001Ch + formula	0DC0 001Ch + formula
00400400h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0		0D40 0400h + formula	0DC0 0400h + formula
00400404h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1		0D40 0404h + formula	0DC0 0404h + formula
00400408h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0		0D40 0408h + formula	0DC0 0408h + formula
0040040Ch + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1		0D40 040Ch + formula	0DC0 040Ch + formula
00400414h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3		0D40 0414h + formula	0DC0 0414h + formula
00400418h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR0		0D40 0418h + formula	0DC0 0418h + formula
0040041Ch + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1		0D40 041Ch + formula	0DC0 041Ch + formula
00400800h + formula	PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0		0D40 0800h + formula	0DC0 0800h + formula
00400804h + formula	PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1		0D40 0804h + formula	0DC0 0804h + formula
00400820h	PCIE_CORE_ATU_CREDIT_THRESHOLD_C0		0D40 0820h	0DC0 0820h
00400824h	PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0		0D40 0824h	0DC0 0824h
00400840h + formula	PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR0		0D40 0840h + formula	0DC0 0840h + formula
00400844h + formula	PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR1		0D40 0844h + formula	0DC0 0844h + formula

Table 9-3. PCIE_CORE_AXI Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
00400000h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0		0E40 0000h + formula	0EC0 0000h + formula
00400004h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1		0E40 0004h + formula	0EC0 0004h + formula
00400008h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_DESC0		0E40 0008h + formula	0EC0 0008h + formula
0040000Ch + formula	PCIE_CORE_ATU_WRAPPER_OB_i_DESC1		0E40 000Ch + formula	0EC0 000Ch + formula
00400014h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_DESC3		0E40 0014h + formula	0EC0 0014h + formula
00400018h + formula	PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0		0E40 0018h + formula	0EC0 0018h + formula
0040001Ch + formula	PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1		0E40 001Ch + formula	0EC0 001Ch + formula
00400400h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0		0E40 0400h + formula	0EC0 0400h + formula
00400404h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1		0E40 0404h + formula	0EC0 0404h + formula
00400408h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0		0E40 0408h + formula	0EC0 0408h + formula
0040040Ch + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1		0E40 040Ch + formula	0EC0 040Ch + formula
00400414h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3		0E40 0414h + formula	0EC0 0414h + formula
00400418h + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR0		0E40 0418h + formula	0EC0 0418h + formula
0040041Ch + formula	PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1		0E40 041Ch + formula	0EC0 041Ch + formula
00400800h + formula	PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0		0E40 0800h + formula	0EC0 0800h + formula
00400804h + formula	PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1		0E40 0804h + formula	0EC0 0804h + formula
00400820h	PCIE_CORE_ATU_CREDIT_THRESHOLD_C0		0E40 0820h	0EC0 0820h
00400824h	PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0		0E40 0824h	0EC0 0824h
00400840h + formula	PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR 0		0E40 0840h + formula	0EC0 0840h + formula
00400844h + formula	PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR 1		0E40 0844h + formula	0EC0 0844h + formula

9.1.1 PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0 Register (Offset = 00400000h + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0 is shown in [Figure 9-1](#) and described in [Table 9-5](#).

Return to the [Summary Table](#).

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Offset = 400000h + (i * 20h); where i = 0h to 1Fh

Table 9-4.
PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0000h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0000h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0000h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0000h + formula

Figure 9-1. PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-5. PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

Table 9-6. Register Call Summary for PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_WRAPPER_OB_i_ADDR0 Register \(Offset = 00400000h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.2 PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1 Register (Offset = 00400004h + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1 is shown in [Figure 9-2](#) and described in [Table 9-8](#).

Return to the [Summary Table](#).

Provides bits 63:32 of the PCIe address

Offset = 400004h + (i * 20h); where i = 0h to 1Fh

Table 9-7.
PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0004h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0004h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0004h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0004h + formula

Figure 9-2. PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-8. PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

Table 9-9. Register Call Summary for PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_WRAPPER_OB_i_ADDR1 Register \(Offset = 00400004h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.3 PCIE_CORE_ATU_WRAPPER_OB_i_DESC0 Register (Offset = 00400008h + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_OB_i_DESC0 is shown in [Figure 9-3](#) and described in [Table 9-11](#).

Return to the [Summary Table](#).

Provides bits 31:0 of the Outbound PCIe Descriptor

Offset = 400008h + (i * 20h); where i = 0h to 1Fh

Table 9-10.
PCIE_CORE_ATU_WRAPPER_OB_i_DESC0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0008h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0008h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0008h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0008h + formula

Figure 9-3. PCIE_CORE_ATU_WRAPPER_OB_i_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-11. PCIE_CORE_ATU_WRAPPER_OB_i_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

Table 9-12. Register Call Summary for PCIE_CORE_ATU_WRAPPER_OB_i_DESC0

PCIE_CORE_AXI Registers

- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)
- [PCIE_CORE_ATU_WRAPPER_OB_i_DESC0 Register \(Offset = 00400008h + formula\) \[reset = 0h\]: \[0\]](#)

9.1.4 PCIE_CORE_ATU_WRAPPER_OB_i_DESC1 Register (Offset = 0040000Ch + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_OB_i_DESC1 is shown in [Figure 9-4](#) and described in [Table 9-14](#).

Return to the [Summary Table](#).

Provides bits 63:32 of the PCIe Descriptor

Offset = 40000Ch + (i * 20h); where i = 0h to 1Fh

Table 9-13.
PCIE_CORE_ATU_WRAPPER_OB_i_DESC1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 000Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 000Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 000Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 000Ch + formula

Figure 9-4. PCIE_CORE_ATU_WRAPPER_OB_i_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-14. PCIE_CORE_ATU_WRAPPER_OB_i_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

Table 9-15. Register Call Summary for PCIE_CORE_ATU_WRAPPER_OB_i_DESC1

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_WRAPPER_OB_i_DESC1 Register \(Offset = 0040000Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.5 PCIE_CORE_ATU_WRAPPER_OB_i_DESC3 Register (Offset = 00400014h + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_OB_i_DESC3 is shown in [Figure 9-5](#) and described in [Table 9-17](#).

Return to the [Summary Table](#).

Provides PASID Value and The present bit

Offset = 400014h + (i * 20h); where i = 0h to 1Fh

Table 9-16.
PCIE_CORE_ATU_WRAPPER_OB_i_DESC3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0014h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0014h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0014h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0014h + formula

Figure 9-5. PCIE_CORE_ATU_WRAPPER_OB_i_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-17. PCIE_CORE_ATU_WRAPPER_OB_i_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

Table 9-18. Register Call Summary for PCIE_CORE_ATU_WRAPPER_OB_i_DESC3

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_WRAPPER_OB_i_DESC3 Register \(Offset = 00400014h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.6 PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0 Register (Offset = 00400018h + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0 is shown in Figure 9-6 and described in Table 9-20.

Return to the [Summary Table](#).

holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Offset = 400018h + (i * 20h); where i = 0h to 1Fh

Table 9-19.
PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0018h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0018h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0018h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0018h + formula

Figure 9-6. PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-20. PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

Table 9-21. Register Call Summary for PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR0 Register \(Offset = 00400018h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.7 PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1 Register (Offset = 0040001Ch + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1 is shown in Figure 9-7 and described in Table 9-23.

Return to the [Summary Table](#).

holds the base address [63:32] of this region.

Offset = 40001Ch + (i * 20h); where i = 0h to 1Fh

Table 9-22.
PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 001Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 001Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 001Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 001Ch + formula

Figure 9-7. PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-23. PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

Table 9-24. Register Call Summary for PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_WRAPPER_OB_i_AXI_ADDR1 Register \(Offset = 0040001Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.8 PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0 Register (Offset = 00400400h + formula) [reset = 0h]

PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0 is shown in Figure 9-8 and described in Table 9-26.

Return to the [Summary Table](#).

Provides bits 31:8 of the PCIe address and the number of AXI address bits passed through

Offset = 400400h + (i * 20h); where i = 0h to 1Fh

Table 9-25.
PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0400h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0400h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0400h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0400h + formula

Figure 9-8. PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-26. PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

Table 9-27. Register Call Summary for PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0

PCIE_CORE_AXI Registers

- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)
- [PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR0 Register \(Offset = 00400400h + formula\) \[reset = 0h\]: \[0\]](#)

9.1.9 PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1 Register (Offset = 00400404h + formula) [reset = 0h]

PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1 is shown in [Figure 9-9](#) and described in [Table 9-29](#).

Return to the [Summary Table](#).

Provides bits 63:32 of the PCIe address

Offset = 400404h + (i * 20h); where i = 0h to 1Fh

Table 9-28.
PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0404h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0404h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0404h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0404h + formula

Figure 9-9. PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-29. PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

Table 9-30. Register Call Summary for PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_HP_WRAPPER_OB_i_ADDR1 Register \(Offset = 00400404h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.10 PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0 Register (Offset = 00400408h + formula) [reset = 0h]

PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0 is shown in [Figure 9-10](#) and described in [Table 9-32](#).

Return to the [Summary Table](#).

Provides bits 31:0 of the Outbound PCIe Descriptor

Offset = 400408h + (i * 20h); where i = 0h to 1Fh

Table 9-31.
PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0408h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0408h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0408h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0408h + formula

Figure 9-10. PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-32. PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

Table 9-33. Register Call Summary for PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC0 Register \(Offset = 00400408h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.11 PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1 Register (Offset = 0040040Ch + formula) [reset = 0h]

PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1 is shown in [Figure 9-11](#) and described in [Table 9-35](#).

Return to the [Summary Table](#).

Provides bits 63:32 of the PCIe Descriptor

Offset = 40040Ch + (i * 20h); where i = 0h to 1Fh

Table 9-34.
PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 040Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 040Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 040Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 040Ch + formula

Figure 9-11. PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-35. PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

Table 9-36. Register Call Summary for PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC1 Register \(Offset = 0040040Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.12 PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3 Register (Offset = 00400414h + formula) [reset = 0h]

PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3 is shown in [Figure 9-12](#) and described in [Table 9-38](#).

Return to the [Summary Table](#).

Provides PASID Value and The present bit

Offset = 400414h + (i * 20h); where i = 0h to 1Fh

Table 9-37.
PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0414h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0414h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0414h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0414h + formula

Figure 9-12. PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									DATA																						
R-0h									R/W-0h																						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-38. PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

Table 9-39. Register Call Summary for PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_HP_WRAPPER_OB_i_DESC3 Register \(Offset = 00400414h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.13 PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR0 Register (Offset = 00400418h + formula) [reset = 0h]

PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR0 is shown in Figure 9-13 and described in Table 9-41.

Return to the [Summary Table](#).

Holds the base address [31:8] of this region. Lower [5:0] is used for region size programmability

Offset = 400418h + (i * 20h); where i = 0h to 1Fh

Table 9-40.
PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR
0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0418h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0418h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0418h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0418h + formula

Figure 9-13. PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-41. PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

Table 9-42. Register Call Summary for PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR0

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR0 Register \(Offset = 00400418h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.14 PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1 Register (Offset = 0040041Ch + formula) [reset = 0h]

PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1 is shown in Figure 9-14 and described in Table 9-44.

Return to the [Summary Table](#).

holds the base address [63:32] of this region.

Offset = 40041Ch + (i * 20h); where i = 0h to 1Fh

Table 9-43.
PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 041Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 041Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 041Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 041Ch + formula

Figure 9-14. PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-44. PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

Table 9-45. Register Call Summary for PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1

PCIE_CORE_AXI Registers	
•	PCIE_CORE_AXI Registers: [0] [1]
•	PCIE_CORE_ATU_HP_WRAPPER_OB_i_AXI_ADDR1 Register (Offset = 0040041Ch + formula) [reset = 0h]: [0]

9.1.15 PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0 Register (Offset = 00400800h + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0 is shown in Figure 9-15 and described in Table 9-47.

Return to the [Summary Table](#).

Provides bits 31:8 of the AXI Address and the number of PCIe address bits passed through

Offset = 400800h + (k * 8h); where k = 0h to 2h

Table 9-46.
PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0800h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0800h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0800h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0800h + formula

Figure 9-15. PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD0		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-47. PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of AXI Address Register for BAR N
7-6	RSVD0	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	The value programmed in this register +1 bits are passed through from PCIe to AXI

Table 9-48. Register Call Summary for PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0

PCIE_CORE_AXI Registers

- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)
- [PCIE_CORE_ATU_WRAPPER_IB_k_ADDR0 Register \(Offset = 00400800h + formula\) \[reset = 0h\]: \[0\]](#)

9.1.16 PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1 Register (Offset = 00400804h + formula) [reset = 0h]

PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1 is shown in Figure 9-16 and described in Table 9-50.

Return to the [Summary Table](#).

Provides bits 63:32 of the AXI Address

Offset = 400804h + (k * 8h); where k = 0h to 2h

Table 9-49.
PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0804h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0804h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0804h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0804h + formula

Figure 9-16. PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-50. PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

Table 9-51. Register Call Summary for PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_WRAPPER_IB_k_ADDR1 Register \(Offset = 00400804h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.17 PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 Register (Offset = 00400820h) [reset = X]

PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 is shown in [Figure 9-17](#) and described in [Table 9-53](#).

Return to the [Summary Table](#).

N/A

Table 9-52.
PCIE_CORE_ATU_CREDIT_THRESHOLD_C0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0820h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0820h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0820h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0820h

Figure 9-17. PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												HEADER						DATA													
R/W-X												R/W-1h						R/W-10h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-53. PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-12	HEADER	R/W	1h	This is the threshold value of the header credits required which is used to flag credit availability in AXI wrapper
11-0	DATA	R/W	10h	This is the threshold value of the payload credits required which is used to flag credit availability in AXI wrapper

Table 9-54. Register Call Summary for PCIE_CORE_ATU_CREDIT_THRESHOLD_C0

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_CREDIT_THRESHOLD_C0 Register \(Offset = 00400820h\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.18 PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 Register (Offset = 00400824h) [reset = X]

PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 is shown in Figure 9-18 and described in Table 9-56.

Return to the [Summary Table](#).

N/A

Table 9-55.
PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0824h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0824h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0824h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0824h

Figure 9-18. PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							CLEAR_LINK_DOWN_BIT_TO_PROCEED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-56. PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	CLEAR_LINK_DOWN_BIT_TO_PROCEED	R/W	0h	This bit will be set when link down reset comes. client should clear this bit before issueing new traffic to the core

Table 9-57. Register Call Summary for PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_LINK_DOWN_INDICATOR_BIT_L0 Register \(Offset = 00400824h\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.19 PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR0 Register (Offset = 00400840h + formula) [reset = 0h]

PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR0 is shown in [Figure 9-19](#) and described in [Table 9-59](#).

Return to the [Summary Table](#).

Provides bits 31:0 of the AXI address

Offset = 400840h + (m * 40h) + (n * 8h); where m = 0 to 15h, n = 0h to 7h

Table 9-58.
PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0840h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0840h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0840h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0840h + formula

Figure 9-19. PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-59. PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

Table 9-60. Register Call Summary for PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR0

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR0 Register \(Offset = 00400840h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.1.20 PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR1 Register (Offset = 00400844h + formula) [reset = 0h]

PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR1 is shown in [Figure 9-20](#) and described in [Table 9-62](#).

Return to the [Summary Table](#).

Provides bits 63:32 of the AXI address

Offset = 400844h + (m * 40h) + (n * 8h); where m = 0 to 15h, n = 0h to 7h

Table 9-61.
PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0844h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0844h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0844h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0844h + formula

Figure 9-20. PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-62. PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

Table 9-63. Register Call Summary for PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR1

PCIE_CORE_AXI Registers

- [PCIE_CORE_ATU_FUNCm_WRAPPER_IB_EP_n_ADDR1 Register \(Offset = 00400844h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_AXI Registers: \[0\] \[1\]](#)

9.2 PCIE_CORE_EP_PF Registers

Table 9-65 lists the PCIE_CORE_EP_PF registers. All register offset addresses not listed in Table 9-65 should be considered as reserved locations and the register contents should not be modified.

EP mode physical function (PF) PCIe core registers. There are 6 Physical Functions, which are assigned to function numbers 0 through 5.

Table 9-64. PCIE_CORE_EP_PF Instances

Instance	Base Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0000h

Table 9-65. PCIE_CORE_EP_PF Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE1_CORE_DBN_CFG_PCIE_CORE Physical Address
0h + formula	PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID		0D00 0000h + formula	0D80 0000h + formula
4h + formula	PCIE_CORE_PFn_I_COMMAND_STATUS		0D00 0004h + formula	0D80 0004h + formula
8h + formula	PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE		0D00 0008h + formula	0D80 0008h + formula
Ch + formula	PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CACHE_LINE		0D00 000Ch + formula	0D80 000Ch + formula
10h + formula	PCIE_CORE_PFn_I_BASE_ADDR_0		0D00 0010h + formula	0D80 0010h + formula
14h + formula	PCIE_CORE_PFn_I_BASE_ADDR_1		0D00 0014h + formula	0D80 0014h + formula
18h + formula	PCIE_CORE_PFn_I_BASE_ADDR_2		0D00 0018h + formula	0D80 0018h + formula
1Ch + formula	PCIE_CORE_PFn_I_BASE_ADDR_3		0D00 001Ch + formula	0D80 001Ch + formula
20h + formula	PCIE_CORE_PFn_I_BASE_ADDR_4		0D00 0020h + formula	0D80 0020h + formula
24h + formula	PCIE_CORE_PFn_I_BASE_ADDR_5		0D00 0024h + formula	0D80 0024h + formula
28h + formula	PCIE_CORE_PFn_RSVD_0A		0D00 0028h + formula	0D80 0028h + formula
2Ch + formula	PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I		0D00 002Ch + formula	0D80 002Ch + formula
30h + formula	PCIE_CORE_PFn_RSVD_0C		0D00 0030h + formula	0D80 0030h + formula
34h + formula	PCIE_CORE_PFn_I_CAPABILITIES_POINTER		0D00 0034h + formula	0D80 0034h + formula
38h + formula	PCIE_CORE_PFn_RSVD_0E		0D00 0038h + formula	0D80 0038h + formula
3Ch + formula	PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN		0D00 003Ch + formula	0D80 003Ch + formula
40h + formula	PCIE_CORE_PFn_RSVD_010_01F		0D00 0040h + formula	0D80 0040h + formula
80h + formula	PCIE_CORE_PFn_I_PWR_MGMT_CAP		0D00 0080h + formula	0D80 0080h + formula
84h + formula	PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP		0D00 0084h + formula	0D80 0084h + formula

Table 9-65. PCIE_CORE_EP_PF Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
88h + formula	PCIE_CORE_PFn_RSVD_022_023		0D00 0088h + formula	0D80 0088h + formula
90h + formula	PCIE_CORE_PFn_I_MSI_CTRL_REG		0D00 0090h + formula	0D80 0090h + formula
94h + formula	PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR		0D00 0094h + formula	0D80 0094h + formula
98h + formula	PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR		0D00 0098h + formula	0D80 0098h + formula
9Ch + formula	PCIE_CORE_PFn_I_MSI_MSG_DATA		0D00 009Ch + formula	0D80 009Ch + formula
A0h + formula	PCIE_CORE_PFn_I_MSI_MASK		0D00 00A0h + formula	0D80 00A0h + formula
A4h + formula	PCIE_CORE_PFn_I_MSI_PENDING_BITS		0D00 00A4h + formula	0D80 00A4h + formula
A8h + formula	PCIE_CORE_PFn_RSVD_02A_02B		0D00 00A8h + formula	0D80 00A8h + formula
B0h + formula	PCIE_CORE_PFn_I_MSIX_CTRL		0D00 00B0h + formula	0D80 00B0h + formula
B4h + formula	PCIE_CORE_PFn_I_MSIX_TBL_OFFSET		0D00 00B4h + formula	0D80 00B4h + formula
B8h + formula	PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT		0D00 00B8h + formula	0D80 00B8h + formula
BCh + formula	PCIE_CORE_PFn_RSVD_02F		0D00 00BCh + formula	0D80 00BCh + formula
C0h + formula	PCIE_CORE_PFn_I_PCIE_CAP_LIST		0D00 00C0h + formula	0D80 00C0h + formula
C4h + formula	PCIE_CORE_PFn_I_PCIE_DEV_CAP		0D00 00C4h + formula	0D80 00C4h + formula
C8h + formula	PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS		0D00 00C8h + formula	0D80 00C8h + formula
CCh + formula	PCIE_CORE_PFn_I_LINK_CAP		0D00 00CCh + formula	0D80 00CCh + formula
D0h + formula	PCIE_CORE_PFn_I_LINK_CTRL_STATUS		0D00 00D0h + formula	0D80 00D0h + formula
D4h + formula	PCIE_CORE_PFn_RSVD_035		0D00 00D4h + formula	0D80 00D4h + formula
D8h + formula	PCIE_CORE_PFn_RSVD_036		0D00 00D8h + formula	0D80 00D8h + formula
DCh + formula	PCIE_CORE_PFn_RSVD_037_038		0D00 00DCh + formula	0D80 00DCh + formula
E4h + formula	PCIE_CORE_PFn_I_PCIE_DEV_CAP_2		0D00 00E4h + formula	0D80 00E4h + formula
E8h + formula	PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2		0D00 00E8h + formula	0D80 00E8h + formula
ECh + formula	PCIE_CORE_PFn_I_LINK_CAP_2_REG		0D00 00ECh + formula	0D80 00ECh + formula
F0h + formula	PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2		0D00 00F0h + formula	0D80 00F0h + formula
F4h + formula	PCIE_CORE_PFn_RSVD_03D_03F		0D00 00F4h + formula	0D80 00F4h + formula
100h + formula	PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR		0D00 0100h + formula	0D80 0100h + formula

Table 9-65. PCIE_CORE_EP_PF Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
104h + formula	PCIE_CORE_PFn_I_UNCORR_ERR_STATUS		0D00 0104h + formula	0D80 0104h + formula
108h + formula	PCIE_CORE_PFn_I_UNCORR_ERR_MASK		0D00 0108h + formula	0D80 0108h + formula
10Ch + formula	PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY		0D00 010Ch + formula	0D80 010Ch + formula
110h + formula	PCIE_CORE_PFn_I_CORR_ERR_STATUS		0D00 0110h + formula	0D80 0110h + formula
114h + formula	PCIE_CORE_PFn_I_CORR_ERR_MASK		0D00 0114h + formula	0D80 0114h + formula
118h + formula	PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL		0D00 0118h + formula	0D80 0118h + formula
11Ch + formula	PCIE_CORE_PFn_I_HDR_LOG_0		0D00 011Ch + formula	0D80 011Ch + formula
120h + formula	PCIE_CORE_PFn_I_HDR_LOG_1		0D00 0120h + formula	0D80 0120h + formula
124h + formula	PCIE_CORE_PFn_I_HDR_LOG_2		0D00 0124h + formula	0D80 0124h + formula
128h + formula	PCIE_CORE_PFn_I_HDR_LOG_3		0D00 0128h + formula	0D80 0128h + formula
12Ch + formula	PCIE_CORE_PFn_RSVD_04B_04D		0D00 012Ch + formula	0D80 012Ch + formula
138h + formula	PCIE_CORE_PFn_I_TLP_PRE_LOG_0		0D00 0138h + formula	0D80 0138h + formula
140h + formula	PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR		0D00 0140h + formula	0D80 0140h + formula
144h + formula	PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL		0D00 0144h + formula	0D80 0144h + formula
148h + formula	PCIE_CORE_PFn_RSVD_052_053		0D00 0148h + formula	0D80 0148h + formula
150h + formula	PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR		0D00 0150h + formula	0D80 0150h + formula
154h + formula	PCIE_CORE_PFn_I_DEV_SER_NUM_0		0D00 0154h + formula	0D80 0154h + formula
158h + formula	PCIE_CORE_PFn_I_DEV_SER_NUM_1		0D00 0158h + formula	0D80 0158h + formula
15Ch + formula	PCIE_CORE_PFn_RSVD_057		0D00 015Ch + formula	0D80 015Ch + formula
160h + formula	PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR		0D00 0160h + formula	0D80 0160h + formula
164h + formula	PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL		0D00 0164h + formula	0D80 0164h + formula
168h + formula	PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER		0D00 0168h + formula	0D80 0168h + formula
16Ch + formula	PCIE_CORE_PFn_I_PWR_BDGT_CAP		0D00 016Ch + formula	0D80 016Ch + formula
170h + formula	PCIE_CORE_PFn_RSVD_05C_05F		0D00 0170h + formula	0D80 0170h + formula
180h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR		0D00 0180h + formula	0D80 0180h + formula
184h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0		0D00 0184h + formula	0D80 0184h + formula

Table 9-65. PCIE_CORE_EP_PF Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
188h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0		0D00 0188h + formula	0D80 0188h + formula
18Ch + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1		0D00 018Ch + formula	0D80 018Ch + formula
190h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1		0D00 0190h + formula	0D80 0190h + formula
194h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2		0D00 0194h + formula	0D80 0194h + formula
198h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2		0D00 0198h + formula	0D80 0198h + formula
19Ch + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3		0D00 019Ch + formula	0D80 019Ch + formula
1A0h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3		0D00 01A0h + formula	0D80 01A0h + formula
1A4h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4		0D00 01A4h + formula	0D80 01A4h + formula
1A8h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4		0D00 01A8h + formula	0D80 01A8h + formula
1ACh + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5		0D00 01ACh + formula	0D80 01ACh + formula
1B0h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5		0D00 01B0h + formula	0D80 01B0h + formula
1B8h	PCIE_CORE_PFn_I_LTR_EXT_CAP_HDR		0D00 01B8h	0D80 01B8h
1BCh	PCIE_CORE_PFn_I_LTR_SNOOP_LAT		0D00 01BCh	0D80 01BCh
1C0h + formula	PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG		0D00 01C0h + formula	0D80 01C0h + formula
1C4h + formula	PCIE_CORE_PFn_I_DPA_CAP_REG		0D00 01C4h + formula	0D80 01C4h + formula
1C8h + formula	PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG		0D00 01C8h + formula	0D80 01C8h + formula
1CCh + formula	PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG		0D00 01CCh + formula	0D80 01CCh + formula
1D0h + formula	PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0		0D00 01D0h + formula	0D80 01D0h + formula
1D4h + formula	PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1		0D00 01D4h + formula	0D80 01D4h + formula
1D8h + formula	PCIE_CORE_PFn_RSVD_07C_07F		0D00 01D8h + formula	0D80 01D8h + formula
200h + formula	PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG		0D00 0200h + formula	0D80 0200h + formula
204h + formula	PCIE_CORE_PFn_I_SRIOV_CAP_REG		0D00 0204h + formula	0D80 0204h + formula
208h + formula	PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG		0D00 0208h + formula	0D80 0208h + formula
20Ch + formula	PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG		0D00 020Ch + formula	0D80 020Ch + formula
210h + formula	PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG		0D00 0210h + formula	0D80 0210h + formula
214h + formula	PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG		0D00 0214h + formula	0D80 0214h + formula
218h + formula	PCIE_CORE_PFn_I_VF_DEVICE_ID_REG		0D00 0218h + formula	0D80 0218h + formula

Table 9-65. PCIE_CORE_EP_PF Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
21Ch + formula	PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG		0D00 021Ch + formula	0D80 021Ch + formula
220h + formula	PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG		0D00 0220h + formula	0D80 0220h + formula
224h + formula	PCIE_CORE_PFn_I_VF_BAR_0_REG		0D00 0224h + formula	0D80 0224h + formula
228h + formula	PCIE_CORE_PFn_I_VF_BAR_1_REG		0D00 0228h + formula	0D80 0228h + formula
22Ch + formula	PCIE_CORE_PFn_I_VF_BAR_2_REG		0D00 022Ch + formula	0D80 022Ch + formula
230h + formula	PCIE_CORE_PFn_I_VF_BAR_3_REG		0D00 0230h + formula	0D80 0230h + formula
234h + formula	PCIE_CORE_PFn_I_VF_BAR_4_REG		0D00 0234h + formula	0D80 0234h + formula
238h + formula	PCIE_CORE_PFn_I_VF_BAR_5_REG		0D00 0238h + formula	0D80 0238h + formula
23Ch + formula	PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFF SET_REG		0D00 023Ch + formula	0D80 023Ch + formula
240h + formula	PCIE_CORE_PFn_RSVD_090_09C		0D00 0240h + formula	0D80 0240h + formula
300h	PCIE_CORE_PFn_I_SEC_PCIE_CAP_HDR_REG		0D00 0300h	0D80 0300h
304h	PCIE_CORE_PFn_I_LINK_CONTROL3_REG		0D00 0304h	0D80 0304h
308h	PCIE_CORE_PFn_I_LANE_ERROR_STATUS_REG		0D00 0308h	0D80 0308h
30Ch	PCIE_CORE_PFn_I_LANE_EQUALIZATION_CONTROL_ REG0		0D00 030Ch	0D80 030Ch
400h + formula	PCIE_CORE_PFn_I_VSEC_HEADER_REG		0D00 0400h + formula	0D80 0400h + formula
404h + formula	PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_RE G		0D00 0404h + formula	0D80 0404h + formula
408h + formula	PCIE_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_R EG		0D00 0408h + formula	0D80 0408h + formula
40Ch + formula	PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0		0D00 040Ch + formula	0D80 040Ch + formula
440h + formula	PCIE_CORE_PFn_I_PASID_HEADER_REG		0D00 0440h + formula	0D80 0440h + formula
444h + formula	PCIE_CORE_PFn_I_PASID_CAP_REG		0D00 0444h + formula	0D80 0444h + formula
4C0h	PCIE_CORE_PFn_I_VC_ENH_CAP_HEADER_REG		0D00 04C0h	0D80 04C0h
4C4h	PCIE_CORE_PFn_I_PORT_VC_CAP_REG_1		0D00 04C4h	0D80 04C4h
4C8h	PCIE_CORE_PFn_I_PORT_VC_CAP_REG_2		0D00 04C8h	0D80 04C8h
4CCh	PCIE_CORE_PFn_I_PORT_VC_CTRL_STS_REG		0D00 04CCh	0D80 04CCh
4D0h	PCIE_CORE_PFn_I_VC_RES_CAP_REG_0		0D00 04D0h	0D80 04D0h
4D4h	PCIE_CORE_PFn_I_VC_RES_CTRL_REG_0		0D00 04D4h	0D80 04D4h
4D8h	PCIE_CORE_PFn_I_VC_RES_STS_REG_0		0D00 04D8h	0D80 04D8h
4DCh	PCIE_CORE_PFn_I_VC_RES_CAP_REG_1		0D00 04DCh	0D80 04DCh
4E0h	PCIE_CORE_PFn_I_VC_RES_CTRL_REG_1		0D00 04E0h	0D80 04E0h
4E4h	PCIE_CORE_PFn_I_VC_RES_STS_REG_1		0D00 04E4h	0D80 04E4h
4E8h	PCIE_CORE_PFn_I_VC_RES_CAP_REG_2		0D00 04E8h	0D80 04E8h
4ECh	PCIE_CORE_PFn_I_VC_RES_CTRL_REG_2		0D00 04ECh	0D80 04ECh
4F0h	PCIE_CORE_PFn_I_VC_RES_STS_REG_2		0D00 04F0h	0D80 04F0h

Table 9-65. PCIE_CORE_EP_PF Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
4F4h	PCIE_CORE_PF0_I_VC_RES_CAP_REG_3		0D00 04F4h	0D80 04F4h
4F8h	PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3		0D00 04F8h	0D80 04F8h
4FCh	PCIE_CORE_PF0_I_VC_RES_STS_REG_3		0D00 04FCh	0D80 04FCh
5C0h + formula	PCIE_CORE_PFn_ATS_CAP_HEADER		0D00 05C0h + formula	0D80 05C0h + formula
5C4h + formula	PCIE_CORE_PFn_ATS_CAP_CONTROL		0D00 05C4h + formula	0D80 05C4h + formula
640h + formula	PCIE_CORE_PFn_ATS_PR_CAP_HEADER		0D00 0640h + formula	0D80 0640h + formula
644h + formula	PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS		0D00 0644h + formula	0D80 0644h + formula
648h + formula	PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY		0D00 0648h + formula	0D80 0648h + formula
64Ch + formula	PCIE_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC		0D00 064Ch + formula	0D80 064Ch + formula
900h	PCIE_CORE_PF0_I_L1_PM_EXT_CAP_HDR		0D00 0900h	0D80 0900h
904h	PCIE_CORE_PF0_I_L1_PM_CAP		0D00 0904h	0D80 0904h
908h	PCIE_CORE_PF0_I_L1_PM_CTRL_1		0D00 0908h	0D80 0908h
90Ch	PCIE_CORE_PF0_I_L1_PM_CTRL_2		0D00 090Ch	0D80 090Ch
910h + formula	PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABI LITY_HEADER_REG		0D00 0910h + formula	0D80 0910h + formula
914h + formula	PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG		0D00 0914h + formula	0D80 0914h + formula
918h + formula	PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG		0D00 0918h + formula	0D80 0918h + formula
920h	PCIE_CORE_PF0_I_MARGINING_EXTENDED_CAPABIL ITY_HEADER_REG		0D00 0920h	0D80 0920h
924h	PCIE_CORE_PF0_I_MARGINING_PORT_CAPABILITIES _STATUS_REG		0D00 0924h	0D80 0924h
928h	PCIE_CORE_PF0_I_MARGINING_LANE_CONTROL_ST ATUS_REG0		0D00 0928h	0D80 0928h
92Ch	PCIE_CORE_PF0_I_MARGINING_LANE_CONTROL_ST ATUS_REG1		0D00 092Ch	0D80 092Ch
9C0h	PCIE_CORE_PF0_I_PL_16GTS_EXTENDED_CAPABILI TY_HEADER_REG		0D00 09C0h	0D80 09C0h
9C4h	PCIE_CORE_PF0_I_PL_16GTS_CAPABILITIES_REG		0D00 09C4h	0D80 09C4h
9C8h	PCIE_CORE_PF0_I_PL_16GTS_CONTROL_REG		0D00 09C8h	0D80 09C8h
9CCh	PCIE_CORE_PF0_I_PL_16GTS_STATUS_REG		0D00 09CCh	0D80 09CCh
9D0h	PCIE_CORE_PF0_I_PL_16GTS_LOCAL_DATA_PARITY_ MISMATCH_STATUS_REG		0D00 09D0h	0D80 09D0h
9D4h	PCIE_CORE_PF0_I_PL_16GTS_FIRST_RETIMER_DATA _PARITY_MISMATCH_STATUS_REG		0D00 09D4h	0D80 09D4h
9D8h	PCIE_CORE_PF0_I_PL_16GTS_SECOND_RETIMER_D ATA_PARITY_MISMATCH_STATUS_REG		0D00 09D8h	0D80 09D8h
9DCh	PCIE_CORE_PF0_I_PL_16GTS_RESERVED_REG		0D00 09DCh	0D80 09DCh
9E0h	PCIE_CORE_PF0_I_PL_16GTS_LANE_EQUALIZATION_ CONTROL_REG0		0D00 09E0h	0D80 09E0h
A20h	PCIE_CORE_PF0_I_PTM_EXTENDED_CAPABILITY_HE ADER_REG		0D00 0A20h	0D80 0A20h
A24h	PCIE_CORE_PF0_I_PTM_CAPABILITIES_REG		0D00 0A24h	0D80 0A24h

Table 9-65. PCIe_CORE_EP_PF Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
A28h	PCIE_CORE_PFn_I_PTM_CONTROL_REG		0D00 0A28h	0D80 0A28h

Table 9-66. PCIe_CORE_EP_PF Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
0h + formula	PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID		0E00 0000h + formula	0E80 0000h + formula
4h + formula	PCIE_CORE_PFn_I_COMMAND_STATUS		0E00 0004h + formula	0E80 0004h + formula
8h + formula	PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE		0E00 0008h + formula	0E80 0008h + formula
Ch + formula	PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CACHE _LINE		0E00 000Ch + formula	0E80 000Ch + formula
10h + formula	PCIE_CORE_PFn_I_BASE_ADDR_0		0E00 0010h + formula	0E80 0010h + formula
14h + formula	PCIE_CORE_PFn_I_BASE_ADDR_1		0E00 0014h + formula	0E80 0014h + formula
18h + formula	PCIE_CORE_PFn_I_BASE_ADDR_2		0E00 0018h + formula	0E80 0018h + formula
1Ch + formula	PCIE_CORE_PFn_I_BASE_ADDR_3		0E00 001Ch + formula	0E80 001Ch + formula
20h + formula	PCIE_CORE_PFn_I_BASE_ADDR_4		0E00 0020h + formula	0E80 0020h + formula
24h + formula	PCIE_CORE_PFn_I_BASE_ADDR_5		0E00 0024h + formula	0E80 0024h + formula
28h + formula	PCIE_CORE_PFn_RSVD_0A		0E00 0028h + formula	0E80 0028h + formula
2Ch + formula	PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSY STEM_I		0E00 002Ch + formula	0E80 002Ch + formula
30h + formula	PCIE_CORE_PFn_RSVD_0C		0E00 0030h + formula	0E80 0030h + formula
34h + formula	PCIE_CORE_PFn_I_CAPABILITIES_POINTER		0E00 0034h + formula	0E80 0034h + formula
38h + formula	PCIE_CORE_PFn_RSVD_0E		0E00 0038h + formula	0E80 0038h + formula
3Ch + formula	PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN		0E00 003Ch + formula	0E80 003Ch + formula
40h + formula	PCIE_CORE_PFn_RSVD_010_01F		0E00 0040h + formula	0E80 0040h + formula
80h + formula	PCIE_CORE_PFn_I_PWR_MGMT_CAP		0E00 0080h + formula	0E80 0080h + formula
84h + formula	PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP		0E00 0084h + formula	0E80 0084h + formula
88h + formula	PCIE_CORE_PFn_RSVD_022_023		0E00 0088h + formula	0E80 0088h + formula
90h + formula	PCIE_CORE_PFn_I_MSI_CTRL_REG		0E00 0090h + formula	0E80 0090h + formula
94h + formula	PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR		0E00 0094h + formula	0E80 0094h + formula
98h + formula	PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR		0E00 0098h + formula	0E80 0098h + formula

Table 9-66. PCIE_CORE_EP_PF Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
9Ch + formula	PCIE_CORE_PFn_I_MSI_MSG_DATA		0E00 009Ch + formula	0E80 009Ch + formula
A0h + formula	PCIE_CORE_PFn_I_MSI_MASK		0E00 00A0h + formula	0E80 00A0h + formula
A4h + formula	PCIE_CORE_PFn_I_MSI_PENDING_BITS		0E00 00A4h + formula	0E80 00A4h + formula
A8h + formula	PCIE_CORE_PFn_RSVD_02A_02B		0E00 00A8h + formula	0E80 00A8h + formula
B0h + formula	PCIE_CORE_PFn_I_MSIX_CTRL		0E00 00B0h + formula	0E80 00B0h + formula
B4h + formula	PCIE_CORE_PFn_I_MSIX_TBL_OFFSET		0E00 00B4h + formula	0E80 00B4h + formula
B8h + formula	PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT		0E00 00B8h + formula	0E80 00B8h + formula
BCh + formula	PCIE_CORE_PFn_RSVD_02F		0E00 00BCh + formula	0E80 00BCh + formula
C0h + formula	PCIE_CORE_PFn_I_PCIE_CAP_LIST		0E00 00C0h + formula	0E80 00C0h + formula
C4h + formula	PCIE_CORE_PFn_I_PCIE_DEV_CAP		0E00 00C4h + formula	0E80 00C4h + formula
C8h + formula	PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS		0E00 00C8h + formula	0E80 00C8h + formula
CCh + formula	PCIE_CORE_PFn_I_LINK_CAP		0E00 00CCh + formula	0E80 00CCh + formula
D0h + formula	PCIE_CORE_PFn_I_LINK_CTRL_STATUS		0E00 00D0h + formula	0E80 00D0h + formula
D4h + formula	PCIE_CORE_PFn_RSVD_035		0E00 00D4h + formula	0E80 00D4h + formula
D8h + formula	PCIE_CORE_PFn_RSVD_036		0E00 00D8h + formula	0E80 00D8h + formula
DCh + formula	PCIE_CORE_PFn_RSVD_037_038		0E00 00DCh + formula	0E80 00DCh + formula
E4h + formula	PCIE_CORE_PFn_I_PCIE_DEV_CAP_2		0E00 00E4h + formula	0E80 00E4h + formula
E8h + formula	PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2		0E00 00E8h + formula	0E80 00E8h + formula
ECh + formula	PCIE_CORE_PFn_I_LINK_CAP_2_REG		0E00 00ECh + formula	0E80 00ECh + formula
F0h + formula	PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2		0E00 00F0h + formula	0E80 00F0h + formula
F4h + formula	PCIE_CORE_PFn_RSVD_03D_03F		0E00 00F4h + formula	0E80 00F4h + formula
100h + formula	PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR		0E00 0100h + formula	0E80 0100h + formula
104h + formula	PCIE_CORE_PFn_I_UNCORR_ERR_STATUS		0E00 0104h + formula	0E80 0104h + formula
108h + formula	PCIE_CORE_PFn_I_UNCORR_ERR_MASK		0E00 0108h + formula	0E80 0108h + formula
10Ch + formula	PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY		0E00 010Ch + formula	0E80 010Ch + formula
110h + formula	PCIE_CORE_PFn_I_CORR_ERR_STATUS		0E00 0110h + formula	0E80 0110h + formula

Table 9-66. PCIE_CORE_EP_PF Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
114h + formula	PCIE_CORE_PFn_I_CORR_ERR_MASK		0E00 0114h + formula	0E80 0114h + formula
118h + formula	PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL		0E00 0118h + formula	0E80 0118h + formula
11Ch + formula	PCIE_CORE_PFn_I_HDR_LOG_0		0E00 011Ch + formula	0E80 011Ch + formula
120h + formula	PCIE_CORE_PFn_I_HDR_LOG_1		0E00 0120h + formula	0E80 0120h + formula
124h + formula	PCIE_CORE_PFn_I_HDR_LOG_2		0E00 0124h + formula	0E80 0124h + formula
128h + formula	PCIE_CORE_PFn_I_HDR_LOG_3		0E00 0128h + formula	0E80 0128h + formula
12Ch + formula	PCIE_CORE_PFn_RSVD_04B_04D		0E00 012Ch + formula	0E80 012Ch + formula
138h + formula	PCIE_CORE_PFn_I_TLP_PRE_LOG_0		0E00 0138h + formula	0E80 0138h + formula
140h + formula	PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR		0E00 0140h + formula	0E80 0140h + formula
144h + formula	PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL		0E00 0144h + formula	0E80 0144h + formula
148h + formula	PCIE_CORE_PFn_RSVD_052_053		0E00 0148h + formula	0E80 0148h + formula
150h + formula	PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR		0E00 0150h + formula	0E80 0150h + formula
154h + formula	PCIE_CORE_PFn_I_DEV_SER_NUM_0		0E00 0154h + formula	0E80 0154h + formula
158h + formula	PCIE_CORE_PFn_I_DEV_SER_NUM_1		0E00 0158h + formula	0E80 0158h + formula
15Ch + formula	PCIE_CORE_PFn_RSVD_057		0E00 015Ch + formula	0E80 015Ch + formula
160h + formula	PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR		0E00 0160h + formula	0E80 0160h + formula
164h + formula	PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL		0E00 0164h + formula	0E80 0164h + formula
168h + formula	PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER		0E00 0168h + formula	0E80 0168h + formula
16Ch + formula	PCIE_CORE_PFn_I_PWR_BDGT_CAP		0E00 016Ch + formula	0E80 016Ch + formula
170h + formula	PCIE_CORE_PFn_RSVD_05C_05F		0E00 0170h + formula	0E80 0170h + formula
180h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR		0E00 0180h + formula	0E80 0180h + formula
184h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0		0E00 0184h + formula	0E80 0184h + formula
188h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0		0E00 0188h + formula	0E80 0188h + formula
18Ch + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1		0E00 018Ch + formula	0E80 018Ch + formula
190h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1		0E00 0190h + formula	0E80 0190h + formula
194h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2		0E00 0194h + formula	0E80 0194h + formula

Table 9-66. PCIE_CORE_EP_PF Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
198h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2		0E00 0198h + formula	0E80 0198h + formula
19Ch + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3		0E00 019Ch + formula	0E80 019Ch + formula
1A0h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3		0E00 01A0h + formula	0E80 01A0h + formula
1A4h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4		0E00 01A4h + formula	0E80 01A4h + formula
1A8h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4		0E00 01A8h + formula	0E80 01A8h + formula
1ACh + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5		0E00 01ACh + formula	0E80 01ACh + formula
1B0h + formula	PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5		0E00 01B0h + formula	0E80 01B0h + formula
1B8h	PCIE_CORE_PFn_I_LTR_EXT_CAP_HDR		0E00 01B8h	0E80 01B8h
1BCh	PCIE_CORE_PFn_I_LTR_SNOOP_LAT		0E00 01BCh	0E80 01BCh
1C0h + formula	PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG		0E00 01C0h + formula	0E80 01C0h + formula
1C4h + formula	PCIE_CORE_PFn_I_DPA_CAP_REG		0E00 01C4h + formula	0E80 01C4h + formula
1C8h + formula	PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG		0E00 01C8h + formula	0E80 01C8h + formula
1CCh + formula	PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG		0E00 01CCh + formula	0E80 01CCh + formula
1D0h + formula	PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0		0E00 01D0h + formula	0E80 01D0h + formula
1D4h + formula	PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1		0E00 01D4h + formula	0E80 01D4h + formula
1D8h + formula	PCIE_CORE_PFn_RSVD_07C_07F		0E00 01D8h + formula	0E80 01D8h + formula
200h + formula	PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG		0E00 0200h + formula	0E80 0200h + formula
204h + formula	PCIE_CORE_PFn_I_SRIOV_CAP_REG		0E00 0204h + formula	0E80 0204h + formula
208h + formula	PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG		0E00 0208h + formula	0E80 0208h + formula
20Ch + formula	PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG		0E00 020Ch + formula	0E80 020Ch + formula
210h + formula	PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG		0E00 0210h + formula	0E80 0210h + formula
214h + formula	PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG		0E00 0214h + formula	0E80 0214h + formula
218h + formula	PCIE_CORE_PFn_I_VF_DEVICE_ID_REG		0E00 0218h + formula	0E80 0218h + formula
21Ch + formula	PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG		0E00 021Ch + formula	0E80 021Ch + formula
220h + formula	PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG		0E00 0220h + formula	0E80 0220h + formula
224h + formula	PCIE_CORE_PFn_I_VF_BAR_0_REG		0E00 0224h + formula	0E80 0224h + formula
228h + formula	PCIE_CORE_PFn_I_VF_BAR_1_REG		0E00 0228h + formula	0E80 0228h + formula

Table 9-66. PCIE_CORE_EP_PF Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
22Ch + formula	PCIE_CORE_PFn_I_VF_BAR_2_REG		0E00 022Ch + formula	0E80 022Ch + formula
230h + formula	PCIE_CORE_PFn_I_VF_BAR_3_REG		0E00 0230h + formula	0E80 0230h + formula
234h + formula	PCIE_CORE_PFn_I_VF_BAR_4_REG		0E00 0234h + formula	0E80 0234h + formula
238h + formula	PCIE_CORE_PFn_I_VF_BAR_5_REG		0E00 0238h + formula	0E80 0238h + formula
23Ch + formula	PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFF SET_REG		0E00 023Ch + formula	0E80 023Ch + formula
240h + formula	PCIE_CORE_PFn_RSVD_090_09C		0E00 0240h + formula	0E80 0240h + formula
300h	PCIE_CORE_PFO_I_SEC_PCIE_CAP_HDR_REG		0E00 0300h	0E80 0300h
304h	PCIE_CORE_PFO_I_LINK_CONTROL3_REG		0E00 0304h	0E80 0304h
308h	PCIE_CORE_PFO_I_LANE_ERROR_STATUS_REG		0E00 0308h	0E80 0308h
30Ch	PCIE_CORE_PFO_I_LANE_EQUALIZATION_CONTROL_ REG0		0E00 030Ch	0E80 030Ch
400h + formula	PCIE_CORE_PFn_I_VSEC_HEADER_REG		0E00 0400h + formula	0E80 0400h + formula
404h + formula	PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_RE G		0E00 0404h + formula	0E80 0404h + formula
408h + formula	PCIE_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_R EG		0E00 0408h + formula	0E80 0408h + formula
40Ch + formula	PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0		0E00 040Ch + formula	0E80 040Ch + formula
440h + formula	PCIE_CORE_PFn_I_PASID_HEADER_REG		0E00 0440h + formula	0E80 0440h + formula
444h + formula	PCIE_CORE_PFn_I_PASID_CAP_REG		0E00 0444h + formula	0E80 0444h + formula
4C0h	PCIE_CORE_PFO_I_VC_ENH_CAP_HEADER_REG		0E00 04C0h	0E80 04C0h
4C4h	PCIE_CORE_PFO_I_PORT_VC_CAP_REG_1		0E00 04C4h	0E80 04C4h
4C8h	PCIE_CORE_PFO_I_PORT_VC_CAP_REG_2		0E00 04C8h	0E80 04C8h
4CCh	PCIE_CORE_PFO_I_PORT_VC_CTRL_STS_REG		0E00 04CCh	0E80 04CCh
4D0h	PCIE_CORE_PFO_I_VC_RES_CAP_REG_0		0E00 04D0h	0E80 04D0h
4D4h	PCIE_CORE_PFO_I_VC_RES_CTRL_REG_0		0E00 04D4h	0E80 04D4h
4D8h	PCIE_CORE_PFO_I_VC_RES_STS_REG_0		0E00 04D8h	0E80 04D8h
4DCh	PCIE_CORE_PFO_I_VC_RES_CAP_REG_1		0E00 04DCh	0E80 04DCh
4E0h	PCIE_CORE_PFO_I_VC_RES_CTRL_REG_1		0E00 04E0h	0E80 04E0h
4E4h	PCIE_CORE_PFO_I_VC_RES_STS_REG_1		0E00 04E4h	0E80 04E4h
4E8h	PCIE_CORE_PFO_I_VC_RES_CAP_REG_2		0E00 04E8h	0E80 04E8h
4ECh	PCIE_CORE_PFO_I_VC_RES_CTRL_REG_2		0E00 04ECh	0E80 04ECh
4F0h	PCIE_CORE_PFO_I_VC_RES_STS_REG_2		0E00 04F0h	0E80 04F0h
4F4h	PCIE_CORE_PFO_I_VC_RES_CAP_REG_3		0E00 04F4h	0E80 04F4h
4F8h	PCIE_CORE_PFO_I_VC_RES_CTRL_REG_3		0E00 04F8h	0E80 04F8h
4FCh	PCIE_CORE_PFO_I_VC_RES_STS_REG_3		0E00 04FCh	0E80 04FCh
5C0h + formula	PCIE_CORE_PFn_ATS_CAP_HEADER		0E00 05C0h + formula	0E80 05C0h + formula
5C4h + formula	PCIE_CORE_PFn_ATS_CAP_CONTROL		0E00 05C4h + formula	0E80 05C4h + formula

Table 9-66. PCIE_CORE_EP_PF Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
640h + formula	PCIE_CORE_PFn_ATS_PR_CAP_HEADER		0E00 0640h + formula	0E80 0640h + formula
644h + formula	PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS		0E00 0644h + formula	0E80 0644h + formula
648h + formula	PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY		0E00 0648h + formula	0E80 0648h + formula
64Ch + formula	PCIE_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC		0E00 064Ch + formula	0E80 064Ch + formula
900h	PCIE_CORE_PFO_I_L1_PM_EXT_CAP_HDR		0E00 0900h	0E80 0900h
904h	PCIE_CORE_PFO_I_L1_PM_CAP		0E00 0904h	0E80 0904h
908h	PCIE_CORE_PFO_I_L1_PM_CTRL_1		0E00 0908h	0E80 0908h
90Ch	PCIE_CORE_PFO_I_L1_PM_CTRL_2		0E00 090Ch	0E80 090Ch
910h + formula	PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABI LITY_HEADER_REG		0E00 0910h + formula	0E80 0910h + formula
914h + formula	PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG		0E00 0914h + formula	0E80 0914h + formula
918h + formula	PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG		0E00 0918h + formula	0E80 0918h + formula
920h	PCIE_CORE_PFO_I_MARGINING_EXTENDED_CAPABIL ITY_HEADER_REG		0E00 0920h	0E80 0920h
924h	PCIE_CORE_PFO_I_MARGINING_PORT_CAPABILITIES _STATUS_REG		0E00 0924h	0E80 0924h
928h	PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_ST ATUS_REG0		0E00 0928h	0E80 0928h
92Ch	PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_ST ATUS_REG1		0E00 092Ch	0E80 092Ch
9C0h	PCIE_CORE_PFO_I_PL_16GTS_EXTENDED_CAPABILIT Y_HEADER_REG		0E00 09C0h	0E80 09C0h
9C4h	PCIE_CORE_PFO_I_PL_16GTS_CAPABILITIES_REG		0E00 09C4h	0E80 09C4h
9C8h	PCIE_CORE_PFO_I_PL_16GTS_CONTROL_REG		0E00 09C8h	0E80 09C8h
9CCh	PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG		0E00 09CCh	0E80 09CCh
9D0h	PCIE_CORE_PFO_I_PL_16GTS_LOCAL_DATA_PARITY_ MISMATCH_STATUS_REG		0E00 09D0h	0E80 09D0h
9D4h	PCIE_CORE_PFO_I_PL_16GTS_FIRST_RETIMER_DATA _PARITY_MISMATCH_STATUS_REG		0E00 09D4h	0E80 09D4h
9D8h	PCIE_CORE_PFO_I_PL_16GTS_SECOND_RETIMER_D ATA_PARITY_MISMATCH_STATUS_REG		0E00 09D8h	0E80 09D8h
9DCh	PCIE_CORE_PFO_I_PL_16GTS_RESERVED_REG		0E00 09DCh	0E80 09DCh
9E0h	PCIE_CORE_PFO_I_PL_16GTS_LANE_EQUALIZATION_ CONTROL_REG0		0E00 09E0h	0E80 09E0h
A20h	PCIE_CORE_PFO_I_PTM_EXTENDED_CAPABILITY_HE ADER_REG		0E00 0A20h	0E80 0A20h
A24h	PCIE_CORE_PFO_I_PTM_CAPABILITIES_REG		0E00 0A24h	0E80 0A24h
A28h	PCIE_CORE_PFO_I_PTM_CONTROL_REG		0E00 0A28h	0E80 0A28h

9.2.1 PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID Register (Offset = 0h + formula) [reset = 010017CDh]

PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID is shown in [Figure 9-21](#) and described in [Table 9-68](#).

Return to the [Summary Table](#).

16-bit Vendor ID register and 16-bit Device ID register.

Offset = 0h + (n * 1000h); where n = 0h to 5h

Table 9-67.
PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0000h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0000h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0000h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0000h + formula

Figure 9-21. PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DID																VID															
R/W-100h																R-17CDh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-68. PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DID	R/W	100h	Device ID assigned by the manufacturer of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be rewritten independently for each Function from the local management bus.
15-0	VID	R	17CDh	This is the Vendor ID assigned by PCI SIG to the manufacturer of the device. The Vendor ID is set in the Vendor ID Register within the local management register block.

Table 9-69. Register Call Summary for PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VENDOR_ID_DEVICE_ID Register \(Offset = 0h + formula\) \[reset = 010017CDh\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.2 PCIE_CORE_PFn_I_COMMAND_STATUS Register (Offset = 4h + formula) [reset = 00100000h]

PCIE_CORE_PFn_I_COMMAND_STATUS is shown in Figure 9-22 and described in Table 9-71.

Return to the [Summary Table](#).

16-bit Command Register and 16-bit Status Register.

Offset = 4h + (n * 1000h); where n = 0h to 5h

**Table 9-70. PCIE_CORE_PFn_I_COMMAND_STATUS
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0004h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0004h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0004h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0004h + formula

Figure 9-22. PCIE_CORE_PFn_I_COMMAND_STATUS Register

31	30	29	28	27	26	25	24
DPE	SSE	RMA	RTA	STA	R6	MDPE	
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	
23	22	21	20	19	18	17	16
R5			CL	IS	R4		
R-0h			R-1h	R-0h	R-0h		
15	14	13	12	11	10	9	8
R3					IMD	R2	SE
R-0h					R/W-0h	R-0h	R/W-0h
7	6	5	4	3	2	1	0
R1	PERE	R0			BE	MSE	ISE
R-0h	R/W-0h	R-0h			R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-71. PCIE_CORE_PFn_I_COMMAND_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DPE	R/W1C	0h	This bit is set when the Controller has received a poisoned TLP. The Parity Error Response enable bit [bit 6] has no effect on the setting of this bit. This field can also be cleared from the local management bus by writing a 1 into this bit position.
30	SSE	R/W1C	0h	If the SERR enable bit is 1, this bit is set when the Controller has sent out a fatal or non-fatal error message on the link to the Root Complex. If the SERR enable bit is 0, this bit remains 0. This field can also be cleared from the local management bus by writing a 1 into this bit position.
29	RMA	R/W1C	0h	This bit is set when the Controller has received a completion from the link with the Unsupported Request status. This field can also be cleared from the local management bus by writing a 1 into this bit position

Table 9-71. PCIE_CORE_PFn_I_COMMAND_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	RTA	R/W1C	0h	This bit is set when the Controller has received a completion from the link with the Completer Abort status. This field can also be cleared from the local management bus by writing a 1 into this bit position
27	STA	R/W1C	0h	This bit is set when the Controller has sent a completion to the link with the Completer Abort status. This field can also be cleared from the local management bus by writing a 1 into this bit position.
26-25	R6	R	0h	Reserved
24	MDPE	R/W1C	0h	When the Parity Error Response enable bit is 1, the Controller sets this bit when it detects the following error conditions: [i] The Controller receives a poisoned completion from the link in response to a request. [ii] The Controller sends out a poisoned write request on the link [this may be because an underflow occurred during the packet transfer at the host interface of the Controller.]. This bit remains 0 when the Parity Error Response enable bit is 0. This field can also be cleared from the local management bus by writing a 1 into this bit position.
23-21	R5	R	0h	Reserved
20	CL	R	1h	Indicates the presence of PCI Extended Capabilities registers. This bit is hardwired to 1.
19	IS	R	0h	This bit is valid only when the Controller is configured to support legacy interrupts. Indicates that the Controller has a pending interrupt, that is, the Controller has sent an Assert_INTx message but has not transmitted a corresponding Deassert_INTx message.
18-16	R4	R	0h	Reserved
15-11	R3	R	0h	Reserved
10	IMD	R/W	0h	Enables or disables the transmission of INTx Assert and De-assert messages from the Controller. Setting this bit to 1 disables generation of INTx assert/de-assert messages in the Controller. This field can be written from the local management bus.
9	R2	R	0h	Reserved
8	SE	R/W	0h	Enables the reporting of fatal and non-fatal errors detected by the Controller to the Root Complex. This field can be written from the local management bus.
7	R1	R	0h	Reserved
6	PERE	R/W	0h	When this bit is 1, the Controller sets the Master Data Parity Error status bit when it detects the following error conditions: [i] The Controller receives a poisoned completion from the link in response to a request. [ii] The Controller sends out a poisoned write request on the link [this may be because an underflow occurred during the packet transfer at the host interface of the Controller.]. When this bit is 0, the Master Data Parity Error status bit is never set. This field can be written from the local management bus.

Table 9-71. PCIE_CORE_PFn_I_COMMAND_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	R0	R	0h	Reserved
2	BE	R/W	0h	Controls the ability of a Function to issue Memory and I/O Read/Write Requests, in the Upstream direction. This field can be written from the local management bus. Note: The Controller does not gate any requests based on this bit. The Client Application logic must use this bit to gate requests as follows: - When this bit is Set, the Function is allowed to issue Memory or I/O Requests on the pcie_master_AXI interface. - When this bit is Clear, the Function must not allowed to issue any Memory or I/O Requests on the pcie_master_AXI interface.
1	MSE	R/W	0h	Controls a Function's response to Memory Space accesses received from PCIe Link. The Controller internally uses this bit to respond to received Memort Requests as follows: - When this bit is Clear, all received Memory Space accesses are handled as Unsupported Requests. - When this bit is Set, all received Memory Space accesses are decoded and processed normally. This field can be written from the local management bus.
0	ISE	R/W	0h	Controls a Function's response to IO Space accesses received from PCIe Link. The Controller internally uses this bit to respond to received IO Requests as follows: - When this bit is Clear, all received IO Space accesses are handled as Unsupported Requests. - When this bit is Set, all received IO Space accesses are decoded and processed normally. This field can be written from the local management bus.

Table 9-72. Register Call Summary for PCIE_CORE_PFn_I_COMMAND_STATUS

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_COMMAND_STATUS Register \(Offset = 4h + formula\) \[reset = 00100000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.3 PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE Register (Offset = 8h + formula) [reset = 0h]

PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE is shown in Figure 9-23 and described in Table 9-74.

Return to the [Summary Table](#).

This register contains the Revision ID and Class Code associated with the device incorporating the PCIe Controller.

Offset = 8h + (n * 1000h); where n = 0h to 5h

Table 9-73.
PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0008h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0008h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0008h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0008h + formula

Figure 9-23. PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC								SCC								PIB								RID							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-74. PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CC	R/W	0h	Identifies the function of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be rewritten independently for each Function from the local management bus
23-16	SCC	R/W	0h	Identifies a sub-category within the selected function. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be re-written independently for each Function from the local management bus.
15-8	PIB	R/W	0h	Identifies the register set layout of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be re-written independently for each Function from the local management bus.
7-0	RID	R/W	0h	Assigned by the manufacturer of the device to identify the revision number of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be re-written independently for each Function from the local management bus.

Table 9-75. Register Call Summary for PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_REVISION_ID_CLASS_CODE Register \(Offset = 8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.4 PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CACHE_LINE Register (Offset = Ch + formula) [reset = 00800000h]

PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CACHE_LINE is shown in Figure 9-24 and described in Table 9-77.

Return to the [Summary Table](#).

This location contains the BIST, header-type, Latency Timer and Cache Line Size Registers.

Offset = Ch + (n * 1000h); where n = 0h to 5h

Table 9-76.
PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CAC
HE_LINE Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 000Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 000Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 000Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 000Ch + formula

Figure 9-24. PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CACHE_LINE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BR								DT	HT						
R/W-0h								R-1h		R-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LT								CLS							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-77. PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CACHE_LINE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BR	R/W	0h	BIST control register. It can be accessed using local management bus. This is a sticky field.
23	DT	R	1h	Identifies whether the device supports a single Function or multiple Functions. This bit is read as 0 when only Function 0 has been enabled in the Physical Function Configuration Register [in the local management block], and as 1 when more than one Function has been enabled.
22-16	HT	R	0h	Identifies format of header. This field is hardwired to 0.
15-8	LT	R	0h	This is an unused field and is hardwired to 0.
7-0	CLS	R/W	0h	Cache Line Size Register defined in PCI Specifications 3.0. This field can be read or written, both from the link and from the local management bus, but its value is not used.

Table 9-78. Register Call Summary for PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CACHE_LINE

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_BIST_HEADER_LATENCY_CACHE_LINE Register \(Offset = Ch + formula\) \[reset = 00800000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.5 PCIE_CORE_PFn_I_BASE_ADDR_0 Register (Offset = 10h + formula) [reset = 0h]

PCIE_CORE_PFn_I_BASE_ADDR_0 is shown in Figure 9-25 and described in Table 9-80.

Return to the [Summary Table](#).

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. These registers are used to define address ranges for memory and I/O accesses to the Endpoint device. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1s into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if BAR 0 is not configured. Otherwise, the number of 1s returned is based on the size of the BAR. BAR0 can be setup as 32-bit memory or IO BAR, or can be paired with BAR 1 to form a 64bit memory BAR. The settings of this BAR is defined in the BAR Configuration Register associated with this PF.

The BAR aperture can be controller in two different ways:

- (i) When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register 1.
- (ii) When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the PF BAR Configuration Register.

Offset = 10h + (n * 1000h); where n = 0h to 5h

**Table 9-79. PCIE_CORE_PFn_I_BASE_ADDR_0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0010h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0010h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0010h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0010h + formula

Figure 9-25. PCIE_CORE_PFn_I_BASE_ADDR_0 Register

31	30	29	28	27	26	25	24
BAMRW							
R/W-0h							
23	22	21	20	19	18	17	16
BAMRW							
R/W-0h							
15	14	13	12	11	10	9	8
BAMRW				BAMR0			
R/W-0h				R-0h			
7	6	5	4	3	2	1	0
R8				P0	S0	R7	MSI0
R-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-80. PCIE_CORE_PFn_I_BASE_ADDR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	BAMRW	R/W	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in BAR Configuration Registers of the associated Physical Function.
11-8	BAMR0	R	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in BAR Configuration Registers of the associated Physical Function. All other bits are not writeable, and are read as 0's.
7-4	R8	R	0h	These bits are hardwired to 0
3	P0	R	0h	When the BAR is used to define a memory address range, this field declares whether data from the address range is prefetchable [0 = non-prefetchable, 1 = prefetchable]. The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function
2	S0	R	0h	When the BAR is used to define a memory address range, this field indicates whether the address range is 32-bit or 64-bit [0 = 32-bit, 1 = 64 bit]. For 64-bit address ranges, the value in BAR 1 is treated as a continuation of the base address in BAR 0. The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function.
1	R7	R	0h	This bit is hardwired to 0 for both memory and I/O BARs.
0	MSI0	R	0h	Specifies whether this BAR defines a memory address range or an I/O address range [0 = memory, 1 = I/O]. The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function

Table 9-81. Register Call Summary for PCIE_CORE_PFn_I_BASE_ADDR_0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_BASE_ADDR_0 Register \(Offset = 10h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.6 PCIE_CORE_PFn_I_BASE_ADDR_1 Register (Offset = 14h + formula) [reset = 0h]

PCIE_CORE_PFn_I_BASE_ADDR_1 is shown in Figure 9-26 and described in Table 9-83.

Return to the [Summary Table](#).

This is one of the six Base Address Registers defined by the PCI

Specifications 3.0. BAR1 can be setup as 32-bit memory or IO BAR, or

can be paired with BAR 0 to form a 64bit memory BAR.

This register can be used in two distinct ways: (i) When BAR 0 defines a 64-bit memory address range, this register is used to define the high-order bits of the base address. The number of writable bits

in this field is based on the aperture setting of the BAR. (ii) When the BAR 0 is

used to define a 32-bit memory address range or an I/O address range, this register can be used

to define a new 32-bit memory address range or an I/O address range. The individual fields in

the register have the same format as those of BAR 0 and is described below. The settings of this BAR

is defined in the BAR Configuration Register associated with this PF.

When configured as a 32-bit memory or IO BAR, the BAR aperture can be controller in two different ways:

(a) When the Resizable BAR Capability is enabled, the aperture is

controlled by the setting of the BAR width field in Resizable BAR Control Register 1.

The Resizable BAR Capability is enabled by setting the Enable Resizable BAR

Capability bit (bit 31) of the associated Physical Function BAR Configuration Register.

(b) When the Resizable BAR Capability is disabled for the Physical

Function, the aperture is controlled by the setting of the Physical Function BAR

Configuration Register.

Offset = 14h + (n * 1000h); where n = 0h to 5h

**Table 9-82. PCIE_CORE_PFn_I_BASE_ADDR_1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0014h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0014h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0014h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0014h + formula

Figure 9-26. PCIE_CORE_PFn_I_BASE_ADDR_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-83. PCIE_CORE_PFn_I_BASE_ADDR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration regisiter in LM space.

Table 9-84. Register Call Summary for PCIE_CORE_PFn_I_BASE_ADDR_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_BASE_ADDR_1 Register \(Offset = 14h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.7 PCIE_CORE_PFn_I_BASE_ADDR_2 Register (Offset = 18h + formula) [reset = 0h]

PCIE_CORE_PFn_I_BASE_ADDR_2 is shown in Figure 9-27 and described in Table 9-86.

Return to the [Summary Table](#).

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. These registers are used to define address ranges for memory and I/O accesses to the Endpoint device. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1s into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if BAR 2 is not configured. Otherwise, the number of 1s returned is based on the size of the BAR. BAR2 can be setup as 32-bit memory or IO BAR, or can be paired with BAR 3 to form a 64bit memory BAR. The settings of this BAR is defined in the BAR Configuration Register associated with this PF.

The BAR aperture can be controller in two different ways:

- (i) When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register 1.
- (ii) When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the PF BAR Configuration Register.

Offset = 18h + (n * 1000h); where n = 0h to 5h

Table 9-85. PCIE_CORE_PFn_I_BASE_ADDR_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0018h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0018h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0018h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0018h + formula

Figure 9-27. PCIE_CORE_PFn_I_BASE_ADDR_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-86. PCIE_CORE_PFn_I_BASE_ADDR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration regisiter in LM space.

Table 9-87. Register Call Summary for PCIE_CORE_PFn_I_BASE_ADDR_2

PCIE_CORE_EP_PF Registers
<ul style="list-style-type: none"> PCIE_CORE_EP_PF Registers: [0] [1] PCIE_CORE_PFn_I_BASE_ADDR_2 Register (Offset = 18h + formula) [reset = 0h]: [0]

9.2.8 PCIE_CORE_PFn_I_BASE_ADDR_3 Register (Offset = 1Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_BASE_ADDR_3 is shown in Figure 9-28 and described in Table 9-89.

Return to the [Summary Table](#).

This is one of the six Base Address Registers defined by the PCI

Specifications 3.0. BAR3 can be setup as 32-bit memory or IO BAR, or

can be paired with BAR 2 to form a 64bit memory BAR.

This register can be used in two distinct ways: (i) When BAR 2 defines a 64-bit memory address range, this register is used to define the high-order bits of the base address. The number of writable bits

in this field is based on the aperture setting of the BAR. (ii) When the BAR 2 is

used to define a 32-bit memory address range or an I/O address range, this register can be used

to define a new 32-bit memory address range or an I/O address range. The individual fields in

the register have the same format as those of BAR 2 and is described below. The settings of this BAR

is defined in the BAR Configuration Register associated with this PF.

When configured as a 32-bit memory or IO BAR, the BAR aperture can be controller in two different ways:

(a) When the Resizable BAR Capability is enabled, the aperture is

controlled by the setting of the BAR width field in Resizable BAR Control Register 3.

The Resizable BAR Capability is enabled by setting the Enable Resizable BAR

Capability bit (bit 31) of the associated Physical Function BAR Configuration Register.

(b) When the Resizable BAR Capability is disabled for the Physical

Function, the aperture is controlled by the setting of the Physical Function BAR

Configuration Register.

Offset = 1Ch + (n * 1000h); where n = 0h to 5h

**Table 9-88. PCIE_CORE_PFn_I_BASE_ADDR_3
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 001Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 001Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 001Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 001Ch + formula

Figure 9-28. PCIE_CORE_PFn_I_BASE_ADDR_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-89. PCIE_CORE_PFn_I_BASE_ADDR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration regisiter in LM space.

Table 9-90. Register Call Summary for PCIE_CORE_PFn_I_BASE_ADDR_3

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_BASE_ADDR_3 Register \(Offset = 1Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.9 PCIE_CORE_PFn_I_BASE_ADDR_4 Register (Offset = 20h + formula) [reset = 0h]

PCIE_CORE_PFn_I_BASE_ADDR_4 is shown in Figure 9-29 and described in Table 9-92.

Return to the [Summary Table](#).

This is one of the six Base Address Registers defined by the PCI Specifications 3.0. These registers are used to define address ranges for memory and I/O accesses to the Endpoint device. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1s into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if BAR 4 is not configured. Otherwise, the number of 1s returned is based on the size of the BAR. BAR4 can be setup as 32-bit memory or IO BAR, or can be paired with BAR 5 to form a 64bit memory BAR. The settings of this BAR is defined in the BAR Configuration Register associated with this PF.

The BAR aperture can be controller in two different ways:

- (i) When the Resizable BAR Capability is enabled, the aperture is controlled by the setting of the BAR width field in Resizable BAR Control Register. The Resizable BAR Capability is enabled by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register 1.
- (ii) When the Resizable BAR Capability is disabled for the Physical Function, the aperture is controlled by the setting of the PF BAR Configuration Register.

Offset = 20h + (n * 1000h); where n = 0h to 5h

Table 9-91. PCIE_CORE_PFn_I_BASE_ADDR_4 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0020h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0020h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0020h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0020h + formula

Figure 9-29. PCIE_CORE_PFn_I_BASE_ADDR_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-92. PCIE_CORE_PFn_I_BASE_ADDR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration regisiter in LM space.

Table 9-93. Register Call Summary for PCIE_CORE_PFn_I_BASE_ADDR_4

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_BASE_ADDR_4 Register \(Offset = 20h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.10 PCIE_CORE_PFn_I_BASE_ADDR_5 Register (Offset = 24h + formula) [reset = 0h]

PCIE_CORE_PFn_I_BASE_ADDR_5 is shown in Figure 9-30 and described in Table 9-95.

Return to the [Summary Table](#).

This is one of the six Base Address Registers defined by the PCI

Specifications 3.0. BAR5 can be setup as 32-bit memory or IO BAR, or

can be paired with BAR 4 to form a 64bit memory BAR.

This register can be used in two distinct ways: (i) When BAR 4 defines a 64-bit memory address range, this register is used to define the high-order bits of the base address. The number of writable bits

in this field is based on the aperture setting of the BAR. (ii) When the BAR 4 is

used to define a 32-bit memory address range or an I/O address range, this register can be used

to define a new 32-bit memory address range or an I/O address range. The individual fields in

the register have the same format as those of BAR 4 and is described below. The settings of this BAR

is defined in the BAR Configuration Register associated with this PF.

When configured as a 32-bit memory or IO BAR, the BAR aperture can be controller in two different ways:

(a) When the Resizable BAR Capability is enabled, the aperture is

controlled by the setting of the BAR width field in Resizable BAR Control Register 5.

The Resizable BAR Capability is enabled by setting the Enable Resizable BAR

Capability bit (bit 31) of the associated Physical Function BAR Configuration Register.

(b) When the Resizable BAR Capability is disabled for the Physical

Function, the aperture is controlled by the setting of the Physical Function BAR

Configuration Register.

Offset = 24h + (n * 1000h); where n = 0h to 5h

**Table 9-94. PCIE_CORE_PFn_I_BASE_ADDR_5
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0024h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0024h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0024h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0024h + formula

Figure 9-30. PCIE_CORE_PFn_I_BASE_ADDR_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-95. PCIE_CORE_PFn_I_BASE_ADDR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.

Table 9-96. Register Call Summary for PCIE_CORE_PFn_I_BASE_ADDR_5

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_BASE_ADDR_5 Register \(Offset = 24h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.11 PCIE_CORE_PFn_RSVD_0A Register (Offset = 28h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_0A is shown in [Figure 9-31](#) and described in [Table 9-98](#).

Return to the [Summary Table](#).

Reserved

Offset = 28h + (n * 1000h); where n = 0h to 5h

Table 9-97. PCIE_CORE_PFn_RSVD_0A Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0028h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0028h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0028h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0028h + formula

Figure 9-31. PCIE_CORE_PFn_RSVD_0A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-98. PCIE_CORE_PFn_RSVD_0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-99. Register Call Summary for PCIE_CORE_PFn_RSVD_0A

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_0A Register \(Offset = 28h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.12 PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Register (Offset = 2Ch + formula) [reset = 17CDh]

PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I is shown in Figure 9-32 and described in Table 9-101.

Return to the [Summary Table](#).

This register contains the Subsystem Vendor ID and Subsystem ID associated with the device incorporating the PCIe Controller.

Offset = 2Ch + (n * 1000h); where n = 0h to 5h

Table 9-100.
PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 002Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 002Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 002Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 002Ch + formula

Figure 9-32. PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SID																SVID															
R/W-0h																R-17CDh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-101. PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SID	R/W	0h	Specifies the Subsystem ID assigned by the manufacturer of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be re-written independently for each Function from the local management bus.
15-0	SVID	R	17CDh	Specifies the Subsystem Vendor ID assigned by the PCI SIG to the manufacturer of the device. Its value comes from the Subsystem Vendor ID Register in the local management register block.

Table 9-102. Register Call Summary for PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I

PCIE_CORE_EP_PF Registers

- PCIE_CORE_PFn_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Register (Offset = 2Ch + formula) [reset = 17CDh]: [0]
- PCIE_CORE_EP_PF Registers: [0] [1]

9.2.13 PCIE_CORE_PFn_RSVD_0C Register (Offset = 30h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_0C is shown in [Figure 9-33](#) and described in [Table 9-104](#).

Return to the [Summary Table](#).

Reserved

Offset = 30h + (n * 1000h); where n = 0h to 5h

Table 9-103. PCIE_CORE_PFn_RSVD_0C Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0030h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0030h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0030h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0030h + formula

Figure 9-33. PCIE_CORE_PFn_RSVD_0C Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-104. PCIE_CORE_PFn_RSVD_0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-105. Register Call Summary for PCIE_CORE_PFn_RSVD_0C

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_0C Register \(Offset = 30h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.14 PCIE_CORE_PFn_I_CAPABILITIES_POINTER Register (Offset = 34h + formula) [reset = 80h]

PCIE_CORE_PFn_I_CAPABILITIES_POINTER is shown in Figure 9-34 and described in Table 9-107.

Return to the [Summary Table](#).

This location contains the pointer to the first PCI Capabilities Structure. Its default value points to the Power Management Capability Structure (register number 0x80 hex).

Offset = 34h + (n * 1000h); where n = 0h to 5h

Table 9-106.
PCIE_CORE_PFn_I_CAPABILITIES_POINTER
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0034h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0034h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0034h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0034h + formula

Figure 9-34. PCIE_CORE_PFn_I_CAPABILITIES_POINTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15																CP															
R-0h																R/W-80h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-107. PCIE_CORE_PFn_I_CAPABILITIES_POINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R15	R	0h	Reserved
7-0	CP	R/W	80h	Contains pointer to the first PCI Capability Structure. This field is set by default to the value defined in the RTL file reg_defaults.h. It can be re-written independently for every Function from the local management bus.

Table 9-108. Register Call Summary for PCIE_CORE_PFn_I_CAPABILITIES_POINTER

PCIE_CORE_EP_PF Registers

- PCIE_CORE_PFn_I_CAPABILITIES_POINTER Register (Offset = 34h + formula) [reset = 80h]: [0]
- PCIE_CORE_EP_PF Registers: [0] [1]

9.2.15 PCIE_CORE_PFn_RSVD_0E Register (Offset = 38h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_0E is shown in [Figure 9-35](#) and described in [Table 9-110](#).

Return to the [Summary Table](#).

Reserved

Offset = 38h + (n * 1000h); where n = 0h to 5h

Table 9-109. PCIE_CORE_PFn_RSVD_0E Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0038h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0038h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0038h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0038h + formula

Figure 9-35. PCIE_CORE_PFn_RSVD_0E Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-110. PCIE_CORE_PFn_RSVD_0E Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-111. Register Call Summary for PCIE_CORE_PFn_RSVD_0E

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_0E Register \(Offset = 38h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.16 PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN Register (Offset = 3Ch + formula) [reset = 1FFh]

PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN is shown in Figure 9-36 and described in Table 9-113.

Return to the [Summary Table](#).

This location contains the PCI 3.0 Interrupt Line and Interrupt Pin Registers. These registers are used only when the Controller is configured to support PCI legacy interrupts. If the legacy interrupt mode is configured, the Controller receives interrupt indications from the client logic on its INTA_IN, INTB_IN, INTC_IN and INTD_IN inputs, and sends out Assert_INTx or Deassert_INTx messages on the link in response to their activation or deactivation, respectively. The Interrupt Pin Register defines which of the four inputs is connected to the Function corresponding to this register set. The Interrupt Line register defines the input of the interrupt controller (IRQ0 - IRQ15) in the Root Complex that is activated by each Assert_INTx message.

Offset = 3Ch + (n * 1000h); where n = 0h to 5h

Table 9-112.
PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 003Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 003Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 003Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 003Ch + formula

Figure 9-36. PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R16																					IPR			ILR							
R-0h											R/W-1h							R/W-FFh													

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-113. PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	R16	R	0h	Reserved
10-8	IPR	R/W	1h	Identifies the interrupt input [A, B, C, D] to which this Functions interrupt output is connected to [01 = INTA, 02 = INTB, 03 = INTC, 04 = INTD]. The assignment of interrupt inputs to Functions is fixed when the Controller is configured. This field can be re-written independently for each Function from the local management bus. Please see the define macros den_db_Fx_INTR_PIN values [where x is the function number] for default values of each function in the reg_defaults.v files.
7-0	ILR	R/W	FFh	Identifies the IRQx input of the interrupt controller at the Root Complex that is activated by this Functions interrupt [00 = IRQ0, ... , 0F = IRQ15, FF = unknown or not connected]. This field is writable from the local management bus. Please see the define macros den_db_Fx_INTR_LINE values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-114. Register Call Summary for PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_INTRPT_LINE_INTRPT_PIN Register \(Offset = 3Ch + formula\) \[reset = 1FFh\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.17 PCIE_CORE_PFn_RSVD_010_01F Register (Offset = 40h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_010_01F is shown in [Figure 9-37](#) and described in [Table 9-116](#).

Return to the [Summary Table](#).

Reserved

Offset = 40h + (n * 1000h); where n = 0h to 5h

**Table 9-115. PCIE_CORE_PFn_RSVD_010_01F
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0040h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0040h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0040h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0040h + formula

Figure 9-37. PCIE_CORE_PFn_RSVD_010_01F Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-116. PCIE_CORE_PFn_RSVD_010_01F Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-117. Register Call Summary for PCIE_CORE_PFn_RSVD_010_01F

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_010_01F Register \(Offset = 40h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.18 PCIE CORE PFn I PWR MGMT CAP Register (Offset = 80h + formula) [reset = 5A039001h]

PCIE CORE PFn I PWR MGMT CAP is shown in [Figure 9-38](#) and described in [Table 9-119](#).

Return to the [Summary Table](#).

This location contains the Power Management Capabilities Register, its Capability ID, and a pointer to the next capability. This version of the Controller supports the PCI power states D0, D1 and D3.

Offset = 80h + (n * 1000h); where n = 0h to 5h

Table 9-118. PCIE_CORE_PFn_I_PWR_MGMT_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0080h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0080h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0080h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0080h + formula

Figure 9-38. PCIE CORE PFn I PWR MGMT CAP Register

31		30		29		28		27		26		25		24	
PSDCS		PSDHS		PSD2S		PSD1S		PSD0S		D2S		D1S		MCRAPS	
R-0h		R/W-1h		R-0h		R/W-1h		R/W-1h		R-0h		R/W-1h		R-0h	
23		22		21		20		19		18		17		16	
MCRAPS				DSI		R0		PC		VID					
R-0h				R-0h		R-0h		R-0h		R/W-3h					
15		14		13		12		11		10		9		8	
CP															
R/W-90h															
7		6		5		4		3		2		1		0	
CID															
R/W-1h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-119. PCIE CORE PFn I PWR MGMT CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PSDCS	R	0h	Indicates whether the Function is capable of sending PME messages when in the D3cold state. Because the device does not have aux power, this bit is hardwired to 0.
30	PSDHS	R/W	1h	Indicates whether the Function is capable of sending PME messages when in the D3hot state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0's Power Management Capabilities Register.
29	PSD2S	R	0h	Indicates whether the Function is capable of sending PME messages when in the D2 state. This bit is hardwired to 0 because D2 state is not supported.

Table 9-119. PCIe_CORE_PFn_I_PWR_MGMT_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	PSD1S	R/W	1h	Indicates whether the Function is capable of sending PME messages when in the D1 state. This bit can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.
27	PSD0S	R/W	1h	Indicates whether the Function is capable of sending PME messages when in the D0 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.
26	D2S	R	0h	Set if the Function supports the D2 power state. Currently hardwired to 0.
25	D1S	R/W	1h	Set if the Function supports the D1 power state. This bit can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.
24-22	MCRAPS	R	0h	Specifies the maximum current drawn by the device from the aux power source in the D3cold state. This field is not implemented in devices not supporting PME notification when in the D3cold state, and is therefore hardwired to 0.
21	DSI	R	0h	This bit, when set, indicates that the device requires additional configuration steps beyond setting up its PCI configuration space, to bring it to the D0 active state from the D0 uninitialized state. This bit is hardwired to 0.
20	R0	R	0h	Reserved
19	PC	R	0h	Not applicable to PCI Express. This bit is hardwired to 0.
18-16	VID	R/W	3h	Indicates the version of the PCI Bus Power Management Specifications that the Function implements. This field is set by default to 011 [Version 1.2]. It can be re-written independently for each Function from the local management bus.
15-8	CP	R/W	90h	Contains pointer to the next PCI Capability Structure. The Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be re-written independently for each Function from the local management bus.
7-0	CID	R/W	1h	Identifies that the capability structure is for Power Management. This field is set by default to 01 hex. It can be re-written independently for each Function from the local management bus.

Table 9-120. Register Call Summary for PCIe_CORE_PFn_I_PWR_MGMT_CAP

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PWR_MGMT_CAP Register \(Offset = 80h + formula\) \[reset = 5A039001h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.19 PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP Register (Offset = 84h + formula) [reset = 8h]

PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP is shown in Figure 9-39 and described in Table 9-122.

Return to the [Summary Table](#).

This location contains the Power Management Control/Status and Data Registers.

Offset = 84h + (n * 1000h); where n = 0h to 5h

Table 9-121.
PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0084h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0084h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0084h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0084h + formula

Figure 9-39. PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP Register

31	30	29	28	27	26	25	24
DR							
R-0h							
23	22	21	20	19	18	17	16
R1							
R-0h							
15	14	13	12	11	10	9	8
PMES	R2						PE
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
R3				NSR	R4	PS	
R-0h				R/W-1h	R-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-122. PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DR	R	0h	This optional register is not implemented in the PCIe Controller. This field is hardwired to 0.
23-16	R1	R	0h	Reserved
15	PMES	R/W	0h	When PME notification is enabled, writing a 1 into this bit position from the local management bus sets this bit and causes the Controller to send a PME message from the associated Function. When the Root Complex processes this message, it will turn off this bit by writing a 1 into this bit position through a Config Write. This bit can be set or cleared from the local management bus, by writing a 1 or 0, respectively. It can only be cleared from the configuration path [by writing a 1]. This is a sticky field.
14-9	R2	R	0h	Reserved

Table 9-122. PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	PE	R/W	0h	Setting this bit enables the notification of PME events from the associated Function. This bit can be set also by writing into this register from the local management bus. This is a sticky field.
7-4	R3	R	0h	Reserved
3	NSR	R/W	1h	When this bit is set to 1, the Function will maintain all its state in the PM state D3hot. The software is not required to re-initialize the Function registers on the transition back to D0. This bit is set to 1 by default, but can be modified independently for each PF from the local management bus.
2	R4	R	0h	Reserved
1-0	PS	R/W	0h	Indicates the power state this Function is currently in. This field can be read by the software to monitor the current power state, or can be written to cause a transition to a new state. The valid settings are 00 [state D0], 01 [state D1] and 11 [state D3hot]. The software should not write any other value into this field. This field can also be written from the local management bus independently for each Function.

Table 9-123. Register Call Summary for PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_I_PWR_MGMT_CTRL_STAT_REP Register \(Offset = 84h + formula\) \[reset = 8h\]: \[0\]](#)

9.2.20 PCIE_CORE_PFn_RSVD_022_023 Register (Offset = 88h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_022_023 is shown in [Figure 9-40](#) and described in [Table 9-125](#).

Return to the [Summary Table](#).

Reserved

Offset = 88h + (n * 1000h); where n = 0h to 5h

**Table 9-124. PCIE_CORE_PFn_RSVD_022_023
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0088h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0088h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0088h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0088h + formula

Figure 9-40. PCIE_CORE_PFn_RSVD_022_023 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-125. PCIE_CORE_PFn_RSVD_022_023 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-126. Register Call Summary for PCIE_CORE_PFn_RSVD_022_023

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_022_023 Register \(Offset = 88h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.21 PCIE_CORE_PFn_I_MSI_CTRL_REG Register (Offset = 90h + formula) [reset = 0180B005h]

PCIE_CORE_PFn_I_MSI_CTRL_REG is shown in [Figure 9-41](#) and described in [Table 9-128](#).

Return to the [Summary Table](#).

This register is used only when the Controller is configured to support Message Signaled Interrupts (MSIs). In addition to the MSI control bits, this location also contains the Capability ID for MSI and the pointer to the next PCI Capability Structure.

Offset = 90h + (n * 1000h); where n = 0h to 5h

Table 9-127. PCIE_CORE_PFn_I_MSI_CTRL_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0090h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0090h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0090h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0090h + formula

Figure 9-41. PCIE_CORE_PFn_I_MSI_CTRL_REG Register

31	30	29	28	27	26	25	24
R0							MC
R-0h							R/W-1h
23	22	21	20	19	18	17	16
BAC64	MME			MMC			ME
R/W-1h	R/W-0h			R/W-0h			R/W-0h
15	14	13	12	11	10	9	8
CP1							
R/W-B0h							
7	6	5	4	3	2	1	0
CID1							
R-5h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-128. PCIE_CORE_PFn_I_MSI_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	R0	R	0h	Reserved
24	MC	R/W	1h	can be modified using localmanagement interface
23	BAC64	R/W	1h	Set to 1 to indicate that the device is capable of generating 64-bit addresses for MSI messages.Can be modified using local management interface
22-20	MME	R/W	0h	Encodes the number of distinct messages that the Controller is programmed to generate for this Function [000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32]. This setting must be based on the number of interrupt inputs of the Controller that are actually used by this Function. This field can be written from the local management bus.

Table 9-128. PCIE_CORE_PFn_I_MSI_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-17	MMC	R/W	0h	Encodes the number of distinct messages that the Controller is capable of generating for this Function [000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32]. Thus, this field defines the number of the interrupt vectors for this Function. The Controller allows up to 32 distinct messages, but the setting of this field must be based on the number of interrupt inputs of the Controller that are actually used by the client. For example, if the client logic uses 8 of the 32 distinct MSI interrupt inputs of the Controller for this Function, then the value of this field must be set to 011. This field can be written from the local management bus. Please see the define den_db_Fx_MSI_MULTIPLE_MSG_CAPABLE values [where x is the function number] for default values of each function in the reg_defaults.v files.
16	ME	R/W	0h	Set by the configuration program to enable the MSI feature. This field can also be written from the local management bus.
15-8	CP1	R/W	B0h	Pointer to the next PCI Capability Structure. This can be modified from the local management bus. This field can be written from the local management bus.
7-0	CID1	R	5h	Specifies that the capability structure is for MSI. Hardwired to 05 hex.

Table 9-129. Register Call Summary for PCIE_CORE_PFn_I_MSI_CTRL_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_MSI_CTRL_REG Register \(Offset = 90h + formula\) \[reset = 0180B005h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.22 PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR Register (Offset = 94h + formula) [reset = 0h]

PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR is shown in Figure 9-42 and described in Table 9-131.

Return to the [Summary Table](#).

This register contains the first 32 bits of the address to be used in the MSI messages generated by the Controller for this Function. This address is taken as a 32-bit address if the value programmed in the MSI Message High Address Register is 0. Otherwise, this address is taken as the least significant 32 bits of the 64-bit address sent in MSI messages.

Offset = 94h + (n * 1000h); where n = 0h to 5h

Table 9-130.
PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0094h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0094h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0094h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0094h + formula

Figure 9-42. PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAL																R1															
R/W-0h																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-131. PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	MAL	R/W	0h	Lower bits of the address to be used in MSI messages. This field can also be written from the local management bus.
1-0	R1	R	0h	The two lower bits of the address are hardwired to 0 to align the address on a double-word boundary.

Table 9-132. Register Call Summary for PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_MSI_MSG_LOW_ADDR Register \(Offset = 94h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.23 PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR Register (Offset = 98h + formula) [reset = 0h]

PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR is shown in Figure 9-43 and described in Table 9-134.

Return to the [Summary Table](#).

This register contains the most significant 32 bits of the 64-bit address sent by the Controller in MSI messages. A value of all zeroes in this register is taken to mean that the Controller should use 32-bit addresses in the messages.

Offset = 98h + (n * 1000h); where n = 0h to 5h

Table 9-133.
PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0098h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0098h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0098h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0098h + formula

Figure 9-43. PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-134. PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAH	R/W	0h	Contains bits 63:32 of the 64-bit address to be used in MSI Messages. A value of 0 specifies that 32-bit addresses are to be used in the messages. This field can also be written from the local management bus.

Table 9-135. Register Call Summary for PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_MSI_MSG_HI_ADDR Register \(Offset = 98h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.24 PCIE_CORE_PFn_I_MSI_MSG_DATA Register (Offset = 9Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_MSI_MSG_DATA is shown in Figure 9-44 and described in Table 9-137.

Return to the [Summary Table](#).

This register contains the write data to be used in the MSI messages to be generated for the associated PCI Function. When the number of distinct messages programmed in the MSI Control Register is 1, the 32-bit value from this register is used as the data value in the MSI packets generated by the Controller for this Function. If the number of distinct messages is more than 1, the least significant bits of the programmed value are replaced with the encoded interrupt vector [31:0] of the specific message to generate the write data value for the message.

Offset = 9Ch + (n * 1000h); where n = 0h to 5h

Table 9-136. PCIE_CORE_PFn_I_MSI_MSG_DATA Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 009Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 009Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 009Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 009Ch + formula

Figure 9-44. PCIE_CORE_PFn_I_MSI_MSG_DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R2																MD															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-137. PCIE_CORE_PFn_I_MSI_MSG_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R2	R	0h	Hardwired to 0
15-0	MD	R/W	0h	Message data to be used for this Function. This field can also be written from the local management bus.

Table 9-138. Register Call Summary for PCIE_CORE_PFn_I_MSI_MSG_DATA

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_MSI_MSG_DATA Register \(Offset = 9Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.25 PCIE_CORE_PFn_I_MSI_MASK Register (Offset = A0h + formula) [reset = 0h]

PCIE_CORE_PFn_I_MSI_MASK is shown in Figure 9-45 and described in Table 9-140.

Return to the [Summary Table](#).

This register contains the MSI mask bits, one for each of the interrupt levels.

Offset = A0h + (n * 1000h); where n = 0h to 5h

Table 9-139. PCIE_CORE_PFn_I_MSI_MASK Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00A0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00A0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00A0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00A0h + formula

Figure 9-45. PCIE_CORE_PFn_I_MSI_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0															MM
R-0h															R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-140. PCIE_CORE_PFn_I_MSI_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R0	R	0h	Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of this field also changes correspondingly
0	MM	R/W	0h	Mask bits for MSI interrupts. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid mask bits. Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of the MSI Mask field also changes correspondingly

Table 9-141. Register Call Summary for PCIE_CORE_PFn_I_MSI_MASK

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_MSI_MASK Register \(Offset = A0h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.26 PCIE_CORE_PFn_I_MSI_PENDING_BITS Register (Offset = A4h + formula) [reset = 0h]

PCIE_CORE_PFn_I_MSI_PENDING_BITS is shown in Figure 9-46 and described in Table 9-143.

Return to the [Summary Table](#).

This register contains the MSI pending interrupt bits, one for each of the interrupt levels.

Offset = A4h + (n * 1000h); where n = 0h to 5h

Table 9-142.
PCIE_CORE_PFn_I_MSI_PENDING_BITS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00A4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00A4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00A4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00A4h + formula

Figure 9-46. PCIE_CORE_PFn_I_MSI_PENDING_BITS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0															MP
R-0h															R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-143. PCIE_CORE_PFn_I_MSI_PENDING_BITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R0	R	0h	Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of this field also changes correspondingly
0	MP	R/W	0h	Pending bits for MSI interrupts. This field can be written from either the APB interface or the MSI_PENDING_STATUS_IN inputs of the Controller depending on the MSI Pending Status In Mode select Bit in the Local Management space. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid pending bits. Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of the MSI Pending Bits field also changes correspondingly

Table 9-144. Register Call Summary for PCIE_CORE_PFn_I_MSI_PENDING_BITS

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_MSI_PENDING_BITS Register \(Offset = A4h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.27 PCIE_CORE_PFn_RSVD_02A_02B Register (Offset = A8h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_02A_02B is shown in [Figure 9-47](#) and described in [Table 9-146](#).

Return to the [Summary Table](#).

Reserved

Offset = A8h + (n * 1000h); where n = 0h to 5h

**Table 9-145. PCIE_CORE_PFn_RSVD_02A_02B
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00A8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00A8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00A8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00A8h + formula

Figure 9-47. PCIE_CORE_PFn_RSVD_02A_02B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-146. PCIE_CORE_PFn_RSVD_02A_02B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-147. Register Call Summary for PCIE_CORE_PFn_RSVD_02A_02B

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_02A_02B Register \(Offset = A8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.28 PCIE_CORE_PFn_I_MSIX_CTRL Register (Offset = B0h + formula) [reset = C011h]

PCIE_CORE_PFn_I_MSIX_CTRL is shown in Figure 9-48 and described in Table 9-149.

Return to the [Summary Table](#).

This register contains the MSI-X configuration bits, the Capability ID for MSI-X and the pointer to the next PCI Capability Structure.

Offset = B0h + (n * 1000h); where n = 0h to 5h

**Table 9-148. PCIE_CORE_PFn_I_MSIX_CTRL
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00B0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00B0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00B0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00B0h + formula

Figure 9-48. PCIE_CORE_PFn_I_MSIX_CTRL Register

31	30	29	28	27	26	25	24
MSIXE	FM		R0			MSIXTS	
R/W-0h	R/W-0h		R-0h			R/W-0h	
23	22	21	20	19	18	17	16
						MSIXTS	
						R/W-0h	
15	14	13	12	11	10	9	8
						CP	
						R/W-C0h	
7	6	5	4	3	2	1	0
						CID	
						R/W-11h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-149. PCIE_CORE_PFn_I_MSIX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSIXE	R/W	0h	Set by the configuration program to enable the MSI-X feature. This field can also be written from the local management bus.
30	FM	R/W	0h	This bit serves as a global mask to all the interrupt conditions associated with this Function. When this bit is set, the Controller will not send out MSI-X messages from this Function. This field can also be written from the local management bus.
29-27	R0	R	0h	Reserved
26-16	MSIXTS	R/W	0h	Specifies the size of the MSI-X Table, that is, the number of interrupt vectors defined for the Function. The programmed value is 1 minus the size of the table [that is, this field is set to 0 if the table size is 1.]. It can be re-written independently for each Function from the local management bus. Please see the define den_db_Fx_MSIX_TABLE_SIZE values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-149. PCIE_CORE_PFn_I_MSIX_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	CP	R/W	C0h	Contains pointer to the next PCI Capability Structure. This is set to point to the PCI Express Capability Structure at 30 hex. This can be rewritten independently for each Function from the local management bus.
7-0	CID	R/W	11h	Identifies that the capability structure is for MSI-X. This field is set by default to 11 hex. It can be rewritten independently for each Function from the local management bus.

Table 9-150. Register Call Summary for PCIE_CORE_PFn_I_MSIX_CTRL

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_I_MSIX_CTRL Register \(Offset = B0h + formula\) \[reset = C011h\]: \[0\]](#)

9.2.29 PCIE_CORE_PFn_I_MSIX_TBL_OFFSET Register (Offset = B4h + formula) [reset = 0h]

PCIE_CORE_PFn_I_MSIX_TBL_OFFSET is shown in Figure 9-49 and described in Table 9-152.

Return to the [Summary Table](#).

This register is used to specify the location of the MSI-X Table in memory. All the 32 bits of this register can be re-written independently for each Function from the local management bus.

Offset = B4h + (n * 1000h); where n = 0h to 5h

Table 9-151.
PCIE_CORE_PFn_I_MSIX_TBL_OFFSET Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00B4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00B4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00B4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00B4h + formula

Figure 9-49. PCIE_CORE_PFn_I_MSIX_TBL_OFFSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO												BARI			
R/W-0h												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-152. PCIE_CORE_PFn_I_MSIX_TBL_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	TO	R/W	0h	Offset of the memory address where the MSI-X Table is located, relative to the selected BAR. The three least significant bits of the address are omitted, as the addresses are QWORD aligned. Please see the define den_db_Fx_MSIX_TABLE_OFFSET values [where x is the function number] for default values of each function in the reg_defaults.v files.
2-0	BARI	R/W	0h	Identifies the BAR corresponding to the memory address range where the MSI-X Table is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. Please see the define den_db_Fx_MSIX_TABLE_BIR values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-153. Register Call Summary for PCIE_CORE_PFn_I_MSIX_TBL_OFFSET

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_MSIX_TBL_OFFSET Register \(Offset = B4h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.30 PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT Register (Offset = B8h + formula) [reset = 8h]

PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT is shown in Figure 9-50 and described in Table 9-155.

Return to the [Summary Table](#).

This register is used to specify the location of the MSI-X Pending Bit Array (PBA). The PBA is a structure in memory containing the pending interrupt bits. All the 32 bits of this register can be rewritten independently for each Function from the local management bus.

Offset = B8h + (n * 1000h); where n = 0h to 5h

Table 9-154.
PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00B8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00B8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00B8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00B8h + formula

Figure 9-50. PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBAO															
R/W-1h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBAO												BARI1			
R/W-1h												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-155. PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	PBAO	R/W	1h	Offset of the memory address where the PBA is located, relative to the selected BAR. The three least significant bits of the address are omitted, as the addresses are QWORD aligned. Please see the define den_db_Fx_MSIX_PBA_OFFSET values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-155. PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BAR1	R/W	0h	Identifies the BAR corresponding to the memory address range where the PBA Structure is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register. Identifies the BAR corresponding to the memory address range where the PBA Structure is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register. Please see the define den_db_Fx_MSIX_PBA_BIR values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-156. Register Call Summary for PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_MSIX_PENDING_INTRPT Register \(Offset = B8h + formula\) \[reset = 8h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.31 PCIE_CORE_PFn_RSVD_02F Register (Offset = BCh + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_02F is shown in [Figure 9-51](#) and described in [Table 9-158](#).

Return to the [Summary Table](#).

Reserved

Offset = BCh + (n * 1000h); where n = 0h to 5h

Table 9-157. PCIE_CORE_PFn_RSVD_02F Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00BCh + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00BCh + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00BCh + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00BCh + formula

Figure 9-51. PCIE_CORE_PFn_RSVD_02F Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-158. PCIE_CORE_PFn_RSVD_02F Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-159. Register Call Summary for PCIE_CORE_PFn_RSVD_02F

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_02F Register \(Offset = BCh + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.32 PCIE_CORE_PFn_I_PCIE_CAP_LIST Register (Offset = C0h + formula) [reset = 00020010h]

PCIE_CORE_PFn_I_PCIE_CAP_LIST is shown in [Figure 9-52](#) and described in [Table 9-161](#).

Return to the [Summary Table](#).

This location identifies the PCI Express device type and its capabilities. It also contains the Capability ID for the PCI Express Structure and the pointer to the next capability structure.

Offset = C0h + (n * 1000h); where n = 0h to 5h

Table 9-160. PCIE_CORE_PFn_I_PCIE_CAP_LIST Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00C0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00C0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00C0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00C0h + formula

Figure 9-52. PCIE_CORE_PFn_I_PCIE_CAP_LIST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0	TRS	IMN				SS		DT			PCV				
R-0h	R-0h	R-0h				R-0h		R-0h			R/W-2h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCP								CID							
R-0h								R-10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-161. PCIE_CORE_PFn_I_PCIE_CAP_LIST Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R0	R	0h	Reserved
30	TRS	R	0h	When set to 1, this bit indicates that the device supports routing of Trusted Configuration Requests. Not valid for Endpoints. Hardwired to 0.
29-25	IMN	R	0h	Identifies the MSI or MSI-X interrupt vector for the interrupt message generated corresponding to the status bits in the Slot Status Register, Root Status Register, or this capability structure. This field must be defined based on the chosen interrupt mode - MSI or MSI-X. This field is hardwired to 0.
24	SS	R	0h	Set to 1 when the link connected to a slot. Hardwired to 0.
23-20	DT	R	0h	Indicates the type of device implementing this Function. This field is hardwired to 0 in the EP mode.
19-16	PCV	R/W	2h	Identifies the version number of the capability structure. This field is set to 2 by default to indicate that the Controller is compatible to PCI Express Base Specification Revision 3.0. This field can be modified through local management interface.
15-8	NCP	R	0h	Points to the next PCI capability structure. Set to 0 because this is the last capability structure.

Table 9-161. PCIE_CORE_PFn_I_PCIE_CAP_LIST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CID	R	10h	Specifies Capability ID assigned by PCI SIG for this structure. This field is hardwired to 10 hex.

Table 9-162. Register Call Summary for PCIE_CORE_PFn_I_PCIE_CAP_LIST

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PCIE_CAP_LIST Register \(Offset = C0h + formula\) \[reset = 00020010h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.33 PCIE_CORE_PFn_I_PCIE_DEV_CAP Register (Offset = C4h + formula) [reset = 10008101h]

PCIE_CORE_PFn_I_PCIE_DEV_CAP is shown in Figure 9-53 and described in Table 9-164.

Return to the [Summary Table](#).

This register advertises the capabilities of the PCI Express device encompassing this Function.

Offset = C4h + (n * 1000h); where n = 0h to 5h

Table 9-163. PCIE_CORE_PFn_I_PCIE_DEV_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00C4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00C4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00C4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00C4h + formula

Figure 9-53. PCIE_CORE_PFn_I_PCIE_DEV_CAP Register

31	30	29	28	27	26	25	24
R3			FC	CPLS		CSPLV	
R-0h			R/W-1h	R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
CSPLV						R2	
R/W-0h						R-0h	
15	14	13	12	11	10	9	8
RBER	R1			AL1SL			AL0SL
R/W-1h	R-0h			R/W-0h			R/W-4h
7	6	5	4	3	2	1	0
AL0SL		ETFS	PFS		MPS		
R/W-4h		R-0h	R-0h		R/W-1h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-164. PCIE_CORE_PFn_I_PCIE_DEV_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	R3	R	0h	Reserved
28	FC	R/W	1h	Set when device has Function-Level Reset capability. It is set by default to 1. It can be re-written independently for each Function from the local management bus.
27-26	CPLS	R/W	0h	Specifies the scale used by Slot Power Limit Value. It is set by default to the value define in reg_defaults.h. It can be re-written independently for each Function from the local management bus.
25-18	CSPLV	R/W	0h	Specifies upper limit on power supplied by slot. It is set by default to the value define in reg_defaults.h. It can be re-written independently for each Function from the local management bus.
17-16	R2	R	0h	Reserved
15	RBER	R/W	1h	Enables role-based error reporting. It is hardwired to 1. It can be re-written independently for each Function from the local management bus.

Table 9-164. PCIE_CORE_PFn_I_PCIE_DEV_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	R1	R	0h	Reserved
11-9	AL1SL	R/W	0h	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L1 to L0. It is set by default to the value define in reg_defaults.h. It can be re-written independently for each Function from the local management bus.
8-6	AL0SL	R/W	4h	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L0S to L0. It is set by default to the value define in reg_defaults.h. It can be re-written independently for each Function from the local management bus.
5	ETFS	R	0h	Extended Tag Field not Supported. Hard coded to 0.
4-3	PFS	R	0h	This field is used to extend the tag field by combining unused Function bits with the tag bits. This field is hardwired to 00 to disable this feature.
2-0	MPS	R/W	1h	Specifies maximum payload size supported by the device.

Table 9-165. Register Call Summary for PCIE_CORE_PFn_I_PCIE_DEV_CAP

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PCIE_DEV_CAP Register \(Offset = C4h + formula\) \[reset = 10008101h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.34 PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS Register (Offset = C8h + formula) [reset = 2810h]

PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS is shown in Figure 9-54 and described in Table 9-167.

Return to the [Summary Table](#).

This register contains control and status bits associated with the device implementing this Function. All the read-write bits in this register can also be written from the local management bus. Likewise, bits designated as RW1C can also be cleared by writing a 1 from the local management bus.

Offset = C8h + (n * 1000h); where n = 0h to 5h

Table 9-166.
PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00C8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00C8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00C8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00C8h + formula

Figure 9-54. PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS Register

31	30	29	28	27	26	25	24
R4							
R-0h							
23	22	21	20	19	18	17	16
R4		TP	APD	URD	FED	NFED	CED
R-0h		R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
FLR	MRRS			ENS	EAP	EPH	ETFE
R/W-0h		R/W-2h		R/W-1h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
MPS			ERO	EURR	EFER	ENFER	ECER
R/W-0h			R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-167. PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R4	R	0h	Reserved
21	TP	R	0h	Indicates if any of the Non-Posted requests issued by the Function are still pending.
20	APD	R	0h	Set when auxiliary power is detected by the device. This is an unused field.
19	URD	R/W1C	0h	Set to 1 by the Controller when it receives an unsupported request, regardless of whether its reporting is enabled or not.
18	FED	R/W1C	0h	Set to 1 by the Controller when it detects a fatal error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.
17	NFED	R/W1C	0h	Set to 1 by the Controller when it detects a non-fatal error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.

Table 9-167. PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CED	R/W1C	0h	Set to 1 by the Controller when it detects a correctable error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.
15	FLR	R/W	0h	Writing a 1 into this bit position generates a Function-Level Reset for the selected Function. This bit reads as 0.
14-12	MRRS	R/W	2h	Specifies the maximum size allowed in read requests generated by the device.
11	ENS	R/W	1h	When set to 1, the device is allowed to set the No Snoop bit in initiated transactions in which cache coherency is not needed.
10	EAP	R	0h	Used only when device used aux power. This field is hardwired to 0.
9	EPH	R	0h	This field is hardwired to 0 as the Controller does not support this feature.
8	ETFE	R	0h	Enables the extension of the tag field from 5 to 8 bits.
7-5	MPS	R/W	0h	Specifies the maximum TLP payload size configured. The device must be able to receive a TLP of this maximum size, and should not generate TLPs larger than this value. The configuration program sets this field based on the maximum payload size in the Device Capabilities Register, and the capability of the other side.
4	ERO	R/W	1h	When set, this bit indicates that the device is allowed to set the Relaxed Ordering bit in the Attributes field of transactions initiated from it, when the transactions do not require Strong Ordering.
3	EURR	R/W	0h	Enables the sending of error messages by the Controller on receiving unsupported requests.
2	EFER	R/W	0h	Enables the sending of ERR_FATAL messages by the Controller on the detection of fatal errors.
1	ENFER	R/W	0h	Enables the sending of ERR_NONFATAL messages by the Controller on the detection of non-fatal errors.
0	ECER	R/W	0h	Enables the sending of ERR_COR messages by the Controller on the detection of correctable errors.

Table 9-168. Register Call Summary for PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS Register \(Offset = C8h + formula\) \[reset = 2810h\]: \[0\]](#)

9.2.35 PCIE_CORE_PFn_I_LINK_CAP Register (Offset = CCh + formula) [reset = 0041AC24h]

PCIE_CORE_PFn_I_LINK_CAP is shown in Figure 9-55 and described in Table 9-170.

Return to the [Summary Table](#).

This register advertises the link-specific capabilities of the device incorporating the PCIe Controller.

Offset = CCh + (n * 1000h); where n = 0h to 5h

Table 9-169. PCIE_CORE_PFn_I_LINK_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00CCh + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00CCh + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00CCh + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00CCh + formula

Figure 9-55. PCIE_CORE_PFn_I_LINK_CAP Register

31	30	29	28	27	26	25	24
PN							
R-0h							
23	22	21	20	19	18	17	16
R5	AOC	LBNC	DLLARC	SDERC	CPM	L1EL	
R-0h	R/W-1h	R-0h	R-0h	R-0h	R/W-0h	R/W-3h	
15	14	13	12	11	10	9	8
L1EL	L0SEL			ASPM		MLW	
R/W-3h	R/W-2h			R/W-3h		R-2h	
7	6	5	4	3	2	1	0
MLW				MLS			
R-2h				R-4h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-170. PCIE_CORE_PFn_I_LINK_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PN	R	0h	Specifies the port number assigned to the PCI Express link connected to this device.
23	R5	R	0h	Reserved
22	AOC	R/W	1h	Setting this bit indicates that the device supports the ASPM Optionality feature. It can be turned off by writing a 0 to this bit position through the local management bus.
21	LBNC	R	0h	A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. Reserved for Endpoint.
20	DLLARC	R	0h	Set to 1 if the device is capable of reporting that the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0, as this version of the Controller does not support the feature.

Table 9-170. PCIE_CORE_PFn_I_LINK_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	SDERC	R	0h	Indicates the capability of the device to report a Surprise Down error condition. This bit is hardwired to 0, as this version of the Controller does not support the feature.
18	CPM	R/W	0h	Indicates that the device supports removal of referenc clocks. It is set by default to the value of the define in reg_defaults.h. It can be re-written independently for each function from the local management bus.
17-15	L1EL	R/W	3h	Specifies the exit latency from L1 state. This parameter is dependent on the Physical Layer implementation. It is set by default to the value define in reg_defaults.h. It can be re-written independently for each Function from the local management bus.
14-12	LOSEL	R/W	2h	Specifies the time required for the device to transition from LOS to L0. This parameter is dependent on the Physical Layer implementation. It is set by default to the value define in reg_defaults.h. It can be re-written independently for each Function from the local management bus.
11-10	ASPM	R/W	3h	Indicates the level of ASPM support provided by the device. This field can be re-written independently for each Function from the local management bus. When SRIS is enabled in local management register bit, L0s capability is not supported and is forced low.
9-4	MLW	R	2h	Indicates the maximum number of lanes supported by the device. This field is hardwired based on the setting of the LANE_COUNT_IN strap input.
3-0	MLS	R	4h	Indicates the maximum speed supported by the link. [2.5 GT/s, 5 GT/s, 8 GT/s, 16 GT/s per lane]. This field is hardwired to 0001 [2.5GT/s] when the strap input PCIE_GENERATION_SEL is set to 0, to 0010 [5 GT/s] when the strap is set to 1, and to 0011 [8 GT/s] when the strap input is set to 10, to 0100 [16 GT/s] when the strap input is set to 11.

Table 9-171. Register Call Summary for PCIE_CORE_PFn_I_LINK_CAP

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_LINK_CAP Register \(Offset = CCh + formula\) \[reset = 0041AC24h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.36 PCIE_CORE_PFn_I_LINK_CTRL_STATUS Register (Offset = D0h + formula) [reset = 00210000h]

PCIE_CORE_PFn_I_LINK_CTRL_STATUS is shown in Figure 9-56 and described in Table 9-173.

Return to the [Summary Table](#).

This register contains control and status bits specific to the PCI Express link. All the read-write bits in this register can also be written from the local management bus.

Offset = D0h + (n * 1000h); where n = 0h to 5h

Table 9-172.
PCIE_CORE_PFn_I_LINK_CTRL_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00D0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00D0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00D0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00D0h + formula

Figure 9-56. PCIE_CORE_PFn_I_LINK_CTRL_STATUS Register

31	30	29	28	27	26	25	24
LABS	LBMS	DLLA	SCC	LTS	R8	NLW	
R/W1C-0h	R/W1C-0h	R-0h	R/W-0h	R-0h	R-0h	R-2h	
23	22	21	20	19	18	17	16
NLW				NLS			
R-2h				R-1h			
15	14	13	12	11	10	9	8
R15_12				LABIE	LBMIE	HAWD	ECPM
R-0h				R-0h	R-0h	R/W-0h	R-0h
7	6	5	4	3	2	1	0
ES	CCC	RL	LD	RCB	R6	ASPMC	
R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-173. PCIE_CORE_PFn_I_LINK_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LABS	R/W1C	0h	This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0. Not applicable to Endpoints where field is hardwired to 0.
30	LBMS	R/W1C	0h	This bit is Set by hardware to indicate that either link training has completed following write to retrain link bit, or when HW has changed link speed or width to attempt to correct unreliable link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0. Not applicable to Endpoints where field is hardwired to 0.
29	DLLA	R	0h	Indicates the status of the Data Link Layer. Set to 1 when the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0 in this version of the Controller.

Table 9-173. PCIE_CORE_PFn_I_LINK_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	SCC	R/W	0h	This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference clock on the connector, this bit must be clear. For PF0, this bit can also be written from the local management bus.
27	LTS	R	0h	This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. Not applicable to Endpoints where field is hardwired to 0.
26	R8	R	0h	Reserved
25-20	NLW	R	2h	Set at the end of link training to the actual link width negotiated between the two sides. Value is undefined if this registers is accessed before link training.
19-16	NLS	R	1h	Negotiated link speed of the device. The only supported speed ids are 2.5 GT/s per lane [0001], 5 GT/s per lane [0010], 8 GT/s per lane [0011], 16 GT/s per lane [0100].
15-12	R15_12	R	0h	Reserved
11	LABIE	R	0h	When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0. Not applicable to Endpoints where field is hardwired to 0.
10	LBMIE	R	0h	When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0. Not applicable to Endpoints where field is hardwired to 0.
9	HAWD	R/W	0h	When this bit is set, the local application must not request to change the operating width of the link, other than attempting to correct unreliable Link operation by reducing Link width.
8	ECPM	R	0h	When this bit is set to 1, the device may use the CLKREQ# pin on the PCIe connector to power manage the Link clock. This bit is writeable only when the Clock Power Management bit in the Link Capability Register is set to 1.
7	ES	R/W	0h	Set to 1 to extend the sequence of ordered sets transmitted while exiting from the LOS state.
6	CCC	R/W	0h	A value of 0 indicates that the reference clock of this device is asynchronous to that of the upstream device. A value of 1 indicates that the reference clock is common.
5	RL	R	0h	Setting this bit to 1 causes the LTSSM to initiate link training. Reserved for Endpoint mode. This bit always reads as 0
4	LD	R	0h	Writing a 1 to this bit position causes the LTSSM to go to the Disable Link state. The LTSSM stays in the Disable Link state while this bit is set. Reserved for Endpoint mode.

Table 9-173. PCIE_CORE_PFn_I_LINK_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RCB	R/W	0h	Indicates the Read Completion Boundary of the Root Port connected to this Endpoint [0 = 64 bytes, 1 = 128 bytes]. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
2	R6	R	0h	Reserved
1-0	ASPMC	R/W	0h	Controls the level of ASPM support on the PCI Express link associated with this Function. The valid setting are 00: ASPM disabled 01: L0s entry enabled, L1 disabled 10: L1 entry enabled, L0s disabled 11: Both L0s and L1 enabled.

Table 9-174. Register Call Summary for PCIE_CORE_PFn_I_LINK_CTRL_STATUS

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_LINK_CTRL_STATUS Register \(Offset = D0h + formula\) \[reset = 00210000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.37 PCIE_CORE_PFn_RSVD_035 Register (Offset = D4h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_035 is shown in Figure 9-57 and described in Table 9-176.

Return to the [Summary Table](#).

Reserved

Offset = D4h + (n * 1000h); where n = 0h to 5h

Table 9-175. PCIE_CORE_PFn_RSVD_035 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00D4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00D4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00D4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00D4h + formula

Figure 9-57. PCIE_CORE_PFn_RSVD_035 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-176. PCIE_CORE_PFn_RSVD_035 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-177. Register Call Summary for PCIE_CORE_PFn_RSVD_035

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_035 Register \(Offset = D4h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.38 PCIE_CORE_PFn_RSVD_036 Register (Offset = D8h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_036 is shown in [Figure 9-58](#) and described in [Table 9-179](#).

Return to the [Summary Table](#).

Reserved

Offset = D8h + (n * 1000h); where n = 0h to 5h

Table 9-178. PCIE_CORE_PFn_RSVD_036 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00D8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00D8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00D8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00D8h + formula

Figure 9-58. PCIE_CORE_PFn_RSVD_036 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-179. PCIE_CORE_PFn_RSVD_036 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-180. Register Call Summary for PCIE_CORE_PFn_RSVD_036

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_036 Register \(Offset = D8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.39 PCIE_CORE_PFn_RSVD_037_038 Register (Offset = DCh + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_037_038 is shown in [Figure 9-59](#) and described in [Table 9-182](#).

Return to the [Summary Table](#).

Reserved

Offset = DCh + (n * 1000h); where n = 0h to 5h

**Table 9-181. PCIE_CORE_PFn_RSVD_037_038
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00DCh + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00DCh + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00DCh + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00DCh + formula

Figure 9-59. PCIE_CORE_PFn_RSVD_037_038 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-182. PCIE_CORE_PFn_RSVD_037_038 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-183. Register Call Summary for PCIE_CORE_PFn_RSVD_037_038

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_037_038 Register \(Offset = DCh + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.40 PCIE_CORE_PFn_I_PCIE_DEV_CAP_2 Register (Offset = E4h + formula) [reset = X]

PCIE_CORE_PFn_I_PCIE_DEV_CAP_2 is shown in Figure 9-60 and described in Table 9-185.

Return to the [Summary Table](#).

This register advertises the capabilities of the PCI Express device encompassing this Function.

Offset = E4h + (n * 1000h); where n = 0h to 5h

**Table 9-184. PCIE_CORE_PFn_I_PCIE_DEV_CAP_2
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00E4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00E4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00E4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00E4h + formula

Figure 9-60. PCIE_CORE_PFn_I_PCIE_DEV_CAP_2 Register

31	30	29	28	27	26	25	24
R14							
R-0h							
23	22	21	20	19	18	17	16
MEEP	EEPS	EXFS	OPFFS	T10RS	T10CS		
R/W-1h	R/W-1h	R-1h	R-0h	R-0h	R-0h	R/W-1h	
15	14	13	12	11	10	9	8
R13	RESERVED	TCS	LMS	R12	BAOCS128	BAOCS64	
R-0h	R/W-X	R-0h	R/W-1h	R-0h	R-0h	R-0h	
7	6	5	4	3	2	1	0
BAOCS32	OPRS	AFS	CTDS	CTR			
R-0h	R-0h	R-0h	R/W-1h	R/W-2h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-185. PCIE_CORE_PFn_I_PCIE_DEV_CAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R14	R	0h	Reserved
23-22	MEEP	R/W	1h	Indicates the maximum number of End-End TLP Prefixes supported by the Function. The supported values are: 01b 1 End-End TLP Prefix 10b 2 End-End TLP Prefixes
21	EEPS	R/W	1h	Indicates whether the Function supports End-End TLP Prefixes. A 1 in this field indicates that the Function supports receiving TLPs containing End-End TLP Prefixes.
20	EXFS	R	1h	Indicates that the Function supports the 3-bit definition of the Fmt field in the TLP header. This bit is hardwired to 1 for all Functions.
19-18	OPFFS	R	0h	A 1 in this bit position indicates that the Function supports the Optimized Buffer Flush/Fill [OBFF] capability using message signaling.
17	T10RS	R	0h	If set function supports 1-bit requester capability otherwise, the function does not. This bit can be disabled using local management register.

Table 9-185. PCIE_CORE_PFn_I_PCIE_DEV_CAP_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	T10CS	R/W	1h	If set function supports 1-bit completer capability otherwise, the function does not. This field can be modified using local management interface.
15-14	R13	R	0h	Reserved
13	RESERVED	R/W	X	
12	TCS	R	0h	Hardwired to 0.
11	LMS	R/W	1h	A 1 in this bit position indicates that the Function supports the Latency Tolerance Reporting [LTR] Capability. This bit is set to 1 by default, but can be turned off for all Physical Functions by writing into PF 0.
10	R12	R	0h	Reserved
9	BAOCS128	R	0h	Hardwired to 0.
8	BAOCS64	R	0h	Hardwired to 0.
7	BAOCS32	R	0h	Hardwired to 0.
6	OPRS	R	0h	Atomic OP routing supported.
5	AFS	R	0h	ARI forwarding supported.
4	CTDS	R/W	1h	A 1 in this field indicates that the associated Function supports the capability to turn off its Completion timeout. This bit is set to 1 by default, but can be re-written independently for each Function from the local management bus.
3-0	CTR	R/W	2h	Specifies the Completion Timeout values supported by the device. This field is set by default to 0010 [10 ms - 250 ms]. The actual timeout values are in two programmable local management registers, which allow the timeout settings of the two sub-ranges within Range B to be programmed independently.

Table 9-186. Register Call Summary for PCIE_CORE_PFn_I_PCIE_DEV_CAP_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PCIE_DEV_CAP_2 Register \(Offset = E4h + formula\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.41 PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2 Register (Offset = E8h + formula) [reset = 0h]

PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2 is shown in Figure 9-61 and described in Table 9-188.

Return to the [Summary Table](#).

This register contains control and status bits associated with the device implementing this Function.

Offset = E8h + (n * 1000h); where n = 0h to 5h

Table 9-187.
PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00E8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00E8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00E8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00E8h + formula

Figure 9-61. PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2 Register

31	30	29	28	27	26	25	24
R18							
R-0h							
23	22	21	20	19	18	17	16
R18							
R-0h							
15	14	13	12	11	10	9	8
R18	OBFFE		T10RE	R17	LTRME	IDOCE	IDORE
R-0h	R-0h		R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
R16	AORE	AFE	CTD	CTV			
R-0h	R-0h	R-0h	R/W-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-188. PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	R18	R	0h	Reserved
14-13	OBFFE	R	0h	Enables the Optimized Buffer Flush/Fill [OBFF] capability in the device. This field is implemented only in PF 0. Valid settings are 00 [disabled], 01 [Variation A] and 10 [Variation B]. This field can also be written from the local management bus. RW if OBFF capability is supported, RO otherwise.
12	T10RE	R	0h	10bit TAGs generation are not supported in this configuration.
11	R17	R	0h	Reserved
10	LTRME	R/W	0h	This must be set to 1 to enable the Latency Tolerance Reporting Mechanism. This bit is implemented only in PF 0. Its default value is 1, but can be modified from the local management bus. This bit is read-only in PF 1.

Table 9-188. PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	IDOCE	R/W	0h	When this bit is 1, the Function is allowed to set the ID-based Ordering [IDO] Attribute bit in the Completions it generates.
8	IDORE	R/W	0h	When this bit is 1, the Function is allowed to set the ID-based Ordering [IDO] Attribute bit in the requests it generates.
7	R16	R	0h	Reserved
6	AORE	R	0h	This bit must be set to enable the generation of Atomic Op Requests from the Function. If the client logic attempts to send an Atomic Op for a Function for which this bit is not set, logic in the Controller will nullify the TLP on its way to the link.
5	AFE	R	0h	ARI forwarding enable
4	CTD	R/W	0h	Setting this bit disables Completion Timeout in the device. This bit can also be written from the local management bus.
3-0	CTV	R/W	0h	Specifies the Completion Timeout value for the device. Allowable values are 0101 [sub-range 1] and 0110 [sub-range 2]. The corresponding timeout values are stored in the local management registers Completion Timeout Interval Registers 0 and 1, respectively. Value of 0 selects completion timeout from Completion-Timeout-Interval-Registers-0 in local management register.

Table 9-189. Register Call Summary for PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PCIE_DEV_CTRL_STATUS_2 Register \(Offset = E8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.42 PCIE_CORE_PFn_I_LINK_CAP_2_REG Register (Offset = ECh + formula) [reset = X]

PCIE_CORE_PFn_I_LINK_CAP_2_REG is shown in Figure 9-62 and described in Table 9-191.

Return to the [Summary Table](#).

This register advertises the supported link speeds of the Controller.

Offset = ECh + (n * 1000h); where n = 0h to 5h

Table 9-190. PCIE_CORE_PFn_I_LINK_CAP_2_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00ECh + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00ECh + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00ECh + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00ECh + formula

Figure 9-62. PCIE_CORE_PFn_I_LINK_CAP_2_REG Register

31	30	29	28	27	26	25	24
R31	R25						TWRTDPS
R-0h				R-0h			
R/W-1h				R/W-1h			
23	22	21	20	19	18	17	16
RTPDS	R3			LSORSSV			
R/W-1h		R-0h		R/W-0h			
15	14	13	12	11	10	9	8
R2			LSOGSSV				R1
R-0h			R/W-0h				R-0h
7	6	5	4	3	2	1	0
R1			SLSV				RESERVED
R-0h			R/W-Fh				R/W-X

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-191. PCIE_CORE_PFn_I_LINK_CAP_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R31	R	0h	Indicates support for the optional Device Readiness Status [DRS] capability. This capability is currently not supported in the Controller.
30-25	R25	R	0h	Reserved
24	TWRTDPS	R/W	1h	When set to 1b, this bit indicates that the associated Port supports detection and reporting of two Retimers presence. This bit is valid for both Downstream Ports and Upstream Ports.
23	RTPDS	R/W	1h	When set to 1b, this bit indicates that the associated Port supports detection and reporting of Retimer presence. This bit is valid for both Downstream Ports and Upstream Ports.
22-20	R3	R	0h	Reserved
19-16	LSORSSV	R/W	0h	If this field is non-zero, it indicates that the Port, when operating at the indicated speed[s] supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS.
15-13	R2	R	0h	Reserved
12-9	LSOGSSV	R/W	0h	If this field is non-zero, it indicates that the Port, when operating at the indicated speed[s] supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate.

Table 9-191. PCIE_CORE_PFn_I_LINK_CAP_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-5	R1	R	0h	Reserved
4-1	SLSV	R/W	Fh	<p>This field indicates the supported link speeds of the Controller. For each bit, a value of 1 indicates that the corresponding link speed is supported, while a value of 0 indicates that the corresponding speed is not supported.</p> <p>The bits corresponding to various link speeds are:</p> <p>Bit</p> <p>1 = Link Speed 2.5 GT/s, Bit</p> <p>2 = Link Speed 5 GT/s, Bit</p> <p>3 = Link Speed 8 GT/s, Bit</p> <p>4 = Link Speed 16 GT/s.</p> <p>This field is hardwired to 0001 [2.5 GT/s] when the PCIE_GENERATION_SEL strap pins of the Controller are set to 0, 0011 [2.5 and 5 GT/s] when the strap is set to 1, and 0111 [2.5, 5, and 8 GT/s] when the strap pin is set to 10, and 1111 [2.5, 5, 8 GT/s and 16 GT/s] when the strap pin is set to 11</p> <p>For PF0, this field can be written through the LM interface.</p>
0	RESERVED	R/W	X	

Table 9-192. Register Call Summary for PCIE_CORE_PFn_I_LINK_CAP_2_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_LINK_CAP_2_REG Register \(Offset = ECh + formula\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.43 PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2 Register (Offset = F0h + formula) [reset = 00010004h]

PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2 is shown in Figure 9-63 and described in Table 9-194.

Return to the [Summary Table](#).

This register contains control and status bits specific to the PCI Express link. All the fields marked RW or RW(STICKY) can also be written from the local management bus.

Offset = F0h + (n * 1000h); where n = 0h to 5h

Table 9-193.
PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00F0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00F0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00F0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00F0h + formula

Figure 9-63. PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2 Register

31	30	29	28	27	26	25	24
DMR	DCP			R21			
R-0h	R-0h			R-0h			
23	22	21	20	19	18	17	16
TWRTP	RTP	LE	EP3S	EP2S	EP1S	EQC	CDEL
R-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h	R-1h
15	14	13	12	11	10	9	8
CDE				CS	EMC	TM	
R/W-0h				R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
TM	SDE	HASD	EC	TLS			
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-4h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-194. PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DMR	R	0h	DRS is not supported by the Controller and hence this field is not implemented.
30-28	DCP	R	0h	DRS is not supported by the Controller and hence this field is not implemented.
27-24	R21	R	0h	Reserved
23	TWRTP	R	0h	When set to 1b, this bit indicates that two Retimers were present during the most recent Link negotiation.
22	RTP	R	0h	When set to 1b, this bit indicates that a Retimer was present during the most recent Link negotiation.

Table 9-194. PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	LE	R/W	0h	This bit can be set by the software running on the EndPoint to force the Endpoint to perform link equalization for 8.0 GT/s. Setting this bit causes the LTSSM of the Controller to enter the Recovery state and request its link partner to perform equalization. This bit is cleared when the LTSSM enters the Recovery.Equalization state. It can also be cleared by writing a 1 to this bit position by the host, or writing a 0 from the LMI. STICKY.
20	EP3S	R	0h	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully for 8.0 GT/s. STICKY.
19	EP2S	R	0h	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully for 8.0 GT/s. STICKY.
18	EP1S	R	0h	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully for 8.0 GT/s. STICKY.
17	EQC	R	0h	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed for 8.0 GT/s. STICKY.
16	CDEL	R	1h	This status bit indicates the current operating de-emphasis level of the transmitter [0 = -6 dB, 1 = -3.5 dB]. This field is undefined when link is not at Gen2 speed.
15-12	CDE	R/W	0h	This bit sets the de-emphasis level [for 5 GT/s operation] or the Transmitter Preset level [for 8 GT/s or 16 GT/s operation] when the LTSSM enters the Polling.Compliance state because of software setting the Enter Compliance bit in this register. It is used only when the link is running at 5 GT/s or 8 GT/s or 16 GT/s. At 5 GT/s, the only valid setting are 0 [-6 dB] and 1 [-3.5 dB]. STICKY.
11	CS	R/W	0h	When this bit is set to 1, the device will transmit SKP ordered sets between compliance patterns. STICKY.
10	EMC	R/W	0h	This field is intended for debug and compliance testing purposes only. If this bit is set to 1, the device will transmit the Modified Compliance Pattern when the LTSSM enters the Polling.Compliance substate. Note: Setting this bit alone will not cause the LTSSM to enter Polling.Compliance. The Enter Compliance bit must also be set and a Hot Reset needs to be initiated by Host to enter Polling.Compliance. STICKY.

Table 9-194. PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-7	TM	R/W	0h	This field is intended for debug and compliance testing purposes only. It controls the non-de-emphasized voltage level at the transmitter outputs. Its encodings are: 000: Normal operating range. 001: 800 - 1200 mV for full swing and 400 - 700 mV for half swing. 010 - 111: See PCI Express Base Specification 2.0. This field is reset to 0 when the LTSSM enters the Polling.Configuration substate during link training. STICKY.
6	SDE	R	0h	This bit selects the de-emphasis level when the Controller is operating at 5 GT/s [0 = -6 dB, 1 = -3.5 dB]. This is reserved for Endpoints.
5	HASD	R/W	0h	When this bit is set, the LTSSM is prevented from changing the operating speed of the link, other than reducing the speed to correct unreliable operation of the link. STICKY
4	EC	R/W	0h	This bit is used to force the Endpoint device to enter the Compliance mode. Software sets this bit to 1 and initiates a hot reset to force the device into the Compliance mode. The target speed for the Compliance mode is determined by the Target Link Speed field of this register. STICKY.
3-0	TLS	R/W	4h	For an upstream component, this field sets an upper limit on Link operational speed during reconfiguration. Additionally for both upstream and downstream components, this field sets the target speed when the software forces the link into Compliance mode by setting the Enter Compliance bit in this register [0001 = 2.5 GT/s, 0010 = 5 GT/s, 0011 = 8 GT/s, 0100 = 16 GT/s]. The default value of this field is 0001 [2.5 GT/s] when the PCIE_GENERATION_SEL strap pins of the Controller are set to 0, 0010 [5 GT/s] when the strap is set to 1, 0011 [8 GT/s] when the strap pin is set to 10 , and 0100 [16 GT/s] when the strap pin is set to 11. These bits are STICKY.

Table 9-195. Register Call Summary for PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_LINK_CTRL_STATUS_2 Register \(Offset = F0h + formula\) \[reset = 00010004h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.44 PCIE_CORE_PFn_RSVD_03D_03F Register (Offset = F4h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_03D_03F is shown in [Figure 9-64](#) and described in [Table 9-197](#).

Return to the [Summary Table](#).

Reserved

Offset = F4h + (n * 1000h); where n = 0h to 5h

Table 9-196. PCIE_CORE_PFn_RSVD_03D_03F Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00F4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00F4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00F4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00F4h + formula

Figure 9-64. PCIE_CORE_PFn_RSVD_03D_03F Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-197. PCIE_CORE_PFn_RSVD_03D_03F Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-198. Register Call Summary for PCIE_CORE_PFn_RSVD_03D_03F

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_03D_03F Register \(Offset = F4h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.45 PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR Register (Offset = 100h + formula) [reset = 14020001h]

PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR is shown in Figure 9-65 and described in Table 9-200.

Return to the [Summary Table](#).

This is the first register in the PCI Express Advanced Error Reporting Capability Structure. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Offset = 100h + (n * 1000h); where n = 0h to 5h

Table 9-199.
PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0100h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0100h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0100h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0100h + formula

Figure 9-65. PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PEECI															
R/W-140h												R/W-2h				R-1h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-200. PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	140h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	2h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 4'h2, but can be modified from the local management bus.
15-0	PEECI	R	1h	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express AER Extended Capability Structure [0001 hex].

Table 9-201. Register Call Summary for PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_AER_ENHANCED_CAP_HDR Register \(Offset = 100h + formula\) \[reset = 14020001h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.46 PCIE_CORE_PFn_I_UNCORR_ERR_STATUS Register (Offset = 104h + formula) [reset = 0h]

PCIE_CORE_PFn_I_UNCORR_ERR_STATUS is shown in Figure 9-66 and described in Table 9-203.

Return to the [Summary Table](#).

This register provides the status of the various uncorrectable errors detected by the PCI Express Controller. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Uncorrectable Error Mask Register have no effect on the status bits of this register. The setting of an uncorrectable error status bit causes the Controller to generate an ERR_FATAL message if the corresponding severity bit of the Uncorrectable Error Severity Register is 1. If the severity bit is 0, however, there are two separate ways the error could be processed: (i) In certain cases, the uncorrectable error is treated as an Advisory Non-Fatal Error. These cases are treated as similar to correctable errors, causing the Controller to generate an ERR_COR message instead of an ERR_NONFATAL message. For details on these special cases, refer to Section 6.2.3.2.4 of the PCI Express Base Specifications, Version 1.1. (ii) In all other cases, the Controller sends an ERR_NONFATAL message when the error is detected. In all cases, the sending of the error message can be suppressed by setting the bit corresponding to the error type in the Uncorrectable Error Mask Register. For errors that are not Function-specific, the error status bus is set in the registers belonging to all the Functions associated with the link, but only a single message is generated for the entire link. In the case of certain errors detected by the Transaction Layer, the associated TLP header is logged in the Header Log Registers. All the RW1C bits can also be cleared from the local management bus by writing a 1 into the bit position.

Offset = 104h + (n * 1000h); where n = 0h to 5h

Table 9-202.
PCIE_CORE_PFn_I_UNCORR_ERR_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0104h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0104h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0104h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0104h + formula

Figure 9-66. PCIE_CORE_PFn_I_UNCORR_ERR_STATUS Register

31	30	29	28	27	26	25	24
R3							
R-0h							
23	22	21	20	19	18	17	16
R3	UIE	R2	URES	EES	MTS	ROS	UCS
R-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
CAS	CTS	FCPES	PTS	R1			
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h			
7	6	5	4	3	2	1	0
R1			DLPES	R0			
R-0h			R/W1C-0h	R-0h			

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-203. PCIE_CORE_PFn_I_UNCORR_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	R3	R	0h	N/A

Table 9-203. PCIE_CORE_PFn_I_UNCORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	UIE	R/W1C	0h	This bit is set when the Controller has detected an internal uncorrectable error [HAL parity error or an uncorrectable ECC error while reading from any of the RAMs]. This bit is also set in response to the client signaling an internal error through the input UNCORRECTABLE_ERROR_IN. This error is not Function-specific. This error is considered fatal by default, and is reported by sending an ERR_FATAL message. STICKY.
21	R2	R	0h	Reserved
20	URES	R/W1C	0h	This bit is set when the Controller has received a request from the link that it does not support. This error is not Function-specific. This error is considered non-fatal by default. In the special case described in Sections 6.2.3.2.4.1 of the PCI Express Specifications, the error is reported by sending an ERR_COR message. In all other cases, the error is reported by sending an ERR_NONFATAL message. The header of the received request that caused the error is logged in the Header Log Registers. STICKY.
19	EES	R/W1C	0h	This bit is set when the Controller has detected an ECRC error in a received TLP. This error is not Function-specific. The header of the received TLP with error is logged in the Header Log Registers. STICKY.
18	MTS	R/W1C	0h	This bit is set when the Controller receives a malformed TLP from the link. This error is not Function-specific. This error is considered fatal by default, and is reported by sending an ERR_FATAL message. The header of the received TLP with error is logged in the Header Log Registers. STICKY.
17	ROS	R/W1C	0h	This bit is set when the Controller receives a TLP in violation of the receive credit currently available. This error is not Function-specific. STICKY.
16	UCS	R/W1C	0h	This bit is set when the Controller has received an unexpected Completion packet from the link. This error is not Function-specific. STICKY.
15	CAS	R/W1C	0h	This bit is set when the Controller has returned the Completer Abort [CA] status to a request received from the link. This error is Function-specific. The header of the received request that caused the error is logged in the Header Log Registers. STICKY.

Table 9-203. PCIE_CORE_PFn_I_UNCORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	CTS	R/W1C	0h	This bit is set when the completion timer associated with an outstanding request times out. This error is Function-specific. This error is considered non-fatal by default. STICKY.
13	FCPES	R/W1C	0h	This bit is set when certain violations of the flow control protocol are detected by the Controller. Controller reports FCPE upon the following conditions: [i] InitFC/UpdateFC DLLP received which issues more than 2047 cumulative outstanding unused credits to the Transmitter for data payload or 127 for header. [ii] InitFC_P is received with Payload Credits less than 128B. Or [iii] InitFC_CPL is received with Payload Credits less than 128B. This error is not Function-specific STICKY.
12	PTS	R/W1C	0h	This bit is set when the Controller receives a poisoned TLP from the link. This error is Function-specific. This error is considered non-fatal by default. The error is reported by sending an ERR_NONFATAL message. The header of the received TLP with error is logged in the Header Log Registers. STICKY.
11-5	R1	R	0h	Reserved
4	DLPES	R/W1C	0h	This bit is set when the Controller receives an Ack or Nak DLLP whose sequence number does not correspond to that of an unacknowledged TLP or that of the last acknowledged TLP [for details, refer to PCI Express Base Specification 1.1, Section 3.5.2]. This error is not Function-specific, and is reported by Function 0. STICKY.
3-0	R0	R	0h	Reserved

Table 9-204. Register Call Summary for PCIE_CORE_PFn_I_UNCORR_ERR_STATUS

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_UNCORR_ERR_STATUS Register \(Offset = 104h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.47 PCIE_CORE_PFn_I_UNCORR_ERR_MASK Register (Offset = 108h + formula) [reset = 00400000h]

PCIE_CORE_PFn_I_UNCORR_ERR_MASK is shown in Figure 9-67 and described in Table 9-206.

Return to the [Summary Table](#).

The mask bits in this register control the reporting of uncorrectable errors. For each error type in the Uncorrectable Error Status Register, there is a corresponding bit in this register to mask its reporting. Setting the mask bit has the following effects: (i) The occurrence of the error is not reported to the Root Complex (by a PCI Express error message). (ii) The header of the TLP in which the error was detected is not logged in the Header Log Registers. (iii) The First Error Pointer in the Advanced Error Capabilities and Control Register is not updated on detection of the error. The individual bits of the mask register are described below. The bits marked RW can also be written from the local management bus.

Offset = 108h + (n * 1000h); where n = 0h to 5h

Table 9-205.
PCIE_CORE_PFn_I_UNCORR_ERR_MASK
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0108h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0108h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0108h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0108h + formula

Figure 9-67. PCIE_CORE_PFn_I_UNCORR_ERR_MASK Register

31	30	29	28	27	26	25	24
R7							
R-0h							
23	22	21	20	19	18	17	16
R7	UIEM	R6	UREM	EEM	MTM	ROM	UCM
R-0h	R/W-1h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CAM	CTM	FCPEM	PTM	R5			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
R5			DLPEM	R4			
R-0h			R/W-0h	R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-206. PCIE_CORE_PFn_I_UNCORR_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	R7	R	0h	Reserved
22	UIEM	R/W	1h	This bit is set to mask the reporting of internal errors. STICKY.
21	R6	R	0h	Reserved
20	UREM	R/W	0h	This bit is set to mask the reporting of unexpected requests received from the link. STICKY.
19	EEM	R/W	0h	This bit is set to mask the reporting of ECRC errors. STICKY.
18	MTM	R/W	0h	This bit is set to mask the reporting of malformed TLPs received from the link. STICKY.

Table 9-206. PCIE_CORE_PFn_I_UNCORR_ERR_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	ROM	R/W	0h	This bit is set to mask the reporting of violations of receive credit. STICKY.
16	UCM	R/W	0h	This bit is set to mask the reporting of unexpected Completions received by the Controller. STICKY.
15	CAM	R/W	0h	This bit is set to mask the reporting of the Controller sending a Completer Abort. STICKY.
14	CTM	R/W	0h	This bit is set to mask the reporting of Completion Timeouts. STICKY.
13	FCPEM	R/W	0h	This bit is set to mask the reporting of Flow Control Protocol Errors. STICKY.
12	PTM	R/W	0h	This bit is set to mask the reporting of a Poisoned TLP. STICKY.
11-5	R5	R	0h	Reserved
4	DLPEM	R/W	0h	This bit is set to mask the reporting of Data Link Protocol Errors. STICKY.
3-0	R4	R	0h	Reserved

Table 9-207. Register Call Summary for PCIE_CORE_PFn_I_UNCORR_ERR_MASK

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_UNCORR_ERR_MASK Register \(Offset = 108h + formula\) \[reset = 00400000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.48 PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY Register (Offset = 10Ch + formula) [reset = 00462030h]

PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY is shown in Figure 9-68 and described in Table 9-209.

Return to the [Summary Table](#).

The setting of this register determines whether an uncorrectable error is reported as a fatal error on non-fatal error to the Root Complex. If a severity bit of this register is 0, the corresponding error is reported by the Controller using an ERR_NONFATAL message. Otherwise, it is reported using an ERR_FATAL message. The bits marked RW can also be written from the local management bus.

Offset = 10Ch + (n * 1000h); where n = 0h to 5h

Table 9-208.
PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 010Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 010Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 010Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 010Ch + formula

Figure 9-68. PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY Register

31	30	29	28	27	26	25	24
R12							
R-0h							
23	22	21	20	19	18	17	16
R12	UIES	R11	URES	EES	MTS	ROS	UCS
R-0h	R/W-1h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
CAS	CTS	FCPES	PTS	R10			
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
R10		SDES	DLPER	R8			
R-0h		R-1h	R/W-1h	R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-209. PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	R12	R	0h	Reserved
22	UIES	R/W	1h	Severity of internal errors [0 = Non-Fatal, 1 = Fatal]. STICKY.
21	R11	R	0h	Reserved
20	URES	R/W	0h	Severity of unexpected requests received from the link [0 = Non-Fatal, 1 = Fatal]. STICKY.
19	EES	R/W	0h	Severity of ECRC errors [0 = Non-Fatal, 1 = Fatal]. STICKY.

Table 9-209. PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	MTS	R/W	1h	Severity of malformed TLPs received from the link [0 = Non-Fatal, 1 = Fatal]. STICKY.
17	ROS	R/W	1h	Severity of receive credit violations [0 = Non-Fatal, 1 = Fatal]. STICKY.
16	UCS	R/W	0h	Severity of unexpected Completions received by the Controller [0 = Non-Fatal, 1 = Fatal]. STICKY.
15	CAS	R/W	0h	Severity of sending a Completer Abort [0 = Non-Fatal, 1 = Fatal]. STICKY.
14	CTS	R/W	0h	Severity of Completion Timeouts [0 = Non-Fatal, 1 = Fatal]. STICKY.
13	FCPES	R/W	1h	Severity of Flow Control Protocol Errors [0 = Non-Fatal, 1 = Fatal]. STICKY.
12	PTS	R/W	0h	Severity of a Poisoned TLP error [0 = Non-Fatal, 1 = Fatal]. STICKY.
11-6	R10	R	0h	Reserved
5	SDES	R	1h	hard coded to 1
4	DLPER	R/W	1h	Severity of Data Link Protocol Errors [0 = Non-Fatal, 1 = Fatal]. STICKY.
3-0	R8	R	0h	Reserved

Table 9-210. Register Call Summary for PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_UNCORR_ERR_SEVERITY Register \(Offset = 10Ch + formula\) \[reset = 00462030h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.49 PCIE_CORE_PFn_I_CORR_ERR_STATUS Register (Offset = 110h + formula) [reset = 0h]

PCIE_CORE_PFn_I_CORR_ERR_STATUS is shown in [Figure 9-69](#) and described in [Table 9-212](#).

Return to the [Summary Table](#).

This register provides the status of the various correctable errors detected by the PCI Express Controller. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Correctable Error Mask Register have no effect on the status bits of this register. The setting of a correctable error status bit causes the Controller to generate an ERR_COR error message to the Root Complex if the error is not masked in the Correctable Error Mask Register. For errors that are not Function-specific, the error status bus is set in the registers belonging to all the Functions associated with the link, but only a single message is generated for the entire link. Header logging of received TLPs does not apply to correctable errors. All the RW1C bits can also be cleared from the local management bus by writing a 1 into the bit position.

Offset = 110h + (n * 1000h); where n = 0h to 5h

Table 9-211.
PCIE_CORE_PFn_I_CORR_ERR_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0110h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0110h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0110h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0110h + formula

Figure 9-69. PCIE_CORE_PFn_I_CORR_ERR_STATUS Register

31	30	29	28	27	26	25	24
R14							
R-0h							
23	22	21	20	19	18	17	16
R14							
R-0h							
15	14	13	12	11	10	9	8
HLOS	CIES	ANFES	RTTS	R13		RNRS	
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h		R/W1C-0h	
7	6	5	4	3	2	1	0
BDS	BTS	R12				RES	
R/W1C-0h	R/W1C-0h	R-0h				R/W1C-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-212. PCIE_CORE_PFn_I_CORR_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R14	R	0h	Reserved
15	HLOS	R/W1C	0h	This bit is set on a Header Log Register overflow, that is, when the header could not be logged in the Header Log Register because it is occupied by a previous header. STICKY.

Table 9-212. PCIE_CORE_PFn_I_CORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	CIES	R/W1C	0h	This bit is set when the Controller has detected an internal correctable error condition [a correctable ECC error while reading from any of the RAMs]. This bit is also set in response to the client signaling an internal error through the input CORRECTABLE_ERROR_IN. This error is not Function-specific. STICKY.
13	ANFES	R/W1C	0h	This bit is set when an uncorrectable error occurs, which is determined to belong to one of the special cases described in Section 6.2.3.2.4 of the PCI Express 2.0 Specifications. This causes the Controller to generate an ERR_COR message in place of an ERR_NONFATAL message. STICKY.
12	RTTS	R/W1C	0h	This bit is set when the replay timer in the Data Link Layer of the Controller times out, causing the Controller to retransmit a TLP. This error is not Function-specific. STICKY.
11-9	R13	R	0h	Reserved
8	RNRS	R/W1C	0h	This bit is set when the replay count rolls over after three re-transmissions of a TLP at the Data Link Layer of the Controller. This error is not Function-specific STICKY.
7	BDS	R/W1C	0h	This bit is set when an LCRC error is detected in a received DLLP, and no errors were detected by the Physical Layer. This error is not Function-specific. STICKY.
6	BTS	R/W1C	0h	This bit is set when an error is detected in a received TLP by the Data Link Layer of the Controller. The conditions causing this error are: [i] An LCRC error [ii] The packet terminates with EDB symbol, but its LCRC field does not equal the inverted value of the calculated CRC. This error is not Function-specific. STICKY.
5-1	R12	R	0h	Reserved
0	RES	R/W1C	0h	This bit is set when an error is detected in the receive side of the Physical Layer of the Controller [e.g. a bit error or coding violation]. This bit is set upon any of the following errors: [1] PHY reported 8B10B error, Disparity Error, Elastic Buffer Overflow Error, Underflow Error [2] GEN3 TLP, DLLP Framing Errors [3] OS Block Received Without EDS [4] Data Block Received After EDS [5] Illegal OS Block After EDS [6] OS Block Received After SKIP OS [7] OS Block Received After SDS [8] Sync Header Error [9] Loss of Gen3 Block Alignment This error is not Function-specific. STICKY.

Table 9-213. Register Call Summary for PCIE_CORE_PFn_I_CORR_ERR_STATUS

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_CORR_ERR_STATUS](#) Register (Offset = 110h + formula) [reset = 0h]: [0]
- [PCIE_CORE_EP_PF](#) Registers: [0] [1]

9.2.50 PCIE_CORE_PFn_I_CORR_ERR_MASK Register (Offset = 114h + formula) [reset = E000h]

PCIE_CORE_PFn_I_CORR_ERR_MASK is shown in Figure 9-70 and described in Table 9-215.

Return to the [Summary Table](#).

The mask bits in this register control the reporting of correctable errors. For each error type in the Correctable Error Status Register, there is a corresponding bit in this register to mask its reporting. When a mask bit is set, the occurrence of the error is not reported to the Root Complex (by a PCI Express error message). The individual bits of the mask register are described below. The bits marked RW can also be written from the local management bus.

Offset = 114h + (n * 1000h); where n = 0h to 5h

Table 9-214. PCIE_CORE_PFn_I_CORR_ERR_MASK Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0114h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0114h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0114h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0114h + formula

Figure 9-70. PCIE_CORE_PFn_I_CORR_ERR_MASK Register

31	30	29	28	27	26	25	24
R17							
R-0h							
23	22	21	20	19	18	17	16
R17							
R-0h							
15	14	13	12	11	10	9	8
HLOM	CIEM	ANFEM	RTTM	R16		RNRM	
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R-0h		R/W-0h	
7	6	5	4	3	2	1	0
BDM	BTM	R15				REM	
R/W-0h	R/W-0h	R-0h				R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-215. PCIE_CORE_PFn_I_CORR_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R17	R	0h	Reserved
15	HLOM	R/W	1h	This bit, when set, masks the generation of error messages in response to a Header Log register overflow. STICKY.
14	CIEM	R/W	1h	This bit, when set, masks the generation of error messages in response to a corrected internal error condition. STICKY.
13	ANFEM	R/W	1h	This bit, when set, masks the generation of error messages in response to an uncorrectable error occur, which is determined to belong to one of the special cases [as described in Section 6.2.3.2.4 of the PCI Express 2.0 Specifications]. STICKY.

Table 9-215. PCIE_CORE_PFn_I_CORR_ERR_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RTTM	R/W	0h	This bit, when set, masks the generation of error messages in response to a Replay Timer timeout event. STICKY.
11-9	R16	R	0h	Reserved
8	RNRM	R/W	0h	This bit, when set, masks the generation of error messages in response to a Replay Number Rollover event. STICKY.
7	BDM	R/W	0h	This bit, when set, masks the generation of error messages in response to a 'Bad DLLP' received. STICKY.
6	BTM	R/W	0h	This bit, when set, masks the generation of error messages in response to a 'Bad TLP' received. STICKY.
5-1	R15	R	0h	Reserved
0	REM	R/W	0h	This bit, when set, masks the generation of error messages in response to the Physical Layer errors STICKY.

Table 9-216. Register Call Summary for PCIE_CORE_PFn_I_CORR_ERR_MASK

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_CORR_ERR_MASK Register \(Offset = 114h + formula\) \[reset = E000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.51 PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL Register (Offset = 118h + formula) [reset = A0h]

PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL is shown in Figure 9-71 and described in Table 9-218.

Return to the [Summary Table](#).

This register contains a pointer to the first error that is reported in the Uncorrectable Error Status Register, and bits to enable ECRC generation and checking.

Offset = 118h + (n * 1000h); where n = 0h to 5h

Table 9-217.
PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0118h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0118h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0118h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0118h + formula

Figure 9-71. PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL Register

31	30	29	28	27	26	25	24
R18							
R-0h							
23	22	21	20	19	18	17	16
R18							
R-0h							
15	14	13	12	11	10	9	8
R18				TPLP	MHRE	MHRC	EEC
R-0h				R-0h	R-0h	R-0h	R/W-0h
7	6	5	4	3	2	1	0
ECC	EEG	EGC	FER				
R/W-1h	R/W-0h	R/W-1h	R-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-218. PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	R18	R	0h	Reserved
11	TPLP	R	0h	If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is RsvdP if the End-End TLP Prefix Supported bit is Clf Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined.
10	MHRE	R	0h	Setting this bit enables the Function to log multiple error headers in its Header Log Registers. It is hardwired to 0

Table 9-218. PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MHRC	R	0h	This bit is set when the Function has the capability to log more than one error header in its Header Log Registers. It is hardwired to 0.
8	EEC	R/W	0h	Setting this bit enables ECRC checking on the receive side of the Controller. This bit is writable from the local management bus. STICKY.
7	ECC	R/W	1h	This read-only bit indicates to the software that the device is capable of checking ECRC in packets received from the link. This bit is writable from the local management bus.
6	EEG	R/W	0h	Setting this bit enables the ECRC generation on the transmit side of the Controller. This bit is writable from the local management bus. STICKY.
5	EGC	R/W	1h	This read-only bit indicates to the software that the device is capable of generating ECRC in packets transmitted on the link. This bit is writable from the local management bus.
4-0	FER	R	0h	This is a 5-bit pointer to the bit position in the Uncorrectable Error Status Register corresponding to the error that was detected first. When there are multiple bits set in the Uncorrectable Error Status Register, this field informs the software which error was observed first. To prevent the field from being overwritten before software was able to read it, this field is not updated while the status bit pointed by it in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will update the First Error Pointer. Any uncorrectable error type, including the special cases where the error is reported using an ERR_COR message, will set the First Error Pointer [assuming the software has reset the error pointed by it in the Uncorrectable Error Status Register]. STICKY.

Table 9-219. Register Call Summary for PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_ADVCD_ERR_CAP_CTRL Register \(Offset = 118h + formula\) \[reset = A0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.52 PCIE_CORE_PFn_I_HDR_LOG_0 Register (Offset = 11Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_HDR_LOG_0 is shown in Figure 9-72 and described in Table 9-221.

Return to the [Summary Table](#).

This is the first of a set of four registers used to capture the header of a TLP received by the Controller from the link upon detection of an uncorrectable error. When multiple bits are set in the Uncorrectable Error Status Register, the captured header corresponds to the error that was detected first, that is, the error pointed by the First Error Pointer. To prevent the captured header from being over-written before software was able to read it, this register is not updated while the status bit pointed by the First Error Pointer in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will also cause the Header Log Registers to be updated. The doublewords of the TLP header are stored in the Header Log Registers with their bytes transposed. That is, the byte containing the Type/Format fields of the header is stored at bit positions 31:24 of the Header Log Register 0.

Offset = 11Ch + (n * 1000h); where n = 0h to 5h

Table 9-220. PCIE_CORE_PFn_I_HDR_LOG_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 011Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 011Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 011Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 011Ch + formula

Figure 9-72. PCIE_CORE_PFn_I_HDR_LOG_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD0																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-221. PCIE_CORE_PFn_I_HDR_LOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD0	R	0h	First DWORD of captured TLP header STICKY.

Table 9-222. Register Call Summary for PCIE_CORE_PFn_I_HDR_LOG_0

PCIE_CORE_EP_PF Registers
<ul style="list-style-type: none"> PCIE_CORE_PFn_I_HDR_LOG_0 Register (Offset = 11Ch + formula) [reset = 0h]: [0] PCIE_CORE_EP_PF Registers: [0] [1]

9.2.53 PCIE_CORE_PFn_I_HDR_LOG_1 Register (Offset = 120h + formula) [reset = 0h]

PCIE_CORE_PFn_I_HDR_LOG_1 is shown in Figure 9-73 and described in Table 9-224.

Return to the [Summary Table](#).

This register contains the second DWORD of the captured TLP header. The bytes are stored in transposed order.

Offset = 120h + (n * 1000h); where n = 0h to 5h

**Table 9-223. PCIE_CORE_PFn_I_HDR_LOG_1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0120h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0120h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0120h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0120h + formula

Figure 9-73. PCIE_CORE_PFn_I_HDR_LOG_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD1																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-224. PCIE_CORE_PFn_I_HDR_LOG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD1	R	0h	Second DWORD of captured TLP header STICKY.

Table 9-225. Register Call Summary for PCIE_CORE_PFn_I_HDR_LOG_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_I_HDR_LOG_1 Register \(Offset = 120h + formula\) \[reset = 0h\]: \[0\]](#)

9.2.54 PCIE_CORE_PFn_I_HDR_LOG_2 Register (Offset = 124h + formula) [reset = 0h]

PCIE_CORE_PFn_I_HDR_LOG_2 is shown in Figure 9-74 and described in Table 9-227.

Return to the [Summary Table](#).

This register contains the third DWORD of the captured TLP header. The bytes are stored in transposed order.

Offset = 124h + (n * 1000h); where n = 0h to 5h

Table 9-226. PCIE_CORE_PFn_I_HDR_LOG_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0124h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0124h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0124h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0124h + formula

Figure 9-74. PCIE_CORE_PFn_I_HDR_LOG_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD2																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-227. PCIE_CORE_PFn_I_HDR_LOG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD2	R	0h	Third DWORD of captured TLP header STICKY.

Table 9-228. Register Call Summary for PCIE_CORE_PFn_I_HDR_LOG_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_HDR_LOG_2 Register \(Offset = 124h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.55 PCIE_CORE_PFn_I_HDR_LOG_3 Register (Offset = 128h + formula) [reset = 0h]

PCIE_CORE_PFn_I_HDR_LOG_3 is shown in Figure 9-75 and described in Table 9-230.

Return to the [Summary Table](#).

If the captured TLP header is 4 DWORDs long, this register contains its fourth DWORD. If the captured header is a 3-DWORD header, this register is unused. The bytes of the DWORD are stored in this register in transposed order.

Offset = 128h + (n * 1000h); where n = 0h to 5h

Table 9-229. PCIE_CORE_PFn_I_HDR_LOG_3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0128h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0128h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0128h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0128h + formula

Figure 9-75. PCIE_CORE_PFn_I_HDR_LOG_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-230. PCIE_CORE_PFn_I_HDR_LOG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD3	R	0h	Fourth DWORD of captured TLP header STICKY.

Table 9-231. Register Call Summary for PCIE_CORE_PFn_I_HDR_LOG_3

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_HDR_LOG_3 Register \(Offset = 128h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.56 PCIE_CORE_PFn_RSVD_04B_04D Register (Offset = 12Ch + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_04B_04D is shown in [Figure 9-76](#) and described in [Table 9-233](#).

Return to the [Summary Table](#).

Reserved

Offset = 12Ch + (n * 1000h); where n = 0h to 5h

**Table 9-232. PCIE_CORE_PFn_RSVD_04B_04D
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 012Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 012Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 012Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 012Ch + formula

Figure 9-76. PCIE_CORE_PFn_RSVD_04B_04D Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-233. PCIE_CORE_PFn_RSVD_04B_04D Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-234. Register Call Summary for PCIE_CORE_PFn_RSVD_04B_04D

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_04B_04D Register \(Offset = 12Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.57 PCIE_CORE_PFn_I_TLP_PRE_LOG_0 Register (Offset = 138h + formula) [reset = 0h]

PCIE_CORE_PFn_I_TLP_PRE_LOG_0 is shown in [Figure 9-77](#) and described in [Table 9-236](#).

Return to the [Summary Table](#).

First TLP Prefix (if present) associated with the TLP whose header is in the Header Log Register.
The bytes are in transposed order.

Offset = 138h + (n * 1000h); where n = 0h to 5h

**Table 9-235. PCIE_CORE_PFn_I_TLP_PRE_LOG_0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0138h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0138h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0138h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0138h + formula

Figure 9-77. PCIE_CORE_PFn_I_TLP_PRE_LOG_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD1																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-236. PCIE_CORE_PFn_I_TLP_PRE_LOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD1	R	0h	First TLP Prefix of captured TLP STICKY.

Table 9-237. Register Call Summary for PCIE_CORE_PFn_I_TLP_PRE_LOG_0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_TLP_PRE_LOG_0 Register \(Offset = 138h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.58 PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR Register (Offset = 140h + formula) [reset = 1501000Eh]

PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR is shown in Figure 9-78 and described in Table 9-239.

Return to the [Summary Table](#).

This register is used to enable the Alternate Routing ID interpretation. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Offset = 140h + (n * 1000h); where n = 0h to 5h

Table 9-238.
PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0140h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0140h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0140h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0140h + formula

Figure 9-78. PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ARINCO												ARICV			
R/W-150h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PECID															
R-Eh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-239. PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	ARINCO	R/W	150h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	ARICV	R/W	1h	Specifies the SIG-assigned value for the version of the capability structure. This field is set to 1 by default, but can be modified independently for each Function from the local management bus
15-0	PECID	R	Eh	This field is hardwired to the Capability ID assigned by PCI-SIG to the ARI Extended Capability [000E hex].

Table 9-240. Register Call Summary for PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR

PCIE_CORE_EP_PF Registers

- PCIE_CORE_PFn_I_ARI_EXT_CAP_HDR Register (Offset = 140h + formula) [reset = 1501000Eh]: [0]
- PCIE_CORE_EP_PF Registers: [0] [1]

9.2.59 PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL Register (Offset = 144h + formula) [reset = X]

PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL is shown in Figure 9-79 and described in Table 9-242.

Return to the [Summary Table](#).

This location contains the ARI Capability Register and the ARI Control Register. The individual fields are described below.

Offset = 144h + (n * 1000h); where n = 0h to 5h

Table 9-241.
PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0144h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0144h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0144h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0144h + formula

Figure 9-79. PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL Register

31	30	29	28	27	26	25	24
ACR							
R-0h							
23	22	21	20	19	18	17	16
ACR							
R-0h							
15	14	13	12	11	10	9	8
NF							
R/W-1h							
7	6	5	4	3	2	1	0
RESERVED						AFGC	MFGC
R/W-X						R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-242. PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ACR	R	0h	ARI Control Register not implemented in this Controller. This field is hardwired to 0.
15-8	NF	R/W	1h	Points to the next Physical Function in the device. This field is set by default to point to the next Physical Function, 0 for last Function. It can be rewritten from the local management bus.
7-2	RESERVED	R/W	X	
1	AFGC	R	0h	Relevant only when ACS Capability is supported. This field is hardwired to 0.
0	MFGC	R	0h	Set when device supports arbitration at the Function Group-level. This field is hardwired to 0.

Table 9-243. Register Call Summary for PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_ARI_CAP_AND_CTRL Register \(Offset = 144h + formula\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.60 PCIE_CORE_PFn_RSVD_052_053 Register (Offset = 148h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_052_053 is shown in [Figure 9-80](#) and described in [Table 9-245](#).

Return to the [Summary Table](#).

Reserved

Offset = 148h + (n * 1000h); where n = 0h to 5h

**Table 9-244. PCIE_CORE_PFn_RSVD_052_053
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0148h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0148h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0148h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0148h + formula

Figure 9-80. PCIE_CORE_PFn_RSVD_052_053 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-245. PCIE_CORE_PFn_RSVD_052_053 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-246. Register Call Summary for PCIE_CORE_PFn_RSVD_052_053

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_052_053 Register \(Offset = 148h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.61 PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR Register (Offset = 150h + formula) [reset = 16010003h]

PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR is shown in Figure 9-81 and described in Table 9-248.

Return to the [Summary Table](#).

This register contains the PCI Express Extended Capability ID for Device Serial Number Capability, the capability version, and the pointer to the next capability structure.

Offset = 150h + (n * 1000h); where n = 0h to 5h

Table 9-247.
PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0150h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0150h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0150h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0150h + formula

Figure 9-81. PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SNNCO												DSNCV			
R/W-160h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PECID															
R-3h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-248. PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	SNNCO	R/W	160h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	DSNCV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus by writing into Function 0 from the local management bus.
15-0	PECID	R	3h	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express Device Serial Number Capability [0001 hex].

Table 9-249. Register Call Summary for PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_I_DEV_SER_NUM_CAP_HDR Register \(Offset = 150h + formula\) \[reset = 16010003h\]: \[0\]](#)

9.2.62 PCIE_CORE_PFn_I_DEV_SER_NUM_0 Register (Offset = 154h + formula) [reset = 0h]

PCIE_CORE_PFn_I_DEV_SER_NUM_0 is shown in [Figure 9-82](#) and described in [Table 9-251](#).

Return to the [Summary Table](#).

This read-only register stored the first 32 bits of the device's serial number. Its setting is common for all the Physical Functions, and can be modified by writing into this register in Function 0 from the local management bus.

Offset = 154h + (n * 1000h); where n = 0h to 5h

Table 9-250. PCIE_CORE_PFn_I_DEV_SER_NUM_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0154h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0154h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0154h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0154h + formula

Figure 9-82. PCIE_CORE_PFn_I_DEV_SER_NUM_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSND0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-251. PCIE_CORE_PFn_I_DEV_SER_NUM_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DSND0	R/W	0h	This field contains the first 32 bits of the device's serial number.

Table 9-252. Register Call Summary for PCIE_CORE_PFn_I_DEV_SER_NUM_0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DEV_SER_NUM_0 Register \(Offset = 154h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.63 PCIE_CORE_PFn_I_DEV_SER_NUM_1 Register (Offset = 158h + formula) [reset = 0h]

PCIE_CORE_PFn_I_DEV_SER_NUM_1 is shown in [Figure 9-83](#) and described in [Table 9-254](#).

Return to the [Summary Table](#).

This read-only register stored the last 32 bits of the device's serial number. Its setting is common for all the Physical Functions, and can be modified by writing into this register in Function 0 from the local management bus.

Offset = 158h + (n * 1000h); where n = 0h to 5h

Table 9-253. PCIE_CORE_PFn_I_DEV_SER_NUM_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0158h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0158h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0158h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0158h + formula

Figure 9-83. PCIE_CORE_PFn_I_DEV_SER_NUM_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSND1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-254. PCIE_CORE_PFn_I_DEV_SER_NUM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DSND1	R/W	0h	This field contains the last 32 bits of the device's serial number.

Table 9-255. Register Call Summary for PCIE_CORE_PFn_I_DEV_SER_NUM_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DEV_SER_NUM_1 Register \(Offset = 158h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.64 PCIE_CORE_PFn_RSVD_057 Register (Offset = 15Ch + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_057 is shown in [Figure 9-84](#) and described in [Table 9-257](#).

Return to the [Summary Table](#).

Reserved

Offset = 15Ch + (n * 1000h); where n = 0h to 5h

Table 9-256. PCIE_CORE_PFn_RSVD_057 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 015Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 015Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 015Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 015Ch + formula

Figure 9-84. PCIE_CORE_PFn_RSVD_057 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-257. PCIE_CORE_PFn_RSVD_057 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-258. Register Call Summary for PCIE_CORE_PFn_RSVD_057

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_057 Register \(Offset = 15Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.65 PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR Register (Offset = 160h + formula) [reset = 1B810004h]

PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR is shown in Figure 9-85 and described in Table 9-260.

Return to the [Summary Table](#).

This register contains the PCI Express Extended Capability ID for Power Budgeting Capability, its capability version, and the pointer to the next capability structure.

Offset = 160h + (n * 1000h); where n = 0h to 5h

Table 9-259.
PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0160h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0160h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0160h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0160h + formula

Figure 9-85. PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBNCO												PCV				PECID															
R/W-1B8h												R/W-1h				R-4h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-260. PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PBNCO	R/W	1B8h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	PCV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus by writing into Function 0 from the local management bus.
15-0	PECID	R	4h	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express Power Budgeting Capability [0004 hex].

Table 9-261. Register Call Summary for PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PWR_BDGTG_ENHC_CAP_HDR Register \(Offset = 160h + formula\) \[reset = 1B810004h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.66 PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL Register (Offset = 164h + formula) [reset = 0h]

PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL is shown in Figure 9-86 and described in Table 9-263.

Return to the [Summary Table](#).

This register is used to select the specific word of specific power-budgeting data returned on a read from the Power Budgeting Data Register. This version of the Controller stores power budgeting data for three distinct power states (D0, D1 and D3hot) for each Physical Function, which can be read from the Power Budgeting Data Register by indexing through this register, as described below.

Offset = 164h + (n * 1000h); where n = 0h to 5h

Table 9-262.
PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0164h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0164h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0164h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0164h + formula

Figure 9-86. PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																PBDN															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-263. PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R0	R	0h	N/A
7-0	PBDN	R/W	0h	This field selects the power budgeting data read from the Power Budgeting Data Register. Its settings are: 00: Selects power budgeting data for power state D0 MAX for the associated PF. 01: Selects power budgeting data for power state D0 SUSTAINED for the associated PF. 10: Selects power budgeting data for power state D3hot for the associated PF. 11: Selects power budgeting data for power state D1 for the associated PF. Others: Not a valid setting. A read from the Power Budgeting Data Register returns all zeroes.

Table 9-264. Register Call Summary for PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL

PCIE_CORE_EP_PF Registers

- PCIE_CORE_PFn_I_PWR_BDGTG_DATA_SEL Register (Offset = 164h + formula) [reset = 0h]: [0]
- PCIE_CORE_EP_PF Registers: [0] [1]

9.2.67 PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER Register (Offset = 168h + formula) [reset = 000B80F0h]

PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER is shown in Figure 9-87 and described in Table 9-266.

Return to the [Summary Table](#).

This read-only register returns the DWORD of Power Budgeting Data selected by the Data Select register. Each DWORD of the Power Budgeting Data describes the power usage of the device in a particular operating condition. All the fields can be modified independently for each PF by writing from the local management bus.

Offset = 168h + (n * 1000h); where n = 0h to 5h

Table 9-265.
PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER
R Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0168h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0168h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0168h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0168h + formula

Figure 9-87. PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R1										PR			TYPE		
R-0h										R/W-2h			R/W-7h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE		PS		PSS			DS		BP						
R/W-7h		R/W-0h		R/W-0h			R/W-0h		R/W-F0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-266. PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	R1	R	0h	Reserved
20-18	PR	R/W	2h	Specifies the power rail corresponding to the power management data in this register.
17-15	TYPE	R/W	7h	Specifies the operation condition for which the data applies.
14-13	PS	R/W	0h	Specifies the power management state of the Function, for which this power management data applies.
12-10	PSS	R/W	0h	Specifies the power management sub-state of the selected power state
9-8	DS	R/W	0h	Scale factor applicable to the Base Power field.
7-0	BP	R/W	F0h	Specifies base power[in watts] of the selected power state

Table 9-267. Register Call Summary for PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PWR_BDGTG_DATA_REGISTER Register \(Offset = 168h + formula\) \[reset = 000B80F0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.68 PCIE_CORE_PFn_I_PWR_BDGT_CAP Register (Offset = 16Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_PWR_BDGT_CAP is shown in Figure 9-88 and described in Table 9-269.

Return to the [Summary Table](#).

This register specifies whether the device power specified by this Capability Structure is included in the system power budget.

Offset = 16Ch + (n * 1000h); where n = 0h to 5h

Table 9-268. PCIE_CORE_PFn_I_PWR_BDGT_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 016Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 016Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 016Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 016Ch + formula

Figure 9-88. PCIE_CORE_PFn_I_PWR_BDGT_CAP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R4															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4															SA
R-0h															R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-269. PCIE_CORE_PFn_I_PWR_BDGT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R4	R	0h	Reserved
0	SA	R/W	0h	This bit is set to indicate that the device power specified by this Power Management Capability Structure is included in the system power budget. When this bit set, the software must exclude the device power reported by this Capability Structure from power calculations, when making power budgeting decisions. This bit is set to 0 by default, but its setting can be modified individually for each PF from the local management bus.

Table 9-270. Register Call Summary for PCIE_CORE_PFn_I_PWR_BDGT_CAP

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PWR_BDGT_CAP Register \(Offset = 16Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.69 PCIE_CORE_PFn_RSVD_05C_05F Register (Offset = 170h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_05C_05F is shown in [Figure 9-89](#) and described in [Table 9-272](#).

Return to the [Summary Table](#).

Reserved

Offset = 170h + (n * 1000h); where n = 0h to 5h

**Table 9-271. PCIE_CORE_PFn_RSVD_05C_05F
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0170h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0170h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0170h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0170h + formula

Figure 9-89. PCIE_CORE_PFn_RSVD_05C_05F Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-272. PCIE_CORE_PFn_RSVD_05C_05F Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-273. Register Call Summary for PCIE_CORE_PFn_RSVD_05C_05F

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_05C_05F Register \(Offset = 170h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.70 PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR Register (Offset = 180h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR is shown in Figure 9-90 and described in Table 9-275.

Return to the [Summary Table](#).

This register contains the PCI Express Extended Capability ID for the Resizable BAR Capability, its capability version, and the pointer to the next capability structure. This register is enabled only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register (Section 8.4.2.24). When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes.

Offset = 180h + (n * 1000h); where n = 0h to 5h

Table 9-274.
PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0180h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0180h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0180h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0180h + formula

Figure 9-90. PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R-0h												R-0h				R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-275. PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R	0h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R	0h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.
15-0	PECID	R	0h	This field is hardwired to the Capability ID assigned by PCI SIG to the Resizable BAR Capability [0015 hex].

Table 9-276. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_EXT_CAP_HDR Register \(Offset = 180h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.71 PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0 Register (Offset = 184h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0 is shown in Figure 9-91 and described in Table 9-278.

Return to the [Summary Table](#).

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4-22 can be modified from the local management bus.

Offset = 184h + (n * 1000h); where n = 0h to 5h

Table 9-277.
PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0184h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0184h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0184h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0184h + formula

Figure 9-91. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0 Register

31	30	29	28	27	26	25	24
R1							
R-0h							
23	22	21	20	19	18	17	16
A512G	A256G	A128G	A64G	A32G	A16G	A8G	A4G
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
A2G	A1G	A512M	A256M	A128M	A64M	A32M	A16M
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
A8M	A4M	A2M	A1M	R0			
R-0h	R-0h	R-0h	R-0h	R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-278. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R1	R	0h	Reserved
23	A512G	R	0h	Indicates that the BAR aperture can be set to 512G.
22	A256G	R	0h	Indicates that the BAR aperture can be set to 256G.
21	A128G	R	0h	Indicates that the BAR aperture can be set to 128G.
20	A64G	R	0h	Indicates that the BAR aperture can be set to 64G.
19	A32G	R	0h	Indicates that the BAR aperture can be set to 32G.
18	A16G	R	0h	Indicates that the BAR aperture can be set to 16G.
17	A8G	R	0h	Indicates that the BAR aperture can be set to 8G.
16	A4G	R	0h	Indicates that the BAR aperture can be set to 4G.
15	A2G	R	0h	Indicates that the BAR aperture can be set to 2G.
14	A1G	R	0h	Indicates that the BAR aperture can be set to 1G.
13	A512M	R	0h	Indicates that the BAR aperture can be set to 512M.

Table 9-278. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	A256M	R	0h	Indicates that the BAR aperture can be set to 256M.
11	A128M	R	0h	Indicates that the BAR aperture can be set to 128M.
10	A64M	R	0h	Indicates that the BAR aperture can be set to 64M.
9	A32M	R	0h	Indicates that the BAR aperture can be set to 32M.
8	A16M	R	0h	Indicates that the BAR aperture can be set to 16M.
7	A8M	R	0h	Indicates that the BAR aperture can be set to 8M.
6	A4M	R	0h	Indicates that the BAR aperture can be set to 4M.
5	A2M	R	0h	Indicates that the BAR aperture can be set to 2M.
4	A1M	R	0h	Indicates that the BAR aperture can be set to 1M.
3-0	R0	R	0h	Reserved

Table 9-279. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CAP_0 Register \(Offset = 184h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.72 PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0 Register (Offset = 188h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0 is shown in Figure 9-92 and described in Table 9-281.

Return to the [Summary Table](#).

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and also has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Offset = 188h + (n * 1000h); where n = 0h to 5h

Table 9-280.
PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0188h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0188h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0188h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0188h + formula

Figure 9-92. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3				BARS				RBARC				R2		BARI	
R-0h				R-0h				R-0h				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-281. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	R3	R	0h	Reserved
12-8	BARS	R	0h	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF [0 = 1M, 1 = 2M, ..., 12 = 4G]. This field can be modified independently for each PF from the local management bus.
7-5	RBARC	R	0h	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus. Please see the define den_db_Fx_RESIZABLE_BAR_COUNT values [where x is the function number] for default values of each function in the reg_defaults.v files.
4-3	R2	R	0h	Reserved

Table 9-281. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BARI	R	0h	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus. Please see the define den_db_Fx_RESIZABLE_BAR_CONTROL_REG0_BAR_INDEX values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-282. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_0 Register \(Offset = 188h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.73 PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1 Register (Offset = 18Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1 is shown in Figure 9-93 and described in Table 9-284.

Return to the [Summary Table](#).

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4-22 can be modified from the local management bus.

Offset = 18Ch + (n * 1000h); where n = 0h to 5h

Table 9-283.
PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 018Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 018Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 018Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 018Ch + formula

Figure 9-93. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1 Register

31	30	29	28	27	26	25	24
R1							
R-0h							
23	22	21	20	19	18	17	16
A512G	A256G	A128G	A64G	A32G	A16G	A8G	A4G
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
A2G	A1G	A512M	A256M	A128M	A64M	A32M	A16M
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
A8M	A4M	A2M	A1M	R0			
R-0h	R-0h	R-0h	R-0h	R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-284. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R1	R	0h	Reserved
23	A512G	R	0h	Indicates that the BAR aperture can be set to 512G.
22	A256G	R	0h	Indicates that the BAR aperture can be set to 256G.
21	A128G	R	0h	Indicates that the BAR aperture can be set to 128G.
20	A64G	R	0h	Indicates that the BAR aperture can be set to 64G.
19	A32G	R	0h	Indicates that the BAR aperture can be set to 32G.
18	A16G	R	0h	Indicates that the BAR aperture can be set to 16G.
17	A8G	R	0h	Indicates that the BAR aperture can be set to 8G.
16	A4G	R	0h	Indicates that the BAR aperture can be set to 4G.
15	A2G	R	0h	Indicates that the BAR aperture can be set to 2G.
14	A1G	R	0h	Indicates that the BAR aperture can be set to 1G.
13	A512M	R	0h	Indicates that the BAR aperture can be set to 512M.

Table 9-284. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	A256M	R	0h	Indicates that the BAR aperture can be set to 256M.
11	A128M	R	0h	Indicates that the BAR aperture can be set to 128M.
10	A64M	R	0h	Indicates that the BAR aperture can be set to 64M.
9	A32M	R	0h	Indicates that the BAR aperture can be set to 32M.
8	A16M	R	0h	Indicates that the BAR aperture can be set to 16M.
7	A8M	R	0h	Indicates that the BAR aperture can be set to 8M.
6	A4M	R	0h	Indicates that the BAR aperture can be set to 4M.
5	A2M	R	0h	Indicates that the BAR aperture can be set to 2M.
4	A1M	R	0h	Indicates that the BAR aperture can be set to 1M.
3-0	R0	R	0h	Reserved

Table 9-285. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CAP_1 Register \(Offset = 18Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.74 PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1 Register (Offset = 190h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1 is shown in Figure 9-94 and described in Table 9-287.

Return to the [Summary Table](#).

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and also has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Offset = 190h + (n * 1000h); where n = 0h to 5h

Table 9-286.
PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0190h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0190h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0190h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0190h + formula

Figure 9-94. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3				BARS				RBARC				R2		BARI	
R-0h				R-0h				R-0h				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-287. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	R3	R	0h	Reserved
12-8	BARS	R	0h	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF [0 = 1M, 1 = 2M, ... , 12 = 4G]. This field can be modified independently for each PF from the local management bus.
7-5	RBARC	R	0h	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus. Please see the define den_db_Fx_RESIZABLE_BAR_COUNT values [where x is the function number] for default values of each function in the reg_defaults.v files.
4-3	R2	R	0h	Reserved

Table 9-287. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BARI	R	0h	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus. Please see the define <code>den_db_Fx_RESIZABLE_BAR_CONTROL_REG0_BAR_INDEX</code> values [where x is the function number] for default values of each function in the <code>reg_defaults.v</code> files.

Table 9-288. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_1 Register \(Offset = 190h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.75 PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2 Register (Offset = 194h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2 is shown in Figure 9-95 and described in Table 9-290.

Return to the [Summary Table](#).

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4-22 can be modified from the local management bus.

Offset = 194h + (n * 1000h); where n = 0h to 5h

Table 9-289.
PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0194h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0194h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0194h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0194h + formula

Figure 9-95. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2 Register

31	30	29	28	27	26	25	24
R1							
R-0h							
23	22	21	20	19	18	17	16
A512G	A256G	A128G	A64G	A32G	A16G	A8G	A4G
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
A2G	A1G	A512M	A256M	A128M	A64M	A32M	A16M
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
A8M	A4M	A2M	A1M	R0			
R-0h	R-0h	R-0h	R-0h	R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-290. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R1	R	0h	Reserved
23	A512G	R	0h	Indicates that the BAR aperture can be set to 512G.
22	A256G	R	0h	Indicates that the BAR aperture can be set to 256G.
21	A128G	R	0h	Indicates that the BAR aperture can be set to 128G.
20	A64G	R	0h	Indicates that the BAR aperture can be set to 64G.
19	A32G	R	0h	Indicates that the BAR aperture can be set to 32G.
18	A16G	R	0h	Indicates that the BAR aperture can be set to 16G.
17	A8G	R	0h	Indicates that the BAR aperture can be set to 8G.
16	A4G	R	0h	Indicates that the BAR aperture can be set to 4G.
15	A2G	R	0h	Indicates that the BAR aperture can be set to 2G.
14	A1G	R	0h	Indicates that the BAR aperture can be set to 1G.
13	A512M	R	0h	Indicates that the BAR aperture can be set to 512M.

Table 9-290. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	A256M	R	0h	Indicates that the BAR aperture can be set to 256M.
11	A128M	R	0h	Indicates that the BAR aperture can be set to 128M.
10	A64M	R	0h	Indicates that the BAR aperture can be set to 64M.
9	A32M	R	0h	Indicates that the BAR aperture can be set to 32M.
8	A16M	R	0h	Indicates that the BAR aperture can be set to 16M.
7	A8M	R	0h	Indicates that the BAR aperture can be set to 8M.
6	A4M	R	0h	Indicates that the BAR aperture can be set to 4M.
5	A2M	R	0h	Indicates that the BAR aperture can be set to 2M.
4	A1M	R	0h	Indicates that the BAR aperture can be set to 1M.
3-0	R0	R	0h	Reserved

Table 9-291. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CAP_2 Register \(Offset = 194h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.76 PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2 Register (Offset = 198h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2 is shown in Figure 9-96 and described in Table 9-293.

Return to the [Summary Table](#).

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and also has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Offset = 198h + (n * 1000h); where n = 0h to 5h

Table 9-292.
PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0198h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0198h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0198h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0198h + formula

Figure 9-96. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3				BARS				RBARC				R2		BARI	
R-0h				R-0h				R-0h				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-293. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	R3	R	0h	Reserved
12-8	BARS	R	0h	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF [0 = 1M, 1 = 2M, ... , 12 = 4G]. This field can be modified independently for each PF from the local management bus.
7-5	RBARC	R	0h	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus. Please see the define den_db_Fx_RESIZABLE_BAR_COUNT values [where x is the function number] for default values of each function in the reg_defaults.v files.
4-3	R2	R	0h	Reserved

Table 9-293. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BARI	R	0h	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus. Please see the define <code>den_db_Fx_RESIZABLE_BAR_CONTROL_REG0_BAR_INDEX</code> values [where x is the function number] for default values of each function in the <code>reg_defaults.v</code> files.

Table 9-294. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_2 Register \(Offset = 198h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.77 PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3 Register (Offset = 19Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3 is shown in Figure 9-97 and described in Table 9-296.

Return to the [Summary Table](#).

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4-22 can be modified from the local management bus.

Offset = 19Ch + (n * 1000h); where n = 0h to 5h

Table 9-295.
PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 019Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 019Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 019Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 019Ch + formula

Figure 9-97. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3 Register

31	30	29	28	27	26	25	24
R1							
R-0h							
23	22	21	20	19	18	17	16
A512G	A256G	A128G	A64G	A32G	A16G	A8G	A4G
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
A2G	A1G	A512M	A256M	A128M	A64M	A32M	A16M
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
A8M	A4M	A2M	A1M	R0			
R-0h	R-0h	R-0h	R-0h	R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-296. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R1	R	0h	Reserved
23	A512G	R	0h	Indicates that the BAR aperture can be set to 512G.
22	A256G	R	0h	Indicates that the BAR aperture can be set to 256G.
21	A128G	R	0h	Indicates that the BAR aperture can be set to 128G.
20	A64G	R	0h	Indicates that the BAR aperture can be set to 64G.
19	A32G	R	0h	Indicates that the BAR aperture can be set to 32G.
18	A16G	R	0h	Indicates that the BAR aperture can be set to 16G.
17	A8G	R	0h	Indicates that the BAR aperture can be set to 8G.
16	A4G	R	0h	Indicates that the BAR aperture can be set to 4G.
15	A2G	R	0h	Indicates that the BAR aperture can be set to 2G.
14	A1G	R	0h	Indicates that the BAR aperture can be set to 1G.
13	A512M	R	0h	Indicates that the BAR aperture can be set to 512M.

Table 9-296. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	A256M	R	0h	Indicates that the BAR aperture can be set to 256M.
11	A128M	R	0h	Indicates that the BAR aperture can be set to 128M.
10	A64M	R	0h	Indicates that the BAR aperture can be set to 64M.
9	A32M	R	0h	Indicates that the BAR aperture can be set to 32M.
8	A16M	R	0h	Indicates that the BAR aperture can be set to 16M.
7	A8M	R	0h	Indicates that the BAR aperture can be set to 8M.
6	A4M	R	0h	Indicates that the BAR aperture can be set to 4M.
5	A2M	R	0h	Indicates that the BAR aperture can be set to 2M.
4	A1M	R	0h	Indicates that the BAR aperture can be set to 1M.
3-0	R0	R	0h	Reserved

Table 9-297. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CAP_3 Register \(Offset = 19Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.78 PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3 Register (Offset = 1A0h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3 is shown in [Figure 9-98](#) and described in [Table 9-299](#).

Return to the [Summary Table](#).

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and also has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Offset = 1A0h + (n * 1000h); where n = 0h to 5h

Table 9-298.
PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01A0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01A0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01A0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01A0h + formula

Figure 9-98. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3				BARS				RBARC				R2		BARI	
R-0h				R-0h				R-0h				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-299. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	R3	R	0h	Reserved
12-8	BARS	R	0h	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF [0 = 1M, 1 = 2M, ..., 12 = 4G]. This field can be modified independently for each PF from the local management bus.
7-5	RBARC	R	0h	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus. Please see the define den_db_Fx_RESIZABLE_BAR_COUNT values [where x is the function number] for default values of each function in the reg_defaults.v files.
4-3	R2	R	0h	Reserved

Table 9-299. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BARI	R	0h	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus. Please see the define <code>den_db_Fx_RESIZABLE_BAR_CONTROL_REG0_BAR_INDEX</code> values [where x is the function number] for default values of each function in the <code>reg_defaults.v</code> files.

Table 9-300. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_3 Register \(Offset = 1A0h + formula\) \[reset = 0h\]: \[0\]](#)

9.2.79 PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4 Register (Offset = 1A4h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4 is shown in Figure 9-99 and described in Table 9-302.

Return to the [Summary Table](#).

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4-22 can be modified from the local management bus.

Offset = 1A4h + (n * 1000h); where n = 0h to 5h

Table 9-301.
PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01A4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01A4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01A4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01A4h + formula

Figure 9-99. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4 Register

31	30	29	28	27	26	25	24
R1							
R-0h							
23	22	21	20	19	18	17	16
A512G	A256G	A128G	A64G	A32G	A16G	A8G	A4G
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
A2G	A1G	A512M	A256M	A128M	A64M	A32M	A16M
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
A8M	A4M	A2M	A1M	R0			
R-0h	R-0h	R-0h	R-0h	R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-302. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R1	R	0h	Reserved
23	A512G	R	0h	Indicates that the BAR aperture can be set to 512G.
22	A256G	R	0h	Indicates that the BAR aperture can be set to 256G.
21	A128G	R	0h	Indicates that the BAR aperture can be set to 128G.
20	A64G	R	0h	Indicates that the BAR aperture can be set to 64G.
19	A32G	R	0h	Indicates that the BAR aperture can be set to 32G.
18	A16G	R	0h	Indicates that the BAR aperture can be set to 16G.
17	A8G	R	0h	Indicates that the BAR aperture can be set to 8G.
16	A4G	R	0h	Indicates that the BAR aperture can be set to 4G.
15	A2G	R	0h	Indicates that the BAR aperture can be set to 2G.
14	A1G	R	0h	Indicates that the BAR aperture can be set to 1G.
13	A512M	R	0h	Indicates that the BAR aperture can be set to 512M.

Table 9-302. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	A256M	R	0h	Indicates that the BAR aperture can be set to 256M.
11	A128M	R	0h	Indicates that the BAR aperture can be set to 128M.
10	A64M	R	0h	Indicates that the BAR aperture can be set to 64M.
9	A32M	R	0h	Indicates that the BAR aperture can be set to 32M.
8	A16M	R	0h	Indicates that the BAR aperture can be set to 16M.
7	A8M	R	0h	Indicates that the BAR aperture can be set to 8M.
6	A4M	R	0h	Indicates that the BAR aperture can be set to 4M.
5	A2M	R	0h	Indicates that the BAR aperture can be set to 2M.
4	A1M	R	0h	Indicates that the BAR aperture can be set to 1M.
3-0	R0	R	0h	Reserved

Table 9-303. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CAP_4 Register \(Offset = 1A4h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.80 PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4 Register (Offset = 1A8h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4 is shown in [Figure 9-100](#) and described in [Table 9-305](#).

Return to the [Summary Table](#).

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and also has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Offset = 1A8h + (n * 1000h); where n = 0h to 5h

Table 9-304.
PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01A8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01A8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01A8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01A8h + formula

Figure 9-100. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3				BARS				RBARC				R2		BARI	
R-0h				R-0h				R-0h				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-305. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	R3	R	0h	Reserved
12-8	BARS	R	0h	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF [0 = 1M, 1 = 2M, ... , 12 = 4G]. This field can be modified independently for each PF from the local management bus.
7-5	RBARC	R	0h	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus. Please see the define den_db_Fx_RESIZABLE_BAR_COUNT values [where x is the function number] for default values of each function in the reg_defaults.v files.
4-3	R2	R	0h	Reserved

Table 9-305. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BARI	R	0h	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus. Please see the define <code>den_db_Fx_RESIZABLE_BAR_CONTROL_REG0_BAR_INDEX</code> values [where x is the function number] for default values of each function in the <code>reg_defaults.v</code> files.

Table 9-306. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_4 Register \(Offset = 1A8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.81 PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5 Register (Offset = 1ACh + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5 is shown in [Figure 9-101](#) and described in [Table 9-308](#).

Return to the [Summary Table](#).

This register advertises the available aperture settings of the first memory BAR of the associated Physical Function. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability (bit 31) of the associated Physical Function BAR Configuration Register 1. When the Resizable BAR Capability is not enabled, a read from this location returns all zeros. When the Resizable BAR Capability is enabled, any of the bits 4-22 can be modified from the local management bus.

Offset = 1ACh + (n * 1000h); where n = 0h to 5h

Table 9-307.
PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01ACh + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01ACh + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01ACh + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01ACh + formula

Figure 9-101. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5 Register

31	30	29	28	27	26	25	24
R1							
R-0h							
23	22	21	20	19	18	17	16
A512G	A256G	A128G	A64G	A32G	A16G	A8G	A4G
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
A2G	A1G	A512M	A256M	A128M	A64M	A32M	A16M
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
A8M	A4M	A2M	A1M	R0			
R-0h	R-0h	R-0h	R-0h	R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-308. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R1	R	0h	Reserved
23	A512G	R	0h	Indicates that the BAR aperture can be set to 512G.
22	A256G	R	0h	Indicates that the BAR aperture can be set to 256G.
21	A128G	R	0h	Indicates that the BAR aperture can be set to 128G.
20	A64G	R	0h	Indicates that the BAR aperture can be set to 64G.
19	A32G	R	0h	Indicates that the BAR aperture can be set to 32G.
18	A16G	R	0h	Indicates that the BAR aperture can be set to 16G.
17	A8G	R	0h	Indicates that the BAR aperture can be set to 8G.
16	A4G	R	0h	Indicates that the BAR aperture can be set to 4G.
15	A2G	R	0h	Indicates that the BAR aperture can be set to 2G.
14	A1G	R	0h	Indicates that the BAR aperture can be set to 1G.
13	A512M	R	0h	Indicates that the BAR aperture can be set to 512M.

Table 9-308. PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	A256M	R	0h	Indicates that the BAR aperture can be set to 256M.
11	A128M	R	0h	Indicates that the BAR aperture can be set to 128M.
10	A64M	R	0h	Indicates that the BAR aperture can be set to 64M.
9	A32M	R	0h	Indicates that the BAR aperture can be set to 32M.
8	A16M	R	0h	Indicates that the BAR aperture can be set to 16M.
7	A8M	R	0h	Indicates that the BAR aperture can be set to 8M.
6	A4M	R	0h	Indicates that the BAR aperture can be set to 4M.
5	A2M	R	0h	Indicates that the BAR aperture can be set to 2M.
4	A1M	R	0h	Indicates that the BAR aperture can be set to 1M.
3-0	R0	R	0h	Reserved

Table 9-309. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CAP_5 Register \(Offset = 1ACh + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.82 PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5 Register (Offset = 1B0h + formula) [reset = 0h]

PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5 is shown in Figure 9-102 and described in Table 9-311.

Return to the [Summary Table](#).

This register controls the aperture setting of the first memory BAR of the associated Physical Function, and also has a field that specifies the number of resizable BARs configurable through the Resizable BAR Capability Structure. This register is active only when the Resizable BAR Capability is enabled for the Physical Function by setting the Enable Resizable BAR Capability bit (bit 31) of the associated Physical Function BAR Configuration Register. When the Resizable BAR Capability is not enabled, a read from this location returns all zeroes. When the Resizable BAR Capability is enabled, all valid fields of this register can be modified from the local management bus.

Offset = 1B0h + (n * 1000h); where n = 0h to 5h

Table 9-310.
PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01B0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01B0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01B0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01B0h + formula

Figure 9-102. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3				BARS				RBARC				R2		BARI	
R-0h				R-0h				R-0h				R-0h		R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-311. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	R3	R	0h	Reserved
12-8	BARS	R	0h	When the Resizable BAR Capability is enabled for the Physical Function, this field controls the BAR aperture for the first BAR of the PF [0 = 1M, 1 = 2M, ... , 12 = 4G]. This field can be modified independently for each PF from the local management bus.
7-5	RBARC	R	0h	Specifies the number of BARs that can be configured through the Resizable BAR Capability Structure for this PF. This field can be modified independently for each PF from the local management bus. Please see the define den_db_Fx_RESIZABLE_BAR_COUNT values [where x is the function number] for default values of each function in the reg_defaults.v files.
4-3	R2	R	0h	Reserved

Table 9-311. PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BARI	R	0h	Specifies the index of the BAR controlled by this register. This field can be modified independently for each PF from the local management bus. Please see the define <code>den_db_Fx_RESIZABLE_BAR_CONTROL_REG0_BAR_INDEX</code> values [where x is the function number] for default values of each function in the <code>reg_defaults.v</code> files.

Table 9-312. Register Call Summary for PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_RESIZE_BAR_CTRL_5 Register \(Offset = 1B0h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.83 PCIE_CORE_PFO_I_LTR_EXT_CAP_HDR Register (Offset = 1B8h) [reset = 1C010018h]

PCIE_CORE_PFO_I_LTR_EXT_CAP_HDR is shown in Figure 9-103 and described in Table 9-314.

Return to the [Summary Table](#).

This register contains the PCI Express Extended Capability ID for the Latency Tolerance Reporting (LTR) Capability, its capability version, and the pointer to the next capability structure. This register is implemented only for Physical Function 0. A read from this address of other Physical Functions configuration space returns all zeroes.

Table 9-313.
PCIE_CORE_PFO_I_LTR_EXT_CAP_HDR Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01B8h

Figure 9-103. PCIE_CORE_PFO_I_LTR_EXT_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R/W-1C0h												R/W-1h				R-18h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-314. PCIE_CORE_PFO_I_LTR_EXT_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	1C0h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.
15-0	PECID	R	18h	This field is hardwired to the Capability ID assigned by PCI SIG to the Latency Tolerance Reporting Capability [0018 hex].

Table 9-315. Register Call Summary for PCIE_CORE_PFO_I_LTR_EXT_CAP_HDR

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_LTR_EXT_CAP_HDR Register \(Offset = 1B8h\) \[reset = 1C010018h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.84 PCIE_CORE_PF0_I_LTR_SNOOP_LAT Register (Offset = 1BCh) [reset = 0h]

PCIE_CORE_PF0_I_LTR_SNOOP_LAT is shown in Figure 9-104 and described in Table 9-317.

Return to the [Summary Table](#).

This register contains the maximum snoop latency and the maximum no-snoop latency that the device is allowed to request in an LTR message it originates.

Table 9-316. PCIE_CORE_PF0_I_LTR_SNOOP_LAT Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01BCh

Figure 9-104. PCIE_CORE_PF0_I_LTR_SNOOP_LAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R1			MNSLS			MNSL									
R-0h			R/W-0h			R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0			MSLS			MSL									
R-0h			R/W-0h			R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-317. PCIE_CORE_PF0_I_LTR_SNOOP_LAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	R1	R	0h	Reserved
28-26	MNSLS	R/W	0h	Specifies the scale value for the Max No-Snoop Latency. When the setting of this field is non-zero, the actual snoop latency is determined by multiplying the Max No-Snoop Latency by the following scale factors: 001: 32 ns, 010: 1024 ns, 011: 32,768 ns, 100: 1,047,576 ns, 101: 33,554,432 ns, 110- 111: Reserved
25-16	MNSL	R/W	0h	When multiplied by the value of the Max No-Snoop Latency Scale, this field defines the maximum no-snoop value the device is permitted to request in an LTR message. This field can be written independently for each Physical Function from the local management bus.
15-13	R0	R	0h	Reserved

Table 9-317. PCIE_CORE_PFO_I_LTR_SNOOP_LAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	MSLS	R/W	0h	Specifies the scale value for the Max Snoop Latency. When the setting of this field is non-zero, the actual snoop latency is determined by multiplying the Max Snoop Latency by the following scale factors: 001: 32 ns, 010: 1024 ns, 011: 32,768 ns, 100: 1,047,576 ns, 101: 33,554,432 ns, 110- 111: Reserved
9-0	MSL	R/W	0h	When multiplied by the value of the Max Snoop Latency Scale, this field defines the maximum snoop value the device is permitted to request in an LTR message. This field can be written independently for each Physical Function from the local management bus.

Table 9-318. Register Call Summary for PCIE_CORE_PFO_I_LTR_SNOOP_LAT

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_LTR_SNOOP_LAT Register \(Offset = 1BCh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.85 PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG Register (Offset = 1C0h + formula) [reset = 20010016h]

PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG is shown in Figure 9-105 and described in Table 9-320.

Return to the [Summary Table](#).

This location contains the PCI Express Extended Capability ID for DPA Capability and the offset to the next capability block.

Offset = 1C0h + (n * 1000h); where n = 0h to 5h

Table 9-319.
PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01C0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01C0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01C0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01C0h + formula

Figure 9-105. PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R/W-200h												R/W-1h				R-16h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-320. PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	200h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.
15-0	PECID	R	16h	This field is hardwired to the Capability ID assigned by PCI SIG to the Dynamic Power Allocation Reporting Capability

Table 9-321. Register Call Summary for PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG

PCIE_CORE_EP_PF Registers	
•	PCIE_CORE_PFn_I_DPA_EXT_CAP_HEADER_REG Register (Offset = 1C0h + formula) [reset = 20010016h]: [0]
•	PCIE_CORE_EP_PF Registers: [0] [1]

9.2.86 PCIE_CORE_PFn_I_DPA_CAP_REG Register (Offset = 1C4h + formula) [reset = 08100007h]

PCIE_CORE_PFn_I_DPA_CAP_REG is shown in [Figure 9-106](#) and described in [Table 9-323](#).

Return to the [Summary Table](#).

This register contains the DPA capability parameters for the associated Function.

Offset = 1C4h + (n * 1000h); where n = 0h to 5h

Table 9-322. PCIE_CORE_PFn_I_DPA_CAP_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01C4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01C4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01C4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01C4h + formula

Figure 9-106. PCIE_CORE_PFn_I_DPA_CAP_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TLV1								TLV0							
R/W-8h								R/W-10h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R2		PAS		R1		TLU		R0		MNS					
R-0h		R/W-0h		R-0h		R/W-0h		R-0h		R/W-7h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-323. PCIE_CORE_PFn_I_DPA_CAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TLV1	R/W	8h	Specifies the second of the two transition latency values for the substates. The unit of latency is specified by the Transition Latency Unit field of this register. Please see the define <code>den_db_Fx_DPA_CAPABILITY_REG_TRANSITION_VALUE1</code> values [where x is the function number] for default values of each function in the <code>reg_defaults.v</code> files.
23-16	TLV0	R/W	10h	Specifies the transition latency for the substate. Each of the 32 substates may specify one of the two transition latency values. This field contains the first of the two latency values. The unit of latency is specified by the Transition Latency Unit field of this register. Please see the define <code>den_db_Fx_DPA_CAPABILITY_REG_TRANSITION_VALUE0</code> values [where x is the function number] for default values of each function in the <code>reg_defaults.v</code> files.
15-14	R2	R	0h	Reserved

Table 9-323. PCIE_CORE_PFn_I_DPA_CAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	PAS	R/W	0h	This is the scale used to compute the actual power from the values specified in the Dynamic Power Allocation Array Registers 0 - 7. The actual power in Watts is obtained by multiplying the value in the Dynamic Power Allocation Array Register by this scale factor [00 = 10x, 01 = 1x, 10 = 0.1x, 11 = 0.01x]. Please see the define den_db_Fx_DPA_CAPABILITY_REG_POWER_ALLOCATION_SCALE values [where x is the function number] for default values of each function in the reg_defaults.v files.
11-10	R1	R	0h	Reserved
9-8	TLU	R/W	0h	This is the unit of the transition latencies specified in the Transition Latency Value 0 and Transition Latency Value 1 fields of this register [00 = 1 ms, 01 = 10 ms, 10 = 100 ms, 11 = reserved]. Please see the define den_db_Fx_DPA_CAPABILITY_REG_TRANSITION_LATENCY_UNIT values [where x is the function number] for default values of each function in the reg_defaults.v files.
7-5	R0	R	0h	Reserved
4-0	MNS	R/W	7h	Maximum number of DPA substates supported by the Function [the value in this field is the number of substates minus 1]. Please see the define den_db_Fx_DPA_CAPABILITY_REG_SUBSTATE_MAX values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-324. Register Call Summary for PCIE_CORE_PFn_I_DPA_CAP_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DPA_CAP_REG Register \(Offset = 1C4h + formula\) \[reset = 08100007h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.87 PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG Register (Offset = 1C8h + formula) [reset = 0h]

PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG is shown in [Figure 9-107](#) and described in [Table 9-326](#).

Return to the [Summary Table](#).

This location contains Transition Latency Indicator bits for the DPA substates.

Offset = 1C8h + (n * 1000h); where n = 0h to 5h

Table 9-325.
PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01C8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01C8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01C8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01C8h + formula

Figure 9-107. PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLIN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-326. PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TLIN	R/W	0h	Bit i of this register indicates the choice of the transition latency value for substate i. A setting of 0 indicates that Transition Latency Value 0 from the DPA Capability Register applies to this substate a setting of 1 indicates that Transition Latency Value 1 applies. Please see the define den_db_Fx_DPA_TRANSITION_LATENCY values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-327. Register Call Summary for PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DPA_LAT_INDICATOR_REG Register \(Offset = 1C8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.88 PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG Register (Offset = 1CCh + formula) [reset = 100h]

PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG is shown in Figure 9-108 and described in Table 9-329.

Return to the [Summary Table](#).

This location contains the DPA Control Register and the DPA Status Register.

Offset = 1CCh + (n * 1000h); where n = 0h to 5h

Table 9-328.
PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01CCh + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01CCh + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01CCh + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01CCh + formula

Figure 9-108. PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R5										SC					
R-0h										R/W-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4							SCE	R3			SS				
R-0h							R/W-1h			R-0h			R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-329. PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	R5	R	0h	Reserved
20-16	SC	R/W	0h	<p>This field is used to initiate a transition of the Function's DPA to a new substate.</p> <p>To initiate the transition, software must write the desired substate value into this field and wait for the transition latency of the substate for the Function to complete the transition.</p> <p>This field can also be written from the local management bus.</p> <p>All substate transitions are disabled when the Substate Control Enabled bit is 0.</p> <p>The Controller generates a one-cycle pulse on the output DPA_INTERRUPT when the value if this field is changed [bit 0 is for PF 0 and so on]</p> <p>This interrupt informs the client of the request from software to change the DPA substate.</p> <p>In response, the client must read the Substate Control field from this register to determine the new substate, and perform the actions necessary to effect the substate change.</p> <p>On completion of the substate change, the client must update the Substate Status field to reflect the new substate the function is in.</p>
15-9	R4	R	0h	Reserved

Table 9-329. PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SCE	R/W	1h	This bit enables the Substate Control field. This bit is initialized to 1 by the hardware on a power-on reset or a Function-Level Reset. Software may clear this bit by writing a 1 to this bit position, but cannot set this bit directly through a configuration write. Clearing this bit disables the Substate Control field, thus preventing further substate transitions for this Function. This bit can be set to 0 or 1 through the local management bus, by writing a 0 or 1, respectively.
7-5	R3	R	0h	Reserved
4-0	SS	R/W	0h	This field provides the current DPA substate of this Function. This field is writable from the local management bus, and must be updated by the local software running on the EndPoint upon completion of a DPA transition to a new substate.

Table 9-330. Register Call Summary for PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DPA_CTRL_STATUS_REG Register \(Offset = 1CCh + formula\) \[reset = 100h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.89 PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0 Register (Offset = 1D0h + formula) [reset = 03020100h]

PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0 is shown in Figure 9-109 and described in Table 9-332.

Return to the [Summary Table](#).

This is a register in an array of 2 registers that contain the power allocations for the DPA substates. Each location contains power allocation values for four substates, 8 bits per substate. The value in each 8-bit field, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.

Offset = 1D0h + (n * 1000h); where n = 0h to 5h

Table 9-331.
PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01D0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01D0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01D0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01D0h + formula

Figure 9-109. PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPA3_0								SPA2_0								SPA1_0								SPA0_0							
R/W-3h								R/W-2h								R/W-1h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-332. PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SPA3_0	R/W	3h	This field contains the power allocation for the DPA substate #3 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.
23-16	SPA2_0	R/W	2h	This field contains the power allocation for the DPA substate #2 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.
15-8	SPA1_0	R/W	1h	This field contains the power allocation for the DPA substate #1 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.
7-0	SPA0_0	R/W	0h	This field contains the power allocation for the DPA substate #0 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.

Table 9-333. Register Call Summary for PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG0 Register \(Offset = 1D0h + formula\) \[reset = 03020100h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.90 PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1 Register (Offset = 1D4h + formula) [reset = 07060504h]

PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1 is shown in Figure 9-110 and described in Table 9-335.

Return to the [Summary Table](#).

This is a register in an array of 2 registers that contain the power allocations for the DPA substates. Each location contains power allocation values for four substates, 8 bits per substate. The value in each 8-bit field, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.

Offset = 1D4h + (n * 1000h); where n = 0h to 5h

Table 9-334.
PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01D4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01D4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01D4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01D4h + formula

Figure 9-110. PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPA3_1								SPA2_1								SPA1_1								SPA0_1							
R/W-7h								R/W-6h								R/W-5h								R/W-4h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-335. PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SPA3_1	R/W	7h	This field contains the power allocation for the DPA substate #7 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.
23-16	SPA2_1	R/W	6h	This field contains the power allocation for the DPA substate #6 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.
15-8	SPA1_1	R/W	5h	This field contains the power allocation for the DPA substate #5 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.
7-0	SPA0_1	R/W	4h	This field contains the power allocation for the DPA substate #4 covered by this register. This value, when multiplied by the Power Allocation Scale programmed in the DPA Capability Register, provides the power associated with the corresponding substate in Watts.

Table 9-336. Register Call Summary for PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DPA_POWER_ALLOC_REG1 Register \(Offset = 1D4h + formula\) \[reset = 07060504h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.91 PCIE_CORE_PFn_RSVD_07C_07F Register (Offset = 1D8h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_07C_07F is shown in [Figure 9-111](#) and described in [Table 9-338](#).

Return to the [Summary Table](#).

Reserved

Offset = 1D8h + (n * 1000h); where n = 0h to 5h

Table 9-337. PCIE_CORE_PFn_RSVD_07C_07F Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 01D8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 01D8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 01D8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 01D8h + formula

Figure 9-111. PCIE_CORE_PFn_RSVD_07C_07F Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-338. PCIE_CORE_PFn_RSVD_07C_07F Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-339. Register Call Summary for PCIE_CORE_PFn_RSVD_07C_07F

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_07C_07F Register \(Offset = 1D8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.92 PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG Register (Offset = 200h + formula) [reset = 30010010h]

PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG is shown in Figure 9-112 and described in Table 9-341.

Return to the [Summary Table](#).

This location contains the PCI Express Extended Capability ID for SR-IOV and the offset to the next capability block.

Offset = 200h + (n * 1000h); where n = 0h to 5h

Table 9-340.
PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0200h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0200h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0200h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0200h + formula

Figure 9-112. PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R/W-300h												R/W-1h				R-10h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-341. PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	300h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	1h	Specifies the SIG-assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each Function from the local management bus.
15-0	PECID	R	10h	This field is hardwired to the Capability ID assigned by PCI-SIG to the SR-IOV Extended Capability Structure [0010 hex].

Table 9-342. Register Call Summary for PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_SRIOV_EXT_CAP_HEADER_REG Register \(Offset = 200h + formula\) \[reset = 30010010h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.93 PCIE_CORE_PFn_I_SRIOV_CAP_REG Register (Offset = 204h + formula) [reset = 2h]

PCIE_CORE_PFn_I_SRIOV_CAP_REG is shown in Figure 9-113 and described in Table 9-344.

Return to the [Summary Table](#).

This register defines various capabilities of the SR-IOV implementation.

Offset = 204h + (n * 1000h); where n = 0h to 5h

Table 9-343. PCIE_CORE_PFn_I_SRIOV_CAP_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0204h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0204h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0204h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0204h + formula

Figure 9-113. PCIE_CORE_PFn_I_SRIOV_CAP_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31				VFT10RS		ACHP	VFMC
R-0h				R-0h		R/W-1h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-344. PCIE_CORE_PFn_I_SRIOV_CAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	R31	R	0h	Reserved
2	VFT10RS	R	0h	If set all VFs associated with this PF supports 1-bit requester capability otherwise, the VF does not. This bit can be disabled using local management register.
1	ACHP	R/W	1h	A 1 in this bit position indicates that the ARI Capable Hierarchy bit in the SR-IOV Control Register is preserved across certain power state transitions [see the PCI-SIG Single Root IO Virtualization and Sharing Specifications, Version 1.1, Section 3.3.3.5 for details]. This bit is set to 1 by default, but can be modified from the local management bus.
0	VFMC	R	0h	Set when the Controller supports VF migration. Hardwired to 0.

Table 9-345. Register Call Summary for PCIE_CORE_PFn_I_SRIOV_CAP_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_SRIOV_CAP_REG Register \(Offset = 204h + formula\) \[reset = 2h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.94 PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG Register (Offset = 208h + formula) [reset = 0h]

PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG is shown in Figure 9-114 and described in Table 9-347.

Return to the [Summary Table](#).

This location contains the SR-IOV Control Register and the SR-IOV Status Register.

Offset = 208h + (n * 1000h); where n = 0h to 5h

Table 9-346.
PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0208h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0208h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0208h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0208h + formula

Figure 9-114. PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG Register

31	30	29	28	27	26	25	24
SSR							
R-0h							
23	22	21	20	19	18	17	16
SSR							
R-0h							
15	14	13	12	11	10	9	8
R15							
R-0h							
7	6	5	4	3	2	1	0
R15	T10RE	ARIE	VFMSE	VFMIE	VFME	VFE	
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-347. PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SSR	R	0h	Not implemented.
15-6	R15	R	0h	Reserved
5	T10RE	R	0h	10bit TAGs generation are not supported in this configuration.
4	ARIE	R/W	0h	This bit enables the ARI mode for Virtual Functions. ARI Capable Hierarchy is only present in the lowest numbered PF which is enabled [for example PF0] and affects all PFs of the Device. ARI Capable Hierarchy is Read Only Zero in other PFs of a Device.
3	VFMSE	R/W	0h	This bit must be set to allow access to the memory space of the VFs associated with this PF.
2	VFMIE	R/W	0h	Not supported. Hardwired to 0
1	VFME	R/W	0h	Not supported. Hardwired to 0
0	VFE	R/W	0h	This bit must be set to enable the VFs associated with this PF.

Table 9-348. Register Call Summary for PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_SRIOV_CTRL_STATUS_REG](#) Register (Offset = 208h + formula) [reset = 0h]: [0]
- [PCIE_CORE_EP_PF](#) Registers: [0] [1]

9.2.95 PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG Register (Offset = 20Ch + formula) [reset = X]

PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG is shown in Figure 9-115 and described in Table 9-350.

Return to the [Summary Table](#).

This location contains registers that specify the initial and the total number Virtual Functions (VFs) in the device.

Offset = 20Ch + (n * 1000h); where n = 0h to 5h

Table 9-349.
PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 020Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 020Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 020Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 020Ch + formula

Figure 9-115. PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											TVF					RESERVED												IVF			
R/W-X											R/W-4h					R/W-X												R/W-4h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-350. PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	TVF	R/W	4h	This field contains the total number of VFs per PF. Its default setting is identical to that of InitialVFs. This field can be modified using local management registers.
15-5	RESERVED	R/W	X	
4-0	IVF	R/W	4h	This field contains the initial number of VFs configured for each PF. This field can be modified using local management registers. Please see the define den_db_PFx_TOTAL_VF_COUNT values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-351. Register Call Summary for PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_INITIAL_TOTAL_VFS_REG Register \(Offset = 20Ch + formula\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.96 PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG Register (Offset = 210h + formula) [reset = X]

PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG is shown in Figure 9-116 and described in Table 9-353.

Return to the [Summary Table](#).

This location contains the Function Dependency Link that defines VF dependencies, and the NumVFs register that stores the number of VFs configured.

Offset = 210h + (n * 1000h); where n = 0h to 5h

Table 9-352.
PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0210h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0210h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0210h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0210h + formula

Figure 9-116. PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FDL								NVF															
R/W-X								R/W-0h								R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-353. PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	FDL	R/W	0h	This field is used to specify dependencies between PFs. It can be modified independently for each Function from the local management bus. Please see the define den_db_Fx_SR_IOV_FUNCTION_DEPENDENCY_LINK values [where x is the function number] for default values of each function in the reg_defaults.v files.
15-0	NVF	R/W	0h	This field must be set by the software to the number of VFs that it wants to enable for each PF. This field can be changed only when the VF Enable bit in the SR-IOV Control Register is 0. Its value should not exceed the setting of TotalVFs for the corresponding Physical Function. This field can also be written from the local management bus.

Table 9-354. Register Call Summary for PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_FUNC_DEP_LINK_NUMVFS_REG Register \(Offset = 210h + formula\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.97 PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG Register (Offset = 214h + formula) [reset = 00010006h]

PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG is shown in [Figure 9-117](#) and described in [Table 9-356](#).

Return to the [Summary Table](#).

Specifies the offset and stride values for VF address assignment.

Offset = 214h + (n * 1000h); where n = 0h to 5h

Table 9-355.
PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0214h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0214h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0214h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0214h + formula

Figure 9-117. PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFS																FVFO															
R-1h																R/W-6h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-356. PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VFS	R	1h	Stride value used to assign RIDs for VFs. The stride value is hardwired to 1 for all Physical Functions.
15-0	FVFO	R/W	6h	Offset of First VF relative to its PF. This field can be re-written independently for each PF from the local management bus. Please see the define den_db_Fx_VF_ADDR_OFFSET values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-357. Register Call Summary for PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VF_OFFSET_STRIDE_REG Register \(Offset = 214h + formula\) \[reset = 00010006h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.98 PCIE_CORE_PFn_I_VF_DEVICE_ID_REG Register (Offset = 218h + formula) [reset = 01000000h]

PCIE_CORE_PFn_I_VF_DEVICE_ID_REG is shown in [Figure 9-118](#) and described in [Table 9-359](#).

Return to the [Summary Table](#).

This register specifies the VF device id for the device.

Offset = 218h + (n * 1000h); where n = 0h to 5h

Table 9-358.
PCIE_CORE_PFn_I_VF_DEVICE_ID_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0218h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0218h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0218h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0218h + formula

Figure 9-118. PCIE_CORE_PFn_I_VF_DEVICE_ID_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFDI																R2															
R/W-100h																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-359. PCIE_CORE_PFn_I_VF_DEVICE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VFDI	R/W	100h	VF device id assigned to the device. Its default value is specified in reg_defaults.h, but can be re-written independently for each PF from the local management bus.
15-0	R2	R	0h	Reserved

Table 9-360. Register Call Summary for PCIE_CORE_PFn_I_VF_DEVICE_ID_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VF_DEVICE_ID_REG Register \(Offset = 218h + formula\) \[reset = 01000000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.99 PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG Register (Offset = 21Ch + formula) [reset = 553h]

PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG is shown in Figure 9-119 and described in Table 9-362.

Return to the [Summary Table](#).

This register specifies all the page sizes supported by the device.

Offset = 21Ch + (n * 1000h); where n = 0h to 5h

Table 9-361.
PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 021Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 021Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 021Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 021Ch + formula

Figure 9-119. PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																PS															
R-0h																R/W-553h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-362. PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R0	R	0h	Reserved
15-0	PS	R/W	553h	Page sizes supported by the device [one bit for each page size]. The Controller implements only bits 15:0 of this register. The default value of this field is specified in reg_defaults.h, but can be re-written independently for each PF from the local management bus.

Table 9-363. Register Call Summary for PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_SUPPORTED_PAGE_SIZE_REG Register \(Offset = 21Ch + formula\) \[reset = 553h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.100 PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG Register (Offset = 220h + formula) [reset = 1h]

PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG is shown in Figure 9-120 and described in Table 9-365.

Return to the [Summary Table](#).

This register identifies the page size currently used by the system.

Offset = 220h + (n * 1000h); where n = 0h to 5h

Table 9-364.
PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0220h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0220h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0220h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0220h + formula

Figure 9-120. PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																SPS															
R-0h																R/W-1h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-365. PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R0	R	0h	Reserved
15-0	SPS	R/W	1h	This field must be programmed by software to the current page size in use. The Controller implements only bits 15:0 of this register. This field can also be written from the local management bus.

Table 9-366. Register Call Summary for PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_SYSTEM_PAGE_SIZE_REG Register \(Offset = 220h + formula\) \[reset = 1h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.101 PCIE_CORE_PFn_I_VF_BAR_0_REG Register (Offset = 224h + formula) [reset = 4h]

PCIE_CORE_PFn_I_VF_BAR_0_REG is shown in Figure 9-121 and described in Table 9-368.

Return to the [Summary Table](#).

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses, or paired with the next adjacent register to define a 64-bit address range. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Offset = 224h + (n * 1000h); where n = 0h to 5h

Table 9-367. PCIE_CORE_PFn_I_VF_BAR_0_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0224h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0224h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0224h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0224h + formula

Figure 9-121. PCIE_CORE_PFn_I_VF_BAR_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAMRW										BAMR0					
R/W-0h										R-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAMR0								R8			P0	S0	R7	MSI	
R-0h								R-0h			R-0h		R-1h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-368. PCIE_CORE_PFn_I_VF_BAR_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	BAMRW	R/W	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in BAR Configuration Registers of the associated Physical Function.
21-8	BAMR0	R	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in BAR Configuration Registers of the associated Physical Function. All other bits are not writeable, and are read as 0's.
7-4	R8	R	0h	These bits are hardwired to 0
3	P0	R	0h	When the BAR is used to define a memory address range, this field declares whether data from the address range is prefetchable [0 = non-prefetchable, 1 = prefetchable]. The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function

Table 9-368. PCIE_CORE_PFn_I_VF_BAR_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	S0	R	1h	When the BAR is used to define a memory address range, this field indicates whether the address range is 32-bit or 64-bit [0 = 32-bit, 1 = 64 bit]. For 64-bit address ranges, the value in BAR 1 is treated as a continuation of the base address in BAR 0. The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function.
1	R7	R	0h	This bit is hardwired to 0 for both memory and I/O BARs.
0	MSI	R	0h	Specifies whether this BAR defines a memory address range or an I/O address range [0 = memory, 1 = I/O]. The value read in this field is determined by the setting of BAR Configuration Registers of the associated Physical Function

Table 9-369. Register Call Summary for PCIE_CORE_PFn_I_VF_BAR_0_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VF_BAR_0_REG Register \(Offset = 224h + formula\) \[reset = 4h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.102 PCIE_CORE_PFn_I_VF_BAR_1_REG Register (Offset = 228h + formula) [reset = 0h]

PCIE_CORE_PFn_I_VF_BAR_1_REG is shown in Figure 9-122 and described in Table 9-371.

Return to the [Summary Table](#).

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Offset = 228h + (n * 1000h); where n = 0h to 5h

Table 9-370. PCIE_CORE_PFn_I_VF_BAR_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0228h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0228h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0228h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0228h + formula

Figure 9-122. PCIE_CORE_PFn_I_VF_BAR_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAMRW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-371. PCIE_CORE_PFn_I_VF_BAR_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BAMRW	R/W	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture setting of BAR Configuration Registers of the associated Physical Function. All other bits are not writeable, and are read as 0's.

Table 9-372. Register Call Summary for PCIE_CORE_PFn_I_VF_BAR_1_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VF_BAR_1_REG Register \(Offset = 228h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.103 PCIE_CORE_PFn_I_VF_BAR_2_REG Register (Offset = 22Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_VF_BAR_2_REG is shown in Figure 9-123 and described in Table 9-374.

Return to the [Summary Table](#).

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses, or paired with the next adjacent register to define a 64-bit address range. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Offset = 22Ch + (n * 1000h); where n = 0h to 5h

Table 9-373. PCIE_CORE_PFn_I_VF_BAR_2_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 022Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 022Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 022Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 022Ch + formula

Figure 9-123. PCIE_CORE_PFn_I_VF_BAR_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-374. PCIE_CORE_PFn_I_VF_BAR_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.

Table 9-375. Register Call Summary for PCIE_CORE_PFn_I_VF_BAR_2_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VF_BAR_2_REG Register \(Offset = 22Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.104 PCIE_CORE_PFn_I_VF_BAR_3_REG Register (Offset = 230h + formula) [reset = 0h]

PCIE_CORE_PFn_I_VF_BAR_3_REG is shown in Figure 9-124 and described in Table 9-377.

Return to the [Summary Table](#).

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Offset = 230h + (n * 1000h); where n = 0h to 5h

Table 9-376. PCIE_CORE_PFn_I_VF_BAR_3_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0230h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0230h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0230h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0230h + formula

Figure 9-124. PCIE_CORE_PFn_I_VF_BAR_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-377. PCIE_CORE_PFn_I_VF_BAR_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.

Table 9-378. Register Call Summary for PCIE_CORE_PFn_I_VF_BAR_3_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_I_VF_BAR_3_REG Register \(Offset = 230h + formula\) \[reset = 0h\]: \[0\]](#)

9.2.105 PCIE_CORE_PFn_I_VF_BAR_4_REG Register (Offset = 234h + formula) [reset = 0h]

PCIE_CORE_PFn_I_VF_BAR_4_REG is shown in Figure 9-125 and described in Table 9-380.

Return to the [Summary Table](#).

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses, or paired with the next adjacent register to define a 64-bit address range. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Offset = 234h + (n * 1000h); where n = 0h to 5h

Table 9-379. PCIE_CORE_PFn_I_VF_BAR_4_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0234h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0234h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0234h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0234h + formula

Figure 9-125. PCIE_CORE_PFn_I_VF_BAR_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-380. PCIE_CORE_PFn_I_VF_BAR_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.

Table 9-381. Register Call Summary for PCIE_CORE_PFn_I_VF_BAR_4_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VF_BAR_4_REG Register \(Offset = 234h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.106 PCIE_CORE_PFn_I_VF_BAR_5_REG Register (Offset = 238h + formula) [reset = 0h]

PCIE_CORE_PFn_I_VF_BAR_5_REG is shown in Figure 9-126 and described in Table 9-383.

Return to the [Summary Table](#).

This is part of the set of six Virtual Function Base Address Registers defined by the SR-IOV Specifications. These registers are used to define address ranges for memory accesses to the Endpoint device. This register may be used to define a range of 32-bit addresses. During the initial configuration of the device, the configuration program determines the size of the address range defined by the BAR by writing a pattern of all 1's into the BAR, reading back from the BAR, and noting the position of the first 1 (the most significant) in the returned value. A value of 0 is returned by the Controller if this BAR is not configured. Otherwise, the number of 1's returned is based on the length of the BAR.

Offset = 238h + (n * 1000h); where n = 0h to 5h

Table 9-382. PCIE_CORE_PFn_I_VF_BAR_5_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0238h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0238h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0238h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0238h + formula

Figure 9-126. PCIE_CORE_PFn_I_VF_BAR_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-383. PCIE_CORE_PFn_I_VF_BAR_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration register in LM space.

Table 9-384. Register Call Summary for PCIE_CORE_PFn_I_VF_BAR_5_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VF_BAR_5_REG Register \(Offset = 238h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.107 PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFFSET_REG Register (Offset = 23Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFFSET_REG is shown in Figure 9-127 and described in Table 9-386.

Return to the [Summary Table](#).

Not implemented

Offset = 23Ch + (n * 1000h); where n = 0h to 5h

Table 9-385.
PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFFSET_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 023Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 023Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 023Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 023Ch

Figure 9-127. PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFFSET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSAOR																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-386. PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSAOR	R	0h	N/A

Table 9-387. Register Call Summary for PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFFSET_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VF_MIGRATION_STATE_ARR_OFFSET_REG Register \(Offset = 23Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.108 PCIE_CORE_PFn_RSVD_090_09C Register (Offset = 240h + formula) [reset = 0h]

PCIE_CORE_PFn_RSVD_090_09C is shown in [Figure 9-128](#) and described in [Table 9-389](#).

Return to the [Summary Table](#).

Reserved

Offset = 240h + (n * 1000h); where n = 0h to 5h

**Table 9-388. PCIE_CORE_PFn_RSVD_090_09C
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0240h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0240h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0240h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0240h + formula

Figure 9-128. PCIE_CORE_PFn_RSVD_090_09C Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-389. PCIE_CORE_PFn_RSVD_090_09C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-390. Register Call Summary for PCIE_CORE_PFn_RSVD_090_09C

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_RSVD_090_09C Register \(Offset = 240h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.109 PCIE_CORE_PF0_I_SEC_PCIE_CAP_HDR_REG Register (Offset = 300h) [reset = 40010019h]

PCIE_CORE_PF0_I_SEC_PCIE_CAP_HDR_REG is shown in Figure 9-129 and described in Table 9-392.

Return to the [Summary Table](#).

This register contains the PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability, its capability version, and the pointer to the next capability structure. This register is implemented only in the configuration space of PF 0.

Table 9-391.
PCIE_CORE_PF0_I_SEC_PCIE_CAP_HDR_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0300h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0300h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0300h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0300h

Figure 9-129. PCIE_CORE_PF0_I_SEC_PCIE_CAP_HDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECI															
R/W-400h												R/W-1h				R-19h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-392. PCIE_CORE_PF0_I_SEC_PCIE_CAP_HDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	400h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.
15-0	PECI	R	19h	This field is hardwired to the Capability ID assigned by PCI SIG to the Secondary PCI Express Capability

Table 9-393. Register Call Summary for PCIE_CORE_PF0_I_SEC_PCIE_CAP_HDR_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PF0_I_SEC_PCIE_CAP_HDR_REG Register \(Offset = 300h\) \[reset = 40010019h\]: \[0\]](#)

9.2.110 PCIE_CORE_PF0_I_LINK_CONTROL3_REG Register (Offset = 304h) [reset = 0h]

PCIE_CORE_PF0_I_LINK_CONTROL3_REG is shown in Figure 9-130 and described in Table 9-395.

Return to the [Summary Table](#).

Link Control3 Register.

Table 9-394.
PCIE_CORE_PF0_I_LINK_CONTROL3_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0304h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0304h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0304h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0304h

Figure 9-130. PCIE_CORE_PF0_I_LINK_CONTROL3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R2															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R2				ELSOSGV				R1							
R-0h				R/W-0h								R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-395. PCIE_CORE_PF0_I_LINK_CONTROL3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	R2	R	0h	Reserved
12-9	ELSOSGV	R/W	0h	When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture.
8-0	R1	R	0h	Reserved

Table 9-396. Register Call Summary for PCIE_CORE_PF0_I_LINK_CONTROL3_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_LINK_CONTROL3_REG Register \(Offset = 304h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.111 PCIE_CORE_PF0_I_LANE_ERROR_STATUS_REG Register (Offset = 308h) [reset = 0h]

PCIE_CORE_PF0_I_LANE_ERROR_STATUS_REG is shown in Figure 9-131 and described in Table 9-398.

Return to the [Summary Table](#).

This register contains one bit per lane indicating the physical-layer error status of the corresponding lane. A 1 indicates that a physical-layer error was detected by the Controller in the corresponding lane. The error can be cleared by writing a 1 into the bit position, either through a Configuration Write transaction from the link or from the local management bus.

The following errors are reported in this status bit:

- (i) Parity error detected in Gen3 SKP OS,
- (ii) Loss of Block Alignment in the lane.

Table 9-397.
PCIE_CORE_PF0_I_LANE_ERROR_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0308h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0308h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0308h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0308h

Figure 9-131. PCIE_CORE_PF0_I_LANE_ERROR_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0													LES		
R-0h													R/W1C-0h		

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-398. PCIE_CORE_PF0_I_LANE_ERROR_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	N/A
1-0	LES	R/W1C	0h	Each of these bits indicates the error status for the corresponding lane. STICKY.

Table 9-399. Register Call Summary for PCIE_CORE_PF0_I_LANE_ERROR_STATUS_REG

PCIE_CORE_EP_PF Registers	
•	PCIE_CORE_EP_PF Registers: [0] [1]
•	PCIE_CORE_PF0_I_LANE_ERROR_STATUS_REG Register (Offset = 308h) [reset = 0h]: [0]

9.2.112 PCIe_CORE_PF0_I_LANE_EQUALIZATION_CONTROL_REG0 Register (Offset = 30Ch) [reset = 7F007F00h]

PCIE_CORE_PF0_I_LANE_EQUALIZATION_CONTROL_REG0 is shown in Figure 9-132 and described in Table 9-401.

Return to the [Summary Table](#).

This register contains the 8.0GT/s Transmitter Preset and the Receiver Preset Hint values for lanes 0 and 1, received from the Upstream Device during the Link Equalization procedure.

Table 9-400.
PCIE_CORE_PF0_I_LANE_EQUALIZATION_CONTR
OL_REG0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 030Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 030Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 030Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 030Ch

Figure 9-132. PCIe_CORE_PF0_I_LANE_EQUALIZATION_CONTROL_REG0 Register

31	30	29	28	27	26	25	24
R3	UPRPH1			UPTP1			
R-0h	R-7h			R-Fh			
23	22	21	20	19	18	17	16
R2_1				R2			
R-0h				R-0h			
15	14	13	12	11	10	9	8
R1	UPRPH0			UPTP0			
R-0h	R-7h			R-Fh			
7	6	5	4	3	2	1	0
R0_1				R0			
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-401. PCIe_CORE_PF0_I_LANE_EQUALIZATION_CONTROL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R3	R	0h	Reserved
30-28	UPRPH1	R	7h	8.0GT/s Lane 1 Receiver Preset Hint value received from the upstream device.
27-24	UPTP1	R	Fh	8.0GT/s Lane 1 Transmitter Preset value received from the upstream device.
23	R2_1	R	0h	Reserved
22-16	R2	R	0h	Reserved
15	R1	R	0h	Reserved
14-12	UPRPH0	R	7h	8.0GT/s Lane 0 Receiver Preset Hint value received from the upstream device.
11-8	UPTP0	R	Fh	8.0GT/s Lane 0 Transmitter Preset value received from the upstream device.
7	R0_1	R	0h	Reserved
6-0	R0	R	0h	Reserved

Table 9-402. Register Call Summary for PCIE_CORE_PF0_I_LANE_EQUALIZATION_CONTROL_REG0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PF0_I_LANE_EQUALIZATION_CONTROL_REG0 Register \(Offset = 30Ch\) \[reset = 7F007F00h\]: \[0\]](#)

9.2.113 PCIE_CORE_PFn_I_VSEC_HEADER_REG Register (Offset = 400h + formula) [reset = 4401000Bh]

PCIE_CORE_PFn_I_VSEC_HEADER_REG is shown in Figure 9-133 and described in Table 9-404.

Return to the [Summary Table](#).

The Vendor-Specific Capability allows device vendors to use the Capability mechanism for vendor specific information.

Offset = 400h + (n * 1000h); where n = 0h to 5h

Table 9-403.
PCIE_CORE_PFn_I_VSEC_HEADER_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0400h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0400h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0400h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0400h + formula

Figure 9-133. PCIE_CORE_PFn_I_VSEC_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECI															
R/W-440h												R/W-1h				R/W-Bh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-404. PCIE_CORE_PFn_I_VSEC_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	440h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.
15-0	PECI	R/W	Bh	This field is hardwired to the Capability ID assigned by PCI SIG to the Vendor-Specific Extended Capability.

Table 9-405. Register Call Summary for PCIE_CORE_PFn_I_VSEC_HEADER_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VSEC_HEADER_REG Register \(Offset = 400h + formula\) \[reset = 4401000Bh\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.114 PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_REG Register (Offset = 404h + formula) [reset = 01010001h]

PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_REG is shown in Figure 9-134 and described in Table 9-407.

Return to the [Summary Table](#).

Vendor-Specific Header Register.

Offset = 404h + (n * 1000h); where n = 0h to 5h

Table 9-406.
PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0404h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0404h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0404h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0404h + formula

Figure 9-134. PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VL												VR				VI															
R/W-10h												R/W-1h				R/W-1h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-407. PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	VL	R/W	10h	Total byte count [in hex format] of the VSEC structure, including the Vendor-Specific Capability Header, the Vendor-Specific Header and the Vendor-Specific registers. This field can be written from the local management bus independently or each PF.
19-16	VR	R/W	1h	Vendor-defined version number for the VSEC structure. This field can be written from the local management bus independently or each PF.
15-0	VI	R/W	1h	This field contains a vendor defined ID number that indicates the nature and format of the information in the Vendor-Specific Capability Structure. This field can be written from the local management bus independently or each PF.

Table 9-408. Register Call Summary for PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_REG

PCIE_CORE_EP_PF Registers

- PCIE_CORE_PFn_I_VENDOR_SPECIFIC_HEADER_REG Register (Offset = 404h + formula) [reset = 01010001h]: [0]
- PCIE_CORE_EP_PF Registers: [0] [1]

9.2.115 PCIe_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_REG Register (Offset = 408h + formula) [reset = 0h]

PCIE_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_REG is shown in Figure 9-135 and described in Table 9-410.

Return to the [Summary Table](#).

This contains the first 4 Bytes of Vendor-Specific Register space. In the current implementation, the first 4 Bytes of Vendor Specific Registers is called as Vendor Specific Control Register and is described in the fields below.

Offset = 408h + (n * 1000h); where n = 0h to 5h

Table 9-409.
PCIE_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL
_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0408h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0408h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0408h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0408h + formula

Figure 9-135. PCIe_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VSEC_COUT															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSEC_COUT								HTI	VSEC_CIN						
R/W-0h								R/W-0h				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-410. PCIe_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	VSEC_COUT	R/W	0h	The state of these bits drive the output pins Fx_VSEC_CONTROL_OUT [where x is the function number]. These are implemented as register bits that can be read and written by the host through a Config transaction, or via the local management interface.
8	HTI	R/W	0h	The state of this bit drives the output pins Fx_VSEC_INTERRUPT_OUT [where x is the function number]. It can be used by the host to signal a software-driven interrupt to the application logic outside the Controller. This bit may be read and written by the host through a Config transaction, or via the local management interface.
7-0	VSEC_CIN	R	0h	The 8-bit value read from this field of PFx reflects the setting of Fx_VSEC_CONTROL_IN [7:0] input to the Controller. This field can also be read from the local management bus

Table 9-411. Register Call Summary for PCIE_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VENDOR_SPECIFIC_CONTROL_REG](#) Register (Offset = 408h + formula) [reset = 0h]: [0]
- [PCIE_CORE_EP_PF](#) Registers: [0] [1]

9.2.116 PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0 Register (Offset = 40Ch + formula) [reset = 0h]

PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0 is shown in Figure 9-136 and described in Table 9-413.

Return to the [Summary Table](#).

This contains the Bytes 4, 5, 6, 7 of Vendor-Specific Register space. In the current implementation, the these 4 Bytes of Vendor Specific Registers are called as Vendor Specific Data Register 0 and is described below.

Offset = 40Ch + (n * 1000h); where n = 0h to 5h

Table 9-412.
PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 040Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 040Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 040Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 040Ch + formula

Figure 9-136. PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-413. PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPD	R/W	0h	These bits are implemented as register bits that can be read and written by the host through a Config transaction, or via the local management interface. Their use is application-dependent.

Table 9-414. Register Call Summary for PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_VENDOR_SPECIFIC_DATA_REG0 Register \(Offset = 40Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.117 PCIE_CORE_PFn_I_PASID_HEADER_REG Register (Offset = 440h + formula) [reset = 4C01001Bh]

PCIE_CORE_PFn_I_PASID_HEADER_REG is shown in Figure 9-137 and described in Table 9-416.

Return to the [Summary Table](#).

The presence of a PASID Extended Capability indicates that the Endpoint supports sending and receiving TLPs containing a PASID TLP Prefix.

Offset = 440h + (n * 1000h); where n = 0h to 5h

Table 9-415.
PCIE_CORE_PFn_I_PASID_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0440h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0440h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0440h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0440h + formula

Figure 9-137. PCIE_CORE_PFn_I_PASID_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECI															
R/W-4C0h												R/W-1h				R-1Bh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-416. PCIE_CORE_PFn_I_PASID_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	4C0h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.
15-0	PECI	R	1Bh	This field is hardwired to the Capability ID assigned by PCI SIG to the PASID Capability.

Table 9-417. Register Call Summary for PCIE_CORE_PFn_I_PASID_HEADER_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PASID_HEADER_REG Register \(Offset = 440h + formula\) \[reset = 4C01001Bh\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.118 PCIe_CORE_PFn_I_PASID_CAP_REG Register (Offset = 444h + formula) [reset = 1406h]

PCIE_CORE_PFn_I_PASID_CAP_REG is shown in Figure 9-138 and described in Table 9-419.

Return to the [Summary Table](#).

PASID Capability Header fields are described below:

Offset = 444h + (n * 1000h); where n = 0h to 5h

Table 9-418. PCIe_CORE_PFn_I_PASID_CAP_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0444h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0444h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0444h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0444h + formula

Figure 9-138. PCIe_CORE_PFn_I_PASID_CAP_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31				PRME		EXPE	PASE
R-0h				R/W-0h		R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
R15			MPSW				
R-0h			R/W-14h				
7	6	5	4	3	2	1	0
RSVD2				PRMS		EXPS	RSVD1
R-0h				R/W-1h		R/W-1h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-419. PCIe_CORE_PFn_I_PASID_CAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	R31	R	0h	Reserved
18	PRME	R/W	0h	If set, the Endpoint is permitted to send requests that have the Privileged Mode Requested bit set. If clear, the Endpoint is not permitted to do so.
17	EXPE	R/W	0h	If set, the Endpoint is permitted to send requests that have the Execute Requested bit set. If clear, the Endpoint is not permitted to do so.
16	PASE	R/W	0h	If set, the Endpoint is permitted to send and receive TLPs that contain a PASID TLP Prefix. If clear, the Endpoint is not permitted to do so.
15-13	R15	R	0h	Reserved
12-8	MPSW	R/W	14h	Indicates the width of the PASID field supported by the Endpoint. The value indicates support for PASID values 0 through 2n-1 [inclusive]. The value 0 indicates support for a single PASID [0]. The value 20 indicates support for all PASID values [20 bits]. This field must be between 0 and 20 [inclusive].

Table 9-419. PCIE_CORE_PFn_I_PASID_CAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-3	RSVD2	R	0h	These bits are currently reserved. These are implemented as register bits that can be read and written by the host through a Config transaction, or via the local management interface.
2	PRMS	R/W	1h	If set, the Endpoint supports operating in Privileged and Non-Privileged modes, and supports sending requests that have the Privileged Mode Requested bit set. If clear, the Endpoint should never set the Privileged Mode Requested bit.
1	EXPS	R/W	1h	If set, the Endpoint supports sending memory requests that have the Execute Requested bit set. If clear, the Endpoint should never set the Execute Requested bit.
0	RSVD1	R	0h	These bits are currently reserved. These are implemented as register bits that can be read and written by the host through a Config transaction, or via the local management interface.

Table 9-420. Register Call Summary for PCIE_CORE_PFn_I_PASID_CAP_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_PASID_CAP_REG Register \(Offset = 444h + formula\) \[reset = 1406h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.119 PCIE_CORE_PFO_I_VC_ENH_CAP_HEADER_REG Register (Offset = 4C0h) [reset = 5C010002h]

PCIE_CORE_PFO_I_VC_ENH_CAP_HEADER_REG is shown in Figure 9-139 and described in Table 9-422.

Return to the [Summary Table](#).

This is the first register in the Virtual Channel Capability Structure. The VC Capability is present only in the configuration space of Physical Function 0. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Table 9-421.
PCIE_CORE_PFO_I_VC_ENH_CAP_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04C0h

Figure 9-139. PCIE_CORE_PFO_I_VC_ENH_CAP_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R/W-5C0h												R/W-1h				R-2h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-422. PCIE_CORE_PFO_I_VC_ENH_CAP_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	5C0h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.
15-0	PECID	R	2h	This field is hardwired to the Capability ID assigned by PCI SIG to the VC Capability.

Table 9-423. Register Call Summary for PCIE_CORE_PFO_I_VC_ENH_CAP_HEADER_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_VC_ENH_CAP_HEADER_REG Register \(Offset = 4C0h\) \[reset = 5C010002h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.120 PCIE_CORE_PF0_I_PORT_VC_CAP_REG_1 Register (Offset = 4C4h) [reset = 3h]

PCIE_CORE_PF0_I_PORT_VC_CAP_REG_1 is shown in Figure 9-140 and described in Table 9-425.

Return to the [Summary Table](#).

This register has fields that describe the capabilities of the device with respect to the virtual channels.

Table 9-424.
PCIE_CORE_PF0_I_PORT_VC_CAP_REG_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04C4h

Figure 9-140. PCIE_CORE_PF0_I_PORT_VC_CAP_REG_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																EVC															
R-0h																R-3h															

LEGEND: R = Read Only; -n = value after reset

Table 9-425. PCIE_CORE_PF0_I_PORT_VC_CAP_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	R0	R	0h	N/A
2-0	EVC	R	3h	Indicates the number of Virtual Channels in addition to the default VC supported by the device. This field is valid for all functions.

Table 9-426. Register Call Summary for PCIE_CORE_PF0_I_PORT_VC_CAP_REG_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_PORT_VC_CAP_REG_1 Register \(Offset = 4C4h\) \[reset = 3h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.121 PCIe_CORE_PF0_I_PORT_VC_CAP_REG_2 Register (Offset = 4C8h) [reset = 0h]

PCIE_CORE_PF0_I_PORT_VC_CAP_REG_2 is shown in [Figure 9-141](#) and described in [Table 9-428](#).

Return to the [Summary Table](#).

This register has fields that describe the capabilities of the device with respect to the virtual channels.
This register is not implemented. A read from this location returns all zeroes.

Table 9-427.
PCIE_CORE_PF0_I_PORT_VC_CAP_REG_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04C8h

Figure 9-141. PCIe_CORE_PF0_I_PORT_VC_CAP_REG_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-428. PCIe_CORE_PF0_I_PORT_VC_CAP_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R1	R	0h	N/A

Table 9-429. Register Call Summary for PCIe_CORE_PF0_I_PORT_VC_CAP_REG_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_PORT_VC_CAP_REG_2 Register \(Offset = 4C8h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.122 PCIE_CORE_PF0_I_PORT_VC_CTRL_STS_REG Register (Offset = 4CCh) [reset = 0h]

PCIE_CORE_PF0_I_PORT_VC_CTRL_STS_REG is shown in Figure 9-142 and described in Table 9-431.

Return to the [Summary Table](#).

This location contains the 16-bit VC Control Register and the 16-bit VC Status Register. These registers are not implemented. A read from this location returns all zeroes.

Table 9-430.
PCIE_CORE_PF0_I_PORT_VC_CTRL_STS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04CCh

Figure 9-142. PCIE_CORE_PF0_I_PORT_VC_CTRL_STS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-431. PCIE_CORE_PF0_I_PORT_VC_CTRL_STS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R2	R	0h	N/A

Table 9-432. Register Call Summary for PCIE_CORE_PF0_I_PORT_VC_CTRL_STS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_PORT_VC_CTRL_STS_REG Register \(Offset = 4CCh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.123 PCIE_CORE_PFO_I_VC_RES_CAP_REG_0 Register (Offset = 4D0h) [reset = 0h]

PCIE_CORE_PFO_I_VC_RES_CAP_REG_0 is shown in [Figure 9-143](#) and described in [Table 9-434](#).

Return to the [Summary Table](#).

This register describes the capabilities associated with VC 0. This register is not implemented. A read from this location returns all zeroes.

Table 9-433.
PCIE_CORE_PFO_I_VC_RES_CAP_REG_0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04D0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04D0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04D0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04D0h

Figure 9-143. PCIE_CORE_PFO_I_VC_RES_CAP_REG_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-434. PCIE_CORE_PFO_I_VC_RES_CAP_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R3	R	0h	N/A

Table 9-435. Register Call Summary for PCIE_CORE_PFO_I_VC_RES_CAP_REG_0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_VC_RES_CAP_REG_0 Register \(Offset = 4D0h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.124 PCIE_CORE_PF0_I_VC_RES_CTRL_REG_0 Register (Offset = 4D4h) [reset = 80000FFh]

PCIE_CORE_PF0_I_VC_RES_CTRL_REG_0 is shown in Figure 9-144 and described in Table 9-437.

Return to the [Summary Table](#).

This register contains bits to configure VC 0.

Table 9-436.
PCIE_CORE_PF0_I_VC_RES_CTRL_REG_0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04D4h

Figure 9-144. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_0 Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R-1h	R-0h				R-0h		
23	22	21	20	19	18	17	16
R5				PARS		LPAT	
R-0h				R-0h		R-0h	
15	14	13	12	11	10	9	8
R4							
R-0h							
7	6	5	4	3	2	1	0
TVM						TVM0	
R/W-7Fh						R-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-437. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R	1h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30-27	R6	R	0h	N/A
26-24	VCI	R	0h	VC ID assigned to VC0. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23-20	R5	R	0h	N/A
19-17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 0. This bit is not implemented, and hardwired to 0.
15-8	R4	R	0h	N/A
7-1	TVM	R/W	7Fh	Indicates the TCs that are mapped to this VC. When bit 0 of this field is set, it indicates that TC 0 is mapped to VC 0. By default, all TCs are mapped to VC 0.

Table 9-437. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TVM0	R	1h	Indicates the TC0 always mapped to VC0.

Table 9-438. Register Call Summary for PCIE_CORE_PF0_I_VC_RES_CTRL_REG_0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_VC_RES_CTRL_REG_0 Register \(Offset = 4D4h\) \[reset = 800000FFh\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.125 PCIE_CORE_PF0_I_VC_RES_STS_REG_0 Register (Offset = 4D8h) [reset = 0h]

PCIE_CORE_PF0_I_VC_RES_STS_REG_0 is shown in [Figure 9-145](#) and described in [Table 9-440](#).

Return to the [Summary Table](#).

This register contains status bits associated with VC 0.

Table 9-439.
PCIE_CORE_PF0_I_VC_RES_STS_REG_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04D8h

Figure 9-145. PCIE_CORE_PF0_I_VC_RES_STS_REG_0 Register

31	30	29	28	27	26	25	24
R7							
R-0h							
23	22	21	20	19	18	17	16
R7							
R-0h							
15	14	13	12	11	10	9	8
R7							
R-0h							
7	6	5	4	3	2	1	0
R7						VCNP	PATS
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-440. PCIE_CORE_PF0_I_VC_RES_STS_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R7	R	0h	N/A
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

Table 9-441. Register Call Summary for PCIE_CORE_PF0_I_VC_RES_STS_REG_0

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_VC_RES_STS_REG_0 Register \(Offset = 4D8h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.126 PCIE_CORE_PF0_I_VC_RES_CAP_REG_1 Register (Offset = 4DCh) [reset = 0h]

PCIE_CORE_PF0_I_VC_RES_CAP_REG_1 is shown in [Figure 9-146](#) and described in [Table 9-443](#).

Return to the [Summary Table](#).

This register describes the capabilities associated with VC 1. This register is not implemented. A read from this location returns all zeroes.

Table 9-442.
PCIE_CORE_PF0_I_VC_RES_CAP_REG_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04DCh

Figure 9-146. PCIE_CORE_PF0_I_VC_RES_CAP_REG_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-443. PCIE_CORE_PF0_I_VC_RES_CAP_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R3	R	0h	N/A

Table 9-444. Register Call Summary for PCIE_CORE_PF0_I_VC_RES_CAP_REG_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_VC_RES_CAP_REG_1 Register \(Offset = 4DCh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.127 PCIE_CORE_PF0_I_VC_RES_CTRL_REG_1 Register (Offset = 4E0h) [reset = 01000000h]

PCIE_CORE_PF0_I_VC_RES_CTRL_REG_1 is shown in Figure 9-147 and described in Table 9-446.

Return to the [Summary Table](#).

This register contains bits to configure VC 1.

Table 9-445.
PCIE_CORE_PF0_I_VC_RES_CTRL_REG_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04E0h

Figure 9-147. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_1 Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W-0h	R-0h				R/W-1h		
23	22	21	20	19	18	17	16
R5				PARS			LPAT
R-0h				R-0h			R-0h
15	14	13	12	11	10	9	8
R4							
R-0h							
7	6	5	4	3	2	1	0
TVM						TVM0	
R/W-0h						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-446. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30-27	R6	R	0h	N/A
26-24	VCI	R/W	1h	VC ID assigned to VC1. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23-20	R5	R	0h	N/A
19-17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 1. This bit is not implemented, and hardwired to 0.
15-8	R4	R	0h	N/A
7-1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 1 of this field is set, it indicates that TC 1 is mapped to VC 1. By default, all TCs are mapped to VC 0.

Table 9-446. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

Table 9-447. Register Call Summary for PCIE_CORE_PF0_I_VC_RES_CTRL_REG_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_VC_RES_CTRL_REG_1 Register \(Offset = 4E0h\) \[reset = 01000000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.128 PCIE_CORE_PF0_I_VC_RES_STS_REG_1 Register (Offset = 4E4h) [reset = 0h]

PCIE_CORE_PF0_I_VC_RES_STS_REG_1 is shown in [Figure 9-148](#) and described in [Table 9-449](#).

Return to the [Summary Table](#).

This register contains status bits associated with VC 1.

Table 9-448.
PCIE_CORE_PF0_I_VC_RES_STS_REG_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04E4h

Figure 9-148. PCIE_CORE_PF0_I_VC_RES_STS_REG_1 Register

31	30	29	28	27	26	25	24
R7							
R-0h							
23	22	21	20	19	18	17	16
R7							
R-0h							
15	14	13	12	11	10	9	8
R7							
R-0h							
7	6	5	4	3	2	1	0
R7						VCNP	PATS
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-449. PCIE_CORE_PF0_I_VC_RES_STS_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R7	R	0h	N/A
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

Table 9-450. Register Call Summary for PCIE_CORE_PF0_I_VC_RES_STS_REG_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_VC_RES_STS_REG_1 Register \(Offset = 4E4h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.129 PCIe_CORE_PF0_I_VC_RES_CAP_REG_2 Register (Offset = 4E8h) [reset = 0h]

PCIE_CORE_PF0_I_VC_RES_CAP_REG_2 is shown in [Figure 9-149](#) and described in [Table 9-452](#).

Return to the [Summary Table](#).

This register describes the capabilities associated with VC 2. This register is not implemented. A read from this location returns all zeroes.

Table 9-451.
PCIE_CORE_PF0_I_VC_RES_CAP_REG_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04E8h

Figure 9-149. PCIe_CORE_PF0_I_VC_RES_CAP_REG_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-452. PCIe_CORE_PF0_I_VC_RES_CAP_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R3	R	0h	N/A

Table 9-453. Register Call Summary for PCIe_CORE_PF0_I_VC_RES_CAP_REG_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_VC_RES_CAP_REG_2 Register \(Offset = 4E8h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.130 PCIE_CORE_PF0_I_VC_RES_CTRL_REG_2 Register (Offset = 4ECh) [reset = 02000000h]

PCIE_CORE_PF0_I_VC_RES_CTRL_REG_2 is shown in Figure 9-150 and described in Table 9-455.

Return to the [Summary Table](#).

This register contains bits to configure VC 2.

Table 9-454.
PCIE_CORE_PF0_I_VC_RES_CTRL_REG_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04ECh

Figure 9-150. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_2 Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W-0h	R-0h				R/W-2h		
23	22	21	20	19	18	17	16
R5				PARS		LPAT	
R-0h				R-0h		R-0h	
15	14	13	12	11	10	9	8
R4							
R-0h							
7	6	5	4	3	2	1	0
TVM						TVM0	
R/W-0h						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-455. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30-27	R6	R	0h	N/A
26-24	VCI	R/W	2h	VC ID assigned to VC2. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23-20	R5	R	0h	N/A
19-17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 2. This bit is not implemented, and hardwired to 0.
15-8	R4	R	0h	N/A
7-1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 2 of this field is set, it indicates that TC 2 is mapped to VC 2.By default, all TCs are mapped to VC 0.

Table 9-455. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

Table 9-456. Register Call Summary for PCIE_CORE_PF0_I_VC_RES_CTRL_REG_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_VC_RES_CTRL_REG_2 Register \(Offset = 4ECh\) \[reset = 02000000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.131 PCIE_CORE_PFO_I_VC_RES_STS_REG_2 Register (Offset = 4F0h) [reset = 0h]

PCIE_CORE_PFO_I_VC_RES_STS_REG_2 is shown in [Figure 9-151](#) and described in [Table 9-458](#).

Return to the [Summary Table](#).

This register contains status bits associated with VC 2.

Table 9-457.
PCIE_CORE_PFO_I_VC_RES_STS_REG_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04F0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04F0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04F0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04F0h

Figure 9-151. PCIE_CORE_PFO_I_VC_RES_STS_REG_2 Register

31	30	29	28	27	26	25	24
R7							
R-0h							
23	22	21	20	19	18	17	16
R7							
R-0h							
15	14	13	12	11	10	9	8
R7							
R-0h							
7	6	5	4	3	2	1	0
R7						VCNP	PATS
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-458. PCIE_CORE_PFO_I_VC_RES_STS_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R7	R	0h	N/A
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

Table 9-459. Register Call Summary for PCIE_CORE_PFO_I_VC_RES_STS_REG_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_VC_RES_STS_REG_2 Register \(Offset = 4F0h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.132 PCIE_CORE_PFO_I_VC_RES_CAP_REG_3 Register (Offset = 4F4h) [reset = 0h]

PCIE_CORE_PFO_I_VC_RES_CAP_REG_3 is shown in [Figure 9-152](#) and described in [Table 9-461](#).

Return to the [Summary Table](#).

This register describes the capabilities associated with VC 3. This register is not implemented. A read from this location returns all zeroes.

Table 9-460.
PCIE_CORE_PFO_I_VC_RES_CAP_REG_3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04F4h

Figure 9-152. PCIE_CORE_PFO_I_VC_RES_CAP_REG_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-461. PCIE_CORE_PFO_I_VC_RES_CAP_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R3	R	0h	N/A

Table 9-462. Register Call Summary for PCIE_CORE_PFO_I_VC_RES_CAP_REG_3

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFO_I_VC_RES_CAP_REG_3 Register \(Offset = 4F4h\) \[reset = 0h\]: \[0\]](#)

9.2.133 PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3 Register (Offset = 4F8h) [reset = 03000000h]

PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3 is shown in Figure 9-153 and described in Table 9-464.

Return to the [Summary Table](#).

This register contains bits to configure VC 3.

Table 9-463.
PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04F8h

Figure 9-153. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3 Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W-0h	R-0h				R/W-3h		
23	22	21	20	19	18	17	16
R5				PARS			LPAT
R-0h				R-0h			R-0h
15	14	13	12	11	10	9	8
R4							
R-0h							
7	6	5	4	3	2	1	0
TVM							TVM0
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-464. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30-27	R6	R	0h	N/A
26-24	VCI	R/W	3h	VC ID assigned to VC3. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23-20	R5	R	0h	N/A
19-17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 3. This bit is not implemented, and hardwired to 0.
15-8	R4	R	0h	N/A
7-1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 3 of this field is set, it indicates that TC 3 is mapped to VC 3. By default, all TCs are mapped to VC 0.

Table 9-464. PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

Table 9-465. Register Call Summary for PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_VC_RES_CTRL_REG_3 Register \(Offset = 4F8h\) \[reset = 03000000h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.134 PCIE_CORE_PF0_I_VC_RES_STS_REG_3 Register (Offset = 4FCh) [reset = 0h]

PCIE_CORE_PF0_I_VC_RES_STS_REG_3 is shown in [Figure 9-154](#) and described in [Table 9-467](#).

Return to the [Summary Table](#).

This register contains status bits associated with VC 3.

Table 9-466.
PCIE_CORE_PF0_I_VC_RES_STS_REG_3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04FCh

Figure 9-154. PCIE_CORE_PF0_I_VC_RES_STS_REG_3 Register

31	30	29	28	27	26	25	24
R7							
R-0h							
23	22	21	20	19	18	17	16
R7							
R-0h							
15	14	13	12	11	10	9	8
R7							
R-0h							
7	6	5	4	3	2	1	0
R7						VCNP	PATS
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-467. PCIE_CORE_PF0_I_VC_RES_STS_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R7	R	0h	N/A
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

Table 9-468. Register Call Summary for PCIE_CORE_PF0_I_VC_RES_STS_REG_3

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PF0_I_VC_RES_STS_REG_3 Register \(Offset = 4FCh\) \[reset = 0h\]: \[0\]](#)

9.2.135 PCIE_CORE_PFn_ATS_CAP_HEADER Register (Offset = 5C0h + formula) [reset = 6401000Fh]

PCIE_CORE_PFn_ATS_CAP_HEADER is shown in Figure 9-155 and described in Table 9-470.

Return to the [Summary Table](#).

This location contains the ATS Extended Capabilities Register, its Capability ID, Version, and a pointer to the next capability.

Offset = 5C0h + (n * 1000h); where n = 0h to 5h

Table 9-469. PCIE_CORE_PFn_ATS_CAP_HEADER Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 05C0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 05C0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 05C0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 05C0h + formula

Figure 9-155. PCIE_CORE_PFn_ATS_CAP_HEADER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ATSNXTCAP												ATSCAPVER			
R/W-640h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATSCAPID															
R-Fh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-470. PCIE_CORE_PFn_ATS_CAP_HEADER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	ATSNXTCAP	R/W	640h	Indicates offset to the next PCI Express capability structure.
19-16	ATSCAPVER	R/W	1h	Specifies the SIG assigned value for the version of the capability structure.
15-0	ATSCAPID	R	Fh	Indicates the ATS Extended Capability structure. This field must return a Capability ID of 000Fh indicating that this is an ATS Extended Capability structure.

Table 9-471. Register Call Summary for PCIE_CORE_PFn_ATS_CAP_HEADER

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_ATS_CAP_HEADER Register \(Offset = 5C0h + formula\) \[reset = 6401000Fh\]: \[0\]](#)

9.2.136 PCIE_CORE_PFn_ATS_CAP_CONTROL Register (Offset = 5C4h + formula) [reset = 61h]

PCIE_CORE_PFn_ATS_CAP_CONTROL is shown in Figure 9-156 and described in Table 9-473.

Return to the [Summary Table](#).

ATS Capability and Control Register

Offset = 5C4h + (n * 1000h); where n = 0h to 5h

Table 9-472. PCIE_CORE_PFn_ATS_CAP_CONTROL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 05C4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 05C4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 05C4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 05C4h + formula

Figure 9-156. PCIE_CORE_PFn_ATS_CAP_CONTROL Register

31	30	29	28	27	26	25	24
ATSEN	R30						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R30				ATSSTU			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
R15							
R-0h							
7	6	5	4	3	2	1	0
R15	ATSGIS	ATSPGALNREQ	ATSINVQD				
R-0h	R/W-1h	R/W-1h	R/W-1h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-473. PCIE_CORE_PFn_ATS_CAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ATSEN	R/W	0h	When Set, the Function is enabled to cache translations. Default value is 0b.
30-21	R30	R	0h	Reserved
20-16	ATSSTU	R/W	0h	This value indicates to the Function the minimum number of 4096-byte blocks that is indicated in a Translation Completions or Invalidate Requests. This is a power of 2 multiplier and the number of blocks is 2STU. A value of 0 0000b indicates one block and a value of 1 1111b indicates 2 ³¹ blocks.
15-7	R15	R	0h	Reserved
6	ATSGIS	R/W	1h	If Set, the Function supports InvalidationRequests that have the Global Invalidate bit Set. If Clear, the Function ignores the Global Invalidate bit in all Invalidate Requests.
5	ATSPGALNREQ	R/W	1h	If Set, indicates the Untranslated Address is always aligned to a 4096 byte boundary.

Table 9-473. PCIE_CORE_PFn_ATS_CAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	ATSINVQD	R/W	1h	The number of Invalidate Requests that the Function can accept before putting backpressure on the upstream connection. If 0 0000b, the Function can accept 32 Invalidate Requests.

Table 9-474. Register Call Summary for PCIE_CORE_PFn_ATS_CAP_CONTROL

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_ATS_CAP_CONTROL Register \(Offset = 5C4h + formula\) \[reset = 61h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.137 PCIE_CORE_PFn_ATS_PR_CAP_HEADER Register (Offset = 640h + formula) [reset = 90010013h]

PCIE_CORE_PFn_ATS_PR_CAP_HEADER is shown in Figure 9-157 and described in Table 9-476.

Return to the [Summary Table](#).

Page Request Extended Capability Structure is used to configure the Page Request Interface mechanism.

Offset = 640h + (n * 1000h); where n = 0h to 5h

Table 9-475.
PCIE_CORE_PFn_ATS_PR_CAP_HEADER
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0640h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0640h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0640h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0640h + formula

Figure 9-157. PCIE_CORE_PFn_ATS_PR_CAP_HEADER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ATSPRNXCAP												ATSPRCAPVER			
R/W-900h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATSPRCAPID															
R-13h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-476. PCIE_CORE_PFn_ATS_PR_CAP_HEADER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	ATSPRNXCAP	R/W	900h	The offset to the next PCI Extended Capability structure.
19-16	ATSPRCAPVER	R/W	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	ATSPRCAPID	R	13h	Indicates that the associated extended capability structure is a Page Request Extended Capability. This field must return a Capability ID of 0013h.

Table 9-477. Register Call Summary for PCIE_CORE_PFn_ATS_PR_CAP_HEADER

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PFn_ATS_PR_CAP_HEADER Register \(Offset = 640h + formula\) \[reset = 90010013h\]: \[0\]](#)

9.2.138 PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS Register (Offset = 644h + formula) [reset = X]

PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS is shown in Figure 9-158 and described in Table 9-479.

Return to the [Summary Table](#).

ATS Page Request Control Status Register.

Offset = 644h + (n * 1000h); where n = 0h to 5h

Table 9-478.
PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0644h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0644h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0644h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0644h + formula

Figure 9-158. PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS Register

31	30	29	28	27	26	25	24
ATSPRGRPR	RESERVED						ATSPRSTOP
R/W-1h	R/W-X						R/W-1h
23	22	21	20	19	18	17	16
RESERVED						ATSPPRUPRGI	ATS_PR_RF
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						ATSPRRST	ATSPREN
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-479. PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ATSPRGRPR	R/W	1h	If Set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding Page Requests had a PASID TLP Prefix. If Clear, the Function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix
30-25	RESERVED	R/W	X	

Table 9-479. PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	ATSPRSTOP	R/W	1h	<p>When this field is Set, the associated page request interface has stopped issuing additional page requests and that all previously issued Page Requests have completed.</p> <p>When this field is Clear the associated page request interface either has not stopped or has stopped issuing new Page Requests but has outstanding Page Requests.</p> <p>This field is only meaningful if Enable is Clear.</p> <p>If Enable is Set, this field is undefined.</p> <p>When the Enable field is Cleared, after having been previously Set, the interface transitions to the stopping state and Clears this field.</p> <p>After all page requests currently outstanding at the Function[s] have completed, this field is Set and the interface enters the disabled state.</p> <p>If there were no outstanding page requests, this field may be Set immediately when Enable is Cleared.</p> <p>Resetting the interface will cause an immediate transition to the disabled state.</p> <p>While in the stopping state, receipt of a Response Failure message will result in the immediate transition to the disabled state [Setting this field].</p> <p>For SR-IOV, this field is Set only when all associated Functions [PF and VFs] have stopped issuing page requests.</p> <p>Default value is 1b.</p>
23-18	RESERVED	R/W	X	
17	ATSPPRUPRGI	R/W	0h	<p>This field, when Set, indicates that the Function has received a PRG Response Message containing a PRG index that has no matching request.</p> <p>This field is Set by the Function and cleared when a one is written to the field.</p> <p>For SR-IOV, this field is Set in the PF if any associated Function [PF or VF] receives a PRG Response Message that does has no matching request.</p> <p>Default value is 0b.</p>
16	ATS_PR_RF	R/W	0h	<p>This field, when Set, indicates that the Function has received a PRG Response Message indicating a Response Failure.</p> <p>The Function expects no further responses from the host [any received are ignored].</p> <p>This field is Set by the Function and Cleared when a one is written to the field.</p> <p>For SR-IOV, this field is Set in the PF if any associated Function [PF or VF] receives a PRG Response Message indicating Response Failure.</p> <p>Default value is 0b.</p>
15-2	RESERVED	R/W	X	

Table 9-479. PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ATSPRRST	R/W	0h	<p>When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit counter and pending request state for the associated Page Request Interface.</p> <p>No action is initiated if this field is written to 0b or if this field is written with any value while the Enable field is Set.</p> <p>Reads of this field through PCIe link return 0b.</p> <p>Once this field is written by '1' through pcie link, a vector output[ATS_PR_CONTROL_REG_RESET] of controller gets set. client logic after clearing the credit counter and pending request state, has to clear this register through local management interface.</p>
0	ATSPREN	R/W	0h	<p>This field, when set, indicates that the Page Request Interface is allowed to make page requests.</p> <p>If this field is Clear, the Page Request Interface is not allowed to issue page requests.</p> <p>If both this field and the Stopped field are Clear, then the Page Request Interface will not issue new page requests, but has outstanding page requests that have been transmitted or are queued for transmission.</p> <p>When the Page Request Interface is transitioned from not-Enabled to Enabled, its status flags [Stopped, Response Failure, and Unexpected Response flags] are cleared.</p> <p>Enabling a Page Request Interface that has not successfully Stopped has indeterminate results.</p> <p>Default value is 0b.</p>

Table 9-480. Register Call Summary for PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_ATS_PR_CONTROL_STATUS Register \(Offset = 644h + formula\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.139 PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY Register (Offset = 648h + formula) [reset = 1h]

PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY is shown in Figure 9-159 and described in Table 9-482.

Return to the [Summary Table](#).

This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface.

Offset = 648h + (n * 1000h); where n = 0h to 5h

Table 9-481.
PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0648h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0648h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0648h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0648h + formula

Figure 9-159. PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATSOUTPRCAP																															
R/W-1h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-482. PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ATSOUTPRCAP	R/W	1h	This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface.

Table 9-483. Register Call Summary for PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY

PCIE_CORE_EP_PF Registers

- PCIE_CORE_PFn_ATS_OUTSTANDING_PR_CAPACITY Register (Offset = 648h + formula) [reset = 1h]: [0]
- PCIE_CORE_EP_PF Registers: [0] [1]

9.2.140 PCIe_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC Register (Offset = 64Ch + formula) [reset = 0h]

PCIE_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC is shown in [Figure 9-160](#) and described in [Table 9-485](#).

Return to the [Summary Table](#).

This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.

Offset = 64Ch + (n * 1000h); where n = 0h to 5h

Table 9-484.
PCIE_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 064Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 064Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 064Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 064Ch + formula

Figure 9-160. PCIe_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATSOUTPRALLOC																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-485. PCIe_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ATSOUTPRALLOC	R/W	0h	This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue

Table 9-486. Register Call Summary for PCIe_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_ATS_OUTSTANDING_PR_ALLOC Register \(Offset = 64Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.141 PCIE_CORE_PF0_I_L1_PM_EXT_CAP_HDR Register (Offset = 900h) [reset = 9101001Eh]

PCIE_CORE_PF0_I_L1_PM_EXT_CAP_HDR is shown in Figure 9-161 and described in Table 9-488.

Return to the [Summary Table](#).

L1 PM Substates Extended Capability Header Register.

For a multi-Function device associated with an Endpoint implementing L1 PM Substates, this Extended Capability Structure is implemented only in Function 0, and controls the Endpoint's Link behavior on behalf of all the Functions of the device.

Table 9-487.
PCIE_CORE_PF0_I_L1_PM_EXT_CAP_HDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0900h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0900h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0900h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0900h

Figure 9-161. PCIE_CORE_PF0_I_L1_PM_EXT_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R/W-910h												R/W-1h				R-1Eh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-488. PCIE_CORE_PF0_I_L1_PM_EXT_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	910h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R/W	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.
15-0	PECID	R	1Eh	This field is hardwired to the Capability ID assigned by PCI SIG to the L1 PM Substates Extended Capability Structure [001E hex].

Table 9-489. Register Call Summary for PCIE_CORE_PF0_I_L1_PM_EXT_CAP_HDR

PCIE_CORE_EP_PF Registers

- PCIE_CORE_PF0_I_L1_PM_EXT_CAP_HDR Register (Offset = 900h) [reset = 9101001Eh]: [0]
- PCIE_CORE_EP_PF Registers: [0] [1]

9.2.142 PCIe_CORE_PF0_I_L1_PM_CAP Register (Offset = 904h) [reset = X]

PCIe_CORE_PF0_I_L1_PM_CAP is shown in [Figure 9-162](#) and described in [Table 9-491](#).

Return to the [Summary Table](#).

This register advertises the L1 PM Substates Capabilities.

Table 9-490. PCIe_CORE_PF0_I_L1_PM_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0904h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0904h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0904h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0904h

Figure 9-162. PCIe_CORE_PF0_I_L1_PM_CAP Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
R0				RESERVED		L1PRTPVRONSCALE	
R/W-Dh				R/W-X		R/W-0h	
15	14	13	12	11	10	9	8
L1PRTCMMMDRESTRTIME							
R/W-FFh							
7	6	5	4	3	2	1	0
RESERVED			L1PMSUPP	L1ASPML11SU PP	L1ASPML12SU PP	L1PML11SUPP	L1PML12SUPP
R/W-X			R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-491. PCIe_CORE_PF0_I_L1_PM_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-19	R0	R/W	Dh	Along with the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register sets the time [in us] that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register. T Power On is the minimum amount of time that each component must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. This is to ensure no device is ever actively driving into an unpowered component.This bit can be modified using local management interface.
18	RESERVED	R/W	X	

Table 9-491. PCIE_CORE_PFO_I_L1_PM_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	L1PRTPVRONSCALE	R/W	0h	Specifies the scale used for the Port T_POWER_ON Value field in the L1 PM Substates Capabilities register. Range of Values 00b = 2us 01b = 10us 10b = 100us 11b = Reserved Default value is 00. This bit can be modified using local management interface.
15-8	L1PRTCMMMDRESTRTIME	R/W	FFh	Time [in us] required for this Port to re-establish common mode during exit from PM or ASPM L1.2 substate. This bit can be modified using local management interface.
7-5	RESERVED	R/W	X	
4	L1PMSUPP	R/W	1h	When Set this bit indicates that this Port supports L1 PM Substates. This bit can be modified using local management interface.
3	L1ASPM L1.1 SUPP	R/W	1h	When Set this bit indicates that ASPM L1.1 is supported. This bit can be modified using local management interface.
2	L1ASPM L1.2 SUPP	R/W	1h	When Set this bit indicates that ASPM L1.2 is supported. This bit can be modified using local management interface.
1	L1PML1.1 SUPP	R/W	1h	When Set this bit indicates that PCI-PM L1.1 is supported. This bit can be modified using local management interface.
0	L1PML1.2 SUPP	R/W	1h	When Set this bit indicates that PCI-PM L1.2 is supported. This bit can be modified using local management interface.

Table 9-492. Register Call Summary for PCIE_CORE_PFO_I_L1_PM_CAP

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_L1_PM_CAP Register \(Offset = 904h\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.143 PCIE_CORE_PFO_I_L1_PM_CTRL_1 Register (Offset = 908h) [reset = X]

PCIE_CORE_PFO_I_L1_PM_CTRL_1 is shown in [Figure 9-163](#) and described in [Table 9-494](#).

Return to the [Summary Table](#).

This register is used to Control ASPM, PCI PM L1 substates.

**Table 9-493. PCIE_CORE_PFO_I_L1_PM_CTRL_1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0908h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0908h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0908h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0908h

Figure 9-163. PCIE_CORE_PFO_I_L1_PM_CTRL_1 Register

31	30	29	28	27	26	25	24
L1THRSHLDSC			RESERVED			L1THRSHLDVAL	
R/W-0h			R/W-X			R/W-0h	
23	22	21	20	19	18	17	16
L1THRSHLDVAL							
R/W-0h							
15	14	13	12	11	10	9	8
L1CMMDRESTRTIME							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				L1ASPML11EN	L1ASPML12EN	L1PML11EN	L1PML12EN
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-494. PCIE_CORE_PFO_I_L1_PM_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	L1THRSHLDSC	R/W	0h	This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. 000 - Value times 1 ns 001 - Value times 32 ns 010 - Value times 1024 ns 011 - Value times 32,768 ns 100 - Value times 1,048,576 ns 101 - Value times 33,554,422ns 110- 111 - Not permitted
28-26	RESERVED	R/W	X	
25-16	L1THRSHLDVAL	R/W	0h	Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 [if enabled] or L1.2 [if enabled].
15-8	L1CMMDRESTRTIME	R	0h	This field is reserved for EP.
7-4	RESERVED	R/W	X	
3	L1ASPML11EN	R/W	0h	When Set this bit enables ASPM L1.1.
2	L1ASPML12EN	R/W	0h	When Set this bit enables ASPM L1.2.
1	L1PML11EN	R/W	0h	When Set this bit enables PCI-PM L1.1.
0	L1PML12EN	R/W	0h	When Set this bit enables PCI-PM L1.2.

Table 9-495. Register Call Summary for PCIE_CORE_PF0_I_L1_PM_CTRL_1

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PF0_I_L1_PM_CTRL_1 Register \(Offset = 908h\) \[reset = X\]: \[0\]](#)

9.2.144 PCIE_CORE_PFO_I_L1_PM_CTRL_2 Register (Offset = 90Ch) [reset = X]

PCIE_CORE_PFO_I_L1_PM_CTRL_2 is shown in [Figure 9-164](#) and described in [Table 9-497](#).

Return to the [Summary Table](#).

L1 PM Substates Control 2 Register

**Table 9-496. PCIE_CORE_PFO_I_L1_PM_CTRL_2
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 090Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 090Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 090Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 090Ch

Figure 9-164. PCIE_CORE_PFO_I_L1_PM_CTRL_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
L1PWRONVAL					RESERVED	L1PWRONSC	
R/W-5h					R/W-X	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-497. PCIE_CORE_PFO_I_L1_PM_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-3	L1PWRONVAL	R/W	5h	Along with the T_POWER_ON Scale sets the minimum amount of time [in us] that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON Scale field.
2	RESERVED	R/W	X	
1-0	L1PWRONSC	R/W	0h	Specifies the scale used for T_POWER_ON Value. Range of Values 00b = 2us 01b = 10us 10b = 100us 11b = Reserved

Table 9-498. Register Call Summary for PCIE_CORE_PFO_I_L1_PM_CTRL_2

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_L1_PM_CTRL_2 Register \(Offset = 90Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.145 PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = 910h + formula) [reset = 92010025h]

PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG is shown in Figure 9-165 and described in Table 9-500.

Return to the [Summary Table](#).

Data Link Feature Extended Capability Structure is used to configure the DL Feature mechanism.

Offset = 910h + (n * 1000h); where n = 0h to 5h

Table 9-499.
PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0910h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0910h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0910h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0910h + formula

Figure 9-165. PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DLFNXCAP												DLFCAPVER			
R/W-920h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLFCAPID															
R-25h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-500. PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG Register Field
Descriptions

Bit	Field	Type	Reset	Description
31-20	DLFNXCAP	R/W	920h	The offset to the next PCI Extended Capability structure.
19-16	DLFCAPVER	R/W	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	DLFCAPID	R	25h	Indicates that the associated extended capability structure is the DL Feature Extended Capability. This field returns a Capability ID of 0025h.

Table 9-501. Register Call Summary for
PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG Register \(Offset = 910h + formula\) \[reset = 92010025h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.146 PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG Register (Offset = 914h + formula) [reset = 80000001h]

PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG is shown in Figure 9-166 and described in Table 9-503.

Return to the [Summary Table](#).

Data Link Feature Capabilities Register..

Offset = 914h + (n * 1000h); where n = 0h to 5h

Table 9-502.
PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0914h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0914h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0914h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0914h + formula

Figure 9-166. PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG Register

31	30	29	28	27	26	25	24
DLFEXEN				R0			
R/W-1h				R-0h			
23	22	21	20	19	18	17	16
				R0			
				R-0h			
15	14	13	12	11	10	9	8
				R0			
				R-0h			
7	6	5	4	3	2	1	0
			R0				DLFCAPVER
			R-0h				R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-503. PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DLFEXEN	R/W	1h	If Set, this bit indicates that this Port will enter the DL_Feature negotiation state prior to Link Initialization.
30-1	R0	R	0h	Reserved
0	DLFCAPVER	R/W	1h	This bit indicates that this Port supports the Scaled Flow Control Feature.

Table 9-504. Register Call Summary for PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DL_FEATURE_CAPABILITIES_REG Register \(Offset = 914h + formula\) \[reset = 80000001h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.147 PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG Register (Offset = 918h + formula) [reset = 0h]

PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG is shown in Figure 9-167 and described in Table 9-506.

Return to the [Summary Table](#).

Data Link Feature Status Register..

Offset = 918h + (n * 1000h); where n = 0h to 5h

Table 9-505.
PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0918h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0918h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0918h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0918h + formula

Figure 9-167. PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG Register

31	30	29	28	27	26	25	24
RDLFSVAL	R1						
R-0h	R-0h						
23	22	21	20	19	18	17	16
R23	R0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						RSFSUP	
R-0h						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-506. PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RDLFSVAL	R	0h	This bit indicates that the Port has received a Data Link Feature DLLP in state DL_Feature [see Section 3.2.1] and that the Remote Data Link Feature Supported and Remote Data Link Feature Ack fields are meaningful. This bit is Cleared on entry to state DL_Inactive. Default is 0b.
30-24	R1	R	0h	Reserved
23	R23	R	0h	Reserved
22-1	R0	R	0h	Reserved
0	RSFSUP	R	0h	This bit indicates that the Remote end Device supports the Scaled Flow Control Feature.

Table 9-507. Register Call Summary for PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFn_I_DL_FEATURE_STATUS_REG Register \(Offset = 918h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.148 PCIE_CORE_PF0_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = 920h) [reset = 9C010027h]

PCIE_CORE_PF0_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG is shown in [Figure 9-168](#) and described in [Table 9-509](#).

Return to the [Summary Table](#).

Margining Extended Capability Structure is used to configure the device for Receiver Margining.

Table 9-508.
PCIE_CORE_PF0_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0920h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0920h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0920h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0920h

Figure 9-168. PCIE_CORE_PF0_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MARNXCAP												MARCAPVER			
R/W-9C0h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MARCAPID															
R-27h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-509. PCIE_CORE_PF0_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	MARNXCAP	R/W	9C0h	The offset to the next PCI Extended Capability structure.
19-16	MARCAPVER	R/W	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	MARCAPID	R	27h	Indicates that the associated extended capability structure is the Margining Extended Capability. This field returns a Capability ID of 0027h.

Table 9-510. Register Call Summary for
PCIE_CORE_PF0_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG Register \(Offset = 920h\) \[reset = 9C010027h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.149 PCIE_CORE_PFO_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register (Offset = 924h) [reset = 1h]

PCIE_CORE_PFO_I_MARGINING_PORT_CAPABILITIES_STATUS_REG is shown in Figure 9-169 and described in Table 9-512.

Return to the [Summary Table](#).

Margining Port Capabilities and Status Register.

Table 9-511.
PCIE_CORE_PFO_I_MARGINING_PORT_CAPABILITIES_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0924h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0924h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0924h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0924h

Figure 9-169. PCIE_CORE_PFO_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register

31	30	29	28	27	26	25	24
R1							
R-0h							
23	22	21	20	19	18	17	16
R1						MSRDY	MRDY
R-0h						R/W-0h	R-0h
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0							MARUDS
R-0h							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-512. PCIE_CORE_PFO_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	R1	R	0h	Reserved
17	MSRDY	R/W	0h	When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization. The value of this bit is Undefined if Margining users Driver Software is Clear. The Controller implementation sets the default value of this bit to 0. The driver software must initialize the Rx Margining parameters in the Local Management Lane Margining Registers and then program this bit to 1.
16	MRDY	R	0h	Indicates when the Margining feature is ready to accept margining commands. If the Margining uses Driver Software bit is 1, then the Controller sets this status bit when the Margining Software Ready bit is set and the Link is in Gen4 L0 state. If the Margining uses Driver Software bit is 0, then the Controller sets this status bit when the Link is in Gen4 L0 state.
15-1	R0	R	0h	Reserved

Table 9-512. PCIE_CORE_PF0_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	MARUDS	R/W	1h	If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining does not require device driver software. The Controller implementation requires driver software to initialize the Rx Margining parameter values in Local Management Registers for Lane Margining. Hence, the default value of this bit is set to 1.

**Table 9-513. Register Call Summary for
PCIE_CORE_PF0_I_MARGINING_PORT_CAPABILITIES_STATUS_REG**

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register \(Offset = 924h\) \[reset = 1h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.150 PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register (Offset = 928h) [reset = 9C38h]

PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG0 is shown in Figure 9-170 and described in Table 9-515.

Return to the [Summary Table](#).

Margining Lane Control and Status Register for Lane 0.

Table 9-514.
PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0928h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0928h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0928h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0928h

Figure 9-170. PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register

31	30	29	28	27	26	25	24
MPSTS							
R/W-0h							
23	22	21	20	19	18	17	16
R1	UMSTS	MTSTS		RNSTS			
R-0h	R/W-0h	R/W-0h		R/W-0h			
15	14	13	12	11	10	9	8
MRGPAY							
R/W-9Ch							
7	6	5	4	3	2	1	0
R0	USGMOD	MRGTYP		RCVNUM			
R-0h	R/W-0h	R/W-7h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-515. PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MPSTS	R/W	0h	Margin Payload Status for Margining Commands. This field is reset upon DL Down.
23	R1	R	0h	Reserved
22	UMSTS	R/W	0h	Usage Model Status for Margining Commands. This field is reset upon DL Down.
21-19	MTSTS	R/W	0h	Margin Type Status for Margining Commands. This field is reset upon DL Down.
18-16	RNSTS	R/W	0h	Receiver Number Status for Margining Commands. This field is reset upon DL Down.
15-8	MRGPAY	R/W	9Ch	Margin Payload for Margining Commands. This field is reset upon DL Down.
7	R0	R	0h	Reserved
6	USGMOD	R/W	0h	Usage Model for Margining Commands. This field is reset upon DL Down.
5-3	MRGTYP	R/W	7h	Margin Type for Margining Commands. This field is reset upon DL Down.

Table 9-515. PCIE_CORE_PF0_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	RCVNUM	R/W	0h	Receiver Number for Margining Commands. This field is reset upon DL Down.

**Table 9-516. Register Call Summary for
PCIE_CORE_PF0_I_MARGINING_LANE_CONTROL_STATUS_REG0**

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PF0_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register \(Offset = 928h\) \[reset = 9C38h\]: \[0\]](#)

9.2.151 PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register (Offset = 92Ch) [reset = 9C38h]

PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG1 is shown in Figure 9-171 and described in Table 9-518.

Return to the [Summary Table](#).

Margining Lane Control and Status Register for Lane 1.

Table 9-517.
PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 092Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 092Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 092Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 092Ch

Figure 9-171. PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register

31	30	29	28	27	26	25	24
MPSTS							
R/W-0h							
23	22	21	20	19	18	17	16
R1	UMSTS	MTSTS		RNSTS			
R-0h	R/W-0h	R/W-0h		R/W-0h			
15	14	13	12	11	10	9	8
MRGPAY							
R/W-9Ch							
7	6	5	4	3	2	1	0
R0	USGMOD	MRGTYP		RCVNUM			
R-0h	R/W-0h	R/W-7h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-518. PCIE_CORE_PFO_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MPSTS	R/W	0h	Margin Payload Status for Margining Commands. This field is reset upon DL Down.
23	R1	R	0h	Reserved
22	UMSTS	R/W	0h	Usage Model Status for Margining Commands. This field is reset upon DL Down.
21-19	MTSTS	R/W	0h	Margin Type Status for Margining Commands. This field is reset upon DL Down.
18-16	RNSTS	R/W	0h	Receiver Number Status for Margining Commands. This field is reset upon DL Down.
15-8	MRGPAY	R/W	9Ch	Margin Payload for Margining Commands. This field is reset upon DL Down.
7	R0	R	0h	Reserved
6	USGMOD	R/W	0h	Usage Model for Margining Commands. This field is reset upon DL Down.
5-3	MRGTYP	R/W	7h	Margin Type for Margining Commands. This field is reset upon DL Down.

Table 9-518. PCIE_CORE_PF0_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	RCVNUM	R/W	0h	Receiver Number for Margining Commands. This field is reset upon DL Down.

**Table 9-519. Register Call Summary for
PCIE_CORE_PF0_I_MARGINING_LANE_CONTROL_STATUS_REG1**

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register \(Offset = 92Ch\) \[reset = 9C38h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.152 PCIE_CORE_PF0_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = 9C0h) [reset = A2010026h]

PCIE_CORE_PF0_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG is shown in Figure 9-172 and described in Table 9-521.

Return to the [Summary Table](#).

Physical Layer 16 GT/s Extended Capability Structure is used to configure the device for Gen4 Equalization and Gen4 Lane Error Reporting.

Table 9-520.
PCIE_CORE_PF0_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09C0h

Figure 9-172. PCIE_CORE_PF0_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PL16NXCAP												PL16CAPVER			
R/W-A20h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL16CAPID															
R-26h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-521. PCIE_CORE_PF0_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PL16NXCAP	R/W	A20h	The offset to the next PCI Extended Capability structure.
19-16	PL16CAPVER	R/W	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	PL16CAPID	R	26h	Indicates that the associated extended capability structure is for Physical layer 16 GT/s. This field returns a Capability ID of 0026h.

Table 9-522. Register Call Summary for
PCIE_CORE_PF0_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG

PCIE_CORE_EP_PF Registers
<ul style="list-style-type: none"> PCIE_CORE_PF0_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = 9C0h) [reset = A2010026h]: [0] PCIE_CORE_EP_PF Registers: [0] [1]

9.2.153 PCIE_CORE_PF0_I_PL_16GTS_CAPABILITIES_REG Register (Offset = 9C4h) [reset = 0h]

PCIE_CORE_PF0_I_PL_16GTS_CAPABILITIES_REG is shown in Figure 9-173 and described in Table 9-524.

Return to the [Summary Table](#).

Physical Layer 16GTs Capabilities Register.

Table 9-523.
PCIE_CORE_PF0_I_PL_16GTS_CAPABILITIES_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09C4h

Figure 9-173. PCIE_CORE_PF0_I_PL_16GTS_CAPABILITIES_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-524. PCIE_CORE_PF0_I_PL_16GTS_CAPABILITIES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R0	R	0h	Reserved

Table 9-525. Register Call Summary for PCIE_CORE_PF0_I_PL_16GTS_CAPABILITIES_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_PL_16GTS_CAPABILITIES_REG Register \(Offset = 9C4h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.154 PCIE_CORE_PF0_I_PL_16GTS_CONTROL_REG Register (Offset = 9C8h) [reset = 0h]

PCIE_CORE_PF0_I_PL_16GTS_CONTROL_REG is shown in Figure 9-174 and described in Table 9-527.

Return to the [Summary Table](#).

Physical Layer 16GTs Control Register.

Table 9-526.
PCIE_CORE_PF0_I_PL_16GTS_CONTROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09C8h

Figure 9-174. PCIE_CORE_PF0_I_PL_16GTS_CONTROL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-527. PCIE_CORE_PF0_I_PL_16GTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R0	R	0h	Reserved

Table 9-528. Register Call Summary for PCIE_CORE_PF0_I_PL_16GTS_CONTROL_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_PL_16GTS_CONTROL_REG Register \(Offset = 9C8h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.155 PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG Register (Offset = 9CCh) [reset = 0h]

PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG is shown in Figure 9-175 and described in Table 9-530.

Return to the [Summary Table](#).

Physical Layer 16GTs Status Register.

Table 9-529.
PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09CCh

Figure 9-175. PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0			LE16	EP3S16	EP2S16	EP1S16	EQC16
R-0h			R/W-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-530. PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	R0	R	0h	Reserved
4	LE16	R/W	0h	This bit can be set by the software running on the EndPoint to force the Endpoint to request link equalization for 16.0 GT/s. Setting this bit causes the LTSSM of the Controller to enter the Recovery state and request its link partner to perform equalization. This bit is cleared when the LTSSM enters the Recovery.Equalization state. It can also be cleared by writing a 1 to this bit position by the host, or writing a 0 from the LMI. STICKY.
3	EP3S16	R	0h	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.
2	EP2S16	R	0h	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.

Table 9-530. PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EP1S16	R	0h	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.
0	EQC16	R	0h	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed for 16.0 GT/s. STICKY.

Table 9-531. Register Call Summary for PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_PL_16GTS_STATUS_REG Register \(Offset = 9CCh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.156 PCIE_CORE_PF0_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG Register (Offset = 9D0h) [reset = 0h]

PCIE_CORE_PF0_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG is shown in Figure 9-176 and described in Table 9-533.

Return to the [Summary Table](#).

Physical Layer 16GTs Local Data Parity Mismatch Status Register.

Table 9-532.
PCIE_CORE_PF0_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09D0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09D0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09D0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09D0h

Figure 9-176. PCIE_CORE_PF0_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						LDPMS16	
R-0h						R/W1C-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-533. PCIE_CORE_PF0_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	N/A
1-0	LDPMS16	R/W1C	0h	Each bit indicates if the corresponding Lane detected a Data Paritymismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number.

Table 9-534. Register Call Summary for
PCIE_CORE_PF0_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_PF0_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG Register \(Offset = 9D0h\) \[reset = 0h\]: \[0\]](#)

9.2.157 PCIE_CORE_PF0_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register (Offset = 9D4h) [reset = 0h]

PCIE_CORE_PF0_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG is shown in Figure 9-177 and described in Table 9-536.

Return to the [Summary Table](#).

Physical Layer 16GTs First Retimer Data Parity Mismatch Status Register.

Table 9-535.
PCIE_CORE_PF0_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09D4h

Figure 9-177. PCIE_CORE_PF0_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						FRDPMS16	
R-0h						R/W1C-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-536. PCIE_CORE_PF0_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	N/A
1-0	FRDPMS16	R/W1C	0h	Each bit indicates if the first retimer in the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The value of this field is undefined when no Retimers are present.

Table 9-537. Register Call Summary for
PCIE_CORE_PF0_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG

PCIE_CORE_EP_PF Registers
<ul style="list-style-type: none"> PCIE_CORE_PF0_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register (Offset = 9D4h) [reset = 0h]: [0] PCIE_CORE_EP_PF Registers: [0] [1]

9.2.158 PCIE_CORE_PFO_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register (Offset = 9D8h) [reset = 0h]

PCIE_CORE_PFO_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG is shown in Figure 9-178 and described in Table 9-539.

Return to the [Summary Table](#).

Physical Layer 16GTs Second Retimer Data Parity Mismatch Status Register.

Table 9-538.
PCIE_CORE_PFO_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09D8h

Figure 9-178.

PCIE_CORE_PFO_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						SRDPMS16	
R-0h						R/W1C-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-539.

PCIE_CORE_PFO_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	N/A
1-0	SRDPMS16	R/W1C	0h	Each bit indicates if the second retimer in the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The value of this field is undefined when no Retimers are present.

Table 9-540. Register Call Summary for

PCIE_CORE_PFO_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register \(Offset = 9D8h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.159 PCIE_CORE_PF0_I_PL_16GTS_RESERVED_REG Register (Offset = 9DCh) [reset = 0h]

PCIE_CORE_PF0_I_PL_16GTS_RESERVED_REG is shown in Figure 9-179 and described in Table 9-542.

Return to the [Summary Table](#).

Register at offset 1Ch in this capability is Reserved.

Table 9-541.
PCIE_CORE_PF0_I_PL_16GTS_RESERVED_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09DCh

Figure 9-179. PCIE_CORE_PF0_I_PL_16GTS_RESERVED_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-542. PCIE_CORE_PF0_I_PL_16GTS_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R0	R	0h	Reserved

Table 9-543. Register Call Summary for PCIE_CORE_PF0_I_PL_16GTS_RESERVED_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_PL_16GTS_RESERVED_REG Register \(Offset = 9DCh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.160 PCIE_CORE_PF0_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 Register (Offset = 9E0h) [reset = F0F0h]

PCIE_CORE_PF0_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 is shown in Figure 9-180 and described in Table 9-545.

Return to the [Summary Table](#).

This register contains the Upstream Port 16.0GT/s Transmitter Preset for lanes 0, 1, 2 and 3, received from the Downstream Port during the 16GT/s Link Equalization procedure.

Table 9-544.
PCIE_CORE_PF0_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09E0h

Figure 9-180. PCIE_CORE_PF0_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPTP116				R8				UPTP016				R0			
R-Fh				R-0h				R-Fh				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-545. PCIE_CORE_PF0_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-12	UPTP116	R	Fh	16.0GT/s Lane 1 Transmitter Preset value received from the upstream device.
11-8	R8	R	0h	Reserved
7-4	UPTP016	R	Fh	16.0GT/s Lane 0 Transmitter Preset value received from the downstream port during 16GT/s Link Equalization.
3-0	R0	R	0h	Reserved

Table 9-546. Register Call Summary for
PCIE_CORE_PF0_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0

PCIE_CORE_EP_PF Registers

- PCIE_CORE_PF0_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 Register (Offset = 9E0h) [reset = F0F0h]: [0]
- PCIE_CORE_EP_PF Registers: [0] [1]

9.2.161 PCIE_CORE_PFO_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = A20h) [reset = 0001001Fh]

PCIE_CORE_PFO_I_PTM_EXTENDED_CAPABILITY_HEADER_REG is shown in Figure 9-181 and described in Table 9-548.

Return to the [Summary Table](#).

Precision Time Measurement Extended Capability Structure is used discovering and controlling the distribution of a PTM hierarchy.

Table 9-547.
PCIE_CORE_PFO_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0A20h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0A20h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0A20h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0A20h

Figure 9-181. PCIE_CORE_PFO_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PTMNXCAP												PTMCAPVER			
R/W-0h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMCAPIID															
R-1Fh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-548. PCIE_CORE_PFO_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PTMNXCAP	R/W	0h	The offset to the next PCIe Extended Capability structure.
19-16	PTMCAPVER	R/W	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	PTMCAPIID	R	1Fh	Indicates that the associated extended capability structure is for Precision Time Measurement capability. This field returns a Capability ID of 001Fh.

**Table 9-549. Register Call Summary for
PCIE_CORE_PFO_I_PTM_EXTENDED_CAPABILITY_HEADER_REG**

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PFO_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register \(Offset = A20h\) \[reset = 0001001Fh\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.162 PCIe_CORE_PFO_I_PTM_CAPABILITIES_REG Register (Offset = A24h) [reset = 1h]

PCIE_CORE_PFO_I_PTM_CAPABILITIES_REG is shown in Figure 9-182 and described in Table 9-551.

Return to the [Summary Table](#).

PTM Capabilities Register.

Table 9-550.
PCIE_CORE_PFO_I_PTM_CAPABILITIES_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0A24h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0A24h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0A24h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0A24h

Figure 9-182. PCIe_CORE_PFO_I_PTM_CAPABILITIES_REG Register

31	30	29	28	27	26	25	24
R16							
R-0h							
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
LOCCLKGR							
R/W-0h							
7	6	5	4	3	2	1	0
R3				PTMRTCAP		PTMRSCAP	PTMRQCAP
R-0h				R/W-0h		R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-551. PCIe_CORE_PFO_I_PTM_CAPABILITIES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-8	LOCCLKGR	R/W	0h	This field indicates the granularity of the PTM Local Clock in a PTM Time Source. In EP Mode: This field is not used and is set to 8'd00 by default. Note: This bit must not be programmed in EP Mode.
7-3	R3	R	0h	Reserved
2	PTMRTCAP	R/W	0h	This bit is used to indicate that the Controller implements PTM Time Source Role and is capable of serving as PTM Root. By default, this bit is set to 0 when the Controller is in Endpoint Mode. Note: This bit must not be programmed in EP Mode.
1	PTMRSCAP	R/W	0h	This bit is used to indicate support for PTM Responder Role. By default, this bit is set to 0 when the Controller is in Endpoint Mode. Note: This bit must not be programmed in EP Mode.
0	PTMRQCAP	R/W	1h	This bit is used to indicate support for PTM Requester Role. By default, this bit is set to 1 when the Controller is in Endpoint Mode. This bit can be programmed through the local management APB interface if required.

Table 9-552. Register Call Summary for PCIE_CORE_PF0_I_PTM_CAPABILITIES_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_PTM_CAPABILITIES_REG Register \(Offset = A24h\) \[reset = 1h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.2.163 PCIE_CORE_PFO_I_PTM_CONTROL_REG Register (Offset = A28h) [reset = 0h]

PCIE_CORE_PFO_I_PTM_CONTROL_REG is shown in [Figure 9-183](#) and described in [Table 9-554](#).

Return to the [Summary Table](#).

PTM Control Register.

Table 9-553.
PCIE_CORE_PFO_I_PTM_CONTROL_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0A28h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0A28h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0A28h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0A28h

Figure 9-183. PCIE_CORE_PFO_I_PTM_CONTROL_REG Register

31	30	29	28	27	26	25	24
R16							
R-0h							
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
EFFGRN							
R/W-0h							
7	6	5	4	3	2	1	0
R2						RTSEL	PTMEN
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-554. PCIE_CORE_PFO_I_PTM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-8	EFFGRN	R/W	0h	In EP Mode: This field provides information relating to the expected accuracy of the PTM Clock. However, this field does not impact the functionality of the PTM Requester. System SW is expected to program this field with to the value representing the maximum Local Clock Granularity reported by the PTM Root and all the intervening PTM Time Sources.
7-2	R2	R	0h	Reserved
1	RTSEL	R/W	0h	Since Endpoint cannot be a PTM Root, this bit is set to 0 by default in Endpoint Mode. Note: This bit must not be programmed in EP Mode.
0	PTMEN	R/W	0h	When Set, this function is permitted to participate in the PTM mechanism as PTM Requester. By default, this bit is set to 0. This field is configured by System SW.

Table 9-555. Register Call Summary for PCIE_CORE_PF0_I_PTM_CONTROL_REG

PCIE_CORE_EP_PF Registers

- [PCIE_CORE_PF0_I_PTM_CONTROL_REG Register \(Offset = A28h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_PF Registers: \[0\] \[1\]](#)

9.3 PCIE_CORE_EP_VF Registers

Table 9-557 lists the PCIE_CORE_EP_VF registers. All register offset addresses not listed in Table 9-557 should be considered as reserved locations and the register contents should not be modified.

EP mode virtual function (VF) PCIE core registers. There are a total of 16 Virtual Functions, which may be assigned among the 6 Physical Functions.

Table 9-556. PCIE_CORE_EP_VF Instances

Instance	Base Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0000h

Table 9-557. PCIE_CORE_EP_VF Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE1_CORE_DBN_CFG_PCIE_CORE Physical Address
6000h + formula	PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID		0D00 6000h + formula	0D80 6000h + formula
6004h + formula	PCIE_CORE_VFm_I_COMMAND_STATUS		0D00 6004h + formula	0D80 6004h + formula
6008h + formula	PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE		0D00 6008h + formula	0D80 6008h + formula
600Ch + formula	PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CACHE_LINE		0D00 600Ch + formula	0D80 600Ch + formula
6010h + formula	PCIE_CORE_VFm_I_BAR_0_REG		0D00 6010h + formula	0D80 6010h + formula
6014h + formula	PCIE_CORE_VFm_I_BAR_1_REG		0D00 6014h + formula	0D80 6014h + formula
6018h + formula	PCIE_CORE_VFm_I_BAR_2_REG		0D00 6018h + formula	0D80 6018h + formula
601Ch + formula	PCIE_CORE_VFm_I_BAR_3_REG		0D00 601Ch + formula	0D80 601Ch + formula
6020h + formula	PCIE_CORE_VFm_I_BAR_4_REG		0D00 6020h + formula	0D80 6020h + formula
6024h + formula	PCIE_CORE_VFm_I_BAR_5_REG		0D00 6024h + formula	0D80 6024h + formula
6028h + formula	PCIE_CORE_VFm_RSVD_0A		0D00 6028h + formula	0D80 6028h + formula
602Ch + formula	PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I		0D00 602Ch + formula	0D80 602Ch + formula
6030h + formula	PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG		0D00 6030h + formula	0D80 6030h + formula
6034h + formula	PCIE_CORE_VFm_I_CAPABILITIES_POINTER		0D00 6034h + formula	0D80 6034h + formula
6038h + formula	PCIE_CORE_VFm_RSVD_0E		0D00 6038h + formula	0D80 6038h + formula
603Ch + formula	PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG		0D00 603Ch + formula	0D80 603Ch + formula
6040h + formula	PCIE_CORE_VFm_RSVD_010_01F		0D00 6040h + formula	0D80 6040h + formula
6080h + formula	PCIE_CORE_VFm_I_PWR_MGMT_CAP		0D00 6080h + formula	0D80 6080h + formula
6084h + formula	PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP		0D00 6084h + formula	0D80 6084h + formula

Table 9-557. PCIE_CORE_EP_VF Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
6088h + formula	PCIE_CORE_VFm_RSVD_022_023		0D00 6088h + formula	0D80 6088h + formula
6090h + formula	PCIE_CORE_VFm_I_MSI_CTRL_REG		0D00 6090h + formula	0D80 6090h + formula
6094h + formula	PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR		0D00 6094h + formula	0D80 6094h + formula
6098h + formula	PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR		0D00 6098h + formula	0D80 6098h + formula
609Ch + formula	PCIE_CORE_VFm_I_MSI_MSG_DATA		0D00 609Ch + formula	0D80 609Ch + formula
60A0h + formula	PCIE_CORE_VFm_I_MSI_MASK		0D00 60A0h + formula	0D80 60A0h + formula
60A4h + formula	PCIE_CORE_VFm_I_MSI_PENDING_BITS		0D00 60A4h + formula	0D80 60A4h + formula
60A8h + formula	PCIE_CORE_VFm_RSVD_02A_02B		0D00 60A8h + formula	0D80 60A8h + formula
60B0h + formula	PCIE_CORE_VFm_I_MSIX_CTRL		0D00 60B0h + formula	0D80 60B0h + formula
60B4h + formula	PCIE_CORE_VFm_I_MSIX_TBL_OFFSET		0D00 60B4h + formula	0D80 60B4h + formula
60B8h + formula	PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT		0D00 60B8h + formula	0D80 60B8h + formula
60BCh + formula	PCIE_CORE_VFm_RSVD_02F		0D00 60BCh + formula	0D80 60BCh + formula
60C0h + formula	PCIE_CORE_VFm_I_PCIE_CAP_LIST		0D00 60C0h + formula	0D80 60C0h + formula
60C4h + formula	PCIE_CORE_VFm_I_PCIE_DEV_CAP		0D00 60C4h + formula	0D80 60C4h + formula
60C8h + formula	PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS		0D00 60C8h + formula	0D80 60C8h + formula
60CCh + formula	PCIE_CORE_VFm_I_LINK_CAP		0D00 60CCh + formula	0D80 60CCh + formula
60D0h + formula	PCIE_CORE_VFm_RSVD_034_038		0D00 60D0h + formula	0D80 60D0h + formula
60E4h + formula	PCIE_CORE_VFm_I_PCIE_DEV_CAP_2		0D00 60E4h + formula	0D80 60E4h + formula
60E8h + formula	PCIE_CORE_VFm_RSVD_03A_03F		0D00 60E8h + formula	0D80 60E8h + formula
6100h + formula	PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR		0D00 6100h + formula	0D80 6100h + formula
6104h + formula	PCIE_CORE_VFm_I_UNCORR_ERR_STATUS		0D00 6104h + formula	0D80 6104h + formula
6108h + formula	PCIE_CORE_VFm_I_UNCORR_ERR_MASK		0D00 6108h + formula	0D80 6108h + formula
610Ch + formula	PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY		0D00 610Ch + formula	0D80 610Ch + formula
6110h + formula	PCIE_CORE_VFm_I_CORR_ERR_STATUS		0D00 6110h + formula	0D80 6110h + formula
6114h + formula	PCIE_CORE_VFm_I_CORR_ERR_MASK		0D00 6114h + formula	0D80 6114h + formula
6118h + formula	PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL		0D00 6118h + formula	0D80 6118h + formula

Table 9-557. PCIE_CORE_EP_VF Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
611Ch + formula	PCIE_CORE_VFm_I_HDR_LOG_0		0D00 611Ch + formula	0D80 611Ch + formula
6120h + formula	PCIE_CORE_VFm_I_HDR_LOG_1		0D00 6120h + formula	0D80 6120h + formula
6124h + formula	PCIE_CORE_VFm_I_HDR_LOG_2		0D00 6124h + formula	0D80 6124h + formula
6128h + formula	PCIE_CORE_VFm_I_HDR_LOG_3		0D00 6128h + formula	0D80 6128h + formula
612Ch + formula	PCIE_CORE_VFm_RSVD_04B_04D		0D00 612Ch + formula	0D80 612Ch + formula
6138h + formula	PCIE_CORE_VFm_I_TLP_PRE_LOG_0		0D00 6138h + formula	0D80 6138h + formula
6140h + formula	PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR		0D00 6140h + formula	0D80 6140h + formula
6144h + formula	PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL		0D00 6144h + formula	0D80 6144h + formula
6148h + formula	PCIE_CORE_VFm_RSVD_052_09C		0D00 6148h + formula	0D80 6148h + formula
65C0h + formula	PCIE_CORE_VFm_ATS_CAP_HEADER		0D00 65C0h + formula	0D80 65C0h + formula
65C4h + formula	PCIE_CORE_VFm_ATS_CAP_CONTROL		0D00 65C4h + formula	0D80 65C4h + formula

Table 9-558. PCIE_CORE_EP_VF Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
6000h + formula	PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID		0E00 6000h + formula	0E80 6000h + formula
6004h + formula	PCIE_CORE_VFm_I_COMMAND_STATUS		0E00 6004h + formula	0E80 6004h + formula
6008h + formula	PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE		0E00 6008h + formula	0E80 6008h + formula
600Ch + formula	PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CACHE_LINE		0E00 600Ch + formula	0E80 600Ch + formula
6010h + formula	PCIE_CORE_VFm_I_BAR_0_REG		0E00 6010h + formula	0E80 6010h + formula
6014h + formula	PCIE_CORE_VFm_I_BAR_1_REG		0E00 6014h + formula	0E80 6014h + formula
6018h + formula	PCIE_CORE_VFm_I_BAR_2_REG		0E00 6018h + formula	0E80 6018h + formula
601Ch + formula	PCIE_CORE_VFm_I_BAR_3_REG		0E00 601Ch + formula	0E80 601Ch + formula
6020h + formula	PCIE_CORE_VFm_I_BAR_4_REG		0E00 6020h + formula	0E80 6020h + formula
6024h + formula	PCIE_CORE_VFm_I_BAR_5_REG		0E00 6024h + formula	0E80 6024h + formula
6028h + formula	PCIE_CORE_VFm_RSVD_0A		0E00 6028h + formula	0E80 6028h + formula
602Ch + formula	PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I		0E00 602Ch + formula	0E80 602Ch + formula

Table 9-558. PCIE_CORE_EP_VF Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
6030h + formula	PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG		0E00 6030h + formula	0E80 6030h + formula
6034h + formula	PCIE_CORE_VFm_I_CAPABILITIES_POINTER		0E00 6034h + formula	0E80 6034h + formula
6038h + formula	PCIE_CORE_VFm_RSVD_0E		0E00 6038h + formula	0E80 6038h + formula
603Ch + formula	PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG		0E00 603Ch + formula	0E80 603Ch + formula
6040h + formula	PCIE_CORE_VFm_RSVD_010_01F		0E00 6040h + formula	0E80 6040h + formula
6080h + formula	PCIE_CORE_VFm_I_PWR_MGMT_CAP		0E00 6080h + formula	0E80 6080h + formula
6084h + formula	PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP		0E00 6084h + formula	0E80 6084h + formula
6088h + formula	PCIE_CORE_VFm_RSVD_022_023		0E00 6088h + formula	0E80 6088h + formula
6090h + formula	PCIE_CORE_VFm_I_MSI_CTRL_REG		0E00 6090h + formula	0E80 6090h + formula
6094h + formula	PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR		0E00 6094h + formula	0E80 6094h + formula
6098h + formula	PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR		0E00 6098h + formula	0E80 6098h + formula
609Ch + formula	PCIE_CORE_VFm_I_MSI_MSG_DATA		0E00 609Ch + formula	0E80 609Ch + formula
60A0h + formula	PCIE_CORE_VFm_I_MSI_MASK		0E00 60A0h + formula	0E80 60A0h + formula
60A4h + formula	PCIE_CORE_VFm_I_MSI_PENDING_BITS		0E00 60A4h + formula	0E80 60A4h + formula
60A8h + formula	PCIE_CORE_VFm_RSVD_02A_02B		0E00 60A8h + formula	0E80 60A8h + formula
60B0h + formula	PCIE_CORE_VFm_I_MSIX_CTRL		0E00 60B0h + formula	0E80 60B0h + formula
60B4h + formula	PCIE_CORE_VFm_I_MSIX_TBL_OFFSET		0E00 60B4h + formula	0E80 60B4h + formula
60B8h + formula	PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT		0E00 60B8h + formula	0E80 60B8h + formula
60BCh + formula	PCIE_CORE_VFm_RSVD_02F		0E00 60BCh + formula	0E80 60BCh + formula
60C0h + formula	PCIE_CORE_VFm_I_PCIE_CAP_LIST		0E00 60C0h + formula	0E80 60C0h + formula
60C4h + formula	PCIE_CORE_VFm_I_PCIE_DEV_CAP		0E00 60C4h + formula	0E80 60C4h + formula
60C8h + formula	PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS		0E00 60C8h + formula	0E80 60C8h + formula
60CCh + formula	PCIE_CORE_VFm_I_LINK_CAP		0E00 60CCh + formula	0E80 60CCh + formula
60D0h + formula	PCIE_CORE_VFm_RSVD_034_038		0E00 60D0h + formula	0E80 60D0h + formula
60E4h + formula	PCIE_CORE_VFm_I_PCIE_DEV_CAP_2		0E00 60E4h + formula	0E80 60E4h + formula
60E8h + formula	PCIE_CORE_VFm_RSVD_03A_03F		0E00 60E8h + formula	0E80 60E8h + formula

Table 9-558. PCIE_CORE_EP_VF Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
6100h + formula	PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR		0E00 6100h + formula	0E80 6100h + formula
6104h + formula	PCIE_CORE_VFm_I_UNCORR_ERR_STATUS		0E00 6104h + formula	0E80 6104h + formula
6108h + formula	PCIE_CORE_VFm_I_UNCORR_ERR_MASK		0E00 6108h + formula	0E80 6108h + formula
610Ch + formula	PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY		0E00 610Ch + formula	0E80 610Ch + formula
6110h + formula	PCIE_CORE_VFm_I_CORR_ERR_STATUS		0E00 6110h + formula	0E80 6110h + formula
6114h + formula	PCIE_CORE_VFm_I_CORR_ERR_MASK		0E00 6114h + formula	0E80 6114h + formula
6118h + formula	PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL		0E00 6118h + formula	0E80 6118h + formula
611Ch + formula	PCIE_CORE_VFm_I_HDR_LOG_0		0E00 611Ch + formula	0E80 611Ch + formula
6120h + formula	PCIE_CORE_VFm_I_HDR_LOG_1		0E00 6120h + formula	0E80 6120h + formula
6124h + formula	PCIE_CORE_VFm_I_HDR_LOG_2		0E00 6124h + formula	0E80 6124h + formula
6128h + formula	PCIE_CORE_VFm_I_HDR_LOG_3		0E00 6128h + formula	0E80 6128h + formula
612Ch + formula	PCIE_CORE_VFm_RSVD_04B_04D		0E00 612Ch + formula	0E80 612Ch + formula
6138h + formula	PCIE_CORE_VFm_I_TLP_PRE_LOG_0		0E00 6138h + formula	0E80 6138h + formula
6140h + formula	PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR		0E00 6140h + formula	0E80 6140h + formula
6144h + formula	PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL		0E00 6144h + formula	0E80 6144h + formula
6148h + formula	PCIE_CORE_VFm_RSVD_052_09C		0E00 6148h + formula	0E80 6148h + formula
65C0h + formula	PCIE_CORE_VFm_ATS_CAP_HEADER		0E00 65C0h + formula	0E80 65C0h + formula
65C4h + formula	PCIE_CORE_VFm_ATS_CAP_CONTROL		0E00 65C4h + formula	0E80 65C4h + formula

9.3.1 PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID Register (Offset = 6000h + formula) [reset = FFFFFFFFh]

PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID is shown in Figure 9-184 and described in Table 9-560.

Return to the [Summary Table](#).

Hardwired to all 1's

Offset = 6000h + (m * 1000h); where m = 0h to Fh

Table 9-559.
PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6000h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6000h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6000h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6000h + formula

Figure 9-184. PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DID																VID															
R-FFFFh																R-FFFFh															

LEGEND: R = Read Only; -n = value after reset

Table 9-560. PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DID	R	FFFFh	Device ID assigned by the manufacturer of the device. On power-up, the core sets it to the value defined in the RTL file reg_defaults.h. This field can be written independently for each Function from the local management bus.
15-0	VID	R	FFFFh	A read to this register returns FFFFh for VFs

Table 9-561. Register Call Summary for PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_VENDOR_ID_DEVICE_ID Register \(Offset = 6000h + formula\) \[reset = FFFFFFFFh\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.2 PCIE_CORE_VFm_I_COMMAND_STATUS Register (Offset = 6004h + formula) [reset = 00100000h]

PCIE_CORE_VFm_I_COMMAND_STATUS is shown in Figure 9-185 and described in Table 9-563.

Return to the [Summary Table](#).

This location contains the 16-bit Command Register and the 16-bit Status Register defined in PCI Specifications 3.0.

Offset = 6004h + (m * 1000h); where m = 0h to Fh

Table 9-562.
PCIE_CORE_VFm_I_COMMAND_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6004h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6004h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6004h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6004h + formula

Figure 9-185. PCIE_CORE_VFm_I_COMMAND_STATUS Register

31	30	29	28	27	26	25	24
DPE	SSE	RMA	RTA	STA	R5		MDPE
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h		R/W1C-0h
23	22	21	20	19	18	17	16
R4			CL	IS	R3		
R-0h			R-1h	R-0h	R-0h		
15	14	13	12	11	10	9	8
R3					IMD	R2	SE
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
R1	PERE	R0			BME	MSE	IOSE
R-0h	R-0h	R-0h			R/W-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-563. PCIE_CORE_VFm_I_COMMAND_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DPE	R/W1C	0h	This bit is set when the core has received a Poisoned TLP targeted at this VF. The Parity Error Response enable bit [bit 6] in the PCI Command Register of the associated PF has no effect on the setting of this bit. STICKY.
30	SSE	R/W1C	0h	If the SERR enable bit in the PCI Command Register of the associated Physical Function is 1, this bit is set when this VF has sent out a fatal or non-fatal error message on the link to the Root Complex. If the SERR enable bit is 0, this bit remains 0. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.
29	RMA	R/W1C	0h	This bit is set when this VF has received a completion from the link with the Unsupported Request status. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.

Table 9-563. PCIE_CORE_VFm_I_COMMAND_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	RTA	R/W1C	0h	This bit is set when this Virtual Function has received a completion from the link with the Completer Abort status. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.
27	STA	R/W1C	0h	This bit is set when the core has sent a completion from this VF to the link with the Completer Abort status. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.
26-25	R5	R	0h	Reserved
24	MDPE	R/W1C	0h	When the Parity Error Response enable bit in the PCI Command Register of the associated Physical Function is set, the core sets this bit when it detects the following error conditions: [i] The core receives a Poisoned Completion TLP from the link in response to a request from this VF. [ii] The core sends out a poisoned write request on the link from this VF. [This bit remains 0 when the Parity Error Response enable bit in the PCI Command Register of the associated Physical Function is 0]. This field can also be cleared from the local management bus by writing a 1 into this bit position. STICKY.
23-21	R4	R	0h	Reserved
20	CL	R	1h	Indicates the presence of PCI Extended Capabilities registers. This bit is hardwired to 1.
19	IS	R	0h	Reserved
18-11	R3	R	0h	Reserved
10	IMD	R	0h	Reserved
9	R2	R	0h	Reserved
8	SE	R	0h	Reserved
7	R1	R	0h	Reserved
6	PERE	R	0h	Reserved
5-3	R0	R	0h	Reserved
2	BME	R/W	0h	Enables the device to issue memory requests from this Function. This field can be written from the local management bus.
1	MSE	R	0h	Reserved
0	IOSE	R	0h	Reserved

Table 9-564. Register Call Summary for PCIE_CORE_VFm_I_COMMAND_STATUS

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_COMMAND_STATUS Register \(Offset = 6004h + formula\) \[reset = 00100000h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.3 PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE Register (Offset = 6008h + formula) [reset = 0h]

PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE is shown in Figure 9-186 and described in Table 9-566.

Return to the [Summary Table](#).

This register contains the Revision ID and Class Code associated with the device incorporating the PCIe core.

Offset = 6008h + (m * 1000h); where m = 0h to Fh

Table 9-565.
PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6008h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6008h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6008h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6008h + formula

Figure 9-186. PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC								SCC								PIB								RID							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-566. PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CC	R	0h	Identifies the function of the device. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.
23-16	SCC	R	0h	Identifies a sub-category within the selected function. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.
15-8	PIB	R	0h	Identifies the register set layout of the device. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.
7-0	RID	R	0h	Assigned by the manufacturer of the device to identify the revision number of the device. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.

Table 9-567. Register Call Summary for PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_REVISION_ID_CLASS_CODE Register \(Offset = 6008h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.4 PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CACHE_LINE Register (Offset = 600Ch + formula) [reset = 0h]

PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CACHE_LINE is shown in Figure 9-187 and described in Table 9-569.

Return to the [Summary Table](#).

This location contains the BIST, header-type, Latency Timer and Cache Line Size Registers.

Offset = 600Ch + (m * 1000h); where m = 0h to Fh

Table 9-568.
PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CAC
HE_LINE Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 600Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 600Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 600Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 600Ch + formula

Figure 9-187. PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CACHE_LINE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BR								DT	HT						
R-0h								R-0h	R-0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LT								CLS							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-569. PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CACHE_LINE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BR	R	0h	Reserved
23	DT	R	0h	Identifies whether the device supports a single Function or multiple Functions. This bit is read as 0 when only Function 0 has been enabled in the Physical Function Configuration Register [in the local management block]. Reserved for VFs
22-16	HT	R	0h	Reserved
15-8	LT	R	0h	Reserved
7-0	CLS	R	0h	Reserved

Table 9-570. Register Call Summary for PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CACHE_LINE

PCIE_CORE_EP_VF Registers

- PCIE_CORE_VFm_I_BIST_HEADER_LATENCY_CACHE_LINE Register (Offset = 600Ch + formula) [reset = 0h]: [0]
- PCIE_CORE_EP_VF Registers: [0] [1]

9.3.5 PCIE_CORE_VFm_I_BAR_0_REG Register (Offset = 6010h + formula) [reset = 0h]

PCIE_CORE_VFm_I_BAR_0_REG is shown in [Figure 9-188](#) and described in [Table 9-572](#).

Return to the [Summary Table](#).

Not Implemented

Offset = 6010h + (m * 1000h); where m = 0h to Fh

**Table 9-571. PCIE_CORE_VFm_I_BAR_0_REG
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6010h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6010h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6010h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6010h + formula

Figure 9-188. PCIE_CORE_VFm_I_BAR_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-572. PCIE_CORE_VFm_I_BAR_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NI	R	0h	N/A

Table 9-573. Register Call Summary for PCIE_CORE_VFm_I_BAR_0_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_BAR_0_REG Register \(Offset = 6010h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.6 PCIE_CORE_VFm_I_BAR_1_REG Register (Offset = 6014h + formula) [reset = 0h]

PCIE_CORE_VFm_I_BAR_1_REG is shown in [Figure 9-189](#) and described in [Table 9-575](#).

Return to the [Summary Table](#).

Not Implemented

Offset = 6014h + (m * 1000h); where m = 0h to Fh

Table 9-574. PCIE_CORE_VFm_I_BAR_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6014h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6014h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6014h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6014h + formula

Figure 9-189. PCIE_CORE_VFm_I_BAR_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-575. PCIE_CORE_VFm_I_BAR_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NI	R	0h	N/A

Table 9-576. Register Call Summary for PCIE_CORE_VFm_I_BAR_1_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_VFm_I_BAR_1_REG Register \(Offset = 6014h + formula\) \[reset = 0h\]: \[0\]](#)

9.3.7 PCIE_CORE_VFm_I_BAR_2_REG Register (Offset = 6018h + formula) [reset = 0h]

PCIE_CORE_VFm_I_BAR_2_REG is shown in [Figure 9-190](#) and described in [Table 9-578](#).

Return to the [Summary Table](#).

Not Implemented

Offset = 6018h + (m * 1000h); where m = 0h to Fh

**Table 9-577. PCIE_CORE_VFm_I_BAR_2_REG
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6018h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6018h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6018h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6018h + formula

Figure 9-190. PCIE_CORE_VFm_I_BAR_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-578. PCIE_CORE_VFm_I_BAR_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NI	R	0h	N/A

Table 9-579. Register Call Summary for PCIE_CORE_VFm_I_BAR_2_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_BAR_2_REG Register \(Offset = 6018h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.8 PCIE_CORE_VFm_I_BAR_3_REG Register (Offset = 601Ch + formula) [reset = 0h]

PCIE_CORE_VFm_I_BAR_3_REG is shown in [Figure 9-191](#) and described in [Table 9-581](#).

Return to the [Summary Table](#).

Not Implemented

Offset = 601Ch + (m * 1000h); where m = 0h to Fh

Table 9-580. PCIE_CORE_VFm_I_BAR_3_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 601Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 601Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 601Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 601Ch + formula

Figure 9-191. PCIE_CORE_VFm_I_BAR_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-581. PCIE_CORE_VFm_I_BAR_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NI	R	0h	N/A

Table 9-582. Register Call Summary for PCIE_CORE_VFm_I_BAR_3_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_BAR_3_REG Register \(Offset = 601Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.9 PCIE_CORE_VFm_I_BAR_4_REG Register (Offset = 6020h + formula) [reset = 0h]

PCIE_CORE_VFm_I_BAR_4_REG is shown in [Figure 9-192](#) and described in [Table 9-584](#).

Return to the [Summary Table](#).

Not Implemented

Offset = 6020h + (m * 1000h); where m = 0h to Fh

**Table 9-583. PCIE_CORE_VFm_I_BAR_4_REG
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6020h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6020h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6020h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6020h + formula

Figure 9-192. PCIE_CORE_VFm_I_BAR_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-584. PCIE_CORE_VFm_I_BAR_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NI	R	0h	N/A

Table 9-585. Register Call Summary for PCIE_CORE_VFm_I_BAR_4_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_BAR_4_REG Register \(Offset = 6020h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.10 PCIE_CORE_VFm_I_BAR_5_REG Register (Offset = 6024h + formula) [reset = 0h]

PCIE_CORE_VFm_I_BAR_5_REG is shown in [Figure 9-193](#) and described in [Table 9-587](#).

Return to the [Summary Table](#).

Not Implemented

Offset = 6024h + (m * 1000h); where m = 0h to Fh

Table 9-586. PCIE_CORE_VFm_I_BAR_5_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6024h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6024h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6024h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6024h + formula

Figure 9-193. PCIE_CORE_VFm_I_BAR_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-587. PCIE_CORE_VFm_I_BAR_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NI	R	0h	N/A

Table 9-588. Register Call Summary for PCIE_CORE_VFm_I_BAR_5_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_BAR_5_REG Register \(Offset = 6024h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.11 PCIE_CORE_VFm_RSVD_0A Register (Offset = 6028h + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_0A is shown in [Figure 9-194](#) and described in [Table 9-590](#).

Return to the [Summary Table](#).

Reserved

Offset = 6028h + (m * 1000h); where m = 0h to Fh

Table 9-589. PCIE_CORE_VFm_RSVD_0A Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6028h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6028h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6028h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6028h + formula

Figure 9-194. PCIE_CORE_VFm_RSVD_0A Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-590. PCIE_CORE_VFm_RSVD_0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-591. Register Call Summary for PCIE_CORE_VFm_RSVD_0A

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_RSVD_0A Register \(Offset = 6028h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.12 PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Register (Offset = 602Ch + formula) [reset = 17CDh]

PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I is shown in Figure 9-195 and described in Table 9-593.

Return to the [Summary Table](#).

This register contains the Subsystem Vendor ID and Subsystem ID associated with the device incorporating the PCIe core.

Offset = 602Ch + (m * 1000h); where m = 0h to Fh

Table 9-592.
PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 602Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 602Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 602Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 602Ch + formula

Figure 9-195. PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SID																SVID															
R-0h																R-17CDh															

LEGEND: R = Read Only; -n = value after reset

Table 9-593. PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SID	R	0h	Specifies the Subsystem ID assigned by the manufacturer of the device. This field reflects the setting of the corresponding register in the configuration space of the associated Physical Function.
15-0	SVID	R	17CDh	Specifies the Subsystem Vendor ID assigned by the PCI SIG to the manufacturer of the device. Its value comes from the Subsystem Vendor ID Register in the local management register block.

Table 9-594. Register Call Summary for PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_VFm_I_SUBSYSTEM_VENDOR_ID_SUBSYSTEM_I Register \(Offset = 602Ch + formula\) \[reset = 17CDh\]: \[0\]](#)

9.3.13 PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG Register (Offset = 6030h + formula) [reset = 0h]

PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG is shown in Figure 9-196 and described in Table 9-596.

Return to the [Summary Table](#).

Not Implemented

Offset = 6030h + (m * 1000h); where m = 0h to Fh

Table 9-595.
PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6030h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6030h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6030h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6030h + formula

Figure 9-196. PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-596. PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NI	R	0h	N/A

Table 9-597. Register Call Summary for PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_EXPANSN_ROM_BAR_REG Register \(Offset = 6030h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.14 PCIE_CORE_VFm_I_CAPABILITIES_POINTER Register (Offset = 6034h + formula) [reset = 80h]

PCIE_CORE_VFm_I_CAPABILITIES_POINTER is shown in Figure 9-197 and described in Table 9-599.

Return to the [Summary Table](#).

This location contains the pointer to the first PCI Capability Structure. Its default value is defined in the RTL file reg_defaults.h.

Offset = 6034h + (m * 1000h); where m = 0h to Fh

Table 9-598.
PCIE_CORE_VFm_I_CAPABILITIES_POINTER
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6034h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6034h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6034h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6034h + formula

Figure 9-197. PCIE_CORE_VFm_I_CAPABILITIES_POINTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R6																CP															
R-0h																R/W-80h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-599. PCIE_CORE_VFm_I_CAPABILITIES_POINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R6	R	0h	Reserved
7-0	CP	R/W	80h	Contains pointer to the first PCI Capability Structure. This field is set by default to point to the Power Management Capability Structure. It can be modified by writing to VF 0 from the local management bus, and the setting is common across all VFs.

Table 9-600. Register Call Summary for PCIE_CORE_VFm_I_CAPABILITIES_POINTER

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_CAPABILITIES_POINTER Register \(Offset = 6034h + formula\) \[reset = 80h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.15 PCIE_CORE_VFm_RSVD_0E Register (Offset = 6038h + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_0E is shown in [Figure 9-198](#) and described in [Table 9-602](#).

Return to the [Summary Table](#).

Reserved

Offset = 6038h + (m * 1000h); where m = 0h to Fh

Table 9-601. PCIE_CORE_VFm_RSVD_0E Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6038h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6038h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6038h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6038h + formula

Figure 9-198. PCIE_CORE_VFm_RSVD_0E Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-602. PCIE_CORE_VFm_RSVD_0E Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-603. Register Call Summary for PCIE_CORE_VFm_RSVD_0E

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_RSVD_0E Register \(Offset = 6038h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.16 PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG Register (Offset = 603Ch + formula) [reset = 0h]

PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG is shown in [Figure 9-199](#) and described in [Table 9-605](#).

Return to the [Summary Table](#).

Not Implemented

Offset = 6003Ch + (m * 1000h); where m = 0h to Fh

Table 9-604.
PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 603Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 603Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 603Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 603Ch + formula

Figure 9-199. PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NI																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-605. PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NI	R	0h	N/A

Table 9-606. Register Call Summary for PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_INTRPT_LINE_INTRPT_PIN_REG Register \(Offset = 603Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.17 PCIE_CORE_VFm_RSVD_010_01F Register (Offset = 6040h + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_010_01F is shown in [Figure 9-200](#) and described in [Table 9-608](#).

Return to the [Summary Table](#).

Reserved

Offset = 6040h + (m * 1000h); where m = 0h to Fh

**Table 9-607. PCIE_CORE_VFm_RSVD_010_01F
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6040h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6040h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6040h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6040h + formula

Figure 9-200. PCIE_CORE_VFm_RSVD_010_01F Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-608. PCIE_CORE_VFm_RSVD_010_01F Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-609. Register Call Summary for PCIE_CORE_VFm_RSVD_010_01F

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_RSVD_010_01F Register \(Offset = 6040h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.18 PCIE CORE VFm | PWR MGMT CAP Register (Offset = 6080h + formula) [reset = 5A039001h]

PCIE CORE VFm I PWR MGMT CAP is shown in Figure 9-201 and described in Table 9-611.

Return to the [Summary Table](#).

This location contains the Power Management Capabilities Register, its Capability ID, and a pointer to the next capability. This version of the core supports the PCI power states D0, D1 and D3.

Offset = 6080h + (m * 1000h); where m = 0h to Fh

Table 9-610. PCIE_CORE_VFm_I_PWR_MGMT_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6080h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6080h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6080h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6080h + formula

Figure 9-201. PCIE CORE VFm I PWR MGMT CAP Register

Figure 3-10. R/W-0h, R/W-1h, R/W-2h, R/W-3h, R/W-90h, and R/W-90h Registers								
31	30		29	28	27	26	25	24
PSDCS	PSDHS	PSD2S	PSD1S	PSD0S	D2S	D1S	MCRAPS	
R-0h	R/W-1h	R-0h	R/W-1h	R/W-1h	R-0h	R/W-1h	R-0h	
23	22	21	20	19	18	17	16	
MCRAPS		DSI	R0	PC	VID			
R-0h		R-0h	R-0h	R-0h	R/W-3h			
15	14	13	12	11	10	9	8	
CP								
R/W-90h								
7	6	5	4	3	2	1	0	
CID								
R/W-1h								

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-611. PCIE CORE VFm I PWR MGMT CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PSDCS	R	0h	Indicates whether the Function is capable of sending PME messages when in the D3cold state. Because the device does not have aux power, this bit is hardwired to 0.
30	PSDHS	R/W	1h	Indicates whether the Function is capable of sending PME messages when in the D3hot state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.
29	PSD2S	R	0h	Indicates whether the Function is capable of sending PME messages when in the D2 state. This bit is hardwired to 0 because D2 state is not supported.

Table 9-611. PCIE_CORE_VFm_I_PWR_MGMT_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	PSD1S	R/W	1h	Indicates whether the Function is capable of sending PME messages when in the D1 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.
27	PSD0S	R/W	1h	Indicates whether the Function is capable of sending PME messages when in the D0 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.
26	D2S	R	0h	Set if the Function supports the D2 power state. Currently hardwired to 0.
25	D1S	R/W	1h	Set if the Function supports the D1 power state. This bit can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.
24-22	MCRAPS	R	0h	Specifies the maximum current drawn by the device from the aux power source in the D3cold state. This field is not implemented in devices not supporting PME notification when in the D3cold state, and is therefore hardwired to 0.
21	DSI	R	0h	This bit, when set, indicates that the device requires additional configuration steps beyond setting up its PCI configuration space, to bring it to the D0active state from the D0uninitialized state. This bit is hardwired to 0.
20	R0	R	0h	Reserved
19	PC	R	0h	Not applicable to PCI Express. This bit is hardwired to 0.
18-16	VID	R/W	3h	Indicates the version of the PCI Bus Power Management Specifications that the Function implements. This field is set by default to 011 [Version 1.2]. It can be re-written independently for each Function from the local management bus.
15-8	CP	R/W	90h	Contains pointer to the next PCI Capability Structure. The core sets it to the value defined in the RTL file reg_defaults.h. By default, this points to the MSI Capability Structure. This field can be re-written independently for each Function from the local management bus.
7-0	CID	R/W	1h	Identifies that the capability structure is for Power Management. This field is set by default to 01 hex. It can be re-written independently for each Function from the local management bus.

Table 9-612. Register Call Summary for PCIE_CORE_VFm_I_PWR_MGMT_CAP

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_PWR_MGMT_CAP Register \(Offset = 6080h + formula\) \[reset = 5A039001h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.19 PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP Register (Offset = 6084h + formula) [reset = 8h]

PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP is shown in Figure 9-202 and described in Table 9-614.

Return to the [Summary Table](#).

This location contains the 16-bit Power Management Control/Status Register.

Offset = 6084h + (m * 1000h); where m = 0h to Fh

Table 9-613.
PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6084h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6084h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6084h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6084h + formula

Figure 9-202. PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP Register

31	30	29	28	27	26	25	24
DR							
R-0h							
23	22	21	20	19	18	17	16
R1							
R-0h							
15	14	13	12	11	10	9	8
PMES	R2						PE
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
R3				NSR	R4	PS	
R-0h				R/W-1h	R-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-614. PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DR	R	0h	This optional register is not implemented in the PCIe core. This field is hardwired to 0.
23-16	R1	R	0h	Reserved
15	PMES	R/W	0h	When PME notification is enabled, writing a 1 into this bit position from the local management bus sets this bit and causes the core to send a PME message from the associated Function. When the Root Complex processes this message, it will turn off this bit by writing a 1 into this bit position through a Config Write. This bit can be set or cleared from the local management bus, by writing a 1 or 0, respectively. It can only be cleared from the configuration path [by writing a 1].
14-9	R2	R	0h	Reserved

Table 9-614. PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	PE	R/W	0h	Setting this bit enables the notification of PME events from the associated Function. This bit can be set also by writing into this register from the local management bus.
7-4	R3	R	0h	Reserved
3	NSR	R/W	1h	When this bit is set to 1, the Function will maintain all its state in the PM state D3hot. The software is not required to re-initialize the Function registers on the transition back to D0. This bit is set to 1 by default, but can be modified independently for each VF from the local management bus.
2	R4	R	0h	Reserved
1-0	PS	R/W	0h	Indicates the power state this Function is currently in. This field can be read by the software to monitor the current power state, or can be written to cause a transition to a new state. The valid settings are 00 [state D0], 01 [state D1] and 11 [state D3hot]. The software should not write any other value into this field. This field can also be written from the local management bus independently for each VF Function.

Table 9-615. Register Call Summary for PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_PWR_MGMT_CTRL_STAT_REP Register \(Offset = 6084h + formula\) \[reset = 8h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.20 PCIE_CORE_VFm_RSVD_022_023 Register (Offset = 6088h + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_022_023 is shown in [Figure 9-203](#) and described in [Table 9-617](#).

Return to the [Summary Table](#).

Reserved

Offset = 6088h + (m * 1000h); where m = 0h to Fh

**Table 9-616. PCIE_CORE_VFm_RSVD_022_023
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6088h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6088h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6088h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6088h + formula

Figure 9-203. PCIE_CORE_VFm_RSVD_022_023 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-617. PCIE_CORE_VFm_RSVD_022_023 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-618. Register Call Summary for PCIE_CORE_VFm_RSVD_022_023

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_VFm_RSVD_022_023 Register \(Offset = 6088h + formula\) \[reset = 0h\]: \[0\]](#)

9.3.21 PCIE_CORE_VFm_I_MSI_CTRL_REG Register (Offset = 6090h + formula) [reset = 0180B005h]

PCIE_CORE_VFm_I_MSI_CTRL_REG is shown in Figure 9-204 and described in Table 9-620.

Return to the [Summary Table](#).

This register is used only when the core is configured to support Message Signaled Interrupts (MSIs). In addition to the MSI control bits, this location also contains the MSI Capability ID and the pointer to the next PCI Capability Structure.

Offset = 6090h + (m * 1000h); where m = 0h to Fh

Table 9-619. PCIE_CORE_VFm_I_MSI_CTRL_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6090h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6090h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6090h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6090h + formula

Figure 9-204. PCIE_CORE_VFm_I_MSI_CTRL_REG Register

31	30	29	28	27	26	25	24
R0							MC
R-0h							R/W-1h
23	22	21	20	19	18	17	16
AC64	MME			MMC			ME
R/W-1h	R/W-0h			R/W-0h			R/W-0h
15	14	13	12	11	10	9	8
CP							
R-B0h							
7	6	5	4	3	2	1	0
CID							
R-5h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-620. PCIE_CORE_VFm_I_MSI_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	R0	R	0h	Reserved
24	MC	R/W	1h	can be modified using localmanagement interface
23	AC64	R/W	1h	Set to 1 to indicate that the device is capable of generating 64-bit addresses for MSI messages.
22-20	MME	R/W	0h	Encodes the number of distinct messages that the core is programmed to generate for this Function [000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32]. This setting must be based on the number of interrupt inputs of the core that are actually used by this Function. This field can be written from the local management bus.

Table 9-620. PCIE_CORE_VFm_I_MSI_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-17	MMC	R/W	0h	Encodes the number of distinct messages that the core is capable of generating for this Function [000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32]. Thus, this field defines the number of the interrupt vectors for this Function. The core allows up to 32 distinct messages, but the setting of this field must be based on the number of interrupt inputs of the core that are actually used by the client. For example, if the client logic uses 8 of the 32 distinct MSI interrupt inputs of the core for this Function, then the value of this field must be set to 011. This field can be written from the local management bus. Please see the define <code>den_db_VF_MSI_MULTIPLE_MSG_CAPABLE</code> for default value in the <code>reg_defaults.v</code> files.
16	ME	R/W	0h	Set by the configuration program to enable the MSI feature. This field can also be written from the local management bus.
15-8	CP	R	B0h	Pointer to the next PCI Capability Structure. The value read from this read-only field is the corresponding pointer in the MSI Capability Structure of the Physical Function this VF is attached to. The setting is common across all the Virtual Functions.
7-0	CID	R	5h	Specifies that the capability structure is for MSI. Hardwired to 05 hex.

Table 9-621. Register Call Summary for PCIE_CORE_VFm_I_MSI_CTRL_REG

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_MSI_CTRL_REG Register \(Offset = 6090h + formula\) \[reset = 0180B005h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.22 PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR Register (Offset = 6094h + formula) [reset = 0h]

PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR is shown in Figure 9-205 and described in Table 9-623.

Return to the [Summary Table](#).

This register contains the first 32 bits of the address to be used in the MSI messages generated by the core for this Function. This address is taken as a 32-bit address if the value programmed in the MSI Message High Address Register is 0. Otherwise, this address is taken as the least significant 32 bits of the 64-bit address sent in MSI messages.

Offset = 6094h + (m * 1000h); where m = 0h to Fh

Table 9-622.
PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6094h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6094h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6094h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6094h + formula

Figure 9-205. PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAL																R1															
R/W-0h																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-623. PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	MAL	R/W	0h	Lower bits of the address to be used in MSI messages. This field can also be written from the local management bus.
1-0	R1	R	0h	The two lower bits of the address are hardwired to 0 to align the address on a double-word boundary.

Table 9-624. Register Call Summary for PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_MSI_MSG_LOW_ADDR Register \(Offset = 6094h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.23 PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR Register (Offset = 6098h + formula) [reset = 0h]

PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR is shown in [Figure 9-206](#) and described in [Table 9-626](#).

Return to the [Summary Table](#).

This register contains the 32 most significant bits of the 64-bit address sent by the core in MSI messages. A value of all zeroes in the register is taken to mean that the core should use 32-bit addresses in the messages.

Offset = 6098h + (m * 1000h); where m = 0h to Fh

Table 9-625.
PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6098h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6098h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6098h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6098h + formula

Figure 9-206. PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-626. PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAH	R/W	0h	Contains bits 63:32 of the 64-bit address to be used in MSI Messages. A value of 0 specifies that 32-bit addresses are to be used in the messages. This field can also be written from the local management bus.

Table 9-627. Register Call Summary for PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_MSI_MSG_HI_ADDR Register \(Offset = 6098h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.24 PCIE_CORE_VFm_I_MSI_MSG_DATA Register (Offset = 609Ch + formula) [reset = 0h]

PCIE_CORE_VFm_I_MSI_MSG_DATA is shown in [Figure 9-207](#) and described in [Table 9-629](#).

Return to the [Summary Table](#).

This register contains the write data to be used in the MSI messages to be generated for the associated PCI Function. When the number of distinct messages programmed in the MSI Control Register is 1, the 32-bit value from this register is used as the data value in the MSI packets generated by the core for this Function. If the number of distinct messages is more than 1, the least significant bits of the programmed value are replaced with the encoded interrupt vector [31:0] of the specific message to generate the write data value for the message.

Offset = 609Ch + (m * 1000h); where m = 0h to Fh

Table 9-628. PCIE_CORE_VFm_I_MSI_MSG_DATA Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 609Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 609Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 609Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 609Ch + formula

Figure 9-207. PCIE_CORE_VFm_I_MSI_MSG_DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R2																MD															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-629. PCIE_CORE_VFm_I_MSI_MSG_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R2	R	0h	Hardwired to 0
15-0	MD	R/W	0h	Message data to be used for this Function. This field can also be written from the local management bus.

Table 9-630. Register Call Summary for PCIE_CORE_VFm_I_MSI_MSG_DATA

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_MSI_MSG_DATA Register \(Offset = 609Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.25 PCIE_CORE_VFm_I_MSI_MASK Register (Offset = 60A0h + formula) [reset = 0h]

PCIE_CORE_VFm_I_MSI_MASK is shown in Figure 9-208 and described in Table 9-632.

Return to the [Summary Table](#).

This register contains the MSI mask bits, one for each of the interrupt levels.

Offset = 60A0h + (m * 1000h); where m = 0h to Fh

**Table 9-631. PCIE_CORE_VFm_I_MSI_MASK
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60A0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60A0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60A0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60A0h + formula

Figure 9-208. PCIE_CORE_VFm_I_MSI_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0														MM	
R-0h														R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-632. PCIE_CORE_VFm_I_MSI_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R0	R	0h	Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of this field also changes correspondingly
0	MM	R/W	0h	Mask bits for MSI interrupts. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid mask bits. Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of the MSI Mask field also changes correspondingly

Table 9-633. Register Call Summary for PCIE_CORE_VFm_I_MSI_MASK

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_MSI_MASK Register \(Offset = 60A0h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.26 PCIE_CORE_VFm_I_MSI_PENDING_BITS Register (Offset = 60A4h + formula) [reset = 0h]

PCIE_CORE_VFm_I_MSI_PENDING_BITS is shown in Figure 9-209 and described in Table 9-635.

Return to the [Summary Table](#).

This register contains the MSI pending interrupt bits, one for each of the interrupt levels. This field can be written from the local management APBbus.

Offset = 60A4h + (m * 1000h); where m = 0h to Fh

Table 9-634.
PCIE_CORE_VFm_I_MSI_PENDING_BITS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60A4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60A4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60A4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60A4h + formula

Figure 9-209. PCIE_CORE_VFm_I_MSI_PENDING_BITS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0															MP
R-0h															R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-635. PCIE_CORE_VFm_I_MSI_PENDING_BITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R0	R	0h	Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of this field also changes correspondingly
0	MP	R/W	0h	Pending bits for MSI interrupts. This register contains the MSI pending interrupt bits, one for each of the interrupt levels. This field can be written from the local management APBbus. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid pending bits. Please note that if the Multiple Message Capable field is changed from the local management APBbus, then the width of the MSI Pending Bits field also changes correspondingly

Table 9-636. Register Call Summary for PCIE_CORE_VFm_I_MSI_PENDING_BITS

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_MSI_PENDING_BITS Register \(Offset = 60A4h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.27 PCIE_CORE_VFm_RSVD_02A_02B Register (Offset = 60A8h + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_02A_02B is shown in [Figure 9-210](#) and described in [Table 9-638](#).

Return to the [Summary Table](#).

Reserved

Offset = 60A8h + (m * 1000h); where m = 0h to Fh

**Table 9-637. PCIE_CORE_VFm_RSVD_02A_02B
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60A8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60A8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60A8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60A8h + formula

Figure 9-210. PCIE_CORE_VFm_RSVD_02A_02B Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-638. PCIE_CORE_VFm_RSVD_02A_02B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-639. Register Call Summary for PCIE_CORE_VFm_RSVD_02A_02B

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_RSVD_02A_02B Register \(Offset = 60A8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.28 PCIE_CORE_VFm_I_MSIX_CTRL Register (Offset = 60B0h + formula) [reset = C011h]

PCIE_CORE_VFm_I_MSIX_CTRL is shown in Figure 9-211 and described in Table 9-641.

Return to the [Summary Table](#).

This register contains the MSI-X configuration bits, the Capability ID for MSI-X, and the pointer to the next PCI Capability structure.

Offset = 60B0h + (m * 1000h); where m = 0h to Fh

Table 9-640. PCIE_CORE_VFm_I_MSIX_CTRL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60B0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60B0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60B0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60B0h + formula

Figure 9-211. PCIE_CORE_VFm_I_MSIX_CTRL Register

31	30	29	28	27	26	25	24
MSIXE	FM		R0			MSIXTS	
R/W-0h	R/W-0h		R-0h			R/W-0h	
23	22	21	20	19	18	17	16
						MSIXTS	
						R/W-0h	
15	14	13	12	11	10	9	8
						CP	
						R-C0h	
7	6	5	4	3	2	1	0
						CID	
						R/W-11h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-641. PCIE_CORE_VFm_I_MSIX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSIXE	R/W	0h	Set by the configuration program to enable the MSI-X feature. This field can also be written from the local management bus.
30	FM	R/W	0h	This bit serves as a global mask to all the interrupt conditions associated with this Function. When this bit is set, the core will not send out MSI messages from this Function. This field can also be written from the local management bus.
29-27	R0	R	0h	Reserved
26-16	MSIXTS	R/W	0h	Specifies the size of the MSI-X Table, that is, the number of interrupt vectors defined for the Function. The programmed value is 1 minus the size of the table [that is, this field is set to 0 if the table size is 1.]. It can be re-written independently for each Function from the local management bus.

Table 9-641. PCIE_CORE_VFm_I_MSIX_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	CP	R	C0h	Contains a pointer to the next PCI Capability Structure. The value read from this read-only field is the corresponding pointer in the MSI-X Capability Structure of the Physical Function this VF is attached to.
7-0	CID	R/W	11h	Identifies that the capability structure is for MSI-X. This field is set by default to 11 hex. It can be rewritten independently for each Function from the local management bus.

Table 9-642. Register Call Summary for PCIE_CORE_VFm_I_MSIX_CTRL

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_MSIX_CTRL Register \(Offset = 60B0h + formula\) \[reset = C011h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.29 PCIE_CORE_VFm_I_MSIX_TBL_OFFSET Register (Offset = 60B4h + formula) [reset = 0h]

PCIE_CORE_VFm_I_MSIX_TBL_OFFSET is shown in Figure 9-212 and described in Table 9-644.

Return to the [Summary Table](#).

This register is used to specify the location of the MSI-X Table in memory. All of the 32 bits of this register can be re-written independently for each Virtual Function from the local management bus.

Offset = 60B4h + (m * 1000h); where m = 0h to Fh

Table 9-643.
PCIE_CORE_VFm_I_MSIX_TBL_OFFSET Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60B4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60B4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60B4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60B4h + formula

Figure 9-212. PCIE_CORE_VFm_I_MSIX_TBL_OFFSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO												BARI			
R/W-0h												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-644. PCIE_CORE_VFm_I_MSIX_TBL_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	TO	R/W	0h	Offset of the memory address where the MSI-X Table is located, relative to the selected BAR. The three least significant bits of the address are omitted, as the addresses are QWORD aligned.
2-0	BARI	R/W	0h	Identifies the BAR corresponding to the memory address range where the MSI-X Table is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5].

Table 9-645. Register Call Summary for PCIE_CORE_VFm_I_MSIX_TBL_OFFSET

PCIE_CORE_EP_VF Registers

- PCIE_CORE_VFm_I_MSIX_TBL_OFFSET Register (Offset = 60B4h + formula) [reset = 0h]: [0]
- PCIE_CORE_EP_VF Registers: [0] [1]

9.3.30 PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT Register (Offset = 60B8h + formula) [reset = 8h]

PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT is shown in Figure 9-213 and described in Table 9-647.

Return to the [Summary Table](#).

This register is used to specify the location of the MSI-X Pending Bit Array (PBA). The PBA is a structure in memory containing the pending interrupt bits. All the 32 bits of this register can be re-written independently for each Virtual Function from the local management bus.

Offset = 60B8h + (m * 1000h); where m = 0h to Fh

Table 9-646.
PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60B8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60B8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60B8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60B8h + formula

Figure 9-213. PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PO															
R/W-1h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO												BARI			
R/W-1h												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-647. PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	PO	R/W	1h	Offset of the memory address where the PBA is located, relative to the selected BAR. The three least significant bits of the address are omitted, as the addresses are QWORD aligned.
2-0	BARI	R/W	0h	Identifies the BAR corresponding to the memory address range where the PBA Structure is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register. Identifies the BAR corresponding to the memory address range where the PBA Structure is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register.

Table 9-648. Register Call Summary for PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_VFm_I_MSIX_PENDING_INTRPT Register \(Offset = 60B8h + formula\) \[reset = 8h\]: \[0\]](#)

9.3.31 PCIE_CORE_VFm_RSVD_02F Register (Offset = 60BCh + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_02F is shown in [Figure 9-214](#) and described in [Table 9-650](#).

Return to the [Summary Table](#).

Reserved

Offset = 60BCh + (m * 1000h); where m = 0h to Fh

**Table 9-649. PCIE_CORE_VFm_RSVD_02F
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60BCh + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60BCh + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60BCh + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60BCh + formula

Figure 9-214. PCIE_CORE_VFm_RSVD_02F Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-650. PCIE_CORE_VFm_RSVD_02F Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-651. Register Call Summary for PCIE_CORE_VFm_RSVD_02F

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_RSVD_02F Register \(Offset = 60BCh + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.32 PCIE_CORE_VFm_I_PCIE_CAP_LIST Register (Offset = 60C0h + formula) [reset = 00020010h]

PCIE_CORE_VFm_I_PCIE_CAP_LIST is shown in Figure 9-215 and described in Table 9-653.

Return to the [Summary Table](#).

This location identifies the PCI Express device type and its capabilities. It also contains the Capability ID for the PCI Express Structure and the pointer to the next capability structure.

Offset = 60C0h + (m * 1000h); where m = 0h to Fh

Table 9-652. PCIE_CORE_VFm_I_PCIE_CAP_LIST Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60C0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60C0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60C0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60C0h + formula

Figure 9-215. PCIE_CORE_VFm_I_PCIE_CAP_LIST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0	TRS	IMN				SS		DT			CV				
R-0h	R-0h	R-0h				R-0h		R-0h			R-2h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCP								CID							
R-0h								R-10h							

LEGEND: R = Read Only; -n = value after reset

Table 9-653. PCIE_CORE_VFm_I_PCIE_CAP_LIST Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R0	R	0h	Reserved
30	TRS	R	0h	When set to 1, this bit indicates that the device supports routing of Trusted Configuration Requests. Not valid for Endpoints. Hardwired to 0.
29-25	IMN	R	0h	Identifies the MSI or MSI-X interrupt vector for the interrupt message generated corresponding to the status bits in the Slot Status Register, Root Status Register, or this capability structure. This field must be defined based on the chosen interrupt mode - MSI or MSI-X. This field is hardwired to 0.
24	SS	R	0h	Set to 1 when the link connected to a slot. Hardwired to 0.
23-20	DT	R	0h	Indicates the type of device implementing this Function. This field is hardwired to 0 in the EP mode.
19-16	CV	R	2h	Identifies the version number of the capability structure. This field is set to 2 by default to indicate that the Controller is compatible to PCI Express Base Specification Revision 3.0.
15-8	NCP	R	0h	Points to the next PCI capability structure. Set to 0 because this is the last capability structure.

Table 9-653. PCIE_CORE_VFm_I_PCIE_CAP_LIST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CID	R	10h	Specifies Capability ID assigned by PCI SIG for this structure. This field is hardwired to 10 hex.

Table 9-654. Register Call Summary for PCIE_CORE_VFm_I_PCIE_CAP_LIST

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_PCIE_CAP_LIST Register \(Offset = 60C0h + formula\) \[reset = 00020010h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.33 PCIE_CORE_VFm_I_PCIE_DEV_CAP Register (Offset = 60C4h + formula) [reset = 10008101h]

PCIE_CORE_VFm_I_PCIE_DEV_CAP is shown in Figure 9-216 and described in Table 9-656.

Return to the [Summary Table](#).

This register advertises the capabilities of the PCI Express device encompassing this Function.

Offset = 60C4h + (m * 1000h); where m = 0h to Fh

Table 9-655. PCIE_CORE_VFm_I_PCIE_DEV_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60C4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60C4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60C4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60C4h + formula

Figure 9-216. PCIE_CORE_VFm_I_PCIE_DEV_CAP Register

31	30	29	28	27	26	25	24
R3			FLRC	CPLS		CSPLV	
R-0h			R-1h	R-0h		R-0h	
23	22	21	20	19	18	17	16
CSPLV						R2	
R-0h						R-0h	
15	14	13	12	11	10	9	8
RBER	R1			AL1SL			AL0SL
R-1h		R-0h			R-0h		R-4h
7	6	5	4	3	2	1	0
AL0SL		ETFS	PFS		MPS		
R-4h		R-0h	R-0h		R-1h		

LEGEND: R = Read Only; -n = value after reset

Table 9-656. PCIE_CORE_VFm_I_PCIE_DEV_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	R3	R	0h	Reserved
28	FLRC	R	1h	Set when device has Function-Level Reset capability. Hardwired to 1.
27-26	CPLS	R	0h	This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.
25-18	CSPLV	R	0h	This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.
17-16	R2	R	0h	Reserved
15	RBER	R	1h	This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.
14-12	R1	R	0h	Reserved

Table 9-656. PCIE_CORE_VFm_I_PCIE_DEV_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	AL1SL	R	0h	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L1 to L0. This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.
8-6	AL0SL	R	4h	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L0S to L0. This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.
5	ETFS	R	0h	Set when device allows the tag field to be extended from 5 to 8 bits. This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0.
4-3	PFS	R	0h	This field is used to extend the tag field by combining unused Function bits with the tag bits. This field is hardwired to 00 to disable this feature.
2-0	MPS	R	1h	Specifies maximum payload size supported by the device. This field reflects the setting of the corresponding field in the PCIe Device Capability Register of PF 0

Table 9-657. Register Call Summary for PCIE_CORE_VFm_I_PCIE_DEV_CAP

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_PCIE_DEV_CAP Register \(Offset = 60C4h + formula\) \[reset = 10008101h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.34 PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS Register (Offset = 60C8h + formula) [reset = 0h]

PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS is shown in Figure 9-217 and described in Table 9-659.

Return to the [Summary Table](#).

This register contains control and status bits associated with the device implementing this Function. All the read-write bits in this register can also be written from the local management bus. Likewise, bits designated as RW1C can also be cleared by writing a 1 from the local management bus.

Offset = 60C8h + (m * 1000h); where m = 0h to Fh

Table 9-658.
PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60C8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60C8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60C8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60C8h + formula

Figure 9-217. PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS Register

31	30	29	28	27	26	25	24
R4							
R-0h							
23	22	21	20	19	18	17	16
R4		TP	APD	URD	FED	NFER	CED
R-0h		R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
FLR	MRRS			EBS	EAP	EPF	ETFE
R/W-0h		R-0h	R-0h		R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
MPS			ERO	EURR	EFER	ENFER	ECER
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-659. PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R4	R	0h	Reserved
21	TP	R	0h	Indicates if any of the Non-Posted requests issued by the VF are still pending.
20	APD	R	0h	Reserved
19	URD	R/W1C	0h	Set to 1 by the core when it receives an unsupported request, regardless of whether its reporting is enabled or not.
18	FED	R/W1C	0h	Set to 1 by the core when it detects a fatal error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.
17	NFER	R/W1C	0h	Set to 1 by the core when it detects a non-fatal error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked.

Table 9-659. PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CED	R/W1C	0h	Set to 1 by the core when it detects a correctable error, regardless of whether error reporting is enabled or not, and regardless of whether the error is masked
15	FLR	R/W	0h	Writing a 1 into this bit position generated a Function-Level Reset for the selected VF. This bit reads as 0.
14-12	MRRS	R	0h	Reserved
11	EBS	R	0h	Reserved
10	EAP	R	0h	Reserved
9	EPF	R	0h	Reserved
8	ETFE	R	0h	Reserved
7-5	MPS	R	0h	Reserved
4	ERO	R	0h	Reserved
3	EURR	R	0h	Reserved
2	EFER	R	0h	Reserved
1	ENFER	R	0h	Reserved
0	ECER	R	0h	Reserved

Table 9-660. Register Call Summary for PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_PCIE_DEV_CTRL_STATUS Register \(Offset = 60C8h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.35 PCIE_CORE_VFm_I_LINK_CAP Register (Offset = 60CCh + formula) [reset = 0041AC24h]

PCIE_CORE_VFm_I_LINK_CAP is shown in Figure 9-218 and described in Table 9-662.

Return to the [Summary Table](#).

This register advertises the link-specific capabilities of the device incorporating the PCIe core. There are no writable bits at this location. A read to this address returns the Link Capability Register fields of Physical Function 0.

Offset = 60CCh + (m * 1000h); where m = 0h to Fh

Table 9-661. PCIE_CORE_VFm_I_LINK_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60CCh + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60CCh + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60CCh + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60CCh + formula

Figure 9-218. PCIE_CORE_VFm_I_LINK_CAP Register

31	30	29	28	27	26	25	24
PN							
R-0h							
23	22	21	20	19	18	17	16
R5	AOC	LBNC	DLLARC	SDERC	CPM	L1EL	
R-0h	R-1h	R-0h	R-0h	R-0h	R-0h	R-3h	
15	14	13	12	11	10	9	8
L1EL	L0SEL			ASPM		MLW	
R-3h	R-2h			R-3h		R-2h	
7	6	5	4	3	2	1	0
MLW				MLS			
R-2h				R-4h			

LEGEND: R = Read Only; -n = value after reset

Table 9-662. PCIE_CORE_VFm_I_LINK_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PN	R	0h	Specifies the port number assigned to the PCI Express link connected to this device.
23	R5	R	0h	Reserved
22	AOC	R	1h	Setting this bit indicates that the device supports the ASPM Optionality feature. It can be turned off by writing a 0 to this bit position through the local management bus.
21	LBNC	R	0h	A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. Reserved for Endpoint.
20	DLLARC	R	0h	Set to 1 if the device is capable of reporting that the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0, as this version of the core does not support the feature.

Table 9-662. PCIE_CORE_VFm_I_LINK_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	SDERC	R	0h	Indicates the capability of the device to report a Surprise Down error condition. This bit is hardwired to 0, as this version of the core does not support the feature.
18	CPM	R	0h	Indicates that the device supports removal of reference clocks. It is set by default to the value of the define in reg_defaults.h. It can be re-written independently for each function from the local management bus.
17-15	L1EL	R	3h	Specifies the exit latency from L1 state. This parameter is dependent on the Physical Layer implementation. It is set by default to the value define in reg_defaults.h. It can be re-written independently for each Function from the local management bus.
14-12	LOSEL	R	2h	Specifies the time required for the device to transition from LOS to L0. This parameter is dependent on the Physical Layer implementation. It is set by default to the value define in reg_defaults.h. It can be re-written independently for each Function from the local management bus.
11-10	ASPM	R	3h	Indicates the level of ASPM support provided by the device. This field can be re-written independently for each Function from the local management bus. When SRIS is enabled in local management register bit, L0s capability is not supported and is forced low.
9-4	MLW	R	2h	Indicates the maximum number of lanes supported by the device. This field is hardwired based on the setting of the LANE_COUNT_IN strap input.
3-0	MLS	R	4h	Indicates the maximum speed supported by the link. [2.5 GT/s, 5 GT/s, 8 GT/s, 16 GT/s per lane]. This field is hardwired to 0001 [2.5GT/s] when the strap input PCIE_GENERATION_SEL is set to 0, to 0010 [5 GT/s] when the strap is set to 1, and to 0011 [8 GT/s] when the strap input is set to 10, to 0100 [16 GT/s] when the strap input is set to 11.

Table 9-663. Register Call Summary for PCIE_CORE_VFm_I_LINK_CAP

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_LINK_CAP Register \(Offset = 60CCh + formula\) \[reset = 0041AC24h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.36 PCIE_CORE_VFm_RSVD_034_038 Register (Offset = 60D0h + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_034_038 is shown in [Figure 9-219](#) and described in [Table 9-665](#).

Return to the [Summary Table](#).

Reserved

Offset = 60D0h + (m * 1000h); where m = 0h to Fh

**Table 9-664. PCIE_CORE_VFm_RSVD_034_038
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60D0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60D0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60D0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60D0h + formula

Figure 9-219. PCIE_CORE_VFm_RSVD_034_038 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-665. PCIE_CORE_VFm_RSVD_034_038 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-666. Register Call Summary for PCIE_CORE_VFm_RSVD_034_038

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_RSVD_034_038 Register \(Offset = 60D0h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.37 PCIE_CORE_VFm_I_PCIE_DEV_CAP_2 Register (Offset = 60E4h + formula) [reset = 00710812h]

PCIE_CORE_VFm_I_PCIE_DEV_CAP_2 is shown in Figure 9-220 and described in Table 9-668.

Return to the [Summary Table](#).

This register is not implemented for Virtual Functions. A read to this address returns the Device Capabilities 2 Register fields of Physical Function 0.

Offset = 60E4h + (m * 1000h); where m = 0h to Fh

**Table 9-667. PCIE_CORE_VFm_I_PCIE_DEV_CAP_2
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60E4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60E4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60E4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60E4h + formula

Figure 9-220. PCIE_CORE_VFm_I_PCIE_DEV_CAP_2 Register

31	30	29	28	27	26	25	24
R14							
R-0h							
23	22	21	20	19	18	17	16
MEEP	EEPS	EXFS	OPFFS	T10RS	T10CS		
R-1h	R-1h	R-1h	R-0h	R-0h	R-1h		
15	14	13	12	11	10	9	8
R13	TCS	LMS	R12	BAOCS128	BAOCS64		
R-0h	R-0h	R-1h	R-0h	R-0h	R-0h		
7	6	5	4	3	2	1	0
BAOCS32	OPRS	AFS	CTDS	CTR			
R-0h	R-0h	R-0h	R-1h	R-2h			

LEGEND: R = Read Only; -n = value after reset

Table 9-668. PCIE_CORE_VFm_I_PCIE_DEV_CAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R14	R	0h	Reserved
23-22	MEEP	R	1h	Indicates the maximum number of End-End TLP Prefixes supported by the Function. The supported values are: 01b 1 End-End TLP Prefix 10b 2 End-End TLP Prefixes
21	EEPS	R	1h	Indicates whether the Function supports End-End TLP Prefixes. A 1 in this field indicates that the Function supports receiving TLPs containing End-End TLP Prefixes.
20	EXFS	R	1h	Indicates that the Function supports the 3-bit definition of the Fmt field in the TLP header. This bit is hardwired to 1 for all Physical Functions.
19-18	OPFFS	R	0h	A 1 in this bit position indicates that the Function supports the Optimized Buffer Flush/Fill [OBFF] capability using message signaling.
17	T10RS	R	0h	If set function supports 1-bit requester capability otherwise, the function does not. This field reflects the value in SRIOV capability register

Table 9-668. PCIE_CORE_VFm_I_PCIE_DEV_CAP_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	T10CS	R	1h	If set function supports 1-bit completer capability otherwise, the function does not. This field is identical to the PF value.
15-14	R13	R	0h	Reserved
13-12	TCS	R	0h	Hardwired to 0.
11	LMS	R	1h	A 1 in this bit position indicates that the Function supports the Latency Tolerance Reporting [LTR] Capability. This bit is set to 1 by default, but can be turned off for all Physical Functions by writing into PF 0.
10	R12	R	0h	Reserved
9	BAOCS128	R	0h	Hardwired to 0.
8	BAOCS64	R	0h	Hardwired to 0.
7	BAOCS32	R	0h	Hardwired to 0.
6	OPRS	R	0h	Atomic OP routing supported.
5	AFS	R	0h	ARI forwarding supported.
4	CTDS	R	1h	A 1 in this field indicates that the associated Function supports the capability to turn off its Completion timeout. This bit is set to 1 by default, but can be re-written independently for each Function from the local management bus.
3-0	CTR	R	2h	Specifies the Completion Timeout values supported by the device. This field is set by default to 0010 [10 ms - 250 ms]. The actual timeout values are in two programmable local management registers, which allow the timeout settings of the two sub-ranges within Range B to be programmed independently.

Table 9-669. Register Call Summary for PCIE_CORE_VFm_I_PCIE_DEV_CAP_2

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_PCIE_DEV_CAP_2 Register \(Offset = 60E4h + formula\) \[reset = 00710812h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.38 PCIE_CORE_VFm_RSVD_03A_03F Register (Offset = 60E8h + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_03A_03F is shown in [Figure 9-221](#) and described in [Table 9-671](#).

Return to the [Summary Table](#).

Reserved

Offset = 60E8h + (m * 1000h); where m = 0h to Fh

**Table 9-670. PCIE_CORE_VFm_RSVD_03A_03F
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 60E8h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 60E8h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 60E8h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 60E8h + formula

Figure 9-221. PCIE_CORE_VFm_RSVD_03A_03F Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-671. PCIE_CORE_VFm_RSVD_03A_03F Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-672. Register Call Summary for PCIE_CORE_VFm_RSVD_03A_03F

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)
- [PCIE_CORE_VFm_RSVD_03A_03F Register \(Offset = 60E8h + formula\) \[reset = 0h\]: \[0\]](#)

9.3.39 PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR Register (Offset = 6100h + formula) [reset = 14020001h]

PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR is shown in Figure 9-222 and described in Table 9-674.

Return to the [Summary Table](#).

This is the first register in the PCI Express Advanced Error Reporting Capability Structure of a Virtual Function. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Offset = 6100h + (m * 1000h); where m = 0h to Fh

Table 9-673.
PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6100h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6100h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6100h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6100h + formula

Figure 9-222. PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R-140h												R-2h				R-1h															

LEGEND: R = Read Only; -n = value after reset

Table 9-674. PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R	140h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R	2h	Specifies the SIG assigned value for the version of the capability structure. This field reflects the setting of the corresponding field in the AER Enhanced Capability Header Register of PF 0.
15-0	PECID	R	1h	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express AER Extended Capability Structure [0001 hex].

Table 9-675. Register Call Summary for PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_AER_ENHANCED_CAP_HDR Register \(Offset = 6100h + formula\) \[reset = 14020001h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.40 PCIE_CORE_VFm_I_UNCORR_ERR_STATUS Register (Offset = 6104h + formula) [reset = 0h]

PCIE_CORE_VFm_I_UNCORR_ERR_STATUS is shown in [Figure 9-223](#) and described in [Table 9-677](#).

Return to the [Summary Table](#).

This register provides the status of the various uncorrectable errors detected by the PCI Express core. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Uncorrectable Error Mask Register have no effect on the status bits of this register. The setting of an uncorrectable error status bit causes the core to generate an ERR_FATAL message if the corresponding severity bit of the Uncorrectable Error Severity Register is 1. If the severity bit is 0, however, there are two separate ways the error could be processed: (i) In certain cases, the uncorrectable error is treated as an Advisory Non-Fatal Error. These cases are treated as similar to correctable errors, causing the core to generate an ERR_COR message instead of an ERR_NONFATAL message. For details on these special cases, refer to Section 6.2.3.2.4 of the PCI Express Base Specifications, Version 1.1. (ii) In all other cases, the core sends an ERR_NONFATAL message when the error is detected. In all cases, the sending of the error message can be suppressed by setting the bit corresponding to the error type in the Uncorrectable Error Mask Register. For errors that are not Function-specific, the error status bus is set in the registers belonging to all the Functions associated with the link, but only a single message is generated for the entire link. In the case of certain errors detected by the Transaction Layer, the associated TLP header is logged in the Shared VF Header Log Registers. All the RW1C bits can also be cleared from the local management bus by writing a 1 into the bit position.

Offset = 6104h + (m * 1000h); where m = 0h to Fh

Table 9-676.
PCIE_CORE_VFm_I_UNCORR_ERR_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6104h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6104h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6104h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6104h + formula

Figure 9-223. PCIE_CORE_VFm_I_UNCORR_ERR_STATUS Register

31	30	29	28	27	26	25	24
R3							
R-0h							
23	22	21	20	19	18	17	16
R3	UNCORR_INT_ERR_STATUS	R2	URES	ECRC_ERR_STATUS	MALFORMED_TLP_STATUS	RCVR_OVERFLOW_STATUS	UCS
R-0h	R-0h	R-0h	R/W1C-0h	R-0h	R-0h	R-0h	R/W1C-0h
15	14	13	12	11	10	9	8
CAS	CTS	FCPES	PTS	R1			
R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R-0h			
7	6	5	4	3	2	1	0
R1			DLPER	R0			
R-0h			R-0h	R-0h			

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-677. PCIE_CORE_VFm_I_UNCORR_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	R3	R	0h	Reserved
22	UNCORR_INT_ERR_STATUS	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
21	R2	R	0h	Reserved
20	URES	R/W1C	0h	This bit is set when the core has received a request from the link that it does not support. This error is not Function-specific. This error is considered non-fatal by default. In the special case described in Sections 6.2.3.2.4.1 of the PCI Express Specifications, the error is reported by sending an ERR_COR message. In all other cases, the error is reported by sending an ERR_NONFATAL message. The header of the received request that caused the error is logged in the Shared VF Header Log Registers. STICKY.
19	ECRC_ERR_STATUS	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
18	MALFORMED_TLP_STATUS	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
17	RCVR_OVERFLOW_STATUS	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
16	UCS	R/W1C	0h	This bit is set when the core has received an unexpected Completion packet from the link. This error is not Function-specific. STICKY.
15	CAS	R/W1C	0h	This bit is set when the core has returned the Completer Abort [CA] status to a request received from the link. This error is Function-specific. The header of the received request that caused the error is logged in the Shared VF Header Log Registers. STICKY.
14	CTS	R/W1C	0h	This bit is set when the completion timer associated with an outstanding request times out. This error is Function-specific. This error is considered non-fatal by default. STICKY.
13	FCPES	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
12	PTS	R/W1C	0h	This bit is set when the core receives a poisoned TLP from the link, targeted at this VF. This error is Function-specific. This error is considered non-fatal by default. The error is reported by sending an ERR_NONFATAL message. The header of the received TLP with error is logged in the Shared VF Header Log Registers associated with the VF. STICKY.
11-5	R1	R	0h	Reserved
4	DLPER	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
3-0	R0	R	0h	Reserved

Table 9-678. Register Call Summary for PCIE_CORE_VFm_I_UNCORR_ERR_STATUS

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_UNCORR_ERR_STATUS](#) Register (Offset = 6104h + formula) [reset = 0h]: [0]
- [PCIE_CORE_EP_VF](#) Registers: [0] [1]

9.3.41 PCIE_CORE_VFm_I_UNCORR_ERR_MASK Register (Offset = 6108h + formula) [reset = 0h]

PCIE_CORE_VFm_I_UNCORR_ERR_MASK is shown in Figure 9-224 and described in Table 9-680.

Return to the [Summary Table](#).

This register is not implemented for Virtual Functions. The setting of the mask bits in the Uncorrectable Error Mask Register of the Physical Function apply to all associated VFs.

Offset = 6108h + (m * 1000h); where m = 0h to Fh

Table 9-679.
PCIE_CORE_VFm_I_UNCORR_ERR_MASK
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6108h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6108h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6108h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6108h + formula

Figure 9-224. PCIE_CORE_VFm_I_UNCORR_ERR_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-680. PCIE_CORE_VFm_I_UNCORR_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R4	R	0h	N/A

Table 9-681. Register Call Summary for PCIE_CORE_VFm_I_UNCORR_ERR_MASK

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_UNCORR_ERR_MASK Register \(Offset = 6108h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.42 PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY Register (Offset = 610Ch + formula) [reset = 0h]

PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY is shown in [Figure 9-225](#) and described in [Table 9-683](#).

Return to the [Summary Table](#).

This register is not implemented for Virtual Functions. The settings of the severity bits in the Uncorrectable Error Severity Register of the Physical Function apply to all associated VFs.

Offset = 610Ch + (m * 1000h); where m = 0h to Fh

Table 9-682.
PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 610Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 610Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 610Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 610Ch + formula

Figure 9-225. PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R8																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-683. PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R8	R	0h	N/A

Table 9-684. Register Call Summary for PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_UNCORR_ERR_SEVERITY Register \(Offset = 610Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.43 PCIE_CORE_VFm_I_CORR_ERR_STATUS Register (Offset = 6110h + formula) [reset = 0h]

PCIE_CORE_VFm_I_CORR_ERR_STATUS is shown in Figure 9-226 and described in Table 9-686.

Return to the [Summary Table](#).

This register provides the status of the various correctable errors detected by the PCI Express core. Software may clear any error bit by writing a 1 into the corresponding bit position. The states of the bits in the Correctable Error Mask Register have no effect on the status bits of this register. The setting of a correctable error status bit causes the core to generate an ERR_COR error message to the Root Complex if the error is not masked in the Correctable Error Mask Register. For errors that are not Function-specific, the error status bus is set in the registers belonging to all the Functions associated with the link, but only a single message is generated for the entire link. Header logging of received TLPs does not apply to correctable errors. All the RW1C bits can also be cleared from the local management bus by writing a 1 into the bit position.

Offset = 6110h + (m * 1000h); where m = 0h to Fh

Table 9-685.
PCIE_CORE_VFm_I_CORR_ERR_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6110h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6110h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6110h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6110h + formula

Figure 9-226. PCIE_CORE_VFm_I_CORR_ERR_STATUS Register

31	30	29	28	27	26	25	24
R14							
R-0h							
23	22	21	20	19	18	17	16
R14							
R-0h							
15	14	13	12	11	10	9	8
HLOS	CIES	ANFES	RTTS	R13		RNRS	
R/W1C-0h	R-0h	R/W1C-0h	R-0h	R-0h		R-0h	
7	6	5	4	3	2	1	0
BDS	BTPS	R12				RES	
R-0h	R-0h	R-0h				R-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-686. PCIE_CORE_VFm_I_CORR_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R14	R	0h	Reserved
15	HLOS	R/W1C	0h	This bit is set on a Header Log Register overflow, that is, when the header could not be logged in the Header Log Register because it is occupied by a previous header. As per SR-IOV specification, this bit is hardwired to 0 since the Header Log is Shared among VFs.
14	CIES	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.

Table 9-686. PCIE_CORE_VFm_I_CORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ANFES	R/W1C	0h	This bit is set when an uncorrectable error occurs, which is determined to belong to one of the special cases described in Section 6.2.3.2.4 of the PCI Express 2.0 Specifications. This causes the core to generate an ERR_COR message in place of an ERR_NONFATAL message. STICKY.
12	RTTS	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
11-9	R13	R	0h	Reserved
8	RNRS	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
7	BDS	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
6	BTPS	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
5-1	R12	R	0h	Reserved
0	RES	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.

Table 9-687. Register Call Summary for PCIE_CORE_VFm_I_CORR_ERR_STATUS

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_CORR_ERR_STATUS Register \(Offset = 6110h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.44 PCIE_CORE_VFm_I_CORR_ERR_MASK Register (Offset = 6114h + formula) [reset = 0h]

PCIE_CORE_VFm_I_CORR_ERR_MASK is shown in Figure 9-227 and described in Table 9-689.

Return to the [Summary Table](#).

The mask bits in this register control the reporting of correctable errors. For each error type in the Correctable Error Status Register, there is a corresponding bit in this register to mask its reporting. When a mask bit is set, the occurrence of the error is not reported (by asserting the CORRECTABLE_ERROR_OUT output).

Offset = 6114h + (m * 1000h); where m = 0h to Fh

Table 9-688.
PCIE_CORE_VFm_I_CORR_ERR_MASK Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6114h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6114h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6114h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6114h + formula

Figure 9-227. PCIE_CORE_VFm_I_CORR_ERR_MASK Register

31	30	29	28	27	26	25	24
R17							
R-0h							
23	22	21	20	19	18	17	16
R17							
R-0h							
15	14	13	12	11	10	9	8
HLOM	CIEM	ANFEM	RTTM	R16		RNRM	
R/W-0h	R-0h	R-0h	R-0h	R-0h		R-0h	
7	6	5	4	3	2	1	0
BDM	BTM	R15				REM	
R-0h	R-0h	R-0h				R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-689. PCIE_CORE_VFm_I_CORR_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R17	R	0h	N/A
15	HLOM	R/W	0h	This bit, when set, masks the generation of error messages in response to a Header Log register overflow. STICKY. Header logs are shared across Vfs hence this field is reserved. This field is reserved since Header log sharing is selected for this configuration.
14	CIEM	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
13	ANFEM	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
12	RTTM	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
11-9	R16	R	0h	Reserved
8	RNRM	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.

Table 9-689. PCIE_CORE_VFm_I_CORR_ERR_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	BDM	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
6	BTM	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.
5-1	R15	R	0h	Reserved
0	REM	R	0h	This bit is not implemented for Virtual Functions. Hardwired to 0.

Table 9-690. Register Call Summary for PCIE_CORE_VFm_I_CORR_ERR_MASK

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_CORR_ERR_MASK Register \(Offset = 6114h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.45 PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL Register (Offset = 6118h + formula) [reset = 0h]

PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL is shown in [Figure 9-228](#) and described in [Table 9-692](#).

Return to the [Summary Table](#).

This location contains a pointer to the first error that is reported in the Uncorrectable Error Status Register.

Offset = 6118h + (m * 1000h); where m = 0h to Fh

Table 9-691.
PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6118h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6118h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6118h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6118h + formula

Figure 9-228. PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL Register

31	30	29	28	27	26	25	24
R18							
R-0h							
23	22	21	20	19	18	17	16
R18							
R-0h							
15	14	13	12	11	10	9	8
R18					MHRE	MHRC	ECC
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
ECCAP	EEG	EGC	FER				
R-0h	R-0h	R-0h	R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 9-692. PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	R18	R	0h	Reserved
10	MHRE	R	0h	Setting this bit enables the Function to log multiple error headers in its Header Log Registers. It is hardwired to 0
9	MHRC	R	0h	This bit is set when the Function has the capability to log more than one error header in its Header Log Registers. It is hardwired to 0.
8	ECC	R	0h	Setting this bit enables ECRC checking on the receive side of the core. This bit is hardwired to 0. The setting of the corresponding bit in the Advanced Error Capabilities and Control Register of PF 0 applies to all Virtual Functions.

Table 9-692. PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ECCAP	R	0h	This read-only bit indicates to the software that the device is capable of checking ECRC in packets received from the link. This bit is hardwired to 0. This setting of the corresponding bit in the Advanced Error Capabilities and Control Register of PF 0 applies to all Virtual Functions.
6	EEG	R	0h	Enables the ECRC generation on the transmit side of the core. This bit is hardwired to 0. The setting of the corresponding bit in the Advanced Error Capabilities and Control Register of PF 0 applies to all Virtual Functions.
5	EGC	R	0h	This read-only bit indicates to the software that the device is capable of generating ECRC in packets transmitted on the link. This bit is hardwired to 0. The setting of the corresponding bit in the Advanced Error Capabilities and Control Register of PF 0 applies to all Virtual Functions.
4-0	FER	R	0h	This is a 5-bit pointer to the bit position in the Uncorrectable Error Status Register corresponding to the error that was detected first. When there are multiple bits set in the Uncorrectable Error Status Register, this field informs the software which error was observed first. To prevent the field from being overwritten before software was able to read it, this field is not updated while the status bit pointed by it in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will update the First Error Pointer. Any uncorrectable error type, including the special cases where the error is reported using an ERR_COR message, will set the First Error Pointer [assuming the software has reset the error pointed by it in the Uncorrectable Error Status Register]. STICKY.

Table 9-693. Register Call Summary for PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_ADVCD_ERR_CAP_CTRL Register \(Offset = 6118h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.46 PCIE_CORE_VFm_I_HDR_LOG_0 Register (Offset = 611Ch + formula) [reset = 0h]

PCIE_CORE_VFm_I_HDR_LOG_0 is shown in [Figure 9-229](#) and described in [Table 9-695](#).

Return to the [Summary Table](#).

This is the first of a set of four registers used to capture the header of a TLP received by the core from the link upon detection of an uncorrectable error.

The Controller implements Shared Header Log for VFs.

All Virtual Functions associated with the same PF share the same Header Log.

When multiple bits are set in the Uncorrectable Error Status Registers of the VFs, the captured header corresponds to the error that was detected first, that is, the error pointed by the First Error Pointer, of the associated VF.

To prevent the captured header from being over-written before the software is able to read it, this register is not updated while the status bit pointed by the First Error Pointer in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will also cause the Header Log Registers to be updated. The doublewords of the TLP header are stored in the Header Log Registers with their bytes transposed. That is the byte containing the Type/Format fields of the header is stored at bit positions 31:24 of the Header Log Register 0.

Offset = 611Ch + (m * 1000h); where m = 0h to Fh

Table 9-694. PCIE_CORE_VFm_I_HDR_LOG_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 611Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 611Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 611Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 611Ch + formula

Figure 9-229. PCIE_CORE_VFm_I_HDR_LOG_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD0																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-695. PCIE_CORE_VFm_I_HDR_LOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD0	R	0h	First DWORD of captured TLP header STICKY.

Table 9-696. Register Call Summary for PCIE_CORE_VFm_I_HDR_LOG_0

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_HDR_LOG_0 Register \(Offset = 611Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.47 PCIE_CORE_VFm_I_HDR_LOG_1 Register (Offset = 6120h + formula) [reset = 0h]

PCIE_CORE_VFm_I_HDR_LOG_1 is shown in [Figure 9-230](#) and described in [Table 9-698](#).

Return to the [Summary Table](#).

This location contains the second Dword of the captured header of a TLP received from the link. The bytes are stored in transposed order.

Offset = 6120h + (m * 1000h); where m = 0h to Fh

**Table 9-697. PCIE_CORE_VFm_I_HDR_LOG_1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6120h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6120h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6120h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6120h + formula

Figure 9-230. PCIE_CORE_VFm_I_HDR_LOG_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD1																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-698. PCIE_CORE_VFm_I_HDR_LOG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD1	R	0h	Second DWORD of captured TLP header STICKY.

Table 9-699. Register Call Summary for PCIE_CORE_VFm_I_HDR_LOG_1

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_HDR_LOG_1 Register \(Offset = 6120h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.48 PCIE_CORE_VFm_I_HDR_LOG_2 Register (Offset = 6124h + formula) [reset = 0h]

PCIE_CORE_VFm_I_HDR_LOG_2 is shown in [Figure 9-231](#) and described in [Table 9-701](#).

Return to the [Summary Table](#).

This location contains the third Dword of the captured header of a TLP received from the link. The bytes are stored in transposed order.

Offset = 6124h + (m * 1000h); where m = 0h to Fh

Table 9-700. PCIE_CORE_VFm_I_HDR_LOG_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6124h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6124h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6124h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6124h + formula

Figure 9-231. PCIE_CORE_VFm_I_HDR_LOG_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD2																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-701. PCIE_CORE_VFm_I_HDR_LOG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD2	R	0h	Third DWORD of captured TLP header STICKY.

Table 9-702. Register Call Summary for PCIE_CORE_VFm_I_HDR_LOG_2

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_HDR_LOG_2 Register \(Offset = 6124h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.49 PCIE_CORE_VFm_I_HDR_LOG_3 Register (Offset = 6128h + formula) [reset = 0h]

PCIE_CORE_VFm_I_HDR_LOG_3 is shown in [Figure 9-232](#) and described in [Table 9-704](#).

Return to the [Summary Table](#).

If the captured TLP header is 4 Dwords long, this location contains the last Dword of the captured header of a TLP received from the link. If the captured header is a 3-Dword header, this register is unused. The bytes of the Dword are stored in this register in transposed order.

Offset = 6128h + (m * 1000h); where m = 0h to Fh

**Table 9-703. PCIE_CORE_VFm_I_HDR_LOG_3
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6128h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6128h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6128h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6128h + formula

Figure 9-232. PCIE_CORE_VFm_I_HDR_LOG_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD3																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-704. PCIE_CORE_VFm_I_HDR_LOG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD3	R	0h	Fourth DWORD of captured TLP header STICKY.

Table 9-705. Register Call Summary for PCIE_CORE_VFm_I_HDR_LOG_3

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_HDR_LOG_3 Register \(Offset = 6128h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.50 PCIE_CORE_VFm_RSVD_04B_04D Register (Offset = 612Ch + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_04B_04D is shown in [Figure 9-233](#) and described in [Table 9-707](#).

Return to the [Summary Table](#).

Reserved

Offset = 612Ch + (m * 1000h); where m = 0h to Fh

**Table 9-706. PCIE_CORE_VFm_RSVD_04B_04D
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 612Ch + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 612Ch + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 612Ch + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 612Ch + formula

Figure 9-233. PCIE_CORE_VFm_RSVD_04B_04D Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-707. PCIE_CORE_VFm_RSVD_04B_04D Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-708. Register Call Summary for PCIE_CORE_VFm_RSVD_04B_04D

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_RSVD_04B_04D Register \(Offset = 612Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.51 PCIE_CORE_VFm_I_TLP_PRE_LOG_0 Register (Offset = 6138h + formula) [reset = 0h]

PCIE_CORE_VFm_I_TLP_PRE_LOG_0 is shown in [Figure 9-234](#) and described in [Table 9-710](#).

Return to the [Summary Table](#).

First TLP Prefix (if present) associated with the TLP whose header is in the Header Log Register.
The bytes are in transposed order.

Offset = 6138h + (m * 1000h); where m = 0h to Fh

**Table 9-709. PCIE_CORE_VFm_I_TLP_PRE_LOG_0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6138h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6138h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6138h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6138h + formula

Figure 9-234. PCIE_CORE_VFm_I_TLP_PRE_LOG_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD1																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-710. PCIE_CORE_VFm_I_TLP_PRE_LOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD1	R	0h	First TLP Prefix of captured TLP STICKY.

Table 9-711. Register Call Summary for PCIE_CORE_VFm_I_TLP_PRE_LOG_0

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_TLP_PRE_LOG_0 Register \(Offset = 6138h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.52 PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR Register (Offset = 6140h + formula) [reset = 5C01000Eh]

PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR is shown in Figure 9-235 and described in Table 9-713.

Return to the [Summary Table](#).

This register is used to enable the Alternate Routing ID interpretation. This register contains the PCI Express Extended Capability ID, the capability version, and the pointer to the next capability structure.

Offset = 6140h + (m * 1000h); where m = 0h to Fh

Table 9-712.
PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6140h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6140h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6140h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6140h + formula

Figure 9-235. PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PCCID															
R/W-5C0h												R-1h				R-Eh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-713. PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R/W	5C0h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R	1h	Specifies the SIG-assigned value for the version of the capability structure. This field is taken from the setting of the corresponding field in the ARI Extended Capability Header Register of PF 0.
15-0	PCCID	R	Eh	This field is hardwired to the Capability ID assigned by PCI-SIG to the ARI Extended Capability [000E hex].

Table 9-714. Register Call Summary for PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_ARI_EXT_CAP_HDR Register \(Offset = 6140h + formula\) \[reset = 5C01000Eh\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.53 PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL Register (Offset = 6144h + formula) [reset = 0h]

PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL is shown in [Figure 9-236](#) and described in [Table 9-716](#).

Return to the [Summary Table](#).

This location contains the ARI Capability Register and the ARI Control Register. All the fields in this register are hardwired to 0.

Offset = 6144h + (m * 1000h); where m = 0h to Fh

Table 9-715.
PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6144h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6144h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6144h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6144h + formula

Figure 9-236. PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R13																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-716. PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R13	R	0h	Reserved

Table 9-717. Register Call Summary for PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_I_ARI_CAP_AND_CTRL Register \(Offset = 6144h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.54 PCIE_CORE_VFm_RSVD_052_09C Register (Offset = 6148h + formula) [reset = 0h]

PCIE_CORE_VFm_RSVD_052_09C is shown in [Figure 9-237](#) and described in [Table 9-719](#).

Return to the [Summary Table](#).

Reserved

Offset = 6148h + (m * 1000h); where m = 0h to Fh

**Table 9-718. PCIE_CORE_VFm_RSVD_052_09C
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 6148h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 6148h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 6148h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 6148h + formula

Figure 9-237. PCIE_CORE_VFm_RSVD_052_09C Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-719. PCIE_CORE_VFm_RSVD_052_09C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

Table 9-720. Register Call Summary for PCIE_CORE_VFm_RSVD_052_09C

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_RSVD_052_09C Register \(Offset = 6148h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.3.55 PCIE_CORE_VFm_ATS_CAP_HEADER Register (Offset = 65C0h + formula) [reset = 0001000Fh]

PCIE_CORE_VFm_ATS_CAP_HEADER is shown in Figure 9-238 and described in Table 9-722.

Return to the [Summary Table](#).

This location contains the ATS Extended Capabilities Register, its Capability ID, Version, and a pointer to the next capability.

Offset = 65C0h + (m * 1000h); where m = 0h to Fh

Table 9-721. PCIE_CORE_VFm_ATS_CAP_HEADER Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 65C0h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 65C0h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 65C0h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 65C0h + formula

Figure 9-238. PCIE_CORE_VFm_ATS_CAP_HEADER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ATSNXTCAP												ATSCAPVER			
R/W-0h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATSCAPID															
R-Fh															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-722. PCIE_CORE_VFm_ATS_CAP_HEADER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	ATSNXTCAP	R/W	0h	Indicates offset to the next PCI Express capability structure.
19-16	ATSCAPVER	R/W	1h	Specifies the SIG assigned value for the version of the capability structure.
15-0	ATSCAPID	R	Fh	Indicates the ATS Extended Capability structure. This field must return a Capability ID of 000Fh indicating that this is an ATS Extended Capability structure.

Table 9-723. Register Call Summary for PCIE_CORE_VFm_ATS_CAP_HEADER

PCIE_CORE_EP_VF Registers

- PCIE_CORE_VFm_ATS_CAP_HEADER Register (Offset = 65C0h + formula) [reset = 0001000Fh]: [0]
- PCIE_CORE_EP_VF Registers: [0] [1]

9.3.56 PCIE_CORE_VFm_ATS_CAP_CONTROL Register (Offset = 65C4h + formula) [reset = X]

PCIE_CORE_VFm_ATS_CAP_CONTROL is shown in Figure 9-239 and described in Table 9-725.

Return to the [Summary Table](#).

ATS Capability and Control Register

Offset = 65C4h + (m * 1000h); where m = 0h to Fh

Table 9-724.
PCIE_CORE_VFm_ATS_CAP_CONTROL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 65C4h + formula
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 65C4h + formula
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 65C4h + formula
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 65C4h + formula

Figure 9-239. PCIE_CORE_VFm_ATS_CAP_CONTROL Register

31	30	29	28	27	26	25	24
ATSEN	R30						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R30				ATSSTU			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	ATSGIS	ATSPGALNREQ	ATSINVQD				
R/W-X	R/W-1h	R/W-1h	R/W-1h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-725. PCIE_CORE_VFm_ATS_CAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ATSEN	R/W	0h	When Set, the Function is enabled to cache translations. Default value is 0b.
30-21	R30	R	0h	Reserved
20-16	ATSSTU	R/W	0h	This value indicates to the Function the minimum number of 4096-byte blocks that is indicated in a Translation Completions or Invalidate Requests. This is a power of 2 multiplier and the number of blocks is 2STU. A value of 0 0000b indicates one block and a value of 1 1111b indicates 2 ³¹ blocks.
15-7	RESERVED	R/W	X	
6	ATSGIS	R/W	1h	If Set, the Function supports InvalidationRequests that have the Global Invalidate bit Set. If Clear, the Function ignores the Global Invalidate bit in all Invalidate Requests.
5	ATSPGALNREQ	R/W	1h	If Set, indicates the Untranslated Address is always aligned to a 4096 byte boundary.

Table 9-725. PCIE_CORE_VFm_ATS_CAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	ATSINVQD	R/W	1h	The number of Invalidate Requests that the Function can accept before putting backpressure on the upstream connection. If 0 0000b, the Function can accept 32 Invalidate Requests.

Table 9-726. Register Call Summary for PCIE_CORE_VFm_ATS_CAP_CONTROL

PCIE_CORE_EP_VF Registers

- [PCIE_CORE_VFm_ATS_CAP_CONTROL Register \(Offset = 65C4h + formula\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_EP_VF Registers: \[0\] \[1\]](#)

9.4 PCIE_CORE_LM Registers

Table 9-728 lists the PCIE_CORE_LM registers. All register offset addresses not listed in Table 9-728 should be considered as reserved locations and the register contents should not be modified.

PCIE core local management (LM) registers. The local management registers are used to configure various operational parameters associated with the core, and for a local processor to monitor its status. These registers are accessible only from the local management bus.

Table 9-727. PCIE_CORE_LM Instances

Instance	Base Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0000h

Table 9-728. PCIE_CORE_LM Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE1_CORE_DBN_CFG_PCIE_CORE Physical Address
00100000h	PCIE_CORE_LM_I_PL_CONFIG_0_REG		0D10 0000h	0D90 0000h
00100004h	PCIE_CORE_LM_I_PL_CONFIG_1_REG		0D10 0004h	0D90 0004h
00100008h	PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG		0D10 0008h	0D90 0008h
0010000Ch	PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG		0D10 000Ch	0D90 000Ch
00100010h	PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG		0D10 0010h	0D90 0010h
00100014h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG		0D10 0014h	0D90 0014h
00100018h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG		0D10 0018h	0D90 0018h
0010001Ch	PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG		0D10 001Ch	0D90 001Ch
00100020h	PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG		0D10 0020h	0D90 0020h
00100024h	PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG		0D10 0024h	0D90 0024h
00100028h	PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG		0D10 0028h	0D90 0028h
0010002Ch	PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG		0D10 002Ch	0D90 002Ch
00100030h	PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG		0D10 0030h	0D90 0030h
00100034h	PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG		0D10 0034h	0D90 0034h
00100038h	PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG		0D10 0038h	0D90 0038h
0010003Ch	PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG		0D10 003Ch	0D90 003Ch
00100040h	PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG		0D10 0040h	0D90 0040h
00100044h	PCIE_CORE_LM_I_VENDOR_ID_REG		0D10 0044h	0D90 0044h
00100048h	PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG		0D10 0048h	0D90 0048h
0010004Ch	PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG		0D10 004Ch	0D90 004Ch
00100050h	PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG		0D10 0050h	0D90 0050h
00100070h	PCIE_CORE_LM_I_MULTI_VC_CONROL_REG		0D10 0070h	0D90 0070h
00100074h	PCIE_CORE_LM_I_SRIS_CONTROL_REG		0D10 0074h	0D90 0074h
00100080h	PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1		0D10 0080h	0D90 0080h
00100084h	PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1		0D10 0084h	0D90 0084h
00100088h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC1		0D10 0088h	0D90 0088h
0010008Ch	PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC1		0D10 008Ch	0D90 008Ch
00100090h	PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2		0D10 0090h	0D90 0090h

Table 9-728. PCIE_CORE_LM Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
00100094h	PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2		0D10 0094h	0D90 0094h
00100098h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC2		0D10 0098h	0D90 0098h
0010009Ch	PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC2		0D10 009Ch	0D90 009Ch
001000A0h	PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3		0D10 00A0h	0D90 00A0h
001000A4h	PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3		0D10 00A4h	0D90 00A4h
001000A8h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC3		0D10 00A8h	0D90 00A8h
001000ACh	PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC3		0D10 00ACh	0D90 00ACh
001000F0h	PCIE_CORE_LM_I_FC_INIT_DELAY_REG		0D10 00F0h	0D90 00F0h
00100100h	PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG		0D10 0100h	0D90 0100h
00100104h	PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG		0D10 0104h	0D90 0104h
00100108h	PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG		0D10 0108h	0D90 0108h
0010010Ch	PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG		0D10 010Ch	0D90 010Ch
00100110h	PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG		0D10 0110h	0D90 0110h
00100114h	PCIE_CORE_LM_I_SHDW_UR_ERR_REG		0D10 0114h	0D90 0114h
00100140h	PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG		0D10 0140h	0D90 0140h
00100144h	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG		0D10 0144h	0D90 0144h
00100148h	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG		0D10 0148h	0D90 0148h
0010014Ch	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_REG		0D10 014Ch	0D90 014Ch
00100150h	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG		0D10 0150h	0D90 0150h
00100158h	PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TA G_REG		0D10 0158h	0D90 0158h
00100200h	PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG		0D10 0200h	0D90 0200h
00100204h	PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG		0D10 0204h	0D90 0204h
00100208h	PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG		0D10 0208h	0D90 0208h
0010020Ch	PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTE R		0D10 020Ch	0D90 020Ch
00100210h	PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG		0D10 0210h	0D90 0210h
00100214h	PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG		0D10 0214h	0D90 0214h
00100218h	PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG		0D10 0218h	0D90 0218h
0010021Ch	PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG		0D10 021Ch	0D90 021Ch
00100220h	PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG		0D10 0220h	0D90 0220h
00100224h	PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_ REG		0D10 0224h	0D90 0224h
00100228h	PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_RE G		0D10 0228h	0D90 0228h
0010022Ch	PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG		0D10 022Ch	0D90 022Ch
00100234h	PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG		0D10 0234h	0D90 0234h
00100238h	PCIE_CORE_LM_I_PHY_STATUS_1_REG		0D10 0238h	0D90 0238h
00100240h	PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG		0D10 0240h	0D90 0240h
00100244h	PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG		0D10 0244h	0D90 0244h
00100248h	PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG		0D10 0248h	0D90 0248h
0010024Ch	PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG		0D10 024Ch	0D90 024Ch
00100250h	PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG		0D10 0250h	0D90 0250h
00100254h	PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG		0D10 0254h	0D90 0254h
00100258h	PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG		0D10 0258h	0D90 0258h
0010025Ch	PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG		0D10 025Ch	0D90 025Ch

Table 9-728. PCIE_CORE_LM Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
00100260h	PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG		0D10 0260h	0D90 0260h
00100264h	PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG		0D10 0264h	0D90 0264h
00100268h	PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG		0D10 0268h	0D90 0268h
0010026Ch	PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG		0D10 026Ch	0D90 026Ch
00100280h	PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG		0D10 0280h	0D90 0280h
00100284h	PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG		0D10 0284h	0D90 0284h
00100288h	PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG		0D10 0288h	0D90 0288h
0010028Ch	PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG		0D10 028Ch	0D90 028Ch
00100290h	PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG		0D10 0290h	0D90 0290h
00100294h	PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG		0D10 0294h	0D90 0294h
00100298h	PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG		0D10 0298h	0D90 0298h
0010029Ch	PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG		0D10 029Ch	0D90 029Ch
001002A0h	PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG		0D10 02A0h	0D90 02A0h
001002A4h	PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG		0D10 02A4h	0D90 02A4h
001002A8h	PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG		0D10 02A8h	0D90 02A8h
001002ACh	PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG		0D10 02ACh	0D90 02ACh
001002C0h	PCIE_CORE_LM_I_PF_CONFIG_REG		0D10 02C0h	0D90 02C0h
00100300h	PCIE_CORE_LM_I_RC_BAR_CONFIG_REG		0D10 0300h	0D90 0300h
00100360h	PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG		0D10 0360h	0D90 0360h
00100364h	PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2 MS_REG		0D10 0364h	0D90 0364h
00100368h	PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG		0D10 0368h	0D90 0368h
00100374h	PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG		0D10 0374h	0D90 0374h
00100378h	PCIE_CORE_LM_I_PHY_CONFIG_REG3		0D10 0378h	0D90 0378h
0010037Ch	PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG		0D10 037Ch	0D90 037Ch
00100380h	PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_ REG_LANE0		0D10 0380h	0D90 0380h
00100384h	PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_ REG_LANE1		0D10 0384h	0D90 0384h
001003C0h	PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_ REG_LANE0		0D10 03C0h	0D90 03C0h
001003C4h	PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_ REG_LANE1		0D10 03C4h	0D90 03C4h
00100C80h	PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_AX I		0D10 0C80h	0D90 0C80h
00100C88h	PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTR OL0		0D10 0C88h	0D90 0C88h
00100C8Ch	PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTR OL1		0D10 0C8Ch	0D90 0C8Ch
00100C90h	PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTR OL2		0D10 0C90h	0D90 0C90h
00100C94h	PCIE_CORE_LM_TL_INTERNAL_CONTROL		0D10 0C94h	0D90 0C94h
00100C98h	PCIE_CORE_LM_I_DTI_ATS_STATUS		0D10 0C98h	0D90 0C98h
00100C9Ch	PCIE_CORE_LM_I_DTI_ATS_CTRL		0D10 0C9Ch	0D90 0C9Ch
00100CC0h	PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_ VC_SELECT_REG		0D10 0CC0h	0D90 0CC0h
00100CC4h	PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_ REG		0D10 0CC4h	0D90 0CC4h

Table 9-728. PCIE_CORE_LM Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
00100CD0h	PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG		0D10 0CD0h	0D90 0CD0h
00100CD4h	PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG		0D10 0CD4h	0D90 0CD4h
00100CD8h	PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_RE G		0D10 0CD8h	0D90 0CD8h
00100CDCh	PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_RE G		0D10 0CDCh	0D90 0CDCh
00100CE0h	PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_RE G		0D10 0CE0h	0D90 0CE0h
00100D00h	PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGIS TER		0D10 0D00h	0D90 0D00h
00100D04h	PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG		0D10 0D04h	0D90 0D04h
00100D10h	PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1		0D10 0D10h	0D90 0D10h
00100D14h	PCIE_CORE_LM_MSI_MASK_SET_STATUS_1		0D10 0D14h	0D90 0D14h
00100D18h	PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_ STATUS_1		0D10 0D18h	0D90 0D18h
00100D1Ch	PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATU S_1		0D10 0D1Ch	0D90 0D1Ch
00100DA0h	PCIE_CORE_LM_I_LD_CTRL		0D10 0DA0h	0D90 0DA0h
00100DA4h	PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL		0D10 0DA4h	0D90 0DA4h
00100DA8h	PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG		0D10 0DA8h	0D90 0DA8h
00100DACH	PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG		0D10 0DACH	0D90 0DACH
00100DB0h	PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_IND EX_REG		0D10 0DB0h	0D90 0DB0h
00100DB4h	PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_RE G		0D10 0DB4h	0D90 0DB4h
00100DB8h	PCIE_CORE_LM_I_PTM_CONTEXT_1_REG		0D10 0DB8h	0D90 0DB8h
00100DBCh	PCIE_CORE_LM_I_PTM_CONTEXT_2_REG		0D10 0DBCh	0D90 0DBCh
00100DC0h	PCIE_CORE_LM_I_PTM_CONTEXT_3_REG		0D10 0DC0h	0D90 0DC0h
00100DC4h	PCIE_CORE_LM_I_PTM_CONTEXT_4_REG		0D10 0DC4h	0D90 0DC4h
00100DC8h	PCIE_CORE_LM_I_PTM_CONTEXT_5_REG		0D10 0DC8h	0D90 0DC8h
00100DCCh	PCIE_CORE_LM_I_PTM_CONTEXT_6_REG		0D10 0DCCh	0D90 0DCCh
00100DD0h	PCIE_CORE_LM_I_PTM_CONTEXT_7_REG		0D10 0DD0h	0D90 0DD0h
00100DD4h	PCIE_CORE_LM_I_PTM_CONTEXT_8_REG		0D10 0DD4h	0D90 0DD4h
00100DD8h	PCIE_CORE_LM_I_PTM_CONTEXT_9_REG		0D10 0DD8h	0D90 0DD8h
00100DDCh	PCIE_CORE_LM_I_PTM_CONTEXT_10_REG		0D10 0DDCh	0D90 0DDCh
00100DE0h	PCIE_CORE_LM_I_PTM_CONTEXT_11_REG		0D10 0DE0h	0D90 0DE0h
00100DECh	PCIE_CORE_LM_I_ASF_INTRPT_STATUS		0D10 0DECh	0D90 0DECh
00100DF0h	PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS		0D10 0DF0h	0D90 0DF0h
00100DF4h	PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG		0D10 0DF4h	0D90 0DF4h
00100DF8h	PCIE_CORE_LM_I_ASF_INTRPT_TEST		0D10 0DF8h	0D90 0DF8h
00100DFCh	PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_S EL		0D10 0DFCh	0D90 0DFCh
00100E00h	PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STATUS		0D10 0E00h	0D90 0E00h
00100E04h	PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_STAT US		0D10 0E04h	0D90 0E04h
00100E08h	PCIE_CORE_LM_I_ASF_SRAM_FAULT_STATSTICS		0D10 0E08h	0D90 0E08h
00100E0Ch	PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL		0D10 0E0Ch	0D90 0E0Ch
00100E10h	PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK		0D10 0E10h	0D90 0E10h

Table 9-728. PCIE_CORE_LM Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE1_CORE_DB N_CFG_PCIE_CO RE Physical Address
00100E14h	PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS		0D10 0E14h	0D90 0E14h
00100E18h	PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK		0D10 0E18h	0D90 0E18h
00100E1Ch	PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG		0D10 0E1Ch	0D90 0E1Ch
00100E20h	PCIE_CORE_LM_DUAL_TL_CTRL		0D10 0E20h	0D90 0E20h
00100E40h	PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_VER_REG		0D10 0E40h	0D90 0E40h

Table 9-729. PCIE_CORE_LM Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
00100000h	PCIE_CORE_LM_I_PL_CONFIG_0_REG		0E10 0000h	0E90 0000h
00100004h	PCIE_CORE_LM_I_PL_CONFIG_1_REG		0E10 0004h	0E90 0004h
00100008h	PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG		0E10 0008h	0E90 0008h
0010000Ch	PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG		0E10 000Ch	0E90 000Ch
00100010h	PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG		0E10 0010h	0E90 0010h
00100014h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG		0E10 0014h	0E90 0014h
00100018h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG		0E10 0018h	0E90 0018h
0010001Ch	PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG		0E10 001Ch	0E90 001Ch
00100020h	PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG		0E10 0020h	0E90 0020h
00100024h	PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG		0E10 0024h	0E90 0024h
00100028h	PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG		0E10 0028h	0E90 0028h
0010002Ch	PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG		0E10 002Ch	0E90 002Ch
00100030h	PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG		0E10 0030h	0E90 0030h
00100034h	PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG		0E10 0034h	0E90 0034h
00100038h	PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG		0E10 0038h	0E90 0038h
0010003Ch	PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG		0E10 003Ch	0E90 003Ch
00100040h	PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG		0E10 0040h	0E90 0040h
00100044h	PCIE_CORE_LM_I_VENDOR_ID_REG		0E10 0044h	0E90 0044h
00100048h	PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG		0E10 0048h	0E90 0048h
0010004Ch	PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG		0E10 004Ch	0E90 004Ch
00100050h	PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG		0E10 0050h	0E90 0050h
00100070h	PCIE_CORE_LM_I_MULTI_VC_CONROL_REG		0E10 0070h	0E90 0070h
00100074h	PCIE_CORE_LM_I_SRIS_CONTROL_REG		0E10 0074h	0E90 0074h
00100080h	PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1		0E10 0080h	0E90 0080h
00100084h	PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1		0E10 0084h	0E90 0084h
00100088h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC1		0E10 0088h	0E90 0088h
0010008Ch	PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC1		0E10 008Ch	0E90 008Ch
00100090h	PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2		0E10 0090h	0E90 0090h
00100094h	PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2		0E10 0094h	0E90 0094h
00100098h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC2		0E10 0098h	0E90 0098h

Table 9-729. PCIE_CORE_LM Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
0010009Ch	PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC2		0E10 009Ch	0E90 009Ch
001000A0h	PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3		0E10 00A0h	0E90 00A0h
001000A4h	PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3		0E10 00A4h	0E90 00A4h
001000A8h	PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC3		0E10 00A8h	0E90 00A8h
001000ACh	PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC3		0E10 00ACh	0E90 00ACh
001000F0h	PCIE_CORE_LM_I_FC_INIT_DELAY_REG		0E10 00F0h	0E90 00F0h
00100100h	PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG		0E10 0100h	0E90 0100h
00100104h	PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG		0E10 0104h	0E90 0104h
00100108h	PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG		0E10 0108h	0E90 0108h
0010010Ch	PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG		0E10 010Ch	0E90 010Ch
00100110h	PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG		0E10 0110h	0E90 0110h
00100114h	PCIE_CORE_LM_I_SHDW_UR_ERR_REG		0E10 0114h	0E90 0114h
00100140h	PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG		0E10 0140h	0E90 0140h
00100144h	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG		0E10 0144h	0E90 0144h
00100148h	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG		0E10 0148h	0E90 0148h
0010014Ch	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_REG		0E10 014Ch	0E90 014Ch
00100150h	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG		0E10 0150h	0E90 0150h
00100158h	PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TA G_REG		0E10 0158h	0E90 0158h
00100200h	PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG		0E10 0200h	0E90 0200h
00100204h	PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG		0E10 0204h	0E90 0204h
00100208h	PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG		0E10 0208h	0E90 0208h
0010020Ch	PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTE R		0E10 020Ch	0E90 020Ch
00100210h	PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG		0E10 0210h	0E90 0210h
00100214h	PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG		0E10 0214h	0E90 0214h
00100218h	PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG		0E10 0218h	0E90 0218h
0010021Ch	PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG		0E10 021Ch	0E90 021Ch
00100220h	PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG		0E10 0220h	0E90 0220h
00100224h	PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_ REG		0E10 0224h	0E90 0224h
00100228h	PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_RE G		0E10 0228h	0E90 0228h
0010022Ch	PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG		0E10 022Ch	0E90 022Ch
00100234h	PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG		0E10 0234h	0E90 0234h
00100238h	PCIE_CORE_LM_I_PHY_STATUS_1_REG		0E10 0238h	0E90 0238h
00100240h	PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG		0E10 0240h	0E90 0240h
00100244h	PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG		0E10 0244h	0E90 0244h
00100248h	PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG		0E10 0248h	0E90 0248h
0010024Ch	PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG		0E10 024Ch	0E90 024Ch
00100250h	PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG		0E10 0250h	0E90 0250h
00100254h	PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG		0E10 0254h	0E90 0254h
00100258h	PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG		0E10 0258h	0E90 0258h
0010025Ch	PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG		0E10 025Ch	0E90 025Ch
00100260h	PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG		0E10 0260h	0E90 0260h
00100264h	PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG		0E10 0264h	0E90 0264h

Table 9-729. PCIE_CORE_LM Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
00100268h	PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG		0E10 0268h	0E90 0268h
0010026Ch	PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG		0E10 026Ch	0E90 026Ch
00100280h	PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG		0E10 0280h	0E90 0280h
00100284h	PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG		0E10 0284h	0E90 0284h
00100288h	PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG		0E10 0288h	0E90 0288h
0010028Ch	PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG		0E10 028Ch	0E90 028Ch
00100290h	PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG		0E10 0290h	0E90 0290h
00100294h	PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG		0E10 0294h	0E90 0294h
00100298h	PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG		0E10 0298h	0E90 0298h
0010029Ch	PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG		0E10 029Ch	0E90 029Ch
001002A0h	PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG		0E10 02A0h	0E90 02A0h
001002A4h	PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG		0E10 02A4h	0E90 02A4h
001002A8h	PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG		0E10 02A8h	0E90 02A8h
001002ACh	PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG		0E10 02ACh	0E90 02ACh
001002C0h	PCIE_CORE_LM_I_PF_CONFIG_REG		0E10 02C0h	0E90 02C0h
00100300h	PCIE_CORE_LM_I_RC_BAR_CONFIG_REG		0E10 0300h	0E90 0300h
00100360h	PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG		0E10 0360h	0E90 0360h
00100364h	PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2 MS_REG		0E10 0364h	0E90 0364h
00100368h	PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG		0E10 0368h	0E90 0368h
00100374h	PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG		0E10 0374h	0E90 0374h
00100378h	PCIE_CORE_LM_I_PHY_CONFIG_REG3		0E10 0378h	0E90 0378h
0010037Ch	PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG		0E10 037Ch	0E90 037Ch
00100380h	PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_ REG_LANE0		0E10 0380h	0E90 0380h
00100384h	PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_ REG_LANE1		0E10 0384h	0E90 0384h
001003C0h	PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_ REG_LANE0		0E10 03C0h	0E90 03C0h
001003C4h	PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_ REG_LANE1		0E10 03C4h	0E90 03C4h
00100C80h	PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_AX I		0E10 0C80h	0E90 0C80h
00100C88h	PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTR OL0		0E10 0C88h	0E90 0C88h
00100C8Ch	PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTR OL1		0E10 0C8Ch	0E90 0C8Ch
00100C90h	PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTR OL2		0E10 0C90h	0E90 0C90h
00100C94h	PCIE_CORE_LM_TL_INTERNAL_CONTROL		0E10 0C94h	0E90 0C94h
00100C98h	PCIE_CORE_LM_I_DTI_ATS_STATUS		0E10 0C98h	0E90 0C98h
00100C9Ch	PCIE_CORE_LM_I_DTI_ATS_CTRL		0E10 0C9Ch	0E90 0C9Ch
00100CC0h	PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_ VC_SELECT_REG		0E10 0CC0h	0E90 0CC0h
00100CC4h	PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_ REG		0E10 0CC4h	0E90 0CC4h
00100CD0h	PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG		0E10 0CD0h	0E90 0CD0h
00100CD4h	PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG		0E10 0CD4h	0E90 0CD4h

Table 9-729. PCIE_CORE_LM Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
00100CD8h	PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_REG		0E10 0CD8h	0E90 0CD8h
00100CDCh	PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_REG		0E10 0CDCh	0E90 0CDCh
00100CE0h	PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_REG		0E10 0CE0h	0E90 0CE0h
00100D00h	PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER		0E10 0D00h	0E90 0D00h
00100D04h	PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG		0E10 0D04h	0E90 0D04h
00100D10h	PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1		0E10 0D10h	0E90 0D10h
00100D14h	PCIE_CORE_LM_MSI_MASK_SET_STATUS_1		0E10 0D14h	0E90 0D14h
00100D18h	PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1		0E10 0D18h	0E90 0D18h
00100D1Ch	PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1		0E10 0D1Ch	0E90 0D1Ch
00100DA0h	PCIE_CORE_LM_I_LD_CTRL		0E10 0DA0h	0E90 0DA0h
00100DA4h	PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL		0E10 0DA4h	0E90 0DA4h
00100DA8h	PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG		0E10 0DA8h	0E90 0DA8h
00100DACH	PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG		0E10 0DACH	0E90 0DACH
00100DB0h	PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_INDEX_REG		0E10 0DB0h	0E90 0DB0h
00100DB4h	PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_REG		0E10 0DB4h	0E90 0DB4h
00100DB8h	PCIE_CORE_LM_I_PTM_CONTEXT_1_REG		0E10 0DB8h	0E90 0DB8h
00100DBCh	PCIE_CORE_LM_I_PTM_CONTEXT_2_REG		0E10 0DBCh	0E90 0DBCh
00100DC0h	PCIE_CORE_LM_I_PTM_CONTEXT_3_REG		0E10 0DC0h	0E90 0DC0h
00100DC4h	PCIE_CORE_LM_I_PTM_CONTEXT_4_REG		0E10 0DC4h	0E90 0DC4h
00100DC8h	PCIE_CORE_LM_I_PTM_CONTEXT_5_REG		0E10 0DC8h	0E90 0DC8h
00100DCCCh	PCIE_CORE_LM_I_PTM_CONTEXT_6_REG		0E10 0DCCCh	0E90 0DCCCh
00100DD0h	PCIE_CORE_LM_I_PTM_CONTEXT_7_REG		0E10 0DD0h	0E90 0DD0h
00100DD4h	PCIE_CORE_LM_I_PTM_CONTEXT_8_REG		0E10 0DD4h	0E90 0DD4h
00100DD8h	PCIE_CORE_LM_I_PTM_CONTEXT_9_REG		0E10 0DD8h	0E90 0DD8h
00100DDCh	PCIE_CORE_LM_I_PTM_CONTEXT_10_REG		0E10 0DDCh	0E90 0DDCh
00100DE0h	PCIE_CORE_LM_I_PTM_CONTEXT_11_REG		0E10 0DE0h	0E90 0DE0h
00100DECh	PCIE_CORE_LM_I_ASF_INTRPT_STATUS		0E10 0DECh	0E90 0DECh
00100DF0h	PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS		0E10 0DF0h	0E90 0DF0h
00100DF4h	PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG		0E10 0DF4h	0E90 0DF4h
00100DF8h	PCIE_CORE_LM_I_ASF_INTRPT_TEST		0E10 0DF8h	0E90 0DF8h
00100DFCh	PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_SEL		0E10 0DFCh	0E90 0DFCh
00100E00h	PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STATUS		0E10 0E00h	0E90 0E00h
00100E04h	PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_STATUS		0E10 0E04h	0E90 0E04h
00100E08h	PCIE_CORE_LM_I_ASF_SRAM_FAULT_STATISTICS		0E10 0E08h	0E90 0E08h
00100E0Ch	PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL		0E10 0E0Ch	0E90 0E0Ch
00100E10h	PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK		0E10 0E10h	0E90 0E10h
00100E14h	PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS		0E10 0E14h	0E90 0E14h
00100E18h	PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK		0E10 0E18h	0E90 0E18h

Table 9-729. PCIE_CORE_LM Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_DB N_CFG_PCIE_CO RE Physical Address	PCIE3_CORE_DB N_CFG_PCIE_CO RE Physical Address
00100E1Ch	PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_ REG		0E10 0E1Ch	0E90 0E1Ch
00100E20h	PCIE_CORE_LM_DUAL_TL_CTRL		0E10 0E20h	0E90 0E20h
00100E40h	PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_VER_ REG		0E10 0E40h	0E90 0E40h

9.4.1 PCIE_CORE_LM_I_PL_CONFIG_0_REG Register (Offset = 00100000h) [reset = 22h]

PCIE_CORE_LM_I_PL_CONFIG_0_REG is shown in Figure 9-240 and described in Table 9-731.

Return to the [Summary Table](#).

This register contains the configured parameters at the Physical Layer of the link, and status information from the Physical Layer.

Table 9-730. PCIE_CORE_LM_I_PL_CONFIG_0_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0000h

Figure 9-240. PCIE_CORE_LM_I_PL_CONFIG_0_REG Register

31	30	29	28	27	26	25	24
MLE	R0	LTSSM					
R/W-0h	R-0h	R-0h					
23	22	21	20	19	18	17	16
RLID							
R-0h							
15	14	13	12	11	10	9	8
RFC							
R-0h							
7	6	5	4	3	2	1	0
TSS	APER	LTD	NS		NLC		LS
R/W-0h	R/W-0h	R-1h	R-0h		R-1h		R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-731. PCIE_CORE_LM_I_PL_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MLE	R/W	0h	When the Controller is operating as a Root Port, setting this to 1 causes the LTSSM to initiate a loopback and become the loopback master. This bit is not used in the EndPoint Mode.
30	R0	R	0h	A 1 in this field indicates that the remote node advertised Linkwidth Upconfigure Capability in the training sequences in the Configuration.Complete state when the link came up. A 0 indicates that the remote node did not set the Link Upconfigure bit.
29-24	LTSSM	R	0h	Current state of the LTSSM. The encoding of the states is given in Appendix C.
23-16	RLID	R	0h	Link ID received from other side during link training.
15-8	RFC	R	0h	FTS count received from the other side during link training for use at the 2.5 GT/s link speed. The Controller transmits this many FTS sequences while exiting the LOS state, when operating at the 2.5 GT/s speed.
7	TSS	R/W	0h	This bit drives the PIPE_TX_SWING output of the Controller.

Table 9-731. PCIE_CORE_LM_I_PL_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	APER	R/W	0h	<p>This bit controls the reporting of Errors Detected by the PHY. The Errors Detected by the PHY include:-</p> <ul style="list-style-type: none"> - Received errors indicated on PIPE RxStatus interface, - 8.0 GT/s Invalid Sync Header received error, - 16.0 GT/s Invalid Sync Header received error, <p>If PHY Error Reporting bit is set to 0, the Controller will only report those errors that caused a TLP or DLLP to be dropped because of a Detected PHY Error. If PHY Error Reporting bit is set to 1, the Controller will report all Detected PHY Errors regardless of whether a TLP or DLLP was dropped.</p> <p>The following registers report PHY error in conjunction with this bit:</p> <ul style="list-style-type: none"> - Correctable Error Status Register, i_corr_err_status, bit-0, Receiver Error Status - Local Error and Status Register, PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER, bit-7, Phy Error <p>In addition to the Errors Detected by the PHY[PCS], the Controller detects the following Physical Layer Protocol Framing Errors:</p> <ul style="list-style-type: none"> - Framing Errors in the received DLLP and TLP - Ordered Set Block Received Without EDS - Data Block Received After EDS - Illegal Ordered Set Block Received After EDS - Ordered Set Block Received After Skip OS <p>Note: These Errors are always reported independent of the setting of this bit.</p>
5	LTD	R	1h	<p>The state of this bit indicates whether the Controller completed link training as an upstream port[EndPoint][=0] or a downstream port[Root Port][=1]. Default value depends on CORE_TYPE strap pin.</p>
4-3	NS	R	0h	<p>Current operating speed of link</p> <p>[00 = 2.5G, 01 = 5G, 10 = 8G, 11 = 16G].</p>
2-1	NLC	R	1h	<p>Lane count negotiated with other side during link training</p> <p>[00 = x1, 01 = x2, 10 = x4, 11 = x8].</p>
0	LS	R	0h	<p>Current state of link</p> <p>[1 = link training complete, 0 = link training not complete].</p>

Table 9-732. Register Call Summary for PCIE_CORE_LM_I_PL_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PL_CONFIG_0_REG](#) Register (Offset = 00100000h) [reset = 22h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.2 PCIE_CORE_LM_I_PL_CONFIG_1_REG Register (Offset = 00100004h) [reset = 40808000h]

PCIE_CORE_LM_I_PL_CONFIG_1_REG is shown in Figure 9-241 and described in Table 9-734.

Return to the [Summary Table](#).

This register contains additional configured parameters at the Physical Layer of the link, and command bits for various Physical Layer functions.

Table 9-733. PCIE_CORE_LM_I_PL_CONFIG_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0004h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0004h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0004h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0004h

Figure 9-241. PCIE_CORE_LM_I_PL_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFC3								TFC2								TFC1								TLI							
R/W-40h								R/W-80h								R/W-80h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-734. PCIE_CORE_LM_I_PL_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TFC3	R/W	40h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from LOS state.
23-16	TFC2	R/W	80h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from LOS state.
15-8	TFC1	R/W	80h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from LOS state.
7-0	TLI	R/W	0h	Link ID transmitted by the device in training sequences in the Root Port mode.

Table 9-735. Register Call Summary for PCIE_CORE_LM_I_PL_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PL_CONFIG_1_REG Register \(Offset = 00100004h\) \[reset = 40808000h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.3 PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG Register (Offset = 00100008h) [reset = 0h]

PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG is shown in Figure 9-242 and described in Table 9-737.

Return to the [Summary Table](#).

This register defines the replay timeout values used by the DL receive and transmit sides of the link. It can be read or written via the local management APB bus.

Table 9-736.
PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0008h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0008h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0008h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0008h

Figure 9-242. PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R25						RSART						R9						TSRT													
R-0h						R/W-0h						R-0h						R/W-0h													

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-737. PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	R25	R	0h	Reserved
24-16	RSART	R/W	0h	Additional receive side ACK-NAK timer timeout interval. This 9-bit value is added as a signed 2's complement number to the internal ACK-NAK timer timeout value computed by the Controller based on the PCI Express Specifications. This enables the user to make minor adjustments to the spec-defined replay timer settings. Its value is in multiples of [2 Symbol Times] At Gen1 adjustment range = [+2040 ns to -2048 ns]. At Gen2 adjustment range = [+1020 ns to -1024 ns]. At Gen3 adjustment range = [+510 ns to -512 ns].
15-9	R9	R	0h	Reserved
8-0	TSRT	R/W	0h	Additional transmit-side replay timer timeout interval. This 9-bit value is added as a signed 2's complement number to the internal replay timer timeout value computed by the Controller based on the PCI Express Specifications. This enables the user to make minor adjustments to the spec-defined replay timer settings. Its value is in multiples of [2 Symbol Times] At Gen1 adjustment range = [+2040 ns to -2048 ns]. At Gen2 adjustment range = [+1020 ns to -1024 ns]. At Gen3 adjustment range = [+510 ns to -512 ns].

Table 9-738. Register Call Summary for PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_DLL_TMR_CONFIG_REG Register \(Offset = 00100008h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.4 PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG Register (Offset = 0010000Ch) [reset = 02020080h]

PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG is shown in Figure 9-243 and described in Table 9-740.

Return to the [Summary Table](#).

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect.

The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values.

The default values are set to advertise the full size of the receive buffers.

If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 9-739.
PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 000Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 000Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 000Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 000Ch

Figure 9-243. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC								PPC											
R/W-20h												R/W-20h								R/W-80h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-740. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R/W	20h	Non-Posted payload credit limit advertised by the Controller for VC 0. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 0. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
19-12	PHC	R/W	20h	Posted header credit limit advertised by the Controller for VC 0. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 9-740. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	PPC	R/W	80h	<p>Posted payload credit limit advertised by the Controller for VC 0. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 0.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-741. Register Call Summary for PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG Register \(Offset = 0010000Ch\) \[reset = 02020080h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.5 PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG Register (Offset = 00100010h) [reset = 20h]

PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG is shown in Figure 9-244 and described in Table 9-743.

Return to the [Summary Table](#).

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect.

The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values.

The default values are set to advertise the full size of the receive buffers.

If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 9-742.
PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0010h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0010h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0010h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0010h

Figure 9-244. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R2				CPC								NPHCL											
R/W-0h								R-0h				R/W-0h								R/W-20h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-743. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 0 [in number of packets]. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23-20	R2	R	0h	Reserved

Table 9-743. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-8	CPC	R/W	0h	<p>Completion payload credit limit advertised by the Controller for VC 0.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 0.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
7-0	NPHCL	R/W	20h	<p>Non-Posted header credit limit advertised by the Controller for VC 0 [in number of packets].</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-744. Register Call Summary for PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG Register \(Offset = 00100010h\) \[reset = 20h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.6 PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG Register (Offset = 00100014h) [reset = 0h]

PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG is shown in Figure 9-245 and described in Table 9-746.

Return to the [Summary Table](#).

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 9-745.
PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0014h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0014h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0014h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0014h

Figure 9-245. PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC									PPC										
R-0h												R-0h									R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 9-746. PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 0. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
19-12	PHC	R	0h	Posted header credit limit received by the Controller for this link . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11-0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 0. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]

Table 9-747. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG Register \(Offset = 00100014h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.7 PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG Register (Offset = 00100018h) [reset = 0h]

PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG is shown in Figure 9-246 and described in Table 9-749.

Return to the [Summary Table](#).

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 9-748.
PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0018h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0018h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0018h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0018h

Figure 9-246. PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R3				CPC								NPHC											
R-0h								R-0h				R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 9-749. PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R	0h	Completion header credit limit received by the Controller for VC 0 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23-20	R3	R	0h	Reserved
19-8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 0. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
7-0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 0 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

Table 9-750. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG Register \(Offset = 00100018h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.8 PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register (Offset = 0010001Ch) [reset = 00040004h]

PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG is shown in Figure 9-247 and described in Table 9-752.

Return to the [Summary Table](#).

This register contains parameters that control how frequently the Controller sends a credit update to the opposite node.

Table 9-751.
PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 001Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 001Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 001Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 001Ch

Figure 9-247. PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MNUI																MPUI															
R/W-4h																R/W-4h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-752. PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MNUI	R/W	4h	<p>Minimum credit update interval for non-posted transactions. The Controller follows this minimum interval between issuing posted credit updates on the link. This is to limit the bandwidth use of credit updates.</p> <p>If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update.</p> <p>The value is in units of 16 ns.</p> <p>This field is re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h.</p> <p>The user may override this default value by writing into this register field.</p> <p>The value written will be lost on a change in the negotiated link width/speed.</p>

Table 9-752. PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	MPUI	R/W	4h	<p>Minimum credit update interval for posted transactions. The Controller follows this minimum interval between issuing posted credit updates on the link. This is to limit the bandwidth use of credit updates.</p> <p>If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update.</p> <p>The value is in units of 16 ns.</p> <p>This field is re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h.</p> <p>The user may override this default value by writing into this register field.</p> <p>The value written will be lost on a change in the negotiated link width/speed.</p>

Table 9-753. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register \(Offset = 0010001Ch\) \[reset = 00040004h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.9 PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register (Offset = 00100020h) [reset = 03AA0004h]

PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG is shown in Figure 9-248 and described in Table 9-755.

Return to the [Summary Table](#).

This register contains parameters that control how frequently the Controller sends a credit update to the opposite node.

Table 9-754.
PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0020h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0020h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0020h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0020h

Figure 9-248. PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MUI																CUI															
R/W-3AAh																R/W-4h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-755. PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MUI	R/W	3AAh	Maximum credit update interval for all transactions. If no new credit has become available since the last update, the Controller will repeat the last update after this interval. This is to recover from any losses of credit update packets. The value is in units of 16 ns. This field could be re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h. The user may override this default value by writing into this register field. The value written will be lost on a change in the negotiated link width/speed.
15-0	CUI	R/W	4h	Minimum credit update interval for Completion packets. The Controller follows this minimum interval between issuing completion credit updates on the link. This is to limit the bandwidth use of credit updates. If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update. The value is in units of 16 ns. This parameter is not used when the Completion credit is infinity.

**Table 9-756. Register Call Summary for
PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG**

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG](#) Register (Offset = 00100020h) [reset = 03AA0004h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.10 PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG Register (Offset = 00100024h) [reset = 177h]

PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG is shown in Figure 9-249 and described in Table 9-758.

Return to the [Summary Table](#).

This register defines the timeout value for transitioning to the L0S power state. If the transmit side has been idle for this interval, the Controller will transmit the idle sequence on the link and transition the state of the link to L0S .

Table 9-757.
PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0024h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0024h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0024h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0024h

Figure 9-249. PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4																LT															
R-0h																R/W-177h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-758. PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R4	R	0h	Reserved
15-0	LT	R/W	177h	Contains the timeout value [in units of 16 ns] for transitioning to the L0S power state. Setting this parameter to 0 permanently disables the transition to the L0S power state.

Table 9-759. Register Call Summary for PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_L0S_TIMEOUT_LIMIT_REG Register (Offset = 00100024h) [reset = 177h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.11 PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG Register (Offset = 00100028h) [reset = 0h]

PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG is shown in Figure 9-250 and described in Table 9-761.

Return to the [Summary Table](#).

This register contains the number of Transaction-Layer packets transmitted by the Controller on the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing any value to this register causes it to be reset to 0.

Table 9-760.
PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0028h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0028h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0028h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0028h

Figure 9-250. PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTC																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-761. PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TTC	R/W1C	0h	Count of TLPs transmitted

Table 9-762. Register Call Summary for PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSMIT_TLP_COUNT_REG Register \(Offset = 00100028h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.12 PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register (Offset = 0010002Ch) [reset = 0h]

PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG is shown in Figure 9-251 and described in Table 9-764.

Return to the [Summary Table](#).

This register contains the aggregate number of payload double-words transmitted in Transaction-Layer Packets by the Controller on the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing any value to this register causes it to be reset to 0.

Table 9-763.
PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 002Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 002Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 002Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 002Ch

Figure 9-251. PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTPBC																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-764. PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TTPBC	R/W1C	0h	Count of TLPs payload Dwords transmitted

Table 9-765. Register Call Summary for
PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register \(Offset = 0010002Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.13 PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG Register (Offset = 00100030h) [reset = 0h]

PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG is shown in Figure 9-252 and described in Table 9-767.

Return to the [Summary Table](#).

This register contains the number of Transaction-Layer packets received by the Controller from the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing any value to this register causes it to be reset to 0.

Table 9-766.
PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0030h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0030h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0030h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0030h

Figure 9-252. PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTC																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-767. PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RTC	R/W1C	0h	Count of TLPs received

Table 9-768. Register Call Summary for PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RECEIVE_TLP_COUNT_REG Register \(Offset = 00100030h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.14 PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register (Offset = 00100034h) [reset = 0h]

PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG is shown in Figure 9-253 and described in Table 9-770.

Return to the [Summary Table](#).

This register contains the aggregate number of payload double-words received in Transaction-Layer packets by the Controller from the link since the register was last reset. This counter saturates on reaching a count of all 1's. Writing any value to this register causes it to be reset to 0.

Table 9-769.
PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0034h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0034h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0034h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0034h

Figure 9-253. PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTPDC																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-770. PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RTPDC	R/W1C	0h	Count of TLP payload Dwords received

Table 9-771. Register Call Summary for PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register \(Offset = 00100034h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.15 PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG Register (Offset = 00100038h) [reset = 00BEBC20h]

PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG is shown in Figure 9-254 and described in Table 9-773.

Return to the [Summary Table](#).

This register contains the timeout value used to detect a completion timeout event for a request originated by the Controller from its master interface, when sub-range 1 is programmed in the Device Control 2 Register.

Table 9-772.
PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0038h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0038h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0038h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0038h

Figure 9-254. PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5								CTL																							
R-0h								R/W-00BEBC20h																							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-773. PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R5	R	0h	Reserved
23-0	CTL	R/W	00BEBC20h	Timeout limit for completion timers [in 4 ns cycles]. Default value is 50 ms in 4 ns cycles. Please note that there could be a variation of 0 to +8us on the programmed Completion Timeout.

Table 9-774. Register Call Summary for PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_0_REG Register \(Offset = 00100038h\) \[reset = 00BEBC20h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.16 PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG Register (Offset = 0010003Ch) [reset = 02FAF080h]

PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG is shown in Figure 9-255 and described in Table 9-776.

Return to the [Summary Table](#).

This register contains the timeout value used to detect a completion timeout event for a request originated by the Controller from its master interface, when sub-range 2 is programmed in the Device Control 2 Register.

Table 9-775.
PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 003Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 003Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 003Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 003Ch

Figure 9-255. PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R6				CTL																											
R-0h				R/W-02FAF080h																											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-776. PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	R6	R	0h	Reserved
27-0	CTL	R/W	02FAF080h	Timeout limit for completion timers [in 4 ns cycles]. Default value is 200ms in 4ns cycles. Please note that there could be a variation of 0 to +8us on the programmed Completion Timeout.

Table 9-777. Register Call Summary for PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG

PCIE_CORE_LM Registers	
•	PCIE_CORE_LM_I_COMPLN_TMOUT_LIM_1_REG Register (Offset = 0010003Ch) [reset = 02FAF080h]: [0]
•	PCIE_CORE_LM Registers: [0] [1]

9.4.17 PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG Register (Offset = 00100040h) [reset = 0h]

PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG is shown in Figure 9-256 and described in Table 9-779.

Return to the [Summary Table](#).

This register specifies the time the Controller will wait before it re-enters the L1 state if its link partner transitions the link to L0 while all the Functions of the Controller are in D3 power state. The Controller will change the power state of the link from L0 to L1 if no activity is detected both on the transmit and receive sides before this interval, while all Functions are in D3 state and the link is in L0. Setting this register to 0 disables re-entry to L1 state if the link partner returns the link to L0 from L1 when all the Functions of the Controller are in D3 state. This register controls only the re-entry to L1. The initial transition to L1 always occurs when all of the Functions of the Controller are set to the D3 state.

Table 9-778.
PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0040h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0040h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0040h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0040h

Figure 9-256. PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L1RD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-779. PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	L1RD	R/W	0h	Delay to re-enter L1 after no activity [in units of 16 ns].

Table 9-780. Register Call Summary for PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_L1_ST_REENTRY_DELAY_REG Register \(Offset = 00100040h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.18 PCIE_CORE_LM_I_VENDOR_ID_REG Register (Offset = 00100044h) [reset = 17CD17CDh]

PCIE_CORE_LM_I_VENDOR_ID_REG is shown in [Figure 9-257](#) and described in [Table 9-782](#).

Return to the [Summary Table](#).

This register contains the Vendor ID and Subsystem Vendor ID that the device advertises during its enumeration of the PCI configuration space.

Table 9-781. PCIE_CORE_LM_I_VENDOR_ID_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0044h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0044h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0044h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0044h

Figure 9-257. PCIE_CORE_LM_I_VENDOR_ID_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVID																VID															
R/W-17CDh																R/W-17CDh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-782. PCIE_CORE_LM_I_VENDOR_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SVID	R/W	17CDh	Subsystem Vendor ID
15-0	VID	R/W	17CDh	Vendor ID

Table 9-783. Register Call Summary for PCIE_CORE_LM_I_VENDOR_ID_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_VENDOR_ID_REG Register \(Offset = 00100044h\) \[reset = 17CD17CDh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.19 PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register (Offset = 00100048h) [reset = 2EEh]

PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG is shown in Figure 9-258 and described in Table 9-785.

Return to the [Summary Table](#).

This register defines the timeout value for transitioning to the L1 power state under Active State Power management. If the transmit side has been idle for this interval, the Controller will initiate a transition of its link to the L1 power state.

Table 9-784.
PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0048h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0048h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0048h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0048h

Figure 9-258. PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register

31	30	29	28	27	26	25	24
DISLNRXCHK	R7						
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
R7				L1T			
R-0h				R/W-2EEh			
15	14	13	12	11	10	9	8
L1T							
R/W-2EEh							
7	6	5	4	3	2	1	0
L1T							
R/W-2EEh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-785. PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISLNRXCHK	R/W	0h	This bit is used to configure the ASPM L1 Entry mechanism: 1: Link is checked for IDLE only on the TX to determine ASPM L1 Entry. ASPM L1 entry is initiated if no TLP is transmitted for the L1 timeout period. 0: Link is checked for IDLE both on the TX and RX to determine ASPM L1 Entry. ASPM L1 entry is initiated if no TLP is transmitted/received for the L1 timeout period.
30-20	R7	R	0h	Reserved
19-0	L1T	R/W	2EEh	Contains the timeout value[in units of 16 ns] for transitioning to the L1 power state. Setting it to 0 permanently disables the transition to the L1 power state.

Table 9-786. Register Call Summary for PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register (Offset = 00100048h) [reset = 2EEh]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.20 PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG Register (Offset = 0010004Ch) [reset = 64h]

PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG is shown in Figure 9-259 and described in Table 9-788.

Return to the [Summary Table](#).

Defines the time interval between the Controller receiving a PME_Turn_Off message from the link and generating an ack for it.

Table 9-787.
PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 004Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 004Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 004Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 004Ch

Figure 9-259. PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																PTOAd															
R-0h																R/W-64h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-788. PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R7	R	0h	Reserved
15-0	PTOAd	R/W	64h	Time in microseconds between the Controller receiving a PME_TurnOff message TLP and the Controller sending a PME_TO_Ack response to it. This field must be set to a non-zero value in order for the Controller to send a response. Setting this field to 0 suppresses the Controller's response to PME_TurnOff message, so that the client may transmit the PME_TO_Ack message through the master interface.

Table 9-789. Register Call Summary for PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PME_TURNOFF_ACK_DELAY_REG Register \(Offset = 0010004Ch\) \[reset = 64h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.21 PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG Register (Offset = 00100050h) [reset = 3h]

PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG is shown in Figure 9-260 and described in Table 9-791.

Return to the [Summary Table](#).

This register can be used to retrain the link to a different width, without bringing the link down.

This register can also be used to retrain the link to a different speed, without bringing the link down.

Table 9-790.
PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0050h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0050h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0050h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0050h

Figure 9-260. PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG Register

31	30	29	28	27	26	25	24
EPLSCL	R2				EPTLS		
R/W-0h	R-0h				R/W-0h		
23	22	21	20	19	18	17	16
R1						RL	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						TLM	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-791. PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EPLSCL	R/W	0h	Writing a 1 into this field results in the Controller re-training the link to change its speed. When setting this bit to 1, the software must also set the EP Target Link Speed field to indicate the speed that the EP desires to change on the link. The EP Controller will attempt to change the link to this speed. This bit is cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. Software must wait for the bit to be clear before setting it again to change the link speed.
30-26	R2	R	0h	Reserved

Table 9-791. PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-24	EPTLS	R/W	0h	This field contains the Link Speed that the EP intends to change to during the re-training. Client needs to ensure that this field is programmed to a speed which is lesser than or equal to the Target Link Speed field of PF0 Configuration Link Control 2 Register. Client also needs to ensure that this does not exceed PCIE_GENERATION_SEL strap input. Defined encodings of this field are: 00 - GEN1 01 - GEN2 10 - GEN3 11 - GEN4
23-17	R1	R	0h	Reserved
16	RL	R/W	0h	Writing a 1 into this field results in the Controller re-training the link to change its width. When setting this bit to 1, the software must also set the target lane-map field to indicate the lanes it desires to be part of the link. The Controller will attempt to form a link with this set of lanes. The link formed at the end of the retraining may include all of these lanes [if both nodes agree on them during re-training], or the largest subset that both sides were able to activate. This bit is cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. Software must wait for the bit to be clear before setting it again to change the link width.
15-2	R0	R	0h	Reserved
1-0	TLM	R/W	3h	This field contains the bitmap of the lanes to be included in forming the link during the re-training. 01 - Retrain to a x1 link 11 - Retrain to a x2 link If the target lane map includes lanes that were inactive when retraining is initiated, then both the Controller and its link partner must support the LinkWidth Upconfigure Capability to be able to activate those lanes. In RC Mode, the user can check if the remote node has this capability by reading the Remote Link Upconfigure Capability Status bit in Physical Layer Configuration Register 0 after the link first came up.

Table 9-792. Register Call Summary for PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_LINKWIDTH_CONTROL_REG Register \(Offset = 00100050h\) \[reset = 3h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.22 PCIE_CORE_LM_I_MULTI_VC_CONROL_REG Register (Offset = 00100070h) [reset = 2h]

PCIE_CORE_LM_I_MULTI_VC_CONROL_REG is shown in Figure 9-261 and described in Table 9-794.

Return to the [Summary Table](#).

This register contains control bits to control certain multi VC features

Table 9-793.
PCIE_CORE_LM_I_MULTI_VC_CONROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0070h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0070h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0070h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0070h

Figure 9-261. PCIE_CORE_LM_I_MULTI_VC_CONROL_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31			RES4	RES2		WAIT_4_ALL_VC_CC_RDY	DMAAM
R-0h			R-0h	R-0h		R/W-1h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-794. PCIE_CORE_LM_I_MULTI_VC_CONROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	R31	R	0h	Reserved
4	RES4	R	0h	Reserved
3-2	RES2	R	0h	Reserved
1	WAIT_4_ALL_VC_CC_RDY	R/W	1h	When this bit is set, the controller waits for credits to be available to be able to send atleast 1 max payload TLP in all enabled VCs. When this bit is not set, the controller waits for credits to be available to be able to send atleast 1 max payload TLP in any of the enabled VCs [PCI-SIG recommended].
0	DMAAM	R	0h	Reserved

Table 9-795. Register Call Summary for PCIE_CORE_LM_I_MULTI_VC_CONROL_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_MULTI_VC_CONROL_REG Register \(Offset = 00100070h\) \[reset = 2h\]: \[0\]](#)

9.4.23 PCIE_CORE_LM_I_SRIS_CONTROL_REG Register (Offset = 00100074h) [reset = 0h]

PCIE_CORE_LM_I_SRIS_CONTROL_REG is shown in Figure 9-262 and described in Table 9-797.

Return to the [Summary Table](#).

This register contains control bits to enable the SRIS operation in the PHY Layer

Table 9-796.
PCIE_CORE_LM_I_SRIS_CONTROL_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0074h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0074h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0074h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0074h

Figure 9-262. PCIE_CORE_LM_I_SRIS_CONTROL_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31							SRISE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-797. PCIE_CORE_LM_I_SRIS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R31	R	0h	Reserved
0	SRISE	R/W	0h	Setting this bit enables SRIS mode in the PHY layer. This bit should be changed before link training begins by holding the LINK_TRAINING_ENABLE input to 1'b0. When SRIS is disabled using this bit the Lower SKP OS Generation Supported Speeds Vector and Lower SKP OS Reception Supported Speeds Vector in the Link Capabilities Register 2 will be forced to ZERO. The default value of this register can be controlled using the SRIS_ENABLE strap input.

Table 9-798. Register Call Summary for PCIE_CORE_LM_I_SRIS_CONTROL_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_SRIS_CONTROL_REG Register (Offset = 00100074h) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.24 PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1 Register (Offset = 00100080h) [reset = 02020080h]

PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1 is shown in Figure 9-263 and described in Table 9-800.

Return to the [Summary Table](#).

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect.

The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values.

The default values are set to advertise the full size of the receive buffers.

If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 9-799.
PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0080h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0080h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0080h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0080h

Figure 9-263. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC									PPC										
R/W-20h												R/W-20h									R/W-80h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-800. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R/W	20h	<p>Non-Posted payload credit limit advertised by the Controller for VC 1.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 1.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-800. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-12	PHC	R/W	20h	<p>Posted header credit limit advertised by the Controller for VC 1. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 1.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
11-0	PPC	R/W	80h	<p>Posted payload credit limit advertised by the Controller for VC 1. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 1.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-801. Register Call Summary for PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC1 Register \(Offset = 00100080h\) \[reset = 02020080h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.25 PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1 Register (Offset = 00100084h) [reset = 20h]

PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1 is shown in Figure 9-264 and described in Table 9-803.

Return to the [Summary Table](#).

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect.

The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values.

The default values are set to advertise the full size of the receive buffers.

If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 9-802.
PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0084h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0084h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0084h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0084h

Figure 9-264. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R2				CPC								NPHCL											
R/W-0h								R-0h				R/W-0h								R/W-20h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-803. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 1 [in number of packets]. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 1. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23-20	R2	R	0h	Reserved

Table 9-803. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-8	CPC	R/W	0h	<p>Completion payload credit limit advertised by the Controller for VC 1.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 1.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
7-0	NPHCL	R/W	20h	<p>Non-Posted header credit limit advertised by the Controller for VC 1 [in number of packets].</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 1.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-804. Register Call Summary for PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC1 Register \(Offset = 00100084h\) \[reset = 20h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.26 PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC1 Register (Offset = 00100088h) [reset = 0h]

PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC1 is shown in Figure 9-265 and described in Table 9-806.

Return to the [Summary Table](#).

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 9-805.
PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC
1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0088h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0088h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0088h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0088h

Figure 9-265. PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC									PPC										
R-0h												R-0h									R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 9-806. PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 1. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
19-12	PHC	R	0h	Posted header credit limit received by the Controller for this link . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 1. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11-0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 1. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]

Table 9-807. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC1 Register \(Offset = 00100088h\) \[reset = 0h\]: \[0\]](#)

9.4.27 PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC1 Register (Offset = 0010008Ch) [reset = 0h]

PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC1 is shown in Figure 9-266 and described in Table 9-809.

Return to the [Summary Table](#).

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 9-808.
PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC
1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 008Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 008Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 008Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 008Ch

Figure 9-266. PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R3				CPC								NPHC											
R-0h								R-0h				R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 9-809. PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R	0h	Completion header credit limit received by the Controller for VC 1 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 1. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23-20	R3	R	0h	Reserved
19-8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 1 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 1. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
7-0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 1 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 1. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

Table 9-810. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC1 Register \(Offset = 0010008Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.28 PCIe_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2 Register (Offset = 00100090h) [reset = 02020080h]

PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2 is shown in Figure 9-267 and described in Table 9-812.

Return to the [Summary Table](#).

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect.

The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values.

The default values are set to advertise the full size of the receive buffers.

If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 9-811.
PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0090h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0090h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0090h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0090h

Figure 9-267. PCIe_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC										PPC									
R/W-20h												R/W-20h										R/W-80h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-812. PCIe_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R/W	20h	Non-Posted payload credit limit advertised by the Controller for VC 2. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 2. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.

Table 9-812. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-12	PHC	R/W	20h	<p>Posted header credit limit advertised by the Controller for VC 2. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 2.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
11-0	PPC	R/W	80h	<p>Posted payload credit limit advertised by the Controller for VC 2. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 2.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-813. Register Call Summary for PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC2 Register \(Offset = 00100090h\) \[reset = 02020080h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.29 PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2 Register (Offset = 00100094h) [reset = 20h]

PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2 is shown in Figure 9-268 and described in Table 9-815.

Return to the [Summary Table](#).

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect.

The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values.

The default values are set to advertise the full size of the receive buffers.

If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 9-814.
PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0094h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0094h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0094h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0094h

Figure 9-268. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R2				CPC								NPHCL											
R/W-0h								R-0h				R/W-0h								R/W-20h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-815. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 2 [in number of packets]. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 2. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23-20	R2	R	0h	Reserved

Table 9-815. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-8	CPC	R/W	0h	<p>Completion payload credit limit advertised by the Controller for VC 2 .</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 2.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
7-0	NPHCL	R/W	20h	<p>Non-Posted header credit limit advertised by the Controller for VC 2 [in number of packets].</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 2.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-816. Register Call Summary for PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC2 Register \(Offset = 00100094h\) \[reset = 20h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.30 PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC2 Register (Offset = 00100098h) [reset = 0h]

PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC2 is shown in Figure 9-269 and described in Table 9-818.

Return to the [Summary Table](#).

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 9-817.
PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC
2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0098h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0098h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0098h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0098h

Figure 9-269. PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC						PPC													
R-0h												R-0h						R-0h													

LEGEND: R = Read Only; -n = value after reset

Table 9-818. PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 2. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
19-12	PHC	R	0h	Posted header credit limit received by the Controller for this link . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 2. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11-0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 2. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]

Table 9-819. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC2

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC2 Register \(Offset = 00100098h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.31 PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC2 Register (Offset = 0010009Ch) [reset = 0h]

PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC2 is shown in Figure 9-270 and described in Table 9-821.

Return to the [Summary Table](#).

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 9-820.
PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC
2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 009Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 009Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 009Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 009Ch

Figure 9-270. PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R3				CPC								NPHC											
R-0h								R-0h				R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 9-821. PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R	0h	Completion header credit limit received by the Controller for VC 2 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 2. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23-20	R3	R	0h	Reserved
19-8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 2 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 2. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
7-0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 2 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 2. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

Table 9-822. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC2

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC2 Register \(Offset = 0010009Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.32 PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3 Register (Offset = 001000A0h) [reset = 02020080h]

PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3 is shown in Figure 9-271 and described in Table 9-824.

Return to the [Summary Table](#).

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect.

The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values.

The default values are set to advertise the full size of the receive buffers.

If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 9-823.
PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00A0h

Figure 9-271. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC									PPC										
R/W-20h												R/W-20h									R/W-80h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-824. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R/W	20h	<p>Non-Posted payload credit limit advertised by the Controller for VC 3.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 3.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-824. PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-12	PHC	R/W	20h	<p>Posted header credit limit advertised by the Controller for VC 3. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 3.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
11-0	PPC	R/W	80h	<p>Posted payload credit limit advertised by the Controller for VC 3. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 3.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-825. Register Call Summary for PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RCV_CRED_LIM_0_REG_VC3 Register \(Offset = 001000A0h\) \[reset = 02020080h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.33 PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3 Register (Offset = 001000A4h) [reset = 20h]

PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3 is shown in Figure 9-272 and described in Table 9-827.

Return to the [Summary Table](#).

This register contains the initial credit limits advertised by the Controller during the DL initialization. If the fields of this register are modified, the link must be re-trained to re-initialize the DL for the modified settings to take effect.

The credit limit fields in this register can be programmed to any value lesser than or equal to the respective default values.

The default values are set to advertise the full size of the receive buffers.

If a value of 0x00 is programmed, it implies infinite credit.

Note: This may result in receiver overflow if received data is back pressured on the Client interface.

Table 9-826.
PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00A4h

Figure 9-272. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R2				CPC								NPHCL											
R/W-0h								R-0h				R/W-0h								R/W-20h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-827. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 3 [in number of packets]. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 3. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23-20	R2	R	0h	Reserved

Table 9-827. PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-8	CPC	R/W	0h	<p>Completion payload credit limit advertised by the Controller for VC 3 .</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 3.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
7-0	NPHCL	R/W	20h	<p>Non-Posted header credit limit advertised by the Controller for VC 3 [in number of packets].</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 3.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-828. Register Call Summary for PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RCV_CRED_LIM_1_REG_VC3 Register \(Offset = 001000A4h\) \[reset = 20h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.34 PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC3 Register (Offset = 001000A8h) [reset = 0h]

PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC3 is shown in Figure 9-273 and described in Table 9-830.

Return to the [Summary Table](#).

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 9-829.
PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC
3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00A8h

Figure 9-273. PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC						PPC													
R-0h												R-0h						R-0h													

LEGEND: R = Read Only; -n = value after reset

Table 9-830. PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 3. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
19-12	PHC	R	0h	Posted header credit limit received by the Controller for this link . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 3. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11-0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 3. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]

Table 9-831. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC3

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_LIM_0_REG_VC3 Register \(Offset = 001000A8h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.35 PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC3 Register (Offset = 001000ACh) [reset = 0h]

PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC3 is shown in Figure 9-274 and described in Table 9-833.

Return to the [Summary Table](#).

This register contains the initial credit limits received from the opposite node during the DL initialization. It is a read-only register.

Table 9-832.
PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC
3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00ACh

Figure 9-274. PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R3				CPC								NPHC											
R-0h								R-0h				R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 9-833. PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R	0h	Completion header credit limit received by the Controller for VC 3 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 3. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23-20	R3	R	0h	Reserved
19-8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 3 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 3. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
7-0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 3 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 3. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

Table 9-834. Register Call Summary for PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC3

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_TRANSM_CRED_LIM_1_REG_VC3 Register \(Offset = 001000ACh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.36 PCIE_CORE_LM_I_FC_INIT_DELAY_REG Register (Offset = 001000F0h) [reset = 64h]

PCIE_CORE_LM_I_FC_INIT_DELAY_REG is shown in [Figure 9-275](#) and described in [Table 9-836](#).

Return to the [Summary Table](#).

This register defines the delay value in between successive FC_INIT DLLPs for VCx.

Table 9-835.
PCIE_CORE_LM_I_FC_INIT_DELAY_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00F0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00F0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00F0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00F0h

Figure 9-275. PCIE_CORE_LM_I_FC_INIT_DELAY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4																FCINITDLY															
R-0h																R/W-64h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-836. PCIE_CORE_LM_I_FC_INIT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R4	R	0h	Reserved
15-0	FCINITDLY	R/W	64h	Delay between successive sets of P, NP, CPL FC_INIT DLLP transmissions for VCx.

Table 9-837. Register Call Summary for PCIE_CORE_LM_I_FC_INIT_DELAY_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_FC_INIT_DELAY_REG Register \(Offset = 001000F0h\) \[reset = 64h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.37 PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG Register (Offset = 00100100h) [reset = 0h]

PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG is shown in Figure 9-276 and described in Table 9-839.

Return to the [Summary Table](#).

N/A

Table 9-838.
PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0100h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0100h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0100h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0100h

Figure 9-276. PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHDW_HDR_LOG_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-839. PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHDW_HDR_LOG_0	R/W	0h	The value here will be reflected in the target function's header log register when f/w sets any bit in the the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [31:0] value of the TLP header.

Table 9-840. Register Call Summary for PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_SHDW_HDR_LOG_0_REG Register (Offset = 00100100h) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.38 PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG Register (Offset = 00100104h) [reset = 0h]

PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG is shown in [Figure 9-277](#) and described in [Table 9-842](#).

Return to the [Summary Table](#).

N/A

Table 9-841.
PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0104h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0104h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0104h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0104h

Figure 9-277. PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHDW_HDR_LOG_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-842. PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHDW_HDR_LOG_1	R/W	0h	The value here will be reflected in the target function's header log register when f/w sets any bit in the the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [63:32] value of the TLP header.

Table 9-843. Register Call Summary for PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_SHDW_HDR_LOG_1_REG Register \(Offset = 00100104h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.39 PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG Register (Offset = 00100108h) [reset = 0h]

PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG is shown in Figure 9-278 and described in Table 9-845.

Return to the [Summary Table](#).

N/A

Table 9-844.
PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0108h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0108h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0108h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0108h

Figure 9-278. PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHDW_HDR_LOG_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-845. PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHDW_HDR_LOG_2	R/W	0h	The value here will be reflected in the target function's header log register when f/w sets any bit in the the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [95:64] value of the TLP header.

Table 9-846. Register Call Summary for PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_SHDW_HDR_LOG_2_REG Register (Offset = 00100108h) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.40 PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG Register (Offset = 0010010Ch) [reset = 0h]

PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG is shown in Figure 9-279 and described in Table 9-848.

Return to the [Summary Table](#).

N/A

Table 9-847.
PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 010Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 010Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 010Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 010Ch

Figure 9-279. PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHDW_HDR_LOG_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-848. PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHDW_HDR_LOG_3	R/W	0h	The value here will be reflected in the target function's header log register when f/w sets any bit in the the shadow error register. If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set. This register holds [127:96] value of the TLP header.

Table 9-849. Register Call Summary for PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG

PCIE_CORE_LM Registers	
•	PCIE_CORE_LM Registers : [0] [1]
•	PCIE_CORE_LM_I_SHDW_HDR_LOG_3_REG Register (Offset = 0010010Ch) [reset = 0h] : [0]

9.4.41 PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG Register (Offset = 00100110h) [reset = 0h]

PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG is shown in [Figure 9-280](#) and described in [Table 9-851](#).

Return to the [Summary Table](#).

N/A

Table 9-850.
PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0110h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0110h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0110h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0110h

Figure 9-280. PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0								SHDW_FUNC_NUM							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-851. PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R0	R	0h	Reserved
7-0	SHDW_FUNC_NUM	R/W	0h	The value here will be the target function number when f/w sets any bit in the shadow error register.

Table 9-852. Register Call Summary for PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_SHDW_FUNC_NUM_REG Register \(Offset = 00100110h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.42 PCIE_CORE_LM_I_SHDW_UR_ERR_REG Register (Offset = 00100114h) [reset = 0h]

PCIE_CORE_LM_I_SHDW_UR_ERR_REG is shown in [Figure 9-281](#) and described in [Table 9-854](#).

Return to the [Summary Table](#).

Shadow register to create UR error via local f/w. Please make sure this register is written to last, after writing to all the header log and function number registers. A write to this register with any bits set, will internally create a single cycle pulse with the corresponding error type and the header log will reflect the value written in the shadow header log registers.

Table 9-853.
PCIE_CORE_LM_I_SHDW_UR_ERR_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0114h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0114h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0114h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0114h

Figure 9-281. PCIE_CORE_LM_I_SHDW_UR_ERR_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						NP_UR_ERR	P_UR_ERR
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-854. PCIE_CORE_LM_I_SHDW_UR_ERR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	Reserved
1	NP_UR_ERR	R/W	0h	If this bit is set, the corresponding non-posted UR error bits will be set in the AER and device status registers of the target function.
0	P_UR_ERR	R/W	0h	If this bit is set, the corresponding posted UR error bits will be set in the AER and device status registers of the target function.

Table 9-855. Register Call Summary for PCIE_CORE_LM_I_SHDW_UR_ERR_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_SHDW_UR_ERR_REG Register \(Offset = 00100114h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.43 PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG Register (Offset = 00100140h) [reset = 19h]

PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG is shown in Figure 9-282 and described in Table 9-857.

Return to the [Summary Table](#).

This register should be programmed with the frequency of the PM_CLK input to the Controller.

The Controller supports the frequency range of 2MHz to 60MHz for PM_CLK.

The reset value reflects the PM_CLK frequency chosen during Controller configuration.

NOTE: PM_CLK will be timed at 60Mhz and the Controller SDC file will be generated accordingly.

If timing is to be closed at a different frequency, then the user needs to update the SDC accordingly.

Table 9-856.
PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0140h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0140h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0140h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0140h

Figure 9-282. PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																PMCLKFRQ															
R-0h																R/W-19h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-857. PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R0	R	0h	Reserved
7-0	PMCLKFRQ	R/W	19h	<p>This field specifies the PM_CLK Frequency selected. The encoding is described below:</p> <p>000000: Reserved</p> <p>000001: Reserved</p> <p>000010: PM_CLK is 2 MHz</p> <p>000011: PM_CLK is 3 MHz</p> <p>000100: PM_CLK is 4 MHz</p> <p>000101: PM_CLK is 5 MHz</p> <p>..</p> <p>111010: PM_CLK is 58 MHz</p> <p>111011: PM_CLK is 59 MHz</p> <p>111100: PM_CLK is 60 MHz</p> <p>111101 : Reserved</p> <p>111110 : Reserved</p> <p>111111 : Reserved</p>

Table 9-858. Register Call Summary for PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_PM_CLK_FREQUENCY_REG Register (Offset = 00100140h) [reset = 19h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.44 PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG Register (Offset = 00100144h) [reset = 0h]

PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG is shown in Figure 9-283 and described in Table 9-860.

Return to the [Summary Table](#).

This register indicates the total number of DLLPs received by the Controller in GEN1.

This counter rolls over back to 0 after 4G DLLPs are received.

This register can be used for Debug purposes.

Table 9-859.
PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0144h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0144h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0144h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0144h

Figure 9-283. PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLPCNT1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-860. PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DLLPCNT1	R	0h	Reflects the total number of DLLPs received by the Controller at GEN1 speed.

Table 9-861. Register Call Summary for PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG

PCIE_CORE_LM Registers				
<ul style="list-style-type: none"> PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN1_REG Register (Offset = 00100144h) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1] 				

9.4.45 PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG Register (Offset = 00100148h) [reset = 0h]

PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG is shown in Figure 9-284 and described in Table 9-863.

Return to the [Summary Table](#).

This register indicates the total number of DLLPs received by the Controller in GEN2.

This counter rolls over back to 0 after 4G DLLPs are received.

This register can be used for Debug purposes.

Table 9-862.
PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0148h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0148h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0148h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0148h

Figure 9-284. PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLPCNT2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-863. PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DLLPCNT2	R	0h	Reflects the total number of DLLPs received by the Controller at GEN2 speed.

Table 9-864. Register Call Summary for PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG

PCIE_CORE_LM Registers	
•	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN2_REG Register (Offset = 00100148h) [reset = 0h]: [0]
•	PCIE_CORE_LM Registers: [0] [1]

9.4.46 PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_REG Register (Offset = 0010014Ch) [reset = 0h]

PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_REG is shown in Figure 9-285 and described in Table 9-866.

Return to the [Summary Table](#).

This register indicates the total number of DLLPs received by the Controller in GEN3.

This counter rolls over back to 0 after 4G DLLPs are received.

This register can be used for Debug purposes.

Table 9-865.
PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_R
EG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 014Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 014Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 014Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 014Ch

Figure 9-285. PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLPCNT3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-866. PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DLLPCNT3	R	0h	Reflects the total number of DLLPs received by the Controller at GEN3 speed.

Table 9-867. Register Call Summary for PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_REG

PCIE_CORE_LM Registers				
<ul style="list-style-type: none"> PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN3_REG Register (Offset = 0010014Ch) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1] 				

9.4.47 PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG Register (Offset = 00100150h) [reset = 0h]

PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG is shown in Figure 9-286 and described in Table 9-869.

Return to the [Summary Table](#).

This register indicates the total number of DLLPs received by the Controller in GEN4.

This counter rolls over back to 0 after 4G DLLPs are received.

This register can be used for Debug purposes.

Table 9-868.
PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0150h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0150h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0150h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0150h

Figure 9-286. PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLPCNT4																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-869. PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DLLPCNT4	R	0h	Reflects the total number of DLLPs received by the Controller at GEN4 speed.

Table 9-870. Register Call Summary for PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG

PCIE_CORE_LM Registers	
•	PCIE_CORE_LM_I_DEBUG_DLLP_COUNT_GEN4_REG Register (Offset = 00100150h) [reset = 0h]: [0]
•	PCIE_CORE_LM Registers: [0] [1]

9.4.48 PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register (Offset = 00100158h) [reset = X]

PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TAG_REG is shown in [Figure 9-287](#) and described in [Table 9-872](#).

Return to the [Summary Table](#).

The 8-bit Tag field of the Outbound Vendor Defined Messages, transmitted by the Controller, can be programmed in this register.

Table 9-871.
PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TAG_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0158h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0158h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0158h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0158h

Figure 9-287. PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VDMTAG							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-872. PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	VDMTAG	R/W	0h	The Controller will use the tag programed in this register for all Outbound Vendor Defined Messages.

Table 9-873. Register Call Summary for PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TAG_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register \(Offset = 00100158h\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.49 PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG Register (Offset = 00100200h) [reset = 0h]

PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG is shown in Figure 9-288 and described in Table 9-875.

Return to the [Summary Table](#).

This register contains a map of the active lanes used by the Controller to form the link during link training. It also contains a bit to indicate whether the Controller reversed the lane number on its lanes during link training.

Table 9-874.
PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0200h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0200h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0200h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0200h

Figure 9-288. PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R71															LRS
R-0h															R-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R70															NLM
R-0h															R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-875. PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	R71	R	0h	Reserved
16	LRS	R	0h	This bit set by the Controller at the end of link training if the LTSSM had to reverse the lane numbers to form the link.
15-2	R70	R	0h	Reserved
1-0	NLM	R	0h	Bit i of this field is set to 1 at the end of link training if Lane i is part of the PCIe link. The value of this field is valid only when the link is in L0 or L0s states.

Table 9-876. Register Call Summary for PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_NEGOTIATED_LANE_MAP_REG Register \(Offset = 00100200h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.50 PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG Register (Offset = 00100204h) [reset = 0h]

PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG is shown in Figure 9-289 and described in Table 9-878.

Return to the [Summary Table](#).

This register contains the FTS count values received from the link partner during link training for use at the 5 GT/s 8 GT/s and 16 GT/s speeds. These values determine the number of Fast Training Sequences transmitted by the Controller when it exits the L0s link power state.

Table 9-877.
PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0204h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0204h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0204h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0204h

Figure 9-289. PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R24								RFC16S								RFC8S								RFC5S							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-878. PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R24	R	0h	Reserved
23-16	RFC16S	R	0h	FTS count received from the other side during link training for use at the 16 GT/s link speed. The Controller transmits this many FTS sequences while exiting the L0S state, when operating at the 16 GT/s speed.
15-8	RFC8S	R	0h	FTS count received from the other side during link training for use at the 8 GT/s link speed. The Controller transmits this many FTS sequences while exiting the L0S state, when operating at the 8 GT/s speed.
7-0	RFC5S	R	0h	FTS count received from the other side during link training for use at the 5 GT/s link speed. The Controller transmits this many FTS sequences while exiting the L0S state, when operating at the 5 GT/s speed.

Table 9-879. Register Call Summary for PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RECEIVE_FTS_COUNT_REG Register \(Offset = 00100204h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.51 PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG Register (Offset = 00100208h) [reset = 80000000h]

PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG is shown in Figure 9-290 and described in Table 9-881.

Return to the [Summary Table](#).

N/A

Table 9-880.
PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0208h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0208h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0208h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0208h

Figure 9-290. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG Register

31	30	29	28	27	26	25	24
EFSRTCA	DOC	DFCUT	DEI	DGLUS	IEDPPE	ESPC	EFLT
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DLUC	DLRFE	DSHEC	DCIVMC	DIOAEFC	DOASFC	HPRSUPP	AWRPRI
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
FDS	DSSPLM	R1313	R1212	R1111	R1010	MSIVCMS	DIDBOC
R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
R77	R6				MS		
R/W-0h	R-0h				R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-881. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EFSRTCA	R/W	1h	Setting this bit to 0 causes all the enabled Functions to report an error when a Type-1 configuration access is received by the Controller, targeted at any Function. Setting it to 1 limits the error reporting to the type-0 Function whose number matches with the Function number specified in the request. If the Function number in the request refers to an unimplemented or disabled Function, all enabled Functions report the error regardless of the setting of this bit.
30	DOC	R/W	0h	Setting this bit to 1 disables the ordering check in the Controller between Completions and Posted requests received from the link.

Table 9-881. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	DFCUT	R/W	0h	When this bit is 0, the Controller will time out and re-train the link when no Flow Control Update DLLPs are received from the link within an interval of 128 us. Setting this bit to 1 disables this timeout. When the advertised receive credit of the link partner is infinity for the header and payload of all credit types, this timeout is always suppressed. The setting of this bit has no effect in this case. This bit should not be set during normal operation, but is useful for testing.
28	DEI	R/W	0h	Setting this bit to 1 disables the inferring of electrical idle in the L0 state. Electrical idle is inferred when no flow control updates and no SKP sequences are received within an interval of 128 us. This bit should not be set during normal operation, but is useful for testing.
27	DGLUS	R/W	0h	Setting this bit to 1 disables the update of the LFSRs in the Gen3 descramblers of the Controller, from the values received in SKP sequences. This bit should not be set during normal operation, but is useful for testing.
26	IEDPPE	R/W	0h	When set to 1, this bit inverts the parity bits generated by the Controller for end-to-end data protection. This will result in the inversion of parity bits for data payloads delivered through the HAL interface. This bit is to be used for diagnostics only, and should not be set during normal operation.
25	ESPC	R/W	0h	When this bit is set to 1, the Controller will capture the Slot Power Limit Value and Slot Power Limit Scale parameters from a Set_Slot_Power_Limit message received in the Device Capabilities Register. When this bit is 0, the capture is disabled. This bit is valid only when the Controller is configured as an EndPoint. It has no effect when the Controller is a Root Complex.
24	EFLT	R/W	0h	This bit is provided to shorten the link training time to facilitate fast simulation of the design, especially at the gate level. Enabling this bit has the following effects: 1. The 1 ms, 2 ms, 12 ms, 24 ms, 32 ms and 48 ms timeout intervals in the LTSSM are shortened by a factor of 500. 2. In the Polling.Active state of the LTSSM, only 16 training sequences are required to be transmitted [Instead of 1024] to make the transition to the Configuration state. This bit should not be set during normal operation of the Controller.

Table 9-881. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	DLUC	R/W	0h	<p>The user may set this bit to turn off the link upconfigure capability of the Controller.</p> <p>Setting this bit prevents the Controller from advertising the link upconfigure capability in training sequences transmitted in the Configuration.Complete state. In addition, setting this bit causes the Controller to put the unused lanes into Turn Off mode.</p> <p>When disable_link_upconfigure_capability==1:</p> <p>Controller drives PIPE_TX_ELEC_IDLE==1 AND PIPE_TX_COMPLIANCE==1 for the Unused upper lanes. The Unused upper lanes are put into Turn Off mode by the PHY as per PIPE specification.</p> <p>When disable_link_upconfigure_capability==0:</p> <p>Controller drives PIPE_TX_ELEC_IDLE==1 AND PIPE_TX_COMPLIANCE==0 for the Unused upper lanes. The Unused upper lanes are put into Electrical Idle by the PHY.</p>
22	DLRFE	R/W	0h	<p>When this bit is 1, the Controller will not transition its LTSSM into the Recovery state when it detects a Framing Error at 8 GT/s or 16 GT/s speed [as defined in Section 4.2.2.3.3 of the PCIe Base Specification 3.0].</p> <p>This bit must normally be set to 0 so that a Framing Error will cause the LTSSM to enter Recovery.</p> <p>The setting of this bit has no effect on the operation of the Controller at 2.5 and 5 GT/s speeds.</p>
21	DSHEC	R/W	0h	<p>When this bit is 0, the Controller will signal a framing error if it detects a sync header error in the received blocks at 8 GT/s or 16 GT/s speed [A 00 or 11 binary setting of the sync header on the received blocks in any lane constitutes a framing error].</p> <p>Setting this bit to 1 suppresses this error check.</p> <p>This bit should normally be set to 0, as the sync header check is mandatory in the PCIe 3.0 Specifications.</p>
20	DCIVMC	R/W	0h	<p>When this bit is 1, the Controller will not check for invalid message codes.</p> <p>This bit should normally be set to 0, as the invalid message code checking is mandatory in the PCIe 3.0 specifications.</p>
19	DIOAEFC	R/W	0h	<p>When this bit is 1, the Controller will not check for illegal OS after EDS as part of Gen3 Framing Error Checks.</p> <p>This bit should normally be set to 0, as this is a mandatory Gen3 Framing Error check in the PCIe 3.0 specifications.</p>
18	DOASFC	R/W	0h	<p>When this bit is 1, the Controller will not check for OS after SKIP OS as part of Gen3 Framing Error Checks.</p> <p>This bit should normally be set to 0, as this is a mandatory Gen3 Framing Error check in the PCIe 3.0 specifications.</p>
17	HPRSUPP	R/W	0h	<p>When this bit is 1, data path parity check is disabled on the TX side of the Controller.</p>
16	AWRPRI	R/W	0h	<p>When this bit is 1, the AXI bridge places a write request on the HAL Master interface in preference over a read request if both AXI write and AXI read requests are available to be asserted on the same clock cycle.</p>
15	FDS	R/W	0h	<p>Disable Scrambling/Descrambling in Gen1/Gen2.</p>
14	DSSPLM	R/W	0h	<p>Disable sending Set Slot Power Limit Message if the Slot Capabilitied register is configured</p>
13	R1313	R	0h	N/A

Table 9-881. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	R1212	R	0h	N/A
11	R1111	R/W	0h	When this bit is 1, Disable Client TX MUX Completion and PNP request arbitration,roundrobin priority logic added to prevent PNP requests from starving when completions are present
10	R1010	R	0h	Reserved
9	MSIVCMS	R/W	0h	Sets the mode of generating MSI_VECTOR_COUNT output for all functions. 0 - MSI_VECTOR_COUNT always outputs the configured value of MSI Multiple Message Enable [2:0] register. 1 - MSI_VECTOR_COUNT outputs the lesser of the MSI Multiple Message Enable [2:0] and MSI Multiple Message Capable [2:0] This mode can be used to handle any programming error form the Host software.
8	DIDBOC	R/W	0h	Setting this bit to 1 disables the ID Based Ordering check in the Controller between Completions and Posted requests received from the link.
7	R77	R/W	0h	This bit should be set to 0 for backward compatibility.
6-5	R6	R	0h	N/A
4-0	MS	R/W	0h	Bits 4:3 select the module and bits 2:0 select the group of signals within the module that are driven on the debug bus. The assignments of signals on the debug outputs of the Controller are given in Appendix B.

Table 9-882. Register Call Summary for PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_REG Register \(Offset = 00100208h\) \[reset = 80000000h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.52 PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER Register (Offset = 0010020Ch) [reset = 0h]

PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER is shown in Figure 9-291 and described in Table 9-884.

Return to the [Summary Table](#).

This register contains the status of the various events, errors and abnormal conditions in the Controller. Any of the status bits can be reset by writing a 1 into the bit position. This register does not capture any errors signaled by remote devices using PCIe error messages when the Controller is operating in the RC mode. Unless masked by the setting of the Local Interrupt Mask Register, the occurrence of any of these conditions causes the Controller to activate the LOCAL_INTERRUPT output.

Table 9-883.
PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGIS
TER Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 020Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 020Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 020Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 020Ch

Figure 9-291. PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER Register

31	30	29	28	27	26	25	24
REORDER_ER_UN	AXISLAVE_WFI FO_ER_UN	AXIMASTER_R FIFO_ER_UN	AXIMASTER_D IB_ER_UN	R27		MSIXMSKST	R24
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h		R/W1C-0h	R-0h
23	22	21	20	19	18	17	16
R24		HAWCD	R22	MMVC	UTC	EEPE	R13
R-0h		R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h
15	14	13	12	11	10	9	8
R13			R12	CT	FCE	UCR	MTR
R-0h			R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
PE	RTR	RT	CRFO	PRFO	RRPE	CRFPE	PRFPE
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-884. PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REORDER_ER_UN	R/W1C	0h	This indicates an uncorrectbale axi slave reorder ram parity/ecc error
30	AXISLAVE_WFI FO_ER_UN	R/W1C	0h	This indicates an uncorrectbale axi slave write fifo ram parity/ecc error
29	AXIMASTER_R FIFO_ER_UN	R/W1C	0h	This indicates an uncorrectbale axi master write fifo ram parity/ecc error
28	AXIMASTER_D IB_ER_UN	R/W1C	0h	This indicates an uncorrectbale axi slave write fifo ram parity/ecc error
27-26	R27	R	0h	Reserved

**Table 9-884. PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
25	MSIXMSKST	R/W1C	0h	This interrupt status bit is used when MSIX Function Mask Enhanced Interrupt Enable bit is set to 0 by the User. This status bit indicates that the MSIX Function Mask bit of any function, PF or VF, was programmed or configured by Local Firmware Or Host SW.
24-22	R24	R	0h	Reserved
21	HAWCD	R/W1C	0h	This interrupt status bit indicates that the Host toggled the Hardware Autonomous Width Change bit in the Link Control Register through a Config Write. Upon this interrupt, the Client firmware must read the Link Control Register to check the value set by Host in the Hardware Autonomous Width Change bit. The Host Software may disable autonomous width change by setting Hardware Autonomous Width Disable bit in the Link Control register. If disabled by the Host and if the Endpoint firmware had initiated an autonomous width downsizing prior to this interrupt, then the local Client firmware is responsible to upconfigure the Link to go to its full functional width by initiating the link_upconfigure_retrain_link within 1 ms of this interrupt.
20	R22	R	0h	Reserved
19	MMVC	R/W1C	0h	This status bit is set whenever the MSI mask register value in the MSI capability register changes value in ANY of the functions in the controller
18	UTC	R/W1C	0h	Unmapped TC error.
17	EEPE	R/W1C	0h	The Controller detected an End to End Parity Error
16-13	R13	R	0h	Reserved
12	R12	R	0h	Reserved
11	CT	R/W1C	0h	A request timed out waiting for completion.
10	FCE	R/W1C	0h	An error was observed in the flow control advertisements from the other side.
9	UCR	R/W1C	0h	Unexpected Completion received from the link.
8	MTR	R/W1C	0h	Malformed TLP received from the link.
7	PE	R/W1C	0h	Phy error detected on receive side. This bit is set when an error is detected in the receive side of the Physical Layer of the Controller [e.g. a bit error or coding violation]. This bit is set upon any of the following errors: [1] PHY reported 8B10B error, Disparity Error, Elastic Buffer Overflow Error, Underflow Error [2] GEN3 TLP, DLLP Framing Errors [3] OS Block Received Without EDS [4] Data Block Received After EDS [5] Illegal OS Block After EDS [6] OS Block Received After SKIP OS [7] OS Block Received After SDS [8] Sync Header Error [9] Loss of Gen3 Block Alignment This error is not Function-specific..
6	RTR	R/W1C	0h	Replay timer rolled over after 4 transmissions of the same TLP.
5	RT	R/W1C	0h	Replay timer timed out
4	CRFO	R/W1C	0h	Overflow occurred in the Completion Receive FIFO.
3	PRFO	R/W1C	0h	Overflow occurred in the PNP Receive FIFO.
2	RRPE	R/W1C	0h	Parity error detected while reading from Replay Buffer RAM.
1	CRFPE	R/W1C	0h	Parity error detected while reading from the Completion Receive FIFO RAM.

**Table 9-884. PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
0	PRFPE	R/W1C	0h	Parity error detected while reading from the PNP Receive FIFO RAM.

Table 9-885. Register Call Summary for PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_REGISTER Register \(Offset = 0010020Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM_I_PL_CONFIG_0_REG Register \(Offset = 00100000h\) \[reset = 22h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.53 PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG Register (Offset = 00100210h) [reset = 022E0FFFh]

PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG is shown in Figure 9-292 and described in Table 9-887.

Return to the [Summary Table](#).

This register contains a mask bit for each interrupting condition. Setting the bit to 1 prevents the corresponding condition in the Local Error Status Register from activating the LOCAL_INTERRUPT output.

Table 9-886.
PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0210h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0210h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0210h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0210h

Figure 9-292. PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG Register

31	30	29	28	27	26	25	24
REORDER_ER_UN	AXISLAVE_WFI FO_ER_UN	AXIMASTER_R FIFO_ER_UN	AXIMASTER_D IB_ER_UN	R27		MSIXMSK	R24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h
23	22	21	20	19	18	17	16
R24		HAWCD	R45	MMVC	UTC	EEPE	R13
R-0h		R/W-1h	R-0h	R/W-1h	R/W-1h	R/W-1h	R-0h
15	14	13	12	11	10	9	8
R13			R12	CT	FCE	UCR	MTR
R-0h			R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
PE	RTR	RT	CRFO	PRFO	RRPE	CRFPE	PRFPE
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-887. PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REORDER_ER_UN	R/W	0h	mask for uncorrectbale axi slave reorder ram parity/ecc error
30	AXISLAVE_WFI FO_ER_UN	R/W	0h	mask for uncorrectbale axi slave write fifo ram parity/ecc error
29	AXIMASTER_R FIFO_ER_UN	R/W	0h	mask for uncorrectbale axi master write fifo ram parity/ecc error
28	AXIMASTER_D IB_ER_UN	R/W	0h	mask for uncorrectbale axi slave write fifo ram parity/ecc error
27-26	R27	R	0h	Reserved
25	MSIXMSK	R/W	1h	This bit is used to mask interrupt that indicates that the MSIX Function Mask bit of any function, PF or VF, was programmed or configured by Local Firmware Or Host SW.
24-22	R24	R	0h	Reserved
21	HAWCD	R/W	1h	This bit is used to mask interrupt that indicates that the Host toggled the Hardware Autonomous Width Change in the Endpoint Link Control Register through a Config Write.
20	R45	R	0h	Reserved

Table 9-887. PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	MMVC	R/W	1h	MSI mask register value in the MSI capability register changes value in ANY of the functions in the controller
18	UTC	R/W	1h	Unmapped TC error
17	EEPE	R/W	1h	The Controller detected an End to End Parity Error
16-13	R13	R	0h	Reserved
12	R12	R	0h	Reserved
11	CT	R/W	1h	A request timed out waiting for completion.
10	FCE	R/W	1h	An error was observed in the flow control advertisements from the other side.
9	UCR	R/W	1h	Unexpected Completion received from the link.
8	MTR	R/W	1h	Malformed TLP received from the link.
7	PE	R/W	1h	Phy error detected on receive side.
6	RTR	R/W	1h	Replay timer rolled over after 4 transmissions of the same TLP.
5	RT	R/W	1h	Replay timer timed out
4	CRFO	R/W	1h	Overflow occurred in the Completion Receive FIFO.
3	PRFO	R/W	1h	Overflow occurred in the PNP Receive FIFO.
2	RRPE	R/W	1h	Parity error detected while reading from Replay Buffer RAM.
1	CRFPE	R/W	1h	Parity error detected while reading from the Completion Receive FIFO RAM.
0	PRFPE	R/W	1h	Parity error detected while reading from the PNP Receive FIFO RAM.

Table 9-888. Register Call Summary for PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_REG Register \(Offset = 00100210h\) \[reset = 022E0FFFh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.54 PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG Register (Offset = 00100214h) [reset = 0h]

PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG is shown in [Figure 9-293](#) and described in [Table 9-890](#).

Return to the [Summary Table](#).

This register contains the count of the number of TLPs received by the Controller with LCRC errors in them. This is a 16-bit saturating counter that can be reset to 0 by writing all 1's into it.

Table 9-889.
PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0214h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0214h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0214h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0214h

Figure 9-293. PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R11																LEC															
R-0h																R/W1C-0h															

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-890. PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R11	R	0h	Reserved
15-0	LEC	R/W1C	0h	Number of TLPs received with LCRC errors.

Table 9-891. Register Call Summary for PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_LCRC_ERR_COUNT_REG Register \(Offset = 00100214h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.55 PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG Register (Offset = 00100218h) [reset = 0h]

PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG is shown in Figure 9-294 and described in Table 9-893.

Return to the [Summary Table](#).

This register contains the count of the number of ECC errors detected and corrected during reads from the PCIe core external RAMs.

Table 9-892.
PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0218h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0218h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0218h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0218h

Figure 9-294. PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R12								RRCER								SFR CER								PFR CER							
R/W1C-0h								R/W1C-0h								R/W1C-0h								R/W1C-0h							

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-893. PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R12	R/W1C	0h	Number of correctable errors detected while reading from the TPH Steering Tag RAM. This is an 8-bit saturating counter that can be cleared by writing all 1s into it.
23-16	RRCER	R/W1C	0h	Number of correctable errors detected while reading from the Replay Buffer RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
15-8	SFR CER	R/W1C	0h	Number of correctable errors detected while reading from the SC FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
7-0	PFR CER	R/W1C	0h	Number of correctable errors detected while reading from the PNP FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.

Table 9-894. Register Call Summary for PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG Register \(Offset = 00100218h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.56 PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG Register (Offset = 0010021Ch) [reset = 0h]

PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG is shown in Figure 9-295 and described in Table 9-896.

Return to the [Summary Table](#).

This register contains the Snoop and No-Snoop Latency parameters used by the Controller when sending Latency Tolerance Reporting (LTR) Message. When the Controller is configured in the EndPoint mode, client software can program these fields to the desired latency settings and then set the Send LTR Message bit in the LTR Message Generation Control Register to send an LTR message to the Root Complex. The fields in this register should not be changed when the Send LTR Message bit in the LTR Message Generation Control Register is 1, which indicates that an LTR message is pending to be transmitted.

Table 9-895.
PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 021Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 021Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 021Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 021Ch

Figure 9-295. PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG Register

31	30	29	28	27	26	25	24
SL	R13		SLS			SLV	
R/W-0h	R-0h		R/W-0h			R/W-0h	
23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
NSLR	R12		NSLS			NSLV	
R/W-0h	R-0h		R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-896. PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SL	R/W	0h	The client software must set this bit to 1 to set the Snoop Latency Requirement bit in the LTR message to be sent.
30-29	R13	R	0h	Reserved
28-26	SLS	R/W	0h	The client software must program this field with the value to be sent in the Snoop Latency Scale field of the LTR message.
25-16	SLV	R/W	0h	The client software must program this field with the value to be sent in the Snoop Latency Value field of the LTR message.
15	NSLR	R/W	0h	The client software must set this bit to 1 to set the No-Snoop Latency Requirement bit in the LTR message to be sent.
14-13	R12	R	0h	N/A

Table 9-896. PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-10	NSLS	R/W	0h	The client software must program this field with the value to be sent in the No-Snoop Latency Scale field of the LTR message.
9-0	NSLV	R/W	0h	The client software must program this field with the value to be sent in the No-Snoop Latency Value field of the LTR message.

Table 9-897. Register Call Summary for PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_LTR_SNOOP_LAT_REG Register \(Offset = 0010021Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.57 PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG Register (Offset = 00100220h) [reset = X]

PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG is shown in Figure 9-296 and described in Table 9-899.

Return to the [Summary Table](#).

This register contains fields for the generation of Latency Tolerance Reporting (LTR) Messages. This register is to be used only when the Controller is configured in the EndPoint mode.

Table 9-898.
PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0220h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0220h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0220h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0220h

Figure 9-296. PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			TMFPSC	TMLMET	SLM	MLI	
R/W-X			R/W-1h	R/W-1h	R-0h	R/W-FAh	
7	6	5	4	3	2	1	0
MLI							
R/W-FAh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-899. PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12	TMFPSC	R/W	1h	When this bit is set to 1, the Controller will automatically transmit an LTR message when all the Functions in the Controller have transitioned to a non-D0 power state, provided that the following conditions are both true: 1. The Controller sent at least one LTR message since the Data Link layer last transitioned from down to up state. 2. The most recent LTR message transmitted by the Controller had as least one of the Requirement bits set. The Controller will set the Requirement bits in this LTR message to 0. When this bit 12 is 0, the Controller will not, by itself, send any LTR messages in response to Function Power State changes. Client logic may monitor the FUNCTION_POWER_STATE outputs of the Controller and transmit LTR messages through the master interface, in response to changes in their states.

Table 9-899. PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TMLMET	R/W	1h	<p>When this bit is set to 1, the Controller will automatically transmit an LTR message whenever the LTR Mechanism Enable bit in the Device Control 2 Register changes from 0 to 1, with the parameters specified in the LTR Snoop/No-Snoop Latency Register.</p> <p>When this bit is 1, the Controller will also transmit an LTR message whenever the LTR Mechanism Enable bit is cleared, if the following conditions are both true:</p> <ol style="list-style-type: none"> 1. The Controller sent at least one LTR message since the LTR Mechanism Enable bit was last set. 2. The most recent LTR message transmitted by the Controller had as least one of the Requirement bits set. <p>The Controller will set the Requirement bits in this LTR message to 0.</p> <p>When this bit 11 is 0, the Controller will not, by itself, send any LTR messages in response to state changes of the LTR Mechanism Enable bit. Client logic may monitor the state of the LTR_MECHANISM_ENABLE output of the Controller and transmit LTR messages through the master interface, in response to its state changes.</p>
10	SLM	R	0h	<p>Setting this bit causes the Controller to transmit an LTR message with the parameters specified in the LTR Snoop/No-Snoop Latency Register [Section 8.4.2.9].</p> <p>This bit is cleared by the Controller on transmitting the LTR message, and stays set until then.</p> <p>Client software must read this register and verify that this bit is 0 before setting it again to send a new message.</p> <p>This field becomes writable when LTR mechanism is enabled in device control-2 register.</p>
9-0	MLI	R/W	FAh	<p>This field specifies the minimum spacing between LTR messages transmitted by the Controller in units of microseconds.</p> <p>The PCI Express Specifications recommend sending no more than two LTR messages within a 500 microsecond interval.</p> <p>The Controller will wait for the minimum delay specified by this field after sending an LTR message, before transmitting a new LTR message.</p> <p>NOTE: The LINK can be in low power states[L0s and L1] when send LTR Message is triggered.</p> <p>So, the user has to consider the exit latencies while programming this field.</p> <p>It is recommended to program this field with about 2 us higher than the required interval to account for the L0s/L1 exit latencies.</p>

Table 9-900. Register Call Summary for PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_LTR_MSG_GEN_CTL_REG Register \(Offset = 00100220h\) \[reset = X\]: \[0\]](#)

9.4.58 PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_REG Register (Offset = 00100224h) [reset = 000186A0h]

PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_REG is shown in Figure 9-297 and described in Table 9-902.

Return to the [Summary Table](#).

This register stores the timeout delay parameter for the service timeout mechanism associated with the generation of PM_PME messages. In the EndPoint mode, the Controller will retransmit a PM_PME message after the expiration of this delay, if the Root Complex did not clear the PME Status bit in the Power Management Control and Status Register. This register is not used when the Controller is configured as Root Complex.

Table 9-901.
PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0224h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0224h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0224h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0224h

Figure 9-297. PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_REG Register

31	30	29	28	27	26	25	24
R21							
R-0h							
23	22	21	20	19	18	17	16
R21			DPMOPS	PSTD			
R-0h			R/W-0h	R/W-000186A0h			
15	14	13	12	11	10	9	8
PSTD							
R/W-000186A0h							
7	6	5	4	3	2	1	0
PSTD							
R/W-000186A0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-902. PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	R21	R	0h	Reserved
20	DPMOPS	R/W	0h	When this bit is set, Controller will not automatically send a PME message, when PM Status bit in PMCSR register is set
19-0	PSTD	R/W	000186A0h	Specifies the timeout delay for retransmission of PM_PME messages. The value is in units of microseconds. The actual time elapsed has a +1 microseconds tolerance from the value programmed.

Table 9-903. Register Call Summary for PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PME_SERVICE_TIMEOUT_DELAY_REG](#) Register (Offset = 00100224h) [reset = 000186A0h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.59 PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_REG Register (Offset = 00100228h) [reset = 0h]

PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_REG is shown in [Figure 9-298](#) and described in [Table 9-905](#).

Return to the [Summary Table](#).

When the Controller is configured as Root Complex, this ID will be used for all internally generated messages.

Table 9-904.
PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0228h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0228h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0228h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0228h

Figure 9-298. PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																RPRI															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-905. PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R0	R	0h	Reserved
15-0	RPRI	R/W	0h	RID [bus, device and function numbers] for all TLPs internally generated by Root Port

Table 9-906. Register Call Summary for PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ROOT_PORT_REQUESTOR_ID_REG Register \(Offset = 00100228h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.60 PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG Register (Offset = 0010022Ch) [reset = 0h]

PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG is shown in Figure 9-299 and described in Table 9-908.

Return to the [Summary Table](#).

When the Controller is configured as End Point, this register holds the Bus and Device number captured for Function 0

Table 9-907.
PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 022Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 022Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 022Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 022Ch

Figure 9-299. PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R16																EPBN				R5				EPDN							
R-0h																R-0h				R-0h				R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-908. PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-8	EPBN	R	0h	Bus Number captured by Function 0 in End Point mode
7-5	R5	R	0h	Reserved
4-0	EPDN	R	0h	Device Number captured by Function 0 in End Point mode

Table 9-909. Register Call Summary for PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_EP_BUS_DEVICE_NUMBER_REG Register \(Offset = 0010022Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.61 PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG Register (Offset = 00100234h) [reset = 10040850h]

PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG is shown in Figure 9-300 and described in Table 9-911.

Return to the [Summary Table](#).

N/A

Table 9-910.
PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0234h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0234h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0234h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0234h

Figure 9-300. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG Register

31	30	29	28	27	26	25	24
R31			DFLRTRB	DTAE2EP	R26	MSIXMSKEN	MSIMSKEN
R-0h			R/W-1h	R/W-0h	R-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
VARCCLKEN	MAXNPREQ						
R/W-0h				R/W-20h			
15	14	13	12	11	10	9	8
MAXNPREQ			AXINSPEN_R SVD	CMPTOADV	PSNADV	MSIPIMS	ENG4REV05
R/W-20h			R-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BLKALNWIN		BLKALNCHK	ARICAPMOD	ENLNCHK	DISSDSCHK	EXTSNP	DLFFS
R/W-1h		R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-911. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	R31	R	0h	Reserved
28	DFLRTRB	R/W	1h	1 : NP Termination due to FLR/Completion Timeout is delayed till the RX Completion FIFO is Empty. 0 : NP Termination due to FLR is done immediately on receiving FLR/Completion Timeout.
27	DTAE2EP	R/W	0h	By default, when End to End Parity error is detected on inbound/outbound data streams, then all the transmitted outbound packets will be Nullified by the Controller. This bit can be used to turn off nullifying Tx packets on End to End Parity Error.
26	R26	R	0h	Reserved

Table 9-911. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	MSIXMSKEN	R/W	0h	By default, the Controller provides a single status bit when any function's MSIX Function Mask is programmed or configured by Local firmware or Host SW. Controller also implements an enhanced MSIX Function Mask Interrupt mechanism, which provides per-function set/clear status when a function's MSIX Function Mask is updated by SW. This Local Management programmable bit allows user to choose between the Default and Enhanced MSIX Function Mask Change Interrupt mechanisms.
24	MSIMSKEN	R/W	0h	By default, the Controller provides a single status bit when any function's MSI Mask is programmed or configured by Local firmware or Host SW. Controller also implements an enhanced MSI Mask Interrupt mechanism, which provides per-function set/clear status when a function's MSI Mask is updated by SW. This Local Management programmable bit allows user to choose between the Default and Enhanced MSI Mask Change Interrupt mechanisms.
23	VARCCLKEN	R/W	0h	If this bit is set the CORE_CLK input can be driven with Variable Clock depending on the Link Speed, similar to the PIPE_PCLK.
22-13	MAXNPREQ	R/W	20h	The Controller supports 32 outstanding NP requests that can be initiated by the User. However, the number of split completion TLPs that can be stored in the Controller is limited to 128. The Completion FIFO will overflow if more than 128 split completion packets are pending. If the User interface can accept inbound Posted and Completion packets at the same rate as received from PCIe link, then the split completion FIFO will never reach the FULL condition. However, if the User cannot guarantee this, then this register needs to be programmed as described in the Programming Guide section of the Controller User guide. The Controller will limit the maximum number of outstanding NP requests to the value programmed in this register. Example: 8 : Controller will limit maximum number of outstanding NP requests to 8. 0-7 : Reserved Default Value is 32
12	AXINSPEN_RSVD	R	0h	RESERVED
11	CMPTOADV	R/W	1h	As per PCIe specification on Error Signaling, the Requester detecting a Completion Timeout is allowed to handle this as an Advisory Non Fatal Error. 1: Completion Timeout is handled as Advisory Non-Fatal Error. 0: Completion Timeout is handled as normally as a Non-Fatal Error.
10	PSNADV	R/W	0h	As per PCIe specification 2.7.2.2, the following Poisoned TLP requests must be handled as Uncorrectable and not as Advisory: I/O Write Request, Memory Write Request, or non-vendor-defined Message with data that target a Control structure. Since it is not possible for the Controller to determine if the target is a Control or a non-Control structure, the Controller implements this bit for the user to determine the required handling. 1: Poisoned TLP of type IOWr, MemWr, MsgD will be handled as Advisory Non-Fatal Error. 0: Poisoned TLP of type IOWr, MemWr, MsgD will be handled as Uncorrectable Error. Note: Poisoned CplD will always be reported as Advisory Non-Fatal and is not controlled by this register setting.

Table 9-911. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MSIPIMS	R/W	0h	If the Client wishes to use the MSI_PENDING_STATUS_IN Signal to Update the MSI pending Bits register, this bit needs to be set to 1. Otherwise the Pending Bits register is updated via the APB Interface
8	ENG4REV05	R/W	0h	When operating in Gen4 16GT/s , This Enables Gen4 Spec Revision 0.5 EIEOS and SKP features. When disabled, the Gen4 1.0 features are enabled, by default this bit is ZERO. 1: Enable Gen4 0.5 Features 0: Disable Gen4 0.5 Features [This enabled the Gen4 1.0 Features] .
7-6	BLKALNWIN	R/W	1h	When in the data stream at Gen3 or higher speeds, the pipe_rx_valid is asserted by the PHY. If the block alignment is lost, then the PHY may deassert pipe_rx_valid. Controller reports loss of block alignment if pipe_rx_valid or pipe_rx_data_valid=0 for a period consecutive clock cycles as programmed in this field. 00: 8 CORE_CLK cycles 01: 16 CORE_CLK cycles 10: 64 CORE_CLK cycles 11: 256 CORE_CLK cycles
5	BLKALNCHK	R/W	0h	When in the data stream at Gen3 or higher speeds, the pipe_rx_valid is asserted by the PHY. If the block alignment is lost, then the PHY may deassert pipe_rx_valid. Block Alignment may be lost if the received sync header is invalid. Controller supports detecting loss of block alignment while in a data stream in Gen3. 0: Enable check for loss of Gen3 Block Alignment during data stream. 1: Disable check for loss of Gen3 Block Alignment.
4	ARICAPMOD	R/W	1h	As per SR IOC specification, ARI Capable Hierarchy bit is only present in the lowest numbered PF of a Device. The Controller has two modes to determine the lowest numbered PF. 0: the first PF which is enabled [PF0] is taken as the lowest numbered PF. 1: the first PF which has a non-zero TOTAL_VF_COUNT field is taken as the lowest numbered PF.[Default Mode]
3	ENLNCHK	R/W	0h	As per PCIe specification, LTSSM should transition to Disabled after any Lanes that are transmitting TS1 Ordered Sets receive two consecutive TS1 Ordered Sets with the Disable Link bit asserted. Similarly, LTSSM should transition to Loopback after all Lanes that are transmitting TS1 Ordered Sets, that are also receiving TS1 Ordered Sets, receive the Loopback bit asserted in two consecutive TS1 Ordered Sets. Controller ignores the Link and Lane Number in the Received TS1s with Loopback/Disable bit set. Setting this bit to 1 turns on the check for link number [assigned by RC in Recovery.Idle] and lane number [PAD in Config.LW.Start or as assigned by RC in Recovery.Idle]. This bit is recommended to be kept at the default value of 0.
2	DISSDSCHK	R/W	0h	As per PCIe specification, When using 128b/130b encoding, next state is L0 if eight consecutive Symbol Times of Idle data are received on all configured Lanes. The Controller checks to ensure that the Idle symbols of data are received in Data Blocks after SDS OS. This check is enabled by default. Setting this bit to 1 turns off this check. This bit is recommended to be kept at the default value of 0.

Table 9-911. PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EXTSNP	R/W	0h	This bit can be set if an extra clock cycle is required by the Client Application logic to respond with the Read Data on Configuration Snoop Interface. Please refer to the user guide section on Configuration Snoop Interface for timing diagrams.
0	DLFFS	R/W	0h	As per PIPE 4.2 specification, the LOCALLF, LOCALFS outputs from PHY can be sampled uponf PHYSTATUS pulse after Reset# OR upon the first PHYSTATUS pulse after speed change to GEN3. This bit can be set to 1 to disable sampling after speed change to GEN3 or higher

Table 9-912. Register Call Summary for PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_DEBUG_MUX_CONTROL_2_REG Register \(Offset = 00100234h\) \[reset = 10040850h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.62 PCIE_CORE_LM_I_PHY_STATUS_1_REG Register (Offset = 00100238h) [reset = 0h]

PCIE_CORE_LM_I_PHY_STATUS_1_REG is shown in Figure 9-301 and described in Table 9-914.

Return to the [Summary Table](#).

This status register provides additional debug information about the PHY. Bits 8:0 provide information to debug Receiver Errors.

Table 9-913.
PCIE_CORE_LM_I_PHY_STATUS_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0238h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0238h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0238h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0238h

Figure 9-301. PCIE_CORE_LM_I_PHY_STATUS_1_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							LOSBLKALN
R-0h							R/W1C-0h
7	6	5	4	3	2	1	0
INVSYNHR	OSAFSDS	G3FRERR	OSWOEDS	DATEDS	ILOSEDS	OSASKP	TLP PHYER
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-914. PCIE_CORE_LM_I_PHY_STATUS_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	R31	R	0h	Reserved
8	LOSBLKALN	R/W1C	0h	This bit is set if the PHY Loses Block Alignment during data stream. This is detected based upon an unexpected PIPE_RX_VALID input deassertion during data stream. Write a 1 to clear this error.
7	INVSYNHR	R/W1C	0h	This bit is set if an invalid Sync Header is detected. 00 and 11 are Invalid Sync Headers. Write a 1 to clear this error.
6	OSAFSDS	R/W1C	0h	This bit is set if an SDS is received after an SDS. This is a framing error. Write a 1 to clear this error.
5	G3FRERR	R/W1C	0h	This bit is set if a framing error is detected while receiving a TLP in Gen3. Example, if an invalid token is received in a data stream, this error is flagged. Write a 1 to clear this error.
4	OSWOEDS	R/W1C	0h	This bit is set if an Ordered Set Block is received without an EDS. This is a framing error. Write a 1 to clear this error.
3	DATEDS	R/W1C	0h	This bit is set if a Data Block is received after an EDS. Write a 1 to clear this error.

Table 9-914. PCIE_CORE_LM_I_PHY_STATUS_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ILOSEDS	R/W1C	0h	The Valid OS blocks after an EDS are EIOS, EIEOS and SKP. If any other OS blocks are received after EDS, then it is a framing error and this bit is asserted.
1	OSASKP	R/W1C	0h	This bit indicates that an Ordered Set BLock was received immediately after a SKIP OS. This is a framing error. Write a 1 to clear this field.
0	TLPPHYER	R/W1C	0h	This bit indicates that a PHY Error was detected on the PIPE_RX_STATUS within a TLP. Write a 1 to clear this field.

Table 9-915. Register Call Summary for PCIE_CORE_LM_I_PHY_STATUS_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PHY_STATUS_1_REG Register \(Offset = 00100238h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.63 PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG Register (Offset = 00100240h) [reset = 05050585h]

PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG is shown in [Figure 9-302](#) and described in [Table 9-917](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 0

Table 9-916.
PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0240h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0240h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0240h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0240h

Figure 9-302. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C				BAR3A				BAR2C				BAR2A			
R/W-0h				R/W-5h				R/W-0h				R/W-5h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C				BAR1A				BAR0C				BAR0A			
R/W-0h				R/W-5h				R/W-4h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-917. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-917. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-917. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-917. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR0C	R/W	4h	Specifies the configuration of BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-917. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-918. Register Call Summary for PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_0_BAR_CONFIG_0_REG](#) Register (Offset = 00100240h) [reset = 05050585h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.64 PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG Register (Offset = 00100244h) [reset = 505h]

PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG is shown in Figure 9-303 and described in Table 9-920.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function.

Table 9-919.
PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0244h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0244h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0244h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0244h

Figure 9-303. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-920. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110-111: Reserved

Table 9-920. PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	BAR5A	R/W	5h	<p>Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
7-5	BAR4C	R/W	0h	<p>Specifies the configuration of BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-920. PCIe_CORE_LM_I_PF_0_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-921. Register Call Summary for PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_0_BAR_CONFIG_1_REG](#) Register (Offset = 00100244h) [reset = 505h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.65 PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG Register (Offset = 00100248h) [reset = 05050585h]

PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG is shown in [Figure 9-304](#) and described in [Table 9-923](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 1

Table 9-922.
PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0248h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0248h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0248h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0248h

Figure 9-304. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C				BAR3A				BAR2C				BAR2A			
R/W-0h				R/W-5h				R/W-0h				R/W-5h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C				BAR1A				BAR0C				BAR0A			
R/W-0h				R/W-5h				R/W-4h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-923. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-923. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-923. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-923. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR0C	R/W	4h	Specifies the configuration of BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-923. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-924. Register Call Summary for PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_1_BAR_CONFIG_0_REG](#) Register (Offset = 00100248h) [reset = 05050585h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.66 PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG Register (Offset = 0010024Ch) [reset = 505h]

PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG is shown in Figure 9-305 and described in Table 9-926.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function.

Table 9-925.
PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 024Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 024Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 024Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 024Ch

Figure 9-305. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-926. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110-111: Reserved

Table 9-926. PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	BAR5A	R/W	5h	<p>Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
7-5	BAR4C	R/W	0h	<p>Specifies the configuration of BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-926. PCIe_CORE_LM_I_PF_1_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-927. Register Call Summary for PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_1_BAR_CONFIG_1_REG](#) Register (Offset = 0010024Ch) [reset = 505h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.67 PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG Register (Offset = 00100250h) [reset = 05050585h]

PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG is shown in [Figure 9-306](#) and described in [Table 9-929](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 2

Table 9-928.
PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0250h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0250h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0250h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0250h

Figure 9-306. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C				BAR3A				BAR2C				BAR2A			
R/W-0h				R/W-5h				R/W-0h				R/W-5h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C				BAR1A				BAR0C				BAR0A			
R/W-0h				R/W-5h				R/W-4h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-929. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-929. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-929. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-929. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR0C	R/W	4h	Specifies the configuration of BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-929. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-930. Register Call Summary for PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_2_BAR_CONFIG_0_REG](#) Register (Offset = 00100250h) [reset = 05050585h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.68 PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG Register (Offset = 00100254h) [reset = 505h]

PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG is shown in Figure 9-307 and described in Table 9-932.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function.

Table 9-931.
PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0254h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0254h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0254h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0254h

Figure 9-307. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-932. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110-111: Reserved

Table 9-932. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	BAR5A	R/W	5h	<p>Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
7-5	BAR4C	R/W	0h	<p>Specifies the configuration of BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-932. PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-933. Register Call Summary for PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_2_BAR_CONFIG_1_REG](#) Register (Offset = 00100254h) [reset = 505h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.69 PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG Register (Offset = 00100258h) [reset = 05050585h]

PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG is shown in [Figure 9-308](#) and described in [Table 9-935](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 3

Table 9-934.
PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0258h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0258h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0258h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0258h

Figure 9-308. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C				BAR3A				BAR2C				BAR2A			
R/W-0h				R/W-5h				R/W-0h				R/W-5h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C				BAR1A				BAR0C				BAR0A			
R/W-0h				R/W-5h				R/W-4h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-935. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-935. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-935. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-935. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR0C	R/W	4h	Specifies the configuration of BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-935. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-936. Register Call Summary for PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_3_BAR_CONFIG_0_REG](#) Register (Offset = 00100258h) [reset = 05050585h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.70 PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG Register (Offset = 0010025Ch) [reset = 505h]

PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG is shown in Figure 9-309 and described in Table 9-938.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function.

Table 9-937.
PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 025Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 025Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 025Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 025Ch

Figure 9-309. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-938. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110-111: Reserved

Table 9-938. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	BAR5A	R/W	5h	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR4C	R/W	0h	Specifies the configuration of BAR4. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-938. PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-939. Register Call Summary for PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_PF_3_BAR_CONFIG_1_REG Register \(Offset = 0010025Ch\) \[reset = 505h\]: \[0\]](#)

9.4.71 PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG Register (Offset = 00100260h) [reset = 05050585h]

PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG is shown in [Figure 9-310](#) and described in [Table 9-941](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 4

Table 9-940.
PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0260h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0260h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0260h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0260h

Figure 9-310. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C				BAR3A				BAR2C				BAR2A			
R/W-0h				R/W-5h				R/W-0h				R/W-5h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C				BAR1A				BAR0C				BAR0A			
R/W-0h				R/W-5h				R/W-4h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-941. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-941. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-941. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-941. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR0C	R/W	4h	Specifies the configuration of BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-941. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-942. Register Call Summary for PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_PF_4_BAR_CONFIG_0_REG Register \(Offset = 00100260h\) \[reset = 05050585h\]: \[0\]](#)

9.4.72 PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG Register (Offset = 00100264h) [reset = 505h]

PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG is shown in Figure 9-311 and described in Table 9-944.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function.

Table 9-943.
PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0264h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0264h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0264h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0264h

Figure 9-311. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-944. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110-111: Reserved

Table 9-944. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	BAR5A	R/W	5h	<p>Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
7-5	BAR4C	R/W	0h	<p>Specifies the configuration of BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-944. PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-945. Register Call Summary for PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_4_BAR_CONFIG_1_REG](#) Register (Offset = 00100264h) [reset = 505h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.73 PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG Register (Offset = 00100268h) [reset = 05050585h]

PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG is shown in [Figure 9-312](#) and described in [Table 9-947](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 5

Table 9-946.
PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0268h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0268h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0268h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0268h

Figure 9-312. PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C				BAR3A				BAR2C				BAR2A			
R/W-0h				R/W-5h				R/W-0h				R/W-5h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C				BAR1A				BAR0C				BAR0A			
R/W-0h				R/W-5h				R/W-4h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-947. PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-947. PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-947. PCIe_CORE_LM_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-947. PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR0C	R/W	4h	Specifies the configuration of BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-947. PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-948. Register Call Summary for PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_5_BAR_CONFIG_0_REG](#) Register (Offset = 00100268h) [reset = 05050585h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.74 PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG Register (Offset = 0010026Ch) [reset = 505h]

PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG is shown in Figure 9-313 and described in Table 9-950.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function.

Table 9-949.
PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 026Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 026Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 026Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 026Ch

Figure 9-313. PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-950. PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110-111: Reserved

Table 9-950. PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	BAR5A	R/W	5h	<p>Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
7-5	BAR4C	R/W	0h	<p>Specifies the configuration of BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-950. PCIe_CORE_LM_I_PF_5_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB</p>

Table 9-951. Register Call Summary for PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_5_BAR_CONFIG_1_REG](#) Register (Offset = 0010026Ch) [reset = 505h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.75 PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG Register (Offset = 00100280h) [reset = 0F0F8FCFh]

PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG is shown in Figure 9-314 and described in Table 9-953.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 0

Table 9-952.
PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0280h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0280h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0280h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0280h

Figure 9-314. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-953. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-953. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-953. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-953. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001-010: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-953. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-954. Register Call Summary for PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_0_REG Register \(Offset = 00100280h\) \[reset = 0F0F8FCFh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.76 PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG Register (Offset = 00100284h) [reset = F0Fh]

PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG is shown in Figure 9-315 and described in Table 9-956.

Return to the [Summary Table](#).

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 9-955.
PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0284h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0284h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0284h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0284h

Figure 9-315. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-956. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-956. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: 00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes
7-5	VFBAR4C	R/W	0h	Specifies the configuration of VF BAR4. The various encodings are: 000: Disabled 001-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-956. PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-957. Register Call Summary for PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_0_VF_BAR_CONFIG_1_REG Register \(Offset = 00100284h\) \[reset = F0Fh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.77 PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG Register (Offset = 00100288h) [reset = 0F0F8FCFh]

PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG is shown in [Figure 9-316](#) and described in [Table 9-959](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 1

Table 9-958.
PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0288h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0288h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0288h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0288h

Figure 9-316. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-959. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-959. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-959. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-959. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-959. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-960. Register Call Summary for PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_0_REG Register \(Offset = 00100288h\) \[reset = 0F0F8FCFh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.78 PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG Register (Offset = 0010028Ch) [reset = F0Fh]

PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG is shown in Figure 9-317 and described in Table 9-962.

Return to the [Summary Table](#).

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 9-961.
PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 028Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 028Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 028Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 028Ch

Figure 9-317. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-962. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-962. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: 00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes
7-5	VFBAR4C	R/W	0h	Specifies the configuration of VF BAR4. The various encodings are: 000: Disabled 001-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-962. PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-963. Register Call Summary for PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_1_VF_BAR_CONFIG_1_REG Register \(Offset = 0010028Ch\) \[reset = F0Fh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.79 PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG Register (Offset = 00100290h) [reset = 0F0F8FCFh]

PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG is shown in [Figure 9-318](#) and described in [Table 9-965](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 2

Table 9-964.
PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0290h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0290h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0290h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0290h

Figure 9-318. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-965. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-965. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001-010: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-965. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-965. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-965. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-966. Register Call Summary for PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_0_REG Register \(Offset = 00100290h\) \[reset = 0F0F8FCFh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.80 PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG Register (Offset = 00100294h) [reset = F0Fh]

PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG is shown in Figure 9-319 and described in Table 9-968.

Return to the [Summary Table](#).

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 9-967.
PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0294h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0294h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0294h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0294h

Figure 9-319. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-968. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-968. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: 00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes
7-5	VFBAR4C	R/W	0h	Specifies the configuration of VF BAR4. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-968. PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-969. Register Call Summary for PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_2_VF_BAR_CONFIG_1_REG Register \(Offset = 00100294h\) \[reset = F0Fh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.81 PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG Register (Offset = 00100298h) [reset = 0F0F8FCFh]

PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG is shown in Figure 9-320 and described in Table 9-971.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 3

Table 9-970.
PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0298h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0298h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0298h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0298h

Figure 9-320. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-971. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-971. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001-010: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-971. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-971. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-971. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-972. Register Call Summary for PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_0_REG Register \(Offset = 00100298h\) \[reset = 0F0F8FCFh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.82 PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG Register (Offset = 0010029Ch) [reset = F0Fh]

PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG is shown in Figure 9-321 and described in Table 9-974.

Return to the [Summary Table](#).

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 9-973.
PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 029Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 029Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 029Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 029Ch

Figure 9-321. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-974. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-974. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: 00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes
7-5	VFBAR4C	R/W	0h	Specifies the configuration of VF BAR4. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-974. PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-975. Register Call Summary for PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_PF_3_VF_BAR_CONFIG_1_REG Register \(Offset = 0010029Ch\) \[reset = F0Fh\]: \[0\]](#)

9.4.83 PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG Register (Offset = 001002A0h) [reset = 0F0F8FCFh]

PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG is shown in [Figure 9-322](#) and described in [Table 9-977](#).

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 4

Table 9-976.
PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02A0h

Figure 9-322. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-977. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-977. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001-010: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-977. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-977. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001-010: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-977. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-978. Register Call Summary for PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_0_REG Register \(Offset = 001002A0h\) \[reset = 0F0F8FCFh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.84 PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG Register (Offset = 001002A4h) [reset = F0Fh]

PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG is shown in Figure 9-323 and described in Table 9-980.

Return to the [Summary Table](#).

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 9-979.
PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02A4h

Figure 9-323. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-980. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-980. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: 00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes
7-5	VFBAR4C	R/W	0h	Specifies the configuration of VF BAR4. The various encodings are: 000: Disabled 001-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-980. PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-981. Register Call Summary for PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_4_VF_BAR_CONFIG_1_REG Register \(Offset = 001002A4h\) \[reset = F0Fh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.85 PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG Register (Offset = 001002A8h) [reset = 0F0F8FCFh]

PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG is shown in Figure 9-324 and described in Table 9-983.

Return to the [Summary Table](#).

This register specifies the configuration of the BARs associated with the Physical Function 5

Table 9-982.
PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02A8h

Figure 9-324. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-983. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-983. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001-010: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-983. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-983. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001-011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-983. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-984. Register Call Summary for PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_0_REG Register \(Offset = 001002A8h\) \[reset = 0F0F8FCFh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.86 PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG Register (Offset = 001002ACh) [reset = F0Fh]

PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG is shown in Figure 9-325 and described in Table 9-986.

Return to the [Summary Table](#).

This register specifies the configuration of the VF BARs associated with the Physical Function.

Table 9-985.
PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02ACh

Figure 9-325. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-986. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-986. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR. The encodings are: 00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes
7-5	VFBAR4C	R/W	0h	Specifies the configuration of VF BAR4. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-986. PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

Table 9-987. Register Call Summary for PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_5_VF_BAR_CONFIG_1_REG Register \(Offset = 001002ACh\) \[reset = F0Fh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.87 PCIE_CORE_LM_I_PF_CONFIG_REG Register (Offset = 001002C0h) [reset = 3Fh]

PCIE_CORE_LM_I_PF_CONFIG_REG is shown in Figure 9-326 and described in Table 9-989.

Return to the [Summary Table](#).

This register contains the enable bits for all the Functions implemented by the Controller. Resetting the enable bit of a Function disables the Function from responding to configuration requests.

Table 9-988. PCIE_CORE_LM_I_PF_CONFIG_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02C0h

Figure 9-326. PCIE_CORE_LM_I_PF_CONFIG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R										F5E	F4E	F3E	F2E	F1E	F0E
R-0h										R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-989. PCIE_CORE_LM_I_PF_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	R	R	0h	Reserved
5	F5E	R/W	1h	Enable for Function 5. This bit can be modified from the local management bus.
4	F4E	R/W	1h	Enable for Function 4. This bit can be modified from the local management bus.
3	F3E	R/W	1h	Enable for Function 3. This bit can be modified from the local management bus.
2	F2E	R/W	1h	Enable for Function 2. This bit can be modified from the local management bus.
1	F1E	R/W	1h	Enable for Function 1. This bit can be modified from the local management bus.
0	F0E	R	1h	Enable for Function 0. This bit is hardwired to 1.

Table 9-990. Register Call Summary for PCIE_CORE_LM_I_PF_CONFIG_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PF_CONFIG_REG Register \(Offset = 001002C0h\) \[reset = 3Fh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.88 PCIE_CORE_LM_I_RC_BAR_CONFIG_REG Register (Offset = 00100300h) [reset = 2914h]

PCIE_CORE_LM_I_RC_BAR_CONFIG_REG is shown in Figure 9-327 and described in Table 9-992.

Return to the [Summary Table](#).

The root complex side of the Controller contains two memory BARs that can be used for address-range checking of incoming requests from devices connected to it. The fields in this register determine the configuration of these BARs.

Table 9-991.
PCIE_CORE_LM_I_RC_BAR_CONFIG_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0300h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0300h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0300h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0300h

Figure 9-327. PCIE_CORE_LM_I_RC_BAR_CONFIG_REG Register

31	30	29	28	27	26	25	24
RCBCE	R10						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R10			RCBARPIS	RCBARPIE	RCBARPMS	RCBARPME	RCBAR1C
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RCBAR1C		RCBAR1A					RCBAR0C
R/W-0h		R/W-14h					R/W-4h
7	6	5	4	3	2	1	0
RCBAR0C		RCBAR0A					
R/W-4h		R/W-14h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-992. PCIE_CORE_LM_I_RC_BAR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RCBCE	R/W	0h	This bit must be set to 1 to enable BAR checking in the RC mode. When this bit is set to 0, the Controller will forward all incoming memory requests to the client logic without checking their address ranges.
30-21	R10	R	0h	Reserved
20	RCBARPIS	R/W	0h	Width of IO Base and Limit registers in type1 config space. 0=32 bits, 1=64bits
19	RCBARPIE	R/W	0h	Enable for IO Base and Limit registers in type1 config space
18	RCBARPMS	R/W	0h	Width of Prefetchable Memory Base and Limit registers in type1 config space. 0=32 bits, 1=64bits
17	RCBARPME	R/W	0h	Enable for Prefetchable memory base and limit registers in type1 config space

Table 9-992. PCIE_CORE_LM_I_RC_BAR_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-14	RCBAR1C	R/W	0h	Specifies the configuration of RC BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
13-9	RCBAR1A	R/W	14h	This field specifies the aperture of the RC BAR 1. The encodings are: 0000 = 4, 00001 =8B,..... 1_ 1101 = 2G
8-6	RCBAR0C	R/W	4h	Specifies the configuration of RC BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable
5-0	RCBAR0A	R/W	14h	This field specifies the aperture of the RC BAR 0. The encodings are: 0000 = 4, 00001 =8B,..... 01_ 1111 = 8G,10_ 0100 = 256G.

Table 9-993. Register Call Summary for PCIE_CORE_LM_I_RC_BAR_CONFIG_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_RC_BAR_CONFIG_REG Register \(Offset = 00100300h\) \[reset = 2914h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.89 PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG Register (Offset = 00100360h) [reset = 0007FF00h]

PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG is shown in Figure 9-328 and described in Table 9-995.

Return to the [Summary Table](#).

This register specifies the default transmitter preset and default receiver preset hint used by Controller for lanes that have not received EQ TS2s during Recovery.RcvrConfig LTSSM state

Table 9-994.
PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0360h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0360h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0360h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0360h

Figure 9-328. PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R31												S8GPR			
R-0h												R/W-7FFh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S8GPR								R7	GDRXPH				GDTXP		
R/W-7FFh								R-0h		R/W-0h			R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-995. PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	R31	R	0h	Reserved
18-8	S8GPR	R/W	7FFh	This register can be used to program the Presets that are supported by local Transmitter at 8Gbps. Default value of this register is determined by the SUPPORTED_PRESET strap input. Note: At 8.0 GT/s and 16.0 GT/s all preset values must be supported for Full swing signaling. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3.
7	R7	R	0h	Reserved
6-4	GDRXPH	R/W	0h	Default receiver preset hint value used for a lane that did not receive EQ TS2 in Recovery.RcvrCfg LTSSM state
3-0	GDTXP	R/W	0h	Default transmitter preset value used for a lane that did not receive EQ TS2 in Recovery.RcvrCfg LTSSM state

Table 9-996. Register Call Summary for PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_GEN3_DEFAULT_PRESET_REG Register \(Offset = 00100360h\) \[reset = 0007FF00h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.90 PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Register (Offset = 00100364h) [reset = C001E848h]

PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG is shown in [Figure 9-329](#) and described in [Table 9-998](#).

Return to the [Summary Table](#).

This register is used to tune the time spent for evaluation per TX Setting in Endpoint Phase 2 (RC Mode Phase 3) of GEN3, GEN4 Link Equalization.

The PCIe Spec defines a timeout of 2ms per TX setting and hence the default value for this register is set to 2ms.

This can be tweaked based on the total number of iterations done and the time required for the PHY to respond with feedback for RXEQEVAL request.

The total time taken in Endpoint Phase 2 (RC Mode Phase 3) must be less than 24 ms as defined by spec.

Guideline: (Total Number of iterations)*(link_eq_timeout_2ms_reg + max time required for PHY to respond to RXEQEVAL) less than 24ms

Table 9-997.
PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0364h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0364h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0364h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0364h

Figure 9-329. PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Register

31	30	29	28	27	26	25	24
RXEQABM		RXEQABD	R28	LEQT2MS			
R/W-3h		R/W-0h	R-0h	R/W-0001E848h			
23	22	21	20	19	18	17	16
LEQT2MS							
R/W-0001E848h							
15	14	13	12	11	10	9	8
LEQT2MS							
R/W-0001E848h							
7	6	5	4	3	2	1	0
LEQT2MS							
R/W-0001E848h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-998. PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RXEQABM	R/W	3h	When a 24ms timeout occurs in the LTSSM Equalization Phase 2, the Controller aborts Equalization Phase 2 and transitions to Recovery.Rcvr.Lock. In this case, the RxEqEval output on the PIPE Interface will be de-asserted immediately [if it was asserted]. The RxEqInProgress output will stay high and waits for PhyStatus pulse. Controller implements a timer to select an upper limit to wait for this PhyStatus pulse during an abort to de-assert RxEqInProgress. 00: Wait for a maximum of 4 PIPE_PCLK period. 01: Wait for a maximum of 8 PIPE_PCLK period. 10: Wait for a maximum of 16 PIPE_PCLK period. 11: Disabled. Wait till PhyStatus Pulse is received. Note: This register is used only if RxEqEval was asserted when LTSSM 24ms timeout occurred in Equalization.
29	RXEQABD	R/W	0h	In an unexpected case where the PIPE_PCLK stops due to error in equalization, this bit can be set to de-couple RxEqInProgress from the rest of the equalization state machine. This bit should not be set for normal usage.
28	R28	R	0h	Reserved
27-0	LEQT2MS	R/W	0001E848h	Time spent for evaluation per TX Setting in Endpoint Phase 2 [RC Mode Phase 3] of Link Equalization specified in multiples of 16ns. eg. the value 125000 will result in 125000*16ns = 2ms. Simulation with reduced time mode[PCIE_SIM define] will give a smaller value of 300 as power on reset value.

Table 9-999. Register Call Summary for PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Register \(Offset = 00100364h\) \[reset = C001E848h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.91 PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG Register (Offset = 00100368h) [reset = 0h]

PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG is shown in Figure 9-330 and described in Table 9-1001.

Return to the [Summary Table](#).

This register includes bits to control pipe fifo latency

Table 9-1000.
PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0368h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0368h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0368h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0368h

Figure 9-330. PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31							DPTFCE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1001. PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R31	R	0h	Reserved
0	DPTFCE	R/W	0h	By default, if FIFO empty is reached, the PIPE TX FIFO accumulates 2 entries before reading the FIFO again. This is to prevent FIFO from reaching empty again. This bit must remain at 0 to allow the PIPE TX FIFO to recover effectively from a Empty condition.

Table 9-1002. Register Call Summary for PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PIPE_FIFO_LATENCY_CTRL_REG Register \(Offset = 00100368h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.92 PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG Register (Offset = 00100374h) [reset = 0007FF00h]

PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG is shown in Figure 9-331 and described in Table 9-1004.

Return to the [Summary Table](#).

This register specifies the default transmitter preset and default receiver preset hint used by Controller for lanes that have not received 16G EQ TS2s during Recovery.RcvrConfig LTSSM state

Table 9-1003.
PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0374h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0374h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0374h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0374h

Figure 9-331. PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R31												S16GPR			
R-0h												R/W-7FFh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S16GPR								R7	GDRXPH				GDTXP		
R/W-7FFh								R-0h		R/W-0h			R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1004. PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	R31	R	0h	Reserved
18-8	S16GPR	R/W	7FFh	This register can be used to program the Presets that are supported by local Transmitter at 16Gbps. Default value of this register is determined by the SUPPORTED_PRESET strap input. Note: At 8.0 GT/s and 16.0 GT/s all preset values must be supported for Full swing signaling. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3.
7	R7	R	0h	Reserved
6-4	GDRXPH	R/W	0h	Default Gen4 receiver preset hint value used for a lane that did not receive 16G EQ TS2 in Recovery.RcvrCfg LTSSM state
3-0	GDTXP	R/W	0h	Default Gen4 transmitter preset value used for a lane that did not receive 16G EQ TS2 in Recovery.RcvrCfg LTSSM state

Table 9-1005. Register Call Summary for PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_GEN4_DEFAULT_PRESET_REG Register \(Offset = 00100374h\) \[reset = 0007FF00h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.93 PCIE_CORE_LM_I_PHY_CONFIG_REG3 Register (Offset = 00100378h) [reset = 40h]

PCIE_CORE_LM_I_PHY_CONFIG_REG3 is shown in [Figure 9-332](#) and described in [Table 9-1007](#).

[Return to the Summary Table.](#)

This register specifies the PHY Specific registers for used in Gen4

Table 9-1006.
PCIE_CORE_LM_I_PHY_CONFIG_REG3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0378h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0378h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0378h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0378h

Figure 9-332. PCIE_CORE_LM_I_PHY_CONFIG_REG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R24																TFC4															
R-0h																R/W-40h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1007. PCIE_CORE_LM_I_PHY_CONFIG_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R24	R	0h	Reserved
7-0	TFC4	R/W	40h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from LOS state at 16 GT/s speed.

Table 9-1008. Register Call Summary for PCIE_CORE_LM_I_PHY_CONFIG_REG3

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PHY_CONFIG_REG3 Register \(Offset = 00100378h\) \[reset = 40h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.94 PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register (Offset = 0010037Ch) [reset = 0h]

PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG is shown in Figure 9-333 and described in Table 9-1010.

Return to the [Summary Table](#).

This register is used to Control GEN3, GEN4 Link Equalization Procedure.

Table 9-1009.
PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_R
EG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 037Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 037Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 037Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 037Ch

Figure 9-333. PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register

31	30	29	28	27	26	25	24
RES20							
R-0h							
23	22	21	20	19	18	17	16
RES20				MX16GERL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
MX8GERL				RES10		QG16GT	QG8GT
R/W-0h				R-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RES6		EP16GRE	EP8GRE	RES3	MXECC		
R-0h		R/W-0h	R/W-0h	R-0h	R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1010. PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RES20	R	0h	Reserved
19-16	MX16GERL	R/W	0h	The number of 16GT/s Equalization Requests must be finite as per PCIe specification. This register can be used to program the maximum number of 16GT/s equalization requests automatically initiated by the Endpoint. 0000: Automatic 16GT/s Equalization Request Disabled. 0001: Automatic 16GT/s Equalization request limit is 1. 0010: Automatic 16GT/s Equalization request limit is 2. 1111: Automatic 16GT/s Equalization request limit is 15,
15-12	MX8GERL	R/W	0h	The number of 8GT/s Equalization Requests must be finite as per PCIe specification. This register can be used to program the maximum number of 8GT/s equalization requests automatically initiated by the Endpoint. 0000: Automatic 8GT/s Equalization Request Disabled. 0001: Automatic 8GT/s Equalization request limit is 1. 0010: Automatic 8GT/s Equalization request limit is 2. 1111: Automatic 8GT/s Equalization request limit is 15,
11-10	RES10	R	0h	Reserved

**Table 9-1010. PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
9	QG16GT	R/W	0h	This bit can be used to program the Quiesce Guarantee bit of the TS2 in Recovery.Rcvr.Cfg state during 16GT/s Request Equalization.
8	QG8GT	R/W	0h	This bit can be used to program the Quiesce Guarantee bit of the TS2 in Recovery.Rcvr.Cfg state during 8GT/s Request Equalization.
7-6	RES6	R	0h	Reserved
5	EP16GRE	R/W	0h	Writing a 1 into this field results in the Controller to transition to Recovery. The Request Equalization bit and Equalization Request Data Rate bit in TS2 Ordered Sets will be set to 1 in Recovery.Rcvr.Cfg to request equalization at 16GTs. This bit is auto-cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. This bit is also auto-cleared when not in Gen3 or Gen4. Device Firmware must wait for the bit to be clear before any subsequent requests.
4	EP8GRE	R/W	0h	This bit can be used by Endpoint Device FW to request for 8GT/s Equalization redo. This bit can be set at any time after the Link is Up. Writing a 1 into this field results in the Controller to transition to Recovery. The Request Equalization bit in TS2 Ordered Sets will be set to 1 in Recovery.Rcvr.Cfg to request equalization at 8GTs. This bit is auto-cleared by the internal logic of the Controller after the re-training has been completed and link has reached the L0 state. This bit is also auto-cleared when not in Gen3 or Gen4. Device Firmware must wait for the bit to be clear before any subsequent retrain requests.
3	RES3	R	0h	Reserved
2-0	MXECC	R/W	0h	Controls the number of consecutive RxEqEval iterations with direction change feedback of 00s before Equalization Convergence is inferred. 0 : Infer Convergence after 1 feedback of 000000 1 : Infer Convergence after 2 feedback of 000000 2 : Infer Convergence after 3 consecutive feedback of 000000 .. 7 : Infer Convergence after 8 consecutive feedback of 000000. Note: Each lane independently counts consecutive feedback of 000000. Note: Count is reset after a non-000000 feedback on each lane.

Table 9-1011. Register Call Summary for PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register \(Offset = 0010037Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.95 PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register (Offset = 00100380h) [reset = 000B4004h]

PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 is shown in Figure 9-334 and described in Table 9-1013.

Return to the [Summary Table](#).

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN3 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen3 Equalization Phase 3.

When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen3 Equalization Phase 2.

Table 9-1012.
PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATU
S_REG_LANE0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0380h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0380h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0380h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0380h

Figure 9-334. PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R-0h						R-B40h	
23	22	21	20	19	18	17	16
LEQTXCO							
R-B40h							
15	14	13	12	11	10	9	8
LEQTXCO							
R-B40h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV		LEQTXPR		
R-0h			R-0h		R-4h		

LEGEND: R = Read Only; -n = value after reset

Table 9-1013. PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES3126	R	0h	Reserved
25-8	LEQTXCO	R	B40h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cursor Coefficient
7-5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3-0	LEQTXPR	R	4h	TX Preset agreed upon for this lane

**Table 9-1014. Register Call Summary for
PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0**

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register \(Offset = 00100380h\) \[reset = 000B4004h\]: \[0\]](#)

9.4.96 PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register (Offset = 00100384h) [reset = 000B4004h]

PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 is shown in Figure 9-335 and described in Table 9-1016.

Return to the [Summary Table](#).

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN3 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen3 Equalization Phase 3.

When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen3 Equalization Phase 2.

Table 9-1015.
PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATU
S_REG_LANE1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0384h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0384h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0384h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0384h

Figure 9-335. PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R-0h						R-B40h	
23	22	21	20	19	18	17	16
LEQTXCO							
R-B40h							
15	14	13	12	11	10	9	8
LEQTXCO							
R-B40h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV		LEQTXPR		
R-0h			R-0h		R-4h		

LEGEND: R = Read Only; -n = value after reset

Table 9-1016. PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES3126	R	0h	Reserved
25-8	LEQTXCO	R	B40h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cursor Coefficient
7-5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3-0	LEQTXPR	R	4h	TX Preset agreed upon for this lane

**Table 9-1017. Register Call Summary for
PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1**

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register \(Offset = 00100384h\) \[reset = 000B4004h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.97 PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register (Offset = 001003C0h) [reset = 00684608h]

PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 is shown in Figure 9-336 and described in Table 9-1019.

Return to the [Summary Table](#).

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN4 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen4 Equalization Phase 3.

When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen4 Equalization Phase 2.

Table 9-1018.
PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATU
S_REG_LANE0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 03C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 03C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 03C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 03C0h

Figure 9-336. PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R-0h						R-6846h	
23	22	21	20	19	18	17	16
LEQTXCO							
R-6846h							
15	14	13	12	11	10	9	8
LEQTXCO							
R-6846h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV		LEQTXPR		
R-0h			R-0h		R-8h		

LEGEND: R = Read Only; -n = value after reset

Table 9-1019. PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES3126	R	0h	Reserved
25-8	LEQTXCO	R	6846h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cursor Coefficient
7-5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3-0	LEQTXPR	R	8h	TX Preset agreed upon for this lane

**Table 9-1020. Register Call Summary for
PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0**

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register \(Offset = 001003C0h\) \[reset = 00684608h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.98 PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register (Offset = 001003C4h) [reset = 00684608h]

PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 is shown in Figure 9-337 and described in Table 9-1022.

Return to the [Summary Table](#).

This register is used to reflect the negotiated TX Preset, Coefficients at the end of GEN4 Link Equalization. When the Controller is an Endpoint, this register reflects the Preset/Coefficients applied to the Endpoint Transmitter at the end of Gen4 Equalization Phase 3.

When the Controller is an RC, this register reflects the Preset/Coefficients applied to the RC Transmitter at the end of Gen4 Equalization Phase 2.

Table 9-1021.
PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATU
S_REG_LANE1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 03C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 03C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 03C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 03C4h

Figure 9-337. PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R-0h						R-6846h	
23	22	21	20	19	18	17	16
LEQTXCO							
R-6846h							
15	14	13	12	11	10	9	8
LEQTXCO							
R-6846h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV		LEQTXPR		
R-0h			R-0h		R-8h		

LEGEND: R = Read Only; -n = value after reset

Table 9-1022. PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES3126	R	0h	Reserved
25-8	LEQTXCO	R	6846h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cursor Coefficient
7-5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3-0	LEQTXPR	R	8h	TX Preset agreed upon for this lane

**Table 9-1023. Register Call Summary for
PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1**

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register \(Offset = 001003C4h\) \[reset = 00684608h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.99 PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_AXI Register (Offset = 00100C80h) [reset = 0h]

PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_AXI is shown in Figure 9-338 and described in Table 9-1025.

Return to the [Summary Table](#).

This register contains the count of the number of ECC errors detected and corrected during reads from PCIe core AXI external RAMs.

Table 9-1024.
PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_
AXI Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C80h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C80h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C80h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C80h

Figure 9-338. PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_AXI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AXI_MASTER_DIB_CER								AXI_MASTER_RFIFO_CER							
R/W1C-0h								R/W1C-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AXI_SLAVE_WFIFO_CER								REORDER_CER							
R/W1C-0h								R/W1C-0h							

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1025. PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_AXI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	AXI_MASTER_DIB_CER	R/W1C	0h	Number of correctable errors detected while reading from the AXI Master Read Data interleave RAM. This is an 8-bit saturating counter that can be cleared by writing all 1s into it.
23-16	AXI_MASTER_RFIFO_CER	R/W1C	0h	Number of correctable errors detected while reading from the AXI master read fifo RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
15-8	AXI_SLAVE_WFIFO_CER	R/W1C	0h	Number of correctable errors detected while reading from the AXI slave write fifo RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
7-0	REORDER_CER	R/W1C	0h	Number of correctable errors detected while reading from the AXI slave reorder RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.

Table 9-1026. Register Call Summary for PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_AXI

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_ECC_CORR_ERR_COUNT_REG_AXI Register (Offset = 00100C80h) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.100 PCIe_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL0 Register (Offset = 00100C88h) [reset = X]

PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL0 is shown in Figure 9-339 and described in Table 9-1028.

Return to the [Summary Table](#).

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

Table 9-1027.
PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C88h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C88h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C88h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C88h

Figure 9-339. PCIe_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL0 Register

31	30	29	28	27	26	25	24
RESERVED				L1DLEUP	L1EM		L1DBRI
R/W-X				R/W-0h	R-0h		R/W-0h
23	22	21	20	19	18	17	16
L1XDELAY							
R/W-0h							
15	14	13	12	11	10	9	8
L1XDELAY							
R/W-0h							
7	6	5	4	3	2	1	0
L1XDELAY							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1028. PCIe_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27	L1DLEUP	R/W	0h	Pending Tlps trigger a L1 exit by default. This includes internally generated messages and internally blocked TLPs. Setting this bit changes the default behavior. This is required only for debug purpose.
26-25	L1EM	R	0h	This field shows the last entered L1 mode. This is useful for debug. bit 0 - Entry mode was ASPM. Bit 1 - Entry mode was PM. This is reset before any new L1 entry.

**Table 9-1028. PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
24	L1DBRI	R/W	0h	Before entering L1, controller internally blocks all TLP and Register Request interface entering controller. interfaces are internally unblocked while exiting L1. This field control this behavior. '1' in this field makes the controller to do not perform any blocking to interfaces. '0' makes the controller behaves normally. This is required only for debug purpose. Power shutoff feature has to be disabled while using this field.
23-0	L1XDELAY	R/W	0h	Normally L1 substate entry process is initiated immediately after LTSSM enters L1. A delay in micro-seconds can be given in this field to delay L1 substate entry process. This timeout has 0-1us margin of error. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_L1_SUBSTATE_ENTRY_DELAY

Table 9-1029. Register Call Summary for PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL0

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL0 Register \(Offset = 00100C88h\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.101 PCIe_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL1 Register (Offset = 00100C8Ch) [reset = X]

PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL1 is shown in Figure 9-340 and described in Table 9-1031.

Return to the [Summary Table](#).

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

Table 9-1030.
PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C8Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C8Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C8Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C8Ch

Figure 9-340. PCIe_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L1ER							
R-X																								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-1031. PCIe_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	L1ER	R	0h	<p>This field shows the values of possible L1 or L1-substate exit triggers. This is useful for debug. this is captured during L1 or L1-substate exit process. this field is reset during L1 entry.</p> <p>0 : CLIENT_REQ_EXIT_L1 asserted 1 : Electrical Idle exit detected at link 2 : New TLP request detected 3 : Internal request to send TLP. This includes CFG completions. internal messages. INTx messages 4 : Pending TX traffic available. This could be traffic from DMA and blocked traffic due to credits at AXI. 5 : #CLKREQ assert detected 6 : CLIENT_REQ_EXIT_L1_SUBSTATE asserted 7 : Reg Access request detected Triggers #5,6,7 are valid only with L1-substate supported configs.</p>

Table 9-1032. Register Call Summary for PCIe_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL1 Register \(Offset = 00100C8Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.102 PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2 Register (Offset = 00100C90h) [reset = X]

PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2 is shown in Figure 9-341 and described in Table 9-1034.

Return to the [Summary Table](#).

This register controls internal behavior of controller for low power operations. Adjustment of this register is not required for normal operations.

Table 9-1033.
PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C90h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C90h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C90h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C90h

Figure 9-341. PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2 Register

31	30	29	28	27	26	25	24
L1UPACR	L1CSC	L1DAET	L1TROW	L1PS	L1ERC	L1EOC	RESERVED
R/W-1h	R/W-0h	R/W-0h	R-0h	R/W-1h	R/W-0h	R/W-0h	R/W-X
23	22	21	20	19	18	17	16
L1TWROI							
R/W-0h							
15	14	13	12	11	10	9	8
L1TWROI							
R/W-0h							
7	6	5	4	3	2	1	0
L1TWROI							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1034. PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	L1UPACR	R/W	1h	Setting this field make the state machine to consider LP_CTRL_POWER_RECOVER_ACK as Client system recovery Complete ACK instead of the Controller power stable ACK. This field is ignored if LP_CTRL_BYPASS_ENABLE unset. If this field is set, L 1-substate machines expect that the client system finishes power up of the controller within power_on time in the L 1-substate capability register and Controller will be waiting in recovery state for ACK. This ensure that the PHY PLL lock and client system initialization goes on in parallel. Default value of this register can be set with the define:den_db_LP_DBG_CTRL_RECOVER_ACK_AS_CLIENT_RECOVER_ACK. Setting this field gives the best system performance.

**Table 9-1034. PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
30	L1CSC	R/W	0h	<p>L</p> <p>1-substate removes CORE_CLK.</p> <p>since the registers are implemented in core-clk, register access is not possible during L</p> <p>1-substate.</p> <p>If client can supply a slow clock to core[CORE_CLK] during L</p> <p>1-substates, APB/mgmt access is possible in L1.x.</p> <p>set this bit if client can supply slow clock to CORE_CLK when CLKREQ_IN_N is 1[de-asserted].</p> <p>If this bit is set, Controller neither wake-up from L1 or generate error response for APB access during L1.x.</p> <p>Controller behavior is undefined if register write is performed while slow clock is supplied to core_clk.</p> <p>Recommended flow is to first exit from L</p> <p>1-substate and perform register writes.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_CLIENT_SUPPLIES_SLOW_CLK_TO_CORE_DURING_L1</p>
29	L1DAET	R/W	0h	<p>L1.x turns off clocks to the controller.</p> <p>Default behavior is made to exit L1.x if Register access request is present at register interface.</p> <p>Setting this bit disables this feature.</p> <p>If this</p> <p>bit is set and CLKREQ_IN_N is 1[de-asserted], Controller responds with ERROR response</p> <p>to APB requests.</p> <p>Client can use CLIENT_EXIT_L1_SUBSTATE</p> <p>pin to trigger L1.x exit if autonomous exit is disabled for register access.</p> <p>This bit is ignored if L1 substate is disabled.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_DISABLE_AUTONOMOUS_L1_EXIT_ON_NEW_REG_REQ</p>
28	L1TROW	R	0h	<p>This is a debug status field.</p> <p>'1' in this field indicates that a timeout has occurred while waiting for RX path or OUTstanding packet IDLE conditions.</p> <p>This is cleared on new entry to L1.</p>
27	L1PS	R/W	1h	<p>This field enabled power shutoff mechanism in L1.2 state.</p> <p>This field is ignored if L1.x is not enabled.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_POWER_SHUTOFF_ENABLE</p>
26	L1ERC	R/W	0h	<p>Enables waiting for RX path IDLE condition before entering L1.x.</p> <p>This checks that all packets from</p> <p>PCIE link has reached client side before entering L1.x.</p> <p>This only a tuning register.</p> <p>Not setting this register will cause controller to enter L1.x to save power without checking this.</p> <p>controller will resume transferring RX data once it exit from L1.x state if RX buffers were not empty.</p> <p>This field is ignored if Power shutoff mechanism is enabled for L1.x and Controller will always check</p> <p>RX path idle condition before turning off internal power[with cpf flow].</p> <p>If timeout is enabled,</p> <p>controller enters L1.x without internal power shutoff after timeout.</p> <p>This bit is ignored if L1 substate is disabled.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_WAIT_FOR_RX_BUFFER_IDLE</p>

**Table 9-1034. PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
25	L1EOC	R/W	0h	<p>Enable waiting for outstanding completions before entering L1.x. Outstanding packets expected from pcie link as well as from AXI side is checked. FOR HAL configurations client has to assert PREVENT_L1x_ENTRY signal to prevent L1x entry. This only a tuning register. Not setting this register will cause controller to enter L1.x to save power without checking this. controller exit from L1.x as soon as it receives expected TLps. This field is ignored if Power shutoff mechanism is selected for L1.x and Controller will always wait for outstanding packets before turning off internal power[with cpf flow]. If timeout is enabled, controller enters L1.x without internal power shutoff after timeout. This bit is ignored if L1 substate is disabled. Power on reset value of this register can be adjusted by modifying the define <code>den_db_LP_DBG_CTRL_WAIT_FOR_OUTSTANDING_CPLS</code></p>
24	RESERVED	R/W	X	
23-0	L1TWROI	R/W	0h	<p>This field enables a timeout mechanism while waiting for RX buffers and Outstanding Pkts before turning off power. Controller enters L1 substate after timeout. A value of 0x0 disables this timeout mechanism. Controller do not select internal power shutoff if it enters L1.x with this timeout. User can give timeout in micro-seconds using this register. This field is ignored if L1 substate is disabled. Power on reset value of this register can be adjusted by modifying the define <code>den_db_LP_DBG_CTRL_RX_CPL_IDLE_CHECK_TIMEOUT</code></p>

Table 9-1035. Register Call Summary for PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_LOW_POWER_DEBUG_AND_CONTROL2 Register](#) (Offset = 00100C90h) [reset = X]: [0]
- [PCIE_CORE_LM Registers](#): [0] [1]

9.4.103 PCIE_CORE_LM_TL_INTERNAL_CONTROL Register (Offset = 00100C94h) [reset = 0h]

PCIE_CORE_LM_TL_INTERNAL_CONTROL is shown in Figure 9-342 and described in Table 9-1037.

Return to the [Summary Table](#).

This register controls internal behavior of Transaction layer of controller.
Adjustment of this register is not required for normal operations.

Table 9-1036.
PCIE_CORE_LM_TL_INTERNAL_CONTROL
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C94h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C94h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C94h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C94h

Figure 9-342. PCIE_CORE_LM_TL_INTERNAL_CONTROL Register

31	30	29	28	27	26	25	24
RES1							
R-0h							
23	22	21	20	19	18	17	16
RES1							
R-0h							
15	14	13	12	11	10	9	8
RES1							
R-0h							
7	6	5	4	3	2	1	0
RES1							ECFLR
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1037. PCIE_CORE_LM_TL_INTERNAL_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RES1	R	0h	Reserved
0	ECFLR	R/W	0h	By default controller ignores config request if a function is under going FLR. Setting this bit Makes the controller to respond with CRS response. Power on reset value of this register can be adjusted by modifying the define den_db_TL_CTRL_ENABLE_CRS_UNDER_FLR

Table 9-1038. Register Call Summary for PCIE_CORE_LM_TL_INTERNAL_CONTROL

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_TL_INTERNAL_CONTROL Register \(Offset = 00100C94h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.104 PCIE_CORE_LM_I_DTI_ATS_STATUS Register (Offset = 00100C98h) [reset = 0h]

PCIE_CORE_LM_I_DTI_ATS_STATUS is shown in [Figure 9-343](#) and described in [Table 9-1040](#).

Return to the [Summary Table](#).

This register is for reporting different error conditions/ State in DTI ATS Master

Table 9-1039. PCIE_CORE_LM_I_DTI_ATS_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C98h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C98h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C98h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C98h

Figure 9-343. PCIE_CORE_LM_I_DTI_ATS_STATUS Register

31	30	29	28	27	26	25	24
R10							
R-0h							
23	22	21	20	19	18	17	16
R10		ITAG				CONSTATE	
R-0h		R-0h				R-0h	
15	14	13	12	11	10	9	8
R12							
R-0h							
7	6	5	4	3	2	1	0
R12				ITAGTIMEOUT	INVREQIGNOR ED	NOTAG	WRONGITAG
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1040. PCIE_CORE_LM_I_DTI_ATS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R10	R	0h	Reserved
21-17	ITAG	R	0h	Itag value which timed out
16	CONSTATE	R	0h	When set indicates the DTI Master in connected state
15-4	R12	R	0h	Reserved
3	ITAGTIMEOUT	R/W1C	0h	When set indicates a timeout in one of the invalidation tags. Invalidation Tag timeout duration = INVTIMERCF * 16ns * INVTIMERCC
2	INVREQIGNORED	R/W1C	0h	When set indicates that the invalidation request is ignored internally by the DTI Master block
1	NOTAG	R/W1C	0h	When set indicates the DTI Slave returned an error for the connection request due to non availability of tags.
0	WRONGITAG	R/W1C	0h	When set indicates that the itag field is wrong in the invalidation completion message.

Table 9-1041. Register Call Summary for PCIE_CORE_LM_I_DTI_ATS_STATUS

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_DTI_ATS_STATUS Register (Offset = 00100C98h) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.105 PCIE_CORE_LM_I_DTI_ATS_CTRL Register (Offset = 00100C9Ch) [reset = 27807A12h]

PCIE_CORE_LM_I_DTI_ATS_CTRL is shown in [Figure 9-344](#) and described in [Table 9-1043](#).

Return to the [Summary Table](#).

This register is for the control of DTI ATS Master

Table 9-1042. PCIE_CORE_LM_I_DTI_ATS_CTRL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C9Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C9Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C9Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C9Ch

Figure 9-344. PCIE_CORE_LM_I_DTI_ATS_CTRL Register

31	30	29	28	27	26	25	24
R3		LDCTRL	DISCONREQ	CONREQ	INVTIMERCC		
R-0h		R/W-1h	R/W-0h	R/W-0h	R/W-78h		
23	22	21	20	19	18	17	16
INVTIMERCC				INVTIMERCF			
R/W-78h				R/W-7A12h			
15	14	13	12	11	10	9	8
INVTIMERCF							
R/W-7A12h							
7	6	5	4	3	2	1	0
INVTIMERCF							
R/W-7A12h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1043. PCIE_CORE_LM_I_DTI_ATS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	R3	R	0h	Reserved
29	LDCTRL	R/W	1h	This bit when programmed to 1 sends a disconnect request when link down reset happens and sends a connect request when link down indication bit is cleared.
28	DISCONREQ	R/W	0h	When set DTI Master triggers a disconnect sequence to the DTI Slave. This bit gets reset to 0 when the DTI master establishes a disconnection.
27	CONREQ	R/W	0h	When set DTI Master triggers a connect sequence to the DTI Slave. This bit gets reset to 0 when the DTI master establishes a connection.
26-20	INVTIMERCC	R/W	78h	This is a coarse value which the individual invalidation timers check for reporting a timeout
19-0	INVTIMERCF	R/W	7A12h	This is a master counter timeout value which triggers the invalidation tag timers to increment if an active invalidation request is present

Table 9-1044. Register Call Summary for PCIE_CORE_LM_I_DTI_ATS_CTRL

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_DTI_ATS_CTRL Register \(Offset = 00100C9Ch\) \[reset = 27807A12h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.106 PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG Register (Offset = 00100CC0h) [reset = 0h]

PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG is shown in Figure 9-345 and described in Table 9-1046.

Return to the [Summary Table](#).

Scaled Flow Control registers are implemented per VC. The VC is selected using this register.

Table 9-1045.
PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CC0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CC0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CC0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CC0h

Figure 9-345. PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES3116															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES3116												SFCVCS			
R-0h												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1046. PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES3116	R	0h	Reserved
3-0	SFCVCS	R/W	0h	The scaled flow management register is implemented per VC. However, to limit the number of registers, only one VC can be accessed at a time. This register is used to select the VC for which Scaled Flow Control Management Register is to be accessed.

Table 9-1047. Register Call Summary for
PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG Register \(Offset = 00100CC0h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.107 PCIe_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_REG Register (Offset = 00100CC4h) [reset = 555h]

PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_REG is shown in Figure 9-346 and described in Table 9-1049.

Return to the [Summary Table](#).

Scaled Flow Control management register. For multi-VC configurations, this register accesses the VC selected in Scaled Flow Control VC Select register.

Table 9-1048.
PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CC4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CC4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CC4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CC4h

Figure 9-346. PCIe_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES2				RCPCS		RCHCS		RNPPCS		RNPHCS		RPPCS		RPHCS	
R-0h				R-0h		R-0h		R-0h		R-0h		R-0h		R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES1				LCPCS		LCHCS		LNPPCS		LNPHCS		LPPCS		LPHCS	
R-0h				R/W-1h		R/W-1h		R/W-1h		R/W-1h		R/W-1h		R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1049. PCIe_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES2	R	0h	Reserved
27-26	RCPCS	R	0h	This register reflects the Completion Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.
25-24	RCHCS	R	0h	This register reflects the Completion Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.
23-22	RNPPCS	R	0h	This register reflects the Non Posted Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.
21-20	RNPHCS	R	0h	This register reflects the Non Posted Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.
19-18	RPPCS	R	0h	This register reflects the Posted Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.
17-16	RPHCS	R	0h	This register reflects the Posted Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.
15-12	RES1	R	0h	Reserved
11-10	LCPCS	R/W	1h	This register can be used to program the Completion Payload Credit Scale that will be advertised by the Controller.
9-8	LCHCS	R/W	1h	This register can be used to program the Completion Header Credit Scale that will be advertised by the Controller.
7-6	LNPPCS	R/W	1h	This register can be used to program the Non Posted Payload Credit Scale that will be advertised by the Controller.

Table 9-1049. PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	LNPHCS	R/W	1h	This register can be used to program the Non Posted Header Credit Scale that will be advertised by the Controller.
3-2	LPPCS	R/W	1h	This register can be used to program the Posted Payload Credit Scale that will be advertised by the Controller.
1-0	LPHCS	R/W	1h	This register can be used to program the Posted Header Credit Scale that will be advertised by the Controller.

Table 9-1050. Register Call Summary for PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_SCALED_FLOW_CONTROL_MGMT_REG Register \(Offset = 00100CC4h\) \[reset = 555h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.108 PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG Register (Offset = 00100CD0h) [reset = 05506417h]

PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG is shown in Figure 9-347 and described in Table 9-1052.

Return to the [Summary Table](#).

The Lane Margining at Receiver Parameters of the PHY are advertised in this Register.

Table 9-1051.
PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CD0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CD0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CD0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CD0h

Figure 9-347. PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG Register

31	30	29	28	27	26	25	24
RES		MMVO					
R-0h		R/W-5h					
23	22	21	20	19	18	17	16
MMTO						MNTS	
R/W-14h						R/W-6h	
15	14	13	12	11	10	9	8
MNTS				MNVS			
R/W-6h				R/W-20h			
7	6	5	4	3	2	1	0
MNVS			MIES	MSRM	MINDLRTS	MINDUDVS	MVS
R/W-20h			R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1052. PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RES	R	0h	Reserved
29-24	MMVO	R/W	5h	Offset from default at maximum step value as percentage of one volt. A 0 value may be reported if the vendor chooses not to report the offset.
23-18	MMTO	R/W	14h	Offset from default at maximum step value as percentage of a nominal UI at 16.0 GT/s. A 0 value may be reported if the vendor chooses not to report the offset.
17-12	MNTS	R/W	6h	Number of time steps from default [to either left or right], range must be at least +/-0.2 UI. Timing offset must increase monotonically. The number of steps in both positive [toward the end of the unit interval] and negative [toward the beginning of the unit interval] must be identical.

Table 9-1052. PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
11-5	MNVS	R/W	20h	Number of voltage steps from default [either up or down], minimum range +/-50 mV as measured by 16.0 GT/s reference equalizer Voltage offset must increase monotonically. The number of steps in both positive and negative direction from the default sample location must be identical This value is undefined if M VoltageSupported is 0b.
4	MIES	R/W	1h	1b Margining will not produce errors [change in the error rate] in data stream [error sampler is independent] 0b Margining may produce errors in the data stream
3	MSRM	R/W	0h	1b - Sampling Rates M SamplingRateVoltage, M SamplingRateTiming are supported 0b - Sample Count is supported
2	MINDLRTS	R/W	1h	1b - Independent Left/Right Timing Margining is supported 0b - Independent Left/Right Timing Margining is not supported
1	MINDUDVS	R/W	1h	1b - Independent Up Down Voltage Margining is supported 0b - Independent Up Down Voltage Margining is not supported
0	MVS	R/W	1h	1b - Voltage Margining is supported 0b - Voltage Margining is not supported

Table 9-1053. Register Call Summary for PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_MARGINING_PARAMETERS_1_REG Register \(Offset = 00100CD0h\) \[reset = 05506417h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.109 PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG Register (Offset = 00100CD4h) [reset = 0h]

PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG is shown in Figure 9-348 and described in Table 9-1055.

Return to the [Summary Table](#).

The Lane Margining at Receiver Parameters of the PHY are advertised in this Register.

Table 9-1054.
PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CD4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CD4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CD4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CD4h

Figure 9-348. PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES1																MML				MSRT				MSRV							
R-0h																R/W-0h				R/W-0h				R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1055. PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RES1	R	0h	Reserved
16-12	MML	R/W	0h	Maximum number of Lanes minus 1 that can be margined at the same time. It is recommended that this value be greater than or equal to the number of Lanes in the Link minus 1. Encoding Behavior is undefined if software attempts to margin more than MMaxLanes+1 at the same time. Note: This value is permitted to exceed the number of Lanes in the Link minus 1.
11-6	MSRT	R/W	0h	The ratio of bits tested to bits received during timing margining. A value of 0 is a ratio of 1:64 [1 bit of every 64 bits received], and a value of 63 is a ratio of 64:64 [all bits received].
5-0	MSRV	R/W	0h	The ratio of bits tested to bits received during voltage margining. A value of 0 is a ratio of 1:64 [1 bit of every 64 bits received], and a value of 63 is a ratio of 64:64 [all bits received].

Table 9-1056. Register Call Summary for PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_MARGINING_PARAMETERS_2_REG Register (Offset = 00100CD4h) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.110 PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_REG Register (Offset = 00100CD8h) [reset = 80000000h]

PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_REG is shown in Figure 9-349 and described in Table 9-1058.

Return to the [Summary Table](#).

The Lane Margining at Receiver local control fields are implemented in this Register.

Table 9-1057.
PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL
_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CD8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CD8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CD8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CD8h

Figure 9-349. PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_REG Register

31	30	29	28	27	26	25	24
WAWTC				RES			
R/W-4h				R-0h			
23	22	21	20	19	18	17	16
RES							
R-0h							
15	14	13	12	11	10	9	8
RES							
R-0h							
7	6	5	4	3	2	1	0
RES				DMSUSC		AMCNG4	MSR
R-0h				R/W-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1058. PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	WAWTC	R/W	4h	When a WriteCommitted command is issued by the Controller, the PHY must respond with a Write_Ack response. The time for which the Controller waits before timing out is controlled by this register. 000: 10us 001: 100us 010: 1ms 011: 2ms 100: 10ms [default] 101: 20ms 110: 100ms 111: No Timeout
28-3	RES	R	0h	Reserved
2	DMSUSC	R/W	0h	By default, when a Step Margin command is received, the Controller will update Lane Margin status to Margining in Progress when an Error Count update Or a Sample Count update is received from PHY. Set this bit to 1 to not update Lane Margin Status on a Sample Count update from PHY.

**Table 9-1058. PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
1	AMCNG4	R/W	0h	By default, the Controller will process a Margin Command only if it is received while in 16GT/s L0 State. If a Margin Command is received when the link is not in Gen 4-L0 state, then the command will be ignored. If this bit is set, then the Controller accepts and stores a margin command that is received when not in Gen4 L0 state. This command will be processed when the link reaches Gen4 L0 state.
0	MSR	R/W	0h	This bit can be used to reset the Margining internal registers and Margining state machines in the Controller. When asserted: [i] The State machines will be reset to their default values. [ii] All internal FIFOs will be cleared. [iii] All the P2M and M2P registers will be reset. [iv] This does not reset the Margining Configuration and Management Registers. Margining Status register will show the last recorded status. This bit will automatically self-clear after 32-CORE_CLK cycles.

Table 9-1059. Register Call Summary for PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_MARGINING_LOCAL_CONTROL_REG Register \(Offset = 00100CD8h\) \[reset = 80000000h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.111 PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_REG Register (Offset = 00100CDCh) [reset = 0h]

PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_REG is shown in Figure 9-350 and described in Table 9-1061.

Return to the [Summary Table](#).

The Lane Margining at Receiver SW Error Status fields are implemented in this Register.

Table 9-1060.
PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CDCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CDCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CDCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CDCh

Figure 9-350. PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES												ISWMCLN			
R-0h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISWMC															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1061. PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RES	R	0h	Reserved
19-16	ISWMCLN	R	0h	This field reports the Lane Number for which the Invalid command was received. 0000: Lane 0. 0001: Lane 1. and so on.. .
15-0	ISWMC	R	0h	When the Controller receives an Invalid Margining Command from SW in its configuration register, the 16-bit command is logged in this register for debug. Only the first Error is logged in this register. Bit-20 of this register has to be cleared by local firmware before another error can be logged in this field. .

Table 9-1062. Register Call Summary for PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_MARGINING_ERROR_STATUS1_REG Register (Offset = 00100CDCh) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.112 PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_REG Register (Offset = 00100CE0h) [reset = 0h]

PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_REG is shown in Figure 9-351 and described in Table 9-1064.

Return to the [Summary Table](#).

The Lane Margining at Receiver PHY Error Status fields are implemented in this Register.

Table 9-1063.
PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CE0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CE0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CE0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CE0h

Figure 9-351. PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES22										UPRLN			WAWTLN		
R-0h										R-0h			R-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WAWTLN		RES12		IPHYMCLN				IPHYMC							
R-0h		R-0h		R-0h				R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-1064. PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RES22	R	0h	Reserved
21-18	UPRLN	R	0h	This field reports the Lane Number for which the Controller received an unexpected PHY Response for Lane Margining. Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeout. 0000: Lane 0. 0001: Lane 1. and so on.. .
17-14	WAWTLN	R	0h	This field reports the Lane Number for which the Controller detected a 10ms timeout. 0000: Lane 0. 0001: Lane 1. and so on.. .
13-12	RES12	R	0h	Reserved
11-8	IPHYMCLN	R	0h	This field reports the Lane Number for which the Invalid command was received. 0000: Lane 0. 0001: Lane 1. and so on.. .

Table 9-1064. PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_REG Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
7-0	IPHYMC	R	0h	When the Controller receives an Invalid Margining Command from PHY over PIPE Interface, the 8-bit PIPE command is logged in this register for debug. Only the first Error is logged in this register. Bit-24 of this register has to be cleared by local firmware before another error can be logged in this field.

Table 9-1065. Register Call Summary for PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_MARGINING_ERROR_STATUS2_REG Register \(Offset = 00100CE0h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.113 PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER Register (Offset = 00100D00h) [reset = 0h]

PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER is shown in Figure 9-352 and described in Table 9-1067.

Return to the [Summary Table](#).

This is an extension of the Local Error and Status Register.

This register contains the status of the various events, errors and abnormal conditions in the Controller. Any of the status bits can be reset by writing a 1 into the bit position.

Unless masked by the setting of the Local Interrupt Mask 2 Register, the occurrence of any of these conditions causes the Controller to activate the LOCAL_INTERRUPT output.

Table 9-1066.
PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D00h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D00h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D00h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D00h

Figure 9-352. PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31	LEQRQIN	R13_11			R10	PTMCNTAINV	NFTSTOS
R-0h	R/W1C-0h	R-0h			R-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
UPRR	WAWTE	IPHYMCR	ISWMCR	MSIXMSKSETST	MSIXMSKCLST	MSIMSKSETST	MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1067. PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	R31	R	0h	Reserved

**Table 9-1067. PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
14	LEQRQIN	R/W1C	0h	<p>EP Mode: Indicates that the Controller hardware detected a problem with equalization and automatically requested for equalization redo at the end of the equalization.</p> <p>Controller checks for problems in Recovery.Rcvr.Lock state by comparing the Tx Coefficients agreed at end of Eq Phase2 with the Tx Coefficients received in TS1s in Recovery.Rcvr.Lock state at the end of equalization.</p> <p>Any mismatch is detected and the Request Equalization bit is set in Recovery.Rcvg.Cfg.</p> <p>This bit is set for both 8GT/s and 16GT/s equalization requests.</p> <p>[i] The Link Eq Request 8GT/s bit-5 in Link Status 2 Register will be set for 8GT/s Eq Request.</p> <p>[ii] The Link Eq Request 16.0 GT/s, bit-4 in 16.0 GT/s Status Register will be set for 16GT/s Eq Request.</p> <p>RC Mode: Indicates that the Controller received Equalization Request from downstream component.</p> <p>This bit is set for both 8GT/s and 16GT/s equalization requests.</p> <p>[i] The Link Eq Request 8GT/s bit-5 in Link Status 2 Register will be set for 8GT/s Eq Request.</p> <p>[ii] The Link Eq Request 16.0 GT/s, bit-4 in 16.0 GT/s Status Register will be set for 16GT/s Eq Request.</p>
13-11	R13_11	R	0h	Reserved
10	R10	R	0h	Reserved
9	PTMCNTAINV	R/W1C	0h	This status bit indicates that the Controller automatically invalidated PTM Context because of PCIe Link exit from L0 State.
8	NFTSTOS	R/W1C	0h	<p>This status bit indicates that a NFTS Timeout occurred.</p> <p>This could occur if the PHY failed to achieve lock on the receive data before the NFTS Timeout during Rx_L0s.FTS state.</p> <p>Local Firmware should consider increasing the advertized NFTS values if this event occurs.</p>
7	UPRR	R/W1C	0h	<p>This bit indicates that the Controller received an unexpected PHY Response for Lane Margining.</p> <p>Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of the MAC RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeou.</p>
6	WAWTE	R/W1C	0h	<p>This bit indicates that the Controller detected a 10ms timeout while waiting for Write Ack Lane Margining response from a PHY.</p> <p>The lane on which this timeout was detected is captured in bits 17:14 of the margining_error_status2_reg register.</p>
5	IPHYMCR	R/W1C	0h	<p>This bit validates the 8-bit command stored in bits [7:0] and the Lane Number stored in bits [11:8] of the margining_error_status1_reg register.</p> <p>This bit is set upon receiving the first Error.</p> <p>Local firmware must clear this bit by writing a 1 to this bit before another error can be logged.</p>

Table 9-1067. PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
4	ISWMCRCR	R/W1C	0h	This bit validates the 16-bit command stored in bits [15:0] and the Lane Number stored in bits [19:16] of the margining_error_status1_reg register. This bit is set upon receiving the first Error. Local firmware must clear this bit by writing a 1 to this bit before another error can be logged.
3	MSIXMSKSETST	R/W1C	0h	This status bit indicates that the MSIX Function Mask of any function, PF or VF, was programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Note that this is a Read Only Status bit. The MSIX Function Mask Clear status per-function is captured in the msix_function_mask_set_status_register. Firmware has to clear the per-function bits in msix_function_mask_set_status_register in order to clear this status bit and to deassert LOCAL_INTERRUPT.
2	MSIXMSKCLST	R/W1C	0h	This status bit indicates that the MSIX Function Mask of any function, PF or VF, was programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Note that this is a Read Only Status bit. The MSIX Function Mask Clear status per-function is captured in the msix_function_mask_cleared_status_register. Firmware has to clear the per-function bits in msix_function_mask_cleared_status_register in order to clear this status bit and to deassert LOCAL_INTERRUPT.
1	MSIMSKSETST	R/W1C	0h	This status bit indicates that One or More bits of MSI Mask of any function, PF or VF, was programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Note that this is a Read Only Status bit. The MSI Mask Clear status per-function is captured in the msi_mask_set_status_register. Firmware has to clear the per-function bits in msi_mask_set_status_register in order to clear this status bit and to deassert LOCAL_INTERRUPT.
0	MSIMSKCLST	R/W1C	0h	This status bit indicates that One or More bits of MSI Mask of any function, PF or VF, was programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Note that this is a Read Only Status bit. The MSI Mask Clear status per-function is captured in the msi_mask_cleared_status_register. Firmware has to clear the per-function bits in msi_mask_cleared_status_register in order to clear this status bit and to deassert LOCAL_INTERRUPT.

Table 9-1068. Register Call Summary for PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_LOCAL_ERROR_STATUS_2_REGISTER Register \(Offset = 00100D00h\) \[reset = 0h\]: \[0\]](#)

9.4.114 PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG Register (Offset = 00100D04h) [reset = 4200h]

PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG is shown in Figure 9-353 and described in Table 9-1070.

Return to the [Summary Table](#).

This is an extension of the Local Interrupt Mask Register.

This register contains a mask bit for each interrupting condition in local_error_status_2_register.

Setting the bit to 1 prevents the corresponding condition in the Local Error Status 2 Register from activating the LOCAL_INTERRUPT output.

Table 9-1069.
PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D04h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D04h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D04h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D04h

Figure 9-353. PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31	LEQRQINM	R13_11			R10	PCAIM	NFTSTOM
R-0h	R/W-1h	R-0h			R-0h	R/W-1h	R/W-0h
7	6	5	4	3	2	1	0
UPREM	WAWTEM	IPHYMEM	ISWMEM	MSIXMSKSET	MSIXMSKCL	MSIMSKSET	MSIMSKCL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1070. PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	R31	R	0h	Reserved
14	LEQRQINM	R/W	1h	Mask for Link Equalization Request Interrupt.
13-11	R13_11	R	0h	Reserved
10	R10	R	0h	Reserved
9	PCAIM	R/W	1h	Mask for PTM Context Auto Invalidated event.
8	NFTSTOM	R/W	0h	Mask for NFTS Timeout.
7	UPREM	R/W	0h	Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeout This bit can be used to Mask asserting the LOCAL_INTERRUPT output upon this error. 1: Error is masked. 0: Error is not masked.

Table 9-1070. PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	WAWTEM	R/W	0h	When a WriteCommitted command is issued by the Controller, the PHY must respond with a Write_Ack within 10ms on the PIPE Message Bus Interface. However, if the Write_Ack is not received within 10ms, the Controller reports Timeout and stops waiting for the write_ack. This bit can be used to Mask asserting the LOCAL_INTERRUPT output upon this 10ms timeout. 1: Error is masked. 0: Error is not masked.
5	IPHYMEM	R/W	0h	When the Controller receives a Margining Command from PHY over the PIPE Interface, it checks if the command is valid. The error status is logged in local_error_status_2_register. This bit can be used to Mask asserting the LOCAL_INTERRUPT output when the Invalid PHY Margining Error Status is set. 1: Error is masked. 0: Error is not masked.
4	ISWMEM	R/W	0h	When the Controller receives a Margining Command from SW in its configuration register, it checks if the command is valid. The error status is logged in local_error_status_2_register. This bit can be used to Mask asserting the LOCAL_INTERRUPT output when the Invalid SW Margining Error Status is set. 1: Error is masked. 0: Error is not masked.
3	MSIXMSKSET	R/W	0h	Mask for MSIX Function Mask Cleared Status.
2	MSIXMSKCL	R/W	0h	Mask for MSIX Function Mask Set Status.
1	MSIMSKSET	R/W	0h	Mask for MSI Mask Set Status.
0	MSIMSKCL	R/W	0h	Mask for MSI Mask Cleared Status.

Table 9-1071. Register Call Summary for PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_I_LOCAL_INTRPT_MASK_2_REG Register \(Offset = 00100D04h\) \[reset = 4200h\]: \[0\]](#)

9.4.115 PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register (Offset = 00100D10h) [reset = 0h]

PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 is shown in Figure 9-354 and described in Table 9-1073.

Return to the [Summary Table](#).

This status register has one bit per function. Each function has a 32-bit MSI Mask.
If any bit in the function's MSI Mask register is configured from 1 to 0,
then the corresponding function's status bit in this register is set.
Local Firmware needs to clear this register by writing a 1.

Table 9-1072.
PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D10h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D10h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D10h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D10h

Figure 9-354. PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31		VF15MSIMSKCLST	VF14MSIMSKCLST	VF13MSIMSKCLST	VF12MSIMSKCLST	VF11MSIMSKCLST	VF10MSIMSKCLST
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
VF9MSIMSKCLST	VF8MSIMSKCLST	VF7MSIMSKCLST	VF6MSIMSKCLST	VF5MSIMSKCLST	VF4MSIMSKCLST	VF3MSIMSKCLST	VF2MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
VF1MSIMSKCLST	VF0MSIMSKCLST	PF5MSIMSKCLST	PF4MSIMSKCLST	PF3MSIMSKCLST	PF2MSIMSKCLST	PF1MSIMSKCLST	PF0MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1073. PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R31	R	0h	Reserved
21	VF15MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF15 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1073. PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
20	VF14MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF14 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
19	VF13MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF13 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
18	VF12MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF12 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
17	VF11MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF11 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
16	VF10MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF10 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1073. PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
15	VF9MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF9 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
14	VF8MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF8 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
13	VF7MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF7 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
12	VF6MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF6 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
11	VF5MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF5 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1073. PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
10	VF4MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF4 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
9	VF3MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF3 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
8	VF2MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF2 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
7	VF1MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF1 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
6	VF0MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF0 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1073. PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
5	PF5MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF5 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
4	PF4MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF4 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
3	PF3MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF3 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
2	PF2MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF2 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
1	PF1MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF1 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1073. PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
0	PF0MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF0 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1074. Register Call Summary for PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_MSI_MASK_CLEARED_STATUS_1 Register \(Offset = 00100D10h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.116 PCIe_CORE_LM_MSI_MASK_SET_STATUS_1 Register (Offset = 00100D14h) [reset = 0h]

PCIe_CORE_LM_MSI_MASK_SET_STATUS_1 is shown in Figure 9-355 and described in Table 9-1076.

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This status register has one bit per function. Each function has a 32-bit MSI Mask. If any bit in the function's MSI Mask register is configured from 0 to 1, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Table 9-1075.
PCIe_CORE_LM_MSI_MASK_SET_STATUS_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D14h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D14h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D14h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D14h

Figure 9-355. PCIe_CORE_LM_MSI_MASK_SET_STATUS_1 Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31		VF15MSIMSKCLST	VF14MSIMSKCLST	VF13MSIMSKCLST	VF12MSIMSKCLST	VF11MSIMSKCLST	VF10MSIMSKCLST
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
VF9MSIMSKCLST	VF8MSIMSKCLST	VF7MSIMSKCLST	VF6MSIMSKCLST	VF5MSIMSKCLST	VF4MSIMSKCLST	VF3MSIMSKCLST	VF2MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
VF1MSIMSKCLST	VF0MSIMSKCLST	PF5MSIMSKCLST	PF4MSIMSKCLST	PF3MSIMSKCLST	PF2MSIMSKCLST	PF1MSIMSKCLST	PF0MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1076. PCIe_CORE_LM_MSI_MASK_SET_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R31	R	0h	Reserved
21	VF15MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF15 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1076. PCIE_CORE_LM_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	VF14MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF14 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
19	VF13MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF13 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
18	VF12MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF12 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
17	VF11MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF11 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
16	VF10MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF10 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1076. PCIE_CORE_LM_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	VF9MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF9 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
14	VF8MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF8 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
13	VF7MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF7 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
12	VF6MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF6 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
11	VF5MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF5 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1076. PCIE_CORE_LM_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	VF4MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF4 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
9	VF3MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF3 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
8	VF2MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF2 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
7	VF1MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF1 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
6	VF0MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF0 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1076. PCIE_CORE_LM_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PF5MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF5 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
4	PF4MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF4 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
3	PF3MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF3 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
2	PF2MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF2 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
1	PF1MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF1 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1076. PCIE_CORE_LM_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PF0MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF0 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1077. Register Call Summary for PCIE_CORE_LM_MSI_MASK_SET_STATUS_1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_MSI_MASK_SET_STATUS_1 Register \(Offset = 00100D14h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.117 PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register (Offset = 00100D18h) [reset = 0h]

PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 is shown in Figure 9-356 and described in Table 9-1079.

Return to the [Summary Table](#).

This status register has one bit per function. Each function has a 1-bit MSIX Function Mask. If the function's MSIX Function Mask register is configured from 1 to 0, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Table 9-1078.
PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D18h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D18h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D18h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D18h

Figure 9-356. PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31		VF15MSIXMSK CLST	VF14MSIXMSK CLST	VF13MSIXMSK CLST	VF12MSIXMSK CLST	VF11MSIXMSK CLST	VF10MSIXMSK CLST
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
VF9MSIXMSKC LST	VF8MSIXMSKC LST	VF7MSIXMSKC LST	VF6MSIXMSKC LST	VF5MSIXMSKC LST	VF4MSIXMSKC LST	VF3MSIXMSKC LST	VF2MSIXMSKC LST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
VF1MSIXMSKC LST	VF0MSIXMSKC LST	PF5MSIXMSKC LST	PF4MSIXMSKC LST	PF3MSIXMSKC LST	PF2MSIXMSKC LST	PF1MSIXMSKC LST	PF0MSIXMSKC LST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1079. PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R31	R	0h	Reserved
21	VF15MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF15 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1079. PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	VF14MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF14 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
19	VF13MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF13 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
18	VF12MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF12 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
17	VF11MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF11 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
16	VF10MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF10 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1079. PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	VF9MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF9 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
14	VF8MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF8 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
13	VF7MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF7 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
12	VF6MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF6 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
11	VF5MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF5 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1079. PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	VF4MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF4 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
9	VF3MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF3 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
8	VF2MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF2 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
7	VF1MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF1 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
6	VF0MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF0 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1079. PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PF5MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF5 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
4	PF4MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF4 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
3	PF3MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF3 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
2	PF2MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF2 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
1	PF1MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF1 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1079. PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PF0MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF0 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1080. Register Call Summary for PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register \(Offset = 00100D18h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.118 PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register (Offset = 00100D1Ch) [reset = 0h]

PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 is shown in Figure 9-357 and described in Table 9-1082.

Return to the [Summary Table](#).

This status register has one bit per function. Each function has a 1-bit MSIX Function Mask. If the function's MSIX Function Mask register is configured from 0 to 1, then the corresponding function's status bit in this register is set. Local Firmware needs to clear this register by writing a 1.

Table 9-1081.
PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D1Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D1Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D1Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D1Ch

Figure 9-357. PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31		VF15MSIXMSK CLST	VF14MSIXMSK CLST	VF13MSIXMSK CLST	VF12MSIXMSK CLST	VF11MSIXMSK CLST	VF10MSIXMSK CLST
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
VF9MSIXMSKC LST	VF8MSIXMSKC LST	VF7MSIXMSKC LST	VF6MSIXMSKC LST	VF5MSIXMSKC LST	VF4MSIXMSKC LST	VF3MSIXMSKC LST	VF2MSIXMSKC LST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
VF1MSIXMSKC LST	VF0MSIXMSKC LST	PF5MSIXMSKC LST	PF4MSIXMSKC LST	PF3MSIXMSKC LST	PF2MSIXMSKC LST	PF1MSIXMSKC LST	PF0MSIXMSKC LST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1082. PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R31	R	0h	Reserved
21	VF15MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF15 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg. Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1082. PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
20	VF14MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF14 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
19	VF13MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF13 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
18	VF12MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF12 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
17	VF11MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF11 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
16	VF10MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF10 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1082. PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15	VF9MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF9 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
14	VF8MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF8 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
13	VF7MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF7 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
12	VF6MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF6 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
11	VF5MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF5 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1082. PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
10	VF4MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF4 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
9	VF3MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF3 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
8	VF2MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF2 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
7	VF1MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF1 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
6	VF0MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF0 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1082. PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
5	PF5MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF5 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
4	PF4MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF4 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
3	PF3MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF3 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
2	PF2MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF2 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
1	PF1MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF1 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1082. PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
0	PF0MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF0 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1083. Register Call Summary for PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_MSIX_FUNCTION_MASK_SET_STATUS_1 Register \(Offset = 00100D1Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.119 PCIE_CORE_LM_I_LD_CTRL Register (Offset = 00100DA0h) [reset = 015F5E10h]

PCIE_CORE_LM_I_LD_CTRL is shown in [Figure 9-358](#) and described in [Table 9-1085](#).

Return to the [Summary Table](#).

This register is for the control of Link Down Indication Auto Reset behavior

Table 9-1084. PCIE_CORE_LM_I_LD_CTRL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DA0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DA0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DA0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DA0h

Figure 9-358. PCIE_CORE_LM_I_LD_CTRL Register

31	30	29	28	27	26	25	24
R7							AUTO_EN
R-0h							R/W-1h
23	22	21	20	19	18	17	16
LDTIMER							
R/W-005F5E10h							
15	14	13	12	11	10	9	8
LDTIMER							
R/W-005F5E10h							
7	6	5	4	3	2	1	0
LDTIMER							
R/W-005F5E10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1085. PCIE_CORE_LM_I_LD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	R7	R	0h	Reserved
24	AUTO_EN	R/W	1h	This bit when set indicates that the link down indication auto reset is enabled
23-0	LDTIMER	R/W	005F5E10h	This is a counter timeout value which triggers the internal logic to reset the link down indication bit in the AXI Configuration registers

Table 9-1086. Register Call Summary for PCIE_CORE_LM_I_LD_CTRL

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_LD_CTRL Register (Offset = 00100DA0h) [reset = 015F5E10h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.120 PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL Register (Offset = 00100DA4h) [reset = 04200000h]

PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL is shown in Figure 9-359 and described in Table 9-1088.

Return to the [Summary Table](#).

This register controls the behavior of glitch filter on the pipe rx Electrical Idle signal from the PHY/PCS. Adjustment of this register is not required for normal operations.

Table 9-1087.
PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DA4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DA4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DA4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DA4h

Figure 9-359. PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFLCP								GFLCC							
R/W-4h								R/W-20h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVGFLD													GFLD		
R-0h													R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1088. PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GFLCP	R/W	4h	This controls the glitch filter on PM Clock domain. This counter indicates the number of PM Clocks the glitch will be filtered out. The total delay of the glitch filter is calculated as [PM Clock Period * Number of PM Clocks] this delay should be same or close enough for both Core Clock[GFLCC] and PM Clock[GFLCP]
23-16	GFLCC	R/W	20h	This controls the glitch filter on CORE Clock domain. This counter indicates the number of CORE Clocks the glitch will be filtered out. The total delay of the glitch filter is calculated as [CORE Clock Period * Number of CORE Clocks] this delay should be same or close enough for both CORE Clock[GFLCC] and PM Clock[GFLCP]
15-2	RSVGFLD	R	0h	Reserved
1-0	GFLD	R/W	0h	By default controller enables glitch filter on all lanes. Setting this bit to one makes the controller to disable the glitch filter on that corresponding lanes in which the bit is set. When all bits are set to one the Glitch filter is completely bypassed, When any bit is zero glitch filter is enabled, and de-glitching is done only on the lanes that are set to zero

Table 9-1089. Register Call Summary for PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL

PCIE_CORE_LM Registers
<ul style="list-style-type: none">• PCIE_CORE_LM_RX_ELEC_IDLE_FILTER_CONTROL Register (Offset = 00100DA4h) [reset = 04200000h]: [0]• PCIE_CORE_LM Registers: [0] [1]

9.4.121 PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG Register (Offset = 00100DA8h) [reset = 1110h]

PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG is shown in Figure 9-360 and described in Table 9-1091.

Return to the [Summary Table](#).

The register bits to Control PTM operation are implemented in this Register.

Table 9-1090.
PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DA8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DA8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DA8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DA8h

Figure 9-360. PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG Register

31	30	29	28	27	26	25	24
RES29			DAINVCNT	INVPTMCNT	RES18		
R-0h			R/W-0h	R/W-0h	R-0h		
23	22	21	20	19	18	17	16
RES18						PTMRSEN	PTMRSM
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PTMRINT				PTMRFRVL			
R/W-1h				R/W-1h			
7	6	5	4	3	2	1	0
PTMRFRSC				RES2		PTMRQEN	PTMRQM
R/W-1h				R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1091. PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RES29	R	0h	Reserved
28	DAINVCNT	R/W	0h	By default, the Controller automatically invalidates PTM Context when the LTSSM exits L0 state. Client may disable this by writing a 1 to this register.
27	INVPTMCNT	R/W	0h	Client Firmware may write a 1 to this bit in order to reset the PTM Context. This is a write-only bit. Controller internally clears this bit. Read from this bit returns 0. EP Mode: Resets the PTM Request State Machine. PTM Context is Cleared. RP Mode: Resets the PTM Response State Machine. PTM Context is Cleared.
26-18	RES18	R	0h	Reserved

Table 9-1091. PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	PTMRSEN	R/W	0h	<p>EP Mode: Reserved</p> <p>RP Mode: This bit enables Controller [RP] to respond to the received PTM Requests. PTM Response/PTM ResponseD is determined by the PTM Response Mode bit. 1 : Controller automatically responds with Response/ResponseD messages. 0 : Controller does not respond for PTM Requests. [PTM Feature is Bypassed.]</p>
16	PTMRSM	R/W	0h	<p>EP Mode: Reserved.</p> <p>RP Mode: This bit is used to control the number of PTM dialogs used during each PTM Master Time Request. 1 : Two Dialog Mode - Each PTM Context will have Response followed by ResponseD. Example: Dialog 0: Request -> Response. Dialog 1: Request -> ResponseD Dialog 2: Request -> Response Dialog 3: Request -> ResponseD 0 : Continuous Dialog Mode - Each PTM Context will have Only ResponseD. Example: Dialog 0: Request -> Response. Dialog 1: Request -> ResponseD Dialog 2: Request -> ResponseD Dialog 3: Request -> ResponseD</p>
15-12	PTMRINT	R/W	1h	<p>EP Mode: In Single, Periodic Request Mode, this field is used to control the time interval [in us] between PTM Requests within a PTM Context. This represents the time the Requester State Machine waits in the WAIT_1US_STATE. 0001 - 1 0010 - 2 0011 - 3 0100 - 4 0101 - 5 0110 - 6 0111 - 7 1000 - 8 1001 - 9 .. 1111 - 15 This value is in [us].</p> <p>RP Mode: Reserved.</p>

Table 9-1091. PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	PTMRFRVL	R/W	1h	<p>EP Mode: In Periodic Request Mode, this field is used to control the time interval [value] between successive PTM Context Refresh. This represents the time the Requester State Machine waits in the VALID_PTM_CONTEXT_STATE.</p> <p>0001 - 1 0010 - 2 0011 - 3 0100 - 4 0101 - 5 0110 - 6 0111 - 7 1000 - 8 1001 - 9 1010 - 1111 Reserved</p> <p>This value is multiplied with the scale to determine the PTM Request Time Interval.</p> <p>RP Mode: Reserved.</p>
7-4	PTMRFRSC	R/W	1h	<p>EP Mode: In Periodic Request Mode, this field is used to control the time interval [scale] between successive PTM Context Refresh. This represents the time the Requester State Machine waits in the VALID_PTM_CONTEXT_STATE.</p> <p>0000 - 1 us 0001 - 10 us 0010 - 100 us 0011 - 1 ms 0100 - 10 ms 0101 - 100 ms 0110 - 1 s 0111 - 10 s 1000 - 100 s 1001 - 1111 - Reserved</p> <p>RP Mode: Reserved.</p>
3-2	RES2	R	0h	Reserved
1	PTMRQEN	R/W	0h	<p>EP Mode: This enables Endpoint to request for PTM Master Time. 1 : PTM Requests are Enabled. In Single Request Mode, this bit is used to trigger PTM dialog to obtain PTM Master time exactly once. This bit is auto-cleared after the PTM Master time is obtained. In Periodic Request Mode, this bit enables periodic requests for PTM Master Time. This bit remains set till it is cleared by the EP local firmware. 0 : PTM Requests are Disabled. [PTM Feature is Bypassed.] User may disable PTM requests in the Controller and, if required, generate requests from Client Master Interface.</p> <p>RP Mode: Reserved.</p>
0	PTMRQM	R/W	0h	<p>EP Mode: This bit controls the pattern of PTM Requests issued by the Endpoint. 0: Single Request Mode. 1: Periodic Request Mode. In Single Request Mode, Endpoint initiates one or two PTM Dialogs till the PTM Master Time is obtained. In Periodic Request Mode, Endpoint initiates PTM Dialogs and obtains PTM Master at periodic intervals. The period is programmable.</p> <p>RP Mode: Reserved.</p>

Table 9-1092. Register Call Summary for PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_LOCAL_CONTROL_REG](#) Register (Offset = 00100DA8h) [reset = 1110h]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.122 PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG Register (Offset = 00100DACH) [reset = 0h]

PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG is shown in Figure 9-361 and described in Table 9-1094.

Return to the [Summary Table](#).

The status of PTM Dialog is reflected in this Register.

Table 9-1093.
PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DACH
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DACH
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DACH
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DACH

Figure 9-361. PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES3												PTMCNST			
R-0h												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-1094. PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES3	R	0h	Reserved
3-0	PTMCNST	R	0h	Reflects the current status of the PTM Context. In EP Mode: 0000 - Invalid PTM Context 0001 - Dialog 1 PTM Request Sent 0011 - Dialog 1 PTM Response Received 0111 - Dialog 2 PTM Request Sent 1111 - Dialog 2 PTM ResponseD Received and PTM Context Valid In RP Mode: 0000 - Invalid PTM Context 0001 - Dialog 1 PTM Request Received 0011 - Dialog 1 PTM Response Sent 0111 - Dialog 2 PTM Request Received 1111 - Dialog 2 PTM ResponseD Sent and PTM Context Valid

Table 9-1095. Register Call Summary for PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM_I_PTM_LOCAL_STATUS_REG Register (Offset = 00100DACH) [reset = 0h]: [0] PCIE_CORE_LM Registers: [0] [1]

9.4.123 PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register (Offset = 00100DB0h) [reset = 0h]

PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_INDEX_REG is shown in Figure 9-362 and described in Table 9-1097.

Return to the [Summary Table](#).

The latency parameters of the PHY may be different at different speeds of operation. Hence, the Controller implements multiple instances of the PTM Latency Parameters Register, one instance for each speed of operation.

This register is used to select the speed prior to programming the speed-specific delay parameter registers.

Table 9-1096.
PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_INDEX_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DB0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DB0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DB0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DB0h

Figure 9-362. PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES4															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES4												PTMLATIN			
R-0h												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1097. PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES4	R	0h	Reserved
3-0	PTMLATIN	R/W	0h	This is used by FW to select the speed for which the Latency parameters are to be programmed. FW is required to set this to each of the supported speeds and program the corresponding latency parameters in the PTM Latency Parameters Register. 0000 - Gen1 Speed Select 0001 - Gen2 Speed Select 0010 - Gen3 Speed Select 0011 - Gen4 Speed Select Others - Reserved

Table 9-1098. Register Call Summary for PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_INDEX_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register \(Offset = 00100DB0h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.124 PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_REG Register (Offset = 00100DB4h) [reset = 0h]

PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_REG is shown in Figure 9-363 and described in Table 9-1100.

Return to the [Summary Table](#).

This register is used to define the PHY specific delay parameters.

This register also implements control bits to fine-tune timestamps that are captured by the Controller.

Internally, one instance of this register is implemented for each of the speeds supported by the Controller and is indexed by the PTM Latency Parameters Index Register.

Table 9-1099.
PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DB4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DB4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DB4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DB4h

Figure 9-363. PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXDLTUN				TXDLTUN				RES20				PTMRXLAT			
R/W-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMRXLAT						PTMTXLAT									
R/W-0h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1100. PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RXDLTUN	R/W	0h	<p>In EP Mode: This field can be used to add a fixed offset to the captured timestamps t4 and t4_tick.</p> <p>In RP Mode: This field can be used to add a fixed offset to the captured timestamps t2 and t2_tick.</p> <p>Encoding: 0000: + 0 ns 0001: + 1ns 0010: + 2ns 1111: + 15ns</p> <p>Separate value can be programmed for each supported speed of operation.</p> <p>The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding value be programmed into this register.</p>

**Table 9-1100. PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
27-24	TXDLTUN	R/W	0h	In EP Mode: This field can be used to add a fixed offset to the captured timestamps t1 and t1_tick. In RP Mode: This field can be used to add a fixed offset to the captured timestamps t3 and t3_tick. Encoding: 0000: + 0 ns 0001: + 1ns 0010: + 2ns 1111: + 15ns Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding value be programmed into this register.
23-20	RES20	R	0h	Reserved
19-10	PTMRXLAT	R/W	0h	This field should be programmed with the parameter Receive Latency in [ns] from the PHY Datasheet. Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding latency be programmed into this register.
9-0	PTMTXLAT	R/W	0h	This field should be programmed with the parameter Transmit Latency in [ns] from the PHY Datasheet. Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding latency be programmed into this register.

Table 9-1101. Register Call Summary for PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_LATENCY_PARAMETERS_REG Register \(Offset = 00100DB4h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.125 PCIE_CORE_LM_I_PTM_CONTEXT_1_REG Register (Offset = 00100DB8h) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_1_REG is shown in Figure 9-364 and described in Table 9-1103.

Return to the [Summary Table](#).

PTM Context 1 Register.

Table 9-1102.
PCIE_CORE_LM_I_PTM_CONTEXT_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DB8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DB8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DB8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DB8h

Figure 9-364. PCIE_CORE_LM_I_PTM_CONTEXT_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT1T2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1103. PCIE_CORE_LM_I_PTM_CONTEXT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT1T2	R	0h	EP Mode : Represents the lower 32-bits of timestamp t1 in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t2 in [ns] as recorded by RP.

Table 9-1104. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_1_REG

PCIE_CORE_LM Registers	
•	PCIE_CORE_LM_I_PTM_CONTEXT_1_REG Register (Offset = 00100DB8h) [reset = 0h]: [0]
•	PCIE_CORE_LM Registers: [0] [1]

9.4.126 PCIE_CORE_LM_I_PTM_CONTEXT_2_REG Register (Offset = 00100DBCh) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_2_REG is shown in Figure 9-365 and described in Table 9-1106.

Return to the [Summary Table](#).

PTM Context 2 Register.

Table 9-1105.
PCIE_CORE_LM_I_PTM_CONTEXT_2_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DBCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DBCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DBCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DBCh

Figure 9-365. PCIE_CORE_LM_I_PTM_CONTEXT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT1T2U																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1106. PCIE_CORE_LM_I_PTM_CONTEXT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT1T2U	R	0h	EP Mode : Represents the upper 32-bits of timestamp t1 in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t2 in [ns] as recorded by RP.

Table 9-1107. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_2_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_CONTEXT_2_REG Register \(Offset = 00100DBCh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.127 PCIE_CORE_LM_I_PTM_CONTEXT_3_REG Register (Offset = 00100DC0h) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_3_REG is shown in Figure 9-366 and described in Table 9-1109.

Return to the [Summary Table](#).

PTM Context 3 Register.

Table 9-1108.
PCIE_CORE_LM_I_PTM_CONTEXT_3_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DC0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DC0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DC0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DC0h

Figure 9-366. PCIE_CORE_LM_I_PTM_CONTEXT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT4T3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1109. PCIE_CORE_LM_I_PTM_CONTEXT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT4T3	R	0h	EP Mode : Represents the lower 32-bits of timestamp t4 in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t3 in [ns] as recorded by RP.

Table 9-1110. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_3_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_CONTEXT_3_REG Register \(Offset = 00100DC0h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.128 PCIE_CORE_LM_I_PTM_CONTEXT_4_REG Register (Offset = 00100DC4h) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_4_REG is shown in [Figure 9-367](#) and described in [Table 9-1112](#).

Return to the [Summary Table](#).

PTM Context 4 Register.

Table 9-1111.
PCIE_CORE_LM_I_PTM_CONTEXT_4_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DC4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DC4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DC4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DC4h

Figure 9-367. PCIE_CORE_LM_I_PTM_CONTEXT_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT4T3U																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1112. PCIE_CORE_LM_I_PTM_CONTEXT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT4T3U	R	0h	EP Mode : Represents the upper 32-bits of timestamp t4 in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t3 in [ns] as recorded by RP.

Table 9-1113. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_4_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_CONTEXT_4_REG Register \(Offset = 00100DC4h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.129 PCIE_CORE_LM_I_PTM_CONTEXT_5_REG Register (Offset = 00100DC8h) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_5_REG is shown in Figure 9-368 and described in Table 9-1115.

Return to the [Summary Table](#).

PTM Context 5 Register.

Table 9-1114.
PCIE_CORE_LM_I_PTM_CONTEXT_5_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DC8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DC8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DC8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DC8h

Figure 9-368. PCIE_CORE_LM_I_PTM_CONTEXT_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT1KT2K																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1115. PCIE_CORE_LM_I_PTM_CONTEXT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT1KT2K	R	0h	EP Mode : Represents the lower 32-bits of timestamp t1_tick in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t2_tick in [ns] as recorded by RP.

Table 9-1116. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_5_REG

PCIE_CORE_LM Registers	
•	PCIE_CORE_LM_I_PTM_CONTEXT_5_REG Register (Offset = 00100DC8h) [reset = 0h]: [0]
•	PCIE_CORE_LM Registers: [0] [1]

9.4.130 PCIE_CORE_LM_I_PTM_CONTEXT_6_REG Register (Offset = 00100DCCh) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_6_REG is shown in Figure 9-369 and described in Table 9-1118.

Return to the [Summary Table](#).

PTM Context 6 Register.

Table 9-1117.
PCIE_CORE_LM_I_PTM_CONTEXT_6_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DCCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DCCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DCCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DCCh

Figure 9-369. PCIE_CORE_LM_I_PTM_CONTEXT_6_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT1KT2KU																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1118. PCIE_CORE_LM_I_PTM_CONTEXT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT1KT2KU	R	0h	EP Mode : Represents the upper 32-bits of timestamp t1_tick in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t2_tick in [ns] as recorded by RP.

Table 9-1119. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_6_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_CONTEXT_6_REG Register \(Offset = 00100DCCh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.131 PCIE_CORE_LM_I_PTM_CONTEXT_7_REG Register (Offset = 00100DD0h) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_7_REG is shown in Figure 9-370 and described in Table 9-1121.

Return to the [Summary Table](#).

PTM Context 7 Register.

Table 9-1120.
PCIE_CORE_LM_I_PTM_CONTEXT_7_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DD0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DD0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DD0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DD0h

Figure 9-370. PCIE_CORE_LM_I_PTM_CONTEXT_7_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT4KT3K																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1121. PCIE_CORE_LM_I_PTM_CONTEXT_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT4KT3K	R	0h	EP Mode : Represents the lower 32-bits of timestamp t4_tick in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t3_tick in [ns] as recorded by RP.

Table 9-1122. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_7_REG

PCIE_CORE_LM Registers
<ul style="list-style-type: none"> PCIE_CORE_LM Registers: [0] [1] PCIE_CORE_LM_I_PTM_CONTEXT_7_REG Register (Offset = 00100DD0h) [reset = 0h]: [0]

9.4.132 PCIE_CORE_LM_I_PTM_CONTEXT_8_REG Register (Offset = 00100DD4h) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_8_REG is shown in Figure 9-371 and described in Table 9-1124.

Return to the [Summary Table](#).

PTM Context 8 Register.

Table 9-1123.
PCIE_CORE_LM_I_PTM_CONTEXT_8_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DD4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DD4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DD4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DD4h

Figure 9-371. PCIE_CORE_LM_I_PTM_CONTEXT_8_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT4KT3KU																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1124. PCIE_CORE_LM_I_PTM_CONTEXT_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT4KT3KU	R	0h	EP Mode : Represents the upper 32-bits of timestamp t4_tick in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t3_tick in [ns] as recorded by RP.

Table 9-1125. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_8_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_CONTEXT_8_REG Register \(Offset = 00100DD4h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.133 PCIE_CORE_LM_I_PTM_CONTEXT_9_REG Register (Offset = 00100DD8h) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_9_REG is shown in Figure 9-372 and described in Table 9-1127.

Return to the [Summary Table](#).

PTM Context 9 Register.

Table 9-1126.
PCIE_CORE_LM_I_PTM_CONTEXT_9_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DD8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DD8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DD8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DD8h

Figure 9-372. PCIE_CORE_LM_I_PTM_CONTEXT_9_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT3MT2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1127. PCIE_CORE_LM_I_PTM_CONTEXT_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT3MT2	R	0h	Propagation Delay. EP Mode : Represents the Propagation Delay [t3 - t2] in [ns] as received in ResponseD Message by Endpoint. RP Mode - Reserved.

Table 9-1128. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_9_REG

PCIE_CORE_LM Registers	
•	PCIE_CORE_LM_I_PTM_CONTEXT_9_REG Register (Offset = 00100DD8h) [reset = 0h]: [0]
•	PCIE_CORE_LM Registers: [0] [1]

9.4.134 PCIE_CORE_LM_I_PTM_CONTEXT_10_REG Register (Offset = 00100DDCh) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_10_REG is shown in Figure 9-373 and described in Table 9-1130.

Return to the [Summary Table](#).

PTM Context 10 Register.

Table 9-1129.
PCIE_CORE_LM_I_PTM_CONTEXT_10_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DDCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DDCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DDCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DDCh

Figure 9-373. PCIE_CORE_LM_I_PTM_CONTEXT_10_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMMSTT1T																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1130. PCIE_CORE_LM_I_PTM_CONTEXT_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMMSTT1T	R	0h	EP Mode - Represents the lower 32-bits of PTM Master Time at timestamp t1_tick in [ns] as computed by Endpoint. RP Mode - Reserved.

Table 9-1131. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_10_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_PTM_CONTEXT_10_REG Register \(Offset = 00100DDCh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.135 PCIE_CORE_LM_I_PTM_CONTEXT_11_REG Register (Offset = 00100DE0h) [reset = 0h]

PCIE_CORE_LM_I_PTM_CONTEXT_11_REG is shown in [Figure 9-374](#) and described in [Table 9-1133](#).

Return to the [Summary Table](#).

PTM Context 11 Register.

Table 9-1132.
PCIE_CORE_LM_I_PTM_CONTEXT_11_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DE0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DE0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DE0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DE0h

Figure 9-374. PCIE_CORE_LM_I_PTM_CONTEXT_11_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMMSTT1TU																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1133. PCIE_CORE_LM_I_PTM_CONTEXT_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMMSTT1TU	R	0h	EP Mode - Represents the upper 32-bits of PTM Master Time at timestamp t1_tick in [ns] as computed by Endpoint. RP Mode - Reserved.

Table 9-1134. Register Call Summary for PCIE_CORE_LM_I_PTM_CONTEXT_11_REG

PCIE_CORE_LM Registers	
•	PCIE_CORE_LM_I_PTM_CONTEXT_11_REG Register (Offset = 00100DE0h) [reset = 0h]: [0]
•	PCIE_CORE_LM Registers: [0] [1]

9.4.136 PCIe_CORE_LM_I_ASF_INTRPT_STATUS Register (Offset = 00100DECh) [reset = 0h]

PCIe_CORE_LM_I_ASF_INTRPT_STATUS is shown in Figure 9-375 and described in Table 9-1136.

Return to the [Summary Table](#).

This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_fatal or asf_nonfatal signal will be asserted. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 9-1135.
PCIe_CORE_LM_I_ASF_INTRPT_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DECh

Figure 9-375. PCIe_CORE_LM_I_ASF_INTRPT_STATUS Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRER	PROTER	TRANSTOER	CSRER	DAPER	SRUCORER	SRCORER
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1136. PCIe_CORE_LM_I_ASF_INTRPT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRER	R/W1C	0h	Integrity error interrupt
5	PROTER	R/W1C	0h	Protocol error interrupt
4	TRANSTOER	R/W1C	0h	Transaction timeouts interrupt
3	CSRER	R/W1C	0h	Configuration and status registers error interrupt
2	DAPER	R/W1C	0h	Data and address paths error interrupt
1	SRUCORER	R/W1C	0h	SRAM Uncorrectable error interrupt
0	SRCORER	R/W1C	0h	SRAM Correctable error interrupt

Table 9-1137. Register Call Summary for PCIe_CORE_LM_I_ASF_INTRPT_STATUS

PCIe_CORE_LM Registers

- [PCIe_CORE_LM_I_ASF_INTRPT_STATUS Register \(Offset = 00100DECh\) \[reset = 0h\]: \[0\]](#)
- [PCIe_CORE_LM Registers: \[0\] \[1\]](#)

9.4.137 PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS Register (Offset = 00100DF0h) [reset = 0h]

PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS is shown in Figure 9-376 and described in Table 9-1139.

Return to the [Summary Table](#).

A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 9-1138.
PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DF0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DF0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DF0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DF0h

Figure 9-376. PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRER	PROTER	TRANSTOER	CSRER	DAPER	SRUCORER	SRCORER
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1139. PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRER	R/W1C	0h	Integrity error interrupt
5	PROTER	R/W1C	0h	Protocol error interrupt
4	TRANSTOER	R/W1C	0h	Transaction timeouts interrupt
3	CSRER	R/W1C	0h	Configuration and status registers error interrupt
2	DAPER	R/W1C	0h	Data and address paths error interrupt
1	SRUCORER	R/W1C	0h	SRAM Uncorrectable error interrupt
0	SRCORER	R/W1C	0h	SRAM Correctable error interrupt

Table 9-1140. Register Call Summary for PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_INTRPT_RAW_STATUS Register \(Offset = 00100DF0h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.138 PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG Register (Offset = 00100DF4h) [reset = 3Fh]

PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG is shown in Figure 9-377 and described in Table 9-1142.

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This Register indicates which interrupt bits in the ASF interrupt status register are masked. Setting the individual bit to zero would enable the corresponding interrupt. This register does not affect the raw interrupt status register

Table 9-1141.
PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DF4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DF4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DF4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DF4h

Figure 9-377. PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRERM	PROTERM	TRANTOEM	CSRERM	DAPERM	SRUCORERM	SRCORERM
R-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1142. PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRERM	R/W	0h	Mask bit for Integrity error interrupt
5	PROTERM	R/W	1h	Mask bit for Protocol error interrupt
4	TRANTOEM	R/W	1h	Mask bit for Transaction timeouts interrupt
3	CSRERM	R/W	1h	Mask bit for Configuration and status registers error interrupt
2	DAPERM	R/W	1h	Mask bit for Data and address paths error interrupt
1	SRUCORERM	R/W	1h	Mask bit for SRAM Uncorrectable error interrupt
0	SRCORERM	R/W	1h	Mask bit for SRAM Correctable error interrupt

Table 9-1143. Register Call Summary for PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_INTRPT_MASK_REG Register \(Offset = 00100DF4h\) \[reset = 3Fh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.139 PCIE_CORE_LM_I_ASF_INTRPT_TEST Register (Offset = 00100DF8h) [reset = 0h]

PCIE_CORE_LM_I_ASF_INTRPT_TEST is shown in Figure 9-378 and described in Table 9-1145.

Return to the [Summary Table](#).

Writing one to individual bits will trigger corresponding interrupt event. The raw interrupt status will be set and the masked interrupt status will be set if the corresponding bit in the interrupt mask register is not set.

Table 9-1144. PCIE_CORE_LM_I_ASF_INTRPT_TEST Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DF8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DF8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DF8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DF8h

Figure 9-378. PCIE_CORE_LM_I_ASF_INTRPT_TEST Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRERT	PROTERT	TRANTOET	CSRERT	DAPERT	SRUCORERT	SRCORERT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1145. PCIE_CORE_LM_I_ASF_INTRPT_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRERT	R/W	0h	Test bit for Integrity error interrupt
5	PROTERT	R/W	0h	Test bit for Protocol error interrupt
4	TRANTOET	R/W	0h	Test bit for Transaction timeouts interrupt
3	CSRERT	R/W	0h	Test bit for Configuration and status registers error interrupt
2	DAPERT	R/W	0h	Test bit for Data and address paths error interrupt
1	SRUCORERT	R/W	0h	Test bit for SRAM Uncorrectable error interrupt
0	SRCORERT	R/W	0h	Test bit for SRAM Correctable error interrupt

Table 9-1146. Register Call Summary for PCIE_CORE_LM_I_ASF_INTRPT_TEST

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_INTRPT_TEST Register \(Offset = 00100DF8h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.140 PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_SEL Register (Offset = 00100DFCh) [reset = 3Fh]

PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_SEL is shown in Figure 9-379 and described in Table 9-1148.

Return to the [Summary Table](#).

This register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. For each select bit, if it is set to one then a fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered. For either a Fatal or Non Fatal Interrupt to be triggered, the corresponding mask bit of the error needs to be zero.

Table 9-1147.
PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_SEL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DFCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DFCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DFCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DFCh

Figure 9-379. PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_SEL Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRERS	PROTERS	TRANTOES	CSRERS	DAPERS	SRUCORERS	SRCORERS
R-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1148. PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRERS	R/W	0h	Enable Integrity error as Fatal
5	PROTERS	R/W	1h	Enable protocol interrupt as fatal
4	TRANTOES	R/W	1h	Enable transaction timeouts interrupt as fatal
3	CSRERS	R/W	1h	Enable configuration and status registers interrupt as fatal
2	DAPERS	R/W	1h	Enable data and address paths interrupt as fatal
1	SRUCORERS	R/W	1h	Enable SRAM Uncorrectable interrupt as fatal
0	SRCORERS	R/W	1h	Enable SRAM correctable interrupt as fatal

Table 9-1149. Register Call Summary for PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_SEL

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_INTRPT_FATAL_NONFATAL_SEL](#) Register (Offset = 00100DFCh) [reset = 3Fh]: [0]
- [PCIE_CORE_LM](#) Registers: [0] [1]

9.4.141 PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 00100E00h) [reset = 0h]

PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STATUS is shown in Figure 9-380 and described in Table 9-1151.

Return to the [Summary Table](#).

These fields are updated whenever asf_sram_corr_fault input is active

Table 9-1150.
PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STAT
US Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E00h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E00h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E00h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E00h

Figure 9-380. PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRCORFI								SRCORFADR																							
R-0h								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 9-1151. PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SRCORFI	R	0h	This ENCODING indicates which SRAM Instance has a Correctable Fault. The Encoding of the SRAM is shown in Table 26
23-0	SRCORFADR	R	0h	This indicates the address where the Correctable fault was observed.

Table 9-1152. Register Call Summary for PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STATUS

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_SRAM_CORR_FAULT_STATUS Register \(Offset = 00100E00h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.142 PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 00100E04h) [reset = 0h]

PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_STATUS is shown in Figure 9-381 and described in Table 9-1154.

Return to the [Summary Table](#).

These fields are updated whenever asf_sram_uncorr_fault input is active

Table 9-1153.
PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_S
TATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E04h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E04h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E04h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E04h

Figure 9-381. PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRUCORFI								SRUCRFADR																							
R-0h								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 9-1154. PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SRUCORFI	R	0h	This ENCODING indicates which SRAM Instance has a Uncorrectable Fault. The Encoding of the SRAM is shown in Table 26
23-0	SRUCRFADR	R	0h	This indicates the address where the Uncorrectable fault was observed.

Table 9-1155. Register Call Summary for PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_STATUS

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_SRAM_UNCORR_FAULT_STATUS Register \(Offset = 00100E04h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.143 PCIe_CORE_LM_I_ASF_SRAM_FAULT_STATSTICS Register (Offset = 00100E08h) [reset = 0h]

PCIe_CORE_LM_I_ASF_SRAM_FAULT_STATSTICS is shown in Figure 9-382 and described in Table 9-1157.

Return to the [Summary Table](#).

Note that this register clears when software writes to any field

Table 9-1156.
PCIe_CORE_LM_I_ASF_SRAM_FAULT_STATSTICS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E08h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E08h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E08h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E08h

Figure 9-382. PCIe_CORE_LM_I_ASF_SRAM_FAULT_STATSTICS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRUCORFS																SRCORFS															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1157. PCIe_CORE_LM_I_ASF_SRAM_FAULT_STATSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SRUCORFS	R/W1C	0h	Counts the number of SRAM Uncorrectable errors seen.
15-0	SRCORFS	R/W1C	0h	Counts the number of SRAM Correctable errors seen.

Table 9-1158. Register Call Summary for PCIe_CORE_LM_I_ASF_SRAM_FAULT_STATSTICS

PCIe_CORE_LM Registers

- [PCIe_CORE_LM_I_ASF_SRAM_FAULT_STATSTICS Register \(Offset = 00100E08h\) \[reset = 0h\]: \[0\]](#)
- [PCIe_CORE_LM Registers: \[0\] \[1\]](#)

9.4.144 PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL Register (Offset = 00100E0Ch) [reset = 0h]

PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL is shown in Figure 9-383 and described in Table 9-1160.

Return to the [Summary Table](#).

Register to program Transaction timeout in monitor and enable it

Table 9-1159.
PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E0Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E0Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E0Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E0Ch

Figure 9-383. PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL Register

31	30	29	28	27	26	25	24
TRTOEN	R1						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R1							
R-0h							
15	14	13	12	11	10	9	8
TRTOCTRL							
R/W-0h							
7	6	5	4	3	2	1	0
TRTOCTRL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1160. PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRTOEN	R/W	0h	Enable transaction timeout monitoring.
30-16	R1	R	0h	Reserved
15-0	TRTOCTRL	R/W	0h	Timer value to use for transaction timeout monitor. This is counted in resolution of 1 ms.

Table 9-1161. Register Call Summary for PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_TRANS_TO_CTRL Register \(Offset = 00100E0Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.145 PCIe_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK Register (Offset = 00100E10h) [reset = 0h]

PCIe_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK is shown in Figure 9-384 and described in Table 9-1163.

Return to the [Summary Table](#).

Disables the Timeout Completion Reporting

Table 9-1162.
PCIe_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E10h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E10h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E10h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E10h

Figure 9-384. PCIe_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
HPAXSLTO	HPAXMSTM	HPHLTGTOM	HPHLMSTOM	DTIDTOM	DTIUTOM	APBTOM	LMITOM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AXSLTOM	AXMSTOM	HLTGTOM	HLMSTOM	LRESPDTOM	LCFLWSTOM	LTPLCFTOM	PCOMTOM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1163. PCIe_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R31	R	0h	Reserved
15	HPAXSLTO	R/W	0h	When written to 1 Disables HP AXI Slave I/F timeout Error status reporting
14	HPAXMSTM	R/W	0h	When written to 1 Disables HP AXI Target I/F timeout Error status reporting
13	HPHLTGTOM	R/W	0h	When written to 1 Disables HP HAL Target I/F timeout Error status reporting
12	HPHLMSTOM	R/W	0h	When written to 1 Disables HP HAL Master I/F timeout Error status reporting
11	DTIDTOM	R/W	0h	When written to 1 Disables DTI DN I/F timeout Reporting Error status reporting
10	DTIUTOM	R/W	0h	When written to 1 Disables DTI UP I/F timeout Reporting Error status reporting
9	APBTOM	R/W	0h	When written to 1 Disables APB I/F timeout Error status reporting
8	LMITOM	R/W	0h	When written to 1 Disables Local Management I/F timeout Error status reporting
7	AXSLTOM	R/W	0h	When written to 1 Disables AXI Slave I/F timeout Error status reporting
6	AXMSTOM	R/W	0h	When written to 1 Disables AXI Target I/F timeout Error status reporting

Table 9-1163. PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	HLTGTOM	R/W	0h	When written to 1 Disables HAL Target I/F timeout Error status reporting
4	HLMSTOM	R/W	0h	When written to 1 Disables HAL Master I/F timeout Error status reporting
3	LRESPDTOM	R/W	0h	When written to 1 Disables LTSSM Recovery Speed Timeout Error status reporting
2	LCFLWSTOM	R/W	0h	When written to 1 Disables LTSSM Cfg Link Width Start Timeout Error status reporting
1	LTPLCFTOM	R/W	0h	When written to 1 Disables LTSSM Polling Configuration Timeout Error status reporting
0	PCOMTOM	R/W	0h	When written to 1 Disables PCIe Completion Timeout Error status reporting

Table 9-1164. Register Call Summary for PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_MASK Register \(Offset = 00100E10h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.146 PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 00100E14h) [reset = 0h]

PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS is shown in Figure 9-385 and described in Table 9-1166.

Return to the [Summary Table](#).

If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit

Table 9-1165.
PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATU
S Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E14h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E14h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E14h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E14h

Figure 9-385. PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
HPAXSLTO	HPAXMSTO	HPHLTGTO	HPHLMSTO	DTIDTO	DTIUUTO	APBTOM	LMITO
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
AXSLTO	AXMSTO	HLTGTO	HLMSTO	LRESPDTO	LCFLWSTO	LTPLCFTO	PCOMTO
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1166. PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R31	R	0h	Reserved
15	HPAXSLTO	R/W1C	0h	HP AXI Slave I/F Timeout detected waiting for a response
14	HPAXMSTO	R/W1C	0h	HP AXI Master I/F Timeout detected waiting for a response
13	HPHLTGTO	R/W1C	0h	HP HAL Target I/F Timeout detected waiting for a response
12	HPHLMSTO	R/W1C	0h	HP HAL Master I/F Timeout detected waiting for a response
11	DTIDTO	R/W1C	0h	DTI DN I/F Timeout detected waiting for a response from User
10	DTIUUTO	R/W1C	0h	DTI UP I/F Timeout detected waiting for a response from User
9	APBTOM	R/W1C	0h	APB I/F Timeout detected waiting for a response from User
8	LMITO	R/W1C	0h	Local Management I/F Timeout detected waiting for a response from User
7	AXSLTO	R/W1C	0h	AXI Slave I/F Timeout detected waiting for a response
6	AXMSTO	R/W1C	0h	AXI Master I/F Timeout detected waiting for a response
5	HLTGTO	R/W1C	0h	HAL Target I/F Timeout detected waiting for a response
4	HLMSTO	R/W1C	0h	HAL Master I/F Timeout detected waiting for a response
3	LRESPDTO	R/W1C	0h	This Indicates if the states of the LTSSM timed out . 48 ms timeout in Rec.Speed-> Detect

Table 9-1166. PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
2	LCFLWSTO	R/W1C	0h	This Indicates if the states of the LTSSM timed out . 24 ms Timeout observed in Cfg.Link.Width.Start -> Detect
1	LTPLCFTO	R/W1C	0h	This Indicates if the states of the LTSSM timed out . 48 ms Timeout observed for Polling.Cfg-> Detect
0	PCOMTO	R/W1C	0h	This indicates if a Non Posted requested did NOT receive any competition from remote device with in the completion time specified

Table 9-1167. Register Call Summary for PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_TRANS_TO_FAULT_STATUS Register \(Offset = 00100E14h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.147 PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK Register (Offset = 00100E18h) [reset = 0h]

PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK is shown in Figure 9-386 and described in Table 9-1169.

Return to the [Summary Table](#).

This control register controls if a particular protocol error is disabled from being used in the generation of the ASF Protocol Error.

Table 9-1168.
PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E18h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E18h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E18h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E18h

Figure 9-386. PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK Register

31	30	29	28	27	26	25	24
R2							
R-0h							
23	22	21	20	19	18	17	16
R2							
R-0h							
15	14	13	12	11	10	9	8
AXISLDECM	RPLTOM	RPLROLM	BADDLPM	BADTLPM	PHRCVERM	USPREQM	ECRCERRM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
MALTLPEM	RCVROVFLM	UNCPLRCM	CMPLABTM	CPLTOM	FCPROERM	POTLRCVM	DLPROTM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1169. PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R2	R	0h	RESERVED
15	AXISLDECM	R/W	0h	When set to 1 disables the AXI Slave/Decode Error status reporting
14	RPLTOM	R/W	0h	When set to 1 disables the Replay Timer Timeout status reporting
13	RPLROLM	R/W	0h	When set to 1 disables the Replay Number Rollover Detected status reporting
12	BADDLPM	R/W	0h	When set to 1 disables the Bad DLLP Detected status reporting
11	BADTLPM	R/W	0h	When set to 1 disables the Bad TLP Detected status reporting
10	PHRCVERM	R/W	0h	When set to 1 disables the PHY Receiver Error Detected status reporting
9	USPREQM	R/W	0h	When set to 1 disables the Unsupported Request Error status reporting
8	ECRCERRM	R/W	0h	When set to 1 disables the ECRC Error Detected status reporting
7	MALTLPEM	R/W	0h	When set to 1 disables the Malformed Error status reporting
6	RCVROVFLM	R/W	0h	When set to 1 disables the Receiver Overflow Error status reporting
5	UNCPLRCM	R/W	0h	When set to 1 disables the Unexpected Completion status reporting
4	CMPLABTM	R/W	0h	When set to 1 disables the Completer Abort Error status reporting
3	CPLTOM	R/W	0h	When set to 1 disables the Completion Timeout status reporting

Table 9-1169. PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
2	FCPROERM	R/W	0h	When set to 1 disables the Flow Control Protocol Error status reporting
1	POTLRCVM	R/W	0h	When set to 1 disables the Poisoned TLP received status reporting
0	DLPROTM	R/W	0h	When set to 1 disables the Data Link Layer Protocol Error status reporting

Table 9-1170. Register Call Summary for PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_MASK Register \(Offset = 00100E18h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.148 PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG Register (Offset = 00100E1Ch) [reset = 0h]

PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG is shown in Figure 9-387 and described in Table 9-1172.

Return to the [Summary Table](#).

This status register holds the different protocol errors observed by the IP.
This error is logged into this register if the corresponding bit in the ASF Protocol Fault Mask Register is not masked.

Table 9-1171.
PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E1Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E1Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E1Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E1Ch

Figure 9-387. PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG Register

31	30	29	28	27	26	25	24
R2							
R-0h							
23	22	21	20	19	18	17	16
R2							
R-0h							
15	14	13	12	11	10	9	8
AXISLVDEC	RPLTOM	RPLROL	BADDLP	BADTLPM	PHRCVER	USPREQ	ECRCERR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
MALTLPER	RCVROVFL	UNCMLRCV	CMPLABT	CPLTO	FCPROER	POTLRVCV	DLPROT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1172. PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R2	R	0h	RESERVED
15	AXISLVDEC	R/W1C	0h	This bit is set when the AXI interface sends SLVERR or DECERR to the user
14	RPLTOM	R/W1C	0h	This bit is set when the replay timer in the Data Link Layer of the Controller times out.
13	RPLROL	R/W1C	0h	This bit is set when the replay count rolls over after three re transmissions of a TLP at the Data Link Layer of the Controller.
12	BADDLP	R/W1C	0h	This bit is set when an LCRC error is detected in a received DLLP
11	BADTLPM	R/W1C	0h	This bit is set when an error is detected in a received TLP by the Data Link Layer of the Controller.
10	PHRCVER	R/W1C	0h	This bit is set when an error is detected in the receive side of the Physical Layer of the Controller
9	USPREQ	R/W1C	0h	This bit is set when the Controller has received a request from the link that it does not support.

Table 9-1172. PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ECRCERR	R/W1C	0h	This bit is set when the Controller has detected an ECRC error in a received TLP
7	MALTLPER	R/W1C	0h	This bit is set when the Controller receives a malformed TLP from the link.
6	RCVROVFL	R/W1C	0h	This bit is set when the Controller receives a TLP in violation of the receive credit currently available.
5	UNCMLRCV	R/W1C	0h	This bit is set when the Controller has received an unexpected Completion packet from the link
4	CMPLABT	R/W1C	0h	This bit is set when the Controller has returned the Completer Abort [CA] status to a request received from the link.
3	CPLTO	R/W1C	0h	This bit is set when the completion timer associated with an outstanding request times out.
2	FCPROER	R/W1C	0h	This bit is set when certain violations of the flow control protocol are detected by the Controller.
1	POTLRCV	R/W1C	0h	This bit is set when the Controller receives a poisoned TLP from the link.
0	DLPROT	R/W1C	0h	This bit is set when the Controller receives an Ack or Nak DLLP whose sequence number does not correspond to that of an unacknowledged TLP or that of the last acknowledged TLP

Table 9-1173. Register Call Summary for PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_PROTOCOL_FAULT_STATUS_REG Register \(Offset = 00100E1Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.4.149 PCIE_CORE_LM_DUAL_TL_CTRL Register (Offset = 00100E20h) [reset = X]

PCIE_CORE_LM_DUAL_TL_CTRL is shown in [Figure 9-388](#) and described in [Table 9-1175](#).

Return to the [Summary Table](#).

This register controls Dual TL functionality.

Table 9-1174. PCIE_CORE_LM_DUAL_TL_CTRL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E20h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E20h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E20h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E20h

Figure 9-388. PCIE_CORE_LM_DUAL_TL_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DTLHDRT							
R/W-2h							
15	14	13	12	11	10	9	8
DTLAW							
R/W-8h							
7	6	5	4	3	2	1	0
DTL_RSVD				DTLTS		GPLP	
R-0h				R/W-4h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1175. PCIE_CORE_LM_DUAL_TL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	DTLHDRT	R/W	2h	Defines the number of translation tokens that are reserved for the HP TL when selecting between inbound DTI requests. LP DTI requests will be stalled when the number of available tokens is equal to or smaller than this value.
15-8	DTLAW	R/W	8h	Defines the number of back to back high priority TLPs output before the arbiter gives highest priority to the low priority TL for 1 TLP. A value of '0' gives continuous highest priority to the high priority TL. The initial value of arbiter weight can be set with the define: den_db_DUAL_TL_CTRL_TX_ARB_WEIGHT
7-4	DTL_RSVD	R	0h	RESERVED

Table 9-1175. PCIE_CORE_LM_DUAL_TL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	DTLTS	R/W	4h	<p>This field set the ratio in which TAGs are shared among HP and LP TL.</p> <p>Following value pairs describes how the value of this field creates the sharing pattern.</p> <p>[0- 0% to HP TL], [1-6.25% to HP TL], [2-12.5%], [3-25%], [4-50%], [5-75%], [6-87.5%], [7-93.75.5%].</p> <p>The initial value of TAG share can be set with the define:den_db_DUAL_TL_CTRL_TAG_SHARE</p>
0	GPLP	R/W	0h	<p>By default high priority TL errors are given priority.</p> <p>If both low priority TL and high priority TL errors happen at the same time, headers from the high priority TL are captured for debug. use this bit to change the default priority.</p>

Table 9-1176. Register Call Summary for PCIE_CORE_LM_DUAL_TL_CTRL

PCIE_CORE_LM Registers

- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)
- [PCIE_CORE_LM_DUAL_TL_CTRL Register \(Offset = 00100E20h\) \[reset = X\]: \[0\]](#)

9.4.150 PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_VER_REG Register (Offset = 00100E40h) [reset = 00010BDAh]

PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_VER_REG is shown in Figure 9-389 and described in Table 9-1178.

Return to the [Summary Table](#).

This register contains two read only 16 bit hardcoded values used by the software.

Table 9-1177.
PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_V
ER_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E40h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E40h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E40h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E40h

Figure 9-389. PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_VER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTVER																MGCNM															
R-1h																R-BDAh															

LEGEND: R = Read Only; -n = value after reset

Table 9-1178. PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CNTVER	R	1h	This 16bit value is used to determine the revision number of the controller by the software
15-0	MGCNM	R	BDAh	This 16bit value is used for verification of base address by the software

Table 9-1179. Register Call Summary for PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_VER_REG

PCIE_CORE_LM Registers

- [PCIE_CORE_LM_I_ASF_MAGIC_NUM_CTRLER_VER_REG Register \(Offset = 00100E40h\) \[reset = 00010BDAh\]: \[0\]](#)
- [PCIE_CORE_LM Registers: \[0\] \[1\]](#)

9.5 PCIE_CORE_RP Registers

Table 9-1181 lists the memory-mapped registers for the PCIE_CORE_RP. All register offset addresses not listed in Table 9-1181 should be considered as reserved locations and the register contents should not be modified.

RC mode PCIE core registers

Table 9-1180. PCIE_CORE_RP Instances

Instance	Base Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0000h

Table 9-1181. PCIE_CORE_RP Registers

Offset	Acronym	Register Name	PCIE0_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE1_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE2_CORE_DBN_CFG_PCIE_CORE Physical Address
0h	PCIE_CORE_RP_I_VENDOR_ID_DEVICE_ID		0D00 0000h	0D80 0000h	0E00 0000h
4h	PCIE_CORE_RP_I_COMMAND_STATUS		0D00 0004h	0D80 0004h	0E00 0004h
8h	PCIE_CORE_RP_I_REVISION_ID_CLASS_CODE		0D00 0008h	0D80 0008h	0E00 0008h
Ch	PCIE_CORE_RP_I_BIST_HEADER_LATENCY_CACHE_LINE		0D00 000Ch	0D80 000Ch	0E00 000Ch
10h	PCIE_CORE_RP_I_RC_BAR_0		0D00 0010h	0D80 0010h	0E00 0010h
14h	PCIE_CORE_RP_I_RC_BAR_1		0D00 0014h	0D80 0014h	0E00 0014h
18h	PCIE_CORE_RP_I_PCIE_BUS_NUMBERS		0D00 0018h	0D80 0018h	0E00 0018h
1Ch	PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT		0D00 001Ch	0D80 001Ch	0E00 001Ch
20h	PCIE_CORE_RP_I_PCIE_MEM_BASE_LIMIT		0D00 0020h	0D80 0020h	0E00 0020h
24h	PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_LIMIT		0D00 0024h	0D80 0024h	0E00 0024h
28h	PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_UPPER		0D00 0028h	0D80 0028h	0E00 0028h
2Ch	PCIE_CORE_RP_I_PCIE_PREFETCH_LIMIT_UPPER		0D00 002Ch	0D80 002Ch	0E00 002Ch
30h	PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT_UPPER		0D00 0030h	0D80 0030h	0E00 0030h
34h	PCIE_CORE_RP_I_CAPABILITIES_POINTER		0D00 0034h	0D80 0034h	0E00 0034h
38h	PCIE_CORE_RP_RSVD_0E		0D00 0038h	0D80 0038h	0E00 0038h
3Ch	PCIE_CORE_RP_I_INTRPT_LINE_INTRPT_PIN		0D00 003Ch	0D80 003Ch	0E00 003Ch
80h	PCIE_CORE_RP_I_PWR_MGMT_CAP		0D00 0080h	0D80 0080h	0E00 0080h
84h	PCIE_CORE_RP_I_PWR_MGMT_CTRL_STAT_REP		0D00 0084h	0D80 0084h	0E00 0084h
90h	PCIE_CORE_RP_I_MSI_CTRL_REG		0D00 0090h	0D80 0090h	0E00 0090h
94h	PCIE_CORE_RP_I_MSI_MSG_LOW_ADDR		0D00 0094h	0D80 0094h	0E00 0094h
98h	PCIE_CORE_RP_I_MSI_MSG_HI_ADDR		0D00 0098h	0D80 0098h	0E00 0098h
9Ch	PCIE_CORE_RP_I_MSI_MSG_DATA		0D00 009Ch	0D80 009Ch	0E00 009Ch
A0h	PCIE_CORE_RP_I_MSI_MASK		0D00 00A0h	0D80 00A0h	0E00 00A0h
A4h	PCIE_CORE_RP_I_MSI_PENDING_BITS		0D00 00A4h	0D80 00A4h	0E00 00A4h
B0h	PCIE_CORE_RP_I_MSIX_CTRL		0D00 00B0h	0D80 00B0h	0E00 00B0h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
B4h	PCIE_CORE_RP_I_MSIX_TBL_OFFSET		0D00 00B4h	0D80 00B4h	0E00 00B4h
B8h	PCIE_CORE_RP_I_MSIX_PENDING_INTRP T		0D00 00B8h	0D80 00B8h	0E00 00B8h
C0h	PCIE_CORE_RP_I_PCIE_CAP_LIST		0D00 00C0h	0D80 00C0h	0E00 00C0h
C4h	PCIE_CORE_RP_I_PCIE_CAP		0D00 00C4h	0D80 00C4h	0E00 00C4h
C8h	PCIE_CORE_RP_I_PCIE_DEV_CTRL_STAT US		0D00 00C8h	0D80 00C8h	0E00 00C8h
CCh	PCIE_CORE_RP_I_LINK_CAP		0D00 00CCh	0D80 00CCh	0E00 00CCh
D0h	PCIE_CORE_RP_I_LINK_CTRL_STATUS		0D00 00D0h	0D80 00D0h	0E00 00D0h
D4h	PCIE_CORE_RP_I_SLOT_CAPABILITY		0D00 00D4h	0D80 00D4h	0E00 00D4h
D8h	PCIE_CORE_RP_I_SLOT_CTRL_STATUS		0D00 00D8h	0D80 00D8h	0E00 00D8h
DCh	PCIE_CORE_RP_I_ROOT_CTRL_CAP		0D00 00DCh	0D80 00DCh	0E00 00DCh
E0h	PCIE_CORE_RP_I_ROOT_STATUS		0D00 00E0h	0D80 00E0h	0E00 00E0h
E4h	PCIE_CORE_RP_I_PCIE_CAP_2		0D00 00E4h	0D80 00E4h	0E00 00E4h
E8h	PCIE_CORE_RP_I_PCIE_DEV_CTRL_STAT US_2		0D00 00E8h	0D80 00E8h	0E00 00E8h
ECh	PCIE_CORE_RP_I_LINK_CAP_2		0D00 00ECh	0D80 00ECh	0E00 00ECh
F0h	PCIE_CORE_RP_I_LINK_CTRL_STATUS_2		0D00 00F0h	0D80 00F0h	0E00 00F0h
100h	PCIE_CORE_RP_I_AER_ENHNCD_CAP		0D00 0100h	0D80 0100h	0E00 0100h
104h	PCIE_CORE_RP_I_UNCORR_ERR_STATU S		0D00 0104h	0D80 0104h	0E00 0104h
108h	PCIE_CORE_RP_I_UNCORR_ERR_MASK		0D00 0108h	0D80 0108h	0E00 0108h
10Ch	PCIE_CORE_RP_I_UNCORR_ERR_SEVER ITY		0D00 010Ch	0D80 010Ch	0E00 010Ch
110h	PCIE_CORE_RP_I_CORR_ERR_STATUS		0D00 0110h	0D80 0110h	0E00 0110h
114h	PCIE_CORE_RP_I_CORR_ERR_MASK		0D00 0114h	0D80 0114h	0E00 0114h
118h	PCIE_CORE_RP_I_ADV_ERR_CAP_CTL		0D00 0118h	0D80 0118h	0E00 0118h
11Ch	PCIE_CORE_RP_I_HDR_LOG_0		0D00 011Ch	0D80 011Ch	0E00 011Ch
120h	PCIE_CORE_RP_I_HDR_LOG_1		0D00 0120h	0D80 0120h	0E00 0120h
124h	PCIE_CORE_RP_I_HDR_LOG_2		0D00 0124h	0D80 0124h	0E00 0124h
128h	PCIE_CORE_RP_I_HDR_LOG_3		0D00 0128h	0D80 0128h	0E00 0128h
12Ch	PCIE_CORE_RP_I_ROOT_ERR_CMD		0D00 012Ch	0D80 012Ch	0E00 012Ch
130h	PCIE_CORE_RP_I_ROOT_ERR_STAT		0D00 0130h	0D80 0130h	0E00 0130h
134h	PCIE_CORE_RP_I_ERR_SRC_ID		0D00 0134h	0D80 0134h	0E00 0134h
138h	PCIE_CORE_RP_I_TLP_PRE_LOG_0		0D00 0138h	0D80 0138h	0E00 0138h
150h	PCIE_CORE_RP_I_DEV_SER_NUM_CAP_ HDR		0D00 0150h	0D80 0150h	0E00 0150h
154h	PCIE_CORE_RP_I_DEV_SER_NUM_0		0D00 0154h	0D80 0154h	0E00 0154h
158h	PCIE_CORE_RP_I_DEV_SER_NUM_1		0D00 0158h	0D80 0158h	0E00 0158h
300h	PCIE_CORE_RP_I_SEC_PCIE_CAP_HDR_ REG		0D00 0300h	0D80 0300h	0E00 0300h
304h	PCIE_CORE_RP_I_LINK_CONTROL3		0D00 0304h	0D80 0304h	0E00 0304h
308h	PCIE_CORE_RP_I_LANE_ERROR_STATUS		0D00 0308h	0D80 0308h	0E00 0308h
30Ch	PCIE_CORE_RP_I_LANE_EQUALIZATION_ CONTROL_0		0D00 030Ch	0D80 030Ch	0E00 030Ch
4C0h	PCIE_CORE_RP_I_VC_ENH_CAP_HEADE R_REG		0D00 04C0h	0D80 04C0h	0E00 04C0h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE1_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE2_CORE_DBN_CFG_PCIE_CORE Physical Address
4C4h	PCIE_CORE_RP_I_PORT_VC_CAP_REG_1		0D00 04C4h	0D80 04C4h	0E00 04C4h
4C8h	PCIE_CORE_RP_I_PORT_VC_CAP_REG_2		0D00 04C8h	0D80 04C8h	0E00 04C8h
4CCh	PCIE_CORE_RP_I_PORT_VC_CTRL_STS_REG		0D00 04CCh	0D80 04CCh	0E00 04CCh
4D0h	PCIE_CORE_RP_I_VC_RES_CAP_REG_0		0D00 04D0h	0D80 04D0h	0E00 04D0h
4D4h	PCIE_CORE_RP_I_VC_RES_CTRL_REG_0		0D00 04D4h	0D80 04D4h	0E00 04D4h
4D8h	PCIE_CORE_RP_I_VC_RES_STS_REG_0		0D00 04D8h	0D80 04D8h	0E00 04D8h
4DCh	PCIE_CORE_RP_I_VC_RES_CAP_REG_1		0D00 04DCh	0D80 04DCh	0E00 04DCh
4E0h	PCIE_CORE_RP_I_VC_RES_CTRL_REG_1		0D00 04E0h	0D80 04E0h	0E00 04E0h
4E4h	PCIE_CORE_RP_I_VC_RES_STS_REG_1		0D00 04E4h	0D80 04E4h	0E00 04E4h
4E8h	PCIE_CORE_RP_I_VC_RES_CAP_REG_2		0D00 04E8h	0D80 04E8h	0E00 04E8h
4ECh	PCIE_CORE_RP_I_VC_RES_CTRL_REG_2		0D00 04ECh	0D80 04ECh	0E00 04ECh
4F0h	PCIE_CORE_RP_I_VC_RES_STS_REG_2		0D00 04F0h	0D80 04F0h	0E00 04F0h
4F4h	PCIE_CORE_RP_I_VC_RES_CAP_REG_3		0D00 04F4h	0D80 04F4h	0E00 04F4h
4F8h	PCIE_CORE_RP_I_VC_RES_CTRL_REG_3		0D00 04F8h	0D80 04F8h	0E00 04F8h
4FCh	PCIE_CORE_RP_I_VC_RES_STS_REG_3		0D00 04FCh	0D80 04FCh	0E00 04FCh
900h	PCIE_CORE_RP_I_L1_PM_EXT_CAP_HDR		0D00 0900h	0D80 0900h	0E00 0900h
904h	PCIE_CORE_RP_I_L1_PM_CAP		0D00 0904h	0D80 0904h	0E00 0904h
908h	PCIE_CORE_RP_I_L1_PM_CTRL_1		0D00 0908h	0D80 0908h	0E00 0908h
90Ch	PCIE_CORE_RP_I_L1_PM_CTRL_2		0D00 090Ch	0D80 090Ch	0E00 090Ch
910h	PCIE_CORE_RP_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG		0D00 0910h	0D80 0910h	0E00 0910h
914h	PCIE_CORE_RP_I_DL_FEATURE_CAPABILITIES_REG		0D00 0914h	0D80 0914h	0E00 0914h
918h	PCIE_CORE_RP_I_DL_FEATURE_STATUS_REG		0D00 0918h	0D80 0918h	0E00 0918h
920h	PCIE_CORE_RP_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG		0D00 0920h	0D80 0920h	0E00 0920h
924h	PCIE_CORE_RP_I_MARGINING_PORT_CAPABILITIES_STATUS_REG		0D00 0924h	0D80 0924h	0E00 0924h
928h	PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG0		0D00 0928h	0D80 0928h	0E00 0928h
92Ch	PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG1		0D00 092Ch	0D80 092Ch	0E00 092Ch
9C0h	PCIE_CORE_RP_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG		0D00 09C0h	0D80 09C0h	0E00 09C0h
9C4h	PCIE_CORE_RP_I_PL_16GTS_CAPABILITIES_REG		0D00 09C4h	0D80 09C4h	0E00 09C4h
9C8h	PCIE_CORE_RP_I_PL_16GTS_CONTROL_REG		0D00 09C8h	0D80 09C8h	0E00 09C8h
9CCh	PCIE_CORE_RP_I_PL_16GTS_STATUS_REG		0D00 09CCh	0D80 09CCh	0E00 09CCh
9D0h	PCIE_CORE_RP_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG		0D00 09D0h	0D80 09D0h	0E00 09D0h
9D4h	PCIE_CORE_RP_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG		0D00 09D4h	0D80 09D4h	0E00 09D4h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
9D8h	PCIE_CORE_RP_I_PL_16GTS_SECOND_R ETIMER_DATA_PARITY_MISMATCH_STAT US_REG		0D00 09D8h	0D80 09D8h	0E00 09D8h
9DCh	PCIE_CORE_RP_I_PL_16GTS_RESERVED _REG		0D00 09DCh	0D80 09DCh	0E00 09DCh
9E0h	PCIE_CORE_RP_I_PL_16GTS_LANE_EQU ALIZATION_CONTROL_REG0		0D00 09E0h	0D80 09E0h	0E00 09E0h
A20h	PCIE_CORE_RP_I_PTM_EXTENDED_CAP ABILITY_HEADER_REG		0D00 0A20h	0D80 0A20h	0E00 0A20h
A24h	PCIE_CORE_RP_I_PTM_CAPABILITIES_R EG		0D00 0A24h	0D80 0A24h	0E00 0A24h
A28h	PCIE_CORE_RP_I_PTM_CONTROL_REG		0D00 0A28h	0D80 0A28h	0E00 0A28h
00100000h	PCIE_CORE_RP_I_PL_CONFIG_0_REG		0D10 0000h	0D90 0000h	0E10 0000h
00100004h	PCIE_CORE_RP_I_PL_CONFIG_1_REG		0D10 0004h	0D90 0004h	0E10 0004h
00100008h	PCIE_CORE_RP_I_DLL_TMR_CONFIG_RE G		0D10 0008h	0D90 0008h	0E10 0008h
0010000Ch	PCIE_CORE_RP_I_RCV_CRED_LIM_0_RE G		0D10 000Ch	0D90 000Ch	0E10 000Ch
00100010h	PCIE_CORE_RP_I_RCV_CRED_LIM_1_RE G		0D10 0010h	0D90 0010h	0E10 0010h
00100014h	PCIE_CORE_RP_I_TRANSM_CRED_LIM_0 _REG		0D10 0014h	0D90 0014h	0E10 0014h
00100018h	PCIE_CORE_RP_I_TRANSM_CRED_LIM_1 _REG		0D10 0018h	0D90 0018h	0E10 0018h
0010001Ch	PCIE_CORE_RP_I_TRANSM_CRED_UPDA TE_INT_CONFIG_0_REG		0D10 001Ch	0D90 001Ch	0E10 001Ch
00100020h	PCIE_CORE_RP_I_TRANSM_CRED_UPDA TE_INT_CONFIG_1_REG		0D10 0020h	0D90 0020h	0E10 0020h
00100024h	PCIE_CORE_RP_I_L0S_TIMEOUT_LIMIT_ REG		0D10 0024h	0D90 0024h	0E10 0024h
00100028h	PCIE_CORE_RP_I_TRANSMIT_TLP_COUN T_REG		0D10 0028h	0D90 0028h	0E10 0028h
0010002Ch	PCIE_CORE_RP_I_TRANSMIT_TLP_PAYL OAD_DWORD_COUNT_REG		0D10 002Ch	0D90 002Ch	0E10 002Ch
00100030h	PCIE_CORE_RP_I_RECEIVE_TLP_COUNT _REG		0D10 0030h	0D90 0030h	0E10 0030h
00100034h	PCIE_CORE_RP_I_RECEIVE_TLP_PAYLO AD_DWORD_COUNT_REG		0D10 0034h	0D90 0034h	0E10 0034h
00100038h	PCIE_CORE_RP_I_COMPLN_TMOUT_LIM _0_REG		0D10 0038h	0D90 0038h	0E10 0038h
0010003Ch	PCIE_CORE_RP_I_COMPLN_TMOUT_LIM _1_REG		0D10 003Ch	0D90 003Ch	0E10 003Ch
00100040h	PCIE_CORE_RP_I_L1_ST_REENTRY_DEL AY_REG		0D10 0040h	0D90 0040h	0E10 0040h
00100044h	PCIE_CORE_RP_I_VENDOR_ID_REG		0D10 0044h	0D90 0044h	0E10 0044h
00100048h	PCIE_CORE_RP_I_ASPM_L1_ENTRY_TM OUT_DELAY_REG		0D10 0048h	0D90 0048h	0E10 0048h
0010004Ch	PCIE_CORE_RP_I_PME_TURNOFF_ACK_ DELAY_REG		0D10 004Ch	0D90 004Ch	0E10 004Ch
00100050h	PCIE_CORE_RP_I_LINKWIDTH_CONTROL _REG		0D10 0050h	0D90 0050h	0E10 0050h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00100070h	PCIE_CORE_RP_I_MULTI_VC_CONROL_REG		0D10 0070h	0D90 0070h	0E10 0070h
00100074h	PCIE_CORE_RP_I_SRIS_CONTROL_REG		0D10 0074h	0D90 0074h	0E10 0074h
00100080h	PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC1		0D10 0080h	0D90 0080h	0E10 0080h
00100084h	PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC1		0D10 0084h	0D90 0084h	0E10 0084h
00100088h	PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC1		0D10 0088h	0D90 0088h	0E10 0088h
0010008Ch	PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC1		0D10 008Ch	0D90 008Ch	0E10 008Ch
00100090h	PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC2		0D10 0090h	0D90 0090h	0E10 0090h
00100094h	PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC2		0D10 0094h	0D90 0094h	0E10 0094h
00100098h	PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC2		0D10 0098h	0D90 0098h	0E10 0098h
0010009Ch	PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC2		0D10 009Ch	0D90 009Ch	0E10 009Ch
001000A0h	PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC3		0D10 00A0h	0D90 00A0h	0E10 00A0h
001000A4h	PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC3		0D10 00A4h	0D90 00A4h	0E10 00A4h
001000A8h	PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC3		0D10 00A8h	0D90 00A8h	0E10 00A8h
001000ACh	PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC3		0D10 00ACh	0D90 00ACh	0E10 00ACh
001000F0h	PCIE_CORE_RP_I_FC_INIT_DELAY_REG		0D10 00F0h	0D90 00F0h	0E10 00F0h
00100100h	PCIE_CORE_RP_I_SHDW_HDR_LOG_0_REG		0D10 0100h	0D90 0100h	0E10 0100h
00100104h	PCIE_CORE_RP_I_SHDW_HDR_LOG_1_REG		0D10 0104h	0D90 0104h	0E10 0104h
00100108h	PCIE_CORE_RP_I_SHDW_HDR_LOG_2_REG		0D10 0108h	0D90 0108h	0E10 0108h
0010010Ch	PCIE_CORE_RP_I_SHDW_HDR_LOG_3_REG		0D10 010Ch	0D90 010Ch	0E10 010Ch
00100110h	PCIE_CORE_RP_I_SHDW_FUNC_NUM_REG		0D10 0110h	0D90 0110h	0E10 0110h
00100114h	PCIE_CORE_RP_I_SHDW_UR_ERR_REG		0D10 0114h	0D90 0114h	0E10 0114h
00100140h	PCIE_CORE_RP_I_PM_CLK_FREQUENCY_REG		0D10 0140h	0D90 0140h	0E10 0140h
00100144h	PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN1_REG		0D10 0144h	0D90 0144h	0E10 0144h
00100148h	PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN2_REG		0D10 0148h	0D90 0148h	0E10 0148h
0010014Ch	PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN3_REG		0D10 014Ch	0D90 014Ch	0E10 014Ch
00100150h	PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN4_REG		0D10 0150h	0D90 0150h	0E10 0150h
00100158h	PCIE_CORE_RP_I_VENDOR_DEFINED_MESSAGE_TAG_REG		0D10 0158h	0D90 0158h	0E10 0158h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00100200h	PCIE_CORE_RP_I_NEGOTIATED_LANE_M AP_REG		0D10 0200h	0D90 0200h	0E10 0200h
00100204h	PCIE_CORE_RP_I_RECEIVE_FTS_COUNT _REG		0D10 0204h	0D90 0204h	0E10 0204h
00100208h	PCIE_CORE_RP_I_DEBUG_MUX_CONTR OL_REG		0D10 0208h	0D90 0208h	0E10 0208h
0010020Ch	PCIE_CORE_RP_I_LOCAL_ERROR_STATU S_REGISTER		0D10 020Ch	0D90 020Ch	0E10 020Ch
00100210h	PCIE_CORE_RP_I_LOCAL_INTRPT_MASK _REG		0D10 0210h	0D90 0210h	0E10 0210h
00100214h	PCIE_CORE_RP_I_LCRC_ERR_COUNT_R EG		0D10 0214h	0D90 0214h	0E10 0214h
00100218h	PCIE_CORE_RP_I_ECC_CORR_ERR_COU NT_REG		0D10 0218h	0D90 0218h	0E10 0218h
0010021Ch	PCIE_CORE_RP_I_LTR_SNOOP_LAT_REG		0D10 021Ch	0D90 021Ch	0E10 021Ch
00100220h	PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_R EG		0D10 0220h	0D90 0220h	0E10 0220h
00100224h	PCIE_CORE_RP_I_PME_SERVICE_TIMEO UT_DELAY_REG		0D10 0224h	0D90 0224h	0E10 0224h
00100228h	PCIE_CORE_RP_I_ROOT_PORT_REQUES TOR_ID_REG		0D10 0228h	0D90 0228h	0E10 0228h
0010022Ch	PCIE_CORE_RP_I_EP_BUS_DEVICE_NUM BER_REG		0D10 022Ch	0D90 022Ch	0E10 022Ch
00100234h	PCIE_CORE_RP_I_DEBUG_MUX_CONTR OL_2_REG		0D10 0234h	0D90 0234h	0E10 0234h
00100238h	PCIE_CORE_RP_I_PHY_STATUS_1_REG		0D10 0238h	0D90 0238h	0E10 0238h
00100240h	PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_ REG		0D10 0240h	0D90 0240h	0E10 0240h
00100244h	PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_ REG		0D10 0244h	0D90 0244h	0E10 0244h
00100248h	PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_ REG		0D10 0248h	0D90 0248h	0E10 0248h
0010024Ch	PCIE_CORE_RP_I_PF_1_BAR_CONFIG_1_ REG		0D10 024Ch	0D90 024Ch	0E10 024Ch
00100250h	PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_ REG		0D10 0250h	0D90 0250h	0E10 0250h
00100254h	PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_ REG		0D10 0254h	0D90 0254h	0E10 0254h
00100258h	PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_ REG		0D10 0258h	0D90 0258h	0E10 0258h
0010025Ch	PCIE_CORE_RP_I_PF_3_BAR_CONFIG_1_ REG		0D10 025Ch	0D90 025Ch	0E10 025Ch
00100260h	PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_ REG		0D10 0260h	0D90 0260h	0E10 0260h
00100264h	PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_ REG		0D10 0264h	0D90 0264h	0E10 0264h
00100268h	PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_ REG		0D10 0268h	0D90 0268h	0E10 0268h
0010026Ch	PCIE_CORE_RP_I_PF_5_BAR_CONFIG_1_ REG		0D10 026Ch	0D90 026Ch	0E10 026Ch
00100280h	PCIE_CORE_RP_I_PF_0_VF_BAR_CONFI G_0_REG		0D10 0280h	0D90 0280h	0E10 0280h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE1_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE2_CORE_DBN_CFG_PCIE_CORE Physical Address
00100284h	PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_1_REG		0D10 0284h	0D90 0284h	0E10 0284h
00100288h	PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG		0D10 0288h	0D90 0288h	0E10 0288h
0010028Ch	PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_1_REG		0D10 028Ch	0D90 028Ch	0E10 028Ch
00100290h	PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG		0D10 0290h	0D90 0290h	0E10 0290h
00100294h	PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_1_REG		0D10 0294h	0D90 0294h	0E10 0294h
00100298h	PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG		0D10 0298h	0D90 0298h	0E10 0298h
0010029Ch	PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_1_REG		0D10 029Ch	0D90 029Ch	0E10 029Ch
001002A0h	PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG		0D10 02A0h	0D90 02A0h	0E10 02A0h
001002A4h	PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_1_REG		0D10 02A4h	0D90 02A4h	0E10 02A4h
001002A8h	PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG		0D10 02A8h	0D90 02A8h	0E10 02A8h
001002ACh	PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_1_REG		0D10 02ACh	0D90 02ACh	0E10 02ACh
001002C0h	PCIE_CORE_RP_I_PF_CONFIG_REG		0D10 02C0h	0D90 02C0h	0E10 02C0h
00100300h	PCIE_CORE_RP_I_RC_BAR_CONFIG_REG		0D10 0300h	0D90 0300h	0E10 0300h
00100360h	PCIE_CORE_RP_I_GEN3_DEFAULT_PRESET_REG		0D10 0360h	0D90 0360h	0E10 0360h
00100364h	PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG		0D10 0364h	0D90 0364h	0E10 0364h
00100368h	PCIE_CORE_RP_I_PIPE_FIFO_LATENCY_CTRL_REG		0D10 0368h	0D90 0368h	0E10 0368h
00100374h	PCIE_CORE_RP_I_GEN4_DEFAULT_PRESET_REG		0D10 0374h	0D90 0374h	0E10 0374h
00100378h	PCIE_CORE_RP_I_PHY_CONFIG_REG3		0D10 0378h	0D90 0378h	0E10 0378h
0010037Ch	PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_CTRL_REG		0D10 037Ch	0D90 037Ch	0E10 037Ch
00100380h	PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0		0D10 0380h	0D90 0380h	0E10 0380h
00100384h	PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1		0D10 0384h	0D90 0384h	0E10 0384h
001003C0h	PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0		0D10 03C0h	0D90 03C0h	0E10 03C0h
001003C4h	PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1		0D10 03C4h	0D90 03C4h	0E10 03C4h
00100C80h	PCIE_CORE_RP_I_ECC_CORR_ERR_COUNTER_REG_AXI		0D10 0C80h	0D90 0C80h	0E10 0C80h
00100C88h	PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL0		0D10 0C88h	0D90 0C88h	0E10 0C88h
00100C8Ch	PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL1		0D10 0C8Ch	0D90 0C8Ch	0E10 0C8Ch
00100C90h	PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2		0D10 0C90h	0D90 0C90h	0E10 0C90h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00100C94h	PCIE_CORE_RP_TL_INTERNAL_CONTRO L		0D10 0C94h	0D90 0C94h	0E10 0C94h
00100C98h	PCIE_CORE_RP_I_DTI_ATS_STATUS		0D10 0C98h	0D90 0C98h	0E10 0C98h
00100C9Ch	PCIE_CORE_RP_I_DTI_ATS_CTRL		0D10 0C9Ch	0D90 0C9Ch	0E10 0C9Ch
00100CC0h	PCIE_CORE_RP_I_SCALED_FLOW_CONT ROL_MGMT_VC_SELECT_REG		0D10 0CC0h	0D90 0CC0h	0E10 0CC0h
00100CC4h	PCIE_CORE_RP_I_SCALED_FLOW_CONT ROL_MGMT_REG		0D10 0CC4h	0D90 0CC4h	0E10 0CC4h
00100CD0h	PCIE_CORE_RP_I_MARGINING_PARAMET ERS_1_REG		0D10 0CD0h	0D90 0CD0h	0E10 0CD0h
00100CD4h	PCIE_CORE_RP_I_MARGINING_PARAMET ERS_2_REG		0D10 0CD4h	0D90 0CD4h	0E10 0CD4h
00100CD8h	PCIE_CORE_RP_I_MARGINING_LOCAL_C ONTROL_REG		0D10 0CD8h	0D90 0CD8h	0E10 0CD8h
00100CDCh	PCIE_CORE_RP_I_MARGINING_ERROR_ STATUS1_REG		0D10 0CDCh	0D90 0CDCh	0E10 0CDCh
00100CE0h	PCIE_CORE_RP_I_MARGINING_ERROR_ STATUS2_REG		0D10 0CE0h	0D90 0CE0h	0E10 0CE0h
00100D00h	PCIE_CORE_RP_I_LOCAL_ERROR_STATU S_2_REGISTER		0D10 0D00h	0D90 0D00h	0E10 0D00h
00100D04h	PCIE_CORE_RP_I_LOCAL_INTRPT_MASK _2_REG		0D10 0D04h	0D90 0D04h	0E10 0D04h
00100D10h	PCIE_CORE_RP_MSI_MASK_CLEARED_S TATUS_1		0D10 0D10h	0D90 0D10h	0E10 0D10h
00100D14h	PCIE_CORE_RP_MSI_MASK_SET_STATU S_1		0D10 0D14h	0D90 0D14h	0E10 0D14h
00100D18h	PCIE_CORE_RP_MSIX_FUNCTION_MASK _CLEARED_STATUS_1		0D10 0D18h	0D90 0D18h	0E10 0D18h
00100D1Ch	PCIE_CORE_RP_MSIX_FUNCTION_MASK _SET_STATUS_1		0D10 0D1Ch	0D90 0D1Ch	0E10 0D1Ch
00100DA0h	PCIE_CORE_RP_I_LD_CTRL		0D10 0DA0h	0D90 0DA0h	0E10 0DA0h
00100DA4h	PCIE_CORE_RP_RX_ELEC_IDLE_FILTER_ CONTROL		0D10 0DA4h	0D90 0DA4h	0E10 0DA4h
00100DA8h	PCIE_CORE_RP_I_PTM_LOCAL_CONTRO L_REG		0D10 0DA8h	0D90 0DA8h	0E10 0DA8h
00100DACH	PCIE_CORE_RP_I_PTM_LOCAL_STATUS_ REG		0D10 0DACH	0D90 0DACH	0E10 0DACH
00100DB0h	PCIE_CORE_RP_I_PTM_LATENCY_PARA METERS_INDEX_REG		0D10 0DB0h	0D90 0DB0h	0E10 0DB0h
00100DB4h	PCIE_CORE_RP_I_PTM_LATENCY_PARA METERS_REG		0D10 0DB4h	0D90 0DB4h	0E10 0DB4h
00100DB8h	PCIE_CORE_RP_I_PTM_CONTEXT_1_RE G		0D10 0DB8h	0D90 0DB8h	0E10 0DB8h
00100DBCh	PCIE_CORE_RP_I_PTM_CONTEXT_2_RE G		0D10 0DBCh	0D90 0DBCh	0E10 0DBCh
00100DC0h	PCIE_CORE_RP_I_PTM_CONTEXT_3_RE G		0D10 0DC0h	0D90 0DC0h	0E10 0DC0h
00100DC4h	PCIE_CORE_RP_I_PTM_CONTEXT_4_RE G		0D10 0DC4h	0D90 0DC4h	0E10 0DC4h
00100DC8h	PCIE_CORE_RP_I_PTM_CONTEXT_5_RE G		0D10 0DC8h	0D90 0DC8h	0E10 0DC8h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00100DCCh	PCIE_CORE_RP_I_PTM_CONTEXT_6_RE G		0D10 0DCCh	0D90 0DCCh	0E10 0DCCh
00100DD0h	PCIE_CORE_RP_I_PTM_CONTEXT_7_RE G		0D10 0DD0h	0D90 0DD0h	0E10 0DD0h
00100DD4h	PCIE_CORE_RP_I_PTM_CONTEXT_8_RE G		0D10 0DD4h	0D90 0DD4h	0E10 0DD4h
00100DD8h	PCIE_CORE_RP_I_PTM_CONTEXT_9_RE G		0D10 0DD8h	0D90 0DD8h	0E10 0DD8h
00100DDCh	PCIE_CORE_RP_I_PTM_CONTEXT_10_RE G		0D10 0DDCh	0D90 0DDCh	0E10 0DDCh
00100DE0h	PCIE_CORE_RP_I_PTM_CONTEXT_11_RE G		0D10 0DE0h	0D90 0DE0h	0E10 0DE0h
00100DECh	PCIE_CORE_RP_I_ASF_INTRPT_STATUS		0D10 0DECh	0D90 0DECh	0E10 0DECh
00100DF0h	PCIE_CORE_RP_I_ASF_INTRPT_RAW_ST ATUS		0D10 0DF0h	0D90 0DF0h	0E10 0DF0h
00100DF4h	PCIE_CORE_RP_I_ASF_INTRPT_MASK_R EG		0D10 0DF4h	0D90 0DF4h	0E10 0DF4h
00100DF8h	PCIE_CORE_RP_I_ASF_INTRPT_TEST		0D10 0DF8h	0D90 0DF8h	0E10 0DF8h
00100DFCh	PCIE_CORE_RP_I_ASF_INTRPT_FATAL_N ONFATAL_SEL		0D10 0DFCh	0D90 0DFCh	0E10 0DFCh
00100E00h	PCIE_CORE_RP_I_ASF_SRAM_CORR_FA ULT_STATUS		0D10 0E00h	0D90 0E00h	0E10 0E00h
00100E04h	PCIE_CORE_RP_I_ASF_SRAM_UNCORR_ FAULT_STATUS		0D10 0E04h	0D90 0E04h	0E10 0E04h
00100E08h	PCIE_CORE_RP_I_ASF_SRAM_FAULT_ST ATSTICS		0D10 0E08h	0D90 0E08h	0E10 0E08h
00100E0Ch	PCIE_CORE_RP_I_ASF_TRANS_TO_CTRL		0D10 0E0Ch	0D90 0E0Ch	0E10 0E0Ch
00100E10h	PCIE_CORE_RP_I_ASF_TRANS_TO_FAUL T_MASK		0D10 0E10h	0D90 0E10h	0E10 0E10h
00100E14h	PCIE_CORE_RP_I_ASF_TRANS_TO_FAUL T_STATUS		0D10 0E14h	0D90 0E14h	0E10 0E14h
00100E18h	PCIE_CORE_RP_I_ASF_PROTOCOL_FAUL T_MASK		0D10 0E18h	0D90 0E18h	0E10 0E18h
00100E1Ch	PCIE_CORE_RP_I_ASF_PROTOCOL_FAUL T_STATUS_REG		0D10 0E1Ch	0D90 0E1Ch	0E10 0E1Ch
00100E20h	PCIE_CORE_RP_DUAL_TL_CTRL		0D10 0E20h	0D90 0E20h	0E10 0E20h
00100E40h	PCIE_CORE_RP_I_ASF_MAGIC_NUM_CT ROLLER_VER_REG		0D10 0E40h	0D90 0E40h	0E10 0E40h
00400000h	PCIE_CORE_RP_ADDR0		0D40 0000h	0DC0 0000h	0E40 0000h
00400004h	PCIE_CORE_RP_ADDR1		0D40 0004h	0DC0 0004h	0E40 0004h
00400008h	PCIE_CORE_RP_DESC0		0D40 0008h	0DC0 0008h	0E40 0008h
0040000Ch	PCIE_CORE_RP_DESC1		0D40 000Ch	0DC0 000Ch	0E40 000Ch
00400014h	PCIE_CORE_RP_DESC3		0D40 0014h	0DC0 0014h	0E40 0014h
00400018h	PCIE_CORE_RP_AXI_ADDR0		0D40 0018h	0DC0 0018h	0E40 0018h
0040001Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 001Ch	0DC0 001Ch	0E40 001Ch
00400020h	PCIE_CORE_RP_ADDR0		0D40 0020h	0DC0 0020h	0E40 0020h
00400024h	PCIE_CORE_RP_ADDR1		0D40 0024h	0DC0 0024h	0E40 0024h
00400028h	PCIE_CORE_RP_DESC0		0D40 0028h	0DC0 0028h	0E40 0028h
0040002Ch	PCIE_CORE_RP_DESC1		0D40 002Ch	0DC0 002Ch	0E40 002Ch

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400034h	PCIE_CORE_RP_DESC3		0D40 0034h	0DC0 0034h	0E40 0034h
00400038h	PCIE_CORE_RP_AXI_ADDR0		0D40 0038h	0DC0 0038h	0E40 0038h
0040003Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 003Ch	0DC0 003Ch	0E40 003Ch
00400040h	PCIE_CORE_RP_ADDR0		0D40 0040h	0DC0 0040h	0E40 0040h
00400044h	PCIE_CORE_RP_ADDR1		0D40 0044h	0DC0 0044h	0E40 0044h
00400048h	PCIE_CORE_RP_DESC0		0D40 0048h	0DC0 0048h	0E40 0048h
0040004Ch	PCIE_CORE_RP_DESC1		0D40 004Ch	0DC0 004Ch	0E40 004Ch
00400054h	PCIE_CORE_RP_DESC3		0D40 0054h	0DC0 0054h	0E40 0054h
00400058h	PCIE_CORE_RP_AXI_ADDR0		0D40 0058h	0DC0 0058h	0E40 0058h
0040005Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 005Ch	0DC0 005Ch	0E40 005Ch
00400060h	PCIE_CORE_RP_ADDR0		0D40 0060h	0DC0 0060h	0E40 0060h
00400064h	PCIE_CORE_RP_ADDR1		0D40 0064h	0DC0 0064h	0E40 0064h
00400068h	PCIE_CORE_RP_DESC0		0D40 0068h	0DC0 0068h	0E40 0068h
0040006Ch	PCIE_CORE_RP_DESC1		0D40 006Ch	0DC0 006Ch	0E40 006Ch
00400074h	PCIE_CORE_RP_DESC3		0D40 0074h	0DC0 0074h	0E40 0074h
00400078h	PCIE_CORE_RP_AXI_ADDR0		0D40 0078h	0DC0 0078h	0E40 0078h
0040007Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 007Ch	0DC0 007Ch	0E40 007Ch
00400080h	PCIE_CORE_RP_ADDR0		0D40 0080h	0DC0 0080h	0E40 0080h
00400084h	PCIE_CORE_RP_ADDR1		0D40 0084h	0DC0 0084h	0E40 0084h
00400088h	PCIE_CORE_RP_DESC0		0D40 0088h	0DC0 0088h	0E40 0088h
0040008Ch	PCIE_CORE_RP_DESC1		0D40 008Ch	0DC0 008Ch	0E40 008Ch
00400094h	PCIE_CORE_RP_DESC3		0D40 0094h	0DC0 0094h	0E40 0094h
00400098h	PCIE_CORE_RP_AXI_ADDR0		0D40 0098h	0DC0 0098h	0E40 0098h
0040009Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 009Ch	0DC0 009Ch	0E40 009Ch
004000A0h	PCIE_CORE_RP_ADDR0		0D40 00A0h	0DC0 00A0h	0E40 00A0h
004000A4h	PCIE_CORE_RP_ADDR1		0D40 00A4h	0DC0 00A4h	0E40 00A4h
004000A8h	PCIE_CORE_RP_DESC0		0D40 00A8h	0DC0 00A8h	0E40 00A8h
004000ACh	PCIE_CORE_RP_DESC1		0D40 00ACh	0DC0 00ACh	0E40 00ACh
004000B4h	PCIE_CORE_RP_DESC3		0D40 00B4h	0DC0 00B4h	0E40 00B4h
004000B8h	PCIE_CORE_RP_AXI_ADDR0		0D40 00B8h	0DC0 00B8h	0E40 00B8h
004000BCh	PCIE_CORE_RP_AXI_ADDR1		0D40 00BCh	0DC0 00BCh	0E40 00BCh
004000C0h	PCIE_CORE_RP_ADDR0		0D40 00C0h	0DC0 00C0h	0E40 00C0h
004000C4h	PCIE_CORE_RP_ADDR1		0D40 00C4h	0DC0 00C4h	0E40 00C4h
004000C8h	PCIE_CORE_RP_DESC0		0D40 00C8h	0DC0 00C8h	0E40 00C8h
004000CCh	PCIE_CORE_RP_DESC1		0D40 00CCh	0DC0 00CCh	0E40 00CCh
004000D4h	PCIE_CORE_RP_DESC3		0D40 00D4h	0DC0 00D4h	0E40 00D4h
004000D8h	PCIE_CORE_RP_AXI_ADDR0		0D40 00D8h	0DC0 00D8h	0E40 00D8h
004000DCh	PCIE_CORE_RP_AXI_ADDR1		0D40 00DCh	0DC0 00DCh	0E40 00DCh
004000E0h	PCIE_CORE_RP_ADDR0		0D40 00E0h	0DC0 00E0h	0E40 00E0h
004000E4h	PCIE_CORE_RP_ADDR1		0D40 00E4h	0DC0 00E4h	0E40 00E4h
004000E8h	PCIE_CORE_RP_DESC0		0D40 00E8h	0DC0 00E8h	0E40 00E8h
004000ECh	PCIE_CORE_RP_DESC1		0D40 00ECh	0DC0 00ECh	0E40 00ECh
004000F4h	PCIE_CORE_RP_DESC3		0D40 00F4h	0DC0 00F4h	0E40 00F4h
004000F8h	PCIE_CORE_RP_AXI_ADDR0		0D40 00F8h	0DC0 00F8h	0E40 00F8h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
004000FCh	PCIE_CORE_RP_AXI_ADDR1		0D40 00FCh	0DC0 00FCh	0E40 00FCh
00400100h	PCIE_CORE_RP_ADDR0		0D40 0100h	0DC0 0100h	0E40 0100h
00400104h	PCIE_CORE_RP_ADDR1		0D40 0104h	0DC0 0104h	0E40 0104h
00400108h	PCIE_CORE_RP_DESC0		0D40 0108h	0DC0 0108h	0E40 0108h
0040010Ch	PCIE_CORE_RP_DESC1		0D40 010Ch	0DC0 010Ch	0E40 010Ch
00400114h	PCIE_CORE_RP_DESC3		0D40 0114h	0DC0 0114h	0E40 0114h
00400118h	PCIE_CORE_RP_AXI_ADDR0		0D40 0118h	0DC0 0118h	0E40 0118h
0040011Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 011Ch	0DC0 011Ch	0E40 011Ch
00400120h	PCIE_CORE_RP_ADDR0		0D40 0120h	0DC0 0120h	0E40 0120h
00400124h	PCIE_CORE_RP_ADDR1		0D40 0124h	0DC0 0124h	0E40 0124h
00400128h	PCIE_CORE_RP_DESC0		0D40 0128h	0DC0 0128h	0E40 0128h
0040012Ch	PCIE_CORE_RP_DESC1		0D40 012Ch	0DC0 012Ch	0E40 012Ch
00400134h	PCIE_CORE_RP_DESC3		0D40 0134h	0DC0 0134h	0E40 0134h
00400138h	PCIE_CORE_RP_AXI_ADDR0		0D40 0138h	0DC0 0138h	0E40 0138h
0040013Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 013Ch	0DC0 013Ch	0E40 013Ch
00400140h	PCIE_CORE_RP_ADDR0		0D40 0140h	0DC0 0140h	0E40 0140h
00400144h	PCIE_CORE_RP_ADDR1		0D40 0144h	0DC0 0144h	0E40 0144h
00400148h	PCIE_CORE_RP_DESC0		0D40 0148h	0DC0 0148h	0E40 0148h
0040014Ch	PCIE_CORE_RP_DESC1		0D40 014Ch	0DC0 014Ch	0E40 014Ch
00400154h	PCIE_CORE_RP_DESC3		0D40 0154h	0DC0 0154h	0E40 0154h
00400158h	PCIE_CORE_RP_AXI_ADDR0		0D40 0158h	0DC0 0158h	0E40 0158h
0040015Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 015Ch	0DC0 015Ch	0E40 015Ch
00400160h	PCIE_CORE_RP_ADDR0		0D40 0160h	0DC0 0160h	0E40 0160h
00400164h	PCIE_CORE_RP_ADDR1		0D40 0164h	0DC0 0164h	0E40 0164h
00400168h	PCIE_CORE_RP_DESC0		0D40 0168h	0DC0 0168h	0E40 0168h
0040016Ch	PCIE_CORE_RP_DESC1		0D40 016Ch	0DC0 016Ch	0E40 016Ch
00400174h	PCIE_CORE_RP_DESC3		0D40 0174h	0DC0 0174h	0E40 0174h
00400178h	PCIE_CORE_RP_AXI_ADDR0		0D40 0178h	0DC0 0178h	0E40 0178h
0040017Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 017Ch	0DC0 017Ch	0E40 017Ch
00400180h	PCIE_CORE_RP_ADDR0		0D40 0180h	0DC0 0180h	0E40 0180h
00400184h	PCIE_CORE_RP_ADDR1		0D40 0184h	0DC0 0184h	0E40 0184h
00400188h	PCIE_CORE_RP_DESC0		0D40 0188h	0DC0 0188h	0E40 0188h
0040018Ch	PCIE_CORE_RP_DESC1		0D40 018Ch	0DC0 018Ch	0E40 018Ch
00400194h	PCIE_CORE_RP_DESC3		0D40 0194h	0DC0 0194h	0E40 0194h
00400198h	PCIE_CORE_RP_AXI_ADDR0		0D40 0198h	0DC0 0198h	0E40 0198h
0040019Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 019Ch	0DC0 019Ch	0E40 019Ch
004001A0h	PCIE_CORE_RP_ADDR0		0D40 01A0h	0DC0 01A0h	0E40 01A0h
004001A4h	PCIE_CORE_RP_ADDR1		0D40 01A4h	0DC0 01A4h	0E40 01A4h
004001A8h	PCIE_CORE_RP_DESC0		0D40 01A8h	0DC0 01A8h	0E40 01A8h
004001ACh	PCIE_CORE_RP_DESC1		0D40 01ACh	0DC0 01ACh	0E40 01ACh
004001B4h	PCIE_CORE_RP_DESC3		0D40 01B4h	0DC0 01B4h	0E40 01B4h
004001B8h	PCIE_CORE_RP_AXI_ADDR0		0D40 01B8h	0DC0 01B8h	0E40 01B8h
004001BCh	PCIE_CORE_RP_AXI_ADDR1		0D40 01BCh	0DC0 01BCh	0E40 01BCh
004001C0h	PCIE_CORE_RP_ADDR0		0D40 01C0h	0DC0 01C0h	0E40 01C0h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
004001C4h	PCIE_CORE_RP_ADDR1		0D40 01C4h	0DC0 01C4h	0E40 01C4h
004001C8h	PCIE_CORE_RP_DESC0		0D40 01C8h	0DC0 01C8h	0E40 01C8h
004001CCh	PCIE_CORE_RP_DESC1		0D40 01CCh	0DC0 01CCh	0E40 01CCh
004001D4h	PCIE_CORE_RP_DESC3		0D40 01D4h	0DC0 01D4h	0E40 01D4h
004001D8h	PCIE_CORE_RP_AXI_ADDR0		0D40 01D8h	0DC0 01D8h	0E40 01D8h
004001DCh	PCIE_CORE_RP_AXI_ADDR1		0D40 01DCh	0DC0 01DCh	0E40 01DCh
004001E0h	PCIE_CORE_RP_ADDR0		0D40 01E0h	0DC0 01E0h	0E40 01E0h
004001E4h	PCIE_CORE_RP_ADDR1		0D40 01E4h	0DC0 01E4h	0E40 01E4h
004001E8h	PCIE_CORE_RP_DESC0		0D40 01E8h	0DC0 01E8h	0E40 01E8h
004001ECh	PCIE_CORE_RP_DESC1		0D40 01ECh	0DC0 01ECh	0E40 01ECh
004001F4h	PCIE_CORE_RP_DESC3		0D40 01F4h	0DC0 01F4h	0E40 01F4h
004001F8h	PCIE_CORE_RP_AXI_ADDR0		0D40 01F8h	0DC0 01F8h	0E40 01F8h
004001FCh	PCIE_CORE_RP_AXI_ADDR1		0D40 01FCh	0DC0 01FCh	0E40 01FCh
00400200h	PCIE_CORE_RP_ADDR0		0D40 0200h	0DC0 0200h	0E40 0200h
00400204h	PCIE_CORE_RP_ADDR1		0D40 0204h	0DC0 0204h	0E40 0204h
00400208h	PCIE_CORE_RP_DESC0		0D40 0208h	0DC0 0208h	0E40 0208h
0040020Ch	PCIE_CORE_RP_DESC1		0D40 020Ch	0DC0 020Ch	0E40 020Ch
00400214h	PCIE_CORE_RP_DESC3		0D40 0214h	0DC0 0214h	0E40 0214h
00400218h	PCIE_CORE_RP_AXI_ADDR0		0D40 0218h	0DC0 0218h	0E40 0218h
0040021Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 021Ch	0DC0 021Ch	0E40 021Ch
00400220h	PCIE_CORE_RP_ADDR0		0D40 0220h	0DC0 0220h	0E40 0220h
00400224h	PCIE_CORE_RP_ADDR1		0D40 0224h	0DC0 0224h	0E40 0224h
00400228h	PCIE_CORE_RP_DESC0		0D40 0228h	0DC0 0228h	0E40 0228h
0040022Ch	PCIE_CORE_RP_DESC1		0D40 022Ch	0DC0 022Ch	0E40 022Ch
00400234h	PCIE_CORE_RP_DESC3		0D40 0234h	0DC0 0234h	0E40 0234h
00400238h	PCIE_CORE_RP_AXI_ADDR0		0D40 0238h	0DC0 0238h	0E40 0238h
0040023Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 023Ch	0DC0 023Ch	0E40 023Ch
00400240h	PCIE_CORE_RP_ADDR0		0D40 0240h	0DC0 0240h	0E40 0240h
00400244h	PCIE_CORE_RP_ADDR1		0D40 0244h	0DC0 0244h	0E40 0244h
00400248h	PCIE_CORE_RP_DESC0		0D40 0248h	0DC0 0248h	0E40 0248h
0040024Ch	PCIE_CORE_RP_DESC1		0D40 024Ch	0DC0 024Ch	0E40 024Ch
00400254h	PCIE_CORE_RP_DESC3		0D40 0254h	0DC0 0254h	0E40 0254h
00400258h	PCIE_CORE_RP_AXI_ADDR0		0D40 0258h	0DC0 0258h	0E40 0258h
0040025Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 025Ch	0DC0 025Ch	0E40 025Ch
00400260h	PCIE_CORE_RP_ADDR0		0D40 0260h	0DC0 0260h	0E40 0260h
00400264h	PCIE_CORE_RP_ADDR1		0D40 0264h	0DC0 0264h	0E40 0264h
00400268h	PCIE_CORE_RP_DESC0		0D40 0268h	0DC0 0268h	0E40 0268h
0040026Ch	PCIE_CORE_RP_DESC1		0D40 026Ch	0DC0 026Ch	0E40 026Ch
00400274h	PCIE_CORE_RP_DESC3		0D40 0274h	0DC0 0274h	0E40 0274h
00400278h	PCIE_CORE_RP_AXI_ADDR0		0D40 0278h	0DC0 0278h	0E40 0278h
0040027Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 027Ch	0DC0 027Ch	0E40 027Ch
00400280h	PCIE_CORE_RP_ADDR0		0D40 0280h	0DC0 0280h	0E40 0280h
00400284h	PCIE_CORE_RP_ADDR1		0D40 0284h	0DC0 0284h	0E40 0284h
00400288h	PCIE_CORE_RP_DESC0		0D40 0288h	0DC0 0288h	0E40 0288h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
0040028Ch	PCIE_CORE_RP_DESC1		0D40 028Ch	0DC0 028Ch	0E40 028Ch
00400294h	PCIE_CORE_RP_DESC3		0D40 0294h	0DC0 0294h	0E40 0294h
00400298h	PCIE_CORE_RP_AXI_ADDR0		0D40 0298h	0DC0 0298h	0E40 0298h
0040029Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 029Ch	0DC0 029Ch	0E40 029Ch
004002A0h	PCIE_CORE_RP_ADDR0		0D40 02A0h	0DC0 02A0h	0E40 02A0h
004002A4h	PCIE_CORE_RP_ADDR1		0D40 02A4h	0DC0 02A4h	0E40 02A4h
004002A8h	PCIE_CORE_RP_DESC0		0D40 02A8h	0DC0 02A8h	0E40 02A8h
004002ACh	PCIE_CORE_RP_DESC1		0D40 02ACh	0DC0 02ACh	0E40 02ACh
004002B4h	PCIE_CORE_RP_DESC3		0D40 02B4h	0DC0 02B4h	0E40 02B4h
004002B8h	PCIE_CORE_RP_AXI_ADDR0		0D40 02B8h	0DC0 02B8h	0E40 02B8h
004002BCh	PCIE_CORE_RP_AXI_ADDR1		0D40 02BCh	0DC0 02BCh	0E40 02BCh
004002C0h	PCIE_CORE_RP_ADDR0		0D40 02C0h	0DC0 02C0h	0E40 02C0h
004002C4h	PCIE_CORE_RP_ADDR1		0D40 02C4h	0DC0 02C4h	0E40 02C4h
004002C8h	PCIE_CORE_RP_DESC0		0D40 02C8h	0DC0 02C8h	0E40 02C8h
004002CCh	PCIE_CORE_RP_DESC1		0D40 02CCh	0DC0 02CCh	0E40 02CCh
004002D4h	PCIE_CORE_RP_DESC3		0D40 02D4h	0DC0 02D4h	0E40 02D4h
004002D8h	PCIE_CORE_RP_AXI_ADDR0		0D40 02D8h	0DC0 02D8h	0E40 02D8h
004002DCh	PCIE_CORE_RP_AXI_ADDR1		0D40 02DCh	0DC0 02DCh	0E40 02DCh
004002E0h	PCIE_CORE_RP_ADDR0		0D40 02E0h	0DC0 02E0h	0E40 02E0h
004002E4h	PCIE_CORE_RP_ADDR1		0D40 02E4h	0DC0 02E4h	0E40 02E4h
004002E8h	PCIE_CORE_RP_DESC0		0D40 02E8h	0DC0 02E8h	0E40 02E8h
004002ECh	PCIE_CORE_RP_DESC1		0D40 02ECh	0DC0 02ECh	0E40 02ECh
004002F4h	PCIE_CORE_RP_DESC3		0D40 02F4h	0DC0 02F4h	0E40 02F4h
004002F8h	PCIE_CORE_RP_AXI_ADDR0		0D40 02F8h	0DC0 02F8h	0E40 02F8h
004002FCh	PCIE_CORE_RP_AXI_ADDR1		0D40 02FCh	0DC0 02FCh	0E40 02FCh
00400300h	PCIE_CORE_RP_ADDR0		0D40 0300h	0DC0 0300h	0E40 0300h
00400304h	PCIE_CORE_RP_ADDR1		0D40 0304h	0DC0 0304h	0E40 0304h
00400308h	PCIE_CORE_RP_DESC0		0D40 0308h	0DC0 0308h	0E40 0308h
0040030Ch	PCIE_CORE_RP_DESC1		0D40 030Ch	0DC0 030Ch	0E40 030Ch
00400314h	PCIE_CORE_RP_DESC3		0D40 0314h	0DC0 0314h	0E40 0314h
00400318h	PCIE_CORE_RP_AXI_ADDR0		0D40 0318h	0DC0 0318h	0E40 0318h
0040031Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 031Ch	0DC0 031Ch	0E40 031Ch
00400320h	PCIE_CORE_RP_ADDR0		0D40 0320h	0DC0 0320h	0E40 0320h
00400324h	PCIE_CORE_RP_ADDR1		0D40 0324h	0DC0 0324h	0E40 0324h
00400328h	PCIE_CORE_RP_DESC0		0D40 0328h	0DC0 0328h	0E40 0328h
0040032Ch	PCIE_CORE_RP_DESC1		0D40 032Ch	0DC0 032Ch	0E40 032Ch
00400334h	PCIE_CORE_RP_DESC3		0D40 0334h	0DC0 0334h	0E40 0334h
00400338h	PCIE_CORE_RP_AXI_ADDR0		0D40 0338h	0DC0 0338h	0E40 0338h
0040033Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 033Ch	0DC0 033Ch	0E40 033Ch
00400340h	PCIE_CORE_RP_ADDR0		0D40 0340h	0DC0 0340h	0E40 0340h
00400344h	PCIE_CORE_RP_ADDR1		0D40 0344h	0DC0 0344h	0E40 0344h
00400348h	PCIE_CORE_RP_DESC0		0D40 0348h	0DC0 0348h	0E40 0348h
0040034Ch	PCIE_CORE_RP_DESC1		0D40 034Ch	0DC0 034Ch	0E40 034Ch
00400354h	PCIE_CORE_RP_DESC3		0D40 0354h	0DC0 0354h	0E40 0354h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400358h	PCIE_CORE_RP_AXI_ADDR0		0D40 0358h	0DC0 0358h	0E40 0358h
0040035Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 035Ch	0DC0 035Ch	0E40 035Ch
00400360h	PCIE_CORE_RP_ADDR0		0D40 0360h	0DC0 0360h	0E40 0360h
00400364h	PCIE_CORE_RP_ADDR1		0D40 0364h	0DC0 0364h	0E40 0364h
00400368h	PCIE_CORE_RP_DESC0		0D40 0368h	0DC0 0368h	0E40 0368h
0040036Ch	PCIE_CORE_RP_DESC1		0D40 036Ch	0DC0 036Ch	0E40 036Ch
00400374h	PCIE_CORE_RP_DESC3		0D40 0374h	0DC0 0374h	0E40 0374h
00400378h	PCIE_CORE_RP_AXI_ADDR0		0D40 0378h	0DC0 0378h	0E40 0378h
0040037Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 037Ch	0DC0 037Ch	0E40 037Ch
00400380h	PCIE_CORE_RP_ADDR0		0D40 0380h	0DC0 0380h	0E40 0380h
00400384h	PCIE_CORE_RP_ADDR1		0D40 0384h	0DC0 0384h	0E40 0384h
00400388h	PCIE_CORE_RP_DESC0		0D40 0388h	0DC0 0388h	0E40 0388h
0040038Ch	PCIE_CORE_RP_DESC1		0D40 038Ch	0DC0 038Ch	0E40 038Ch
00400394h	PCIE_CORE_RP_DESC3		0D40 0394h	0DC0 0394h	0E40 0394h
00400398h	PCIE_CORE_RP_AXI_ADDR0		0D40 0398h	0DC0 0398h	0E40 0398h
0040039Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 039Ch	0DC0 039Ch	0E40 039Ch
004003A0h	PCIE_CORE_RP_ADDR0		0D40 03A0h	0DC0 03A0h	0E40 03A0h
004003A4h	PCIE_CORE_RP_ADDR1		0D40 03A4h	0DC0 03A4h	0E40 03A4h
004003A8h	PCIE_CORE_RP_DESC0		0D40 03A8h	0DC0 03A8h	0E40 03A8h
004003ACh	PCIE_CORE_RP_DESC1		0D40 03ACh	0DC0 03ACh	0E40 03ACh
004003B4h	PCIE_CORE_RP_DESC3		0D40 03B4h	0DC0 03B4h	0E40 03B4h
004003B8h	PCIE_CORE_RP_AXI_ADDR0		0D40 03B8h	0DC0 03B8h	0E40 03B8h
004003BCh	PCIE_CORE_RP_AXI_ADDR1		0D40 03BCh	0DC0 03BCh	0E40 03BCh
004003C0h	PCIE_CORE_RP_ADDR0		0D40 03C0h	0DC0 03C0h	0E40 03C0h
004003C4h	PCIE_CORE_RP_ADDR1		0D40 03C4h	0DC0 03C4h	0E40 03C4h
004003C8h	PCIE_CORE_RP_DESC0		0D40 03C8h	0DC0 03C8h	0E40 03C8h
004003CCh	PCIE_CORE_RP_DESC1		0D40 03CCh	0DC0 03CCh	0E40 03CCh
004003D4h	PCIE_CORE_RP_DESC3		0D40 03D4h	0DC0 03D4h	0E40 03D4h
004003D8h	PCIE_CORE_RP_AXI_ADDR0		0D40 03D8h	0DC0 03D8h	0E40 03D8h
004003DCh	PCIE_CORE_RP_AXI_ADDR1		0D40 03DCh	0DC0 03DCh	0E40 03DCh
004003E0h	PCIE_CORE_RP_ADDR0		0D40 03E0h	0DC0 03E0h	0E40 03E0h
004003E4h	PCIE_CORE_RP_ADDR1		0D40 03E4h	0DC0 03E4h	0E40 03E4h
004003E8h	PCIE_CORE_RP_DESC0		0D40 03E8h	0DC0 03E8h	0E40 03E8h
004003ECh	PCIE_CORE_RP_DESC1		0D40 03ECh	0DC0 03ECh	0E40 03ECh
004003F4h	PCIE_CORE_RP_DESC3		0D40 03F4h	0DC0 03F4h	0E40 03F4h
004003F8h	PCIE_CORE_RP_AXI_ADDR0		0D40 03F8h	0DC0 03F8h	0E40 03F8h
004003FCh	PCIE_CORE_RP_AXI_ADDR1		0D40 03FCh	0DC0 03FCh	0E40 03FCh
00400400h	PCIE_CORE_RP_ADDR0		0D40 0400h	0DC0 0400h	0E40 0400h
00400404h	PCIE_CORE_RP_ADDR1		0D40 0404h	0DC0 0404h	0E40 0404h
00400408h	PCIE_CORE_RP_DESC0		0D40 0408h	0DC0 0408h	0E40 0408h
0040040Ch	PCIE_CORE_RP_DESC1		0D40 040Ch	0DC0 040Ch	0E40 040Ch
00400414h	PCIE_CORE_RP_DESC3		0D40 0414h	0DC0 0414h	0E40 0414h
00400418h	PCIE_CORE_RP_AXI_ADDR0		0D40 0418h	0DC0 0418h	0E40 0418h
0040041Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 041Ch	0DC0 041Ch	0E40 041Ch

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400420h	PCIE_CORE_RP_ADDR0		0D40 0420h	0DC0 0420h	0E40 0420h
00400424h	PCIE_CORE_RP_ADDR1		0D40 0424h	0DC0 0424h	0E40 0424h
00400428h	PCIE_CORE_RP_DESC0		0D40 0428h	0DC0 0428h	0E40 0428h
0040042Ch	PCIE_CORE_RP_DESC1		0D40 042Ch	0DC0 042Ch	0E40 042Ch
00400434h	PCIE_CORE_RP_DESC3		0D40 0434h	0DC0 0434h	0E40 0434h
00400438h	PCIE_CORE_RP_AXI_ADDR0		0D40 0438h	0DC0 0438h	0E40 0438h
0040043Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 043Ch	0DC0 043Ch	0E40 043Ch
00400440h	PCIE_CORE_RP_ADDR0		0D40 0440h	0DC0 0440h	0E40 0440h
00400444h	PCIE_CORE_RP_ADDR1		0D40 0444h	0DC0 0444h	0E40 0444h
00400448h	PCIE_CORE_RP_DESC0		0D40 0448h	0DC0 0448h	0E40 0448h
0040044Ch	PCIE_CORE_RP_DESC1		0D40 044Ch	0DC0 044Ch	0E40 044Ch
00400454h	PCIE_CORE_RP_DESC3		0D40 0454h	0DC0 0454h	0E40 0454h
00400458h	PCIE_CORE_RP_AXI_ADDR0		0D40 0458h	0DC0 0458h	0E40 0458h
0040045Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 045Ch	0DC0 045Ch	0E40 045Ch
00400460h	PCIE_CORE_RP_ADDR0		0D40 0460h	0DC0 0460h	0E40 0460h
00400464h	PCIE_CORE_RP_ADDR1		0D40 0464h	0DC0 0464h	0E40 0464h
00400468h	PCIE_CORE_RP_DESC0		0D40 0468h	0DC0 0468h	0E40 0468h
0040046Ch	PCIE_CORE_RP_DESC1		0D40 046Ch	0DC0 046Ch	0E40 046Ch
00400474h	PCIE_CORE_RP_DESC3		0D40 0474h	0DC0 0474h	0E40 0474h
00400478h	PCIE_CORE_RP_AXI_ADDR0		0D40 0478h	0DC0 0478h	0E40 0478h
0040047Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 047Ch	0DC0 047Ch	0E40 047Ch
00400480h	PCIE_CORE_RP_ADDR0		0D40 0480h	0DC0 0480h	0E40 0480h
00400484h	PCIE_CORE_RP_ADDR1		0D40 0484h	0DC0 0484h	0E40 0484h
00400488h	PCIE_CORE_RP_DESC0		0D40 0488h	0DC0 0488h	0E40 0488h
0040048Ch	PCIE_CORE_RP_DESC1		0D40 048Ch	0DC0 048Ch	0E40 048Ch
00400494h	PCIE_CORE_RP_DESC3		0D40 0494h	0DC0 0494h	0E40 0494h
00400498h	PCIE_CORE_RP_AXI_ADDR0		0D40 0498h	0DC0 0498h	0E40 0498h
0040049Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 049Ch	0DC0 049Ch	0E40 049Ch
004004A0h	PCIE_CORE_RP_ADDR0		0D40 04A0h	0DC0 04A0h	0E40 04A0h
004004A4h	PCIE_CORE_RP_ADDR1		0D40 04A4h	0DC0 04A4h	0E40 04A4h
004004A8h	PCIE_CORE_RP_DESC0		0D40 04A8h	0DC0 04A8h	0E40 04A8h
004004ACh	PCIE_CORE_RP_DESC1		0D40 04ACh	0DC0 04ACh	0E40 04ACh
004004B4h	PCIE_CORE_RP_DESC3		0D40 04B4h	0DC0 04B4h	0E40 04B4h
004004B8h	PCIE_CORE_RP_AXI_ADDR0		0D40 04B8h	0DC0 04B8h	0E40 04B8h
004004BCh	PCIE_CORE_RP_AXI_ADDR1		0D40 04BCh	0DC0 04BCh	0E40 04BCh
004004C0h	PCIE_CORE_RP_ADDR0		0D40 04C0h	0DC0 04C0h	0E40 04C0h
004004C4h	PCIE_CORE_RP_ADDR1		0D40 04C4h	0DC0 04C4h	0E40 04C4h
004004C8h	PCIE_CORE_RP_DESC0		0D40 04C8h	0DC0 04C8h	0E40 04C8h
004004CCh	PCIE_CORE_RP_DESC1		0D40 04CCh	0DC0 04CCh	0E40 04CCh
004004D4h	PCIE_CORE_RP_DESC3		0D40 04D4h	0DC0 04D4h	0E40 04D4h
004004D8h	PCIE_CORE_RP_AXI_ADDR0		0D40 04D8h	0DC0 04D8h	0E40 04D8h
004004DCh	PCIE_CORE_RP_AXI_ADDR1		0D40 04DCh	0DC0 04DCh	0E40 04DCh
004004E0h	PCIE_CORE_RP_ADDR0		0D40 04E0h	0DC0 04E0h	0E40 04E0h
004004E4h	PCIE_CORE_RP_ADDR1		0D40 04E4h	0DC0 04E4h	0E40 04E4h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
004004E8h	PCIE_CORE_RP_DESC0		0D40 04E8h	0DC0 04E8h	0E40 04E8h
004004ECh	PCIE_CORE_RP_DESC1		0D40 04ECh	0DC0 04ECh	0E40 04ECh
004004F4h	PCIE_CORE_RP_DESC3		0D40 04F4h	0DC0 04F4h	0E40 04F4h
004004F8h	PCIE_CORE_RP_AXI_ADDR0		0D40 04F8h	0DC0 04F8h	0E40 04F8h
004004FCh	PCIE_CORE_RP_AXI_ADDR1		0D40 04FCh	0DC0 04FCh	0E40 04FCh
00400500h	PCIE_CORE_RP_ADDR0		0D40 0500h	0DC0 0500h	0E40 0500h
00400504h	PCIE_CORE_RP_ADDR1		0D40 0504h	0DC0 0504h	0E40 0504h
00400508h	PCIE_CORE_RP_DESC0		0D40 0508h	0DC0 0508h	0E40 0508h
0040050Ch	PCIE_CORE_RP_DESC1		0D40 050Ch	0DC0 050Ch	0E40 050Ch
00400514h	PCIE_CORE_RP_DESC3		0D40 0514h	0DC0 0514h	0E40 0514h
00400518h	PCIE_CORE_RP_AXI_ADDR0		0D40 0518h	0DC0 0518h	0E40 0518h
0040051Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 051Ch	0DC0 051Ch	0E40 051Ch
00400520h	PCIE_CORE_RP_ADDR0		0D40 0520h	0DC0 0520h	0E40 0520h
00400524h	PCIE_CORE_RP_ADDR1		0D40 0524h	0DC0 0524h	0E40 0524h
00400528h	PCIE_CORE_RP_DESC0		0D40 0528h	0DC0 0528h	0E40 0528h
0040052Ch	PCIE_CORE_RP_DESC1		0D40 052Ch	0DC0 052Ch	0E40 052Ch
00400534h	PCIE_CORE_RP_DESC3		0D40 0534h	0DC0 0534h	0E40 0534h
00400538h	PCIE_CORE_RP_AXI_ADDR0		0D40 0538h	0DC0 0538h	0E40 0538h
0040053Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 053Ch	0DC0 053Ch	0E40 053Ch
00400540h	PCIE_CORE_RP_ADDR0		0D40 0540h	0DC0 0540h	0E40 0540h
00400544h	PCIE_CORE_RP_ADDR1		0D40 0544h	0DC0 0544h	0E40 0544h
00400548h	PCIE_CORE_RP_DESC0		0D40 0548h	0DC0 0548h	0E40 0548h
0040054Ch	PCIE_CORE_RP_DESC1		0D40 054Ch	0DC0 054Ch	0E40 054Ch
00400554h	PCIE_CORE_RP_DESC3		0D40 0554h	0DC0 0554h	0E40 0554h
00400558h	PCIE_CORE_RP_AXI_ADDR0		0D40 0558h	0DC0 0558h	0E40 0558h
0040055Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 055Ch	0DC0 055Ch	0E40 055Ch
00400560h	PCIE_CORE_RP_ADDR0		0D40 0560h	0DC0 0560h	0E40 0560h
00400564h	PCIE_CORE_RP_ADDR1		0D40 0564h	0DC0 0564h	0E40 0564h
00400568h	PCIE_CORE_RP_DESC0		0D40 0568h	0DC0 0568h	0E40 0568h
0040056Ch	PCIE_CORE_RP_DESC1		0D40 056Ch	0DC0 056Ch	0E40 056Ch
00400574h	PCIE_CORE_RP_DESC3		0D40 0574h	0DC0 0574h	0E40 0574h
00400578h	PCIE_CORE_RP_AXI_ADDR0		0D40 0578h	0DC0 0578h	0E40 0578h
0040057Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 057Ch	0DC0 057Ch	0E40 057Ch
00400580h	PCIE_CORE_RP_ADDR0		0D40 0580h	0DC0 0580h	0E40 0580h
00400584h	PCIE_CORE_RP_ADDR1		0D40 0584h	0DC0 0584h	0E40 0584h
00400588h	PCIE_CORE_RP_DESC0		0D40 0588h	0DC0 0588h	0E40 0588h
0040058Ch	PCIE_CORE_RP_DESC1		0D40 058Ch	0DC0 058Ch	0E40 058Ch
00400594h	PCIE_CORE_RP_DESC3		0D40 0594h	0DC0 0594h	0E40 0594h
00400598h	PCIE_CORE_RP_AXI_ADDR0		0D40 0598h	0DC0 0598h	0E40 0598h
0040059Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 059Ch	0DC0 059Ch	0E40 059Ch
004005A0h	PCIE_CORE_RP_ADDR0		0D40 05A0h	0DC0 05A0h	0E40 05A0h
004005A4h	PCIE_CORE_RP_ADDR1		0D40 05A4h	0DC0 05A4h	0E40 05A4h
004005A8h	PCIE_CORE_RP_DESC0		0D40 05A8h	0DC0 05A8h	0E40 05A8h
004005ACh	PCIE_CORE_RP_DESC1		0D40 05ACh	0DC0 05ACh	0E40 05ACh

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
004005B4h	PCIE_CORE_RP_DESC3		0D40 05B4h	0DC0 05B4h	0E40 05B4h
004005B8h	PCIE_CORE_RP_AXI_ADDR0		0D40 05B8h	0DC0 05B8h	0E40 05B8h
004005BCh	PCIE_CORE_RP_AXI_ADDR1		0D40 05BCh	0DC0 05BCh	0E40 05BCh
004005C0h	PCIE_CORE_RP_ADDR0		0D40 05C0h	0DC0 05C0h	0E40 05C0h
004005C4h	PCIE_CORE_RP_ADDR1		0D40 05C4h	0DC0 05C4h	0E40 05C4h
004005C8h	PCIE_CORE_RP_DESC0		0D40 05C8h	0DC0 05C8h	0E40 05C8h
004005CCh	PCIE_CORE_RP_DESC1		0D40 05CCh	0DC0 05CCh	0E40 05CCh
004005D4h	PCIE_CORE_RP_DESC3		0D40 05D4h	0DC0 05D4h	0E40 05D4h
004005D8h	PCIE_CORE_RP_AXI_ADDR0		0D40 05D8h	0DC0 05D8h	0E40 05D8h
004005DCh	PCIE_CORE_RP_AXI_ADDR1		0D40 05DCh	0DC0 05DCh	0E40 05DCh
004005E0h	PCIE_CORE_RP_ADDR0		0D40 05E0h	0DC0 05E0h	0E40 05E0h
004005E4h	PCIE_CORE_RP_ADDR1		0D40 05E4h	0DC0 05E4h	0E40 05E4h
004005E8h	PCIE_CORE_RP_DESC0		0D40 05E8h	0DC0 05E8h	0E40 05E8h
004005ECh	PCIE_CORE_RP_DESC1		0D40 05ECh	0DC0 05ECh	0E40 05ECh
004005F4h	PCIE_CORE_RP_DESC3		0D40 05F4h	0DC0 05F4h	0E40 05F4h
004005F8h	PCIE_CORE_RP_AXI_ADDR0		0D40 05F8h	0DC0 05F8h	0E40 05F8h
004005FCh	PCIE_CORE_RP_AXI_ADDR1		0D40 05FCh	0DC0 05FCh	0E40 05FCh
00400600h	PCIE_CORE_RP_ADDR0		0D40 0600h	0DC0 0600h	0E40 0600h
00400604h	PCIE_CORE_RP_ADDR1		0D40 0604h	0DC0 0604h	0E40 0604h
00400608h	PCIE_CORE_RP_DESC0		0D40 0608h	0DC0 0608h	0E40 0608h
0040060Ch	PCIE_CORE_RP_DESC1		0D40 060Ch	0DC0 060Ch	0E40 060Ch
00400614h	PCIE_CORE_RP_DESC3		0D40 0614h	0DC0 0614h	0E40 0614h
00400618h	PCIE_CORE_RP_AXI_ADDR0		0D40 0618h	0DC0 0618h	0E40 0618h
0040061Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 061Ch	0DC0 061Ch	0E40 061Ch
00400620h	PCIE_CORE_RP_ADDR0		0D40 0620h	0DC0 0620h	0E40 0620h
00400624h	PCIE_CORE_RP_ADDR1		0D40 0624h	0DC0 0624h	0E40 0624h
00400628h	PCIE_CORE_RP_DESC0		0D40 0628h	0DC0 0628h	0E40 0628h
0040062Ch	PCIE_CORE_RP_DESC1		0D40 062Ch	0DC0 062Ch	0E40 062Ch
00400634h	PCIE_CORE_RP_DESC3		0D40 0634h	0DC0 0634h	0E40 0634h
00400638h	PCIE_CORE_RP_AXI_ADDR0		0D40 0638h	0DC0 0638h	0E40 0638h
0040063Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 063Ch	0DC0 063Ch	0E40 063Ch
00400640h	PCIE_CORE_RP_ADDR0		0D40 0640h	0DC0 0640h	0E40 0640h
00400644h	PCIE_CORE_RP_ADDR1		0D40 0644h	0DC0 0644h	0E40 0644h
00400648h	PCIE_CORE_RP_DESC0		0D40 0648h	0DC0 0648h	0E40 0648h
0040064Ch	PCIE_CORE_RP_DESC1		0D40 064Ch	0DC0 064Ch	0E40 064Ch
00400654h	PCIE_CORE_RP_DESC3		0D40 0654h	0DC0 0654h	0E40 0654h
00400658h	PCIE_CORE_RP_AXI_ADDR0		0D40 0658h	0DC0 0658h	0E40 0658h
0040065Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 065Ch	0DC0 065Ch	0E40 065Ch
00400660h	PCIE_CORE_RP_ADDR0		0D40 0660h	0DC0 0660h	0E40 0660h
00400664h	PCIE_CORE_RP_ADDR1		0D40 0664h	0DC0 0664h	0E40 0664h
00400668h	PCIE_CORE_RP_DESC0		0D40 0668h	0DC0 0668h	0E40 0668h
0040066Ch	PCIE_CORE_RP_DESC1		0D40 066Ch	0DC0 066Ch	0E40 066Ch
00400674h	PCIE_CORE_RP_DESC3		0D40 0674h	0DC0 0674h	0E40 0674h
00400678h	PCIE_CORE_RP_AXI_ADDR0		0D40 0678h	0DC0 0678h	0E40 0678h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
0040067Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 067Ch	0DC0 067Ch	0E40 067Ch
00400680h	PCIE_CORE_RP_ADDR0		0D40 0680h	0DC0 0680h	0E40 0680h
00400684h	PCIE_CORE_RP_ADDR1		0D40 0684h	0DC0 0684h	0E40 0684h
00400688h	PCIE_CORE_RP_DESC0		0D40 0688h	0DC0 0688h	0E40 0688h
0040068Ch	PCIE_CORE_RP_DESC1		0D40 068Ch	0DC0 068Ch	0E40 068Ch
00400694h	PCIE_CORE_RP_DESC3		0D40 0694h	0DC0 0694h	0E40 0694h
00400698h	PCIE_CORE_RP_AXI_ADDR0		0D40 0698h	0DC0 0698h	0E40 0698h
0040069Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 069Ch	0DC0 069Ch	0E40 069Ch
004006A0h	PCIE_CORE_RP_ADDR0		0D40 06A0h	0DC0 06A0h	0E40 06A0h
004006A4h	PCIE_CORE_RP_ADDR1		0D40 06A4h	0DC0 06A4h	0E40 06A4h
004006A8h	PCIE_CORE_RP_DESC0		0D40 06A8h	0DC0 06A8h	0E40 06A8h
004006ACh	PCIE_CORE_RP_DESC1		0D40 06ACh	0DC0 06ACh	0E40 06ACh
004006B4h	PCIE_CORE_RP_DESC3		0D40 06B4h	0DC0 06B4h	0E40 06B4h
004006B8h	PCIE_CORE_RP_AXI_ADDR0		0D40 06B8h	0DC0 06B8h	0E40 06B8h
004006BCh	PCIE_CORE_RP_AXI_ADDR1		0D40 06BCh	0DC0 06BCh	0E40 06BCh
004006C0h	PCIE_CORE_RP_ADDR0		0D40 06C0h	0DC0 06C0h	0E40 06C0h
004006C4h	PCIE_CORE_RP_ADDR1		0D40 06C4h	0DC0 06C4h	0E40 06C4h
004006C8h	PCIE_CORE_RP_DESC0		0D40 06C8h	0DC0 06C8h	0E40 06C8h
004006CCh	PCIE_CORE_RP_DESC1		0D40 06CCh	0DC0 06CCh	0E40 06CCh
004006D4h	PCIE_CORE_RP_DESC3		0D40 06D4h	0DC0 06D4h	0E40 06D4h
004006D8h	PCIE_CORE_RP_AXI_ADDR0		0D40 06D8h	0DC0 06D8h	0E40 06D8h
004006DCh	PCIE_CORE_RP_AXI_ADDR1		0D40 06DCh	0DC0 06DCh	0E40 06DCh
004006E0h	PCIE_CORE_RP_ADDR0		0D40 06E0h	0DC0 06E0h	0E40 06E0h
004006E4h	PCIE_CORE_RP_ADDR1		0D40 06E4h	0DC0 06E4h	0E40 06E4h
004006E8h	PCIE_CORE_RP_DESC0		0D40 06E8h	0DC0 06E8h	0E40 06E8h
004006ECh	PCIE_CORE_RP_DESC1		0D40 06ECh	0DC0 06ECh	0E40 06ECh
004006F4h	PCIE_CORE_RP_DESC3		0D40 06F4h	0DC0 06F4h	0E40 06F4h
004006F8h	PCIE_CORE_RP_AXI_ADDR0		0D40 06F8h	0DC0 06F8h	0E40 06F8h
004006FCh	PCIE_CORE_RP_AXI_ADDR1		0D40 06FCh	0DC0 06FCh	0E40 06FCh
00400700h	PCIE_CORE_RP_ADDR0		0D40 0700h	0DC0 0700h	0E40 0700h
00400704h	PCIE_CORE_RP_ADDR1		0D40 0704h	0DC0 0704h	0E40 0704h
00400708h	PCIE_CORE_RP_DESC0		0D40 0708h	0DC0 0708h	0E40 0708h
0040070Ch	PCIE_CORE_RP_DESC1		0D40 070Ch	0DC0 070Ch	0E40 070Ch
00400714h	PCIE_CORE_RP_DESC3		0D40 0714h	0DC0 0714h	0E40 0714h
00400718h	PCIE_CORE_RP_AXI_ADDR0		0D40 0718h	0DC0 0718h	0E40 0718h
0040071Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 071Ch	0DC0 071Ch	0E40 071Ch
00400720h	PCIE_CORE_RP_ADDR0		0D40 0720h	0DC0 0720h	0E40 0720h
00400724h	PCIE_CORE_RP_ADDR1		0D40 0724h	0DC0 0724h	0E40 0724h
00400728h	PCIE_CORE_RP_DESC0		0D40 0728h	0DC0 0728h	0E40 0728h
0040072Ch	PCIE_CORE_RP_DESC1		0D40 072Ch	0DC0 072Ch	0E40 072Ch
00400734h	PCIE_CORE_RP_DESC3		0D40 0734h	0DC0 0734h	0E40 0734h
00400738h	PCIE_CORE_RP_AXI_ADDR0		0D40 0738h	0DC0 0738h	0E40 0738h
0040073Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 073Ch	0DC0 073Ch	0E40 073Ch
00400740h	PCIE_CORE_RP_ADDR0		0D40 0740h	0DC0 0740h	0E40 0740h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400744h	PCIE_CORE_RP_ADDR1		0D40 0744h	0DC0 0744h	0E40 0744h
00400748h	PCIE_CORE_RP_DESC0		0D40 0748h	0DC0 0748h	0E40 0748h
0040074Ch	PCIE_CORE_RP_DESC1		0D40 074Ch	0DC0 074Ch	0E40 074Ch
00400754h	PCIE_CORE_RP_DESC3		0D40 0754h	0DC0 0754h	0E40 0754h
00400758h	PCIE_CORE_RP_AXI_ADDR0		0D40 0758h	0DC0 0758h	0E40 0758h
0040075Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 075Ch	0DC0 075Ch	0E40 075Ch
00400760h	PCIE_CORE_RP_ADDR0		0D40 0760h	0DC0 0760h	0E40 0760h
00400764h	PCIE_CORE_RP_ADDR1		0D40 0764h	0DC0 0764h	0E40 0764h
00400768h	PCIE_CORE_RP_DESC0		0D40 0768h	0DC0 0768h	0E40 0768h
0040076Ch	PCIE_CORE_RP_DESC1		0D40 076Ch	0DC0 076Ch	0E40 076Ch
00400774h	PCIE_CORE_RP_DESC3		0D40 0774h	0DC0 0774h	0E40 0774h
00400778h	PCIE_CORE_RP_AXI_ADDR0		0D40 0778h	0DC0 0778h	0E40 0778h
0040077Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 077Ch	0DC0 077Ch	0E40 077Ch
00400780h	PCIE_CORE_RP_ADDR0		0D40 0780h	0DC0 0780h	0E40 0780h
00400784h	PCIE_CORE_RP_ADDR1		0D40 0784h	0DC0 0784h	0E40 0784h
00400788h	PCIE_CORE_RP_DESC0		0D40 0788h	0DC0 0788h	0E40 0788h
0040078Ch	PCIE_CORE_RP_DESC1		0D40 078Ch	0DC0 078Ch	0E40 078Ch
00400794h	PCIE_CORE_RP_DESC3		0D40 0794h	0DC0 0794h	0E40 0794h
00400798h	PCIE_CORE_RP_AXI_ADDR0		0D40 0798h	0DC0 0798h	0E40 0798h
0040079Ch	PCIE_CORE_RP_AXI_ADDR1		0D40 079Ch	0DC0 079Ch	0E40 079Ch
004007A0h	PCIE_CORE_RP_ADDR0		0D40 07A0h	0DC0 07A0h	0E40 07A0h
004007A4h	PCIE_CORE_RP_ADDR1		0D40 07A4h	0DC0 07A4h	0E40 07A4h
004007A8h	PCIE_CORE_RP_DESC0		0D40 07A8h	0DC0 07A8h	0E40 07A8h
004007ACh	PCIE_CORE_RP_DESC1		0D40 07ACh	0DC0 07ACh	0E40 07ACh
004007B4h	PCIE_CORE_RP_DESC3		0D40 07B4h	0DC0 07B4h	0E40 07B4h
004007B8h	PCIE_CORE_RP_AXI_ADDR0		0D40 07B8h	0DC0 07B8h	0E40 07B8h
004007BCh	PCIE_CORE_RP_AXI_ADDR1		0D40 07BCh	0DC0 07BCh	0E40 07BCh
004007C0h	PCIE_CORE_RP_ADDR0		0D40 07C0h	0DC0 07C0h	0E40 07C0h
004007C4h	PCIE_CORE_RP_ADDR1		0D40 07C4h	0DC0 07C4h	0E40 07C4h
004007C8h	PCIE_CORE_RP_DESC0		0D40 07C8h	0DC0 07C8h	0E40 07C8h
004007CCh	PCIE_CORE_RP_DESC1		0D40 07CCh	0DC0 07CCh	0E40 07CCh
004007D4h	PCIE_CORE_RP_DESC3		0D40 07D4h	0DC0 07D4h	0E40 07D4h
004007D8h	PCIE_CORE_RP_AXI_ADDR0		0D40 07D8h	0DC0 07D8h	0E40 07D8h
004007DCh	PCIE_CORE_RP_AXI_ADDR1		0D40 07DCh	0DC0 07DCh	0E40 07DCh
004007E0h	PCIE_CORE_RP_ADDR0		0D40 07E0h	0DC0 07E0h	0E40 07E0h
004007E4h	PCIE_CORE_RP_ADDR1		0D40 07E4h	0DC0 07E4h	0E40 07E4h
004007E8h	PCIE_CORE_RP_DESC0		0D40 07E8h	0DC0 07E8h	0E40 07E8h
004007ECh	PCIE_CORE_RP_DESC1		0D40 07ECh	0DC0 07ECh	0E40 07ECh
004007F4h	PCIE_CORE_RP_DESC3		0D40 07F4h	0DC0 07F4h	0E40 07F4h
004007F8h	PCIE_CORE_RP_AXI_ADDR0		0D40 07F8h	0DC0 07F8h	0E40 07F8h
004007FCh	PCIE_CORE_RP_AXI_ADDR1		0D40 07FCh	0DC0 07FCh	0E40 07FCh
00400800h	PCIE_CORE_RP_ADDR0		0D40 0800h	0DC0 0800h	0E40 0800h
00400804h	PCIE_CORE_RP_ADDR1		0D40 0804h	0DC0 0804h	0E40 0804h
00400808h	PCIE_CORE_RP_ADDR0		0D40 0808h	0DC0 0808h	0E40 0808h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
0040080Ch	PCIE_CORE_RP_ADDR1		0D40 080Ch	0DC0 080Ch	0E40 080Ch
00400810h	PCIE_CORE_RP_ADDR0		0D40 0810h	0DC0 0810h	0E40 0810h
00400814h	PCIE_CORE_RP_ADDR1		0D40 0814h	0DC0 0814h	0E40 0814h
00400820h	PCIE_CORE_RP_C0		0D40 0820h	0DC0 0820h	0E40 0820h
00400824h	PCIE_CORE_RP_L0		0D40 0824h	0DC0 0824h	0E40 0824h
00400840h	PCIE_CORE_RP_ADDR0		0D40 0840h	0DC0 0840h	0E40 0840h
00400844h	PCIE_CORE_RP_ADDR1		0D40 0844h	0DC0 0844h	0E40 0844h
00400848h	PCIE_CORE_RP_ADDR0		0D40 0848h	0DC0 0848h	0E40 0848h
0040084Ch	PCIE_CORE_RP_ADDR1		0D40 084Ch	0DC0 084Ch	0E40 084Ch
00400850h	PCIE_CORE_RP_ADDR0		0D40 0850h	0DC0 0850h	0E40 0850h
00400854h	PCIE_CORE_RP_ADDR1		0D40 0854h	0DC0 0854h	0E40 0854h
00400858h	PCIE_CORE_RP_ADDR0		0D40 0858h	0DC0 0858h	0E40 0858h
0040085Ch	PCIE_CORE_RP_ADDR1		0D40 085Ch	0DC0 085Ch	0E40 085Ch
00400860h	PCIE_CORE_RP_ADDR0		0D40 0860h	0DC0 0860h	0E40 0860h
00400864h	PCIE_CORE_RP_ADDR1		0D40 0864h	0DC0 0864h	0E40 0864h
00400868h	PCIE_CORE_RP_ADDR0		0D40 0868h	0DC0 0868h	0E40 0868h
0040086Ch	PCIE_CORE_RP_ADDR1		0D40 086Ch	0DC0 086Ch	0E40 086Ch
00400870h	PCIE_CORE_RP_ADDR0		0D40 0870h	0DC0 0870h	0E40 0870h
00400874h	PCIE_CORE_RP_ADDR1		0D40 0874h	0DC0 0874h	0E40 0874h
00400878h	PCIE_CORE_RP_ADDR0		0D40 0878h	0DC0 0878h	0E40 0878h
0040087Ch	PCIE_CORE_RP_ADDR1		0D40 087Ch	0DC0 087Ch	0E40 087Ch
00400880h	PCIE_CORE_RP_ADDR0		0D40 0880h	0DC0 0880h	0E40 0880h
00400884h	PCIE_CORE_RP_ADDR1		0D40 0884h	0DC0 0884h	0E40 0884h
00400888h	PCIE_CORE_RP_ADDR0		0D40 0888h	0DC0 0888h	0E40 0888h
0040088Ch	PCIE_CORE_RP_ADDR1		0D40 088Ch	0DC0 088Ch	0E40 088Ch
00400890h	PCIE_CORE_RP_ADDR0		0D40 0890h	0DC0 0890h	0E40 0890h
00400894h	PCIE_CORE_RP_ADDR1		0D40 0894h	0DC0 0894h	0E40 0894h
00400898h	PCIE_CORE_RP_ADDR0		0D40 0898h	0DC0 0898h	0E40 0898h
0040089Ch	PCIE_CORE_RP_ADDR1		0D40 089Ch	0DC0 089Ch	0E40 089Ch
004008A0h	PCIE_CORE_RP_ADDR0		0D40 08A0h	0DC0 08A0h	0E40 08A0h
004008A4h	PCIE_CORE_RP_ADDR1		0D40 08A4h	0DC0 08A4h	0E40 08A4h
004008A8h	PCIE_CORE_RP_ADDR0		0D40 08A8h	0DC0 08A8h	0E40 08A8h
004008ACh	PCIE_CORE_RP_ADDR1		0D40 08ACh	0DC0 08ACh	0E40 08ACh
004008B0h	PCIE_CORE_RP_ADDR0		0D40 08B0h	0DC0 08B0h	0E40 08B0h
004008B4h	PCIE_CORE_RP_ADDR1		0D40 08B4h	0DC0 08B4h	0E40 08B4h
004008B8h	PCIE_CORE_RP_ADDR0		0D40 08B8h	0DC0 08B8h	0E40 08B8h
004008BCh	PCIE_CORE_RP_ADDR1		0D40 08BCh	0DC0 08BCh	0E40 08BCh
004008C0h	PCIE_CORE_RP_ADDR0		0D40 08C0h	0DC0 08C0h	0E40 08C0h
004008C4h	PCIE_CORE_RP_ADDR1		0D40 08C4h	0DC0 08C4h	0E40 08C4h
004008C8h	PCIE_CORE_RP_ADDR0		0D40 08C8h	0DC0 08C8h	0E40 08C8h
004008CCh	PCIE_CORE_RP_ADDR1		0D40 08CCh	0DC0 08CCh	0E40 08CCh
004008D0h	PCIE_CORE_RP_ADDR0		0D40 08D0h	0DC0 08D0h	0E40 08D0h
004008D4h	PCIE_CORE_RP_ADDR1		0D40 08D4h	0DC0 08D4h	0E40 08D4h
004008D8h	PCIE_CORE_RP_ADDR0		0D40 08D8h	0DC0 08D8h	0E40 08D8h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
004008DCh	PCIE_CORE_RP_ADDR1		0D40 08DCh	0DC0 08DCh	0E40 08DCh
004008E0h	PCIE_CORE_RP_ADDR0		0D40 08E0h	0DC0 08E0h	0E40 08E0h
004008E4h	PCIE_CORE_RP_ADDR1		0D40 08E4h	0DC0 08E4h	0E40 08E4h
004008E8h	PCIE_CORE_RP_ADDR0		0D40 08E8h	0DC0 08E8h	0E40 08E8h
004008ECh	PCIE_CORE_RP_ADDR1		0D40 08ECh	0DC0 08ECh	0E40 08ECh
004008F0h	PCIE_CORE_RP_ADDR0		0D40 08F0h	0DC0 08F0h	0E40 08F0h
004008F4h	PCIE_CORE_RP_ADDR1		0D40 08F4h	0DC0 08F4h	0E40 08F4h
004008F8h	PCIE_CORE_RP_ADDR0		0D40 08F8h	0DC0 08F8h	0E40 08F8h
004008FCh	PCIE_CORE_RP_ADDR1		0D40 08FCh	0DC0 08FCh	0E40 08FCh
00400900h	PCIE_CORE_RP_ADDR0		0D40 0900h	0DC0 0900h	0E40 0900h
00400904h	PCIE_CORE_RP_ADDR1		0D40 0904h	0DC0 0904h	0E40 0904h
00400908h	PCIE_CORE_RP_ADDR0		0D40 0908h	0DC0 0908h	0E40 0908h
0040090Ch	PCIE_CORE_RP_ADDR1		0D40 090Ch	0DC0 090Ch	0E40 090Ch
00400910h	PCIE_CORE_RP_ADDR0		0D40 0910h	0DC0 0910h	0E40 0910h
00400914h	PCIE_CORE_RP_ADDR1		0D40 0914h	0DC0 0914h	0E40 0914h
00400918h	PCIE_CORE_RP_ADDR0		0D40 0918h	0DC0 0918h	0E40 0918h
0040091Ch	PCIE_CORE_RP_ADDR1		0D40 091Ch	0DC0 091Ch	0E40 091Ch
00400920h	PCIE_CORE_RP_ADDR0		0D40 0920h	0DC0 0920h	0E40 0920h
00400924h	PCIE_CORE_RP_ADDR1		0D40 0924h	0DC0 0924h	0E40 0924h
00400928h	PCIE_CORE_RP_ADDR0		0D40 0928h	0DC0 0928h	0E40 0928h
0040092Ch	PCIE_CORE_RP_ADDR1		0D40 092Ch	0DC0 092Ch	0E40 092Ch
00400930h	PCIE_CORE_RP_ADDR0		0D40 0930h	0DC0 0930h	0E40 0930h
00400934h	PCIE_CORE_RP_ADDR1		0D40 0934h	0DC0 0934h	0E40 0934h
00400938h	PCIE_CORE_RP_ADDR0		0D40 0938h	0DC0 0938h	0E40 0938h
0040093Ch	PCIE_CORE_RP_ADDR1		0D40 093Ch	0DC0 093Ch	0E40 093Ch
00400940h	PCIE_CORE_RP_ADDR0		0D40 0940h	0DC0 0940h	0E40 0940h
00400944h	PCIE_CORE_RP_ADDR1		0D40 0944h	0DC0 0944h	0E40 0944h
00400948h	PCIE_CORE_RP_ADDR0		0D40 0948h	0DC0 0948h	0E40 0948h
0040094Ch	PCIE_CORE_RP_ADDR1		0D40 094Ch	0DC0 094Ch	0E40 094Ch
00400950h	PCIE_CORE_RP_ADDR0		0D40 0950h	0DC0 0950h	0E40 0950h
00400954h	PCIE_CORE_RP_ADDR1		0D40 0954h	0DC0 0954h	0E40 0954h
00400958h	PCIE_CORE_RP_ADDR0		0D40 0958h	0DC0 0958h	0E40 0958h
0040095Ch	PCIE_CORE_RP_ADDR1		0D40 095Ch	0DC0 095Ch	0E40 095Ch
00400960h	PCIE_CORE_RP_ADDR0		0D40 0960h	0DC0 0960h	0E40 0960h
00400964h	PCIE_CORE_RP_ADDR1		0D40 0964h	0DC0 0964h	0E40 0964h
00400968h	PCIE_CORE_RP_ADDR0		0D40 0968h	0DC0 0968h	0E40 0968h
0040096Ch	PCIE_CORE_RP_ADDR1		0D40 096Ch	0DC0 096Ch	0E40 096Ch
00400970h	PCIE_CORE_RP_ADDR0		0D40 0970h	0DC0 0970h	0E40 0970h
00400974h	PCIE_CORE_RP_ADDR1		0D40 0974h	0DC0 0974h	0E40 0974h
00400978h	PCIE_CORE_RP_ADDR0		0D40 0978h	0DC0 0978h	0E40 0978h
0040097Ch	PCIE_CORE_RP_ADDR1		0D40 097Ch	0DC0 097Ch	0E40 097Ch
00400980h	PCIE_CORE_RP_ADDR0		0D40 0980h	0DC0 0980h	0E40 0980h
00400984h	PCIE_CORE_RP_ADDR1		0D40 0984h	0DC0 0984h	0E40 0984h
00400988h	PCIE_CORE_RP_ADDR0		0D40 0988h	0DC0 0988h	0E40 0988h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
0040098Ch	PCIE_CORE_RP_ADDR1		0D40 098Ch	0DC0 098Ch	0E40 098Ch
00400990h	PCIE_CORE_RP_ADDR0		0D40 0990h	0DC0 0990h	0E40 0990h
00400994h	PCIE_CORE_RP_ADDR1		0D40 0994h	0DC0 0994h	0E40 0994h
00400998h	PCIE_CORE_RP_ADDR0		0D40 0998h	0DC0 0998h	0E40 0998h
0040099Ch	PCIE_CORE_RP_ADDR1		0D40 099Ch	0DC0 099Ch	0E40 099Ch
004009A0h	PCIE_CORE_RP_ADDR0		0D40 09A0h	0DC0 09A0h	0E40 09A0h
004009A4h	PCIE_CORE_RP_ADDR1		0D40 09A4h	0DC0 09A4h	0E40 09A4h
004009A8h	PCIE_CORE_RP_ADDR0		0D40 09A8h	0DC0 09A8h	0E40 09A8h
004009ACh	PCIE_CORE_RP_ADDR1		0D40 09ACh	0DC0 09ACh	0E40 09ACh
004009B0h	PCIE_CORE_RP_ADDR0		0D40 09B0h	0DC0 09B0h	0E40 09B0h
004009B4h	PCIE_CORE_RP_ADDR1		0D40 09B4h	0DC0 09B4h	0E40 09B4h
004009B8h	PCIE_CORE_RP_ADDR0		0D40 09B8h	0DC0 09B8h	0E40 09B8h
004009BCh	PCIE_CORE_RP_ADDR1		0D40 09BCh	0DC0 09BCh	0E40 09BCh
004009C0h	PCIE_CORE_RP_ADDR0		0D40 09C0h	0DC0 09C0h	0E40 09C0h
004009C4h	PCIE_CORE_RP_ADDR1		0D40 09C4h	0DC0 09C4h	0E40 09C4h
004009C8h	PCIE_CORE_RP_ADDR0		0D40 09C8h	0DC0 09C8h	0E40 09C8h
004009CCh	PCIE_CORE_RP_ADDR1		0D40 09CCh	0DC0 09CCh	0E40 09CCh
004009D0h	PCIE_CORE_RP_ADDR0		0D40 09D0h	0DC0 09D0h	0E40 09D0h
004009D4h	PCIE_CORE_RP_ADDR1		0D40 09D4h	0DC0 09D4h	0E40 09D4h
004009D8h	PCIE_CORE_RP_ADDR0		0D40 09D8h	0DC0 09D8h	0E40 09D8h
004009DCh	PCIE_CORE_RP_ADDR1		0D40 09DCh	0DC0 09DCh	0E40 09DCh
004009E0h	PCIE_CORE_RP_ADDR0		0D40 09E0h	0DC0 09E0h	0E40 09E0h
004009E4h	PCIE_CORE_RP_ADDR1		0D40 09E4h	0DC0 09E4h	0E40 09E4h
004009E8h	PCIE_CORE_RP_ADDR0		0D40 09E8h	0DC0 09E8h	0E40 09E8h
004009ECh	PCIE_CORE_RP_ADDR1		0D40 09ECh	0DC0 09ECh	0E40 09ECh
004009F0h	PCIE_CORE_RP_ADDR0		0D40 09F0h	0DC0 09F0h	0E40 09F0h
004009F4h	PCIE_CORE_RP_ADDR1		0D40 09F4h	0DC0 09F4h	0E40 09F4h
004009F8h	PCIE_CORE_RP_ADDR0		0D40 09F8h	0DC0 09F8h	0E40 09F8h
004009FCh	PCIE_CORE_RP_ADDR1		0D40 09FCh	0DC0 09FCh	0E40 09FCh
00400A00h	PCIE_CORE_RP_ADDR0		0D40 0A00h	0DC0 0A00h	0E40 0A00h
00400A04h	PCIE_CORE_RP_ADDR1		0D40 0A04h	0DC0 0A04h	0E40 0A04h
00400A08h	PCIE_CORE_RP_ADDR0		0D40 0A08h	0DC0 0A08h	0E40 0A08h
00400A0Ch	PCIE_CORE_RP_ADDR1		0D40 0A0Ch	0DC0 0A0Ch	0E40 0A0Ch
00400A10h	PCIE_CORE_RP_ADDR0		0D40 0A10h	0DC0 0A10h	0E40 0A10h
00400A14h	PCIE_CORE_RP_ADDR1		0D40 0A14h	0DC0 0A14h	0E40 0A14h
00400A18h	PCIE_CORE_RP_ADDR0		0D40 0A18h	0DC0 0A18h	0E40 0A18h
00400A1Ch	PCIE_CORE_RP_ADDR1		0D40 0A1Ch	0DC0 0A1Ch	0E40 0A1Ch
00400A20h	PCIE_CORE_RP_ADDR0		0D40 0A20h	0DC0 0A20h	0E40 0A20h
00400A24h	PCIE_CORE_RP_ADDR1		0D40 0A24h	0DC0 0A24h	0E40 0A24h
00400A28h	PCIE_CORE_RP_ADDR0		0D40 0A28h	0DC0 0A28h	0E40 0A28h
00400A2Ch	PCIE_CORE_RP_ADDR1		0D40 0A2Ch	0DC0 0A2Ch	0E40 0A2Ch
00400A30h	PCIE_CORE_RP_ADDR0		0D40 0A30h	0DC0 0A30h	0E40 0A30h
00400A34h	PCIE_CORE_RP_ADDR1		0D40 0A34h	0DC0 0A34h	0E40 0A34h
00400A38h	PCIE_CORE_RP_ADDR0		0D40 0A38h	0DC0 0A38h	0E40 0A38h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400A3Ch	PCIE_CORE_RP_ADDR1		0D40 0A3Ch	0DC0 0A3Ch	0E40 0A3Ch
00400A40h	PCIE_CORE_RP_ADDR0		0D40 0A40h	0DC0 0A40h	0E40 0A40h
00400A44h	PCIE_CORE_RP_ADDR1		0D40 0A44h	0DC0 0A44h	0E40 0A44h
00400A48h	PCIE_CORE_RP_ADDR0		0D40 0A48h	0DC0 0A48h	0E40 0A48h
00400A4Ch	PCIE_CORE_RP_ADDR1		0D40 0A4Ch	0DC0 0A4Ch	0E40 0A4Ch
00400A50h	PCIE_CORE_RP_ADDR0		0D40 0A50h	0DC0 0A50h	0E40 0A50h
00400A54h	PCIE_CORE_RP_ADDR1		0D40 0A54h	0DC0 0A54h	0E40 0A54h
00400A58h	PCIE_CORE_RP_ADDR0		0D40 0A58h	0DC0 0A58h	0E40 0A58h
00400A5Ch	PCIE_CORE_RP_ADDR1		0D40 0A5Ch	0DC0 0A5Ch	0E40 0A5Ch
00400A60h	PCIE_CORE_RP_ADDR0		0D40 0A60h	0DC0 0A60h	0E40 0A60h
00400A64h	PCIE_CORE_RP_ADDR1		0D40 0A64h	0DC0 0A64h	0E40 0A64h
00400A68h	PCIE_CORE_RP_ADDR0		0D40 0A68h	0DC0 0A68h	0E40 0A68h
00400A6Ch	PCIE_CORE_RP_ADDR1		0D40 0A6Ch	0DC0 0A6Ch	0E40 0A6Ch
00400A70h	PCIE_CORE_RP_ADDR0		0D40 0A70h	0DC0 0A70h	0E40 0A70h
00400A74h	PCIE_CORE_RP_ADDR1		0D40 0A74h	0DC0 0A74h	0E40 0A74h
00400A78h	PCIE_CORE_RP_ADDR0		0D40 0A78h	0DC0 0A78h	0E40 0A78h
00400A7Ch	PCIE_CORE_RP_ADDR1		0D40 0A7Ch	0DC0 0A7Ch	0E40 0A7Ch
00400A80h	PCIE_CORE_RP_ADDR0		0D40 0A80h	0DC0 0A80h	0E40 0A80h
00400A84h	PCIE_CORE_RP_ADDR1		0D40 0A84h	0DC0 0A84h	0E40 0A84h
00400A88h	PCIE_CORE_RP_ADDR0		0D40 0A88h	0DC0 0A88h	0E40 0A88h
00400A8Ch	PCIE_CORE_RP_ADDR1		0D40 0A8Ch	0DC0 0A8Ch	0E40 0A8Ch
00400A90h	PCIE_CORE_RP_ADDR0		0D40 0A90h	0DC0 0A90h	0E40 0A90h
00400A94h	PCIE_CORE_RP_ADDR1		0D40 0A94h	0DC0 0A94h	0E40 0A94h
00400A98h	PCIE_CORE_RP_ADDR0		0D40 0A98h	0DC0 0A98h	0E40 0A98h
00400A9Ch	PCIE_CORE_RP_ADDR1		0D40 0A9Ch	0DC0 0A9Ch	0E40 0A9Ch
00400AA0h	PCIE_CORE_RP_ADDR0		0D40 0AA0h	0DC0 0AA0h	0E40 0AA0h
00400AA4h	PCIE_CORE_RP_ADDR1		0D40 0AA4h	0DC0 0AA4h	0E40 0AA4h
00400AA8h	PCIE_CORE_RP_ADDR0		0D40 0AA8h	0DC0 0AA8h	0E40 0AA8h
00400AACH	PCIE_CORE_RP_ADDR1		0D40 0AACH	0DC0 0AACH	0E40 0AACH
00400AB0h	PCIE_CORE_RP_ADDR0		0D40 0AB0h	0DC0 0AB0h	0E40 0AB0h
00400AB4h	PCIE_CORE_RP_ADDR1		0D40 0AB4h	0DC0 0AB4h	0E40 0AB4h
00400AB8h	PCIE_CORE_RP_ADDR0		0D40 0AB8h	0DC0 0AB8h	0E40 0AB8h
00400ABCh	PCIE_CORE_RP_ADDR1		0D40 0ABCh	0DC0 0ABCh	0E40 0ABCh
00400AC0h	PCIE_CORE_RP_ADDR0		0D40 0AC0h	0DC0 0AC0h	0E40 0AC0h
00400AC4h	PCIE_CORE_RP_ADDR1		0D40 0AC4h	0DC0 0AC4h	0E40 0AC4h
00400AC8h	PCIE_CORE_RP_ADDR0		0D40 0AC8h	0DC0 0AC8h	0E40 0AC8h
00400ACCh	PCIE_CORE_RP_ADDR1		0D40 0ACCh	0DC0 0ACCh	0E40 0ACCh
00400AD0h	PCIE_CORE_RP_ADDR0		0D40 0AD0h	0DC0 0AD0h	0E40 0AD0h
00400AD4h	PCIE_CORE_RP_ADDR1		0D40 0AD4h	0DC0 0AD4h	0E40 0AD4h
00400AD8h	PCIE_CORE_RP_ADDR0		0D40 0AD8h	0DC0 0AD8h	0E40 0AD8h
00400ADCh	PCIE_CORE_RP_ADDR1		0D40 0ADCh	0DC0 0ADCh	0E40 0ADCh
00400AE0h	PCIE_CORE_RP_ADDR0		0D40 0AE0h	0DC0 0AE0h	0E40 0AE0h
00400AE4h	PCIE_CORE_RP_ADDR1		0D40 0AE4h	0DC0 0AE4h	0E40 0AE4h
00400AE8h	PCIE_CORE_RP_ADDR0		0D40 0AE8h	0DC0 0AE8h	0E40 0AE8h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400AECh	PCIE_CORE_RP_ADDR1		0D40 0AECCh	0DC0 0AECCh	0E40 0AECCh
00400AF0h	PCIE_CORE_RP_ADDR0		0D40 0AF0h	0DC0 0AF0h	0E40 0AF0h
00400AF4h	PCIE_CORE_RP_ADDR1		0D40 0AF4h	0DC0 0AF4h	0E40 0AF4h
00400AF8h	PCIE_CORE_RP_ADDR0		0D40 0AF8h	0DC0 0AF8h	0E40 0AF8h
00400AFCh	PCIE_CORE_RP_ADDR1		0D40 0AFCh	0DC0 0AFCh	0E40 0AFCh
00400B00h	PCIE_CORE_RP_ADDR0		0D40 0B00h	0DC0 0B00h	0E40 0B00h
00400B04h	PCIE_CORE_RP_ADDR1		0D40 0B04h	0DC0 0B04h	0E40 0B04h
00400B08h	PCIE_CORE_RP_ADDR0		0D40 0B08h	0DC0 0B08h	0E40 0B08h
00400B0Ch	PCIE_CORE_RP_ADDR1		0D40 0B0Ch	0DC0 0B0Ch	0E40 0B0Ch
00400B10h	PCIE_CORE_RP_ADDR0		0D40 0B10h	0DC0 0B10h	0E40 0B10h
00400B14h	PCIE_CORE_RP_ADDR1		0D40 0B14h	0DC0 0B14h	0E40 0B14h
00400B18h	PCIE_CORE_RP_ADDR0		0D40 0B18h	0DC0 0B18h	0E40 0B18h
00400B1Ch	PCIE_CORE_RP_ADDR1		0D40 0B1Ch	0DC0 0B1Ch	0E40 0B1Ch
00400B20h	PCIE_CORE_RP_ADDR0		0D40 0B20h	0DC0 0B20h	0E40 0B20h
00400B24h	PCIE_CORE_RP_ADDR1		0D40 0B24h	0DC0 0B24h	0E40 0B24h
00400B28h	PCIE_CORE_RP_ADDR0		0D40 0B28h	0DC0 0B28h	0E40 0B28h
00400B2Ch	PCIE_CORE_RP_ADDR1		0D40 0B2Ch	0DC0 0B2Ch	0E40 0B2Ch
00400B30h	PCIE_CORE_RP_ADDR0		0D40 0B30h	0DC0 0B30h	0E40 0B30h
00400B34h	PCIE_CORE_RP_ADDR1		0D40 0B34h	0DC0 0B34h	0E40 0B34h
00400B38h	PCIE_CORE_RP_ADDR0		0D40 0B38h	0DC0 0B38h	0E40 0B38h
00400B3Ch	PCIE_CORE_RP_ADDR1		0D40 0B3Ch	0DC0 0B3Ch	0E40 0B3Ch
00400B40h	PCIE_CORE_RP_ADDR0		0D40 0B40h	0DC0 0B40h	0E40 0B40h
00400B44h	PCIE_CORE_RP_ADDR1		0D40 0B44h	0DC0 0B44h	0E40 0B44h
00400B48h	PCIE_CORE_RP_ADDR0		0D40 0B48h	0DC0 0B48h	0E40 0B48h
00400B4Ch	PCIE_CORE_RP_ADDR1		0D40 0B4Ch	0DC0 0B4Ch	0E40 0B4Ch
00400B50h	PCIE_CORE_RP_ADDR0		0D40 0B50h	0DC0 0B50h	0E40 0B50h
00400B54h	PCIE_CORE_RP_ADDR1		0D40 0B54h	0DC0 0B54h	0E40 0B54h
00400B58h	PCIE_CORE_RP_ADDR0		0D40 0B58h	0DC0 0B58h	0E40 0B58h
00400B5Ch	PCIE_CORE_RP_ADDR1		0D40 0B5Ch	0DC0 0B5Ch	0E40 0B5Ch
00400B60h	PCIE_CORE_RP_ADDR0		0D40 0B60h	0DC0 0B60h	0E40 0B60h
00400B64h	PCIE_CORE_RP_ADDR1		0D40 0B64h	0DC0 0B64h	0E40 0B64h
00400B68h	PCIE_CORE_RP_ADDR0		0D40 0B68h	0DC0 0B68h	0E40 0B68h
00400B6Ch	PCIE_CORE_RP_ADDR1		0D40 0B6Ch	0DC0 0B6Ch	0E40 0B6Ch
00400B70h	PCIE_CORE_RP_ADDR0		0D40 0B70h	0DC0 0B70h	0E40 0B70h
00400B74h	PCIE_CORE_RP_ADDR1		0D40 0B74h	0DC0 0B74h	0E40 0B74h
00400B78h	PCIE_CORE_RP_ADDR0		0D40 0B78h	0DC0 0B78h	0E40 0B78h
00400B7Ch	PCIE_CORE_RP_ADDR1		0D40 0B7Ch	0DC0 0B7Ch	0E40 0B7Ch
00400B80h	PCIE_CORE_RP_ADDR0		0D40 0B80h	0DC0 0B80h	0E40 0B80h
00400B84h	PCIE_CORE_RP_ADDR1		0D40 0B84h	0DC0 0B84h	0E40 0B84h
00400B88h	PCIE_CORE_RP_ADDR0		0D40 0B88h	0DC0 0B88h	0E40 0B88h
00400B8Ch	PCIE_CORE_RP_ADDR1		0D40 0B8Ch	0DC0 0B8Ch	0E40 0B8Ch
00400B90h	PCIE_CORE_RP_ADDR0		0D40 0B90h	0DC0 0B90h	0E40 0B90h
00400B94h	PCIE_CORE_RP_ADDR1		0D40 0B94h	0DC0 0B94h	0E40 0B94h
00400B98h	PCIE_CORE_RP_ADDR0		0D40 0B98h	0DC0 0B98h	0E40 0B98h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400B9Ch	PCIE_CORE_RP_ADDR1		0D40 0B9Ch	0DC0 0B9Ch	0E40 0B9Ch
00400BA0h	PCIE_CORE_RP_ADDR0		0D40 0BA0h	0DC0 0BA0h	0E40 0BA0h
00400BA4h	PCIE_CORE_RP_ADDR1		0D40 0BA4h	0DC0 0BA4h	0E40 0BA4h
00400BA8h	PCIE_CORE_RP_ADDR0		0D40 0BA8h	0DC0 0BA8h	0E40 0BA8h
00400BACH	PCIE_CORE_RP_ADDR1		0D40 0BACH	0DC0 0BACH	0E40 0BACH
00400BB0h	PCIE_CORE_RP_ADDR0		0D40 0BB0h	0DC0 0BB0h	0E40 0BB0h
00400BB4h	PCIE_CORE_RP_ADDR1		0D40 0BB4h	0DC0 0BB4h	0E40 0BB4h
00400BB8h	PCIE_CORE_RP_ADDR0		0D40 0BB8h	0DC0 0BB8h	0E40 0BB8h
00400BBCh	PCIE_CORE_RP_ADDR1		0D40 0BBCh	0DC0 0BBCh	0E40 0BBCh
00400BC0h	PCIE_CORE_RP_ADDR0		0D40 0BC0h	0DC0 0BC0h	0E40 0BC0h
00400BC4h	PCIE_CORE_RP_ADDR1		0D40 0BC4h	0DC0 0BC4h	0E40 0BC4h
00400BC8h	PCIE_CORE_RP_ADDR0		0D40 0BC8h	0DC0 0BC8h	0E40 0BC8h
00400BCCh	PCIE_CORE_RP_ADDR1		0D40 0BCCh	0DC0 0BCCh	0E40 0BCCh
00400BD0h	PCIE_CORE_RP_ADDR0		0D40 0BD0h	0DC0 0BD0h	0E40 0BD0h
00400BD4h	PCIE_CORE_RP_ADDR1		0D40 0BD4h	0DC0 0BD4h	0E40 0BD4h
00400BD8h	PCIE_CORE_RP_ADDR0		0D40 0BD8h	0DC0 0BD8h	0E40 0BD8h
00400BDCh	PCIE_CORE_RP_ADDR1		0D40 0BDCh	0DC0 0BDCh	0E40 0BDCh
00400BE0h	PCIE_CORE_RP_ADDR0		0D40 0BE0h	0DC0 0BE0h	0E40 0BE0h
00400BE4h	PCIE_CORE_RP_ADDR1		0D40 0BE4h	0DC0 0BE4h	0E40 0BE4h
00400BE8h	PCIE_CORE_RP_ADDR0		0D40 0BE8h	0DC0 0BE8h	0E40 0BE8h
00400BECh	PCIE_CORE_RP_ADDR1		0D40 0BECh	0DC0 0BECh	0E40 0BECh
00400BF0h	PCIE_CORE_RP_ADDR0		0D40 0BF0h	0DC0 0BF0h	0E40 0BF0h
00400BF4h	PCIE_CORE_RP_ADDR1		0D40 0BF4h	0DC0 0BF4h	0E40 0BF4h
00400BF8h	PCIE_CORE_RP_ADDR0		0D40 0BF8h	0DC0 0BF8h	0E40 0BF8h
00400BFCh	PCIE_CORE_RP_ADDR1		0D40 0BFCh	0DC0 0BFCh	0E40 0BFCh
00400C00h	PCIE_CORE_RP_ADDR0		0D40 0C00h	0DC0 0C00h	0E40 0C00h
00400C04h	PCIE_CORE_RP_ADDR1		0D40 0C04h	0DC0 0C04h	0E40 0C04h
00400C08h	PCIE_CORE_RP_ADDR0		0D40 0C08h	0DC0 0C08h	0E40 0C08h
00400C0Ch	PCIE_CORE_RP_ADDR1		0D40 0C0Ch	0DC0 0C0Ch	0E40 0C0Ch
00400C10h	PCIE_CORE_RP_ADDR0		0D40 0C10h	0DC0 0C10h	0E40 0C10h
00400C14h	PCIE_CORE_RP_ADDR1		0D40 0C14h	0DC0 0C14h	0E40 0C14h
00400C18h	PCIE_CORE_RP_ADDR0		0D40 0C18h	0DC0 0C18h	0E40 0C18h
00400C1Ch	PCIE_CORE_RP_ADDR1		0D40 0C1Ch	0DC0 0C1Ch	0E40 0C1Ch
00400C20h	PCIE_CORE_RP_ADDR0		0D40 0C20h	0DC0 0C20h	0E40 0C20h
00400C24h	PCIE_CORE_RP_ADDR1		0D40 0C24h	0DC0 0C24h	0E40 0C24h
00400C28h	PCIE_CORE_RP_ADDR0		0D40 0C28h	0DC0 0C28h	0E40 0C28h
00400C2Ch	PCIE_CORE_RP_ADDR1		0D40 0C2Ch	0DC0 0C2Ch	0E40 0C2Ch
00400C30h	PCIE_CORE_RP_ADDR0		0D40 0C30h	0DC0 0C30h	0E40 0C30h
00400C34h	PCIE_CORE_RP_ADDR1		0D40 0C34h	0DC0 0C34h	0E40 0C34h
00400C38h	PCIE_CORE_RP_ADDR0		0D40 0C38h	0DC0 0C38h	0E40 0C38h
00400C3Ch	PCIE_CORE_RP_ADDR1		0D40 0C3Ch	0DC0 0C3Ch	0E40 0C3Ch
00400C40h	PCIE_CORE_RP_ADDR0		0D40 0C40h	0DC0 0C40h	0E40 0C40h
00400C44h	PCIE_CORE_RP_ADDR1		0D40 0C44h	0DC0 0C44h	0E40 0C44h
00400C48h	PCIE_CORE_RP_ADDR0		0D40 0C48h	0DC0 0C48h	0E40 0C48h

Table 9-1181. PCIe_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400C4Ch	PCIE_CORE_RP_ADDR1		0D40 0C4Ch	0DC0 0C4Ch	0E40 0C4Ch
00400C50h	PCIE_CORE_RP_ADDR0		0D40 0C50h	0DC0 0C50h	0E40 0C50h
00400C54h	PCIE_CORE_RP_ADDR1		0D40 0C54h	0DC0 0C54h	0E40 0C54h
00400C58h	PCIE_CORE_RP_ADDR0		0D40 0C58h	0DC0 0C58h	0E40 0C58h
00400C5Ch	PCIE_CORE_RP_ADDR1		0D40 0C5Ch	0DC0 0C5Ch	0E40 0C5Ch
00400C60h	PCIE_CORE_RP_ADDR0		0D40 0C60h	0DC0 0C60h	0E40 0C60h
00400C64h	PCIE_CORE_RP_ADDR1		0D40 0C64h	0DC0 0C64h	0E40 0C64h
00400C68h	PCIE_CORE_RP_ADDR0		0D40 0C68h	0DC0 0C68h	0E40 0C68h
00400C6Ch	PCIE_CORE_RP_ADDR1		0D40 0C6Ch	0DC0 0C6Ch	0E40 0C6Ch
00400C70h	PCIE_CORE_RP_ADDR0		0D40 0C70h	0DC0 0C70h	0E40 0C70h
00400C74h	PCIE_CORE_RP_ADDR1		0D40 0C74h	0DC0 0C74h	0E40 0C74h
00400C78h	PCIE_CORE_RP_ADDR0		0D40 0C78h	0DC0 0C78h	0E40 0C78h
00400C7Ch	PCIE_CORE_RP_ADDR1		0D40 0C7Ch	0DC0 0C7Ch	0E40 0C7Ch
00400C80h	PCIE_CORE_RP_ADDR0		0D40 0C80h	0DC0 0C80h	0E40 0C80h
00400C84h	PCIE_CORE_RP_ADDR1		0D40 0C84h	0DC0 0C84h	0E40 0C84h
00400C88h	PCIE_CORE_RP_ADDR0		0D40 0C88h	0DC0 0C88h	0E40 0C88h
00400C8Ch	PCIE_CORE_RP_ADDR1		0D40 0C8Ch	0DC0 0C8Ch	0E40 0C8Ch
00400C90h	PCIE_CORE_RP_ADDR0		0D40 0C90h	0DC0 0C90h	0E40 0C90h
00400C94h	PCIE_CORE_RP_ADDR1		0D40 0C94h	0DC0 0C94h	0E40 0C94h
00400C98h	PCIE_CORE_RP_ADDR0		0D40 0C98h	0DC0 0C98h	0E40 0C98h
00400C9Ch	PCIE_CORE_RP_ADDR1		0D40 0C9Ch	0DC0 0C9Ch	0E40 0C9Ch
00400CA0h	PCIE_CORE_RP_ADDR0		0D40 0CA0h	0DC0 0CA0h	0E40 0CA0h
00400CA4h	PCIE_CORE_RP_ADDR1		0D40 0CA4h	0DC0 0CA4h	0E40 0CA4h
00400CA8h	PCIE_CORE_RP_ADDR0		0D40 0CA8h	0DC0 0CA8h	0E40 0CA8h
00400CACH	PCIE_CORE_RP_ADDR1		0D40 0CACH	0DC0 0CACH	0E40 0CACH
00400CB0h	PCIE_CORE_RP_ADDR0		0D40 0CB0h	0DC0 0CB0h	0E40 0CB0h
00400CB4h	PCIE_CORE_RP_ADDR1		0D40 0CB4h	0DC0 0CB4h	0E40 0CB4h
00400CB8h	PCIE_CORE_RP_ADDR0		0D40 0CB8h	0DC0 0CB8h	0E40 0CB8h
00400CBCh	PCIE_CORE_RP_ADDR1		0D40 0CBCh	0DC0 0CBCh	0E40 0CBCh
00400CC0h	PCIE_CORE_RP_ADDR0		0D40 0CC0h	0DC0 0CC0h	0E40 0CC0h
00400CC4h	PCIE_CORE_RP_ADDR1		0D40 0CC4h	0DC0 0CC4h	0E40 0CC4h
00400CC8h	PCIE_CORE_RP_ADDR0		0D40 0CC8h	0DC0 0CC8h	0E40 0CC8h
00400CCCh	PCIE_CORE_RP_ADDR1		0D40 0CCCh	0DC0 0CCCh	0E40 0CCCh
00400CD0h	PCIE_CORE_RP_ADDR0		0D40 0CD0h	0DC0 0CD0h	0E40 0CD0h
00400CD4h	PCIE_CORE_RP_ADDR1		0D40 0CD4h	0DC0 0CD4h	0E40 0CD4h
00400CD8h	PCIE_CORE_RP_ADDR0		0D40 0CD8h	0DC0 0CD8h	0E40 0CD8h
00400CDCh	PCIE_CORE_RP_ADDR1		0D40 0CDCh	0DC0 0CDCh	0E40 0CDCh
00400CE0h	PCIE_CORE_RP_ADDR0		0D40 0CE0h	0DC0 0CE0h	0E40 0CE0h
00400CE4h	PCIE_CORE_RP_ADDR1		0D40 0CE4h	0DC0 0CE4h	0E40 0CE4h
00400CE8h	PCIE_CORE_RP_ADDR0		0D40 0CE8h	0DC0 0CE8h	0E40 0CE8h
00400CECh	PCIE_CORE_RP_ADDR1		0D40 0CECh	0DC0 0CECh	0E40 0CECh
00400CF0h	PCIE_CORE_RP_ADDR0		0D40 0CF0h	0DC0 0CF0h	0E40 0CF0h
00400CF4h	PCIE_CORE_RP_ADDR1		0D40 0CF4h	0DC0 0CF4h	0E40 0CF4h
00400CF8h	PCIE_CORE_RP_ADDR0		0D40 0CF8h	0DC0 0CF8h	0E40 0CF8h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE1_CORE _DBN_CFG_ PCIE_CORE Physical Address	PCIE2_CORE _DBN_CFG_ PCIE_CORE Physical Address
00400CFCh	PCIE_CORE_RP_ADDR1		0D40 0CFCh	0DC0 0CFCh	0E40 0CFCh
00400D00h	PCIE_CORE_RP_ADDR0		0D40 0D00h	0DC0 0D00h	0E40 0D00h
00400D04h	PCIE_CORE_RP_ADDR1		0D40 0D04h	0DC0 0D04h	0E40 0D04h
00400D08h	PCIE_CORE_RP_ADDR0		0D40 0D08h	0DC0 0D08h	0E40 0D08h
00400D0Ch	PCIE_CORE_RP_ADDR1		0D40 0D0Ch	0DC0 0D0Ch	0E40 0D0Ch
00400D10h	PCIE_CORE_RP_ADDR0		0D40 0D10h	0DC0 0D10h	0E40 0D10h
00400D14h	PCIE_CORE_RP_ADDR1		0D40 0D14h	0DC0 0D14h	0E40 0D14h
00400D18h	PCIE_CORE_RP_ADDR0		0D40 0D18h	0DC0 0D18h	0E40 0D18h
00400D1Ch	PCIE_CORE_RP_ADDR1		0D40 0D1Ch	0DC0 0D1Ch	0E40 0D1Ch
00400D20h	PCIE_CORE_RP_ADDR0		0D40 0D20h	0DC0 0D20h	0E40 0D20h
00400D24h	PCIE_CORE_RP_ADDR1		0D40 0D24h	0DC0 0D24h	0E40 0D24h
00400D28h	PCIE_CORE_RP_ADDR0		0D40 0D28h	0DC0 0D28h	0E40 0D28h
00400D2Ch	PCIE_CORE_RP_ADDR1		0D40 0D2Ch	0DC0 0D2Ch	0E40 0D2Ch
00400D30h	PCIE_CORE_RP_ADDR0		0D40 0D30h	0DC0 0D30h	0E40 0D30h
00400D34h	PCIE_CORE_RP_ADDR1		0D40 0D34h	0DC0 0D34h	0E40 0D34h
00400D38h	PCIE_CORE_RP_ADDR0		0D40 0D38h	0DC0 0D38h	0E40 0D38h
00400D3Ch	PCIE_CORE_RP_ADDR1		0D40 0D3Ch	0DC0 0D3Ch	0E40 0D3Ch
00400D40h	PCIE_CORE_RP_ADDR0		0D40 0D40h	0DC0 0D40h	0E40 0D40h
00400D44h	PCIE_CORE_RP_ADDR1		0D40 0D44h	0DC0 0D44h	0E40 0D44h
00400D48h	PCIE_CORE_RP_ADDR0		0D40 0D48h	0DC0 0D48h	0E40 0D48h
00400D4Ch	PCIE_CORE_RP_ADDR1		0D40 0D4Ch	0DC0 0D4Ch	0E40 0D4Ch
00400D50h	PCIE_CORE_RP_ADDR0		0D40 0D50h	0DC0 0D50h	0E40 0D50h
00400D54h	PCIE_CORE_RP_ADDR1		0D40 0D54h	0DC0 0D54h	0E40 0D54h
00400D58h	PCIE_CORE_RP_ADDR0		0D40 0D58h	0DC0 0D58h	0E40 0D58h
00400D5Ch	PCIE_CORE_RP_ADDR1		0D40 0D5Ch	0DC0 0D5Ch	0E40 0D5Ch
00400D60h	PCIE_CORE_RP_ADDR0		0D40 0D60h	0DC0 0D60h	0E40 0D60h
00400D64h	PCIE_CORE_RP_ADDR1		0D40 0D64h	0DC0 0D64h	0E40 0D64h
00400D68h	PCIE_CORE_RP_ADDR0		0D40 0D68h	0DC0 0D68h	0E40 0D68h
00400D6Ch	PCIE_CORE_RP_ADDR1		0D40 0D6Ch	0DC0 0D6Ch	0E40 0D6Ch
00400D70h	PCIE_CORE_RP_ADDR0		0D40 0D70h	0DC0 0D70h	0E40 0D70h
00400D74h	PCIE_CORE_RP_ADDR1		0D40 0D74h	0DC0 0D74h	0E40 0D74h
00400D78h	PCIE_CORE_RP_ADDR0		0D40 0D78h	0DC0 0D78h	0E40 0D78h
00400D7Ch	PCIE_CORE_RP_ADDR1		0D40 0D7Ch	0DC0 0D7Ch	0E40 0D7Ch
00400D80h	PCIE_CORE_RP_ADDR0		0D40 0D80h	0DC0 0D80h	0E40 0D80h
00400D84h	PCIE_CORE_RP_ADDR1		0D40 0D84h	0DC0 0D84h	0E40 0D84h
00400D88h	PCIE_CORE_RP_ADDR0		0D40 0D88h	0DC0 0D88h	0E40 0D88h
00400D8Ch	PCIE_CORE_RP_ADDR1		0D40 0D8Ch	0DC0 0D8Ch	0E40 0D8Ch
00400D90h	PCIE_CORE_RP_ADDR0		0D40 0D90h	0DC0 0D90h	0E40 0D90h
00400D94h	PCIE_CORE_RP_ADDR1		0D40 0D94h	0DC0 0D94h	0E40 0D94h
00400D98h	PCIE_CORE_RP_ADDR0		0D40 0D98h	0DC0 0D98h	0E40 0D98h
00400D9Ch	PCIE_CORE_RP_ADDR1		0D40 0D9Ch	0DC0 0D9Ch	0E40 0D9Ch
00400DA0h	PCIE_CORE_RP_ADDR0		0D40 0DA0h	0DC0 0DA0h	0E40 0DA0h
00400DA4h	PCIE_CORE_RP_ADDR1		0D40 0DA4h	0DC0 0DA4h	0E40 0DA4h
00400DA8h	PCIE_CORE_RP_ADDR0		0D40 0DA8h	0DC0 0DA8h	0E40 0DA8h

Table 9-1181. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE0_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE1_CORE_DBN_CFG_PCIE_CORE Physical Address	PCIE2_CORE_DBN_CFG_PCIE_CORE Physical Address
00400DACH	PCIE_CORE_RP_ADDR1		0D40 0DACH	0DC0 0DACH	0E40 0DACH
00400DB0h	PCIE_CORE_RP_ADDR0		0D40 0DB0h	0DC0 0DB0h	0E40 0DB0h
00400DB4h	PCIE_CORE_RP_ADDR1		0D40 0DB4h	0DC0 0DB4h	0E40 0DB4h
00400DB8h	PCIE_CORE_RP_ADDR0		0D40 0DB8h	0DC0 0DB8h	0E40 0DB8h
00400DBCh	PCIE_CORE_RP_ADDR1		0D40 0DBCh	0DC0 0DBCh	0E40 0DBCh

Table 9-1182. PCIE_CORE_RP Registers

Offset	Acronym	Register Name	PCIE3_CORE_DBN_CFG_PCIE_CORE Physical Address	Section
0h	PCIE_CORE_RP_I_VENDOR_ID_DE VICE_ID		0E80 0000h	Section 9.5.1
4h	PCIE_CORE_RP_I_COMMAND_STA TUS		0E80 0004h	Section 9.5.2
8h	PCIE_CORE_RP_I_REVISION_ID_CL ASS_CODE		0E80 0008h	Section 9.5.3
Ch	PCIE_CORE_RP_I_BIST_HEADER_L ATENCY_CACHE_LINE		0E80 000Ch	Section 9.5.4
10h	PCIE_CORE_RP_I_RC_BAR_0		0E80 0010h	Section 9.5.5
14h	PCIE_CORE_RP_I_RC_BAR_1		0E80 0014h	Section 9.5.6
18h	PCIE_CORE_RP_I_PCIE_BUS_NUM BERS		0E80 0018h	Section 9.5.7
1Ch	PCIE_CORE_RP_I_PCIE_IO_BASE_ LIMIT		0E80 001Ch	Section 9.5.8
20h	PCIE_CORE_RP_I_PCIE_MEM_BAS E_LIMIT		0E80 0020h	Section 9.5.9
24h	PCIE_CORE_RP_I_PCIE_PREFETC H_BASE_LIMIT		0E80 0024h	Section 9.5.10
28h	PCIE_CORE_RP_I_PCIE_PREFETC H_BASE_UPPER		0E80 0028h	Section 9.5.11
2Ch	PCIE_CORE_RP_I_PCIE_PREFETC H_LIMIT_UPPER		0E80 002Ch	Section 9.5.12
30h	PCIE_CORE_RP_I_PCIE_IO_BASE_ LIMIT_UPPER		0E80 0030h	Section 9.5.13
34h	PCIE_CORE_RP_I_CAPABILITIES_P OINTER		0E80 0034h	Section 9.5.14
38h	PCIE_CORE_RP_RSVD_0E		0E80 0038h	Section 9.5.15
3Ch	PCIE_CORE_RP_I_INTRPT_LINE_IN TRPT_PIN		0E80 003Ch	Section 9.5.16
80h	PCIE_CORE_RP_I_PWR_MGMT_CA P		0E80 0080h	Section 9.5.17
84h	PCIE_CORE_RP_I_PWR_MGMT_CT RL_STAT_REP		0E80 0084h	Section 9.5.18
90h	PCIE_CORE_RP_I_MSI_CTRL_REG		0E80 0090h	Section 9.5.19
94h	PCIE_CORE_RP_I_MSI_MSG_LOW_ ADDR		0E80 0094h	Section 9.5.20
98h	PCIE_CORE_RP_I_MSI_MSG_HI_AD DR		0E80 0098h	Section 9.5.21

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
9Ch	PCIE_CORE_RP_I_MSI_MSG_DATA		0E80 009Ch	Section 9.5.22
A0h	PCIE_CORE_RP_I_MSI_MASK		0E80 00A0h	Section 9.5.23
A4h	PCIE_CORE_RP_I_MSI_PENDING_B ITS		0E80 00A4h	Section 9.5.24
B0h	PCIE_CORE_RP_I_MSIX_CTRL		0E80 00B0h	Section 9.5.25
B4h	PCIE_CORE_RP_I_MSIX_TBL_OFFS ET		0E80 00B4h	Section 9.5.26
B8h	PCIE_CORE_RP_I_MSIX_PENDING_ INTRPT		0E80 00B8h	Section 9.5.27
C0h	PCIE_CORE_RP_I_PCIE_CAP_LIST		0E80 00C0h	Section 9.5.28
C4h	PCIE_CORE_RP_I_PCIE_CAP		0E80 00C4h	Section 9.5.29
C8h	PCIE_CORE_RP_I_PCIE_DEV_CTRL _STATUS		0E80 00C8h	Section 9.5.30
CCh	PCIE_CORE_RP_I_LINK_CAP		0E80 00CCh	Section 9.5.31
D0h	PCIE_CORE_RP_I_LINK_CTRL_STA TUS		0E80 00D0h	Section 9.5.32
D4h	PCIE_CORE_RP_I_SLOT_CAPABILI TY		0E80 00D4h	Section 9.5.33
D8h	PCIE_CORE_RP_I_SLOT_CTRL_ST ATUS		0E80 00D8h	Section 9.5.34
DCh	PCIE_CORE_RP_I_ROOT_CTRL_CA P		0E80 00DCh	Section 9.5.35
E0h	PCIE_CORE_RP_I_ROOT_STATUS		0E80 00E0h	Section 9.5.36
E4h	PCIE_CORE_RP_I_PCIE_CAP_2		0E80 00E4h	Section 9.5.37
E8h	PCIE_CORE_RP_I_PCIE_DEV_CTRL _STATUS_2		0E80 00E8h	Section 9.5.38
ECh	PCIE_CORE_RP_I_LINK_CAP_2		0E80 00ECh	Section 9.5.39
F0h	PCIE_CORE_RP_I_LINK_CTRL_STA TUS_2		0E80 00F0h	Section 9.5.40
100h	PCIE_CORE_RP_I_AER_ENHNCD_C AP		0E80 0100h	Section 9.5.41
104h	PCIE_CORE_RP_I_UNCORR_ERR_ STATUS		0E80 0104h	Section 9.5.42
108h	PCIE_CORE_RP_I_UNCORR_ERR_ MASK		0E80 0108h	Section 9.5.43
10Ch	PCIE_CORE_RP_I_UNCORR_ERR_ SEVERITY		0E80 010Ch	Section 9.5.44
110h	PCIE_CORE_RP_I_CORR_ERR_STA TUS		0E80 0110h	Section 9.5.45
114h	PCIE_CORE_RP_I_CORR_ERR_MA SK		0E80 0114h	Section 9.5.46

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
118h	PCIE_CORE_RP_I_ADV_ERR_CAP_CTL		0E80 0118h	Section 9.5.47
11Ch	PCIE_CORE_RP_I_HDR_LOG_0		0E80 011Ch	Section 9.5.48
120h	PCIE_CORE_RP_I_HDR_LOG_1		0E80 0120h	Section 9.5.49
124h	PCIE_CORE_RP_I_HDR_LOG_2		0E80 0124h	Section 9.5.50
128h	PCIE_CORE_RP_I_HDR_LOG_3		0E80 0128h	Section 9.5.51
12Ch	PCIE_CORE_RP_I_ROOT_ERR_CM D		0E80 012Ch	Section 9.5.52
130h	PCIE_CORE_RP_I_ROOT_ERR_STA T		0E80 0130h	Section 9.5.53
134h	PCIE_CORE_RP_I_ERR_SRC_ID		0E80 0134h	Section 9.5.54
138h	PCIE_CORE_RP_I_TLP_PRE_LOG_ 0		0E80 0138h	Section 9.5.55
150h	PCIE_CORE_RP_I_DEV_SER_NUM_ CAP_HDR		0E80 0150h	Section 9.5.56
154h	PCIE_CORE_RP_I_DEV_SER_NUM_ 0		0E80 0154h	Section 9.5.57
158h	PCIE_CORE_RP_I_DEV_SER_NUM_ 1		0E80 0158h	Section 9.5.58
300h	PCIE_CORE_RP_I_SEC_PCIE_CAP_ HDR_REG		0E80 0300h	Section 9.5.59
304h	PCIE_CORE_RP_I_LINK_CONTROL 3		0E80 0304h	Section 9.5.60
308h	PCIE_CORE_RP_I_LANE_ERROR_S TATUS		0E80 0308h	Section 9.5.61
30Ch	PCIE_CORE_RP_I_LANE_EQUALIZA TION_CONTROL_0		0E80 030Ch	Section 9.5.62
4C0h	PCIE_CORE_RP_I_VC_ENH_CAP_H EADER_REG		0E80 04C0h	Section 9.5.63
4C4h	PCIE_CORE_RP_I_PORT_VC_CAP_ REG_1		0E80 04C4h	Section 9.5.64
4C8h	PCIE_CORE_RP_I_PORT_VC_CAP_ REG_2		0E80 04C8h	Section 9.5.65
4CCh	PCIE_CORE_RP_I_PORT_VC_CTRL_ STS_REG		0E80 04CCh	Section 9.5.66
4D0h	PCIE_CORE_RP_I_VC_RES_CAP_R EG_0		0E80 04D0h	Section 9.5.67
4D4h	PCIE_CORE_RP_I_VC_RES_CTRL_ REG_0		0E80 04D4h	Section 9.5.68
4D8h	PCIE_CORE_RP_I_VC_RES_STS_R EG_0		0E80 04D8h	Section 9.5.69
4DCh	PCIE_CORE_RP_I_VC_RES_CAP_R EG_1		0E80 04DCh	Section 9.5.70
4E0h	PCIE_CORE_RP_I_VC_RES_CTRL_ REG_1		0E80 04E0h	Section 9.5.71
4E4h	PCIE_CORE_RP_I_VC_RES_STS_R EG_1		0E80 04E4h	Section 9.5.72
4E8h	PCIE_CORE_RP_I_VC_RES_CAP_R EG_2		0E80 04E8h	Section 9.5.73

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
4ECh	PCIE_CORE_RP_I_VC_RES_CTRL_REG_2		0E80 04ECh	Section 9.5.74
4F0h	PCIE_CORE_RP_I_VC_RES_STS_REG_2		0E80 04F0h	Section 9.5.75
4F4h	PCIE_CORE_RP_I_VC_RES_CAP_REG_3		0E80 04F4h	Section 9.5.76
4F8h	PCIE_CORE_RP_I_VC_RES_CTRL_REG_3		0E80 04F8h	Section 9.5.77
4FCh	PCIE_CORE_RP_I_VC_RES_STS_REG_3		0E80 04FCh	Section 9.5.78
900h	PCIE_CORE_RP_I_L1_PM_EXT_CAP_HDR		0E80 0900h	Section 9.5.79
904h	PCIE_CORE_RP_I_L1_PM_CAP		0E80 0904h	Section 9.5.80
908h	PCIE_CORE_RP_I_L1_PM_CTRL_1		0E80 0908h	Section 9.5.81
90Ch	PCIE_CORE_RP_I_L1_PM_CTRL_2		0E80 090Ch	Section 9.5.82
910h	PCIE_CORE_RP_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG		0E80 0910h	Section 9.5.83
914h	PCIE_CORE_RP_I_DL_FEATURE_CAPABILITIES_REG		0E80 0914h	Section 9.5.84
918h	PCIE_CORE_RP_I_DL_FEATURE_STATUS_REG		0E80 0918h	Section 9.5.85
920h	PCIE_CORE_RP_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG		0E80 0920h	Section 9.5.86
924h	PCIE_CORE_RP_I_MARGINING_PORT_CAPABILITIES_STATUS_REG		0E80 0924h	Section 9.5.87
928h	PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG0		0E80 0928h	Section 9.5.88
92Ch	PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG1		0E80 092Ch	Section 9.5.89
9C0h	PCIE_CORE_RP_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG		0E80 09C0h	Section 9.5.90
9C4h	PCIE_CORE_RP_I_PL_16GTS_CAPABILITIES_REG		0E80 09C4h	Section 9.5.91
9C8h	PCIE_CORE_RP_I_PL_16GTS_CONTROL_REG		0E80 09C8h	Section 9.5.92
9CCh	PCIE_CORE_RP_I_PL_16GTS_STATUS_REG		0E80 09CCh	Section 9.5.93
9D0h	PCIE_CORE_RP_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG		0E80 09D0h	Section 9.5.94
9D4h	PCIE_CORE_RP_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG		0E80 09D4h	Section 9.5.95
9D8h	PCIE_CORE_RP_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG		0E80 09D8h	Section 9.5.96
9DCh	PCIE_CORE_RP_I_PL_16GTS_RESERVED_REG		0E80 09DCh	Section 9.5.97

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
9E0h	PCIE_CORE_RP_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0		0E80 09E0h	Section 9.5.98
A20h	PCIE_CORE_RP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG		0E80 0A20h	Section 9.5.99
A24h	PCIE_CORE_RP_I_PTM_CAPABILITYES_REG		0E80 0A24h	Section 9.5.100
A28h	PCIE_CORE_RP_I_PTM_CONTROL_REG		0E80 0A28h	Section 9.5.101
00100000h	PCIE_CORE_RP_I_PL_CONFIG_0_REG		0E90 0000h	Section 9.5.102
00100004h	PCIE_CORE_RP_I_PL_CONFIG_1_REG		0E90 0004h	Section 9.5.103
00100008h	PCIE_CORE_RP_I_DLL_TMR_CONFIG_REG		0E90 0008h	Section 9.5.104
0010000Ch	PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG		0E90 000Ch	Section 9.5.105
00100010h	PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG		0E90 0010h	Section 9.5.106
00100014h	PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG		0E90 0014h	Section 9.5.107
00100018h	PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG		0E90 0018h	Section 9.5.108
0010001Ch	PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG		0E90 001Ch	Section 9.5.109
00100020h	PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG		0E90 0020h	Section 9.5.110
00100024h	PCIE_CORE_RP_I_L0S_TIMEOUT_LIMIT_REG		0E90 0024h	Section 9.5.111
00100028h	PCIE_CORE_RP_I_TRANSMIT_TLP_COUNT_REG		0E90 0028h	Section 9.5.112
0010002Ch	PCIE_CORE_RP_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG		0E90 002Ch	Section 9.5.113
00100030h	PCIE_CORE_RP_I_RECEIVE_TLP_COUNT_REG		0E90 0030h	Section 9.5.114
00100034h	PCIE_CORE_RP_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG		0E90 0034h	Section 9.5.115
00100038h	PCIE_CORE_RP_I_COMPLN_TMOU_T_LIM_0_REG		0E90 0038h	Section 9.5.116
0010003Ch	PCIE_CORE_RP_I_COMPLN_TMOU_T_LIM_1_REG		0E90 003Ch	Section 9.5.117
00100040h	PCIE_CORE_RP_I_L1_ST_REENTRY_DELAY_REG		0E90 0040h	Section 9.5.118
00100044h	PCIE_CORE_RP_I_VENDOR_ID_REG		0E90 0044h	Section 9.5.119
00100048h	PCIE_CORE_RP_I_ASPM_L1_ENTR_Y_TMOUT_DELAY_REG		0E90 0048h	Section 9.5.120
0010004Ch	PCIE_CORE_RP_I_PME_TURNOFF_ACK_DELAY_REG		0E90 004Ch	Section 9.5.121
00100050h	PCIE_CORE_RP_I_LINKWIDTH_CONTROL_REG		0E90 0050h	Section 9.5.122

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00100070h	PCIE_CORE_RP_I_MULTI_VC_CON ROL_REG		0E90 0070h	Section 9.5.123
00100074h	PCIE_CORE_RP_I_SRIS_CONTROL _REG		0E90 0074h	Section 9.5.124
00100080h	PCIE_CORE_RP_I_RCV_CRED_LIM _0_REG_VC1		0E90 0080h	Section 9.5.125
00100084h	PCIE_CORE_RP_I_RCV_CRED_LIM _1_REG_VC1		0E90 0084h	Section 9.5.126
00100088h	PCIE_CORE_RP_I_TRANSM_CRED_ LIM_0_REG_VC1		0E90 0088h	Section 9.5.127
0010008Ch	PCIE_CORE_RP_I_TRANSM_CRED_ LIM_1_REG_VC1		0E90 008Ch	Section 9.5.128
00100090h	PCIE_CORE_RP_I_RCV_CRED_LIM _0_REG_VC2		0E90 0090h	Section 9.5.129
00100094h	PCIE_CORE_RP_I_RCV_CRED_LIM _1_REG_VC2		0E90 0094h	Section 9.5.130
00100098h	PCIE_CORE_RP_I_TRANSM_CRED_ LIM_0_REG_VC2		0E90 0098h	Section 9.5.131
0010009Ch	PCIE_CORE_RP_I_TRANSM_CRED_ LIM_1_REG_VC2		0E90 009Ch	Section 9.5.132
001000A0h	PCIE_CORE_RP_I_RCV_CRED_LIM _0_REG_VC3		0E90 00A0h	Section 9.5.133
001000A4h	PCIE_CORE_RP_I_RCV_CRED_LIM _1_REG_VC3		0E90 00A4h	Section 9.5.134
001000A8h	PCIE_CORE_RP_I_TRANSM_CRED_ LIM_0_REG_VC3		0E90 00A8h	Section 9.5.135
001000ACh	PCIE_CORE_RP_I_TRANSM_CRED_ LIM_1_REG_VC3		0E90 00ACh	Section 9.5.136
001000F0h	PCIE_CORE_RP_I_FC_INIT_DELAY_ REG		0E90 00F0h	Section 9.5.137
00100100h	PCIE_CORE_RP_I_SHDW_HDR_LO G_0_REG		0E90 0100h	Section 9.5.138
00100104h	PCIE_CORE_RP_I_SHDW_HDR_LO G_1_REG		0E90 0104h	Section 9.5.139
00100108h	PCIE_CORE_RP_I_SHDW_HDR_LO G_2_REG		0E90 0108h	Section 9.5.140
0010010Ch	PCIE_CORE_RP_I_SHDW_HDR_LO G_3_REG		0E90 010Ch	Section 9.5.141
00100110h	PCIE_CORE_RP_I_SHDW_FUNC_N UM_REG		0E90 0110h	Section 9.5.142
00100114h	PCIE_CORE_RP_I_SHDW_UR_ERR _REG		0E90 0114h	Section 9.5.143
00100140h	PCIE_CORE_RP_I_PM_CLK_FREQU ENCY_REG		0E90 0140h	Section 9.5.144
00100144h	PCIE_CORE_RP_I_DEBUG_DLLP_C OUNT_GEN1_REG		0E90 0144h	Section 9.5.145
00100148h	PCIE_CORE_RP_I_DEBUG_DLLP_C OUNT_GEN2_REG		0E90 0148h	Section 9.5.146
0010014Ch	PCIE_CORE_RP_I_DEBUG_DLLP_C OUNT_GEN3_REG		0E90 014Ch	Section 9.5.147

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00100150h	PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN4_REG		0E90 0150h	Section 9.5.148
00100158h	PCIE_CORE_RP_I_VENDOR_DEFINED_MESSAGE_TAG_REG		0E90 0158h	Section 9.5.149
00100200h	PCIE_CORE_RP_I_NEGOTIATED_LANE_MAP_REG		0E90 0200h	Section 9.5.150
00100204h	PCIE_CORE_RP_I_RECEIVE_FTS_COUNT_REG		0E90 0204h	Section 9.5.151
00100208h	PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_REG		0E90 0208h	Section 9.5.152
0010020Ch	PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGISTER		0E90 020Ch	Section 9.5.153
00100210h	PCIE_CORE_RP_I_LOCAL_INTRPT_MASK_REG		0E90 0210h	Section 9.5.154
00100214h	PCIE_CORE_RP_I_LCRC_ERR_COUNT_REG		0E90 0214h	Section 9.5.155
00100218h	PCIE_CORE_RP_I_ECC_CORR_ERR_COUNT_REG		0E90 0218h	Section 9.5.156
0010021Ch	PCIE_CORE_RP_I_LTR_SNOOP_LAT_REG		0E90 021Ch	Section 9.5.157
00100220h	PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_REG		0E90 0220h	Section 9.5.158
00100224h	PCIE_CORE_RP_I_PME_SERVICE_TIMEOUT_DELAY_REG		0E90 0224h	Section 9.5.159
00100228h	PCIE_CORE_RP_I_ROOT_PORT_REQUESTOR_ID_REG		0E90 0228h	Section 9.5.160
0010022Ch	PCIE_CORE_RP_I_EP_BUS_DEVICE_NUMBER_REG		0E90 022Ch	Section 9.5.161
00100234h	PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG		0E90 0234h	Section 9.5.162
00100238h	PCIE_CORE_RP_I_PHY_STATUS_1_REG		0E90 0238h	Section 9.5.163
00100240h	PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG		0E90 0240h	Section 9.5.164
00100244h	PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG		0E90 0244h	Section 9.5.165
00100248h	PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG		0E90 0248h	Section 9.5.166
0010024Ch	PCIE_CORE_RP_I_PF_1_BAR_CONFIG_1_REG		0E90 024Ch	Section 9.5.167
00100250h	PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG		0E90 0250h	Section 9.5.168
00100254h	PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG		0E90 0254h	Section 9.5.169
00100258h	PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG		0E90 0258h	Section 9.5.170
0010025Ch	PCIE_CORE_RP_I_PF_3_BAR_CONFIG_1_REG		0E90 025Ch	Section 9.5.171
00100260h	PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG		0E90 0260h	Section 9.5.172

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00100264h	PCIE_CORE_RP_I_PF_4_BAR_CON FIG_1_REG		0E90 0264h	Section 9.5.173
00100268h	PCIE_CORE_RP_I_PF_5_BAR_CON FIG_0_REG		0E90 0268h	Section 9.5.174
0010026Ch	PCIE_CORE_RP_I_PF_5_BAR_CON FIG_1_REG		0E90 026Ch	Section 9.5.175
00100280h	PCIE_CORE_RP_I_PF_0_VF_BAR_C ONFIG_0_REG		0E90 0280h	Section 9.5.176
00100284h	PCIE_CORE_RP_I_PF_0_VF_BAR_C ONFIG_1_REG		0E90 0284h	Section 9.5.177
00100288h	PCIE_CORE_RP_I_PF_1_VF_BAR_C ONFIG_0_REG		0E90 0288h	Section 9.5.178
0010028Ch	PCIE_CORE_RP_I_PF_1_VF_BAR_C ONFIG_1_REG		0E90 028Ch	Section 9.5.179
00100290h	PCIE_CORE_RP_I_PF_2_VF_BAR_C ONFIG_0_REG		0E90 0290h	Section 9.5.180
00100294h	PCIE_CORE_RP_I_PF_2_VF_BAR_C ONFIG_1_REG		0E90 0294h	Section 9.5.181
00100298h	PCIE_CORE_RP_I_PF_3_VF_BAR_C ONFIG_0_REG		0E90 0298h	Section 9.5.182
0010029Ch	PCIE_CORE_RP_I_PF_3_VF_BAR_C ONFIG_1_REG		0E90 029Ch	Section 9.5.183
001002A0h	PCIE_CORE_RP_I_PF_4_VF_BAR_C ONFIG_0_REG		0E90 02A0h	Section 9.5.184
001002A4h	PCIE_CORE_RP_I_PF_4_VF_BAR_C ONFIG_1_REG		0E90 02A4h	Section 9.5.185
001002A8h	PCIE_CORE_RP_I_PF_5_VF_BAR_C ONFIG_0_REG		0E90 02A8h	Section 9.5.186
001002ACh	PCIE_CORE_RP_I_PF_5_VF_BAR_C ONFIG_1_REG		0E90 02ACh	Section 9.5.187
001002C0h	PCIE_CORE_RP_I_PF_CONFIG_RE G		0E90 02C0h	Section 9.5.188
00100300h	PCIE_CORE_RP_I_RC_BAR_CONFI G_REG		0E90 0300h	Section 9.5.189
00100360h	PCIE_CORE_RP_I_GEN3_DEFAULT _PRESET_REG		0E90 0360h	Section 9.5.190
00100364h	PCIE_CORE_RP_I_GEN3_GEN4_LIN K_EQ_TIMEOUT_2MS_REG		0E90 0364h	Section 9.5.191
00100368h	PCIE_CORE_RP_I_PIPE_FIFO_LATE NCY_CTRL_REG		0E90 0368h	Section 9.5.192
00100374h	PCIE_CORE_RP_I_GEN4_DEFAULT _PRESET_REG		0E90 0374h	Section 9.5.193
00100378h	PCIE_CORE_RP_I_PHY_CONFIG_R EG3		0E90 0378h	Section 9.5.194
0010037Ch	PCIE_CORE_RP_I_GEN3_GEN4_LIN K_EQ_CTRL_REG		0E90 037Ch	Section 9.5.195
00100380h	PCIE_CORE_RP_I_GEN3_LINK_EQ_ DEBUG_STATUS_REG_LANE0		0E90 0380h	Section 9.5.196
00100384h	PCIE_CORE_RP_I_GEN3_LINK_EQ_ DEBUG_STATUS_REG_LANE1		0E90 0384h	Section 9.5.197

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
001003C0h	PCIE_CORE_RP_I_GEN4_LINK_EQ_ DEBUG_STATUS_REG_LANE0		0E90 03C0h	Section 9.5.198
001003C4h	PCIE_CORE_RP_I_GEN4_LINK_EQ_ DEBUG_STATUS_REG_LANE1		0E90 03C4h	Section 9.5.199
00100C80h	PCIE_CORE_RP_I_ECC_CORR_ER R_COUNT_REG_AXI		0E90 0C80h	Section 9.5.200
00100C88h	PCIE_CORE_RP_LOW_POWER_DE BUG_AND_CONTROL0		0E90 0C88h	Section 9.5.201
00100C8Ch	PCIE_CORE_RP_LOW_POWER_DE BUG_AND_CONTROL1		0E90 0C8Ch	Section 9.5.202
00100C90h	PCIE_CORE_RP_LOW_POWER_DE BUG_AND_CONTROL2		0E90 0C90h	Section 9.5.203
00100C94h	PCIE_CORE_RP_TL_INTERNAL_CO NTROL		0E90 0C94h	Section 9.5.204
00100C98h	PCIE_CORE_RP_I_DTI_ATS_STATU S		0E90 0C98h	Section 9.5.205
00100C9Ch	PCIE_CORE_RP_I_DTI_ATS_CTRL		0E90 0C9Ch	Section 9.5.206
00100CC0h	PCIE_CORE_RP_I_SCALED_FLOW_ CONTROL_MGMT_VC_SELECT_RE G		0E90 0CC0h	Section 9.5.207
00100CC4h	PCIE_CORE_RP_I_SCALED_FLOW_ CONTROL_MGMT_REG		0E90 0CC4h	Section 9.5.208
00100CD0h	PCIE_CORE_RP_I_MARGINING_PA RAMETERS_1_REG		0E90 0CD0h	Section 9.5.209
00100CD4h	PCIE_CORE_RP_I_MARGINING_PA RAMETERS_2_REG		0E90 0CD4h	Section 9.5.210
00100CD8h	PCIE_CORE_RP_I_MARGINING_LO CAL_CONTROL_REG		0E90 0CD8h	Section 9.5.211
00100CDCh	PCIE_CORE_RP_I_MARGINING_ER ROR_STATUS1_REG		0E90 0CDCh	Section 9.5.212
00100CE0h	PCIE_CORE_RP_I_MARGINING_ER ROR_STATUS2_REG		0E90 0CE0h	Section 9.5.213
00100D00h	PCIE_CORE_RP_I_LOCAL_ERROR_ STATUS_2_REGISTER		0E90 0D00h	Section 9.5.214
00100D04h	PCIE_CORE_RP_I_LOCAL_INTRPT_ MASK_2_REG		0E90 0D04h	Section 9.5.215
00100D10h	PCIE_CORE_RP_MSI_MASK_CLEA RED_STATUS_1		0E90 0D10h	Section 9.5.216
00100D14h	PCIE_CORE_RP_MSI_MASK_SET_S TATUS_1		0E90 0D14h	Section 9.5.217
00100D18h	PCIE_CORE_RP_MSIX_FUNCTION_ MASK_CLEARED_STATUS_1		0E90 0D18h	Section 9.5.218
00100D1Ch	PCIE_CORE_RP_MSIX_FUNCTION_ MASK_SET_STATUS_1		0E90 0D1Ch	Section 9.5.219
00100DA0h	PCIE_CORE_RP_I_LD_CTRL		0E90 0DA0h	Section 9.5.220
00100DA4h	PCIE_CORE_RP_RX_ELEC_IDLE_FI LTER_CONTROL		0E90 0DA4h	Section 9.5.221
00100DA8h	PCIE_CORE_RP_I_PTM_LOCAL_CO NTROL_REG		0E90 0DA8h	Section 9.5.222

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00100DAC h	PCIE_CORE_RP_I_PTM_LOCAL_ST ATUS_REG		0E90 0DACh	Section 9.5.223
00100DB0h	PCIE_CORE_RP_I_PTM_LATENCY_ PARAMETERS_INDEX_REG		0E90 0DB0h	Section 9.5.224
00100DB4h	PCIE_CORE_RP_I_PTM_LATENCY_ PARAMETERS_REG		0E90 0DB4h	Section 9.5.225
00100DB8h	PCIE_CORE_RP_I_PTM_CONTEXT_ 1_REG		0E90 0DB8h	Section 9.5.226
00100DBC h	PCIE_CORE_RP_I_PTM_CONTEXT_ 2_REG		0E90 0DBCCh	Section 9.5.227
00100DC0h	PCIE_CORE_RP_I_PTM_CONTEXT_ 3_REG		0E90 0DC0h	Section 9.5.228
00100DC4h	PCIE_CORE_RP_I_PTM_CONTEXT_ 4_REG		0E90 0DC4h	Section 9.5.229
00100DC8h	PCIE_CORE_RP_I_PTM_CONTEXT_ 5_REG		0E90 0DC8h	Section 9.5.230
00100DCC h	PCIE_CORE_RP_I_PTM_CONTEXT_ 6_REG		0E90 0DCCCh	Section 9.5.231
00100DD0h	PCIE_CORE_RP_I_PTM_CONTEXT_ 7_REG		0E90 0DD0h	Section 9.5.232
00100DD4h	PCIE_CORE_RP_I_PTM_CONTEXT_ 8_REG		0E90 0DD4h	Section 9.5.233
00100DD8h	PCIE_CORE_RP_I_PTM_CONTEXT_ 9_REG		0E90 0DD8h	Section 9.5.234
00100DDC h	PCIE_CORE_RP_I_PTM_CONTEXT_ 10_REG		0E90 0DDCh	Section 9.5.235
00100DE0h	PCIE_CORE_RP_I_PTM_CONTEXT_ 11_REG		0E90 0DE0h	Section 9.5.236
00100DEC h	PCIE_CORE_RP_I_ASF_INTRPT_ST ATUS		0E90 0DECCh	Section 9.5.237
00100DF0h	PCIE_CORE_RP_I_ASF_INTRPT_RA W_STATUS		0E90 0DF0h	Section 9.5.238
00100DF4h	PCIE_CORE_RP_I_ASF_INTRPT_MA SK_REG		0E90 0DF4h	Section 9.5.239
00100DF8h	PCIE_CORE_RP_I_ASF_INTRPT_TE ST		0E90 0DF8h	Section 9.5.240
00100DFCh	PCIE_CORE_RP_I_ASF_INTRPT_FA TAL_NONFATAL_SEL		0E90 0DFCh	Section 9.5.241
00100E00h	PCIE_CORE_RP_I_ASF_SRAM_COR R_FAULT_STATUS		0E90 0E00h	Section 9.5.242
00100E04h	PCIE_CORE_RP_I_ASF_SRAM_UNC ORR_FAULT_STATUS		0E90 0E04h	Section 9.5.243
00100E08h	PCIE_CORE_RP_I_ASF_SRAM_FAU LT_STATISTICS		0E90 0E08h	Section 9.5.244
00100E0Ch	PCIE_CORE_RP_I_ASF_TRANS_TO _CTRL		0E90 0E0Ch	Section 9.5.245
00100E10h	PCIE_CORE_RP_I_ASF_TRANS_TO _FAULT_MASK		0E90 0E10h	Section 9.5.246
00100E14h	PCIE_CORE_RP_I_ASF_TRANS_TO _FAULT_STATUS		0E90 0E14h	Section 9.5.247

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00100E18h	PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_MASK		0E90 0E18h	Section 9.5.248
00100E1Ch	PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_STATUS_REG		0E90 0E1Ch	Section 9.5.249
00100E20h	PCIE_CORE_RP_DUAL_TL_CTRL		0E90 0E20h	Section 9.5.250
00100E40h	PCIE_CORE_RP_I_ASF_MAGIC_NUM_CTRLER_VER_REG		0E90 0E40h	Section 9.5.251
00400000h	PCIE_CORE_RP_ADDR0		0EC0 0000h	Section 9.5.252
00400004h	PCIE_CORE_RP_ADDR1		0EC0 0004h	Section 9.5.253
00400008h	PCIE_CORE_RP_DESC0		0EC0 0008h	Section 9.5.254
0040000Ch	PCIE_CORE_RP_DESC1		0EC0 000Ch	Section 9.5.255
00400014h	PCIE_CORE_RP_DESC3		0EC0 0014h	Section 9.5.256
00400018h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0018h	Section 9.5.257
0040001Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 001Ch	Section 9.5.258
00400020h	PCIE_CORE_RP_ADDR0		0EC0 0020h	Section 9.5.259
00400024h	PCIE_CORE_RP_ADDR1		0EC0 0024h	Section 9.5.260
00400028h	PCIE_CORE_RP_DESC0		0EC0 0028h	Section 9.5.261
0040002Ch	PCIE_CORE_RP_DESC1		0EC0 002Ch	Section 9.5.262
00400034h	PCIE_CORE_RP_DESC3		0EC0 0034h	Section 9.5.263
00400038h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0038h	Section 9.5.264
0040003Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 003Ch	Section 9.5.265
00400040h	PCIE_CORE_RP_ADDR0		0EC0 0040h	Section 9.5.266
00400044h	PCIE_CORE_RP_ADDR1		0EC0 0044h	Section 9.5.267
00400048h	PCIE_CORE_RP_DESC0		0EC0 0048h	Section 9.5.268
0040004Ch	PCIE_CORE_RP_DESC1		0EC0 004Ch	Section 9.5.269
00400054h	PCIE_CORE_RP_DESC3		0EC0 0054h	Section 9.5.270
00400058h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0058h	Section 9.5.271
0040005Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 005Ch	Section 9.5.272

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400060h	PCIE_CORE_RP_ADDR0		0EC0 0060h	Section 9.5.273
00400064h	PCIE_CORE_RP_ADDR1		0EC0 0064h	Section 9.5.274
00400068h	PCIE_CORE_RP_DESC0		0EC0 0068h	Section 9.5.275
0040006Ch	PCIE_CORE_RP_DESC1		0EC0 006Ch	Section 9.5.276
00400074h	PCIE_CORE_RP_DESC3		0EC0 0074h	Section 9.5.277
00400078h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0078h	Section 9.5.278
0040007Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 007Ch	Section 9.5.279
00400080h	PCIE_CORE_RP_ADDR0		0EC0 0080h	Section 9.5.280
00400084h	PCIE_CORE_RP_ADDR1		0EC0 0084h	Section 9.5.281
00400088h	PCIE_CORE_RP_DESC0		0EC0 0088h	Section 9.5.282
0040008Ch	PCIE_CORE_RP_DESC1		0EC0 008Ch	Section 9.5.283
00400094h	PCIE_CORE_RP_DESC3		0EC0 0094h	Section 9.5.284
00400098h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0098h	Section 9.5.285
0040009Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 009Ch	Section 9.5.286
004000A0h	PCIE_CORE_RP_ADDR0		0EC0 00A0h	Section 9.5.287
004000A4h	PCIE_CORE_RP_ADDR1		0EC0 00A4h	Section 9.5.288
004000A8h	PCIE_CORE_RP_DESC0		0EC0 00A8h	Section 9.5.289
004000ACh	PCIE_CORE_RP_DESC1		0EC0 00ACh	Section 9.5.290
004000B4h	PCIE_CORE_RP_DESC3		0EC0 00B4h	Section 9.5.291
004000B8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 00B8h	Section 9.5.292
004000BCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 00BCh	Section 9.5.293
004000C0h	PCIE_CORE_RP_ADDR0		0EC0 00C0h	Section 9.5.294
004000C4h	PCIE_CORE_RP_ADDR1		0EC0 00C4h	Section 9.5.295
004000C8h	PCIE_CORE_RP_DESC0		0EC0 00C8h	Section 9.5.296
004000CCh	PCIE_CORE_RP_DESC1		0EC0 00CCh	Section 9.5.297

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004000D4h	PCIE_CORE_RP_DESC3		0EC0 00D4h	Section 9.5.298
004000D8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 00D8h	Section 9.5.299
004000DCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 00DCh	Section 9.5.300
004000E0h	PCIE_CORE_RP_ADDR0		0EC0 00E0h	Section 9.5.301
004000E4h	PCIE_CORE_RP_ADDR1		0EC0 00E4h	Section 9.5.302
004000E8h	PCIE_CORE_RP_DESC0		0EC0 00E8h	Section 9.5.303
004000ECh	PCIE_CORE_RP_DESC1		0EC0 00ECh	Section 9.5.304
004000F4h	PCIE_CORE_RP_DESC3		0EC0 00F4h	Section 9.5.305
004000F8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 00F8h	Section 9.5.306
004000FCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 00FCh	Section 9.5.307
00400100h	PCIE_CORE_RP_ADDR0		0EC0 0100h	Section 9.5.308
00400104h	PCIE_CORE_RP_ADDR1		0EC0 0104h	Section 9.5.309
00400108h	PCIE_CORE_RP_DESC0		0EC0 0108h	Section 9.5.310
0040010Ch	PCIE_CORE_RP_DESC1		0EC0 010Ch	Section 9.5.311
00400114h	PCIE_CORE_RP_DESC3		0EC0 0114h	Section 9.5.312
00400118h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0118h	Section 9.5.313
0040011Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 011Ch	Section 9.5.314
00400120h	PCIE_CORE_RP_ADDR0		0EC0 0120h	Section 9.5.315
00400124h	PCIE_CORE_RP_ADDR1		0EC0 0124h	Section 9.5.316
00400128h	PCIE_CORE_RP_DESC0		0EC0 0128h	Section 9.5.317
0040012Ch	PCIE_CORE_RP_DESC1		0EC0 012Ch	Section 9.5.318
00400134h	PCIE_CORE_RP_DESC3		0EC0 0134h	Section 9.5.319
00400138h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0138h	Section 9.5.320
0040013Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 013Ch	Section 9.5.321
00400140h	PCIE_CORE_RP_ADDR0		0EC0 0140h	Section 9.5.322

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400144h	PCIE_CORE_RP_ADDR1		0EC0 0144h	Section 9.5.323
00400148h	PCIE_CORE_RP_DESC0		0EC0 0148h	Section 9.5.324
0040014Ch	PCIE_CORE_RP_DESC1		0EC0 014Ch	Section 9.5.325
00400154h	PCIE_CORE_RP_DESC3		0EC0 0154h	Section 9.5.326
00400158h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0158h	Section 9.5.327
0040015Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 015Ch	Section 9.5.328
00400160h	PCIE_CORE_RP_ADDR0		0EC0 0160h	Section 9.5.329
00400164h	PCIE_CORE_RP_ADDR1		0EC0 0164h	Section 9.5.330
00400168h	PCIE_CORE_RP_DESC0		0EC0 0168h	Section 9.5.331
0040016Ch	PCIE_CORE_RP_DESC1		0EC0 016Ch	Section 9.5.332
00400174h	PCIE_CORE_RP_DESC3		0EC0 0174h	Section 9.5.333
00400178h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0178h	Section 9.5.334
0040017Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 017Ch	Section 9.5.335
00400180h	PCIE_CORE_RP_ADDR0		0EC0 0180h	Section 9.5.336
00400184h	PCIE_CORE_RP_ADDR1		0EC0 0184h	Section 9.5.337
00400188h	PCIE_CORE_RP_DESC0		0EC0 0188h	Section 9.5.338
0040018Ch	PCIE_CORE_RP_DESC1		0EC0 018Ch	Section 9.5.339
00400194h	PCIE_CORE_RP_DESC3		0EC0 0194h	Section 9.5.340
00400198h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0198h	Section 9.5.341
0040019Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 019Ch	Section 9.5.342
004001A0h	PCIE_CORE_RP_ADDR0		0EC0 01A0h	Section 9.5.343
004001A4h	PCIE_CORE_RP_ADDR1		0EC0 01A4h	Section 9.5.344
004001A8h	PCIE_CORE_RP_DESC0		0EC0 01A8h	Section 9.5.345
004001ACh	PCIE_CORE_RP_DESC1		0EC0 01ACh	Section 9.5.346
004001B4h	PCIE_CORE_RP_DESC3		0EC0 01B4h	Section 9.5.347

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004001B8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 01B8h	Section 9.5.348
004001BCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 01BCh	Section 9.5.349
004001C0h	PCIE_CORE_RP_ADDR0		0EC0 01C0h	Section 9.5.350
004001C4h	PCIE_CORE_RP_ADDR1		0EC0 01C4h	Section 9.5.351
004001C8h	PCIE_CORE_RP_DESC0		0EC0 01C8h	Section 9.5.352
004001CCh	PCIE_CORE_RP_DESC1		0EC0 01CCh	Section 9.5.353
004001D4h	PCIE_CORE_RP_DESC3		0EC0 01D4h	Section 9.5.354
004001D8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 01D8h	Section 9.5.355
004001DCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 01DCh	Section 9.5.356
004001E0h	PCIE_CORE_RP_ADDR0		0EC0 01E0h	Section 9.5.357
004001E4h	PCIE_CORE_RP_ADDR1		0EC0 01E4h	Section 9.5.358
004001E8h	PCIE_CORE_RP_DESC0		0EC0 01E8h	Section 9.5.359
004001ECh	PCIE_CORE_RP_DESC1		0EC0 01ECh	Section 9.5.360
004001F4h	PCIE_CORE_RP_DESC3		0EC0 01F4h	Section 9.5.361
004001F8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 01F8h	Section 9.5.362
004001FCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 01FCh	Section 9.5.363
00400200h	PCIE_CORE_RP_ADDR0		0EC0 0200h	Section 9.5.364
00400204h	PCIE_CORE_RP_ADDR1		0EC0 0204h	Section 9.5.365
00400208h	PCIE_CORE_RP_DESC0		0EC0 0208h	Section 9.5.366
0040020Ch	PCIE_CORE_RP_DESC1		0EC0 020Ch	Section 9.5.367
00400214h	PCIE_CORE_RP_DESC3		0EC0 0214h	Section 9.5.368
00400218h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0218h	Section 9.5.369
0040021Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 021Ch	Section 9.5.370
00400220h	PCIE_CORE_RP_ADDR0		0EC0 0220h	Section 9.5.371
00400224h	PCIE_CORE_RP_ADDR1		0EC0 0224h	Section 9.5.372

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400228h	PCIE_CORE_RP_DESC0		0EC0 0228h	Section 9.5.373
0040022Ch	PCIE_CORE_RP_DESC1		0EC0 022Ch	Section 9.5.374
00400234h	PCIE_CORE_RP_DESC3		0EC0 0234h	Section 9.5.375
00400238h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0238h	Section 9.5.376
0040023Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 023Ch	Section 9.5.377
00400240h	PCIE_CORE_RP_ADDR0		0EC0 0240h	Section 9.5.378
00400244h	PCIE_CORE_RP_ADDR1		0EC0 0244h	Section 9.5.379
00400248h	PCIE_CORE_RP_DESC0		0EC0 0248h	Section 9.5.380
0040024Ch	PCIE_CORE_RP_DESC1		0EC0 024Ch	Section 9.5.381
00400254h	PCIE_CORE_RP_DESC3		0EC0 0254h	Section 9.5.382
00400258h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0258h	Section 9.5.383
0040025Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 025Ch	Section 9.5.384
00400260h	PCIE_CORE_RP_ADDR0		0EC0 0260h	Section 9.5.385
00400264h	PCIE_CORE_RP_ADDR1		0EC0 0264h	Section 9.5.386
00400268h	PCIE_CORE_RP_DESC0		0EC0 0268h	Section 9.5.387
0040026Ch	PCIE_CORE_RP_DESC1		0EC0 026Ch	Section 9.5.388
00400274h	PCIE_CORE_RP_DESC3		0EC0 0274h	Section 9.5.389
00400278h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0278h	Section 9.5.390
0040027Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 027Ch	Section 9.5.391
00400280h	PCIE_CORE_RP_ADDR0		0EC0 0280h	Section 9.5.392
00400284h	PCIE_CORE_RP_ADDR1		0EC0 0284h	Section 9.5.393
00400288h	PCIE_CORE_RP_DESC0		0EC0 0288h	Section 9.5.394
0040028Ch	PCIE_CORE_RP_DESC1		0EC0 028Ch	Section 9.5.395
00400294h	PCIE_CORE_RP_DESC3		0EC0 0294h	Section 9.5.396
00400298h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0298h	Section 9.5.397

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
0040029Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 029Ch	Section 9.5.398
004002A0h	PCIE_CORE_RP_ADDR0		0EC0 02A0h	Section 9.5.399
004002A4h	PCIE_CORE_RP_ADDR1		0EC0 02A4h	Section 9.5.400
004002A8h	PCIE_CORE_RP_DESC0		0EC0 02A8h	Section 9.5.401
004002ACh	PCIE_CORE_RP_DESC1		0EC0 02ACh	Section 9.5.402
004002B4h	PCIE_CORE_RP_DESC3		0EC0 02B4h	Section 9.5.403
004002B8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 02B8h	Section 9.5.404
004002BCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 02BCh	Section 9.5.405
004002C0h	PCIE_CORE_RP_ADDR0		0EC0 02C0h	Section 9.5.406
004002C4h	PCIE_CORE_RP_ADDR1		0EC0 02C4h	Section 9.5.407
004002C8h	PCIE_CORE_RP_DESC0		0EC0 02C8h	Section 9.5.408
004002CCh	PCIE_CORE_RP_DESC1		0EC0 02CCh	Section 9.5.409
004002D4h	PCIE_CORE_RP_DESC3		0EC0 02D4h	Section 9.5.410
004002D8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 02D8h	Section 9.5.411
004002DCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 02DCh	Section 9.5.412
004002E0h	PCIE_CORE_RP_ADDR0		0EC0 02E0h	Section 9.5.413
004002E4h	PCIE_CORE_RP_ADDR1		0EC0 02E4h	Section 9.5.414
004002E8h	PCIE_CORE_RP_DESC0		0EC0 02E8h	Section 9.5.415
004002ECh	PCIE_CORE_RP_DESC1		0EC0 02ECh	Section 9.5.416
004002F4h	PCIE_CORE_RP_DESC3		0EC0 02F4h	Section 9.5.417
004002F8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 02F8h	Section 9.5.418
004002FCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 02FCh	Section 9.5.419
00400300h	PCIE_CORE_RP_ADDR0		0EC0 0300h	Section 9.5.420
00400304h	PCIE_CORE_RP_ADDR1		0EC0 0304h	Section 9.5.421
00400308h	PCIE_CORE_RP_DESC0		0EC0 0308h	Section 9.5.422

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
0040030Ch	PCIE_CORE_RP_DESC1		0EC0 030Ch	Section 9.5.423
00400314h	PCIE_CORE_RP_DESC3		0EC0 0314h	Section 9.5.424
00400318h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0318h	Section 9.5.425
0040031Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 031Ch	Section 9.5.426
00400320h	PCIE_CORE_RP_ADDR0		0EC0 0320h	Section 9.5.427
00400324h	PCIE_CORE_RP_ADDR1		0EC0 0324h	Section 9.5.428
00400328h	PCIE_CORE_RP_DESC0		0EC0 0328h	Section 9.5.429
0040032Ch	PCIE_CORE_RP_DESC1		0EC0 032Ch	Section 9.5.430
00400334h	PCIE_CORE_RP_DESC3		0EC0 0334h	Section 9.5.431
00400338h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0338h	Section 9.5.432
0040033Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 033Ch	Section 9.5.433
00400340h	PCIE_CORE_RP_ADDR0		0EC0 0340h	Section 9.5.434
00400344h	PCIE_CORE_RP_ADDR1		0EC0 0344h	Section 9.5.435
00400348h	PCIE_CORE_RP_DESC0		0EC0 0348h	Section 9.5.436
0040034Ch	PCIE_CORE_RP_DESC1		0EC0 034Ch	Section 9.5.437
00400354h	PCIE_CORE_RP_DESC3		0EC0 0354h	Section 9.5.438
00400358h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0358h	Section 9.5.439
0040035Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 035Ch	Section 9.5.440
00400360h	PCIE_CORE_RP_ADDR0		0EC0 0360h	Section 9.5.441
00400364h	PCIE_CORE_RP_ADDR1		0EC0 0364h	Section 9.5.442
00400368h	PCIE_CORE_RP_DESC0		0EC0 0368h	Section 9.5.443
0040036Ch	PCIE_CORE_RP_DESC1		0EC0 036Ch	Section 9.5.444
00400374h	PCIE_CORE_RP_DESC3		0EC0 0374h	Section 9.5.445
00400378h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0378h	Section 9.5.446
0040037Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 037Ch	Section 9.5.447

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400380h	PCIE_CORE_RP_ADDR0		0EC0 0380h	Section 9.5.448
00400384h	PCIE_CORE_RP_ADDR1		0EC0 0384h	Section 9.5.449
00400388h	PCIE_CORE_RP_DESC0		0EC0 0388h	Section 9.5.450
0040038Ch	PCIE_CORE_RP_DESC1		0EC0 038Ch	Section 9.5.451
00400394h	PCIE_CORE_RP_DESC3		0EC0 0394h	Section 9.5.452
00400398h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0398h	Section 9.5.453
0040039Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 039Ch	Section 9.5.454
004003A0h	PCIE_CORE_RP_ADDR0		0EC0 03A0h	Section 9.5.455
004003A4h	PCIE_CORE_RP_ADDR1		0EC0 03A4h	Section 9.5.456
004003A8h	PCIE_CORE_RP_DESC0		0EC0 03A8h	Section 9.5.457
004003ACh	PCIE_CORE_RP_DESC1		0EC0 03ACh	Section 9.5.458
004003B4h	PCIE_CORE_RP_DESC3		0EC0 03B4h	Section 9.5.459
004003B8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 03B8h	Section 9.5.460
004003BCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 03BCh	Section 9.5.461
004003C0h	PCIE_CORE_RP_ADDR0		0EC0 03C0h	Section 9.5.462
004003C4h	PCIE_CORE_RP_ADDR1		0EC0 03C4h	Section 9.5.463
004003C8h	PCIE_CORE_RP_DESC0		0EC0 03C8h	Section 9.5.464
004003CCh	PCIE_CORE_RP_DESC1		0EC0 03CCh	Section 9.5.465
004003D4h	PCIE_CORE_RP_DESC3		0EC0 03D4h	Section 9.5.466
004003D8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 03D8h	Section 9.5.467
004003DCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 03DCh	Section 9.5.468
004003E0h	PCIE_CORE_RP_ADDR0		0EC0 03E0h	Section 9.5.469
004003E4h	PCIE_CORE_RP_ADDR1		0EC0 03E4h	Section 9.5.470
004003E8h	PCIE_CORE_RP_DESC0		0EC0 03E8h	Section 9.5.471
004003ECh	PCIE_CORE_RP_DESC1		0EC0 03ECh	Section 9.5.472

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004003F4h	PCIE_CORE_RP_DESC3		0EC0 03F4h	Section 9.5.473
004003F8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 03F8h	Section 9.5.474
004003FCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 03FCh	Section 9.5.475
00400400h	PCIE_CORE_RP_ADDR0		0EC0 0400h	Section 9.5.476
00400404h	PCIE_CORE_RP_ADDR1		0EC0 0404h	Section 9.5.477
00400408h	PCIE_CORE_RP_DESC0		0EC0 0408h	Section 9.5.478
0040040Ch	PCIE_CORE_RP_DESC1		0EC0 040Ch	Section 9.5.479
00400414h	PCIE_CORE_RP_DESC3		0EC0 0414h	Section 9.5.480
00400418h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0418h	Section 9.5.481
0040041Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 041Ch	Section 9.5.482
00400420h	PCIE_CORE_RP_ADDR0		0EC0 0420h	Section 9.5.483
00400424h	PCIE_CORE_RP_ADDR1		0EC0 0424h	Section 9.5.484
00400428h	PCIE_CORE_RP_DESC0		0EC0 0428h	Section 9.5.485
0040042Ch	PCIE_CORE_RP_DESC1		0EC0 042Ch	Section 9.5.486
00400434h	PCIE_CORE_RP_DESC3		0EC0 0434h	Section 9.5.487
00400438h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0438h	Section 9.5.488
0040043Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 043Ch	Section 9.5.489
00400440h	PCIE_CORE_RP_ADDR0		0EC0 0440h	Section 9.5.490
00400444h	PCIE_CORE_RP_ADDR1		0EC0 0444h	Section 9.5.491
00400448h	PCIE_CORE_RP_DESC0		0EC0 0448h	Section 9.5.492
0040044Ch	PCIE_CORE_RP_DESC1		0EC0 044Ch	Section 9.5.493
00400454h	PCIE_CORE_RP_DESC3		0EC0 0454h	Section 9.5.494
00400458h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0458h	Section 9.5.495
0040045Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 045Ch	Section 9.5.496
00400460h	PCIE_CORE_RP_ADDR0		0EC0 0460h	Section 9.5.497

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400464h	PCIE_CORE_RP_ADDR1		0EC0 0464h	Section 9.5.498
00400468h	PCIE_CORE_RP_DESC0		0EC0 0468h	Section 9.5.499
0040046Ch	PCIE_CORE_RP_DESC1		0EC0 046Ch	Section 9.5.500
00400474h	PCIE_CORE_RP_DESC3		0EC0 0474h	Section 9.5.501
00400478h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0478h	Section 9.5.502
0040047Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 047Ch	Section 9.5.503
00400480h	PCIE_CORE_RP_ADDR0		0EC0 0480h	Section 9.5.504
00400484h	PCIE_CORE_RP_ADDR1		0EC0 0484h	Section 9.5.505
00400488h	PCIE_CORE_RP_DESC0		0EC0 0488h	Section 9.5.506
0040048Ch	PCIE_CORE_RP_DESC1		0EC0 048Ch	Section 9.5.507
00400494h	PCIE_CORE_RP_DESC3		0EC0 0494h	Section 9.5.508
00400498h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0498h	Section 9.5.509
0040049Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 049Ch	Section 9.5.510
004004A0h	PCIE_CORE_RP_ADDR0		0EC0 04A0h	Section 9.5.511
004004A4h	PCIE_CORE_RP_ADDR1		0EC0 04A4h	Section 9.5.512
004004A8h	PCIE_CORE_RP_DESC0		0EC0 04A8h	Section 9.5.513
004004ACh	PCIE_CORE_RP_DESC1		0EC0 04ACh	Section 9.5.514
004004B4h	PCIE_CORE_RP_DESC3		0EC0 04B4h	Section 9.5.515
004004B8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 04B8h	Section 9.5.516
004004BCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 04BCh	Section 9.5.517
004004C0h	PCIE_CORE_RP_ADDR0		0EC0 04C0h	Section 9.5.518
004004C4h	PCIE_CORE_RP_ADDR1		0EC0 04C4h	Section 9.5.519
004004C8h	PCIE_CORE_RP_DESC0		0EC0 04C8h	Section 9.5.520
004004CCh	PCIE_CORE_RP_DESC1		0EC0 04CCh	Section 9.5.521
004004D4h	PCIE_CORE_RP_DESC3		0EC0 04D4h	Section 9.5.522

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004004D8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 04D8h	Section 9.5.523
004004DCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 04DCh	Section 9.5.524
004004E0h	PCIE_CORE_RP_ADDR0		0EC0 04E0h	Section 9.5.525
004004E4h	PCIE_CORE_RP_ADDR1		0EC0 04E4h	Section 9.5.526
004004E8h	PCIE_CORE_RP_DESC0		0EC0 04E8h	Section 9.5.527
004004ECh	PCIE_CORE_RP_DESC1		0EC0 04ECh	Section 9.5.528
004004F4h	PCIE_CORE_RP_DESC3		0EC0 04F4h	Section 9.5.529
004004F8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 04F8h	Section 9.5.530
004004FCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 04FCh	Section 9.5.531
00400500h	PCIE_CORE_RP_ADDR0		0EC0 0500h	Section 9.5.532
00400504h	PCIE_CORE_RP_ADDR1		0EC0 0504h	Section 9.5.533
00400508h	PCIE_CORE_RP_DESC0		0EC0 0508h	Section 9.5.534
0040050Ch	PCIE_CORE_RP_DESC1		0EC0 050Ch	Section 9.5.535
00400514h	PCIE_CORE_RP_DESC3		0EC0 0514h	Section 9.5.536
00400518h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0518h	Section 9.5.537
0040051Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 051Ch	Section 9.5.538
00400520h	PCIE_CORE_RP_ADDR0		0EC0 0520h	Section 9.5.539
00400524h	PCIE_CORE_RP_ADDR1		0EC0 0524h	Section 9.5.540
00400528h	PCIE_CORE_RP_DESC0		0EC0 0528h	Section 9.5.541
0040052Ch	PCIE_CORE_RP_DESC1		0EC0 052Ch	Section 9.5.542
00400534h	PCIE_CORE_RP_DESC3		0EC0 0534h	Section 9.5.543
00400538h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0538h	Section 9.5.544
0040053Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 053Ch	Section 9.5.545
00400540h	PCIE_CORE_RP_ADDR0		0EC0 0540h	Section 9.5.546
00400544h	PCIE_CORE_RP_ADDR1		0EC0 0544h	Section 9.5.547

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400548h	PCIE_CORE_RP_DESC0		0EC0 0548h	Section 9.5.548
0040054Ch	PCIE_CORE_RP_DESC1		0EC0 054Ch	Section 9.5.549
00400554h	PCIE_CORE_RP_DESC3		0EC0 0554h	Section 9.5.550
00400558h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0558h	Section 9.5.551
0040055Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 055Ch	Section 9.5.552
00400560h	PCIE_CORE_RP_ADDR0		0EC0 0560h	Section 9.5.553
00400564h	PCIE_CORE_RP_ADDR1		0EC0 0564h	Section 9.5.554
00400568h	PCIE_CORE_RP_DESC0		0EC0 0568h	Section 9.5.555
0040056Ch	PCIE_CORE_RP_DESC1		0EC0 056Ch	Section 9.5.556
00400574h	PCIE_CORE_RP_DESC3		0EC0 0574h	Section 9.5.557
00400578h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0578h	Section 9.5.558
0040057Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 057Ch	Section 9.5.559
00400580h	PCIE_CORE_RP_ADDR0		0EC0 0580h	Section 9.5.560
00400584h	PCIE_CORE_RP_ADDR1		0EC0 0584h	Section 9.5.561
00400588h	PCIE_CORE_RP_DESC0		0EC0 0588h	Section 9.5.562
0040058Ch	PCIE_CORE_RP_DESC1		0EC0 058Ch	Section 9.5.563
00400594h	PCIE_CORE_RP_DESC3		0EC0 0594h	Section 9.5.564
00400598h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0598h	Section 9.5.565
0040059Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 059Ch	Section 9.5.566
004005A0h	PCIE_CORE_RP_ADDR0		0EC0 05A0h	Section 9.5.567
004005A4h	PCIE_CORE_RP_ADDR1		0EC0 05A4h	Section 9.5.568
004005A8h	PCIE_CORE_RP_DESC0		0EC0 05A8h	Section 9.5.569
004005ACh	PCIE_CORE_RP_DESC1		0EC0 05ACh	Section 9.5.570
004005B4h	PCIE_CORE_RP_DESC3		0EC0 05B4h	Section 9.5.571
004005B8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 05B8h	Section 9.5.572

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004005BCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 05BCh	Section 9.5.573
004005C0h	PCIE_CORE_RP_ADDR0		0EC0 05C0h	Section 9.5.574
004005C4h	PCIE_CORE_RP_ADDR1		0EC0 05C4h	Section 9.5.575
004005C8h	PCIE_CORE_RP_DESC0		0EC0 05C8h	Section 9.5.576
004005CCh	PCIE_CORE_RP_DESC1		0EC0 05CCh	Section 9.5.577
004005D4h	PCIE_CORE_RP_DESC3		0EC0 05D4h	Section 9.5.578
004005D8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 05D8h	Section 9.5.579
004005DCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 05DCh	Section 9.5.580
004005E0h	PCIE_CORE_RP_ADDR0		0EC0 05E0h	Section 9.5.581
004005E4h	PCIE_CORE_RP_ADDR1		0EC0 05E4h	Section 9.5.582
004005E8h	PCIE_CORE_RP_DESC0		0EC0 05E8h	Section 9.5.583
004005ECh	PCIE_CORE_RP_DESC1		0EC0 05ECh	Section 9.5.584
004005F4h	PCIE_CORE_RP_DESC3		0EC0 05F4h	Section 9.5.585
004005F8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 05F8h	Section 9.5.586
004005FCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 05FCh	Section 9.5.587
00400600h	PCIE_CORE_RP_ADDR0		0EC0 0600h	Section 9.5.588
00400604h	PCIE_CORE_RP_ADDR1		0EC0 0604h	Section 9.5.589
00400608h	PCIE_CORE_RP_DESC0		0EC0 0608h	Section 9.5.590
0040060Ch	PCIE_CORE_RP_DESC1		0EC0 060Ch	Section 9.5.591
00400614h	PCIE_CORE_RP_DESC3		0EC0 0614h	Section 9.5.592
00400618h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0618h	Section 9.5.593
0040061Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 061Ch	Section 9.5.594
00400620h	PCIE_CORE_RP_ADDR0		0EC0 0620h	Section 9.5.595
00400624h	PCIE_CORE_RP_ADDR1		0EC0 0624h	Section 9.5.596
00400628h	PCIE_CORE_RP_DESC0		0EC0 0628h	Section 9.5.597

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
0040062Ch	PCIE_CORE_RP_DESC1		0EC0 062Ch	Section 9.5.598
00400634h	PCIE_CORE_RP_DESC3		0EC0 0634h	Section 9.5.599
00400638h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0638h	Section 9.5.600
0040063Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 063Ch	Section 9.5.601
00400640h	PCIE_CORE_RP_ADDR0		0EC0 0640h	Section 9.5.602
00400644h	PCIE_CORE_RP_ADDR1		0EC0 0644h	Section 9.5.603
00400648h	PCIE_CORE_RP_DESC0		0EC0 0648h	Section 9.5.604
0040064Ch	PCIE_CORE_RP_DESC1		0EC0 064Ch	Section 9.5.605
00400654h	PCIE_CORE_RP_DESC3		0EC0 0654h	Section 9.5.606
00400658h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0658h	Section 9.5.607
0040065Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 065Ch	Section 9.5.608
00400660h	PCIE_CORE_RP_ADDR0		0EC0 0660h	Section 9.5.609
00400664h	PCIE_CORE_RP_ADDR1		0EC0 0664h	Section 9.5.610
00400668h	PCIE_CORE_RP_DESC0		0EC0 0668h	Section 9.5.611
0040066Ch	PCIE_CORE_RP_DESC1		0EC0 066Ch	Section 9.5.612
00400674h	PCIE_CORE_RP_DESC3		0EC0 0674h	Section 9.5.613
00400678h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0678h	Section 9.5.614
0040067Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 067Ch	Section 9.5.615
00400680h	PCIE_CORE_RP_ADDR0		0EC0 0680h	Section 9.5.616
00400684h	PCIE_CORE_RP_ADDR1		0EC0 0684h	Section 9.5.617
00400688h	PCIE_CORE_RP_DESC0		0EC0 0688h	Section 9.5.618
0040068Ch	PCIE_CORE_RP_DESC1		0EC0 068Ch	Section 9.5.619
00400694h	PCIE_CORE_RP_DESC3		0EC0 0694h	Section 9.5.620
00400698h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0698h	Section 9.5.621
0040069Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 069Ch	Section 9.5.622

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004006A0h	PCIE_CORE_RP_ADDR0		0EC0 06A0h	Section 9.5.623
004006A4h	PCIE_CORE_RP_ADDR1		0EC0 06A4h	Section 9.5.624
004006A8h	PCIE_CORE_RP_DESC0		0EC0 06A8h	Section 9.5.625
004006ACh	PCIE_CORE_RP_DESC1		0EC0 06ACh	Section 9.5.626
004006B4h	PCIE_CORE_RP_DESC3		0EC0 06B4h	Section 9.5.627
004006B8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 06B8h	Section 9.5.628
004006BCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 06BCh	Section 9.5.629
004006C0h	PCIE_CORE_RP_ADDR0		0EC0 06C0h	Section 9.5.630
004006C4h	PCIE_CORE_RP_ADDR1		0EC0 06C4h	Section 9.5.631
004006C8h	PCIE_CORE_RP_DESC0		0EC0 06C8h	Section 9.5.632
004006CCh	PCIE_CORE_RP_DESC1		0EC0 06CCh	Section 9.5.633
004006D4h	PCIE_CORE_RP_DESC3		0EC0 06D4h	Section 9.5.634
004006D8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 06D8h	Section 9.5.635
004006DCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 06DCh	Section 9.5.636
004006E0h	PCIE_CORE_RP_ADDR0		0EC0 06E0h	Section 9.5.637
004006E4h	PCIE_CORE_RP_ADDR1		0EC0 06E4h	Section 9.5.638
004006E8h	PCIE_CORE_RP_DESC0		0EC0 06E8h	Section 9.5.639
004006ECh	PCIE_CORE_RP_DESC1		0EC0 06ECh	Section 9.5.640
004006F4h	PCIE_CORE_RP_DESC3		0EC0 06F4h	Section 9.5.641
004006F8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 06F8h	Section 9.5.642
004006FCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 06FCh	Section 9.5.643
00400700h	PCIE_CORE_RP_ADDR0		0EC0 0700h	Section 9.5.644
00400704h	PCIE_CORE_RP_ADDR1		0EC0 0704h	Section 9.5.645
00400708h	PCIE_CORE_RP_DESC0		0EC0 0708h	Section 9.5.646
0040070Ch	PCIE_CORE_RP_DESC1		0EC0 070Ch	Section 9.5.647

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400714h	PCIE_CORE_RP_DESC3		0EC0 0714h	Section 9.5.648
00400718h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0718h	Section 9.5.649
0040071Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 071Ch	Section 9.5.650
00400720h	PCIE_CORE_RP_ADDR0		0EC0 0720h	Section 9.5.651
00400724h	PCIE_CORE_RP_ADDR1		0EC0 0724h	Section 9.5.652
00400728h	PCIE_CORE_RP_DESC0		0EC0 0728h	Section 9.5.653
0040072Ch	PCIE_CORE_RP_DESC1		0EC0 072Ch	Section 9.5.654
00400734h	PCIE_CORE_RP_DESC3		0EC0 0734h	Section 9.5.655
00400738h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0738h	Section 9.5.656
0040073Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 073Ch	Section 9.5.657
00400740h	PCIE_CORE_RP_ADDR0		0EC0 0740h	Section 9.5.658
00400744h	PCIE_CORE_RP_ADDR1		0EC0 0744h	Section 9.5.659
00400748h	PCIE_CORE_RP_DESC0		0EC0 0748h	Section 9.5.660
0040074Ch	PCIE_CORE_RP_DESC1		0EC0 074Ch	Section 9.5.661
00400754h	PCIE_CORE_RP_DESC3		0EC0 0754h	Section 9.5.662
00400758h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0758h	Section 9.5.663
0040075Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 075Ch	Section 9.5.664
00400760h	PCIE_CORE_RP_ADDR0		0EC0 0760h	Section 9.5.665
00400764h	PCIE_CORE_RP_ADDR1		0EC0 0764h	Section 9.5.666
00400768h	PCIE_CORE_RP_DESC0		0EC0 0768h	Section 9.5.667
0040076Ch	PCIE_CORE_RP_DESC1		0EC0 076Ch	Section 9.5.668
00400774h	PCIE_CORE_RP_DESC3		0EC0 0774h	Section 9.5.669
00400778h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0778h	Section 9.5.670
0040077Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 077Ch	Section 9.5.671
00400780h	PCIE_CORE_RP_ADDR0		0EC0 0780h	Section 9.5.672

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400784h	PCIE_CORE_RP_ADDR1		0EC0 0784h	Section 9.5.673
00400788h	PCIE_CORE_RP_DESC0		0EC0 0788h	Section 9.5.674
0040078Ch	PCIE_CORE_RP_DESC1		0EC0 078Ch	Section 9.5.675
00400794h	PCIE_CORE_RP_DESC3		0EC0 0794h	Section 9.5.676
00400798h	PCIE_CORE_RP_AXI_ADDR0		0EC0 0798h	Section 9.5.677
0040079Ch	PCIE_CORE_RP_AXI_ADDR1		0EC0 079Ch	Section 9.5.678
004007A0h	PCIE_CORE_RP_ADDR0		0EC0 07A0h	Section 9.5.679
004007A4h	PCIE_CORE_RP_ADDR1		0EC0 07A4h	Section 9.5.680
004007A8h	PCIE_CORE_RP_DESC0		0EC0 07A8h	Section 9.5.681
004007ACh	PCIE_CORE_RP_DESC1		0EC0 07ACh	Section 9.5.682
004007B4h	PCIE_CORE_RP_DESC3		0EC0 07B4h	Section 9.5.683
004007B8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 07B8h	Section 9.5.684
004007BCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 07BCh	Section 9.5.685
004007C0h	PCIE_CORE_RP_ADDR0		0EC0 07C0h	Section 9.5.686
004007C4h	PCIE_CORE_RP_ADDR1		0EC0 07C4h	Section 9.5.687
004007C8h	PCIE_CORE_RP_DESC0		0EC0 07C8h	Section 9.5.688
004007CCh	PCIE_CORE_RP_DESC1		0EC0 07CCh	Section 9.5.689
004007D4h	PCIE_CORE_RP_DESC3		0EC0 07D4h	Section 9.5.690
004007D8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 07D8h	Section 9.5.691
004007DCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 07DCh	Section 9.5.692
004007E0h	PCIE_CORE_RP_ADDR0		0EC0 07E0h	Section 9.5.693
004007E4h	PCIE_CORE_RP_ADDR1		0EC0 07E4h	Section 9.5.694
004007E8h	PCIE_CORE_RP_DESC0		0EC0 07E8h	Section 9.5.695
004007ECh	PCIE_CORE_RP_DESC1		0EC0 07ECh	Section 9.5.696
004007F4h	PCIE_CORE_RP_DESC3		0EC0 07F4h	Section 9.5.697

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004007F8h	PCIE_CORE_RP_AXI_ADDR0		0EC0 07F8h	Section 9.5.698
004007FCh	PCIE_CORE_RP_AXI_ADDR1		0EC0 07FCh	Section 9.5.699
00400800h	PCIE_CORE_RP_ADDR0		0EC0 0800h	Section 9.5.700
00400804h	PCIE_CORE_RP_ADDR1		0EC0 0804h	Section 9.5.701
00400808h	PCIE_CORE_RP_ADDR0		0EC0 0808h	Section 9.5.702
0040080Ch	PCIE_CORE_RP_ADDR1		0EC0 080Ch	Section 9.5.703
00400810h	PCIE_CORE_RP_ADDR0		0EC0 0810h	Section 9.5.704
00400814h	PCIE_CORE_RP_ADDR1		0EC0 0814h	Section 9.5.705
00400820h	PCIE_CORE_RP_C0		0EC0 0820h	Section 9.5.706
00400824h	PCIE_CORE_RP_L0		0EC0 0824h	Section 9.5.707
00400840h	PCIE_CORE_RP_ADDR0		0EC0 0840h	Section 9.5.708
00400844h	PCIE_CORE_RP_ADDR1		0EC0 0844h	Section 9.5.709
00400848h	PCIE_CORE_RP_ADDR0		0EC0 0848h	Section 9.5.710
0040084Ch	PCIE_CORE_RP_ADDR1		0EC0 084Ch	Section 9.5.711
00400850h	PCIE_CORE_RP_ADDR0		0EC0 0850h	Section 9.5.712
00400854h	PCIE_CORE_RP_ADDR1		0EC0 0854h	Section 9.5.713
00400858h	PCIE_CORE_RP_ADDR0		0EC0 0858h	Section 9.5.714
0040085Ch	PCIE_CORE_RP_ADDR1		0EC0 085Ch	Section 9.5.715
00400860h	PCIE_CORE_RP_ADDR0		0EC0 0860h	Section 9.5.716
00400864h	PCIE_CORE_RP_ADDR1		0EC0 0864h	Section 9.5.717
00400868h	PCIE_CORE_RP_ADDR0		0EC0 0868h	Section 9.5.718
0040086Ch	PCIE_CORE_RP_ADDR1		0EC0 086Ch	Section 9.5.719
00400870h	PCIE_CORE_RP_ADDR0		0EC0 0870h	Section 9.5.720
00400874h	PCIE_CORE_RP_ADDR1		0EC0 0874h	Section 9.5.721
00400878h	PCIE_CORE_RP_ADDR0		0EC0 0878h	Section 9.5.722

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
0040087Ch	PCIE_CORE_RP_ADDR1		0EC0 087Ch	Section 9.5.723
00400880h	PCIE_CORE_RP_ADDR0		0EC0 0880h	Section 9.5.724
00400884h	PCIE_CORE_RP_ADDR1		0EC0 0884h	Section 9.5.725
00400888h	PCIE_CORE_RP_ADDR0		0EC0 0888h	Section 9.5.726
0040088Ch	PCIE_CORE_RP_ADDR1		0EC0 088Ch	Section 9.5.727
00400890h	PCIE_CORE_RP_ADDR0		0EC0 0890h	Section 9.5.728
00400894h	PCIE_CORE_RP_ADDR1		0EC0 0894h	Section 9.5.729
00400898h	PCIE_CORE_RP_ADDR0		0EC0 0898h	Section 9.5.730
0040089Ch	PCIE_CORE_RP_ADDR1		0EC0 089Ch	Section 9.5.731
004008A0h	PCIE_CORE_RP_ADDR0		0EC0 08A0h	Section 9.5.732
004008A4h	PCIE_CORE_RP_ADDR1		0EC0 08A4h	Section 9.5.733
004008A8h	PCIE_CORE_RP_ADDR0		0EC0 08A8h	Section 9.5.734
004008ACh	PCIE_CORE_RP_ADDR1		0EC0 08ACh	Section 9.5.735
004008B0h	PCIE_CORE_RP_ADDR0		0EC0 08B0h	Section 9.5.736
004008B4h	PCIE_CORE_RP_ADDR1		0EC0 08B4h	Section 9.5.737
004008B8h	PCIE_CORE_RP_ADDR0		0EC0 08B8h	Section 9.5.738
004008BCh	PCIE_CORE_RP_ADDR1		0EC0 08BCh	Section 9.5.739
004008C0h	PCIE_CORE_RP_ADDR0		0EC0 08C0h	Section 9.5.740
004008C4h	PCIE_CORE_RP_ADDR1		0EC0 08C4h	Section 9.5.741
004008C8h	PCIE_CORE_RP_ADDR0		0EC0 08C8h	Section 9.5.742
004008CCh	PCIE_CORE_RP_ADDR1		0EC0 08CCh	Section 9.5.743
004008D0h	PCIE_CORE_RP_ADDR0		0EC0 08D0h	Section 9.5.744
004008D4h	PCIE_CORE_RP_ADDR1		0EC0 08D4h	Section 9.5.745
004008D8h	PCIE_CORE_RP_ADDR0		0EC0 08D8h	Section 9.5.746
004008DCh	PCIE_CORE_RP_ADDR1		0EC0 08DCh	Section 9.5.747

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004008E0h	PCIE_CORE_RP_ADDR0		0EC0 08E0h	Section 9.5.748
004008E4h	PCIE_CORE_RP_ADDR1		0EC0 08E4h	Section 9.5.749
004008E8h	PCIE_CORE_RP_ADDR0		0EC0 08E8h	Section 9.5.750
004008ECh	PCIE_CORE_RP_ADDR1		0EC0 08ECh	Section 9.5.751
004008F0h	PCIE_CORE_RP_ADDR0		0EC0 08F0h	Section 9.5.752
004008F4h	PCIE_CORE_RP_ADDR1		0EC0 08F4h	Section 9.5.753
004008F8h	PCIE_CORE_RP_ADDR0		0EC0 08F8h	Section 9.5.754
004008FCh	PCIE_CORE_RP_ADDR1		0EC0 08FCh	Section 9.5.755
00400900h	PCIE_CORE_RP_ADDR0		0EC0 0900h	Section 9.5.756
00400904h	PCIE_CORE_RP_ADDR1		0EC0 0904h	Section 9.5.757
00400908h	PCIE_CORE_RP_ADDR0		0EC0 0908h	Section 9.5.758
0040090Ch	PCIE_CORE_RP_ADDR1		0EC0 090Ch	Section 9.5.759
00400910h	PCIE_CORE_RP_ADDR0		0EC0 0910h	Section 9.5.760
00400914h	PCIE_CORE_RP_ADDR1		0EC0 0914h	Section 9.5.761
00400918h	PCIE_CORE_RP_ADDR0		0EC0 0918h	Section 9.5.762
0040091Ch	PCIE_CORE_RP_ADDR1		0EC0 091Ch	Section 9.5.763
00400920h	PCIE_CORE_RP_ADDR0		0EC0 0920h	Section 9.5.764
00400924h	PCIE_CORE_RP_ADDR1		0EC0 0924h	Section 9.5.765
00400928h	PCIE_CORE_RP_ADDR0		0EC0 0928h	Section 9.5.766
0040092Ch	PCIE_CORE_RP_ADDR1		0EC0 092Ch	Section 9.5.767
00400930h	PCIE_CORE_RP_ADDR0		0EC0 0930h	Section 9.5.768
00400934h	PCIE_CORE_RP_ADDR1		0EC0 0934h	Section 9.5.769
00400938h	PCIE_CORE_RP_ADDR0		0EC0 0938h	Section 9.5.770
0040093Ch	PCIE_CORE_RP_ADDR1		0EC0 093Ch	Section 9.5.771
00400940h	PCIE_CORE_RP_ADDR0		0EC0 0940h	Section 9.5.772

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400944h	PCIE_CORE_RP_ADDR1		0EC0 0944h	Section 9.5.773
00400948h	PCIE_CORE_RP_ADDR0		0EC0 0948h	Section 9.5.774
0040094Ch	PCIE_CORE_RP_ADDR1		0EC0 094Ch	Section 9.5.775
00400950h	PCIE_CORE_RP_ADDR0		0EC0 0950h	Section 9.5.776
00400954h	PCIE_CORE_RP_ADDR1		0EC0 0954h	Section 9.5.777
00400958h	PCIE_CORE_RP_ADDR0		0EC0 0958h	Section 9.5.778
0040095Ch	PCIE_CORE_RP_ADDR1		0EC0 095Ch	Section 9.5.779
00400960h	PCIE_CORE_RP_ADDR0		0EC0 0960h	Section 9.5.780
00400964h	PCIE_CORE_RP_ADDR1		0EC0 0964h	Section 9.5.781
00400968h	PCIE_CORE_RP_ADDR0		0EC0 0968h	Section 9.5.782
0040096Ch	PCIE_CORE_RP_ADDR1		0EC0 096Ch	Section 9.5.783
00400970h	PCIE_CORE_RP_ADDR0		0EC0 0970h	Section 9.5.784
00400974h	PCIE_CORE_RP_ADDR1		0EC0 0974h	Section 9.5.785
00400978h	PCIE_CORE_RP_ADDR0		0EC0 0978h	Section 9.5.786
0040097Ch	PCIE_CORE_RP_ADDR1		0EC0 097Ch	Section 9.5.787
00400980h	PCIE_CORE_RP_ADDR0		0EC0 0980h	Section 9.5.788
00400984h	PCIE_CORE_RP_ADDR1		0EC0 0984h	Section 9.5.789
00400988h	PCIE_CORE_RP_ADDR0		0EC0 0988h	Section 9.5.790
0040098Ch	PCIE_CORE_RP_ADDR1		0EC0 098Ch	Section 9.5.791
00400990h	PCIE_CORE_RP_ADDR0		0EC0 0990h	Section 9.5.792
00400994h	PCIE_CORE_RP_ADDR1		0EC0 0994h	Section 9.5.793
00400998h	PCIE_CORE_RP_ADDR0		0EC0 0998h	Section 9.5.794
0040099Ch	PCIE_CORE_RP_ADDR1		0EC0 099Ch	Section 9.5.795
004009A0h	PCIE_CORE_RP_ADDR0		0EC0 09A0h	Section 9.5.796
004009A4h	PCIE_CORE_RP_ADDR1		0EC0 09A4h	Section 9.5.797

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
004009A8h	PCIE_CORE_RP_ADDR0		0EC0 09A8h	Section 9.5.798
004009ACh	PCIE_CORE_RP_ADDR1		0EC0 09ACh	Section 9.5.799
004009B0h	PCIE_CORE_RP_ADDR0		0EC0 09B0h	Section 9.5.800
004009B4h	PCIE_CORE_RP_ADDR1		0EC0 09B4h	Section 9.5.801
004009B8h	PCIE_CORE_RP_ADDR0		0EC0 09B8h	Section 9.5.802
004009BCh	PCIE_CORE_RP_ADDR1		0EC0 09BCh	Section 9.5.803
004009C0h	PCIE_CORE_RP_ADDR0		0EC0 09C0h	Section 9.5.804
004009C4h	PCIE_CORE_RP_ADDR1		0EC0 09C4h	Section 9.5.805
004009C8h	PCIE_CORE_RP_ADDR0		0EC0 09C8h	Section 9.5.806
004009CCh	PCIE_CORE_RP_ADDR1		0EC0 09CCh	Section 9.5.807
004009D0h	PCIE_CORE_RP_ADDR0		0EC0 09D0h	Section 9.5.808
004009D4h	PCIE_CORE_RP_ADDR1		0EC0 09D4h	Section 9.5.809
004009D8h	PCIE_CORE_RP_ADDR0		0EC0 09D8h	Section 9.5.810
004009DCh	PCIE_CORE_RP_ADDR1		0EC0 09DCh	Section 9.5.811
004009E0h	PCIE_CORE_RP_ADDR0		0EC0 09E0h	Section 9.5.812
004009E4h	PCIE_CORE_RP_ADDR1		0EC0 09E4h	Section 9.5.813
004009E8h	PCIE_CORE_RP_ADDR0		0EC0 09E8h	Section 9.5.814
004009ECh	PCIE_CORE_RP_ADDR1		0EC0 09ECh	Section 9.5.815
004009F0h	PCIE_CORE_RP_ADDR0		0EC0 09F0h	Section 9.5.816
004009F4h	PCIE_CORE_RP_ADDR1		0EC0 09F4h	Section 9.5.817
004009F8h	PCIE_CORE_RP_ADDR0		0EC0 09F8h	Section 9.5.818
004009FCh	PCIE_CORE_RP_ADDR1		0EC0 09FCh	Section 9.5.819
00400A00h	PCIE_CORE_RP_ADDR0		0EC0 0A00h	Section 9.5.820
00400A04h	PCIE_CORE_RP_ADDR1		0EC0 0A04h	Section 9.5.821
00400A08h	PCIE_CORE_RP_ADDR0		0EC0 0A08h	Section 9.5.822

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400A0Ch	PCIE_CORE_RP_ADDR1		0EC0 0A0Ch	Section 9.5.823
00400A10h	PCIE_CORE_RP_ADDR0		0EC0 0A10h	Section 9.5.824
00400A14h	PCIE_CORE_RP_ADDR1		0EC0 0A14h	Section 9.5.825
00400A18h	PCIE_CORE_RP_ADDR0		0EC0 0A18h	Section 9.5.826
00400A1Ch	PCIE_CORE_RP_ADDR1		0EC0 0A1Ch	Section 9.5.827
00400A20h	PCIE_CORE_RP_ADDR0		0EC0 0A20h	Section 9.5.828
00400A24h	PCIE_CORE_RP_ADDR1		0EC0 0A24h	Section 9.5.829
00400A28h	PCIE_CORE_RP_ADDR0		0EC0 0A28h	Section 9.5.830
00400A2Ch	PCIE_CORE_RP_ADDR1		0EC0 0A2Ch	Section 9.5.831
00400A30h	PCIE_CORE_RP_ADDR0		0EC0 0A30h	Section 9.5.832
00400A34h	PCIE_CORE_RP_ADDR1		0EC0 0A34h	Section 9.5.833
00400A38h	PCIE_CORE_RP_ADDR0		0EC0 0A38h	Section 9.5.834
00400A3Ch	PCIE_CORE_RP_ADDR1		0EC0 0A3Ch	Section 9.5.835
00400A40h	PCIE_CORE_RP_ADDR0		0EC0 0A40h	Section 9.5.836
00400A44h	PCIE_CORE_RP_ADDR1		0EC0 0A44h	Section 9.5.837
00400A48h	PCIE_CORE_RP_ADDR0		0EC0 0A48h	Section 9.5.838
00400A4Ch	PCIE_CORE_RP_ADDR1		0EC0 0A4Ch	Section 9.5.839
00400A50h	PCIE_CORE_RP_ADDR0		0EC0 0A50h	Section 9.5.840
00400A54h	PCIE_CORE_RP_ADDR1		0EC0 0A54h	Section 9.5.841
00400A58h	PCIE_CORE_RP_ADDR0		0EC0 0A58h	Section 9.5.842
00400A5Ch	PCIE_CORE_RP_ADDR1		0EC0 0A5Ch	Section 9.5.843
00400A60h	PCIE_CORE_RP_ADDR0		0EC0 0A60h	Section 9.5.844
00400A64h	PCIE_CORE_RP_ADDR1		0EC0 0A64h	Section 9.5.845
00400A68h	PCIE_CORE_RP_ADDR0		0EC0 0A68h	Section 9.5.846
00400A6Ch	PCIE_CORE_RP_ADDR1		0EC0 0A6Ch	Section 9.5.847

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400A70h	PCIE_CORE_RP_ADDR0		0EC0 0A70h	Section 9.5.848
00400A74h	PCIE_CORE_RP_ADDR1		0EC0 0A74h	Section 9.5.849
00400A78h	PCIE_CORE_RP_ADDR0		0EC0 0A78h	Section 9.5.850
00400A7Ch	PCIE_CORE_RP_ADDR1		0EC0 0A7Ch	Section 9.5.851
00400A80h	PCIE_CORE_RP_ADDR0		0EC0 0A80h	Section 9.5.852
00400A84h	PCIE_CORE_RP_ADDR1		0EC0 0A84h	Section 9.5.853
00400A88h	PCIE_CORE_RP_ADDR0		0EC0 0A88h	Section 9.5.854
00400A8Ch	PCIE_CORE_RP_ADDR1		0EC0 0A8Ch	Section 9.5.855
00400A90h	PCIE_CORE_RP_ADDR0		0EC0 0A90h	Section 9.5.856
00400A94h	PCIE_CORE_RP_ADDR1		0EC0 0A94h	Section 9.5.857
00400A98h	PCIE_CORE_RP_ADDR0		0EC0 0A98h	Section 9.5.858
00400A9Ch	PCIE_CORE_RP_ADDR1		0EC0 0A9Ch	Section 9.5.859
00400AA0h	PCIE_CORE_RP_ADDR0		0EC0 0AA0h	Section 9.5.860
00400AA4h	PCIE_CORE_RP_ADDR1		0EC0 0AA4h	Section 9.5.861
00400AA8h	PCIE_CORE_RP_ADDR0		0EC0 0AA8h	Section 9.5.862
00400AACh	PCIE_CORE_RP_ADDR1		0EC0 0AACh	Section 9.5.863
00400AB0h	PCIE_CORE_RP_ADDR0		0EC0 0AB0h	Section 9.5.864
00400AB4h	PCIE_CORE_RP_ADDR1		0EC0 0AB4h	Section 9.5.865
00400AB8h	PCIE_CORE_RP_ADDR0		0EC0 0AB8h	Section 9.5.866
00400ABCh	PCIE_CORE_RP_ADDR1		0EC0 0ABCh	Section 9.5.867
00400AC0h	PCIE_CORE_RP_ADDR0		0EC0 0AC0h	Section 9.5.868
00400AC4h	PCIE_CORE_RP_ADDR1		0EC0 0AC4h	Section 9.5.869
00400AC8h	PCIE_CORE_RP_ADDR0		0EC0 0AC8h	Section 9.5.870
00400ACC h	PCIE_CORE_RP_ADDR1		0EC0 0ACCh	Section 9.5.871
00400AD0h	PCIE_CORE_RP_ADDR0		0EC0 0AD0h	Section 9.5.872

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400AD4h	PCIE_CORE_RP_ADDR1		0EC0 0AD4h	Section 9.5.873
00400AD8h	PCIE_CORE_RP_ADDR0		0EC0 0AD8h	Section 9.5.874
00400ADC h	PCIE_CORE_RP_ADDR1		0EC0 0ADCh	Section 9.5.875
00400AE0h	PCIE_CORE_RP_ADDR0		0EC0 0AE0h	Section 9.5.876
00400AE4h	PCIE_CORE_RP_ADDR1		0EC0 0AE4h	Section 9.5.877
00400AE8h	PCIE_CORE_RP_ADDR0		0EC0 0AE8h	Section 9.5.878
00400AECh	PCIE_CORE_RP_ADDR1		0EC0 0AECh	Section 9.5.879
00400AF0h	PCIE_CORE_RP_ADDR0		0EC0 0AF0h	Section 9.5.880
00400AF4h	PCIE_CORE_RP_ADDR1		0EC0 0AF4h	Section 9.5.881
00400AF8h	PCIE_CORE_RP_ADDR0		0EC0 0AF8h	Section 9.5.882
00400AFCh	PCIE_CORE_RP_ADDR1		0EC0 0AFCh	Section 9.5.883
00400B00h	PCIE_CORE_RP_ADDR0		0EC0 0B00h	Section 9.5.884
00400B04h	PCIE_CORE_RP_ADDR1		0EC0 0B04h	Section 9.5.885
00400B08h	PCIE_CORE_RP_ADDR0		0EC0 0B08h	Section 9.5.886
00400B0Ch	PCIE_CORE_RP_ADDR1		0EC0 0B0Ch	Section 9.5.887
00400B10h	PCIE_CORE_RP_ADDR0		0EC0 0B10h	Section 9.5.888
00400B14h	PCIE_CORE_RP_ADDR1		0EC0 0B14h	Section 9.5.889
00400B18h	PCIE_CORE_RP_ADDR0		0EC0 0B18h	Section 9.5.890
00400B1Ch	PCIE_CORE_RP_ADDR1		0EC0 0B1Ch	Section 9.5.891
00400B20h	PCIE_CORE_RP_ADDR0		0EC0 0B20h	Section 9.5.892
00400B24h	PCIE_CORE_RP_ADDR1		0EC0 0B24h	Section 9.5.893
00400B28h	PCIE_CORE_RP_ADDR0		0EC0 0B28h	Section 9.5.894
00400B2Ch	PCIE_CORE_RP_ADDR1		0EC0 0B2Ch	Section 9.5.895
00400B30h	PCIE_CORE_RP_ADDR0		0EC0 0B30h	Section 9.5.896
00400B34h	PCIE_CORE_RP_ADDR1		0EC0 0B34h	Section 9.5.897

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400B38h	PCIE_CORE_RP_ADDR0		0EC0 0B38h	Section 9.5.898
00400B3Ch	PCIE_CORE_RP_ADDR1		0EC0 0B3Ch	Section 9.5.899
00400B40h	PCIE_CORE_RP_ADDR0		0EC0 0B40h	Section 9.5.900
00400B44h	PCIE_CORE_RP_ADDR1		0EC0 0B44h	Section 9.5.901
00400B48h	PCIE_CORE_RP_ADDR0		0EC0 0B48h	Section 9.5.902
00400B4Ch	PCIE_CORE_RP_ADDR1		0EC0 0B4Ch	Section 9.5.903
00400B50h	PCIE_CORE_RP_ADDR0		0EC0 0B50h	Section 9.5.904
00400B54h	PCIE_CORE_RP_ADDR1		0EC0 0B54h	Section 9.5.905
00400B58h	PCIE_CORE_RP_ADDR0		0EC0 0B58h	Section 9.5.906
00400B5Ch	PCIE_CORE_RP_ADDR1		0EC0 0B5Ch	Section 9.5.907
00400B60h	PCIE_CORE_RP_ADDR0		0EC0 0B60h	Section 9.5.908
00400B64h	PCIE_CORE_RP_ADDR1		0EC0 0B64h	Section 9.5.909
00400B68h	PCIE_CORE_RP_ADDR0		0EC0 0B68h	Section 9.5.910
00400B6Ch	PCIE_CORE_RP_ADDR1		0EC0 0B6Ch	Section 9.5.911
00400B70h	PCIE_CORE_RP_ADDR0		0EC0 0B70h	Section 9.5.912
00400B74h	PCIE_CORE_RP_ADDR1		0EC0 0B74h	Section 9.5.913
00400B78h	PCIE_CORE_RP_ADDR0		0EC0 0B78h	Section 9.5.914
00400B7Ch	PCIE_CORE_RP_ADDR1		0EC0 0B7Ch	Section 9.5.915
00400B80h	PCIE_CORE_RP_ADDR0		0EC0 0B80h	Section 9.5.916
00400B84h	PCIE_CORE_RP_ADDR1		0EC0 0B84h	Section 9.5.917
00400B88h	PCIE_CORE_RP_ADDR0		0EC0 0B88h	Section 9.5.918
00400B8Ch	PCIE_CORE_RP_ADDR1		0EC0 0B8Ch	Section 9.5.919
00400B90h	PCIE_CORE_RP_ADDR0		0EC0 0B90h	Section 9.5.920
00400B94h	PCIE_CORE_RP_ADDR1		0EC0 0B94h	Section 9.5.921
00400B98h	PCIE_CORE_RP_ADDR0		0EC0 0B98h	Section 9.5.922

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400B9Ch	PCIE_CORE_RP_ADDR1		0EC0 0B9Ch	Section 9.5.923
00400BA0h	PCIE_CORE_RP_ADDR0		0EC0 0BA0h	Section 9.5.924
00400BA4h	PCIE_CORE_RP_ADDR1		0EC0 0BA4h	Section 9.5.925
00400BA8h	PCIE_CORE_RP_ADDR0		0EC0 0BA8h	Section 9.5.926
00400BACH	PCIE_CORE_RP_ADDR1		0EC0 0BACH	Section 9.5.927
00400BB0h	PCIE_CORE_RP_ADDR0		0EC0 0BB0h	Section 9.5.928
00400BB4h	PCIE_CORE_RP_ADDR1		0EC0 0BB4h	Section 9.5.929
00400BB8h	PCIE_CORE_RP_ADDR0		0EC0 0BB8h	Section 9.5.930
00400BBCh	PCIE_CORE_RP_ADDR1		0EC0 0BBCh	Section 9.5.931
00400BC0h	PCIE_CORE_RP_ADDR0		0EC0 0BC0h	Section 9.5.932
00400BC4h	PCIE_CORE_RP_ADDR1		0EC0 0BC4h	Section 9.5.933
00400BC8h	PCIE_CORE_RP_ADDR0		0EC0 0BC8h	Section 9.5.934
00400BCC h	PCIE_CORE_RP_ADDR1		0EC0 0BCCCh	Section 9.5.935
00400BD0h	PCIE_CORE_RP_ADDR0		0EC0 0BD0h	Section 9.5.936
00400BD4h	PCIE_CORE_RP_ADDR1		0EC0 0BD4h	Section 9.5.937
00400BD8h	PCIE_CORE_RP_ADDR0		0EC0 0BD8h	Section 9.5.938
00400BDC h	PCIE_CORE_RP_ADDR1		0EC0 0BDCCh	Section 9.5.939
00400BE0h	PCIE_CORE_RP_ADDR0		0EC0 0BE0h	Section 9.5.940
00400BE4h	PCIE_CORE_RP_ADDR1		0EC0 0BE4h	Section 9.5.941
00400BE8h	PCIE_CORE_RP_ADDR0		0EC0 0BE8h	Section 9.5.942
00400BECh	PCIE_CORE_RP_ADDR1		0EC0 0BECh	Section 9.5.943
00400BF0h	PCIE_CORE_RP_ADDR0		0EC0 0BF0h	Section 9.5.944
00400BF4h	PCIE_CORE_RP_ADDR1		0EC0 0BF4h	Section 9.5.945
00400BF8h	PCIE_CORE_RP_ADDR0		0EC0 0BF8h	Section 9.5.946
00400BFCh	PCIE_CORE_RP_ADDR1		0EC0 0BFCh	Section 9.5.947

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400C00h	PCIE_CORE_RP_ADDR0		0EC0 0C00h	Section 9.5.948
00400C04h	PCIE_CORE_RP_ADDR1		0EC0 0C04h	Section 9.5.949
00400C08h	PCIE_CORE_RP_ADDR0		0EC0 0C08h	Section 9.5.950
00400C0Ch	PCIE_CORE_RP_ADDR1		0EC0 0C0Ch	Section 9.5.951
00400C10h	PCIE_CORE_RP_ADDR0		0EC0 0C10h	Section 9.5.952
00400C14h	PCIE_CORE_RP_ADDR1		0EC0 0C14h	Section 9.5.953
00400C18h	PCIE_CORE_RP_ADDR0		0EC0 0C18h	Section 9.5.954
00400C1Ch	PCIE_CORE_RP_ADDR1		0EC0 0C1Ch	Section 9.5.955
00400C20h	PCIE_CORE_RP_ADDR0		0EC0 0C20h	Section 9.5.956
00400C24h	PCIE_CORE_RP_ADDR1		0EC0 0C24h	Section 9.5.957
00400C28h	PCIE_CORE_RP_ADDR0		0EC0 0C28h	Section 9.5.958
00400C2Ch	PCIE_CORE_RP_ADDR1		0EC0 0C2Ch	Section 9.5.959
00400C30h	PCIE_CORE_RP_ADDR0		0EC0 0C30h	Section 9.5.960
00400C34h	PCIE_CORE_RP_ADDR1		0EC0 0C34h	Section 9.5.961
00400C38h	PCIE_CORE_RP_ADDR0		0EC0 0C38h	Section 9.5.962
00400C3Ch	PCIE_CORE_RP_ADDR1		0EC0 0C3Ch	Section 9.5.963
00400C40h	PCIE_CORE_RP_ADDR0		0EC0 0C40h	Section 9.5.964
00400C44h	PCIE_CORE_RP_ADDR1		0EC0 0C44h	Section 9.5.965
00400C48h	PCIE_CORE_RP_ADDR0		0EC0 0C48h	Section 9.5.966
00400C4Ch	PCIE_CORE_RP_ADDR1		0EC0 0C4Ch	Section 9.5.967
00400C50h	PCIE_CORE_RP_ADDR0		0EC0 0C50h	Section 9.5.968
00400C54h	PCIE_CORE_RP_ADDR1		0EC0 0C54h	Section 9.5.969
00400C58h	PCIE_CORE_RP_ADDR0		0EC0 0C58h	Section 9.5.970
00400C5Ch	PCIE_CORE_RP_ADDR1		0EC0 0C5Ch	Section 9.5.971
00400C60h	PCIE_CORE_RP_ADDR0		0EC0 0C60h	Section 9.5.972

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400C64h	PCIE_CORE_RP_ADDR1		0EC0 0C64h	Section 9.5.973
00400C68h	PCIE_CORE_RP_ADDR0		0EC0 0C68h	Section 9.5.974
00400C6Ch	PCIE_CORE_RP_ADDR1		0EC0 0C6Ch	Section 9.5.975
00400C70h	PCIE_CORE_RP_ADDR0		0EC0 0C70h	Section 9.5.976
00400C74h	PCIE_CORE_RP_ADDR1		0EC0 0C74h	Section 9.5.977
00400C78h	PCIE_CORE_RP_ADDR0		0EC0 0C78h	Section 9.5.978
00400C7Ch	PCIE_CORE_RP_ADDR1		0EC0 0C7Ch	Section 9.5.979
00400C80h	PCIE_CORE_RP_ADDR0		0EC0 0C80h	Section 9.5.980
00400C84h	PCIE_CORE_RP_ADDR1		0EC0 0C84h	Section 9.5.981
00400C88h	PCIE_CORE_RP_ADDR0		0EC0 0C88h	Section 9.5.982
00400C8Ch	PCIE_CORE_RP_ADDR1		0EC0 0C8Ch	Section 9.5.983
00400C90h	PCIE_CORE_RP_ADDR0		0EC0 0C90h	Section 9.5.984
00400C94h	PCIE_CORE_RP_ADDR1		0EC0 0C94h	Section 9.5.985
00400C98h	PCIE_CORE_RP_ADDR0		0EC0 0C98h	Section 9.5.986
00400C9Ch	PCIE_CORE_RP_ADDR1		0EC0 0C9Ch	Section 9.5.987
00400CA0h	PCIE_CORE_RP_ADDR0		0EC0 0CA0h	Section 9.5.988
00400CA4h	PCIE_CORE_RP_ADDR1		0EC0 0CA4h	Section 9.5.989
00400CA8h	PCIE_CORE_RP_ADDR0		0EC0 0CA8h	Section 9.5.990
00400CAC h	PCIE_CORE_RP_ADDR1		0EC0 0CACCh	Section 9.5.991
00400CB0h	PCIE_CORE_RP_ADDR0		0EC0 0CB0h	Section 9.5.992
00400CB4h	PCIE_CORE_RP_ADDR1		0EC0 0CB4h	Section 9.5.993
00400CB8h	PCIE_CORE_RP_ADDR0		0EC0 0CB8h	Section 9.5.994
00400CBC h	PCIE_CORE_RP_ADDR1		0EC0 0CBCh	Section 9.5.995
00400CC0h	PCIE_CORE_RP_ADDR0		0EC0 0CC0h	Section 9.5.996
00400CC4h	PCIE_CORE_RP_ADDR1		0EC0 0CC4h	Section 9.5.997

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400CC8h	PCIE_CORE_RP_ADDR0		0EC0 0CC8h	Section 9.5.998
00400CCC h	PCIE_CORE_RP_ADDR1		0EC0 0CCCCh	Section 9.5.999
00400CD0h	PCIE_CORE_RP_ADDR0		0EC0 0CD0h	Section 9.5.1000
00400CD4h	PCIE_CORE_RP_ADDR1		0EC0 0CD4h	Section 9.5.1001
00400CD8h	PCIE_CORE_RP_ADDR0		0EC0 0CD8h	Section 9.5.1002
00400CDC h	PCIE_CORE_RP_ADDR1		0EC0 0CDCh	Section 9.5.1003
00400CE0h	PCIE_CORE_RP_ADDR0		0EC0 0CE0h	Section 9.5.1004
00400CE4h	PCIE_CORE_RP_ADDR1		0EC0 0CE4h	Section 9.5.1005
00400CE8h	PCIE_CORE_RP_ADDR0		0EC0 0CE8h	Section 9.5.1006
00400CEC h	PCIE_CORE_RP_ADDR1		0EC0 0CECh	Section 9.5.1007
00400CF0h	PCIE_CORE_RP_ADDR0		0EC0 0CF0h	Section 9.5.1008
00400CF4h	PCIE_CORE_RP_ADDR1		0EC0 0CF4h	Section 9.5.1009
00400CF8h	PCIE_CORE_RP_ADDR0		0EC0 0CF8h	Section 9.5.1010
00400CFCh	PCIE_CORE_RP_ADDR1		0EC0 0CFCh	Section 9.5.1011
00400D00h	PCIE_CORE_RP_ADDR0		0EC0 0D00h	Section 9.5.1012
00400D04h	PCIE_CORE_RP_ADDR1		0EC0 0D04h	Section 9.5.1013
00400D08h	PCIE_CORE_RP_ADDR0		0EC0 0D08h	Section 9.5.1014
00400D0Ch	PCIE_CORE_RP_ADDR1		0EC0 0D0Ch	Section 9.5.1015
00400D10h	PCIE_CORE_RP_ADDR0		0EC0 0D10h	Section 9.5.1016
00400D14h	PCIE_CORE_RP_ADDR1		0EC0 0D14h	Section 9.5.1017
00400D18h	PCIE_CORE_RP_ADDR0		0EC0 0D18h	Section 9.5.1018
00400D1Ch	PCIE_CORE_RP_ADDR1		0EC0 0D1Ch	Section 9.5.1019
00400D20h	PCIE_CORE_RP_ADDR0		0EC0 0D20h	Section 9.5.1020
00400D24h	PCIE_CORE_RP_ADDR1		0EC0 0D24h	Section 9.5.1021
00400D28h	PCIE_CORE_RP_ADDR0		0EC0 0D28h	Section 9.5.1022

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400D2Ch	PCIE_CORE_RP_ADDR1		0EC0 0D2Ch	Section 9.5.1023
00400D30h	PCIE_CORE_RP_ADDR0		0EC0 0D30h	Section 9.5.1024
00400D34h	PCIE_CORE_RP_ADDR1		0EC0 0D34h	Section 9.5.1025
00400D38h	PCIE_CORE_RP_ADDR0		0EC0 0D38h	Section 9.5.1026
00400D3Ch	PCIE_CORE_RP_ADDR1		0EC0 0D3Ch	Section 9.5.1027
00400D40h	PCIE_CORE_RP_ADDR0		0EC0 0D40h	Section 9.5.1028
00400D44h	PCIE_CORE_RP_ADDR1		0EC0 0D44h	Section 9.5.1029
00400D48h	PCIE_CORE_RP_ADDR0		0EC0 0D48h	Section 9.5.1030
00400D4Ch	PCIE_CORE_RP_ADDR1		0EC0 0D4Ch	Section 9.5.1031
00400D50h	PCIE_CORE_RP_ADDR0		0EC0 0D50h	Section 9.5.1032
00400D54h	PCIE_CORE_RP_ADDR1		0EC0 0D54h	Section 9.5.1033
00400D58h	PCIE_CORE_RP_ADDR0		0EC0 0D58h	Section 9.5.1034
00400D5Ch	PCIE_CORE_RP_ADDR1		0EC0 0D5Ch	Section 9.5.1035
00400D60h	PCIE_CORE_RP_ADDR0		0EC0 0D60h	Section 9.5.1036
00400D64h	PCIE_CORE_RP_ADDR1		0EC0 0D64h	Section 9.5.1037
00400D68h	PCIE_CORE_RP_ADDR0		0EC0 0D68h	Section 9.5.1038
00400D6Ch	PCIE_CORE_RP_ADDR1		0EC0 0D6Ch	Section 9.5.1039
00400D70h	PCIE_CORE_RP_ADDR0		0EC0 0D70h	Section 9.5.1040
00400D74h	PCIE_CORE_RP_ADDR1		0EC0 0D74h	Section 9.5.1041
00400D78h	PCIE_CORE_RP_ADDR0		0EC0 0D78h	Section 9.5.1042
00400D7Ch	PCIE_CORE_RP_ADDR1		0EC0 0D7Ch	Section 9.5.1043
00400D80h	PCIE_CORE_RP_ADDR0		0EC0 0D80h	Section 9.5.1044
00400D84h	PCIE_CORE_RP_ADDR1		0EC0 0D84h	Section 9.5.1045
00400D88h	PCIE_CORE_RP_ADDR0		0EC0 0D88h	Section 9.5.1046
00400D8Ch	PCIE_CORE_RP_ADDR1		0EC0 0D8Ch	Section 9.5.1047

Table 9-1182. PCIE_CORE_RP Registers (continued)

Offset	Acronym	Register Name	PCIE3_CO RE_DBN_C FG_PCIE_ CORE Physical Address	Section
00400D90h	PCIE_CORE_RP_ADDR0		0EC0 0D90h	Section 9.5.1048
00400D94h	PCIE_CORE_RP_ADDR1		0EC0 0D94h	Section 9.5.1049
00400D98h	PCIE_CORE_RP_ADDR0		0EC0 0D98h	Section 9.5.1050
00400D9Ch	PCIE_CORE_RP_ADDR1		0EC0 0D9Ch	Section 9.5.1051
00400DA0h	PCIE_CORE_RP_ADDR0		0EC0 0DA0h	Section 9.5.1052
00400DA4h	PCIE_CORE_RP_ADDR1		0EC0 0DA4h	Section 9.5.1053
00400DA8h	PCIE_CORE_RP_ADDR0		0EC0 0DA8h	Section 9.5.1054
00400DAC h	PCIE_CORE_RP_ADDR1		0EC0 0DACH	Section 9.5.1055
00400DB0h	PCIE_CORE_RP_ADDR0		0EC0 0DB0h	Section 9.5.1056
00400DB4h	PCIE_CORE_RP_ADDR1		0EC0 0DB4h	Section 9.5.1057
00400DB8h	PCIE_CORE_RP_ADDR0		0EC0 0DB8h	Section 9.5.1058
00400DBC h	PCIE_CORE_RP_ADDR1		0EC0 0DBCCh	Section 9.5.1059

9.5.1 PCIE_CORE_RP_I_VENDOR_ID_DEVICE_ID Register (Offset = 0h) [reset = 010017CDh]

PCIE_CORE_RP_I_VENDOR_ID_DEVICE_ID is shown in [Figure 9-390](#) and described in [Table 9-1184](#).

Return to [Summary Table](#).

N/A

Table 9-1183.
PCIE_CORE_RP_I_VENDOR_ID_DEVICE_ID
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0000h

Figure 9-390. PCIE_CORE_RP_I_VENDOR_ID_DEVICE_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DID																VID															
R-100h																R-17CDh															

LEGEND: R = Read Only; -n = value after reset

Table 9-1184. PCIE_CORE_RP_I_VENDOR_ID_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DID	R	100h	Device ID assigned by the manufacturer of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
15-0	VID	R	17CDh	This is the Vendor ID assigned by PCI SIG to the manufacturer of the device. The Vendor ID is set in the Vendor ID Register within the local management register block.

9.5.2 PCIe_CORE_RP_I_COMMAND_STATUS Register (Offset = 4h) [reset = 00100000h]

PCIE_CORE_RP_I_COMMAND_STATUS is shown in [Figure 9-391](#) and described in [Table 9-1186](#).

Return to [Summary Table](#).

N/A

Table 9-1185.
PCIE_CORE_RP_I_COMMAND_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0004h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0004h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0004h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0004h

Figure 9-391. PCIe_CORE_RP_I_COMMAND_STATUS Register

31	30	29	28	27	26	25	24
DPE	SSE	RMA	RTA	STA	R6	MDPE	
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	
23	22	21	20	19	18	17	16
	R5		CL	IS		R4	
	R-0h		R-1h	R-0h		R-0h	
15	14	13	12	11	10	9	8
		R3			IMD	R2	SE
		R-0h			R/W-0h	R-0h	R/W-0h
7	6	5	4	3	2	1	0
R1	PERE		R0		BE	MSE	ISE
R-0h	R/W-0h		R-0h		R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1186. PCIe_CORE_RP_I_COMMAND_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DPE	R/W1C	0h	This bit is set when the Controller has received a poisoned TLP. The Parity Error Response enable bit [bit 6] has no effect on the setting of this bit. This field can also be cleared from the local management bus APB by writing a 1 into this bit position. This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 9-1186. PCIE_CORE_RP_I_COMMAND_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	SSE	R/W1C	0h	<p>The Controller sets this bit [i]On receiving an error message from the link, if SERR-Enable in PCI Command Register is 1 and SERR-Enable in the Bridge Control Register is also 1.</p> <p>[ii]On any internal Fatal/Non-Fatal error detected, if SERR-Enable in PCI Command Register is 1.</p> <p>This field can also be cleared from the local management APB bus by writing a 1 into this bit position.</p> <p>This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.</p>
29	RMA	R/W1C	0h	<p>This bit is set when the Controller has received a completion from the link with the Unsupported Request status.</p> <p>This field can also be cleared from the local management APB bus by writing a 1 into this bit position</p> <p>This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.</p>
28	RTA	R/W1C	0h	<p>This bit is set when the Controller has received a completion from the link with the Completer Abort status.</p> <p>This field can also be cleared from the local management APB bus by writing a 1 into this bit position.</p> <p>This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.</p>
27	STA	R/W1C	0h	<p>This bit is set when the Controller has sent a completion to the link with the Completer Abort status.</p> <p>This field can also be cleared from the local management APB bus by writing a 1 into this bit position.</p> <p>This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.</p>
26-25	R6	R	0h	Reserved
24	MDPE	R/W1C	0h	<p>When the Parity Error Response enable bit is 1, the Controller sets this bit when it detects the following error conditions: [i] The Controller receives a poisoned request from the link.</p> <p>[ii] The Controller has sent a Poisoned Completion downstream to the link This bit remains 0 when the Parity Error Response enable bit is 0.</p> <p>This field can be forced to 1 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.</p>
23-21	R5	R	0h	Reserved
20	CL	R	1h	<p>Indicates the presence of PCI Extended Capabilities registers.</p> <p>This bit is hardwired to 1.</p>

Table 9-1186. PCIE_CORE_RP_I_COMMAND_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	IS	R	0h	This bit is valid only when the Controller is configured to support legacy interrupts. Indicates that the Controller has a pending interrupt, that is, the Controller has sent an Assert_INTx message but has not transmitted a corresponding Deassert_INTx message.
18-16	R4	R	0h	Reserved
15-11	R3	R	0h	Reserved
10	IMD	R/W	0h	Enables or disables the transmission of INTx Assert and De-assert messages from the Controller. The setting of this bit has no effect on the operation of the Controller in the RC mode.
9	R2	R	0h	Reserved
8	SE	R/W	0h	Enables the reporting of fatal and non-fatal errors detected by the Controller to the Root Complex.
7	R1	R	0h	Reserved
6	PERE	R/W	0h	When this bit is 1, the Controller sets the Master Data Parity Error status bit when it detects the following error conditions: [i] The Controller receives a poisoned completion from the link in response to a request. [ii] The Controller sends out a poisoned write request on the link [this may be because an underflow occurred during the packet transfer at the host interface of the Controller.]. When this bit is 0, the Master Data Parity Error status bit is never set.
5-3	R0	R	0h	Reserved
2	BE	R/W	0h	For a Function with a Type 1 Configurations Space header[Controller in RP Mode], this bit controls forwarding of Memory or I/O Requests by a Port in the Upstream direction. Note: The Controller does not generate any response based on this bit. Client application logic must use this bit and respond to requests appropriately: - When this bit is '1', Client logic can process the Memory and IO Requests received from PCIe Link normally. - When this bit is '0', Client logic must handle Memory and IO Requests received from PCIe Link as Unsupported Requests.
1	MSE	R/W	0h	For a Function with a Type 1 Configuration Space header[Controller in RP Mode], this bit controls the response to Memory Space accesses received on its Primary Side. Note: The Controller does not generate any response based on this bit. - Client must check for this bit to be '1' before initiating any Memory requests on the pcie_master_AXI interface.

Table 9-1186. PCIE_CORE_RP_I_COMMAND_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ISE	R/W	0h	<p>For a Function with a Type 1 Configuration Space header [Controller in RP Mode] , this bit controls the response to I/O Space accesses received on its Primary Side.</p> <p>Note: The Controller does not generate any response based on this bit.</p> <p>- Client must check for this bit to be '1' before initiating any IO requests on the pcie_master_AXI interface.</p>

9.5.3 PCIE_CORE_RP_I_REVISION_ID_CLASS_CODE Register (Offset = 8h) [reset = 0h]

PCIE_CORE_RP_I_REVISION_ID_CLASS_CODE is shown in [Figure 9-392](#) and described in [Table 9-1188](#).

Return to [Summary Table](#).

N/A

Table 9-1187.
PCIE_CORE_RP_I_REVISION_ID_CLASS_CODE
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0008h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0008h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0008h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0008h

Figure 9-392. PCIE_CORE_RP_I_REVISION_ID_CLASS_CODE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC								SCC								PIB								RID							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-1188. PCIE_CORE_RP_I_REVISION_ID_CLASS_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CC	R	0h	Identifies the function of the device. On power-up, the Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
23-16	SCC	R	0h	Identifies a sub-category within the selected function. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
15-8	PIB	R	0h	Identifies the register set layout of the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
7-0	RID	R	0h	Assigned by the manufacturer of the device to identify the revision number of the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

9.5.4 PCIE_CORE_RP_I_BIST_HEADER_LATENCY_CACHE_LINE Register (Offset = Ch) [reset = 00010000h]

PCIE_CORE_RP_I_BIST_HEADER_LATENCY_CACHE_LINE is shown in [Figure 9-393](#) and described in [Table 9-1190](#).

Return to [Summary Table](#).

N/A

Table 9-1189.
PCIE_CORE_RP_I_BIST_HEADER_LATENCY_CACH
E_LINE Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 000Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 000Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 000Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 000Ch

Figure 9-393. PCIE_CORE_RP_I_BIST_HEADER_LATENCY_CACHE_LINE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BR								DT	HT						
R-0h								R-0h	R-1h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LT								CLS							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1190. PCIE_CORE_RP_I_BIST_HEADER_LATENCY_CACHE_LINE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BR	R	0h	BIST control register. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
23	DT	R	0h	Identifies whether the device supports a single Function or multiple Functions. Hardwired to zero
22-16	HT	R	1h	Identifies format of header. This field is hardwired to 1.
15-8	LT	R	0h	This is an unused field and is hardwired to 0.
7-0	CLS	R/W	0h	Cache Line Size Register defined in PCI Specifications 3.0. This field can be read or written, both from the link and from the local management bus, but its value is not used.

9.5.5 PCIE_CORE_RP_I_RC_BAR_0 Register (Offset = 10h) [reset = 0h]

PCIE_CORE_RP_I_RC_BAR_0 is shown in [Figure 9-394](#) and described in [Table 9-1192](#).

Return to [Summary Table](#).

N/A

**Table 9-1191. PCIE_CORE_RP_I_RC_BAR_0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0010h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0010h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0010h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0010h

Figure 9-394. PCIE_CORE_RP_I_RC_BAR_0 Register

31	30	29	28	27	26	25	24
BAMRW							
R/W-0h							
23	22	21	20	19	18	17	16
BAMRW		BAMR0					
R/W-0h		R-0h					
15	14	13	12	11	10	9	8
BAMR0							
R-0h							
7	6	5	4	3	2	1	0
BAMR0				P0	S0	R7	MSI0
R-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1192. PCIE_CORE_RP_I_RC_BAR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	BAMRW	R/W	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in Root Complex BAR Configuration Register. All other bits are not writeable, and are read as 0's.
21-4	BAMR0	R	0h	This field defines the base address of the memory address range. The number of implemented bits in this field determines the BAR aperture configured in Root Complex BAR Configuration Register. All other bits are not writeable, and are read as 0's.
3	P0	R	0h	For memory BAR: This bit reads as 1 when BAR 0 is configured as a prefetchable BAR, and as 0 when configured as a non-prefetchable BAR. For IO BAR: This is bit 3 of the base address. The value read in this field is determined by the setting of Root Complex BAR Configuration Register.

Table 9-1192. PCIE_CORE_RP_I_RC_BAR_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	S0	R	0h	For memory BAR: This bit reads as 0 when BAR 0 is configured as a 32-bit BAR, and as 1 when configured as a 64-bit BAR. For IO BAR: This is bit 3 of the base address. The value read in this field is determined by the setting of Root Complex BAR Configuration Register.
1	R7	R	0h	This bit is hardwired to 0 for both memory and I/O BARs.
0	MSI0	R	0h	Specifies whether this BAR defines a memory address range or an I/O address range [0 = memory, 1 = I/O]. The value read in this field is determined by the setting of Root Complex BAR Configuration Register.

9.5.6 PCIE_CORE_RP_I_RC_BAR_1 Register (Offset = 14h) [reset = 0h]

PCIE_CORE_RP_I_RC_BAR_1 is shown in [Figure 9-395](#) and described in [Table 9-1194](#).

Return to [Summary Table](#).

N/A

**Table 9-1193. PCIE_CORE_RP_I_RC_BAR_1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0014h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0014h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0014h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0014h

Figure 9-395. PCIE_CORE_RP_I_RC_BAR_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1194. PCIE_CORE_RP_I_RC_BAR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R7	R	0h	This field is reserved at power-on. This can be changed using BAR configuration regsiter in LM space.

9.5.7 PCIE_CORE_RP_I_PCIE_BUS_NUMBERS Register (Offset = 18h) [reset = 0h]

PCIE_CORE_RP_I_PCIE_BUS_NUMBERS is shown in [Figure 9-396](#) and described in [Table 9-1196](#).

Return to [Summary Table](#).

N/A

Table 9-1195.
PCIE_CORE_RP_I_PCIE_BUS_NUMBERS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0018h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0018h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0018h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0018h

Figure 9-396. PCIE_CORE_RP_I_PCIE_BUS_NUMBERS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLTN								SUBN								SBN								PBN							
R-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1196. PCIE_CORE_RP_I_PCIE_BUS_NUMBERS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SLTN	R	0h	This field is not implemented.
23-16	SUBN	R/W	0h	This field can be read and written from the local management bus, but its value is not used within the Controller.
15-8	SBN	R/W	0h	This field can be read and written from the local management bus, but its value is not used within the Controller.
7-0	PBN	R/W	0h	This field can be read and written from the local management bus, but its value is not used within the Controller.

9.5.8 PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT Register (Offset = 1Ch) [reset = 0h]

PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT is shown in [Figure 9-397](#) and described in [Table 9-1198](#).

Return to [Summary Table](#).

N/A

Table 9-1197.
PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 001Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 001Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 001Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 001Ch

Figure 9-397. PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT Register

31	30	29	28	27	26	25	24
DPE	RSE	RMA	RTA	STA	R4		MPE
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h		R/W1C-0h
23	22	21	20	19	18	17	16
R3							
R-0h							
15	14	13	12	11	10	9	8
ILR				R2		IOBS2	
R-0h				R-0h		R-0h	
7	6	5	4	3	2	1	0
IBR				R1		IOBS1	
R-0h				R-0h		R-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1198. PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DPE	R/W1C	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
30	RSE	R/W1C	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
29	RMA	R/W1C	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 9-1198. PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	RTA	R/W1C	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
27	STA	R/W1C	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
26-25	R4	R	0h	Reserved
24	MPE	R/W1C	0h	The Controller does not set this bit by itself. This bit can be cleared by writing a 1 into this bit position from the local management APB bus. This field can be forced to 1 or 0 from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write. Note that this bit can be set only when the Parity Error Response Enable bit is set in the Bridge Control Register
23-16	R3	R	0h	Reserved
15-12	ILR	R	0h	This field can be read and written from the local management bus if IO BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.
11-9	R2	R	0h	Reserved
8	IOBS2	R	0h	value set in Type1 cfg IO bar size[bit 20 of RC BAR CONFIG register].If type1 cfg IObar enable bit[bit 19 in RC BAR CONFIG register] is not set, then this field will be hard coded to 0.
7-4	IBR	R	0h	This field can be read and written from the local management bus if IO BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.
3-1	R1	R	0h	Reserved
0	IOBS1	R	0h	value set in Type1 cfg IO bar size[bit 20 of RC BAR CONFIG register]. If type1 cfg IObar enable bit[bit 19 in RC BAR CONFIG register] is not set, then this field will be hard coded to 0.

9.5.9 PCIe_CORE_RP_I_PCIE_MEM_BASE_LIMIT Register (Offset = 20h) [reset = 0h]

PCIe_CORE_RP_I_PCIE_MEM_BASE_LIMIT is shown in [Figure 9-398](#) and described in [Table 9-1200](#).

Return to [Summary Table](#).

N/A

Table 9-1199.
PCIe_CORE_RP_I_PCIE_MEM_BASE_LIMIT
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0020h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0020h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0020h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0020h

Figure 9-398. PCIe_CORE_RP_I_PCIE_MEM_BASE_LIMIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MLR												R2				MBR								R1							
R/W-0h												R-0h				R/W-0h								R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1200. PCIe_CORE_RP_I_PCIE_MEM_BASE_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	MLR	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
19-16	R2	R	0h	Reserved
15-4	MBR	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
3-0	R1	R	0h	Reserved

9.5.10 PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_LIMIT Register (Offset = 24h) [reset = 0h]

PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_LIMIT is shown in [Figure 9-399](#) and described in [Table 9-1202](#).

Return to [Summary Table](#).

N/A

Table 9-1201.
PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_LIMIT
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0024h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0024h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0024h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0024h

Figure 9-399. PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_LIMIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMLR																PMBR															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1202. PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PMLR	R	0h	This field can be read and written from the local management APB bus if prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.
15-0	PMBR	R	0h	This field can be read and written from the local management APB bus if prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.

9.5.11 PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_UPPER Register (Offset = 28h) [reset = 0h]

PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_UPPER is shown in [Figure 9-400](#) and described in [Table 9-1204](#).

Return to [Summary Table](#).

N/A

Table 9-1203.
PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_UPPER
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0028h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0028h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0028h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0028h

Figure 9-400. PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_UPPER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBRU																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1204. PCIE_CORE_RP_I_PCIE_PREFETCH_BASE_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PBRU	R	0h	This field can be read and written from the local management APB bus if 64bit prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.

9.5.12 PCIE_CORE_RP_I_PCIE_PREFETCH_LIMIT_UPPER Register (Offset = 2Ch) [reset = 0h]

PCIE_CORE_RP_I_PCIE_PREFETCH_LIMIT_UPPER is shown in [Figure 9-401](#) and described in [Table 9-1206](#).

Return to [Summary Table](#).

N/A

Table 9-1205.
PCIE_CORE_RP_I_PCIE_PREFETCH_LIMIT_UPPER
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 002Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 002Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 002Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 002Ch

Figure 9-401. PCIE_CORE_RP_I_PCIE_PREFETCH_LIMIT_UPPER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLRU																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1206. PCIE_CORE_RP_I_PCIE_PREFETCH_LIMIT_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PLRU	R	0h	This field can be read and written from the local management APB bus if 64bit prefetchable memory is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.

9.5.13 PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT_UPPER Register (Offset = 30h) [reset = 0h]

PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT_UPPER is shown in [Figure 9-402](#) and described in [Table 9-1208](#).

Return to [Summary Table](#).

N/A

Table 9-1207.
PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT_UPPER
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0030h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0030h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0030h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0030h

Figure 9-402. PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT_UPPER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ILR																IBRU															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1208. PCIE_CORE_RP_I_PCIE_IO_BASE_LIMIT_UPPER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ILR	R	0h	This field can be read and written from the local management bus if 32bit IO BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.
15-0	IBRU	R	0h	This field can be read and written from the local management bus if 32bit IO BAR is enabled in the Root Complex BAR configuration register, else it is hardwired to zero. Its value is not used within the Controller.

9.5.14 PCIE_CORE_RP_I_CAPABILITIES_POINTER Register (Offset = 34h) [reset = 80h]

PCIE_CORE_RP_I_CAPABILITIES_POINTER is shown in [Figure 9-403](#) and described in [Table 9-1210](#).

Return to [Summary Table](#).

N/A

Table 9-1209.
PCIE_CORE_RP_I_CAPABILITIES_POINTER
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0034h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0034h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0034h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0034h

Figure 9-403. PCIE_CORE_RP_I_CAPABILITIES_POINTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15																CP															
R-0h																R-80h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1210. PCIE_CORE_RP_I_CAPABILITIES_POINTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R15	R	0h	Reserved
7-0	CP	R	80h	Contains pointer to the first PCI Capability Structure. This field is set by default to the value defined in the RTL file reg_defaults.h. It can be re-written independently for every Function from the local management APB bus.

9.5.15 PCIe_CORE_RP_RSVD_0E Register (Offset = 38h) [reset = 0h]

PCIE_CORE_RP_RSVD_0E is shown in [Figure 9-404](#) and described in [Table 9-1212](#).

Return to [Summary Table](#).

N/A

Table 9-1211. PCIe_CORE_RP_RSVD_0E Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0038h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0038h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0038h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0038h

Figure 9-404. PCIe_CORE_RP_RSVD_0E Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1212. PCIe_CORE_RP_RSVD_0E Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RSVD	R	0h	Reserved

9.5.16 PCIE_CORE_RP_I_INTRPT_LINE_INTRPT_PIN Register (Offset = 3Ch) [reset = 1FFh]

PCIE_CORE_RP_I_INTRPT_LINE_INTRPT_PIN is shown in [Figure 9-405](#) and described in [Table 9-1214](#).

Return to [Summary Table](#).

N/A

Table 9-1213.
PCIE_CORE_RP_I_INTRPT_LINE_INTRPT_PIN
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 003Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 003Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 003Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 003Ch

Figure 9-405. PCIE_CORE_RP_I_INTRPT_LINE_INTRPT_PIN Register

31	30	29	28	27	26	25	24
R23							
R-0h							
23	22	21	20	19	18	17	16
R23	BCRSBR	R21	VGA16D	VGAE	ISAE	BCSE	PERE
R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
R5				IPR			
R-0h				R-1h			
7	6	5	4	3	2	1	0
ILR							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1214. PCIE_CORE_RP_I_INTRPT_LINE_INTRPT_PIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	R23	R	0h	Reserved
22	BCRSBR	R/W	0h	This field can be read and written from the local management APB bus. When set, it initiates a hot reset on the link.
21	R21	R	0h	Reserved
20	VGA16D	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
19	VGAE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
18	ISAE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
17	BCSE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
16	PERE	R/W	0h	This field can be read and written from the local management APB bus. It is used only to enable the Master Data Parity Error bit in the Secondary Status Register.

Table 9-1214. PCIE_CORE_RP_I_INTRPT_LINE_INTRPT_PIN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	R5	R	0h	Reserved
10-8	IPR	R	1h	Identifies the interrupt input [A, B, C, D] to which this Functions interrupt output is connected to [01 = INTA, 02 = INTB, 03 = INTC, 04 = INTD]. The assignment of interrupt inputs to Functions is fixed when the Controller is configured. This field can be re-written independently for each Function from the local management bus. Default values - PF 0: 01 [INTA], PF 1: 02 [INTB].
7-0	ILR	R/W	FFh	This field can be read and written from the local management bus, but its value is not used within the Controller. The given reset value is for PF0.

9.5.17 PCIE_CORE_RP_I_PWR_MGMT_CAP Register (Offset = 80h) [reset = 5A039001h]

PCIE_CORE_RP_I_PWR_MGMT_CAP is shown in [Figure 9-406](#) and described in [Table 9-1216](#).

Return to [Summary Table](#).

N/A

Table 9-1215. PCIE_CORE_RP_I_PWR_MGMT_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0080h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0080h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0080h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0080h

Figure 9-406. PCIE_CORE_RP_I_PWR_MGMT_CAP Register

31	30	29	28	27	26	25	24
PSDCS	PSDHS	PSD2S	PSD1S	PSD0S	D2S	D1S	MCRAPS
R-0h	R-1h	R-0h	R-1h	R-1h	R-0h	R-1h	R-0h
23	22	21	20	19	18	17	16
MCRAPS		DSI	R0	PC		VID	
R-0h		R-0h	R-0h	R-0h		R-3h	
15	14	13	12	11	10	9	8
			CP				
			R-90h				
7	6	5	4	3	2	1	0
			CID				
			R-1h				

LEGEND: R = Read Only; -n = value after reset

Table 9-1216. PCIE_CORE_RP_I_PWR_MGMT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PSDCS	R	0h	Indicates whether the Function is capable of sending PME messages when in the D3cold state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
30	PSDHS	R	1h	Indicates whether the Function is capable of sending PME messages when in the D3hot state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
29	PSD2S	R	0h	Indicates whether the Function is capable of sending PME messages when in the D2 state. This bit is hardwired to 0 because D2 state is not supported.

Table 9-1216. PCIE_CORE_RP_I_PWR_MGMT_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	PSD1S	R	1h	Indicates whether the Function is capable of sending PME messages when in the D1 state. This bit is set to 1 by default, but can be modified from the local management bus by writing into Function 0. All other Functions assume the value set in Function 0s Power Management Capabilities Register.
27	PSD0S	R	1h	Indicates whether the Function is capable of sending PME messages when in the D0 state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
26	D2S	R	0h	Set if the Function supports the D2 power state. Currently hardwired to 0.
25	D1S	R	1h	Set if the Function supports the D1 power state. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
24-22	MCRAPS	R	0h	Specifies the maximum current drawn by the device from the aux power source in the D3cold state. This field is not implemented in devices not supporting PME notification when in the D3cold state, and is therefore hardwired to 0.
21	DSI	R	0h	This bit, when set, indicates that the device requires additional configuration steps beyond setting up its PCI configuration space, to bring it to the D0 active state from the D0 uninitialized state. This bit is hardwired to 0.
20	R0	R	0h	Reserved
19	PC	R	0h	Not applicable to PCI Express. This bit is hardwired to 0.
18-16	VID	R	3h	Indicates the version of the PCI Bus Power Management Specifications that the Function implements. This field is set by default to 011 [Version 1.2]. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
15-8	CP	R	90h	Contains pointer to the next PCI Capability Structure. The Controller sets it to the value defined in the RTL file reg_defaults.h. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 9-1216. PCIE_CORE_RP_I_PWR_MGMT_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CID	R	1h	Identifies that the capability structure is for Power Management. This field is set by default to 01 hex. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

9.5.18 PCIE_CORE_RP_I_PWR_MGMT_CTRL_STAT_REP Register (Offset = 84h) [reset = 8h]

PCIE_CORE_RP_I_PWR_MGMT_CTRL_STAT_REP is shown in [Figure 9-407](#) and described in [Table 9-1218](#).

Return to [Summary Table](#).

N/A

Table 9-1217.
PCIE_CORE_RP_I_PWR_MGMT_CTRL_STAT_REP
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0084h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0084h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0084h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0084h

Figure 9-407. PCIE_CORE_RP_I_PWR_MGMT_CTRL_STAT_REP Register

31	30	29	28	27	26	25	24
DR							
R-0h							
23	22	21	20	19	18	17	16
R1							
R-0h							
15	14	13	12	11	10	9	8
PMES	R2						PE
R/W1C-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
R3				NSR	R4	PS	
R-0h				R-1h	R-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1218. PCIE_CORE_RP_I_PWR_MGMT_CTRL_STAT_REP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DR	R	0h	This optional register is not implemented in the Cadence PCIe Controller. This field is hardwired to 0.
23-16	R1	R	0h	Reserved
15	PMES	R/W1C	0h	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write..
14-9	R2	R	0h	Reserved
8	PE	R/W	0h	This bit can be set or cleared from the local management APB bus, by writing a 1 or 0, respectively.
7-4	R3	R	0h	Reserved
3	NSR	R	1h	This bit is set to 1 by default. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
2	R4	R	0h	Reserved

Table 9-1218. PCIE_CORE_RP_I_PWR_MGMT_CTRL_STAT_REP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PS	R/W	0h	This field can also be read or written from the local management APBbus.

9.5.19 PCIE_CORE_RP_I_MSI_CTRL_REG Register (Offset = 90h) [reset = 0180B005h]

PCIE_CORE_RP_I_MSI_CTRL_REG is shown in [Figure 9-408](#) and described in [Table 9-1220](#).

Return to [Summary Table](#).

N/A

**Table 9-1219. PCIE_CORE_RP_I_MSI_CTRL_REG
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0090h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0090h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0090h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0090h

Figure 9-408. PCIE_CORE_RP_I_MSI_CTRL_REG Register

31	30	29	28	27	26	25	24
R0							MC
R-0h							R-1h
23	22	21	20	19	18	17	16
BAC64	MME			MMC			ME
R-1h	R/W-0h			R-0h			R/W-0h
15	14	13	12	11	10	9	8
CP1							
R-B0h							
7	6	5	4	3	2	1	0
CID1							
R-5h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1220. PCIE_CORE_RP_I_MSI_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	R0	R	0h	Reserved
24	MC	R	1h	can be modified using localmanagement interface
23	BAC64	R	1h	Set to 1 to indicate that the device is capable of generating 64-bit addresses for MSI messages.Can be modified using local management interface
22-20	MME	R/W	0h	Encodes the number of distinct messages that the Controller is programmed to generate for this Function [000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32]. This setting must be based on the number of interrupt inputs of the Controller that are actually used by this Function. This field can be written from the local management bus.

Table 9-1220. PCIE_CORE_RP_I_MSI_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-17	MMC	R	0h	<p>Encodes the number of distinct messages that the Controller is capable of generating for this Function</p> <p>[000 = 1, 001 = 2, 010 = 4, 011 = 8, 100 = 16, 101 = 32].</p> <p>Thus, this field defines the number of the interrupt vectors for this Function. The Controller allows up to 32 distinct messages, but the setting of this field must be based on the number of interrupt inputs of the Controller that are actually used by the client. For example, if the client logic uses 8 of the 32 distinct MSI interrupt inputs of the Controller for this Function, then the value of this field must be set to 011.</p> <p>This field can be written from the local management bus. Please see the define den_db_Fx_MSI_MULTIPLE_MSG_CAPABLE values [where x is the function number] for default values of each function in the reg_defaults.v files.</p>
16	ME	R/W	0h	<p>Set by the configuration program to enable the MSI feature. This field can also be written from the local management bus.</p>
15-8	CP1	R	B0h	<p>Pointer to the next PCI Capability Structure. This can be modified from the local management bus.</p> <p>This field can be written from the local management bus.</p>
7-0	CID1	R	5h	<p>Specifies that the capability structure is for MSI. Hardwired to 05 hex.</p>

9.5.20 PCIE_CORE_RP_I_MSI_MSG_LOW_ADDR Register (Offset = 94h) [reset = 0h]

PCIE_CORE_RP_I_MSI_MSG_LOW_ADDR is shown in [Figure 9-409](#) and described in [Table 9-1222](#).

Return to [Summary Table](#).

N/A

Table 9-1221.
PCIE_CORE_RP_I_MSI_MSG_LOW_ADDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0094h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0094h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0094h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0094h

Figure 9-409. PCIE_CORE_RP_I_MSI_MSG_LOW_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAL																R1															
R/W-0h																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1222. PCIE_CORE_RP_I_MSI_MSG_LOW_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	MAL	R/W	0h	Lower bits of the address to be used in MSI messages. This field can also be written from the local management bus.
1-0	R1	R	0h	The two lower bits of the address are hardwired to 0 to align the address on a double-word boundary.

9.5.21 PCIE_CORE_RP_I_MSI_MSG_HI_ADDR Register (Offset = 98h) [reset = 0h]

PCIE_CORE_RP_I_MSI_MSG_HI_ADDR is shown in [Figure 9-410](#) and described in [Table 9-1224](#).

Return to [Summary Table](#).

N/A

Table 9-1223.
PCIE_CORE_RP_I_MSI_MSG_HI_ADDR Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0098h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0098h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0098h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0098h

Figure 9-410. PCIE_CORE_RP_I_MSI_MSG_HI_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1224. PCIE_CORE_RP_I_MSI_MSG_HI_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAH	R/W	0h	Contains bits 63:32 of the 64-bit address to be used in MSI Messages. A value of 0 specifies that 32-bit addresses are to be used in the messages. This field can also be written from the local management bus.

9.5.22 PCIE_CORE_RP_I_MSI_MSG_DATA Register (Offset = 9Ch) [reset = 0h]

PCIE_CORE_RP_I_MSI_MSG_DATA is shown in [Figure 9-411](#) and described in [Table 9-1226](#).

Return to [Summary Table](#).

N/A

Table 9-1225. PCIE_CORE_RP_I_MSI_MSG_DATA Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 009Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 009Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 009Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 009Ch

Figure 9-411. PCIE_CORE_RP_I_MSI_MSG_DATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R2																MD															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1226. PCIE_CORE_RP_I_MSI_MSG_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R2	R	0h	Hardwired to 0
15-0	MD	R/W	0h	Message data to be used for this Function. This field can also be written from the local management bus.

9.5.23 PCIE_CORE_RP_I_MSI_MASK Register (Offset = A0h) [reset = X]

PCIE_CORE_RP_I_MSI_MASK is shown in [Figure 9-412](#) and described in [Table 9-1228](#).

Return to [Summary Table](#).

N/A

Table 9-1227. PCIE_CORE_RP_I_MSI_MASK Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00A0h

Figure 9-412. PCIE_CORE_RP_I_MSI_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MM
R/W-X															R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1228. PCIE_CORE_RP_I_MSI_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	MM	R/W	0h	Mask bits for MSI interrupts. The Multiple Message Capable field of the MSI Control Register specifies the number of distinct interrupts for the Function, which determines the number of valid mask bits.

9.5.24 PCIE_CORE_RP_I_MSI_PENDING_BITS Register (Offset = A4h) [reset = X]

PCIE_CORE_RP_I_MSI_PENDING_BITS is shown in [Figure 9-413](#) and described in [Table 9-1230](#).

Return to [Summary Table](#).

N/A

Table 9-1229.
PCIE_CORE_RP_I_MSI_PENDING_BITS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00A4h

Figure 9-413. PCIE_CORE_RP_I_MSI_PENDING_BITS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															MP
R-X															R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-1230. PCIE_CORE_RP_I_MSI_PENDING_BITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	MP	R	0h	Pending bits for MSI interrupts. This field can be written from the APB interface to reflect the current pending status.

9.5.25 PCIE_CORE_RP_I_MSIX_CTRL Register (Offset = B0h) [reset = C011h]

PCIE_CORE_RP_I_MSIX_CTRL is shown in [Figure 9-414](#) and described in [Table 9-1232](#).

Return to [Summary Table](#).

N/A

Table 9-1231. PCIE_CORE_RP_I_MSIX_CTRL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00B0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00B0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00B0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00B0h

Figure 9-414. PCIE_CORE_RP_I_MSIX_CTRL Register

31	30	29	28	27	26	25	24
MSIXE	FM	R0			MSIXTS		
R/W-0h	R/W-0h	R-0h			R-0h		
23	22	21	20	19	18	17	16
MSIXTS							
R-0h							
15	14	13	12	11	10	9	8
CP							
R-C0h							
7	6	5	4	3	2	1	0
CID							
R-11h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1232. PCIE_CORE_RP_I_MSIX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MSIXE	R/W	0h	Set by the configuration program to enable the MSI-X feature. This field can also be written from the local management bus.
30	FM	R/W	0h	This bit serves as a global mask to all the interrupt conditions associated with this Function. When this bit is set, the Controller will not send out MSI-X messages from this Function. This field can also be written from the local management bus.
29-27	R0	R	0h	Reserved

Table 9-1232. PCIE_CORE_RP_I_MSIX_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-16	MSIXTS	R	0h	Specifies the size of the MSI-X Table, that is, the number of interrupt vectors defined for the Function. The programmed value is 1 minus the size of the table [that is, this field is set to 0 if the table size is 1]. It can be re-written independently for each Function from the local management bus. Please see the define den_db_Fx_MSIX_TABLE_SIZE values [where x is the function number] for default values of each function in the reg_defaults.v files.
15-8	CP	R	C0h	Contains pointer to the next PCI Capability Structure. This is set to point to the PCI Express Capability Structure at 30 hex. This can be rewritten independently for each Function from the local management bus.
7-0	CID	R	11h	Identifies that the capability structure is for MSI-X. This field is set by default to 11 hex. It can be rewritten independently for each Function from the local management bus.

9.5.26 PCIE_CORE_RP_I_MSIX_TBL_OFFSET Register (Offset = B4h) [reset = 0h]

PCIE_CORE_RP_I_MSIX_TBL_OFFSET is shown in [Figure 9-415](#) and described in [Table 9-1234](#).

Return to [Summary Table](#).

N/A

Table 9-1233.
PCIE_CORE_RP_I_MSIX_TBL_OFFSET Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00B4h

Figure 9-415. PCIE_CORE_RP_I_MSIX_TBL_OFFSET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO												BARI			
R-0h												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-1234. PCIE_CORE_RP_I_MSIX_TBL_OFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	TO	R	0h	Offset of the memory address where the MSI-X Table is located, relative to the selected BAR. The three least significant bits of the address are omitted, as the addresses are QWORD aligned. Please see the define den_db_Fx_MSIX_TABLE_OFFSET values [where x is the function number] for default values of each function in the reg_defaults.v files.
2-0	BARI	R	0h	Identifies the BAR corresponding to the memory address range where the MSI-X Table is located [000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5]. Please see the define den_db_Fx_MSIX_TABLE_BIR values [where x is the function number] for default values of each function in the reg_defaults.v files.

9.5.27 PCIE_CORE_RP_I_MSIX_PENDING_INTRPT Register (Offset = B8h) [reset = 8h]

PCIE_CORE_RP_I_MSIX_PENDING_INTRPT is shown in [Figure 9-416](#) and described in [Table 9-1236](#).

Return to [Summary Table](#).

N/A

Table 9-1235.
PCIE_CORE_RP_I_MSIX_PENDING_INTRPT
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00B8h

Figure 9-416. PCIE_CORE_RP_I_MSIX_PENDING_INTRPT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBAO															
R-1h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBAO												BARI1			
R-1h												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-1236. PCIE_CORE_RP_I_MSIX_PENDING_INTRPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	PBAO	R	1h	Offset of the memory address where the PBA is located, relative to the selected BAR. The three least significant bits of the address are omitted, as the addresses are QWORD aligned. Please see the define den_db_Fx_MSIX_PBA_OFFSET values [where x is the function number] for default values of each function in the reg_defaults.v files.

Table 9-1236. PCIE_CORE_RP_I_MSIX_PENDING_INTRPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	BAR11	R	0h	<p>Identifies the BAR corresponding to the memory address range where the PBA Structure is located</p> <p>[000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5].</p> <p>The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register.</p> <p>Identifies the BAR corresponding to the memory address range where the PBA Structure is located</p> <p>[000 = BAR 0, 001 = BAR 1, ... , 101 = BAR 5].</p> <p>The value programmed must be the same as the BAR Indicator configured in the MSI-X Table Offset Register.</p> <p>Please see the define den_db_Fx_MSIX_PBA_BIR values [where x is the function number] for default values of each function in the reg_defaults.v files.</p>

9.5.28 PCIE_CORE_RP_I_PCIE_CAP_LIST Register (Offset = C0h) [reset = 01420010h]

PCIE_CORE_RP_I_PCIE_CAP_LIST is shown in [Figure 9-417](#) and described in [Table 9-1238](#).

Return to [Summary Table](#).

N/A

**Table 9-1237. PCIE_CORE_RP_I_PCIE_CAP_LIST
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00C0h

Figure 9-417. PCIE_CORE_RP_I_PCIE_CAP_LIST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0	TRS	IMN				SI		DT				PCV			
R-0h	R-0h	R-0h				R-1h		R-4h				R-2h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCP								CID							
R-0h								R-10h							

LEGEND: R = Read Only; -n = value after reset

Table 9-1238. PCIE_CORE_RP_I_PCIE_CAP_LIST Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R0	R	0h	Reserved
30	TRS	R	0h	When set to 1, this bit indicates that the device supports routing of Trusted Configuration Requests. Not valid for Endpoints. Hardwired to 0.
29-25	IMN	R	0h	Identifies the MSI or MSI-X interrupt vector for the interrupt message generated corresponding to the status bits in the Slot Status Register, Root Status Register, or this capability structure. This field must be defined based on the chosen interrupt mode - MSI or MSI-X. This field is hardwired to 0.
24	SI	R	1h	When Set, this bit indicates that the Link associated with this Port is connected to a slot
23-20	DT	R	4h	Indicates the type of device implementing this Function. This field is hardwired to 4 in the RP mode.
19-16	PCV	R	2h	Identifies the version number of the capability structure. This field is set to 2 by default to indicate that the Controller is compatible to PCI Express Base Specification Revision 3.0. Can be modified using local management interface after asserting input signal MGMT_TYPE1_CONFIG_REG_ACCESS high.

Table 9-1238. PCIE_CORE_RP_I_PCIE_CAP_LIST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	NCP	R	0h	Points to the next PCI capability structure. Set to 0 because this is the last capability structure.
7-0	CID	R	10h	Specifies Capability ID assigned by PCI SIG for this structure. This field is hardwired to 10 hex.

9.5.29 PCIE_CORE_RP_I_PCIE_CAP Register (Offset = C4h) [reset = 8001h]

PCIE_CORE_RP_I_PCIE_CAP is shown in [Figure 9-418](#) and described in [Table 9-1240](#).

Return to [Summary Table](#).

N/A

**Table 9-1239. PCIE_CORE_RP_I_PCIE_CAP
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00C4h

Figure 9-418. PCIE_CORE_RP_I_PCIE_CAP Register

31	30	29	28	27	26	25	24
R5			FLRC	CPLS		CSP	
R-0h			R-0h	R-0h		R-0h	
23	22	21	20	19	18	17	16
CSP						R4	
R-0h						R-0h	
15	14	13	12	11	10	9	8
RER	R3			AL1L			AL0L
R-1h	R-0h			R-0h			R-0h
7	6	5	4	3	2	1	0
AL0L		ETFS	PFS		MP		
R-0h		R-0h	R-0h		R-1h		

LEGEND: R = Read Only; -n = value after reset

Table 9-1240. PCIE_CORE_RP_I_PCIE_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	R5	R	0h	Reserved
28	FLRC	R	0h	A value of 1b indicates the Function supports the optional Function Level Reset mechanism
27-26	CPLS	R	0h	Specifies the scale used by Slot Power Limit Value. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
25-18	CSP	R	0h	Specifies upper limit on power supplied by slot. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
17-16	R4	R	0h	Reserved
15	RER	R	1h	Enables role-based error reporting. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 9-1240. PCIE_CORE_RP_I_PCIE_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	R3	R	0h	Reserved
11-9	AL1L	R	0h	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L1 to PCIE_CORE_RP_L0. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
8-6	AL0L	R	0h	Specifies acceptable latency that the Endpoint can tolerate while transitioning from L0S to PCIE_CORE_RP_L0. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
5	ETFS	R	0h	hard coded to zero .
4-3	PFS	R	0h	This field is used to extend the tag field by combining unused Function bits with the tag bits. This field is hardwired to 00 to disable this feature.
2-0	MP	R	1h	Specifies maximum payload size supported by the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

9.5.30 PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS Register (Offset = C8h) [reset = 2810h]

PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS is shown in [Figure 9-419](#) and described in [Table 9-1242](#).

Return to [Summary Table](#).

N/A

Table 9-1241.
PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00C8h

Figure 9-419. PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS Register

31	30	29	28	27	26	25	24
R8							
R-0h							
23	22	21	20	19	18	17	16
R8	TP	APD	URD	FED	NFED	CED	
R-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	
15	14	13	12	11	10	9	8
R7	MRR	ENS	APPME	PFE	ETE		
R-0h	R/W-2h	R/W-1h	R-0h	R-0h	R-0h		
7	6	5	4	3	2	1	0
MP	ERO	EURR	EFER	ENFER	ECER		
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1242. PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R8	R	0h	N/A
21	TP	R	0h	Indicates if any of the Non-Posted requests issued by the RC are still pending.
20	APD	R	0h	Set when auxiliary power is detected by the device. This is an unused field.
19	URD	R/W1C	0h	Set to 1 by the Controller when it receives an unsupported request.
18	FED	R/W1C	0h	Set to 1 by the Controller when it detects a fatal error, regardless of whether the error is masked.
17	NFED	R/W1C	0h	Set to 1 by the Controller when it detects a non-fatal error, regardless of whether the error is masked.
16	CED	R/W1C	0h	Set to 1 by the Controller when it detects a correctable error, regardless of whether the error is masked.
15	R7	R	0h	Hardwired to 0.

Table 9-1242. PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	MRR	R/W	2h	Specifies the maximum size allowed in read requests generated by the device.
11	ENS	R/W	1h	If this bit is Set, the Function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency.
10	APPME	R	0h	Hardwired to 0
9	PFE	R	0h	Hardwired to 0
8	ETE	R	0h	extended tag not enabled. Hence hard coded to zero .
7-5	MP	R/W	0h	Specifies the maximum TLP payload size configured. The device must be able to receive a TLP of this maximum size, and should not generate TLP's larger than this value. Software must set this field based on the maximum payload size in the Device Capabilities Register, and the capability of the other side.
4	ERO	R/W	1h	When set, this bit indicates that the device is allowed to set the Relaxed Ordering bit in the Attributes field of transactions initiated from it., when the transactions do not require Strong Ordering.
3	EURR	R/W	0h	This bit is used to gate the CORRECTABLE_ERROR_OUT, NON_FATAL_ERROR_OUT, FATAL_ERROR_OUT output in Root Port mode on receiving unsupported requests. Note: Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of FATAL_ERROR_OUT on receiving uncorrectable unsupported requests.
2	EFER	R/W	0h	This bit is used to gate the FATAL_ERROR_OUT output of the Controller in Root Port mode. When an Uncorrectable, Unmasked Error with Uncorrectable Error Severity set to 1 is detected Internally or when a ERR_FATAL message is received by the Controller, in Root Port mode, this bit gates the assertion of FATAL_ERROR_OUT output. Note: Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of FATAL_ERROR_OUT.
1	ENFER	R/W	0h	This bit is used to gate the NON_FATAL_ERROR_OUT output of the Controller in Root Port mode. When an Uncorrectable, Unmasked Error with Uncorrectable Error Severity set to 0 is detected Internally or when a ERR_NON_FATAL message is received by the Controller, in Root Port mode, this bit gates the assertion of NON_FATAL_ERROR_OUT output. Note: Alternately, the SERR Enable bit in the Command Register can also be set to enable assertion of NON_FATAL_ERROR_OUT.

Table 9-1242. PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECER	R/W	0h	<p>This bit is used to gate the CORRECTABLE_ERROR_OUT output of the Controller in Root Port mode.</p> <p>When a Correctable and Unmasked Error is detected Internally or when a ERR_CORR message is received by the Controller, in Root Port mode, this bit gates the assertion of CORRECTABLE_ERROR_OUT output.</p>

9.5.31 PCIE_CORE_RP_I_LINK_CAP Register (Offset = CCh) [reset = 0061AC24h]

PCIE_CORE_RP_I_LINK_CAP is shown in [Figure 9-420](#) and described in [Table 9-1244](#).

Return to [Summary Table](#).

N/A

Table 9-1243. PCIE_CORE_RP_I_LINK_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00CCh

Figure 9-420. PCIE_CORE_RP_I_LINK_CAP Register

31	30	29	28	27	26	25	24
PN							
R-0h							
23	22	21	20	19	18	17	16
R9	ASPMOC	LBNC	DARC	SERC	CPM	L1EL	
R-0h	R-1h	R-1h	R-0h	R-0h	R-0h	R-3h	
15	14	13	12	11	10	9	8
L1EL	L0EL		ASPM			MLW	
R-3h	R-2h		R-3h			R-2h	
7	6	5	4	3	2	1	0
MLW				MLS			
R-2h				R-4h			

LEGEND: R = Read Only; -n = value after reset

Table 9-1244. PCIE_CORE_RP_I_LINK_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PN	R	0h	Specifies the port number assigned to the PCI Express link connected to this device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
23	R9	R	0h	Reserved
22	ASPMOC	R	1h	A 1 in this position indicates the device supports the ASPM Optionality feature. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
21	LBNC	R	1h	A value of 1b indicates support for the Link Bandwidth Notification status and interrupt mechanisms. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 9-1244. PCIE_CORE_RP_I_LINK_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DARC	R	0h	Set to 1 if the device is capable of reporting that the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0, as this version of the Controller does not support the feature.
19	SERC	R	0h	Indicates the capability of the device to report a Surprise Down error condition. This bit is hardwired to 0, as this version of the Controller does not support the feature.
18	CPM	R	0h	Indicates that the device supports removal of reference clocks. Not supported in this version of the Controller. Hardwired to 0.
17-15	L1EL	R	3h	Specifies the exit latency from L1 state. This parameter is dependent on the Physical Layer implementation. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
14-12	L0EL	R	2h	Specifies the time required for the device to transition from L0S to PCIE_CORE_RP_L0. This parameter is dependent on the Physical Layer implementation. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
11-10	ASPM	R	3h	Indicates the level of ASPM support provided by the device. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
9-4	MLW	R	2h	Indicates the maximum number of lanes supported by the device. This field is hardwired based on the setting of the LANE_COUNT_IN strap input.
3-0	MLS	R	4h	Indicates the speeds supported by the link [2.5 GT/s , 5 GT/s , 8 GT/s , 16 GT/s per lane]. This field is hardwired to 0001 [2.5GT/s] when the strap input PCIE_GENERATION_SEL is set to 0, to 0010 [5 GT/s] when the strap is set to 1 , and to 0011 [8 GT/s] when the strap input is set to 10 , and to 0100 [16 GT/s] when the strap input is set to 11 .

9.5.32 PCIE_CORE_RP_I_LINK_CTRL_STATUS Register (Offset = D0h) [reset = 00210000h]

PCIE_CORE_RP_I_LINK_CTRL_STATUS is shown in [Figure 9-421](#) and described in [Table 9-1246](#).

Return to [Summary Table](#).

N/A

Table 9-1245.
PCIE_CORE_RP_I_LINK_CTRL_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00D0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00D0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00D0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00D0h

Figure 9-421. PCIE_CORE_RP_I_LINK_CTRL_STATUS Register

31	30	29	28	27	26	25	24
LABS	LBMS	DA	SCC	LTS	R12	NLW	
R/W1C-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h	R-2h	
23	22	21	20	19	18	17	16
NLW				NLS			
R-2h				R-1h			
15	14	13	12	11	10	9	8
R11				LABIE	LBMIE	HAWD	ECPM
R-0h				R/W-0h	R/W-0h	R/W-0h	R-0h
7	6	5	4	3	2	1	0
ES	CCC	RL	LD	RCB	R10	ASPMC	
R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1246. PCIE_CORE_RP_I_LINK_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LABS	R/W1C	0h	This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0.
30	LBMS	R/W1C	0h	This bit is Set by hardware to indicate that either link training has completed following write to retrain link bit, or when HW has changed link speed or width to attempt to correct unreliable link operation. This triggers an interrupt to be generated through PHY_INTERRUPT_OUT if enabled. Hardwired to 0 if Link Bandwidth Notification Capability is 0.
29	DA	R	0h	Indicates the status of the Data Link Layer. Set to 1 when the DL Control and Management State Machine has reached the DL_Active state. This bit is hardwired to 0 in this version of the Controller.

Table 9-1246. PCIE_CORE_RP_I_LINK_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	SCC	R	0h	Indicates that the device uses the reference clock provided by the connector. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
27	LTS	R	0h	This bit is set to 1 when the LTSSM is in the Recovery or Configuration states, or if a 1 has been written to the Retrain Link bit but the link training has not yet begun.
26	R12	R	0h	Reserved
25-20	NLW	R	2h	Set at the end of link training to the actual link width negotiated between the two sides.
19-16	NLS	R	1h	Negotiated link speed of the device. The only supported speed ids are 2.5 GT/s per lane [0001], 5 GT/s per lane [0010], 8 GT/s per lane [0011], 16 GT/s per lane [0100].
15-12	R11	R	0h	Reserved
11	LABIE	R/W	0h	When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0.
10	LBMIE	R/W	0h	When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This enables an interrupt to be generated through PHY_INTERRUPT_OUT if triggered. Hardwired to 0 if Link Bandwidth Notification Capability is 0.
9	HAWD	R/W	0h	When this bit is set, the local application must not request to change the operating width of the link, other than attempting to correct unreliable Link operation by reducing Link width.
8	ECPM	R	0h	This field is hardwired to 0 when the Controller is in the RC mode.
7	ES	R/W	0h	Set to 1 to extend the sequence of ordered sets transmitted while exiting from the LOS state.
6	CCC	R/W	0h	A value of 0 indicates that the reference clock of this device is asynchronous to that of the upstream device. A value of 1 indicates that the reference clock is common.

Table 9-1246. PCIE_CORE_RP_I_LINK_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RL	R	0h	Setting this bit to 1 causes the LTSSM to initiate link training. This bit always reads as 0. This bit can be set by Host SW at any time independent of the LTSSM state. If the LTSSM is not in PCIE_CORE_RP_L0 state, the Controller will internally register the retrain command and initiate the link retrain immediately after the LTSSM reaches PCIE_CORE_RP_L0. For example, if the LTSSM is already in Recovery, the Controller will initiate Retrain Link after the LTSSM transitions back to PCIE_CORE_RP_L0 state.
4	LD	R/W	0h	Writing a 1 to this bit position causes the LTSSM to go to the Disable Link state. The LTSSM stays in the Disable Link state while this bit is set.
3	RCB	R	0h	Indicates the Read Completion Boundary of the Root Port [0 = 64 bytes, 1 = 128 bytes]. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
2	R10	R	0h	Reserved
1-0	ASPMC	R/W	0h	Controls the level of ASPM support on the PCI Express link associated with the function. The valid setting are 00: ASPM disabled 01: L0s entry enabled, L1 disabled 10: L1 entry enabled, L0s disabled 11: Both L0s and L1 enabled. Note that the ASPM Control bits can be enabled only if the corresponding ASPM Support [1:0] bit is 1 in the Link Capabilities Register.

9.5.33 PCIE_CORE_RP_I_SLOT_CAPABILITY Register (Offset = D4h) [reset = 0h]

PCIE_CORE_RP_I_SLOT_CAPABILITY is shown in [Figure 9-422](#) and described in [Table 9-1248](#).

Return to [Summary Table](#).

N/A

**Table 9-1247. PCIE_CORE_RP_I_SLOT_CAPABILITY
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00D4h

Figure 9-422. PCIE_CORE_RP_I_SLOT_CAPABILITY Register

31	30	29	28	27	26	25	24
PSN							
R-0h							
23	22	21	20	19	18	17	16
PSN				NCCS		EIP	SPLS
R-0h				R-0h		R-0h	R-0h
15	14	13	12	11	10	9	8
SPLS	SPLV						
R-0h	R-0h						
7	6	5	4	3	2	1	0
SPLV	HPC	HPS	PIP	AIP	MRLSP	PCP	ABPRSNT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-1248. PCIE_CORE_RP_I_SLOT_CAPABILITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	PSN	R	0h	This field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to zero for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port.
18	NCCS	R	0h	When Set, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be Set if the hot-plug capable Port is able to accept writes to all fields of the Slot Control register without delay between successive writes.
17	EIP	R	0h	When Set, this bit indicates that an Electromechanical Interlock is implemented on the chassis for this slot.

Table 9-1248. PCIE_CORE_RP_I_SLOT_CAPABILITY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-15	SPLS	R	0h	Specifies the scale used for the Slot Power Limit Value . Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x This register must be implemented if the Slot Implemented bit is Set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 00b.
14-7	SPLV	R	0h	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot [see Section 6.9] or by other means to the adapter. Power limit [in Watts] is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b [1.0x] and Slot Power Limit Value exceeds EFh, the following alternative encodings are used: F0h = 250 W Slot Power Limit F1h = 275 W Slot Power Limit F2h = 300 W Slot Power Limit F3h to FFh = Reserved for Slot Power Limit values above 300 W This register must be implemented if the Slot Implemented bit is Set. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 0000 0000b.
6	HPC	R	0h	When Set, this bit indicates that this slot is capable of supporting hot-plug operations.
5	HPS	R	0h	When Set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation.
4	PIP	R	0h	When Set, this bit indicates that a Power Indicator is electrically controlled by the chassis for this slot.
3	AIP	R	0h	When Set, this bit indicates that an Attention Indicator is electrically controlled by the chassis.
2	MRLSP	R	0h	When Set, this bit indicates that an MRL Sensor is implemented on the chassis for this slot.
1	PCP	R	0h	When Set, this bit indicates that a software programmable Power Controller is implemented for this slot/adapter [depending on form factor].
0	ABPRSNT	R	0h	When Set, this bit indicates that an Attention Button for this slot is electrically controlled by the chassis.

9.5.34 PCIE_CORE_RP_I_SLOT_CTRL_STATUS Register (Offset = D8h) [reset = 002007C0h]

PCIE_CORE_RP_I_SLOT_CTRL_STATUS is shown in [Figure 9-423](#) and described in [Table 9-1250](#).

Return to [Summary Table](#).

N/A

Table 9-1249.
PCIE_CORE_RP_I_SLOT_CTRL_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00D8h

Figure 9-423. PCIE_CORE_RP_I_SLOT_CTRL_STATUS Register

31	30	29	28	27	26	25	24
RSCS2							DLLSC
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
EMIS	PDS	MRLSS	CMDCMPL	PDC	MRLSC	PFD	ABPRSD
R-0h	R-0h	R-1h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RSCS1			DLLSCE	EMIC	PCC	PIC	
R-0h			R/W-0h	R-0h	R/W-1h	R/W-3h	
7	6	5	4	3	2	1	0
AIC		HPIE	CCIE	PDCE	MSCE	PFDE	ABPE
R/W-3h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1250. PCIE_CORE_RP_I_SLOT_CTRL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RSCS2	R	0h	N/A
24	DLLSC	R/W1C	0h	This bit is Set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active bit of the Link Status register to determine if the Link is active before initiating configuration cycles to the hot plugged device.
23	EMIS	R	0h	If an Electromechanical Interlock is implemented, this bit indicates the status of the Electromechanical Interlock. Defined encodings are: 0b Electromechanical Interlock Disengaged 1b Electromechanical Interlock Engaged

Table 9-1250. PCIE_CORE_RP_I_SLOT_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	PDS	R	0h	<p>This bit indicates the presence of an adapter in the slot, reflected by the logical 'OR' of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor.</p> <p>Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected.</p> <p>Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism.</p> <p>Defined encodings are:</p> <p>0b Slot Empty</p> <p>1b Card Present in slot.</p>
21	MRLSS	R	1h	<p>This bit reports the status of the MRL sensor if implemented.</p> <p>Defined encodings are:</p> <p>0b MRL Closed</p> <p>1b MRL Open</p>
20	CMDCMPL	R/W1C	0h	<p>If Command Completed notification is supported [if the No Command Completed Support bit in the Slot Capabilities register is 0b], this bit is Set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command.</p> <p>The Command Completed status bit is Set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command</p> <p>it provides no guarantee that the action corresponding to the command is complete.</p> <p>If Command Completed notification is not supported, this bit must be hardwired to 0b.</p>
19	PDC	R/W1C	0h	<p>This bit is set when the value reported in the Presence Detect State bit is changed.</p>
18	MRLSC	R/W1C	0h	<p>If an MRL sensor is implemented, this bit is Set when a MRL Sensor state change is detected.</p> <p>If an MRL sensor is not implemented, this bit must not be Set.</p>
17	PFD	R/W1C	0h	<p>If a Power Controller that supports power fault detection is implemented, this bit is Set when the Power Controller detects a power fault at this slot.</p> <p>Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot.</p> <p>If power fault detection is not supported, this bit must not be Set.</p>
16	ABPRSD	R/W1C	0h	<p>If an Attention Button is implemented, this bit is Set when the attention button is pressed.</p> <p>If an Attention Button is not supported, this bit must not be Set.</p>
15-13	RSCS1	R	0h	Reserved

Table 9-1250. PCIE_CORE_RP_I_SLOT_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	DLLSCE	R/W	0h	If the Data Link Layer Link Active Reporting capability is 1b, this bit enables software notification when Data Link Layer Link Active bit is changed. If the Data Link Layer Link Active Reporting Capable bit is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.
11	EMIC	R	0h	If an Electromechanical Interlock is implemented, a write of 1b to this bit causes the state of the interlock to toggle. A write of 0b to this bit has no effect. A read of this bit always returns a 0b.
10	PCC	R/W	1h	If a Power Controller is implemented, this bit when written sets the power state of the slot per the defined encodings. Reads of this bit must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write, if required to, without waiting for the previous command to complete in which case the read value is undefined. The defined encodings are: 0b Power On 1b Power Off
9-8	PIC	R/W	3h	If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, Defined encodings are: 00b Reserved 01b On 10b Blink 11b Off
7-6	AIC	R/W	3h	If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, Defined encodings are: 00b Reserved 01b On 10b Blink 11b Off
5	HPIE	R/W	0h	When Set, this bit enables generation of an interrupt on enabled hot-plug events. If the Hot Plug Capable bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.

Table 9-1250. PCIE_CORE_RP_I_SLOT_CTRL_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CCIE	R/W	0h	If Command Completed notification is supported [if the No Command Completed Support bit in the Slot Capabilities register is 0b], when Set, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, this bit must be hardwired to 0b. Default value of this bit is 0b.
3	PDCE	R/W	0h	When Set, this bit enables software notification on a presence detect changed event. If the Hot-Plug Capable bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.
2	MSCE	R/W	0h	When Set, this bit enables software notification on a MRL sensor changed event If the MRL Sensor Present bit in the Slot Capabilities register is Clear, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.
1	PFDE	R/W	0h	When Set, this bit enables software notification on a power fault event If a Power Controller that supports power fault detection is not implemented, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.
0	ABPE	R/W	0h	When Set to 1b, this bit enables software notification on an attention button pressed event. If the Attention Button Present bit in the Slot Capabilities register is 0b, this bit is permitted to be read-only with a value of 0b. Default value of this bit is 0b.

9.5.35 PCIe_CORE_RP_I_ROOT_CTRL_CAP Register (Offset = DCh) [reset = 0h]

PCIe_CORE_RP_I_ROOT_CTRL_CAP is shown in [Figure 9-424](#) and described in [Table 9-1252](#).

Return to [Summary Table](#).

N/A

Table 9-1251. PCIe_CORE_RP_I_ROOT_CTRL_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00DCh

Figure 9-424. PCIe_CORE_RP_I_ROOT_CTRL_CAP Register

31	30	29	28	27	26	25	24
R27							
R-0h							
23	22	21	20	19	18	17	16
R27							
R-0h							
15	14	13	12	11	10	9	8
R27							
R-0h							
7	6	5	4	3	2	1	0
R27			CRSSVE	PMEIE	SEFEE	SENFEE	SECEE
R-0h			R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1252. PCIe_CORE_RP_I_ROOT_CTRL_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	R27	R	0h	Reserved
4	CRSSVE	R	0h	This capability is not implemented and this bit is hardwired to 0b.
3	PMEIE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
2	SEFEE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
1	SENFEE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.
0	SECEE	R/W	0h	This field can be read and written from the local management APB bus, but its value is not used within the Controller.

9.5.36 PCIE_CORE_RP_I_ROOT_STATUS Register (Offset = E0h) [reset = 0h]

PCIE_CORE_RP_I_ROOT_STATUS is shown in [Figure 9-425](#) and described in [Table 9-1254](#).

Return to [Summary Table](#).

N/A

Table 9-1253. PCIE_CORE_RP_I_ROOT_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00E0h

Figure 9-425. PCIE_CORE_RP_I_ROOT_STATUS Register

31	30	29	28	27	26	25	24
R18							
R-0h							
23	22	21	20	19	18	17	16
R18						PMEP	PMES
R-0h						R-0h	R/W1C-0h
15	14	13	12	11	10	9	8
PMERID							
R-0h							
7	6	5	4	3	2	1	0
PMERID							
R-0h							

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1254. PCIE_CORE_RP_I_ROOT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	R18	R	0h	Reserved
17	PMEP	R	0h	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
16	PMES	R/W1C	0h	This field is not set by the Controller but can be cleared by writing a 1 from the local management APB bus. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
15-0	PMERID	R	0h	This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

9.5.37 PCIE_CORE_RP_I_PCIE_CAP_2 Register (Offset = E4h) [reset = X]

PCIE_CORE_RP_I_PCIE_CAP_2 is shown in [Figure 9-426](#) and described in [Table 9-1256](#).

Return to [Summary Table](#).

N/A

**Table 9-1255. PCIE_CORE_RP_I_PCIE_CAP_2
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00E4h

Figure 9-426. PCIE_CORE_RP_I_PCIE_CAP_2 Register

31	30	29	28	27	26	25	24
R16							
R-0h							
23	22	21	20	19	18	17	16
MEEP		EEPS	EXFS		OBFF	T10RS	T10CS
R-1h		R-1h	R-1h		R-0h	R-0h	R-1h
15	14	13	12	11	10	9	8
R15		RESERVED	TPHC	LMS	R14	ACS128	ACS64
R-0h		R-X	R-0h	R-1h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
ACS32	AOPRS	AFS	CTDS				
R-0h	R-0h	R-1h	R-1h				R-2h

LEGEND: R = Read Only; -n = value after reset

Table 9-1256. PCIE_CORE_RP_I_PCIE_CAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R16	R	0h	Reserved
23-22	MEEP	R	1h	Indicates the maximum number of End-End TLP Prefixes supported by the Function. The supported values are: 01b 1 End-End TLP Prefix 10b 2 End-End TLP Prefixes. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write
21	EEPS	R	1h	Indicates whether the Function supports End-End TLP Prefixes. A 1 in this field indicates that the Function supports receiving TLPs containing End-End TLP Prefixes. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write
20	EXFS	R	1h	Indicates that the Function supports the 3-bit definition of the Fmt field in the TLP header. This bit is hardwired to 1 for all Physical Functions.
19-18	OBFF	R	0h	Hard coded to zero

Table 9-1256. PCIE_CORE_RP_I_PCIE_CAP_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	T10RS	R	0h	If set function supports 1-bit requester capability otherwise, the function does not. This bit can be disabled using local management register.
16	T10CS	R	1h	If set function supports 1-bit completer capability otherwise, the function does not. This field can be modified using local management interface.
15-14	R15	R	0h	Reserved
13	RESERVED	R	X	
12	TPHC	R	0h	Hardwired to 0.
11	LMS	R	1h	A value of 1b indicates support for the optional Latency Tolerance Reporting [LTR] mechanism. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
10	R14	R	0h	Reserved
9	ACS128	R	0h	Hardwired to 0.
8	ACS64	R	0h	Hardwired to 0.
7	ACS32	R	0h	Hardwired to 0.
6	AOPRS	R	0h	Applicable only to Switch Upstream Ports, Switch Downstream Ports, and Root Ports must be 0b for other Function types. This bit must be set to 1b if the Port supports this optional capability. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
5	AFS	R	1h	A 1 in this bit indicates that the device is able to forward TLPs with function number greater than 8. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.
4	CTDS	R	1h	A 1 in this field indicates that the associated Function supports the capability to turn off its Completion timeout. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

Table 9-1256. PCIE_CORE_RP_I_PCIE_CAP_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CTR	R	2h	<p>Specifies the Completion Timeout values supported by the device. This field is set by default to 0010 [10 ms - 250 ms], but can be modified from the local management APB bus.</p> <p>The actual timeout values are in two programmable local management registers, which allow the timeout settings of the two sub-ranges within Range B to be programmed independently.</p> <p>This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.</p>

9.5.38 PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS_2 Register (Offset = E8h) [reset = 0h]

PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS_2 is shown in [Figure 9-427](#) and described in [Table 9-1258](#).

Return to [Summary Table](#).

N/A

Table 9-1257.
PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00E8h

Figure 9-427. PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS_2 Register

31	30	29	28	27	26	25	24
R20							
R-0h							
23	22	21	20	19	18	17	16
R20							
R-0h							
15	14	13	12	11	10	9	8
R20	OBFFE		T10RE	R19	LTRME	ICE	IRE
R-0h	R-0h		R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
R18	AORE	AFE	CTD	CTV			
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1258. PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	R20	R	0h	N/A
14-13	OBFFE	R	0h	Enables the Optimized Buffer Flush/Fill [OBFF] capability in the device. Valid settings are 00 [disabled], 01 [Variation A], and 10 [Variation B].
12	T10RE	R	0h	10bit TAGs generation are not supported in this configuration.
11	R19	R	0h	Reserved
10	LTRME	R/W	0h	This must be set to 1 to enable the Latency Tolerance Reporting Mechanism. This bit is implemented only in PF 0. Its default value is 1, but can be modified from the local management bus. This bit is read-only in PF 1.
9	ICE	R/W	0h	When this bit is 1, the RC is allowed to set the ID-based Ordering [IDO] Attribute bit in the Completions it generates.

Table 9-1258. PCIE_CORE_RP_I_PCIE_DEV_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	IRE	R/W	0h	When this bit is 1, the RC is allowed to set the ID-based Ordering [IDO] Attribute bit in the requests it generates.
7	R18	R	0h	Reserved
6	AORE	R	0h	This bit must be set to enable the generation of Atomic Op Requests. If the client logic attempts to send an Atomic Op when this bit is not set, logic in the Controller will nullify the TLP on its way to the link.
5	AFE	R/W	0h	A 1 in this field indicates that the port treats fields 7:0 of the ID as function number while converting a Type 1 config packet to type 0 config packet.
4	CTD	R/W	0h	Setting this bit disables the Completion Timeout in the device.
3-0	CTV	R/W	0h	Specifies the Completion Timeout value for the device. Allowable values are 0101 [sub-range 1] and 0110 [sub-range 2]. The corresponding timeout values are stored in the local management register's Completion Timeout Interval Registers 0 and 1, respectively. Value of 0 selects completion timeout from Completion-Timeout-Interval-Registers-0 in local management register.

9.5.39 PCIE_CORE_RP_I_LINK_CAP_2 Register (Offset = ECh) [reset = X]

PCIE_CORE_RP_I_LINK_CAP_2 is shown in [Figure 9-428](#) and described in [Table 9-1260](#).

Return to [Summary Table](#).

N/A

Table 9-1259. PCIE_CORE_RP_I_LINK_CAP_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00ECh

Figure 9-428. PCIE_CORE_RP_I_LINK_CAP_2 Register

31	30	29	28	27	26	25	24
R31	R25					TWRTDPS	
R-0h				R-0h			R-1h
23	22	21	20	19	18	17	16
RTPDS	R3			LSORSSV			
R-1h		R-0h			R-0h		
15	14	13	12	11	10	9	8
R2			LSOGSSV				R1
R-0h				R-0h			R-0h
7	6	5	4	3	2	1	0
R1			SLSV				RESERVED
R-0h				R-Fh			R-X

LEGEND: R = Read Only; -n = value after reset

Table 9-1260. PCIE_CORE_RP_I_LINK_CAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R31	R	0h	Indicates support for the optional Device Readiness Status [DRS] capability. This capability is currently not supported in the Controller.
30-25	R25	R	0h	Reserved
24	TWRTDPS	R	1h	When set to 1b, this bit indicates that the associated Port supports detection and reporting of two Retimers presence. This bit is valid for both Downstream Ports and Upstream Ports.
23	RTPDS	R	1h	When set to 1b, this bit indicates that the associated Port supports detection and reporting of Retimer presence. This bit is valid for both Downstream Ports and Upstream Ports.
22-20	R3	R	0h	Reserved
19-16	LSORSSV	R	0h	If this field is non-zero, it indicates that the Port, when operating at the indicated speed[s] supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS.
15-13	R2	R	0h	Reserved

Table 9-1260. PCIE_CORE_RP_I_LINK_CAP_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-9	LSOGSSV	R	0h	If this field is non-zero, it indicates that the Port, when operating at the indicated speed[s] supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate.
8-5	R1	R	0h	Reserved
4-1	SLSV	R	Fh	<p>This field indicates the supported link speeds of the Controller. For each bit, a value of 1 indicates that the corresponding link speed is supported, while a value of 0 indicates that the corresponding speed is not supported.</p> <p>The bits corresponding to various link speeds are:</p> <p>Bit</p> <p>1 = Link Speed 2.5 GT/s, Bit</p> <p>2 = Link Speed 5 GT/s, Bit</p> <p>3 = Link Speed 8 GT/s, Bit</p> <p>4 = Link Speed 16 GT/s.</p> <p>This field is hardwired to 0001 [2.5 GT/s] when the PCIE_GENERATION_SEL strap pins of the Controller are set to 0, 0011 [2.5 and 5 GT/s] when the strap is set to 1, and 0111 [2.5, 5, and 8 GT/s] when the strap pin is set to 10, and 1111 [2.5, 5, 8 and 16 GT/s] when the strap pin is set to 11.</p>
0	RESERVED	R	X	

9.5.40 PCIE_CORE_RP_I_LINK_CTRL_STATUS_2 Register (Offset = F0h) [reset = 00010004h]

PCIE_CORE_RP_I_LINK_CTRL_STATUS_2 is shown in [Figure 9-429](#) and described in [Table 9-1262](#).

Return to [Summary Table](#).

N/A

Table 9-1261.
PCIE_CORE_RP_I_LINK_CTRL_STATUS_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 00F0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 00F0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 00F0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 00F0h

Figure 9-429. PCIE_CORE_RP_I_LINK_CTRL_STATUS_2 Register

31	30	29	28	27	26	25	24
DMR	DCP			R21			
R-0h	R-0h			R-0h			
23	22	21	20	19	18	17	16
TWRTP	RTP	LE	EP3S	EP2S	EP1S	EQC	CDEL
R-0h	R-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h	R-1h
15	14	13	12	11	10	9	8
CD				CS	EMC	TM	
R/W-0h				R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
TM	SD	HASD	EC	TLS			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-4h			

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1262. PCIE_CORE_RP_I_LINK_CTRL_STATUS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DMR	R	0h	DRS is not supported by the Controller and hence this field is not implemented.
30-28	DCP	R	0h	DRS is not supported by the Controller and hence this field is not implemented.
27-24	R21	R	0h	Reserved
23	TWRTP	R	0h	When set to 1b, this bit indicates that two Retimers were present during the most recent Link negotiation.
22	RTP	R	0h	When set to 1b, this bit indicates that a Retimer was present during the most recent Link negotiation.

Table 9-1262. PCIE_CORE_RP_I_LINK_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	LE	R/W1C	0h	This bit can be set by the software running on the EndPoint to force the Endpoint to perform link equalization. Setting this bit causes the LTSSM of the Controller to enter the Recovery state and request its link partner to perform equalization. This bit is cleared when the LTSSM enters the Recovery.Equalization state. It can also be cleared by writing a 1 to this bit position by the host, or writing a 0 from the LMI. STICKY
20	EP3S	R	0h	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully. STICKY
19	EP2S	R	0h	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully. STICKY
18	EP1S	R	0h	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully. STICKY
17	EQC	R	0h	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed. STICKY
16	CDEL	R	1h	This status bit indicates the current operating de-emphasis level of the transmitter [0 = -6dB, 1 = -3.5dB].
15-12	CD	R/W	0h	This bit sets the de-emphasis level [for 5 GT/s operation] or the Transmitter Preset level [for 8 GT/s or 16 GT/s operation] when the LTSSM enters the Polling.Compliance state because of software setting the Enter Compliance bit in this register. It is used only when the link is running at 5 GT/s or 8 GT/s or 16 GT/s. At 5 GT/s, the only valid setting are 0 [-6 dB] and 1 [-3.5 dB]. STICKY
11	CS	R/W	0h	When this bit is set to 1, the device will transmit SKP ordered sets between compliance patterns. STICKY

Table 9-1262. PCIE_CORE_RP_I_LINK_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	EMC	R/W	0h	This field is intended for debug and compliance testing purposes only. If this bit is set to 1, the device will transmit the Modified Compliance Pattern when the LTSSM enters the Polling.Compliance substate. STICKY
9-7	TM	R/W	0h	This field is intended for debug and compliance testing purposes only. It controls the non-deemphasized voltage level at the transmitter outputs. Its encodings are: 000 = Normal operating range, 001 = 800 - 1200 mV for full swing and 400 - 700 mV for half swing, 010 - 111 = See PCI Express Base Specification 2.0. This field is reset to 0 when th LTSSM enters the Polling.Configuration substate during link training. STICKY.
6	SD	R/W	0h	This bit selects the de-emphasis level when the Controller is operating at 5 GT/s [0 = -6 dB, 1 = -3.5 dB].
5	HASD	R/W	0h	When this bit is set, the LTSSM is prevented from changing the operating speed of the link, other than reducing the speed to correct unreliable operation of the link. STICKY
4	EC	R/W	0h	This bit is used to force the Endpoint device to enter the Compliance mode. Software sets this bit to 1 and initiates a hot reset to force the device into the Compliance mode. The target speed for the Compliance mode is determined by the Target Link Speed field of this register. STICKY.

Table 9-1262. PCIE_CORE_RP_I_LINK_CTRL_STATUS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	TLS	R/W	4h	<p>This field sets the target speed when the software forces the link into Compliance mode by setting the Enter Compliance bit in this register</p> <p>[0001 = 2.5 GT/s, 0010 = 5 GT/s, 0100 = 8 GT/s, 1000 = 16 GT/s].</p> <p>The default value of this field is 0001 [2.5 GT/s] when the PCIE_GENERATION_SEL [1:0] strap pins of the Controller are set to 0, 0010 [5 GT/s] when the strap is set to 1, and 0011 [8 GT/s] when the strap pin is set to 10, and 0100 [16 GT/s] when the strap pin is set to 11.</p> <p>STICKY.</p>

9.5.41 PCIE_CORE_RP_I_AER_ENHNCD_CAP Register (Offset = 100h) [reset = 15020001h]

PCIE_CORE_RP_I_AER_ENHNCD_CAP is shown in [Figure 9-430](#) and described in [Table 9-1264](#).

[Return to Summary Table.](#)

N/A

Table 9-1263.
PCIE_CORE_RP_I_AER_ENHNCD_CAP Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0100h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0100h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0100h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0100h

Figure 9-430. PCIE_CORE_RP_I_AER_ENHNCD_CAP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R-150h												R-2h				R-1h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1264. PCIE_CORE_RP_I_AER_ENHNCD_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R	150h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R	2h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 4'h2.
15-0	PECID	R	1h	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express AER Extended Capability Structure [0001 hex].

9.5.42 PCIE_CORE_RP_I_UNCORR_ERR_STATUS Register (Offset = 104h) [reset = 0h]

PCIE_CORE_RP_I_UNCORR_ERR_STATUS is shown in [Figure 9-431](#) and described in [Table 9-1266](#).

Return to [Summary Table](#).

N/A

Table 9-1265.
PCIE_CORE_RP_I_UNCORR_ERR_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0104h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0104h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0104h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0104h

Figure 9-431. PCIE_CORE_RP_I_UNCORR_ERR_STATUS Register

31	30	29	28	27	26	25	24
R28							
R-0h							
23	22	21	20	19	18	17	16
R28	UIE	R27	URE	EE	MT	RO	UC
R-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
CA	CT	FCPE	PT	R26			
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h			
7	6	5	4	3	2	1	0
R26			DLPE	R25			
R-0h			R/W1C-0h	R-0h			

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1266. PCIE_CORE_RP_I_UNCORR_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	R28	R	0h	Reserved
22	UIE	R/W1C	0h	This bit is set when the Controller has detected an internal uncorrectable error [HAL parity error or an uncorrectable ECC error while reading from any of the RAMs]. This bit is also set in response to the client signaling an internal error through the input UNCORRECTABLE_ERROR_IN. This error is considered fatal by default.
21	R27	R	0h	Reserved

Table 9-1266. PCIE_CORE_RP_I_UNCORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	URE	R/W1C	0h	This bit is set when the Controller has received a request from the link that it does not support. This error is not Function-specific. This error is considered non-fatal by default, except for the special case outlined in PCI Express Base Specification 2.0. The header of the received request that caused the error is logged in the Header Log Registers.
19	EE	R/W1C	0h	This bit is set when the Controller has detected an ECRC error in a received TLP.
18	MT	R/W1C	0h	This bit is set when the Controller receives a malformed TLP from the link. This error is considered fatal by default. The header of the received TLP with error is logged in the Header Log Registers.
17	RO	R/W1C	0h	This bit is set when the Controller receives a TLP in violation of the receive credit currently available.
16	UC	R/W1C	0h	This bit is set when the Controller has received an unexpected Completion packet from the link.
15	CA	R/W1C	0h	This bit is set when the Controller has returned the Completer Abort [CA] status to a request received from the link. This error is considered non-fatal by default, except for the special cases outlined in PCI Express Base Specification 2.0. The header of the received request that caused the error is logged in the Header Log Registers.
14	CT	R/W1C	0h	This bit is set when the completion timer associated with an outstanding request times out. This error is considered non-fatal by default.
13	FCPE	R/W1C	0h	This bit is set when certain violations of the flow control protocol are detected by the Controller.
12	PT	R/W1C	0h	This bit is set when the Controller receives a poisoned TLP from the link. This error is considered non-fatal by default. The header of the received TLP with error is logged in the Header Log Registers.
11-5	R26	R	0h	Reserved
4	DLPE	R/W1C	0h	This bit is set when the Controller receives an Ack or Nak DLLP whose sequence does not correspond to that of an unacknowledged TLP or that of the last acknowledged TLP [for details, refer to the PCI Express Base Specifications].

Table 9-1266. PCIE_CORE_RP_I_UNCORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	R25	R	0h	N/A

9.5.43 PCIE_CORE_RP_I_UNCORR_ERR_MASK Register (Offset = 108h) [reset = 00400000h]

PCIE_CORE_RP_I_UNCORR_ERR_MASK is shown in [Figure 9-432](#) and described in [Table 9-1268](#).

Return to [Summary Table](#).

N/A

Table 9-1267.
PCIE_CORE_RP_I_UNCORR_ERR_MASK Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0108h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0108h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0108h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0108h

Figure 9-432. PCIE_CORE_RP_I_UNCORR_ERR_MASK Register

31	30	29	28	27	26	25	24
R32							
R-0h							
23	22	21	20	19	18	17	16
R32	UIEM	R31	UREM	EEM	MTM	ROM	UCM
R-0h	R/W-1h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CAM	CTM	FCPER	PTM	R30			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
R30			DLPER	R29			
R-0h			R/W-0h	R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1268. PCIE_CORE_RP_I_UNCORR_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	R32	R	0h	Reserved
22	UIEM	R/W	1h	This bit is set to mask the reporting of internal errors. STICKY.
21	R31	R	0h	Reserved
20	UREM	R/W	0h	This bit is set to mask the reporting of unexpected requests received from the link. STICKY.
19	EEM	R/W	0h	This bit is set to mask the reporting of ECRC errors. STICKY.
18	MTM	R/W	0h	This bit is set to mask the reporting of malformed TLPs received from the link. STICKY.
17	ROM	R/W	0h	This bit is set to mask the reporting of violations of receive credit. STICKY.
16	UCM	R/W	0h	This bit is set to mask the reporting of unexpected Completions received by the Controller. STICKY.

Table 9-1268. PCIE_CORE_RP_I_UNCORR_ERR_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	CAM	R/W	0h	This bit is set to mask the reporting of the Controller sending a Completer Abort. STICKY.
14	CTM	R/W	0h	This bit is set to mask the reporting of Completion Timeouts. STICKY.
13	FCPER	R/W	0h	This bit is set to mask the reporting of Flow Control Protocol Errors. STICKY.
12	PTM	R/W	0h	This bit is set to mask the reporting of a Poisoned TLP. STICKY.
11-5	R30	R	0h	Reserved
4	DLPER	R/W	0h	This bit is set to mask the reporting of Data Link Protocol Errors. STICKY.
3-0	R29	R	0h	Reserved

9.5.44 PCIE_CORE_RP_I_UNCORR_ERR_SEVERITY Register (Offset = 10Ch) [reset = 00462030h]

PCIE_CORE_RP_I_UNCORR_ERR_SEVERITY is shown in [Figure 9-433](#) and described in [Table 9-1270](#).

Return to [Summary Table](#).

N/A

Table 9-1269.
PCIE_CORE_RP_I_UNCORR_ERR_SEVERITY
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 010Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 010Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 010Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 010Ch

Figure 9-433. PCIE_CORE_RP_I_UNCORR_ERR_SEVERITY Register

31	30	29	28	27	26	25	24
R37							
R-0h							
23	22	21	20	19	18	17	16
R37	UNCORR_INT RNL_ERR_SV RTY	R36	URES	EES	MTS	ROS	UCS
R-0h	R/W-1h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
CAS	CTS	FCPES	PTS	R35			
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
R35		SDES	DLPES	R33			
R-0h		R-1h	R/W-1h	R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1270. PCIE_CORE_RP_I_UNCORR_ERR_SEVERITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	R37	R	0h	N/A
22	UNCORR_INTRNL_ERR_SVRTY	R/W	1h	Severity of internal errors [0 = Non-Fatal, 1 = Fatal].
21	R36	R	0h	Reserved
20	URES	R/W	0h	Severity of unexpected requests received from the link [0 = Non-Fatal, 1 = Fatal]. STICKY.
19	EES	R/W	0h	Severity of ECRC errors [0 = Non-Fatal, 1 = Fatal]. STICKY.

Table 9-1270. PCIE_CORE_RP_I_UNCORR_ERR_SEVERITY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	MTS	R/W	1h	Severity of malformed TLPs received from the link [0 = Non-Fatal, 1 = Fatal]. STICKY.
17	ROS	R/W	1h	Severity of receive credit violations [0 = Non-Fatal, 1 = Fatal]. STICKY.
16	UCS	R/W	0h	Severity of unexpected Completions received by the Controller [0 = Non-Fatal, 1 = Fatal]. STICKY.
15	CAS	R/W	0h	Severity of sending a Completer Abort [0 = Non-Fatal, 1 = Fatal]. STICKY.
14	CTS	R/W	0h	Severity of Completion Timeouts [0 = Non-Fatal, 1 = Fatal]. STICKY.
13	FCPES	R/W	1h	Severity of a Flow Control Protocol Error [0 = Non-Fatal, 1 = Fatal]. STICKY.
12	PTS	R/W	0h	Severity of a Poisoned TLP error [0 = Non-Fatal, 1 = Fatal]. STICKY.
11-6	R35	R	0h	N/A
5	SDES	R	1h	surprise down error severity. This field is hard coded to 1.
4	DLPES	R/W	1h	Severity of Data Link Protocol Errors [0 = Non-Fatal, 1 = Fatal]. STICKY.
3-0	R33	R	0h	Reserved

9.5.45 PCIE_CORE_RP_I_CORR_ERR_STATUS Register (Offset = 110h) [reset = 0h]

PCIE_CORE_RP_I_CORR_ERR_STATUS is shown in [Figure 9-434](#) and described in [Table 9-1272](#).

Return to [Summary Table](#).

N/A

Table 9-1271.
PCIE_CORE_RP_I_CORR_ERR_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0110h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0110h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0110h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0110h

Figure 9-434. PCIE_CORE_RP_I_CORR_ERR_STATUS Register

31	30	29	28	27	26	25	24
R39							
R-0h							
23	22	21	20	19	18	17	16
R39							
R-0h							
15	14	13	12	11	10	9	8
HLOS	CIES	ANES	RTTS	R38		RNRS	
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h		R/W1C-0h	
7	6	5	4	3	2	1	0
BDS	BTS	R37				RES	
R/W1C-0h	R/W1C-0h	R-0h				R/W1C-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1272. PCIE_CORE_RP_I_CORR_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R39	R	0h	Reserved
15	HLOS	R/W1C	0h	This bit is set on a Header Log Register overflow, that is, when the header could not be logged in the Header Log Register because it is occupied by a previous header.
14	CIES	R/W1C	0h	This bit is set when the Controller has detected an internal correctable error condition [a correctable ECC error while reading from any of the RAMs]. This bit is also set in response to the client signaling an internal error through the input CORRECTABLE_ERROR_IN.
13	ANES	R/W1C	0h	This bit is set when an uncorrectable error occurs, which is determined to belong to one of the special cases described in the PCI Express Base Specification 2.0. This causes the Controller to assert the CORRECTABLE_ERROR_OUT output in place of NON_FATAL_ERROR_OUT.

Table 9-1272. PCIE_CORE_RP_I_CORR_ERR_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RTTS	R/W1C	0h	This bit is set when the replay timer in the Data Link Layer of the Controller times out, causing the Controller to re-transmit a TLP.
11-9	R38	R	0h	Reserved
8	RNRS	R/W1C	0h	This bit is set when the replay count rolls over after three re-transmissions of a TLP at the Data Link Layer of the Controller.
7	BDS	R/W1C	0h	This bit is set when an LCRC error is detected in a received DLLP, and no errors were detected by the Physical Layer.
6	BTS	R/W1C	0h	This bit is set when an error is detected in a received TLP by the Data Link Layer of the Controller the conditions causing this error are [1] an LCRC error, [2] the packet terminates with EDB symbol, but its LCRC field does not equal the inverted value of the calculated CRC.
5-1	R37	R	0h	Reserved
0	RES	R/W1C	0h	This bit is set when an error is detected in the receive side of the Physical Layer of the Controller [e.g. an 8b10b decode error].

9.5.46 PCIE_CORE_RP_I_CORR_ERR_MASK Register (Offset = 114h) [reset = E000h]

PCIE_CORE_RP_I_CORR_ERR_MASK is shown in [Figure 9-435](#) and described in [Table 9-1274](#).

Return to [Summary Table](#).

N/A

Table 9-1273. PCIE_CORE_RP_I_CORR_ERR_MASK Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0114h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0114h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0114h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0114h

Figure 9-435. PCIE_CORE_RP_I_CORR_ERR_MASK Register

31	30	29	28	27	26	25	24
R42							
R-0h							
23	22	21	20	19	18	17	16
R42							
R-0h							
15	14	13	12	11	10	9	8
HLOM	CIEM	ANEM	RTTM	R41		RNRM	
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R-0h		R/W-0h	
7	6	5	4	3	2	1	0
BDM	BTM	R40				REM	
R/W-0h	R/W-0h	R-0h				R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1274. PCIE_CORE_RP_I_CORR_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R42	R	0h	Reserved
15	HLOM	R/W	1h	This bit, when set, masks the reporting of an error in response to a Header Log register overflow. STICKY.
14	CIEM	R/W	1h	This bit, when set, masks the reporting of an error in response to a corrected internal error condition. STICKY.
13	ANEM	R/W	1h	This bit, when set, masks the reporting of an error in response to an uncorrectable error occurrence, which is determined to belong to one of the special cases in the PCI Express Base Specification 2.0. STICKY.
12	RTTM	R/W	0h	This bit, when set, masks the reporting of an error in response to a Replay Timer timeout event. STICKY.

Table 9-1274. PCIE_CORE_RP_I_CORR_ERR_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	R41	R	0h	Reserved
8	RNRM	R/W	0h	This bit, when set, masks the reporting of an error in response to a Replay Number Rollover event. STICKY.
7	BDM	R/W	0h	This bit, when set, masks the reporting of an error in response to a 'Bad DLLP' received. STICKY.
6	BTM	R/W	0h	This bit, when set, masks the reporting of an error in response to a 'Bad TLP' received. STICKY.
5-1	R40	R	0h	Reserved
0	REM	R/W	0h	This bit, when set, masks the reporting of Physical Layer errors. STICKY.

9.5.47 PCIE_CORE_RP_I_ADV_ERR_CAP_CTL Register (Offset = 118h) [reset = A0h]

PCIE_CORE_RP_I_ADV_ERR_CAP_CTL is shown in [Figure 9-436](#) and described in [Table 9-1276](#).

Return to [Summary Table](#).

N/A

Table 9-1275.
PCIE_CORE_RP_I_ADV_ERR_CAP_CTL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0118h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0118h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0118h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0118h

Figure 9-436. PCIE_CORE_RP_I_ADV_ERR_CAP_CTL Register

31	30	29	28	27	26	25	24
R43							
R-0h							
23	22	21	20	19	18	17	16
R43							
R-0h							
15	14	13	12	11	10	9	8
R43				TPLP	MHRE	MHRC	EEC
R-0h				R-0h	R-0h	R-0h	R/W-0h
7	6	5	4	3	2	1	0
ECC	EEG	EGC	FEP				
R-1h	R/W-0h	R-1h	R-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1276. PCIE_CORE_RP_I_ADV_ERR_CAP_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	R43	R	0h	Reserved
11	TPLP	R	0h	If Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined. Default value of this bit is 0. This bit is RsvdP if the End-End TLP Prefix Supported bit is Clf Set and the First Error Pointer is valid, indicates that the TLP Prefix Log register contains valid information. If Clear or if First Error Pointer is invalid, the TLP Prefix Log register is undefined.
10	MHRE	R	0h	Setting this bit enables the RC to log multiple error headers in its Header Log Registers. It is hardwired to 0.

Table 9-1276. PCIE_CORE_RP_I_ADV_ERR_CAP_CTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MHRC	R	0h	This bit is set when the RC has the capability to log more than one error header in its Header Log Registers. It is hardwired to 0.
8	EEC	R/W	0h	Setting this bit enables ECRC checking on the receive side of the Controller. This bit is writable from the local management bus. STICKY.
7	ECC	R	1h	This read-only bit indicates to the software that the device is capable of checking ECRC in packets received from the link.
6	EEG	R/W	0h	Setting this bit enables the ECRC generation on the transmit side of the Controller. This bit is writable from the local management bus. STICKY.
5	EGC	R	1h	This read-only bit indicates to the software that the device is capable of generating ECRC in packets transmitted on the link.
4-0	FEP	R	0h	This is a 5-bit pointer to the bit position in the Uncorrectable Error Status Register corresponding to the error that was detected first. When there are multiple bits set in the Uncorrectable Error Status Register, this field informs the software which error was observed first. To prevent the field from being overwritten before the software is able to read it, this field is not updated while the status bit it points to in the Uncorrectable Error Status Register remains set. After the software clears this status bit, a subsequent error condition that sets any bit in the Uncorrectable Error Status Register will update the First Error Pointer. Any uncorrectable error type, including the special cases where the error is reported using an ERR_COR message, will set the First Error Pointer [assuming the software has reset the error pointed by it in the Uncorrectable Error Status Register]. STICKY.

9.5.48 PCIE_CORE_RP_I_HDR_LOG_0 Register (Offset = 11Ch) [reset = 0h]

PCIE_CORE_RP_I_HDR_LOG_0 is shown in [Figure 9-437](#) and described in [Table 9-1278](#).

Return to [Summary Table](#).

N/A

Table 9-1277. PCIE_CORE_RP_I_HDR_LOG_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 011Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 011Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 011Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 011Ch

Figure 9-437. PCIE_CORE_RP_I_HDR_LOG_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1278. PCIE_CORE_RP_I_HDR_LOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD0	R	0h	First Dword of captured TLP header. STICKY.

9.5.49 PCIE_CORE_RP_I_HDR_LOG_1 Register (Offset = 120h) [reset = 0h]

PCIE_CORE_RP_I_HDR_LOG_1 is shown in [Figure 9-438](#) and described in [Table 9-1280](#).

Return to [Summary Table](#).

N/A

**Table 9-1279. PCIE_CORE_RP_I_HDR_LOG_1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0120h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0120h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0120h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0120h

Figure 9-438. PCIE_CORE_RP_I_HDR_LOG_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1280. PCIE_CORE_RP_I_HDR_LOG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD1	R	0h	Second Dword of captured TLP header. STICKY.

9.5.50 PCIE_CORE_RP_I_HDR_LOG_2 Register (Offset = 124h) [reset = 0h]

PCIE_CORE_RP_I_HDR_LOG_2 is shown in [Figure 9-439](#) and described in [Table 9-1282](#).

Return to [Summary Table](#).

N/A

Table 9-1281. PCIE_CORE_RP_I_HDR_LOG_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0124h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0124h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0124h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0124h

Figure 9-439. PCIE_CORE_RP_I_HDR_LOG_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1282. PCIE_CORE_RP_I_HDR_LOG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD2	R	0h	Third Dword of captured TLP header. STICKY.

9.5.51 PCIE_CORE_RP_I_HDR_LOG_3 Register (Offset = 128h) [reset = 0h]

PCIE_CORE_RP_I_HDR_LOG_3 is shown in [Figure 9-440](#) and described in [Table 9-1284](#).

Return to [Summary Table](#).

N/A

**Table 9-1283. PCIE_CORE_RP_I_HDR_LOG_3
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0128h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0128h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0128h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0128h

Figure 9-440. PCIE_CORE_RP_I_HDR_LOG_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1284. PCIE_CORE_RP_I_HDR_LOG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD3	R	0h	Fourth Dword of captured TLP header. STICKY.

9.5.52 PCIE_CORE_RP_I_ROOT_ERR_CMD Register (Offset = 12Ch) [reset = 0h]

PCIE_CORE_RP_I_ROOT_ERR_CMD is shown in [Figure 9-441](#) and described in [Table 9-1286](#).

[Return to Summary Table.](#)

N/A

Table 9-1285. PCIE_CORE_RP_I_ROOT_ERR_CMD Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 012Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 012Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 012Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 012Ch

Figure 9-441. PCIE_CORE_RP_I_ROOT_ERR_CMD Register

31	30	29	28	27	26	25	24
R44							
R-0h							
23	22	21	20	19	18	17	16
R44							
R-0h							
15	14	13	12	11	10	9	8
R44							
R-0h							
7	6	5	4	3	2	1	0
R44				FERE		NFERE	CERE
R-0h				R/W-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1286. PCIE_CORE_RP_I_ROOT_ERR_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	R44	R	0h	Reserved
2	FERE	R/W	0h	If this bit is set, the Controller will active its FATAL_ERROR_OUT output in response to an error message received from the link.
1	NFERE	R/W	0h	If this bit is set, the Controller will active its NON_FATAL_ERROR_OUT output in response to an error message received from the link.
0	CERE	R/W	0h	If this bit is set, the Controller will active its CORRECTABLE_ERROR_OUT output in response to an error message received from the link.

9.5.53 PCIE_CORE_RP_I_ROOT_ERR_STAT Register (Offset = 130h) [reset = 0h]

PCIE_CORE_RP_I_ROOT_ERR_STAT is shown in [Figure 9-442](#) and described in [Table 9-1288](#).

Return to [Summary Table](#).

N/A

Table 9-1287. PCIE_CORE_RP_I_ROOT_ERR_STAT Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0130h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0130h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0130h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0130h

Figure 9-442. PCIE_CORE_RP_I_ROOT_ERR_STAT Register

31	30	29	28	27	26	25	24
R45							
R-0h							
23	22	21	20	19	18	17	16
R45							
R-0h							
15	14	13	12	11	10	9	8
R45							
R-0h							
7	6	5	4	3	2	1	0
R45	FEMR	NEMR	FUF	MEFNR	EFNR	MECR	ECR
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1288. PCIE_CORE_RP_I_ROOT_ERR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R45	R	0h	Reserved
6	FEMR	R/W1C	0h	This bit, when set, indicates that the RC has received one or more Fatal error messages from the link. STICKY
5	NEMR	R/W1C	0h	This bit, when set, indicates that the RC has received one or more Non-Fatal error messages from the link. STICKY
4	FUF	R/W1C	0h	This bit, when set, indicates that the first Uncorrectable error message received was for a Fatal error. STICKY
3	MEFNR	R/W1C	0h	This bit is set when the RC receives either a Fatal or Non-Fatal error message from the link, and the ERR_FATAL/NONFATAL Received bit is already set. STICKY

Table 9-1288. PCIE_CORE_RP_I_ROOT_ERR_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EFNR	R/W1C	0h	This bit is set when the RC receives either a Fatal or Non-Fatal error message from the link. STICKY
1	MECR	R/W1C	0h	This bit is set when the RC receives a Correctable error message from the link, if the ERR_COR received bit is already set. STICKY
0	ECR	R/W1C	0h	This bit is set when the RC receives a Correctable error message from the link. STICKY

9.5.54 PCIE_CORE_RP_I_ERR_SRC_ID Register (Offset = 134h) [reset = 0h]

PCIE_CORE_RP_I_ERR_SRC_ID is shown in [Figure 9-443](#) and described in [Table 9-1290](#).

Return to [Summary Table](#).

N/A

**Table 9-1289. PCIE_CORE_RP_I_ERR_SRC_ID
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0134h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0134h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0134h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0134h

Figure 9-443. PCIE_CORE_RP_I_ERR_SRC_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFNSI																ECSI															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1290. PCIE_CORE_RP_I_ERR_SRC_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	EFNSI	R	0h	This field captures and stores the Requester ID from an ERR_FATAL or ERROR_NONFATAL message received by the RC, if the ERR_FATAL or NONFATAL Received bit was not set at the time the message was received. STICKY
15-0	ECSI	R	0h	This field captures and stores the Requester ID from an ERR_COR message received by the RC, if the ERR_COR bit was not set at the time the message was received. STICKY

9.5.55 PCIE_CORE_RP_I_TLP_PRE_LOG_0 Register (Offset = 138h) [reset = 0h]

PCIE_CORE_RP_I_TLP_PRE_LOG_0 is shown in [Figure 9-444](#) and described in [Table 9-1292](#).

Return to [Summary Table](#).

N/A

Table 9-1291. PCIE_CORE_RP_I_TLP_PRE_LOG_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0138h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0138h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0138h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0138h

Figure 9-444. PCIE_CORE_RP_I_TLP_PRE_LOG_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HD1																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1292. PCIE_CORE_RP_I_TLP_PRE_LOG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	HD1	R	0h	First TLP Prefix of captured TLP STICKY.

9.5.56 PCIE_CORE_RP_I_DEV_SER_NUM_CAP_HDR Register (Offset = 150h) [reset = 30010003h]

PCIE_CORE_RP_I_DEV_SER_NUM_CAP_HDR is shown in [Figure 9-445](#) and described in [Table 9-1294](#).

Return to [Summary Table](#).

N/A

Table 9-1293.
PCIE_CORE_RP_I_DEV_SER_NUM_CAP_HDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0150h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0150h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0150h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0150h

Figure 9-445. PCIE_CORE_RP_I_DEV_SER_NUM_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SNNCO												DSNCV			
R-300h												R-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PECID															
R-3h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1294. PCIE_CORE_RP_I_DEV_SER_NUM_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	SNNCO	R	300h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	DSNCV	R	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus by writing into Function 0 from the local management bus.
15-0	PECID	R	3h	This field is hardwired to the Capability ID assigned by PCI SIG to the PCI Express Device Serial Number Capability [0001 hex].

9.5.57 PCIE_CORE_RP_I_DEV_SER_NUM_0 Register (Offset = 154h) [reset = 0h]

PCIE_CORE_RP_I_DEV_SER_NUM_0 is shown in [Figure 9-446](#) and described in [Table 9-1296](#).

Return to [Summary Table](#).

N/A

Table 9-1295. PCIE_CORE_RP_I_DEV_SER_NUM_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0154h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0154h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0154h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0154h

Figure 9-446. PCIE_CORE_RP_I_DEV_SER_NUM_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSND0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1296. PCIE_CORE_RP_I_DEV_SER_NUM_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DSND0	R	0h	This field contains the first 32 bits of the device's serial number. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

9.5.58 PCIE_CORE_RP_I_DEV_SER_NUM_1 Register (Offset = 158h) [reset = 0h]

PCIE_CORE_RP_I_DEV_SER_NUM_1 is shown in [Figure 9-447](#) and described in [Table 9-1298](#).

Return to [Summary Table](#).

N/A

**Table 9-1297. PCIE_CORE_RP_I_DEV_SER_NUM_1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0158h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0158h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0158h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0158h

Figure 9-447. PCIE_CORE_RP_I_DEV_SER_NUM_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSND1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1298. PCIE_CORE_RP_I_DEV_SER_NUM_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DSND1	R	0h	This field contains the last 32 bits of the device's serial number. This field can be written from the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write.

9.5.59 PCIE_CORE_RP_I_SEC_PCIE_CAP_HDR_REG Register (Offset = 300h) [reset = 4C010019h]

PCIE_CORE_RP_I_SEC_PCIE_CAP_HDR_REG is shown in [Figure 9-448](#) and described in [Table 9-1300](#).

Return to [Summary Table](#).

N/A

Table 9-1299.
PCIE_CORE_RP_I_SEC_PCIE_CAP_HDR_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0300h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0300h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0300h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0300h

Figure 9-448. PCIE_CORE_RP_I_SEC_PCIE_CAP_HDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECI															
R-4C0h												R-1h				R-19h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1300. PCIE_CORE_RP_I_SEC_PCIE_CAP_HDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R	4C0h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1 , but can be modified independently for each PF from [the APB bus by setting [21] bit high of the pcie_mgmt_APB_ADDR during a local management register write] .
15-0	PECI	R	19h	This field is hardwired to the Capability ID assigned by PCI SIG to the Secondary PCI Express Capability

9.5.60 PCIE_CORE_RP_I_LINK_CONTROL3 Register (Offset = 304h) [reset = 0h]

PCIE_CORE_RP_I_LINK_CONTROL3 is shown in [Figure 9-449](#) and described in [Table 9-1302](#).

Return to [Summary Table](#).

N/A

**Table 9-1301. PCIE_CORE_RP_I_LINK_CONTROL3
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0304h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0304h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0304h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0304h

Figure 9-449. PCIE_CORE_RP_I_LINK_CONTROL3 Register

31	30	29	28	27	26	25	24
R2							
R-0h							
23	22	21	20	19	18	17	16
R2							
R-0h							
15	14	13	12	11	10	9	8
R2				ELSOSGV			R1
R-0h				R/W-0h			R-0h
7	6	5	4	3	2	1	0
R1						LERIE	PE
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1302. PCIE_CORE_RP_I_LINK_CONTROL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	R2	R	0h	Reserved
12-9	ELSOSGV	R/W	0h	When the Link is in PCIE_CORE_RP_L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture.
8-2	R1	R	0h	Reserved
1	LERIE	R/W	0h	This bit enables the activation of the PHY_INTERRUPT_OUT output of the Controller when the Link Equalization Request bit in the Link Status 2 Register is set. This is not implemented in controller

Table 9-1302. PCIE_CORE_RP_I_LINK_CONTROL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PE	R/W	0h	<p>The state of this bit determines whether the Controller performs link equalization when the link is retrained by the local software.</p> <p>If this bit is set to 1 when the local software sets the Link Retrain bit in the Link Control Register, and the target link speed is 8 GT/s or 16 GT/s, the LTSSM of the Controller will go through the link equalization states during the retraining.</p>

9.5.61 PCIE_CORE_RP_I_LANE_ERROR_STATUS Register (Offset = 308h) [reset = 0h]

PCIE_CORE_RP_I_LANE_ERROR_STATUS is shown in [Figure 9-450](#) and described in [Table 9-1304](#).

Return to [Summary Table](#).

N/A

Table 9-1303.
PCIE_CORE_RP_I_LANE_ERROR_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0308h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0308h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0308h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0308h

Figure 9-450. PCIE_CORE_RP_I_LANE_ERROR_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0													LES		
R-0h													R/W1C-0h		

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1304. PCIE_CORE_RP_I_LANE_ERROR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	N/A
1-0	LES	R/W1C	0h	Each of these bits indicates the error status for the corresponding lane. STICKY.

9.5.62 PCIE_CORE_RP_I_LANE_EQUALIZATION_CONTROL_0 Register (Offset = 30Ch) [reset = 7F7F7F7Fh]

PCIE_CORE_RP_I_LANE_EQUALIZATION_CONTROL_0 is shown in [Figure 9-451](#) and described in [Table 9-1306](#).

Return to [Summary Table](#).

N/A

Table 9-1305.
PCIE_CORE_RP_I_LANE_EQUALIZATION_CONTROL_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 030Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 030Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 030Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 030Ch

Figure 9-451. PCIE_CORE_RP_I_LANE_EQUALIZATION_CONTROL_0 Register

31	30	29	28	27	26	25	24
R3	UPRPH1			UPTP1			
R-0h	R-7h			R-Fh			
23	22	21	20	19	18	17	16
R2_1	DNRPH1			DNTP1			
R-0h	R-7h			R-Fh			
15	14	13	12	11	10	9	8
R1	UPRPH0			UPTP0			
R-0h	R-7h			R-Fh			
7	6	5	4	3	2	1	0
R0_1	DNRPH0			DNTP0			
R-0h	R-7h			R-Fh			

LEGEND: R = Read Only; -n = value after reset

Table 9-1306. PCIE_CORE_RP_I_LANE_EQUALIZATION_CONTROL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	R3	R	0h	Reserved
30-28	UPRPH1	R	7h	8.0GT/s Value sent by the Controller as the Receiver Preset Hint for the remote receiver associated with Lane 1. The remote node may use this value to adapt its receiver at the start of the link equalization procedure.
27-24	UPTP1	R	Fh	8.0GT/s Value sent by the Controller as the Transmitter Preset for the remote transmitter associated with Lane 1. The remote node uses this value to set up its transmitter at the start of the link equalization procedure.
23	R2_1	R	0h	Reserved
22-20	DNRPH1	R	7h	8.0GT/s Receiver Preset Hint value to be used for the local receiver associated with Lane 1. The Controller uses this value to set up the receiver attached to Lane 1

**Table 9-1306. PCIE_CORE_RP_I_LANE_EQUALIZATION_CONTROL_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	DNTP1	R	Fh	8.0GT/s Transmitter Preset value to be used for the local transmitter associated with Lane 1. The Controller uses this value to set up the Lane 1 transmitter during link equalization.
15	R1	R	0h	Reserved
14-12	UPRPH0	R	7h	8.0GT/s Value sent by the Controller as the Receiver Preset Hint for the remote receiver associated with Lane 0. The remote node may use this value to adapt its receiver at the start of the link equalization procedure.
11-8	UPTP0	R	Fh	8.0GT/s Value sent by the Controller as the Transmitter Preset for the remote transmitter associated with Lane 0. The remote node uses this value to set up its transmitter at the start of the link equalization procedure.
7	R0_1	R	0h	Reserved
6-4	DNRPH0	R	7h	8.0GT/s Receiver Preset Hint value to be used for the local receiver associated with Lane 0. The Controller uses this value to set up the receiver attached to Lane 0
3-0	DNTP0	R	Fh	8.0GT/s Transmitter Preset value to be used for the local transmitter associated with Lane 0. The Controller uses this value to set up the Lane 0 transmitter during link equalization.

9.5.63 PCIE_CORE_RP_I_VC_ENH_CAP_HEADER_REG Register (Offset = 4C0h) [reset = 5C010002h]

PCIE_CORE_RP_I_VC_ENH_CAP_HEADER_REG is shown in [Figure 9-452](#) and described in [Table 9-1308](#).

Return to [Summary Table](#).

N/A

Table 9-1307.
PCIE_CORE_RP_I_VC_ENH_CAP_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04C0h

Figure 9-452. PCIE_CORE_RP_I_VC_ENH_CAP_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R-5C0h												R-1h				R-2h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1308. PCIE_CORE_RP_I_VC_ENH_CAP_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R	5C0h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified independently for each PF from the local management bus.
15-0	PECID	R	2h	This field is hardwired to the Capability ID assigned by PCI SIG to the VC Capability.

9.5.64 PCIE_CORE_RP_I_PORT_VC_CAP_REG_1 Register (Offset = 4C4h) [reset = X]

PCIE_CORE_RP_I_PORT_VC_CAP_REG_1 is shown in [Figure 9-453](#) and described in [Table 9-1310](#).

Return to [Summary Table](#).

N/A

Table 9-1309.
PCIE_CORE_RP_I_PORT_VC_CAP_REG_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04C4h

Figure 9-453. PCIE_CORE_RP_I_PORT_VC_CAP_REG_1 Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0				RESERVED	EVC		
R-0h				R-X	R-3h		

LEGEND: R = Read Only; -n = value after reset

Table 9-1310. PCIE_CORE_RP_I_PORT_VC_CAP_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	R0	R	0h	N/A
3	RESERVED	R	X	
2-0	EVC	R	3h	N/A

9.5.65 PCIE_CORE_RP_I_PORT_VC_CAP_REG_2 Register (Offset = 4C8h) [reset = 0h]

PCIE_CORE_RP_I_PORT_VC_CAP_REG_2 is shown in [Figure 9-454](#) and described in [Table 9-1312](#).

Return to [Summary Table](#).

N/A

Table 9-1311.
PCIE_CORE_RP_I_PORT_VC_CAP_REG_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04C8h

Figure 9-454. PCIE_CORE_RP_I_PORT_VC_CAP_REG_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1312. PCIE_CORE_RP_I_PORT_VC_CAP_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R1	R	0h	N/A

9.5.66 PCIE_CORE_RP_I_PORT_VC_CTRL_STS_REG Register (Offset = 4CCh) [reset = 0h]

PCIE_CORE_RP_I_PORT_VC_CTRL_STS_REG is shown in [Figure 9-455](#) and described in [Table 9-1314](#).

Return to [Summary Table](#).

N/A

Table 9-1313.
PCIE_CORE_RP_I_PORT_VC_CTRL_STS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04CCh

Figure 9-455. PCIE_CORE_RP_I_PORT_VC_CTRL_STS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1314. PCIE_CORE_RP_I_PORT_VC_CTRL_STS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R2	R	0h	N/A

9.5.67 PCIE_CORE_RP_I_VC_RES_CAP_REG_0 Register (Offset = 4D0h) [reset = 0h]

PCIE_CORE_RP_I_VC_RES_CAP_REG_0 is shown in [Figure 9-456](#) and described in [Table 9-1316](#).

Return to [Summary Table](#).

N/A

Table 9-1315.
PCIE_CORE_RP_I_VC_RES_CAP_REG_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04D0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04D0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04D0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04D0h

Figure 9-456. PCIE_CORE_RP_I_VC_RES_CAP_REG_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	R1														
R-0h	R-0h														

LEGEND: R = Read Only; -n = value after reset

Table 9-1316. PCIE_CORE_RP_I_VC_RES_CAP_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R3	R	0h	N/A
15	RST	R	0h	N/A
14-0	R1	R	0h	N/A

9.5.68 PCIE_CORE_RP_I_VC_RES_CTRL_REG_0 Register (Offset = 4D4h) [reset = X]

PCIE_CORE_RP_I_VC_RES_CTRL_REG_0 is shown in [Figure 9-457](#) and described in [Table 9-1318](#).

Return to [Summary Table](#).

N/A

Table 9-1317.
PCIE_CORE_RP_I_VC_RES_CTRL_REG_0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04D4h

Figure 9-457. PCIE_CORE_RP_I_VC_RES_CTRL_REG_0 Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R-1h	R-0h				R-0h		
23	22	21	20	19	18	17	16
R5				PARS		LPAT	
R-0h				R-0h		R-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
TVM						TVM0	
R/W-7Fh						R-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1318. PCIE_CORE_RP_I_VC_RES_CTRL_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R	1h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30-27	R6	R	0h	N/A
26-24	VCI	R	0h	VC ID assigned to VC0. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23-20	R5	R	0h	N/A
19-17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 0. This bit is not implemented, and hardwired to 0.
15-8	RESERVED	R/W	X	

Table 9-1318. PCIE_CORE_RP_I_VC_RES_CTRL_REG_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-1	TVM	R/W	7Fh	Indicates the TCs that are mapped to this VC. When bit 0 of this field is set, it indicates that TC 0 is mapped to VC 0. By default, all TCs are mapped to VC 0.
0	TVM0	R	1h	Indicates the TC0 always mapped to VC0.

9.5.69 PCIE_CORE_RP_I_VC_RES_STS_REG_0 Register (Offset = 4D8h) [reset = X]

PCIE_CORE_RP_I_VC_RES_STS_REG_0 is shown in [Figure 9-458](#) and described in [Table 9-1320](#).

Return to [Summary Table](#).

N/A

Table 9-1319.
PCIE_CORE_RP_I_VC_RES_STS_REG_0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04D8h

Figure 9-458. PCIE_CORE_RP_I_VC_RES_STS_REG_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						VCNP	PATS
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-1320. PCIE_CORE_RP_I_VC_RES_STS_REG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

9.5.70 PCIE_CORE_RP_I_VC_RES_CAP_REG_1 Register (Offset = 4DCh) [reset = 0h]

PCIE_CORE_RP_I_VC_RES_CAP_REG_1 is shown in [Figure 9-459](#) and described in [Table 9-1322](#).

Return to [Summary Table](#).

N/A

Table 9-1321.
PCIE_CORE_RP_I_VC_RES_CAP_REG_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04DCh

Figure 9-459. PCIE_CORE_RP_I_VC_RES_CAP_REG_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	R1														
R-0h	R-0h														

LEGEND: R = Read Only; -n = value after reset

Table 9-1322. PCIE_CORE_RP_I_VC_RES_CAP_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R3	R	0h	N/A
15	RST	R	0h	N/A
14-0	R1	R	0h	N/A

9.5.71 PCIE_CORE_RP_I_VC_RES_CTRL_REG_1 Register (Offset = 4E0h) [reset = X]

PCIE_CORE_RP_I_VC_RES_CTRL_REG_1 is shown in [Figure 9-460](#) and described in [Table 9-1324](#).

Return to [Summary Table](#).

N/A

Table 9-1323.
PCIE_CORE_RP_I_VC_RES_CTRL_REG_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04E0h

Figure 9-460. PCIE_CORE_RP_I_VC_RES_CTRL_REG_1 Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W-0h	R-0h				R/W-1h		
23	22	21	20	19	18	17	16
R5				PARS		LPAT	
R-0h				R-0h		R-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
TVM						TVM0	
R/W-0h						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1324. PCIE_CORE_RP_I_VC_RES_CTRL_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30-27	R6	R	0h	N/A
26-24	VCI	R/W	1h	VC ID assigned to VC1. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23-20	R5	R	0h	N/A
19-17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 1. This bit is not implemented, and hardwired to 0.
15-8	RESERVED	R/W	X	

Table 9-1324. PCIE_CORE_RP_I_VC_RES_CTRL_REG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 1 of this field is set, it indicates that TC 1 is mapped to VC 1. By default, all TCs are mapped to VC 0.
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

9.5.72 PCIE_CORE_RP_I_VC_RES_STS_REG_1 Register (Offset = 4E4h) [reset = X]

PCIE_CORE_RP_I_VC_RES_STS_REG_1 is shown in [Figure 9-461](#) and described in [Table 9-1326](#).

Return to [Summary Table](#).

N/A

Table 9-1325.
PCIE_CORE_RP_I_VC_RES_STS_REG_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04E4h

Figure 9-461. PCIE_CORE_RP_I_VC_RES_STS_REG_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						VCNP	PATS
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-1326. PCIE_CORE_RP_I_VC_RES_STS_REG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

9.5.73 PCIE_CORE_RP_I_VC_RES_CAP_REG_2 Register (Offset = 4E8h) [reset = 0h]

PCIE_CORE_RP_I_VC_RES_CAP_REG_2 is shown in [Figure 9-462](#) and described in [Table 9-1328](#).

Return to [Summary Table](#).

N/A

Table 9-1327.
PCIE_CORE_RP_I_VC_RES_CAP_REG_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04E8h

Figure 9-462. PCIE_CORE_RP_I_VC_RES_CAP_REG_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	R1														
R-0h	R-0h														

LEGEND: R = Read Only; -n = value after reset

Table 9-1328. PCIE_CORE_RP_I_VC_RES_CAP_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R3	R	0h	N/A
15	RST	R	0h	N/A
14-0	R1	R	0h	N/A

9.5.74 PCIE_CORE_RP_I_VC_RES_CTRL_REG_2 Register (Offset = 4ECh) [reset = X]

PCIE_CORE_RP_I_VC_RES_CTRL_REG_2 is shown in [Figure 9-463](#) and described in [Table 9-1330](#).

Return to [Summary Table](#).

N/A

Table 9-1329.
PCIE_CORE_RP_I_VC_RES_CTRL_REG_2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04ECh

Figure 9-463. PCIE_CORE_RP_I_VC_RES_CTRL_REG_2 Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W-0h	R-0h				R/W-2h		
23	22	21	20	19	18	17	16
R5				PARS			LPAT
R-0h				R-0h			R-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
TVM							TVM0
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1330. PCIE_CORE_RP_I_VC_RES_CTRL_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30-27	R6	R	0h	N/A
26-24	VCI	R/W	2h	VC ID assigned to VC2. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23-20	R5	R	0h	N/A
19-17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 2. This bit is not implemented, and hardwired to 0.
15-8	RESERVED	R/W	X	

Table 9-1330. PCIE_CORE_RP_I_VC_RES_CTRL_REG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 2 of this field is set, it indicates that TC 2 is mapped to VC 2. By default, all TCs are mapped to VC 0.
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

9.5.75 PCIE_CORE_RP_I_VC_RES_STS_REG_2 Register (Offset = 4F0h) [reset = X]

PCIE_CORE_RP_I_VC_RES_STS_REG_2 is shown in [Figure 9-464](#) and described in [Table 9-1332](#).

Return to [Summary Table](#).

N/A

Table 9-1331.
PCIE_CORE_RP_I_VC_RES_STS_REG_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04F0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04F0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04F0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04F0h

Figure 9-464. PCIE_CORE_RP_I_VC_RES_STS_REG_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						VCNP	PATS
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-1332. PCIE_CORE_RP_I_VC_RES_STS_REG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

9.5.76 PCIE_CORE_RP_I_VC_RES_CAP_REG_3 Register (Offset = 4F4h) [reset = 0h]

PCIE_CORE_RP_I_VC_RES_CAP_REG_3 is shown in [Figure 9-465](#) and described in [Table 9-1334](#).

Return to [Summary Table](#).

N/A

Table 9-1333.
PCIE_CORE_RP_I_VC_RES_CAP_REG_3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04F4h

Figure 9-465. PCIE_CORE_RP_I_VC_RES_CAP_REG_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	R1														
R-0h	R-0h														

LEGEND: R = Read Only; -n = value after reset

Table 9-1334. PCIE_CORE_RP_I_VC_RES_CAP_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R3	R	0h	N/A
15	RST	R	0h	N/A
14-0	R1	R	0h	N/A

9.5.77 PCIE_CORE_RP_I_VC_RES_CTRL_REG_3 Register (Offset = 4F8h) [reset = X]

PCIE_CORE_RP_I_VC_RES_CTRL_REG_3 is shown in [Figure 9-466](#) and described in [Table 9-1336](#).

Return to [Summary Table](#).

N/A

Table 9-1335.
PCIE_CORE_RP_I_VC_RES_CTRL_REG_3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04F8h

Figure 9-466. PCIE_CORE_RP_I_VC_RES_CTRL_REG_3 Register

31	30	29	28	27	26	25	24
VCEN	R6				VCI		
R/W-0h	R-0h				R/W-3h		
23	22	21	20	19	18	17	16
R5				PARS		LPAT	
R-0h				R-0h		R-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
TVM						TVM0	
R/W-0h						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1336. PCIE_CORE_RP_I_VC_RES_CTRL_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VCEN	R/W	0h	Software uses this bit to enable the VC. For VC0 this bit is hardwired to 1.
30-27	R6	R	0h	N/A
26-24	VCI	R/W	3h	VC ID assigned to VC3. For the VC0, this field is read-only and it is hardwired to 00b. For non VC0 case, it is allowed to use any VC-ID. This VC-ID has to be unique across all VCs. This must not be same as VC0's ID[VC0 ID=0].
23-20	R5	R	0h	N/A
19-17	PARS	R	0h	Configures the VC to use a specific port arbitration scheme. This field is not implemented, and hardwired to 0.
16	LPAT	R	0h	Updates the port arbitration logic from the Port Arbitration Table for VC 3. This bit is not implemented, and hardwired to 0.
15-8	RESERVED	R/W	X	

Table 9-1336. PCIE_CORE_RP_I_VC_RES_CTRL_REG_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-1	TVM	R/W	0h	Indicates the TCs that are mapped to this VC. When bit 3 of this field is set, it indicates that TC 3 is mapped to VC 3. By default, all TCs are mapped to VC 0.
0	TVM0	R	0h	Indicates the TC0 always mapped to VC0.

9.5.78 PCIE_CORE_RP_I_VC_RES_STS_REG_3 Register (Offset = 4FCh) [reset = X]

PCIE_CORE_RP_I_VC_RES_STS_REG_3 is shown in [Figure 9-467](#) and described in [Table 9-1338](#).

Return to [Summary Table](#).

N/A

Table 9-1337.
PCIE_CORE_RP_I_VC_RES_STS_REG_3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 04FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 04FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 04FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 04FCh

Figure 9-467. PCIE_CORE_RP_I_VC_RES_STS_REG_3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						VCNP	PATS
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-1338. PCIE_CORE_RP_I_VC_RES_STS_REG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	VCNP	R	0h	This indicates whether the Virtual Channel negotiation is in pending state. The value of this bit is defined only when the link is in the DL_Active state and Virtual Channel is enabled. When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete.
0	PATS	R	0h	This is not implemented and hardwired to 0.

9.5.79 PCIE_CORE_RP_I_L1_PM_EXT_CAP_HDR Register (Offset = 900h) [reset = 9101001Eh]

PCIE_CORE_RP_I_L1_PM_EXT_CAP_HDR is shown in [Figure 9-468](#) and described in [Table 9-1340](#).

Return to [Summary Table](#).

N/A

Table 9-1339.
PCIE_CORE_RP_I_L1_PM_EXT_CAP_HDR
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0900h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0900h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0900h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0900h

Figure 9-468. PCIE_CORE_RP_I_L1_PM_EXT_CAP_HDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NCO												CV				PECID															
R-910h												R-1h				R-1Eh															

LEGEND: R = Read Only; -n = value after reset

Table 9-1340. PCIE_CORE_RP_I_L1_PM_EXT_CAP_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NCO	R	910h	Indicates offset to the next PCI Express capability structure. The default next pointer value is dynamic and is dependent on whether the strap or LMI bits are set.
19-16	CV	R	1h	Specifies the SIG assigned value for the version of the capability structure. This field is set by default to 1, but can be modified from the local management bus.
15-0	PECID	R	1Eh	This field is hardwired to the Capability ID assigned by PCI SIG to the L1 PM Substates Extended Capability Structure [001E hex].

9.5.80 PCIE_CORE_RP_I_L1_PM_CAP Register (Offset = 904h) [reset = X]

PCIE_CORE_RP_I_L1_PM_CAP is shown in [Figure 9-469](#) and described in [Table 9-1342](#).

Return to [Summary Table](#).

N/A

**Table 9-1341. PCIE_CORE_RP_I_L1_PM_CAP
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0904h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0904h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0904h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0904h

Figure 9-469. PCIE_CORE_RP_I_L1_PM_CAP Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
R0				RESERVED		L1PRTPVRONSCALE	
R-Dh				R-X		R-0h	
15	14	13	12	11	10	9	8
L1PRTCMMMDRESTRTIME							
R-FFh							
7	6	5	4	3	2	1	0
RESERVED			L1PMSUPP	L1ASPML11SU PP	L1ASPML12SU PP	L1PML11SUPP	L1PML12SUPP
R-X			R-1h	R-1h	R-1h	R-1h	R-1h

LEGEND: R = Read Only; -n = value after reset

Table 9-1342. PCIE_CORE_RP_I_L1_PM_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-19	R0	R	Dh	Along with the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register sets the time [in us] that this Port requires the port on the opposite side of Link to wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. The value of Port T_POWER_ON is calculated by multiplying the value in this field by the scale value in the Port T_POWER_ON Scale field in the L1 PM Substates Capabilities register. T Power On is the minimum amount of time that each component must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. This is to ensure no device is ever actively driving into an unpowered component.
18	RESERVED	R	X	

Table 9-1342. PCIE_CORE_RP_I_L1_PM_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	L1PRTPVRONSCALE	R	0h	Specifies the scale used for the Port T_POWER_ON Value field in the L1 PM Substates Capabilities register. Range of Values 00b = 2us 01b = 10us 10b = 100us 11b = Reserved Default value is 00.
15-8	L1PRTCMMMDRESTRTIME	R	FFh	N/A
7-5	RESERVED	R	X	
4	L1PMSUPP	R	1h	N/A
3	L1ASPML11SUPP	R	1h	When Set this bit indicates that ASPM L1.1 is supported.
2	L1ASPML12SUPP	R	1h	When Set this bit indicates that ASPM L1.2 is supported.
1	L1PML11SUPP	R	1h	When Set this bit indicates that PCI-PM L1.1 is supported.
0	L1PML12SUPP	R	1h	When Set this bit indicates that PCI-PM L1.2 is supported.

9.5.81 PCIE_CORE_RP_I_L1_PM_CTRL_1 Register (Offset = 908h) [reset = X]

PCIE_CORE_RP_I_L1_PM_CTRL_1 is shown in [Figure 9-470](#) and described in [Table 9-1344](#).

Return to [Summary Table](#).

N/A

**Table 9-1343. PCIE_CORE_RP_I_L1_PM_CTRL_1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0908h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0908h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0908h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0908h

Figure 9-470. PCIE_CORE_RP_I_L1_PM_CTRL_1 Register

31	30	29	28	27	26	25	24
L1THRSHLDSC			RESERVED			L1THRSHLDVAL	
R/W-0h			R/W-X			R/W-0h	
23	22	21	20	19	18	17	16
L1THRSHLDVAL							
R/W-0h							
15	14	13	12	11	10	9	8
L1CMMDRESTRTIME							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				L1ASPML11EN	L1ASPML12EN	L1PML11EN	L1PML12EN
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1344. PCIE_CORE_RP_I_L1_PM_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	L1THRSHLDSC	R/W	0h	This field provides a scale for the value contained within the LTR_L1.2_THRESHOLD_Value. 000 - Value times 1 ns 001 - Value times 32 ns 010 - Value times 1024 ns 011 - Value times 32,768 ns 100 - Value times 1,048,576 ns 101 - Value times 33,554,422ns 110- 111 - Not permitted
28-26	RESERVED	R/W	X	
25-16	L1THRSHLDVAL	R/W	0h	Along with the LTR_L1.2_THRESHOLD_Scale, this field indicates the LTR threshold used to determine if entry into L1 results in L1.1 [if enabled] or L1.2 [if enabled].
15-8	L1CMMDRESTRTIME	R/W	0h	Sets value of TCOMMONMODE [in us], which must be used by the Downstream Port for timing the re-establishment of common mode. This field must only be modified when the ASPM L1.2 Enable and PCI-PM L1.2 Enable bits are both Clear. This field is reserved since both PCI-PM L1.2 and ASPM L1.2 are Not Supported in this configuration of the Controller.

Table 9-1344. PCIE_CORE_RP_I_L1_PM_CTRL_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	
3	L1ASPML11EN	R/W	0h	When Set this bit enables ASPM L1.1.
2	L1ASPML12EN	R/W	0h	When Set this bit enables ASPM L1.2.
1	L1PML11EN	R/W	0h	When Set this bit enables PCI-PM L1.1.
0	L1PML12EN	R/W	0h	When Set this bit enables PCI-PM L1.2.

9.5.82 PCIE_CORE_RP_I_L1_PM_CTRL_2 Register (Offset = 90Ch) [reset = X]

PCIE_CORE_RP_I_L1_PM_CTRL_2 is shown in [Figure 9-471](#) and described in [Table 9-1346](#).

Return to [Summary Table](#).

N/A

Table 9-1345. PCIE_CORE_RP_I_L1_PM_CTRL_2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 090Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 090Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 090Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 090Ch

Figure 9-471. PCIE_CORE_RP_I_L1_PM_CTRL_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
L1PWRONVAL				RESERVED		L1PWRONSC	
R/W-5h				R/W-X		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1346. PCIE_CORE_RP_I_L1_PM_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-3	L1PWRONVAL	R/W	5h	Along with the T_POWER_ON Scale sets the minimum amount of time [in us] that the Port must wait in L1.2.Exit after sampling CLKREQ# asserted before actively driving the interface. T_POWER_ON is calculated by multiplying the value in this field by the value in the T_POWER_ON Scale field.
2	RESERVED	R/W	X	
1-0	L1PWRONSC	R/W	0h	Specifies the scale used for T_POWER_ON Value. Range of Values 00b = 2us 01b = 10us 10b = 100us 11b = Reserved

9.5.83 PCIE_CORE_RP_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = 910h) [reset = 92010025h]

PCIE_CORE_RP_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG is shown in [Figure 9-472](#) and described in [Table 9-1348](#).

Return to [Summary Table](#).

N/A

Table 9-1347.
PCIE_CORE_RP_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0910h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0910h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0910h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0910h

Figure 9-472. PCIE_CORE_RP_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DLFNXCAP												DLFCAPVER			
R-920h												R-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLFCAPID															
R-25h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1348. PCIE_CORE_RP_I_DL_FEATURE_EXTENDED_CAPABILITY_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	DLFNXCAP	R	920h	The offset to the next PCI Extended Capability structure.
19-16	DLFCAPVER	R	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	DLFCAPID	R	25h	Indicates that the associated extended capability structure is the DL Feature Extended Capability. This field returns a Capability ID of 0025h.

9.5.84 PCIE_CORE_RP_I_DL_FEATURE_CAPABILITIES_REG Register (Offset = 914h) [reset = 80000001h]

PCIE_CORE_RP_I_DL_FEATURE_CAPABILITIES_REG is shown in [Figure 9-473](#) and described in [Table 9-1350](#).

[Return to Summary Table.](#)

N/A

Table 9-1349.
PCIE_CORE_RP_I_DL_FEATURE_CAPABILITIES_R
EG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0914h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0914h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0914h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0914h

Figure 9-473. PCIE_CORE_RP_I_DL_FEATURE_CAPABILITIES_REG Register

31	30	29	28	27	26	25	24
DLFEXEN	R0						
R-1h	R-0h						
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0							DLFCAPVER
R-0h							R-1h

LEGEND: R = Read Only; -n = value after reset

Table 9-1350. PCIE_CORE_RP_I_DL_FEATURE_CAPABILITIES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DLFEXEN	R	1h	If Set, this bit indicates that this Port will enter the DL_Feature negotiation state prior to Link Initialization.
30-1	R0	R	0h	Reserved
0	DLFCAPVER	R	1h	This bit indicates that this Port supports the Scaled Flow Control Feature.

9.5.85 PCIE_CORE_RP_I_DL_FEATURE_STATUS_REG Register (Offset = 918h) [reset = 0h]

PCIE_CORE_RP_I_DL_FEATURE_STATUS_REG is shown in [Figure 9-474](#) and described in [Table 9-1352](#).

Return to [Summary Table](#).

N/A

Table 9-1351.
PCIE_CORE_RP_I_DL_FEATURE_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0918h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0918h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0918h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0918h

Figure 9-474. PCIE_CORE_RP_I_DL_FEATURE_STATUS_REG Register

31	30	29	28	27	26	25	24
RDLFSVAL	R1						
R-0h	R-0h						
23	22	21	20	19	18	17	16
R23	R0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						RSFSUP	
R-0h						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-1352. PCIE_CORE_RP_I_DL_FEATURE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RDLFSVAL	R	0h	This bit indicates that the Port has received a Data Link Feature DLLP in state DL_Feature [see Section 3.2.1] and that the Remote Data Link Feature Supported and Remote Data Link Feature Ack fields are meaningful. This bit is Cleared on entry to state DL_Inactive. Default is 0b.
30-24	R1	R	0h	Reserved
23	R23	R	0h	Reserved
22-1	R0	R	0h	Reserved
0	RSFSUP	R	0h	This bit indicates that the Remote end Device supports the Scaled Flow Control Feature.

9.5.86 PCIE_CORE_RP_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = 920h) [reset = 9C010027h]

PCIE_CORE_RP_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG is shown in [Figure 9-475](#) and described in [Table 9-1354](#).

Return to [Summary Table](#).

N/A

Table 9-1353.
PCIE_CORE_RP_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0920h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0920h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0920h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0920h

Figure 9-475. PCIE_CORE_RP_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MARNXCAP												MARCAPVER			
R-9C0h												R-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MARCAPID															
R-27h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1354. PCIE_CORE_RP_I_MARGINING_EXTENDED_CAPABILITY_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	MARNXCAP	R	9C0h	The offset to the next PCI Extended Capability structure.
19-16	MARCAPVER	R	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	MARCAPID	R	27h	Indicates that the associated extended capability structure is the Margining Extended Capability. This field returns a Capability ID of 0027h.

9.5.87 PCIE_CORE_RP_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register (Offset = 924h) [reset = 1h]

PCIE_CORE_RP_I_MARGINING_PORT_CAPABILITIES_STATUS_REG is shown in [Figure 9-476](#) and described in [Table 9-1356](#).

Return to [Summary Table](#).

N/A

Table 9-1355.
PCIE_CORE_RP_I_MARGINING_PORT_CAPABILITIES_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0924h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0924h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0924h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0924h

Figure 9-476. PCIE_CORE_RP_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register

31	30	29	28	27	26	25	24
R1							
R-0h							
23	22	21	20	19	18	17	16
R1						MSRDY	MRDY
R-0h						R-0h	R-0h
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0							MARUDS
R-0h							R-1h

LEGEND: R = Read Only; -n = value after reset

Table 9-1356. PCIE_CORE_RP_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	R1	R	0h	Reserved
17	MSRDY	R	0h	When Margining uses Driver Software is Set, then this bit, when Set, indicates that the required software has performed the required initialization. The value of this bit is Undefined if Margining users Driver Software is Clear. The Controller implementation sets the default value of this bit to 0. The driver software must initialize the Rx Margining parameters in the Local Management Lane Margining Registers and then program this bit to 1.

Table 9-1356. PCIE_CORE_RP_I_MARGINING_PORT_CAPABILITIES_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	MRDY	R	0h	Indicates when the Margining feature is ready to accept margining commands. If the Margining uses Driver Software bit is 1, then the Controller sets this status bit when the Margining Software Ready bit is set and the Link is in Gen4 PCIE_CORE_RP_L0 state. If the Margining uses Driver Software bit is 0, then the Controller sets this status bit when the Link is in Gen4 PCIE_CORE_RP_L0 state.
15-1	R0	R	0h	Reserved
0	MARUDS	R	1h	If Set, indicates that Margining is partially implemented using Device Driver software. Margining Software Ready indicates when this software is initialized. If Clear, Margining does not require device driver software. The Controller implementation requires driver software to initialize the Rx Margining parameter values in Local Management Registers for Lane Margining. Hence, the default value of this bit is set to 1.

9.5.88 PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register (Offset = 928h) [reset = 9C38h]

PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG0 is shown in [Figure 9-477](#) and described in [Table 9-1358](#).

Return to [Summary Table](#).

N/A

Table 9-1357.
PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0928h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0928h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0928h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0928h

Figure 9-477. PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register

31	30	29	28	27	26	25	24
MPSTS							
R-0h							
23	22	21	20	19	18	17	16
R1	UMSTS	MTSTS		RNSTS			
R-0h	R-0h	R-0h		R-0h			
15	14	13	12	11	10	9	8
MRGPAY							
R/W-9Ch							
7	6	5	4	3	2	1	0
R0	USGMOD	MRGTYP		RCVNUM			
R-0h	R/W-0h	R/W-7h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1358. PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MPSTS	R	0h	Margin Payload Status for Margining Commands. This field is reset upon DL Down.
23	R1	R	0h	Reserved
22	UMSTS	R	0h	Usage Model Status for Margining Commands. This field is reset upon DL Down.
21-19	MTSTS	R	0h	Margin Type Status for Margining Commands. This field is reset upon DL Down.
18-16	RNSTS	R	0h	Receiver Number Status for Margining Commands. This field is reset upon DL Down.
15-8	MRGPAY	R/W	9Ch	Margin Payload for Margining Commands. This field is reset upon DL Down.
7	R0	R	0h	Reserved
6	USGMOD	R/W	0h	Usage Model for Margining Commands. This field is reset upon DL Down.

Table 9-1358. PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	MRGTYP	R/W	7h	Margin Type for Margining Commands. This field is reset upon DL Down.
2-0	RCVNUM	R/W	0h	Receiver Number for Margining Commands. This field is reset upon DL Down.

9.5.89 PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register (Offset = 92Ch) [reset = 9C38h]

PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG1 is shown in [Figure 9-478](#) and described in [Table 9-1360](#).

Return to [Summary Table](#).

N/A

Table 9-1359.
PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 092Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 092Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 092Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 092Ch

Figure 9-478. PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register

31	30	29	28	27	26	25	24
MPSTS							
R-0h							
23	22	21	20	19	18	17	16
R1	UMSTS	MTSTS		RNSTS			
R-0h	R-0h	R-0h		R-0h			
15	14	13	12	11	10	9	8
MRGPAY							
R/W-9Ch							
7	6	5	4	3	2	1	0
R0	USGMOD	MRGTYP		RCVNUM			
R-0h	R/W-0h	R/W-7h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1360. PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MPSTS	R	0h	Margin Payload Status for Margining Commands. This field is reset upon DL Down.
23	R1	R	0h	Reserved
22	UMSTS	R	0h	Usage Model Status for Margining Commands. This field is reset upon DL Down.
21-19	MTSTS	R	0h	Margin Type Status for Margining Commands. This field is reset upon DL Down.
18-16	RNSTS	R	0h	Receiver Number Status for Margining Commands. This field is reset upon DL Down.
15-8	MRGPAY	R/W	9Ch	Margin Payload for Margining Commands. This field is reset upon DL Down.
7	R0	R	0h	Reserved
6	USGMOD	R/W	0h	Usage Model for Margining Commands. This field is reset upon DL Down.

Table 9-1360. PCIE_CORE_RP_I_MARGINING_LANE_CONTROL_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	MRGTYP	R/W	7h	Margin Type for Margining Commands. This field is reset upon DL Down.
2-0	RCVNUM	R/W	0h	Receiver Number for Margining Commands. This field is reset upon DL Down.

9.5.90 PCIE_CORE_RP_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = 9C0h) [reset = A2010026h]

PCIE_CORE_RP_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG is shown in [Figure 9-479](#) and described in [Table 9-1362](#).

Return to [Summary Table](#).

N/A

Table 9-1361.
PCIE_CORE_RP_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09C0h

Figure 9-479. PCIE_CORE_RP_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PL16NXCAP												PL16CAPVER			
R-A20h												R-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL16CAPID															
R-26h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1362. PCIE_CORE_RP_I_PL_16GTS_EXTENDED_CAPABILITY_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PL16NXCAP	R	A20h	The offset to the next PCI Extended Capability structure.
19-16	PL16CAPVER	R	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	PL16CAPID	R	26h	Indicates that the associated extended capability structure is for Physical layer 16 GT/s. This field returns a Capability ID of 0026h.

9.5.91 PCIE_CORE_RP_I_PL_16GTS_CAPABILITIES_REG Register (Offset = 9C4h) [reset = 0h]

PCIE_CORE_RP_I_PL_16GTS_CAPABILITIES_REG is shown in [Figure 9-480](#) and described in [Table 9-1364](#).

Return to [Summary Table](#).

N/A

Table 9-1363.
PCIE_CORE_RP_I_PL_16GTS_CAPABILITIES_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09C4h

Figure 9-480. PCIE_CORE_RP_I_PL_16GTS_CAPABILITIES_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1364. PCIE_CORE_RP_I_PL_16GTS_CAPABILITIES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R0	R	0h	Reserved

9.5.92 PCIE_CORE_RP_I_PL_16GTS_CONTROL_REG Register (Offset = 9C8h) [reset = 0h]

PCIE_CORE_RP_I_PL_16GTS_CONTROL_REG is shown in [Figure 9-481](#) and described in [Table 9-1366](#).

Return to [Summary Table](#).

N/A

Table 9-1365.
PCIE_CORE_RP_I_PL_16GTS_CONTROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09C8h

Figure 9-481. PCIE_CORE_RP_I_PL_16GTS_CONTROL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1366. PCIE_CORE_RP_I_PL_16GTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R0	R	0h	Reserved

9.5.93 PCIE_CORE_RP_I_PL_16GTS_STATUS_REG Register (Offset = 9CCh) [reset = 0h]

PCIE_CORE_RP_I_PL_16GTS_STATUS_REG is shown in [Figure 9-482](#) and described in [Table 9-1368](#).

Return to [Summary Table](#).

N/A

Table 9-1367.
PCIE_CORE_RP_I_PL_16GTS_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09CCh

Figure 9-482. PCIE_CORE_RP_I_PL_16GTS_STATUS_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0			LE16	EP3S16	EP2S16	EP1S16	EQC16
R-0h			R/W1C-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1368. PCIE_CORE_RP_I_PL_16GTS_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	R0	R	0h	Reserved
4	LE16	R/W1C	0h	This bit can be set by the software running on the EndPoint to force the Endpoint to request link equalization for 16.0 GT/s. Setting this bit causes the LTSSM of the Controller to enter the Recovery state and request its link partner to perform equalization. This bit is cleared when the LTSSM enters the Recovery.Equalization state. It can also be cleared by writing a 1 to this bit position by the host, or writing a 0 from the LMI. STICKY.
3	EP3S16	R	0h	This bit, when set to 1, indicates that the Phase 3 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.

Table 9-1368. PCIE_CORE_RP_I_PL_16GTS_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EP2S16	R	0h	This bit, when set to 1, indicates that the Phase 2 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.
1	EP1S16	R	0h	This bit, when set to 1, indicates that the Phase 1 of the Transmitter Equalization procedure has completed successfully for 16.0 GT/s. STICKY.
0	EQC16	R	0h	This bit, when set to 1, indicates that the Transmitter Equalization procedure has completed for 16.0 GT/s. STICKY.

9.5.94 PCIE_CORE_RP_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG Register (Offset = 9D0h) [reset = 0h]

PCIE_CORE_RP_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG is shown in [Figure 9-483](#) and described in [Table 9-1370](#).

Return to [Summary Table](#).

N/A

Table 9-1369.
PCIE_CORE_RP_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_R
EG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09D0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09D0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09D0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09D0h

Figure 9-483. PCIE_CORE_RP_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						LDPMS16	
R-0h						R/W1C-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1370. PCIE_CORE_RP_I_PL_16GTS_LOCAL_DATA_PARITY_MISMATCH_STATUS_REG Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	N/A
1-0	LDPMS16	R/W1C	0h	Each bit indicates if the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number.

9.5.95 PCIE_CORE_RP_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG

Register (Offset = 9D4h) [reset = 0h]

PCIE_CORE_RP_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG is shown in [Figure 9-484](#) and described in [Table 9-1372](#).

Return to [Summary Table](#).

N/A

Table 9-1371.
PCIE_CORE_RP_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_S
TATUS_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09D4h

Figure 9-484. PCIE_CORE_RP_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG
Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						FRDPMS16	
R-0h						R/W1C-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1372. PCIE_CORE_RP_I_PL_16GTS_FIRST_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG
Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	N/A
1-0	FRDPMS16	R/W1C	0h	Each bit indicates if the first retimer in the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The value of this field is undefined when no Retimers are present.

9.5.96 PCIE_CORE_RP_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register (Offset = 9D8h) [reset = 0h]

PCIE_CORE_RP_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG is shown in [Figure 9-485](#) and described in [Table 9-1374](#).

Return to [Summary Table](#).

N/A

Table 9-1373.
PCIE_CORE_RP_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09D8h

Figure 9-485.
PCIE_CORE_RP_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						SRDPMS16	
R-0h						R/W1C-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1374.
PCIE_CORE_RP_I_PL_16GTS_SECOND_RETIMER_DATA_PARITY_MISMATCH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	N/A
1-0	SRDPMS16	R/W1C	0h	Each bit indicates if the second retimer in the corresponding Lane detected a Data Parity mismatch. A value of 1b indicates that a mismatch was detected on the corresponding Lane Number. The value of this field is undefined when no Retimers are present.

9.5.97 PCIE_CORE_RP_I_PL_16GTS_RESERVED_REG Register (Offset = 9DCh) [reset = 0h]

PCIE_CORE_RP_I_PL_16GTS_RESERVED_REG is shown in [Figure 9-486](#) and described in [Table 9-1376](#).

Return to [Summary Table](#).

N/A

Table 9-1375.
PCIE_CORE_RP_I_PL_16GTS_RESERVED_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09DCh

Figure 9-486. PCIE_CORE_RP_I_PL_16GTS_RESERVED_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1376. PCIE_CORE_RP_I_PL_16GTS_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	R0	R	0h	Reserved

9.5.98 PCIE_CORE_RP_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 Register (Offset = 9E0h) [reset = FFFFh]

PCIE_CORE_RP_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 is shown in [Figure 9-487](#) and described in [Table 9-1378](#).

Return to [Summary Table](#).

N/A

Table 9-1377.
PCIE_CORE_RP_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 09E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 09E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 09E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 09E0h

Figure 9-487. PCIE_CORE_RP_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPTP116				DPTP116				UPTP016				DPTP016			
R-Fh				R-Fh				R-Fh				R-Fh			

LEGEND: R = Read Only; -n = value after reset

Table 9-1378. PCIE_CORE_RP_I_PL_16GTS_LANE_EQUALIZATION_CONTROL_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-12	UPTP116	R	Fh	16.0GT/s Lane 1 Transmitter Preset value that the Downstream Port sends on the associated Lane to the Endpoint device during 16GT/s Link Equalization.
11-8	DPTP116	R	Fh	Transmitter Preset used for 16.0 GT/s equalization by this Port when the Port is operating as a Downstream Port.
7-4	UPTP016	R	Fh	16.0GT/s Lane 0 Transmitter Preset value that the Downstream Port sends on the associated Lane to the Endpoint device during 16GT/s Link Equalization.
3-0	DPTP016	R	Fh	Transmitter Preset used for 16.0 GT/s equalization by this Port when the Port is operating as a Downstream Port.

9.5.99 PCIE_CORE_RP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register (Offset = A20h) [reset = 0001001Fh]

PCIE_CORE_RP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG is shown in [Figure 9-488](#) and described in [Table 9-1380](#).

Return to [Summary Table](#).

N/A

Table 9-1379.
PCIE_CORE_RP_I_PTM_EXTENDED_CAPABILITY_
HEADER_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0A20h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0A20h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0A20h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0A20h

Figure 9-488. PCIE_CORE_RP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PTMNXCAP												PTMCAPVER			
R-0h												R-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMCAPIID															
R-1Fh															

LEGEND: R = Read Only; -n = value after reset

Table 9-1380. PCIE_CORE_RP_I_PTM_EXTENDED_CAPABILITY_HEADER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PTMNXCAP	R	0h	The offset to the next PCIe Extended Capability structure.
19-16	PTMCAPVER	R	1h	This field is a PCI-SIG defined version number that indicates the version of the Capability structure present.
15-0	PTMCAPIID	R	1Fh	Indicates that the associated extended capability structure is for Precision Time Measurement capability. This field returns a Capability ID of 001Fh.

9.5.100 PCIe_CORE_RP_I_PTM_CAPABILITIES_REG Register (Offset = A24h) [reset = 206h]

PCIE_CORE_RP_I_PTM_CAPABILITIES_REG is shown in [Figure 9-489](#) and described in [Table 9-1382](#).

Return to [Summary Table](#).

N/A

Table 9-1381.
PCIE_CORE_RP_I_PTM_CAPABILITIES_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0A24h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0A24h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0A24h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0A24h

Figure 9-489. PCIe_CORE_RP_I_PTM_CAPABILITIES_REG Register

31	30	29	28	27	26	25	24
R16							
R-0h							
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
LOCCLKGR							
R-2h							
7	6	5	4	3	2	1	0
R3				PTMRTCAP		PTMRSCAP	PTMRQCAP
R-0h				R-1h		R-1h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-1382. PCIe_CORE_RP_I_PTM_CAPABILITIES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-8	LOCCLKGR	R	2h	In RC Mode: The Controller uses the CORE_CLK as the Local Clock for PTM. This field is used to indicate the Time Period of the CORE_CLK. If the PTM Root Select is 1, then CORE_CLK is used to provide PTM Master Time. If the PTM Root Select is 0, then CORE_CLK is used to locally track the PTM Master Time received on the PTM_LOCAL_TIMER_IN [63:0] input. By default, this field is set to 8'd2. This bit can be programmed through the local management APB interface if required.
7-3	R3	R	0h	Reserved

Table 9-1382. PCIE_CORE_RP_I_PTM_CAPABILITIES_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PTMRTCAP	R	1h	<p>This bit is used to indicate that the Controller implements PTM Time Source Role and is capable of serving as PTM Root.</p> <p>By default, this bit is set to 1 when the Controller is in RC Mode.</p> <p>This bit can be programmed through the local management APB interface if required.</p> <p>Note: If this bit is programmed to 1, then the PTM Responder Capable bit must also be programmed to 1 by FW.</p>
1	PTMRSCAP	R	1h	<p>This bit is used to indicate support for PTM Responder Role.</p> <p>By default, this bit is set to 1 when the Controller is in RC Mode.</p> <p>This bit can be programmed through the local management APB interface if required.</p> <p>Note: If the PTM Root Capable is programmed to 1, then this bit must also be programmed to 1 by FW.</p>
0	PTMRQCAP	R	0h	<p>This bit is used to indicate support for PTM Requester Role.</p> <p>By default, this bit is set to 0 when the Controller is in RC Mode.</p> <p>This bit can be programmed through the local management APB interface if required.</p>

9.5.101 PCIE_CORE_RP_I_PTM_CONTROL_REG Register (Offset = A28h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTROL_REG is shown in [Figure 9-490](#) and described in [Table 9-1384](#).

Return to [Summary Table](#).

N/A

Table 9-1383.
PCIE_CORE_RP_I_PTM_CONTROL_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D00 0A28h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D80 0A28h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E00 0A28h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E80 0A28h

Figure 9-490. PCIE_CORE_RP_I_PTM_CONTROL_REG Register

31	30	29	28	27	26	25	24
R16							
R-0h							
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
EFFGRN							
R-0h							
7	6	5	4	3	2	1	0
R2						RTSEL	PTMEN
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1384. PCIE_CORE_RP_I_PTM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-8	EFFGRN	R	0h	This field is used only in PTM Requester Mode and is not used in RC Mode. This field is set to 00 by default in RC Mode.
7-2	R2	R	0h	Reserved
1	RTSEL	R/W	0h	This field is configured by System SW. When set to 1 and when PTM Enable bit is also set to 1, this PTM Source is the PTM Root. Default value of this bit is 0.
0	PTMEN	R/W	0h	When Set, this function is permitted to participate in the PTM mechanism as PTM Requester. By default, this bit is set to 0.

9.5.102 PCIE_CORE_RP_I_PL_CONFIG_0_REG Register (Offset = 00100000h) [reset = 22h]

PCIE_CORE_RP_I_PL_CONFIG_0_REG is shown in [Figure 9-491](#) and described in [Table 9-1386](#).

[Return to Summary Table.](#)

N/A

Table 9-1385.
PCIE_CORE_RP_I_PL_CONFIG_0_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0000h

Figure 9-491. PCIE_CORE_RP_I_PL_CONFIG_0_REG Register

31	30	29	28	27	26	25	24
MLE	R0	LTSSM					
R/W-0h	R-0h	R-0h					
23	22	21	20	19	18	17	16
RLID							
R-0h							
15	14	13	12	11	10	9	8
RFC							
R-0h							
7	6	5	4	3	2	1	0
TSS	APER	LTD	NS		NLC		LS
R/W-0h	R/W-0h	R-1h	R-0h		R-1h		R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1386. PCIE_CORE_RP_I_PL_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MLE	R/W	0h	When the Controller is operating as a Root Port, setting this to 1 causes the LTSSM to initiate a loopback and become the loopback master. This bit is not used in the EndPoint Mode.
30	R0	R	0h	A 1 in this field indicates that the remote node advertised Linkwidth Upconfigure Capability in the training sequences in the Configuration.Complete state when the link came up. A 0 indicates that the remote node did not set the Link Upconfigure bit.
29-24	LTSSM	R	0h	Current state of the LTSSM. The encoding of the states is given in Appendix C.
23-16	RLID	R	0h	Link ID received from other side during link training.

Table 9-1386. PCIE_CORE_RP_I_PL_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	RFC	R	0h	FTS count received from the other side during link training for use at the 2.5 GT/s link speed. The Controller transmits this many FTS sequences while exiting the LOS state, when operating at the 2.5 GT/s speed.
7	TSS	R/W	0h	This bit drives the PIPE_TX_SWING output of the Controller.
6	APER	R/W	0h	This bit controls the reporting of Errors Detected by the PHY. The Errors Detected by the PHY include:- - Received errors indicated on PIPE RxStatus interface, - 8.0 GT/s Invalid Sync Header received error, - 16.0 GT/s Invalid Sync Header received error, If PHY Error Reporting bit is set to 0, the Controller will only report those errors that caused a TLP or DLLP to be dropped because of a Detected PHY Error. If PHY Error Reporting bit is set to 1, the Controller will report all Detected PHY Errors regardless of whether a TLP or DLLP was dropped. The following registers report PHY error in conjunction with this bit: - Correctable Error Status Register, PCIE_CORE_RP_I_CORR_ERR_STATUS, bit-0, Receiver Error Status - Local Error and Status Register, PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGISTER, bit-7, Phy Error In addition to the Errors Detected by the PHY[PCS], the Controller detects the following Physical Layer Protocol Framing Errors: - Framing Errors in the received DLLP and TLP - Ordered Set Block Received Without EDS - Data Block Received After EDS - Illegal Ordered Set Block Received After EDS - Ordered Set Block Received After Skip OS Note: These Errors are always reported independent of the setting of this bit.
5	LTD	R	1h	The state of this bit indicates whether the Controller completed link training as an upstream port[EndPoint][=0] or a downstream port[Root Port][=1]. Default value depends on CORE_TYPE strap pin.
4-3	NS	R	0h	Current operating speed of link [00 = 2.5G, 01 = 5G, 10 = 8G, 11 = 16G].
2-1	NLC	R	1h	Lane count negotiated with other side during link training [00 = x1, 01 = x2, 10 = x4, 11 = x8].
0	LS	R	0h	Current state of link [1 = link training complete, 0 = link training not complete].

9.5.103 PCIE_CORE_RP_I_PL_CONFIG_1_REG Register (Offset = 00100004h) [reset = 40808000h]

PCIE_CORE_RP_I_PL_CONFIG_1_REG is shown in [Figure 9-492](#) and described in [Table 9-1388](#).

Return to [Summary Table](#).

N/A

Table 9-1387.
PCIE_CORE_RP_I_PL_CONFIG_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0004h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0004h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0004h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0004h

Figure 9-492. PCIE_CORE_RP_I_PL_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFC3								TFC2								TFC1								TLI							
R/W-40h								R/W-80h								R/W-80h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1388. PCIE_CORE_RP_I_PL_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TFC3	R/W	40h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from LOS state.
23-16	TFC2	R/W	80h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from LOS state.
15-8	TFC1	R/W	80h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from LOS state.
7-0	TLI	R/W	0h	Link ID transmitted by the device in training sequences in the Root Port mode.

9.5.104 PCIE_CORE_RP_I_DLL_TMR_CONFIG_REG Register (Offset = 00100008h) [reset = 0h]

PCIE_CORE_RP_I_DLL_TMR_CONFIG_REG is shown in [Figure 9-493](#) and described in [Table 9-1390](#).

Return to [Summary Table](#).

N/A

Table 9-1389.
PCIE_CORE_RP_I_DLL_TMR_CONFIG_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0008h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0008h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0008h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0008h

Figure 9-493. PCIE_CORE_RP_I_DLL_TMR_CONFIG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R25								RSART								R9								TSRT							
R-0h								R/W-0h								R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1390. PCIE_CORE_RP_I_DLL_TMR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	R25	R	0h	Reserved
24-16	RSART	R/W	0h	Additional receive side ACK-NAK timer timeout interval. This 9-bit value is added as a signed 2's complement number to the internal ACK-NAK timer timeout value computed by the Controller based on the PCI Express Specifications. This enables the user to make minor adjustments to the spec-defined replay timer settings. Its value is in multiples of [2 Symbol Times] At Gen1 adjustment range = [+2040 ns to -2048 ns]. At Gen2 adjustment range = [+1020 ns to -1024 ns]. At Gen3 adjustment range = [+510 ns to -512 ns].
15-9	R9	R	0h	Reserved
8-0	TSRT	R/W	0h	Additional transmit-side replay timer timeout interval. This 9-bit value is added as a signed 2's complement number to the internal replay timer timeout value computed by the Controller based on the PCI Express Specifications. This enables the user to make minor adjustments to the spec-defined replay timer settings. Its value is in multiples of [2 Symbol Times] At Gen1 adjustment range = [+2040 ns to -2048 ns]. At Gen2 adjustment range = [+1020 ns to -1024 ns]. At Gen3 adjustment range = [+510 ns to -512 ns].

9.5.105 PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG Register (Offset = 0010000Ch) [reset = 02020080h]

PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG is shown in [Figure 9-494](#) and described in [Table 9-1392](#).

Return to [Summary Table](#).

N/A

Table 9-1391.
PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 000Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 000Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 000Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 000Ch

Figure 9-494. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC										PPC									
R/W-20h												R/W-20h										R/W-80h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1392. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R/W	20h	<p>Non-Posted payload credit limit advertised by the Controller for VC 0.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 0.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
19-12	PHC	R/W	20h	<p>Posted header credit limit advertised by the Controller for VC 0.</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-1392. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	PPC	R/W	80h	<p>Posted payload credit limit advertised by the Controller for VC 0. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 0.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

9.5.106 PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG Register (Offset = 00100010h) [reset = 20h]

PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG is shown in [Figure 9-495](#) and described in [Table 9-1394](#).

Return to [Summary Table](#).

N/A

Table 9-1393.
PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0010h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0010h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0010h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0010h

Figure 9-495. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R2				CPC								NPHCL											
R/W-0h								R-0h				R/W-0h								R/W-20h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1394. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 0 [in number of packets]. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23-20	R2	R	0h	Reserved

Table 9-1394. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-8	CPC	R/W	0h	<p>Completion payload credit limit advertised by the Controller for VC 0.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 0.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
7-0	NPHCL	R/W	20h	<p>Non-Posted header credit limit advertised by the Controller for VC 0 [in number of packets].</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 0.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

9.5.107 PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG Register (Offset = 00100014h) [reset = 0h]

PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG is shown in [Figure 9-496](#) and described in [Table 9-1396](#).

Return to [Summary Table](#).

N/A

Table 9-1395.
PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0014h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0014h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0014h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0014h

Figure 9-496. PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC									PPC										
R-0h												R-0h									R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 9-1396. PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 0. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
19-12	PHC	R	0h	Posted header credit limit received by the Controller for this link . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11-0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 0. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]

9.5.108 PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG Register (Offset = 00100018h) [reset = 0h]

PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG is shown in [Figure 9-497](#) and described in [Table 9-1398](#).

Return to [Summary Table](#).

N/A

Table 9-1397.
PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0018h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0018h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0018h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0018h

Figure 9-497. PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R3				CPC								NPHC											
R-0h								R-0h				R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 9-1398. PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R	0h	Completion header credit limit received by the Controller for VC 0 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23-20	R3	R	0h	Reserved
19-8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 0. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
7-0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 0 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 0. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

9.5.109 PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register (Offset = 0010001Ch) [reset = 00040004h]

PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG is shown in [Figure 9-498](#) and described in [Table 9-1400](#).

Return to [Summary Table](#).

N/A

Table 9-1399.
PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 001Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 001Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 001Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 001Ch

Figure 9-498. PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MNUI																MPUI															
R/W-4h																R/W-4h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1400. PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MNUI	R/W	4h	<p>Minimum credit update interval for non-posted transactions. The Controller follows this minimum interval between issuing posted credit updates on the link. This is to limit the bandwidth use of credit updates.</p> <p>If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update.</p> <p>The value is in units of 16 ns.</p> <p>This field is re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h.</p> <p>The user may override this default value by writing into this register field.</p> <p>The value written will be lost on a change in the negotiated link width/speed.</p>

Table 9-1400. PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	MPUI	R/W	4h	<p>Minimum credit update interval for posted transactions. The Controller follows this minimum interval between issuing posted credit updates on the link. This is to limit the bandwidth use of credit updates.</p> <p>If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update.</p> <p>The value is in units of 16 ns.</p> <p>This field is re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h.</p> <p>The user may override this default value by writing into this register field.</p> <p>The value written will be lost on a change in the negotiated link width/speed.</p>

9.5.110 PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register (Offset = 00100020h) [reset = 03AA0004h]

PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG is shown in [Figure 9-499](#) and described in [Table 9-1402](#).

Return to [Summary Table](#).

N/A

Table 9-1401.
PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0020h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0020h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0020h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0020h

Figure 9-499. PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MUI																CUI															
R/W-3AAh																R/W-4h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1402. PCIE_CORE_RP_I_TRANSM_CRED_UPDATE_INT_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MUI	R/W	3AAh	<p>Maximum credit update interval for all transactions.</p> <p>If no new credit has become available since the last update, the Controller will repeat the last update after this interval.</p> <p>This is to recover from any losses of credit update packets.</p> <p>The value is in units of 16 ns.</p> <p>This field could be re-written by the internal logic when the negotiated link width or link speed changes, to correspond to the default values defined in defines.h.</p> <p>The user may override this default value by writing into this register field.</p> <p>The value written will be lost on a change in the negotiated link width/speed.</p>
15-0	CUI	R/W	4h	<p>Minimum credit update interval for Completion packets.</p> <p>The Controller follows this minimum interval between issuing completion credit updates on the link.</p> <p>This is to limit the bandwidth use of credit updates.</p> <p>If new credit becomes available in the receive FIFO since the last update was sent, the Controller will issue a new update only after this interval has elapsed since the last update.</p> <p>The value is in units of 16 ns.</p> <p>This parameter is not used when the Completion credit is infinity.</p>

9.5.111 PCIE_CORE_RP_I_L0S_TIMEOUT_LIMIT_REG Register (Offset = 00100024h) [reset = 177h]

PCIE_CORE_RP_I_L0S_TIMEOUT_LIMIT_REG is shown in [Figure 9-500](#) and described in [Table 9-1404](#).

Return to [Summary Table](#).

N/A

Table 9-1403.
PCIE_CORE_RP_I_L0S_TIMEOUT_LIMIT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0024h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0024h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0024h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0024h

Figure 9-500. PCIE_CORE_RP_I_L0S_TIMEOUT_LIMIT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4																LT															
R-0h																R/W-177h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1404. PCIE_CORE_RP_I_L0S_TIMEOUT_LIMIT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R4	R	0h	Reserved
15-0	LT	R/W	177h	Contains the timeout value [in units of 16 ns] for transitioning to the L0S power state. Setting this parameter to 0 permanently disables the transition to the L0S power state.

9.5.112 PCIE_CORE_RP_I_TRANSMIT_TLP_COUNT_REG Register (Offset = 00100028h) [reset = 0h]

PCIE_CORE_RP_I_TRANSMIT_TLP_COUNT_REG is shown in [Figure 9-501](#) and described in [Table 9-1406](#).

Return to [Summary Table](#).

N/A

Table 9-1405.
PCIE_CORE_RP_I_TRANSMIT_TLP_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0028h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0028h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0028h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0028h

Figure 9-501. PCIE_CORE_RP_I_TRANSMIT_TLP_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTC																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1406. PCIE_CORE_RP_I_TRANSMIT_TLP_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TTC	R/W1C	0h	Count of TLPs transmitted

9.5.113 PCIE_CORE_RP_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register (Offset = 0010002Ch) [reset = 0h]

PCIE_CORE_RP_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG is shown in [Figure 9-502](#) and described in [Table 9-1408](#).

Return to [Summary Table](#).

N/A

Table 9-1407.
PCIE_CORE_RP_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 002Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 002Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 002Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 002Ch

Figure 9-502. PCIE_CORE_RP_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTPBC																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1408. PCIE_CORE_RP_I_TRANSMIT_TLP_PAYLOAD_DWORD_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TTPBC	R/W1C	0h	Count of TLPs payload Dwords transmitted

9.5.114 PCIE_CORE_RP_I_RECEIVE_TLP_COUNT_REG Register (Offset = 00100030h) [reset = 0h]

PCIE_CORE_RP_I_RECEIVE_TLP_COUNT_REG is shown in [Figure 9-503](#) and described in [Table 9-1410](#).

Return to [Summary Table](#).

N/A

Table 9-1409.
PCIE_CORE_RP_I_RECEIVE_TLP_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0030h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0030h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0030h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0030h

Figure 9-503. PCIE_CORE_RP_I_RECEIVE_TLP_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTC																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1410. PCIE_CORE_RP_I_RECEIVE_TLP_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RTC	R/W1C	0h	Count of TLPs received

9.5.115 PCIE_CORE_RP_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register (Offset = 00100034h) [reset = 0h]

PCIE_CORE_RP_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG is shown in [Figure 9-504](#) and described in [Table 9-1412](#).

Return to [Summary Table](#).

N/A

Table 9-1411.
PCIE_CORE_RP_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0034h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0034h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0034h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0034h

Figure 9-504. PCIE_CORE_RP_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTPDC																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1412. PCIE_CORE_RP_I_RECEIVE_TLP_PAYLOAD_DWORD_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RTPDC	R/W1C	0h	Count of TLP payload Dwords received

9.5.116 PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_0_REG Register (Offset = 00100038h) [reset = 00BEBC20h]

PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_0_REG is shown in [Figure 9-505](#) and described in [Table 9-1414](#).

Return to [Summary Table](#).

N/A

Table 9-1413.
PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0038h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0038h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0038h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0038h

Figure 9-505. PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R5								CTL																							
R-0h								R/W-00BEBC20h																							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1414. PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R5	R	0h	Reserved
23-0	CTL	R/W	00BEBC20h	Timeout limit for completion timers [in 4 ns cycles]. Default value is 50 ms in 4 ns cycles. Please note that there could be a variation of 0 to +8us on the programmed Completion Timeout.

9.5.117 PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_1_REG Register (Offset = 0010003Ch) [reset = 02FAF080h]

PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_1_REG is shown in [Figure 9-506](#) and described in [Table 9-1416](#).

Return to [Summary Table](#).

N/A

Table 9-1415.
PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 003Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 003Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 003Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 003Ch

Figure 9-506. PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R6				CTL																											
R-0h				R/W-02FAF080h																											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1416. PCIE_CORE_RP_I_COMPLN_TMOUT_LIM_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	R6	R	0h	Reserved
27-0	CTL	R/W	02FAF080h	Timeout limit for completion timers [in 4 ns cycles]. Default value is 200ms in 4ns cycles. Please note that there could be a variation of 0 to +8us on the programmed Completion Timeout.

9.5.118 PCIE_CORE_RP_I_L1_ST_REENTRY_DELAY_REG Register (Offset = 00100040h) [reset = 0h]

PCIE_CORE_RP_I_L1_ST_REENTRY_DELAY_REG is shown in [Figure 9-507](#) and described in [Table 9-1418](#).

Return to [Summary Table](#).

N/A

Table 9-1417.
PCIE_CORE_RP_I_L1_ST_REENTRY_DELAY_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0040h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0040h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0040h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0040h

Figure 9-507. PCIE_CORE_RP_I_L1_ST_REENTRY_DELAY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L1RD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1418. PCIE_CORE_RP_I_L1_ST_REENTRY_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	L1RD	R/W	0h	Delay to re-enter L1 after no activity [in units of 16 ns].

9.5.119 PCIe_CORE_RP_I_VENDOR_ID_REG Register (Offset = 00100044h) [reset = 17CD17CDh]

PCIE_CORE_RP_I_VENDOR_ID_REG is shown in [Figure 9-508](#) and described in [Table 9-1420](#).

Return to [Summary Table](#).

N/A

**Table 9-1419. PCIe_CORE_RP_I_VENDOR_ID_REG
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0044h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0044h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0044h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0044h

Figure 9-508. PCIe_CORE_RP_I_VENDOR_ID_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVID																VID															
R/W-17CDh																R/W-17CDh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1420. PCIe_CORE_RP_I_VENDOR_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SVID	R/W	17CDh	Subsystem Vendor ID
15-0	VID	R/W	17CDh	Vendor ID

9.5.120 PCIE_CORE_RP_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register (Offset = 00100048h) [reset = 2EEh]

PCIE_CORE_RP_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG is shown in [Figure 9-509](#) and described in [Table 9-1422](#).

Return to [Summary Table](#).

N/A

Table 9-1421.
PCIE_CORE_RP_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0048h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0048h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0048h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0048h

Figure 9-509. PCIE_CORE_RP_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register

31	30	29	28	27	26	25	24
DISLNRXCHK	R7						
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
R7				L1T			
R-0h				R/W-2EEh			
15	14	13	12	11	10	9	8
L1T							
R/W-2EEh							
7	6	5	4	3	2	1	0
L1T							
R/W-2EEh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1422. PCIE_CORE_RP_I_ASPM_L1_ENTRY_TMOUT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DISLNRXCHK	R/W	0h	This bit is used to configure the ASPM L1 Entry mechanism: 1: Link is checked for IDLE only on the TX to determine ASPM L1 Entry. ASPM L1 entry is initiated if no TLP is transmitted for the L1 timeout period. 0: Link is checked for IDLE both on the TX and RX to determine ASPM L1 Entry. ASPM L1 entry is initiated if no TLP is transmitted/received for the L1 timeout period.
30-20	R7	R	0h	Reserved
19-0	L1T	R/W	2EEh	Contains the timeout value[in units of 16 ns] for transitioning to the L1 power state. Setting it to 0 permanently disables the transition to the L1 power state.

9.5.121 PCIe_CORE_RP_I_PME_TURNOFF_ACK_DELAY_REG Register (Offset = 0010004Ch) [reset = 64h]

PCIE_CORE_RP_I_PME_TURNOFF_ACK_DELAY_REG is shown in [Figure 9-510](#) and described in [Table 9-1424](#).

[Return to Summary Table.](#)

N/A

Table 9-1423.
PCIE_CORE_RP_I_PME_TURNOFF_ACK_DELAY_R
EG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 004Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 004Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 004Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 004Ch

Figure 9-510. PCIe_CORE_RP_I_PME_TURNOFF_ACK_DELAY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7																PTOAd															
R-0h																R/W-64h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1424. PCIe_CORE_RP_I_PME_TURNOFF_ACK_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R7	R	0h	Reserved
15-0	PTOAd	R/W	64h	Time in microseconds between the Controller receiving a PME_TurnOff message TLP and the Controller sending a PME_TO_Ack response to it. This field must be set to a non-zero value in order for the Controller to send a response. Setting this field to 0 suppresses the Controller's response to PME_TurnOff message, so that the client may transmit the PME_TO_Ack message through the master interface.

9.5.122 PCIE_CORE_RP_I_LINKWIDTH_CONTROL_REG Register (Offset = 00100050h) [reset = 3h]

PCIE_CORE_RP_I_LINKWIDTH_CONTROL_REG is shown in [Figure 9-511](#) and described in [Table 9-1426](#).

Return to [Summary Table](#).

N/A

Table 9-1425.
PCIE_CORE_RP_I_LINKWIDTH_CONTROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0050h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0050h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0050h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0050h

Figure 9-511. PCIE_CORE_RP_I_LINKWIDTH_CONTROL_REG Register

31	30	29	28	27	26	25	24
EPLSCRL	R2				EPTLS		
R/W-0h	R-0h				R/W-0h		
23	22	21	20	19	18	17	16
R1						RL	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						TLM	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1426. PCIE_CORE_RP_I_LINKWIDTH_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EPLSCRL	R/W	0h	Writing a 1 into this field results in the Controller re-training the link to change its speed. When setting this bit to 1, the software must also set the EP Target Link Speed field to indicate the speed that the EP desires to change on the link. The EP Controller will attempt to change the link to this speed. This bit is cleared by the internal logic of the Controller after the re-training has been completed and link has reached the PCIE_CORE_RP_L0 state. Software must wait for the bit to be clear before setting it again to change the link speed.
30-26	R2	R	0h	Reserved

Table 9-1426. PCIE_CORE_RP_I_LINKWIDTH_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-24	EPTLS	R/W	0h	<p>This field contains the Link Speed that the EP intends to change to during the re-training.</p> <p>Client needs to ensure that this field is programmed to a speed which is lesser than or equal to the Target Link Speed field of PF0 Configuration Link Control 2 Register.</p> <p>Client also needs to ensure that this does not exceed PCIE_GENERATION_SEL strap input.</p> <p>Defined encodings of this field are:</p> <p>00 - GEN1 01 - GEN2 10 - GEN3 11 - GEN4</p>
23-17	R1	R	0h	Reserved
16	RL	R/W	0h	<p>Writing a 1 into this field results in the Controller re-training the link to change its width.</p> <p>When setting this bit to 1, the software must also set the target lane-map field to indicate the lanes it desires to be part of the link.</p> <p>The Controller will attempt to form a link with this set of lanes.</p> <p>The link formed at the end of the retraining may include all of these lanes [if both nodes agree on them during re-training], or the largest subset that both sides were able to activate.</p> <p>This bit is cleared by the internal logic of the Controller after the re-training has been completed and link has reached the PCIE_CORE_RP_L0 state.</p> <p>Software must wait for the bit to be clear before setting it again to change the link width.</p>
15-2	R0	R	0h	Reserved
1-0	TLM	R/W	3h	<p>This field contains the bitmap of the lanes to be included in forming the link during the re-training.</p> <p>01 - Retrain to a x1 link 11 - Retrain to a x2 link</p> <p>If the target lane map includes lanes that were inactive when retraining is initiated, then both the Controller and its link partner must support the LinkWidth Upconfigure Capability to be able to activate those lanes.</p> <p>In RC Mode, the user can check if the remote node has this capability by reading the Remote Link Upconfigure Capability Status bit in Physical Layer Configuration Register 0 after the link first came up.</p>

9.5.123 PCIE_CORE_RP_I_MULTI_VC_CONROL_REG Register (Offset = 00100070h) [reset = 2h]

PCIE_CORE_RP_I_MULTI_VC_CONROL_REG is shown in [Figure 9-512](#) and described in [Table 9-1428](#).

Return to [Summary Table](#).

N/A

Table 9-1427.
PCIE_CORE_RP_I_MULTI_VC_CONROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0070h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0070h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0070h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0070h

Figure 9-512. PCIE_CORE_RP_I_MULTI_VC_CONROL_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31			RES4	RES2		WAIT_4_ALL_VC_CC_RDY	DMAAM
R-0h			R-0h	R-0h		R/W-1h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1428. PCIE_CORE_RP_I_MULTI_VC_CONROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	R31	R	0h	Reserved
4	RES4	R	0h	Reserved
3-2	RES2	R	0h	Reserved
1	WAIT_4_ALL_VC_CC_RDY	R/W	1h	When this bit is set, the controller waits for credits to be available to be able to send atleast 1 max payload TLP in all enabled VCs. When this bit is not set, the controller waits for credits to be available to be able to send atleast 1 max payload TLP in any of the enabled VCs [PCI-SIG recommended].
0	DMAAM	R	0h	Reserved

9.5.124 PCIE_CORE_RP_I_SRIS_CONTROL_REG Register (Offset = 00100074h) [reset = 1h]

PCIE_CORE_RP_I_SRIS_CONTROL_REG is shown in [Figure 9-513](#) and described in [Table 9-1430](#).

Return to [Summary Table](#).

N/A

Table 9-1429.
PCIE_CORE_RP_I_SRIS_CONTROL_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0074h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0074h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0074h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0074h

Figure 9-513. PCIE_CORE_RP_I_SRIS_CONTROL_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31							SRISE
R-0h							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1430. PCIE_CORE_RP_I_SRIS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R31	R	0h	Reserved
0	SRISE	R/W	1h	Setting this bit enables SRIS mode in the PHY layer. This bit should be changed before link training begins by holding the LINK_TRAINING_ENABLE input to 1'b0. When SRIS is disabled using this bit the Lower SKP OS Generation Supported Speeds Vector and Lower SKP OS Reception Supported Speeds Vector in the Link Capabilities Register 2 will be forced to ZERO. The default value of this register can be controlled using the SRIS_ENABLE strap input.

9.5.125 PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC1 Register (Offset = 00100080h) [reset = 02020080h]

PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC1 is shown in [Figure 9-514](#) and described in [Table 9-1432](#).

Return to [Summary Table](#).

N/A

Table 9-1431.
PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0080h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0080h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0080h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0080h

Figure 9-514. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC						PPC													
R/W-20h												R/W-20h						R/W-80h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1432. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R/W	20h	<p>Non-Posted payload credit limit advertised by the Controller for VC 1.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 1.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
19-12	PHC	R/W	20h	<p>Posted header credit limit advertised by the Controller for VC 1.</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 1.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-1432. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	PPC	R/W	80h	<p>Posted payload credit limit advertised by the Controller for VC 1. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 1.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

9.5.126 PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC1 Register (Offset = 00100084h) [reset = 20h]

PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC1 is shown in [Figure 9-515](#) and described in [Table 9-1434](#).

Return to [Summary Table](#).

N/A

Table 9-1433.
PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0084h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0084h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0084h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0084h

Figure 9-515. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R2				CPC								NPHCL											
R/W-0h								R-0h				R/W-0h								R/W-20h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1434. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 1 [in number of packets]. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 1. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23-20	R2	R	0h	Reserved

Table 9-1434. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-8	CPC	R/W	0h	<p>Completion payload credit limit advertised by the Controller for VC 1.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 1.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
7-0	NPHCL	R/W	20h	<p>Non-Posted header credit limit advertised by the Controller for VC 1 [in number of packets].</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 1.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

9.5.127 PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC1 Register (Offset = 00100088h) [reset = 0h]

PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC1 is shown in [Figure 9-516](#) and described in [Table 9-1436](#).

Return to [Summary Table](#).

N/A

Table 9-1435.
PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC
1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0088h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0088h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0088h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0088h

Figure 9-516. PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC									PPC										
R-0h												R-0h									R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 9-1436. PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 1. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
19-12	PHC	R	0h	Posted header credit limit received by the Controller for this link . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 1. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11-0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 1. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]

9.5.128 PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC1 Register (Offset = 0010008Ch) [reset = 0h]

PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC1 is shown in [Figure 9-517](#) and described in [Table 9-1438](#).

Return to [Summary Table](#).

N/A

Table 9-1437.
PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC
1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 008Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 008Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 008Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 008Ch

Figure 9-517. PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R3				CPC								NPHC											
R-0h								R-0h				R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 9-1438. PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R	0h	Completion header credit limit received by the Controller for VC 1 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 1 . 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23-20	R3	R	0h	Reserved
19-8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 1 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 1 . 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
7-0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 1 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 1 . 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

9.5.129 PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC2 Register (Offset = 00100090h) [reset = 02020080h]

PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC2 is shown in [Figure 9-518](#) and described in [Table 9-1440](#).

Return to [Summary Table](#).

N/A

Table 9-1439.
PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0090h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0090h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0090h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0090h

Figure 9-518. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC						PPC													
R/W-20h												R/W-20h						R/W-80h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1440. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R/W	20h	<p>Non-Posted payload credit limit advertised by the Controller for VC 2.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 2.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
19-12	PHC	R/W	20h	<p>Posted header credit limit advertised by the Controller for VC 2.</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 2.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-1440. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	PPC	R/W	80h	<p>Posted payload credit limit advertised by the Controller for VC 2. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 2.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

9.5.130 PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC2 Register (Offset = 00100094h) [reset = 20h]

PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC2 is shown in [Figure 9-519](#) and described in [Table 9-1442](#).

Return to [Summary Table](#).

N/A

Table 9-1441.
PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC2
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0094h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0094h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0094h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0094h

Figure 9-519. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R2				CPC								NPHCL											
R/W-0h								R-0h				R/W-0h								R/W-20h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1442. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 2 [in number of packets]. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 2. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23-20	R2	R	0h	Reserved

Table 9-1442. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-8	CPC	R/W	0h	<p>Completion payload credit limit advertised by the Controller for VC 2.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 2.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
7-0	NPHCL	R/W	20h	<p>Non-Posted header credit limit advertised by the Controller for VC 2 [in number of packets].</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 2.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

9.5.131 PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC2 Register (Offset = 00100098h) [reset = 0h]

PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC2 is shown in [Figure 9-520](#) and described in [Table 9-1444](#).

Return to [Summary Table](#).

N/A

Table 9-1443.
PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC
2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0098h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0098h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0098h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0098h

Figure 9-520. PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC						PPC													
R-0h												R-0h						R-0h													

LEGEND: R = Read Only; -n = value after reset

Table 9-1444. PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 2. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
19-12	PHC	R	0h	Posted header credit limit received by the Controller for this link . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 2. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11-0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 2. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]

9.5.132 PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC2 Register (Offset = 0010009Ch) [reset = 0h]

PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC2 is shown in [Figure 9-521](#) and described in [Table 9-1446](#).

Return to [Summary Table](#).

N/A

Table 9-1445.
PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC
2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 009Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 009Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 009Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 009Ch

Figure 9-521. PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R3				CPC								NPHC											
R-0h								R-0h				R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 9-1446. PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R	0h	Completion header credit limit received by the Controller for VC 2 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 2. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23-20	R3	R	0h	Reserved
19-8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 2 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 2. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
7-0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 2 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 2. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

9.5.133 PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC3 Register (Offset = 001000A0h) [reset = 02020080h]

PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC3 is shown in [Figure 9-522](#) and described in [Table 9-1448](#).

Return to [Summary Table](#).

N/A

Table 9-1447.
PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00A0h

Figure 9-522. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC						PPC													
R/W-20h												R/W-20h						R/W-80h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1448. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R/W	20h	<p>Non-Posted payload credit limit advertised by the Controller for VC 3.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 3.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
19-12	PHC	R/W	20h	<p>Posted header credit limit advertised by the Controller for VC 3.</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 3.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

Table 9-1448. PCIE_CORE_RP_I_RCV_CRED_LIM_0_REG_VC3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	PPC	R/W	80h	<p>Posted payload credit limit advertised by the Controller for VC 3. This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 3.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

9.5.134 PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC3 Register (Offset = 001000A4h) [reset = 20h]

PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC3 is shown in [Figure 9-523](#) and described in [Table 9-1450](#).

Return to [Summary Table](#).

N/A

Table 9-1449.
PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC3
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00A4h

Figure 9-523. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R2				CPC								NPHCL											
R/W-0h								R-0h				R/W-0h								R/W-20h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1450. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R/W	0h	Completion header credit limit advertised by the Controller for VC 3 [in number of packets]. This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 3. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs. Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs. Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP. Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.
23-20	R2	R	0h	Reserved

Table 9-1450. PCIE_CORE_RP_I_RCV_CRED_LIM_1_REG_VC3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-8	CPC	R/W	0h	<p>Completion payload credit limit advertised by the Controller for VC 3.</p> <p>This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Local Posted Payload Credit Scale for VC 3.</p> <p>00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of 4 DW and then advertised in the InitFC DLLPs.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>
7-0	NPHCL	R/W	20h	<p>Non-Posted header credit limit advertised by the Controller for VC 3 [in number of packets].</p> <p>This field is in units of 1, 4 or 16 Packet Headers based on the Local Posted Header Credit Scale for VC 3.</p> <p>00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers]</p> <p>Note: When Scaled FLOW Control is Activated, the programmed credit value is advertised in the InitFC DLLPs.</p> <p>Else, the programmed credit value is internally normalized to units of [1 Packet Header] and then advertised in the InitFC DLLPs.</p> <p>Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.</p> <p>Caution: The programmed Header and Payload credit values must not exceed the actual size of the Receive Buffer.</p>

9.5.135 PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC3 Register (Offset = 001000A8h) [reset = 0h]

PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC3 is shown in [Figure 9-524](#) and described in [Table 9-1452](#).

[Return to Summary Table.](#)

N/A

Table 9-1451.
PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC
3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00A8h

Figure 9-524. PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPPC												PHC									PPC										
R-0h												R-0h									R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 9-1452. PCIE_CORE_RP_I_TRANSM_CRED_LIM_0_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	NPPC	R	0h	Non-Posted payload credit limit received by the Controller for Link 0 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 3. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
19-12	PHC	R	0h	Posted header credit limit received by the Controller for this link . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 3. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
11-0	PPC	R	0h	Posted payload credit limit received by the Controller for this link . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 3. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]

9.5.136 PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC3 Register (Offset = 001000ACh) [reset = 0h]

PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC3 is shown in [Figure 9-525](#) and described in [Table 9-1454](#).

Return to [Summary Table](#).

N/A

Table 9-1453.
PCIE_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC
3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00ACh

Figure 9-525. PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHC								R3				CPC								NPHC											
R-0h								R-0h				R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 9-1454. PCIe_CORE_RP_I_TRANSM_CRED_LIM_1_REG_VC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CHC	R	0h	Completion header credit limit received by the Controller for VC 3 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 3. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.
23-20	R3	R	0h	Reserved
19-8	CPC	R	0h	Completion payload credit limit received by the Controller for VC 3 . This field is in units of 4 DWords, 16 DWords or 64 DWords based on the Remote Posted Payload Credit Scale for VC 3. 00b => [units of 4 DWords] 01b => [units of 4 DWords] 10b => [units of 16 DWords] 11b => [units of 64 DWords]
7-0	NPHC	R	0h	Non-Posted header credit limit received by the Controller for VC 3 . This field is in units of 1, 4 or 16 Packet Headers based on the Remote Posted Header Credit Scale for VC 3. 00b => [units of 1 Packet Header] 01b => [units of 1 Packet Header] 10b => [units of 4 Packet Headers] 11b => [units of 16 Packet Headers] Note: Packet Header represents one maximum-size TLP Header + TLP Digest + maximum number of EndEnd TLP Prefixes permitted in a TLP.

9.5.137 PCIE_CORE_RP_I_FC_INIT_DELAY_REG Register (Offset = 001000F0h) [reset = 64h]

PCIE_CORE_RP_I_FC_INIT_DELAY_REG is shown in [Figure 9-526](#) and described in [Table 9-1456](#).

Return to [Summary Table](#).

N/A

Table 9-1455.
PCIE_CORE_RP_I_FC_INIT_DELAY_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 00F0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 00F0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 00F0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 00F0h

Figure 9-526. PCIE_CORE_RP_I_FC_INIT_DELAY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R4																FCINITDLY															
R-0h																R/W-64h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1456. PCIE_CORE_RP_I_FC_INIT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R4	R	0h	Reserved
15-0	FCINITDLY	R/W	64h	Delay between successive sets of P, NP, CPL FC_INIT DLLP transmissions for VCx.

9.5.138 PCIE_CORE_RP_I_SHDW_HDR_LOG_0_REG Register (Offset = 00100100h) [reset = 0h]

PCIE_CORE_RP_I_SHDW_HDR_LOG_0_REG is shown in [Figure 9-527](#) and described in [Table 9-1458](#).

Return to [Summary Table](#).

N/A

Table 9-1457.
PCIE_CORE_RP_I_SHDW_HDR_LOG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0100h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0100h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0100h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0100h

Figure 9-527. PCIE_CORE_RP_I_SHDW_HDR_LOG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHDW_HDR_LOG_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1458. PCIE_CORE_RP_I_SHDW_HDR_LOG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHDW_HDR_LOG_0	R/W	0h	<p>The value here will be reflected in the target function's header log register when f/w sets any bit in the shadow error register.</p> <p>If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set.</p> <p>This register holds [31:0] value of the TLP header.</p>

9.5.139 PCIE_CORE_RP_I_SHDW_HDR_LOG_1_REG Register (Offset = 00100104h) [reset = 0h]

PCIE_CORE_RP_I_SHDW_HDR_LOG_1_REG is shown in [Figure 9-528](#) and described in [Table 9-1460](#).

Return to [Summary Table](#).

N/A

Table 9-1459.
PCIE_CORE_RP_I_SHDW_HDR_LOG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0104h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0104h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0104h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0104h

Figure 9-528. PCIE_CORE_RP_I_SHDW_HDR_LOG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHDW_HDR_LOG_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1460. PCIE_CORE_RP_I_SHDW_HDR_LOG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHDW_HDR_LOG_1	R/W	0h	<p>The value here will be reflected in the target function's header log register when f/w sets any bit in the shadow error register.</p> <p>If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set.</p> <p>This register holds [63:32] value of the TLP header.</p>

9.5.140 PCIE_CORE_RP_I_SHDW_HDR_LOG_2_REG Register (Offset = 00100108h) [reset = 0h]

PCIE_CORE_RP_I_SHDW_HDR_LOG_2_REG is shown in [Figure 9-529](#) and described in [Table 9-1462](#).

Return to [Summary Table](#).

N/A

Table 9-1461.
PCIE_CORE_RP_I_SHDW_HDR_LOG_2_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0108h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0108h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0108h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0108h

Figure 9-529. PCIE_CORE_RP_I_SHDW_HDR_LOG_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHDW_HDR_LOG_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1462. PCIE_CORE_RP_I_SHDW_HDR_LOG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHDW_HDR_LOG_2	R/W	0h	<p>The value here will be reflected in the target function's header log register when f/w sets any bit in the shadow error register.</p> <p>If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set.</p> <p>This register holds [95:64] value of the TLP header.</p>

9.5.141 PCIE_CORE_RP_I_SHDW_HDR_LOG_3_REG Register (Offset = 0010010Ch) [reset = 0h]

PCIE_CORE_RP_I_SHDW_HDR_LOG_3_REG is shown in [Figure 9-530](#) and described in [Table 9-1464](#).

Return to [Summary Table](#).

N/A

Table 9-1463.
PCIE_CORE_RP_I_SHDW_HDR_LOG_3_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 010Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 010Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 010Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 010Ch

Figure 9-530. PCIE_CORE_RP_I_SHDW_HDR_LOG_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHDW_HDR_LOG_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1464. PCIE_CORE_RP_I_SHDW_HDR_LOG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHDW_HDR_LOG_3	R/W	0h	<p>The value here will be reflected in the target function's header log register when f/w sets any bit in the shadow error register.</p> <p>If the header log is already set in the function's AER space, the value here may not get written and a header log overflow bit would get set.</p> <p>This register holds [127:96] value of the TLP header.</p>

9.5.142 PCIE_CORE_RP_I_SHDW_FUNC_NUM_REG Register (Offset = 00100110h) [reset = 0h]

PCIE_CORE_RP_I_SHDW_FUNC_NUM_REG is shown in [Figure 9-531](#) and described in [Table 9-1466](#).

Return to [Summary Table](#).

N/A

Table 9-1465.
PCIE_CORE_RP_I_SHDW_FUNC_NUM_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0110h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0110h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0110h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0110h

Figure 9-531. PCIE_CORE_RP_I_SHDW_FUNC_NUM_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0								SHDW_FUNC_NUM							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1466. PCIE_CORE_RP_I_SHDW_FUNC_NUM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R0	R	0h	Reserved
7-0	SHDW_FUNC_NUM	R/W	0h	The value here will be the target function number when f/w sets any bit in the shadow error register.

9.5.143 PCIE_CORE_RP_I_SHDW_UR_ERR_REG Register (Offset = 00100114h) [reset = 0h]

PCIE_CORE_RP_I_SHDW_UR_ERR_REG is shown in [Figure 9-532](#) and described in [Table 9-1468](#).

Return to [Summary Table](#).

N/A

Table 9-1467.
PCIE_CORE_RP_I_SHDW_UR_ERR_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0114h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0114h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0114h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0114h

Figure 9-532. PCIE_CORE_RP_I_SHDW_UR_ERR_REG Register

31	30	29	28	27	26	25	24
R0							
R-0h							
23	22	21	20	19	18	17	16
R0							
R-0h							
15	14	13	12	11	10	9	8
R0							
R-0h							
7	6	5	4	3	2	1	0
R0						NP_UR_ERR	P_UR_ERR
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1468. PCIE_CORE_RP_I_SHDW_UR_ERR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	R0	R	0h	Reserved
1	NP_UR_ERR	R/W	0h	If this bit is set, the corresponding non-posted UR error bits will be set in the AER and device status registers of the target function.
0	P_UR_ERR	R/W	0h	If this bit is set, the corresponding posted UR error bits will be set in the AER and device status registers of the target function.

9.5.144 PCIE_CORE_RP_I_PM_CLK_FREQUENCY_REG Register (Offset = 00100140h) [reset = 19h]

PCIE_CORE_RP_I_PM_CLK_FREQUENCY_REG is shown in [Figure 9-533](#) and described in [Table 9-1470](#).

Return to [Summary Table](#).

N/A

Table 9-1469.
PCIE_CORE_RP_I_PM_CLK_FREQUENCY_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0140h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0140h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0140h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0140h

Figure 9-533. PCIE_CORE_RP_I_PM_CLK_FREQUENCY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0														PMCLKFRQ																	
R-0h														R/W-19h																	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1470. PCIE_CORE_RP_I_PM_CLK_FREQUENCY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R0	R	0h	Reserved
7-0	PMCLKFRQ	R/W	19h	<p>This field specifies the PM_CLK Frequency selected.</p> <p>The encoding is described below:</p> <p>000000: Reserved</p> <p>000001: Reserved</p> <p>000010: PM_CLK is 2 MHz</p> <p>000011: PM_CLK is 3 MHz</p> <p>000100: PM_CLK is 4 MHz</p> <p>000101: PM_CLK is 5 MHz</p> <p>..</p> <p>111010: PM_CLK is 58 MHz</p> <p>111011: PM_CLK is 59 MHz</p> <p>111100: PM_CLK is 60 MHz</p> <p>111101 : Reserved</p> <p>111110 : Reserved</p> <p>111111 : Reserved</p> <p>.</p>

9.5.145 PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN1_REG Register (Offset = 00100144h) [reset = 0h]

PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN1_REG is shown in [Figure 9-534](#) and described in [Table 9-1472](#).

Return to [Summary Table](#).

N/A

Table 9-1471.
PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0144h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0144h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0144h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0144h

Figure 9-534. PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLPCNT1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1472. PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DLLPCNT1	R	0h	Reflects the total number of DLLPs received by the Controller at GEN1 speed.

9.5.146 PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN2_REG Register (Offset = 00100148h) [reset = 0h]

PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN2_REG is shown in [Figure 9-535](#) and described in [Table 9-1474](#).

Return to [Summary Table](#).

N/A

Table 9-1473.
PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN2_R
EG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0148h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0148h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0148h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0148h

Figure 9-535. PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLPCNT2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1474. PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DLLPCNT2	R	0h	Reflects the total number of DLLPs received by the Controller at GEN2 speed.

9.5.147 PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN3_REG Register (Offset = 0010014Ch) [reset = 0h]

PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN3_REG is shown in [Figure 9-536](#) and described in [Table 9-1476](#).

Return to [Summary Table](#).

N/A

Table 9-1475.
PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN3_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 014Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 014Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 014Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 014Ch

Figure 9-536. PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLPCNT3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1476. PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DLLPCNT3	R	0h	Reflects the total number of DLLPs received by the Controller at GEN3 speed.

9.5.148 PCIe_CORE_RP_I_DEBUG_DLLP_COUNT_GEN4_REG Register (Offset = 00100150h) [reset = 0h]

PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN4_REG is shown in [Figure 9-537](#) and described in [Table 9-1478](#).

Return to [Summary Table](#).

N/A

Table 9-1477.
PCIE_CORE_RP_I_DEBUG_DLLP_COUNT_GEN4_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0150h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0150h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0150h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0150h

Figure 9-537. PCIe_CORE_RP_I_DEBUG_DLLP_COUNT_GEN4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLLPCNT4																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1478. PCIe_CORE_RP_I_DEBUG_DLLP_COUNT_GEN4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DLLPCNT4	R	0h	Reflects the total number of DLLPs received by the Controller at GEN4 speed.

9.5.149 PCIE_CORE_RP_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register (Offset = 00100158h) [reset = X]

PCIE_CORE_RP_I_VENDOR_DEFINED_MESSAGE_TAG_REG is shown in [Figure 9-538](#) and described in [Table 9-1480](#).

Return to [Summary Table](#).

N/A

Table 9-1479.
PCIE_CORE_RP_I_VENDOR_DEFINED_MESSAGE_TAG_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0158h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0158h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0158h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0158h

Figure 9-538. PCIE_CORE_RP_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VDMTAG							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1480. PCIE_CORE_RP_I_VENDOR_DEFINED_MESSAGE_TAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	VDMTAG	R/W	0h	The Controller will use the tag programed in this register for all Outbound Vendor Defined Messages.

9.5.150 PCIe_CORE_RP_I_NEGOTIATED_LANE_MAP_REG Register (Offset = 00100200h) [reset = 0h]

PCIE_CORE_RP_I_NEGOTIATED_LANE_MAP_REG is shown in [Figure 9-539](#) and described in [Table 9-1482](#).

Return to [Summary Table](#).

N/A

Table 9-1481.
PCIE_CORE_RP_I_NEGOTIATED_LANE_MAP_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0200h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0200h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0200h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0200h

Figure 9-539. PCIe_CORE_RP_I_NEGOTIATED_LANE_MAP_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R71															LRS
R-0h															R-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R70															NLM
R-0h															R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-1482. PCIe_CORE_RP_I_NEGOTIATED_LANE_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	R71	R	0h	Reserved
16	LRS	R	0h	This bit set by the Controller at the end of link training if the LTSSM had to reverse the lane numbers to form the link.
15-2	R70	R	0h	Reserved
1-0	NLM	R	0h	Bit i of this field is set to 1 at the end of link training if Lane i is part of the PCIe link. The value of this field is valid only when the link is in PCIe_CORE_RP_L0 or L0s states.

9.5.151 PCIE_CORE_RP_I_RECEIVE_FTS_COUNT_REG Register (Offset = 00100204h) [reset = 0h]

PCIE_CORE_RP_I_RECEIVE_FTS_COUNT_REG is shown in [Figure 9-540](#) and described in [Table 9-1484](#).

Return to [Summary Table](#).

N/A

Table 9-1483.
PCIE_CORE_RP_I_RECEIVE_FTS_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0204h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0204h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0204h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0204h

Figure 9-540. PCIE_CORE_RP_I_RECEIVE_FTS_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R24								RFC16S								RFC8S								RFC5S							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-1484. PCIE_CORE_RP_I_RECEIVE_FTS_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R24	R	0h	Reserved
23-16	RFC16S	R	0h	FTS count received from the other side during link training for use at the 16 GT/s link speed. The Controller transmits this many FTS sequences while exiting the LOS state, when operating at the 16 GT/s speed.
15-8	RFC8S	R	0h	FTS count received from the other side during link training for use at the 8 GT/s link speed. The Controller transmits this many FTS sequences while exiting the LOS state, when operating at the 8 GT/s speed.
7-0	RFC5S	R	0h	FTS count received from the other side during link training for use at the 5 GT/s link speed. The Controller transmits this many FTS sequences while exiting the LOS state, when operating at the 5 GT/s speed.

9.5.152 PCIe_CORE_RP_I_DEBUG_MUX_CONTROL_REG Register (Offset = 00100208h) [reset = 80000000h]

PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_REG is shown in [Figure 9-541](#) and described in [Table 9-1486](#).

Return to [Summary Table](#).

N/A

Table 9-1485.
PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0208h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0208h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0208h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0208h

Figure 9-541. PCIe_CORE_RP_I_DEBUG_MUX_CONTROL_REG Register

31	30	29	28	27	26	25	24
EFSRTCA	DOC	DFCUT	DEI	DGLUS	IEDPPE	ESPC	EFLT
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DLUC	DLRFE	DSHEC	DCIVMC	DIOAEFC	DOASFC	HPRSUPP	AWRPRI
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
FDS	DSSPLM	R1313	R1212	R1111	R1010	MSIVCMS	DIDBOC
R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
R77	R6				MS		
R/W-0h	R-0h				R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1486. PCIe_CORE_RP_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EFSRTCA	R/W	1h	Setting this bit to 0 causes all the enabled Functions to report an error when a Type-1 configuration access is received by the Controller, targeted at any Function. Setting it to 1 limits the error reporting to the type-0 Function whose number matches with the Function number specified in the request. If the Function number in the request refers to an unimplemented or disabled Function, all enabled Functions report the error regardless of the setting of this bit.
30	DOC	R/W	0h	Setting this bit to 1 disables the ordering check in the Controller between Completions and Posted requests received from the link.

Table 9-1486. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	DFCUT	R/W	0h	<p>When this bit is 0, the Controller will time out and re-train the link when no Flow Control Update DLLPs are received from the link within an interval of 128 us. Setting this bit to 1 disables this timeout.</p> <p>When the advertised receive credit of the link partner is infinity for the header and payload of all credit types, this timeout is always suppressed.</p> <p>The setting of this bit has no effect in this case.</p> <p>This bit should not be set during normal operation, but is useful for testing.</p>
28	DEI	R/W	0h	<p>Setting this bit to 1 disables the inferring of electrical idle in the PCIE_CORE_RP_L0 state.</p> <p>Electrical idle is inferred when no flow control updates and no SKP sequences are received within an interval of 128 us.</p> <p>This bit should not be set during normal operation, but is useful for testing.</p>
27	DGLUS	R/W	0h	<p>Setting this bit to 1 disables the update of the LFSRs in the Gen3 descramblers of the Controller, from the values received in SKP sequences.</p> <p>This bit should not be set during normal operation, but is useful for testing.</p>
26	IEDPPE	R/W	0h	<p>When set to 1, this bit inverts the parity bits generated by the Controller for end-to-end data protection.</p> <p>This will result in the inversion of parity bits for data payloads delivered through the HAL interface.</p> <p>This bit is to be used for diagnostics only, and should not be set during normal operation.</p>
25	ESPC	R/W	0h	<p>When this bit is set to 1, the Controller will capture the Slot Power Limit Value and Slot Power Limit Scale parameters from a Set_Slot_Power_Limit message received in the Device Capabilities Register.</p> <p>When this bit is 0, the capture is disabled.</p> <p>This bit is valid only when the Controller is configured as an EndPoint. It has no effect when the Controller is a Root Complex.</p>

Table 9-1486. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	EFLT	R/W	0h	<p>This bit is provided to shorten the link training time to facilitate fast simulation of the design, especially at the gate level.</p> <p>Enabling this bit has the following effects:</p> <ol style="list-style-type: none"> 1. The 1 ms, 2 ms, 12 ms, 24 ms, 32 ms and 48 ms timeout intervals in the LTSSM are shortened by a factor of 500. 2. In the Polling.Active state of the LTSSM, only 16 training sequences are required to be transmitted [Instead of 1024] to make the transition to the Configuration state. <p>This bit should not be set during normal operation of the Controller.</p>
23	DLUC	R/W	0h	<p>The user may set this bit to turn off the link upconfigure capability of the Controller.</p> <p>Setting this bit prevents the Controller from advertising the link upconfigure capability in training sequences transmitted in the Configuration.Complete state.</p> <p>In addition, setting this bit causes the Controller to put the unused lanes into Turn Off mode.</p> <p>When disable_link_upconfigure_capability==</p> <ol style="list-style-type: none"> 1: Controller drives PIPE_TX_ELEC_IDLE==1 AND PIPE_TX_COMPLIANCE==1 for the Unused upper lanes. The Unused upper lanes are put into Turn Off mode by the PHY as per PIPE specification. <p>When disable_link_upconfigure_capability==</p> <ol style="list-style-type: none"> 0: Controller drives PIPE_TX_ELEC_IDLE==1 AND PIPE_TX_COMPLIANCE==0 for the Unused upper lanes. The Unused upper lanes are put into Electrical Idle by the PHY.
22	DLRFE	R/W	0h	<p>When this bit is 1, the Controller will not transition its LTSSM into the Recovery state when it detects a Framing Error at 8 GT/s or 16 GT/s speed [as defined in Section 4.2.2.3.3 of the PCIe Base Specification 3.0.</p> <p>This bit must normally be set to 0 so that a Framing Error will cause the LTSSM to enter Recovery.</p> <p>The setting of this bit has no effect on the operation of the Controller at 2.5 and 5 GT/s speeds.</p>
21	DSHEC	R/W	0h	<p>When this bit is 0, the Controller will signal a framing error if it detects a sync header error in the received blocks at 8 GT/s or 16 GT/s speed [A 00 or 11 binary setting of the sync header on the received blocks in any lane constitutes a framing error].</p> <p>Setting this bit to 1 suppresses this error check.</p> <p>This bit should normally be set to 0, as the sync header check is mandatory in the PCIe 3.0 Specifications.</p>

Table 9-1486. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	DCIVMC	R/W	0h	When this bit is 1, the Controller will not check for invalid message codes. This bit should normally set to 0, as the invalid message code checking is mandatory in the PCIe 3.0 specifications.
19	DIOAEFC	R/W	0h	When this bit is 1, the Controller will not check for illegal OS after EDS as part of Gen3 Framing Error Checks. This bit should normally set to 0, as this is a mandatory Gen3 Framing Error check in the PCIe 3.0 specifications.
18	DOASFC	R/W	0h	When this bit is 1, the Controller will not check for OS after SKIP OS as part of Gen3 Framing Error Checks. This bit should normally set to 0, as this is a mandatory Gen3 Framing Error check in the PCIe 3.0 specifications.
17	HPRSUPP	R/W	0h	When this bit is 1, data path parity check is disabled on the TX side of the Controller.
16	AWRPRI	R/W	0h	When this bit is 1, the AXI bridge places a write request on the HAL Master interface in preference over a read request if both AXI write and AXI read requests are available to be asserted on the same clock cycle.
15	FDS	R/W	0h	Disable Scrambling/Descrambling in Gen1/Gen2.
14	DSSPLM	R/W	0h	Disable sending Set Slot Power Limit Message if the Slot Capabilitied register is configured
13	R1313	R	0h	N/A
12	R1212	R	0h	N/A
11	R1111	R/W	0h	When this bit is 1, Disable Client TX MUX Completion and PNP request arbitartion,roundrobin priority logic added to prevent PNP requests from starving when completions are present
10	R1010	R	0h	Reserved
9	MSIVCMS	R/W	0h	Sets the mode of generating MSI_VECTOR_COUNT output for all functions. 0 - MSI_VECTOR_COUNT always outputs the configured value of MSI Multiple Message Enable [2:0] register. 1 - MSI_VECTOR_COUNT outputs the lesser of the MSI Multiple Message Enable [2:0] and MSI Multiple Message Capable [2:0] This mode can be used to handle any programming error form the Host software.
8	DIDBOC	R/W	0h	Setting this bit to 1 disables the ID Based Ordering check in the Controller between Completions and Posted requests received from the link.
7	R77	R/W	0h	This bit should be set to 0 for backward compatibility.
6-5	R6	R	0h	N/A

Table 9-1486. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	MS	R/W	0h	<p>Bits</p> <p>4:3 select the module and bits</p> <p>2:0 select the group of signals within the module that are driven on the debug bus.</p> <p>The assignments of signals on the debug outputs of the Controller are given in Appendix B.</p>

9.5.153 PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGISTER Register (Offset = 0010020Ch) [reset = 0h]

PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGISTER is shown in [Figure 9-542](#) and described in [Table 9-1488](#).

Return to [Summary Table](#).

N/A

Table 9-1487.
PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGIS
TER Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 020Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 020Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 020Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 020Ch

Figure 9-542. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGISTER Register

31	30	29	28	27	26	25	24
REORDER_ER_UN	AXISLAVE_WFIFO_ER_UN	AXIMASTER_RFIFO_ER_UN	AXIMASTER_DIB_ER_UN	R27		MSIXMSKST	R24
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h		R/W1C-0h	R-0h
23	22	21	20	19	18	17	16
R24		HAWCD	R22	MMVC	UTC	EEPE	R13
R-0h		R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h
15	14	13	12	11	10	9	8
	R13		R12	CT	FCE	UCR	MTR
	R-0h		R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
PE	RTR	RT	CRFO	PRFO	RRPE	CRFPE	PRFPE
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1488. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REORDER_ER_UN	R/W1C	0h	This indicates an uncorrectbale axi slave reorder ram parity/ecc error
30	AXISLAVE_WFIFO_ER_UN	R/W1C	0h	This indicates an uncorrectbale axi slave write fifo ram parity/ecc error
29	AXIMASTER_RFIFO_ER_UN	R/W1C	0h	This indicates an uncorrectbale axi master write fifo ram parity/ecc error
28	AXIMASTER_DIB_ER_UN	R/W1C	0h	This indicates an uncorrectbale axi slave write fifo ram parity/ecc error
27-26	R27	R	0h	Reserved
25	MSIXMSKST	R/W1C	0h	This interrupt status bit is used when MSIX Function Mask Enhanced Interrupt Enable bit is set to 0 by the User. This status bit indicates that the MSIX Function Mask bit of any function, PF or VF, was programmed or configured by Local Firmware Or Host SW.
24-22	R24	R	0h	Reserved

**Table 9-1488. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGISTER Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
21	HAWCD	R/W1C	0h	This interrupt status bit indicates that the Host toggled the Hardware Autonomous Width Change bit in the Link Control Register through a Config Write. Upon this interrupt, the Client firmware must read the Link Control Register to check the value set by Host in the Hardware Autonomous Width Change bit. The Host Software may disable autonomous width change by setting Hardware Autonomous Width Disable bit in the Link Control register. If disabled by the Host and if the Endpoint firmware had initiated an autonomous width downsizing prior to this interrupt, then the local Client firmware is responsible to upconfigure the Link to go to its full functional width by initiating the link_upconfigure_retrain_link within 1 ms of this interrupt.
20	R22	R	0h	Reserved
19	MMVC	R/W1C	0h	This status bit is set whenever the MSI mask register value in the MSI capability register changes value in ANY of the functions in the controller
18	UTC	R/W1C	0h	Unmapped TC error.
17	EEPE	R/W1C	0h	The Controller detected an End to End Parity Error
16-13	R13	R	0h	Reserved
12	R12	R	0h	Reserved
11	CT	R/W1C	0h	A request timed out waiting for completion.
10	FCE	R/W1C	0h	An error was observed in the flow control advertisements from the other side.
9	UCR	R/W1C	0h	Unexpected Completion received from the link.
8	MTR	R/W1C	0h	Malformed TLP received from the link.
7	PE	R/W1C	0h	Phy error detected on receive side. This bit is set when an error is detected in the receive side of the Physical Layer of the Controller [e.g. a bit error or coding violation]. This bit is set upon any of the following errors: [1] PHY reported 8B10B error, Disparity Error, Elastic Buffer Overflow Error, Underflow Error [2] GEN3 TLP, DLLP Framing Errors [3] OS Block Received Without EDS [4] Data Block Received After EDS [5] Illegal OS Block After EDS [6] OS Block Received After SKIP OS [7] OS Block Received After SDS [8] Sync Header Error [9] Loss of Gen3 Block Alignment This error is not Function-specific..
6	RTR	R/W1C	0h	Replay timer rolled over after 4 transmissions of the same TLP.
5	RT	R/W1C	0h	Replay timer timed out
4	CRFO	R/W1C	0h	Overflow occurred in the Completion Receive FIFO.
3	PRFO	R/W1C	0h	Overflow occurred in the PNP Receive FIFO.

Table 9-1488. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_REGISTER Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
2	RRPE	R/W1C	0h	Parity error detected while reading from Replay Buffer RAM.
1	CRFPE	R/W1C	0h	Parity error detected while reading from the Completion Receive FIFO RAM.
0	PRFPE	R/W1C	0h	Parity error detected while reading from the PNP Receive FIFO RAM.

9.5.154 PCIe_CORE_RP_I_LOCAL_INTRPT_MASK_REG Register (Offset = 00100210h) [reset = 022E0FFFh]

PCIe_CORE_RP_I_LOCAL_INTRPT_MASK_REG is shown in [Figure 9-543](#) and described in [Table 9-1490](#).

Return to [Summary Table](#).

N/A

Table 9-1489.
PCIe_CORE_RP_I_LOCAL_INTRPT_MASK_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0210h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0210h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0210h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0210h

Figure 9-543. PCIe_CORE_RP_I_LOCAL_INTRPT_MASK_REG Register

31	30	29	28	27	26	25	24
REORDER_ER_UN	AXISLAVE_WFIFO_ER_UN	AXIMASTER_RFIFO_ER_UN	AXIMASTER_DIB_ER_UN	R27		MSIXMSK	R24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h
23	22	21	20	19	18	17	16
R24		HAWCD	R45	MMVC	UTC	EEPE	R13
R-0h		R/W-1h	R-0h	R/W-1h	R/W-1h	R/W-1h	R-0h
15	14	13	12	11	10	9	8
R13			R12	CT	FCE	UCR	MTR
R-0h			R-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
PE	RTR	RT	CRFO	PRFO	RRPE	CRFPE	PRFPE
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1490. PCIe_CORE_RP_I_LOCAL_INTRPT_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	REORDER_ER_UN	R/W	0h	mask for uncorrectbale axi slave reorder ram parity/ecc error
30	AXISLAVE_WFIFO_ER_UN	R/W	0h	mask for uncorrectbale axi slave write fifo ram parity/ecc error
29	AXIMASTER_RFIFO_ER_UN	R/W	0h	mask for uncorrectbale axi master write fifo ram parity/ecc error
28	AXIMASTER_DIB_ER_UN	R/W	0h	mask for uncorrectbale axi slave write fifo ram parity/ecc error
27-26	R27	R	0h	Reserved
25	MSIXMSK	R/W	1h	This bit is used to mask interrupt that indicates that the MSIX Function Mask bit of any function, PF or VF, was programmed or configured by Local Firmware Or Host SW.
24-22	R24	R	0h	Reserved
21	HAWCD	R/W	1h	This bit is used to mask interrupt that indicates that the Host toggled the Hardware Autonomous Width Change in the Endpoint Link Control Register through a Config Write.
20	R45	R	0h	Reserved

Table 9-1490. PCIE_CORE_RP_I_LOCAL_INTRPT_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	MMVC	R/W	1h	MSI mask register value in the MSI capability register changes value in ANY of the functions in the controller
18	UTC	R/W	1h	Unmapped TC error
17	EEPE	R/W	1h	The Controller detected an End to End Parity Error
16-13	R13	R	0h	Reserved
12	R12	R	0h	Reserved
11	CT	R/W	1h	A request timed out waiting for completion.
10	FCE	R/W	1h	An error was observed in the flow control advertisements from the other side.
9	UCR	R/W	1h	Unexpected Completion received from the link.
8	MTR	R/W	1h	Malformed TLP received from the link.
7	PE	R/W	1h	Phy error detected on receive side.
6	RTR	R/W	1h	Replay timer rolled over after 4 transmissions of the same TLP.
5	RT	R/W	1h	Replay timer timed out
4	CRFO	R/W	1h	Overflow occurred in the Completion Receive FIFO.
3	PRFO	R/W	1h	Overflow occurred in the PNP Receive FIFO.
2	RRPE	R/W	1h	Parity error detected while reading from Replay Buffer RAM.
1	CRFPE	R/W	1h	Parity error detected while reading from the Completion Receive FIFO RAM.
0	PRFPE	R/W	1h	Parity error detected while reading from the PNP Receive FIFO RAM.

9.5.155 PCIE_CORE_RP_I_LCRC_ERR_COUNT_REG Register (Offset = 00100214h) [reset = 0h]

PCIE_CORE_RP_I_LCRC_ERR_COUNT_REG is shown in [Figure 9-544](#) and described in [Table 9-1492](#).

Return to [Summary Table](#).

N/A

Table 9-1491.
PCIE_CORE_RP_I_LCRC_ERR_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0214h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0214h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0214h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0214h

Figure 9-544. PCIE_CORE_RP_I_LCRC_ERR_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R11																LEC															
R-0h																R/W1C-0h															

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1492. PCIE_CORE_RP_I_LCRC_ERR_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R11	R	0h	Reserved
15-0	LEC	R/W1C	0h	Number of TLPs received with LCRC errors.

9.5.156 PCIE_CORE_RP_I_ECC_CORR_ERR_COUNT_REG Register (Offset = 00100218h) [reset = 0h]

PCIE_CORE_RP_I_ECC_CORR_ERR_COUNT_REG is shown in [Figure 9-545](#) and described in [Table 9-1494](#).

Return to [Summary Table](#).

N/A

Table 9-1493.
PCIE_CORE_RP_I_ECC_CORR_ERR_COUNT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0218h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0218h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0218h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0218h

Figure 9-545. PCIE_CORE_RP_I_ECC_CORR_ERR_COUNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R12								RRCER								SFCER								PFCER							
R/W1C-0h								R/W1C-0h								R/W1C-0h								R/W1C-0h							

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1494. PCIE_CORE_RP_I_ECC_CORR_ERR_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	R12	R/W1C	0h	Number of correctable errors detected while reading from the TPH Steering Tag RAM. This is an 8-bit saturating counter that can be cleared by writing all 1s into it.
23-16	RRCER	R/W1C	0h	Number of correctable errors detected while reading from the Replay Buffer RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
15-8	SFCER	R/W1C	0h	Number of correctable errors detected while reading from the SC FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
7-0	PFCER	R/W1C	0h	Number of correctable errors detected while reading from the PNP FIFO RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.

9.5.157 PCIe_CORE_RP_I_LTR_SNOOP_LAT_REG Register (Offset = 0010021Ch) [reset = 0h]

PCIe_CORE_RP_I_LTR_SNOOP_LAT_REG is shown in [Figure 9-546](#) and described in [Table 9-1496](#).

Return to [Summary Table](#).

N/A

Table 9-1495.
PCIe_CORE_RP_I_LTR_SNOOP_LAT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 021Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 021Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 021Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 021Ch

Figure 9-546. PCIe_CORE_RP_I_LTR_SNOOP_LAT_REG Register

31	30	29	28	27	26	25	24
SL	R13		SLS		SLV		
R/W-0h	R-0h		R/W-0h		R/W-0h		
23	22	21	20	19	18	17	16
SLV							
R/W-0h							
15	14	13	12	11	10	9	8
NSLR	R12		NSLS		NSLV		
R/W-0h	R-0h		R/W-0h		R/W-0h		
7	6	5	4	3	2	1	0
NSLV							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1496. PCIe_CORE_RP_I_LTR_SNOOP_LAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SL	R/W	0h	The client software must set this bit to 1 to set the Snoop Latency Requirement bit in the LTR message to be sent.
30-29	R13	R	0h	Reserved
28-26	SLS	R/W	0h	The client software must program this field with the value to be sent in the Snoop Latency Scale field of the LTR message.
25-16	SLV	R/W	0h	The client software must program this field with the value to be sent in the Snoop Latency Value field of the LTR message.
15	NSLR	R/W	0h	The client software must set this bit to 1 to set the No-Snoop Latency Requirement bit in the LTR message to be sent.
14-13	R12	R	0h	N/A
12-10	NSLS	R/W	0h	The client software must program this field with the value to be sent in the No-Snoop Latency Scale field of the LTR message.

Table 9-1496. PCIE_CORE_RP_I_LTR_SNOOP_LAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	NSLV	R/W	0h	The client software must program this field with the value to be sent in the No-Snoop Latency Value field of the LTR message.

9.5.158 PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_REG Register (Offset = 00100220h) [reset = X]

PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_REG is shown in [Figure 9-547](#) and described in [Table 9-1498](#).

Return to [Summary Table](#).

N/A

Table 9-1497.
PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0220h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0220h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0220h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0220h

Figure 9-547. PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			TMFPSC	TMLMET	SLM	MLI	
R/W-X			R/W-1h	R/W-1h	R-0h	R/W-FAh	
7	6	5	4	3	2	1	0
MLI							
R/W-FAh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1498. PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	

Table 9-1498. PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	TMFPSC	R/W	1h	<p>When this bit is set to 1, the Controller will automatically transmit an LTR message when all the Functions in the Controller have transitioned to a non-D0 power state, provided that the following conditions are both true:</p> <ol style="list-style-type: none"> 1. The Controller sent at least one LTR message since the Data Link layer last transitioned from down to up state. 2. The most recent LTR message transmitted by the Controller had as least one of the Requirement bits set. <p>The Controller will set the Requirement bits in this LTR message to 0.</p> <p>When this bit 12 is 0, the Controller will not, by itself, send any LTR messages in response to Function Power State changes.</p> <p>Client logic may monitor the FUNCTION_POWER_STATE outputs of the Controller and transmit LTR messages through the master interface, in response to changes in their states.</p>
11	TMLMET	R/W	1h	<p>When this bit is set to 1, the Controller will automatically transmit an LTR message whenever the LTR Mechanism Enable bit in the Device Control 2 Register changes from 0 to 1, with the parameters specified in the LTR Snoop/No-Snoop Latency Register.</p> <p>When this bit is 1, the Controller will also transmit an LTR message whenever the LTR Mechanism Enable bit is cleared, if the following conditions are both true:</p> <ol style="list-style-type: none"> 1. The Controller sent at least one LTR message since the LTR Mechanism Enable bit was last set. 2. The most recent LTR message transmitted by the Controller had as least one of the Requirement bits set. <p>The Controller will set the Requirement bits in this LTR message to 0.</p> <p>When this bit 11 is 0, the Controller will not, by itself, send any LTR messages in response to state changes of the LTR Mechanism Enable bit.</p> <p>Client logic may monitor the state of the LTR_MECHANISM_ENABLE output of the Controller and transmit LTR messages through the master interface, in response to its state changes.</p>

Table 9-1498. PCIE_CORE_RP_I_LTR_MSG_GEN_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SLM	R	0h	<p>Setting this bit causes the Controller to transmit an LTR message with the parameters specified in the LTR Snoop/No-Snoop Latency Register [Section 8.4.2.9].</p> <p>This bit is cleared by the Controller on transmitting the LTR message, and stays set until then.</p> <p>Client software must read this register and verify that this bit is 0 before setting it again to send a new message.</p> <p>This field becomes writable when LTR mechanism is enabled in device control-2 register.</p>
9-0	MLI	R/W	FAh	<p>This field specifies the minimum spacing between LTR messages transmitted by the Controller in units of microseconds.</p> <p>The PCI Express Specifications recommend sending no more than two LTR messages within a 500 microsecond interval.</p> <p>The Controller will wait for the minimum delay specified by this field after sending an LTR message, before transmitting a new LTR message.</p> <p>NOTE: The LINK can be in low power states[L0s and L1] when send LTR Message is triggered.</p> <p>So, the user has to consider the exit latencies while programming this field.</p> <p>It is recommended to program this field with about 2 us higher than the required interval to account for the L0s/L1 exit latencies.</p>

9.5.159 PCIE_CORE_RP_I_PME_SERVICE_TIMEOUT_DELAY_REG Register (Offset = 00100224h) [reset = 000186A0h]

PCIE_CORE_RP_I_PME_SERVICE_TIMEOUT_DELAY_REG is shown in [Figure 9-548](#) and described in [Table 9-1500](#).

Return to [Summary Table](#).

N/A

Table 9-1499.
PCIE_CORE_RP_I_PME_SERVICE_TIMEOUT_DELAY_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0224h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0224h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0224h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0224h

Figure 9-548. PCIE_CORE_RP_I_PME_SERVICE_TIMEOUT_DELAY_REG Register

31	30	29	28	27	26	25	24
R21							
R-0h							
23	22	21	20	19	18	17	16
R21		DPMOPS		PSTD			
R-0h		R/W-0h		R/W-000186A0h			
15	14	13	12	11	10	9	8
PSTD							
R/W-000186A0h							
7	6	5	4	3	2	1	0
PSTD							
R/W-000186A0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1500. PCIE_CORE_RP_I_PME_SERVICE_TIMEOUT_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	R21	R	0h	Reserved
20	DPMOPS	R/W	0h	When this bit is set, Controller will not automatically send a PME message, when PM Status bit in PMCSR register is set
19-0	PSTD	R/W	000186A0h	Specifies the timeout delay for retransmission of PM_PME messages. The value is in units of microseconds. The actual time elapsed has a +1 microseconds tolerance from the value programmed.

9.5.160 PCIE_CORE_RP_I_ROOT_PORT_REQUESTOR_ID_REG Register (Offset = 00100228h) [reset = 0h]

PCIE_CORE_RP_I_ROOT_PORT_REQUESTOR_ID_REG is shown in [Figure 9-549](#) and described in [Table 9-1502](#).

Return to [Summary Table](#).

N/A

Table 9-1501.
PCIE_CORE_RP_I_ROOT_PORT_REQUESTOR_ID_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0228h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0228h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0228h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0228h

Figure 9-549. PCIE_CORE_RP_I_ROOT_PORT_REQUESTOR_ID_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0																RPRI															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1502. PCIE_CORE_RP_I_ROOT_PORT_REQUESTOR_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R0	R	0h	Reserved
15-0	RPRI	R/W	0h	RID [bus, device and function numbers] for all TLPs internally generated by Root Port

9.5.161 PCIE_CORE_RP_I_EP_BUS_DEVICE_NUMBER_REG Register (Offset = 0010022Ch) [reset = 0h]

PCIE_CORE_RP_I_EP_BUS_DEVICE_NUMBER_REG is shown in [Figure 9-550](#) and described in [Table 9-1504](#).

Return to [Summary Table](#).

N/A

Table 9-1503.
PCIE_CORE_RP_I_EP_BUS_DEVICE_NUMBER_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 022Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 022Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 022Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 022Ch

Figure 9-550. PCIE_CORE_RP_I_EP_BUS_DEVICE_NUMBER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R16																EPBN				R5		EPDN									
R-0h																R-0h				R-0h		R-0h									

LEGEND: R = Read Only; -n = value after reset

Table 9-1504. PCIE_CORE_RP_I_EP_BUS_DEVICE_NUMBER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-8	EPBN	R	0h	Bus Number captured by Function 0 in End Point mode
7-5	R5	R	0h	Reserved
4-0	EPDN	R	0h	Device Number captured by Function 0 in End Point mode

9.5.162 PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG Register (Offset = 00100234h) [reset = 10040850h]

PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG is shown in [Figure 9-551](#) and described in [Table 9-1506](#).

Return to [Summary Table](#).

N/A

Table 9-1505.
PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0234h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0234h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0234h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0234h

Figure 9-551. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG Register

31	30	29	28	27	26	25	24
R31			DFLRTRB	DTAE2EP	R26	MSIXMSKEN	MSIMSKEN
R-0h			R/W-1h	R/W-0h	R-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
VARCCLKEN	MAXNPREQ						
R/W-0h				R/W-20h			
15	14	13	12	11	10	9	8
MAXNPREQ			AXINPSPEN_R SVD	CMPTOADV	PSNADV	MSIPIMS	ENG4REV05
R/W-20h			R-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
BLKALNWIN	BLKALNCHK	ARICAPMOD	ENLNCHK	DISSDSCHK	EXTSNP	DLFFS	
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1506. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	R31	R	0h	Reserved
28	DFLRTRB	R/W	1h	1 : NP Termination due to FLR/Completion Timeout is delayed till the RX Completion FIFO is Empty. 0 : NP Termination due to FLR is done immediately on receiving FLR/Completion Timeout.
27	DTAE2EP	R/W	0h	By default, when End to End Parity error is detected on inbound/outbound data streams, then all the transmitted outbound packets will be Nullified by the Controller. This bit can be used to turn off nullifying Tx packets on End to End Parity Error.
26	R26	R	0h	Reserved

**Table 9-1506. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
25	MSIXMSKEN	R/W	0h	By default, the Controller provides a single status bit when any function's MSIX Function Mask is programmed or configured by Local firmware or Host SW. Controller also implements an enhanced MSIX Function Mask Interrupt mechanism, which provides per-function set/clear status when a function's MSIX Function Mask is updated by SW. This Local Management programmable bit allows user to choose between the Default and Enhanced MSIX Function Mask Change Interrupt mechanisms.
24	MSIMSKEN	R/W	0h	By default, the Controller provides a single status bit when any function's MSI Mask is programmed or configured by Local firmware or Host SW. Controller also implements an enhanced MSI Mask Interrupt mechanism, which provides per-function set/clear status when a function's MSI Mask is updated by SW. This Local Management programmable bit allows user to choose between the Default and Enhanced MSI Mask Change Interrupt mechanisms.
23	VARCCLKEN	R/W	0h	If this bit is set the CORE_CLK input can be driven with Variable Clock depending on the Link Speed, similar to the PIPE_PCLK.
22-13	MAXNPREQ	R/W	20h	The Controller supports 32 outstanding NP requests that can be initiated by the User. However, the number of split completion TLPs that can be stored in the Controller is limited to 128. The Completion FIFO will overflow if more than 128 split completion packets are pending. If the User interface can accept inbound Posted and Completion packets at the same rate as received from PCIe link, then the split completion FIFO will never reach the FULL condition. However, if the User cannot guarantee this, then this register needs to be programmed as described in the Programming Guide section of the Controller User guide. The Controller will limit the maximum number of outstanding NP requests to the value programmed in this register. Example: 8 : Controller will limit maximum number of outstanding NP requests to 8. 0-7 : Reserved Default Value is 32
12	AXINSPEN_RSVD	R	0h	RESERVED
11	CMPTOADV	R/W	1h	As per PCIe specification on Error Signaling, the Requester detecting a Completion Timeout is allowed to handle this as an Advisory Non Fatal Error. 1: Completion Timeout is handled as Advisory Non-Fatal Error. 0: Completion Timeout is handled as normally as a Non-Fatal Error.

**Table 9-1506. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
10	PSNADV	R/W	0h	As per PCIe specification 2.7.2.2, the following Poisoned TLP requests must be handled as Uncorrectable and not as Advisory: I/O Write Request, Memory Write Request, or non-vendor-defined Message with data that target a Control structure. Since it is not possible for the Controller to determine if the target is a Control or a non-Control structure, the Controller implements this bit for the user to determine the required handling. 1: Poisoned TLP of type IOWr, MemWr, MsgD will be handled as Advisory Non-Fatal Error. 0: Poisoned TLP of type IOWr, MemWr, MsgD will be handled as Uncorrectable Error. Note: Poisoned CpID will always be reported as Advisory Non-Fatal and is not controlled by this register setting.
9	MSIPIMS	R/W	0h	If the Client wishes to use the MSI_PENDING_STATUS_IN Signal to Update the MSI pending Bits register, this bit needs to be set to 1. Otherwise the Pending Bits register is updated via the APB Interface
8	ENG4REV05	R/W	0h	When operating in Gen4 16GT/s , This Enables Gen4 Spec Revision 0.5 EIEOS and SKP features. When disabled, the Gen4 1.0 features are enabled, by default this bit is ZERO. 1: Enable Gen4 0.5 Features 0: Disable Gen4 0.5 Features [This enabled the Gen4 1.0 Features] .
7-6	BLKALNWIN	R/W	1h	When in the data stream at Gen3 or higher speeds, the pipe_rx_valid is asserted by the PHY. If the block alignment is lost, then the PHY may deassert pipe_rx_valid. Controller reports loss of block alignment if pipe_rx_valid or pipe_rx_data_valid=0 for a period consecutive clock cycles as programmed in this field. 00: 8 CORE_CLK cycles 01: 16 CORE_CLK cycles 10: 64 CORE_CLK cycles 11: 256 CORE_CLK cycles
5	BLKALNCHK	R/W	0h	When in the data stream at Gen3 or higher speeds, the pipe_rx_valid is asserted by the PHY. If the block alignment is lost, then the PHY may deassert pipe_rx_valid. Block Alignment may be lost if the received sync header is invalid. Controller supports detecting loss of block alignment while in a data stream in Gen3. 0: Enable check for loss of Gen3 Block Alignment during data stream. 1: Disable check for loss of Gen3 Block Alignment.

**Table 9-1506. PCIE_CORE_RP_I_DEBUG_MUX_CONTROL_2_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	ARICAPMOD	R/W	1h	As per SR IOC specification, ARI Capable Hierarchy bit is only present in the lowest numbered PF of a Device. The Controller has two modes to determine the lowest numbered PF. 0: the first PF which is enabled [PF0] is taken as the lowest numbered PF. 1: the first PF which has a non-zero TOTAL_VF_COUNT field is taken as the lowest numbered PF.[Default Mode]
3	ENLNCHK	R/W	0h	As per PCIe specification, LTSSM should transition to Disabled after any Lanes that are transmitting TS1 Ordered Sets receive two consecutive TS1 Ordered Sets with the Disable Link bit asserted. Similarly, LTSSM should transition to Loopback after all Lanes that are transmitting TS1 Ordered Sets, that are also receiving TS1 Ordered Sets, receive the Loopback bit asserted in two consecutive TS1 Ordered Sets. Controller ignores the Link and Lane Number in the Received TS1s with Loopback/Disable bit set. Setting this bit to 1 turns on the check for link number [assigned by RC in Recovery.Idle] and lane number [PAD in Config.LW.Start or as assigned by RC in Recovery.Idle]. This bit is recommended to be kept at the default value of 0.
2	DISSDSCHK	R/W	0h	As per PCIe specification, When using 128b/130b encoding, next state is PCIE_CORE_RP_L0 if eight consecutive Symbol Times of Idle data are received on all configured Lanes. The Controller checks to ensure that the Idle symbols of data are received in Data Blocks after SDS OS. This check is enabled by default. Setting this bit to 1 turns off this check. This bit is recommended to be kept at the default value of 0.
1	EXTSNP	R/W	0h	This bit can be set if an extra clock cycle is required by the Client Application logic to respond with the Read Data on Configuration Snoop Interface. Please refer to the user guide section on Configuration Snoop Interface for timing diagrams.
0	DLFFS	R/W	0h	As per PIPE 4.2 specification, the LOCALLF, LOCALFS outputs from PHY can be sampled uponf PHYSTATUS pulse after Reset# OR upon the first PHYSTATUS pulse after speed change to GEN3. This bit can be set to 1 to disable sampling after speed change to GEN3 or higher

9.5.163 PCIE_CORE_RP_I_PHY_STATUS_1_REG Register (Offset = 00100238h) [reset = 0h]

PCIE_CORE_RP_I_PHY_STATUS_1_REG is shown in [Figure 9-552](#) and described in [Table 9-1508](#).

Return to [Summary Table](#).

N/A

Table 9-1507.
PCIE_CORE_RP_I_PHY_STATUS_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0238h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0238h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0238h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0238h

Figure 9-552. PCIE_CORE_RP_I_PHY_STATUS_1_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							LOSBLKALN
R-0h							R/W1C-0h
7	6	5	4	3	2	1	0
INVSYNHR	OSAFSDS	G3FRERR	OSWOEDS	DATEDS	ILOSEDS	OSASKP	TLPPHYER
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1508. PCIE_CORE_RP_I_PHY_STATUS_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	R31	R	0h	Reserved
8	LOSBLKALN	R/W1C	0h	This bit is set if the PHY Loses Block Alignment during data stream. This is detected based upon an unexpected PIPE_RX_VALID input deassertion during data stream. Write a 1 to clear this error.
7	INVSYNHR	R/W1C	0h	This bit is set if an invalid Sync Header is detected. 00 and 11 are Invalid Sync Headers. Write a 1 to clear this error.
6	OSAFSDS	R/W1C	0h	This bit is set if an SDS is received after an SDS. This is a framing error. Write a 1 to clear this error.
5	G3FRERR	R/W1C	0h	This bit is set if a framing error is detected while receiving a TLP in Gen3. Example, if an invalid token is received in a data stream, this error is flagged. Write a 1 to clear this error.

Table 9-1508. PCIE_CORE_RP_I_PHY_STATUS_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	OSWOEDS	R/W1C	0h	This bit is set if an Ordered Set Block is received without an EDS. This is a framing error. Write a 1 to clear this error.
3	DATEDS	R/W1C	0h	This bit is set if a Data Block is received after an EDS. Write a 1 to clear this error.
2	ILOSEDS	R/W1C	0h	The Valid OS blocks after an EDS are EIOS, EIEOS and SKP. If any other OS blocks are received after EDS, then it is a framing error and this bit is asserted.
1	OSASKP	R/W1C	0h	This bit indicates that an Ordered Set BLock was received immediately after a SKIP OS. This is a framing error. Write a 1 to clear this field.
0	TLPPHYER	R/W1C	0h	This bit indicates that a PHY Error was detected on the PIPE_RX_STATUS within a TLP. Write a 1 to clear this field.

9.5.164 PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register (Offset = 00100240h) [reset = 05050585h]

PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG is shown in [Figure 9-553](#) and described in [Table 9-1510](#).

Return to [Summary Table](#).

N/A

Table 9-1509.
PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0240h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0240h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0240h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0240h

Figure 9-553. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C			BAR3A			BAR2C			BAR2A						
R/W-0h			R/W-5h			R/W-0h			R/W-5h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C			BAR1A			BAR0C			BAR0A						
R/W-0h			R/W-5h			R/W-4h			R/W-5h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1510. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1510. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1510. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1510. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB

Table 9-1510. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	BAR0C	R/W	4h	<p>Specifies the configuration of BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled</p> <p>001: 32bit IO BAR</p> <p>010-</p> <p>011: Reserved</p> <p>100: 32bit memory BAR, non prefetchable</p> <p>101: 32bit memory BAR, prefetchable</p> <p>110: 64bit memory BAR, non prefetchable</p> <p>111: 64bit memory BAR, prefetchable</p>

Table 9-1510. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1510. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.165 PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG Register (Offset = 00100244h) [reset = 505h]

PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG is shown in [Figure 9-554](#) and described in [Table 9-1512](#).

Return to [Summary Table](#).

N/A

Table 9-1511.
PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0244h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0244h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0244h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0244h

Figure 9-554. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1512. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved

Table 9-1512. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR5A	R/W	5h	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR4C	R/W	0h	Specifies the configuration of BAR4. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-1512. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1512. PCIE_CORE_RP_I_PF_0_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.166 PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register (Offset = 00100248h) [reset = 05050585h]

PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG is shown in [Figure 9-555](#) and described in [Table 9-1514](#).

Return to [Summary Table](#).

N/A

Table 9-1513.
PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0248h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0248h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0248h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0248h

Figure 9-555. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
BAR3C			BAR3A					BAR2C			BAR2A								
R/W-0h					R/W-5h					R/W-0h					R/W-5h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
BAR1C			BAR1A					BAR0C			BAR0A								
R/W-0h					R/W-5h					R/W-4h					R/W-5h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1514. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1514. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1514. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1514. PCIe_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB

Table 9-1514. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	BAR0C	R/W	4h	<p>Specifies the configuration of BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled</p> <p>001: 32bit IO BAR</p> <p>010-</p> <p>011: Reserved</p> <p>100: 32bit memory BAR, non prefetchable</p> <p>101: 32bit memory BAR, prefetchable</p> <p>110: 64bit memory BAR, non prefetchable</p> <p>111: 64bit memory BAR, prefetchable</p>

Table 9-1514. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1514. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.167 PCIe_CORE_RP_I_PF_1_BAR_CONFIG_1_REG Register (Offset = 0010024Ch) [reset = 505h]

PCIe_CORE_RP_I_PF_1_BAR_CONFIG_1_REG is shown in [Figure 9-556](#) and described in [Table 9-1516](#).

Return to [Summary Table](#).

N/A

Table 9-1515.
PCIe_CORE_RP_I_PF_1_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 024Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 024Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 024Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 024Ch

Figure 9-556. PCIe_CORE_RP_I_PF_1_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1516. PCIe_CORE_RP_I_PF_1_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved

Table 9-1516. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR5A	R/W	5h	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR4C	R/W	0h	Specifies the configuration of BAR4. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-1516. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1516. PCIE_CORE_RP_I_PF_1_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.168 PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register (Offset = 00100250h) [reset = 05050585h]

PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG is shown in [Figure 9-557](#) and described in [Table 9-1518](#).

Return to [Summary Table](#).

N/A

Table 9-1517.
PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0250h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0250h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0250h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0250h

Figure 9-557. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C			BAR3A			BAR2C			BAR2A						
R/W-0h			R/W-5h			R/W-0h			R/W-5h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C			BAR1A			BAR0C			BAR0A						
R/W-0h			R/W-5h			R/W-4h			R/W-5h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1518. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1518. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1518. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1518. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB

Table 9-1518. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	BAR0C	R/W	4h	<p>Specifies the configuration of BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled</p> <p>001: 32bit IO BAR</p> <p>010-</p> <p>011: Reserved</p> <p>100: 32bit memory BAR, non prefetchable</p> <p>101: 32bit memory BAR, prefetchable</p> <p>110: 64bit memory BAR, non prefetchable</p> <p>111: 64bit memory BAR, prefetchable</p>

Table 9-1518. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1518. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.169 PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG Register (Offset = 00100254h) [reset = 505h]

PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG is shown in [Figure 9-558](#) and described in [Table 9-1520](#).

Return to [Summary Table](#).

N/A

Table 9-1519.
PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0254h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0254h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0254h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0254h

Figure 9-558. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1520. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved

Table 9-1520. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR5A	R/W	5h	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR4C	R/W	0h	Specifies the configuration of BAR4. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-1520. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1520. PCIE_CORE_RP_I_PF_2_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.170 PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register (Offset = 00100258h) [reset = 05050585h]

PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG is shown in [Figure 9-559](#) and described in [Table 9-1522](#).

Return to [Summary Table](#).

N/A

Table 9-1521.
PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0258h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0258h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0258h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0258h

Figure 9-559. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAR3C				BAR3A				BAR2C				BAR2A			
R/W-0h				R/W-5h				R/W-0h				R/W-5h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAR1C				BAR1A				BAR0C				BAR0A			
R/W-0h				R/W-5h				R/W-4h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1522. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1522. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1522. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1522. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB

Table 9-1522. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	BAR0C	R/W	4h	<p>Specifies the configuration of BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled</p> <p>001: 32bit IO BAR</p> <p>010-</p> <p>011: Reserved</p> <p>100: 32bit memory BAR, non prefetchable</p> <p>101: 32bit memory BAR, prefetchable</p> <p>110: 64bit memory BAR, non prefetchable</p> <p>111: 64bit memory BAR, prefetchable</p>

Table 9-1522. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1522. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.171 PCIe_CORE_RP_I_PF_3_BAR_CONFIG_1_REG Register (Offset = 0010025Ch) [reset = 505h]

PCIe_CORE_RP_I_PF_3_BAR_CONFIG_1_REG is shown in [Figure 9-560](#) and described in [Table 9-1524](#).

Return to [Summary Table](#).

N/A

Table 9-1523.
PCIe_CORE_RP_I_PF_3_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 025Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 025Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 025Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 025Ch

Figure 9-560. PCIe_CORE_RP_I_PF_3_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1524. PCIe_CORE_RP_I_PF_3_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved

Table 9-1524. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR5A	R/W	5h	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR4C	R/W	0h	Specifies the configuration of BAR4. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-1524. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1524. PCIE_CORE_RP_I_PF_3_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.172 PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register (Offset = 00100260h) [reset = 05050585h]

PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG is shown in [Figure 9-561](#) and described in [Table 9-1526](#).

Return to [Summary Table](#).

N/A

Table 9-1525.
PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0260h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0260h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0260h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0260h

Figure 9-561. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
BAR3C			BAR3A					BAR2C			BAR2A								
R/W-0h					R/W-5h					R/W-0h					R/W-5h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
BAR1C			BAR1A					BAR0C			BAR0A								
R/W-0h					R/W-5h					R/W-4h					R/W-5h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1526. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1526. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1526. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1526. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB

Table 9-1526. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	BAR0C	R/W	4h	<p>Specifies the configuration of BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled</p> <p>001: 32bit IO BAR</p> <p>010-</p> <p>011: Reserved</p> <p>100: 32bit memory BAR, non prefetchable</p> <p>101: 32bit memory BAR, prefetchable</p> <p>110: 64bit memory BAR, non prefetchable</p> <p>111: 64bit memory BAR, prefetchable</p>

Table 9-1526. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1526. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.173 PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_REG Register (Offset = 00100264h) [reset = 505h]

PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_REG is shown in [Figure 9-562](#) and described in [Table 9-1528](#).

Return to [Summary Table](#).

N/A

Table 9-1527.
PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0264h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0264h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0264h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0264h

Figure 9-562. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1528. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved

Table 9-1528. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR5A	R/W	5h	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR4C	R/W	0h	Specifies the configuration of BAR4. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-1528. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1528. PCIE_CORE_RP_I_PF_4_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.174 PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register (Offset = 00100268h) [reset = 05050585h]

PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG is shown in [Figure 9-563](#) and described in [Table 9-1530](#).

Return to [Summary Table](#).

N/A

Table 9-1529.
PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0268h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0268h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0268h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0268h

Figure 9-563. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
BAR3C			BAR3A					BAR2C			BAR2A								
R/W-0h					R/W-5h					R/W-0h					R/W-5h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
BAR1C			BAR1A					BAR0C			BAR0A								
R/W-0h					R/W-5h					R/W-4h					R/W-5h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1530. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	BAR3C	R/W	0h	Specifies the configuration of BAR3. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1530. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	BAR3A	R/W	5h	<p>Specifies the aperture of the BAR 3 when it is configured as a 32-bit BAR.</p> <p>For 32-bit BAR 3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p>
23-21	BAR2C	R/W	0h	<p>Specifies the configuration of BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1530. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BAR2A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 2 or 64bit BAR 2-3.</p> <p>For 32-bit BAR 2, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 2-3, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1530. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB
15-13	BAR1C	R/W	0h	Specifies the configuration of BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR1A	R/W	5h	Specifies the aperture of the BAR 1 when it is configured as a 32-bit BAR. For 32-bit BAR 1, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB

Table 9-1530. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	BAR0C	R/W	4h	<p>Specifies the configuration of BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled</p> <p>001: 32bit IO BAR</p> <p>010-</p> <p>011: Reserved</p> <p>100: 32bit memory BAR, non prefetchable</p> <p>101: 32bit memory BAR, prefetchable</p> <p>110: 64bit memory BAR, non prefetchable</p> <p>111: 64bit memory BAR, prefetchable</p>

Table 9-1530. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR0A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 0 or 64bit BAR 0-1.</p> <p>For 32-bit BAR 0, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 0-1, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1530. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.175 PCIe_CORE_RP_I_PF_5_BAR_CONFIG_1_REG Register (Offset = 0010026Ch) [reset = 505h]

PCIe_CORE_RP_I_PF_5_BAR_CONFIG_1_REG is shown in [Figure 9-564](#) and described in [Table 9-1532](#).

Return to [Summary Table](#).

N/A

Table 9-1531.
PCIe_CORE_RP_I_PF_5_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 026Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 026Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 026Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 026Ch

Figure 9-564. PCIe_CORE_RP_I_PF_5_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24
ERBC	R24						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R16							
R-0h							
15	14	13	12	11	10	9	8
BAR5C				BAR5A			
R/W-0h				R/W-5h			
7	6	5	4	3	2	1	0
BAR4C				BAR4A			
R/W-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1532. PCIe_CORE_RP_I_PF_5_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERBC	R/W	0h	Setting this bit to 1 enables the Resizable BAR Capability in the PCI Express Configuration Space of the associated Function. When the Resizable BAR Capability is enabled, the apertures of the memory BARs of the corresponding Function are no longer selected by the fields in this register, but by the setting of the registers in the Resizable BAR Capability Structure.
30-24	R24	R	0h	Reserved
23-16	R16	R	0h	Reserved

Table 9-1532. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	BAR5C	R/W	0h	Specifies the configuration of BAR5. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
12-8	BAR5A	R/W	5h	Specifies the aperture of the BAR 5 when it is configured as a 32-bit BAR. For 32-bit BAR 5, the valid encodings are: 00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB
7-5	BAR4C	R/W	0h	Specifies the configuration of BAR4. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable

Table 9-1532. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	BAR4A	R/W	5h	<p>Specifies the aperture of the 32-bit BAR 4 or 64bit BAR 4-5.</p> <p>For 32-bit BAR 4, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB, 10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB</p> <p>For 64-bit BAR 4-5, the valid encodings are:</p> <p>00000 = 128 B, 00001 = 256 B, 00010 = 512 B, 00011 = 1 KB, 00100 = 2 KB, 00101 = 4 KB, 00110 = 8 KB, 00111 = 16 KB, 01000 = 32 KB, 01001 = 64 KB, 01010 = 128 KB, 01011 = 256 KB, 01100 = 512 KB, 01101 = 1 MB, 01110 = 2 MB, 01111 = 4 MB, 10000 = 8 MB, 10001 = 16 MB, 10010 = 32 MB, 10011 = 64 MB, 10100 = 128 MB,</p>

Table 9-1532. PCIE_CORE_RP_I_PF_5_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				10101 = 256 MB, 10110 = 512 MB, 10111 = 1 GB, 11000 = 2 GB, 11001 = 4 GB, 11010 = 8 GB, 11011 = 16 GB, 11100 = 32 GB, 11101 = 64 GB, 11110 = 128 GB, 11111 = 256 GB

9.5.176 PCIe_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG Register (Offset = 00100280h) [reset = 0F0F8FCFh]

PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG is shown in [Figure 9-565](#) and described in [Table 9-1534](#).

Return to [Summary Table](#).

N/A

Table 9-1533.
PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0280h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0280h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0280h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0280h

Figure 9-565. PCIe_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1534. PCIe_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1534. PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1534. PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-1534. PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1534. PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.177 PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_1_REG Register (Offset = 00100284h) [reset = F0Fh]

PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_1_REG is shown in [Figure 9-566](#) and described in [Table 9-1536](#).

Return to [Summary Table](#).

N/A

Table 9-1535.
PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0284h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0284h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0284h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0284h

Figure 9-566. PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1536. PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1536. PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	<p>Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR4C	R/W	0h	<p>Specifies the configuration of VF BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1536. PCIE_CORE_RP_I_PF_0_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.178 PCIe_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG Register (Offset = 00100288h) [reset = 0F0F8FCFh]

PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG is shown in [Figure 9-567](#) and described in [Table 9-1538](#).

Return to [Summary Table](#).

N/A

Table 9-1537.
PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0288h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0288h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0288h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0288h

Figure 9-567. PCIe_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1538. PCIe_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1538. PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001-010: Reserved 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1538. PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-1538. PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1538. PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.179 PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_1_REG Register (Offset = 0010028Ch) [reset = F0Fh]

PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_1_REG is shown in [Figure 9-568](#) and described in [Table 9-1540](#).

Return to [Summary Table](#).

N/A

Table 9-1539.
PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 028Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 028Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 028Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 028Ch

Figure 9-568. PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1540. PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1540. PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	<p>Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR4C	R/W	0h	<p>Specifies the configuration of VF BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1540. PCIE_CORE_RP_I_PF_1_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.180 PCIe_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG Register (Offset = 00100290h) [reset = 0F0F8FCFh]

PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG is shown in [Figure 9-569](#) and described in [Table 9-1542](#).

Return to [Summary Table](#).

N/A

Table 9-1541.
PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0290h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0290h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0290h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0290h

Figure 9-569. PCIe_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1542. PCIe_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1542. PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1542. PCIE_CORE_RP_1_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-1542. PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1542. PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.181 PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_1_REG Register (Offset = 00100294h) [reset = F0Fh]

PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_1_REG is shown in [Figure 9-570](#) and described in [Table 9-1544](#).

Return to [Summary Table](#).

N/A

Table 9-1543.
PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0294h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0294h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0294h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0294h

Figure 9-570. PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1544. PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1544. PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	<p>Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR4C	R/W	0h	<p>Specifies the configuration of VF BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1544. PCIE_CORE_RP_I_PF_2_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.182 PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG Register (Offset = 00100298h) [reset = 0F0F8FCFh]

PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG is shown in [Figure 9-571](#) and described in [Table 9-1546](#).

Return to [Summary Table](#).

N/A

Table 9-1545.
PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0298h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0298h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0298h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0298h

Figure 9-571. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1546. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1546. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1546. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-1546. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1546. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.183 PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_1_REG Register (Offset = 0010029Ch) [reset = F0Fh]

PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_1_REG is shown in [Figure 9-572](#) and described in [Table 9-1548](#).

Return to [Summary Table](#).

N/A

Table 9-1547.
PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 029Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 029Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 029Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 029Ch

Figure 9-572. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1548. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1548. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	<p>Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR4C	R/W	0h	<p>Specifies the configuration of VF BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1548. PCIE_CORE_RP_I_PF_3_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.184 PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG Register (Offset = 001002A0h) [reset = 0F0F8FCFh]

PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG is shown in [Figure 9-573](#) and described in [Table 9-1550](#).

Return to [Summary Table](#).

N/A

Table 9-1549.
PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02A0h

Figure 9-573. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1550. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1550. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1550. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-1550. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001-010: Reserved 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1550. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.185 PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_1_REG Register (Offset = 001002A4h) [reset = F0Fh]

PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_1_REG is shown in [Figure 9-574](#) and described in [Table 9-1552](#).

Return to [Summary Table](#).

N/A

Table 9-1551.
PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02A4h

Figure 9-574. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1552. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1552. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	<p>Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR4C	R/W	0h	<p>Specifies the configuration of VF BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1552. PCIE_CORE_RP_I_PF_4_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.186 PCIe_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG Register (Offset = 001002A8h) [reset = 0F0F8FCFh]

PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG is shown in [Figure 9-575](#) and described in [Table 9-1554](#).

Return to [Summary Table](#).

N/A

Table 9-1553.
PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02A8h

Figure 9-575. PCIe_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VFBAR3C				VFBAR3A				VFBAR2C				VFBAR2A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR1C				VFBAR1A				VFBAR0C				VFBAR0A			
R/W-4h				R/W-Fh				R/W-6h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1554. PCIe_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	VFBAR3C	R/W	0h	Specifies the configuration of VF BAR3. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1554. PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-24	VFBAR3A	R/W	Fh	<p>Specifies the aperture of the VF BAR 3 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
23-21	VFBAR2C	R/W	0h	<p>Specifies the configuration of VF BAR2.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1554. PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	VFBAR2A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 2 or 64bit VF BAR 2-3.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>
15-13	VFBAR1C	R/W	4h	<p>Specifies the configuration of VF BAR1.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved</p>

Table 9-1554. PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR1A	R/W	Fh	<p>Specifies the aperture of the VF BAR 1 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR0C	R/W	6h	<p>Specifies the configuration of VF BAR0.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1554. PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_0_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR0A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 0 or 64bit VF BAR 0-1.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.187 PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_1_REG Register (Offset = 001002ACh) [reset = F0Fh]

PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_1_REG is shown in [Figure 9-576](#) and described in [Table 9-1556](#).

Return to [Summary Table](#).

N/A

Table 9-1555.
PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02ACh

Figure 9-576. PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R16															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VFBAR5C				VFBAR5A				VFBAR4C				VFBAR4A			
R/W-0h				R/W-Fh				R/W-0h				R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1556. PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R16	R	0h	Reserved
15-13	VFBAR5C	R/W	0h	Specifies the configuration of VF BAR5. The various encodings are: 000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved

Table 9-1556. PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	VFBAR5A	R/W	Fh	<p>Specifies the aperture of the VF BAR 5 when it is configured as a 32-bit BAR.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes</p>
7-5	VFBAR4C	R/W	0h	<p>Specifies the configuration of VF BAR4.</p> <p>The various encodings are:</p> <p>000: Disabled 001- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable</p>

Table 9-1556. PCIE_CORE_RP_I_PF_5_VF_BAR_CONFIG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	VFBAR4A	R/W	Fh	<p>Specifies the aperture of the 32-bit VF BAR 4 or 64bit VF BAR 4-5.</p> <p>The encodings are:</p> <p>00000 = 128 Bytes, 0001 = 256 Bytes, 0010 = 512 Bytes, 0011 = 1 Kbytes, 00100 = 2 Kbytes, 00101 = 4 Kbytes, 00110 = 8 Kbytes, 00111 = 16 Kbytes, 01000 = 32 Kbytes, 01001 = 64 Kbytes, 01010 = 128 Kbytes, 01011 = 256 Kbytes, 01100 = 512 Kbytes, 01101 = 1 Mbyte, 01110 = 2 Mbytes, 01111 = 4 Mbytes, 10000 = 8 Mbytes, 10001 = 16 Mbytes, 10010 = 32 Mbytes, 10011 = 64 Mbytes, 10100 = 128 Mbytes, 10101 = 256 Mbytes, 10110 = 512 Mbytes, 10111 = 1 Gbyte, 11000 = 2 Gbytes, 11001 = 4 Gbytes, 11010 = 8 Gbytes, 11011 = 16 Gbytes, 11100 = 32 Gbytes, 11101 = 64 Gbytes, 11110 = 128 Gbytes, 11111 = 256 Gbytes</p>

9.5.188 PCIe_CORE_RP_I_PF_CONFIG_REG Register (Offset = 001002C0h) [reset = 3Fh]

PCIe_CORE_RP_I_PF_CONFIG_REG is shown in [Figure 9-577](#) and described in [Table 9-1558](#).

Return to [Summary Table](#).

N/A

**Table 9-1557. PCIe_CORE_RP_I_PF_CONFIG_REG
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 02C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 02C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 02C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 02C0h

Figure 9-577. PCIe_CORE_RP_I_PF_CONFIG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R										F5E	F4E	F3E	F2E	F1E	F0E
R-0h										R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1558. PCIe_CORE_RP_I_PF_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	R	R	0h	Reserved
5	F5E	R/W	1h	Enable for Function 5. This bit can be modified from the local management bus.
4	F4E	R/W	1h	Enable for Function 4. This bit can be modified from the local management bus.
3	F3E	R/W	1h	Enable for Function 3. This bit can be modified from the local management bus.
2	F2E	R/W	1h	Enable for Function 2. This bit can be modified from the local management bus.
1	F1E	R/W	1h	Enable for Function 1. This bit can be modified from the local management bus.
0	F0E	R	1h	Enable for Function 0. This bit is hardwired to 1.

9.5.189 PCIE_CORE_RP_I_RC_BAR_CONFIG_REG Register (Offset = 00100300h) [reset = 2914h]

PCIE_CORE_RP_I_RC_BAR_CONFIG_REG is shown in [Figure 9-578](#) and described in [Table 9-1560](#).

Return to [Summary Table](#).

N/A

Table 9-1559.
PCIE_CORE_RP_I_RC_BAR_CONFIG_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0300h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0300h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0300h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0300h

Figure 9-578. PCIE_CORE_RP_I_RC_BAR_CONFIG_REG Register

31	30	29	28	27	26	25	24
RCBCE	R10						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R10			RCBARPIS	RCBARPIE	RCBARPMS	RCBARPME	RCBAR1C
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RCBAR1C		RCBAR1A					RCBAR0C
R/W-0h		R/W-14h					R/W-4h
7	6	5	4	3	2	1	0
RCBAR0C		RCBAR0A					
R/W-4h		R/W-14h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1560. PCIE_CORE_RP_I_RC_BAR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RCBCE	R/W	0h	This bit must be set to 1 to enable BAR checking in the RC mode. When this bit is set to 0, the Controller will forward all incoming memory requests to the client logic without checking their address ranges.
30-21	R10	R	0h	Reserved
20	RCBARPIS	R/W	0h	Width of IO Base and Limit registers in type1 config space. 0=32 bits, 1=64bits
19	RCBARPIE	R/W	0h	Enable for IO Base and Limit registers in type1 config space
18	RCBARPMS	R/W	0h	Width of Prefetchable Memory Base and Limit registers in type1 config space. 0=32 bits, 1=64bits
17	RCBARPME	R/W	0h	Enable for Prefetchable memory base and limit registers in type1 config space

Table 9-1560. PCIE_CORE_RP_I_RC_BAR_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-14	RCBAR1C	R/W	0h	Specifies the configuration of RC BAR1. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110- 111: Reserved
13-9	RCBAR1A	R/W	14h	This field specifies the aperture of the RC BAR 1. The encodings are: 0000 = 4, 00001 =8B,..... 1_ 1101 = 2G
8-6	RCBAR0C	R/W	4h	Specifies the configuration of RC BAR0. The various encodings are: 000: Disabled 001: 32bit IO BAR 010- 011: Reserved 100: 32bit memory BAR, non prefetchable 101: 32bit memory BAR, prefetchable 110: 64bit memory BAR, non prefetchable 111: 64bit memory BAR, prefetchable
5-0	RCBAR0A	R/W	14h	This field specifies the aperture of the RC BAR 0. The encodings are: 0000 = 4, 00001 =8B,..... 01_ 1111 = 8G,10_ 0100 = 256G.

9.5.190 PCIE_CORE_RP_I_GEN3_DEFAULT_PRESET_REG Register (Offset = 00100360h) [reset = 0007FF00h]

PCIE_CORE_RP_I_GEN3_DEFAULT_PRESET_REG is shown in [Figure 9-579](#) and described in [Table 9-1562](#).

Return to [Summary Table](#).

N/A

Table 9-1561.
PCIE_CORE_RP_I_GEN3_DEFAULT_PRESET_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0360h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0360h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0360h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0360h

Figure 9-579. PCIE_CORE_RP_I_GEN3_DEFAULT_PRESET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R31												S8GPR			
R-0h												R/W-7FFh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S8GPR								R7	GDRXPH				GDTXP		
R/W-7FFh								R-0h	R/W-0h				R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1562. PCIE_CORE_RP_I_GEN3_DEFAULT_PRESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	R31	R	0h	Reserved
18-8	S8GPR	R/W	7FFh	This register can be used to program the Presets that are supported by local Transmitter at 8Gbps. Default value of this register is determined by the SUPPORTED_PRESET strap input. Note: At 8.0 GT/s and 16.0 GT/s all preset values must be supported for Full swing signaling. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3.
7	R7	R	0h	Reserved
6-4	GDRXPH	R/W	0h	Default receiver preset hint value used for a lane that did not receive EQ TS2 in Recovery.RcvrCfg LTSSM state
3-0	GDTXP	R/W	0h	Default transmitter preset value used for a lane that did not receive EQ TS2 in Recovery.RcvrCfg LTSSM state

9.5.191 PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Register (Offset = 00100364h) [reset = C001E848h]

PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG is shown in [Figure 9-580](#) and described in [Table 9-1564](#).

Return to [Summary Table](#).

N/A

Table 9-1563.
PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0364h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0364h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0364h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0364h

Figure 9-580. PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Register

31	30	29	28	27	26	25	24
RXEQABM		RXEQABD	R28	LEQT2MS			
R/W-3h		R/W-0h	R-0h	R/W-0001E848h			
23	22	21	20	19	18	17	16
LEQT2MS							
R/W-0001E848h							
15	14	13	12	11	10	9	8
LEQT2MS							
R/W-0001E848h							
7	6	5	4	3	2	1	0
LEQT2MS							
R/W-0001E848h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1564. PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RXEQABM	R/W	3h	<p>When a 24ms timeout occurs in the LTSSM Equalization Phase 2, the Controller aborts Equalization Phase 2 and transitions to Recovery.Rcvr.Lock. In this case, the RxEqEval output on the PIPE Interface will be de-asserted immediately [if it was asserted]. The RxEqInProgress output will stay high and waits for PhyStatus pulse.</p> <p>Controller implements a timer to select an upper limit to wait for this PhyStatus pulse during an abort to de-assert RxEqInProgress.</p> <p>00: Wait for a maximum of 4 PIPE_PCLK period.</p> <p>01: Wait for a maximum of 8 PIPE_PCLK period.</p> <p>10: Wait for a maximum of 16 PIPE_PCLK period.</p> <p>11: Disabled.</p> <p>Wait till PhyStatus Pulse is received.</p> <p>Note: This register is used only if RxEqEval was asserted when LTSSM 24ms timeout occurred in Equalization.</p>

Table 9-1564. PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_TIMEOUT_2MS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	RXEQABD	R/W	0h	In an unexpected case where the PIPE_PCLK stops due to error in equalization, this bit can be set to de-couple RxEqInProgress from the rest of the equalization state machine. This bit should not be set for normal usage.
28	R28	R	0h	Reserved
27-0	LEQT2MS	R/W	0001E848h	Time spent for evaluation per TX Setting in Endpoint Phase 2 [RC Mode Phase 3] of Link Equalization specified in multiples of 16ns. eg. the value 125000 will result in 125000*16ns = 2ms. Simulation with reduced time mode[PCIE_SIM define] will give a smaller value of 300 as power on reset value.

9.5.192 PCIE_CORE_RP_I_PIPE_FIFO_LATENCY_CTRL_REG Register (Offset = 00100368h) [reset = 0h]

PCIE_CORE_RP_I_PIPE_FIFO_LATENCY_CTRL_REG is shown in [Figure 9-581](#) and described in [Table 9-1566](#).

Return to [Summary Table](#).

N/A

Table 9-1565.
PCIE_CORE_RP_I_PIPE_FIFO_LATENCY_CTRL_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0368h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0368h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0368h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0368h

Figure 9-581. PCIE_CORE_RP_I_PIPE_FIFO_LATENCY_CTRL_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31							DPTFCE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1566. PCIE_CORE_RP_I_PIPE_FIFO_LATENCY_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	R31	R	0h	Reserved
0	DPTFCE	R/W	0h	By default, if FIFO empty is reached, the PIPE TX FIFO accumulates 2 entries before reading the FIFO again. This is to prevent FIFO from reaching empty again. This bit must remain at 0 to allow the PIPE TX FIFO to recover effectively from a Empty condition.

9.5.193 PCIE_CORE_RP_I_GEN4_DEFAULT_PRESET_REG Register (Offset = 00100374h) [reset = 0007FF00h]

PCIE_CORE_RP_I_GEN4_DEFAULT_PRESET_REG is shown in [Figure 9-582](#) and described in [Table 9-1568](#).

Return to [Summary Table](#).

N/A

Table 9-1567.
PCIE_CORE_RP_I_GEN4_DEFAULT_PRESET_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0374h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0374h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0374h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0374h

Figure 9-582. PCIE_CORE_RP_I_GEN4_DEFAULT_PRESET_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R31												S16GPR			
R-0h												R/W-7FFh			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S16GPR								R7	GDRXPH				GDTXP		
R/W-7FFh								R-0h	R/W-0h				R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1568. PCIE_CORE_RP_I_GEN4_DEFAULT_PRESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	R31	R	0h	Reserved
18-8	S16GPR	R/W	7FFh	This register can be used to program the Presets that are supported by local Transmitter at 16Gbps. Default value of this register is determined by the SUPPORTED_PRESET strap input. Note: At 8.0 GT/s and 16.0 GT/s all preset values must be supported for Full swing signaling. Reduced swing signaling must implement presets #4, #1, #9, #5, #6, and #3.
7	R7	R	0h	Reserved
6-4	GDRXPH	R/W	0h	Default Gen4 receiver preset hint value used for a lane that did not receive 16G EQ TS2 in Recovery.RcvrCfg LTSSM state
3-0	GDTXP	R/W	0h	Default Gen4 transmitter preset value used for a lane that did not receive 16G EQ TS2 in Recovery.RcvrCfg LTSSM state

9.5.194 PCIE_CORE_RP_I_PHY_CONFIG_REG3 Register (Offset = 00100378h) [reset = 40h]

PCIE_CORE_RP_I_PHY_CONFIG_REG3 is shown in [Figure 9-583](#) and described in [Table 9-1570](#).

Return to [Summary Table](#).

N/A

Table 9-1569.
PCIE_CORE_RP_I_PHY_CONFIG_REG3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0378h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0378h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0378h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0378h

Figure 9-583. PCIE_CORE_RP_I_PHY_CONFIG_REG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R24																TFC4															
R-0h																R/W-40h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1570. PCIE_CORE_RP_I_PHY_CONFIG_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	R24	R	0h	Reserved
7-0	TFC4	R/W	40h	FTS count transmitted by the Controller in TS1/TS2 sequences during link training. This value must be set based on the time needed by the receiver to acquire sync while exiting from LOS state at 16 GT/s speed.

9.5.195 PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register (Offset = 0010037Ch) [reset = 0h]

PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_CTRL_REG is shown in [Figure 9-584](#) and described in [Table 9-1572](#).

Return to [Summary Table](#).

N/A

Table 9-1571.
PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_CTRL_R
EG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 037Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 037Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 037Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 037Ch

Figure 9-584. PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register

31	30	29	28	27	26	25	24
RES20							
R-0h							
23	22	21	20	19	18	17	16
RES20				MX16GERL			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
MX8GERL				RES10		QG16GT	QG8GT
R/W-0h				R-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RES6		EP16GRE	EP8GRE	RES3	MXECC		
R-0h		R/W-0h	R/W-0h	R-0h	R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1572. PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RES20	R	0h	Reserved
19-16	MX16GERL	R/W	0h	The number of 16GT/s Equalization Requests must be finite as per PCIe specification. This register can be used to program the maximum number of 16GT/s equalization requests automatically initiated by the Endpoint. 0000: Automatic 16GT/s Equalization Request Disabled. 0001: Automatic 16GT/s Equalization request limit is 1. 0010: Automatic 16GT/s Equalization request limit is 2. 1111: Automatic 16GT/s Equalization request limit is 15,

**Table 9-1572. PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15-12	MX8GERL	R/W	0h	The number of 8GT/s Equalization Requests must be finite as per PCIe specification. This register can be used to program the maximum number of 8GT/s equalization requests automatically initiated by the Endpoint. 0000: Automatic 8GT/s Equalization Request Disabled. 0001: Automatic 8GT/s Equalization request limit is 1. 0010: Automatic 8GT/s Equalization request limit is 2. 1111: Automatic 8GT/s Equalization request limit is 15,
11-10	RES10	R	0h	Reserved
9	QG16GT	R/W	0h	This bit can be used to program the Quiesce Guarantee bit of the TS2 in Recovery.Rcvr.Cfg state during 16GT/s Request Equalization.
8	QG8GT	R/W	0h	This bit can be used to program the Quiesce Guarantee bit of the TS2 in Recovery.Rcvr.Cfg state during 8GT/s Request Equalization.
7-6	RES6	R	0h	Reserved
5	EP16GRE	R/W	0h	Writing a 1 into this field results in the Controller to transition to Recovery. The Request Equalization bit and Equalization Request Data Rate bit in TS2 Ordered Sets will be set to 1 in Recovery.Rcvr.Cfg to request equalization at 16GTs. This bit is auto-cleared by the internal logic of the Controller after the re-training has been completed and link has reached the PCIE_CORE_RP_L0 state. This bit is also auto-cleared when not in Gen3 or Gen4. Device Firmware must wait for the bit to be clear before any subsequent requests.
4	EP8GRE	R/W	0h	This bit can be used by Endpoint Device FW to request for 8GT/s Equalization redo. This bit can be set at any time after the Link is Up. Writing a 1 into this field results in the Controller to transition to Recovery. The Request Equalization bit in TS2 Ordered Sets will be set to 1 in Recovery.Rcvr.Cfg to request equalization at 8GTs. This bit is auto-cleared by the internal logic of the Controller after the re-training has been completed and link has reached the PCIE_CORE_RP_L0 state. This bit is also auto-cleared when not in Gen3 or Gen4. Device Firmware must wait for the bit to be clear before any subsequent retrain requests.
3	RES3	R	0h	Reserved

Table 9-1572. PCIE_CORE_RP_I_GEN3_GEN4_LINK_EQ_CTRL_REG Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
2-0	MXECC	R/W	0h	<p>Controls the number of consecutive RxEqEval iterations with direction change feedback of 00s before Equalization Convergence is inferred.</p> <p>0 : Infer Convergence after 1 feedback of 000000 1 : Infer Convergence after 2 feedback of 000000 2 : Infer Convergence after 3 consecutive feedback of 000000 .. 7 : Infer Convergence after 8 consecutive feedback of 000000.</p> <p>Note: Each lane independently counts consecutive feedback of 000000.</p> <p>Note: Count is reset after a non-000000 feedback on each lane.</p>

9.5.196 PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register (Offset = 00100380h) [reset = 000B4004h]

PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 is shown in [Figure 9-585](#) and described in [Table 9-1574](#).

Return to [Summary Table](#).

N/A

Table 9-1573.
PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATU
S_REG_LANE0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0380h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0380h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0380h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0380h

Figure 9-585. PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R-0h						R-B40h	
23	22	21	20	19	18	17	16
LEQTXCO							
R-B40h							
15	14	13	12	11	10	9	8
LEQTXCO							
R-B40h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV	LEQTXPR			
R-0h			R-0h	R-4h			

LEGEND: R = Read Only; -n = value after reset

Table 9-1574. PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES3126	R	0h	Reserved
25-8	LEQTXCO	R	B40h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cursor Coefficient
7-5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3-0	LEQTXPR	R	4h	TX Preset agreed upon for this lane

9.5.197 PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register (Offset = 00100384h) [reset = 000B4004h]

PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 is shown in [Figure 9-586](#) and described in [Table 9-1576](#).

Return to [Summary Table](#).

N/A

Table 9-1575.
PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATU
S_REG_LANE1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0384h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0384h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0384h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0384h

Figure 9-586. PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R-0h						R-B40h	
23	22	21	20	19	18	17	16
LEQTXCO							
R-B40h							
15	14	13	12	11	10	9	8
LEQTXCO							
R-B40h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV		LEQTXPR		
R-0h			R-0h		R-4h		

LEGEND: R = Read Only; -n = value after reset

Table 9-1576. PCIE_CORE_RP_I_GEN3_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES3126	R	0h	Reserved
25-8	LEQTXCO	R	B40h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cursor Coefficient
7-5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3-0	LEQTXPR	R	4h	TX Preset agreed upon for this lane

9.5.198 PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register (Offset = 001003C0h) [reset = 00684608h]

PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 is shown in [Figure 9-587](#) and described in [Table 9-1578](#).

Return to [Summary Table](#).

N/A

Table 9-1577.
PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATU
S_REG_LANE0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 03C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 03C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 03C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 03C0h

Figure 9-587. PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R-0h						R-6846h	
23	22	21	20	19	18	17	16
LEQTXCO							
R-6846h							
15	14	13	12	11	10	9	8
LEQTXCO							
R-6846h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV	LEQTXPR			
R-0h			R-0h	R-8h			

LEGEND: R = Read Only; -n = value after reset

Table 9-1578. PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES3126	R	0h	Reserved
25-8	LEQTXCO	R	6846h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cursor Coefficient
7-5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3-0	LEQTXPR	R	8h	TX Preset agreed upon for this lane

9.5.199 PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register (Offset = 001003C4h) [reset = 00684608h]

PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 is shown in [Figure 9-588](#) and described in [Table 9-1580](#).

Return to [Summary Table](#).

N/A

Table 9-1579.
PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATU
S_REG_LANE1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 03C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 03C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 03C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 03C4h

Figure 9-588. PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register

31	30	29	28	27	26	25	24
RES3126						LEQTXCO	
R-0h						R-6846h	
23	22	21	20	19	18	17	16
LEQTXCO							
R-6846h							
15	14	13	12	11	10	9	8
LEQTXCO							
R-6846h							
7	6	5	4	3	2	1	0
RES75			LEQTXPRV		LEQTXPR		
R-0h			R-0h		R-8h		

LEGEND: R = Read Only; -n = value after reset

Table 9-1580. PCIE_CORE_RP_I_GEN4_LINK_EQ_DEBUG_STATUS_REG_LANE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RES3126	R	0h	Reserved
25-8	LEQTXCO	R	6846h	TX Coefficients agreed upon for this lane. [25:20] : Post Cursor Coefficient [19:14] : Cursor Coefficient [13:8] : Pre-Cursor Coefficient
7-5	RES75	R	0h	Reserved
4	LEQTXPRV	R	0h	TX Preset Valid Indicator. This bit is set when a TX Preset is received in TS1s with the use_preset bit set in Endpoint Mode Phase 3 or RC Mode Phase 2.
3-0	LEQTXPR	R	8h	TX Preset agreed upon for this lane

9.5.200 PCIe_CORE_RP_I_ECC_CORR_ERR_COUNT_REG_AXI Register (Offset = 00100C80h) [reset = 0h]

PCIE_CORE_RP_I_ECC_CORR_ERR_COUNT_REG_AXI is shown in [Figure 9-589](#) and described in [Table 9-1582](#).

Return to [Summary Table](#).

N/A

Table 9-1581.
PCIE_CORE_RP_I_ECC_CORR_ERR_COUNT_REG_
AXI Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C80h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C80h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C80h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C80h

Figure 9-589. PCIe_CORE_RP_I_ECC_CORR_ERR_COUNT_REG_AXI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AXI_MASTER_DIB_CER								AXI_MASTER_RFIFO_CER							
R/W1C-0h								R/W1C-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AXI_SLAVE_WFIFO_CER								REORDER_CER							
R/W1C-0h								R/W1C-0h							

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1582. PCIe_CORE_RP_I_ECC_CORR_ERR_COUNT_REG_AXI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	AXI_MASTER_DIB_CER	R/W1C	0h	Number of correctable errors detected while reading from the AXI Master Read Data interleave RAM. This is an 8-bit saturating counter that can be cleared by writing all 1s into it.
23-16	AXI_MASTER_RFIFO_CER	R/W1C	0h	Number of correctable errors detected while reading from the AXI master read fifo RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
15-8	AXI_SLAVE_WFIFO_CER	R/W1C	0h	Number of correctable errors detected while reading from the AXI slave write fifo RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.
7-0	REORDER_CER	R/W1C	0h	Number of correctable errors detected while reading from the AXI slave reorder RAM. This is an 8-bit saturating counter that can be cleared by writing all 1's into it.

9.5.201 PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL0 Register (Offset = 00100C88h) [reset = X]

PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL0 is shown in [Figure 9-590](#) and described in [Table 9-1584](#).

Return to [Summary Table](#).

N/A

Table 9-1583.
PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C88h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C88h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C88h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C88h

Figure 9-590. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL0 Register

31	30	29	28	27	26	25	24
RESERVED				L1DLEUP	L1EM		L1DBRI
R/W-X				R/W-0h	R-0h		R/W-0h
23	22	21	20	19	18	17	16
L1XDELAY							
R/W-0h							
15	14	13	12	11	10	9	8
L1XDELAY							
R/W-0h							
7	6	5	4	3	2	1	0
L1XDELAY							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1584. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27	L1DLEUP	R/W	0h	Pending Tlps trigger a L1 exit by default. This includes internally generated messages and internally blocked TLPs. Setting this bit changes the default behavior. This is required only for debug purpose.
26-25	L1EM	R	0h	This field shows the last entered L1 mode. This is useful for debug. bit 0 - Entry mode was ASPM. Bit 1 - Entry mode was PM. This is reset before any new L1 entry.

**Table 9-1584. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
24	L1DBRI	R/W	0h	<p>Before entering L1, controller internally blocks all TLP and Register Request interface entering controller.</p> <p>interfaces are internally unblocked while exiting L1.</p> <p>This field control this behavior.</p> <p>'1' in this field makes the controller to do not perform any blocking to interfaces.</p> <p>'0' makes the controller behaves normaly.</p> <p>This is required only for debug purpose.</p> <p>Power shutoff feature has to be disabled while using this field.</p>
23-0	L1XDELAY	R/W	0h	<p>Normaly L1 substate entry process is initiated immedaitely after LTSSM enters L1.</p> <p>A delay in micro-seconds can be given in this field to delay L1 substate entry process.</p> <p>This timeout has 0-1us margin of error.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_L1_SUBSTATE_ENTRY_DELAY</p>

9.5.202 PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL1 Register (Offset = 00100C8Ch) [reset = X]

PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL1 is shown in [Figure 9-591](#) and described in [Table 9-1586](#).

Return to [Summary Table](#).

N/A

Table 9-1585.
PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C8Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C8Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C8Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C8Ch

Figure 9-591. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								L1ER							
R-X																								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-1586. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	L1ER	R	0h	<p>This field shows the values of possible L1 or L1-substate exit triggers. This is useful for debug. this is captured during L1 or L1-substate exit process. this field is reset during L1 entry.</p> <p>0 : CLIENT_REQ_EXIT_L1 asserted 1 : Electrical Idle exit detected at link 2 : New TLP request detected 3 : Internal request to send TLP. This includes CFG completions. internal messages. INTx messages 4 : Pending TX traffic available. This could be traffic from DMA and blocked traffic due to credits at AXI. 5 : #CLKREQ assert detected 6 : CLIENT_REQ_EXIT_L1_SUBSTATE asserted 7 : Reg Access request detected Triggers #5,6,7 are valid only with L1-substate supported configs.</p>

9.5.203 PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2 Register (Offset = 00100C90h) [reset = X]

PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2 is shown in [Figure 9-592](#) and described in [Table 9-1588](#).

Return to [Summary Table](#).

N/A

Table 9-1587.
PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C90h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C90h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C90h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C90h

Figure 9-592. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2 Register

31	30	29	28	27	26	25	24
L1UPACR	L1CSC	L1DAET	L1TROW	L1PS	L1ERC	L1EOC	RESERVED
R/W-1h	R/W-0h	R/W-0h	R-0h	R/W-1h	R/W-0h	R/W-0h	R/W-X
23	22	21	20	19	18	17	16
L1TWROI							
R/W-0h							
15	14	13	12	11	10	9	8
L1TWROI							
R/W-0h							
7	6	5	4	3	2	1	0
L1TWROI							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1588. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	L1UPACR	R/W	1h	Setting this field make the state machine to consider LP_CTRL_POWER_RECOVER_ACK as Client system recovery Complete ACK instead of the Controller power stable ACK. This field is ignored if LP_CTRL_BYPASS_ENABLE unset. If this field is set, L 1-substate machines expect that the client system finishes power up of the controller within power_on time in the L 1-substate capability register and Controller will be waiting in recovery state for ACK. This ensure that the PHY PLL lock and client system initialization goes on in parallel. Default value of this register can be set with the define:den_db_LP_DBG_CTRL_RECOVER_ACK_AS_CLIENT_RECOVER_ACK. Setting this field gives the best system performance.

**Table 9-1588. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
30	L1CSC	R/W	0h	<p>L</p> <p>1-substate removes CORE_CLK.</p> <p>since the registers are implemented in core-clk, register access is not possible during L</p> <p>1-substate.</p> <p>If client can supply a slow clock to core[CORE_CLK] during L</p> <p>1-substates, APB/mgmt access is possible in L1.x.</p> <p>set this bit if client can supply slow clock to CORE_CLK when CLKREQ_IN_N is 1[de-asserted].</p> <p>If this bit is set, Controller neither wake-up from L1 or generate error response for APB access during L1.x.</p> <p>Controller behavior is undefined if register write is performed while slow clock is supplied to core_clk.</p> <p>Recommended flow is to first exit from L</p> <p>1-substate and perform register writes.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_CLIENT_SUPPLIES_SLOW_CLK_TO_CORE_DURING_L1</p>
29	L1DAET	R/W	0h	<p>L1.x turns off clocks to the controller.</p> <p>Default behavior is made to exit L1.x if Register access request is present at register interface.</p> <p>Setting this bit disables this feature.</p> <p>If this</p> <p>bit is set and CLKREQ_IN_N is 1[de-asserted], Controller responds with ERROR response</p> <p>to APB requests.</p> <p>Client can use CLIENT_EXIT_L1_SUBSTATE</p> <p>pin to trigger L1.x exit if autonomous exit is disabled for register access.</p> <p>This bit is ignored if L1 substate is disabled.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_DISABLE_AUTONOMOUS_L1_EXIT_ON_NEW_REG_REQ</p>
28	L1TROW	R	0h	<p>This is a debug status field.</p> <p>'1' in this field indicates that a timeout has occurred while waiting for RX path or OUTstanding packet IDLE conditions.</p> <p>This is cleared on new entry to L1.</p>
27	L1PS	R/W	1h	<p>This field enabled power shutoff mechanism in L1.2 state.</p> <p>This field is ignored if L1.x is not enabled.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_POWER_SHUTOFF_ENABLE</p>

**Table 9-1588. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26	L1ERC	R/W	0h	<p>Enables waiting for RX path IDLE condition before entering L1.x. This checks that all packets from PCIE link has reached client side before entering L1.x. This only a tuning register. Not setting this register will cause controller to enter L1.x to save power without checking this. controller will resume transferring RX data once it exit from L1.x state if RX buffers were not empty. This field is ignored if Power shutoff mechanism is enabled for L1.x and Controller will always check RX path idle condition before turning off internal power[with cpf flow]. If timeout is enabled, controller enters L1.x without internal power shutoff after timeout. This bit is ignored if L1 substate is disabled. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_WAIT_FOR_RX_BUFFER_IDLE</p>
25	L1EOC	R/W	0h	<p>Enable waiting for outstanding completions before entering L1.x. Outstanding packets expected from pcie link as well as from AXI side is checked. FOR HAL configurations client has to assert PREVENT_L1x_ENTRY signal to prevent L1x entry. This only a tuning register. Not setting this register will cause controller to enter L1.x to save power without checking this. controller exit from L1.x as soon as it receives expected TLps. This field is ignored if Power shutoff mechanism is selected for L1.x and Controller will always wait for outstanding packets before turning off internal power[with cpf flow]. If timeout is enabled, controller enters L1.x without internal power shutoff after timeout. This bit is ignored if L1 substate is disabled. Power on reset value of this register can be adjusted by modifying the define den_db_LP_DBG_CTRL_WAIT_FOR_OUTSTANDING_CPLS</p>
24	RESERVED	R/W	X	

Table 9-1588. PCIE_CORE_RP_LOW_POWER_DEBUG_AND_CONTROL2 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
23-0	L1TWROI	R/W	0h	<p>This field enables a timeout mechanism while waiting for RX buffers and Outstanding Pkts before turning off power.</p> <p>Controller enters L1 substate after timeout.</p> <p>A value of 0x0 disables this timeout mechanism.</p> <p>Controller do not select internal power shutoff if it enters L1.x with this timeout.</p> <p>User can give timeout in micro-seconds using this register.</p> <p>This field is ignored if L1 substate is disabled.</p> <p>Power on reset value of this register can be adjusted by modifying the define</p> <p>den_db_LP_DBG_CTRL_RX_CPL_IDLE_CHECK_TIMEOUT</p>

9.5.204 PCIE_CORE_RP_TL_INTERNAL_CONTROL Register (Offset = 00100C94h) [reset = 0h]

PCIE_CORE_RP_TL_INTERNAL_CONTROL is shown in [Figure 9-593](#) and described in [Table 9-1590](#).

Return to [Summary Table](#).

N/A

Table 9-1589.
PCIE_CORE_RP_TL_INTERNAL_CONTROL
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C94h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C94h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C94h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C94h

Figure 9-593. PCIE_CORE_RP_TL_INTERNAL_CONTROL Register

31	30	29	28	27	26	25	24
RES1							
R-0h							
23	22	21	20	19	18	17	16
RES1							
R-0h							
15	14	13	12	11	10	9	8
RES1							
R-0h							
7	6	5	4	3	2	1	0
RES1							ECFLR
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1590. PCIE_CORE_RP_TL_INTERNAL_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RES1	R	0h	Reserved
0	ECFLR	R/W	0h	By default controller ignores config request if a function is under going FLR. Setting this bit Makes the controller to respond with CRS response. Power on reset value of this register can be adjusted by modifying the define den_db_TL_CTRL_ENABLE_CRS_UNDER_FLR

9.5.205 PCIE_CORE_RP_I_DTI_ATS_STATUS Register (Offset = 00100C98h) [reset = 0h]

PCIE_CORE_RP_I_DTI_ATS_STATUS is shown in [Figure 9-594](#) and described in [Table 9-1592](#).

[Return to Summary Table.](#)

N/A

Table 9-1591. PCIE_CORE_RP_I_DTI_ATS_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C98h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C98h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C98h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C98h

Figure 9-594. PCIE_CORE_RP_I_DTI_ATS_STATUS Register

31	30	29	28	27	26	25	24
R10							
R-0h							
23	22	21	20	19	18	17	16
R10		ITAG				CONSTATE	
R-0h		R-0h				R-0h	
15	14	13	12	11	10	9	8
R12							
R-0h							
7	6	5	4	3	2	1	0
R12				ITAGTIMEOUT	INVREQIGNOR ED	NOTAG	WRONGITAG
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1592. PCIE_CORE_RP_I_DTI_ATS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R10	R	0h	Reserved
21-17	ITAG	R	0h	Itag value which timed out
16	CONSTATE	R	0h	When set indicates the DTI Master in connected state
15-4	R12	R	0h	Reserved
3	ITAGTIMEOUT	R/W1C	0h	When set indicates a timeout in one of the invalidation tags. Invalidation Tag timeout duration = INVTIMERCF * 16ns * INVTIMERCC
2	INVREQIGNORED	R/W1C	0h	When set indicates that the invalidation request is ignored internally by the DTI Master block
1	NOTAG	R/W1C	0h	When set indicates the DTI Slave returned an error for the connection request due to non availability of tags.
0	WRONGITAG	R/W1C	0h	When set indicates that the itag field is wrong in the invalidation completion message.

9.5.206 PCIE_CORE_RP_I_DTI_ATS_CTRL Register (Offset = 00100C9Ch) [reset = 27807A12h]

PCIE_CORE_RP_I_DTI_ATS_CTRL is shown in [Figure 9-595](#) and described in [Table 9-1594](#).

Return to [Summary Table](#).

N/A

Table 9-1593. PCIE_CORE_RP_I_DTI_ATS_CTRL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0C9Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0C9Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0C9Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0C9Ch

Figure 9-595. PCIE_CORE_RP_I_DTI_ATS_CTRL Register

31	30	29	28	27	26	25	24
R3		LDCTRL	DISCONREQ	CONREQ	INVTIMERCC		
R-0h		R/W-1h	R/W-0h	R/W-0h	R/W-78h		
23	22	21	20	19	18	17	16
INVTIMERCC				INVTIMERCF			
R/W-78h				R/W-7A12h			
15	14	13	12	11	10	9	8
INVTIMERCF							
R/W-7A12h							
7	6	5	4	3	2	1	0
INVTIMERCF							
R/W-7A12h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1594. PCIE_CORE_RP_I_DTI_ATS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	R3	R	0h	Reserved
29	LDCTRL	R/W	1h	This bit when programmed to 1 sends a disconnect request when link down reset happens and sends a connect request when link down indication bit is cleared.
28	DISCONREQ	R/W	0h	When set DTI Master triggers a disconnect sequence to the DTI Slave. This bit gets reset to 0 when the DTI master establishes a disconnection.
27	CONREQ	R/W	0h	When set DTI Master triggers a connect sequence to the DTI Slave. This bit gets reset to 0 when the DTI master establishes a connection.
26-20	INVTIMERCC	R/W	78h	This is a coarse value which the individual invalidation timers check for reporting a timeout
19-0	INVTIMERCF	R/W	7A12h	This is a master counter timeout value which triggers the invalidation tag timers to increment if an active invalidation request is present

9.5.207 PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG Register (Offset = 00100CC0h) [reset = 0h]

PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG is shown in [Figure 9-596](#) and described in [Table 9-1596](#).

Return to [Summary Table](#).

N/A

Table 9-1595.
PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CC0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CC0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CC0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CC0h

Figure 9-596. PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES3116															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES3116												SFCVCS			
R-0h												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1596. PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_VC_SELECT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES3116	R	0h	Reserved
3-0	SFCVCS	R/W	0h	The scaled flow management register is implemented per VC. However, to limit the number of registers, only one VC can be accessed at a time. This register is used to select the VC for which Scaled Flow Control Management Register is to be accessed.

9.5.208 PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_REG Register (Offset = 00100CC4h) [reset = 555h]

PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_REG is shown in [Figure 9-597](#) and described in [Table 9-1598](#).

Return to [Summary Table](#).

N/A

Table 9-1597.
PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CC4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CC4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CC4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CC4h

Figure 9-597. PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES2				RCPCS		RCHCS		RNPPCS		RNPHCS		RPPCS		RPHCS	
R-0h				R-0h		R-0h		R-0h		R-0h		R-0h		R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES1				LCPCS		LCHCS		LNPPCS		LNPHCS		LPPCS		LPHCS	
R-0h				R/W-1h		R/W-1h		R/W-1h		R/W-1h		R/W-1h		R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1598. PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RES2	R	0h	Reserved
27-26	RCPCS	R	0h	This register reflects the Completion Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.
25-24	RCHCS	R	0h	This register reflects the Completion Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.
23-22	RNPPCS	R	0h	This register reflects the Non Posted Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.
21-20	RNPHCS	R	0h	This register reflects the Non Posted Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.
19-18	RPPCS	R	0h	This register reflects the Posted Payload Credit Scale that is advertised by the remote end device during DL Feature Exchange.
17-16	RPHCS	R	0h	This register reflects the Posted Header Credit Scale that is advertised by the remote end device during DL Feature Exchange.
15-12	RES1	R	0h	Reserved
11-10	LCPCS	R/W	1h	This register can be used to program the Completion Payload Credit Scale that will be advertised by the Controller.
9-8	LCHCS	R/W	1h	This register can be used to program the Completion Header Credit Scale that will be advertised by the Controller.

**Table 9-1598. PCIE_CORE_RP_I_SCALED_FLOW_CONTROL_MGMT_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
7-6	LNPPCS	R/W	1h	This register can be used to program the Non Posted Payload Credit Scale that will be advertised by the Controller.
5-4	LNPHCS	R/W	1h	This register can be used to program the Non Posted Header Credit Scale that will be advertised by the Controller.
3-2	LPPCS	R/W	1h	This register can be used to program the Posted Payload Credit Scale that will be advertised by the Controller.
1-0	LPHCS	R/W	1h	This register can be used to program the Posted Header Credit Scale that will be advertised by the Controller.

9.5.209 PCIe_CORE_RP_I_MARGINING_PARAMETERS_1_REG Register (Offset = 00100CD0h) [reset = 05506417h]

PCIE_CORE_RP_I_MARGINING_PARAMETERS_1_REG is shown in [Figure 9-598](#) and described in [Table 9-1600](#).

[Return to Summary Table.](#)

N/A

Table 9-1599.
PCIE_CORE_RP_I_MARGINING_PARAMETERS_1_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CD0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CD0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CD0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CD0h

Figure 9-598. PCIe_CORE_RP_I_MARGINING_PARAMETERS_1_REG Register

31	30	29	28	27	26	25	24
RES		MMVO					
R-0h		R/W-5h					
23	22	21	20	19	18	17	16
MMTO						MNTS	
R/W-14h						R/W-6h	
15	14	13	12	11	10	9	8
MNTS				MNVS			
R/W-6h				R/W-20h			
7	6	5	4	3	2	1	0
MNVS			MIES	MSRM	MINDLRTS	MINDUDVS	MVS
R/W-20h			R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1600. PCIe_CORE_RP_I_MARGINING_PARAMETERS_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RES	R	0h	Reserved
29-24	MMVO	R/W	5h	Offset from default at maximum step value as percentage of one volt. A 0 value may be reported if the vendor chooses not to report the offset.
23-18	MMTO	R/W	14h	Offset from default at maximum step value as percentage of a nominal UI at 16.0 GT/s. A 0 value may be reported if the vendor chooses not to report the offset.
17-12	MNTS	R/W	6h	Number of time steps from default [to either left or right], range must be at least +/-0.2 UI. Timing offset must increase monotonically. The number of steps in both positive [toward the end of the unit interval] and negative [toward the beginning of the unit interval] must be identical.

Table 9-1600. PCIE_CORE_RP_I_MARGINING_PARAMETERS_1_REG Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
11-5	MNVS	R/W	20h	Number of voltage steps from default [either up or down], minimum range +/-50 mV as measured by 16.0 GT/s reference equalizer Voltage offset must increase monotonically. The number of steps in both positive and negative direction from the default sample location must be identical This value is undefined if M VoltageSupported is 0b.
4	MIES	R/W	1h	1b Margining will not produce errors [change in the error rate] in data stream [error sampler is independent] 0b Margining may produce errors in the data stream
3	MSRM	R/W	0h	1b - Sampling Rates M SamplingRateVoltage, M SamplingRateTiming are supported 0b - Sample Count is supported
2	MINDLRTS	R/W	1h	1b - Independent Left/Right Timing Margining is supported 0b - Independent Left/Right Timing Margining is not supported
1	MINDUDVS	R/W	1h	1b - Independent Up Down Voltage Margining is supported 0b - Independent Up Down Voltage Margining is not supported
0	MVS	R/W	1h	1b - Voltage Margining is supported 0b - Voltage Margining is not supported

9.5.210 PCIe_CORE_RP_I_MARGINING_PARAMETERS_2_REG Register (Offset = 00100CD4h) [reset = 0h]

PCIE_CORE_RP_I_MARGINING_PARAMETERS_2_REG is shown in [Figure 9-599](#) and described in [Table 9-1602](#).

[Return to Summary Table.](#)

N/A

Table 9-1601.
PCIE_CORE_RP_I_MARGINING_PARAMETERS_2_R
EG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CD4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CD4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CD4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CD4h

Figure 9-599. PCIe_CORE_RP_I_MARGINING_PARAMETERS_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES1																MML				MSRT				MSRV							
R-0h																R/W-0h				R/W-0h				R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1602. PCIe_CORE_RP_I_MARGINING_PARAMETERS_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RES1	R	0h	Reserved
16-12	MML	R/W	0h	Maximum number of Lanes minus 1 that can be margined at the same time. It is recommended that this value be greater than or equal to the number of Lanes in the Link minus 1. Encoding Behavior is undefined if software attempts to margin more than MMaxLanes+1 at the same time. Note: This value is permitted to exceed the number of Lanes in the Link minus 1.
11-6	MSRT	R/W	0h	The ratio of bits tested to bits received during timing margining. A value of 0 is a ratio of 1:64 [1 bit of every 64 bits received], and a value of 63 is a ratio of 64:64 [all bits received].
5-0	MSRV	R/W	0h	The ratio of bits tested to bits received during voltage margining. A value of 0 is a ratio of 1:64 [1 bit of every 64 bits received], and a value of 63 is a ratio of 64:64 [all bits received].

9.5.211 PCIE_CORE_RP_I_MARGINING_LOCAL_CONTROL_REG Register (Offset = 00100CD8h) [reset = 80000000h]

PCIE_CORE_RP_I_MARGINING_LOCAL_CONTROL_REG is shown in [Figure 9-600](#) and described in [Table 9-1604](#).

[Return to Summary Table.](#)

N/A

Table 9-1603.
PCIE_CORE_RP_I_MARGINING_LOCAL_CONTROL
_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CD8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CD8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CD8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CD8h

Figure 9-600. PCIE_CORE_RP_I_MARGINING_LOCAL_CONTROL_REG Register

31	30	29	28	27	26	25	24
WAWTC				RES			
R/W-4h				R-0h			
23	22	21	20	19	18	17	16
RES							
R-0h							
15	14	13	12	11	10	9	8
RES							
R-0h							
7	6	5	4	3	2	1	0
RES				DMSUSC		AMCNG4	MSR
R-0h				R/W-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1604. PCIE_CORE_RP_I_MARGINING_LOCAL_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	WAWTC	R/W	4h	When a WriteCommitted command is issued by the Controller, the PHY must respond with a Write_Ack response. The time for which the Controller waits before timing out is controlled by this register. 000: 10us 001: 100us 010: 1ms 011: 2ms 100: 10ms [default] 101: 20ms 110: 100ms 111: No Timeout
28-3	RES	R	0h	Reserved

**Table 9-1604. PCIe_CORE_RP_I_MARGINING_LOCAL_CONTROL_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2	DMSUSC	R/W	0h	By default, when a Step Margin command is received, the Controller will update Lane Margin status to Margining in Progress when an Error Count update Or a Sample Count update is received from PHY. Set this bit to 1 to not update Lane Margin Status on a Sample Count update from PHY.
1	AMCNG4	R/W	0h	By default, the Controller will process a Margin Command only if it is received while in 16GT/s PCIe_CORE_RP_L0 State. If a Margin Command is received when the link is not in Gen 4-PCIe_CORE_RP_L0 state, then the command will be ignored. If this bit is set, then the Controller accepts and stores a margin command that is received when not in Gen4 PCIe_CORE_RP_L0 state. This command will be processed when the link reaches Gen4 PCIe_CORE_RP_L0 state.
0	MSR	R/W	0h	This bit can be used to reset the Margining internal registers and Margining state machines in the Controller. When asserted: [i] The State machines will be reset to their default values. [ii] All internal FIFOs will be cleared. [iii] All the P2M and M2P registers will be reset. [iv] This does not reset the Margining Configuration and Management Registers. Margining Status register will show the last recorded status. This bit will automatically self-clear after 32-CORE_CLK cycles.

9.5.212 PCIE_CORE_RP_I_MARGINING_ERROR_STATUS1_REG Register (Offset = 00100CDCh) [reset = 0h]

PCIE_CORE_RP_I_MARGINING_ERROR_STATUS1_REG is shown in [Figure 9-601](#) and described in [Table 9-1606](#).

Return to [Summary Table](#).

N/A

Table 9-1605.
PCIE_CORE_RP_I_MARGINING_ERROR_STATUS1_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CDCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CDCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CDCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CDCh

Figure 9-601. PCIE_CORE_RP_I_MARGINING_ERROR_STATUS1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES												ISWMCLN			
R-0h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISWMC															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-1606. PCIE_CORE_RP_I_MARGINING_ERROR_STATUS1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RES	R	0h	Reserved
19-16	ISWMCLN	R	0h	This field reports the Lane Number for which the Invalid command was received. 0000: Lane 0. 0001: Lane 1. and so on.. .
15-0	ISWMC	R	0h	When the Controller receives an Invalid Margining Command from SW in its configuration register, the 16-bit command is logged in this register for debug. Only the first Error is logged in this register. Bit-20 of this register has to be cleared by local firmware before another error can be logged in this field. .

9.5.213 PCIE_CORE_RP_I_MARGINING_ERROR_STATUS2_REG Register (Offset = 00100CE0h) [reset = 0h]

PCIE_CORE_RP_I_MARGINING_ERROR_STATUS2_REG is shown in [Figure 9-602](#) and described in [Table 9-1608](#).

Return to [Summary Table](#).

N/A

Table 9-1607.
PCIE_CORE_RP_I_MARGINING_ERROR_STATUS2_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0CE0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0CE0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0CE0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0CE0h

Figure 9-602. PCIE_CORE_RP_I_MARGINING_ERROR_STATUS2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES22										UPRLN			WAWTLN		
R-0h										R-0h			R-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WAWTLN		RES12		IPHYMCLN				IPHYMC							
R-0h		R-0h		R-0h				R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-1608. PCIE_CORE_RP_I_MARGINING_ERROR_STATUS2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RES22	R	0h	Reserved
21-18	UPRLN	R	0h	This field reports the Lane Number for which the Controller received an unexpected PHY Response for Lane Margining. Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeout. 0000: Lane 0. 0001: Lane 1. and so on..
17-14	WAWTLN	R	0h	This field reports the Lane Number for which the Controller detected a 10ms timeout. 0000: Lane 0. 0001: Lane 1. and so on..
13-12	RES12	R	0h	Reserved

Table 9-1608. PCIE_CORE_RP_I_MARGINING_ERROR_STATUS2_REG Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
11-8	IPHYMCLN	R	0h	This field reports the Lane Number for which the Invalid command was received. 0000: Lane 0. 0001: Lane 1. and so on.. .
7-0	IPHYMC	R	0h	When the Controller receives an Invalid Margining Command from PHY over PIPE Interface, the 8-bit PIPE command is logged in this register for debug. Only the first Error is logged in this register. Bit-24 of this register has to be cleared by local firmware before another error can be logged in this field. .

9.5.214 PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_2_REGISTER Register (Offset = 00100D00h) [reset = 0h]

PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_2_REGISTER is shown in [Figure 9-603](#) and described in [Table 9-1610](#).

[Return to Summary Table.](#)

N/A

Table 9-1609.
PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_2_REGISTER Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D00h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D00h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D00h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D00h

Figure 9-603. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_2_REGISTER Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31	LEQRQIN	R13_11			R10	PTMCNTAINV	NFTSTOS
R-0h	R/W1C-0h	R-0h			R-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
UPRR	WAWTE	IPHYMCR	ISWMCR	MSIXMSKSETST	MSIXMSKCLST	MSIMSKSETST	MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1610. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	R31	R	0h	Reserved

**Table 9-1610. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
14	LEQRQIN	R/W1C	0h	<p>EP Mode: Indicates that the Controller hardware detected a problem with equalization and automatically requested for equalization redo at the end of the equalization.</p> <p>Controller checks for problems in Recovery.Rcvr.Lock state by comparing the Tx Coefficients agreed at end of Eq Phase2 with the Tx Coefficients received in TS1s in Recovery.Rcvr.Lock state at the end of equalization.</p> <p>Any mismatch is detected and the Request Equalization bit is set in Recovery.Rcvg.Cfg.</p> <p>This bit is set for both 8GT/s and 16GT/s equalization requests.</p> <p>[i] The Link Eq Request 8GT/s bit-5 in Link Status 2 Register will be set for 8GT/s Eq Request.</p> <p>[ii] The Link Eq Request 16.0 GT/s, bit-4 in 16.0 GT/s Status Register will be set for 16GT/s Eq Request.</p> <p>RC Mode: Indicates that the Controller received Equalization Request from downstream component.</p> <p>This bit is set for both 8GT/s and 16GT/s equalization requests.</p> <p>[i] The Link Eq Request 8GT/s bit-5 in Link Status 2 Register will be set for 8GT/s Eq Request.</p> <p>[ii] The Link Eq Request 16.0 GT/s, bit-4 in 16.0 GT/s Status Register will be set for 16GT/s Eq Request.</p>
13-11	R13_11	R	0h	Reserved
10	R10	R	0h	Reserved
9	PTMCNTAINV	R/W1C	0h	<p>This status bit indicates that the Controller automatically invalidated PTM Context because of PCIe Link exit from PCIE_CORE_RP_L0 State.</p>
8	NFTSTOS	R/W1C	0h	<p>This status bit indicates that a NFTS Timeout occurred.</p> <p>This could occur if the PHY failed to achieve lock on the receive data before the NFTS Timeout during Rx_L0s.FTS state.</p> <p>Local Firmware should consider increasing the advertized NFTS values if this event occurs.</p>
7	UPRR	R/W1C	0h	<p>This bit indicates that the Controller received an unexpected PHY Response for Lane Margining.</p> <p>Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of the MAC RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeou.</p>
6	WAWTE	R/W1C	0h	<p>This bit indicates that the Controller detected a 10ms timeout while waiting for Write Ack Lane Margining response from a PHY.</p> <p>The lane on which this timeout was detected is captured in bits 17:14 of the margining_error_status2_reg register.</p>

**Table 9-1610. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
5	IPHYMCR	R/W1C	0h	This bit validates the 8-bit command stored in bits [7:0] and the Lane Number stored in bits [11:8] of the margining_error_status1_reg register. This bit is set upon receiving the first Error. Local firmware must clear this bit by writing a 1 to this bit before another error can be logged.
4	ISWMCR	R/W1C	0h	This bit validates the 16-bit command stored in bits [15:0] and the Lane Number stored in bits [19:16] of the margining_error_status1_reg register. This bit is set upon receiving the first Error. Local firmware must clear this bit by writing a 1 to this bit before another error can be logged.
3	MSIXMSKSETST	R/W1C	0h	This status bit indicates that the MSIX Function Mask of any function, PF or VF, was programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Note that this is a Read Only Status bit. The MSIX Function Mask Clear status per-function is captured in the msix_function_mask_set_status_register. Firmware has to clear the per-function bits in msix_function_mask_set_status_register in order to clear this status bit and to deassert LOCAL_INTERRUPT.
2	MSIXMSKCLST	R/W1C	0h	This status bit indicates that the MSIX Function Mask of any function, PF or VF, was programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Note that this is a Read Only Status bit. The MSIX Function Mask Clear status per-function is captured in the msix_function_mask_cleared_status_register. Firmware has to clear the per-function bits in msix_function_mask_cleared_status_register in order to clear this status bit and to deassert LOCAL_INTERRUPT.

**Table 9-1610. PCIE_CORE_RP_I_LOCAL_ERROR_STATUS_2_REGISTER Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
1	MSIMSKSETST	R/W1C	0h	<p>This status bit indicates that One or More bits of MSI Mask of any function, PF or VF, was programmed or configured from 0 to 1 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.</p> <p>When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg .</p> <p>Note that this is a Read Only Status bit.</p> <p>The MSI Mask Clear status per-function is captured in the msi_mask_set_status_register.</p> <p>Firmware has to clear the per-function bits in msi_mask_set_status_register in order to clear this status bit and to deassert LOCAL_INTERRUPT.</p>
0	MSIMSKCLST	R/W1C	0h	<p>This status bit indicates that One or More bits of MSI Mask of any function, PF or VF, was programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.</p> <p>When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg .</p> <p>Note that this is a Read Only Status bit.</p> <p>The MSI Mask Clear status per-function is captured in the msi_mask_cleared_status_register.</p> <p>Firmware has to clear the per-function bits in msi_mask_cleared_status_register in order to clear this status bit and to deassert LOCAL_INTERRUPT.</p>

9.5.215 PCIe_CORE_RP_I_LOCAL_INTRPT_MASK_2_REG Register (Offset = 00100D04h) [reset = 4200h]

PCIE_CORE_RP_I_LOCAL_INTRPT_MASK_2_REG is shown in [Figure 9-604](#) and described in [Table 9-1612](#).

Return to [Summary Table](#).

N/A

Table 9-1611.
PCIE_CORE_RP_I_LOCAL_INTRPT_MASK_2_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D04h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D04h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D04h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D04h

Figure 9-604. PCIe_CORE_RP_I_LOCAL_INTRPT_MASK_2_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31	LEQRQINM	R13_11			R10	PCAIM	NFTSTOM
R-0h	R/W-1h	R-0h			R-0h	R/W-1h	R/W-0h
7	6	5	4	3	2	1	0
UPREM	WAWTEM	IPHYMEM	ISWMEM	MSIXMSKSET	MSIXMSKCL	MSIMSKSET	MSIMSKCL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1612. PCIe_CORE_RP_I_LOCAL_INTRPT_MASK_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	R31	R	0h	Reserved
14	LEQRQINM	R/W	1h	Mask for Link Equalization Request Interrupt.
13-11	R13_11	R	0h	Reserved
10	R10	R	0h	Reserved
9	PCAIM	R/W	1h	Mask for PTM Context Auto Invalidated event.
8	NFTSTOM	R/W	0h	Mask for NFTS Timeout.
7	UPREM	R/W	0h	Unexpected PHY Response is detected by Controller if PHY writes to the Margin Status or the Margin NAK bits of RX Margin Status 0 Register when no change in Start Margin or Margin Offset issued by Controller or after the Write Ack Wait Timeout This bit can be used to Mask asserting the LOCAL_INTERRUPT output upon this error. 1: Error is masked. 0: Error is not masked.

Table 9-1612. PCIE_CORE_RP_I_LOCAL_INTRPT_MASK_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	WAWTEM	R/W	0h	<p>When a WriteCommitted command is issued by the Controller, the PHY must respond with a Write_Ack within 10ms on the PIPE Message Bus Interface. However, if the Write_Ack is not received within 10ms, the Controller reports Timeout and stops waiting for the write_ack.</p> <p>This bit can be used to Mask asserting the LOCAL_INTERRUPT output upon this 10ms timeout.</p> <p>1: Error is masked. 0: Error is not masked.</p>
5	IPHYMEM	R/W	0h	<p>When the Controller receives a Margining Command from PHY over the PIPE Interface, it checks if the command is valid.</p> <p>The error status is logged in local_error_status_2_register.</p> <p>This bit can be used to Mask asserting the LOCAL_INTERRUPT output when the Invalid PHY Margining Error Status is set.</p> <p>1: Error is masked. 0: Error is not masked.</p>
4	ISWMEM	R/W	0h	<p>When the Controller receives a Margining Command from SW in its configuration register, it checks if the command is valid.</p> <p>The error status is logged in local_error_status_2_register.</p> <p>This bit can be used to Mask asserting the LOCAL_INTERRUPT output when the Invalid SW Margining Error Status is set.</p> <p>1: Error is masked. 0: Error is not masked.</p>
3	MSIXMSKSET	R/W	0h	Mask for MSIX Function Mask Cleared Status.
2	MSIXMSKCL	R/W	0h	Mask for MSIX Function Mask Set Status.
1	MSIMSKSET	R/W	0h	Mask for MSI Mask Set Status.
0	MSIMSKCL	R/W	0h	Mask for MSI Mask Cleared Status.

9.5.216 PCIe_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register (Offset = 00100D10h) [reset = 0h]

PCIe_CORE_RP_MSI_MASK_CLEARED_STATUS_1 is shown in [Figure 9-605](#) and described in [Table 9-1614](#).

Return to [Summary Table](#).

N/A

Table 9-1613.
PCIe_CORE_RP_MSI_MASK_CLEARED_STATUS_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D10h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D10h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D10h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D10h

Figure 9-605. PCIe_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31		VF15MSIMSKCLST	VF14MSIMSKCLST	VF13MSIMSKCLST	VF12MSIMSKCLST	VF11MSIMSKCLST	VF10MSIMSKCLST
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
VF9MSIMSKCLST	VF8MSIMSKCLST	VF7MSIMSKCLST	VF6MSIMSKCLST	VF5MSIMSKCLST	VF4MSIMSKCLST	VF3MSIMSKCLST	VF2MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
VF1MSIMSKCLST	VF0MSIMSKCLST	PF5MSIMSKCLST	PF4MSIMSKCLST	PF3MSIMSKCLST	PF2MSIMSKCLST	PF1MSIMSKCLST	PF0MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1614. PCIe_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R31	R	0h	Reserved
21	VF15MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF15 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1614. PCIE_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
20	VF14MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF14 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
19	VF13MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF13 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
18	VF12MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF12 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
17	VF11MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF11 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1614. PCIE_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
16	VF10MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF10 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
15	VF9MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF9 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
14	VF8MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF8 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
13	VF7MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF7 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1614. PCIE_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
12	VF6MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF6 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
11	VF5MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF5 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
10	VF4MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF4 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
9	VF3MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF3 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1614. PCIE_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
8	VF2MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF2 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
7	VF1MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF1 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
6	VF0MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF0 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
5	PF5MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF5 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1614. PCIE_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
4	PF4MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF4 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
3	PF3MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF3 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
2	PF2MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF2 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
1	PF1MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF1 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1614. PCIE_CORE_RP_MSI_MASK_CLEARED_STATUS_1 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
0	PF0MSIMSKCLST	R/W1C	0h	<p>Each PF has a 32-bit MSI Mask.</p> <p>This status bit is set when any of the 32-bits in PF0 MSI Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.</p> <p>When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg .</p> <p>Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>

9.5.217 PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register (Offset = 00100D14h) [reset = 0h]

PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 is shown in [Figure 9-606](#) and described in [Table 9-1616](#).

Return to [Summary Table](#).

N/A

Table 9-1615.
PCIE_CORE_RP_MSI_MASK_SET_STATUS_1
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D14h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D14h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D14h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D14h

Figure 9-606. PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31		VF15MSIMSKCLST	VF14MSIMSKCLST	VF13MSIMSKCLST	VF12MSIMSKCLST	VF11MSIMSKCLST	VF10MSIMSKCLST
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
VF9MSIMSKCLST	VF8MSIMSKCLST	VF7MSIMSKCLST	VF6MSIMSKCLST	VF5MSIMSKCLST	VF4MSIMSKCLST	VF3MSIMSKCLST	VF2MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
VF1MSIMSKCLST	VF0MSIMSKCLST	PF5MSIMSKCLST	PF4MSIMSKCLST	PF3MSIMSKCLST	PF2MSIMSKCLST	PF1MSIMSKCLST	PF0MSIMSKCLST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1616. PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R31	R	0h	Reserved
21	VF15MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF15 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1616. PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	VF14MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF14 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
19	VF13MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF13 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
18	VF12MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF12 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
17	VF11MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF11 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1616. PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VF10MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF10 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
15	VF9MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF9 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
14	VF8MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF8 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
13	VF7MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF7 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1616. PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	VF6MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF6 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
11	VF5MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF5 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
10	VF4MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF4 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
9	VF3MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF3 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1616. PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	VF2MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF2 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
7	VF1MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF1 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
6	VF0MSIMSKCLST	R/W1C	0h	Each VF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in VF0 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
5	PF5MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF5 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1616. PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PF4MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF4 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
3	PF3MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF3 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
2	PF2MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF2 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
1	PF1MSIMSKCLST	R/W1C	0h	Each PF has a 32-bit MSI Mask. This status bit is set when any of the 32-bits in PF1 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1616. PCIE_CORE_RP_MSI_MASK_SET_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PF0MSIMSKCLST	R/W1C	0h	<p>Each PF has a 32-bit MSI Mask.</p> <p>This status bit is set when any of the 32-bits in PF0 MSI Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSI Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.</p> <p>When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg .</p> <p>Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>

9.5.218 PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register (Offset = 00100D18h) [reset = 0h]

PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 is shown in [Figure 9-607](#) and described in [Table 9-1618](#).

Return to [Summary Table](#).

N/A

Table 9-1617.
PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D18h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D18h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D18h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D18h

Figure 9-607. PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31		VF15MSIXMSK CLST	VF14MSIXMSK CLST	VF13MSIXMSK CLST	VF12MSIXMSK CLST	VF11MSIXMSK CLST	VF10MSIXMSK CLST
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
VF9MSIXMSKC LST	VF8MSIXMSKC LST	VF7MSIXMSKC LST	VF6MSIXMSKC LST	VF5MSIXMSKC LST	VF4MSIXMSKC LST	VF3MSIXMSKC LST	VF2MSIXMSKC LST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
VF1MSIXMSKC LST	VF0MSIXMSKC LST	PF5MSIXMSKC LST	PF4MSIXMSKC LST	PF3MSIXMSKC LST	PF2MSIXMSKC LST	PF1MSIXMSKC LST	PF0MSIXMSKC LST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1618. PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R31	R	0h	Reserved
21	VF15MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF15 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1618. PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	VF14MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF14 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
19	VF13MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF13 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
18	VF12MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF12 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
17	VF11MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF11 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>

Table 9-1618. PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	VF10MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF10 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
15	VF9MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF9 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
14	VF8MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF8 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
13	VF7MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF7 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1618. PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	VF6MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF6 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
11	VF5MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF5 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
10	VF4MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF4 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
9	VF3MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF3 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>

Table 9-1618. PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	VF2MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF2 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
7	VF1MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF1 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
6	VF0MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF0 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
5	PF5MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF5 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1618. PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PF4MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF4 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
3	PF3MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF3 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
2	PF2MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF2 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
1	PF1MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF1 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1618. PCIE_CORE_RP_MSIX_FUNCTION_MASK_CLEARED_STATUS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PF0MSIXMSKCLST	R/W1C	0h	<p>Each PF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the PF0 MSIX Function Mask is programmed or configured from 1 to 0 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.</p> <p>When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg .</p> <p>Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>

9.5.219 PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register (Offset = 00100D1Ch) [reset = 0h]

PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 is shown in [Figure 9-608](#) and described in [Table 9-1620](#).

Return to [Summary Table](#).

N/A

Table 9-1619.
PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0D1Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0D1Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0D1Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0D1Ch

Figure 9-608. PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31		VF15MSIXMSK CLST	VF14MSIXMSK CLST	VF13MSIXMSK CLST	VF12MSIXMSK CLST	VF11MSIXMSK CLST	VF10MSIXMSK CLST
R-0h		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
VF9MSIXMSKC LST	VF8MSIXMSKC LST	VF7MSIXMSKC LST	VF6MSIXMSKC LST	VF5MSIXMSKC LST	VF4MSIXMSKC LST	VF3MSIXMSKC LST	VF2MSIXMSKC LST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
VF1MSIXMSKC LST	VF0MSIXMSKC LST	PF5MSIXMSKC LST	PF4MSIXMSKC LST	PF3MSIXMSKC LST	PF2MSIXMSKC LST	PF1MSIXMSKC LST	PF0MSIXMSKC LST
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1620. PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	R31	R	0h	Reserved
21	VF15MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF15 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1620. PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
20	VF14MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF14 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
19	VF13MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF13 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
18	VF12MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF12 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
17	VF11MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF11 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1620. PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
16	VF10MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF10 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
15	VF9MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF9 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
14	VF8MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF8 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>
13	VF7MSIXMSKCLST	R/W1C	0h	<p>Each VF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the VF7 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>

**Table 9-1620. PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
12	VF6MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF6 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
11	VF5MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF5 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
10	VF4MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF4 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
9	VF3MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF3 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1620. PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
8	VF2MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF2 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
7	VF1MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF1 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
6	VF0MSIXMSKCLST	R/W1C	0h	Each VF has a 1-bit MSIX Function Mask. This status bit is set when the VF0 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
5	PF5MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF5 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

**Table 9-1620. PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	PF4MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF4 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
3	PF3MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF3 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
2	PF2MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF2 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.
1	PF1MSIXMSKCLST	R/W1C	0h	Each PF has a 1-bit MSIX Function Mask. This status bit is set when the PF1 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW. This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg. When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg . Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.

Table 9-1620. PCIE_CORE_RP_MSIX_FUNCTION_MASK_SET_STATUS_1 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
0	PF0MSIXMSKCLST	R/W1C	0h	<p>Each PF has a 1-bit MSIX Function Mask.</p> <p>This status bit is set when the PF0 MSIX Function Mask is programmed or configured from 0 to 1 by Local Firmware Or Host SW.</p> <p>This bit is set only when the MSIX Function Mask Change Enhanced Interrupt Enable bit is set by the User in debug_mux_control_2_reg.</p> <p>When this status bit is set, the Controller asserts LOCAL_INTERRUPT if not masked in local_intrpt_mask_2_reg .</p> <p>Firmware has to clear this bit in order to deassert LOCAL_INTERRUPT.</p>

9.5.220 PCIE_CORE_RP_I_LD_CTRL Register (Offset = 00100DA0h) [reset = 015F5E10h]

PCIE_CORE_RP_I_LD_CTRL is shown in [Figure 9-609](#) and described in [Table 9-1622](#).

Return to [Summary Table](#).

N/A

**Table 9-1621. PCIE_CORE_RP_I_LD_CTRL
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DA0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DA0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DA0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DA0h

Figure 9-609. PCIE_CORE_RP_I_LD_CTRL Register

31	30	29	28	27	26	25	24
R7							AUTO_EN
R-0h							R/W-1h
23	22	21	20	19	18	17	16
LDTIMER							
R/W-005F5E10h							
15	14	13	12	11	10	9	8
LDTIMER							
R/W-005F5E10h							
7	6	5	4	3	2	1	0
LDTIMER							
R/W-005F5E10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1622. PCIE_CORE_RP_I_LD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	R7	R	0h	Reserved
24	AUTO_EN	R/W	1h	This bit when set indicates that the link down indication auto reset is enabled
23-0	LDTIMER	R/W	005F5E10h	This is a counter timeout value which triggers the internal logic to reset the link down indication bit in the AXI Configuration registers

9.5.221 PCIE_CORE_RP_RX_ELEC_IDLE_FILTER_CONTROL Register (Offset = 00100DA4h) [reset = 04200000h]

PCIE_CORE_RP_RX_ELEC_IDLE_FILTER_CONTROL is shown in [Figure 9-610](#) and described in [Table 9-1624](#).

Return to [Summary Table](#).

N/A

Table 9-1623.
PCIE_CORE_RP_RX_ELEC_IDLE_FILTER_CONTROL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DA4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DA4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DA4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DA4h

Figure 9-610. PCIE_CORE_RP_RX_ELEC_IDLE_FILTER_CONTROL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GFLCP								GFLCC							
R/W-4h								R/W-20h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVGFLD													GFLD		
R-0h													R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1624. PCIE_CORE_RP_RX_ELEC_IDLE_FILTER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GFLCP	R/W	4h	This controls the glitch filter on PM Clock domain. This counter indicates the number of PM Clocks the glitch will be filtered out. The total delay of the glitch filter is calculated as [PM Clock Period * Number of PM Clocks] this delay should be same or close enough for both Core Clock[GFLCC] and PM Clock[GFLCP]
23-16	GFLCC	R/W	20h	This controls the glitch filter on CORE Clock domain. This counter indicates the number of CORE Clocks the glitch will be filtered out. The total delay of the glitch filter is calculated as [CORE Clock Period * Number of CORE Clocks] this delay should be same or close enough for both CORE Clock[GFLCC] and PM Clock[GFLCP]
15-2	RSVGFLD	R	0h	Reserved

**Table 9-1624. PCIE_CORE_RP_RX_ELEC_IDLE_FILTER_CONTROL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
1-0	GFLD	R/W	0h	<p>By default controller enables glitch filter on all lanes. Setting this bit to one makes the controller to disable the glitch filter on that corresponding lanes in which the bit is set. When all bits are set to one the Glitch filter is completely bypassed, When any bit is zero glitch filter is enabled, and de-glitching is done only on the lanes that are set to zero</p>

9.5.222 PCIE_CORE_RP_I_PTM_LOCAL_CONTROL_REG Register (Offset = 00100DA8h) [reset = 1110h]

PCIE_CORE_RP_I_PTM_LOCAL_CONTROL_REG is shown in [Figure 9-611](#) and described in [Table 9-1626](#).

Return to [Summary Table](#).

N/A

Table 9-1625.
PCIE_CORE_RP_I_PTM_LOCAL_CONTROL_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DA8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DA8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DA8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DA8h

Figure 9-611. PCIE_CORE_RP_I_PTM_LOCAL_CONTROL_REG Register

31	30	29	28	27	26	25	24
RES29			DAINV CNT	INVPTMCNT	RES18		
R-0h			R/W-0h	R/W-0h	R-0h		
23	22	21	20	19	18	17	16
RES18						PTMRSEN	PTMRSM
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PTMRINT				PTMRFRVL			
R/W-1h				R/W-1h			
7	6	5	4	3	2	1	0
PTMRFRSC				RES2		PTMRQEN	PTMRQM
R/W-1h				R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1626. PCIE_CORE_RP_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RES29	R	0h	Reserved
28	DAINV CNT	R/W	0h	By default, the Controller automatically invalidates PTM Context when the LTSSM exits PCIE_CORE_RP_L0 state. Client may disable this by writing a 1 to this register.
27	INVPTMCNT	R/W	0h	Client Firmware may write a 1 to this bit in order to reset the PTM Context. This is a write-only bit. Controller internally clears this bit. Read from this bit returns 0. EP Mode: Resets the PTM Request State Machine. PTM Context is Cleared. RP Mode: Resets the PTM Response State Machine. PTM Context is Cleared.
26-18	RES18	R	0h	Reserved

Table 9-1626. PCIE_CORE_RP_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	PTMRSEN	R/W	0h	<p>EP Mode: Reserved</p> <p>RP Mode: This bit enables Controller [RP] to respond to the received PTM Requests. PTM Response/PTM ResponseD is determined by the PTM Response Mode bit. 1 : Controller automatically responds with Response/ResponseD messages. 0 : Controller does not respond for PTM Requests. [PTM Feature is Bypassed.]</p>
16	PTMRSM	R/W	0h	<p>EP Mode: Reserved.</p> <p>RP Mode: This bit is used to control the number of PTM dialogs used during each PTM Master Time Request. 1 : Two Dialog Mode - Each PTM Context will have Response followed by ResponseD. Example: Dialog 0: Request -> Response. Dialog 1: Request -> ResponseD Dialog 2: Request -> Response Dialog 3: Request -> ResponseD 0 : Continuous Dialog Mode - Each PTM Context will have Only ResponseD. Example: Dialog 0: Request -> Response. Dialog 1: Request -> ResponseD Dialog 2: Request -> ResponseD Dialog 3: Request -> ResponseD</p>

Table 9-1626. PCIE_CORE_RP_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	PTMRINT	R/W	1h	<p>EP Mode:</p> <p>In Single, Periodic Request Mode, this field is used to control the time interval [in us] between PTM Requests within a PTM Context. This represents the time the Requester State Machine waits in the WAIT_1US_STATE.</p> <p>0001 - 1 0010 - 2 0011 - 3 0100 - 4 0101 - 5 0110 - 6 0111 - 7 1000 - 8 1001 - 9 .. 1111 - 15</p> <p>This value is in [us].</p> <p>RP Mode: Reserved.</p>
11-8	PTMRFRVL	R/W	1h	<p>EP Mode:</p> <p>In Periodic Request Mode, this field is used to control the time interval [value] between successive PTM Context Refresh. This represents the time the Requester State Machine waits in the VALID_PTM_CONTEXT_STATE.</p> <p>0001 - 1 0010 - 2 0011 - 3 0100 - 4 0101 - 5 0110 - 6 0111 - 7 1000 - 8 1001 - 9 1010 - 1111 Reserved</p> <p>This value is multiplied with the scale to determine the PTM Request Time Interval.</p> <p>RP Mode: Reserved.</p>

Table 9-1626. PCIE_CORE_RP_I_PTM_LOCAL_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	PTMRFRSC	R/W	1h	<p>EP Mode:</p> <p>In Periodic Request Mode, this field is used to control the time interval [scale] between successive PTM Context Refresh. This represents the time the Requester State Machine waits in the VALID_PTM_CONTEXT_STATE.</p> <p>0000 - 1 us 0001 - 10 us 0010 - 100 us 0011 - 1 ms 0100 - 10 ms 0101 - 100 ms 0110 - 1 s 0111 - 10 s 1000 - 100 s 1001 - 1111 - Reserved</p> <p>RP Mode: Reserved.</p>
3-2	RES2	R	0h	Reserved
1	PTMRQEN	R/W	0h	<p>EP Mode:</p> <p>This enables Endpoint to request for PTM Master Time. 1 : PTM Requests are Enabled.</p> <p>In Single Request Mode, this bit is used to trigger PTM dialog to obtain PTM Master time exactly once. This bit is auto-cleared after the PTM Master time is obtained.</p> <p>In Periodic Request Mode, this bit enables periodic requests for PTM Master Time. This bit remains set till it is cleared by the EP local firmware. 0 : PTM Requests are Disabled. [PTM Feature is Bypassed.]</p> <p>User may disable PTM requests in the Controller and, if required, generate requests from Client Master Interface.</p> <p>RP Mode: Reserved.</p>
0	PTMRQM	R/W	0h	<p>EP Mode:</p> <p>This bit controls the pattern of PTM Requests issued by the Endpoint. 0: Single Request Mode. 1: Periodic Request Mode.</p> <p>In Single Request Mode, Endpoint initiates one or two PTM Dialogs till the PTM Master Time is obtained.</p> <p>In Periodic Request Mode, Endpoint initiates PTM Dialogs and obtains PTM Master at periodic intervals. The period is programmable.</p> <p>RP Mode: Reserved.</p>

9.5.223 PCIE_CORE_RP_I_PTM_LOCAL_STATUS_REG Register (Offset = 00100DACH) [reset = 0h]

PCIE_CORE_RP_I_PTM_LOCAL_STATUS_REG is shown in [Figure 9-612](#) and described in [Table 9-1628](#).

Return to [Summary Table](#).

N/A

Table 9-1627.
PCIE_CORE_RP_I_PTM_LOCAL_STATUS_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DACH
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DACH
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DACH
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DACH

Figure 9-612. PCIE_CORE_RP_I_PTM_LOCAL_STATUS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES3															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES3												PTMCNST			
R-0h												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-1628. PCIE_CORE_RP_I_PTM_LOCAL_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RES3	R	0h	Reserved
3-0	PTMCNST	R	0h	Reflects the current status of the PTM Context. In EP Mode: 0000 - Invalid PTM Context 0001 - Dialog 1 PTM Request Sent 0011 - Dialog 1 PTM Response Received 0111 - Dialog 2 PTM Request Sent 1111 - Dialog 2 PTM ResponseD Received and PTM Context Valid In RP Mode: 0000 - Invalid PTM Context 0001 - Dialog 1 PTM Request Received 0011 - Dialog 1 PTM Response Sent 0111 - Dialog 2 PTM Request Received 1111 - Dialog 2 PTM ResponseD Sent and PTM Context Valid

9.5.224 PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register (Offset = 00100DB0h) [reset = 0h]

PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_INDEX_REG is shown in [Figure 9-613](#) and described in [Table 9-1630](#).

Return to [Summary Table](#).

N/A

Table 9-1629.
PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_I
NDEX_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DB0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DB0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DB0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DB0h

Figure 9-613. PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES4															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES4												PTMLATIN			
R-0h												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1630. PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_INDEX_REG Register Field
Descriptions

Bit	Field	Type	Reset	Description
31-4	RES4	R	0h	Reserved
3-0	PTMLATIN	R/W	0h	This is used by FW to select the speed for which the Latency parameters are to be programmed. FW is required to set this to each of the supported speeds and program the corresponding latency parameters in the PTM Latency Parameters Register. 0000 - Gen1 Speed Select 0001 - Gen2 Speed Select 0010 - Gen3 Speed Select 0011 - Gen4 Speed Select Others - Reserved

9.5.225 PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_REG Register (Offset = 00100DB4h) [reset = 0h]

PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_REG is shown in [Figure 9-614](#) and described in [Table 9-1632](#).

Return to [Summary Table](#).

N/A

Table 9-1631.
PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_
REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DB4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DB4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DB4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DB4h

Figure 9-614. PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RXDLTUN				TXDLTUN				RES20				PTMRXLAT			
R/W-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMRXLAT						PTMTXLAT									
R/W-0h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1632. PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RXDLTUN	R/W	0h	<p>In EP Mode: This field can be used to add a fixed offset to the captured timestamps t4 and t4_tick.</p> <p>In RP Mode: This field can be used to add a fixed offset to the captured timestamps t2 and t2_tick.</p> <p>Encoding: 0000: + 0 ns 0001: + 1ns 0010: + 2ns 1111: + 15ns</p> <p>Separate value can be programmed for each supported speed of operation.</p> <p>The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding value be programmed into this register.</p>

**Table 9-1632. PCIE_CORE_RP_I_PTM_LATENCY_PARAMETERS_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
27-24	TXDLTUN	R/W	0h	<p>In EP Mode: This field can be used to add a fixed offset to the captured timestamps t1 and t1_tick.</p> <p>In RP Mode: This field can be used to add a fixed offset to the captured timestamps t3 and t3_tick.</p> <p>Encoding: 0000: + 0 ns 0001: + 1ns 0010: + 2ns 1111: + 15ns</p> <p>Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding value be programmed into this register.</p>
23-20	RES20	R	0h	Reserved
19-10	PTMRXLAT	R/W	0h	<p>This field should be programmed with the parameter Receive Latency in [ns] from the PHY Datasheet. Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding latency be programmed into this register.</p>
9-0	PTMTXLAT	R/W	0h	<p>This field should be programmed with the parameter Transmit Latency in [ns] from the PHY Datasheet. Separate value can be programmed for each supported speed of operation. The speed of operation must first be programmed in the PTM Latency Parameters Index Register and then the corresponding latency be programmed into this register.</p>

9.5.226 PCIE_CORE_RP_I_PTM_CONTEXT_1_REG Register (Offset = 00100DB8h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_1_REG is shown in [Figure 9-615](#) and described in [Table 9-1634](#).

Return to [Summary Table](#).

N/A

Table 9-1633.
PCIE_CORE_RP_I_PTM_CONTEXT_1_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DB8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DB8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DB8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DB8h

Figure 9-615. PCIE_CORE_RP_I_PTM_CONTEXT_1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT1T2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1634. PCIE_CORE_RP_I_PTM_CONTEXT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT1T2	R	0h	EP Mode : Represents the lower 32-bits of timestamp t1 in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t2 in [ns] as recorded by RP.

9.5.227 PCIE_CORE_RP_I_PTM_CONTEXT_2_REG Register (Offset = 00100DBCh) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_2_REG is shown in [Figure 9-616](#) and described in [Table 9-1636](#).

Return to [Summary Table](#).

N/A

Table 9-1635.
PCIE_CORE_RP_I_PTM_CONTEXT_2_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DBCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DBCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DBCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DBCh

Figure 9-616. PCIE_CORE_RP_I_PTM_CONTEXT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT1T2U																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1636. PCIE_CORE_RP_I_PTM_CONTEXT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT1T2U	R	0h	EP Mode : Represents the upper 32-bits of timestamp t1 in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t2 in [ns] as recorded by RP.

9.5.228 PCIE_CORE_RP_I_PTM_CONTEXT_3_REG Register (Offset = 00100DC0h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_3_REG is shown in [Figure 9-617](#) and described in [Table 9-1638](#).

Return to [Summary Table](#).

N/A

Table 9-1637.
PCIE_CORE_RP_I_PTM_CONTEXT_3_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DC0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DC0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DC0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DC0h

Figure 9-617. PCIE_CORE_RP_I_PTM_CONTEXT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT4T3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1638. PCIE_CORE_RP_I_PTM_CONTEXT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT4T3	R	0h	EP Mode : Represents the lower 32-bits of timestamp t4 in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t3 in [ns] as recorded by RP.

9.5.229 PCIe_CORE_RP_I_PTM_CONTEXT_4_REG Register (Offset = 00100DC4h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_4_REG is shown in [Figure 9-618](#) and described in [Table 9-1640](#).

Return to [Summary Table](#).

N/A

Table 9-1639.
PCIE_CORE_RP_I_PTM_CONTEXT_4_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DC4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DC4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DC4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DC4h

Figure 9-618. PCIe_CORE_RP_I_PTM_CONTEXT_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT4T3U																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1640. PCIe_CORE_RP_I_PTM_CONTEXT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT4T3U	R	0h	EP Mode : Represents the upper 32-bits of timestamp t4 in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t3 in [ns] as recorded by RP.

9.5.230 PCIE_CORE_RP_I_PTM_CONTEXT_5_REG Register (Offset = 00100DC8h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_5_REG is shown in [Figure 9-619](#) and described in [Table 9-1642](#).

Return to [Summary Table](#).

N/A

Table 9-1641.
PCIE_CORE_RP_I_PTM_CONTEXT_5_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DC8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DC8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DC8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DC8h

Figure 9-619. PCIE_CORE_RP_I_PTM_CONTEXT_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT1KT2K																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1642. PCIE_CORE_RP_I_PTM_CONTEXT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT1KT2K	R	0h	EP Mode : Represents the lower 32-bits of timestamp t1_tick in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t2_tick in [ns] as recorded by RP.

9.5.231 PCIE_CORE_RP_I_PTM_CONTEXT_6_REG Register (Offset = 00100DCCh) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_6_REG is shown in [Figure 9-620](#) and described in [Table 9-1644](#).

Return to [Summary Table](#).

N/A

Table 9-1643.
PCIE_CORE_RP_I_PTM_CONTEXT_6_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DCCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DCCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DCCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DCCh

Figure 9-620. PCIE_CORE_RP_I_PTM_CONTEXT_6_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT1KT2KU																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1644. PCIE_CORE_RP_I_PTM_CONTEXT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT1KT2KU	R	0h	EP Mode : Represents the upper 32-bits of timestamp t1_tick in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t2_tick in [ns] as recorded by RP.

9.5.232 PCIE_CORE_RP_I_PTM_CONTEXT_7_REG Register (Offset = 00100DD0h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_7_REG is shown in [Figure 9-621](#) and described in [Table 9-1646](#).

Return to [Summary Table](#).

N/A

Table 9-1645.
PCIE_CORE_RP_I_PTM_CONTEXT_7_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DD0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DD0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DD0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DD0h

Figure 9-621. PCIE_CORE_RP_I_PTM_CONTEXT_7_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT4KT3K																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1646. PCIE_CORE_RP_I_PTM_CONTEXT_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT4KT3K	R	0h	EP Mode : Represents the lower 32-bits of timestamp t4_tick in [ns] as recorded by Endpoint. RP Mode : Represents the lower 32-bits of timestamp t3_tick in [ns] as recorded by RP.

9.5.233 PCIE_CORE_RP_I_PTM_CONTEXT_8_REG Register (Offset = 00100DD4h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_8_REG is shown in [Figure 9-622](#) and described in [Table 9-1648](#).

Return to [Summary Table](#).

N/A

Table 9-1647.
PCIE_CORE_RP_I_PTM_CONTEXT_8_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DD4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DD4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DD4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DD4h

Figure 9-622. PCIE_CORE_RP_I_PTM_CONTEXT_8_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT4KT3KU																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1648. PCIE_CORE_RP_I_PTM_CONTEXT_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT4KT3KU	R	0h	EP Mode : Represents the upper 32-bits of timestamp t4_tick in [ns] as recorded by Endpoint. RP Mode : Represents the upper 32-bits of timestamp t3_tick in [ns] as recorded by RP.

9.5.234 PCIE_CORE_RP_I_PTM_CONTEXT_9_REG Register (Offset = 00100DD8h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_9_REG is shown in [Figure 9-623](#) and described in [Table 9-1650](#).

Return to [Summary Table](#).

N/A

Table 9-1649.
PCIE_CORE_RP_I_PTM_CONTEXT_9_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DD8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DD8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DD8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DD8h

Figure 9-623. PCIE_CORE_RP_I_PTM_CONTEXT_9_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMT3MT2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1650. PCIE_CORE_RP_I_PTM_CONTEXT_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMT3MT2	R	0h	Propagation Delay. EP Mode : Represents the Propagation Delay [t3 - t2] in [ns] as received in ResponseD Message by Endpoint. RP Mode - Reserved.

9.5.235 PCIE_CORE_RP_I_PTM_CONTEXT_10_REG Register (Offset = 00100DDCh) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_10_REG is shown in [Figure 9-624](#) and described in [Table 9-1652](#).

Return to [Summary Table](#).

N/A

Table 9-1651.
PCIE_CORE_RP_I_PTM_CONTEXT_10_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DDCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DDCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DDCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DDCh

Figure 9-624. PCIE_CORE_RP_I_PTM_CONTEXT_10_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMMSTT1T																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1652. PCIE_CORE_RP_I_PTM_CONTEXT_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMMSTT1T	R	0h	EP Mode - Represents the lower 32-bits of PTM Master Time at timestamp t1_tick in [ns] as computed by Endpoint. RP Mode - Reserved.

9.5.236 PCIE_CORE_RP_I_PTM_CONTEXT_11_REG Register (Offset = 00100DE0h) [reset = 0h]

PCIE_CORE_RP_I_PTM_CONTEXT_11_REG is shown in [Figure 9-625](#) and described in [Table 9-1654](#).

Return to [Summary Table](#).

N/A

Table 9-1653.
PCIE_CORE_RP_I_PTM_CONTEXT_11_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DE0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DE0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DE0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DE0h

Figure 9-625. PCIE_CORE_RP_I_PTM_CONTEXT_11_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTMMSTT1TU																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-1654. PCIE_CORE_RP_I_PTM_CONTEXT_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTMMSTT1TU	R	0h	EP Mode - Represents the upper 32-bits of PTM Master Time at timestamp t1_tick in [ns] as computed by Endpoint. RP Mode - Reserved.

9.5.237 PCIe_CORE_RP_I_ASF_INTRPT_STATUS Register (Offset = 00100DECh) [reset = 0h]

PCIe_CORE_RP_I_ASF_INTRPT_STATUS is shown in [Figure 9-626](#) and described in [Table 9-1656](#).

Return to [Summary Table](#).

N/A

Table 9-1655.
PCIe_CORE_RP_I_ASF_INTRPT_STATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DECh

Figure 9-626. PCIe_CORE_RP_I_ASF_INTRPT_STATUS Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRER	PROTER	TRANSTOER	CSRER	DAPER	SRUCORER	SRCORER
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1656. PCIe_CORE_RP_I_ASF_INTRPT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRER	R/W1C	0h	Integrity error interrupt
5	PROTER	R/W1C	0h	Protocol error interrupt
4	TRANSTOER	R/W1C	0h	Transaction timeouts interrupt
3	CSRER	R/W1C	0h	Configuration and status registers error interrupt
2	DAPER	R/W1C	0h	Data and address paths error interrupt
1	SRUCORER	R/W1C	0h	SRAM Uncorrectable error interrupt
0	SRCORER	R/W1C	0h	SRAM Correctable error interrupt

9.5.238 PCIE_CORE_RP_I_ASF_INTRPT_RAW_STATUS Register (Offset = 00100DF0h) [reset = 0h]

PCIE_CORE_RP_I_ASF_INTRPT_RAW_STATUS is shown in [Figure 9-627](#) and described in [Table 9-1658](#).

Return to [Summary Table](#).

N/A

Table 9-1657.
PCIE_CORE_RP_I_ASF_INTRPT_RAW_STATUS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DF0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DF0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DF0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DF0h

Figure 9-627. PCIE_CORE_RP_I_ASF_INTRPT_RAW_STATUS Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRER	PROTER	TRANSTOER	CSRER	DAPER	SRUCORER	SRCORER
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1658. PCIE_CORE_RP_I_ASF_INTRPT_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRER	R/W1C	0h	Integrity error interrupt
5	PROTER	R/W1C	0h	Protocol error interrupt
4	TRANSTOER	R/W1C	0h	Transaction timeouts interrupt
3	CSRER	R/W1C	0h	Configuration and status registers error interrupt
2	DAPER	R/W1C	0h	Data and address paths error interrupt
1	SRUCORER	R/W1C	0h	SRAM Uncorrectable error interrupt
0	SRCORER	R/W1C	0h	SRAM Correctable error interrupt

9.5.239 PCIe_CORE_RP_I_ASF_INTRPT_MASK_REG Register (Offset = 00100DF4h) [reset = 3Fh]

PCIe_CORE_RP_I_ASF_INTRPT_MASK_REG is shown in [Figure 9-628](#) and described in [Table 9-1660](#).

Return to [Summary Table](#).

N/A

Table 9-1659.
PCIe_CORE_RP_I_ASF_INTRPT_MASK_REG
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DF4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DF4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DF4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DF4h

Figure 9-628. PCIe_CORE_RP_I_ASF_INTRPT_MASK_REG Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRERM	PROTERM	TRANTOEM	CSRERM	DAPERM	SRUCORERM	SRCORERM
R-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1660. PCIe_CORE_RP_I_ASF_INTRPT_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRERM	R/W	0h	Mask bit for Integrity error interrupt
5	PROTERM	R/W	1h	Mask bit for Protocol error interrupt
4	TRANTOEM	R/W	1h	Mask bit for Transaction timeouts interrupt
3	CSRERM	R/W	1h	Mask bit for Configuration and status registers error interrupt
2	DAPERM	R/W	1h	Mask bit for Data and address paths error interrupt
1	SRUCORERM	R/W	1h	Mask bit for SRAM Uncorrectable error interrupt
0	SRCORERM	R/W	1h	Mask bit for SRAM Correctable error interrupt

9.5.240 PCIE_CORE_RP_I_ASF_INTRPT_TEST Register (Offset = 00100DF8h) [reset = 0h]

PCIE_CORE_RP_I_ASF_INTRPT_TEST is shown in [Figure 9-629](#) and described in [Table 9-1662](#).

Return to [Summary Table](#).

N/A

Table 9-1661. PCIE_CORE_RP_I_ASF_INTRPT_TEST Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DF8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DF8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DF8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DF8h

Figure 9-629. PCIE_CORE_RP_I_ASF_INTRPT_TEST Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRERT	PROTERT	TRANTOET	CSRERT	DAPERT	SRUCORERT	SRCORERT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1662. PCIE_CORE_RP_I_ASF_INTRPT_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRERT	R/W	0h	Test bit for Integrity error interrupt
5	PROTERT	R/W	0h	Test bit for Protocol error interrupt
4	TRANTOET	R/W	0h	Test bit for Transaction timeouts interrupt
3	CSRERT	R/W	0h	Test bit for Configuration and status registers error interrupt
2	DAPERT	R/W	0h	Test bit for Data and address paths error interrupt
1	SRUCORERT	R/W	0h	Test bit for SRAM Uncorrectable error interrupt
0	SRCORERT	R/W	0h	Test bit for SRAM Correctable error interrupt

9.5.241 PCIE_CORE_RP_I_ASF_INTRPT_FATAL_NONFATAL_SEL Register (Offset = 00100DFCh) [reset = 3Fh]

PCIE_CORE_RP_I_ASF_INTRPT_FATAL_NONFATAL_SEL is shown in [Figure 9-630](#) and described in [Table 9-1664](#).

[Return to Summary Table.](#)

N/A

Table 9-1663.
PCIE_CORE_RP_I_ASF_INTRPT_FATAL_NONFATAL_SEL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0DFCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0DFCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0DFCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0DFCh

Figure 9-630. PCIE_CORE_RP_I_ASF_INTRPT_FATAL_NONFATAL_SEL Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
R31							
R-0h							
7	6	5	4	3	2	1	0
R31	INTEGRERS	PROTERS	TRANTOES	CSRERS	DAPERS	SRUCORERS	SRCORERS
R-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1664. PCIE_CORE_RP_I_ASF_INTRPT_FATAL_NONFATAL_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	R31	R	0h	Reserved
6	INTEGRERS	R/W	0h	Enable Integrity error as Fatal
5	PROTERS	R/W	1h	Enable protocol interrupt as fatal
4	TRANTOES	R/W	1h	Enable transaction timeouts interrupt as fatal
3	CSRERS	R/W	1h	Enable configuration and status registers interrupt as fatal
2	DAPERS	R/W	1h	Enable data and address paths interrupt as fatal
1	SRUCORERS	R/W	1h	Enable SRAM Uncorrectable interrupt as fatal
0	SRCORERS	R/W	1h	Enable SRAM correctable interrupt as fatal

9.5.242 PCIE_CORE_RP_I_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 00100E00h) [reset = 0h]

PCIE_CORE_RP_I_ASF_SRAM_CORR_FAULT_STATUS is shown in [Figure 9-631](#) and described in [Table 9-1666](#).

Return to [Summary Table](#).

N/A

Table 9-1665.
PCIE_CORE_RP_I_ASF_SRAM_CORR_FAULT_STAT
US Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E00h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E00h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E00h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E00h

Figure 9-631. PCIE_CORE_RP_I_ASF_SRAM_CORR_FAULT_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRCORFI								SRCORFADR																							
R-0h								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 9-1666. PCIE_CORE_RP_I_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SRCORFI	R	0h	This ENCODING indicates which SRAM Instance has a Correctable Fault. The Encoding of the SRAM is shown in Table 26
23-0	SRCORFADR	R	0h	This indicates the address where the Correctable fault was observed.

9.5.243 PCIe_CORE_RP_I_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 00100E04h) [reset = 0h]

PCIE_CORE_RP_I_ASF_SRAM_UNCORR_FAULT_STATUS is shown in [Figure 9-632](#) and described in [Table 9-1668](#).

Return to [Summary Table](#).

N/A

Table 9-1667.
PCIE_CORE_RP_I_ASF_SRAM_UNCORR_FAULT_S
TATUS Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E04h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E04h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E04h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E04h

Figure 9-632. PCIe_CORE_RP_I_ASF_SRAM_UNCORR_FAULT_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRUCORFI								SRUCRFADR																							
R-0h								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 9-1668. PCIe_CORE_RP_I_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SRUCORFI	R	0h	This ENCODING indicates which SRAM Instance has a Uncorrectable Fault. The Encoding of the SRAM is shown in Table 26
23-0	SRUCRFADR	R	0h	This indicates the address where the Uncorrectable fault was observed.

9.5.244 PCIE_CORE_RP_I_ASF_SRAM_FAULT_STATSTICS Register (Offset = 00100E08h) [reset = 0h]

PCIE_CORE_RP_I_ASF_SRAM_FAULT_STATSTICS is shown in [Figure 9-633](#) and described in [Table 9-1670](#).

Return to [Summary Table](#).

N/A

Table 9-1669.
PCIE_CORE_RP_I_ASF_SRAM_FAULT_STATSTICS
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E08h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E08h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E08h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E08h

Figure 9-633. PCIE_CORE_RP_I_ASF_SRAM_FAULT_STATSTICS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRUCORFS																SRCORFS															
R/W1C-0h																R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1670. PCIE_CORE_RP_I_ASF_SRAM_FAULT_STATSTICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SRUCORFS	R/W1C	0h	Counts the number of SRAM Uncorrectable errors seen.
15-0	SRCORFS	R/W1C	0h	Counts the number of SRAM Correctable errors seen.

9.5.245 PCIe_CORE_RP_I_ASF_TRANS_TO_CTRL Register (Offset = 00100E0Ch) [reset = 0h]

PCIe_CORE_RP_I_ASF_TRANS_TO_CTRL is shown in [Figure 9-634](#) and described in [Table 9-1672](#).

Return to [Summary Table](#).

N/A

Table 9-1671.
PCIe_CORE_RP_I_ASF_TRANS_TO_CTRL
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E0Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E0Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E0Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E0Ch

Figure 9-634. PCIe_CORE_RP_I_ASF_TRANS_TO_CTRL Register

31	30	29	28	27	26	25	24
TRTOEN	R1						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
R1							
R-0h							
15	14	13	12	11	10	9	8
TRTOCTRL							
R/W-0h							
7	6	5	4	3	2	1	0
TRTOCTRL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1672. PCIe_CORE_RP_I_ASF_TRANS_TO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRTOEN	R/W	0h	Enable transaction timeout monitoring.
30-16	R1	R	0h	Reserved
15-0	TRTOCTRL	R/W	0h	Timer value to use for transaction timeout monitor. This is counted in resolution of 1 ms.

9.5.246 PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_MASK Register (Offset = 00100E10h) [reset = 0h]

PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_MASK is shown in Figure 9-635 and described in Table 9-1674.

Return to [Summary Table](#).

N/A

Table 9-1673.
PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_MASK
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E10h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E10h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E10h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E10h

Figure 9-635. PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_MASK Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
HPAXSLTO	HPAXMSTM	HPHLTGTO	HPHLMSTOM	DTIDTOM	DTIUTOM	APBTOM	LMITOM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AXSLTOM	AXMSTOM	HLTGTO	HLMSTOM	LRESPDTOM	LCFLWSTOM	LTPLCFTOM	PCOMTOM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1674. PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R31	R	0h	Reserved
15	HPAXSLTO	R/W	0h	When written to 1 Disables HP AXI Slave I/F timeout Error status reporting
14	HPAXMSTM	R/W	0h	When written to 1 Disables HP AXI Target I/F timeout Error status reporting
13	HPHLTGTO	R/W	0h	When written to 1 Disables HP HAL Target I/F timeout Error status reporting
12	HPHLMSTOM	R/W	0h	When written to 1 Disables HP HAL Master I/F timeout Error status reporting
11	DTIDTOM	R/W	0h	When written to 1 Disables DTI DN I/F timeout Reporting Error status reporting
10	DTIUTOM	R/W	0h	When written to 1 Disables DTI UP I/F timeout Reporting Error status reporting
9	APBTOM	R/W	0h	When written to 1 Disables APB I/F timeout Error status reporting
8	LMITOM	R/W	0h	When written to 1 Disables Local Management I/F timeout Error status reporting

Table 9-1674. PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	AXSLTOM	R/W	0h	When written to 1 Disables AXI Slave I/F timeout Error status reporting
6	AXMSTOM	R/W	0h	When written to 1 Disables AXI Target I/F timeout Error status reporting
5	HLTGTOM	R/W	0h	When written to 1 Disables HAL Target I/F timeout Error status reporting
4	HLMSTOM	R/W	0h	When written to 1 Disables HAL Master I/F timeout Error status reporting
3	LRESPDTOM	R/W	0h	When written to 1 Disables LTSSM Recovery Speed Timeout Error status reporting
2	LCFLWSTOM	R/W	0h	When written to 1 Disables LTSSM Cfg Link Width Start Timeout Error status reporting
1	LTPLCFTOM	R/W	0h	When written to 1 Disables LTSSM Polling Configuration Timeout Error status reporting
0	PCOMTOM	R/W	0h	When written to 1 Disables PCIe Completion Timeout Error status reporting

9.5.247 PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 00100E14h) [reset = 0h]

PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_STATUS is shown in [Figure 9-636](#) and described in [Table 9-1676](#).

Return to [Summary Table](#).

N/A

Table 9-1675.
PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_STATU
S Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E14h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E14h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E14h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E14h

Figure 9-636. PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_STATUS Register

31	30	29	28	27	26	25	24
R31							
R-0h							
23	22	21	20	19	18	17	16
R31							
R-0h							
15	14	13	12	11	10	9	8
HPAXSLTO	HPAXMSTO	HPHLTGTO	HPHLMSTO	DTIDTO	DTIUTO	APBTOM	LMITO
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
AXSLTO	AXMSTO	HLTGTO	HLMSTO	LRESPDTO	LCFLWSTO	LTPLCFTO	PCOMTO
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1676. PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R31	R	0h	Reserved
15	HPAXSLTO	R/W1C	0h	HP AXI Slave I/F Timeout detected waiting for a response
14	HPAXMSTO	R/W1C	0h	HP AXI Master I/F Timeout detected waiting for a response
13	HPHLTGTO	R/W1C	0h	HP HAL Target I/F Timeout detected waiting for a response
12	HPHLMSTO	R/W1C	0h	HP HAL Master I/F Timeout detected waiting for a response
11	DTIDTO	R/W1C	0h	DTI DN I/F Timeout detected waiting for a response from User
10	DTIUTO	R/W1C	0h	DTI UP I/F Timeout detected waiting for a response from User
9	APBTOM	R/W1C	0h	APB I/F Timeout detected waiting for a response from User
8	LMITO	R/W1C	0h	Local Management I/F Timeout detected waiting for a response from User
7	AXSLTO	R/W1C	0h	AXI Slave I/F Timeout detected waiting for a response
6	AXMSTO	R/W1C	0h	AXI Master I/F Timeout detected waiting for a response
5	HLTGTO	R/W1C	0h	HAL Target I/F Timeout detected waiting for a response
4	HLMSTO	R/W1C	0h	HAL Master I/F Timeout detected waiting for a response

**Table 9-1676. PCIE_CORE_RP_I_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
3	LRESPDTO	R/W1C	0h	This Indicates if the states of the LTSSM timed out . 48 ms timeout in Rec.Speed-> Detect
2	LCFLWSTO	R/W1C	0h	This Indicates if the states of the LTSSM timed out . 24 ms Timeout observed in Cfg.Link.Width.Start -> Detect
1	LTPLCFTO	R/W1C	0h	This Indicates if the states of the LTSSM timed out . 48 ms Timeout observed for Polling.Cfg-> Detect
0	PCOMTO	R/W1C	0h	This indicates if a Non Posted requested did NOT receive any competition from remote device with in the completion time specified

9.5.248 PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_MASK Register (Offset = 00100E18h) [reset = 0h]

PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_MASK is shown in [Figure 9-637](#) and described in [Table 9-1678](#).

Return to [Summary Table](#).

N/A

Table 9-1677.
PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_MASK
Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E18h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E18h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E18h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E18h

Figure 9-637. PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_MASK Register

31	30	29	28	27	26	25	24
R2							
R-0h							
23	22	21	20	19	18	17	16
R2							
R-0h							
15	14	13	12	11	10	9	8
AXISLDECM	RPLTOM	RPLROLM	BADDLPM	BADTLPM	PHRCVERM	USPREQM	ECRCERRM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
MALTLPEM	RCVROVFLM	UNCPLRCM	CMPLABTM	CPLTOM	FCPROERM	POTLRVM	DLPROTM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1678. PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R2	R	0h	RESERVED
15	AXISLDECM	R/W	0h	When set to 1 disables the AXI Slave/Decode Error status reporting
14	RPLTOM	R/W	0h	When set to 1 disables the Replay Timer Timeout status reporting
13	RPLROLM	R/W	0h	When set to 1 disables the Replay Number Rollover Detected status reporting
12	BADDLPM	R/W	0h	When set to 1 disables the Bad DLLP Detected status reporting
11	BADTLPM	R/W	0h	When set to 1 disables the Bad TLP Detected status reporting
10	PHRCVERM	R/W	0h	When set to 1 disables the PHY Receiver Error Detected status reporting
9	USPREQM	R/W	0h	When set to 1 disables the Unsupported Request Error status reporting
8	ECRCERRM	R/W	0h	When set to 1 disables the ECRC Error Detected status reporting
7	MALTLPEM	R/W	0h	When set to 1 disables the Malformed Error status reporting
6	RCVROVFLM	R/W	0h	When set to 1 disables the Receiver Overflow Error status reporting
5	UNCPLRCM	R/W	0h	When set to 1 disables the Unexpected Completion status reporting

**Table 9-1678. PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	CMPLABTM	R/W	0h	When set to 1 disables the Completer Abort Error status reporting
3	CPLTOM	R/W	0h	When set to 1 disables the Completion Timeout status reporting
2	FCPROERM	R/W	0h	When set to 1 disables the Flow Control Protocol Error status reporting
1	POTLRVM	R/W	0h	When set to 1 disables the Poisoned TLP received status reporting
0	DLPROTM	R/W	0h	When set to 1 disables the Data Link Layer Protocol Error status reporting

9.5.249 PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_STATUS_REG Register (Offset = 00100E1Ch) [reset = 0h]

PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_STATUS_REG is shown in [Figure 9-638](#) and described in [Table 9-1680](#).

Return to [Summary Table](#).

N/A

Table 9-1679.
PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_STATU
S_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E1Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E1Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E1Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E1Ch

Figure 9-638. PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_STATUS_REG Register

31	30	29	28	27	26	25	24
R2							
R-0h							
23	22	21	20	19	18	17	16
R2							
R-0h							
15	14	13	12	11	10	9	8
AXISLVDEC	RPLTOM	RPLROL	BADDLP	BADTLPM	PHRCVER	USPREQ	ECRCERR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
MALTLPER	RCVROVFL	UNCMLRCV	CMPLABT	CPLTO	FCPROER	POTLRCV	DLPROT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-1680. PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	R2	R	0h	RESERVED
15	AXISLVDEC	R/W1C	0h	This bit is set when the AXI interface sends SLVERR or DECERR to the user
14	RPLTOM	R/W1C	0h	This bit is set when the replay timer in the Data Link Layer of the Controller times out.
13	RPLROL	R/W1C	0h	This bit is set when the replay count rolls over after three re transmissions of a TLP at the Data Link Layer of the Controller.
12	BADDLP	R/W1C	0h	This bit is set when an LCRC error is detected in a received DLLP
11	BADTLPM	R/W1C	0h	This bit is set when an error is detected in a received TLP by the Data Link Layer of the Controller.
10	PHRCVER	R/W1C	0h	This bit is set when an error is detected in the receive side of the Physical Layer of the Controller
9	USPREQ	R/W1C	0h	This bit is set when the Controller has received a request from the link that it does not support.

**Table 9-1680. PCIE_CORE_RP_I_ASF_PROTOCOL_FAULT_STATUS_REG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
8	ECRCERR	R/W1C	0h	This bit is set when the Controller has detected an ECRC error in a received TLP
7	MALTLPER	R/W1C	0h	This bit is set when the Controller receives a malformed TLP from the link.
6	RCVROVFL	R/W1C	0h	This bit is set when the Controller receives a TLP in violation of the receive credit currently available.
5	UNCMLRCV	R/W1C	0h	This bit is set when the Controller has received an unexpected Completion packet from the link
4	CMPLABT	R/W1C	0h	This bit is set when the Controller has returned the Completer Abort [CA] status to a request received from the link.
3	CPLTO	R/W1C	0h	This bit is set when the completion timer associated with an outstanding request times out.
2	FCPROER	R/W1C	0h	This bit is set when certain violations of the flow control protocol are detected by the Controller.
1	POTLRCV	R/W1C	0h	This bit is set when the Controller receives a poisoned TLP from the link.
0	DLPROT	R/W1C	0h	This bit is set when the Controller receives an Ack or Nak DLLP whose sequence number does not correspond to that of an unacknowledged TLP or that of the last acknowledged TLP

9.5.250 PCIE_CORE_RP_DUAL_TL_CTRL Register (Offset = 00100E20h) [reset = X]

PCIE_CORE_RP_DUAL_TL_CTRL is shown in [Figure 9-639](#) and described in [Table 9-1682](#).

Return to [Summary Table](#).

N/A

Table 9-1681. PCIE_CORE_RP_DUAL_TL_CTRL Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E20h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E20h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E20h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E20h

Figure 9-639. PCIE_CORE_RP_DUAL_TL_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DTLHDRT							
R/W-2h							
15	14	13	12	11	10	9	8
DTLAW							
R/W-8h							
7	6	5	4	3	2	1	0
DTL_RSVD				DTLTS		GPLP	
R-0h				R/W-4h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1682. PCIE_CORE_RP_DUAL_TL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	DTLHDRT	R/W	2h	Defines the number of translation tokens that are reserved for the HP TL when selecting between inbound DTI requests. LP DTI requests will be stalled when the number of available tokens is equal to or smaller than this value.
15-8	DTLAW	R/W	8h	Defines the number of back to back high priority TLPs output before the arbiter gives highest priority to the low priority TL for 1 TLP. A value of '0' gives continuous highest priority to the high priority TL. The initial value of arbiter weight can be set with the define: den_db_DUAL_TL_CTRL_TX_ARB_WEIGHT
7-4	DTL_RSVD	R	0h	RESERVED

Table 9-1682. PCIE_CORE_RP_DUAL_TL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	DTLTS	R/W	4h	<p>This field set the ratio in which TAGs are shared among HP and LP TL.</p> <p>Following value pairs describes how the value of this field creates the sharing pattern.</p> <p>[0- 0% to HP TL], [1-6.25% to HP TL], [2-12.5%], [3-25%], [4-50%], [5-75%], [6-87.5%], [7-93.75.5%].</p> <p>The initial value of TAG share can be set with the define:den_db_DUAL_TL_CTRL_TAG_SHARE</p>
0	GPLP	R/W	0h	<p>By default high priority TL errors are given priority.</p> <p>If both low priority TL and high priority TL errors happen at the same time, headers from the high priority TL are captured for debug. use this bit to change the default priority.</p>

9.5.251 PCIE_CORE_RP_I_ASF_MAGIC_NUM_CTRLER_VER_REG Register (Offset = 00100E40h) [reset = 00010BDAh]

PCIE_CORE_RP_I_ASF_MAGIC_NUM_CTRLER_VER_REG is shown in [Figure 9-640](#) and described in [Table 9-1684](#).

Return to [Summary Table](#).

N/A

Table 9-1683.
PCIE_CORE_RP_I_ASF_MAGIC_NUM_CTRLER_V
ER_REG Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D10 0E40h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0D90 0E40h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E10 0E40h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0E90 0E40h

Figure 9-640. PCIE_CORE_RP_I_ASF_MAGIC_NUM_CTRLER_VER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTVER																MGCNM															
R-1h																R-BDAh															

LEGEND: R = Read Only; -n = value after reset

Table 9-1684. PCIE_CORE_RP_I_ASF_MAGIC_NUM_CTRLER_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CNTVER	R	1h	This 16bit value is used to determine the revision number of the controller by the software
15-0	MGCNM	R	BDAh	This 16bit value is used for verification of base address by the software

9.5.252 PCIe_CORE_RP_ADDR0 Register (Offset = 00400000h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-641](#) and described in [Table 9-1686](#).

Return to [Summary Table](#).

N/A

Table 9-1685. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0000h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0000h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0000h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0000h

Figure 9-641. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1686. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.253 PCIE_CORE_RP_ADDR1 Register (Offset = 00400004h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-642](#) and described in [Table 9-1688](#).

Return to [Summary Table](#).

N/A

Table 9-1687. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0004h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0004h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0004h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0004h

Figure 9-642. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1688. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.254 PCIe_CORE_RP_DESC0 Register (Offset = 00400008h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-643](#) and described in [Table 9-1690](#).

Return to [Summary Table](#).

N/A

Table 9-1689. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0008h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0008h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0008h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0008h

Figure 9-643. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1690. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.255 PCIE_CORE_RP_DESC1 Register (Offset = 0040000Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-644](#) and described in [Table 9-1692](#).

Return to [Summary Table](#).

N/A

Table 9-1691. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 000Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 000Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 000Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 000Ch

Figure 9-644. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1692. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.256 PCIe_CORE_RP_DESC3 Register (Offset = 00400014h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-645](#) and described in [Table 9-1694](#).

Return to [Summary Table](#).

N/A

Table 9-1693. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0014h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0014h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0014h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0014h

Figure 9-645. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1694. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.257 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400018h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-646](#) and described in [Table 9-1696](#).

Return to [Summary Table](#).

N/A

**Table 9-1695. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0018h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0018h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0018h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0018h

Figure 9-646. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1696. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.258 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040001Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-647](#) and described in [Table 9-1698](#).

Return to [Summary Table](#).

N/A

**Table 9-1697. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 001Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 001Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 001Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 001Ch

Figure 9-647. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1698. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.259 PCIE_CORE_RP_ADDR0 Register (Offset = 00400020h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-648](#) and described in [Table 9-1700](#).

Return to [Summary Table](#).

N/A

Table 9-1699. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0020h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0020h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0020h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0020h

Figure 9-648. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1700. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.260 PCIe_CORE_RP_ADDR1 Register (Offset = 00400024h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-649](#) and described in [Table 9-1702](#).

Return to [Summary Table](#).

N/A

Table 9-1701. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0024h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0024h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0024h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0024h

Figure 9-649. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1702. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.261 PCIE_CORE_RP_DESC0 Register (Offset = 00400028h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-650](#) and described in [Table 9-1704](#).

Return to [Summary Table](#).

N/A

Table 9-1703. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0028h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0028h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0028h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0028h

Figure 9-650. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1704. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.262 PCIe_CORE_RP_DESC1 Register (Offset = 0040002Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-651](#) and described in [Table 9-1706](#).

Return to [Summary Table](#).

N/A

Table 9-1705. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 002Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 002Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 002Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 002Ch

Figure 9-651. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1706. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.263 PCIE_CORE_RP_DESC3 Register (Offset = 00400034h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-652](#) and described in [Table 9-1708](#).

Return to [Summary Table](#).

N/A

Table 9-1707. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0034h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0034h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0034h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0034h

Figure 9-652. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1708. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.264 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400038h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-653](#) and described in [Table 9-1710](#).

Return to [Summary Table](#).

N/A

**Table 9-1709. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0038h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0038h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0038h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0038h

Figure 9-653. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1710. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.265 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040003Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-654](#) and described in [Table 9-1712](#).

Return to [Summary Table](#).

N/A

**Table 9-1711. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 003Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 003Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 003Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 003Ch

Figure 9-654. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1712. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.266 PCIe_CORE_RP_ADDR0 Register (Offset = 00400040h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-655](#) and described in [Table 9-1714](#).

Return to [Summary Table](#).

N/A

Table 9-1713. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0040h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0040h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0040h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0040h

Figure 9-655. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1714. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.267 PCIE_CORE_RP_ADDR1 Register (Offset = 00400044h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-656](#) and described in [Table 9-1716](#).

Return to [Summary Table](#).

N/A

Table 9-1715. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0044h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0044h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0044h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0044h

Figure 9-656. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1716. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.268 PCIe_CORE_RP_DESC0 Register (Offset = 00400048h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-657](#) and described in [Table 9-1718](#).

Return to [Summary Table](#).

N/A

Table 9-1717. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0048h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0048h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0048h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0048h

Figure 9-657. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1718. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.269 PCIE_CORE_RP_DESC1 Register (Offset = 0040004Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-658](#) and described in [Table 9-1720](#).

Return to [Summary Table](#).

N/A

Table 9-1719. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 004Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 004Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 004Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 004Ch

Figure 9-658. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1720. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.270 PCIe_CORE_RP_DESC3 Register (Offset = 00400054h) [reset = 0h]

PCIe_CORE_RP_DESC3 is shown in [Figure 9-659](#) and described in [Table 9-1722](#).

Return to [Summary Table](#).

N/A

Table 9-1721. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0054h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0054h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0054h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0054h

Figure 9-659. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									DATA																						
R-0h									R/W-0h																						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1722. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.271 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400058h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-660](#) and described in [Table 9-1724](#).

Return to [Summary Table](#).

N/A

**Table 9-1723. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0058h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0058h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0058h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0058h

Figure 9-660. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1724. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.272 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040005Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-661](#) and described in [Table 9-1726](#).

Return to [Summary Table](#).

N/A

**Table 9-1725. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 005Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 005Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 005Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 005Ch

Figure 9-661. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1726. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.273 PCIE_CORE_RP_ADDR0 Register (Offset = 00400060h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-662](#) and described in [Table 9-1728](#).

Return to [Summary Table](#).

N/A

Table 9-1727. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0060h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0060h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0060h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0060h

Figure 9-662. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1728. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.274 PCIe_CORE_RP_ADDR1 Register (Offset = 00400064h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-663](#) and described in [Table 9-1730](#).

Return to [Summary Table](#).

N/A

Table 9-1729. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0064h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0064h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0064h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0064h

Figure 9-663. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1730. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.275 PCIE_CORE_RP_DESC0 Register (Offset = 00400068h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-664](#) and described in [Table 9-1732](#).

Return to [Summary Table](#).

N/A

Table 9-1731. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0068h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0068h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0068h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0068h

Figure 9-664. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1732. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.276 PCIe_CORE_RP_DESC1 Register (Offset = 0040006Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-665](#) and described in [Table 9-1734](#).

Return to [Summary Table](#).

N/A

Table 9-1733. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 006Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 006Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 006Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 006Ch

Figure 9-665. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1734. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.277 PCIE_CORE_RP_DESC3 Register (Offset = 00400074h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-666](#) and described in [Table 9-1736](#).

Return to [Summary Table](#).

N/A

Table 9-1735. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0074h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0074h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0074h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0074h

Figure 9-666. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1736. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.278 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400078h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-667](#) and described in [Table 9-1738](#).

Return to [Summary Table](#).

N/A

**Table 9-1737. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0078h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0078h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0078h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0078h

Figure 9-667. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1738. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.279 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040007Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-668](#) and described in [Table 9-1740](#).

Return to [Summary Table](#).

N/A

**Table 9-1739. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 007Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 007Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 007Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 007Ch

Figure 9-668. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1740. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.280 PCIe_CORE_RP_ADDR0 Register (Offset = 00400080h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-669](#) and described in [Table 9-1742](#).

Return to [Summary Table](#).

N/A

Table 9-1741. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0080h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0080h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0080h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0080h

Figure 9-669. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1742. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.281 PCIE_CORE_RP_ADDR1 Register (Offset = 00400084h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-670](#) and described in [Table 9-1744](#).

Return to [Summary Table](#).

N/A

Table 9-1743. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0084h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0084h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0084h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0084h

Figure 9-670. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1744. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.282 PCIe_CORE_RP_DESC0 Register (Offset = 00400088h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-671](#) and described in [Table 9-1746](#).

Return to [Summary Table](#).

N/A

Table 9-1745. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0088h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0088h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0088h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0088h

Figure 9-671. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1746. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.283 PCIE_CORE_RP_DESC1 Register (Offset = 0040008Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-672](#) and described in [Table 9-1748](#).

Return to [Summary Table](#).

N/A

Table 9-1747. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 008Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 008Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 008Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 008Ch

Figure 9-672. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1748. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.284 PCIe_CORE_RP_DESC3 Register (Offset = 00400094h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-673](#) and described in [Table 9-1750](#).

Return to [Summary Table](#).

N/A

Table 9-1749. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0094h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0094h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0094h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0094h

Figure 9-673. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1750. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.285 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400098h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-674](#) and described in [Table 9-1752](#).

Return to [Summary Table](#).

N/A

**Table 9-1751. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0098h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0098h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0098h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0098h

Figure 9-674. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1752. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.286 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040009Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-675](#) and described in [Table 9-1754](#).

Return to [Summary Table](#).

N/A

**Table 9-1753. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 009Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 009Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 009Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 009Ch

Figure 9-675. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1754. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.287 PCIE_CORE_RP_ADDR0 Register (Offset = 004000A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-676](#) and described in [Table 9-1756](#).

Return to [Summary Table](#).

N/A

Table 9-1755. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00A0h

Figure 9-676. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1756. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.288 PCIe_CORE_RP_ADDR1 Register (Offset = 004000A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-677](#) and described in [Table 9-1758](#).

Return to [Summary Table](#).

N/A

Table 9-1757. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00A4h

Figure 9-677. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1758. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.289 PCIE_CORE_RP_DESC0 Register (Offset = 004000A8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-678](#) and described in [Table 9-1760](#).

Return to [Summary Table](#).

N/A

Table 9-1759. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00A8h

Figure 9-678. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1760. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.290 PCIe_CORE_RP_DESC1 Register (Offset = 004000ACh) [reset = 0h]

PCIe_CORE_RP_DESC1 is shown in [Figure 9-679](#) and described in [Table 9-1762](#).

Return to [Summary Table](#).

N/A

Table 9-1761. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCI00_CORE_DBN_CFG_PCIE_CORE	0D40 00ACh
PCI01_CORE_DBN_CFG_PCIE_CORE	0DC0 00ACh
PCI02_CORE_DBN_CFG_PCIE_CORE	0E40 00ACh
PCI03_CORE_DBN_CFG_PCIE_CORE	0EC0 00ACh

Figure 9-679. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1762. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.291 PCIE_CORE_RP_DESC3 Register (Offset = 004000B4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-680](#) and described in [Table 9-1764](#).

Return to [Summary Table](#).

N/A

Table 9-1763. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00B4h

Figure 9-680. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									DATA																						
R-0h									R/W-0h																						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1764. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.292 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004000B8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-681](#) and described in [Table 9-1766](#).

Return to [Summary Table](#).

N/A

**Table 9-1765. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00B8h

Figure 9-681. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1766. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.293 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004000BCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-682](#) and described in [Table 9-1768](#).

Return to [Summary Table](#).

N/A

**Table 9-1767. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00BCh

Figure 9-682. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1768. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.294 PCIe_CORE_RP_ADDR0 Register (Offset = 004000C0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-683](#) and described in [Table 9-1770](#).

Return to [Summary Table](#).

N/A

Table 9-1769. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00C0h

Figure 9-683. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1770. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.295 PCIE_CORE_RP_ADDR1 Register (Offset = 004000C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-684](#) and described in [Table 9-1772](#).

Return to [Summary Table](#).

N/A

Table 9-1771. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00C4h

Figure 9-684. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1772. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.296 PCIe_CORE_RP_DESC0 Register (Offset = 004000C8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-685](#) and described in [Table 9-1774](#).

Return to [Summary Table](#).

N/A

Table 9-1773. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00C8h

Figure 9-685. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1774. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.297 PCIE_CORE_RP_DESC1 Register (Offset = 004000CCh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-686](#) and described in [Table 9-1776](#).

Return to [Summary Table](#).

N/A

Table 9-1775. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00CCh

Figure 9-686. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1776. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.298 PCIe_CORE_RP_DESC3 Register (Offset = 004000D4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-687](#) and described in [Table 9-1778](#).

Return to [Summary Table](#).

N/A

Table 9-1777. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00D4h

Figure 9-687. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1778. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.299 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004000D8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-688](#) and described in [Table 9-1780](#).

Return to [Summary Table](#).

N/A

**Table 9-1779. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00D8h

Figure 9-688. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1780. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.300 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004000DCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-689](#) and described in [Table 9-1782](#).

Return to [Summary Table](#).

N/A

**Table 9-1781. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00DCh

Figure 9-689. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1782. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.301 PCIE_CORE_RP_ADDR0 Register (Offset = 004000E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-690](#) and described in [Table 9-1784](#).

Return to [Summary Table](#).

N/A

Table 9-1783. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00E0h

Figure 9-690. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1784. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.302 PCIe_CORE_RP_ADDR1 Register (Offset = 004000E4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-691](#) and described in [Table 9-1786](#).

Return to [Summary Table](#).

N/A

Table 9-1785. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00E4h

Figure 9-691. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1786. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.303 PCIE_CORE_RP_DESC0 Register (Offset = 004000E8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-692](#) and described in [Table 9-1788](#).

Return to [Summary Table](#).

N/A

Table 9-1787. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00E8h

Figure 9-692. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1788. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.304 PCIE_CORE_RP_DESC1 Register (Offset = 004000ECh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-693](#) and described in [Table 9-1790](#).

Return to [Summary Table](#).

N/A

Table 9-1789. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00ECh

Figure 9-693. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1790. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.305 PCIE_CORE_RP_DESC3 Register (Offset = 004000F4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-694](#) and described in [Table 9-1792](#).

Return to [Summary Table](#).

N/A

Table 9-1791. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00F4h

Figure 9-694. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1792. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.306 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400F8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-695](#) and described in [Table 9-1794](#).

Return to [Summary Table](#).

N/A

**Table 9-1793. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00F8h

Figure 9-695. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1794. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.307 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004000FCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-696](#) and described in [Table 9-1796](#).

Return to [Summary Table](#).

N/A

**Table 9-1795. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 00FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 00FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 00FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 00FCh

Figure 9-696. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1796. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.308 PCIe_CORE_RP_ADDR0 Register (Offset = 00400100h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-697](#) and described in [Table 9-1798](#).

Return to [Summary Table](#).

N/A

Table 9-1797. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0100h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0100h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0100h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0100h

Figure 9-697. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1798. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.309 PCIE_CORE_RP_ADDR1 Register (Offset = 00400104h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-698](#) and described in [Table 9-1800](#).

Return to [Summary Table](#).

N/A

Table 9-1799. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0104h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0104h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0104h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0104h

Figure 9-698. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1800. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.310 PCIe_CORE_RP_DESC0 Register (Offset = 00400108h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-699](#) and described in [Table 9-1802](#).

Return to [Summary Table](#).

N/A

Table 9-1801. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0108h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0108h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0108h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0108h

Figure 9-699. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1802. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.311 PCIE_CORE_RP_DESC1 Register (Offset = 0040010Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-700](#) and described in [Table 9-1804](#).

Return to [Summary Table](#).

N/A

Table 9-1803. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 010Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 010Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 010Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 010Ch

Figure 9-700. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1804. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.312 PCIe_CORE_RP_DESC3 Register (Offset = 00400114h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-701](#) and described in [Table 9-1806](#).

Return to [Summary Table](#).

N/A

Table 9-1805. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0114h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0114h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0114h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0114h

Figure 9-701. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1806. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.313 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400118h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-702](#) and described in [Table 9-1808](#).

Return to [Summary Table](#).

N/A

**Table 9-1807. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0118h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0118h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0118h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0118h

Figure 9-702. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1808. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.314 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040011Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-703](#) and described in [Table 9-1810](#).

Return to [Summary Table](#).

N/A

**Table 9-1809. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 011Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 011Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 011Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 011Ch

Figure 9-703. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1810. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.315 PCIE_CORE_RP_ADDR0 Register (Offset = 00400120h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-704](#) and described in [Table 9-1812](#).

Return to [Summary Table](#).

N/A

Table 9-1811. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0120h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0120h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0120h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0120h

Figure 9-704. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1812. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.316 PCIe_CORE_RP_ADDR1 Register (Offset = 00400124h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-705](#) and described in [Table 9-1814](#).

Return to [Summary Table](#).

N/A

Table 9-1813. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0124h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0124h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0124h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0124h

Figure 9-705. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1814. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.317 PCIE_CORE_RP_DESC0 Register (Offset = 00400128h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-706](#) and described in [Table 9-1816](#).

Return to [Summary Table](#).

N/A

Table 9-1815. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0128h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0128h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0128h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0128h

Figure 9-706. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1816. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.318 PCIe_CORE_RP_DESC1 Register (Offset = 0040012Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-707](#) and described in [Table 9-1818](#).

Return to [Summary Table](#).

N/A

Table 9-1817. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 012Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 012Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 012Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 012Ch

Figure 9-707. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1818. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.319 PCIE_CORE_RP_DESC3 Register (Offset = 00400134h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-708](#) and described in [Table 9-1820](#).

Return to [Summary Table](#).

N/A

Table 9-1819. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0134h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0134h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0134h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0134h

Figure 9-708. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1820. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.320 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400138h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-709](#) and described in [Table 9-1822](#).

Return to [Summary Table](#).

N/A

**Table 9-1821. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0138h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0138h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0138h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0138h

Figure 9-709. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1822. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.321 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040013Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-710](#) and described in [Table 9-1824](#).

Return to [Summary Table](#).

N/A

**Table 9-1823. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 013Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 013Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 013Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 013Ch

Figure 9-710. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1824. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.322 PCIe_CORE_RP_ADDR0 Register (Offset = 00400140h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-711](#) and described in [Table 9-1826](#).

Return to [Summary Table](#).

N/A

Table 9-1825. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0140h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0140h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0140h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0140h

Figure 9-711. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1826. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.323 PCIE_CORE_RP_ADDR1 Register (Offset = 00400144h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-712](#) and described in [Table 9-1828](#).

Return to [Summary Table](#).

N/A

Table 9-1827. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0144h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0144h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0144h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0144h

Figure 9-712. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1828. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.324 PCIe_CORE_RP_DESC0 Register (Offset = 00400148h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-713](#) and described in [Table 9-1830](#).

Return to [Summary Table](#).

N/A

Table 9-1829. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0148h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0148h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0148h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0148h

Figure 9-713. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1830. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.325 PCIE_CORE_RP_DESC1 Register (Offset = 0040014Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-714](#) and described in [Table 9-1832](#).

Return to [Summary Table](#).

N/A

Table 9-1831. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 014Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 014Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 014Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 014Ch

Figure 9-714. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1832. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.326 PCIe_CORE_RP_DESC3 Register (Offset = 00400154h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-715](#) and described in [Table 9-1834](#).

Return to [Summary Table](#).

N/A

Table 9-1833. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0154h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0154h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0154h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0154h

Figure 9-715. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1834. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.327 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400158h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-716](#) and described in [Table 9-1836](#).

Return to [Summary Table](#).

N/A

**Table 9-1835. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0158h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0158h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0158h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0158h

Figure 9-716. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1836. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.328 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040015Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-717](#) and described in [Table 9-1838](#).

Return to [Summary Table](#).

N/A

**Table 9-1837. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 015Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 015Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 015Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 015Ch

Figure 9-717. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1838. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.329 PCIE_CORE_RP_ADDR0 Register (Offset = 00400160h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-718](#) and described in [Table 9-1840](#).

Return to [Summary Table](#).

N/A

Table 9-1839. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0160h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0160h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0160h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0160h

Figure 9-718. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1840. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.330 PCIe_CORE_RP_ADDR1 Register (Offset = 00400164h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-719](#) and described in [Table 9-1842](#).

Return to [Summary Table](#).

N/A

Table 9-1841. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0164h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0164h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0164h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0164h

Figure 9-719. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1842. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.331 PCIE_CORE_RP_DESC0 Register (Offset = 00400168h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-720](#) and described in [Table 9-1844](#).

Return to [Summary Table](#).

N/A

Table 9-1843. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0168h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0168h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0168h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0168h

Figure 9-720. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1844. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.332 PCIe_CORE_RP_DESC1 Register (Offset = 0040016Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-721](#) and described in [Table 9-1846](#).

Return to [Summary Table](#).

N/A

Table 9-1845. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 016Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 016Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 016Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 016Ch

Figure 9-721. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1846. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.333 PCIE_CORE_RP_DESC3 Register (Offset = 00400174h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-722](#) and described in [Table 9-1848](#).

Return to [Summary Table](#).

N/A

Table 9-1847. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0174h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0174h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0174h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0174h

Figure 9-722. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									DATA																						
R-0h									R/W-0h																						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1848. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.334 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400178h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-723](#) and described in [Table 9-1850](#).

Return to [Summary Table](#).

N/A

**Table 9-1849. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0178h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0178h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0178h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0178h

Figure 9-723. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1850. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.335 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040017Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-724](#) and described in [Table 9-1852](#).

Return to [Summary Table](#).

N/A

**Table 9-1851. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 017Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 017Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 017Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 017Ch

Figure 9-724. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1852. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.336 PCIe_CORE_RP_ADDR0 Register (Offset = 00400180h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-725](#) and described in [Table 9-1854](#).

Return to [Summary Table](#).

N/A

Table 9-1853. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0180h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0180h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0180h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0180h

Figure 9-725. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1854. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.337 PCIE_CORE_RP_ADDR1 Register (Offset = 00400184h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-726](#) and described in [Table 9-1856](#).

Return to [Summary Table](#).

N/A

Table 9-1855. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0184h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0184h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0184h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0184h

Figure 9-726. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1856. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.338 PCIe_CORE_RP_DESC0 Register (Offset = 00400188h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-727](#) and described in [Table 9-1858](#).

Return to [Summary Table](#).

N/A

Table 9-1857. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0188h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0188h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0188h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0188h

Figure 9-727. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1858. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.339 PCIE_CORE_RP_DESC1 Register (Offset = 0040018Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-728](#) and described in [Table 9-1860](#).

Return to [Summary Table](#).

N/A

Table 9-1859. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 018Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 018Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 018Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 018Ch

Figure 9-728. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1860. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.340 PCIe_CORE_RP_DESC3 Register (Offset = 00400194h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-729](#) and described in [Table 9-1862](#).

Return to [Summary Table](#).

N/A

Table 9-1861. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0194h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0194h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0194h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0194h

Figure 9-729. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1862. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.341 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400198h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-730](#) and described in [Table 9-1864](#).

Return to [Summary Table](#).

N/A

**Table 9-1863. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0198h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0198h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0198h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0198h

Figure 9-730. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1864. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.342 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040019Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-731](#) and described in [Table 9-1866](#).

Return to [Summary Table](#).

N/A

**Table 9-1865. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 019Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 019Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 019Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 019Ch

Figure 9-731. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1866. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.343 PCIE_CORE_RP_ADDR0 Register (Offset = 004001A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-732](#) and described in [Table 9-1868](#).

Return to [Summary Table](#).

N/A

Table 9-1867. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01A0h

Figure 9-732. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1868. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.344 PCIe_CORE_RP_ADDR1 Register (Offset = 004001A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-733](#) and described in [Table 9-1870](#).

Return to [Summary Table](#).

N/A

Table 9-1869. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01A4h

Figure 9-733. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1870. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.345 PCIE_CORE_RP_DESC0 Register (Offset = 004001A8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-734](#) and described in [Table 9-1872](#).

Return to [Summary Table](#).

N/A

Table 9-1871. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01A8h

Figure 9-734. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1872. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.346 PCIe_CORE_RP_DESC1 Register (Offset = 004001ACh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-735](#) and described in [Table 9-1874](#).

Return to [Summary Table](#).

N/A

Table 9-1873. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01ACh

Figure 9-735. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1874. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.347 PCIE_CORE_RP_DESC3 Register (Offset = 004001B4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-736](#) and described in [Table 9-1876](#).

Return to [Summary Table](#).

N/A

Table 9-1875. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01B4h

Figure 9-736. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1876. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.348 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004001B8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-737](#) and described in [Table 9-1878](#).

Return to [Summary Table](#).

N/A

**Table 9-1877. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01B8h

Figure 9-737. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1878. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.349 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004001BCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-738](#) and described in [Table 9-1880](#).

Return to [Summary Table](#).

N/A

**Table 9-1879. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01BCh

Figure 9-738. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1880. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.350 PCIe_CORE_RP_ADDR0 Register (Offset = 004001C0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-739](#) and described in [Table 9-1882](#).

Return to [Summary Table](#).

N/A

Table 9-1881. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01C0h

Figure 9-739. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1882. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.351 PCIE_CORE_RP_ADDR1 Register (Offset = 004001C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-740](#) and described in [Table 9-1884](#).

Return to [Summary Table](#).

N/A

Table 9-1883. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01C4h

Figure 9-740. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1884. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.352 PCIe_CORE_RP_DESC0 Register (Offset = 004001C8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-741](#) and described in [Table 9-1886](#).

Return to [Summary Table](#).

N/A

Table 9-1885. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01C8h

Figure 9-741. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1886. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.353 PCIE_CORE_RP_DESC1 Register (Offset = 004001CCh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-742](#) and described in [Table 9-1888](#).

Return to [Summary Table](#).

N/A

Table 9-1887. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01CCh

Figure 9-742. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1888. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.354 PCIe_CORE_RP_DESC3 Register (Offset = 004001D4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-743](#) and described in [Table 9-1890](#).

Return to [Summary Table](#).

N/A

Table 9-1889. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01D4h

Figure 9-743. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1890. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.355 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004001D8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-744](#) and described in [Table 9-1892](#).

Return to [Summary Table](#).

N/A

**Table 9-1891. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01D8h

Figure 9-744. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1892. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.356 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004001DCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-745](#) and described in [Table 9-1894](#).

Return to [Summary Table](#).

N/A

**Table 9-1893. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01DCh

Figure 9-745. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1894. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.357 PCIE_CORE_RP_ADDR0 Register (Offset = 004001E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-746](#) and described in [Table 9-1896](#).

Return to [Summary Table](#).

N/A

Table 9-1895. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01E0h

Figure 9-746. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1896. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.358 PCIe_CORE_RP_ADDR1 Register (Offset = 004001E4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-747](#) and described in [Table 9-1898](#).

Return to [Summary Table](#).

N/A

Table 9-1897. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01E4h

Figure 9-747. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1898. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.359 PCIE_CORE_RP_DESC0 Register (Offset = 004001E8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-748](#) and described in [Table 9-1900](#).

Return to [Summary Table](#).

N/A

Table 9-1899. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01E8h

Figure 9-748. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1900. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.360 PCIe_CORE_RP_DESC1 Register (Offset = 004001ECh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-749](#) and described in [Table 9-1902](#).

Return to [Summary Table](#).

N/A

Table 9-1901. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01ECh

Figure 9-749. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1902. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.361 PCIE_CORE_RP_DESC3 Register (Offset = 004001F4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-750](#) and described in [Table 9-1904](#).

Return to [Summary Table](#).

N/A

Table 9-1903. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01F4h

Figure 9-750. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1904. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.362 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004001F8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-751](#) and described in [Table 9-1906](#).

Return to [Summary Table](#).

N/A

**Table 9-1905. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01F8h

Figure 9-751. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1906. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.363 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004001FCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-752](#) and described in [Table 9-1908](#).

Return to [Summary Table](#).

N/A

**Table 9-1907. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 01FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 01FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 01FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 01FCh

Figure 9-752. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1908. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.364 PCIe_CORE_RP_ADDR0 Register (Offset = 00400200h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-753](#) and described in [Table 9-1910](#).

Return to [Summary Table](#).

N/A

Table 9-1909. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0200h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0200h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0200h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0200h

Figure 9-753. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1910. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.365 PCIE_CORE_RP_ADDR1 Register (Offset = 00400204h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-754](#) and described in [Table 9-1912](#).

Return to [Summary Table](#).

N/A

Table 9-1911. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0204h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0204h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0204h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0204h

Figure 9-754. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1912. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.366 PCIe_CORE_RP_DESC0 Register (Offset = 00400208h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-755](#) and described in [Table 9-1914](#).

Return to [Summary Table](#).

N/A

Table 9-1913. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0208h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0208h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0208h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0208h

Figure 9-755. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1914. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.367 PCIE_CORE_RP_DESC1 Register (Offset = 0040020Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-756](#) and described in [Table 9-1916](#).

Return to [Summary Table](#).

N/A

Table 9-1915. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 020Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 020Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 020Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 020Ch

Figure 9-756. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1916. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.368 PCIe_CORE_RP_DESC3 Register (Offset = 00400214h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-757](#) and described in [Table 9-1918](#).

Return to [Summary Table](#).

N/A

Table 9-1917. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0214h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0214h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0214h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0214h

Figure 9-757. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1918. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.369 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400218h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-758](#) and described in [Table 9-1920](#).

Return to [Summary Table](#).

N/A

**Table 9-1919. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0218h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0218h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0218h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0218h

Figure 9-758. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1920. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.370 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040021Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-759](#) and described in [Table 9-1922](#).

Return to [Summary Table](#).

N/A

**Table 9-1921. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 021Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 021Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 021Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 021Ch

Figure 9-759. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1922. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.371 PCIE_CORE_RP_ADDR0 Register (Offset = 00400220h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-760](#) and described in [Table 9-1924](#).

Return to [Summary Table](#).

N/A

Table 9-1923. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0220h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0220h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0220h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0220h

Figure 9-760. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1924. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.372 PCIe_CORE_RP_ADDR1 Register (Offset = 00400224h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-761](#) and described in [Table 9-1926](#).

Return to [Summary Table](#).

N/A

Table 9-1925. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0224h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0224h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0224h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0224h

Figure 9-761. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1926. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.373 PCIE_CORE_RP_DESC0 Register (Offset = 00400228h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-762](#) and described in [Table 9-1928](#).

Return to [Summary Table](#).

N/A

Table 9-1927. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0228h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0228h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0228h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0228h

Figure 9-762. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1928. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.374 PCIe_CORE_RP_DESC1 Register (Offset = 0040022Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-763](#) and described in [Table 9-1930](#).

Return to [Summary Table](#).

N/A

Table 9-1929. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 022Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 022Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 022Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 022Ch

Figure 9-763. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1930. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.375 PCIE_CORE_RP_DESC3 Register (Offset = 00400234h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-764](#) and described in [Table 9-1932](#).

Return to [Summary Table](#).

N/A

Table 9-1931. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0234h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0234h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0234h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0234h

Figure 9-764. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1932. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.376 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400238h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-765](#) and described in [Table 9-1934](#).

Return to [Summary Table](#).

N/A

**Table 9-1933. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0238h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0238h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0238h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0238h

Figure 9-765. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1934. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.377 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040023Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-766](#) and described in [Table 9-1936](#).

Return to [Summary Table](#).

N/A

**Table 9-1935. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 023Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 023Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 023Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 023Ch

Figure 9-766. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1936. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.378 PCIe_CORE_RP_ADDR0 Register (Offset = 00400240h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-767](#) and described in [Table 9-1938](#).

Return to [Summary Table](#).

N/A

Table 9-1937. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0240h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0240h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0240h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0240h

Figure 9-767. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1938. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.379 PCIE_CORE_RP_ADDR1 Register (Offset = 00400244h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-768](#) and described in [Table 9-1940](#).

Return to [Summary Table](#).

N/A

Table 9-1939. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0244h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0244h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0244h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0244h

Figure 9-768. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1940. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.380 PCIe_CORE_RP_DESC0 Register (Offset = 00400248h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-769](#) and described in [Table 9-1942](#).

Return to [Summary Table](#).

N/A

Table 9-1941. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0248h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0248h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0248h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0248h

Figure 9-769. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1942. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.381 PCIE_CORE_RP_DESC1 Register (Offset = 0040024Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-770](#) and described in [Table 9-1944](#).

Return to [Summary Table](#).

N/A

Table 9-1943. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 024Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 024Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 024Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 024Ch

Figure 9-770. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1944. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.382 PCIe_CORE_RP_DESC3 Register (Offset = 00400254h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-771](#) and described in [Table 9-1946](#).

Return to [Summary Table](#).

N/A

Table 9-1945. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0254h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0254h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0254h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0254h

Figure 9-771. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1946. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.383 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400258h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-772](#) and described in [Table 9-1948](#).

Return to [Summary Table](#).

N/A

**Table 9-1947. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0258h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0258h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0258h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0258h

Figure 9-772. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1948. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.384 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040025Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-773](#) and described in [Table 9-1950](#).

Return to [Summary Table](#).

N/A

**Table 9-1949. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 025Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 025Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 025Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 025Ch

Figure 9-773. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1950. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.385 PCIE_CORE_RP_ADDR0 Register (Offset = 00400260h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-774](#) and described in [Table 9-1952](#).

Return to [Summary Table](#).

N/A

Table 9-1951. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0260h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0260h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0260h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0260h

Figure 9-774. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1952. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.386 PCIe_CORE_RP_ADDR1 Register (Offset = 00400264h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-775](#) and described in [Table 9-1954](#).

Return to [Summary Table](#).

N/A

Table 9-1953. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0264h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0264h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0264h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0264h

Figure 9-775. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1954. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.387 PCIE_CORE_RP_DESC0 Register (Offset = 00400268h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-776](#) and described in [Table 9-1956](#).

Return to [Summary Table](#).

N/A

Table 9-1955. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0268h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0268h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0268h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0268h

Figure 9-776. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1956. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.388 PCIE_CORE_RP_DESC1 Register (Offset = 0040026Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-777](#) and described in [Table 9-1958](#).

Return to [Summary Table](#).

N/A

Table 9-1957. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 026Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 026Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 026Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 026Ch

Figure 9-777. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1958. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.389 PCIE_CORE_RP_DESC3 Register (Offset = 00400274h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-778](#) and described in [Table 9-1960](#).

Return to [Summary Table](#).

N/A

Table 9-1959. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0274h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0274h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0274h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0274h

Figure 9-778. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1960. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.390 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400278h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-779](#) and described in [Table 9-1962](#).

Return to [Summary Table](#).

N/A

**Table 9-1961. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0278h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0278h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0278h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0278h

Figure 9-779. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1962. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.391 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040027Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-780](#) and described in [Table 9-1964](#).

Return to [Summary Table](#).

N/A

Table 9-1963. PCIE_CORE_RP_AXI_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 027Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 027Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 027Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 027Ch

Figure 9-780. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1964. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.392 PCIe_CORE_RP_ADDR0 Register (Offset = 00400280h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-781](#) and described in [Table 9-1966](#).

Return to [Summary Table](#).

N/A

Table 9-1965. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0280h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0280h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0280h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0280h

Figure 9-781. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1966. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.393 PCIE_CORE_RP_ADDR1 Register (Offset = 00400284h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-782](#) and described in [Table 9-1968](#).

Return to [Summary Table](#).

N/A

Table 9-1967. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0284h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0284h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0284h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0284h

Figure 9-782. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1968. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.394 PCIe_CORE_RP_DESC0 Register (Offset = 00400288h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-783](#) and described in [Table 9-1970](#).

Return to [Summary Table](#).

N/A

Table 9-1969. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0288h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0288h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0288h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0288h

Figure 9-783. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1970. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.395 PCIE_CORE_RP_DESC1 Register (Offset = 0040028Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-784](#) and described in [Table 9-1972](#).

Return to [Summary Table](#).

N/A

Table 9-1971. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 028Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 028Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 028Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 028Ch

Figure 9-784. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1972. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.396 PCIe_CORE_RP_DESC3 Register (Offset = 00400294h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-785](#) and described in [Table 9-1974](#).

Return to [Summary Table](#).

N/A

Table 9-1973. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0294h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0294h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0294h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0294h

Figure 9-785. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1974. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.397 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400298h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-786](#) and described in [Table 9-1976](#).

Return to [Summary Table](#).

N/A

**Table 9-1975. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0298h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0298h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0298h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0298h

Figure 9-786. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1976. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.398 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040029Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-787](#) and described in [Table 9-1978](#).

Return to [Summary Table](#).

N/A

**Table 9-1977. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 029Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 029Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 029Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 029Ch

Figure 9-787. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1978. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.399 PCIE_CORE_RP_ADDR0 Register (Offset = 004002A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-788](#) and described in [Table 9-1980](#).

Return to [Summary Table](#).

N/A

Table 9-1979. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02A0h

Figure 9-788. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1980. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.400 PCIe_CORE_RP_ADDR1 Register (Offset = 004002A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-789](#) and described in [Table 9-1982](#).

Return to [Summary Table](#).

N/A

Table 9-1981. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02A4h

Figure 9-789. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1982. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.401 PCIE_CORE_RP_DESC0 Register (Offset = 004002A8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-790](#) and described in [Table 9-1984](#).

Return to [Summary Table](#).

N/A

Table 9-1983. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02A8h

Figure 9-790. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1984. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.402 PCIE_CORE_RP_DESC1 Register (Offset = 004002ACh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-791](#) and described in [Table 9-1986](#).

Return to [Summary Table](#).

N/A

Table 9-1985. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02ACh

Figure 9-791. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1986. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.403 PCIE_CORE_RP_DESC3 Register (Offset = 004002B4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-792](#) and described in [Table 9-1988](#).

Return to [Summary Table](#).

N/A

Table 9-1987. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02B4h

Figure 9-792. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									DATA																						
R-0h									R/W-0h																						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1988. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.404 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004002B8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-793](#) and described in [Table 9-1990](#).

Return to [Summary Table](#).

N/A

**Table 9-1989. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02B8h

Figure 9-793. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1990. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.405 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004002BCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-794](#) and described in [Table 9-1992](#).

Return to [Summary Table](#).

N/A

Table 9-1991. PCIE_CORE_RP_AXI_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02BCh

Figure 9-794. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1992. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.406 PCIe_CORE_RP_ADDR0 Register (Offset = 004002C0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-795](#) and described in [Table 9-1994](#).

Return to [Summary Table](#).

N/A

Table 9-1993. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02C0h

Figure 9-795. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-1994. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.407 PCIE_CORE_RP_ADDR1 Register (Offset = 004002C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-796](#) and described in [Table 9-1996](#).

Return to [Summary Table](#).

N/A

Table 9-1995. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02C4h

Figure 9-796. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1996. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.408 PCIe_CORE_RP_DESC0 Register (Offset = 004002C8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-797](#) and described in [Table 9-1998](#).

Return to [Summary Table](#).

N/A

Table 9-1997. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02C8h

Figure 9-797. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-1998. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.409 PCIE_CORE_RP_DESC1 Register (Offset = 004002CCh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-798](#) and described in [Table 9-2000](#).

Return to [Summary Table](#).

N/A

Table 9-1999. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02CCh

Figure 9-798. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2000. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.410 PCIe_CORE_RP_DESC3 Register (Offset = 004002D4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-799](#) and described in [Table 9-2002](#).

Return to [Summary Table](#).

N/A

Table 9-2001. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02D4h

Figure 9-799. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2002. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.411 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004002D8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-800](#) and described in [Table 9-2004](#).

Return to [Summary Table](#).

N/A

**Table 9-2003. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02D8h

Figure 9-800. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2004. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.412 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004002DCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-801](#) and described in [Table 9-2006](#).

Return to [Summary Table](#).

N/A

**Table 9-2005. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02DCh

Figure 9-801. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2006. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.413 PCIE_CORE_RP_ADDR0 Register (Offset = 004002E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-802](#) and described in [Table 9-2008](#).

Return to [Summary Table](#).

N/A

Table 9-2007. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02E0h

Figure 9-802. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2008. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.414 PCIe_CORE_RP_ADDR1 Register (Offset = 004002E4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-803](#) and described in [Table 9-2010](#).

Return to [Summary Table](#).

N/A

Table 9-2009. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02E4h

Figure 9-803. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2010. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.415 PCIE_CORE_RP_DESC0 Register (Offset = 004002E8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-804](#) and described in [Table 9-2012](#).

Return to [Summary Table](#).

N/A

Table 9-2011. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02E8h

Figure 9-804. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2012. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.416 PCIe_CORE_RP_DESC1 Register (Offset = 004002ECh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-805](#) and described in [Table 9-2014](#).

Return to [Summary Table](#).

N/A

Table 9-2013. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02ECh

Figure 9-805. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2014. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.417 PCIE_CORE_RP_DESC3 Register (Offset = 004002F4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-806](#) and described in [Table 9-2016](#).

Return to [Summary Table](#).

N/A

Table 9-2015. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02F4h

Figure 9-806. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									DATA																						
R-0h									R/W-0h																						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2016. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.418 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004002F8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-807](#) and described in [Table 9-2018](#).

Return to [Summary Table](#).

N/A

**Table 9-2017. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02F8h

Figure 9-807. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2018. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.419 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004002FCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-808](#) and described in [Table 9-2020](#).

Return to [Summary Table](#).

N/A

**Table 9-2019. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 02FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 02FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 02FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 02FCh

Figure 9-808. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2020. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.420 PCIe_CORE_RP_ADDR0 Register (Offset = 00400300h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-809](#) and described in [Table 9-2022](#).

Return to [Summary Table](#).

N/A

Table 9-2021. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0300h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0300h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0300h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0300h

Figure 9-809. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2022. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.421 PCIE_CORE_RP_ADDR1 Register (Offset = 00400304h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-810](#) and described in [Table 9-2024](#).

Return to [Summary Table](#).

N/A

Table 9-2023. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0304h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0304h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0304h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0304h

Figure 9-810. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2024. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.422 PCIe_CORE_RP_DESC0 Register (Offset = 00400308h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-811](#) and described in [Table 9-2026](#).

Return to [Summary Table](#).

N/A

Table 9-2025. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0308h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0308h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0308h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0308h

Figure 9-811. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2026. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.423 PCIE_CORE_RP_DESC1 Register (Offset = 0040030Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-812](#) and described in [Table 9-2028](#).

Return to [Summary Table](#).

N/A

Table 9-2027. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 030Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 030Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 030Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 030Ch

Figure 9-812. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2028. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.424 PCIe_CORE_RP_DESC3 Register (Offset = 00400314h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-813](#) and described in [Table 9-2030](#).

Return to [Summary Table](#).

N/A

Table 9-2029. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0314h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0314h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0314h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0314h

Figure 9-813. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2030. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.425 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400318h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-814](#) and described in [Table 9-2032](#).

Return to [Summary Table](#).

N/A

**Table 9-2031. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0318h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0318h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0318h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0318h

Figure 9-814. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2032. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.426 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040031Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-815](#) and described in [Table 9-2034](#).

Return to [Summary Table](#).

N/A

**Table 9-2033. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 031Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 031Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 031Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 031Ch

Figure 9-815. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2034. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.427 PCIE_CORE_RP_ADDR0 Register (Offset = 00400320h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-816](#) and described in [Table 9-2036](#).

Return to [Summary Table](#).

N/A

Table 9-2035. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0320h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0320h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0320h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0320h

Figure 9-816. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2036. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.428 PCIe_CORE_RP_ADDR1 Register (Offset = 00400324h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-817](#) and described in [Table 9-2038](#).

Return to [Summary Table](#).

N/A

Table 9-2037. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0324h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0324h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0324h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0324h

Figure 9-817. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2038. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.429 PCIE_CORE_RP_DESC0 Register (Offset = 00400328h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-818](#) and described in [Table 9-2040](#).

Return to [Summary Table](#).

N/A

Table 9-2039. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0328h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0328h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0328h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0328h

Figure 9-818. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2040. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.430 PCIe_CORE_RP_DESC1 Register (Offset = 0040032Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-819](#) and described in [Table 9-2042](#).

Return to [Summary Table](#).

N/A

Table 9-2041. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 032Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 032Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 032Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 032Ch

Figure 9-819. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2042. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.431 PCIE_CORE_RP_DESC3 Register (Offset = 00400334h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-820](#) and described in [Table 9-2044](#).

Return to [Summary Table](#).

N/A

Table 9-2043. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0334h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0334h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0334h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0334h

Figure 9-820. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2044. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.432 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400338h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-821](#) and described in [Table 9-2046](#).

Return to [Summary Table](#).

N/A

**Table 9-2045. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0338h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0338h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0338h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0338h

Figure 9-821. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2046. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.433 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040033Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-822](#) and described in [Table 9-2048](#).

Return to [Summary Table](#).

N/A

**Table 9-2047. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 033Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 033Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 033Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 033Ch

Figure 9-822. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2048. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.434 PCIE_CORE_RP_ADDR0 Register (Offset = 00400340h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-823](#) and described in [Table 9-2050](#).

Return to [Summary Table](#).

N/A

Table 9-2049. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0340h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0340h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0340h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0340h

Figure 9-823. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2050. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.435 PCIE_CORE_RP_ADDR1 Register (Offset = 00400344h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-824](#) and described in [Table 9-2052](#).

Return to [Summary Table](#).

N/A

Table 9-2051. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0344h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0344h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0344h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0344h

Figure 9-824. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2052. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.436 PCIe_CORE_RP_DESC0 Register (Offset = 00400348h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-825](#) and described in [Table 9-2054](#).

Return to [Summary Table](#).

N/A

Table 9-2053. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0348h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0348h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0348h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0348h

Figure 9-825. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2054. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.437 PCIE_CORE_RP_DESC1 Register (Offset = 0040034Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-826](#) and described in [Table 9-2056](#).

Return to [Summary Table](#).

N/A

Table 9-2055. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 034Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 034Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 034Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 034Ch

Figure 9-826. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2056. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.438 PCIe_CORE_RP_DESC3 Register (Offset = 00400354h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-827](#) and described in [Table 9-2058](#).

Return to [Summary Table](#).

N/A

Table 9-2057. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0354h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0354h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0354h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0354h

Figure 9-827. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2058. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.439 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400358h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-828](#) and described in [Table 9-2060](#).

Return to [Summary Table](#).

N/A

Table 9-2059. PCIE_CORE_RP_AXI_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0358h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0358h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0358h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0358h

Figure 9-828. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2060. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.440 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040035Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-829](#) and described in [Table 9-2062](#).

Return to [Summary Table](#).

N/A

**Table 9-2061. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 035Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 035Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 035Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 035Ch

Figure 9-829. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2062. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.441 PCIE_CORE_RP_ADDR0 Register (Offset = 00400360h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-830](#) and described in [Table 9-2064](#).

Return to [Summary Table](#).

N/A

Table 9-2063. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0360h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0360h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0360h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0360h

Figure 9-830. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2064. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.442 PCIe_CORE_RP_ADDR1 Register (Offset = 00400364h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-831](#) and described in [Table 9-2066](#).

Return to [Summary Table](#).

N/A

Table 9-2065. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0364h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0364h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0364h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0364h

Figure 9-831. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2066. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.443 PCIE_CORE_RP_DESC0 Register (Offset = 00400368h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-832](#) and described in [Table 9-2068](#).

Return to [Summary Table](#).

N/A

Table 9-2067. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0368h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0368h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0368h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0368h

Figure 9-832. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2068. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.444 PCIE_CORE_RP_DESC1 Register (Offset = 0040036Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-833](#) and described in [Table 9-2070](#).

Return to [Summary Table](#).

N/A

Table 9-2069. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 036Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 036Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 036Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 036Ch

Figure 9-833. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2070. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.445 PCIE_CORE_RP_DESC3 Register (Offset = 00400374h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-834](#) and described in [Table 9-2072](#).

Return to [Summary Table](#).

N/A

Table 9-2071. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0374h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0374h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0374h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0374h

Figure 9-834. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2072. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.446 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400378h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-835](#) and described in [Table 9-2074](#).

Return to [Summary Table](#).

N/A

**Table 9-2073. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0378h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0378h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0378h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0378h

Figure 9-835. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2074. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.447 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040037Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-836](#) and described in [Table 9-2076](#).

Return to [Summary Table](#).

N/A

**Table 9-2075. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 037Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 037Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 037Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 037Ch

Figure 9-836. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2076. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.448 PCIe_CORE_RP_ADDR0 Register (Offset = 00400380h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-837](#) and described in [Table 9-2078](#).

Return to [Summary Table](#).

N/A

Table 9-2077. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0380h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0380h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0380h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0380h

Figure 9-837. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2078. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.449 PCIE_CORE_RP_ADDR1 Register (Offset = 00400384h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-838](#) and described in [Table 9-2080](#).

Return to [Summary Table](#).

N/A

Table 9-2079. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0384h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0384h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0384h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0384h

Figure 9-838. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2080. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.450 PCIe_CORE_RP_DESC0 Register (Offset = 00400388h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-839](#) and described in [Table 9-2082](#).

Return to [Summary Table](#).

N/A

Table 9-2081. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0388h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0388h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0388h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0388h

Figure 9-839. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2082. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.451 PCIE_CORE_RP_DESC1 Register (Offset = 0040038Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-840](#) and described in [Table 9-2084](#).

Return to [Summary Table](#).

N/A

Table 9-2083. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 038Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 038Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 038Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 038Ch

Figure 9-840. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2084. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.452 PCIe_CORE_RP_DESC3 Register (Offset = 00400394h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-841](#) and described in [Table 9-2086](#).

Return to [Summary Table](#).

N/A

Table 9-2085. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0394h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0394h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0394h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0394h

Figure 9-841. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2086. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.453 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400398h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-842](#) and described in [Table 9-2088](#).

Return to [Summary Table](#).

N/A

**Table 9-2087. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0398h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0398h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0398h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0398h

Figure 9-842. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2088. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.454 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040039Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-843](#) and described in [Table 9-2090](#).

Return to [Summary Table](#).

N/A

**Table 9-2089. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 039Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 039Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 039Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 039Ch

Figure 9-843. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2090. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.455 PCIE_CORE_RP_ADDR0 Register (Offset = 004003A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-844](#) and described in [Table 9-2092](#).

Return to [Summary Table](#).

N/A

Table 9-2091. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03A0h

Figure 9-844. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2092. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.456 PCIe_CORE_RP_ADDR1 Register (Offset = 004003A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-845](#) and described in [Table 9-2094](#).

Return to [Summary Table](#).

N/A

Table 9-2093. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03A4h

Figure 9-845. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2094. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.457 PCIE_CORE_RP_DESC0 Register (Offset = 004003A8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-846](#) and described in [Table 9-2096](#).

Return to [Summary Table](#).

N/A

Table 9-2095. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03A8h

Figure 9-846. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2096. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.458 PCIe_CORE_RP_DESC1 Register (Offset = 004003ACh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-847](#) and described in [Table 9-2098](#).

Return to [Summary Table](#).

N/A

Table 9-2097. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03ACh

Figure 9-847. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2098. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.459 PCIE_CORE_RP_DESC3 Register (Offset = 004003B4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-848](#) and described in [Table 9-2100](#).

Return to [Summary Table](#).

N/A

Table 9-2099. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03B4h

Figure 9-848. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2100. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.460 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004003B8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-849](#) and described in [Table 9-2102](#).

Return to [Summary Table](#).

N/A

**Table 9-2101. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03B8h

Figure 9-849. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2102. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.461 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004003BCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-850](#) and described in [Table 9-2104](#).

Return to [Summary Table](#).

N/A

**Table 9-2103. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03BCh

Figure 9-850. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2104. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.462 PCIe_CORE_RP_ADDR0 Register (Offset = 004003C0h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-851](#) and described in [Table 9-2106](#).

Return to [Summary Table](#).

N/A

Table 9-2105. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03C0h

Figure 9-851. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2106. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.463 PCIE_CORE_RP_ADDR1 Register (Offset = 004003C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-852](#) and described in [Table 9-2108](#).

Return to [Summary Table](#).

N/A

Table 9-2107. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03C4h

Figure 9-852. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2108. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.464 PCIe_CORE_RP_DESC0 Register (Offset = 004003C8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-853](#) and described in [Table 9-2110](#).

Return to [Summary Table](#).

N/A

Table 9-2109. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03C8h

Figure 9-853. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2110. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.465 PCIE_CORE_RP_DESC1 Register (Offset = 004003CCh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-854](#) and described in [Table 9-2112](#).

Return to [Summary Table](#).

N/A

Table 9-2111. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03CCh

Figure 9-854. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2112. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.466 PCIe_CORE_RP_DESC3 Register (Offset = 004003D4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-855](#) and described in [Table 9-2114](#).

Return to [Summary Table](#).

N/A

Table 9-2113. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03D4h

Figure 9-855. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2114. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.467 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004003D8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-856](#) and described in [Table 9-2116](#).

Return to [Summary Table](#).

N/A

**Table 9-2115. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03D8h

Figure 9-856. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2116. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.468 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004003DCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-857](#) and described in [Table 9-2118](#).

Return to [Summary Table](#).

N/A

**Table 9-2117. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03DCh

Figure 9-857. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2118. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.469 PCIE_CORE_RP_ADDR0 Register (Offset = 004003E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-858](#) and described in [Table 9-2120](#).

Return to [Summary Table](#).

N/A

Table 9-2119. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03E0h

Figure 9-858. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2120. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.470 PCIe_CORE_RP_ADDR1 Register (Offset = 004003E4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-859](#) and described in [Table 9-2122](#).

Return to [Summary Table](#).

N/A

Table 9-2121. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03E4h

Figure 9-859. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2122. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.471 PCIE_CORE_RP_DESC0 Register (Offset = 004003E8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-860](#) and described in [Table 9-2124](#).

Return to [Summary Table](#).

N/A

Table 9-2123. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03E8h

Figure 9-860. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2124. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.472 PCIe_CORE_RP_DESC1 Register (Offset = 004003ECh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-861](#) and described in [Table 9-2126](#).

Return to [Summary Table](#).

N/A

Table 9-2125. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03ECh

Figure 9-861. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2126. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.473 PCIE_CORE_RP_DESC3 Register (Offset = 004003F4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-862](#) and described in [Table 9-2128](#).

Return to [Summary Table](#).

N/A

Table 9-2127. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03F4h

Figure 9-862. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2128. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.474 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004003F8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-863](#) and described in [Table 9-2130](#).

Return to [Summary Table](#).

N/A

**Table 9-2129. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03F8h

Figure 9-863. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2130. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.475 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004003FCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-864](#) and described in [Table 9-2132](#).

Return to [Summary Table](#).

N/A

**Table 9-2131. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 03FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 03FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 03FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 03FCh

Figure 9-864. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2132. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.476 PCIe_CORE_RP_ADDR0 Register (Offset = 00400400h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-865](#) and described in [Table 9-2134](#).

Return to [Summary Table](#).

N/A

Table 9-2133. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0400h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0400h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0400h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0400h

Figure 9-865. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2134. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.477 PCIE_CORE_RP_ADDR1 Register (Offset = 00400404h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-866](#) and described in [Table 9-2136](#).

Return to [Summary Table](#).

N/A

Table 9-2135. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0404h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0404h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0404h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0404h

Figure 9-866. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2136. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.478 PCIe_CORE_RP_DESC0 Register (Offset = 00400408h) [reset = 0h]

PCIe_CORE_RP_DESC0 is shown in [Figure 9-867](#) and described in [Table 9-2138](#).

Return to [Summary Table](#).

N/A

Table 9-2137. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0408h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0408h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0408h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0408h

Figure 9-867. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2138. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.479 PCIE_CORE_RP_DESC1 Register (Offset = 0040040Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-868](#) and described in [Table 9-2140](#).

Return to [Summary Table](#).

N/A

Table 9-2139. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 040Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 040Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 040Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 040Ch

Figure 9-868. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2140. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.480 PCIe_CORE_RP_DESC3 Register (Offset = 00400414h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-869](#) and described in [Table 9-2142](#).

Return to [Summary Table](#).

N/A

Table 9-2141. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0414h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0414h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0414h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0414h

Figure 9-869. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2142. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.481 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400418h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-870](#) and described in [Table 9-2144](#).

Return to [Summary Table](#).

N/A

**Table 9-2143. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0418h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0418h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0418h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0418h

Figure 9-870. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2144. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.482 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040041Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-871](#) and described in [Table 9-2146](#).

Return to [Summary Table](#).

N/A

**Table 9-2145. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 041Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 041Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 041Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 041Ch

Figure 9-871. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2146. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.483 PCIE_CORE_RP_ADDR0 Register (Offset = 00400420h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-872](#) and described in [Table 9-2148](#).

Return to [Summary Table](#).

N/A

Table 9-2147. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0420h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0420h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0420h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0420h

Figure 9-872. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2148. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.484 PCIe_CORE_RP_ADDR1 Register (Offset = 00400424h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-873](#) and described in [Table 9-2150](#).

Return to [Summary Table](#).

N/A

Table 9-2149. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0424h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0424h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0424h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0424h

Figure 9-873. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2150. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.485 PCIE_CORE_RP_DESC0 Register (Offset = 00400428h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-874](#) and described in [Table 9-2152](#).

Return to [Summary Table](#).

N/A

Table 9-2151. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0428h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0428h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0428h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0428h

Figure 9-874. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2152. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.486 PCIe_CORE_RP_DESC1 Register (Offset = 0040042Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-875](#) and described in [Table 9-2154](#).

Return to [Summary Table](#).

N/A

Table 9-2153. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 042Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 042Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 042Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 042Ch

Figure 9-875. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2154. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.487 PCIE_CORE_RP_DESC3 Register (Offset = 00400434h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-876](#) and described in [Table 9-2156](#).

Return to [Summary Table](#).

N/A

Table 9-2155. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0434h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0434h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0434h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0434h

Figure 9-876. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2156. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.488 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400438h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-877](#) and described in [Table 9-2158](#).

Return to [Summary Table](#).

N/A

**Table 9-2157. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0438h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0438h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0438h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0438h

Figure 9-877. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2158. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.489 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040043Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-878](#) and described in [Table 9-2160](#).

Return to [Summary Table](#).

N/A

**Table 9-2159. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 043Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 043Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 043Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 043Ch

Figure 9-878. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2160. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.490 PCIe_CORE_RP_ADDR0 Register (Offset = 00400440h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-879](#) and described in [Table 9-2162](#).

Return to [Summary Table](#).

N/A

Table 9-2161. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0440h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0440h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0440h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0440h

Figure 9-879. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2162. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.491 PCIE_CORE_RP_ADDR1 Register (Offset = 00400444h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-880](#) and described in [Table 9-2164](#).

Return to [Summary Table](#).

N/A

Table 9-2163. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0444h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0444h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0444h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0444h

Figure 9-880. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2164. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.492 PCIe_CORE_RP_DESC0 Register (Offset = 00400448h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-881](#) and described in [Table 9-2166](#).

Return to [Summary Table](#).

N/A

Table 9-2165. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0448h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0448h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0448h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0448h

Figure 9-881. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2166. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.493 PCIE_CORE_RP_DESC1 Register (Offset = 0040044Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-882](#) and described in [Table 9-2168](#).

Return to [Summary Table](#).

N/A

Table 9-2167. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 044Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 044Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 044Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 044Ch

Figure 9-882. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2168. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.494 PCIe_CORE_RP_DESC3 Register (Offset = 00400454h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-883](#) and described in [Table 9-2170](#).

Return to [Summary Table](#).

N/A

Table 9-2169. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0454h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0454h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0454h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0454h

Figure 9-883. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2170. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.495 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400458h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-884](#) and described in [Table 9-2172](#).

Return to [Summary Table](#).

N/A

**Table 9-2171. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0458h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0458h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0458h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0458h

Figure 9-884. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2172. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.496 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040045Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-885](#) and described in [Table 9-2174](#).

Return to [Summary Table](#).

N/A

**Table 9-2173. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 045Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 045Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 045Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 045Ch

Figure 9-885. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2174. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.497 PCIE_CORE_RP_ADDR0 Register (Offset = 00400460h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-886](#) and described in [Table 9-2176](#).

Return to [Summary Table](#).

N/A

Table 9-2175. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0460h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0460h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0460h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0460h

Figure 9-886. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2176. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.498 PCIe_CORE_RP_ADDR1 Register (Offset = 00400464h) [reset = 0h]

PCIe_CORE_RP_ADDR1 is shown in [Figure 9-887](#) and described in [Table 9-2178](#).

Return to [Summary Table](#).

N/A

Table 9-2177. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0464h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0464h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0464h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0464h

Figure 9-887. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2178. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.499 PCIE_CORE_RP_DESC0 Register (Offset = 00400468h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-888](#) and described in [Table 9-2180](#).

Return to [Summary Table](#).

N/A

Table 9-2179. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0468h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0468h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0468h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0468h

Figure 9-888. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2180. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.500 PCIe_CORE_RP_DESC1 Register (Offset = 0040046Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-889](#) and described in [Table 9-2182](#).

Return to [Summary Table](#).

N/A

Table 9-2181. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 046Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 046Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 046Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 046Ch

Figure 9-889. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2182. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.501 PCIE_CORE_RP_DESC3 Register (Offset = 00400474h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-890](#) and described in [Table 9-2184](#).

Return to [Summary Table](#).

N/A

Table 9-2183. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0474h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0474h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0474h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0474h

Figure 9-890. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2184. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.502 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400478h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-891](#) and described in [Table 9-2186](#).

Return to [Summary Table](#).

N/A

**Table 9-2185. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0478h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0478h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0478h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0478h

Figure 9-891. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2186. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.503 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040047Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-892](#) and described in [Table 9-2188](#).

Return to [Summary Table](#).

N/A

**Table 9-2187. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 047Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 047Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 047Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 047Ch

Figure 9-892. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2188. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.504 PCIE_CORE_RP_ADDR0 Register (Offset = 00400480h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-893](#) and described in [Table 9-2190](#).

Return to [Summary Table](#).

N/A

Table 9-2189. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0480h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0480h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0480h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0480h

Figure 9-893. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2190. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.505 PCIE_CORE_RP_ADDR1 Register (Offset = 00400484h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-894](#) and described in [Table 9-2192](#).

Return to [Summary Table](#).

N/A

Table 9-2191. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0484h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0484h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0484h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0484h

Figure 9-894. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2192. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.506 PCIe_CORE_RP_DESC0 Register (Offset = 00400488h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-895](#) and described in [Table 9-2194](#).

Return to [Summary Table](#).

N/A

Table 9-2193. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0488h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0488h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0488h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0488h

Figure 9-895. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2194. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.507 PCIE_CORE_RP_DESC1 Register (Offset = 0040048Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-896](#) and described in [Table 9-2196](#).

Return to [Summary Table](#).

N/A

Table 9-2195. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 048Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 048Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 048Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 048Ch

Figure 9-896. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2196. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.508 PCIE_CORE_RP_DESC3 Register (Offset = 00400494h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-897](#) and described in [Table 9-2198](#).

Return to [Summary Table](#).

N/A

Table 9-2197. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0494h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0494h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0494h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0494h

Figure 9-897. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2198. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.509 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400498h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-898](#) and described in [Table 9-2200](#).

Return to [Summary Table](#).

N/A

**Table 9-2199. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0498h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0498h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0498h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0498h

Figure 9-898. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2200. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.510 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040049Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-899](#) and described in [Table 9-2202](#).

Return to [Summary Table](#).

N/A

**Table 9-2201. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 049Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 049Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 049Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 049Ch

Figure 9-899. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2202. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.511 PCIE_CORE_RP_ADDR0 Register (Offset = 004004A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-900](#) and described in [Table 9-2204](#).

Return to [Summary Table](#).

N/A

Table 9-2203. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04A0h

Figure 9-900. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2204. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.512 PCIe_CORE_RP_ADDR1 Register (Offset = 004004A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-901](#) and described in [Table 9-2206](#).

Return to [Summary Table](#).

N/A

Table 9-2205. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04A4h

Figure 9-901. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2206. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.513 PCIE_CORE_RP_DESC0 Register (Offset = 004004A8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-902](#) and described in [Table 9-2208](#).

Return to [Summary Table](#).

N/A

Table 9-2207. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04A8h

Figure 9-902. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2208. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.514 PCIe_CORE_RP_DESC1 Register (Offset = 004004ACh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-903](#) and described in [Table 9-2210](#).

Return to [Summary Table](#).

N/A

Table 9-2209. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04ACh

Figure 9-903. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2210. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.515 PCIE_CORE_RP_DESC3 Register (Offset = 004004B4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-904](#) and described in [Table 9-2212](#).

Return to [Summary Table](#).

N/A

Table 9-2211. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04B4h

Figure 9-904. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									DATA																						
R-0h									R/W-0h																						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2212. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.516 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004004B8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-905](#) and described in [Table 9-2214](#).

Return to [Summary Table](#).

N/A

**Table 9-2213. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04B8h

Figure 9-905. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2214. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.517 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004004BCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-906](#) and described in [Table 9-2216](#).

Return to [Summary Table](#).

N/A

**Table 9-2215. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04BCh

Figure 9-906. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2216. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.518 PCIe_CORE_RP_ADDR0 Register (Offset = 004004C0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-907](#) and described in [Table 9-2218](#).

Return to [Summary Table](#).

N/A

Table 9-2217. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04C0h

Figure 9-907. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2218. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.519 PCIE_CORE_RP_ADDR1 Register (Offset = 004004C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-908](#) and described in [Table 9-2220](#).

Return to [Summary Table](#).

N/A

Table 9-2219. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04C4h

Figure 9-908. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2220. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.520 PCIe_CORE_RP_DESC0 Register (Offset = 004004C8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-909](#) and described in [Table 9-2222](#).

Return to [Summary Table](#).

N/A

Table 9-2221. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04C8h

Figure 9-909. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2222. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.521 PCIE_CORE_RP_DESC1 Register (Offset = 004004CCh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-910](#) and described in [Table 9-2224](#).

Return to [Summary Table](#).

N/A

Table 9-2223. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04CCh

Figure 9-910. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2224. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.522 PCIe_CORE_RP_DESC3 Register (Offset = 004004D4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-911](#) and described in [Table 9-2226](#).

Return to [Summary Table](#).

N/A

Table 9-2225. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04D4h

Figure 9-911. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									DATA																						
R-0h									R/W-0h																						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2226. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.523 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004004D8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-912](#) and described in [Table 9-2228](#).

Return to [Summary Table](#).

N/A

**Table 9-2227. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04D8h

Figure 9-912. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2228. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.524 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004004DCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-913](#) and described in [Table 9-2230](#).

Return to [Summary Table](#).

N/A

**Table 9-2229. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04DCh

Figure 9-913. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2230. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.525 PCIE_CORE_RP_ADDR0 Register (Offset = 004004E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-914](#) and described in [Table 9-2232](#).

Return to [Summary Table](#).

N/A

Table 9-2231. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04E0h

Figure 9-914. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2232. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.526 PCIe_CORE_RP_ADDR1 Register (Offset = 004004E4h) [reset = 0h]

PCIe_CORE_RP_ADDR1 is shown in [Figure 9-915](#) and described in [Table 9-2234](#).

Return to [Summary Table](#).

N/A

Table 9-2233. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIe0_CORE_DBN_CFG_PCIE_CORE	0D40 04E4h
PCIe1_CORE_DBN_CFG_PCIE_CORE	0DC0 04E4h
PCIe2_CORE_DBN_CFG_PCIE_CORE	0E40 04E4h
PCIe3_CORE_DBN_CFG_PCIE_CORE	0EC0 04E4h

Figure 9-915. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2234. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.527 PCIE_CORE_RP_DESC0 Register (Offset = 004004E8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-916](#) and described in [Table 9-2236](#).

Return to [Summary Table](#).

N/A

Table 9-2235. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04E8h

Figure 9-916. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2236. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.528 PCIe_CORE_RP_DESC1 Register (Offset = 004004ECh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-917](#) and described in [Table 9-2238](#).

Return to [Summary Table](#).

N/A

Table 9-2237. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04ECh

Figure 9-917. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2238. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.529 PCIE_CORE_RP_DESC3 Register (Offset = 004004F4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-918](#) and described in [Table 9-2240](#).

Return to [Summary Table](#).

N/A

Table 9-2239. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04F4h

Figure 9-918. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2240. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.530 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004004F8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-919](#) and described in [Table 9-2242](#).

Return to [Summary Table](#).

N/A

**Table 9-2241. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04F8h

Figure 9-919. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2242. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.531 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004004FCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-920](#) and described in [Table 9-2244](#).

Return to [Summary Table](#).

N/A

**Table 9-2243. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 04FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 04FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 04FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 04FCh

Figure 9-920. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2244. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.532 PCIe_CORE_RP_ADDR0 Register (Offset = 00400500h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-921](#) and described in [Table 9-2246](#).

Return to [Summary Table](#).

N/A

Table 9-2245. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0500h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0500h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0500h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0500h

Figure 9-921. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2246. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.533 PCIE_CORE_RP_ADDR1 Register (Offset = 00400504h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-922](#) and described in [Table 9-2248](#).

Return to [Summary Table](#).

N/A

Table 9-2247. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0504h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0504h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0504h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0504h

Figure 9-922. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2248. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.534 PCIe_CORE_RP_DESC0 Register (Offset = 00400508h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-923](#) and described in [Table 9-2250](#).

Return to [Summary Table](#).

N/A

Table 9-2249. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0508h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0508h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0508h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0508h

Figure 9-923. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2250. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.535 PCIE_CORE_RP_DESC1 Register (Offset = 0040050Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-924](#) and described in [Table 9-2252](#).

Return to [Summary Table](#).

N/A

Table 9-2251. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 050Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 050Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 050Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 050Ch

Figure 9-924. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2252. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.536 PCIe_CORE_RP_DESC3 Register (Offset = 00400514h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-925](#) and described in [Table 9-2254](#).

Return to [Summary Table](#).

N/A

Table 9-2253. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0514h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0514h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0514h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0514h

Figure 9-925. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2254. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.537 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400518h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-926](#) and described in [Table 9-2256](#).

Return to [Summary Table](#).

N/A

**Table 9-2255. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0518h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0518h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0518h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0518h

Figure 9-926. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2256. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.538 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040051Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-927](#) and described in [Table 9-2258](#).

Return to [Summary Table](#).

N/A

**Table 9-2257. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 051Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 051Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 051Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 051Ch

Figure 9-927. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2258. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.539 PCIE_CORE_RP_ADDR0 Register (Offset = 00400520h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-928](#) and described in [Table 9-2260](#).

Return to [Summary Table](#).

N/A

Table 9-2259. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0520h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0520h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0520h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0520h

Figure 9-928. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2260. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.540 PCIe_CORE_RP_ADDR1 Register (Offset = 00400524h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-929](#) and described in [Table 9-2262](#).

Return to [Summary Table](#).

N/A

Table 9-2261. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0524h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0524h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0524h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0524h

Figure 9-929. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2262. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.541 PCIE_CORE_RP_DESC0 Register (Offset = 00400528h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-930](#) and described in [Table 9-2264](#).

Return to [Summary Table](#).

N/A

Table 9-2263. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0528h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0528h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0528h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0528h

Figure 9-930. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2264. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.542 PCIe_CORE_RP_DESC1 Register (Offset = 0040052Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-931](#) and described in [Table 9-2266](#).

Return to [Summary Table](#).

N/A

Table 9-2265. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 052Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 052Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 052Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 052Ch

Figure 9-931. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2266. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.543 PCIE_CORE_RP_DESC3 Register (Offset = 00400534h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-932](#) and described in [Table 9-2268](#).

Return to [Summary Table](#).

N/A

Table 9-2267. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0534h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0534h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0534h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0534h

Figure 9-932. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2268. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.544 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400538h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-933](#) and described in [Table 9-2270](#).

Return to [Summary Table](#).

N/A

**Table 9-2269. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0538h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0538h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0538h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0538h

Figure 9-933. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2270. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.545 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040053Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-934](#) and described in [Table 9-2272](#).

Return to [Summary Table](#).

N/A

**Table 9-2271. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 053Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 053Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 053Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 053Ch

Figure 9-934. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2272. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.546 PCIe_CORE_RP_ADDR0 Register (Offset = 00400540h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-935](#) and described in [Table 9-2274](#).

Return to [Summary Table](#).

N/A

Table 9-2273. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0540h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0540h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0540h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0540h

Figure 9-935. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2274. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.547 PCIE_CORE_RP_ADDR1 Register (Offset = 00400544h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-936](#) and described in [Table 9-2276](#).

Return to [Summary Table](#).

N/A

Table 9-2275. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0544h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0544h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0544h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0544h

Figure 9-936. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2276. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.548 PCIe_CORE_RP_DESC0 Register (Offset = 00400548h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-937](#) and described in [Table 9-2278](#).

Return to [Summary Table](#).

N/A

Table 9-2277. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0548h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0548h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0548h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0548h

Figure 9-937. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2278. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.549 PCIE_CORE_RP_DESC1 Register (Offset = 0040054Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-938](#) and described in [Table 9-2280](#).

Return to [Summary Table](#).

N/A

Table 9-2279. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 054Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 054Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 054Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 054Ch

Figure 9-938. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2280. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.550 PCIe_CORE_RP_DESC3 Register (Offset = 00400554h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-939](#) and described in [Table 9-2282](#).

Return to [Summary Table](#).

N/A

Table 9-2281. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0554h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0554h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0554h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0554h

Figure 9-939. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2282. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.551 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400558h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-940](#) and described in [Table 9-2284](#).

Return to [Summary Table](#).

N/A

**Table 9-2283. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0558h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0558h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0558h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0558h

Figure 9-940. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2284. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.552 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040055Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-941](#) and described in [Table 9-2286](#).

Return to [Summary Table](#).

N/A

**Table 9-2285. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 055Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 055Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 055Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 055Ch

Figure 9-941. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2286. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.553 PCIE_CORE_RP_ADDR0 Register (Offset = 00400560h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-942](#) and described in [Table 9-2288](#).

Return to [Summary Table](#).

N/A

Table 9-2287. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0560h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0560h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0560h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0560h

Figure 9-942. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2288. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.554 PCIe_CORE_RP_ADDR1 Register (Offset = 00400564h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-943](#) and described in [Table 9-2290](#).

Return to [Summary Table](#).

N/A

Table 9-2289. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0564h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0564h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0564h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0564h

Figure 9-943. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2290. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.555 PCIE_CORE_RP_DESC0 Register (Offset = 00400568h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-944](#) and described in [Table 9-2292](#).

Return to [Summary Table](#).

N/A

Table 9-2291. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0568h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0568h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0568h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0568h

Figure 9-944. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2292. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.556 PCIe_CORE_RP_DESC1 Register (Offset = 0040056Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-945](#) and described in [Table 9-2294](#).

Return to [Summary Table](#).

N/A

Table 9-2293. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 056Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 056Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 056Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 056Ch

Figure 9-945. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2294. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.557 PCIE_CORE_RP_DESC3 Register (Offset = 00400574h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-946](#) and described in [Table 9-2296](#).

Return to [Summary Table](#).

N/A

Table 9-2295. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0574h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0574h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0574h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0574h

Figure 9-946. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2296. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.558 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400578h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-947](#) and described in [Table 9-2298](#).

Return to [Summary Table](#).

N/A

**Table 9-2297. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0578h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0578h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0578h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0578h

Figure 9-947. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2298. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.559 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040057Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-948](#) and described in [Table 9-2300](#).

Return to [Summary Table](#).

N/A

**Table 9-2299. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 057Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 057Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 057Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 057Ch

Figure 9-948. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2300. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.560 PCIe_CORE_RP_ADDR0 Register (Offset = 00400580h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-949](#) and described in [Table 9-2302](#).

Return to [Summary Table](#).

N/A

Table 9-2301. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0580h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0580h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0580h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0580h

Figure 9-949. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2302. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.561 PCIE_CORE_RP_ADDR1 Register (Offset = 00400584h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-950](#) and described in [Table 9-2304](#).

Return to [Summary Table](#).

N/A

Table 9-2303. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0584h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0584h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0584h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0584h

Figure 9-950. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2304. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.562 PCIe_CORE_RP_DESC0 Register (Offset = 00400588h) [reset = 0h]

PCIe_CORE_RP_DESC0 is shown in [Figure 9-951](#) and described in [Table 9-2306](#).

Return to [Summary Table](#).

N/A

Table 9-2305. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0588h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0588h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0588h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0588h

Figure 9-951. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2306. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.563 PCIE_CORE_RP_DESC1 Register (Offset = 0040058Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-952](#) and described in [Table 9-2308](#).

Return to [Summary Table](#).

N/A

Table 9-2307. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 058Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 058Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 058Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 058Ch

Figure 9-952. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2308. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.564 PCIe_CORE_RP_DESC3 Register (Offset = 00400594h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-953](#) and described in [Table 9-2310](#).

Return to [Summary Table](#).

N/A

Table 9-2309. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0594h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0594h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0594h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0594h

Figure 9-953. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2310. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.565 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400598h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-954](#) and described in [Table 9-2312](#).

Return to [Summary Table](#).

N/A

**Table 9-2311. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0598h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0598h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0598h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0598h

Figure 9-954. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2312. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.566 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040059Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-955](#) and described in [Table 9-2314](#).

Return to [Summary Table](#).

N/A

**Table 9-2313. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 059Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 059Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 059Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 059Ch

Figure 9-955. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2314. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.567 PCIE_CORE_RP_ADDR0 Register (Offset = 004005A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-956](#) and described in [Table 9-2316](#).

Return to [Summary Table](#).

N/A

Table 9-2315. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05A0h

Figure 9-956. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2316. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.568 PCIe_CORE_RP_ADDR1 Register (Offset = 004005A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-957](#) and described in [Table 9-2318](#).

Return to [Summary Table](#).

N/A

Table 9-2317. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05A4h

Figure 9-957. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2318. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.569 PCIE_CORE_RP_DESC0 Register (Offset = 004005A8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-958](#) and described in [Table 9-2320](#).

Return to [Summary Table](#).

N/A

Table 9-2319. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05A8h

Figure 9-958. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2320. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.570 PCIe_CORE_RP_DESC1 Register (Offset = 004005ACh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-959](#) and described in [Table 9-2322](#).

Return to [Summary Table](#).

N/A

Table 9-2321. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05ACh

Figure 9-959. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2322. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.571 PCIE_CORE_RP_DESC3 Register (Offset = 004005B4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-960](#) and described in [Table 9-2324](#).

Return to [Summary Table](#).

N/A

Table 9-2323. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05B4h

Figure 9-960. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2324. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.572 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004005B8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-961](#) and described in [Table 9-2326](#).

Return to [Summary Table](#).

N/A

**Table 9-2325. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05B8h

Figure 9-961. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2326. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.573 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004005BCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-962](#) and described in [Table 9-2328](#).

Return to [Summary Table](#).

N/A

**Table 9-2327. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05BCh

Figure 9-962. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2328. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.574 PCIe_CORE_RP_ADDR0 Register (Offset = 004005C0h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-963](#) and described in [Table 9-2330](#).

Return to [Summary Table](#).

N/A

Table 9-2329. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05C0h

Figure 9-963. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2330. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.575 PCIE_CORE_RP_ADDR1 Register (Offset = 004005C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-964](#) and described in [Table 9-2332](#).

Return to [Summary Table](#).

N/A

Table 9-2331. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05C4h

Figure 9-964. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2332. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.576 PCIe_CORE_RP_DESC0 Register (Offset = 004005C8h) [reset = 0h]

PCIe_CORE_RP_DESC0 is shown in [Figure 9-965](#) and described in [Table 9-2334](#).

Return to [Summary Table](#).

N/A

Table 9-2333. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05C8h

Figure 9-965. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2334. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.577 PCIE_CORE_RP_DESC1 Register (Offset = 004005CCh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-966](#) and described in [Table 9-2336](#).

Return to [Summary Table](#).

N/A

Table 9-2335. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05CCh

Figure 9-966. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2336. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.578 PCIe_CORE_RP_DESC3 Register (Offset = 004005D4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-967](#) and described in [Table 9-2338](#).

Return to [Summary Table](#).

N/A

Table 9-2337. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05D4h

Figure 9-967. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2338. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.579 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004005D8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-968](#) and described in [Table 9-2340](#).

Return to [Summary Table](#).

N/A

**Table 9-2339. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05D8h

Figure 9-968. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2340. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.580 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004005DCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-969](#) and described in [Table 9-2342](#).

Return to [Summary Table](#).

N/A

**Table 9-2341. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05DCh

Figure 9-969. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2342. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.581 PCIE_CORE_RP_ADDR0 Register (Offset = 004005E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-970](#) and described in [Table 9-2344](#).

Return to [Summary Table](#).

N/A

Table 9-2343. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05E0h

Figure 9-970. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2344. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.582 PCIe_CORE_RP_ADDR1 Register (Offset = 004005E4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-971](#) and described in [Table 9-2346](#).

Return to [Summary Table](#).

N/A

Table 9-2345. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05E4h

Figure 9-971. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2346. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.583 PCIE_CORE_RP_DESC0 Register (Offset = 004005E8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-972](#) and described in [Table 9-2348](#).

Return to [Summary Table](#).

N/A

Table 9-2347. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05E8h

Figure 9-972. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2348. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.584 PCIE_CORE_RP_DESC1 Register (Offset = 004005ECh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-973](#) and described in [Table 9-2350](#).

Return to [Summary Table](#).

N/A

Table 9-2349. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05ECh

Figure 9-973. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2350. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.585 PCIE_CORE_RP_DESC3 Register (Offset = 004005F4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-974](#) and described in [Table 9-2352](#).

Return to [Summary Table](#).

N/A

Table 9-2351. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05F4h

Figure 9-974. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2352. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.586 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004005F8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-975](#) and described in [Table 9-2354](#).

Return to [Summary Table](#).

N/A

**Table 9-2353. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05F8h

Figure 9-975. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2354. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.587 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004005FCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-976](#) and described in [Table 9-2356](#).

Return to [Summary Table](#).

N/A

**Table 9-2355. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 05FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 05FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 05FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 05FCh

Figure 9-976. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2356. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.588 PCIe_CORE_RP_ADDR0 Register (Offset = 00400600h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-977](#) and described in [Table 9-2358](#).

Return to [Summary Table](#).

N/A

Table 9-2357. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0600h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0600h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0600h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0600h

Figure 9-977. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2358. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.589 PCIE_CORE_RP_ADDR1 Register (Offset = 00400604h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-978](#) and described in [Table 9-2360](#).

Return to [Summary Table](#).

N/A

Table 9-2359. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0604h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0604h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0604h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0604h

Figure 9-978. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2360. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.590 PCIe_CORE_RP_DESC0 Register (Offset = 00400608h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-979](#) and described in [Table 9-2362](#).

Return to [Summary Table](#).

N/A

Table 9-2361. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0608h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0608h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0608h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0608h

Figure 9-979. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2362. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.591 PCIE_CORE_RP_DESC1 Register (Offset = 0040060Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-980](#) and described in [Table 9-2364](#).

Return to [Summary Table](#).

N/A

Table 9-2363. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 060Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 060Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 060Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 060Ch

Figure 9-980. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2364. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.592 PCIe_CORE_RP_DESC3 Register (Offset = 00400614h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-981](#) and described in [Table 9-2366](#).

Return to [Summary Table](#).

N/A

Table 9-2365. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0614h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0614h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0614h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0614h

Figure 9-981. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2366. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.593 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400618h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-982](#) and described in [Table 9-2368](#).

Return to [Summary Table](#).

N/A

**Table 9-2367. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0618h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0618h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0618h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0618h

Figure 9-982. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2368. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.594 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040061Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-983](#) and described in [Table 9-2370](#).

Return to [Summary Table](#).

N/A

**Table 9-2369. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 061Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 061Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 061Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 061Ch

Figure 9-983. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2370. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.595 PCIE_CORE_RP_ADDR0 Register (Offset = 00400620h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-984](#) and described in [Table 9-2372](#).

Return to [Summary Table](#).

N/A

Table 9-2371. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0620h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0620h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0620h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0620h

Figure 9-984. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2372. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.596 PCIe_CORE_RP_ADDR1 Register (Offset = 00400624h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-985](#) and described in [Table 9-2374](#).

Return to [Summary Table](#).

N/A

Table 9-2373. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0624h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0624h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0624h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0624h

Figure 9-985. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2374. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.597 PCIE_CORE_RP_DESC0 Register (Offset = 00400628h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-986](#) and described in [Table 9-2376](#).

Return to [Summary Table](#).

N/A

Table 9-2375. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0628h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0628h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0628h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0628h

Figure 9-986. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2376. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.598 PCIe_CORE_RP_DESC1 Register (Offset = 0040062Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-987](#) and described in [Table 9-2378](#).

Return to [Summary Table](#).

N/A

Table 9-2377. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 062Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 062Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 062Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 062Ch

Figure 9-987. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2378. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.599 PCIE_CORE_RP_DESC3 Register (Offset = 00400634h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-988](#) and described in [Table 9-2380](#).

Return to [Summary Table](#).

N/A

Table 9-2379. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0634h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0634h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0634h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0634h

Figure 9-988. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2380. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.600 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400638h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-989](#) and described in [Table 9-2382](#).

Return to [Summary Table](#).

N/A

**Table 9-2381. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0638h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0638h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0638h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0638h

Figure 9-989. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2382. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.601 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040063Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-990](#) and described in [Table 9-2384](#).

Return to [Summary Table](#).

N/A

**Table 9-2383. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 063Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 063Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 063Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 063Ch

Figure 9-990. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2384. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.602 PCIe_CORE_RP_ADDR0 Register (Offset = 00400640h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-991](#) and described in [Table 9-2386](#).

Return to [Summary Table](#).

N/A

Table 9-2385. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0640h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0640h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0640h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0640h

Figure 9-991. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2386. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.603 PCIE_CORE_RP_ADDR1 Register (Offset = 00400644h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-992](#) and described in [Table 9-2388](#).

Return to [Summary Table](#).

N/A

Table 9-2387. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0644h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0644h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0644h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0644h

Figure 9-992. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2388. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.604 PCIe_CORE_RP_DESC0 Register (Offset = 00400648h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-993](#) and described in [Table 9-2390](#).

Return to [Summary Table](#).

N/A

Table 9-2389. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0648h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0648h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0648h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0648h

Figure 9-993. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2390. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.605 PCIE_CORE_RP_DESC1 Register (Offset = 0040064Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-994](#) and described in [Table 9-2392](#).

Return to [Summary Table](#).

N/A

Table 9-2391. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 064Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 064Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 064Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 064Ch

Figure 9-994. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2392. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.606 PCIe_CORE_RP_DESC3 Register (Offset = 00400654h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-995](#) and described in [Table 9-2394](#).

Return to [Summary Table](#).

N/A

Table 9-2393. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0654h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0654h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0654h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0654h

Figure 9-995. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2394. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.607 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400658h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-996](#) and described in [Table 9-2396](#).

Return to [Summary Table](#).

N/A

**Table 9-2395. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0658h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0658h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0658h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0658h

Figure 9-996. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2396. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.608 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040065Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-997](#) and described in [Table 9-2398](#).

Return to [Summary Table](#).

N/A

**Table 9-2397. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 065Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 065Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 065Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 065Ch

Figure 9-997. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2398. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.609 PCIE_CORE_RP_ADDR0 Register (Offset = 00400660h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-998](#) and described in [Table 9-2400](#).

Return to [Summary Table](#).

N/A

Table 9-2399. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0660h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0660h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0660h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0660h

Figure 9-998. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2400. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.610 PCIe_CORE_RP_ADDR1 Register (Offset = 00400664h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-999](#) and described in [Table 9-2402](#).

Return to [Summary Table](#).

N/A

Table 9-2401. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0664h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0664h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0664h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0664h

Figure 9-999. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2402. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.611 PCIE_CORE_RP_DESC0 Register (Offset = 00400668h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1000](#) and described in [Table 9-2404](#).

Return to [Summary Table](#).

N/A

Table 9-2403. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0668h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0668h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0668h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0668h

Figure 9-1000. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2404. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.612 PCIe_CORE_RP_DESC1 Register (Offset = 0040066Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1001](#) and described in [Table 9-2406](#).

Return to [Summary Table](#).

N/A

Table 9-2405. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 066Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 066Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 066Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 066Ch

Figure 9-1001. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2406. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.613 PCIE_CORE_RP_DESC3 Register (Offset = 00400674h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1002](#) and described in [Table 9-2408](#).

Return to [Summary Table](#).

N/A

Table 9-2407. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0674h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0674h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0674h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0674h

Figure 9-1002. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2408. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.614 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400678h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1003](#) and described in [Table 9-2410](#).

Return to [Summary Table](#).

N/A

**Table 9-2409. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0678h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0678h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0678h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0678h

Figure 9-1003. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2410. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.615 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040067Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1004](#) and described in [Table 9-2412](#).

Return to [Summary Table](#).

N/A

**Table 9-2411. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 067Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 067Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 067Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 067Ch

Figure 9-1004. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2412. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.616 PCIe_CORE_RP_ADDR0 Register (Offset = 00400680h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1005](#) and described in [Table 9-2414](#).

Return to [Summary Table](#).

N/A

Table 9-2413. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0680h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0680h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0680h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0680h

Figure 9-1005. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2414. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.617 PCIE_CORE_RP_ADDR1 Register (Offset = 00400684h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1006](#) and described in [Table 9-2416](#).

Return to [Summary Table](#).

N/A

Table 9-2415. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0684h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0684h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0684h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0684h

Figure 9-1006. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2416. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.618 PCIe_CORE_RP_DESC0 Register (Offset = 00400688h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1007](#) and described in [Table 9-2418](#).

Return to [Summary Table](#).

N/A

Table 9-2417. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0688h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0688h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0688h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0688h

Figure 9-1007. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2418. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.619 PCIE_CORE_RP_DESC1 Register (Offset = 0040068Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1008](#) and described in [Table 9-2420](#).

Return to [Summary Table](#).

N/A

Table 9-2419. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 068Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 068Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 068Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 068Ch

Figure 9-1008. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2420. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.620 PCIe_CORE_RP_DESC3 Register (Offset = 00400694h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1009](#) and described in [Table 9-2422](#).

Return to [Summary Table](#).

N/A

Table 9-2421. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0694h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0694h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0694h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0694h

Figure 9-1009. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2422. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.621 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400698h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1010](#) and described in [Table 9-2424](#).

Return to [Summary Table](#).

N/A

**Table 9-2423. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0698h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0698h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0698h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0698h

Figure 9-1010. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2424. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.622 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040069Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1011](#) and described in [Table 9-2426](#).

Return to [Summary Table](#).

N/A

**Table 9-2425. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 069Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 069Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 069Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 069Ch

Figure 9-1011. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2426. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.623 PCIE_CORE_RP_ADDR0 Register (Offset = 004006A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1012](#) and described in [Table 9-2428](#).

Return to [Summary Table](#).

N/A

Table 9-2427. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06A0h

Figure 9-1012. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2428. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.624 PCIe_CORE_RP_ADDR1 Register (Offset = 004006A4h) [reset = 0h]

PCIe_CORE_RP_ADDR1 is shown in [Figure 9-1013](#) and described in [Table 9-2430](#).

Return to [Summary Table](#).

N/A

Table 9-2429. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06A4h

Figure 9-1013. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2430. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.625 PCIE_CORE_RP_DESC0 Register (Offset = 004006A8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1014](#) and described in [Table 9-2432](#).

Return to [Summary Table](#).

N/A

Table 9-2431. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06A8h

Figure 9-1014. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2432. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.626 PCIe_CORE_RP_DESC1 Register (Offset = 004006ACh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1015](#) and described in [Table 9-2434](#).

Return to [Summary Table](#).

N/A

Table 9-2433. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06ACh

Figure 9-1015. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2434. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.627 PCIE_CORE_RP_DESC3 Register (Offset = 004006B4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1016](#) and described in [Table 9-2436](#).

Return to [Summary Table](#).

N/A

Table 9-2435. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06B4h

Figure 9-1016. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2436. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.628 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004006B8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1017](#) and described in [Table 9-2438](#).

Return to [Summary Table](#).

N/A

**Table 9-2437. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06B8h

Figure 9-1017. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2438. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.629 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004006BCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1018](#) and described in [Table 9-2440](#).

Return to [Summary Table](#).

N/A

**Table 9-2439. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06BCh

Figure 9-1018. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2440. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.630 PCIe_CORE_RP_ADDR0 Register (Offset = 004006C0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1019](#) and described in [Table 9-2442](#).

Return to [Summary Table](#).

N/A

Table 9-2441. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06C0h

Figure 9-1019. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2442. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.631 PCIE_CORE_RP_ADDR1 Register (Offset = 004006C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1020](#) and described in [Table 9-2444](#).

Return to [Summary Table](#).

N/A

Table 9-2443. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06C4h

Figure 9-1020. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2444. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.632 PCIe_CORE_RP_DESC0 Register (Offset = 004006C8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1021](#) and described in [Table 9-2446](#).

Return to [Summary Table](#).

N/A

Table 9-2445. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06C8h

Figure 9-1021. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2446. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.633 PCIE_CORE_RP_DESC1 Register (Offset = 004006CCh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1022](#) and described in [Table 9-2448](#).

Return to [Summary Table](#).

N/A

Table 9-2447. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06CCh

Figure 9-1022. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2448. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.634 PCIE_CORE_RP_DESC3 Register (Offset = 004006D4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1023](#) and described in [Table 9-2450](#).

Return to [Summary Table](#).

N/A

Table 9-2449. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06D4h

Figure 9-1023. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2450. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.635 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004006D8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1024](#) and described in [Table 9-2452](#).

Return to [Summary Table](#).

N/A

**Table 9-2451. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06D8h

Figure 9-1024. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2452. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.636 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004006DCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1025](#) and described in [Table 9-2454](#).

Return to [Summary Table](#).

N/A

**Table 9-2453. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06DCh

Figure 9-1025. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2454. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.637 PCIE_CORE_RP_ADDR0 Register (Offset = 004006E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1026](#) and described in [Table 9-2456](#).

Return to [Summary Table](#).

N/A

Table 9-2455. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06E0h

Figure 9-1026. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2456. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.638 PCIe_CORE_RP_ADDR1 Register (Offset = 004006E4h) [reset = 0h]

PCIe_CORE_RP_ADDR1 is shown in [Figure 9-1027](#) and described in [Table 9-2458](#).

Return to [Summary Table](#).

N/A

Table 9-2457. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06E4h

Figure 9-1027. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2458. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.639 PCIE_CORE_RP_DESC0 Register (Offset = 004006E8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1028](#) and described in [Table 9-2460](#).

Return to [Summary Table](#).

N/A

Table 9-2459. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06E8h

Figure 9-1028. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2460. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.640 PCIe_CORE_RP_DESC1 Register (Offset = 004006ECh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1029](#) and described in [Table 9-2462](#).

Return to [Summary Table](#).

N/A

Table 9-2461. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06ECh

Figure 9-1029. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2462. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.641 PCIE_CORE_RP_DESC3 Register (Offset = 004006F4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1030](#) and described in [Table 9-2464](#).

Return to [Summary Table](#).

N/A

Table 9-2463. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06F4h

Figure 9-1030. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2464. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.642 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004006F8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1031](#) and described in [Table 9-2466](#).

Return to [Summary Table](#).

N/A

**Table 9-2465. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06F8h

Figure 9-1031. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2466. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.643 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004006FCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1032](#) and described in [Table 9-2468](#).

Return to [Summary Table](#).

N/A

**Table 9-2467. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 06FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 06FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 06FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 06FCh

Figure 9-1032. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2468. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.644 PCIE_CORE_RP_ADDR0 Register (Offset = 00400700h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1033](#) and described in [Table 9-2470](#).

Return to [Summary Table](#).

N/A

Table 9-2469. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0700h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0700h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0700h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0700h

Figure 9-1033. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2470. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.645 PCIE_CORE_RP_ADDR1 Register (Offset = 00400704h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1034](#) and described in [Table 9-2472](#).

Return to [Summary Table](#).

N/A

Table 9-2471. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0704h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0704h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0704h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0704h

Figure 9-1034. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2472. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.646 PCIe_CORE_RP_DESC0 Register (Offset = 00400708h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1035](#) and described in [Table 9-2474](#).

Return to [Summary Table](#).

N/A

Table 9-2473. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0708h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0708h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0708h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0708h

Figure 9-1035. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2474. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.647 PCIE_CORE_RP_DESC1 Register (Offset = 0040070Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1036](#) and described in [Table 9-2476](#).

Return to [Summary Table](#).

N/A

Table 9-2475. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 070Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 070Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 070Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 070Ch

Figure 9-1036. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2476. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.648 PCIE_CORE_RP_DESC3 Register (Offset = 00400714h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1037](#) and described in [Table 9-2478](#).

Return to [Summary Table](#).

N/A

Table 9-2477. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0714h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0714h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0714h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0714h

Figure 9-1037. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2478. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.649 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400718h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1038](#) and described in [Table 9-2480](#).

Return to [Summary Table](#).

N/A

**Table 9-2479. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0718h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0718h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0718h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0718h

Figure 9-1038. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2480. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.650 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040071Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1039](#) and described in [Table 9-2482](#).

Return to [Summary Table](#).

N/A

**Table 9-2481. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 071Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 071Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 071Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 071Ch

Figure 9-1039. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2482. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.651 PCIE_CORE_RP_ADDR0 Register (Offset = 00400720h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1040](#) and described in [Table 9-2484](#).

Return to [Summary Table](#).

N/A

Table 9-2483. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0720h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0720h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0720h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0720h

Figure 9-1040. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2484. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.652 PCIe_CORE_RP_ADDR1 Register (Offset = 00400724h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1041](#) and described in [Table 9-2486](#).

Return to [Summary Table](#).

N/A

Table 9-2485. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0724h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0724h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0724h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0724h

Figure 9-1041. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2486. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.653 PCIE_CORE_RP_DESC0 Register (Offset = 00400728h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1042](#) and described in [Table 9-2488](#).

Return to [Summary Table](#).

N/A

Table 9-2487. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0728h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0728h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0728h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0728h

Figure 9-1042. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2488. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.654 PCIe_CORE_RP_DESC1 Register (Offset = 0040072Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1043](#) and described in [Table 9-2490](#).

Return to [Summary Table](#).

N/A

Table 9-2489. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 072Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 072Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 072Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 072Ch

Figure 9-1043. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2490. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.655 PCIE_CORE_RP_DESC3 Register (Offset = 00400734h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1044](#) and described in [Table 9-2492](#).

Return to [Summary Table](#).

N/A

Table 9-2491. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0734h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0734h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0734h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0734h

Figure 9-1044. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2492. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.656 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400738h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1045](#) and described in [Table 9-2494](#).

Return to [Summary Table](#).

N/A

**Table 9-2493. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0738h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0738h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0738h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0738h

Figure 9-1045. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2494. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.657 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040073Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1046](#) and described in [Table 9-2496](#).

Return to [Summary Table](#).

N/A

**Table 9-2495. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 073Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 073Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 073Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 073Ch

Figure 9-1046. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2496. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.658 PCIe_CORE_RP_ADDR0 Register (Offset = 00400740h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1047](#) and described in [Table 9-2498](#).

Return to [Summary Table](#).

N/A

Table 9-2497. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0740h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0740h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0740h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0740h

Figure 9-1047. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2498. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.659 PCIE_CORE_RP_ADDR1 Register (Offset = 00400744h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1048](#) and described in [Table 9-2500](#).

Return to [Summary Table](#).

N/A

Table 9-2499. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0744h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0744h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0744h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0744h

Figure 9-1048. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2500. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.660 PCIe_CORE_RP_DESC0 Register (Offset = 00400748h) [reset = 0h]

PCIe_CORE_RP_DESC0 is shown in [Figure 9-1049](#) and described in [Table 9-2502](#).

Return to [Summary Table](#).

N/A

Table 9-2501. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0748h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0748h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0748h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0748h

Figure 9-1049. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2502. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.661 PCIE_CORE_RP_DESC1 Register (Offset = 0040074Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1050](#) and described in [Table 9-2504](#).

Return to [Summary Table](#).

N/A

Table 9-2503. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 074Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 074Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 074Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 074Ch

Figure 9-1050. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2504. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.662 PCIe_CORE_RP_DESC3 Register (Offset = 00400754h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1051](#) and described in [Table 9-2506](#).

Return to [Summary Table](#).

N/A

Table 9-2505. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0754h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0754h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0754h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0754h

Figure 9-1051. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2506. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.663 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400758h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1052](#) and described in [Table 9-2508](#).

Return to [Summary Table](#).

N/A

**Table 9-2507. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0758h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0758h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0758h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0758h

Figure 9-1052. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2508. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.664 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040075Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1053](#) and described in [Table 9-2510](#).

Return to [Summary Table](#).

N/A

**Table 9-2509. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 075Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 075Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 075Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 075Ch

Figure 9-1053. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2510. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.665 PCIE_CORE_RP_ADDR0 Register (Offset = 00400760h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1054](#) and described in [Table 9-2512](#).

Return to [Summary Table](#).

N/A

Table 9-2511. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0760h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0760h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0760h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0760h

Figure 9-1054. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2512. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.666 PCIe_CORE_RP_ADDR1 Register (Offset = 00400764h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1055](#) and described in [Table 9-2514](#).

Return to [Summary Table](#).

N/A

Table 9-2513. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0764h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0764h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0764h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0764h

Figure 9-1055. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2514. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.667 PCIE_CORE_RP_DESC0 Register (Offset = 00400768h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1056](#) and described in [Table 9-2516](#).

Return to [Summary Table](#).

N/A

Table 9-2515. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0768h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0768h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0768h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0768h

Figure 9-1056. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2516. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.668 PCIe_CORE_RP_DESC1 Register (Offset = 0040076Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1057](#) and described in [Table 9-2518](#).

Return to [Summary Table](#).

N/A

Table 9-2517. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 076Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 076Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 076Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 076Ch

Figure 9-1057. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2518. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.669 PCIE_CORE_RP_DESC3 Register (Offset = 00400774h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1058](#) and described in [Table 9-2520](#).

Return to [Summary Table](#).

N/A

Table 9-2519. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0774h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0774h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0774h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0774h

Figure 9-1058. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2520. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.670 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400778h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1059](#) and described in [Table 9-2522](#).

Return to [Summary Table](#).

N/A

**Table 9-2521. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0778h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0778h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0778h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0778h

Figure 9-1059. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2522. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.671 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040077Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1060](#) and described in [Table 9-2524](#).

Return to [Summary Table](#).

N/A

**Table 9-2523. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 077Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 077Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 077Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 077Ch

Figure 9-1060. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2524. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.672 PCIe_CORE_RP_ADDR0 Register (Offset = 00400780h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1061](#) and described in [Table 9-2526](#).

Return to [Summary Table](#).

N/A

Table 9-2525. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0780h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0780h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0780h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0780h

Figure 9-1061. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2526. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.673 PCIE_CORE_RP_ADDR1 Register (Offset = 00400784h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1062](#) and described in [Table 9-2528](#).

Return to [Summary Table](#).

N/A

Table 9-2527. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0784h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0784h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0784h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0784h

Figure 9-1062. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2528. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.674 PCIE_CORE_RP_DESC0 Register (Offset = 00400788h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1063](#) and described in [Table 9-2530](#).

Return to [Summary Table](#).

N/A

Table 9-2529. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0788h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0788h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0788h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0788h

Figure 9-1063. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2530. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.675 PCIE_CORE_RP_DESC1 Register (Offset = 0040078Ch) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1064](#) and described in [Table 9-2532](#).

Return to [Summary Table](#).

N/A

Table 9-2531. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 078Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 078Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 078Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 078Ch

Figure 9-1064. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2532. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.676 PCIe_CORE_RP_DESC3 Register (Offset = 00400794h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1065](#) and described in [Table 9-2534](#).

Return to [Summary Table](#).

N/A

Table 9-2533. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0794h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0794h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0794h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0794h

Figure 9-1065. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2534. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.677 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 00400798h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1066](#) and described in [Table 9-2536](#).

Return to [Summary Table](#).

N/A

**Table 9-2535. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0798h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0798h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0798h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0798h

Figure 9-1066. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2536. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.678 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 0040079Ch) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1067](#) and described in [Table 9-2538](#).

Return to [Summary Table](#).

N/A

**Table 9-2537. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 079Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 079Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 079Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 079Ch

Figure 9-1067. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2538. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.679 PCIE_CORE_RP_ADDR0 Register (Offset = 004007A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1068](#) and described in [Table 9-2540](#).

Return to [Summary Table](#).

N/A

Table 9-2539. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07A0h

Figure 9-1068. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2540. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.680 PCIe_CORE_RP_ADDR1 Register (Offset = 004007A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1069](#) and described in [Table 9-2542](#).

Return to [Summary Table](#).

N/A

Table 9-2541. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07A4h

Figure 9-1069. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2542. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.681 PCIE_CORE_RP_DESC0 Register (Offset = 004007A8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1070](#) and described in [Table 9-2544](#).

Return to [Summary Table](#).

N/A

Table 9-2543. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07A8h

Figure 9-1070. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2544. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.682 PCIe_CORE_RP_DESC1 Register (Offset = 004007ACh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1071](#) and described in [Table 9-2546](#).

Return to [Summary Table](#).

N/A

Table 9-2545. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07ACh

Figure 9-1071. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2546. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.683 PCIE_CORE_RP_DESC3 Register (Offset = 004007B4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1072](#) and described in [Table 9-2548](#).

Return to [Summary Table](#).

N/A

Table 9-2547. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07B4h

Figure 9-1072. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2548. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.684 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004007B8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1073](#) and described in [Table 9-2550](#).

Return to [Summary Table](#).

N/A

**Table 9-2549. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07B8h

Figure 9-1073. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2550. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.685 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004007BCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1074](#) and described in [Table 9-2552](#).

Return to [Summary Table](#).

N/A

Table 9-2551. PCIE_CORE_RP_AXI_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07BCh

Figure 9-1074. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2552. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.686 PCIe_CORE_RP_ADDR0 Register (Offset = 004007C0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1075](#) and described in [Table 9-2554](#).

Return to [Summary Table](#).

N/A

Table 9-2553. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07C0h

Figure 9-1075. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2554. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.687 PCIE_CORE_RP_ADDR1 Register (Offset = 004007C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1076](#) and described in [Table 9-2556](#).

Return to [Summary Table](#).

N/A

Table 9-2555. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07C4h

Figure 9-1076. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2556. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.688 PCIe_CORE_RP_DESC0 Register (Offset = 004007C8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1077](#) and described in [Table 9-2558](#).

Return to [Summary Table](#).

N/A

Table 9-2557. PCIe_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07C8h

Figure 9-1077. PCIe_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2558. PCIe_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.689 PCIE_CORE_RP_DESC1 Register (Offset = 004007CCh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1078](#) and described in [Table 9-2560](#).

Return to [Summary Table](#).

N/A

Table 9-2559. PCIE_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07CCh

Figure 9-1078. PCIE_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2560. PCIE_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.690 PCIe_CORE_RP_DESC3 Register (Offset = 004007D4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1079](#) and described in [Table 9-2562](#).

Return to [Summary Table](#).

N/A

Table 9-2561. PCIe_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07D4h

Figure 9-1079. PCIe_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2562. PCIe_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.691 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004007D8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1080](#) and described in [Table 9-2564](#).

Return to [Summary Table](#).

N/A

**Table 9-2563. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07D8h

Figure 9-1080. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2564. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.692 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004007DCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1081](#) and described in [Table 9-2566](#).

Return to [Summary Table](#).

N/A

**Table 9-2565. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07DCh

Figure 9-1081. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2566. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.693 PCIE_CORE_RP_ADDR0 Register (Offset = 004007E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1082](#) and described in [Table 9-2568](#).

Return to [Summary Table](#).

N/A

Table 9-2567. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07E0h

Figure 9-1082. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2568. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of PCIe Address Register for region N
7-6	RSVD	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	Number_bits + 1 bits are passed through from AXI address to the PCIe address

9.5.694 PCIe_CORE_RP_ADDR1 Register (Offset = 004007E4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1083](#) and described in [Table 9-2570](#).

Return to [Summary Table](#).

N/A

Table 9-2569. PCIe_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07E4h

Figure 9-1083. PCIe_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2570. PCIe_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of PCIe Address Register for region N

9.5.695 PCIE_CORE_RP_DESC0 Register (Offset = 004007E8h) [reset = 0h]

PCIE_CORE_RP_DESC0 is shown in [Figure 9-1084](#) and described in [Table 9-2572](#).

Return to [Summary Table](#).

N/A

Table 9-2571. PCIE_CORE_RP_DESC0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07E8h

Figure 9-1084. PCIE_CORE_RP_DESC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2572. PCIE_CORE_RP_DESC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lowest 32-bits of PCIe Descriptor Register for region N

9.5.696 PCIe_CORE_RP_DESC1 Register (Offset = 004007ECh) [reset = 0h]

PCIE_CORE_RP_DESC1 is shown in [Figure 9-1085](#) and described in [Table 9-2574](#).

Return to [Summary Table](#).

N/A

Table 9-2573. PCIe_CORE_RP_DESC1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07ECh

Figure 9-1085. PCIe_CORE_RP_DESC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2574. PCIe_CORE_RP_DESC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Lower middle 32-bits of PCIe Descriptor Register for region N

9.5.697 PCIE_CORE_RP_DESC3 Register (Offset = 004007F4h) [reset = 0h]

PCIE_CORE_RP_DESC3 is shown in [Figure 9-1086](#) and described in [Table 9-2576](#).

Return to [Summary Table](#).

N/A

Table 9-2575. PCIE_CORE_RP_DESC3 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07F4h

Figure 9-1086. PCIE_CORE_RP_DESC3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										DATA																					
R-0h										R/W-0h																					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2576. PCIE_CORE_RP_DESC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RSVD	R	0h	reserved
22-0	DATA	R/W	0h	{Execute Permission Supported, Privileged Mode Supported, PASID Value, PASID present bit}

9.5.698 PCIE_CORE_RP_AXI_ADDR0 Register (Offset = 004007F8h) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR0 is shown in [Figure 9-1087](#) and described in [Table 9-2578](#).

Return to [Summary Table](#).

N/A

**Table 9-2577. PCIE_CORE_RP_AXI_ADDR0
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07F8h

Figure 9-1087. PCIE_CORE_RP_AXI_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD		REGION_SIZE					
R/W-0h								R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2578. PCIE_CORE_RP_AXI_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of Outbound AXI Region Base Address Register used to decode the region
7-6	RSVD	R/W	0h	These needs to be forced to 0
5-0	REGION_SIZE	R/W	0h	the value programmed in this field + 1 gives the region size

9.5.699 PCIE_CORE_RP_AXI_ADDR1 Register (Offset = 004007FCh) [reset = 0h]

PCIE_CORE_RP_AXI_ADDR1 is shown in [Figure 9-1088](#) and described in [Table 9-2580](#).

Return to [Summary Table](#).

N/A

**Table 9-2579. PCIE_CORE_RP_AXI_ADDR1
Instances**

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 07FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 07FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 07FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 07FCh

Figure 9-1088. PCIE_CORE_RP_AXI_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2580. PCIE_CORE_RP_AXI_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI outbound Base Address Register used to decode the region

9.5.700 PCIe_CORE_RP_ADDR0 Register (Offset = 00400800h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1089](#) and described in [Table 9-2582](#).

Return to [Summary Table](#).

N/A

Table 9-2581. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0800h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0800h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0800h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0800h

Figure 9-1089. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD0		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2582. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of AXI Address Register for BAR N
7-6	RSVD0	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	The value programmed in this register +1 bits are passed through from PCIe to AXI

9.5.701 PCIE_CORE_RP_ADDR1 Register (Offset = 00400804h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1090](#) and described in [Table 9-2584](#).

Return to [Summary Table](#).

N/A

Table 9-2583. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0804h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0804h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0804h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0804h

Figure 9-1090. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2584. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.702 PCIE_CORE_RP_ADDR0 Register (Offset = 00400808h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1091](#) and described in [Table 9-2586](#).

Return to [Summary Table](#).

N/A

Table 9-2585. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0808h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0808h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0808h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0808h

Figure 9-1091. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD0		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2586. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of AXI Address Register for BAR N
7-6	RSVD0	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	The value programmed in this register +1 bits are passed through from PCIe to AXI

9.5.703 PCIE_CORE_RP_ADDR1 Register (Offset = 0040080Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1092](#) and described in [Table 9-2588](#).

Return to [Summary Table](#).

N/A

Table 9-2587. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 080Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 080Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 080Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 080Ch

Figure 9-1092. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2588. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.704 PCIE_CORE_RP_ADDR0 Register (Offset = 00400810h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1093](#) and described in [Table 9-2590](#).

Return to [Summary Table](#).

N/A

Table 9-2589. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0810h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0810h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0810h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0810h

Figure 9-1093. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA								RSVD0		NUM_BITS					
R/W-0h								R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-2590. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	DATA	R/W	0h	Bits [31:8] of AXI Address Register for BAR N
7-6	RSVD0	R	0h	Bits 7 and 6 are reserved
5-0	NUM_BITS	R/W	0h	The value programmed in this register +1 bits are passed through from PCIe to AXI

9.5.705 PCIE_CORE_RP_ADDR1 Register (Offset = 00400814h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1094](#) and described in [Table 9-2592](#).

Return to [Summary Table](#).

N/A

Table 9-2591. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0814h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0814h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0814h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0814h

Figure 9-1094. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2592. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.706 PCIe_CORE_RP_C0 Register (Offset = 00400820h) [reset = X]

PCIe_CORE_RP_C0 is shown in [Figure 9-1095](#) and described in [Table 9-2594](#).

Return to [Summary Table](#).

N/A

Table 9-2593. PCIe_CORE_RP_C0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0820h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0820h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0820h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0820h

Figure 9-1095. PCIe_CORE_RP_C0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												HEADER						DATA													
R/W-X												R/W-1h						R/W-10h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2594. PCIe_CORE_RP_C0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-12	HEADER	R/W	1h	This is the threshold value of the header credits required which is used to flag credit availability in AXI wrapper
11-0	DATA	R/W	10h	This is the threshold value of the payload credits required which is used to flag credit availability in AXI wrapper

9.5.707 PCIE_CORE_RP_L0 Register (Offset = 00400824h) [reset = X]

PCIE_CORE_RP_L0 is shown in [Figure 9-1096](#) and described in [Table 9-2596](#).

Return to [Summary Table](#).

N/A

Table 9-2595. PCIE_CORE_RP_L0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0824h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0824h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0824h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0824h

Figure 9-1096. PCIE_CORE_RP_L0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							CLEAR_LINK_DOWN_BIT_TO_PROCEED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2596. PCIE_CORE_RP_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	CLEAR_LINK_DOWN_BIT_TO_PROCEED	R/W	0h	This bit will be set when link down reset comes. client should clear this bit before issuing new traffic to the core

9.5.708 PCIe_CORE_RP_ADDR0 Register (Offset = 00400840h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1097](#) and described in [Table 9-2598](#).

Return to [Summary Table](#).

N/A

Table 9-2597. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0840h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0840h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0840h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0840h

Figure 9-1097. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2598. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.709 PCIE_CORE_RP_ADDR1 Register (Offset = 00400844h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1098](#) and described in [Table 9-2600](#).

Return to [Summary Table](#).

N/A

Table 9-2599. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0844h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0844h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0844h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0844h

Figure 9-1098. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2600. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.710 PCIe_CORE_RP_ADDR0 Register (Offset = 00400848h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1099](#) and described in [Table 9-2602](#).

Return to [Summary Table](#).

N/A

Table 9-2601. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0848h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0848h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0848h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0848h

Figure 9-1099. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2602. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.711 PCIE_CORE_RP_ADDR1 Register (Offset = 0040084Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1100](#) and described in [Table 9-2604](#).

Return to [Summary Table](#).

N/A

Table 9-2603. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 084Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 084Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 084Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 084Ch

Figure 9-1100. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2604. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.712 PCIe_CORE_RP_ADDR0 Register (Offset = 00400850h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1101](#) and described in [Table 9-2606](#).

Return to [Summary Table](#).

N/A

Table 9-2605. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0850h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0850h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0850h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0850h

Figure 9-1101. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2606. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.713 PCIE_CORE_RP_ADDR1 Register (Offset = 00400854h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1102](#) and described in [Table 9-2608](#).

Return to [Summary Table](#).

N/A

Table 9-2607. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0854h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0854h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0854h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0854h

Figure 9-1102. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2608. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.714 PCIe_CORE_RP_ADDR0 Register (Offset = 00400858h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1103](#) and described in [Table 9-2610](#).

Return to [Summary Table](#).

N/A

Table 9-2609. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0858h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0858h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0858h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0858h

Figure 9-1103. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2610. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.715 PCIE_CORE_RP_ADDR1 Register (Offset = 0040085Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1104](#) and described in [Table 9-2612](#).

Return to [Summary Table](#).

N/A

Table 9-2611. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 085Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 085Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 085Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 085Ch

Figure 9-1104. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2612. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.716 PCIe_CORE_RP_ADDR0 Register (Offset = 00400860h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1105](#) and described in [Table 9-2614](#).

Return to [Summary Table](#).

N/A

Table 9-2613. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0860h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0860h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0860h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0860h

Figure 9-1105. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2614. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.717 PCIE_CORE_RP_ADDR1 Register (Offset = 00400864h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1106](#) and described in [Table 9-2616](#).

Return to [Summary Table](#).

N/A

Table 9-2615. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0864h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0864h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0864h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0864h

Figure 9-1106. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2616. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.718 PCIe_CORE_RP_ADDR0 Register (Offset = 00400868h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1107](#) and described in [Table 9-2618](#).

Return to [Summary Table](#).

N/A

Table 9-2617. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0868h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0868h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0868h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0868h

Figure 9-1107. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2618. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.719 PCIE_CORE_RP_ADDR1 Register (Offset = 0040086Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1108](#) and described in [Table 9-2620](#).

Return to [Summary Table](#).

N/A

Table 9-2619. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 086Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 086Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 086Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 086Ch

Figure 9-1108. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2620. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.720 PCIe_CORE_RP_ADDR0 Register (Offset = 00400870h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1109](#) and described in [Table 9-2622](#).

Return to [Summary Table](#).

N/A

Table 9-2621. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0870h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0870h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0870h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0870h

Figure 9-1109. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2622. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.721 PCIE_CORE_RP_ADDR1 Register (Offset = 00400874h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1110](#) and described in [Table 9-2624](#).

Return to [Summary Table](#).

N/A

Table 9-2623. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0874h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0874h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0874h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0874h

Figure 9-1110. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2624. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.722 PCIe_CORE_RP_ADDR0 Register (Offset = 00400878h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1111](#) and described in [Table 9-2626](#).

Return to [Summary Table](#).

N/A

Table 9-2625. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0878h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0878h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0878h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0878h

Figure 9-1111. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2626. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.723 PCIE_CORE_RP_ADDR1 Register (Offset = 0040087Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1112](#) and described in [Table 9-2628](#).

Return to [Summary Table](#).

N/A

Table 9-2627. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 087Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 087Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 087Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 087Ch

Figure 9-1112. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2628. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.724 PCIe_CORE_RP_ADDR0 Register (Offset = 00400880h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1113](#) and described in [Table 9-2630](#).

Return to [Summary Table](#).

N/A

Table 9-2629. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0880h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0880h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0880h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0880h

Figure 9-1113. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2630. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.725 PCIE_CORE_RP_ADDR1 Register (Offset = 00400884h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1114](#) and described in [Table 9-2632](#).

Return to [Summary Table](#).

N/A

Table 9-2631. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0884h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0884h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0884h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0884h

Figure 9-1114. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2632. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.726 PCIe_CORE_RP_ADDR0 Register (Offset = 00400888h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1115](#) and described in [Table 9-2634](#).

Return to [Summary Table](#).

N/A

Table 9-2633. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0888h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0888h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0888h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0888h

Figure 9-1115. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2634. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.727 PCIE_CORE_RP_ADDR1 Register (Offset = 0040088Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1116](#) and described in [Table 9-2636](#).

Return to [Summary Table](#).

N/A

Table 9-2635. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 088Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 088Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 088Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 088Ch

Figure 9-1116. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2636. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.728 PCIe_CORE_RP_ADDR0 Register (Offset = 00400890h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1117](#) and described in [Table 9-2638](#).

Return to [Summary Table](#).

N/A

Table 9-2637. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0890h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0890h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0890h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0890h

Figure 9-1117. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2638. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.729 PCIE_CORE_RP_ADDR1 Register (Offset = 00400894h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1118](#) and described in [Table 9-2640](#).

Return to [Summary Table](#).

N/A

Table 9-2639. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0894h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0894h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0894h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0894h

Figure 9-1118. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2640. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.730 PCIe_CORE_RP_ADDR0 Register (Offset = 00400898h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1119](#) and described in [Table 9-2642](#).

Return to [Summary Table](#).

N/A

Table 9-2641. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0898h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0898h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0898h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0898h

Figure 9-1119. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2642. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.731 PCIE_CORE_RP_ADDR1 Register (Offset = 0040089Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1120](#) and described in [Table 9-2644](#).

Return to [Summary Table](#).

N/A

Table 9-2643. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 089Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 089Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 089Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 089Ch

Figure 9-1120. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2644. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.732 PCIe_CORE_RP_ADDR0 Register (Offset = 004008A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1121](#) and described in [Table 9-2646](#).

Return to [Summary Table](#).

N/A

Table 9-2645. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08A0h

Figure 9-1121. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2646. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.733 PCIE_CORE_RP_ADDR1 Register (Offset = 004008A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1122](#) and described in [Table 9-2648](#).

Return to [Summary Table](#).

N/A

Table 9-2647. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08A4h

Figure 9-1122. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2648. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.734 PCIe_CORE_RP_ADDR0 Register (Offset = 004008A8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1123](#) and described in [Table 9-2650](#).

Return to [Summary Table](#).

N/A

Table 9-2649. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08A8h

Figure 9-1123. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2650. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.735 PCIE_CORE_RP_ADDR1 Register (Offset = 004008ACh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1124](#) and described in [Table 9-2652](#).

Return to [Summary Table](#).

N/A

Table 9-2651. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08ACh

Figure 9-1124. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2652. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.736 PCIE_CORE_RP_ADDR0 Register (Offset = 004008B0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1125](#) and described in [Table 9-2654](#).

Return to [Summary Table](#).

N/A

Table 9-2653. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08B0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08B0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08B0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08B0h

Figure 9-1125. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2654. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.737 PCIE_CORE_RP_ADDR1 Register (Offset = 004008B4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1126](#) and described in [Table 9-2656](#).

Return to [Summary Table](#).

N/A

Table 9-2655. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08B4h

Figure 9-1126. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2656. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.738 PCIe_CORE_RP_ADDR0 Register (Offset = 004008B8h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1127](#) and described in [Table 9-2658](#).

Return to [Summary Table](#).

N/A

Table 9-2657. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08B8h

Figure 9-1127. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2658. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.739 PCIE_CORE_RP_ADDR1 Register (Offset = 004008BCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1128](#) and described in [Table 9-2660](#).

Return to [Summary Table](#).

N/A

Table 9-2659. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08BCh

Figure 9-1128. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2660. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.740 PCIe_CORE_RP_ADDR0 Register (Offset = 004008C0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1129](#) and described in [Table 9-2662](#).

Return to [Summary Table](#).

N/A

Table 9-2661. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08C0h

Figure 9-1129. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2662. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.741 PCIE_CORE_RP_ADDR1 Register (Offset = 004008C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1130](#) and described in [Table 9-2664](#).

Return to [Summary Table](#).

N/A

Table 9-2663. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08C4h

Figure 9-1130. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2664. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.742 PCIe_CORE_RP_ADDR0 Register (Offset = 004008C8h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1131](#) and described in [Table 9-2666](#).

Return to [Summary Table](#).

N/A

Table 9-2665. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08C8h

Figure 9-1131. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2666. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.743 PCIE_CORE_RP_ADDR1 Register (Offset = 004008CCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1132](#) and described in [Table 9-2668](#).

Return to [Summary Table](#).

N/A

Table 9-2667. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08CCh

Figure 9-1132. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2668. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.744 PCIE_CORE_RP_ADDR0 Register (Offset = 004008D0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1133](#) and described in [Table 9-2670](#).

Return to [Summary Table](#).

N/A

Table 9-2669. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08D0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08D0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08D0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08D0h

Figure 9-1133. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2670. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.745 PCIE_CORE_RP_ADDR1 Register (Offset = 004008D4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1134](#) and described in [Table 9-2672](#).

Return to [Summary Table](#).

N/A

Table 9-2671. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08D4h

Figure 9-1134. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2672. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.746 PCIe_CORE_RP_ADDR0 Register (Offset = 004008D8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1135](#) and described in [Table 9-2674](#).

Return to [Summary Table](#).

N/A

Table 9-2673. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08D8h

Figure 9-1135. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2674. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.747 PCIE_CORE_RP_ADDR1 Register (Offset = 004008DCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1136](#) and described in [Table 9-2676](#).

Return to [Summary Table](#).

N/A

Table 9-2675. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08DCh

Figure 9-1136. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2676. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.748 PCIe_CORE_RP_ADDR0 Register (Offset = 004008E0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1137](#) and described in [Table 9-2678](#).

Return to [Summary Table](#).

N/A

Table 9-2677. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08E0h

Figure 9-1137. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2678. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.749 PCIE_CORE_RP_ADDR1 Register (Offset = 004008E4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1138](#) and described in [Table 9-2680](#).

Return to [Summary Table](#).

N/A

Table 9-2679. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08E4h

Figure 9-1138. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2680. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.750 PCIe_CORE_RP_ADDR0 Register (Offset = 004008E8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1139](#) and described in [Table 9-2682](#).

Return to [Summary Table](#).

N/A

Table 9-2681. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08E8h

Figure 9-1139. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2682. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.751 PCIE_CORE_RP_ADDR1 Register (Offset = 004008ECh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1140](#) and described in [Table 9-2684](#).

Return to [Summary Table](#).

N/A

Table 9-2683. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08ECh

Figure 9-1140. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2684. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.752 PCIe_CORE_RP_ADDR0 Register (Offset = 004008F0h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1141](#) and described in [Table 9-2686](#).

Return to [Summary Table](#).

N/A

Table 9-2685. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08F0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08F0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08F0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08F0h

Figure 9-1141. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2686. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.753 PCIE_CORE_RP_ADDR1 Register (Offset = 004008F4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1142](#) and described in [Table 9-2688](#).

Return to [Summary Table](#).

N/A

Table 9-2687. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08F4h

Figure 9-1142. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2688. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.754 PCIe_CORE_RP_ADDR0 Register (Offset = 004008F8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1143](#) and described in [Table 9-2690](#).

Return to [Summary Table](#).

N/A

Table 9-2689. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08F8h

Figure 9-1143. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2690. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.755 PCIE_CORE_RP_ADDR1 Register (Offset = 004008FCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1144](#) and described in [Table 9-2692](#).

Return to [Summary Table](#).

N/A

Table 9-2691. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 08FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 08FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 08FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 08FCh

Figure 9-1144. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2692. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.756 PCIe_CORE_RP_ADDR0 Register (Offset = 00400900h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1145](#) and described in [Table 9-2694](#).

Return to [Summary Table](#).

N/A

Table 9-2693. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0900h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0900h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0900h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0900h

Figure 9-1145. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2694. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.757 PCIE_CORE_RP_ADDR1 Register (Offset = 00400904h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1146](#) and described in [Table 9-2696](#).

Return to [Summary Table](#).

N/A

Table 9-2695. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0904h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0904h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0904h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0904h

Figure 9-1146. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2696. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.758 PCIe_CORE_RP_ADDR0 Register (Offset = 00400908h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1147](#) and described in [Table 9-2698](#).

Return to [Summary Table](#).

N/A

Table 9-2697. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0908h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0908h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0908h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0908h

Figure 9-1147. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2698. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.759 PCIE_CORE_RP_ADDR1 Register (Offset = 0040090Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1148](#) and described in [Table 9-2700](#).

Return to [Summary Table](#).

N/A

Table 9-2699. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 090Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 090Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 090Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 090Ch

Figure 9-1148. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2700. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.760 PCIe_CORE_RP_ADDR0 Register (Offset = 00400910h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1149](#) and described in [Table 9-2702](#).

Return to [Summary Table](#).

N/A

Table 9-2701. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0910h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0910h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0910h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0910h

Figure 9-1149. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2702. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.761 PCIE_CORE_RP_ADDR1 Register (Offset = 00400914h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1150](#) and described in [Table 9-2704](#).

Return to [Summary Table](#).

N/A

Table 9-2703. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0914h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0914h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0914h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0914h

Figure 9-1150. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2704. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.762 PCIe_CORE_RP_ADDR0 Register (Offset = 00400918h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1151](#) and described in [Table 9-2706](#).

Return to [Summary Table](#).

N/A

Table 9-2705. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0918h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0918h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0918h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0918h

Figure 9-1151. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2706. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.763 PCIE_CORE_RP_ADDR1 Register (Offset = 0040091Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1152](#) and described in [Table 9-2708](#).

Return to [Summary Table](#).

N/A

Table 9-2707. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 091Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 091Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 091Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 091Ch

Figure 9-1152. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2708. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.764 PCIE_CORE_RP_ADDR0 Register (Offset = 00400920h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1153](#) and described in [Table 9-2710](#).

Return to [Summary Table](#).

N/A

Table 9-2709. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0920h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0920h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0920h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0920h

Figure 9-1153. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2710. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.765 PCIE_CORE_RP_ADDR1 Register (Offset = 00400924h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1154](#) and described in [Table 9-2712](#).

Return to [Summary Table](#).

N/A

Table 9-2711. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0924h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0924h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0924h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0924h

Figure 9-1154. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2712. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.766 PCIe_CORE_RP_ADDR0 Register (Offset = 00400928h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1155](#) and described in [Table 9-2714](#).

Return to [Summary Table](#).

N/A

Table 9-2713. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0928h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0928h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0928h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0928h

Figure 9-1155. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2714. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.767 PCIE_CORE_RP_ADDR1 Register (Offset = 0040092Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1156](#) and described in [Table 9-2716](#).

Return to [Summary Table](#).

N/A

Table 9-2715. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 092Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 092Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 092Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 092Ch

Figure 9-1156. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2716. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.768 PCIe_CORE_RP_ADDR0 Register (Offset = 00400930h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1157](#) and described in [Table 9-2718](#).

Return to [Summary Table](#).

N/A

Table 9-2717. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0930h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0930h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0930h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0930h

Figure 9-1157. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2718. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.769 PCIE_CORE_RP_ADDR1 Register (Offset = 00400934h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1158](#) and described in [Table 9-2720](#).

Return to [Summary Table](#).

N/A

Table 9-2719. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0934h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0934h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0934h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0934h

Figure 9-1158. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2720. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.770 PCIe_CORE_RP_ADDR0 Register (Offset = 00400938h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1159](#) and described in [Table 9-2722](#).

Return to [Summary Table](#).

N/A

Table 9-2721. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0938h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0938h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0938h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0938h

Figure 9-1159. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2722. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.771 PCIE_CORE_RP_ADDR1 Register (Offset = 0040093Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1160](#) and described in [Table 9-2724](#).

Return to [Summary Table](#).

N/A

Table 9-2723. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 093Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 093Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 093Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 093Ch

Figure 9-1160. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2724. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.772 PCIE_CORE_RP_ADDR0 Register (Offset = 00400940h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1161](#) and described in [Table 9-2726](#).

Return to [Summary Table](#).

N/A

Table 9-2725. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0940h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0940h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0940h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0940h

Figure 9-1161. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2726. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.773 PCIE_CORE_RP_ADDR1 Register (Offset = 00400944h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1162](#) and described in [Table 9-2728](#).

Return to [Summary Table](#).

N/A

Table 9-2727. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0944h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0944h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0944h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0944h

Figure 9-1162. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2728. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.774 PCIe_CORE_RP_ADDR0 Register (Offset = 00400948h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1163](#) and described in [Table 9-2730](#).

Return to [Summary Table](#).

N/A

Table 9-2729. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0948h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0948h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0948h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0948h

Figure 9-1163. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2730. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.775 PCIE_CORE_RP_ADDR1 Register (Offset = 0040094Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1164](#) and described in [Table 9-2732](#).

Return to [Summary Table](#).

N/A

Table 9-2731. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 094Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 094Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 094Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 094Ch

Figure 9-1164. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2732. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.776 PCIe_CORE_RP_ADDR0 Register (Offset = 00400950h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1165](#) and described in [Table 9-2734](#).

Return to [Summary Table](#).

N/A

Table 9-2733. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0950h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0950h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0950h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0950h

Figure 9-1165. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2734. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.777 PCIE_CORE_RP_ADDR1 Register (Offset = 00400954h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1166](#) and described in [Table 9-2736](#).

Return to [Summary Table](#).

N/A

Table 9-2735. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0954h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0954h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0954h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0954h

Figure 9-1166. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2736. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.778 PCIe_CORE_RP_ADDR0 Register (Offset = 00400958h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1167](#) and described in [Table 9-2738](#).

Return to [Summary Table](#).

N/A

Table 9-2737. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0958h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0958h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0958h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0958h

Figure 9-1167. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2738. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.779 PCIE_CORE_RP_ADDR1 Register (Offset = 0040095Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1168](#) and described in [Table 9-2740](#).

Return to [Summary Table](#).

N/A

Table 9-2739. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 095Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 095Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 095Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 095Ch

Figure 9-1168. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2740. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.780 PCIe_CORE_RP_ADDR0 Register (Offset = 00400960h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1169](#) and described in [Table 9-2742](#).

Return to [Summary Table](#).

N/A

Table 9-2741. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0960h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0960h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0960h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0960h

Figure 9-1169. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2742. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.781 PCIE_CORE_RP_ADDR1 Register (Offset = 00400964h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1170](#) and described in [Table 9-2744](#).

Return to [Summary Table](#).

N/A

Table 9-2743. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0964h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0964h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0964h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0964h

Figure 9-1170. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2744. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.782 PCIe_CORE_RP_ADDR0 Register (Offset = 00400968h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1171](#) and described in [Table 9-2746](#).

Return to [Summary Table](#).

N/A

Table 9-2745. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0968h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0968h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0968h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0968h

Figure 9-1171. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2746. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.783 PCIE_CORE_RP_ADDR1 Register (Offset = 0040096Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1172](#) and described in [Table 9-2748](#).

Return to [Summary Table](#).

N/A

Table 9-2747. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 096Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 096Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 096Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 096Ch

Figure 9-1172. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2748. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.784 PCIE_CORE_RP_ADDR0 Register (Offset = 00400970h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1173](#) and described in [Table 9-2750](#).

Return to [Summary Table](#).

N/A

Table 9-2749. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0970h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0970h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0970h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0970h

Figure 9-1173. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2750. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.785 PCIE_CORE_RP_ADDR1 Register (Offset = 00400974h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1174](#) and described in [Table 9-2752](#).

Return to [Summary Table](#).

N/A

Table 9-2751. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0974h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0974h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0974h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0974h

Figure 9-1174. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2752. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.786 PCIe_CORE_RP_ADDR0 Register (Offset = 00400978h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1175](#) and described in [Table 9-2754](#).

Return to [Summary Table](#).

N/A

Table 9-2753. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0978h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0978h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0978h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0978h

Figure 9-1175. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2754. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.787 PCIE_CORE_RP_ADDR1 Register (Offset = 0040097Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1176](#) and described in [Table 9-2756](#).

Return to [Summary Table](#).

N/A

Table 9-2755. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 097Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 097Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 097Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 097Ch

Figure 9-1176. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2756. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.788 PCIE_CORE_RP_ADDR0 Register (Offset = 00400980h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1177](#) and described in [Table 9-2758](#).

Return to [Summary Table](#).

N/A

Table 9-2757. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0980h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0980h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0980h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0980h

Figure 9-1177. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2758. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.789 PCIE_CORE_RP_ADDR1 Register (Offset = 00400984h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1178](#) and described in [Table 9-2760](#).

Return to [Summary Table](#).

N/A

Table 9-2759. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0984h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0984h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0984h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0984h

Figure 9-1178. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2760. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.790 PCIe_CORE_RP_ADDR0 Register (Offset = 00400988h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1179](#) and described in [Table 9-2762](#).

Return to [Summary Table](#).

N/A

Table 9-2761. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0988h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0988h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0988h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0988h

Figure 9-1179. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2762. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.791 PCIE_CORE_RP_ADDR1 Register (Offset = 0040098Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1180](#) and described in [Table 9-2764](#).

Return to [Summary Table](#).

N/A

Table 9-2763. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 098Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 098Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 098Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 098Ch

Figure 9-1180. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2764. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.792 PCIe_CORE_RP_ADDR0 Register (Offset = 00400990h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1181](#) and described in [Table 9-2766](#).

Return to [Summary Table](#).

N/A

Table 9-2765. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0990h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0990h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0990h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0990h

Figure 9-1181. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2766. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.793 PCIE_CORE_RP_ADDR1 Register (Offset = 00400994h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1182](#) and described in [Table 9-2768](#).

Return to [Summary Table](#).

N/A

Table 9-2767. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0994h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0994h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0994h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0994h

Figure 9-1182. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2768. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.794 PCIe_CORE_RP_ADDR0 Register (Offset = 00400998h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1183](#) and described in [Table 9-2770](#).

Return to [Summary Table](#).

N/A

Table 9-2769. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0998h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0998h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0998h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0998h

Figure 9-1183. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2770. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.795 PCIE_CORE_RP_ADDR1 Register (Offset = 0040099Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1184](#) and described in [Table 9-2772](#).

Return to [Summary Table](#).

N/A

Table 9-2771. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 099Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 099Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 099Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 099Ch

Figure 9-1184. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2772. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.796 PCIe_CORE_RP_ADDR0 Register (Offset = 004009A0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1185](#) and described in [Table 9-2774](#).

Return to [Summary Table](#).

N/A

Table 9-2773. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09A0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09A0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09A0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09A0h

Figure 9-1185. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2774. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.797 PCIE_CORE_RP_ADDR1 Register (Offset = 004009A4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1186](#) and described in [Table 9-2776](#).

Return to [Summary Table](#).

N/A

Table 9-2775. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09A4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09A4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09A4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09A4h

Figure 9-1186. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2776. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.798 PCIe_CORE_RP_ADDR0 Register (Offset = 004009A8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1187](#) and described in [Table 9-2778](#).

Return to [Summary Table](#).

N/A

Table 9-2777. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09A8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09A8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09A8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09A8h

Figure 9-1187. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2778. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.799 PCIE_CORE_RP_ADDR1 Register (Offset = 004009ACh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1188](#) and described in [Table 9-2780](#).

Return to [Summary Table](#).

N/A

Table 9-2779. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09ACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09ACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09ACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09ACh

Figure 9-1188. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2780. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.800 PCIE_CORE_RP_ADDR0 Register (Offset = 004009B0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1189](#) and described in [Table 9-2782](#).

Return to [Summary Table](#).

N/A

Table 9-2781. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09B0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09B0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09B0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09B0h

Figure 9-1189. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2782. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.801 PCIE_CORE_RP_ADDR1 Register (Offset = 004009B4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1190](#) and described in [Table 9-2784](#).

Return to [Summary Table](#).

N/A

Table 9-2783. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09B4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09B4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09B4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09B4h

Figure 9-1190. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2784. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.802 PCIE_CORE_RP_ADDR0 Register (Offset = 004009B8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1191](#) and described in [Table 9-2786](#).

Return to [Summary Table](#).

N/A

Table 9-2785. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09B8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09B8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09B8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09B8h

Figure 9-1191. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2786. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.803 PCIE_CORE_RP_ADDR1 Register (Offset = 004009BCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1192](#) and described in [Table 9-2788](#).

Return to [Summary Table](#).

N/A

Table 9-2787. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09BCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09BCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09BCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09BCh

Figure 9-1192. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2788. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.804 PCIE_CORE_RP_ADDR0 Register (Offset = 004009C0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1193](#) and described in [Table 9-2790](#).

Return to [Summary Table](#).

N/A

Table 9-2789. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09C0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09C0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09C0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09C0h

Figure 9-1193. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2790. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.805 PCIE_CORE_RP_ADDR1 Register (Offset = 004009C4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1194](#) and described in [Table 9-2792](#).

Return to [Summary Table](#).

N/A

Table 9-2791. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09C4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09C4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09C4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09C4h

Figure 9-1194. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2792. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.806 PCIe_CORE_RP_ADDR0 Register (Offset = 004009C8h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1195](#) and described in [Table 9-2794](#).

Return to [Summary Table](#).

N/A

Table 9-2793. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09C8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09C8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09C8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09C8h

Figure 9-1195. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2794. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.807 PCIE_CORE_RP_ADDR1 Register (Offset = 004009CCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1196](#) and described in [Table 9-2796](#).

Return to [Summary Table](#).

N/A

Table 9-2795. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09CCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09CCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09CCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09CCh

Figure 9-1196. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2796. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.808 PCIE_CORE_RP_ADDR0 Register (Offset = 004009D0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1197](#) and described in [Table 9-2798](#).

Return to [Summary Table](#).

N/A

Table 9-2797. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09D0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09D0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09D0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09D0h

Figure 9-1197. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2798. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.809 PCIE_CORE_RP_ADDR1 Register (Offset = 004009D4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1198](#) and described in [Table 9-2800](#).

Return to [Summary Table](#).

N/A

Table 9-2799. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09D4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09D4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09D4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09D4h

Figure 9-1198. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2800. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.810 PCIe_CORE_RP_ADDR0 Register (Offset = 004009D8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1199](#) and described in [Table 9-2802](#).

Return to [Summary Table](#).

N/A

Table 9-2801. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09D8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09D8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09D8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09D8h

Figure 9-1199. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2802. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.811 PCIE_CORE_RP_ADDR1 Register (Offset = 004009DCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1200](#) and described in [Table 9-2804](#).

Return to [Summary Table](#).

N/A

Table 9-2803. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09DCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09DCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09DCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09DCh

Figure 9-1200. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2804. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.812 PCIe_CORE_RP_ADDR0 Register (Offset = 004009E0h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1201](#) and described in [Table 9-2806](#).

Return to [Summary Table](#).

N/A

Table 9-2805. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09E0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09E0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09E0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09E0h

Figure 9-1201. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2806. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.813 PCIE_CORE_RP_ADDR1 Register (Offset = 004009E4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1202](#) and described in [Table 9-2808](#).

Return to [Summary Table](#).

N/A

Table 9-2807. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09E4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09E4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09E4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09E4h

Figure 9-1202. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2808. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.814 PCIe_CORE_RP_ADDR0 Register (Offset = 004009E8h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1203](#) and described in [Table 9-2810](#).

Return to [Summary Table](#).

N/A

Table 9-2809. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09E8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09E8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09E8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09E8h

Figure 9-1203. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2810. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.815 PCIE_CORE_RP_ADDR1 Register (Offset = 004009ECh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1204](#) and described in [Table 9-2812](#).

Return to [Summary Table](#).

N/A

Table 9-2811. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09ECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09ECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09ECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09ECh

Figure 9-1204. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2812. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.816 PCIe_CORE_RP_ADDR0 Register (Offset = 004009F0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1205](#) and described in [Table 9-2814](#).

Return to [Summary Table](#).

N/A

Table 9-2813. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09F0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09F0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09F0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09F0h

Figure 9-1205. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2814. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.817 PCIE_CORE_RP_ADDR1 Register (Offset = 004009F4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1206](#) and described in [Table 9-2816](#).

Return to [Summary Table](#).

N/A

Table 9-2815. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09F4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09F4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09F4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09F4h

Figure 9-1206. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2816. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.818 PCIe_CORE_RP_ADDR0 Register (Offset = 004009F8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1207](#) and described in [Table 9-2818](#).

Return to [Summary Table](#).

N/A

Table 9-2817. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09F8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09F8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09F8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09F8h

Figure 9-1207. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2818. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.819 PCIE_CORE_RP_ADDR1 Register (Offset = 004009FCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1208](#) and described in [Table 9-2820](#).

Return to [Summary Table](#).

N/A

Table 9-2819. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 09FCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 09FCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 09FCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 09FCh

Figure 9-1208. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2820. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.820 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A00h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1209](#) and described in [Table 9-2822](#).

Return to [Summary Table](#).

N/A

Table 9-2821. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A00h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A00h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A00h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A00h

Figure 9-1209. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2822. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.821 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A04h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1210](#) and described in [Table 9-2824](#).

Return to [Summary Table](#).

N/A

Table 9-2823. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A04h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A04h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A04h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A04h

Figure 9-1210. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2824. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.822 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A08h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1211](#) and described in [Table 9-2826](#).

Return to [Summary Table](#).

N/A

Table 9-2825. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A08h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A08h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A08h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A08h

Figure 9-1211. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2826. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.823 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A0Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1212](#) and described in [Table 9-2828](#).

Return to [Summary Table](#).

N/A

Table 9-2827. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A0Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A0Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A0Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A0Ch

Figure 9-1212. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2828. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.824 PCIE_CORE_RP_ADDR0 Register (Offset = 00400A10h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1213](#) and described in [Table 9-2830](#).

Return to [Summary Table](#).

N/A

Table 9-2829. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A10h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A10h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A10h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A10h

Figure 9-1213. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2830. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.825 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A14h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1214](#) and described in [Table 9-2832](#).

Return to [Summary Table](#).

N/A

Table 9-2831. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A14h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A14h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A14h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A14h

Figure 9-1214. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2832. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.826 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A18h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1215](#) and described in [Table 9-2834](#).

Return to [Summary Table](#).

N/A

Table 9-2833. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A18h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A18h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A18h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A18h

Figure 9-1215. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2834. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.827 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A1Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1216](#) and described in [Table 9-2836](#).

Return to [Summary Table](#).

N/A

Table 9-2835. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A1Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A1Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A1Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A1Ch

Figure 9-1216. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2836. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.828 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A20h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1217](#) and described in [Table 9-2838](#).

Return to [Summary Table](#).

N/A

Table 9-2837. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A20h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A20h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A20h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A20h

Figure 9-1217. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2838. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.829 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A24h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1218](#) and described in [Table 9-2840](#).

Return to [Summary Table](#).

N/A

Table 9-2839. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A24h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A24h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A24h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A24h

Figure 9-1218. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2840. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.830 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A28h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1219](#) and described in [Table 9-2842](#).

Return to [Summary Table](#).

N/A

Table 9-2841. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A28h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A28h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A28h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A28h

Figure 9-1219. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2842. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.831 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A2Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1220](#) and described in [Table 9-2844](#).

Return to [Summary Table](#).

N/A

Table 9-2843. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A2Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A2Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A2Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A2Ch

Figure 9-1220. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2844. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.832 PCIE_CORE_RP_ADDR0 Register (Offset = 00400A30h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1221](#) and described in [Table 9-2846](#).

Return to [Summary Table](#).

N/A

Table 9-2845. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A30h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A30h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A30h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A30h

Figure 9-1221. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2846. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.833 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A34h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1222](#) and described in [Table 9-2848](#).

Return to [Summary Table](#).

N/A

Table 9-2847. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A34h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A34h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A34h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A34h

Figure 9-1222. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2848. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.834 PCIE_CORE_RP_ADDR0 Register (Offset = 00400A38h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1223](#) and described in [Table 9-2850](#).

Return to [Summary Table](#).

N/A

Table 9-2849. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A38h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A38h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A38h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A38h

Figure 9-1223. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2850. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.835 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A3Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1224](#) and described in [Table 9-2852](#).

Return to [Summary Table](#).

N/A

Table 9-2851. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A3Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A3Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A3Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A3Ch

Figure 9-1224. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2852. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.836 PCIE_CORE_RP_ADDR0 Register (Offset = 00400A40h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1225](#) and described in [Table 9-2854](#).

Return to [Summary Table](#).

N/A

Table 9-2853. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A40h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A40h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A40h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A40h

Figure 9-1225. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2854. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.837 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A44h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1226](#) and described in [Table 9-2856](#).

Return to [Summary Table](#).

N/A

Table 9-2855. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A44h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A44h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A44h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A44h

Figure 9-1226. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2856. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.838 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A48h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1227](#) and described in [Table 9-2858](#).

Return to [Summary Table](#).

N/A

Table 9-2857. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A48h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A48h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A48h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A48h

Figure 9-1227. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2858. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.839 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A4Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1228](#) and described in [Table 9-2860](#).

Return to [Summary Table](#).

N/A

Table 9-2859. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A4Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A4Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A4Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A4Ch

Figure 9-1228. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2860. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.840 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A50h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1229](#) and described in [Table 9-2862](#).

Return to [Summary Table](#).

N/A

Table 9-2861. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A50h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A50h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A50h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A50h

Figure 9-1229. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2862. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.841 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A54h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1230](#) and described in [Table 9-2864](#).

Return to [Summary Table](#).

N/A

Table 9-2863. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A54h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A54h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A54h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A54h

Figure 9-1230. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2864. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.842 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A58h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1231](#) and described in [Table 9-2866](#).

Return to [Summary Table](#).

N/A

Table 9-2865. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A58h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A58h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A58h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A58h

Figure 9-1231. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2866. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.843 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A5Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1232](#) and described in [Table 9-2868](#).

Return to [Summary Table](#).

N/A

Table 9-2867. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A5Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A5Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A5Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A5Ch

Figure 9-1232. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2868. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.844 PCIE_CORE_RP_ADDR0 Register (Offset = 00400A60h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1233](#) and described in [Table 9-2870](#).

Return to [Summary Table](#).

N/A

Table 9-2869. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A60h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A60h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A60h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A60h

Figure 9-1233. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2870. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.845 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A64h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1234](#) and described in [Table 9-2872](#).

Return to [Summary Table](#).

N/A

Table 9-2871. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A64h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A64h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A64h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A64h

Figure 9-1234. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2872. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.846 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A68h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1235](#) and described in [Table 9-2874](#).

Return to [Summary Table](#).

N/A

Table 9-2873. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A68h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A68h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A68h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A68h

Figure 9-1235. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2874. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.847 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A6Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1236](#) and described in [Table 9-2876](#).

Return to [Summary Table](#).

N/A

Table 9-2875. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A6Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A6Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A6Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A6Ch

Figure 9-1236. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2876. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.848 PCIE_CORE_RP_ADDR0 Register (Offset = 00400A70h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1237](#) and described in [Table 9-2878](#).

Return to [Summary Table](#).

N/A

Table 9-2877. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A70h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A70h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A70h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A70h

Figure 9-1237. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2878. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.849 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A74h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1238](#) and described in [Table 9-2880](#).

Return to [Summary Table](#).

N/A

Table 9-2879. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A74h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A74h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A74h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A74h

Figure 9-1238. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2880. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.850 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A78h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1239](#) and described in [Table 9-2882](#).

Return to [Summary Table](#).

N/A

Table 9-2881. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A78h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A78h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A78h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A78h

Figure 9-1239. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2882. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.851 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A7Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1240](#) and described in [Table 9-2884](#).

Return to [Summary Table](#).

N/A

Table 9-2883. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A7Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A7Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A7Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A7Ch

Figure 9-1240. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2884. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.852 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A80h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1241](#) and described in [Table 9-2886](#).

Return to [Summary Table](#).

N/A

Table 9-2885. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A80h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A80h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A80h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A80h

Figure 9-1241. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2886. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.853 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A84h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1242](#) and described in [Table 9-2888](#).

Return to [Summary Table](#).

N/A

Table 9-2887. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A84h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A84h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A84h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A84h

Figure 9-1242. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2888. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.854 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A88h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1243](#) and described in [Table 9-2890](#).

Return to [Summary Table](#).

N/A

Table 9-2889. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A88h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A88h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A88h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A88h

Figure 9-1243. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2890. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.855 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A8Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1244](#) and described in [Table 9-2892](#).

Return to [Summary Table](#).

N/A

Table 9-2891. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A8Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A8Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A8Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A8Ch

Figure 9-1244. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2892. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.856 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A90h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1245](#) and described in [Table 9-2894](#).

Return to [Summary Table](#).

N/A

Table 9-2893. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A90h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A90h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A90h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A90h

Figure 9-1245. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2894. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.857 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A94h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1246](#) and described in [Table 9-2896](#).

Return to [Summary Table](#).

N/A

Table 9-2895. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A94h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A94h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A94h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A94h

Figure 9-1246. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2896. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.858 PCIe_CORE_RP_ADDR0 Register (Offset = 00400A98h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1247](#) and described in [Table 9-2898](#).

Return to [Summary Table](#).

N/A

Table 9-2897. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A98h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A98h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A98h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A98h

Figure 9-1247. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2898. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.859 PCIE_CORE_RP_ADDR1 Register (Offset = 00400A9Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1248](#) and described in [Table 9-2900](#).

Return to [Summary Table](#).

N/A

Table 9-2899. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0A9Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0A9Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0A9Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0A9Ch

Figure 9-1248. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2900. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.860 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AA0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1249](#) and described in [Table 9-2902](#).

Return to [Summary Table](#).

N/A

Table 9-2901. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AA0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AA0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AA0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AA0h

Figure 9-1249. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2902. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.861 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AA4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1250](#) and described in [Table 9-2904](#).

Return to [Summary Table](#).

N/A

Table 9-2903. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AA4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AA4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AA4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AA4h

Figure 9-1250. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2904. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.862 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AA8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1251](#) and described in [Table 9-2906](#).

Return to [Summary Table](#).

N/A

Table 9-2905. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AA8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AA8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AA8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AA8h

Figure 9-1251. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2906. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.863 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AACh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1252](#) and described in [Table 9-2908](#).

Return to [Summary Table](#).

N/A

Table 9-2907. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AACh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AACh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AACh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AACh

Figure 9-1252. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2908. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.864 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AB0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1253](#) and described in [Table 9-2910](#).

Return to [Summary Table](#).

N/A

Table 9-2909. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AB0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AB0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AB0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AB0h

Figure 9-1253. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2910. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.865 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AB4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1254](#) and described in [Table 9-2912](#).

Return to [Summary Table](#).

N/A

Table 9-2911. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AB4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AB4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AB4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AB4h

Figure 9-1254. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2912. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.866 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AB8h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1255](#) and described in [Table 9-2914](#).

Return to [Summary Table](#).

N/A

Table 9-2913. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AB8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AB8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AB8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AB8h

Figure 9-1255. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2914. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.867 PCIE_CORE_RP_ADDR1 Register (Offset = 00400ABCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1256](#) and described in [Table 9-2916](#).

Return to [Summary Table](#).

N/A

Table 9-2915. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0ABCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0ABCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0ABCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0ABCh

Figure 9-1256. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2916. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.868 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AC0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1257](#) and described in [Table 9-2918](#).

Return to [Summary Table](#).

N/A

Table 9-2917. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AC0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AC0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AC0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AC0h

Figure 9-1257. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2918. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.869 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AC4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1258](#) and described in [Table 9-2920](#).

Return to [Summary Table](#).

N/A

Table 9-2919. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AC4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AC4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AC4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AC4h

Figure 9-1258. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2920. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.870 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AC8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1259](#) and described in [Table 9-2922](#).

Return to [Summary Table](#).

N/A

Table 9-2921. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AC8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AC8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AC8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AC8h

Figure 9-1259. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2922. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.871 PCIE_CORE_RP_ADDR1 Register (Offset = 00400ACCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1260](#) and described in [Table 9-2924](#).

Return to [Summary Table](#).

N/A

Table 9-2923. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0ACCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0ACCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0ACCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0ACCh

Figure 9-1260. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2924. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.872 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AD0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1261](#) and described in [Table 9-2926](#).

Return to [Summary Table](#).

N/A

Table 9-2925. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AD0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AD0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AD0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AD0h

Figure 9-1261. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2926. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.873 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AD4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1262](#) and described in [Table 9-2928](#).

Return to [Summary Table](#).

N/A

Table 9-2927. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AD4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AD4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AD4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AD4h

Figure 9-1262. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2928. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.874 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AD8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1263](#) and described in [Table 9-2930](#).

Return to [Summary Table](#).

N/A

Table 9-2929. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AD8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AD8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AD8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AD8h

Figure 9-1263. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2930. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.875 PCIE_CORE_RP_ADDR1 Register (Offset = 00400ADCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1264](#) and described in [Table 9-2932](#).

Return to [Summary Table](#).

N/A

Table 9-2931. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0ADCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0ADCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0ADCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0ADCh

Figure 9-1264. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2932. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.876 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AE0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1265](#) and described in [Table 9-2934](#).

Return to [Summary Table](#).

N/A

Table 9-2933. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AE0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AE0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AE0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AE0h

Figure 9-1265. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2934. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.877 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AE4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1266](#) and described in [Table 9-2936](#).

Return to [Summary Table](#).

N/A

Table 9-2935. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AE4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AE4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AE4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AE4h

Figure 9-1266. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2936. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.878 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AE8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1267](#) and described in [Table 9-2938](#).

Return to [Summary Table](#).

N/A

Table 9-2937. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AE8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AE8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AE8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AE8h

Figure 9-1267. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2938. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.879 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AECh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1268](#) and described in [Table 9-2940](#).

Return to [Summary Table](#).

N/A

Table 9-2939. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AECh

Figure 9-1268. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2940. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.880 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AF0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1269](#) and described in [Table 9-2942](#).

Return to [Summary Table](#).

N/A

Table 9-2941. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AF0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AF0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AF0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AF0h

Figure 9-1269. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2942. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.881 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AF4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1270](#) and described in [Table 9-2944](#).

Return to [Summary Table](#).

N/A

Table 9-2943. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AF4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AF4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AF4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AF4h

Figure 9-1270. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2944. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.882 PCIe_CORE_RP_ADDR0 Register (Offset = 00400AF8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1271](#) and described in [Table 9-2946](#).

Return to [Summary Table](#).

N/A

Table 9-2945. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AF8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AF8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AF8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AF8h

Figure 9-1271. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2946. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.883 PCIE_CORE_RP_ADDR1 Register (Offset = 00400AFCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1272](#) and described in [Table 9-2948](#).

Return to [Summary Table](#).

N/A

Table 9-2947. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0AFCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0AFCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0AFCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0AFCh

Figure 9-1272. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2948. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.884 PCIE_CORE_RP_ADDR0 Register (Offset = 00400B00h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1273](#) and described in [Table 9-2950](#).

Return to [Summary Table](#).

N/A

Table 9-2949. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B00h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B00h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B00h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B00h

Figure 9-1273. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2950. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.885 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B04h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1274](#) and described in [Table 9-2952](#).

Return to [Summary Table](#).

N/A

Table 9-2951. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B04h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B04h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B04h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B04h

Figure 9-1274. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2952. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.886 PCIE_CORE_RP_ADDR0 Register (Offset = 00400B08h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1275](#) and described in [Table 9-2954](#).

Return to [Summary Table](#).

N/A

Table 9-2953. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B08h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B08h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B08h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B08h

Figure 9-1275. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2954. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.887 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B0Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1276](#) and described in [Table 9-2956](#).

Return to [Summary Table](#).

N/A

Table 9-2955. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B0Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B0Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B0Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B0Ch

Figure 9-1276. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2956. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.888 PCIE_CORE_RP_ADDR0 Register (Offset = 00400B10h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1277](#) and described in [Table 9-2958](#).

Return to [Summary Table](#).

N/A

Table 9-2957. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B10h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B10h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B10h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B10h

Figure 9-1277. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2958. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.889 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B14h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1278](#) and described in [Table 9-2960](#).

Return to [Summary Table](#).

N/A

Table 9-2959. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B14h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B14h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B14h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B14h

Figure 9-1278. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2960. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.890 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B18h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1279](#) and described in [Table 9-2962](#).

Return to [Summary Table](#).

N/A

Table 9-2961. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B18h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B18h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B18h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B18h

Figure 9-1279. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2962. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.891 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B1Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1280](#) and described in [Table 9-2964](#).

Return to [Summary Table](#).

N/A

Table 9-2963. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B1Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B1Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B1Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B1Ch

Figure 9-1280. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2964. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.892 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B20h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1281](#) and described in [Table 9-2966](#).

Return to [Summary Table](#).

N/A

Table 9-2965. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B20h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B20h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B20h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B20h

Figure 9-1281. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2966. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.893 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B24h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1282](#) and described in [Table 9-2968](#).

Return to [Summary Table](#).

N/A

Table 9-2967. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B24h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B24h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B24h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B24h

Figure 9-1282. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2968. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.894 PCIE_CORE_RP_ADDR0 Register (Offset = 00400B28h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1283](#) and described in [Table 9-2970](#).

Return to [Summary Table](#).

N/A

Table 9-2969. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B28h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B28h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B28h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B28h

Figure 9-1283. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2970. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.895 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B2Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1284](#) and described in [Table 9-2972](#).

Return to [Summary Table](#).

N/A

Table 9-2971. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B2Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B2Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B2Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B2Ch

Figure 9-1284. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2972. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.896 PCIE_CORE_RP_ADDR0 Register (Offset = 00400B30h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1285](#) and described in [Table 9-2974](#).

Return to [Summary Table](#).

N/A

Table 9-2973. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B30h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B30h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B30h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B30h

Figure 9-1285. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2974. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.897 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B34h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1286](#) and described in [Table 9-2976](#).

Return to [Summary Table](#).

N/A

Table 9-2975. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B34h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B34h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B34h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B34h

Figure 9-1286. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2976. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.898 PCIE_CORE_RP_ADDR0 Register (Offset = 00400B38h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1287](#) and described in [Table 9-2978](#).

Return to [Summary Table](#).

N/A

Table 9-2977. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B38h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B38h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B38h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B38h

Figure 9-1287. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2978. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.899 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B3Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1288](#) and described in [Table 9-2980](#).

Return to [Summary Table](#).

N/A

Table 9-2979. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B3Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B3Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B3Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B3Ch

Figure 9-1288. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2980. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.900 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B40h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1289](#) and described in [Table 9-2982](#).

Return to [Summary Table](#).

N/A

Table 9-2981. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B40h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B40h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B40h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B40h

Figure 9-1289. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2982. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.901 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B44h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1290](#) and described in [Table 9-2984](#).

Return to [Summary Table](#).

N/A

Table 9-2983. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B44h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B44h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B44h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B44h

Figure 9-1290. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2984. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.902 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B48h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1291](#) and described in [Table 9-2986](#).

Return to [Summary Table](#).

N/A

Table 9-2985. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B48h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B48h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B48h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B48h

Figure 9-1291. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2986. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.903 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B4Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1292](#) and described in [Table 9-2988](#).

Return to [Summary Table](#).

N/A

Table 9-2987. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B4Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B4Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B4Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B4Ch

Figure 9-1292. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2988. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.904 PCIE_CORE_RP_ADDR0 Register (Offset = 00400B50h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1293](#) and described in [Table 9-2990](#).

Return to [Summary Table](#).

N/A

Table 9-2989. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B50h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B50h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B50h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B50h

Figure 9-1293. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2990. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.905 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B54h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1294](#) and described in [Table 9-2992](#).

Return to [Summary Table](#).

N/A

Table 9-2991. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B54h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B54h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B54h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B54h

Figure 9-1294. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2992. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.906 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B58h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1295](#) and described in [Table 9-2994](#).

Return to [Summary Table](#).

N/A

Table 9-2993. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B58h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B58h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B58h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B58h

Figure 9-1295. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2994. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.907 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B5Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1296](#) and described in [Table 9-2996](#).

Return to [Summary Table](#).

N/A

Table 9-2995. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B5Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B5Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B5Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B5Ch

Figure 9-1296. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2996. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.908 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B60h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1297](#) and described in [Table 9-2998](#).

Return to [Summary Table](#).

N/A

Table 9-2997. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B60h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B60h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B60h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B60h

Figure 9-1297. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-2998. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.909 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B64h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1298](#) and described in [Table 9-3000](#).

Return to [Summary Table](#).

N/A

Table 9-2999. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B64h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B64h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B64h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B64h

Figure 9-1298. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3000. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.910 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B68h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1299](#) and described in [Table 9-3002](#).

Return to [Summary Table](#).

N/A

Table 9-3001. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B68h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B68h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B68h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B68h

Figure 9-1299. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3002. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.911 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B6Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1300](#) and described in [Table 9-3004](#).

Return to [Summary Table](#).

N/A

Table 9-3003. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B6Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B6Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B6Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B6Ch

Figure 9-1300. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3004. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.912 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B70h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1301](#) and described in [Table 9-3006](#).

Return to [Summary Table](#).

N/A

Table 9-3005. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B70h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B70h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B70h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B70h

Figure 9-1301. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3006. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.913 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B74h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1302](#) and described in [Table 9-3008](#).

Return to [Summary Table](#).

N/A

Table 9-3007. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B74h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B74h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B74h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B74h

Figure 9-1302. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3008. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.914 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B78h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1303](#) and described in [Table 9-3010](#).

Return to [Summary Table](#).

N/A

Table 9-3009. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B78h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B78h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B78h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B78h

Figure 9-1303. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3010. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.915 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B7Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1304](#) and described in [Table 9-3012](#).

Return to [Summary Table](#).

N/A

Table 9-3011. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B7Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B7Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B7Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B7Ch

Figure 9-1304. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3012. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.916 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B80h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1305](#) and described in [Table 9-3014](#).

Return to [Summary Table](#).

N/A

Table 9-3013. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B80h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B80h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B80h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B80h

Figure 9-1305. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3014. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.917 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B84h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1306](#) and described in [Table 9-3016](#).

Return to [Summary Table](#).

N/A

Table 9-3015. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B84h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B84h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B84h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B84h

Figure 9-1306. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3016. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.918 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B88h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1307](#) and described in [Table 9-3018](#).

Return to [Summary Table](#).

N/A

Table 9-3017. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B88h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B88h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B88h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B88h

Figure 9-1307. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3018. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.919 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B8Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1308](#) and described in [Table 9-3020](#).

Return to [Summary Table](#).

N/A

Table 9-3019. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B8Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B8Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B8Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B8Ch

Figure 9-1308. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3020. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.920 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B90h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1309](#) and described in [Table 9-3022](#).

Return to [Summary Table](#).

N/A

Table 9-3021. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B90h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B90h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B90h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B90h

Figure 9-1309. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3022. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.921 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B94h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1310](#) and described in [Table 9-3024](#).

Return to [Summary Table](#).

N/A

Table 9-3023. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B94h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B94h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B94h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B94h

Figure 9-1310. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3024. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.922 PCIe_CORE_RP_ADDR0 Register (Offset = 00400B98h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1311](#) and described in [Table 9-3026](#).

Return to [Summary Table](#).

N/A

Table 9-3025. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B98h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B98h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B98h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B98h

Figure 9-1311. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3026. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.923 PCIE_CORE_RP_ADDR1 Register (Offset = 00400B9Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1312](#) and described in [Table 9-3028](#).

Return to [Summary Table](#).

N/A

Table 9-3027. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0B9Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0B9Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0B9Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0B9Ch

Figure 9-1312. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3028. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.924 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BA0h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1313](#) and described in [Table 9-3030](#).

Return to [Summary Table](#).

N/A

Table 9-3029. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BA0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BA0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BA0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BA0h

Figure 9-1313. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3030. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.925 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BA4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1314](#) and described in [Table 9-3032](#).

Return to [Summary Table](#).

N/A

Table 9-3031. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BA4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BA4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BA4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BA4h

Figure 9-1314. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3032. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.926 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BA8h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1315](#) and described in [Table 9-3034](#).

Return to [Summary Table](#).

N/A

Table 9-3033. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BA8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BA8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BA8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BA8h

Figure 9-1315. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3034. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.927 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BACH) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1316](#) and described in [Table 9-3036](#).

Return to [Summary Table](#).

N/A

Table 9-3035. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BACH
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BACH
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BACH
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BACH

Figure 9-1316. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3036. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.928 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BB0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1317](#) and described in [Table 9-3038](#).

Return to [Summary Table](#).

N/A

Table 9-3037. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BB0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BB0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BB0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BB0h

Figure 9-1317. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3038. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.929 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BB4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1318](#) and described in [Table 9-3040](#).

Return to [Summary Table](#).

N/A

Table 9-3039. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BB4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BB4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BB4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BB4h

Figure 9-1318. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3040. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.930 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BB8h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1319](#) and described in [Table 9-3042](#).

Return to [Summary Table](#).

N/A

Table 9-3041. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BB8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BB8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BB8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BB8h

Figure 9-1319. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3042. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.931 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BBCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1320](#) and described in [Table 9-3044](#).

Return to [Summary Table](#).

N/A

Table 9-3043. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BBCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BBCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BBCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BBCh

Figure 9-1320. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3044. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.932 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BC0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1321](#) and described in [Table 9-3046](#).

Return to [Summary Table](#).

N/A

Table 9-3045. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BC0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BC0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BC0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BC0h

Figure 9-1321. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3046. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.933 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BC4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1322](#) and described in [Table 9-3048](#).

Return to [Summary Table](#).

N/A

Table 9-3047. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BC4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BC4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BC4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BC4h

Figure 9-1322. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3048. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.934 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BC8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1323](#) and described in [Table 9-3050](#).

Return to [Summary Table](#).

N/A

Table 9-3049. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BC8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BC8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BC8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BC8h

Figure 9-1323. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3050. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.935 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BCCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1324](#) and described in [Table 9-3052](#).

Return to [Summary Table](#).

N/A

Table 9-3051. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BCCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BCCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BCCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BCCh

Figure 9-1324. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3052. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.936 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BD0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1325](#) and described in [Table 9-3054](#).

Return to [Summary Table](#).

N/A

Table 9-3053. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BD0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BD0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BD0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BD0h

Figure 9-1325. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3054. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.937 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BD4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1326](#) and described in [Table 9-3056](#).

Return to [Summary Table](#).

N/A

Table 9-3055. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BD4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BD4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BD4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BD4h

Figure 9-1326. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3056. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.938 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BD8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1327](#) and described in [Table 9-3058](#).

Return to [Summary Table](#).

N/A

Table 9-3057. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BD8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BD8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BD8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BD8h

Figure 9-1327. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3058. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.939 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BDCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1328](#) and described in [Table 9-3060](#).

Return to [Summary Table](#).

N/A

Table 9-3059. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BDCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BDCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BDCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BDCh

Figure 9-1328. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3060. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.940 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BE0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1329](#) and described in [Table 9-3062](#).

Return to [Summary Table](#).

N/A

Table 9-3061. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BE0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BE0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BE0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BE0h

Figure 9-1329. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3062. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.941 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BE4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1330](#) and described in [Table 9-3064](#).

Return to [Summary Table](#).

N/A

Table 9-3063. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BE4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BE4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BE4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BE4h

Figure 9-1330. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3064. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.942 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BE8h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1331](#) and described in [Table 9-3066](#).

Return to [Summary Table](#).

N/A

Table 9-3065. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCI00_CORE_DBN_CFG_PCIE_CORE	0D40 0BE8h
PCI01_CORE_DBN_CFG_PCIE_CORE	0DC0 0BE8h
PCI02_CORE_DBN_CFG_PCIE_CORE	0E40 0BE8h
PCI03_CORE_DBN_CFG_PCIE_CORE	0EC0 0BE8h

Figure 9-1331. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3066. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.943 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BECh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1332](#) and described in [Table 9-3068](#).

Return to [Summary Table](#).

N/A

Table 9-3067. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BECh

Figure 9-1332. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3068. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.944 PCIE_CORE_RP_ADDR0 Register (Offset = 00400BF0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1333](#) and described in [Table 9-3070](#).

Return to [Summary Table](#).

N/A

Table 9-3069. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BF0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BF0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BF0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BF0h

Figure 9-1333. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3070. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.945 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BF4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1334](#) and described in [Table 9-3072](#).

Return to [Summary Table](#).

N/A

Table 9-3071. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BF4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BF4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BF4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BF4h

Figure 9-1334. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3072. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.946 PCIe_CORE_RP_ADDR0 Register (Offset = 00400BF8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1335](#) and described in [Table 9-3074](#).

Return to [Summary Table](#).

N/A

Table 9-3073. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BF8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BF8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BF8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BF8h

Figure 9-1335. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3074. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.947 PCIE_CORE_RP_ADDR1 Register (Offset = 00400BFCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1336](#) and described in [Table 9-3076](#).

Return to [Summary Table](#).

N/A

Table 9-3075. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0BFCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0BFCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0BFCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0BFCh

Figure 9-1336. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3076. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.948 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C00h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1337](#) and described in [Table 9-3078](#).

Return to [Summary Table](#).

N/A

Table 9-3077. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C00h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C00h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C00h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C00h

Figure 9-1337. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3078. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.949 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C04h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1338](#) and described in [Table 9-3080](#).

Return to [Summary Table](#).

N/A

Table 9-3079. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C04h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C04h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C04h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C04h

Figure 9-1338. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3080. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.950 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C08h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1339](#) and described in [Table 9-3082](#).

Return to [Summary Table](#).

N/A

Table 9-3081. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C08h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C08h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C08h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C08h

Figure 9-1339. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3082. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.951 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C0Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1340](#) and described in [Table 9-3084](#).

Return to [Summary Table](#).

N/A

Table 9-3083. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C0Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C0Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C0Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C0Ch

Figure 9-1340. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3084. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.952 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C10h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1341](#) and described in [Table 9-3086](#).

Return to [Summary Table](#).

N/A

Table 9-3085. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C10h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C10h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C10h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C10h

Figure 9-1341. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3086. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.953 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C14h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1342](#) and described in [Table 9-3088](#).

Return to [Summary Table](#).

N/A

Table 9-3087. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C14h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C14h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C14h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C14h

Figure 9-1342. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3088. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.954 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C18h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1343](#) and described in [Table 9-3090](#).

Return to [Summary Table](#).

N/A

Table 9-3089. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C18h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C18h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C18h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C18h

Figure 9-1343. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3090. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.955 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C1Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1344](#) and described in [Table 9-3092](#).

Return to [Summary Table](#).

N/A

Table 9-3091. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C1Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C1Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C1Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C1Ch

Figure 9-1344. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3092. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.956 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C20h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1345](#) and described in [Table 9-3094](#).

Return to [Summary Table](#).

N/A

Table 9-3093. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C20h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C20h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C20h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C20h

Figure 9-1345. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3094. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.957 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C24h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1346](#) and described in [Table 9-3096](#).

Return to [Summary Table](#).

N/A

Table 9-3095. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C24h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C24h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C24h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C24h

Figure 9-1346. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3096. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.958 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C28h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1347](#) and described in [Table 9-3098](#).

Return to [Summary Table](#).

N/A

Table 9-3097. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C28h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C28h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C28h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C28h

Figure 9-1347. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3098. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.959 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C2Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1348](#) and described in [Table 9-3100](#).

Return to [Summary Table](#).

N/A

Table 9-3099. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C2Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C2Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C2Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C2Ch

Figure 9-1348. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3100. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.960 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C30h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1349](#) and described in [Table 9-3102](#).

Return to [Summary Table](#).

N/A

Table 9-3101. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C30h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C30h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C30h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C30h

Figure 9-1349. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3102. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.961 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C34h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1350](#) and described in [Table 9-3104](#).

Return to [Summary Table](#).

N/A

Table 9-3103. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C34h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C34h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C34h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C34h

Figure 9-1350. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3104. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.962 PCIE_CORE_RP_ADDR0 Register (Offset = 00400C38h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1351](#) and described in [Table 9-3106](#).

Return to [Summary Table](#).

N/A

Table 9-3105. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C38h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C38h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C38h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C38h

Figure 9-1351. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3106. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.963 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C3Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1352](#) and described in [Table 9-3108](#).

Return to [Summary Table](#).

N/A

Table 9-3107. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C3Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C3Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C3Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C3Ch

Figure 9-1352. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3108. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.964 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C40h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1353](#) and described in [Table 9-3110](#).

Return to [Summary Table](#).

N/A

Table 9-3109. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C40h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C40h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C40h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C40h

Figure 9-1353. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3110. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.965 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C44h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1354](#) and described in [Table 9-3112](#).

Return to [Summary Table](#).

N/A

Table 9-3111. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C44h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C44h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C44h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C44h

Figure 9-1354. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3112. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.966 PCIE_CORE_RP_ADDR0 Register (Offset = 00400C48h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1355](#) and described in [Table 9-3114](#).

Return to [Summary Table](#).

N/A

Table 9-3113. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C48h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C48h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C48h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C48h

Figure 9-1355. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3114. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.967 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C4Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1356](#) and described in [Table 9-3116](#).

Return to [Summary Table](#).

N/A

Table 9-3115. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C4Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C4Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C4Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C4Ch

Figure 9-1356. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3116. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.968 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C50h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1357](#) and described in [Table 9-3118](#).

Return to [Summary Table](#).

N/A

Table 9-3117. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C50h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C50h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C50h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C50h

Figure 9-1357. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3118. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.969 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C54h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1358](#) and described in [Table 9-3120](#).

Return to [Summary Table](#).

N/A

Table 9-3119. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C54h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C54h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C54h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C54h

Figure 9-1358. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3120. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.970 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C58h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1359](#) and described in [Table 9-3122](#).

Return to [Summary Table](#).

N/A

Table 9-3121. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C58h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C58h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C58h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C58h

Figure 9-1359. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3122. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.971 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C5Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1360](#) and described in [Table 9-3124](#).

Return to [Summary Table](#).

N/A

Table 9-3123. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C5Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C5Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C5Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C5Ch

Figure 9-1360. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3124. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.972 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C60h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1361](#) and described in [Table 9-3126](#).

Return to [Summary Table](#).

N/A

Table 9-3125. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C60h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C60h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C60h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C60h

Figure 9-1361. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3126. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.973 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C64h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1362](#) and described in [Table 9-3128](#).

Return to [Summary Table](#).

N/A

Table 9-3127. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C64h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C64h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C64h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C64h

Figure 9-1362. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3128. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.974 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C68h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1363](#) and described in [Table 9-3130](#).

Return to [Summary Table](#).

N/A

Table 9-3129. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C68h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C68h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C68h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C68h

Figure 9-1363. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3130. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.975 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C6Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1364](#) and described in [Table 9-3132](#).

Return to [Summary Table](#).

N/A

Table 9-3131. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C6Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C6Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C6Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C6Ch

Figure 9-1364. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3132. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.976 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C70h) [reset = 0h]

PCIe_CORE_RP_ADDR0 is shown in [Figure 9-1365](#) and described in [Table 9-3134](#).

Return to [Summary Table](#).

N/A

Table 9-3133. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C70h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C70h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C70h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C70h

Figure 9-1365. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3134. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.977 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C74h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1366](#) and described in [Table 9-3136](#).

Return to [Summary Table](#).

N/A

Table 9-3135. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C74h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C74h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C74h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C74h

Figure 9-1366. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3136. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.978 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C78h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1367](#) and described in [Table 9-3138](#).

Return to [Summary Table](#).

N/A

Table 9-3137. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C78h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C78h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C78h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C78h

Figure 9-1367. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3138. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.979 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C7Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1368](#) and described in [Table 9-3140](#).

Return to [Summary Table](#).

N/A

Table 9-3139. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C7Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C7Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C7Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C7Ch

Figure 9-1368. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3140. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.980 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C80h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1369](#) and described in [Table 9-3142](#).

Return to [Summary Table](#).

N/A

Table 9-3141. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C80h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C80h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C80h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C80h

Figure 9-1369. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3142. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.981 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C84h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1370](#) and described in [Table 9-3144](#).

Return to [Summary Table](#).

N/A

Table 9-3143. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C84h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C84h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C84h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C84h

Figure 9-1370. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3144. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.982 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C88h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1371](#) and described in [Table 9-3146](#).

Return to [Summary Table](#).

N/A

Table 9-3145. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C88h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C88h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C88h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C88h

Figure 9-1371. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3146. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.983 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C8Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1372](#) and described in [Table 9-3148](#).

Return to [Summary Table](#).

N/A

Table 9-3147. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C8Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C8Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C8Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C8Ch

Figure 9-1372. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3148. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.984 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C90h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1373](#) and described in [Table 9-3150](#).

Return to [Summary Table](#).

N/A

Table 9-3149. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C90h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C90h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C90h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C90h

Figure 9-1373. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3150. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.985 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C94h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1374](#) and described in [Table 9-3152](#).

Return to [Summary Table](#).

N/A

Table 9-3151. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C94h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C94h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C94h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C94h

Figure 9-1374. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3152. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.986 PCIe_CORE_RP_ADDR0 Register (Offset = 00400C98h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1375](#) and described in [Table 9-3154](#).

Return to [Summary Table](#).

N/A

Table 9-3153. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C98h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C98h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C98h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C98h

Figure 9-1375. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3154. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.987 PCIE_CORE_RP_ADDR1 Register (Offset = 00400C9Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1376](#) and described in [Table 9-3156](#).

Return to [Summary Table](#).

N/A

Table 9-3155. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0C9Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0C9Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0C9Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0C9Ch

Figure 9-1376. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3156. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.988 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CA0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1377](#) and described in [Table 9-3158](#).

Return to [Summary Table](#).

N/A

Table 9-3157. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CA0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CA0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CA0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CA0h

Figure 9-1377. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3158. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.989 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CA4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1378](#) and described in [Table 9-3160](#).

Return to [Summary Table](#).

N/A

Table 9-3159. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CA4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CA4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CA4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CA4h

Figure 9-1378. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3160. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.990 PCIe_CORE_RP_ADDR0 Register (Offset = 00400CA8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1379](#) and described in [Table 9-3162](#).

Return to [Summary Table](#).

N/A

Table 9-3161. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CA8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CA8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CA8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CA8h

Figure 9-1379. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3162. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.991 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CACH) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1380](#) and described in [Table 9-3164](#).

Return to [Summary Table](#).

N/A

Table 9-3163. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CACH
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CACH
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CACH
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CACH

Figure 9-1380. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3164. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.992 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CB0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1381](#) and described in [Table 9-3166](#).

Return to [Summary Table](#).

N/A

Table 9-3165. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CB0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CB0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CB0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CB0h

Figure 9-1381. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3166. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.993 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CB4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1382](#) and described in [Table 9-3168](#).

Return to [Summary Table](#).

N/A

Table 9-3167. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CB4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CB4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CB4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CB4h

Figure 9-1382. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3168. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.994 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CB8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1383](#) and described in [Table 9-3170](#).

Return to [Summary Table](#).

N/A

Table 9-3169. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CB8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CB8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CB8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CB8h

Figure 9-1383. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3170. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.995 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CBCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1384](#) and described in [Table 9-3172](#).

Return to [Summary Table](#).

N/A

Table 9-3171. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CBCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CBCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CBCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CBCh

Figure 9-1384. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3172. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.996 PCIe_CORE_RP_ADDR0 Register (Offset = 00400CC0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1385](#) and described in [Table 9-3174](#).

Return to [Summary Table](#).

N/A

Table 9-3173. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CC0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CC0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CC0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CC0h

Figure 9-1385. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3174. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.997 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CC4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1386](#) and described in [Table 9-3176](#).

Return to [Summary Table](#).

N/A

Table 9-3175. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CC4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CC4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CC4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CC4h

Figure 9-1386. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3176. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.998 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CC8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1387](#) and described in [Table 9-3178](#).

Return to [Summary Table](#).

N/A

Table 9-3177. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CC8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CC8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CC8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CC8h

Figure 9-1387. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3178. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.999 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CCCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1388](#) and described in [Table 9-3180](#).

Return to [Summary Table](#).

N/A

Table 9-3179. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CCCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CCCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CCCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CCCh

Figure 9-1388. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3180. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1000 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CD0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1389](#) and described in [Table 9-3182](#).

Return to [Summary Table](#).

N/A

Table 9-3181. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CD0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CD0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CD0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CD0h

Figure 9-1389. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3182. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1001 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CD4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1390](#) and described in [Table 9-3184](#).

Return to [Summary Table](#).

N/A

Table 9-3183. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CD4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CD4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CD4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CD4h

Figure 9-1390. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3184. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1002 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CD8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1391](#) and described in [Table 9-3186](#).

Return to [Summary Table](#).

N/A

Table 9-3185. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CD8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CD8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CD8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CD8h

Figure 9-1391. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3186. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1003 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CDCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1392](#) and described in [Table 9-3188](#).

Return to [Summary Table](#).

N/A

Table 9-3187. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CDCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CDCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CDCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CDCh

Figure 9-1392. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3188. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1004 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CE0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1393](#) and described in [Table 9-3190](#).

Return to [Summary Table](#).

N/A

Table 9-3189. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CE0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CE0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CE0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CE0h

Figure 9-1393. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3190. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1005 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CE4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1394](#) and described in [Table 9-3192](#).

Return to [Summary Table](#).

N/A

Table 9-3191. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CE4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CE4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CE4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CE4h

Figure 9-1394. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3192. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1006 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CE8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1395](#) and described in [Table 9-3194](#).

Return to [Summary Table](#).

N/A

Table 9-3193. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CE8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CE8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CE8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CE8h

Figure 9-1395. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3194. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1007 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CECh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1396](#) and described in [Table 9-3196](#).

Return to [Summary Table](#).

N/A

Table 9-3195. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CECh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CECh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CECh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CECh

Figure 9-1396. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3196. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1008 PCIE_CORE_RP_ADDR0 Register (Offset = 00400CF0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1397](#) and described in [Table 9-3198](#).

Return to [Summary Table](#).

N/A

Table 9-3197. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CF0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CF0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CF0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CF0h

Figure 9-1397. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3198. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1009 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CF4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1398](#) and described in [Table 9-3200](#).

Return to [Summary Table](#).

N/A

Table 9-3199. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CF4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CF4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CF4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CF4h

Figure 9-1398. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3200. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1010 PCIe_CORE_RP_ADDR0 Register (Offset = 00400CF8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1399](#) and described in [Table 9-3202](#).

Return to [Summary Table](#).

N/A

Table 9-3201. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CF8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CF8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CF8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CF8h

Figure 9-1399. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3202. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1011 PCIE_CORE_RP_ADDR1 Register (Offset = 00400CFCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1400](#) and described in [Table 9-3204](#).

Return to [Summary Table](#).

N/A

Table 9-3203. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0CFCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0CFCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0CFCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0CFCh

Figure 9-1400. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3204. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1012 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D00h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1401](#) and described in [Table 9-3206](#).

Return to [Summary Table](#).

N/A

Table 9-3205. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D00h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D00h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D00h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D00h

Figure 9-1401. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3206. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1013 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D04h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1402](#) and described in [Table 9-3208](#).

Return to [Summary Table](#).

N/A

Table 9-3207. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D04h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D04h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D04h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D04h

Figure 9-1402. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3208. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1014 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D08h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1403](#) and described in [Table 9-3210](#).

Return to [Summary Table](#).

N/A

Table 9-3209. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D08h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D08h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D08h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D08h

Figure 9-1403. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3210. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1015 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D0Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1404](#) and described in [Table 9-3212](#).

Return to [Summary Table](#).

N/A

Table 9-3211. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D0Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D0Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D0Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D0Ch

Figure 9-1404. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3212. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1016 PCIe_CORE_RP_ADDR0 Register (Offset = 00400D10h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1405](#) and described in [Table 9-3214](#).

Return to [Summary Table](#).

N/A

Table 9-3213. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D10h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D10h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D10h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D10h

Figure 9-1405. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3214. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1017 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D14h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1406](#) and described in [Table 9-3216](#).

Return to [Summary Table](#).

N/A

Table 9-3215. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D14h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D14h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D14h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D14h

Figure 9-1406. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3216. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1018 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D18h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1407](#) and described in [Table 9-3218](#).

Return to [Summary Table](#).

N/A

Table 9-3217. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D18h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D18h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D18h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D18h

Figure 9-1407. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3218. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1019 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D1Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1408](#) and described in [Table 9-3220](#).

Return to [Summary Table](#).

N/A

Table 9-3219. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D1Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D1Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D1Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D1Ch

Figure 9-1408. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3220. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1020 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D20h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1409](#) and described in [Table 9-3222](#).

Return to [Summary Table](#).

N/A

Table 9-3221. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D20h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D20h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D20h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D20h

Figure 9-1409. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3222. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1021 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D24h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1410](#) and described in [Table 9-3224](#).

Return to [Summary Table](#).

N/A

Table 9-3223. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D24h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D24h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D24h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D24h

Figure 9-1410. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3224. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1022 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D28h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1411](#) and described in [Table 9-3226](#).

Return to [Summary Table](#).

N/A

Table 9-3225. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D28h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D28h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D28h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D28h

Figure 9-1411. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3226. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1023 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D2Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1412](#) and described in [Table 9-3228](#).

Return to [Summary Table](#).

N/A

Table 9-3227. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D2Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D2Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D2Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D2Ch

Figure 9-1412. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3228. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1024 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D30h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1413](#) and described in [Table 9-3230](#).

Return to [Summary Table](#).

N/A

Table 9-3229. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D30h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D30h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D30h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D30h

Figure 9-1413. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3230. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1025 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D34h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1414](#) and described in [Table 9-3232](#).

Return to [Summary Table](#).

N/A

Table 9-3231. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D34h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D34h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D34h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D34h

Figure 9-1414. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3232. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1026 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D38h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1415](#) and described in [Table 9-3234](#).

Return to [Summary Table](#).

N/A

Table 9-3233. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D38h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D38h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D38h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D38h

Figure 9-1415. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3234. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1027 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D3Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1416](#) and described in [Table 9-3236](#).

Return to [Summary Table](#).

N/A

Table 9-3235. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D3Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D3Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D3Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D3Ch

Figure 9-1416. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3236. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1028 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D40h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1417](#) and described in [Table 9-3238](#).

Return to [Summary Table](#).

N/A

Table 9-3237. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D40h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D40h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D40h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D40h

Figure 9-1417. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3238. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1029 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D44h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1418](#) and described in [Table 9-3240](#).

Return to [Summary Table](#).

N/A

Table 9-3239. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D44h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D44h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D44h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D44h

Figure 9-1418. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3240. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1030 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D48h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1419](#) and described in [Table 9-3242](#).

Return to [Summary Table](#).

N/A

Table 9-3241. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D48h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D48h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D48h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D48h

Figure 9-1419. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3242. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1031 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D4Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1420](#) and described in [Table 9-3244](#).

Return to [Summary Table](#).

N/A

Table 9-3243. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D4Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D4Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D4Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D4Ch

Figure 9-1420. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3244. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1032 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D50h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1421](#) and described in [Table 9-3246](#).

Return to [Summary Table](#).

N/A

Table 9-3245. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D50h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D50h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D50h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D50h

Figure 9-1421. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3246. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1033 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D54h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1422](#) and described in [Table 9-3248](#).

Return to [Summary Table](#).

N/A

Table 9-3247. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D54h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D54h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D54h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D54h

Figure 9-1422. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3248. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1034 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D58h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1423](#) and described in [Table 9-3250](#).

Return to [Summary Table](#).

N/A

Table 9-3249. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D58h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D58h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D58h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D58h

Figure 9-1423. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3250. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1035 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D5Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1424](#) and described in [Table 9-3252](#).

Return to [Summary Table](#).

N/A

Table 9-3251. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D5Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D5Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D5Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D5Ch

Figure 9-1424. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3252. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1036 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D60h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1425](#) and described in [Table 9-3254](#).

Return to [Summary Table](#).

N/A

Table 9-3253. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D60h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D60h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D60h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D60h

Figure 9-1425. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3254. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1037 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D64h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1426](#) and described in [Table 9-3256](#).

Return to [Summary Table](#).

N/A

Table 9-3255. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D64h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D64h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D64h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D64h

Figure 9-1426. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3256. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1038 PCIe_CORE_RP_ADDR0 Register (Offset = 00400D68h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1427](#) and described in [Table 9-3258](#).

Return to [Summary Table](#).

N/A

Table 9-3257. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D68h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D68h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D68h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D68h

Figure 9-1427. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3258. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1039 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D6Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1428](#) and described in [Table 9-3260](#).

Return to [Summary Table](#).

N/A

Table 9-3259. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D6Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D6Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D6Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D6Ch

Figure 9-1428. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3260. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1040 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D70h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1429](#) and described in [Table 9-3262](#).

Return to [Summary Table](#).

N/A

Table 9-3261. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D70h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D70h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D70h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D70h

Figure 9-1429. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3262. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1041 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D74h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1430](#) and described in [Table 9-3264](#).

Return to [Summary Table](#).

N/A

Table 9-3263. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D74h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D74h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D74h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D74h

Figure 9-1430. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3264. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1042 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D78h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1431](#) and described in [Table 9-3266](#).

Return to [Summary Table](#).

N/A

Table 9-3265. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D78h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D78h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D78h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D78h

Figure 9-1431. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3266. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1043 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D7Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1432](#) and described in [Table 9-3268](#).

Return to [Summary Table](#).

N/A

Table 9-3267. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D7Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D7Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D7Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D7Ch

Figure 9-1432. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3268. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1044 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D80h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1433](#) and described in [Table 9-3270](#).

Return to [Summary Table](#).

N/A

Table 9-3269. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D80h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D80h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D80h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D80h

Figure 9-1433. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3270. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1045 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D84h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1434](#) and described in [Table 9-3272](#).

Return to [Summary Table](#).

N/A

Table 9-3271. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D84h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D84h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D84h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D84h

Figure 9-1434. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3272. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1046 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D88h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1435](#) and described in [Table 9-3274](#).

Return to [Summary Table](#).

N/A

Table 9-3273. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D88h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D88h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D88h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D88h

Figure 9-1435. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3274. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1047 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D8Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1436](#) and described in [Table 9-3276](#).

Return to [Summary Table](#).

N/A

Table 9-3275. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D8Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D8Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D8Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D8Ch

Figure 9-1436. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3276. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1048 PCIE_CORE_RP_ADDR0 Register (Offset = 00400D90h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1437](#) and described in [Table 9-3278](#).

Return to [Summary Table](#).

N/A

Table 9-3277. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D90h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D90h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D90h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D90h

Figure 9-1437. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3278. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1049 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D94h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1438](#) and described in [Table 9-3280](#).

Return to [Summary Table](#).

N/A

Table 9-3279. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D94h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D94h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D94h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D94h

Figure 9-1438. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3280. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1050 PCIe_CORE_RP_ADDR0 Register (Offset = 00400D98h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1439](#) and described in [Table 9-3282](#).

Return to [Summary Table](#).

N/A

Table 9-3281. PCIe_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D98h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D98h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D98h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D98h

Figure 9-1439. PCIe_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3282. PCIe_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1051 PCIE_CORE_RP_ADDR1 Register (Offset = 00400D9Ch) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1440](#) and described in [Table 9-3284](#).

Return to [Summary Table](#).

N/A

Table 9-3283. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0D9Ch
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0D9Ch
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0D9Ch
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0D9Ch

Figure 9-1440. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3284. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1052 PCIE_CORE_RP_ADDR0 Register (Offset = 00400DA0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1441](#) and described in [Table 9-3286](#).

Return to [Summary Table](#).

N/A

Table 9-3285. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0DA0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0DA0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0DA0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0DA0h

Figure 9-1441. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3286. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1053 PCIE_CORE_RP_ADDR1 Register (Offset = 00400DA4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1442](#) and described in [Table 9-3288](#).

Return to [Summary Table](#).

N/A

Table 9-3287. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0DA4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0DA4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0DA4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0DA4h

Figure 9-1442. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3288. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1054 PCIE_CORE_RP_ADDR0 Register (Offset = 00400DA8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1443](#) and described in [Table 9-3290](#).

Return to [Summary Table](#).

N/A

Table 9-3289. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0DA8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0DA8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0DA8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0DA8h

Figure 9-1443. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3290. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1055 PCIE_CORE_RP_ADDR1 Register (Offset = 00400DACH) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1444](#) and described in [Table 9-3292](#).

Return to [Summary Table](#).

N/A

Table 9-3291. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0DACH
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0DACH
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0DACH
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0DACH

Figure 9-1444. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3292. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1056 PCIE_CORE_RP_ADDR0 Register (Offset = 00400DB0h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1445](#) and described in [Table 9-3294](#).

Return to [Summary Table](#).

N/A

Table 9-3293. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0DB0h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0DB0h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0DB0h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0DB0h

Figure 9-1445. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3294. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1057 PCIE_CORE_RP_ADDR1 Register (Offset = 00400DB4h) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1446](#) and described in [Table 9-3296](#).

Return to [Summary Table](#).

N/A

Table 9-3295. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0DB4h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0DB4h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0DB4h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0DB4h

Figure 9-1446. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3296. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.5.1058 PCIE_CORE_RP_ADDR0 Register (Offset = 00400DB8h) [reset = 0h]

PCIE_CORE_RP_ADDR0 is shown in [Figure 9-1447](#) and described in [Table 9-3298](#).

Return to [Summary Table](#).

N/A

Table 9-3297. PCIE_CORE_RP_ADDR0 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0DB8h
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0DB8h
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0DB8h
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0DB8h

Figure 9-1447. PCIE_CORE_RP_ADDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3298. PCIE_CORE_RP_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [31:0] of Address Register for BAR N

9.5.1059 PCIE_CORE_RP_ADDR1 Register (Offset = 00400DBCh) [reset = 0h]

PCIE_CORE_RP_ADDR1 is shown in [Figure 9-1448](#) and described in [Table 9-3300](#).

Return to [Summary Table](#).

N/A

Table 9-3299. PCIE_CORE_RP_ADDR1 Instances

Instance	Physical Address
PCIE0_CORE_DBN_CFG_PCIE_CORE	0D40 0DBCh
PCIE1_CORE_DBN_CFG_PCIE_CORE	0DC0 0DBCh
PCIE2_CORE_DBN_CFG_PCIE_CORE	0E40 0DBCh
PCIE3_CORE_DBN_CFG_PCIE_CORE	0EC0 0DBCh

Figure 9-1448. PCIE_CORE_RP_ADDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3300. PCIE_CORE_RP_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Bits [63:32] of AXI Address Register for BAR N

9.6 PCIe_INTD Registers

Table 9-3302 lists the memory-mapped registers for the PCIe_INTD. All register offset addresses not listed in Table 9-3302 should be considered as reserved locations and the register contents should not be modified.

Table 9-3301. PCIe_INTD Instances

Instance	Base Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0000h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0000h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0000h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0000h

Table 9-3302. PCIe_INTD Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG Physical Address	PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG Physical Address
0h	PCIE_INTD_REVISION		0290 0000h	0291 0000h
10h	PCIE_INTD_EOI_REG		0290 0010h	0291 0010h
14h	PCIE_INTD_INTR_VECTOR_REG		0290 0014h	0291 0014h
100h	PCIE_INTD_ENABLE_REG_SYS_0		0290 0100h	0291 0100h
104h	PCIE_INTD_ENABLE_REG_SYS_1		0290 0104h	0291 0104h
108h	PCIE_INTD_ENABLE_REG_SYS_2		0290 0108h	0291 0108h
300h	PCIE_INTD_ENABLE_CLR_REG_SYS_0		0290 0300h	0291 0300h
304h	PCIE_INTD_ENABLE_CLR_REG_SYS_1		0290 0304h	0291 0304h
308h	PCIE_INTD_ENABLE_CLR_REG_SYS_2		0290 0308h	0291 0308h
500h	PCIE_INTD_STATUS_REG_SYS_0		0290 0500h	0291 0500h
504h	PCIE_INTD_STATUS_REG_SYS_1		0290 0504h	0291 0504h
508h	PCIE_INTD_STATUS_REG_SYS_2		0290 0508h	0291 0508h
700h	PCIE_INTD_STATUS_CLR_REG_SYS_0		0290 0700h	0291 0700h
704h	PCIE_INTD_STATUS_CLR_REG_SYS_1		0290 0704h	0291 0704h
708h	PCIE_INTD_STATUS_CLR_REG_SYS_2		0290 0708h	0291 0708h
A80h	PCIE_INTD_INTR_VECTOR_REG_SYS		0290 0A80h	0291 0A80h

Table 9-3303. PCIe_INTD Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG Physical Address	PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG Physical Address
0h	PCIE_INTD_REVISION		0292 0000h	0293 0000h
10h	PCIE_INTD_EOI_REG		0292 0010h	0293 0010h
14h	PCIE_INTD_INTR_VECTOR_REG		0292 0014h	0293 0014h
100h	PCIE_INTD_ENABLE_REG_SYS_0		0292 0100h	0293 0100h
104h	PCIE_INTD_ENABLE_REG_SYS_1		0292 0104h	0293 0104h
108h	PCIE_INTD_ENABLE_REG_SYS_2		0292 0108h	0293 0108h
300h	PCIE_INTD_ENABLE_CLR_REG_SYS_0		0292 0300h	0293 0300h
304h	PCIE_INTD_ENABLE_CLR_REG_SYS_1		0292 0304h	0293 0304h
308h	PCIE_INTD_ENABLE_CLR_REG_SYS_2		0292 0308h	0293 0308h
500h	PCIE_INTD_STATUS_REG_SYS_0		0292 0500h	0293 0500h
504h	PCIE_INTD_STATUS_REG_SYS_1		0292 0504h	0293 0504h
508h	PCIE_INTD_STATUS_REG_SYS_2		0292 0508h	0293 0508h
700h	PCIE_INTD_STATUS_CLR_REG_SYS_0		0292 0700h	0293 0700h
704h	PCIE_INTD_STATUS_CLR_REG_SYS_1		0292 0704h	0293 0704h

Table 9-3303. PCIE_INTD Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_PC IE_INTD_CFG_IN TD_CFG Physical Address	PCIE3_CORE_PC IE_INTD_CFG_IN TD_CFG Physical Address
708h	PCIE_INTD_STATUS_CLR_REG_SYS_2		0292 0708h	0293 0708h
A80h	PCIE_INTD_INTR_VECTOR_REG_SYS		0292 0A80h	0293 0A80h

9.6.1 PCIe_INTD_REVISION Register (Offset = 0h) [reset = 6690A200h]

PCIE_INTD_REVISION is shown in [Figure 9-1449](#) and described in [Table 9-3305](#).

Return to [Summary Table](#).

PCIE_INTD_REVISION Register

Table 9-3304. PCIe_INTD_REVISION Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0000h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0000h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0000h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0000h

Figure 9-1449. PCIe_INTD_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNCTION									
R-1h				R-2h		R-690h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER					MAJREV			CUSTOM		MINREV					
R-14h					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 9-3305. PCIe_INTD_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	BU
27-16	FUNCTION	R	690h	Module ID
15-11	RTLVER	R	14h	RTL revisions
10-8	MAJREV	R	2h	Major PCIE_INTD_REVISION
7-6	CUSTOM	R	0h	Custom PCIE_INTD_REVISION
5-0	MINREV	R	0h	Minor PCIE_INTD_REVISION

Table 9-3306. Register Call Summary for PCIe_INTD_REVISION

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_REVISION Register \(Offset = 0h\) \[reset = 6690A200h\]: \[0\] \[1\] \[2\] \[3\] \[4\]](#)

9.6.2 PCIE_INTD_EOI_REG Register (Offset = 10h) [reset = X]

PCIE_INTD_EOI_REG is shown in [Figure 9-1450](#) and described in [Table 9-3308](#).

[Return to Summary Table.](#)

End of Interrupt Register

Table 9-3307. PCIE_INTD_EOI_REG Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0010h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0010h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0010h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0010h

Figure 9-1450. PCIE_INTD_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3308. PCIE_INTD_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	EOI_VECTOR	R/W	0h	End of Interrupt Vector

Table 9-3309. Register Call Summary for PCIE_INTD_EOI_REG

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_EOI_REG Register \(Offset = 10h\) \[reset = X\]: \[0\]](#)

9.6.3 PCIE_INTD_INTR_VECTOR_REG Register (Offset = 14h) [reset = 0h]

PCIE_INTD_INTR_VECTOR_REG is shown in [Figure 9-1451](#) and described in [Table 9-3311](#).

Return to [Summary Table](#).

Interrupt Vector Register

**Table 9-3310. PCIE_INTD_INTR_VECTOR_REG
Instances**

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0014h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0014h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0014h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0014h

Figure 9-1451. PCIE_INTD_INTR_VECTOR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VECTOR																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3311. PCIE_INTD_INTR_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INTR_VECTOR	R	0h	Interrupt Vector Register

Table 9-3312. Register Call Summary for PCIE_INTD_INTR_VECTOR_REG

PCIE_INTD Registers
<ul style="list-style-type: none"> • PCIE_INTD Registers: [0] [1] • PCIE_INTD_INTR_VECTOR_REG Register (Offset = 14h) [reset = 0h]: [0]

9.6.4 PCIE_INTD_ENABLE_REG_SYS_0 Register (Offset = 100h) [reset = X]

PCIE_INTD_ENABLE_REG_SYS_0 is shown in Figure 9-1452 and described in Table 9-3314.

Return to [Summary Table](#).

Enable Register 0

**Table 9-3313. PCIE_INTD_ENABLE_REG_SYS_0
Instances**

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0100h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0100h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0100h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0100h

Figure 9-1452. PCIE_INTD_ENABLE_REG_SYS_0 Register

31	30	29	28	27	26	25	24
RESERVED							ENABLE_SYS_EN_PCIE_ASF_8
R/W-X							R/W1S-0h
23	22	21	20	19	18	17	16
ENABLE_SYS_EN_PCIE_ASF_7	ENABLE_SYS_EN_PCIE_ASF_6	ENABLE_SYS_EN_PCIE_ASF_5	ENABLE_SYS_EN_PCIE_ASF_4	ENABLE_SYS_EN_PCIE_ASF_3	ENABLE_SYS_EN_PCIE_ASF_2	ENABLE_SYS_EN_PCIE_ASF_1	ENABLE_SYS_EN_PCIE_ASF_0
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RESERVED					ENABLE_SYS_EN_PCIE_ERR_OR_2	ENABLE_SYS_EN_PCIE_ERR_OR_1	ENABLE_SYS_EN_PCIE_ERR_OR_0
R/W-X					R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RESERVED				ENABLE_SYS_EN_PCIE_LEGACY_3	ENABLE_SYS_EN_PCIE_LEGACY_2	ENABLE_SYS_EN_PCIE_LEGACY_1	ENABLE_SYS_EN_PCIE_LEGACY_0
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3314. PCIE_INTD_ENABLE_REG_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ENABLE_SYS_EN_PCIE_ASF_8	R/W1S	0h	Enable Set for sys_en_pcie_asf_8
23	ENABLE_SYS_EN_PCIE_ASF_7	R/W1S	0h	Enable Set for sys_en_pcie_asf_7
22	ENABLE_SYS_EN_PCIE_ASF_6	R/W1S	0h	Enable Set for sys_en_pcie_asf_6
21	ENABLE_SYS_EN_PCIE_ASF_5	R/W1S	0h	Enable Set for sys_en_pcie_asf_5
20	ENABLE_SYS_EN_PCIE_ASF_4	R/W1S	0h	Enable Set for sys_en_pcie_asf_4

Table 9-3314. PCIE_INTD_ENABLE_REG_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	ENABLE_SYS_EN_PCIE_ASF_3	R/W1S	0h	Enable Set for sys_en_pcie_asf_3
18	ENABLE_SYS_EN_PCIE_ASF_2	R/W1S	0h	Enable Set for sys_en_pcie_asf_2
17	ENABLE_SYS_EN_PCIE_ASF_1	R/W1S	0h	Enable Set for sys_en_pcie_asf_1
16	ENABLE_SYS_EN_PCIE_ASF_0	R/W1S	0h	Enable Set for sys_en_pcie_asf_0
15-11	RESERVED	R/W	X	
10	ENABLE_SYS_EN_PCIE_ERROR_2	R/W1S	0h	Enable Set for sys_en_pcie_error_2
9	ENABLE_SYS_EN_PCIE_ERROR_1	R/W1S	0h	Enable Set for sys_en_pcie_error_1
8	ENABLE_SYS_EN_PCIE_ERROR_0	R/W1S	0h	Enable Set for sys_en_pcie_error_0
7-4	RESERVED	R/W	X	
3	ENABLE_SYS_EN_PCIE_LEGACY_3	R/W1S	0h	Enable Set for sys_en_pcie_legacy_3
2	ENABLE_SYS_EN_PCIE_LEGACY_2	R/W1S	0h	Enable Set for sys_en_pcie_legacy_2
1	ENABLE_SYS_EN_PCIE_LEGACY_1	R/W1S	0h	Enable Set for sys_en_pcie_legacy_1
0	ENABLE_SYS_EN_PCIE_LEGACY_0	R/W1S	0h	Enable Set for sys_en_pcie_legacy_0

Table 9-3315. Register Call Summary for PCIE_INTD_ENABLE_REG_SYS_0

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_ENABLE_REG_SYS_0 Register \(Offset = 100h\) \[reset = X\]: \[0\]](#)

9.6.5 PCIE_INTD_ENABLE_REG_SYS_1 Register (Offset = 104h) [reset = X]

PCIE_INTD_ENABLE_REG_SYS_1 is shown in Figure 9-1453 and described in Table 9-3317.

Return to [Summary Table](#).

Enable Register 1

**Table 9-3316. PCIE_INTD_ENABLE_REG_SYS_1
Instances**

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0104h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0104h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0104h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0104h

Figure 9-1453. PCIE_INTD_ENABLE_REG_SYS_1 Register

31	30	29	28	27	26	25	24
RESERVED		ENABLE_SYS_EN_PCIE_DO_WNSTREAM_5	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_4	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_3	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_2	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_1	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_0
R/W-X		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
RESERVED		ENABLE_SYS_EN_PCIE_FLR_21	ENABLE_SYS_EN_PCIE_FLR_20	ENABLE_SYS_EN_PCIE_FLR_19	ENABLE_SYS_EN_PCIE_FLR_18	ENABLE_SYS_EN_PCIE_FLR_17	ENABLE_SYS_EN_PCIE_FLR_16
R/W-X		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
ENABLE_SYS_EN_PCIE_FLR_15	ENABLE_SYS_EN_PCIE_FLR_14	ENABLE_SYS_EN_PCIE_FLR_13	ENABLE_SYS_EN_PCIE_FLR_12	ENABLE_SYS_EN_PCIE_FLR_11	ENABLE_SYS_EN_PCIE_FLR_10	ENABLE_SYS_EN_PCIE_FLR_9	ENABLE_SYS_EN_PCIE_FLR_8
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
ENABLE_SYS_EN_PCIE_FLR_7	ENABLE_SYS_EN_PCIE_FLR_6	ENABLE_SYS_EN_PCIE_FLR_5	ENABLE_SYS_EN_PCIE_FLR_4	ENABLE_SYS_EN_PCIE_FLR_3	ENABLE_SYS_EN_PCIE_FLR_2	ENABLE_SYS_EN_PCIE_FLR_1	ENABLE_SYS_EN_PCIE_FLR_0
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3317. PCIE_INTD_ENABLE_REG_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29	ENABLE_SYS_EN_PCIE_DOWNSTREAM_5	R/W1S	0h	Enable Set for sys_en_pcie_downstream_5
28	ENABLE_SYS_EN_PCIE_DOWNSTREAM_4	R/W1S	0h	Enable Set for sys_en_pcie_downstream_4
27	ENABLE_SYS_EN_PCIE_DOWNSTREAM_3	R/W1S	0h	Enable Set for sys_en_pcie_downstream_3
26	ENABLE_SYS_EN_PCIE_DOWNSTREAM_2	R/W1S	0h	Enable Set for sys_en_pcie_downstream_2
25	ENABLE_SYS_EN_PCIE_DOWNSTREAM_1	R/W1S	0h	Enable Set for sys_en_pcie_downstream_1

Table 9-3317. PCIE_INTD_ENABLE_REG_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	ENABLE_SYS_EN_PCIE_DOWNSTREAM_0	R/W1S	0h	Enable Set for sys_en_pcie_downstream_0
23-22	RESERVED	R/W	X	
21	ENABLE_SYS_EN_PCIE_FLR_21	R/W1S	0h	Enable Set for sys_en_pcie_flr_21
20	ENABLE_SYS_EN_PCIE_FLR_20	R/W1S	0h	Enable Set for sys_en_pcie_flr_20
19	ENABLE_SYS_EN_PCIE_FLR_19	R/W1S	0h	Enable Set for sys_en_pcie_flr_19
18	ENABLE_SYS_EN_PCIE_FLR_18	R/W1S	0h	Enable Set for sys_en_pcie_flr_18
17	ENABLE_SYS_EN_PCIE_FLR_17	R/W1S	0h	Enable Set for sys_en_pcie_flr_17
16	ENABLE_SYS_EN_PCIE_FLR_16	R/W1S	0h	Enable Set for sys_en_pcie_flr_16
15	ENABLE_SYS_EN_PCIE_FLR_15	R/W1S	0h	Enable Set for sys_en_pcie_flr_15
14	ENABLE_SYS_EN_PCIE_FLR_14	R/W1S	0h	Enable Set for sys_en_pcie_flr_14
13	ENABLE_SYS_EN_PCIE_FLR_13	R/W1S	0h	Enable Set for sys_en_pcie_flr_13
12	ENABLE_SYS_EN_PCIE_FLR_12	R/W1S	0h	Enable Set for sys_en_pcie_flr_12
11	ENABLE_SYS_EN_PCIE_FLR_11	R/W1S	0h	Enable Set for sys_en_pcie_flr_11
10	ENABLE_SYS_EN_PCIE_FLR_10	R/W1S	0h	Enable Set for sys_en_pcie_flr_10
9	ENABLE_SYS_EN_PCIE_FLR_9	R/W1S	0h	Enable Set for sys_en_pcie_flr_9
8	ENABLE_SYS_EN_PCIE_FLR_8	R/W1S	0h	Enable Set for sys_en_pcie_flr_8
7	ENABLE_SYS_EN_PCIE_FLR_7	R/W1S	0h	Enable Set for sys_en_pcie_flr_7
6	ENABLE_SYS_EN_PCIE_FLR_6	R/W1S	0h	Enable Set for sys_en_pcie_flr_6
5	ENABLE_SYS_EN_PCIE_FLR_5	R/W1S	0h	Enable Set for sys_en_pcie_flr_5
4	ENABLE_SYS_EN_PCIE_FLR_4	R/W1S	0h	Enable Set for sys_en_pcie_flr_4
3	ENABLE_SYS_EN_PCIE_FLR_3	R/W1S	0h	Enable Set for sys_en_pcie_flr_3
2	ENABLE_SYS_EN_PCIE_FLR_2	R/W1S	0h	Enable Set for sys_en_pcie_flr_2
1	ENABLE_SYS_EN_PCIE_FLR_1	R/W1S	0h	Enable Set for sys_en_pcie_flr_1
0	ENABLE_SYS_EN_PCIE_FLR_0	R/W1S	0h	Enable Set for sys_en_pcie_flr_0

Table 9-3318. Register Call Summary for PCIE_INTD_ENABLE_REG_SYS_1

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_ENABLE_REG_SYS_1 Register \(Offset = 104h\) \[reset = X\]: \[0\]](#)

9.6.6 PCIE_INTD_ENABLE_REG_SYS_2 Register (Offset = 108h) [reset = X]

PCIE_INTD_ENABLE_REG_SYS_2 is shown in Figure 9-1454 and described in Table 9-3320.

Return to [Summary Table](#).

Enable Register 2

**Table 9-3319. PCIE_INTD_ENABLE_REG_SYS_2
Instances**

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0108h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0108h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0108h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0108h

Figure 9-1454. PCIE_INTD_ENABLE_REG_SYS_2 Register

31	30	29	28	27	26	25	24
RESERVED							ENABLE_SYS_EN_PCIE_PTM
R/W-X							R/W1S-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	ENABLE_SYS_EN_PCIE_PWR_STATE_6	ENABLE_SYS_EN_PCIE_PWR_STATE_5	ENABLE_SYS_EN_PCIE_PWR_STATE_4	ENABLE_SYS_EN_PCIE_PWR_STATE_3	ENABLE_SYS_EN_PCIE_PWR_STATE_2	ENABLE_SYS_EN_PCIE_PWR_STATE_1	ENABLE_SYS_EN_PCIE_PWR_STATE_0
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RESERVED						ENABLE_SYS_EN_PCIE_LINK_STATE	ENABLE_SYS_EN_PCIE_HOT_RESET
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3320. PCIE_INTD_ENABLE_REG_SYS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ENABLE_SYS_EN_PCIE_PTM	R/W1S	0h	Enable Set for sys_en_pcie_ptm
23-15	RESERVED	R/W	X	
14	ENABLE_SYS_EN_PCIE_PWR_STATE_6	R/W1S	0h	Enable Set for sys_en_pcie_pwr_state_6
13	ENABLE_SYS_EN_PCIE_PWR_STATE_5	R/W1S	0h	Enable Set for sys_en_pcie_pwr_state_5
12	ENABLE_SYS_EN_PCIE_PWR_STATE_4	R/W1S	0h	Enable Set for sys_en_pcie_pwr_state_4
11	ENABLE_SYS_EN_PCIE_PWR_STATE_3	R/W1S	0h	Enable Set for sys_en_pcie_pwr_state_3
10	ENABLE_SYS_EN_PCIE_PWR_STATE_2	R/W1S	0h	Enable Set for sys_en_pcie_pwr_state_2

Table 9-3320. PCIE_INTD_ENABLE_REG_SYS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	ENABLE_SYS_EN_PCIE_PWR_STATE_1	R/W1S	0h	Enable Set for sys_en_pcie_pwr_state_1
8	ENABLE_SYS_EN_PCIE_PWR_STATE_0	R/W1S	0h	Enable Set for sys_en_pcie_pwr_state_0
7-2	RESERVED	R/W	X	
1	ENABLE_SYS_EN_PCIE_LINK_STATE	R/W1S	0h	Enable Set for sys_en_pcie_link_state
0	ENABLE_SYS_EN_PCIE_HOT_RESET	R/W1S	0h	Enable Set for sys_en_pcie_hot_reset

Table 9-3321. Register Call Summary for PCIE_INTD_ENABLE_REG_SYS_2

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_ENABLE_REG_SYS_2 Register \(Offset = 108h\) \[reset = X\]: \[0\]](#)

9.6.7 PCIE_INTD_ENABLE_CLR_REG_SYS_0 Register (Offset = 300h) [reset = X]

PCIE_INTD_ENABLE_CLR_REG_SYS_0 is shown in [Figure 9-1455](#) and described in [Table 9-3323](#).

Return to [Summary Table](#).

Enable Clear Register 0

Table 9-3322.
PCIE_INTD_ENABLE_CLR_REG_SYS_0 Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0300h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0300h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0300h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0300h

Figure 9-1455. PCIE_INTD_ENABLE_CLR_REG_SYS_0 Register

31	30	29	28	27	26	25	24
RESERVED							ENABLE_SYS_EN_PCIE_ASF_8_CLR
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
ENABLE_SYS_EN_PCIE_ASF_7_CLR	ENABLE_SYS_EN_PCIE_ASF_6_CLR	ENABLE_SYS_EN_PCIE_ASF_5_CLR	ENABLE_SYS_EN_PCIE_ASF_4_CLR	ENABLE_SYS_EN_PCIE_ASF_3_CLR	ENABLE_SYS_EN_PCIE_ASF_2_CLR	ENABLE_SYS_EN_PCIE_ASF_1_CLR	ENABLE_SYS_EN_PCIE_ASF_0_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RESERVED					ENABLE_SYS_EN_PCIE_ERR_OR_2_CLR	ENABLE_SYS_EN_PCIE_ERR_OR_1_CLR	ENABLE_SYS_EN_PCIE_ERR_OR_0_CLR
R/W-X					R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RESERVED				ENABLE_SYS_EN_PCIE_LEG_ACY_3_CLR	ENABLE_SYS_EN_PCIE_LEG_ACY_2_CLR	ENABLE_SYS_EN_PCIE_LEG_ACY_1_CLR	ENABLE_SYS_EN_PCIE_LEG_ACY_0_CLR
R/W-X				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3323. PCIE_INTD_ENABLE_CLR_REG_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ENABLE_SYS_EN_PCIE_ASF_8_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_8
23	ENABLE_SYS_EN_PCIE_ASF_7_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_7
22	ENABLE_SYS_EN_PCIE_ASF_6_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_6
21	ENABLE_SYS_EN_PCIE_ASF_5_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_5
20	ENABLE_SYS_EN_PCIE_ASF_4_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_4

Table 9-3323. PCIE_INTD_ENABLE_CLR_REG_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	ENABLE_SYS_EN_PCIE_ASF_3_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_3
18	ENABLE_SYS_EN_PCIE_ASF_2_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_2
17	ENABLE_SYS_EN_PCIE_ASF_1_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_1
16	ENABLE_SYS_EN_PCIE_ASF_0_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_asf_0
15-11	RESERVED	R/W	X	
10	ENABLE_SYS_EN_PCIE_ERROR_2_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_error_2
9	ENABLE_SYS_EN_PCIE_ERROR_1_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_error_1
8	ENABLE_SYS_EN_PCIE_ERROR_0_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_error_0
7-4	RESERVED	R/W	X	
3	ENABLE_SYS_EN_PCIE_LEGACY_3_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_legacy_3
2	ENABLE_SYS_EN_PCIE_LEGACY_2_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_legacy_2
1	ENABLE_SYS_EN_PCIE_LEGACY_1_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_legacy_1
0	ENABLE_SYS_EN_PCIE_LEGACY_0_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_legacy_0

Table 9-3324. Register Call Summary for PCIE_INTD_ENABLE_CLR_REG_SYS_0

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_ENABLE_CLR_REG_SYS_0 Register \(Offset = 300h\) \[reset = X\]: \[0\]](#)

9.6.8 PCIE_INTD_ENABLE_CLR_REG_SYS_1 Register (Offset = 304h) [reset = X]

PCIE_INTD_ENABLE_CLR_REG_SYS_1 is shown in Figure 9-1456 and described in Table 9-3326.

Return to [Summary Table](#).

Enable Clear Register 1

Table 9-3325.
PCIE_INTD_ENABLE_CLR_REG_SYS_1 Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0304h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0304h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0304h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0304h

Figure 9-1456. PCIE_INTD_ENABLE_CLR_REG_SYS_1 Register

31	30	29	28	27	26	25	24
RESERVED		ENABLE_SYS_EN_PCIE_DO_WNSTREAM_5_CLR	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_4_CLR	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_3_CLR	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_2_CLR	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_1_CLR	ENABLE_SYS_EN_PCIE_DO_WNSTREAM_0_CLR
R/W-X		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
RESERVED		ENABLE_SYS_EN_PCIE_FLR_21_CLR	ENABLE_SYS_EN_PCIE_FLR_20_CLR	ENABLE_SYS_EN_PCIE_FLR_19_CLR	ENABLE_SYS_EN_PCIE_FLR_18_CLR	ENABLE_SYS_EN_PCIE_FLR_17_CLR	ENABLE_SYS_EN_PCIE_FLR_16_CLR
R/W-X		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
ENABLE_SYS_EN_PCIE_FLR_15_CLR	ENABLE_SYS_EN_PCIE_FLR_14_CLR	ENABLE_SYS_EN_PCIE_FLR_13_CLR	ENABLE_SYS_EN_PCIE_FLR_12_CLR	ENABLE_SYS_EN_PCIE_FLR_11_CLR	ENABLE_SYS_EN_PCIE_FLR_10_CLR	ENABLE_SYS_EN_PCIE_FLR_9_CLR	ENABLE_SYS_EN_PCIE_FLR_8_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
ENABLE_SYS_EN_PCIE_FLR_7_CLR	ENABLE_SYS_EN_PCIE_FLR_6_CLR	ENABLE_SYS_EN_PCIE_FLR_5_CLR	ENABLE_SYS_EN_PCIE_FLR_4_CLR	ENABLE_SYS_EN_PCIE_FLR_3_CLR	ENABLE_SYS_EN_PCIE_FLR_2_CLR	ENABLE_SYS_EN_PCIE_FLR_1_CLR	ENABLE_SYS_EN_PCIE_FLR_0_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3326. PCIE_INTD_ENABLE_CLR_REG_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29	ENABLE_SYS_EN_PCIE_DOWNSTREAM_5_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_downstream_5
28	ENABLE_SYS_EN_PCIE_DOWNSTREAM_4_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_downstream_4
27	ENABLE_SYS_EN_PCIE_DOWNSTREAM_3_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_downstream_3
26	ENABLE_SYS_EN_PCIE_DOWNSTREAM_2_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_downstream_2

Table 9-3326. PCIE_INTD_ENABLE_CLR_REG_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	ENABLE_SYS_EN_PCIE_DOWNSTREAM_1_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_downstream_1
24	ENABLE_SYS_EN_PCIE_DOWNSTREAM_0_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_downstream_0
23-22	RESERVED	R/W	X	
21	ENABLE_SYS_EN_PCIE_FLR_21_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_21
20	ENABLE_SYS_EN_PCIE_FLR_20_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_20
19	ENABLE_SYS_EN_PCIE_FLR_19_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_19
18	ENABLE_SYS_EN_PCIE_FLR_18_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_18
17	ENABLE_SYS_EN_PCIE_FLR_17_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_17
16	ENABLE_SYS_EN_PCIE_FLR_16_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_16
15	ENABLE_SYS_EN_PCIE_FLR_15_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_15
14	ENABLE_SYS_EN_PCIE_FLR_14_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_14
13	ENABLE_SYS_EN_PCIE_FLR_13_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_13
12	ENABLE_SYS_EN_PCIE_FLR_12_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_12
11	ENABLE_SYS_EN_PCIE_FLR_11_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_11
10	ENABLE_SYS_EN_PCIE_FLR_10_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_10
9	ENABLE_SYS_EN_PCIE_FLR_9_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_9
8	ENABLE_SYS_EN_PCIE_FLR_8_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_8
7	ENABLE_SYS_EN_PCIE_FLR_7_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_7
6	ENABLE_SYS_EN_PCIE_FLR_6_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_6
5	ENABLE_SYS_EN_PCIE_FLR_5_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_5
4	ENABLE_SYS_EN_PCIE_FLR_4_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_4
3	ENABLE_SYS_EN_PCIE_FLR_3_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_3
2	ENABLE_SYS_EN_PCIE_FLR_2_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_2
1	ENABLE_SYS_EN_PCIE_FLR_1_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_1
0	ENABLE_SYS_EN_PCIE_FLR_0_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_flr_0

Table 9-3327. Register Call Summary for PCIE_INTD_ENABLE_CLR_REG_SYS_1

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_ENABLE_CLR_REG_SYS_1 Register \(Offset = 304h\) \[reset = X\]: \[0\]](#)

9.6.9 PCIE_INTD_ENABLE_CLR_REG_SYS_2 Register (Offset = 308h) [reset = X]

PCIE_INTD_ENABLE_CLR_REG_SYS_2 is shown in [Figure 9-1457](#) and described in [Table 9-3329](#).

Return to [Summary Table](#).

Enable Clear Register 2

Table 9-3328.
PCIE_INTD_ENABLE_CLR_REG_SYS_2 Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0308h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0308h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0308h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0308h

Figure 9-1457. PCIE_INTD_ENABLE_CLR_REG_SYS_2 Register

31	30	29	28	27	26	25	24
RESERVED							ENABLE_SYS_EN_PCIE_PTM_CLR
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	ENABLE_SYS_EN_PCIE_PWR_STATE_6_CLR	ENABLE_SYS_EN_PCIE_PWR_STATE_5_CLR	ENABLE_SYS_EN_PCIE_PWR_STATE_4_CLR	ENABLE_SYS_EN_PCIE_PWR_STATE_3_CLR	ENABLE_SYS_EN_PCIE_PWR_STATE_2_CLR	ENABLE_SYS_EN_PCIE_PWR_STATE_1_CLR	ENABLE_SYS_EN_PCIE_PWR_STATE_0_CLR
R/W-X	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RESERVED						ENABLE_SYS_EN_PCIE_LINK_STATE_CLR	ENABLE_SYS_EN_PCIE_HOT_RESET_CLR
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3329. PCIE_INTD_ENABLE_CLR_REG_SYS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ENABLE_SYS_EN_PCIE_PTM_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_ptm
23-15	RESERVED	R/W	X	
14	ENABLE_SYS_EN_PCIE_PWR_STATE_6_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_pwr_state_6
13	ENABLE_SYS_EN_PCIE_PWR_STATE_5_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_pwr_state_5
12	ENABLE_SYS_EN_PCIE_PWR_STATE_4_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_pwr_state_4
11	ENABLE_SYS_EN_PCIE_PWR_STATE_3_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_pwr_state_3

Table 9-3329. PCIE_INTD_ENABLE_CLR_REG_SYS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ENABLE_SYS_EN_PCIE_PWR_STATE_2_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_pwr_state_2
9	ENABLE_SYS_EN_PCIE_PWR_STATE_1_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_pwr_state_1
8	ENABLE_SYS_EN_PCIE_PWR_STATE_0_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_pwr_state_0
7-2	RESERVED	R/W	X	
1	ENABLE_SYS_EN_PCIE_LINK_STATE_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_link_state
0	ENABLE_SYS_EN_PCIE_HOT_RESET_CLR	R/W1C	0h	Enable Clear for sys_en_pcie_hot_reset

Table 9-3330. Register Call Summary for PCIE_INTD_ENABLE_CLR_REG_SYS_2

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_ENABLE_CLR_REG_SYS_2 Register \(Offset = 308h\) \[reset = X\]: \[0\]](#)

9.6.10 PCIE_INTD_STATUS_REG_SYS_0 Register (Offset = 500h) [reset = X]

PCIE_INTD_STATUS_REG_SYS_0 is shown in Figure 9-1458 and described in Table 9-3332.

Return to [Summary Table](#).

Status Register 0

**Table 9-3331. PCIE_INTD_STATUS_REG_SYS_0
Instances**

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0500h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0500h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0500h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0500h

Figure 9-1458. PCIE_INTD_STATUS_REG_SYS_0 Register

31	30	29	28	27	26	25	24
RESERVED							STATUS_SYS_PCIE_ASF_8
R/W-X							R/W1S-0h
23	22	21	20	19	18	17	16
STATUS_SYS_PCIE_ASF_7	STATUS_SYS_PCIE_ASF_6	STATUS_SYS_PCIE_ASF_5	STATUS_SYS_PCIE_ASF_4	STATUS_SYS_PCIE_ASF_3	STATUS_SYS_PCIE_ASF_2	STATUS_SYS_PCIE_ASF_1	STATUS_SYS_PCIE_ASF_0
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
RESERVED					STATUS_SYS_PCIE_ERROR_2	STATUS_SYS_PCIE_ERROR_1	STATUS_SYS_PCIE_ERROR_0
R/W-X					R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RESERVED				STATUS_SYS_PCIE_LEGACY_3	STATUS_SYS_PCIE_LEGACY_2	STATUS_SYS_PCIE_LEGACY_1	STATUS_SYS_PCIE_LEGACY_0
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3332. PCIE_INTD_STATUS_REG_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	STATUS_SYS_PCIE_ASF_8	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_8
23	STATUS_SYS_PCIE_ASF_7	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_7
22	STATUS_SYS_PCIE_ASF_6	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_6
21	STATUS_SYS_PCIE_ASF_5	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_5
20	STATUS_SYS_PCIE_ASF_4	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_4
19	STATUS_SYS_PCIE_ASF_3	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_3

Table 9-3332. PCIE_INTD_STATUS_REG_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	STATUS_SYS_PCIE_ASF_2	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_2
17	STATUS_SYS_PCIE_ASF_1	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_1
16	STATUS_SYS_PCIE_ASF_0	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_asf_0
15-11	RESERVED	R/W	X	
10	STATUS_SYS_PCIE_ERR_OR_2	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_error_2
9	STATUS_SYS_PCIE_ERR_OR_1	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_error_1
8	STATUS_SYS_PCIE_ERR_OR_0	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_error_0
7-4	RESERVED	R/W	X	
3	STATUS_SYS_PCIE_LEGACY_3	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_legacy_3
2	STATUS_SYS_PCIE_LEGACY_2	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_legacy_2
1	STATUS_SYS_PCIE_LEGACY_1	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_legacy_1
0	STATUS_SYS_PCIE_LEGACY_0	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_legacy_0

Table 9-3333. Register Call Summary for PCIE_INTD_STATUS_REG_SYS_0

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_STATUS_REG_SYS_0 Register \(Offset = 500h\) \[reset = X\]: \[0\]](#)

9.6.11 PCIE_INTD_STATUS_REG_SYS_1 Register (Offset = 504h) [reset = X]

PCIE_INTD_STATUS_REG_SYS_1 is shown in Figure 9-1459 and described in Table 9-3335.

Return to [Summary Table](#).

Status Register 1

**Table 9-3334. PCIE_INTD_STATUS_REG_SYS_1
Instances**

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0504h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0504h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0504h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0504h

Figure 9-1459. PCIE_INTD_STATUS_REG_SYS_1 Register

31	30	29	28	27	26	25	24
RESERVED		STATUS_SYS_PCIE_DOWNSTREAM_5	STATUS_SYS_PCIE_DOWNSTREAM_4	STATUS_SYS_PCIE_DOWNSTREAM_3	STATUS_SYS_PCIE_DOWNSTREAM_2	STATUS_SYS_PCIE_DOWNSTREAM_1	STATUS_SYS_PCIE_DOWNSTREAM_0
R/W-X		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
RESERVED		STATUS_SYS_PCIE_FLR_21	STATUS_SYS_PCIE_FLR_20	STATUS_SYS_PCIE_FLR_19	STATUS_SYS_PCIE_FLR_18	STATUS_SYS_PCIE_FLR_17	STATUS_SYS_PCIE_FLR_16
R/W-X		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
STATUS_SYS_PCIE_FLR_15	STATUS_SYS_PCIE_FLR_14	STATUS_SYS_PCIE_FLR_13	STATUS_SYS_PCIE_FLR_12	STATUS_SYS_PCIE_FLR_11	STATUS_SYS_PCIE_FLR_10	STATUS_SYS_PCIE_FLR_9	STATUS_SYS_PCIE_FLR_8
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
STATUS_SYS_PCIE_FLR_7	STATUS_SYS_PCIE_FLR_6	STATUS_SYS_PCIE_FLR_5	STATUS_SYS_PCIE_FLR_4	STATUS_SYS_PCIE_FLR_3	STATUS_SYS_PCIE_FLR_2	STATUS_SYS_PCIE_FLR_1	STATUS_SYS_PCIE_FLR_0
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3335. PCIE_INTD_STATUS_REG_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29	STATUS_SYS_PCIE_DOWNSTREAM_5	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_downstream_5
28	STATUS_SYS_PCIE_DOWNSTREAM_4	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_downstream_4
27	STATUS_SYS_PCIE_DOWNSTREAM_3	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_downstream_3
26	STATUS_SYS_PCIE_DOWNSTREAM_2	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_downstream_2
25	STATUS_SYS_PCIE_DOWNSTREAM_1	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_downstream_1
24	STATUS_SYS_PCIE_DOWNSTREAM_0	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_downstream_0
23-22	RESERVED	R/W	X	

Table 9-3335. PCIE_INTD_STATUS_REG_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	STATUS_SYS_PCIE_FLR_21	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_21
20	STATUS_SYS_PCIE_FLR_20	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_20
19	STATUS_SYS_PCIE_FLR_19	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_19
18	STATUS_SYS_PCIE_FLR_18	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_18
17	STATUS_SYS_PCIE_FLR_17	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_17
16	STATUS_SYS_PCIE_FLR_16	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_16
15	STATUS_SYS_PCIE_FLR_15	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_15
14	STATUS_SYS_PCIE_FLR_14	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_14
13	STATUS_SYS_PCIE_FLR_13	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_13
12	STATUS_SYS_PCIE_FLR_12	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_12
11	STATUS_SYS_PCIE_FLR_11	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_11
10	STATUS_SYS_PCIE_FLR_10	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_10
9	STATUS_SYS_PCIE_FLR_9	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_9
8	STATUS_SYS_PCIE_FLR_8	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_8
7	STATUS_SYS_PCIE_FLR_7	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_7
6	STATUS_SYS_PCIE_FLR_6	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_6
5	STATUS_SYS_PCIE_FLR_5	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_5
4	STATUS_SYS_PCIE_FLR_4	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_4
3	STATUS_SYS_PCIE_FLR_3	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_3
2	STATUS_SYS_PCIE_FLR_2	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_2
1	STATUS_SYS_PCIE_FLR_1	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_1
0	STATUS_SYS_PCIE_FLR_0	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_flr_0

Table 9-3336. Register Call Summary for PCIE_INTD_STATUS_REG_SYS_1

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_STATUS_REG_SYS_1 Register \(Offset = 504h\) \[reset = X\]: \[0\]](#)

9.6.12 PCIE_INTD_STATUS_REG_SYS_2 Register (Offset = 508h) [reset = X]

PCIE_INTD_STATUS_REG_SYS_2 is shown in Figure 9-1460 and described in Table 9-3338.

Return to [Summary Table](#).

Status Register 2

**Table 9-3337. PCIE_INTD_STATUS_REG_SYS_2
Instances**

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0508h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0508h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0508h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0508h

Figure 9-1460. PCIE_INTD_STATUS_REG_SYS_2 Register

31	30	29	28	27	26	25	24
RESERVED							STATUS_SYS_PCIE_PTM
R/W-X							R/W1S-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	STATUS_SYS_PCIE_PWR_ST_ATE_6	STATUS_SYS_PCIE_PWR_ST_ATE_5	STATUS_SYS_PCIE_PWR_ST_ATE_4	STATUS_SYS_PCIE_PWR_ST_ATE_3	STATUS_SYS_PCIE_PWR_ST_ATE_2	STATUS_SYS_PCIE_PWR_ST_ATE_1	STATUS_SYS_PCIE_PWR_ST_ATE_0
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
RESERVED						STATUS_SYS_PCIE_LINK_ST_ATE	STATUS_SYS_PCIE_HOT_RE_SET
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3338. PCIE_INTD_STATUS_REG_SYS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	STATUS_SYS_PCIE_PTM	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_ptm
23-15	RESERVED	R/W	X	
14	STATUS_SYS_PCIE_PWR_STATE_6	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_pwr_state_6
13	STATUS_SYS_PCIE_PWR_STATE_5	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_pwr_state_5
12	STATUS_SYS_PCIE_PWR_STATE_4	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_pwr_state_4
11	STATUS_SYS_PCIE_PWR_STATE_3	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_pwr_state_3
10	STATUS_SYS_PCIE_PWR_STATE_2	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_pwr_state_2

Table 9-3338. PCIE_INTD_STATUS_REG_SYS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	STATUS_SYS_PCIE_PWR_STATE_1	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_pwr_state_1
8	STATUS_SYS_PCIE_PWR_STATE_0	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_pwr_state_0
7-2	RESERVED	R/W	X	
1	STATUS_SYS_PCIE_LINK_STATE	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_link_state
0	STATUS_SYS_PCIE_HOT_RESET	R/W1S	0h	Status ,write 1 to set, for sys_en_pcie_hot_reset

Table 9-3339. Register Call Summary for PCIE_INTD_STATUS_REG_SYS_2

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_STATUS_REG_SYS_2 Register \(Offset = 508h\) \[reset = X\]: \[0\]](#)

9.6.13 PCIE_INTD_STATUS_CLR_REG_SYS_0 Register (Offset = 700h) [reset = X]

PCIE_INTD_STATUS_CLR_REG_SYS_0 is shown in Figure 9-1461 and described in Table 9-3341.

Return to [Summary Table](#).

Status Clear Register 0

Table 9-3340.
PCIE_INTD_STATUS_CLR_REG_SYS_0 Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0700h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0700h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0700h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0700h

Figure 9-1461. PCIE_INTD_STATUS_CLR_REG_SYS_0 Register

31	30	29	28	27	26	25	24
RESERVED							STATUS_SYS_PCIE_ASF_8_CLR
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
STATUS_SYS_PCIE_ASF_7_CLR	STATUS_SYS_PCIE_ASF_6_CLR	STATUS_SYS_PCIE_ASF_5_CLR	STATUS_SYS_PCIE_ASF_4_CLR	STATUS_SYS_PCIE_ASF_3_CLR	STATUS_SYS_PCIE_ASF_2_CLR	STATUS_SYS_PCIE_ASF_1_CLR	STATUS_SYS_PCIE_ASF_0_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RESERVED					STATUS_SYS_PCIE_ERROR_2_CLR	STATUS_SYS_PCIE_ERROR_1_CLR	STATUS_SYS_PCIE_ERROR_0_CLR
R/W-X					R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RESERVED				STATUS_SYS_PCIE_LEGACY_3_CLR	STATUS_SYS_PCIE_LEGACY_2_CLR	STATUS_SYS_PCIE_LEGACY_1_CLR	STATUS_SYS_PCIE_LEGACY_0_CLR
R/W-X				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3341. PCIE_INTD_STATUS_CLR_REG_SYS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	STATUS_SYS_PCIE_ASF_8_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_8
23	STATUS_SYS_PCIE_ASF_7_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_7
22	STATUS_SYS_PCIE_ASF_6_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_6
21	STATUS_SYS_PCIE_ASF_5_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_5
20	STATUS_SYS_PCIE_ASF_4_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_4

Table 9-3341. PCIE_INTD_STATUS_CLR_REG_SYS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	STATUS_SYS_PCIE_ASF_3_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_3
18	STATUS_SYS_PCIE_ASF_2_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_2
17	STATUS_SYS_PCIE_ASF_1_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_1
16	STATUS_SYS_PCIE_ASF_0_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_asf_0
15-11	RESERVED	R/W	X	
10	STATUS_SYS_PCIE_ERR_OR_2_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_error_2
9	STATUS_SYS_PCIE_ERR_OR_1_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_error_1
8	STATUS_SYS_PCIE_ERR_OR_0_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_error_0
7-4	RESERVED	R/W	X	
3	STATUS_SYS_PCIE_LEGACY_3_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_legacy_3
2	STATUS_SYS_PCIE_LEGACY_2_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_legacy_2
1	STATUS_SYS_PCIE_LEGACY_1_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_legacy_1
0	STATUS_SYS_PCIE_LEGACY_0_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_legacy_0

Table 9-3342. Register Call Summary for PCIE_INTD_STATUS_CLR_REG_SYS_0

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_STATUS_CLR_REG_SYS_0 Register \(Offset = 700h\) \[reset = X\]: \[0\]](#)

9.6.14 PCIE_INTD_STATUS_CLR_REG_SYS_1 Register (Offset = 704h) [reset = X]

PCIE_INTD_STATUS_CLR_REG_SYS_1 is shown in Figure 9-1462 and described in Table 9-3344.

Return to [Summary Table](#).

Status Clear Register 1

Table 9-3343.
PCIE_INTD_STATUS_CLR_REG_SYS_1 Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0704h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0704h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0704h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0704h

Figure 9-1462. PCIE_INTD_STATUS_CLR_REG_SYS_1 Register

31	30	29	28	27	26	25	24
RESERVED		STATUS_SYS_PCIE_DOWNS_TREAM_5_CLR	STATUS_SYS_PCIE_DOWNS_TREAM_4_CLR	STATUS_SYS_PCIE_DOWNS_TREAM_3_CLR	STATUS_SYS_PCIE_DOWNS_TREAM_2_CLR	STATUS_SYS_PCIE_DOWNS_TREAM_1_CLR	STATUS_SYS_PCIE_DOWNS_TREAM_0_CLR
R/W-X		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
RESERVED		STATUS_SYS_PCIE_FLR_21_CLR	STATUS_SYS_PCIE_FLR_20_CLR	STATUS_SYS_PCIE_FLR_19_CLR	STATUS_SYS_PCIE_FLR_18_CLR	STATUS_SYS_PCIE_FLR_17_CLR	STATUS_SYS_PCIE_FLR_16_CLR
R/W-X		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
STATUS_SYS_PCIE_FLR_15_CLR	STATUS_SYS_PCIE_FLR_14_CLR	STATUS_SYS_PCIE_FLR_13_CLR	STATUS_SYS_PCIE_FLR_12_CLR	STATUS_SYS_PCIE_FLR_11_CLR	STATUS_SYS_PCIE_FLR_10_CLR	STATUS_SYS_PCIE_FLR_9_CLR	STATUS_SYS_PCIE_FLR_8_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
STATUS_SYS_PCIE_FLR_7_CLR	STATUS_SYS_PCIE_FLR_6_CLR	STATUS_SYS_PCIE_FLR_5_CLR	STATUS_SYS_PCIE_FLR_4_CLR	STATUS_SYS_PCIE_FLR_3_CLR	STATUS_SYS_PCIE_FLR_2_CLR	STATUS_SYS_PCIE_FLR_1_CLR	STATUS_SYS_PCIE_FLR_0_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3344. PCIE_INTD_STATUS_CLR_REG_SYS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29	STATUS_SYS_PCIE_DOWNS_TREAM_5_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_downstream_5
28	STATUS_SYS_PCIE_DOWNS_TREAM_4_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_downstream_4
27	STATUS_SYS_PCIE_DOWNS_TREAM_3_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_downstream_3
26	STATUS_SYS_PCIE_DOWNS_TREAM_2_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_downstream_2
25	STATUS_SYS_PCIE_DOWNS_TREAM_1_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_downstream_1

Table 9-3344. PCIE_INTD_STATUS_CLR_REG_SYS_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	STATUS_SYS_PCIE_DO_WNSTREAM_0_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_downstream_0
23-22	RESERVED	R/W	X	
21	STATUS_SYS_PCIE_FLR_21_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_21
20	STATUS_SYS_PCIE_FLR_20_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_20
19	STATUS_SYS_PCIE_FLR_19_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_19
18	STATUS_SYS_PCIE_FLR_18_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_18
17	STATUS_SYS_PCIE_FLR_17_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_17
16	STATUS_SYS_PCIE_FLR_16_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_16
15	STATUS_SYS_PCIE_FLR_15_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_15
14	STATUS_SYS_PCIE_FLR_14_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_14
13	STATUS_SYS_PCIE_FLR_13_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_13
12	STATUS_SYS_PCIE_FLR_12_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_12
11	STATUS_SYS_PCIE_FLR_11_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_11
10	STATUS_SYS_PCIE_FLR_10_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_10
9	STATUS_SYS_PCIE_FLR_9_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_9
8	STATUS_SYS_PCIE_FLR_8_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_8
7	STATUS_SYS_PCIE_FLR_7_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_7
6	STATUS_SYS_PCIE_FLR_6_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_6
5	STATUS_SYS_PCIE_FLR_5_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_5
4	STATUS_SYS_PCIE_FLR_4_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_4
3	STATUS_SYS_PCIE_FLR_3_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_3
2	STATUS_SYS_PCIE_FLR_2_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_2
1	STATUS_SYS_PCIE_FLR_1_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_1
0	STATUS_SYS_PCIE_FLR_0_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_flr_0

Table 9-3345. Register Call Summary for PCIE_INTD_STATUS_CLR_REG_SYS_1

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_STATUS_CLR_REG_SYS_1 Register \(Offset = 704h\) \[reset = X\]: \[0\]](#)

9.6.15 PCIE_INTD_STATUS_CLR_REG_SYS_2 Register (Offset = 708h) [reset = X]

PCIE_INTD_STATUS_CLR_REG_SYS_2 is shown in Figure 9-1463 and described in Table 9-3347.

Return to [Summary Table](#).

Status Clear Register 2

Table 9-3346.
PCIE_INTD_STATUS_CLR_REG_SYS_2 Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0708h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0708h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0708h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0708h

Figure 9-1463. PCIE_INTD_STATUS_CLR_REG_SYS_2 Register

31	30	29	28	27	26	25	24
RESERVED							STATUS_SYS_PCIE_PTM_CLR
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	STATUS_SYS_PCIE_PWR_STATE_6_CLR	STATUS_SYS_PCIE_PWR_STATE_5_CLR	STATUS_SYS_PCIE_PWR_STATE_4_CLR	STATUS_SYS_PCIE_PWR_STATE_3_CLR	STATUS_SYS_PCIE_PWR_STATE_2_CLR	STATUS_SYS_PCIE_PWR_STATE_1_CLR	STATUS_SYS_PCIE_PWR_STATE_0_CLR
R/W-X	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RESERVED						STATUS_SYS_PCIE_LINK_STATE_CLR	STATUS_SYS_PCIE_HOT_RESET_CLR
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3347. PCIE_INTD_STATUS_CLR_REG_SYS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	STATUS_SYS_PCIE_PTM_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_ptm
23-15	RESERVED	R/W	X	
14	STATUS_SYS_PCIE_PWR_STATE_6_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_pwr_state_6
13	STATUS_SYS_PCIE_PWR_STATE_5_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_pwr_state_5
12	STATUS_SYS_PCIE_PWR_STATE_4_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_pwr_state_4
11	STATUS_SYS_PCIE_PWR_STATE_3_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_pwr_state_3

Table 9-3347. PCIE_INTD_STATUS_CLR_REG_SYS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	STATUS_SYS_PCIE_PWR_STATE_2_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_pwr_state_2
9	STATUS_SYS_PCIE_PWR_STATE_1_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_pwr_state_1
8	STATUS_SYS_PCIE_PWR_STATE_0_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_pwr_state_0
7-2	RESERVED	R/W	X	
1	STATUS_SYS_PCIE_LINK_STATE_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_link_state
0	STATUS_SYS_PCIE_HOT_RESET_CLR	R/W1C	0h	Status ,write 1 to clear, for sys_en_pcie_hot_reset

Table 9-3348. Register Call Summary for PCIE_INTD_STATUS_CLR_REG_SYS_2

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_STATUS_CLR_REG_SYS_2 Register \(Offset = 708h\) \[reset = X\]: \[0\]](#)

9.6.16 PCIE_INTD_INTR_VECTOR_REG_SYS Register (Offset = A80h) [reset = 0h]

PCIE_INTD_INTR_VECTOR_REG_SYS is shown in [Figure 9-1464](#) and described in [Table 9-3350](#).

Return to [Summary Table](#).

Interrupt Vector for sys

Table 9-3349. PCIE_INTD_INTR_VECTOR_REG_SYS Instances

Instance	Physical Address
PCIE0_CORE_PCIE_INTD_CFG_INTD_CFG	0290 0A80h
PCIE1_CORE_PCIE_INTD_CFG_INTD_CFG	0291 0A80h
PCIE2_CORE_PCIE_INTD_CFG_INTD_CFG	0292 0A80h
PCIE3_CORE_PCIE_INTD_CFG_INTD_CFG	0293 0A80h

Figure 9-1464. PCIE_INTD_INTR_VECTOR_REG_SYS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VECTOR_SYS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3350. PCIE_INTD_INTR_VECTOR_REG_SYS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INTR_VECTOR_SYS	R	0h	Interrupt Vector

Table 9-3351. Register Call Summary for PCIE_INTD_INTR_VECTOR_REG_SYS

PCIE_INTD Registers

- [PCIE_INTD Registers: \[0\] \[1\]](#)
- [PCIE_INTD_INTR_VECTOR_REG_SYS Register \(Offset = A80h\) \[reset = 0h\]: \[0\]](#)

9.7 PCIe_CPTS Registers

Table 9-3353 lists the memory-mapped registers for the PCIe_CPTS. All register offset addresses not listed in Table 9-3353 should be considered as reserved locations and the register contents should not be modified.

Table 9-3352. PCIe_CPTS Instances

Instance	Base Address
PCIE0_CORE_CPTS_CFG_CPTS_VBUSP	0290 6000h
PCIE1_CORE_CPTS_CFG_CPTS_VBUSP	0291 6000h
PCIE2_CORE_CPTS_CFG_CPTS_VBUSP	0292 6000h
PCIE3_CORE_CPTS_CFG_CPTS_VBUSP	0293 6000h

Table 9-3353. PCIe_CPTS Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_CP TS_CFG_CPTS_V BUSP Physical Address	PCIE1_CORE_CP TS_CFG_CPTS_ VBUSP Physical Address
0h	PCIE_CPTS_IDVER_REG		0290 6000h	0291 6000h
4h	PCIE_CPTS_CONTROL_REG		0290 6004h	0291 6004h
8h	PCIE_CPTS_RFTCLK_SEL_REG		0290 6008h	0291 6008h
Ch	PCIE_CPTS_TS_PUSH_REG		0290 600Ch	0291 600Ch
10h	PCIE_CPTS_TS_LOAD_VAL_REG		0290 6010h	0291 6010h
14h	PCIE_CPTS_TS_LOAD_EN_REG		0290 6014h	0291 6014h
18h	PCIE_CPTS_TS_COMP_VAL_REG		0290 6018h	0291 6018h
1Ch	PCIE_CPTS_TS_COMP_LEN_REG		0290 601Ch	0291 601Ch
20h	PCIE_CPTS_INTSTAT_RAW_REG		0290 6020h	0291 6020h
24h	PCIE_CPTS_INTSTAT_MASKED_REG		0290 6024h	0291 6024h
28h	PCIE_CPTS_INT_ENABLE_REG		0290 6028h	0291 6028h
2Ch	PCIE_CPTS_TS_COMP_NUDGE_REG		0290 602Ch	0291 602Ch
30h	PCIE_CPTS_EVENT_POP_REG		0290 6030h	0291 6030h
34h	PCIE_CPTS_EVENT_0_REG		0290 6034h	0291 6034h
38h	PCIE_CPTS_EVENT_1_REG		0290 6038h	0291 6038h
3Ch	PCIE_CPTS_EVENT_2_REG		0290 603Ch	0291 603Ch
40h	PCIE_CPTS_EVENT_3_REG		0290 6040h	0291 6040h
44h	PCIE_CPTS_TS_LOAD_HIGH_VAL_REG		0290 6044h	0291 6044h
48h	PCIE_CPTS_TS_COMP_HIGH_VAL_REG		0290 6048h	0291 6048h
4Ch	PCIE_CPTS_TS_ADD_VAL_REG		0290 604Ch	0291 604Ch
50h	PCIE_CPTS_TS_PPM_LOW_VAL_REG		0290 6050h	0291 6050h
54h	PCIE_CPTS_TS_PPM_HIGH_VAL_REG		0290 6054h	0291 6054h
58h	PCIE_CPTS_TS_NUDGE_VAL_REG		0290 6058h	0291 6058h
E0h	PCIE_CPTS_COMP_LOW_REG		0290 60E0h	0291 60E0h
E4h	PCIE_CPTS_COMP_HIGH_REG		0290 60E4h	0291 60E4h
E8h	PCIE_CPTS_CONTROL_REG		0290 60E8h	0291 60E8h
ECh	PCIE_CPTS_LENGTH_REG		0290 60ECh	0291 60ECh
F0h	PCIE_CPTS_PPM_LOW_REG		0290 60F0h	0291 60F0h
F4h	PCIE_CPTS_PPM_HIGH_REG		0290 60F4h	0291 60F4h
F8h	PCIE_CPTS_NUDGE_REG		0290 60F8h	0291 60F8h
200h	PCIE_CPTS_COMP_LOW_REG		0290 6200h	0291 6200h
204h	PCIE_CPTS_COMP_HIGH_REG		0290 6204h	0291 6204h
208h	PCIE_CPTS_CONTROL_REG		0290 6208h	0291 6208h
20Ch	PCIE_CPTS_LENGTH_REG		0290 620Ch	0291 620Ch

Table 9-3353. PCIE_CPTS Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_CP TS_CFG_CPTS_V BUSP Physical Address	PCIE1_CORE_CP TS_CFG_CPTS_ VBUSP Physical Address
210h	PCIE_CPTS_PPM_LOW_REG		0290 6210h	0291 6210h
214h	PCIE_CPTS_PPM_HIGH_REG		0290 6214h	0291 6214h
218h	PCIE_CPTS_NUDGE_REG		0290 6218h	0291 6218h

Table 9-3354. PCIE_CPTS Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_CP TS_CFG_CPTS_V BUSP Physical Address	PCIE3_CORE_CP TS_CFG_CPTS_ VBUSP Physical Address
0h	PCIE_CPTS_IDVER_REG		0292 6000h	0293 6000h
4h	PCIE_CPTS_CONTROL_REG		0292 6004h	0293 6004h
8h	PCIE_CPTS_RFTCLK_SEL_REG		0292 6008h	0293 6008h
Ch	PCIE_CPTS_TS_PUSH_REG		0292 600Ch	0293 600Ch
10h	PCIE_CPTS_TS_LOAD_VAL_REG		0292 6010h	0293 6010h
14h	PCIE_CPTS_TS_LOAD_EN_REG		0292 6014h	0293 6014h
18h	PCIE_CPTS_TS_COMP_VAL_REG		0292 6018h	0293 6018h
1Ch	PCIE_CPTS_TS_COMP_LEN_REG		0292 601Ch	0293 601Ch
20h	PCIE_CPTS_INTSTAT_RAW_REG		0292 6020h	0293 6020h
24h	PCIE_CPTS_INTSTAT_MASKED_REG		0292 6024h	0293 6024h
28h	PCIE_CPTS_INT_ENABLE_REG		0292 6028h	0293 6028h
2Ch	PCIE_CPTS_TS_COMP_NUDGE_REG		0292 602Ch	0293 602Ch
30h	PCIE_CPTS_EVENT_POP_REG		0292 6030h	0293 6030h
34h	PCIE_CPTS_EVENT_0_REG		0292 6034h	0293 6034h
38h	PCIE_CPTS_EVENT_1_REG		0292 6038h	0293 6038h
3Ch	PCIE_CPTS_EVENT_2_REG		0292 603Ch	0293 603Ch
40h	PCIE_CPTS_EVENT_3_REG		0292 6040h	0293 6040h
44h	PCIE_CPTS_TS_LOAD_HIGH_VAL_REG		0292 6044h	0293 6044h
48h	PCIE_CPTS_TS_COMP_HIGH_VAL_REG		0292 6048h	0293 6048h
4Ch	PCIE_CPTS_TS_ADD_VAL_REG		0292 604Ch	0293 604Ch
50h	PCIE_CPTS_TS_PPM_LOW_VAL_REG		0292 6050h	0293 6050h
54h	PCIE_CPTS_TS_PPM_HIGH_VAL_REG		0292 6054h	0293 6054h
58h	PCIE_CPTS_TS_NUDGE_VAL_REG		0292 6058h	0293 6058h
E0h	PCIE_CPTS_COMP_LOW_REG		0292 60E0h	0293 60E0h
E4h	PCIE_CPTS_COMP_HIGH_REG		0292 60E4h	0293 60E4h
E8h	PCIE_CPTS_CONTROL_REG		0292 60E8h	0293 60E8h
ECh	PCIE_CPTS_LENGTH_REG		0292 60ECh	0293 60ECh
F0h	PCIE_CPTS_PPM_LOW_REG		0292 60F0h	0293 60F0h
F4h	PCIE_CPTS_PPM_HIGH_REG		0292 60F4h	0293 60F4h
F8h	PCIE_CPTS_NUDGE_REG		0292 60F8h	0293 60F8h
200h	PCIE_CPTS_COMP_LOW_REG		0292 6200h	0293 6200h
204h	PCIE_CPTS_COMP_HIGH_REG		0292 6204h	0293 6204h
208h	PCIE_CPTS_CONTROL_REG		0292 6208h	0293 6208h
20Ch	PCIE_CPTS_LENGTH_REG		0292 620Ch	0293 620Ch
210h	PCIE_CPTS_PPM_LOW_REG		0292 6210h	0293 6210h
214h	PCIE_CPTS_PPM_HIGH_REG		0292 6214h	0293 6214h

Table 9-3354. PCIe_CPTS Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_CP TS_CFG_CPTS_V BUSP Physical Address	PCIE3_CORE_CP TS_CFG_CPTS_ VBUSP Physical Address
218h	PCIe_CPTS_NUDGE_REG		0292 6218h	0293 6218h

9.7.1 PCIE_CPTS_IDVER_REG Register (Offset = 0h) [reset = 4E8A010Ah]

PCIE_CPTS_IDVER_REG is shown in Figure 9-1465 and described in Table 9-3356.

Return to [Summary Table](#).

Identification and Version Register

Table 9-3355. PCIE_CPTS_IDVER_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6000h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6000h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6000h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6000h

Figure 9-1465. PCIE_CPTS_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R-4E8Ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER					MINOR_VER					
R-0h					R-1h					R-Ah					

LEGEND: R = Read Only; -n = value after reset

Table 9-3356. PCIE_CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_IDENT	R	4E8Ah	Identification value
15-11	RTL_VER	R	0h	RTL version value
10-8	MAJOR_VER	R	1h	Major version value
7-0	MINOR_VER	R	Ah	Minor version value

Table 9-3357. Register Call Summary for PCIE_CPTS_IDVER_REG

PCIE_CPTS Registers

- [PCIE_CPTS_IDVER_REG Register \(Offset = 0h\) \[reset = 4E8A010Ah\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.2 PCIE_CPTS_CONTROL_REG Register (Offset = 4h) [reset = X]

PCIE_CPTS_CONTROL_REG is shown in Figure 9-1466 and described in Table 9-3359.

Return to [Summary Table](#).

Time Sync Control Register

**Table 9-3358. PCIE_CPTS_CONTROL_REG
Instances**

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6004h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6004h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6004h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6004h

Figure 9-1466. PCIE_CPTS_CONTROL_REG Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED							TS_RX_NO_EV ENT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
HW8_TS_PUS H_EN	HW7_TS_PUS H_EN	HW6_TS_PUS H_EN	HW5_TS_PUS H_EN	HW4_TS_PUS H_EN	HW3_TS_PUS H_EN	HW2_TS_PUS H_EN	HW1_TS_PUS H_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TS_PPM_DIR	TS_COMP_TO G	MODE	SEQUENCE_E N	TSTAMP_EN	TS_COMP_PO LARITY	INT_TEST	CPTS_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3359. PCIE_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TS_SYNC_SEL	R/W	0h	TS_SYNC output timestamp counter bit select
27-17	RESERVED	R/W	X	
16	TS_RX_NO_EVENT	R/W	0h	Receive Produces no Events
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable

Table 9-3359. PCIE_CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TS_PPM_DIR	R/W	0h	Timestamp PPM Direction
6	TS_COMP_TOG	R/W	0h	Timestamp Compare Toggle mode: 0=TS_COMP is in non-toggle mode, 1=TS_COMP is in toggle mode
5	MODE	R/W	0h	Timestamp mode
4	SEQUENCE_EN	R/W	0h	Sequence Enable
3	TSTAMP_EN	R/W	0h	Host Receive Timestamp Enable
2	TS_COMP_POLARITY	R/W	1h	TS_COMP polarity
1	INT_TEST	R/W	0h	Interrupt test
0	CPTS_EN	R/W	0h	Time sync enable

Table 9-3360. Register Call Summary for PCIE_CPTS_CONTROL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_CONTROL_REG Register \(Offset = E8h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_CONTROL_REG Register \(Offset = 208h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_CONTROL_REG Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\] \[4\] \[5\]](#)

9.7.3 PCIE_CPTS_RFTCLK_SEL_REG Register (Offset = 8h) [reset = X]

PCIE_CPTS_RFTCLK_SEL_REG is shown in [Figure 9-1467](#) and described in [Table 9-3362](#).

Return to [Summary Table](#).

RFTCLK Select Register

Table 9-3361. PCIE_CPTS_RFTCLK_SEL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6008h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6008h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6008h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6008h

Figure 9-1467. PCIE_CPTS_RFTCLK_SEL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											RFTCLK_SEL				
R/W-X											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3362. PCIE_CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	RFTCLK_SEL	R/W	0h	Reference clock select

Table 9-3363. Register Call Summary for PCIE_CPTS_RFTCLK_SEL_REG

Peripheral Component Interconnect Express (PCIe) Subsystem
PCIE_CPTS Registers <ul style="list-style-type: none"> • PCIE_CPTS_RFTCLK_SEL_REG Register (Offset = 8h) [reset = X]: [0] • PCIE_CPTS Registers: [0] [1]
PCIe Subsystem Functional Description <ul style="list-style-type: none"> • PCIe Subsystem Precision Time Measurement Support: [0]

9.7.4 PCIE_CPTS_TS_PUSH_REG Register (Offset = Ch) [reset = X]

PCIE_CPTS_TS_PUSH_REG is shown in [Figure 9-1468](#) and described in [Table 9-3365](#).

Return to [Summary Table](#).

Time Stamp Event Push Register

Table 9-3364. PCIE_CPTS_TS_PUSH_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 600Ch
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 600Ch
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 600Ch
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 600Ch

Figure 9-1468. PCIE_CPTS_TS_PUSH_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 9-3365. PCIE_CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_PUSH	W	0h	Time stamp event push

Table 9-3366. Register Call Summary for PCIE_CPTS_TS_PUSH_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_PUSH_REG Register \(Offset = Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.5 PCIE_CPTS_TS_LOAD_VAL_REG Register (Offset = 10h) [reset = 0h]

PCIE_CPTS_TS_LOAD_VAL_REG is shown in [Figure 9-1469](#) and described in [Table 9-3368](#).

[Return to Summary Table.](#)

Time Stamp Load Low Value Register

**Table 9-3367. PCIE_CPTS_TS_LOAD_VAL_REG
Instances**

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6010h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6010h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6010h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6010h

Figure 9-1469. PCIE_CPTS_TS_LOAD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3368. PCIE_CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	Time stamp load low value

Table 9-3369. Register Call Summary for PCIE_CPTS_TS_LOAD_VAL_REG

PCIE_CPTS Registers
<ul style="list-style-type: none"> PCIE_CPTS_TS_LOAD_VAL_REG Register (Offset = 10h) [reset = 0h]: [0] PCIE_CPTS Registers: [0] [1]

9.7.6 PCIE_CPTS_TS_LOAD_EN_REG Register (Offset = 14h) [reset = X]

PCIE_CPTS_TS_LOAD_EN_REG is shown in [Figure 9-1470](#) and described in [Table 9-3371](#).

Return to [Summary Table](#).

Time Stamp Load Enable Register

Table 9-3370. PCIE_CPTS_TS_LOAD_EN_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6014h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6014h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6014h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6014h

Figure 9-1470. PCIE_CPTS_TS_LOAD_EN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 9-3371. PCIE_CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_LOAD_EN	W	0h	Time stamp load enable

Table 9-3372. Register Call Summary for PCIE_CPTS_TS_LOAD_EN_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_LOAD_EN_REG Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.7 PCIE_CPTS_TS_COMP_VAL_REG Register (Offset = 18h) [reset = 0h]

PCIE_CPTS_TS_COMP_VAL_REG is shown in [Figure 9-1471](#) and described in [Table 9-3374](#).

Return to [Summary Table](#).

Time Stamp Comparison Low Value Register

Table 9-3373. PCIE_CPTS_TS_COMP_VAL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6018h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6018h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6018h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6018h

Figure 9-1471. PCIE_CPTS_TS_COMP_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3374. PCIE_CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_VAL	R/W	0h	Time stamp comparison low value

Table 9-3375. Register Call Summary for PCIE_CPTS_TS_COMP_VAL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_COMP_VAL_REG Register \(Offset = 18h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.8 PCIE_CPTS_TS_COMP_LEN_REG Register (Offset = 1Ch) [reset = 0h]

PCIE_CPTS_TS_COMP_LEN_REG is shown in [Figure 9-1472](#) and described in [Table 9-3377](#).

Return to [Summary Table](#).

Time Stamp Comparison Length Register

Table 9-3376. PCIE_CPTS_TS_COMP_LEN_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 601Ch
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 601Ch
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 601Ch
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 601Ch

Figure 9-1472. PCIE_CPTS_TS_COMP_LEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3377. PCIE_CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_LENGTH	R/W	0h	Time stamp comparison length

Table 9-3378. Register Call Summary for PCIE_CPTS_TS_COMP_LEN_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_COMP_LEN_REG Register \(Offset = 1Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.9 PCIE_CPTS_INTSTAT_RAW_REG Register (Offset = 20h) [reset = X]

PCIE_CPTS_INTSTAT_RAW_REG is shown in [Figure 9-1473](#) and described in [Table 9-3380](#).

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Interrupt Status Register Raw

Table 9-3379. PCIE_CPTS_INTSTAT_RAW_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6020h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6020h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6020h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6020h

Figure 9-1473. PCIE_CPTS_INTSTAT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_RAW
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3380. PCIE_CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable)

Table 9-3381. Register Call Summary for PCIE_CPTS_INTSTAT_RAW_REG

PCIE_CPTS Registers
<ul style="list-style-type: none"> PCIE_CPTS_INTSTAT_RAW_REG Register (Offset = 20h) [reset = X]: [0] PCIE_CPTS Registers: [0] [1]

9.7.10 PCIE_CPTS_INTSTAT_MASKED_REG Register (Offset = 24h) [reset = X]

PCIE_CPTS_INTSTAT_MASKED_REG is shown in [Figure 9-1474](#) and described in [Table 9-3383](#).

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Interrupt Status Register Masked

Table 9-3382. PCIE_CPTS_INTSTAT_MASKED_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6024h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6024h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6024h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6024h

Figure 9-1474. PCIE_CPTS_INTSTAT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 9-3383. PCIE_CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

Table 9-3384. Register Call Summary for PCIE_CPTS_INTSTAT_MASKED_REG

PCIE_CPTS Registers

- [PCIE_CPTS_INTSTAT_MASKED_REG Register \(Offset = 24h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.11 PCIE_CPTS_INT_ENABLE_REG Register (Offset = 28h) [reset = X]

PCIE_CPTS_INT_ENABLE_REG is shown in [Figure 9-1475](#) and described in [Table 9-3386](#).

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Interrupt Enable Register

**Table 9-3385. PCIE_CPTS_INT_ENABLE_REG
Instances**

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6028h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6028h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6028h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6028h

Figure 9-1475. PCIE_CPTS_INT_ENABLE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3386. PCIE_CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

Table 9-3387. Register Call Summary for PCIE_CPTS_INT_ENABLE_REG

PCIE_CPTS Registers

- [PCIE_CPTS_INT_ENABLE_REG Register \(Offset = 28h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.12 PCIE_CPTS_TS_COMP_NUDGE_REG Register (Offset = 2Ch) [reset = X]

PCIE_CPTS_TS_COMP_NUDGE_REG is shown in [Figure 9-1476](#) and described in [Table 9-3389](#).

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Time Stamp Comparison Nudge Register

Table 9-3388. PCIE_CPTS_TS_COMP_NUDGE_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 602Ch
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 602Ch
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 602Ch
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 602Ch

Figure 9-1476. PCIE_CPTS_TS_COMP_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3389. PCIE_CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	This 2s complement number is added to the ts_comp_length value to increase or decrease the TS_COMP length by the nudge amount

Table 9-3390. Register Call Summary for PCIE_CPTS_TS_COMP_NUDGE_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_COMP_NUDGE_REG Register \(Offset = 2Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.13 PCIE_CPTS_EVENT_POP_REG Register (Offset = 30h) [reset = X]

PCIE_CPTS_EVENT_POP_REG is shown in [Figure 9-1477](#) and described in [Table 9-3392](#).

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Event Pop Register

**Table 9-3391. PCIE_CPTS_EVENT_POP_REG
Instances**

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6030h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6030h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6030h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6030h

Figure 9-1477. PCIE_CPTS_EVENT_POP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 9-3392. PCIE_CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	EVENT_POP	W	0h	Event pop

Table 9-3393. Register Call Summary for PCIE_CPTS_EVENT_POP_REG

PCIE_CPTS Registers

- [PCIE_CPTS_EVENT_POP_REG Register \(Offset = 30h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.14 PCIE_CPTS_EVENT_0_REG Register (Offset = 34h) [reset = 0h]

PCIE_CPTS_EVENT_0_REG is shown in [Figure 9-1478](#) and described in [Table 9-3395](#).

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Event 0 Register

Table 9-3394. PCIE_CPTS_EVENT_0_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6034h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6034h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6034h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6034h

Figure 9-1478. PCIE_CPTS_EVENT_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3395. PCIE_CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp

Table 9-3396. Register Call Summary for PCIE_CPTS_EVENT_0_REG

PCIE_CPTS Registers
<ul style="list-style-type: none"> PCIE_CPTS_EVENT_0_REG Register (Offset = 34h) [reset = 0h]: [0] PCIE_CPTS Registers: [0] [1]

9.7.15 PCIE_CPTS_EVENT_1_REG Register (Offset = 38h) [reset = X]

PCIE_CPTS_EVENT_1_REG is shown in [Figure 9-1479](#) and described in [Table 9-3398](#).

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Event 1 Register

Table 9-3397. PCIE_CPTS_EVENT_1_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6038h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6038h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6038h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6038h

Figure 9-1479. PCIE_CPTS_EVENT_1_REG Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
R-X		R-0h	R-0h				
23	22	21	20	19	18	17	16
EVENT_TYPE				MESSAGE_TYPE			
R-0h				R-0h			
15	14	13	12	11	10	9	8
SEQUENCE_ID							
R-0h							
7	6	5	4	3	2	1	0
SEQUENCE_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 9-3398. PCIE_CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29	PREMPT_QUEUE	R	0h	Preempt QUEUE
28-24	PORT_NUMBER	R	0h	Port number
23-20	EVENT_TYPE	R	0h	Event type
19-16	MESSAGE_TYPE	R	0h	Message type
15-0	SEQUENCE_ID	R	0h	Sequence ID

Table 9-3399. Register Call Summary for PCIE_CPTS_EVENT_1_REG

PCIE_CPTS Registers

- [PCIE_CPTS_EVENT_1_REG Register \(Offset = 38h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.16 PCIE_CPTS_EVENT_2_REG Register (Offset = 3Ch) [reset = X]

PCIE_CPTS_EVENT_2_REG is shown in [Figure 9-1480](#) and described in [Table 9-3401](#).

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Event 2 Register

Table 9-3400. PCIE_CPTS_EVENT_2_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 603Ch
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 603Ch
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 603Ch
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 603Ch

Figure 9-1480. PCIE_CPTS_EVENT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DOMAIN																	
R-X														R-0h																	

LEGEND: R = Read Only; -n = value after reset

Table 9-3401. PCIE_CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	DOMAIN	R	0h	Domain

Table 9-3402. Register Call Summary for PCIE_CPTS_EVENT_2_REG

PCIE_CPTS Registers

- [PCIE_CPTS_EVENT_2_REG Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.17 PCIE_CPTS_EVENT_3_REG Register (Offset = 40h) [reset = 0h]

PCIE_CPTS_EVENT_3_REG is shown in [Figure 9-1481](#) and described in [Table 9-3404](#).

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Event 3 Register

Table 9-3403. PCIE_CPTS_EVENT_3_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6040h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6040h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6040h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6040h

Figure 9-1481. PCIE_CPTS_EVENT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3404. PCIE_CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp

Table 9-3405. Register Call Summary for PCIE_CPTS_EVENT_3_REG

PCIE_CPTS Registers
<ul style="list-style-type: none"> PCIE_CPTS_EVENT_3_REG Register (Offset = 40h) [reset = 0h]: [0] PCIE_CPTS Registers: [0] [1]

9.7.18 PCIE_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 44h) [reset = 0h]

PCIE_CPTS_TS_LOAD_HIGH_VAL_REG is shown in [Figure 9-1482](#) and described in [Table 9-3407](#).

Return to [Summary Table](#).

Time Stamp Load High Value Register

Table 9-3406.
PCIE_CPTS_TS_LOAD_HIGH_VAL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6044h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6044h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6044h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6044h

Figure 9-1482. PCIE_CPTS_TS_LOAD_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3407. PCIE_CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	Time stamp load high value

Table 9-3408. Register Call Summary for PCIE_CPTS_TS_LOAD_HIGH_VAL_REG

PCIE_CPTS Registers	
•	PCIE_CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 44h) [reset = 0h]: [0]
•	PCIE_CPTS Registers: [0] [1]

9.7.19 PCIE_CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 48h) [reset = 0h]

PCIE_CPTS_TS_COMP_HIGH_VAL_REG is shown in [Figure 9-1483](#) and described in [Table 9-3410](#).

Return to [Summary Table](#).

Time Stamp Comparison High Value Register

Table 9-3409.
PCIE_CPTS_TS_COMP_HIGH_VAL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6048h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6048h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6048h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6048h

Figure 9-1483. PCIE_CPTS_TS_COMP_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3410. PCIE_CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_HIGH_VAL	R/W	0h	Time stamp comparison high value

Table 9-3411. Register Call Summary for PCIE_CPTS_TS_COMP_HIGH_VAL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_COMP_HIGH_VAL_REG Register \(Offset = 48h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.20 PCIE_CPTS_TS_ADD_VAL_REG Register (Offset = 4Ch) [reset = X]

PCIE_CPTS_TS_ADD_VAL_REG is shown in [Figure 9-1484](#) and described in [Table 9-3413](#).

Return to [Summary Table](#).

TS Add Value Register

Table 9-3412. PCIE_CPTS_TS_ADD_VAL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 604Ch
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 604Ch
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 604Ch
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 604Ch

Figure 9-1484. PCIE_CPTS_TS_ADD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ADD_VAL		
R/W-X													R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3413. PCIE_CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	ADD_VAL	R/W	0h	Add Value

Table 9-3414. Register Call Summary for PCIE_CPTS_TS_ADD_VAL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_ADD_VAL_REG Register \(Offset = 4Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.21 PCIE_CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 50h) [reset = 0h]

PCIE_CPTS_TS_PPM_LOW_VAL_REG is shown in [Figure 9-1485](#) and described in [Table 9-3416](#).

Return to [Summary Table](#).

Time Stamp PPM Low Value Register

Table 9-3415. PCIE_CPTS_TS_PPM_LOW_VAL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6050h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6050h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6050h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6050h

Figure 9-1485. PCIE_CPTS_TS_PPM_LOW_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3416. PCIE_CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_PPM_LOW_VAL	R/W	0h	Time stamp PPM Low value

Table 9-3417. Register Call Summary for PCIE_CPTS_TS_PPM_LOW_VAL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_PPM_LOW_VAL_REG Register \(Offset = 50h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.22 PCIE_CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 54h) [reset = X]

PCIE_CPTS_TS_PPM_HIGH_VAL_REG is shown in [Figure 9-1486](#) and described in [Table 9-3419](#).

Return to [Summary Table](#).

Time Stamp PPM High Value Register

Table 9-3418. PCIE_CPTS_TS_PPM_HIGH_VAL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6054h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6054h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6054h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6054h

Figure 9-1486. PCIE_CPTS_TS_PPM_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TS_PPM_HIGH_VAL									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3419. PCIE_CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TS_PPM_HIGH_VAL	R/W	0h	Time stamp PPM High value

Table 9-3420. Register Call Summary for PCIE_CPTS_TS_PPM_HIGH_VAL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_PPM_HIGH_VAL_REG Register \(Offset = 54h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.23 PCIE_CPTS_TS_NUDGE_VAL_REG Register (Offset = 58h) [reset = X]

PCIE_CPTS_TS_NUDGE_VAL_REG is shown in [Figure 9-1487](#) and described in [Table 9-3422](#).

Return to [Summary Table](#).

Time Stamp Nudge Value Register

Table 9-3421. PCIE_CPTS_TS_NUDGE_VAL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6058h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6058h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6058h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6058h

Figure 9-1487. PCIE_CPTS_TS_NUDGE_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_NUDGE_VAL							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3422. PCIE_CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge value

Table 9-3423. Register Call Summary for PCIE_CPTS_TS_NUDGE_VAL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_TS_NUDGE_VAL_REG Register \(Offset = 58h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\]](#)

9.7.24 PCIE_CPTS_COMP_LOW_REG Register (Offset = E0h) [reset = 0h]

PCIE_CPTS_COMP_LOW_REG is shown in [Figure 9-1488](#) and described in [Table 9-3425](#).

Return to [Summary Table](#).

Time Stamp Generate Function Comparison Low Value

Table 9-3424. PCIE_CPTS_COMP_LOW_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 60E0h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 60E0h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 60E0h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 60E0h

Figure 9-1488. PCIE_CPTS_COMP_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3425. PCIE_CPTS_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value

Table 9-3426. Register Call Summary for PCIE_CPTS_COMP_LOW_REG

PCIE_CPTS Registers

- [PCIE_CPTS_COMP_LOW_REG Register \(Offset = E0h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS_COMP_LOW_REG Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\]](#)

9.7.25 PCIE_CPTS_COMP_HIGH_REG Register (Offset = E4h) [reset = 0h]

PCIE_CPTS_COMP_HIGH_REG is shown in [Figure 9-1489](#) and described in [Table 9-3428](#).

Return to [Summary Table](#).

Time Stamp Generate Function Comparison high Value

**Table 9-3427. PCIE_CPTS_COMP_HIGH_REG
Instances**

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 60E4h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 60E4h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 60E4h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 60E4h

Figure 9-1489. PCIE_CPTS_COMP_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3428. PCIE_CPTS_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value

Table 9-3429. Register Call Summary for PCIE_CPTS_COMP_HIGH_REG

PCIE_CPTS Registers

- [PCIE_CPTS_COMP_HIGH_REG Register \(Offset = 204h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS_COMP_HIGH_REG Register \(Offset = E4h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\]](#)

9.7.26 PCIE_CPTS_CONTROL_REG Register (Offset = E8h) [reset = X]

PCIE_CPTS_CONTROL_REG is shown in Figure 9-1490 and described in Table 9-3431.

Return to [Summary Table](#).

Time Stamp Generate Function Control

Table 9-3430. PCIE_CPTS_CONTROL_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 60E8h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 60E8h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 60E8h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 60E8h

Figure 9-1490. PCIE_CPTS_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3431. PCIE_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert
0	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction

Table 9-3432. Register Call Summary for PCIE_CPTS_CONTROL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_CONTROL_REG Register \(Offset = E8h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_CONTROL_REG Register \(Offset = 208h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_CONTROL_REG Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\] \[4\] \[5\]](#)

9.7.27 PCIE_CPTS_LENGTH_REG Register (Offset = ECh) [reset = 0h]

PCIE_CPTS_LENGTH_REG is shown in [Figure 9-1491](#) and described in [Table 9-3434](#).

Return to [Summary Table](#).

Time Stamp Generate Function Length Value

Table 9-3433. PCIE_CPTS_LENGTH_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 60ECh
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 60ECh
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 60ECh
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 60ECh

Figure 9-1491. PCIE_CPTS_LENGTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3434. PCIE_CPTS_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value

Table 9-3435. Register Call Summary for PCIE_CPTS_LENGTH_REG

PCIE_CPTS Registers

- [PCIE_CPTS_LENGTH_REG Register \(Offset = ECh\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS_LENGTH_REG Register \(Offset = 20Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\]](#)

9.7.28 PCIE_CPTS_PPM_LOW_REG Register (Offset = F0h) [reset = 0h]

PCIE_CPTS_PPM_LOW_REG is shown in [Figure 9-1492](#) and described in [Table 9-3437](#).

Return to [Summary Table](#).

Time Stamp Generate Function PPM Low Value

Table 9-3436. PCIE_CPTS_PPM_LOW_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 60F0h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 60F0h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 60F0h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 60F0h

Figure 9-1492. PCIE_CPTS_PPM_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3437. PCIE_CPTS_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp Generate Function PPM Low Value

Table 9-3438. Register Call Summary for PCIE_CPTS_PPM_LOW_REG

PCIE_CPTS Registers
<ul style="list-style-type: none"> PCIE_CPTS_PPM_LOW_REG Register (Offset = 210h) [reset = 0h]: [0] PCIE_CPTS_PPM_LOW_REG Register (Offset = F0h) [reset = 0h]: [0] PCIE_CPTS Registers: [0] [1] [2] [3]

9.7.29 PCIE_CPTS_PPM_HIGH_REG Register (Offset = F4h) [reset = X]

PCIE_CPTS_PPM_HIGH_REG is shown in [Figure 9-1493](#) and described in [Table 9-3440](#).

Return to [Summary Table](#).

Time Stamp Generate Function PPM High Value

Table 9-3439. PCIE_CPTS_PPM_HIGH_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 60F4h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 60F4h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 60F4h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 60F4h

Figure 9-1493. PCIE_CPTS_PPM_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3440. PCIE_CPTS_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value

Table 9-3441. Register Call Summary for PCIE_CPTS_PPM_HIGH_REG

PCIE_CPTS Registers

- [PCIE_CPTS_PPM_HIGH_REG Register \(Offset = F4h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_PPM_HIGH_REG Register \(Offset = 214h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\]](#)

9.7.30 PCIE_CPTS_NUDGE_REG Register (Offset = F8h) [reset = X]

PCIE_CPTS_NUDGE_REG is shown in [Figure 9-1494](#) and described in [Table 9-3443](#).

Return to [Summary Table](#).

Time Stamp Generate Function Nudge Value

Table 9-3442. PCIE_CPTS_NUDGE_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 60F8h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 60F8h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 60F8h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 60F8h

Figure 9-1494. PCIE_CPTS_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3443. PCIE_CPTS_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value

Table 9-3444. Register Call Summary for PCIE_CPTS_NUDGE_REG

PCIE_CPTS Registers				
<ul style="list-style-type: none"> • PCIE_CPTS_NUDGE_REG Register (Offset = 218h) [reset = X]: [0] • PCIE_CPTS_NUDGE_REG Register (Offset = F8h) [reset = X]: [0] • PCIE_CPTS Registers: [0] [1] [2] [3] 				

9.7.31 PCIE_CPTS_COMP_LOW_REG Register (Offset = 200h) [reset = 0h]

PCIE_CPTS_COMP_LOW_REG is shown in [Figure 9-1495](#) and described in [Table 9-3446](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Comparison Low Value

**Table 9-3445. PCIE_CPTS_COMP_LOW_REG
Instances**

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6200h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6200h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6200h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6200h

Figure 9-1495. PCIE_CPTS_COMP_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3446. PCIE_CPTS_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp ESTF Generate Function Comparison Low Value

Table 9-3447. Register Call Summary for PCIE_CPTS_COMP_LOW_REG

PCIE_CPTS Registers				
<ul style="list-style-type: none"> • PCIE_CPTS_COMP_LOW_REG Register (Offset = E0h) [reset = 0h]: [0] • PCIE_CPTS_COMP_LOW_REG Register (Offset = 200h) [reset = 0h]: [0] • PCIE_CPTS Registers: [0] [1] [2] [3] 				

9.7.32 PCIE_CPTS_COMP_HIGH_REG Register (Offset = 204h) [reset = 0h]

PCIE_CPTS_COMP_HIGH_REG is shown in [Figure 9-1496](#) and described in [Table 9-3449](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Comparison high Value

Table 9-3448. PCIE_CPTS_COMP_HIGH_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6204h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6204h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6204h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6204h

Figure 9-1496. PCIE_CPTS_COMP_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3449. PCIE_CPTS_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp ESTF Generate Function Comparison High Value

Table 9-3450. Register Call Summary for PCIE_CPTS_COMP_HIGH_REG

PCIE_CPTS Registers				
<ul style="list-style-type: none"> PCIE_CPTS_COMP_HIGH_REG Register (Offset = 204h) [reset = 0h]: [0] PCIE_CPTS_COMP_HIGH_REG Register (Offset = E4h) [reset = 0h]: [0] PCIE_CPTS Registers: [0] [1] [2] [3] 				

9.7.33 PCIE_CPTS_CONTROL_REG Register (Offset = 208h) [reset = X]

PCIE_CPTS_CONTROL_REG is shown in [Figure 9-1497](#) and described in [Table 9-3452](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Control

**Table 9-3451. PCIE_CPTS_CONTROL_REG
Instances**

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6208h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6208h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6208h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6208h

Figure 9-1497. PCIE_CPTS_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						POLARITY_INV	PPM_DIR
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3452. PCIE_CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	POLARITY_INV	R/W	0h	Time Stamp ESTF Generate Function Polarity Invert
0	PPM_DIR	R/W	0h	Time Stamp ESTF Generate Function PPM Direction

Table 9-3453. Register Call Summary for PCIE_CPTS_CONTROL_REG

PCIE_CPTS Registers

- [PCIE_CPTS_CONTROL_REG Register \(Offset = E8h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_CONTROL_REG Register \(Offset = 208h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_CONTROL_REG Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\] \[4\] \[5\]](#)

9.7.34 PCIE_CPTS_LENGTH_REG Register (Offset = 20Ch) [reset = 0h]

PCIE_CPTS_LENGTH_REG is shown in [Figure 9-1498](#) and described in [Table 9-3455](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Length Value

Table 9-3454. PCIE_CPTS_LENGTH_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 620Ch
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 620Ch
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 620Ch
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 620Ch

Figure 9-1498. PCIE_CPTS_LENGTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3455. PCIE_CPTS_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp ESTF Generate Function Length Value

Table 9-3456. Register Call Summary for PCIE_CPTS_LENGTH_REG

PCIE_CPTS Registers	
•	PCIE_CPTS_LENGTH_REG Register (Offset = ECh) [reset = 0h]: [0]
•	PCIE_CPTS_LENGTH_REG Register (Offset = 20Ch) [reset = 0h]: [0]
•	PCIE_CPTS Registers: [0] [1] [2] [3]

9.7.35 PCIE_CPTS_PPM_LOW_REG Register (Offset = 210h) [reset = 0h]

PCIE_CPTS_PPM_LOW_REG is shown in [Figure 9-1499](#) and described in [Table 9-3458](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function PPM Low Value

**Table 9-3457. PCIE_CPTS_PPM_LOW_REG
Instances**

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6210h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6210h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6210h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6210h

Figure 9-1499. PCIE_CPTS_PPM_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3458. PCIE_CPTS_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp ESTF Generate Function PPM Low Value

Table 9-3459. Register Call Summary for PCIE_CPTS_PPM_LOW_REG

PCIE_CPTS Registers				
<ul style="list-style-type: none"> • PCIE_CPTS_PPM_LOW_REG Register (Offset = 210h) [reset = 0h]: [0] • PCIE_CPTS_PPM_LOW_REG Register (Offset = F0h) [reset = 0h]: [0] • PCIE_CPTS Registers: [0] [1] [2] [3] 				

9.7.36 PCIE_CPTS_PPM_HIGH_REG Register (Offset = 214h) [reset = X]

PCIE_CPTS_PPM_HIGH_REG is shown in [Figure 9-1500](#) and described in [Table 9-3461](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function PPM High Value

Table 9-3460. PCIE_CPTS_PPM_HIGH_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6214h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6214h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6214h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6214h

Figure 9-1500. PCIE_CPTS_PPM_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3461. PCIE_CPTS_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp ESTF Generate Function PPM High Value

Table 9-3462. Register Call Summary for PCIE_CPTS_PPM_HIGH_REG

PCIE_CPTS Registers

- [PCIE_CPTS_PPM_HIGH_REG Register \(Offset = F4h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_PPM_HIGH_REG Register \(Offset = 214h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\]](#)

9.7.37 PCIE_CPTS_NUDGE_REG Register (Offset = 218h) [reset = X]

PCIE_CPTS_NUDGE_REG is shown in [Figure 9-1501](#) and described in [Table 9-3464](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Nudge Value

Table 9-3463. PCIE_CPTS_NUDGE_REG Instances

Instance	Physical Address
PCIE0_CORE_CPTS_CFG_CPTS_VBU SP	0290 6218h
PCIE1_CORE_CPTS_CFG_CPTS_VBU SP	0291 6218h
PCIE2_CORE_CPTS_CFG_CPTS_VBU SP	0292 6218h
PCIE3_CORE_CPTS_CFG_CPTS_VBU SP	0293 6218h

Figure 9-1501. PCIE_CPTS_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RESERVED																								NUDGE											
R/W-X																								R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3464. PCIE_CPTS_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp ESTF Generate Function Nudge Value

Table 9-3465. Register Call Summary for PCIE_CPTS_NUDGE_REG

PCIE_CPTS Registers

- [PCIE_CPTS_NUDGE_REG Register \(Offset = 218h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS_NUDGE_REG Register \(Offset = F8h\) \[reset = X\]: \[0\]](#)
- [PCIE_CPTS Registers: \[0\] \[1\] \[2\] \[3\]](#)

9.8 PCIE_VMAP_HP Registers

Table 9-3467 lists the memory-mapped registers for the PCIE_VMAP_HP. All register offset addresses not listed in Table 9-3467 should be considered as reserved locations and the register contents should not be modified.

RequesterID to virtID mapping registers

Table 9-3466. PCIE_VMAP_HP Instances

Instance	Base Address
PCIE0_CORE_VMAP_HP_MMRS	0290 4000h
PCIE1_CORE_VMAP_HP_MMRS	0291 4000h
PCIE2_CORE_VMAP_HP_MMRS	0292 4000h
PCIE3_CORE_VMAP_HP_MMRS	0293 4000h

Table 9-3467. PCIE_VMAP_HP Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_VM AP_HP_MMRS Physical Address	PCIE1_CORE_V MAP_HP_MMRS Physical Address
0h + formula	PCIE_VMAP_HP_CTRL_J		0290 4000h + formula	0291 4000h + formula
4h + formula	PCIE_VMAP_HP_REQID_J		0290 4004h + formula	0291 4004h + formula
8h + formula	PCIE_VMAP_HP_VIRTID_J		0290 4008h + formula	0291 4008h + formula
200h	PCIE_VMAP_HP_DEFMAP		0290 4200h	0291 4200h

Table 9-3468. PCIE_VMAP_HP Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_VM AP_HP_MMRS Physical Address	PCIE3_CORE_V MAP_HP_MMRS Physical Address
0h + formula	PCIE_VMAP_HP_CTRL_J		0292 4000h + formula	0293 4000h + formula
4h + formula	PCIE_VMAP_HP_REQID_J		0292 4004h + formula	0293 4004h + formula
8h + formula	PCIE_VMAP_HP_VIRTID_J		0292 4008h + formula	0293 4008h + formula
200h	PCIE_VMAP_HP_DEFMAP		0292 4200h	0293 4200h

9.8.1 PCIE_VMAP_HP_CTRL_j Register (Offset = 0h + formula) [reset = X]

PCIE_VMAP_HP_CTRL_j is shown in [Figure 9-1502](#) and described in [Table 9-3470](#).

Return to [Summary Table](#).

Control register

Offset = 0h + (j * Ch); where j = 0h to 1Fh

Table 9-3469. PCIE_VMAP_HP_CTRL_j Instances

Instance	Physical Address
PCIE0_CORE_VMAP_HP_MMRS	0290 4000h + formula
PCIE1_CORE_VMAP_HP_MMRS	0291 4000h + formula
PCIE2_CORE_VMAP_HP_MMRS	0292 4000h + formula
PCIE3_CORE_VMAP_HP_MMRS	0293 4000h + formula

Figure 9-1502. PCIE_VMAP_HP_CTRL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EN
R/W-X															R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3470. PCIE_VMAP_HP_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EN	R/W	0h	ID enable

Table 9-3471. Register Call Summary for PCIE_VMAP_HP_CTRL_j

PCIE_VMAP_HP Registers <ul style="list-style-type: none"> • PCIE_VMAP_HP_CTRL_j Register (Offset = 0h + formula) [reset = X]: [0] • PCIE_VMAP_HP Registers: [0] [1]
PCIe Subsystem Functional Description <ul style="list-style-type: none"> • PCIe Subsystem Virtid Mapping: [0] [1] [2]

9.8.2 PCIE_VMAP_HP_REQID_j Register (Offset = 4h + formula) [reset = 0h]

PCIE_VMAP_HP_REQID_j is shown in [Figure 9-1503](#) and described in [Table 9-3473](#).

Return to [Summary Table](#).

Requester ID mask and value register

Offset = 4h + (j * Ch); where j = 0h to 1Fh

Table 9-3472. PCIE_VMAP_HP_REQID_j Instances

Instance	Physical Address
PCIE0_CORE_VMAP_HP_MMRS	0290 4004h + formula
PCIE1_CORE_VMAP_HP_MMRS	0291 4004h + formula
PCIE2_CORE_VMAP_HP_MMRS	0292 4004h + formula
PCIE3_CORE_VMAP_HP_MMRS	0293 4004h + formula

Figure 9-1503. PCIE_VMAP_HP_REQID_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK																RID															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3473. PCIE_VMAP_HP_REQID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MASK	R/W	0h	RequesterID mask
15-0	RID	R/W	0h	RequesterID

Table 9-3474. Register Call Summary for PCIE_VMAP_HP_REQID_j

PCIE_VMAP_HP Registers
<ul style="list-style-type: none"> PCIE_VMAP_HP Registers: [0] [1] PCIE_VMAP_HP_REQID_j Register (Offset = 4h + formula) [reset = 0h]: [0]
PCIE Subsystem Functional Description
<ul style="list-style-type: none"> PCIE Subsystem Virtid Mapping: [0] [1] [2] [3] [4] [5] [6]

9.8.3 PCIE_VMAP_HP_VIRTID_j Register (Offset = 8h + formula) [reset = X]

PCIE_VMAP_HP_VIRTID_j is shown in [Figure 9-1504](#) and described in [Table 9-3476](#).

Return to [Summary Table](#).

Virt ID and Atype register

Offset = 8h + (j * Ch); where j = 0h to 1Fh

Table 9-3475. PCIE_VMAP_HP_VIRTID_j Instances

Instance	Physical Address
PCIE0_CORE_VMAP_HP_MMRS	0290 4008h + formula
PCIE1_CORE_VMAP_HP_MMRS	0291 4008h + formula
PCIE2_CORE_VMAP_HP_MMRS	0292 4008h + formula
PCIE3_CORE_VMAP_HP_MMRS	0293 4008h + formula

Figure 9-1504. PCIE_VMAP_HP_VIRTID_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														ATYPE	
R/W-X														R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				VID											
R/W-X				R/W-FFFh											

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3476. PCIE_VMAP_HP_VIRTID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	ATYPE	R/W	0h	Address type attribute. 0-Physical Address, 1-Intermediate Address, 2-Virtual Address, 3-Translated Address
15-12	RESERVED	R/W	X	
11-0	VID	R/W	FFFh	Match ID

Table 9-3477. Register Call Summary for PCIE_VMAP_HP_VIRTID_j

PCIE_VMAP_HP Registers
<ul style="list-style-type: none"> PCIE_VMAP_HP Registers: [0] [1] PCIE_VMAP_HP_VIRTID_j Register (Offset = 8h + formula) [reset = X]: [0]
PCIe Subsystem Functional Description
<ul style="list-style-type: none"> PCIe Subsystem Virtid Mapping: [0] [1] [2] [3]

9.8.4 PCIE_VMAP_HP_DEFMAP Register (Offset = 200h) [reset = X]

PCIE_VMAP_HP_DEFMAP is shown in Figure 9-1505 and described in Table 9-3479.

Return to [Summary Table](#).

virtID default value register

Table 9-3478. PCIE_VMAP_HP_DEFMAP Instances

Instance	Physical Address
PCIE0_CORE_VMAP_HP_MMRS	0290 4200h
PCIE1_CORE_VMAP_HP_MMRS	0291 4200h
PCIE2_CORE_VMAP_HP_MMRS	0292 4200h
PCIE3_CORE_VMAP_HP_MMRS	0293 4200h

Figure 9-1505. PCIE_VMAP_HP_DEFMAP Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED			ATS_DIS	BDF_MODE	RESERVED	DEF_ATYPE	
R/W-X			R/W-0h	R/W-0h	R/W-X	R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				DEF_VID			
R/W-X				R/W-FFFh			
7	6	5	4	3	2	1	0
DEF_VID							
R/W-FFFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3479. PCIE_VMAP_HP_DEFMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20	ATS_DIS	R/W	0h	ATS mode. 1-ATS is enabled, 0-ATS is disabled
19	BDF_MODE	R/W	0h	Bus default mode. 0-Use default bus numbers, 1-Use offset bus numbers
18	RESERVED	R/W	X	
17-16	DEF_ATYPE	R/W	0h	Default address type attribute. 0-Physical Address, 1-Intermediate Address, 2-Virtual Address, 3-Translated Address
15-12	RESERVED	R/W	X	
11-0	DEF_VID	R/W	FFFh	Default match ID

Table 9-3480. Register Call Summary for PCIE_VMAP_HP_DEFMAP

PCIE_VMAP_HP Registers

- [PCIE_VMAP_HP Registers: \[0\] \[1\]](#)
- [PCIE_VMAP_HP_DEFMAP Register \(Offset = 200h\) \[reset = X\]: \[0\]](#)

Table 9-3480. Register Call Summary for PCIE_VMAP_HP_DEFMAP (continued)

PCIe Subsystem Functional Description
<ul style="list-style-type: none">• PCIe Subsystem Virtid Mapping: [0] [1] [2] [3] [4] [5] [6]

9.9 PCIE_VMAP_LP Registers

Table 9-3482 lists the memory-mapped registers for the PCIE_VMAP_LP. All register offset addresses not listed in Table 9-3482 should be considered as reserved locations and the register contents should not be modified.

RequesterID to virtID mapping registers

Table 9-3481. PCIE_VMAP_LP Instances

Instance	Base Address
PCIE0_CORE_VMAP_LP_MMRS	0290 5000h
PCIE1_CORE_VMAP_LP_MMRS	0291 5000h
PCIE2_CORE_VMAP_LP_MMRS	0292 5000h
PCIE3_CORE_VMAP_LP_MMRS	0293 5000h

Table 9-3482. PCIE_VMAP_LP Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_VM AP_LP_MMRS Physical Address	PCIE1_CORE_V MAP_LP_MMRS Physical Address
0h + formula	PCIE_VMAP_LP_CTRL_j		0290 5000h + formula	0291 5000h + formula
4h + formula	PCIE_VMAP_LP_REQID_j		0290 5004h + formula	0291 5004h + formula
8h + formula	PCIE_VMAP_LP_VIRTID_j		0290 5008h + formula	0291 5008h + formula
200h	PCIE_VMAP_LP_DEFMAP		0290 5200h	0291 5200h

Table 9-3483. PCIE_VMAP_LP Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_VM AP_LP_MMRS Physical Address	PCIE3_CORE_V MAP_LP_MMRS Physical Address
0h + formula	PCIE_VMAP_LP_CTRL_j		0292 5000h + formula	0293 5000h + formula
4h + formula	PCIE_VMAP_LP_REQID_j		0292 5004h + formula	0293 5004h + formula
8h + formula	PCIE_VMAP_LP_VIRTID_j		0292 5008h + formula	0293 5008h + formula
200h	PCIE_VMAP_LP_DEFMAP		0292 5200h	0293 5200h

9.9.1 PCIE_VMAP_LP_CTRL_j Register (Offset = 0h + formula) [reset = X]

PCIE_VMAP_LP_CTRL_j is shown in [Figure 9-1506](#) and described in [Table 9-3485](#).

Return to [Summary Table](#).

Control register

Offset = 0h + (j * Ch); where j = 0h to 1Fh

Table 9-3484. PCIE_VMAP_LP_CTRL_j Instances

Instance	Physical Address
PCIE0_CORE_VMAP_LP_MMRS	0290 5000h + formula
PCIE1_CORE_VMAP_LP_MMRS	0291 5000h + formula
PCIE2_CORE_VMAP_LP_MMRS	0292 5000h + formula
PCIE3_CORE_VMAP_LP_MMRS	0293 5000h + formula

Figure 9-1506. PCIE_VMAP_LP_CTRL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EN
R/W-X															R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3485. PCIE_VMAP_LP_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EN	R/W	0h	ID enable

Table 9-3486. Register Call Summary for PCIE_VMAP_LP_CTRL_j

PCIe Subsystem Functional Description
<ul style="list-style-type: none"> PCIe Subsystem Virtid Mapping: [0] [1] [2]
PCIE_VMAP_LP Registers
<ul style="list-style-type: none"> PCIE_VMAP_LP Registers: [0] [1] PCIE_VMAP_LP_CTRL_j Register (Offset = 0h + formula) [reset = X]: [0]

9.9.2 PCIE_VMAP_LP_REQID_j Register (Offset = 4h + formula) [reset = 0h]

PCIE_VMAP_LP_REQID_j is shown in Figure 9-1507 and described in Table 9-3488.

Return to [Summary Table](#).

Requester ID mask and value register

Offset = 4h + (j * Ch); where j = 0h to 1Fh

Table 9-3487. PCIE_VMAP_LP_REQID_j Instances

Instance	Physical Address
PCIE0_CORE_VMAP_LP_MMRS	0290 5004h + formula
PCIE1_CORE_VMAP_LP_MMRS	0291 5004h + formula
PCIE2_CORE_VMAP_LP_MMRS	0292 5004h + formula
PCIE3_CORE_VMAP_LP_MMRS	0293 5004h + formula

Figure 9-1507. PCIE_VMAP_LP_REQID_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASK																RID															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3488. PCIE_VMAP_LP_REQID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MASK	R/W	0h	RequesterID mask
15-0	RID	R/W	0h	RequesterID

Table 9-3489. Register Call Summary for PCIE_VMAP_LP_REQID_j

PCIE Subsystem Functional Description
<ul style="list-style-type: none"> PCIE Subsystem Virtid Mapping: [0] [1] [2] [3] [4] [5] [6]
PCIE_VMAP_LP Registers
<ul style="list-style-type: none"> PCIE_VMAP_LP Registers: [0] [1] PCIE_VMAP_LP_REQID_j Register (Offset = 4h + formula) [reset = 0h]: [0]

9.9.3 PCIE_VMAP_LP_VIRTID_j Register (Offset = 8h + formula) [reset = X]

PCIE_VMAP_LP_VIRTID_j is shown in [Figure 9-1508](#) and described in [Table 9-3491](#).

Return to [Summary Table](#).

Virt ID and Atype register

Offset = 8h + (j * Ch); where j = 0h to 1Fh

Table 9-3490. PCIE_VMAP_LP_VIRTID_j Instances

Instance	Physical Address
PCIE0_CORE_VMAP_LP_MMRS	0290 5008h + formula
PCIE1_CORE_VMAP_LP_MMRS	0291 5008h + formula
PCIE2_CORE_VMAP_LP_MMRS	0292 5008h + formula
PCIE3_CORE_VMAP_LP_MMRS	0293 5008h + formula

Figure 9-1508. PCIE_VMAP_LP_VIRTID_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														ATYPE	
R/W-X														R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				VID											
R/W-X				R/W-FFFh											

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3491. PCIE_VMAP_LP_VIRTID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	ATYPE	R/W	0h	Address type attribute. 0-Physical Address, 1-Intermediate Address, 2-Virtual Address, 3-Translated Address
15-12	RESERVED	R/W	X	
11-0	VID	R/W	FFFh	Match ID

Table 9-3492. Register Call Summary for PCIE_VMAP_LP_VIRTID_j

PCIe Subsystem Functional Description
<ul style="list-style-type: none"> PCIe Subsystem Virtid Mapping: [0] [1] [2] [3]
PCIE_VMAP_LP Registers
<ul style="list-style-type: none"> PCIE_VMAP_LP Registers: [0] [1] PCIE_VMAP_LP_VIRTID_j Register (Offset = 8h + formula) [reset = X]: [0]

9.9.4 PCIE_VMAP_LP_DEFMAP Register (Offset = 200h) [reset = X]

PCIE_VMAP_LP_DEFMAP is shown in [Figure 9-1509](#) and described in [Table 9-3494](#).

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virtID default value register

Table 9-3493. PCIE_VMAP_LP_DEFMAP Instances

Instance	Physical Address
PCIE0_CORE_VMAP_LP_MMRS	0290 5200h
PCIE1_CORE_VMAP_LP_MMRS	0291 5200h
PCIE2_CORE_VMAP_LP_MMRS	0292 5200h
PCIE3_CORE_VMAP_LP_MMRS	0293 5200h

Figure 9-1509. PCIE_VMAP_LP_DEFMAP Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED			ATS_DIS	BDF_MODE	RESERVED	DEF_ATYPE	
R/W-X			R/W-0h	R/W-0h	R/W-X	R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				DEF_VID			
R/W-X				R/W-FFFh			
7	6	5	4	3	2	1	0
DEF_VID							
R/W-FFFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3494. PCIE_VMAP_LP_DEFMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20	ATS_DIS	R/W	0h	ATS mode. 1-ATS is enabled, 0-ATS is disabled
19	BDF_MODE	R/W	0h	Bus default mode. 0-Use default bus numbers, 1-Use offset bus numbers
18	RESERVED	R/W	X	
17-16	DEF_ATYPE	R/W	0h	Default address type attribute. 0-Physical Address, 1-Intermediate Address, 2-Virtual Address, 3-Translated Address
15-12	RESERVED	R/W	X	
11-0	DEF_VID	R/W	FFFh	Default match ID

Table 9-3495. Register Call Summary for PCIE_VMAP_LP_DEFMAP

PCIE Subsystem Functional Description

- [PCIE Subsystem Virtid Mapping: \[0\] \[1\] \[2\] \[3\] \[4\] \[5\] \[6\]](#)

Table 9-3495. Register Call Summary for PCIE_VMAP_LP_DEFMAP (continued)

PCIE_VMAP_LP Registers
<ul style="list-style-type: none">• PCIE_VMAP_LP Registers: [0] [1]• PCIE_VMAP_LP_DEFMAP Register (Offset = 200h) [reset = X]: [0]

9.10 PCIE_ECC_AGGR0 Registers

Table 9-3497 lists the memory-mapped registers for the PCIE_ECC_AGGR0. All register offset addresses not listed in Table 9-3497 should be considered as reserved locations and the register contents should not be modified.

Table 9-3496. PCIE_ECC_AGGR0 Instances

Instance	Base Address
PCIE0_CORE_ECC_AGGR0	02A0 0000h
PCIE1_CORE_ECC_AGGR0	02A0 2000h
PCIE2_CORE_ECC_AGGR0	02A0 4000h
PCIE3_CORE_ECC_AGGR0	02A0 6000h

Table 9-3497. PCIE_ECC_AGGR0 Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_ECC_AGGR0 Physical Address	PCIE1_CORE_ECC_AGGR0 Physical Address
0h	PCIE_ECC0_REV	Aggregator Revision Register	02A0 0000h	02A0 2000h
8h	PCIE_ECC0_VECTOR	ECC PCIE_ECC0_VECTOR Register	02A0 0008h	02A0 2008h
Ch	PCIE_ECC0_STAT	Misc Status	02A0 000Ch	02A0 200Ch
10h + formula	PCIE_ECC0_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	02A0 0010h + formula	02A0 2010h + formula
3Ch	PCIE_ECC0_SEC_EOI_REG	EOI Register	02A0 003Ch	02A0 203Ch
40h	PCIE_ECC0_SEC_STATUS_REG0	Interrupt Status Register 0	02A0 0040h	02A0 2040h
80h	PCIE_ECC0_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A0 0080h	02A0 2080h
C0h	PCIE_ECC0_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A0 00C0h	02A0 20C0h
13Ch	PCIE_ECC0_DED_EOI_REG	EOI Register	02A0 013Ch	02A0 213Ch
140h	PCIE_ECC0_DED_STATUS_REG0	Interrupt Status Register 0	02A0 0140h	02A0 2140h
180h	PCIE_ECC0_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A0 0180h	02A0 2180h
1C0h	PCIE_ECC0_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A0 01C0h	02A0 21C0h
200h	PCIE_ECC0_AGGR_ENABLE_SET	AGGR interrupt enable set Register	02A0 0200h	02A0 2200h
204h	PCIE_ECC0_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	02A0 0204h	02A0 2204h
208h	PCIE_ECC0_AGGR_STATUS_SET	AGGR interrupt status set Register	02A0 0208h	02A0 2208h
20Ch	PCIE_ECC0_AGGR_STATUS_CLR	AGGR interrupt status clear Register	02A0 020Ch	02A0 220Ch

Table 9-3498. PCIE_ECC_AGGR0 Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_ECC_AGGR0 Physical Address	PCIE3_CORE_ECC_AGGR0 Physical Address
0h	PCIE_ECC0_REV	Aggregator Revision Register	02A0 4000h	02A0 6000h
8h	PCIE_ECC0_VECTOR	ECC PCIE_ECC0_VECTOR Register	02A0 4008h	02A0 6008h
Ch	PCIE_ECC0_STAT	Misc Status	02A0 400Ch	02A0 600Ch
10h + formula	PCIE_ECC0_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	02A0 4010h + formula	02A0 6010h + formula
3Ch	PCIE_ECC0_SEC_EOI_REG	EOI Register	02A0 403Ch	02A0 603Ch
40h	PCIE_ECC0_SEC_STATUS_REG0	Interrupt Status Register 0	02A0 4040h	02A0 6040h
80h	PCIE_ECC0_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A0 4080h	02A0 6080h

Table 9-3498. PCIe_ECC_AGGR0 Registers - 2 (continued)

Offset	Acronym	Register Name	PCIe2_CORE_ ECC_AGGR0 Physical Address	PCIe3_CORE_ ECC_AGGR0 Physical Address
C0h	PCIe_ECC0_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A0 40C0h	02A0 60C0h
13Ch	PCIe_ECC0_DED_EOI_REG	EOI Register	02A0 413Ch	02A0 613Ch
140h	PCIe_ECC0_DED_STATUS_REG0	Interrupt Status Register 0	02A0 4140h	02A0 6140h
180h	PCIe_ECC0_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A0 4180h	02A0 6180h
1C0h	PCIe_ECC0_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A0 41C0h	02A0 61C0h
200h	PCIe_ECC0_AGGR_ENABLE_SET	AGGR interrupt enable set Register	02A0 4200h	02A0 6200h
204h	PCIe_ECC0_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	02A0 4204h	02A0 6204h
208h	PCIe_ECC0_AGGR_STATUS_SET	AGGR interrupt status set Register	02A0 4208h	02A0 6208h
20Ch	PCIe_ECC0_AGGR_STATUS_CLR	AGGR interrupt status clear Register	02A0 420Ch	02A0 620Ch

9.10.1 PCIE_ECC0_REV Register (Offset = 0h) [reset = 66A0EA00h]

PCIE_ECC0_REV is shown in [Figure 9-1510](#) and described in [Table 9-3500](#).

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Revision parameters

Table 9-3499. PCIE_ECC0_REV Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0000h
PCIE1_CORE_ECC_AGGR0	02A0 2000h
PCIE2_CORE_ECC_AGGR0	02A0 4000h
PCIE3_CORE_ECC_AGGR0	02A0 6000h

Figure 9-1510. PCIE_ECC0_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 9-3500. PCIE_ECC0_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

Table 9-3501. Register Call Summary for PCIE_ECC0_REV

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]: \[0\]](#)

9.10.2 PCIE_ECC0_VECTOR Register (Offset = 8h) [reset = X]

PCIE_ECC0_VECTOR is shown in [Figure 9-1511](#) and described in [Table 9-3503](#).

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ECC PCIE_ECC0_VECTOR Register

Table 9-3502. PCIE_ECC0_VECTOR Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0008h
PCIE1_CORE_ECC_AGGR0	02A0 2008h
PCIE2_CORE_ECC_AGGR0	02A0 4008h
PCIE3_CORE_ECC_AGGR0	02A0 6008h

Figure 9-1511. PCIE_ECC0_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3503. PCIE_ECC0_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

Table 9-3504. Register Call Summary for PCIE_ECC0_VECTOR

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\] \[2\] \[3\]](#)
- [PCIE_ECC0_VECTOR Register \(Offset = 8h\) \[reset = X\]: \[0\] \[1\]](#)

9.10.3 PCIE_ECC0_STAT Register (Offset = Ch) [reset = X]

PCIE_ECC0_STAT is shown in [Figure 9-1512](#) and described in [Table 9-3506](#).

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Misc Status

Table 9-3505. PCIE_ECC0_STAT Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 000Ch
PCIE1_CORE_ECC_AGGR0	02A0 200Ch
PCIE2_CORE_ECC_AGGR0	02A0 400Ch
PCIE3_CORE_ECC_AGGR0	02A0 600Ch

Figure 9-1512. PCIE_ECC0_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											NUM_RAMs																				
R-X											R-9h																				

LEGEND: R = Read Only; -n = value after reset

Table 9-3506. PCIE_ECC0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	9h	Indicates the number of RAMs serviced by the ECC aggregator

Table 9-3507. Register Call Summary for PCIE_ECC0_STAT

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_STAT Register \(Offset = Ch\) \[reset = X\]: \[0\]](#)

9.10.4 PCIE_ECC0_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

PCIE_ECC0_RESERVED_SVBUS_y is shown in Figure 9-1513 and described in Table 9-3509.

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Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 9-3508. PCIE_ECC0_RESERVED_SVBUS_y
Instances**

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0010h + formula
PCIE1_CORE_ECC_AGGR0	02A0 2010h + formula
PCIE2_CORE_ECC_AGGR0	02A0 4010h + formula
PCIE3_CORE_ECC_AGGR0	02A0 6010h + formula

Figure 9-1513. PCIE_ECC0_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3509. PCIE_ECC0_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

Table 9-3510. Register Call Summary for PCIE_ECC0_RESERVED_SVBUS_y

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_RESERVED_SVBUS_y Register \(Offset = 10h + formula\) \[reset = 0h\]: \[0\]](#)

9.10.5 PCIE_ECC0_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

PCIE_ECC0_SEC_EOI_REG is shown in Figure 9-1514 and described in Table 9-3512.

Return to [Summary Table](#).

EOI Register

Table 9-3511. PCIE_ECC0_SEC_EOI_REG Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 003Ch
PCIE1_CORE_ECC_AGGR0	02A0 203Ch
PCIE2_CORE_ECC_AGGR0	02A0 403Ch
PCIE3_CORE_ECC_AGGR0	02A0 603Ch

Figure 9-1514. PCIE_ECC0_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3512. PCIE_ECC0_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

Table 9-3513. Register Call Summary for PCIE_ECC0_SEC_EOI_REG

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)

9.10.6 PCIE_ECC0_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

PCIE_ECC0_SEC_STATUS_REG0 is shown in Figure 9-1515 and described in Table 9-3515.

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 9-3514. PCIE_ECC0_SEC_STATUS_REG0
Instances**

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0040h
PCIE1_CORE_ECC_AGGR0	02A0 2040h
PCIE2_CORE_ECC_AGGR0	02A0 4040h
PCIE3_CORE_ECC_AGGR0	02A0 6040h

Figure 9-1515. PCIE_ECC0_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							AXI2VBUSM_M ST_LP_PEND
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
AXI2VBUSM_M ST_HP_PEND	HP_DIBRAM_R AMECC_PEND	HP_AXISFIFO_ RAMECC_PEN D	HP_AXIMFIFO_ RAMECC_PEN D	DIBRAM_RAM ECC_PEND	AXISFIFO_RA MECC_PEND	AXIMFIFO_RA MECC_PEND	EDC_CTRL_PE ND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3515. PCIE_ECC0_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	AXI2VBUSM_MST_LP_P END	R/W1S	0h	Interrupt Pending Status for axi2vbusm_mst_lp_pend
7	AXI2VBUSM_MST_HP_P END	R/W1S	0h	Interrupt Pending Status for axi2vbusm_mst_hp_pend
6	HP_DIBRAM_RAMECC_ PEND	R/W1S	0h	Interrupt Pending Status for hp_dibram_amecc_pend
5	HP_AXISFIFO_RAMECC_ PEND	R/W1S	0h	Interrupt Pending Status for hp_axisfifo_amecc_pend
4	HP_AXIMFIFO_RAMECC_ PEND	R/W1S	0h	Interrupt Pending Status for hp_aximfifo_amecc_pend
3	DIBRAM_RAMECC_PEN D	R/W1S	0h	Interrupt Pending Status for dibram_amecc_pend
2	AXISFIFO_RAMECC_PE ND	R/W1S	0h	Interrupt Pending Status for axisfifo_amecc_pend
1	AXIMFIFO_RAMECC_PE ND	R/W1S	0h	Interrupt Pending Status for aximfifo_amecc_pend

Table 9-3515. PCIE_ECC0_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EDC_CTRL_PEND	R/W1S	0h	Interrupt Pending Status for edc_ctrl_pend

Table 9-3516. Register Call Summary for PCIE_ECC0_SEC_STATUS_REG0

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)

9.10.7 PCIE_ECC0_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

PCIE_ECC0_SEC_ENABLE_SET_REG0 is shown in Figure 9-1516 and described in Table 9-3518.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 9-3517.
PCIE_ECC0_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0080h
PCIE1_CORE_ECC_AGGR0	02A0 2080h
PCIE2_CORE_ECC_AGGR0	02A0 4080h
PCIE3_CORE_ECC_AGGR0	02A0 6080h

Figure 9-1516. PCIE_ECC0_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							AXI2VBUSM_MST_LP_ENABLE_SET
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
AXI2VBUSM_MST_HP_ENABLE_SET	HP_DIBRAM_RAMECC_ENABLE_SET	HP_AXISFIFO_RAMECC_ENABLE_SET	HP_AXIMFIFO_RAMECC_ENABLE_SET	DIBRAM_RAM_ECC_ENABLE_SET	AXISFIFO_RA_MECC_ENABLE_SET	AXIMFIFO_RA_MECC_ENABLE_SET	EDC_CTRL_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3518. PCIE_ECC0_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	AXI2VBUSM_MST_LP_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for axi2vbusm_mst_lp_pend
7	AXI2VBUSM_MST_HP_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for axi2vbusm_mst_hp_pend
6	HP_DIBRAM_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_dibram_amecc_pend
5	HP_AXISFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_axisfifo_amecc_pend
4	HP_AXIMFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_aximfifo_amecc_pend
3	DIBRAM_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for dibram_amecc_pend
2	AXISFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for axisfifo_amecc_pend
1	AXIMFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for aximfifo_amecc_pend

Table 9-3518. PCIE_ECC0_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EDC_CTRL_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for edc_ctrl_pend

Table 9-3519. Register Call Summary for PCIE_ECC0_SEC_ENABLE_SET_REG0

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = X\]: \[0\]](#)

9.10.8 PCIE_ECC0_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

PCIE_ECC0_SEC_ENABLE_CLR_REG0 is shown in Figure 9-1517 and described in Table 9-3521.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 9-3520.
PCIE_ECC0_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 00C0h
PCIE1_CORE_ECC_AGGR0	02A0 20C0h
PCIE2_CORE_ECC_AGGR0	02A0 40C0h
PCIE3_CORE_ECC_AGGR0	02A0 60C0h

Figure 9-1517. PCIE_ECC0_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							AXI2VBUSM_MST_LP_ENABLE_CLR
R/W-X							R/W1C-0h
7	6	5	4	3	2	1	0
AXI2VBUSM_MST_HP_ENABLE_CLR	HP_DIBRAM_RAMECC_ENABLE_CLR	HP_AXISFIFO_RAMECC_ENABLE_CLR	HP_AXIMFIFO_RAMECC_ENABLE_CLR	DIBRAM_RAM_ECC_ENABLE_CLR	AXISFIFO_RAMECC_ENABLE_CLR	AXIMFIFO_RAMECC_ENABLE_CLR	EDC_CTRL_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3521. PCIE_ECC0_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	AXI2VBUSM_MST_LP_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for axi2vbusm_mst_lp_pend
7	AXI2VBUSM_MST_HP_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for axi2vbusm_mst_hp_pend
6	HP_DIBRAM_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_dibram_ramecc_pend
5	HP_AXISFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_axisfifo_ramecc_pend
4	HP_AXIMFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_aximfifo_ramecc_pend
3	DIBRAM_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for dibram_ramecc_pend
2	AXISFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for axisfifo_ramecc_pend
1	AXIMFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for aximfifo_ramecc_pend

Table 9-3521. PCIE_ECC0_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EDC_CTRL_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for edc_ctrl_pend

Table 9-3522. Register Call Summary for PCIE_ECC0_SEC_ENABLE_CLR_REG0

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = X\]: \[0\]](#)

9.10.9 PCIE_ECC0_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

PCIE_ECC0_DED_EOI_REG is shown in Figure 9-1518 and described in Table 9-3524.

Return to [Summary Table](#).

EOI Register

Table 9-3523. PCIE_ECC0_DED_EOI_REG Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 013Ch
PCIE1_CORE_ECC_AGGR0	02A0 213Ch
PCIE2_CORE_ECC_AGGR0	02A0 413Ch
PCIE3_CORE_ECC_AGGR0	02A0 613Ch

Figure 9-1518. PCIE_ECC0_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3524. PCIE_ECC0_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

Table 9-3525. Register Call Summary for PCIE_ECC0_DED_EOI_REG

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = X\]: \[0\]](#)

9.10.10 PCIE_ECC0_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

PCIE_ECC0_DED_STATUS_REG0 is shown in Figure 9-1519 and described in Table 9-3527.

Return to [Summary Table](#).

Interrupt Status Register 0

Table 9-3526. PCIE_ECC0_DED_STATUS_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0140h
PCIE1_CORE_ECC_AGGR0	02A0 2140h
PCIE2_CORE_ECC_AGGR0	02A0 4140h
PCIE3_CORE_ECC_AGGR0	02A0 6140h

Figure 9-1519. PCIE_ECC0_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							AXI2VBUSM_MST_LP_PEND
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
AXI2VBUSM_MST_HP_PEND	HP_DIBRAM_RAMECC_PEND	HP_AXISFIFO_RAMECC_PEND	HP_AXIMFIFO_RAMECC_PEND	DIBRAM_RAM_ECC_PEND	AXISFIFO_RA_MECC_PEND	AXIMFIFO_RA_MECC_PEND	EDC_CTRL_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3527. PCIE_ECC0_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	AXI2VBUSM_MST_LP_PEND	R/W1S	0h	Interrupt Pending Status for axi2vbusm_mst_lp_pend
7	AXI2VBUSM_MST_HP_PEND	R/W1S	0h	Interrupt Pending Status for axi2vbusm_mst_hp_pend
6	HP_DIBRAM_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_dibram_amecc_pend
5	HP_AXISFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_axisfifo_amecc_pend
4	HP_AXIMFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_aximfifo_amecc_pend
3	DIBRAM_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for dibram_amecc_pend
2	AXISFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for axisfifo_amecc_pend
1	AXIMFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for aximfifo_amecc_pend

Table 9-3527. PCIE_ECC0_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EDC_CTRL_PEND	R/W1S	0h	Interrupt Pending Status for edc_ctrl_pend

Table 9-3528. Register Call Summary for PCIE_ECC0_DED_STATUS_REG0

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_DED_STATUS_REG0 Register \(Offset = 140h\) \[reset = X\]: \[0\]](#)

9.10.11 PCIE_ECC0_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

PCIE_ECC0_DED_ENABLE_SET_REG0 is shown in Figure 9-1520 and described in Table 9-3530.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 9-3529.
PCIE_ECC0_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0180h
PCIE1_CORE_ECC_AGGR0	02A0 2180h
PCIE2_CORE_ECC_AGGR0	02A0 4180h
PCIE3_CORE_ECC_AGGR0	02A0 6180h

Figure 9-1520. PCIE_ECC0_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							AXI2VBUSM_MST_LP_ENABLE_SET
R/W-X							R/W1S-0h
7	6	5	4	3	2	1	0
AXI2VBUSM_MST_HP_ENABLE_SET	HP_DIBRAM_RAMECC_ENABLE_SET	HP_AXISFIFO_RAMECC_ENABLE_SET	HP_AXIMFIFO_RAMECC_ENABLE_SET	DIBRAM_RAM_ECC_ENABLE_SET	AXISFIFO_RA_MECC_ENABLE_SET	AXIMFIFO_RA_MECC_ENABLE_SET	EDC_CTRL_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3530. PCIE_ECC0_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	AXI2VBUSM_MST_LP_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for axi2vbusm_mst_lp_pend
7	AXI2VBUSM_MST_HP_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for axi2vbusm_mst_hp_pend
6	HP_DIBRAM_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_dibram_amecc_pend
5	HP_AXISFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_axisfifo_amecc_pend
4	HP_AXIMFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_aximfifo_amecc_pend
3	DIBRAM_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for dibram_amecc_pend
2	AXISFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for axisfifo_amecc_pend
1	AXIMFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for aximfifo_amecc_pend

Table 9-3530. PCIE_ECC0_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EDC_CTRL_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for edc_ctrl_pend

Table 9-3531. Register Call Summary for PCIE_ECC0_DED_ENABLE_SET_REG0

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_DED_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = X\]: \[0\]](#)

9.10.12 PCIE_ECC0_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

PCIE_ECC0_DED_ENABLE_CLR_REG0 is shown in Figure 9-1521 and described in Table 9-3533.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 9-3532.
PCIE_ECC0_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 01C0h
PCIE1_CORE_ECC_AGGR0	02A0 21C0h
PCIE2_CORE_ECC_AGGR0	02A0 41C0h
PCIE3_CORE_ECC_AGGR0	02A0 61C0h

Figure 9-1521. PCIE_ECC0_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							AXI2VBUSM_MST_LP_ENABLE_CLR
R/W-X							R/W1C-0h
7	6	5	4	3	2	1	0
AXI2VBUSM_MST_HP_ENABLE_CLR	HP_DIBRAM_RAMECC_ENABLE_CLR	HP_AXISFIFO_RAMECC_ENABLE_CLR	HP_AXIMFIFO_RAMECC_ENABLE_CLR	DIBRAM_RAM_ECC_ENABLE_CLR	AXISFIFO_RA_MECC_ENABLE_CLR	AXIMFIFO_RA_MECC_ENABLE_CLR	EDC_CTRL_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3533. PCIE_ECC0_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	AXI2VBUSM_MST_LP_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for axi2vbusm_mst_lp_pend
7	AXI2VBUSM_MST_HP_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for axi2vbusm_mst_hp_pend
6	HP_DIBRAM_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_dibram_ramecc_pend
5	HP_AXISFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_axisfifo_ramecc_pend
4	HP_AXIMFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_aximfifo_ramecc_pend
3	DIBRAM_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for dibram_ramecc_pend
2	AXISFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for axisfifo_ramecc_pend
1	AXIMFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for aximfifo_ramecc_pend

Table 9-3533. PCIE_ECC0_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EDC_CTRL_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for edc_ctrl_pend

Table 9-3534. Register Call Summary for PCIE_ECC0_DED_ENABLE_CLR_REG0

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = X\]: \[0\]](#)

9.10.13 PCIE_ECC0_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

PCIE_ECC0_AGGR_ENABLE_SET is shown in Figure 9-1522 and described in Table 9-3536.

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 9-3535. PCIE_ECC0_AGGR_ENABLE_SET Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0200h
PCIE1_CORE_ECC_AGGR0	02A0 2200h
PCIE2_CORE_ECC_AGGR0	02A0 4200h
PCIE3_CORE_ECC_AGGR0	02A0 6200h

Figure 9-1522. PCIE_ECC0_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3536. PCIE_ECC0_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

Table 9-3537. Register Call Summary for PCIE_ECC0_AGGR_ENABLE_SET

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_AGGR_ENABLE_SET Register \(Offset = 200h\) \[reset = X\]: \[0\]](#)

9.10.14 PCIE_ECC0_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

PCIE_ECC0_AGGR_ENABLE_CLR is shown in Figure 9-1523 and described in Table 9-3539.

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 9-3538. PCIE_ECC0_AGGR_ENABLE_CLR Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0204h
PCIE1_CORE_ECC_AGGR0	02A0 2204h
PCIE2_CORE_ECC_AGGR0	02A0 4204h
PCIE3_CORE_ECC_AGGR0	02A0 6204h

Figure 9-1523. PCIE_ECC0_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3539. PCIE_ECC0_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

Table 9-3540. Register Call Summary for PCIE_ECC0_AGGR_ENABLE_CLR

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_AGGR_ENABLE_CLR Register \(Offset = 204h\) \[reset = X\]: \[0\]](#)

9.10.15 PCIE_ECC0_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

PCIE_ECC0_AGGR_STATUS_SET is shown in Figure 9-1524 and described in Table 9-3542.

Return to [Summary Table](#).

AGGR interrupt status set Register

Table 9-3541. PCIE_ECC0_AGGR_STATUS_SET Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 0208h
PCIE1_CORE_ECC_AGGR0	02A0 2208h
PCIE2_CORE_ECC_AGGR0	02A0 4208h
PCIE3_CORE_ECC_AGGR0	02A0 6208h

Figure 9-1524. PCIE_ECC0_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 9-3542. PCIE_ECC0_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

Table 9-3543. Register Call Summary for PCIE_ECC0_AGGR_STATUS_SET

PCIE_ECC_AGGR0 Registers

- [PCIE_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIE_ECC0_AGGR_STATUS_SET Register \(Offset = 208h\) \[reset = X\]: \[0\]](#)

9.10.16 PCIe_ECC0_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

PCIe_ECC0_AGGR_STATUS_CLR is shown in [Figure 9-1525](#) and described in [Table 9-3545](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

Table 9-3544. PCIe_ECC0_AGGR_STATUS_CLR Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR0	02A0 020Ch
PCIE1_CORE_ECC_AGGR0	02A0 220Ch
PCIE2_CORE_ECC_AGGR0	02A0 420Ch
PCIE3_CORE_ECC_AGGR0	02A0 620Ch

Figure 9-1525. PCIe_ECC0_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 9-3545. PCIe_ECC0_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

Table 9-3546. Register Call Summary for PCIe_ECC0_AGGR_STATUS_CLR

PCIe_ECC_AGGR0 Registers

- [PCIe_ECC_AGGR0 Registers: \[0\] \[1\]](#)
- [PCIe_ECC0_AGGR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = X\]: \[0\]](#)

9.11 PCIE_ECC_AGGR1 Registers

Table 9-3548 lists the memory-mapped registers for the PCIE_ECC_AGGR1. All register offset addresses not listed in Table 9-3548 should be considered as reserved locations and the register contents should not be modified.

Table 9-3547. PCIE_ECC_AGGR1 Instances

Instance	Base Address
PCIE0_CORE_ECC_AGGR1	02A0 1000h
PCIE1_CORE_ECC_AGGR1	02A0 3000h
PCIE2_CORE_ECC_AGGR1	02A0 5000h
PCIE3_CORE_ECC_AGGR1	02A0 7000h

Table 9-3548. PCIE_ECC_AGGR1 Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_ECC_AGGR1 Physical Address	PCIE1_CORE_ECC_AGGR1 Physical Address
0h	PCIE_ECC1_REV	Aggregator Revision Register	02A0 1000h	02A0 3000h
8h	PCIE_ECC1_VECTOR	ECC PCIE_ECC1_VECTOR Register	02A0 1008h	02A0 3008h
Ch	PCIE_ECC1_STAT	Misc Status	02A0 100Ch	02A0 300Ch
10h + formula	PCIE_ECC1_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	02A0 1010h + formula	02A0 3010h + formula
3Ch	PCIE_ECC1_SEC_EOI_REG	EOI Register	02A0 103Ch	02A0 303Ch
40h	PCIE_ECC1_SEC_STATUS_REG0	Interrupt Status Register 0	02A0 1040h	02A0 3040h
80h	PCIE_ECC1_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A0 1080h	02A0 3080h
C0h	PCIE_ECC1_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A0 10C0h	02A0 30C0h
13Ch	PCIE_ECC1_DED_EOI_REG	EOI Register	02A0 113Ch	02A0 313Ch
140h	PCIE_ECC1_DED_STATUS_REG0	Interrupt Status Register 0	02A0 1140h	02A0 3140h
180h	PCIE_ECC1_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A0 1180h	02A0 3180h
1C0h	PCIE_ECC1_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A0 11C0h	02A0 31C0h
200h	PCIE_ECC1_AGGR_ENABLE_SET	AGGR interrupt enable set Register	02A0 1200h	02A0 3200h
204h	PCIE_ECC1_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	02A0 1204h	02A0 3204h
208h	PCIE_ECC1_AGGR_STATUS_SET	AGGR interrupt status set Register	02A0 1208h	02A0 3208h
20Ch	PCIE_ECC1_AGGR_STATUS_CLR	AGGR interrupt status clear Register	02A0 120Ch	02A0 320Ch

Table 9-3549. PCIE_ECC_AGGR1 Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_ECC_AGGR1 Physical Address	PCIE3_CORE_ECC_AGGR1 Physical Address
0h	PCIE_ECC1_REV	Aggregator Revision Register	02A0 5000h	02A0 7000h
8h	PCIE_ECC1_VECTOR	ECC PCIE_ECC1_VECTOR Register	02A0 5008h	02A0 7008h
Ch	PCIE_ECC1_STAT	Misc Status	02A0 500Ch	02A0 700Ch
10h + formula	PCIE_ECC1_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	02A0 5010h + formula	02A0 7010h + formula
3Ch	PCIE_ECC1_SEC_EOI_REG	EOI Register	02A0 503Ch	02A0 703Ch
40h	PCIE_ECC1_SEC_STATUS_REG0	Interrupt Status Register 0	02A0 5040h	02A0 7040h
80h	PCIE_ECC1_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A0 5080h	02A0 7080h

Table 9-3549. PCIe_ECC_AGGR1 Registers - 2 (continued)

Offset	Acronym	Register Name	PCIe2_CORE_ ECC_AGGR1 Physical Address	PCIe3_CORE_ ECC_AGGR1 Physical Address
C0h	PCIe_ECC1_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A0 50C0h	02A0 70C0h
13Ch	PCIe_ECC1_DED_EOI_REG	EOI Register	02A0 513Ch	02A0 713Ch
140h	PCIe_ECC1_DED_STATUS_REG0	Interrupt Status Register 0	02A0 5140h	02A0 7140h
180h	PCIe_ECC1_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A0 5180h	02A0 7180h
1C0h	PCIe_ECC1_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A0 51C0h	02A0 71C0h
200h	PCIe_ECC1_AGGR_ENABLE_SET	AGGR interrupt enable set Register	02A0 5200h	02A0 7200h
204h	PCIe_ECC1_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	02A0 5204h	02A0 7204h
208h	PCIe_ECC1_AGGR_STATUS_SET	AGGR interrupt status set Register	02A0 5208h	02A0 7208h
20Ch	PCIe_ECC1_AGGR_STATUS_CLR	AGGR interrupt status clear Register	02A0 520Ch	02A0 720Ch

9.11.1 PCIE_ECC1_REV Register (Offset = 0h) [reset = 66A0EA00h]

PCIE_ECC1_REV is shown in Figure 9-1526 and described in Table 9-3551.

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Revision parameters

Table 9-3550. PCIE_ECC1_REV Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1000h
PCIE1_CORE_ECC_AGGR1	02A0 3000h
PCIE2_CORE_ECC_AGGR1	02A0 5000h
PCIE3_CORE_ECC_AGGR1	02A0 7000h

Figure 9-1526. PCIE_ECC1_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
R-1Dh				R-2h				R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 9-3551. PCIE_ECC1_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

Table 9-3552. Register Call Summary for PCIE_ECC1_REV

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.2 PCIe_ECC1_VECTOR Register (Offset = 8h) [reset = X]

PCIE_ECC1_VECTOR is shown in [Figure 9-1527](#) and described in [Table 9-3554](#).

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ECC PCIe_ECC1_VECTOR Register

Table 9-3553. PCIe_ECC1_VECTOR Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1008h
PCIE1_CORE_ECC_AGGR1	02A0 3008h
PCIE2_CORE_ECC_AGGR1	02A0 5008h
PCIE3_CORE_ECC_AGGR1	02A0 7008h

Figure 9-1527. PCIe_ECC1_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED					ECC_VECTOR	
R/W1S-0h	R/W-X					R/W-0h	
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3554. PCIe_ECC1_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

Table 9-3555. Register Call Summary for PCIe_ECC1_VECTOR

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_VECTOR Register \(Offset = 8h\) \[reset = X\]: \[0\] \[1\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\] \[2\] \[3\]](#)

9.11.3 PCIE_ECC1_STAT Register (Offset = Ch) [reset = X]

PCIE_ECC1_STAT is shown in [Figure 9-1528](#) and described in [Table 9-3557](#).

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Misc Status

Table 9-3556. PCIE_ECC1_STAT Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 100Ch
PCIE1_CORE_ECC_AGGR1	02A0 300Ch
PCIE2_CORE_ECC_AGGR1	02A0 500Ch
PCIE3_CORE_ECC_AGGR1	02A0 700Ch

Figure 9-1528. PCIE_ECC1_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											NUM_RAMs																				
R-X											R-7h																				

LEGEND: R = Read Only; -n = value after reset

Table 9-3557. PCIE_ECC1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	7h	Indicates the number of RAMs serviced by the ECC aggregator

Table 9-3558. Register Call Summary for PCIE_ECC1_STAT

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_STAT Register \(Offset = Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.4 PCIE_ECC1_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

PCIE_ECC1_RESERVED_SVBUS_y is shown in Figure 9-1529 and described in Table 9-3560.

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Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 9-3559. PCIE_ECC1_RESERVED_SVBUS_y
Instances**

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1010h + formula
PCIE1_CORE_ECC_AGGR1	02A0 3010h + formula
PCIE2_CORE_ECC_AGGR1	02A0 5010h + formula
PCIE3_CORE_ECC_AGGR1	02A0 7010h + formula

Figure 9-1529. PCIE_ECC1_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3560. PCIE_ECC1_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

Table 9-3561. Register Call Summary for PCIE_ECC1_RESERVED_SVBUS_y

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_RESERVED_SVBUS_y Register \(Offset = 10h + formula\) \[reset = 0h\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.5 PCIE_ECC1_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

PCIE_ECC1_SEC_EOI_REG is shown in Figure 9-1530 and described in Table 9-3563.

Return to [Summary Table](#).

EOI Register

Table 9-3562. PCIE_ECC1_SEC_EOI_REG Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 103Ch
PCIE1_CORE_ECC_AGGR1	02A0 303Ch
PCIE2_CORE_ECC_AGGR1	02A0 503Ch
PCIE3_CORE_ECC_AGGR1	02A0 703Ch

Figure 9-1530. PCIE_ECC1_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3563. PCIE_ECC1_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

Table 9-3564. Register Call Summary for PCIE_ECC1_SEC_EOI_REG

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.6 PCIE_ECC1_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

PCIE_ECC1_SEC_STATUS_REG0 is shown in [Figure 9-1531](#) and described in [Table 9-3566](#).

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 9-3565. PCIE_ECC1_SEC_STATUS_REG0
Instances**

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1040h
PCIE1_CORE_ECC_AGGR1	02A0 3040h
PCIE2_CORE_ECC_AGGR1	02A0 5040h
PCIE3_CORE_ECC_AGGR1	02A0 7040h

Figure 9-1531. PCIE_ECC1_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	HP_AXISRODR_RAMECC_PEND	AXISRODR_RAMECC_PEND	RPLYBUF_RAMECC_PEND	HP_RXCPLFIFO_RAMECC_PEND	RXCPLFIFO_RAMECC_PEND	HP_PNPFFIFO_RAMECC_PEND	PNPFFIFO_RAMECC_PEND
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3566. PCIE_ECC1_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	HP_AXISRODR_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_axisrodr_amecc_pend
5	AXISRODR_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for axisrodr_amecc_pend
4	RPLYBUF_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for rplybuf_amecc_pend
3	HP_RXCPLFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_rxcpfifo_amecc_pend
2	RXCPLFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for rxcpfifo_amecc_pend
1	HP_PNPFFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_pnpfifo_amecc_pend
0	PNPFFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pnpfifo_amecc_pend

Table 9-3567. Register Call Summary for PCIE_ECC1_SEC_STATUS_REG0

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.7 PCIE_ECC1_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

PCIE_ECC1_SEC_ENABLE_SET_REG0 is shown in Figure 9-1532 and described in Table 9-3569.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 9-3568.
PCIE_ECC1_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1080h
PCIE1_CORE_ECC_AGGR1	02A0 3080h
PCIE2_CORE_ECC_AGGR1	02A0 5080h
PCIE3_CORE_ECC_AGGR1	02A0 7080h

Figure 9-1532. PCIE_ECC1_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	HP_AXISRODR_RAMECC_ENABLE_SET	AXISRODR_RAMECC_ENABLE_SET	RPLYBUF_RAMECC_ENABLE_SET	HP_RXCPLFIFO_RAMECC_ENABLE_SET	RXCPLFIFO_RAMECC_ENABLE_SET	HP_PNPFIFO_RAMECC_ENABLE_SET	PNPFIFO_RAMECC_ENABLE_SET
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3569. PCIE_ECC1_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	HP_AXISRODR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_axisrodr_amecc_pend
5	AXISRODR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for axisrodr_amecc_pend
4	RPLYBUF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for rplybuf_amecc_pend
3	HP_RXCPLFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_rxcplfifo_amecc_pend
2	RXCPLFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for rxcplfifo_amecc_pend
1	HP_PNPFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_pnplfifo_amecc_pend
0	PNPFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pnplfifo_amecc_pend

Table 9-3570. Register Call Summary for PCIE_ECC1_SEC_ENABLE_SET_REG0

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = X\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.8 PCIe_ECC1_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

PCIe_ECC1_SEC_ENABLE_CLR_REG0 is shown in [Figure 9-1533](#) and described in [Table 9-3572](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 9-3571.
PCIe_ECC1_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 10C0h
PCIE1_CORE_ECC_AGGR1	02A0 30C0h
PCIE2_CORE_ECC_AGGR1	02A0 50C0h
PCIE3_CORE_ECC_AGGR1	02A0 70C0h

Figure 9-1533. PCIe_ECC1_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	HP_AXISRODR_RAMECC_EN ABLE_CLR	AXISRODR_RA MECC_ENABL E_CLR	RPLYBUF_RA MECC_ENABL E_CLR	HP_RXCPLFIF O_RAMECC_E NABLE_CLR	RXCPLFIFO_R AMECC_ENAB LE_CLR	HP_PNPFIPO_ RAMECC_ENA BLE_CLR	PNPFIPO_RAM ECC_ENABLE_ CLR
R/W-X	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3572. PCIe_ECC1_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	HP_AXISRODR_RAMECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_axisrodr_amecc_pend
5	AXISRODR_RAMECC_E NABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for axisrodr_amecc_pend
4	RPLYBUF_RAMECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for rplybuf_amecc_pend
3	HP_RXCPLFIFO_RAMECC_E NABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_rxcpfifo_amecc_pend
2	RXCPLFIFO_RAMECC_E NABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for rxcpfifo_amecc_pend
1	HP_PNPFIPO_RAMECC_E NABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_pnpfifo_amecc_pend
0	PNPFIPO_RAMECC_E NABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pnpfifo_amecc_pend

Table 9-3573. Register Call Summary for PCIE_ECC1_SEC_ENABLE_CLR_REG0

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = X\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.9 PCIE_ECC1_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

PCIE_ECC1_DED_EOI_REG is shown in Figure 9-1534 and described in Table 9-3575.

Return to [Summary Table](#).

EOI Register

Table 9-3574. PCIE_ECC1_DED_EOI_REG Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 113Ch
PCIE1_CORE_ECC_AGGR1	02A0 313Ch
PCIE2_CORE_ECC_AGGR1	02A0 513Ch
PCIE3_CORE_ECC_AGGR1	02A0 713Ch

Figure 9-1534. PCIE_ECC1_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3575. PCIE_ECC1_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

Table 9-3576. Register Call Summary for PCIE_ECC1_DED_EOI_REG

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = X\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.10 PCIE_ECC1_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

PCIE_ECC1_DED_STATUS_REG0 is shown in Figure 9-1535 and described in Table 9-3578.

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Interrupt Status Register 0

**Table 9-3577. PCIE_ECC1_DED_STATUS_REG0
Instances**

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1140h
PCIE1_CORE_ECC_AGGR1	02A0 3140h
PCIE2_CORE_ECC_AGGR1	02A0 5140h
PCIE3_CORE_ECC_AGGR1	02A0 7140h

Figure 9-1535. PCIE_ECC1_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	HP_AXISRODR_RAMECC_PEND	AXISRODR_RAMECC_PEND	RPLYBUF_RAMECC_PEND	HP_RXCPLFIFO_RAMECC_PEND	RXCPLFIFO_RAMECC_PEND	HP_PNPFFIFO_RAMECC_PEND	PNPFFIFO_RAMECC_PEND
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3578. PCIE_ECC1_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	HP_AXISRODR_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_axisrodr_amecc_pending
5	AXISRODR_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for axisrodr_amecc_pending
4	RPLYBUF_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for rplybuf_amecc_pending
3	HP_RXCPLFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_rxcplfifo_amecc_pending
2	RXCPLFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for rxcplfifo_amecc_pending
1	HP_PNPFFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for hp_pnpfifo_amecc_pending
0	PNPFFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pnpfifo_amecc_pending

Table 9-3579. Register Call Summary for PCIE_ECC1_DED_STATUS_REG0

PCIE_ECC_AGGR1 Registers
<ul style="list-style-type: none">• PCIE_ECC1_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]: [0]• PCIE_ECC_AGGR1 Registers: [0] [1]

9.11.11 PCIE_ECC1_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

PCIE_ECC1_DED_ENABLE_SET_REG0 is shown in Figure 9-1536 and described in Table 9-3581.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 9-3580.
PCIE_ECC1_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1180h
PCIE1_CORE_ECC_AGGR1	02A0 3180h
PCIE2_CORE_ECC_AGGR1	02A0 5180h
PCIE3_CORE_ECC_AGGR1	02A0 7180h

Figure 9-1536. PCIE_ECC1_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	HP_AXISRODR_RAMECC_ENABLE_SET	AXISRODR_RAMECC_ENABLE_SET	RPLYBUF_RAMECC_ENABLE_SET	HP_RXCPLFIFO_RAMECC_ENABLE_SET	RXCPLFIFO_RAMECC_ENABLE_SET	HP_PNPFIFO_RAMECC_ENABLE_SET	PNPFIFO_RAMECC_ENABLE_SET
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3581. PCIE_ECC1_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	HP_AXISRODR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_axisrodr_amecc_pend
5	AXISRODR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for axisrodr_amecc_pend
4	RPLYBUF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for rplybuf_amecc_pend
3	HP_RXCPLFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_rxcplfifo_amecc_pend
2	RXCPLFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for rxcplfifo_amecc_pend
1	HP_PNPFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for hp_pnpfifo_amecc_pend
0	PNPFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pnpfifo_amecc_pend

Table 9-3582. Register Call Summary for PCIE_ECC1_DED_ENABLE_SET_REG0

PCIE_ECC_AGGR1 Registers
<ul style="list-style-type: none">• PCIE_ECC1_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]: [0]• PCIE_ECC_AGGR1 Registers: [0] [1]

9.11.12 PCIE_ECC1_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

PCIE_ECC1_DED_ENABLE_CLR_REG0 is shown in Figure 9-1537 and described in Table 9-3584.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 9-3583.
PCIE_ECC1_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 11C0h
PCIE1_CORE_ECC_AGGR1	02A0 31C0h
PCIE2_CORE_ECC_AGGR1	02A0 51C0h
PCIE3_CORE_ECC_AGGR1	02A0 71C0h

Figure 9-1537. PCIE_ECC1_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	HP_AXISRODR_RAMECC_ENABLE_CLR	AXISRODR_RAMECC_ENABLE_CLR	RPLYBUF_RAMECC_ENABLE_CLR	HP_RXCPLFIFO_RAMECC_ENABLE_CLR	RXCPLFIFO_RAMECC_ENABLE_CLR	HP_PNPFIFO_RAMECC_ENABLE_CLR	PNPFIFO_RAMECC_ENABLE_CLR
R/W-X	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3584. PCIE_ECC1_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	HP_AXISRODR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_axisrodr_amecc_pend
5	AXISRODR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for axisrodr_amecc_pend
4	RPLYBUF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for rplybuf_amecc_pend
3	HP_RXCPLFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_rxcpfifo_amecc_pend
2	RXCPLFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for rxcpfifo_amecc_pend
1	HP_PNPFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for hp_pnpfifo_amecc_pend
0	PNPFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pnpfifo_amecc_pend

Table 9-3585. Register Call Summary for PCIE_ECC1_DED_ENABLE_CLR_REG0

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = X\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.13 PCIE_ECC1_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

PCIE_ECC1_AGGR_ENABLE_SET is shown in Figure 9-1538 and described in Table 9-3587.

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 9-3586. PCIE_ECC1_AGGR_ENABLE_SET Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1200h
PCIE1_CORE_ECC_AGGR1	02A0 3200h
PCIE2_CORE_ECC_AGGR1	02A0 5200h
PCIE3_CORE_ECC_AGGR1	02A0 7200h

Figure 9-1538. PCIE_ECC1_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-3587. PCIE_ECC1_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

Table 9-3588. Register Call Summary for PCIE_ECC1_AGGR_ENABLE_SET

PCIE_ECC_AGGR1 Registers

- PCIE_ECC1_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]: [0]
- PCIE_ECC_AGGR1 Registers: [0] [1]

9.11.14 PCIE_ECC1_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

PCIE_ECC1_AGGR_ENABLE_CLR is shown in [Figure 9-1539](#) and described in [Table 9-3590](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 9-3589. PCIE_ECC1_AGGR_ENABLE_CLR Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1204h
PCIE1_CORE_ECC_AGGR1	02A0 3204h
PCIE2_CORE_ECC_AGGR1	02A0 5204h
PCIE3_CORE_ECC_AGGR1	02A0 7204h

Figure 9-1539. PCIE_ECC1_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-3590. PCIE_ECC1_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

Table 9-3591. Register Call Summary for PCIE_ECC1_AGGR_ENABLE_CLR

PCIE_ECC_AGGR1 Registers

- [PCIE_ECC1_AGGR_ENABLE_CLR Register \(Offset = 204h\) \[reset = X\]: \[0\]](#)
- [PCIE_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.11.15 PCIE_ECC1_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

PCIE_ECC1_AGGR_STATUS_SET is shown in Figure 9-1540 and described in Table 9-3593.

Return to [Summary Table](#).

AGGR interrupt status set Register

Table 9-3592. PCIE_ECC1_AGGR_STATUS_SET Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 1208h
PCIE1_CORE_ECC_AGGR1	02A0 3208h
PCIE2_CORE_ECC_AGGR1	02A0 5208h
PCIE3_CORE_ECC_AGGR1	02A0 7208h

Figure 9-1540. PCIE_ECC1_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 9-3593. PCIE_ECC1_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

Table 9-3594. Register Call Summary for PCIE_ECC1_AGGR_STATUS_SET

PCIE_ECC_AGGR1 Registers	
•	PCIE_ECC1_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]: [0]
•	PCIE_ECC_AGGR1 Registers: [0] [1]

9.11.16 PCIe_ECC1_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

PCIe_ECC1_AGGR_STATUS_CLR is shown in [Figure 9-1541](#) and described in [Table 9-3596](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

Table 9-3595. PCIe_ECC1_AGGR_STATUS_CLR Instances

Instance	Physical Address
PCIE0_CORE_ECC_AGGR1	02A0 120Ch
PCIE1_CORE_ECC_AGGR1	02A0 320Ch
PCIE2_CORE_ECC_AGGR1	02A0 520Ch
PCIE3_CORE_ECC_AGGR1	02A0 720Ch

Figure 9-1541. PCIe_ECC1_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 9-3596. PCIe_ECC1_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

Table 9-3597. Register Call Summary for PCIe_ECC1_AGGR_STATUS_CLR

PCIe_ECC_AGGR1 Registers

- [PCIe_ECC1_AGGR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = X\]: \[0\]](#)
- [PCIe_ECC_AGGR1 Registers: \[0\] \[1\]](#)

9.12 PCIE_HP_DAT0 Registers

Table 9-3599 lists the memory-mapped registers for the PCIE_HP_DAT0. All register offset addresses not listed in Table 9-3599 should be considered as reserved locations and the register contents should not be modified.

PCIE HP data region0

Table 9-3598. PCIE_HP_DAT0 Instances

Instance	Base Address
PCIE0_DAT0	1000 0000h
PCIE1_DAT0	1800 0000h
PCIE2_DAT0	440000 0000h
PCIE3_DAT0	441000 0000h

Table 9-3599. PCIE_HP_DAT0 Registers - 1

Offset	Acronym	Register Name	PCIE0_DAT0 Physical Address	PCIE1_DAT0 Physical Address
0h + formula	PCIE_HP_DATA_MEM_Y	PCie data region0	1000 0000h + formula	1800 0000h + formula

Table 9-3600. PCIE_HP_DAT0 Registers - 2

Offset	Acronym	Register Name	PCIE2_DAT0 Physical Address	PCIE3_DAT0 Physical Address
0h + formula	PCIE_HP_DATA_MEM_Y	PCie data region0	440000 0000h + formula	441000 0000h + formula

9.12.1 PCIE_HP_DATA_MEM_Y Register (Offset = 0h + formula) [reset = 0h]

PCIE_HP_DATA_MEM_Y is shown in [Figure 9-1542](#) and described in [Table 9-3602](#).

Return to [Summary Table](#).

PCIE data region0

Offset = 0h + (y * 4h); where y = 0h to 03FFFFFFh

Table 9-3601. PCIE_HP_DATA_MEM_Y Instances

Instance	Physical Address
PCIE0_DAT0	1000 0000h + formula
PCIE1_DAT0	1800 0000h + formula
PCIE2_DAT0	440000 0000h + formula
PCIE3_DAT0	441000 0000h + formula

Figure 9-1542. PCIE_HP_DATA_MEM_Y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCIE_HP_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3602. PCIE_HP_DATA_MEM_Y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PCIE_HP_DATA	R/W	0h	PCIE data region0

Table 9-3603. Register Call Summary for PCIE_HP_DATA_MEM_Y

PCIE_HP_DAT1 Registers
<ul style="list-style-type: none"> PCIE_HP_DATA_MEM_Y Register (Offset = 0h + formula) [reset = 0h]: [0] PCIE_HP_DAT1 Registers: [0] [1]
PCIE_HP_DAT0 Registers
<ul style="list-style-type: none"> PCIE_HP_DAT0 Registers: [0] [1] PCIE_HP_DATA_MEM_Y Register (Offset = 0h + formula) [reset = 0h]: [0]

9.13 PCIE_HP_DAT1 Registers

Table 9-3605 lists the memory-mapped registers for the PCIE_HP_DAT1. All register offset addresses not listed in Table 9-3605 should be considered as reserved locations and the register contents should not be modified.

PCIE HP data region1

Table 9-3604. PCIE_HP_DAT1 Instances

Instance	Base Address
PCIE0_DAT1	400000 0000h
PCIE1_DAT1	410000 0000h
PCIE2_DAT1	420000 0000h
PCIE3_DAT1	430000 0000h

Table 9-3605. PCIE_HP_DAT1 Registers - 1

Offset	Acronym	Register Name	PCIE0_DAT1 Physical Address	PCIE1_DAT1 Physical Address
0h + formula	PCIE_HP_DATA_MEM_Y	PCie data region1	400000 0000h + formula	410000 0000h + formula

Table 9-3606. PCIE_HP_DAT1 Registers - 2

Offset	Acronym	Register Name	PCIE2_DAT1 Physical Address	PCIE3_DAT1 Physical Address
0h + formula	PCIE_HP_DATA_MEM_Y	PCie data region1	420000 0000h + formula	430000 0000h + formula

9.13.1 PCIE_HP_DATA_MEM_Y Register (Offset = 0h + formula) [reset = 0h]

PCIE_HP_DATA_MEM_Y is shown in [Figure 9-1543](#) and described in [Table 9-3608](#).

Return to [Summary Table](#).

PCIe data region1

Offset = 0h + (y * 4h); where y = 0h to 03FFFFFFh

Table 9-3607. PCIE_HP_DATA_MEM_Y Instances

Instance	Physical Address
PCIE0_DAT1	400000 0000h + formula
PCIE1_DAT1	410000 0000h + formula
PCIE2_DAT1	420000 0000h + formula
PCIE3_DAT1	430000 0000h + formula

Figure 9-1543. PCIE_HP_DATA_MEM_Y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCIE_HP_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3608. PCIE_HP_DATA_MEM_Y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PCIE_HP_DATA	R/W	0h	PCIe data region1

Table 9-3609. Register Call Summary for PCIE_HP_DATA_MEM_Y

PCIE_HP_DAT1 Registers
<ul style="list-style-type: none"> PCIE_HP_DATA_MEM_Y Register (Offset = 0h + formula) [reset = 0h]: [0] PCIE_HP_DAT1 Registers: [0] [1]
PCIE_HP_DAT0 Registers
<ul style="list-style-type: none"> PCIE_HP_DAT0 Registers: [0] [1] PCIE_HP_DATA_MEM_Y Register (Offset = 0h + formula) [reset = 0h]: [0]

9.14 PCIE_USER_CFG Registers

Table 9-3611 lists the memory-mapped registers for the PCIE_USER_CFG. All register offset addresses not listed in Table 9-3611 should be considered as reserved locations and the register contents should not be modified.

PCIE Gen4x2 user config registers. Local host access only.

Table 9-3610. PCIE_USER_CFG Instances

Instance	Base Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7000h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7000h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7000h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7000h

Table 9-3611. PCIE_USER_CFG Registers - 1

Offset	Acronym	Register Name	PCIE0_CORE_USER_CFG Physical Address	PCIE1_CORE_USER_CFG Physical Address
0h	PCIE_USER_REVID		0290 7000h	0291 7000h
4h	PCIE_USER_CMD_STATUS		0290 7004h	0291 7004h
8h	PCIE_USER_RSTCMD		0290 7008h	0291 7008h
Ch	PCIE_USER_INITCFG		0290 700Ch	0291 700Ch
10h	PCIE_USER_PMCMD		0290 7010h	0291 7010h
14h	PCIE_USER_LINKSTATUS		0290 7014h	0291 7014h
18h	PCIE_USER_LEGACY_INTR_SET		0290 7018h	0291 7018h
1Ch	PCIE_USER_LEGACY_INT_PENDING		0290 701Ch	0291 701Ch
20h	PCIE_USER_MSI_STAT		0290 7020h	0291 7020h
24h	PCIE_USER_MSI_VECTOR		0290 7024h	0291 7024h
28h	PCIE_USER_MSI_MASK_PF0		0290 7028h	0291 7028h
2Ch	PCIE_USER_MSI_MASK_PF1		0290 702Ch	0291 702Ch
30h	PCIE_USER_MSI_MASK_PF2		0290 7030h	0291 7030h
34h	PCIE_USER_MSI_MASK_PF3		0290 7034h	0291 7034h
38h	PCIE_USER_MSI_MASK_PF4		0290 7038h	0291 7038h
3Ch	PCIE_USER_MSI_MASK_PF5		0290 703Ch	0291 703Ch
40h	PCIE_USER_MSI_PENDING_STATUS_PF0		0290 7040h	0291 7040h
44h	PCIE_USER_MSI_PENDING_STATUS_PF1		0290 7044h	0291 7044h
48h	PCIE_USER_MSI_PENDING_STATUS_PF2		0290 7048h	0291 7048h
4Ch	PCIE_USER_MSI_PENDING_STATUS_PF3		0290 704Ch	0291 704Ch
50h	PCIE_USER_MSI_PENDING_STATUS_PF4		0290 7050h	0291 7050h
54h	PCIE_USER_MSI_PENDING_STATUS_PF5		0290 7054h	0291 7054h
58h	PCIE_USER_MSI_STAT_VF		0290 7058h	0291 7058h
5Ch	PCIE_USER_MSI_VECTOR0_VF		0290 705Ch	0291 705Ch
60h	PCIE_USER_MSI_VECTOR1_VF		0290 7060h	0291 7060h
64h	PCIE_USER_MSI_MASK_VF0		0290 7064h	0291 7064h
68h	PCIE_USER_MSI_MASK_VF1		0290 7068h	0291 7068h
6Ch	PCIE_USER_MSI_MASK_VF2		0290 706Ch	0291 706Ch
70h	PCIE_USER_MSI_MASK_VF3		0290 7070h	0291 7070h

Table 9-3611. PCIe_USER_CFG Registers - 1 (continued)

Offset	Acronym	Register Name	PCIE0_CORE_US ER_CFG_USER_ CFG Physical Address	PCIE1_CORE_US ER_CFG_USER_ CFG Physical Address
74h	PCIE_USER_MSI_MASK_VF4		0290 7074h	0291 7074h
78h	PCIE_USER_MSI_MASK_VF5		0290 7078h	0291 7078h
7Ch	PCIE_USER_MSI_MASK_VF6		0290 707Ch	0291 707Ch
80h	PCIE_USER_MSI_MASK_VF7		0290 7080h	0291 7080h
84h	PCIE_USER_MSI_MASK_VF8		0290 7084h	0291 7084h
88h	PCIE_USER_MSI_MASK_VF9		0290 7088h	0291 7088h
8Ch	PCIE_USER_MSI_MASK_VF10		0290 708Ch	0291 708Ch
90h	PCIE_USER_MSI_MASK_VF11		0290 7090h	0291 7090h
94h	PCIE_USER_MSI_MASK_VF12		0290 7094h	0291 7094h
98h	PCIE_USER_MSI_MASK_VF13		0290 7098h	0291 7098h
9Ch	PCIE_USER_MSI_MASK_VF14		0290 709Ch	0291 709Ch
A0h	PCIE_USER_MSI_MASK_VF15		0290 70A0h	0291 70A0h
A4h	PCIE_USER_MSIX_STAT		0290 70A4h	0291 70A4h
A8h	PCIE_USER_MSIX_MASK		0290 70A8h	0291 70A8h
ACh	PCIE_USER_MSIX_STAT_VF		0290 70ACh	0291 70ACh
B0h	PCIE_USER_MSIX_MASK_VF		0290 70B0h	0291 70B0h
B4h	PCIE_USER_FLR_DONE		0290 70B4h	0291 70B4h
B8h	PCIE_USER_VF_FLR_DONE		0290 70B8h	0291 70B8h
BCh	PCIE_USER_PTM_TIMER_LOW		0290 70BCh	0291 70BCh
C0h	PCIE_USER_PTM_TIMER_HIGH		0290 70C0h	0291 70C0h

Table 9-3612. PCIe_USER_CFG Registers - 2

Offset	Acronym	Register Name	PCIE2_CORE_US ER_CFG_USER_ CFG Physical Address	PCIE3_CORE_US ER_CFG_USER_ CFG Physical Address
0h	PCIE_USER_REVID		0292 7000h	0293 7000h
4h	PCIE_USER_CMD_STATUS		0292 7004h	0293 7004h
8h	PCIE_USER_RSTCMD		0292 7008h	0293 7008h
Ch	PCIE_USER_INITCFG		0292 700Ch	0293 700Ch
10h	PCIE_USER_PMCMD		0292 7010h	0293 7010h
14h	PCIE_USER_LINKSTATUS		0292 7014h	0293 7014h
18h	PCIE_USER_LEGACY_INTR_SET		0292 7018h	0293 7018h
1Ch	PCIE_USER_LEGACY_INT_PENDING		0292 701Ch	0293 701Ch
20h	PCIE_USER_MSI_STAT		0292 7020h	0293 7020h
24h	PCIE_USER_MSI_VECTOR		0292 7024h	0293 7024h
28h	PCIE_USER_MSI_MASK_PF0		0292 7028h	0293 7028h
2Ch	PCIE_USER_MSI_MASK_PF1		0292 702Ch	0293 702Ch
30h	PCIE_USER_MSI_MASK_PF2		0292 7030h	0293 7030h
34h	PCIE_USER_MSI_MASK_PF3		0292 7034h	0293 7034h
38h	PCIE_USER_MSI_MASK_PF4		0292 7038h	0293 7038h
3Ch	PCIE_USER_MSI_MASK_PF5		0292 703Ch	0293 703Ch
40h	PCIE_USER_MSI_PENDING_STATUS_PF0		0292 7040h	0293 7040h
44h	PCIE_USER_MSI_PENDING_STATUS_PF1		0292 7044h	0293 7044h
48h	PCIE_USER_MSI_PENDING_STATUS_PF2		0292 7048h	0293 7048h
4Ch	PCIE_USER_MSI_PENDING_STATUS_PF3		0292 704Ch	0293 704Ch

Table 9-3612. PCIE_USER_CFG Registers - 2 (continued)

Offset	Acronym	Register Name	PCIE2_CORE_US ER_CFG_USER_ CFG Physical Address	PCIE3_CORE_US ER_CFG_USER_ CFG Physical Address
50h	PCIE_USER_MSI_PENDING_STATUS_PF4		0292 7050h	0293 7050h
54h	PCIE_USER_MSI_PENDING_STATUS_PF5		0292 7054h	0293 7054h
58h	PCIE_USER_MSI_STAT_VF		0292 7058h	0293 7058h
5Ch	PCIE_USER_MSI_VECTOR0_VF		0292 705Ch	0293 705Ch
60h	PCIE_USER_MSI_VECTOR1_VF		0292 7060h	0293 7060h
64h	PCIE_USER_MSI_MASK_VF0		0292 7064h	0293 7064h
68h	PCIE_USER_MSI_MASK_VF1		0292 7068h	0293 7068h
6Ch	PCIE_USER_MSI_MASK_VF2		0292 706Ch	0293 706Ch
70h	PCIE_USER_MSI_MASK_VF3		0292 7070h	0293 7070h
74h	PCIE_USER_MSI_MASK_VF4		0292 7074h	0293 7074h
78h	PCIE_USER_MSI_MASK_VF5		0292 7078h	0293 7078h
7Ch	PCIE_USER_MSI_MASK_VF6		0292 707Ch	0293 707Ch
80h	PCIE_USER_MSI_MASK_VF7		0292 7080h	0293 7080h
84h	PCIE_USER_MSI_MASK_VF8		0292 7084h	0293 7084h
88h	PCIE_USER_MSI_MASK_VF9		0292 7088h	0293 7088h
8Ch	PCIE_USER_MSI_MASK_VF10		0292 708Ch	0293 708Ch
90h	PCIE_USER_MSI_MASK_VF11		0292 7090h	0293 7090h
94h	PCIE_USER_MSI_MASK_VF12		0292 7094h	0293 7094h
98h	PCIE_USER_MSI_MASK_VF13		0292 7098h	0293 7098h
9Ch	PCIE_USER_MSI_MASK_VF14		0292 709Ch	0293 709Ch
A0h	PCIE_USER_MSI_MASK_VF15		0292 70A0h	0293 70A0h
A4h	PCIE_USER_MSIX_STAT		0292 70A4h	0293 70A4h
A8h	PCIE_USER_MSIX_MASK		0292 70A8h	0293 70A8h
ACh	PCIE_USER_MSIX_STAT_VF		0292 70ACh	0293 70ACh
B0h	PCIE_USER_MSIX_MASK_VF		0292 70B0h	0293 70B0h
B4h	PCIE_USER_FLR_DONE		0292 70B4h	0293 70B4h
B8h	PCIE_USER_VF_FLR_DONE		0292 70B8h	0293 70B8h
BCh	PCIE_USER_PTM_TIMER_LOW		0292 70BCh	0293 70BCh
C0h	PCIE_USER_PTM_TIMER_HIGH		0292 70C0h	0293 70C0h

9.14.1 PCIE_USER_REVID Register (Offset = 0h) [reset = 68128100h]

PCIE_USER_REVID is shown in [Figure 9-1544](#) and described in [Table 9-3614](#).

[Return to Summary Table.](#)

Module ID register

Table 9-3613. PCIE_USER_REVID Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7000h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7000h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7000h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7000h

Figure 9-1544. PCIE_USER_REVID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-6812h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM				REVMIN			
R-10h				R-1h				R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 9-3614. PCIE_USER_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6812h	Module ID field
15-11	REVRTL	R	10h	RTL revision. Will vary depending on release
10-8	REVMAJ	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	0h	Minor revision

Table 9-3615. Register Call Summary for PCIE_USER_REVID

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_REVID Register \(Offset = 0h\) \[reset = 68128100h\]: \[0\]](#)

9.14.2 PCIE_USER_CMD_STATUS Register (Offset = 4h) [reset = X]

PCIE_USER_CMD_STATUS is shown in [Figure 9-1545](#) and described in [Table 9-3617](#).

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Command Status register

Table 9-3616. PCIE_USER_CMD_STATUS Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7004h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7004h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7004h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7004h

Figure 9-1545. PCIE_USER_CMD_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							LINK_TRAINING_ENABLE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3617. PCIE_USER_CMD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	LINK_TRAINING_ENABLE	R/W	0h	This bit must be set to 1 to enable the LTSSM to bring up the link. Setting it to 0 forces the LTSSM to stay in the Detect.Quiet state.

Table 9-3618. Register Call Summary for PCIE_USER_CMD_STATUS

PCIE Subsystem Functional Description	
PCIE_USER_CFG Registers	
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_CMD_STATUS Register (Offset = 4h) [reset = X]: [0] 	

9.14.3 PCIE_USER_RSTCMD Register (Offset = 8h) [reset = X]

PCIE_USER_RSTCMD is shown in [Figure 9-1546](#) and described in [Table 9-3620](#).

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Reset Command and Status register

Table 9-3619. PCIE_USER_RSTCMD Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7008h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7008h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7008h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7008h

Figure 9-1546. PCIE_USER_RSTCMD Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							INIT_HOT_RESET
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3620. PCIE_USER_RSTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	INIT_HOT_RESET	R/W	0h	When this bit is set to 1'b1 in the RP mode, the core initiates a Hot Reset sequence on the PCIe link. The controller will keep the PCIe link in hot reset till the time this bit asserted. When de-asserted, controller will bring the PCIe link out of hot reset and initiate link training.

Table 9-3621. Register Call Summary for PCIE_USER_RSTCMD

PCIe Subsystem Functional Description
<ul style="list-style-type: none"> Root Port Reset with Device Not Reset: [0] End Point Device Reset with Root Port Not Reset: [0]
PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_RSTCMD Register (Offset = 8h) [reset = X]: [0]

9.14.4 PCIE_USER_INITCFG Register (Offset = Ch) [reset = X]

PCIE_USER_INITCFG is shown in [Figure 9-1547](#) and described in [Table 9-3623](#).

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Initialization configuration register

Table 9-3622. PCIE_USER_INITCFG Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 700Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 700Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 700Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 700Ch

Figure 9-1547. PCIE_USER_INITCFG Register

31	30	29	28	27	26	25	24
RESERVED							CONFIG_ENABLE
R/W-X							R/W-1h
23	22	21	20	19	18	17	16
VC_COUNT		MAX_EVAL_ITERATION					
R/W-3h		R/W-8h					
15	14	13	12	11	10	9	8
MAX_EVAL_ITERATION	BYPASS_PHASE23	BYPASS_REMOVE_TX_EQUALIZATION	SUPPORTED_PRESET				
R/W-8h	R/W-0h	R/W-0h	R/W-7FFh				
7	6	5	4	3	2	1	0
SUPPORTED_PRESET						DISABLE_GEN3_DC_BALANCE	SRIS_ENABLE
R/W-7FFh						R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3623. PCIE_USER_INITCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	CONFIG_ENABLE	R/W	1h	<p>When this bit is set to 0 in the EP mode, the Controller will generate a CRS Completion in response to Configuration Requests.</p> <p>When this bit is set to 1 in the EP mode, the Controller will generate SC/UR Completion in response to Configuration Requests based on the target function.</p> <p>In systems where the Controller configuration registers are loaded from RAM on power-up, this prevents the Controller from responding to Configuration Requests before all the registers are loaded.</p> <p>This bit is unused in RP Mode.</p> <p>The default value of this bit will be 1 in EP mode and 0 in RP mode</p>

Table 9-3623. PCIE_USER_INITCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-22	VC_COUNT	R/W	3h	Number of VCs configured. 00 = 1 VC 01 = 2 VCs, 10 = 3 VCs, 11 = 4 VCs, .. and so on
21-15	MAX_EVAL_ITERATION	R/W	8h	Denotes the maximum number of iterations to be performed during the DirectionChange Feedback Link Equalization in case the direction change feedback does not converge to 00. Supported values are 8-63. Recommended Value is from 8-16 to avoid the 24ms timeout as defined in PCIe spec.
14	BYPASS_PHASE23	R/W	0h	This MMR should be programmed during system boot or initialization. This is used only in Root Port Mode of the PCIe Core. If BYPASS_PHASE23== 1: * Phase 2 AND Phase 3 of Link Equalization are bypassed during link equalization If BYPASS_PHASE23== 0: * Phase 2 AND Phase 3 of Link Equalization are performed during link equalization
13	BYPASS_REMOTE_TX_EQUALIZATION	R/W	0h	This MMR should be programmed during system boot or initialization. IF BYPASS_REMOTE_TX_EQUALIZATION== 1: * In End-Point mode, Phase 2 of link equalization is bypassed * In Root-Port mode, Phase 3 of link equalization is bypassed IF BYPASS_REMOTE_TX_EQUALIZATION== 0: * Remote TX Equalization is performed during link equalization
12-2	SUPPORTED_PRESET	R/W	7FFh	This MMR should be programmed during system boot or initialization. SUPPORTED_PRESET[i]=1. Indicates Preset #i supported by PHY. SUPPORTED_PRESET[i]=0. Indicates Preset #i is not supported by PHY. * For Full Swing, all presets [P0 - P10] must be supported. * For Reduced Swing, [P4, P1, P9, P5, P6, P3] must be supported, others are optional as per PCIe spec.

Table 9-3623. PCIE_USER_INITCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DISABLE_GEN3_DC_BALANCE	R/W	0h	<p>This bit it is used to disable the transmission of special DC Balance symbols in TS1 training sequences for improving the DC balance of the bit stream at 8.0 GT/s or higher speed.</p> <p>This feature was introduced in the 0.71 version of the Gen3 spec. Setting this input to 1 disables the transmission of the special DC Balance symbols by the Controller.</p> <p>Note that the Controller can decode received training sequences with the special DC balance symbols in them correctly regardless of the setting of this input.</p>
0	SRIS_ENABLE	R/W	1h	<p>Should be set as per the System Reference Clocking Implementation.</p> <p>0 = Separate Tx and Rx Reference Clocks with No Spread Spectrum Clocking - SRNS Mode</p> <p>1 = Separate Tx and Rx Reference Clocks with Spread Spectrum Clocking - SRIS Mode.</p> <p>This is the default setting.</p> <p>Note that the common Refclk architecture utilizes the same Refclk for Tx and Rx and so does not introduce any difference between the Tx and Rx Refclk rates.</p> <p>SRIS_ENABLE should be tied to 0 in this case also.</p>

Table 9-3624. Register Call Summary for PCIE_USER_INITCFG

PCle Subsystem Functional Description
PCIE_USER_CFG Registers <ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_INITCFG Register (Offset = Ch) [reset = X]: [0]

9.14.5 PCIe_USER_PMCMD Register (Offset = 10h) [reset = X]

PCIe_USER_PMCMD is shown in [Figure 9-1548](#) and described in [Table 9-3626](#).

[Return to Summary Table.](#)

Power Management command register

Table 9-3625. PCIe_USER_PMCMD Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7010h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7010h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7010h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7010h

Figure 9-1548. PCIe_USER_PMCMD Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					POWER_STATE_CHANGE_ACK	CLIENT_REQ_EXIT_L1_SUBSTATE	CLIENT_REQ_EXIT_L1
R/W-X					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3626. PCIe_USER_PMCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	POWER_STATE_CHANGE_ACK	R/W	0h	Software must assert this bit for a minimum of one cycle in response to the assertion of POWER_STATE_CHANGE_INTERRUPT, when it is ready to transition to the low-power state requested by the configuration write request. Software may maintain this input high if it does not need to delay the return of the completions for the configuration write transactions causing power-state changes.

Table 9-3626. PCIE_USER_PMCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLIENT_REQ_EXIT_L1_SUBSTATE	R/W	0h	<p>Client logic can trigger an explicit L1-substate exit by setting this bit.</p> <p>This bit triggers an exit from L1-substates to L0 if controller is already in L1-substates.</p> <p>Controller waits in L1 state for this signal to become de-asserted before entering L1-substate.</p> <p>Controller will respond to normal L1-exit triggers while it waits for de-assertion of this bit.</p>
0	CLIENT_REQ_EXIT_L1	R/W	0h	<p>Client logic can trigger an explicit L1 exit by setting this bit.</p> <p>This bit triggers an exit to L0 from L1 or from L1-substates.</p> <p>This bit can also be used to block L1 entry in End point controllers.</p>

Table 9-3627. Register Call Summary for PCIE_USER_PMCMD

PCIE Subsystem Functional Description <ul style="list-style-type: none"> • PCIE Subsystem Power Management: [0] [1] [2] [3] • Power Management Event Interrupt: [0]
PCIE_USER_CFG Registers <ul style="list-style-type: none"> • PCIE_USER_PMCMD Register (Offset = 10h) [reset = X]: [0] • PCIE_USER_CFG Registers: [0] [1]

9.14.6 PCIE_USER_LINKSTATUS Register (Offset = 14h) [reset = X]

PCIE_USER_LINKSTATUS is shown in [Figure 9-1549](#) and described in [Table 9-3629](#).

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Link Status register

Table 9-3628. PCIE_USER_LINKSTATUS Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7014h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7014h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7014h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7014h

Figure 9-1549. PCIE_USER_LINKSTATUS Register

31	30	29	28	27	26	25	24
RESERVED				LTSSM_STATE			
R-X				R-0h			
23	22	21	20	19	18	17	16
POWER_STATE_CHANGE_FUNCTION_NUM							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		L1_PM_SUBSTATE			LINK_POWER_STATE		
R-X		R-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED			NEGOTIATED_SPEED		NEGOTIATED_LINK_WIDTH	LINK_STATUS	
R-X			R-0h		R-1h	R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 9-3629. PCIE_USER_LINKSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29-24	LTSSM_STATE	R	0h	Current state of the Link Training and Status State Machine within the core.
23-16	POWER_STATE_CHANGE_FUNCTION_NUM	R	0h	Function number of the function for which a power state change occurred. Software can read this value when the power_state_change interrupt is asserted to determine the physical function for which the power state change occurred.
15	RESERVED	R	X	

Table 9-3629. PCIE_USER_LINKSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	L1_PM_SUBSTATE	R	0h	This register provides the current state of the L1 PM substates state machine. Its encodings are: 000 = L 1-substate machine not active 001 = L1.0 substate. L1_PM_SUBSTATE shows "L1.0" after the delay programmed in L1 substate entry delay in reg:low_power_debug_control0 010 = L1.1 substate 011 = Reserved 100 = L1.2.Entry substate 101 = L1.2.Idle substate 110 = L1.2.Exit substate 111 = Reserved
11-8	LINK_POWER_STATE	R	0h	Current power state of the PCIe link. 0001 = L0 0010 = L0s 0100 = L1 1000 = L2
7-5	RESERVED	R	X	
4-3	NEGOTIATED_SPEED	R	0h	Current operating speed of the link is as follows: 11: 16 GT/s 10: 8GT/s 01: 5GT/s 00: 2.5GT/s
2	NEGOTIATED_LINK_WIDTH	R	1h	Current link width are as follows: 1: x2 0: x1 Others: Reserved
1-0	LINK_STATUS	R	0h	Status of the PCI Express link. 00 = No receivers detected. 01 = Link training in progress. 10 = Link up, DL initialization in progress. 11 = Link up, DL initialization completed.

Table 9-3630. Register Call Summary for PCIE_USER_LINKSTATUS

PCIE Subsystem Functional Description <ul style="list-style-type: none"> Power Management Event Interrupt: [0]
PCIE_USER_CFG Registers <ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_LINKSTATUS Register (Offset = 14h) [reset = X]: [0]

9.14.7 PCIE_USER_LEGACY_INTR_SET Register (Offset = 18h) [reset = X]

PCIE_USER_LEGACY_INTR_SET is shown in [Figure 9-1550](#) and described in [Table 9-3632](#).

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Legacy interrupt set register

Table 9-3631. PCIE_USER_LEGACY_INTR_SET Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7018h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7018h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7018h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7018h

Figure 9-1550. PCIE_USER_LEGACY_INTR_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				INTD_IN	INTC_IN	INTB_IN	INTA_IN
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3632. PCIE_USER_LEGACY_INTR_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	INTD_IN	R/W	0h	When the core is configured as EP, this bit is used by the client application to signal an interrupt from any of its PCI Functions to the RP using the Legacy PCI Express Interrupt Delivery mechanism of PCI Express. This bit corresponds to INTD of the PCI bus. Asserting this bit causes the core to send out an Assert_INTx message, and de-asserting this bit causes the core to transmit a Deassert_INTx message.
2	INTC_IN	R/W	0h	When the core is configured as EP, this bit is used by the client application to signal an interrupt from any of its PCI Functions to the RP using the Legacy PCI Express Interrupt Delivery mechanism of PCI Express. This bit corresponds to INTC of the PCI bus. Asserting this bit causes the core to send out an Assert_INTx message, and de-asserting this bit causes the core to transmit a Deassert_INTx message.

Table 9-3632. PCIE_USER_LEGACY_INTR_SET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	INTB_IN	R/W	0h	<p>When the core is configured as EP, this bit is used by the client application to signal an interrupt from any of its PCI Functions to the RP using the Legacy PCI Express Interrupt Delivery mechanism of PCI Express.</p> <p>This bit corresponds to INTB of the PCI bus.</p> <p>Asserting this bit causes the core to send out an Assert_INTx message, and de-asserting this bit causes the core to transmit a Deassert_INTx message.</p>
0	INTA_IN	R/W	0h	<p>When the core is configured as EP, this bit is used by the client application to signal an interrupt from any of its PCI Functions to the RP using the Legacy PCI Express Interrupt Delivery mechanism of PCI Express.</p> <p>This bit corresponds to INTA of the PCI bus.</p> <p>Asserting this bit causes the core to send out an Assert_INTx message, and de-asserting this bit causes the core to transmit a Deassert_INTx message.</p>

Table 9-3633. Register Call Summary for PCIE_USER_LEGACY_INTR_SET

PCle Subsystem Functional Description <ul style="list-style-type: none"> Legacy Interrupt Generation in EP Mode: [0]
PCIE_USER_CFG Registers <ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_LEGACY_INTR_SET Register (Offset = 18h) [reset = X]: [0]

9.14.8 PCIE_USER_LEGACY_INT_PENDING Register (Offset = 1Ch) [reset = X]

PCIE_USER_LEGACY_INT_PENDING is shown in [Figure 9-1551](#) and described in [Table 9-3635](#).

Return to [Summary Table](#).

Legacy interrupt pending set register

Table 9-3634. PCIE_USER_LEGACY_INT_PENDING Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 701Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 701Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 701Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 701Ch

Figure 9-1551. PCIE_USER_LEGACY_INT_PENDING Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										INT_PENDING_STATUS					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3635. PCIE_USER_LEGACY_INT_PENDING Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	INT_PENDING_STATUS	R/W	0h	When using legacy interrupts, this input is used to indicate the interrupt pending status of the Physical Functions. The bit i must be set when an interrupt is pending in Function i.

Table 9-3636. Register Call Summary for PCIE_USER_LEGACY_INT_PENDING

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_LEGACY_INT_PENDING Register \(Offset = 1Ch\) \[reset = X\]: \[0\]](#)

9.14.9 PCIE_USER_MSI_STAT Register (Offset = 20h) [reset = X]

PCIE_USER_MSI_STAT is shown in [Figure 9-1552](#) and described in [Table 9-3638](#).

[Return to Summary Table.](#)

MSI status register

Table 9-3637. PCIE_USER_MSI_STAT Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7020h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7020h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7020h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7020h

Figure 9-1552. PCIE_USER_MSI_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										MSI_ENABLE					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 9-3638. PCIE_USER_MSI_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	MSI_ENABLE	R	0h	When the core is configured in the EndPoint mode to support MSI interrupts, this output is driven by the MSI Enable bit of the MSI Control Registers of the Physical Functions. Bit0 represents the MSI Enable for Physical Function0 and Bit1 represents the MSI Enable for Physical Function 1

Table 9-3639. Register Call Summary for PCIE_USER_MSI_STAT

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_STAT Register (Offset = 20h) [reset = X]: [0]

9.14.10 PCIE_USER_MSI_VECTOR Register (Offset = 24h) [reset = X]

PCIE_USER_MSI_VECTOR is shown in [Figure 9-1553](#) and described in [Table 9-3641](#).

[Return to Summary Table.](#)

MSI vector register

Table 9-3640. PCIE_USER_MSI_VECTOR Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7024h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7024h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7024h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7024h

Figure 9-1553. PCIE_USER_MSI_VECTOR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MSI_VECTOR_COUNT																	
R-X														R-0h																	

LEGEND: R = Read Only; -n = value after reset

Table 9-3641. PCIE_USER_MSI_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17-0	MSI_VECTOR_COUNT	R	0h	When the core is configured in the EndPoint mode to support MSI interrupts, these outputs are driven by the Multiple Message Enable bits of the MSI Control Registers associated with Physical Functions. These bits encode the number of allocated MSI interrupt vectors for the corresponding Function. Bits [2:0] represents Physical Function0 and Bits [5:3] represents Physical Function 1

Table 9-3642. Register Call Summary for PCIE_USER_MSI_VECTOR

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_VECTOR Register \(Offset = 24h\) \[reset = X\]: \[0\]](#)

9.14.11 PCIE_USER_MSI_MASK_PF0 Register (Offset = 28h) [reset = 0h]

PCIE_USER_MSI_MASK_PF0 is shown in [Figure 9-1554](#) and described in [Table 9-3644](#).

Return to [Summary Table](#).

PF0 MSI mask register

Table 9-3643. PCIE_USER_MSI_MASK_PF0 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7028h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7028h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7028h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7028h

Figure 9-1554. PCIE_USER_MSI_MASK_PF0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_PF0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3644. PCIE_USER_MSI_MASK_PF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_PF0	R	0h	These bits provide the setting of the MSI Mask registers of the Physical Function0.

Table 9-3645. Register Call Summary for PCIE_USER_MSI_MASK_PF0

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_MASK_PF0 Register (Offset = 28h) [reset = 0h]: [0]

9.14.12 PCIE_USER_MSI_MASK_PF1 Register (Offset = 2Ch) [reset = 0h]

PCIE_USER_MSI_MASK_PF1 is shown in [Figure 9-1555](#) and described in [Table 9-3647](#).

Return to [Summary Table](#).

PF1 MSI mask register

**Table 9-3646. PCIE_USER_MSI_MASK_PF1
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 702Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 702Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 702Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 702Ch

Figure 9-1555. PCIE_USER_MSI_MASK_PF1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_PF1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3647. PCIE_USER_MSI_MASK_PF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_PF1	R	0h	These bits provide the setting of the MSI Mask registers of the Physical Function1.

Table 9-3648. Register Call Summary for PCIE_USER_MSI_MASK_PF1

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_MASK_PF1 Register (Offset = 2Ch) [reset = 0h]: [0]

9.14.13 PCIE_USER_MSI_MASK_PF2 Register (Offset = 30h) [reset = 0h]

PCIE_USER_MSI_MASK_PF2 is shown in [Figure 9-1556](#) and described in [Table 9-3650](#).

Return to [Summary Table](#).

PF2 MSI mask register

Table 9-3649. PCIE_USER_MSI_MASK_PF2 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7030h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7030h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7030h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7030h

Figure 9-1556. PCIE_USER_MSI_MASK_PF2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_PF2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3650. PCIE_USER_MSI_MASK_PF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_PF2	R	0h	These bits provide the setting of the MSI Mask registers of the Physical Function2.

Table 9-3651. Register Call Summary for PCIE_USER_MSI_MASK_PF2

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_PF2 Register \(Offset = 30h\) \[reset = 0h\]: \[0\]](#)

9.14.14 PCIE_USER_MSI_MASK_PF3 Register (Offset = 34h) [reset = 0h]

PCIE_USER_MSI_MASK_PF3 is shown in [Figure 9-1557](#) and described in [Table 9-3653](#).

Return to [Summary Table](#).

PF3 MSI mask register

**Table 9-3652. PCIE_USER_MSI_MASK_PF3
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7034h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7034h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7034h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7034h

Figure 9-1557. PCIE_USER_MSI_MASK_PF3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_PF3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3653. PCIE_USER_MSI_MASK_PF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_PF3	R	0h	These bits provide the setting of the MSI Mask registers of the Physical Function3.

Table 9-3654. Register Call Summary for PCIE_USER_MSI_MASK_PF3

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_PF3 Register \(Offset = 34h\) \[reset = 0h\]: \[0\]](#)

9.14.15 PCIE_USER_MSI_MASK_PF4 Register (Offset = 38h) [reset = 0h]

PCIE_USER_MSI_MASK_PF4 is shown in [Figure 9-1558](#) and described in [Table 9-3656](#).

Return to [Summary Table](#).

PF4 MSI mask register

Table 9-3655. PCIE_USER_MSI_MASK_PF4 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7038h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7038h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7038h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7038h

Figure 9-1558. PCIE_USER_MSI_MASK_PF4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_PF4																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3656. PCIE_USER_MSI_MASK_PF4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_PF4	R	0h	These bits provide the setting of the MSI Mask registers of the Physical Function4.

Table 9-3657. Register Call Summary for PCIE_USER_MSI_MASK_PF4

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_PF4 Register \(Offset = 38h\) \[reset = 0h\]: \[0\]](#)

9.14.16 PCIE_USER_MSI_MASK_PF5 Register (Offset = 3Ch) [reset = 0h]

PCIE_USER_MSI_MASK_PF5 is shown in [Figure 9-1559](#) and described in [Table 9-3659](#).

Return to [Summary Table](#).

PF5 MSI mask register

**Table 9-3658. PCIE_USER_MSI_MASK_PF5
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 703Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 703Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 703Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 703Ch

Figure 9-1559. PCIE_USER_MSI_MASK_PF5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_PF5																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3659. PCIE_USER_MSI_MASK_PF5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_PF5	R	0h	These bits provide the setting of the MSI Mask registers of the Physical Function5.

Table 9-3660. Register Call Summary for PCIE_USER_MSI_MASK_PF5

PCIE_USER_CFG Registers

- [PCIE_USER_MSI_MASK_PF5 Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)
- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)

9.14.17 PCIE_USER_MSI_PENDING_STATUS_PFO Register (Offset = 40h) [reset = 0h]

PCIE_USER_MSI_PENDING_STATUS_PFO is shown in [Figure 9-1560](#) and described in [Table 9-3662](#).

Return to [Summary Table](#).

PF0 MSI pending status input register

Table 9-3661.
PCIE_USER_MSI_PENDING_STATUS_PFO Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7040h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7040h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7040h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7040h

Figure 9-1560. PCIE_USER_MSI_PENDING_STATUS_PFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_PENDING_STATUS_PFO																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3662. PCIE_USER_MSI_PENDING_STATUS_PFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_PENDING_STATUS_PFO	R/W	0h	These inputs provide the status of the MSI pending interrupts for the Physical Function0 from the client to the core. If MSI Pending Status In Mode Select is set to 1 in the Debug Mux Control 2 register in local management, the setting of this register determines the value read from the MSI Pending Bits Register PF0.

Table 9-3663. Register Call Summary for PCIE_USER_MSI_PENDING_STATUS_PFO

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_PENDING_STATUS_PFO Register (Offset = 40h) [reset = 0h]: [0]

9.14.18 PCIE_USER_MSI_PENDING_STATUS_PF1 Register (Offset = 44h) [reset = 0h]

PCIE_USER_MSI_PENDING_STATUS_PF1 is shown in [Figure 9-1561](#) and described in [Table 9-3665](#).

Return to [Summary Table](#).

PF1 MSI pending status input register

Table 9-3664.
PCIE_USER_MSI_PENDING_STATUS_PF1 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7044h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7044h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7044h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7044h

Figure 9-1561. PCIE_USER_MSI_PENDING_STATUS_PF1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_PENDING_STATUS_PF1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3665. PCIE_USER_MSI_PENDING_STATUS_PF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_PENDING_STATUS_PF1	R/W	0h	These inputs provide the status of the MSI pending interrupts for the Physical Function1 from the client to the core, if MSI Pending Status In Mode Select is set to 1 in the Debug Mux Control 2 register in local management, the setting of this register determines the value read from the MSI Pending Bits Register PF1.

Table 9-3666. Register Call Summary for PCIE_USER_MSI_PENDING_STATUS_PF1

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_PENDING_STATUS_PF1 Register (Offset = 44h) [reset = 0h]: [0]

9.14.19 PCIE_USER_MSI_PENDING_STATUS_PF2 Register (Offset = 48h) [reset = 0h]

PCIE_USER_MSI_PENDING_STATUS_PF2 is shown in [Figure 9-1562](#) and described in [Table 9-3668](#).

Return to [Summary Table](#).

PF2 MSI pending status input register

Table 9-3667.
PCIE_USER_MSI_PENDING_STATUS_PF2 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7048h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7048h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7048h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7048h

Figure 9-1562. PCIE_USER_MSI_PENDING_STATUS_PF2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_PENDING_STATUS_PF2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3668. PCIE_USER_MSI_PENDING_STATUS_PF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_PENDING_STATUS_PF2	R/W	0h	These inputs provide the status of the MSI pending interrupts for the Physical Function1 from the client to the core, if MSI Pending Status In Mode Select is set to 1 in the Debug Mux Control 2 register in local management, the setting of this register determines the value read from the MSI Pending Bits Register PF2.

Table 9-3669. Register Call Summary for PCIE_USER_MSI_PENDING_STATUS_PF2

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_PENDING_STATUS_PF2 Register (Offset = 48h) [reset = 0h]: [0]

9.14.20 PCIE_USER_MSI_PENDING_STATUS_PF3 Register (Offset = 4Ch) [reset = 0h]

PCIE_USER_MSI_PENDING_STATUS_PF3 is shown in [Figure 9-1563](#) and described in [Table 9-3671](#).

Return to [Summary Table](#).

PF3 MSI pending status input register

Table 9-3670.
PCIE_USER_MSI_PENDING_STATUS_PF3 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 704Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 704Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 704Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 704Ch

Figure 9-1563. PCIE_USER_MSI_PENDING_STATUS_PF3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_PENDING_STATUS_PF3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3671. PCIE_USER_MSI_PENDING_STATUS_PF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_PENDING_STATUS_PF3	R/W	0h	These inputs provide the status of the MSI pending interrupts for the Physical Function1 from the client to the core, if MSI Pending Status In Mode Select is set to 1 in the Debug Mux Control 2 register in local management,the setting of this register determines the value read from the MSI Pending Bits Register PF3.

Table 9-3672. Register Call Summary for PCIE_USER_MSI_PENDING_STATUS_PF3

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_PENDING_STATUS_PF3 Register \(Offset = 4Ch\) \[reset = 0h\]: \[0\]](#)

9.14.21 PCIE_USER_MSI_PENDING_STATUS_PF4 Register (Offset = 50h) [reset = 0h]

PCIE_USER_MSI_PENDING_STATUS_PF4 is shown in [Figure 9-1564](#) and described in [Table 9-3674](#).

Return to [Summary Table](#).

PF4 MSI pending status input register

Table 9-3673.
PCIE_USER_MSI_PENDING_STATUS_PF4 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7050h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7050h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7050h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7050h

Figure 9-1564. PCIE_USER_MSI_PENDING_STATUS_PF4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_PENDING_STATUS_PF4																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3674. PCIE_USER_MSI_PENDING_STATUS_PF4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_PENDING_STATUS_PF4	R/W	0h	These inputs provide the status of the MSI pending interrupts for the Physical Function1 from the client to the core, if MSI Pending Status In Mode Select is set to 1 in the Debug Mux Control 2 register in local management, the setting of this register determines the value read from the MSI Pending Bits Register PF4.

Table 9-3675. Register Call Summary for PCIE_USER_MSI_PENDING_STATUS_PF4

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_PENDING_STATUS_PF4 Register (Offset = 50h) [reset = 0h]: [0]

9.14.22 PCIe_USER_MSI_PENDING_STATUS_PF5 Register (Offset = 54h) [reset = 0h]

PCIE_USER_MSI_PENDING_STATUS_PF5 is shown in [Figure 9-1565](#) and described in [Table 9-3677](#).

Return to [Summary Table](#).

PF5 MSI pending status input register

Table 9-3676.
PCIE_USER_MSI_PENDING_STATUS_PF5 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7054h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7054h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7054h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7054h

Figure 9-1565. PCIe_USER_MSI_PENDING_STATUS_PF5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_PENDING_STATUS_PF5																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-3677. PCIe_USER_MSI_PENDING_STATUS_PF5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_PENDING_STATUS_PF5	R/W	0h	These inputs provide the status of the MSI pending interrupts for the Physical Function1 from the client to the core, if MSI Pending Status In Mode Select is set to 1 in the Debug Mux Control 2 register in local management,the setting of this register determines the value read from the MSI Pending Bits Register PF5.

Table 9-3678. Register Call Summary for PCIe_USER_MSI_PENDING_STATUS_PF5

PCIE_USER_CFG Registers

- [PCIE_USER_MSI_PENDING_STATUS_PF5 Register \(Offset = 54h\) \[reset = 0h\]: \[0\]](#)
- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)

9.14.23 PCIE_USER_MSI_STAT_VF Register (Offset = 58h) [reset = X]

PCIE_USER_MSI_STAT_VF is shown in [Figure 9-1566](#) and described in [Table 9-3680](#).

Return to [Summary Table](#).

MSI_VF status register

Table 9-3679. PCIE_USER_MSI_STAT_VF Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7058h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7058h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7058h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7058h

Figure 9-1566. PCIE_USER_MSI_STAT_VF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VF_MSI_ENABLE															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-3680. PCIE_USER_MSI_STAT_VF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	VF_MSI_ENABLE	R	0h	When the core is configured in the EndPoint mode to support MSI interrupts, this output is driven by the MSI Enable bit of the MSI Control Registers of the Virtual Functions. Bit0 represents the MSI Enable for Virtual Function0, Bit1 represents the MSI Enable for Virtual Function 1 and so on

Table 9-3681. Register Call Summary for PCIE_USER_MSI_STAT_VF

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_MSI_STAT_VF Register (Offset = 58h) [reset = X]: [0] PCIE_USER_CFG Registers: [0] [1]

9.14.24 PCIE_USER_MSI_VECTOR0_VF Register (Offset = 5Ch) [reset = X]

PCIE_USER_MSI_VECTOR0_VF is shown in [Figure 9-1567](#) and described in [Table 9-3683](#).

Return to [Summary Table](#).

MSI_VF vector count register0

**Table 9-3682. PCIE_USER_MSI_VECTOR0_VF
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 705Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 705Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 705Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 705Ch

Figure 9-1567. PCIE_USER_MSI_VECTOR0_VF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VF_MSI_VECTOR_COUNT0																							
R-X								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 9-3683. PCIE_USER_MSI_VECTOR0_VF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-0	VF_MSI_VECTOR_COUNT0	R	0h	When the core is configured in the Endpoint mode to support MSI interrupts, these outputs are driven by the Multiple Message Enable bits of the MSI Control Registers associated with Virtual Function0 thru Virtual Function7. These bits encode the number of allocated MSI interrupt vectors for the corresponding Function. Bits [2:0] represents Virtual Function0, Bits [5:3] represents Virtual Function 1 and so on

Table 9-3684. Register Call Summary for PCIE_USER_MSI_VECTOR0_VF

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_VECTOR0_VF Register \(Offset = 5Ch\) \[reset = X\]: \[0\]](#)

9.14.25 PCIE_USER_MSI_VECTOR1_VF Register (Offset = 60h) [reset = X]

PCIE_USER_MSI_VECTOR1_VF is shown in [Figure 9-1568](#) and described in [Table 9-3686](#).

Return to [Summary Table](#).

MSI_VF vector count register1

Table 9-3685. PCIE_USER_MSI_VECTOR1_VF Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7060h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7060h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7060h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7060h

Figure 9-1568. PCIE_USER_MSI_VECTOR1_VF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VF_MSI_VECTOR_COUNT1																							
R-X								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 9-3686. PCIE_USER_MSI_VECTOR1_VF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-0	VF_MSI_VECTOR_COUNT1	R	0h	<p>When the core is configured in the Endpoint mode to support MSI interrupts, these outputs are driven by the Multiple Message Enable bits of the MSI Control Registers associated with Virtual Function8 thru Virtual Function15.</p> <p>These bits encode the number of allocated MSI interrupt vectors for the corresponding Function.</p> <p>Bits</p> <p>[2:0] represents Virtual Function11, Bits</p> <p>[5:3] represents Virtual Function12 and so on</p>

Table 9-3687. Register Call Summary for PCIE_USER_MSI_VECTOR1_VF

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_VECTOR1_VF Register (Offset = 60h) [reset = X]: [0]

9.14.26 PCIE_USER_MSI_MASK_VF0 Register (Offset = 64h) [reset = 0h]

PCIE_USER_MSI_MASK_VF0 is shown in [Figure 9-1569](#) and described in [Table 9-3689](#).

Return to [Summary Table](#).

VF0MSI mask register

**Table 9-3688. PCIE_USER_MSI_MASK_VF0
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7064h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7064h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7064h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7064h

Figure 9-1569. PCIE_USER_MSI_MASK_VF0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3689. PCIE_USER_MSI_MASK_VF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF0	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function0.

Table 9-3690. Register Call Summary for PCIE_USER_MSI_MASK_VF0

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF0 Register \(Offset = 64h\) \[reset = 0h\]: \[0\]](#)

9.14.27 PCIE_USER_MSI_MASK_VF1 Register (Offset = 68h) [reset = 0h]

PCIE_USER_MSI_MASK_VF1 is shown in Figure 9-1570 and described in Table 9-3692.

Return to [Summary Table](#).

VF1MSI mask register

Table 9-3691. PCIE_USER_MSI_MASK_VF1 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7068h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7068h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7068h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7068h

Figure 9-1570. PCIE_USER_MSI_MASK_VF1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3692. PCIE_USER_MSI_MASK_VF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF1	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function1.

Table 9-3693. Register Call Summary for PCIE_USER_MSI_MASK_VF1

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF1 Register \(Offset = 68h\) \[reset = 0h\]: \[0\]](#)

9.14.28 PCIE_USER_MSI_MASK_VF2 Register (Offset = 6Ch) [reset = 0h]

PCIE_USER_MSI_MASK_VF2 is shown in [Figure 9-1571](#) and described in [Table 9-3695](#).

Return to [Summary Table](#).

VF2MSI mask register

**Table 9-3694. PCIE_USER_MSI_MASK_VF2
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 706Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 706Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 706Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 706Ch

Figure 9-1571. PCIE_USER_MSI_MASK_VF2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3695. PCIE_USER_MSI_MASK_VF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF2	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function2.

Table 9-3696. Register Call Summary for PCIE_USER_MSI_MASK_VF2

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_MASK_VF2 Register (Offset = 6Ch) [reset = 0h]: [0]

9.14.29 PCIE_USER_MSI_MASK_VF3 Register (Offset = 70h) [reset = 0h]

PCIE_USER_MSI_MASK_VF3 is shown in Figure 9-1572 and described in Table 9-3698.

Return to [Summary Table](#).

VF3MSI mask register

Table 9-3697. PCIE_USER_MSI_MASK_VF3 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7070h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7070h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7070h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7070h

Figure 9-1572. PCIE_USER_MSI_MASK_VF3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3698. PCIE_USER_MSI_MASK_VF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF3	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function3.

Table 9-3699. Register Call Summary for PCIE_USER_MSI_MASK_VF3

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_MSI_MASK_VF3 Register (Offset = 70h) [reset = 0h]: [0] PCIE_USER_CFG Registers: [0] [1]

9.14.30 PCIE_USER_MSI_MASK_VF4 Register (Offset = 74h) [reset = 0h]

PCIE_USER_MSI_MASK_VF4 is shown in [Figure 9-1573](#) and described in [Table 9-3701](#).

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VF4MSI mask register

**Table 9-3700. PCIE_USER_MSI_MASK_VF4
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7074h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7074h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7074h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7074h

Figure 9-1573. PCIE_USER_MSI_MASK_VF4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF4																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3701. PCIE_USER_MSI_MASK_VF4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF4	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function4.

Table 9-3702. Register Call Summary for PCIE_USER_MSI_MASK_VF4

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_MASK_VF4 Register (Offset = 74h) [reset = 0h]: [0]

9.14.31 PCIE_USER_MSI_MASK_VF5 Register (Offset = 78h) [reset = 0h]

PCIE_USER_MSI_MASK_VF5 is shown in Figure 9-1574 and described in Table 9-3704.

Return to [Summary Table](#).

VF5MSI mask register

Table 9-3703. PCIE_USER_MSI_MASK_VF5 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7078h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7078h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7078h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7078h

Figure 9-1574. PCIE_USER_MSI_MASK_VF5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF5																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3704. PCIE_USER_MSI_MASK_VF5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF5	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function5.

Table 9-3705. Register Call Summary for PCIE_USER_MSI_MASK_VF5

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_MASK_VF5 Register (Offset = 78h) [reset = 0h]: [0]

9.14.32 PCIE_USER_MSI_MASK_VF6 Register (Offset = 7Ch) [reset = 0h]

PCIE_USER_MSI_MASK_VF6 is shown in [Figure 9-1575](#) and described in [Table 9-3707](#).

Return to [Summary Table](#).

VF6MSI mask register

**Table 9-3706. PCIE_USER_MSI_MASK_VF6
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 707Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 707Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 707Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 707Ch

Figure 9-1575. PCIE_USER_MSI_MASK_VF6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF6																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3707. PCIE_USER_MSI_MASK_VF6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF6	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function6.

Table 9-3708. Register Call Summary for PCIE_USER_MSI_MASK_VF6

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF6 Register \(Offset = 7Ch\) \[reset = 0h\]: \[0\]](#)

9.14.33 PCIE_USER_MSI_MASK_VF7 Register (Offset = 80h) [reset = 0h]

PCIE_USER_MSI_MASK_VF7 is shown in [Figure 9-1576](#) and described in [Table 9-3710](#).

Return to [Summary Table](#).

VF7MSI mask register

**Table 9-3709. PCIE_USER_MSI_MASK_VF7
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7080h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7080h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7080h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7080h

Figure 9-1576. PCIE_USER_MSI_MASK_VF7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF7																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3710. PCIE_USER_MSI_MASK_VF7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF7	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function7.

Table 9-3711. Register Call Summary for PCIE_USER_MSI_MASK_VF7

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF7 Register \(Offset = 80h\) \[reset = 0h\]: \[0\]](#)

9.14.34 PCIE_USER_MSI_MASK_VF8 Register (Offset = 84h) [reset = 0h]

PCIE_USER_MSI_MASK_VF8 is shown in [Figure 9-1577](#) and described in [Table 9-3713](#).

Return to [Summary Table](#).

VF8MSI mask register

**Table 9-3712. PCIE_USER_MSI_MASK_VF8
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7084h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7084h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7084h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7084h

Figure 9-1577. PCIE_USER_MSI_MASK_VF8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF8																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3713. PCIE_USER_MSI_MASK_VF8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF8	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function8.

Table 9-3714. Register Call Summary for PCIE_USER_MSI_MASK_VF8

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF8 Register \(Offset = 84h\) \[reset = 0h\]: \[0\]](#)

9.14.35 PCIE_USER_MSI_MASK_VF9 Register (Offset = 88h) [reset = 0h]

PCIE_USER_MSI_MASK_VF9 is shown in Figure 9-1578 and described in Table 9-3716.

Return to [Summary Table](#).

VF9MSI mask register

Table 9-3715. PCIE_USER_MSI_MASK_VF9 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7088h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7088h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7088h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7088h

Figure 9-1578. PCIE_USER_MSI_MASK_VF9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF9																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3716. PCIE_USER_MSI_MASK_VF9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF9	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function9.

Table 9-3717. Register Call Summary for PCIE_USER_MSI_MASK_VF9

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF9 Register \(Offset = 88h\) \[reset = 0h\]: \[0\]](#)

9.14.36 PCIE_USER_MSI_MASK_VF10 Register (Offset = 8Ch) [reset = 0h]

PCIE_USER_MSI_MASK_VF10 is shown in Figure 9-1579 and described in Table 9-3719.

Return to [Summary Table](#).

VF10MSI mask register

**Table 9-3718. PCIE_USER_MSI_MASK_VF10
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 708Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 708Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 708Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 708Ch

Figure 9-1579. PCIE_USER_MSI_MASK_VF10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF10																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3719. PCIE_USER_MSI_MASK_VF10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF10	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function10.

Table 9-3720. Register Call Summary for PCIE_USER_MSI_MASK_VF10

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF10 Register \(Offset = 8Ch\) \[reset = 0h\]: \[0\]](#)

9.14.37 PCIE_USER_MSI_MASK_VF11 Register (Offset = 90h) [reset = 0h]

PCIE_USER_MSI_MASK_VF11 is shown in Figure 9-1580 and described in Table 9-3722.

Return to [Summary Table](#).

VF11MSI mask register

Table 9-3721. PCIE_USER_MSI_MASK_VF11 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7090h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7090h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7090h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7090h

Figure 9-1580. PCIE_USER_MSI_MASK_VF11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF11																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3722. PCIE_USER_MSI_MASK_VF11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF11	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function11.

Table 9-3723. Register Call Summary for PCIE_USER_MSI_MASK_VF11

PCIE_USER_CFG Registers	
•	PCIE_USER_CFG Registers: [0] [1]
•	PCIE_USER_MSI_MASK_VF11 Register (Offset = 90h) [reset = 0h]: [0]

9.14.38 PCIE_USER_MSI_MASK_VF12 Register (Offset = 94h) [reset = 0h]

PCIE_USER_MSI_MASK_VF12 is shown in [Figure 9-1581](#) and described in [Table 9-3725](#).

Return to [Summary Table](#).

VF12MSI mask register

**Table 9-3724. PCIE_USER_MSI_MASK_VF12
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7094h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7094h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7094h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7094h

Figure 9-1581. PCIE_USER_MSI_MASK_VF12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF12																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3725. PCIE_USER_MSI_MASK_VF12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF12	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function12.

Table 9-3726. Register Call Summary for PCIE_USER_MSI_MASK_VF12

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF12 Register \(Offset = 94h\) \[reset = 0h\]: \[0\]](#)

9.14.39 PCIE_USER_MSI_MASK_VF13 Register (Offset = 98h) [reset = 0h]

PCIE_USER_MSI_MASK_VF13 is shown in Figure 9-1582 and described in Table 9-3728.

Return to [Summary Table](#).

VF13MSI mask register

Table 9-3727. PCIE_USER_MSI_MASK_VF13 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 7098h
PCIE1_CORE_USER_CFG_USER_CFG	0291 7098h
PCIE2_CORE_USER_CFG_USER_CFG	0292 7098h
PCIE3_CORE_USER_CFG_USER_CFG	0293 7098h

Figure 9-1582. PCIE_USER_MSI_MASK_VF13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF13																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3728. PCIE_USER_MSI_MASK_VF13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF13	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function13.

Table 9-3729. Register Call Summary for PCIE_USER_MSI_MASK_VF13

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_MSI_MASK_VF13 Register (Offset = 98h) [reset = 0h]: [0] PCIE_USER_CFG Registers: [0] [1]

9.14.40 PCIE_USER_MSI_MASK_VF14 Register (Offset = 9Ch) [reset = 0h]

PCIE_USER_MSI_MASK_VF14 is shown in Figure 9-1583 and described in Table 9-3731.

Return to [Summary Table](#).

VF14MSI mask register

**Table 9-3730. PCIE_USER_MSI_MASK_VF14
Instances**

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 709Ch
PCIE1_CORE_USER_CFG_USER_CFG	0291 709Ch
PCIE2_CORE_USER_CFG_USER_CFG	0292 709Ch
PCIE3_CORE_USER_CFG_USER_CFG	0293 709Ch

Figure 9-1583. PCIE_USER_MSI_MASK_VF14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF14																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3731. PCIE_USER_MSI_MASK_VF14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF14	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function14.

Table 9-3732. Register Call Summary for PCIE_USER_MSI_MASK_VF14

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSI_MASK_VF14 Register (Offset = 9Ch) [reset = 0h]: [0]

9.14.41 PCIE_USER_MSI_MASK_VF15 Register (Offset = A0h) [reset = 0h]

PCIE_USER_MSI_MASK_VF15 is shown in Figure 9-1584 and described in Table 9-3734.

Return to [Summary Table](#).

VF15MSI mask register

Table 9-3733. PCIE_USER_MSI_MASK_VF15 Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70A0h
PCIE1_CORE_USER_CFG_USER_CFG	0291 70A0h
PCIE2_CORE_USER_CFG_USER_CFG	0292 70A0h
PCIE3_CORE_USER_CFG_USER_CFG	0293 70A0h

Figure 9-1584. PCIE_USER_MSI_MASK_VF15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSI_MASK_VF15																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3734. PCIE_USER_MSI_MASK_VF15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MSI_MASK_VF15	R	0h	These bits provide the setting of the MSI Mask registers of the Virtual Function15.

Table 9-3735. Register Call Summary for PCIE_USER_MSI_MASK_VF15

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSI_MASK_VF15 Register \(Offset = A0h\) \[reset = 0h\]: \[0\]](#)

9.14.42 PCIE_USER_MSIX_STAT Register (Offset = A4h) [reset = X]

PCIE_USER_MSIX_STAT is shown in [Figure 9-1585](#) and described in [Table 9-3737](#).

Return to [Summary Table](#).

MSIX status register

Table 9-3736. PCIE_USER_MSIX_STAT Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70A4h
PCIE1_CORE_USER_CFG_USER_CFG	0291 70A4h
PCIE2_CORE_USER_CFG_USER_CFG	0292 70A4h
PCIE3_CORE_USER_CFG_USER_CFG	0293 70A4h

Figure 9-1585. PCIE_USER_MSIX_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										MSIX_ENABLE					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 9-3737. PCIE_USER_MSIX_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	MSIX_ENABLE	R	0h	These bits reflect the states of the MSI-X Enable bits in the PCI configuration space of Physical Functions. Bit0 represents the MSIX Enable for Physical Function0 and Bit1 represents the MSIX Enable for Physical Function 1

Table 9-3738. Register Call Summary for PCIE_USER_MSIX_STAT

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSIX_STAT Register \(Offset = A4h\) \[reset = X\]: \[0\]](#)

9.14.43 PCIE_USER_MSIX_MASK Register (Offset = A8h) [reset = X]

PCIE_USER_MSIX_MASK is shown in Figure 9-1586 and described in Table 9-3740.

Return to [Summary Table](#).

MSIX mask register

Table 9-3739. PCIE_USER_MSIX_MASK Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70A8h
PCIE1_CORE_USER_CFG_USER_CFG	0291 70A8h
PCIE2_CORE_USER_CFG_USER_CFG	0292 70A8h
PCIE3_CORE_USER_CFG_USER_CFG	0293 70A8h

Figure 9-1586. PCIE_USER_MSIX_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										MSIX_MASK					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 9-3740. PCIE_USER_MSIX_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	MSIX_MASK	R	0h	These bits reflect the states of the MSI-X Function Mask bits in the PCI configuration space of Physical Functions. Bit0 represents Physical Function0 and Bit1 represents Physical Function1

Table 9-3741. Register Call Summary for PCIE_USER_MSIX_MASK

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSIX_MASK Register \(Offset = A8h\) \[reset = X\]: \[0\]](#)

9.14.44 PCIE_USER_MSIX_STAT_VF Register (Offset = ACh) [reset = X]

PCIE_USER_MSIX_STAT_VF is shown in [Figure 9-1587](#) and described in [Table 9-3743](#).

Return to [Summary Table](#).

Virtual Function MSIX status register

Table 9-3742. PCIE_USER_MSIX_STAT_VF Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70ACh
PCIE1_CORE_USER_CFG_USER_CFG	0291 70ACh
PCIE2_CORE_USER_CFG_USER_CFG	0292 70ACh
PCIE3_CORE_USER_CFG_USER_CFG	0293 70ACh

Figure 9-1587. PCIE_USER_MSIX_STAT_VF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VF_MSIX_ENABLE															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-3743. PCIE_USER_MSIX_STAT_VF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	VF_MSIX_ENABLE	R	0h	These bits reflect the states of the MSI-X Enable bits in the PCI configuration space of virtual Functions. Bit0 represents the MSIX Enable for Virtual Function0, Bit1 represents the MSIX Enable for Virtual Function 1 and so on

Table 9-3744. Register Call Summary for PCIE_USER_MSIX_STAT_VF

PCIE_USER_CFG Registers

- [PCIE_USER_CFG Registers: \[0\] \[1\]](#)
- [PCIE_USER_MSIX_STAT_VF Register \(Offset = ACh\) \[reset = X\]: \[0\]](#)

9.14.45 PCIE_USER_MSIX_MASK_VF Register (Offset = B0h) [reset = X]

PCIE_USER_MSIX_MASK_VF is shown in [Figure 9-1588](#) and described in [Table 9-3746](#).

Return to [Summary Table](#).

Virtual Function MSIX mask register

Table 9-3745. PCIE_USER_MSIX_MASK_VF Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70B0h
PCIE1_CORE_USER_CFG_USER_CFG	0291 70B0h
PCIE2_CORE_USER_CFG_USER_CFG	0292 70B0h
PCIE3_CORE_USER_CFG_USER_CFG	0293 70B0h

Figure 9-1588. PCIE_USER_MSIX_MASK_VF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VF_MSIX_MASK															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 9-3746. PCIE_USER_MSIX_MASK_VF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	VF_MSIX_MASK	R	0h	These bits reflect the states of the MSI-X Function Mask bits in the PCI configuration space of Virtual Functions. Bit0 represents Virtual Function0, Bit1 represents Virtual Function1 and so on

Table 9-3747. Register Call Summary for PCIE_USER_MSIX_MASK_VF

PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_MSIX_MASK_VF Register (Offset = B0h) [reset = X]: [0]

9.14.46 PCIE_USER_FLR_DONE Register (Offset = B4h) [reset = X]

PCIE_USER_FLR_DONE is shown in [Figure 9-1589](#) and described in [Table 9-3749](#).

Return to [Summary Table](#).

Physical Function-Level Reset Done register

Table 9-3748. PCIE_USER_FLR_DONE Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70B4h
PCIE1_CORE_USER_CFG_USER_CFG	0291 70B4h
PCIE2_CORE_USER_CFG_USER_CFG	0292 70B4h
PCIE3_CORE_USER_CFG_USER_CFG	0293 70B4h

Figure 9-1589. PCIE_USER_FLR_DONE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										FLR_DONE					
W-X										W-0h					

LEGEND: W = Write Only; -n = value after reset

Table 9-3749. PCIE_USER_FLR_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	W	X	
5-0	FLR_DONE	W	0h	<p>These bits are connected to the PCIE_USER_FLR_DONE bits on the PCIe controller core.</p> <p>In EP mode, software needs to write a 1 to bit0 within 100ms after PF0 function-level reset interrupt is asserted.</p> <p>The PCIE_USER_FLR_DONE[0] input of the PCIe controller is pulsed for one cycle to acknowledge to the core that the application level function level reset processing is complete.</p> <p>This bit will self-clear once the PCIE_USER_FLR_DONE[0] is pulsed.</p> <p>The PCIe controller will maintain FLR_IN_PROGRESS[0] output high until it is acknowledged by asserting PCIE_USER_FLR_DONE.</p> <p>Bit 1 is used to acknowledge PCIE_USER_FLR_DONE for PF1.</p> <p>These bits are not used in RP mode</p>

Table 9-3750. Register Call Summary for PCIE_USER_FLR_DONE

PCIe Subsystem Functional Description
<ul style="list-style-type: none"> PCIe Core Function Level Reset Interrupts: [0]
PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_FLR_DONE Register (Offset = B4h) [reset = X]: [0] [1] [2] [3] [4] [5]

9.14.47 PCIE_USER_VF_FLR_DONE Register (Offset = B8h) [reset = X]

PCIE_USER_VF_FLR_DONE is shown in [Figure 9-1590](#) and described in [Table 9-3752](#).

Return to [Summary Table](#).

Virtual Function-Level Reset Done register

Table 9-3751. PCIE_USER_VF_FLR_DONE Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70B8h
PCIE1_CORE_USER_CFG_USER_CFG	0291 70B8h
PCIE2_CORE_USER_CFG_USER_CFG	0292 70B8h
PCIE3_CORE_USER_CFG_USER_CFG	0293 70B8h

Figure 9-1590. PCIE_USER_VF_FLR_DONE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VF_FLR_DONE															
W-X																W-0h															

LEGEND: W = Write Only; -n = value after reset

Table 9-3752. PCIE_USER_VF_FLR_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	W	X	
15-0	VF_FLR_DONE	W	0h	<p>These bits are connected to the PCIE_USER_VF_FLR_DONE bits on the PCIe controller core.</p> <p>In EP mode, software needs to write a 1 to bit0 within 100ms after VF0 function-level reset interrupt is asserted.</p> <p>The PCIE_USER_VF_FLR_DONE[0] input of the PCIe controller is pulsed for one cycle to acknowledge to the core that the application level virtual function level reset processing is complete.</p> <p>This bit will self-clear once the PCIE_USER_VF_FLR_DONE[0] is pulsed The PCIe controller will maintain VF_FLR_IN_PROGRESS[0] output high until it is acknowledged by asserting PCIE_USER_VF_FLR_DONE[0].</p> <p>Bit 1 is used to acknowledge PCIE_USER_VF_FLR_DONE for VF1, bit2 is used to acknowledge PCIE_USER_VF_FLR_DONE for VF2 and so on.</p> <p>These bits are not used in RP mode</p>

Table 9-3753. Register Call Summary for PCIE_USER_VF_FLR_DONE

PCIE Subsystem Functional Description <ul style="list-style-type: none"> PCIE Core Function Level Reset Interrupts: [0]
PCIE_USER_CFG Registers <ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_VF_FLR_DONE Register (Offset = B8h) [reset = X]: [0] [1] [2] [3] [4] [5] [6]

9.14.48 PCIE_USER_PTM_TIMER_LOW Register (Offset = BCh) [reset = 0h]

PCIE_USER_PTM_TIMER_LOW is shown in Figure 9-1591 and described in Table 9-3755.

Return to [Summary Table](#).

PTM timer value lower 32-bits

Table 9-3754. PCIE_USER_PTM_TIMER_LOW Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70BCh
PCIE1_CORE_USER_CFG_USER_CFG	0291 70BCh
PCIE2_CORE_USER_CFG_USER_CFG	0292 70BCh
PCIE3_CORE_USER_CFG_USER_CFG	0293 70BCh

Figure 9-1591. PCIE_USER_PTM_TIMER_LOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTM_TIMER_OUT_LOW																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3755. PCIE_USER_PTM_TIMER_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTM_TIMER_OUT_LOW	R	0h	ptm_timer_out[31:0] value from PCIe core. Valid in EP mode only

Table 9-3756. Register Call Summary for PCIE_USER_PTM_TIMER_LOW

PCIe Subsystem Functional Description
<ul style="list-style-type: none"> • PCIe Subsystem Precision Time Measurement Support: [0]
PCI_USER_CFG Registers
<ul style="list-style-type: none"> • PCI_USER_CFG Registers: [0] [1] • PCIE_USER_PTM_TIMER_LOW Register (Offset = BCh) [reset = 0h]: [0]

9.14.49 PCIE_USER_PTM_TIMER_HIGH Register (Offset = C0h) [reset = 0h]

PCIE_USER_PTM_TIMER_HIGH is shown in [Figure 9-1592](#) and described in [Table 9-3758](#).

Return to [Summary Table](#).

PTM timer value upper 32-bits

Table 9-3757. PCIE_USER_PTM_TIMER_HIGH Instances

Instance	Physical Address
PCIE0_CORE_USER_CFG_USER_CFG	0290 70C0h
PCIE1_CORE_USER_CFG_USER_CFG	0291 70C0h
PCIE2_CORE_USER_CFG_USER_CFG	0292 70C0h
PCIE3_CORE_USER_CFG_USER_CFG	0293 70C0h

Figure 9-1592. PCIE_USER_PTM_TIMER_HIGH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PTM_TIMER_OUT_HIGH																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 9-3758. PCIE_USER_PTM_TIMER_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PTM_TIMER_OUT_HIGH	R	0h	ptm_timer_out[63:32] value from PCIe core. Valid in EP mode only

Table 9-3759. Register Call Summary for PCIE_USER_PTM_TIMER_HIGH

PCIE Subsystem Functional Description
<ul style="list-style-type: none"> PCIE Subsystem Precision Time Measurement Support: [0]
PCIE_USER_CFG Registers
<ul style="list-style-type: none"> PCIE_USER_CFG Registers: [0] [1] PCIE_USER_PTM_TIMER_HIGH Register (Offset = C0h) [reset = 0h]: [0]

10 USB Registers

Note

Details on the USB controller registers are not provided in this TRM. The existing Linux or RTOS drivers should be used for proper USB operation. For those who do wish to substantially modify the existing Linux or RTOS USB driver(s), or create new drivers, contact TI for more information on how to obtain the third-party documentation under NDA.

10.1 USB_ECC_AGGR_CFG Registers

Table 10-2 lists the memory-mapped registers for the USB_ECC_AGGR_CFG registers. All register offset addresses not listed in Table 10-2 should be considered as reserved locations and the register contents should not be modified.

Table 10-1. USB_ECC_AGGR_CFG Instances

Instance	Base Address
USB0_ECC_AGGR	02A1 3000h
USB1_ECC_AGGR	02A1 6000h

Table 10-2. USB_ECC_AGGR_CFG Registers

Offset	Acronym	Register Name	USB0_ECC_AGGR Physical Address	USB1_ECC_AGGR Physical Address
0h	USB_REV	Aggregator Revision Register	02A1 3000h	02A1 6000h
8h	USB_VECTOR	ECC Vector Register	02A1 3008h	02A1 6008h
Ch	USB_STAT	Misc Status	02A1 300Ch	02A1 600Ch
10h + formula	USB_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	02A1 3010h + formula	02A1 6010h + formula
3Ch	USB_SEC_EOI_REG	EOI Register	02A1 303Ch	02A1 603Ch
40h	USB_SEC_STATUS_REG0	Interrupt Status Register 0	02A1 3040h	02A1 6040h
80h	USB_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A1 3080h	02A1 6080h
C0h	USB_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A1 30C0h	02A1 60C0h
13Ch	USB_DED_EOI_REG	EOI Register	02A1 313Ch	02A1 613Ch
140h	USB_DED_STATUS_REG0	Interrupt Status Register 0	02A1 3140h	02A1 6140h
180h	USB_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	02A1 3180h	02A1 6180h
1C0h	USB_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	02A1 31C0h	02A1 61C0h
200h	USB_AGGR_ENABLE_SET	AGGR interrupt enable set Register	02A1 3200h	02A1 6200h
204h	USB_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	02A1 3204h	02A1 6204h
208h	USB_AGGR_STATUS_SET	AGGR interrupt status set Register	02A1 3208h	02A1 6208h
20Ch	USB_AGGR_STATUS_CLR	AGGR interrupt status clear Register	02A1 320Ch	02A1 620Ch

10.1.1 USB_REV Register (Offset = 0h) [reset = 66A0EA00h]

USB_REV is shown in [Figure 10-1](#) and described in [Table 10-4](#).

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Revision parameters

Table 10-3. USB_REV Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 3000h
USB1_ECC_AGGR	02A1 6000h

Figure 10-1. USB_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 10-4. USB_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

10.1.2 USB_VECTOR Register (Offset = 8h) [reset = X]

USB_VECTOR is shown in [Figure 10-2](#) and described in [Table 10-6](#).

Return to [Summary Table](#).

ECC Vector Register

Table 10-5. USB_VECTOR Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 3008h
USB1_ECC_AGGR	02A1 6008h

Figure 10-2. USB_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-6. USB_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

10.1.3 USB_STAT Register (Offset = Ch) [reset = X]

USB_STAT is shown in [Figure 10-3](#) and described in [Table 10-8](#).

Return to [Summary Table](#).

Misc Status

Table 10-7. USB_STAT Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 300Ch
USB1_ECC_AGGR	02A1 600Ch

Figure 10-3. USB_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											NUM_RAMs																				
R-X											R-1h																				

LEGEND: R = Read Only; -n = value after reset

Table 10-8. USB_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	1h	Indicates the number of RAMs serviced by the ECC aggregator

10.1.4 USB_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

USB_RESERVED_SVBUS_y is shown in [Figure 10-4](#) and described in [Table 10-10](#).

Return to [Summary Table](#).

Offset = 10h + (y * 4h); where y = 0h to 7h

Table 10-9. USB_RESERVED_SVBUS_y Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 3010h + formula
USB1_ECC_AGGR	02A1 6010h + formula

Figure 10-4. USB_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-10. USB_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

10.1.5 USB_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

USB_SEC_EOI_REG is shown in [Figure 10-5](#) and described in [Table 10-12](#).

Return to [Summary Table](#).

EOI Register

Table 10-11. USB_SEC_EOI_REG Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 303Ch
USB1_ECC_AGGR	02A1 603Ch

Figure 10-5. USB_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-12. USB_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

10.1.6 USB_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

USB_SEC_STATUS_REG0 is shown in [Figure 10-6](#) and described in [Table 10-14](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 10-13. USB_SEC_STATUS_REG0 Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 3040h
USB1_ECC_AGGR	02A1 6040h

Figure 10-6. USB_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_PEN D
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-14. USB_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for ramecc_pend

10.1.7 USB_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

USB_SEC_ENABLE_SET_REG0 is shown in [Figure 10-7](#) and described in [Table 10-16](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

**Table 10-15. USB_SEC_ENABLE_SET_REG0
Instances**

Instance	Physical Address
USB0_ECC_AGGR	02A1 3080h
USB1_ECC_AGGR	02A1 6080h

Figure 10-7. USB_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-16. USB_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc_pend

10.1.8 USB_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

USB_SEC_ENABLE_CLR_REG0 is shown in [Figure 10-8](#) and described in [Table 10-18](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 10-17. USB_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 30C0h
USB1_ECC_AGGR	02A1 60C0h

Figure 10-8. USB_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-18. USB_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc_pend

10.1.9 USB_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

USB_DED_EOI_REG is shown in [Figure 10-9](#) and described in [Table 10-20](#).

Return to [Summary Table](#).

EOI Register

Table 10-19. USB_DED_EOI_REG Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 313Ch
USB1_ECC_AGGR	02A1 613Ch

Figure 10-9. USB_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-20. USB_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

10.1.10 USB_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

USB_DED_STATUS_REG0 is shown in [Figure 10-10](#) and described in [Table 10-22](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 10-21. USB_DED_STATUS_REG0 Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 3140h
USB1_ECC_AGGR	02A1 6140h

Figure 10-10. USB_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_PEN D
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-22. USB_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for ramecc_pend

10.1.11 USB_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

USB_DED_ENABLE_SET_REG0 is shown in [Figure 10-11](#) and described in [Table 10-24](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

**Table 10-23. USB_DED_ENABLE_SET_REG0
Instances**

Instance	Physical Address
USB0_ECC_AGGR	02A1 3180h
USB1_ECC_AGGR	02A1 6180h

Figure 10-11. USB_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-24. USB_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ramecc_pend

10.1.12 USB_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

USB_DED_ENABLE_CLR_REG0 is shown in [Figure 10-12](#) and described in [Table 10-26](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 10-25. USB_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 31C0h
USB1_ECC_AGGR	02A1 61C0h

Figure 10-12. USB_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							RAMECC_ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-26. USB_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ramecc_pend

10.1.13 USB_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

USB_AGGR_ENABLE_SET is shown in [Figure 10-13](#) and described in [Table 10-28](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 10-27. USB_AGGR_ENABLE_SET Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 3200h
USB1_ECC_AGGR	02A1 6200h

Figure 10-13. USB_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-28. USB_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

10.1.14 USB_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

USB_AGGR_ENABLE_CLR is shown in [Figure 10-14](#) and described in [Table 10-30](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 10-29. USB_AGGR_ENABLE_CLR Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 3204h
USB1_ECC_AGGR	02A1 6204h

Figure 10-14. USB_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-30. USB_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

10.1.15 USB_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

USB_AGGR_STATUS_SET is shown in [Figure 10-15](#) and described in [Table 10-32](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

Table 10-31. USB_AGGR_STATUS_SET Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 3208h
USB1_ECC_AGGR	02A1 6208h

Figure 10-15. USB_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 10-32. USB_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

10.1.16 USB_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

USB_AGGR_STATUS_CLR is shown in [Figure 10-16](#) and described in [Table 10-34](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

Table 10-33. USB_AGGR_STATUS_CLR Instances

Instance	Physical Address
USB0_ECC_AGGR	02A1 320Ch
USB1_ECC_AGGR	02A1 620Ch

Figure 10-16. USB_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 10-34. USB_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

10.2 USB_RAM5_INJ_CFG Registers

Table 10-36 lists the memory-mapped registers for the USB_RAM5_INJ_CFG registers. All register offset addresses not listed in Table 10-36 should be considered as reserved locations and the register contents should not be modified.

Error Injector Registers

Table 10-35. USB_RAM5_INJ_CFG Instances

Instance	Base Address
USB0_RAM5_INJ_CFG	02A1 0000h
USB1_RAM5_INJ_CFG	02A1 7000h

Table 10-36. USB_RAM5_INJ_CFG Registers

Offset	Acronym	Register Name	USB0_RAM5_INJ_CFG Physical Address	USB1_RAM5_INJ_CFG Physical Address
0h	USB_PID	Revision Register	02A1 0000h	02A1 7000h
4h	USB_INFO	Info Register	02A1 0004h	02A1 7004h
8h	USB_SFT_RST	Global Soft Reset Register	02A1 0008h	02A1 7008h
10h	USB_BIT1	Bit 1 Mask Register	02A1 0010h	02A1 7010h
14h	USB_BIT2	Bit 2 Mask Register	02A1 0014h	02A1 7014h
18h	USB_TRGT	Target Select	02A1 0018h	02A1 7018h
1Ch	USB_CTRL	Control Register	02A1 001Ch	02A1 701Ch
20h	USB_STATUS	Control Register	02A1 0020h	02A1 7020h

10.2.1 USB_PID Register (Offset = 0h) [reset = 60000001h]

USB_PID is shown in [Figure 10-17](#) and described in [Table 10-38](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 10-37. USB_PID Instances

Instance	Physical Address
USB0_RAMC_INJ_CFG	02A1 0000h
USB1_RAMC_INJ_CFG	02A1 7000h

Figure 10-17. USB_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNC									
R-1h				R-2h		R-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-0h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 10-38. USB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	0h	Module ID
15-11	RTL	R	0h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	0h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	1h	Minor revision

10.2.2 USB_INFO Register (Offset = 4h) [reset = X]

USB_INFO is shown in [Figure 10-18](#) and described in [Table 10-40](#).

Return to [Summary Table](#).

The Info Register gives the configuration Information of this module.

Table 10-39. USB_INFO Instances

Instance	Physical Address
USB0_RAMIS_INJ_CFG	02A1 0004h
USB1_RAMIS_INJ_CFG	02A1 7004h

Figure 10-18. USB_INFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										ENDPOINTS					
R-X										R-1Eh					

LEGEND: R = Read Only; -n = value after reset

Table 10-40. USB_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	ENDPOINTS	R	1Eh	Total number of Targets supported by this configuration

10.2.3 USB_SFT_RST Register (Offset = 8h) [reset = X]

USB_SFT_RST is shown in [Figure 10-19](#) and described in [Table 10-42](#).

Return to [Summary Table](#).

The Global Soft Reset Register clears all programmable registers and returns the injector to idle state

Table 10-41. USB_SFT_RST Instances

Instance	Physical Address
USB0_RAMC_INJ_CFG	02A1 0008h
USB1_RAMC_INJ_CFG	02A1 7008h

Figure 10-19. USB_SFT_RST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												KEY			
W-X																												W-0h			

LEGEND: W = Write Only; -n = value after reset

Table 10-42. USB_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	X	
3-0	KEY	W	0h	Write 4'b1010 to issue a soft reset. All other written values are ignored. Always read as 0

10.2.4 USB_BIT1 Register (Offset = 10h) [reset = X]

USB_BIT1 is shown in [Figure 10-20](#) and described in [Table 10-44](#).

Return to [Summary Table](#).

This register defines the first bit to be flipped when injection is enabled

Table 10-43. USB_BIT1 Instances

Instance	Physical Address
USB0_RAMC_INJ_CFG	02A1 0010h
USB1_RAMC_INJ_CFG	02A1 7010h

Figure 10-20. USB_BIT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BIT1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-44. USB_BIT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	BIT1	R/W	0h	First bit to be flipped on an error injection

10.2.5 USB_BIT2 Register (Offset = 14h) [reset = X]

USB_BIT2 is shown in [Figure 10-21](#) and described in [Table 10-46](#).

Return to [Summary Table](#).

This register defines the second bit to be flipped if 2-bit injection is enabled

Table 10-45. USB_BIT2 Instances

Instance	Physical Address
USB0_RAMC_INJ_CFG	02A1 0014h
USB1_RAMC_INJ_CFG	02A1 7014h

Figure 10-21. USB_BIT2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BIT2															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-46. USB_BIT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	BIT2	R/W	0h	Second bit to be flipped on an error injection if 2-bit injection is chosen.

10.2.6 USB_TRGT Register (Offset = 18h) [reset = X]

USB_TRGT is shown in [Figure 10-22](#) and described in [Table 10-48](#).

Return to [Summary Table](#).

This is the target selection register

Table 10-47. USB_TRGT Instances

Instance	Physical Address
USB0_RAM5_INJ_CFG	02A1 0018h
USB1_RAM5_INJ_CFG	02A1 7018h

Figure 10-22. USB_TRGT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												TRGT			
R/W-X																												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-48. USB_TRGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	TRGT	R/W	0h	Select which target to interact with. Writes of a value higher than the number of targets supported by this configuration will have no effect

10.2.7 USB_CTRL Register (Offset = 1Ch) [reset = X]

USB_CTRL is shown in [Figure 10-23](#) and described in [Table 10-50](#).

Return to [Summary Table](#).

Controls the injection

Table 10-49. USB_CTRL Instances

Instance	Physical Address
USB0_RAMIS_INJ_CFG	02A1 001Ch
USB1_RAMIS_INJ_CFG	02A1 701Ch

Figure 10-23. USB_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				TRGT			
R/W-X				R-0h			
7	6	5	4	3	2	1	0
RESERVED					DONE	TWOBIT	ONEBIT
R/W-X					R-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-50. USB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12-8	TRGT	R	0h	Indicates which target is selected by the USB_TRGT register
7-3	RESERVED	R/W	X	
2	DONE	R	0h	Indicates that the target selected by USB_TRGT has completed error injection. This USB_STATUS supercedes the armed bit
1	TWOBIT	R/W	0h	Write 1 to trigger a 2-bit error in target selected by USB_TRGT register. Write 0 to finish or cancel 2-bit injection. If both 1 and 2-bit injection are set, 2-bit injection will be performed
0	ONEBIT	R/W	0h	Write 1 to trigger a 1-bit error in target selected by USB_TRGT register. Write 0 to finish or cancel 1-bit injection

10.2.8 USB_STATUS Register (Offset = 20h) [reset = X]

USB_STATUS is shown in [Figure 10-24](#) and described in [Table 10-52](#).

Return to [Summary Table](#).

Controls the injection

Table 10-51. USB_STATUS Instances

Instance	Physical Address
USB0_RAMC_INJ_CFG	02A1 0020h
USB1_RAMC_INJ_CFG	02A1 7020h

Figure 10-24. USB_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED					ARMED	RESERVED	
R-X					R-0h	R-X	

LEGEND: R = Read Only; -n = value after reset

Table 10-52. USB_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	X	
2	ARMED	R	0h	Indicates that the target selected by USB_TRGT is ARMED for error injection
1-0	RESERVED	R	X	

10.3 USB2 PHY Registers

[Table 10-53](#) lists the memory-mapped registers for the USB_RAMC_INJ_CFG registers. All register offset addresses not listed in [Table 10-53](#) should be considered as reserved locations and the register contents should not be modified.

Table 10-53. PHY2, PHY2 Registers, Base Address=0x04118000, Length=1024

Offset	Length	Acronym	Register Name	USB0	Section
4 h	1	AFE_TX_REG1	AFE_TX_REG1	04108004h	Section 10.3.1
8 h	1	AFE_TX_REG2	AFE_TX_REG2	04108008h	Section 10.3.2
30 h	1	AFE_TX_REG12	AFE_TX_REG12	04108030h	Section 10.3.3

10.3.1 USB0_AFE_TX_REG1 Register (Offset = 4 h) [reset = 0]

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Return to [Summary Table](#)
Table 10-54. Instance Table

Instance Name	Base Address
USB0	04108004h

Figure 10-25. AFE_TX_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_AN A_RE G1	BF_6_1				BF_0		
NONE								R/W	R/W				R/W		
								0	0				0		

Table 10-55. AFE_TX_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7	tx_ana_reg1_1	R/W	0h	0 SCALE1 VALUE IS 0, 1 SCALE1 VALUE IS 0.5
6 - 1	BF_6_1	R/W	0h	000000 BOOST CODE VALUE IS 0, 000001 BOOST CODE VALUE IS 1, 000010 BOOST CODE VALUE IS 2, 000011 BOOST CODE VALUE IS 3, 000100 BOOST CODE VALUE IS 4, 000101 BOOST CODE VALUE IS 5, 000110 BOOST CODE VALUE IS 6, 000111 BOOST CODE VALUE IS 7, 001000 BOOST CODE VALUE IS 8, 001001 BOOST CODE VALUE IS 9, 001010 BOOST CODE VALUE IS 10, 001011 BOOST CODE VALUE IS 11, 001100 BOOST CODE VALUE IS 12, 001101 BOOST CODE VALUE IS 13, 001110 BOOST CODE VALUE IS 14, 001111 BOOST CODE VALUE IS 15, 010000 BOOST CODE VALUE IS 16, 010001 BOOST CODE VALUE IS 17, 010010 BOOST CODE VALUE IS 18, 010011 BOOST CODE VALUE IS 19, 010100 BOOST CODE VALUE IS 20, 010101 BOOST CODE VALUE IS 21, 010110 BOOST CODE VALUE IS 22, 010111 BOOST CODE VALUE IS 23, 011000 BOOST CODE VALUE IS 24, 011001 BOOST CODE VALUE IS 25, 011010 BOOST CODE VALUE IS 26, 011011 BOOST CODE VALUE IS 27, 011100 BOOST CODE VALUE IS 28, 011101 BOOST CODE VALUE IS 29, 011110 BOOST CODE VALUE IS 30, 011111 BOOST CODE VALUE IS 31, 100000 BOOST CODE VALUE IS 32, 100001 BOOST CODE VALUE IS 33, 100010 BOOST CODE VALUE IS 34, 100011 BOOST CODE VALUE IS 35, 100100 BOOST CODE VALUE IS 36, 100101 BOOST CODE VALUE IS 37, 100110 BOOST CODE VALUE IS 38, 100111 BOOST CODE VALUE IS 39, 101000 BOOST CODE VALUE IS 40, 101001 BOOST CODE VALUE IS 41, 101010 BOOST CODE VALUE IS 42, 101011 BOOST CODE VALUE IS 43, 101100 BOOST CODE VALUE IS 44, 101101 BOOST CODE VALUE IS 45, 101110 BOOST CODE VALUE IS 46, 101111 BOOST CODE VALUE IS 47
0	x_ana_reg1_3	R/W	0h	0 Default BOOST CODE = 8, 1 BOOST CODE can be controlled by BITS <6:1>

10.3.2 USB0_AFE_TX_REG2 Register (Offset = 8 h) [reset = 0]

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Return to [Summary Table](#)

Table 10-56. Instance Table

Instance Name	Base Address
USB0	04108008h

Figure 10-26. AFE_TX_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_AN A_RE G2	BF_6	BF_5_1				BF_0	
NONE								R/W	R/W	R/W				R/W	
								0	0	0				0	

Table 10-57. AFE_TX_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7- 6	x_ana_reg2_1	R/W	0h	Reserved
5 - 1	x_ana_reg2_2	R/W	0h	00000 DEEMP CODE VALUE IS 0, 00001 DEEMP CODE VALUE IS 1, 00010 DEEMP CODE VALUE IS 2, 00011 DEEMP CODE VALUE IS 3, 00100 DEEMP CODE VALUE IS 4, 00101 DEEMP CODE VALUE IS 5, 00110 DEEMP CODE VALUE IS 6, 00111 DEEMP CODE VALUE IS 7, 01000 DEEMP CODE VALUE IS 8, 01001 DEEMP CODE VALUE IS 9, 01010 DEEMP CODE VALUE IS 10, 01011 DEEMP CODE VALUE IS 11, 01100 DEEMP CODE VALUE IS 12, 01101 DEEMP CODE VALUE IS 13, 01110 DEEMP CODE VALUE IS 14, 01111 DEEMP CODE VALUE IS 15, 10000 DEEMP CODE VALUE IS 16, 10001 DEEMP CODE VALUE IS 17, 10010 DEEMP CODE VALUE IS 18, 10011 DEEMP CODE VALUE IS 19, 10100 DEEMP CODE VALUE IS 20, 10101 DEEMP CODE VALUE IS 21, 10110 DEEMP CODE VALUE IS 22, 10111 DEEMP CODE VALUE IS 23
0	x_ana_reg2_3	R/W	0h	0 Default DEEMP CODE = 8, 1 DEEMP CODE can be controlled by BITS <5:1>

10.3.3 USB0_AFE_TX_REG12 Register (Offset = 48 h) [reset = 0]

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Return to [Summary Table](#)
Table 10-58. Instance Table

Instance Name	Base Address
USB0	04108030h

Figure 10-27. AFE_TX_REG12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_AN A_RE G12	BF_6	BF_5	BF_4	BF_3	BF_2	BF_1_0	
NONE								R/W	R/W	R/W	R/W	R/W	R/W	R/W	
								0	0	0	0	0	0	0	

Table 10-59. AFE_TX_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 2	tx_ana_reg12_1	R/W	0h	Reserved
1 - 0	tx_ana_reg12_2	R/W	0h	00 SCALE2 set to 0, 01 SCALE2 set to 1, 10 SCALE2 set to 1, 11 SCALE2 set to 2

10.4 USB3P0SS_MMR_MMRVBP_USBSS_CMN Registers

[Table 10-61](#) lists the memory-mapped registers for the USB3P0SS_MMR_MMRVBP_USBSS_CMN registers. All register offset addresses not listed in [Table 10-61](#) should be considered as reserved locations and the register contents should not be modified.

Global Control Registers

**Table 10-60.
USB3P0SS_MMR_MMRVBP_USBSS_CMN Instances**

Instance	Base Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 4000h
USB1_MMR_MMRVBP_USBSS_CMN	0411 4000h

Table 10-61. USB3P0SS_MMR_MMRVBP_USBSS_CMN Registers

Offset	Acronym	Register Name	USB0_MMR_MM RVBP_USBSS_C MN Physical Address	USB1_MMR_MM RVBP_USBSS_C MN Physical Address
0h	USB3P0SS_PID	Revision Register	0410 4000h	0411 4000h
4h	USB3P0SS_W1	Wrapper Register 1	0410 4004h	0411 4004h
8h	USB3P0SS_STATIC_CONFIG	Static Configuration Register	0410 4008h	0411 4008h
Ch	USB3P0SS_PHY_TEST	USB2 PHY Test Control and Status	0410 400Ch	0411 400Ch
10h	USB3P0SS_DEBUG_CTRL	USB debug control	0410 4010h	0411 4010h
14h	USB3P0SS_DEBUG_INFO	USB debug information	0410 4014h	0411 4014h
18h	USB3P0SS_DEBUG_LINK_STATE	USB debug link state	0410 4018h	0411 4018h
1Ch	USB3P0SS_DEVICE_CTRL	Register for device control	0410 401Ch	0411 401Ch

10.4.1 USB3P0SS_PID Register (Offset = 0h) [reset = 68224100h]

USB3P0SS_PID is shown in [Figure 10-28](#) and described in [Table 10-63](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 10-62. USB3P0SS_PID Instances

Instance	Physical Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 4000h
USB1_MMR_MMRVBP_USBSS_CMN	0411 4000h

Figure 10-28. USB3P0SS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-822h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-8h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 10-63. USB3P0SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Register scheme
29-28	BU	R	2h	BU
27-16	MODULE_ID	R	822h	Module ID
15-11	RTL	R	8h	RTL revision.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

10.4.2 USB3P0SS_W1 Register (Offset = 4h) [reset = 00010000h]

USB3P0SS_W1 is shown in [Figure 10-29](#) and described in [Table 10-65](#).

Return to [Summary Table](#).

Wrapper register containing soft reset, mode selection, and overcurrent indicator.

Table 10-64. USB3P0SS_W1 Instances

Instance	Physical Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 4004h
USB1_MMR_MMRVBP_USBSS_CMN	0411 4004h

Figure 10-29. USB3P0SS_W1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				USB2_ONLY_MODE	MODESTRAP		OVERCURRENT_N
R-0h				R/W-0h	R/W-0h		R/W-1h
15	14	13	12	11	10	9	8
RESERVED						MODESTRAP_SEL	OVERCURRENT_SEL
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PWRUP_RST_N
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-65. USB3P0SS_W1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	USB2_ONLY_MODE	R/W	0h	Selects USB2 only mode. Has to be written before setting PWRUP_RST_N bit. This bit has to be set when SERDES is not assigned to this USB instance. For example, when the Wiz is configured to allocate the serdes lanes for another function, like PCIe. Without setting this bit in those cases, the Controller will not function even at USB2 speeds, or may be erratic.
18-17	MODESTRAP	R/W	0h	Modestrap input to the Controller. Has to be written before setting PWRUP_RST_N bit. 00 - Controller not configured as Host or Device, 01 - Controller is initially configured as Host, 10 - Controller is initially configured as Device.
16	OVERCURRENT_N	R/W	1h	Overcurrent indicator to the controller. Software writes 0 when overcurrent was detected by external circuitry.
15-10	RESERVED	R	0h	Reserved
9	MODESTRAP_SEL	R/W	0h	This bit has to be always set to 1. Has to be written before setting PWRUP_RST_N bit.

Table 10-65. USB3P0SS_W1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	OVERCURRENT_SEL	R/W	0h	Overcurrent select. Has to be written before setting PWRUP_RST_N bit. 0 - OVERCURRENT_N bit in not functional 1 - OVERCURRENT_N bit can be used
7-1	RESERVED	R	0h	Reserved
0	PWRUP_RST_N	R/W	0h	Power up reset for the controller. This bit has to be set in order to release controller from reset.

10.4.3 USB3P0SS_STATIC_CONFIG Register (Offset = 8h) [reset = 80h]

USB3P0SS_STATIC_CONFIG is shown in [Figure 10-30](#) and described in [Table 10-67](#).

Return to [Summary Table](#).

Wrapper register containing static settings. All bits in this register have to be written before setting PWRUP_RST_N bit in USB3P0SS_W1 register.

Table 10-66. USB3P0SS_STATIC_CONFIG Instances

Instance	Physical Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 4008h
USB1_MMR_MMRVBP_USBSS_CMN	0411 4008h

Figure 10-30. USB3P0SS_STATIC_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							PLL_REF_SEL
R-0h							R/W-4h
7	6	5	4	3	2	1	0
PLL_REF_SEL			RESERVED		VBUS_SEL		LANE_REVERSE
R/W-4h			R/W-0h		R/W-0h		R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-67. USB3P0SS_STATIC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8-5	PLL_REF_SEL	R/W	4h	Indicates the frequency of the REF_CLOCK input used by the USB PLL. This value must match the frequency of the HFOSC oscillator selected in CTRLMMR_USB0_CLKSEL register. 0x0 - 9.6 MHz 0x1 - 10 MHz 0x2 - 12 MHz 0x3 - 19.2 MHz 0x4 - 20 MHz 0x5 - 24 MHz 0x6 - 25 MHz 0x7 - 26 MHz 0x8 - 38.4 MHz 0x9 - 40 MHz 0xA - 48 MHz 0xB - 50 MHz 0xC - 52 MHz (Others are reserved) NOTE: Refer to <i>Mapping of Clock Inputs</i> in chapter Clocking for the supported system clock (HFOSC) speeds in this SoC.
4-3	RESERVED	R/W	0h	Reserved. Always keep at 0x0

Table 10-67. USB3P0SS_STATIC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	VBUS_SEL	R/W	0h	VBUS select. Always set to 0x1
0	LANE_REVERSE	R/W	0h	USB2PHY D+/D- reverse selection. When set, this bit causes D+ and D- lines to be swapped.

10.4.4 USB3P0SS_PHY_TEST Register (Offset = Ch) [reset = 0h]

USB3P0SS_PHY_TEST is shown in [Figure 10-31](#) and described in [Table 10-69](#).

Return to [Summary Table](#).

Register containing PLL bypass select, BIST control and status

Table 10-68. USB3P0SS_PHY_TEST Instances

Instance	Physical Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 400Ch
USB1_MMR_MMRVBP_USBSS_CMN	0411 400Ch

Figure 10-31. USB3P0SS_PHY_TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						BIST_MODE	BIST_ERROR_COUNT
R-0h						R/W-0h	R-0h
15	14	13	12	11	10	9	8
BIST_ERROR_COUNT						BIST_ERROR	
R-0h						R-0h	
7	6	5	4	3	2	1	0
BIST_COMPLETE	BIST_ON	BIST_MODE_EN	BIST_MODE_SEL				RESERVED
R-0h	R/W-0h	R/W-0h	R/W-0h				R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-69. USB3P0SS_PHY_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved bits
17	BIST_MODE	R/W	0h	Set for bist mode. This is used for overriding PHY ports for BIST.
16-9	BIST_ERROR_COUNT	R	0h	Number of bytes that have errors while running BIST. The count resets when BIST_ON is set.
8	BIST_ERROR	R	0h	If set, this bit indicates that BIST completed with error.
7	BIST_COMPLETE	R	0h	If set, this bit indicates that the BIST operation is completed.
6	BIST_ON	R/W	0h	Setting this bit starts the BIST operation.
5	BIST_MODE_EN	R/W	0h	BIST Mode Enable. 0 = BIST not enabled, 1 = BIST enabled

Table 10-69. USB3P0SS_PHY_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-1	BIST_MODE_SEL	R/W	0h	BIST Mode Selection. BIST_MODE_SEL[3]: 0 = 8-bit interface, 1 = 16-bit interface BIST_MODE_SEL[2]: 0 = error injection disabled, 1 = error injection enabled BIST_MODE_SEL[1]: 0 = device mode, 1 = host mode BIST_MODE_SEL[0]: 0 = High Speed mode, 1 = Full Speed mode.
0	RESERVED	R/W	0h	Reserved. Keep at 0x0

10.4.5 USB3P0SS_DEBUG_CTRL Register (Offset = 10h) [reset = 0h]

USB3P0SS_DEBUG_CTRL is shown in [Figure 10-32](#) and described in [Table 10-71](#).

Return to [Summary Table](#).

USB Controller debug selection register

Table 10-70. USB3P0SS_DEBUG_CTRL Instances

Instance	Physical Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 4010h
USB1_MMR_MMRVBP_USBSS_CMN	0411 4010h

Figure 10-32. USB3P0SS_DEBUG_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											DEBUG_SEL				
R-0h											R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-71. USB3P0SS_DEBUG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved bits
4-0	DEBUG_SEL	R/W	0h	Debug selection to be shown in DEBUG_INFO

10.4.6 USB3P0SS_DEBUG_INFO Register (Offset = 14h) [reset = 0h]

USB3P0SS_DEBUG_INFO is shown in [Figure 10-33](#) and described in [Table 10-73](#).

Return to [Summary Table](#).

USB Controller debug information register

Table 10-72. USB3P0SS_DEBUG_INFO Instances

Instance	Physical Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 4014h
USB1_MMR_MMRVBP_USBSS_CMN	0411 4014h

Figure 10-33. USB3P0SS_DEBUG_INFO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_INFO																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 10-73. USB3P0SS_DEBUG_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_INFO	R	0h	Debug information selected by DEBUG_SEL

10.4.7 USB3P0SS_DEBUG_LINK_STATE Register (Offset = 18h) [reset = 0h]

USB3P0SS_DEBUG_LINK_STATE is shown in [Figure 10-34](#) and described in [Table 10-75](#).

Return to [Summary Table](#).

USB Controller debug link state information

Table 10-74. USB3P0SS_DEBUG_LINK_STATE Instances

Instance	Physical Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 4018h
USB1_MMR_MMRVBP_USBSS_CMN	0411 4018h

Figure 10-34. USB3P0SS_DEBUG_LINK_STATE Register

31	30	29	28	27	26	25	24
RESERVED	DEBUG_LINK_STATE						
R-0h	R-0h						
23	22	21	20	19	18	17	16
DEBUG_LINK_STATE							
R-0h							
15	14	13	12	11	10	9	8
DEBUG_LINK_STATE							
R-0h							
7	6	5	4	3	2	1	0
DEBUG_LINK_STATE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 10-75. USB3P0SS_DEBUG_LINK_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved bits
30-0	DEBUG_LINK_STATE	R	0h	Debug link state information

10.4.8 USB3P0SS_DEVICE_CTRL Register (Offset = 1Ch) [reset = 0h]

USB3P0SS_DEVICE_CTRL is shown in [Figure 10-35](#) and described in [Table 10-77](#).

Return to [Summary Table](#).

Register for device control

Table 10-76. USB3P0SS_DEVICE_CTRL Instances

Instance	Physical Address
USB0_MMR_MMRVBP_USBSS_CMN	0410 401Ch
USB1_MMR_MMRVBP_USBSS_CMN	0411 401Ch

Figure 10-35. USB3P0SS_DEVICE_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DEV_WAKEUP
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-77. USB3P0SS_DEVICE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved bits
0	DEV_WAKEUP	R/W	0h	Set this bit to trigger device wakeup interrupt on IRQ[7]

11 2-L SerDes Registers

Table 11-2 lists the memory-mapped registers for the SERDES_16G registers. All register offset addresses not listed in Table 11-2 should be considered as reserved locations and the register contents should not be modified.

This is the register region for the SERDES_16G component. WIZ registers are overlaid and placed in the 0x400-0x7FF range.

Table 11-1. SERDES_16G Instances

Instance	Base Address
SERDES_16G0	0500 0000h
SERDES_16G1	0501 0000h
SERDES_16G2	0502 0000h
SERDES_16G3	0503 0000h

Table 11-2. SERDES_16G Registers

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
0h	MACRO_ID_REG		0500 0000h	0501 0000h
4h	MACRO_ID_NUMBER_REG		0500 0004h	0501 0004h
8h	MACRO_ID_REV_REG		0500 0008h	0501 0008h
10h	MACRO_ID_NODE_REG__MACRO_ID_MFG_REG		0500 0010h	0501 0010h
14h	MACRO_ID_FLAVOR_REG		0500 0014h	0501 0014h
18h	MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG		0500 0018h	0501 0018h
20h	MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG		0500 0020h	0501 0020h
24h	MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG		0500 0024h	0501 0024h
28h	MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG		0500 0028h	0501 0028h
40h	CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG		0500 0040h	0501 0040h
60h	CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BAND_GAP_TMR_PREG		0500 0060h	0501 0060h
64h	CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG		0500 0064h	0501 0064h
68h	CMN_SMCSM_STATE_PREG		0500 0068h	0501 0068h
80h	CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG		0500 0080h	0501 0080h
84h	CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG		0500 0084h	0501 0084h
88h	CMN_PLLLC_DCOAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG		0500 0088h	0501 0088h
8Ch	CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG		0500 008Ch	0501 008Ch
90h	CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG		0500 0090h	0501 0090h
94h	CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG		0500 0094h	0501 0094h
98h	CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG		0500 0098h	0501 0098h
9Ch	CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG		0500 009Ch	0501 009Ch
A0h	CMN_PLLLC_DSMLCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG		0500 00A0h	0501 00A0h

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
A4h	CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG		0500 00A4h	0501 00A4h
A8h	CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG		0500 00A8h	0501 00A8h
ACh	CMN_PLLLC_DSMCORR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG		0500 00ACh	0501 00ACh
B0h	CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG		0500 00B0h	0501 00B0h
B4h	CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG		0500 00B4h	0501 00B4h
B8h	CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG		0500 00B8h	0501 00B8h
BCh	CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG		0500 00BCh	0501 00BCh
C0h	CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG		0500 00C0h	0501 00C0h
C4h	CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG		0500 00C4h	0501 00C4h
D0h	SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG		0500 00D0h	0501 00D0h
D4h	SDOSCCAL_INIT_TMR_PREG__SDOSCCAL_OVR_PREG		0500 00D4h	0501 00D4h
D8h	SDOSCCAL_TMR_PREG__SDOSCCAL_ITER_TMR_PREG		0500 00D8h	0501 00D8h
DCh	SDOSCCAL_START_PREG__SDOSCCAL_CLK_CNT_PREG		0500 00DCh	0501 00DCh
E0h	PROCمون_STATUS_PREG__PROCمون_CTRL_PREG		0500 00E0h	0501 00E0h
E4h	PROCمون_CNTWAIT_PREG__PROCمون_INITWAIT_PREG		0500 00E4h	0501 00E4h
E8h	PROCمون_DIAGNOSTIC_PREG__PROCمون_OVRD_PREG		0500 00E8h	0501 00E8h
100h	CMN_CTRL_DIAG_RESET_PREG__CDB_DIAG_PREG		0500 0100h	0501 0100h
104h	CMN_FUNC_DIAG_RESET_PREG		0500 0104h	0501 0104h
108h	CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG		0500 0108h	0501 0108h
10Ch	CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG		0500 010Ch	0501 010Ch
110h	CMN_SPARE_REG_PREG		0500 0110h	0501 0110h
120h	CMN_BIAS_TRIM_PREG__CMN_BIAS_EN_OVRD_PREG		0500 0120h	0501 0120h
124h	CMN_BIAS_VREF_TRIM_PREG		0500 0124h	0501 0124h
130h	CMN_PSMCLK_SDOSCSEL_CTRL_PREG__CMN_REFRCV_PREG		0500 0130h	0501 0130h
140h	CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG		0500 0140h	0501 0140h
144h	CMN_RESCAL_STATUS_PREG__CMN_RESCAL_OVRD_PREG		0500 0144h	0501 0144h
150h	CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG		0500 0150h	0501 0150h
154h	CMN_CORE_ATB_EN_PREG__CMN_ATB_ADC_EN_TMR_PREG		0500 0154h	0501 0154h

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
160h	HSRRSM_STATUS_PREG__HSRRSM_CTRL_PREG		0500 0160h	0501 0160h
170h	CMN_REFRCV1_PREG		0500 0170h	0501 0170h
180h	CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG		0500 0180h	0501 0180h
184h	CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG		0500 0184h	0501 0184h
188h	CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG		0500 0188h	0501 0188h
18Ch	CMN_PLLLC1_ITER_TMR_PREG__CMN_PLLLC1_I_NIT_PREG		0500 018Ch	0501 018Ch
190h	CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG		0500 0190h	0501 0190h
194h	CMN_PLLLC1_LOCK_CNTSTART_PREG__CMN_PLLLC1_LF_COEFF_MODE0_PREG		0500 0194h	0501 0194h
198h	CMN_PLLLC1_CLK1_PREG__CMN_PLLLC1_LOCK_CNTTHRESH_PREG		0500 0198h	0501 0198h
19Ch	CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG		0500 019Ch	0501 019Ch
1A0h	CMN_PLLLC1_DSMLCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG		0500 01A0h	0501 01A0h
1A4h	CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC1_SS_PREG		0500 01A4h	0501 01A4h
1A8h	CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLLLC1_SSTWOPT_PREG		0500 01A8h	0501 01A8h
1ACh	CMN_PLLLC1_DSMLCORR_OVR_PREG__CMN_PLLLC1_LF_INT_OVR_PREG		0500 01ACh	0501 01ACh
1B0h	CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG		0500 01B0h	0501 01B0h
1B4h	CMN_PLLLC1SM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG		0500 01B4h	0501 01B4h
1B8h	CMN_PLLLC1SM1_PLEN_TMR_PREG__CMN_PLLLC1SM1_CTRL_PREG		0500 01B8h	0501 01B8h
1BCh	CMN_PLLLC1SM1_PLLVREF_TMR_PREG__CMN_PLLLC1SM1_PLLPRE_TMR_PREG		0500 01BCh	0501 01BCh
1C0h	CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG		0500 01C0h	0501 01C0h
1C4h	CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG		0500 01C4h	0501 01C4h
400h	MOD_VER	Module and Version	0500 0400h	0501 0400h
404h	SERDES_CTRL	Serdes Control	0500 0404h	0501 0404h
408h	SERDES_TOP_CTRL	Serdes Top Level Control	0500 0408h	0501 0408h
40Ch	SERDES_RST	Serdes Reset	0500 040Ch	0501 040Ch
410h	SERDES_TYPEC	Serdes Type C control	0500 0410h	0501 0410h
414h	SERDES_CORE_STATUS	Serdes core power state status	0500 0414h	0501 0414h
480h	LANECTL0	Lane Control 0	0500 0480h	0501 0480h
484h	LANEDIV0	Lane Divider 0	0500 0484h	0501 0484h
488h	LANALIGN0	Lane Align 0	0500 0488h	0501 0488h
48Ch	LANESTS0	Lane Status 0	0500 048Ch	0501 048Ch
4C0h	LANECTL1	Lane Control 1	0500 04C0h	0501 04C0h
4C4h	LANEDIV1	Lane Divider 1	0500 04C4h	0501 04C4h

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
4C8h	LANALIGN1	Lane Align 1	0500 04C8h	0501 04C8h
4CCh	LANESTS1	Lane Status 1	0500 04CCh	0501 04CCh
5F4h	RES_CAL	Resistor Calibration	0500 05F4h	0501 05F4h
5FCh	DIAG_TEST	Diagnostic Test Register	0500 05FCh	0501 05FCh
2000h + formula	RESERVEDBIT13ADDRESSA_y		0500 2000h + formula	0501 2000h + formula
4000h + formula	DET_STANDEC_B_PREG__DET_STANDEC_A_PR EG_j		0500 4000h + formula	0501 4000h + formula
4004h + formula	DET_STANDEC_D_PREG__DET_STANDEC_C_P REG_j		0500 4004h + formula	0501 4004h + formula
4008h + formula	FPWRISO_OVRD_PREG__DET_STANDEC_E_PR EG_j		0500 4008h + formula	0501 4008h + formula
400Ch + formula	FPWRISO_CTRL_PREG_j		0500 400Ch + formula	0501 400Ch + formula
4010h + formula	PSM_A0IN_TMR_PREG__PSM_LANECAL_DLY_A 1_RESETS_PREG_j		0500 4010h + formula	0501 4010h + formula
4014h + formula	PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG _j		0500 4014h + formula	0501 4014h + formula
4018h + formula	PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG _j		0500 4018h + formula	0501 4018h + formula
401Ch + formula	PSM_A0OUT_TMR_PREG_j		0500 401Ch + formula	0501 401Ch + formula
4020h + formula	PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_P REG_j		0500 4020h + formula	0501 4020h + formula
4024h + formula	PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_P REG_j		0500 4024h + formula	0501 4024h + formula
4028h + formula	PSM_DIAG_PREG_j		0500 4028h + formula	0501 4028h + formula
402Ch + formula	PSM_STATE_L_PREG__PSM_STATE_H_PREG_j		0500 402Ch + formula	0501 402Ch + formula
4030h + formula	PSTG_STATUS_PREG__PSTG_CTRL_PREG_j		0500 4030h + formula	0501 4030h + formula
4038h + formula	PCSM_STATUS_PREG__PCSM_CTRL_PREG_j		0500 4038h + formula	0501 4038h + formula
4040h + formula	PSC_LN_A1_PREG__PSC_LN_A0_PREG_j		0500 4040h + formula	0501 4040h + formula
4044h + formula	PSC_LN_A3_PREG__PSC_LN_A2_PREG_j		0500 4044h + formula	0501 4044h + formula
4048h + formula	PSC_LN_A5_PREG__PSC_LN_A4_PREG_j		0500 4048h + formula	0501 4048h + formula
404Ch + formula	PSC_LN_IDLE_PREG_j		0500 404Ch + formula	0501 404Ch + formula
4050h + formula	PSC_TX_A1_PREG__PSC_TX_A0_PREG_j		0500 4050h + formula	0501 4050h + formula
4054h + formula	PSC_TX_A3_PREG__PSC_TX_A2_PREG_j		0500 4054h + formula	0501 4054h + formula
4058h + formula	PSC_TX_A5_PREG__PSC_TX_A4_PREG_j		0500 4058h + formula	0501 4058h + formula
405Ch + formula	PSC_TX_IDLE_PREG_j		0500 405Ch + formula	0501 405Ch + formula
4060h + formula	PSC_RX_A1_PREG__PSC_RX_A0_PREG_j		0500 4060h + formula	0501 4060h + formula

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
4064h + formula	PSC_RX_A3_PREG_PSC_RX_A2_PREG_j		0500 4064h + formula	0501 4064h + formula
4068h + formula	PSC_RX_A5_PREG_PSC_RX_A4_PREG_j		0500 4068h + formula	0501 4068h + formula
406Ch + formula	PSC_RX_IDLE_PREG_j		0500 406Ch + formula	0501 406Ch + formula
4070h + formula	PLLCTRL_FBDIV_MODE01_PREG_PLLCTRL_FB DIV_MODE23_PREG_j		0500 4070h + formula	0501 4070h + formula
4074h + formula	PLLCTRL_GEN_A_PREG_PLLCTRL_SUBRATE_ PREG_j		0500 4074h + formula	0501 4074h + formula
4078h + formula	PLLCTRL_GEN_C_PREG_PLLCTRL_GEN_B_PR EG_j		0500 4078h + formula	0501 4078h + formula
407Ch + formula	PLLCTRL_CPGAIN_MODE_PREG_PLLCTRL_GE N_D_PREG_j		0500 407Ch + formula	0501 407Ch + formula
4080h + formula	PLLCTRL_PHASE1EN_PREG_LNCTRL_CLKRST _LN_PLLCLK_OVR_PREG_j		0500 4080h + formula	0501 4080h + formula
4084h + formula	PLLCTRL_AVDDREG_PREG_PLLCTRL_PHASE2 EN_PREG_j		0500 4084h + formula	0501 4084h + formula
4088h + formula	PLLNC_STATUS_PREG_PLLCTRL_STATUS_PR EG_j		0500 4088h + formula	0501 4088h + formula
4090h + formula	LOOPBACK_BIASTRIM_PREG_TX_BIASTRIM_P REG_j		0500 4090h + formula	0501 4090h + formula
4094h + formula	CLKPATH_BIASTRIM_PREG_RXFE_BIASTRIM_P REG_j		0500 4094h + formula	0501 4094h + formula
4098h + formula	DPE_BIASTRIM_PREG_j		0500 4098h + formula	0501 4098h + formula
40A0h + formula	BSCAN_LPBKLINE_PREG_LANE_LOOPBACK_C TRL_PREG_j		0500 40A0h + formula	0501 40A0h + formula
40A8h + formula	TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j		0500 40A8h + formula	0501 40A8h + formula
40ACh + formula	TX_LOWLAT_CTRL_PREG_j		0500 40ACh + formula	0501 40ACh + formula
40B0h + formula	TX_ELEC_IDLE_PREG_j		0500 40B0h + formula	0501 40B0h + formula
40B4h + formula	TX_SER_LOADDELAY_PREG_j		0500 40B4h + formula	0501 40B4h + formula
40B8h + formula	TX_HSRSM_STATUS_PREG_j		0500 40B8h + formula	0501 40B8h + formula
40C0h + formula	DRVCTRL_PRESET_C0_OVRD_PREG_DRVCTR L_PRESET_CM1_OVRD_PREG_j		0500 40C0h + formula	0501 40C0h + formula
40C4h + formula	DRVCTRL_INIT_CM1_OVRD_PREG_DRVCTRL_ PRESET_CP1_OVRD_PREG_j		0500 40C4h + formula	0501 40C4h + formula
40C8h + formula	DRVCTRL_INIT_CP1_OVRD_PREG_DRVCTRL_I NIT_C0_OVRD_PREG_j		0500 40C8h + formula	0501 40C8h + formula
40CCh + formula	DRVCTRL_C0_OVRD_PREG_DRVCTRL_CM1_O VRD_PREG_j		0500 40CCh + formula	0501 40CCh + formula
40D0h + formula	DRVCTRL_C0M_OVRD_PREG_DRVCTRL_CP1_ OVRD_PREG_j		0500 40D0h + formula	0501 40D0h + formula
40D4h + formula	DRVCTRL_CM1_CV_PREG_DRVCTRL_ATTEN_ PREG_j		0500 40D4h + formula	0501 40D4h + formula
40D8h + formula	DRVCTRL_CP1_CV_PREG_DRVCTRL_C0_CV_P REG_j		0500 40D8h + formula	0501 40D8h + formula
40DCh + formula	DRVCTRL_BOOST_PREG_DRVCTRL_C0M_CV_ PREG_j		0500 40DCh + formula	0501 40DCh + formula

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
40E0h + formula	LANE_TX_RECEIVER_DETECT_PREG__DRVCTR L_BSCAN_PREG_j		0500 40E0h + formula	0501 40E0h + formula
40E4h + formula	TX_RCVDDET_OVRD_PREG_j		0500 40E4h + formula	0501 40E4h + formula
40E8h + formula	TXCOEF_STATUS_PREG_j		0500 40E8h + formula	0501 40E8h + formula
40F0h + formula	LANE_TX_BIST_UDD_PREG__TX_BIST_CONTR LS_PREG_j		0500 40F0h + formula	0501 40F0h + formula
40F8h + formula	TX_LFPSGEN_STATUS_PREG_j		0500 40F8h + formula	0501 40F8h + formula
4100h + formula	CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OV R_PREG_j		0500 4100h + formula	0501 4100h + formula
4108h + formula	RX_CREQ_FLTR_A_MODE3_PREG_j		0500 4108h + formula	0501 4108h + formula
410Ch + formula	RX_CREQ_FLTR_A_MODE1_PREG__RX_CREQ_ FLTR_A_MODE2_PREG_j		0500 410Ch + formula	0501 410Ch + formula
4110h + formula	RX_CREQ_FLTR_B_PREG__RX_CREQ_FLTR_A_ MODE0_PREG_j		0500 4110h + formula	0501 4110h + formula
4114h + formula	RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BU MP_PREG_j		0500 4114h + formula	0501 4114h + formula
4118h + formula	CREQ_CCLKDET_MODE23_PREG__CREQ_DCBI ASATTEN_OVR_PREG_j		0500 4118h + formula	0501 4118h + formula
411Ch + formula	RX_CTLE_CAL_PREG__CREQ_CCLKDET_MODE 01_PREG_j		0500 411Ch + formula	0501 411Ch + formula
4120h + formula	RX_CTLE_MAINTENANCE_PREG__RX_CTLE_CT RL_PREG_j		0500 4120h + formula	0501 4120h + formula
4124h + formula	CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_ PREG_j		0500 4124h + formula	0501 4124h + formula
4128h + formula	RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_ PREG_j		0500 4128h + formula	0501 4128h + formula
412Ch + formula	CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_ SPARE_PREG_j		0500 412Ch + formula	0501 412Ch + formula
4130h + formula	CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_ PREG_j		0500 4130h + formula	0501 4130h + formula
4134h + formula	CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_ PREG_j		0500 4134h + formula	0501 4134h + formula
4138h + formula	CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_ PREG_j		0500 4138h + formula	0501 4138h + formula
413Ch + formula	CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_ PREG_j		0500 413Ch + formula	0501 413Ch + formula
4140h + formula	CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_ PREG_j		0500 4140h + formula	0501 4140h + formula
4144h + formula	CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_ PREG_j		0500 4144h + formula	0501 4144h + formula
4148h + formula	CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_ PREG_j		0500 4148h + formula	0501 4148h + formula
414Ch + formula	CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_ PREG_j		0500 414Ch + formula	0501 414Ch + formula
4150h + formula	CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_ PREG_j		0500 4150h + formula	0501 4150h + formula
4154h + formula	CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_ PREG_j		0500 4154h + formula	0501 4154h + formula
4158h + formula	CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_ PREG_j		0500 4158h + formula	0501 4158h + formula

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
415Ch + formula	CTLELUT_OVR_10B_PREG__CTLELUT_OVR_10A_PREG_j		0500 415Ch + formula	0501 415Ch + formula
4160h + formula	CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j		0500 4160h + formula	0501 4160h + formula
4164h + formula	CTLELUT_OVR_12B_PREG__CTLELUT_OVR_12A_PREG_j		0500 4164h + formula	0501 4164h + formula
4168h + formula	CTLELUT_OVR_13B_PREG__CTLELUT_OVR_13A_PREG_j		0500 4168h + formula	0501 4168h + formula
416Ch + formula	CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j		0500 416Ch + formula	0501 416Ch + formula
4170h + formula	CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j		0500 4170h + formula	0501 4170h + formula
4180h + formula	DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j		0500 4180h + formula	0501 4180h + formula
4184h + formula	DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j		0500 4184h + formula	0501 4184h + formula
4188h + formula	DEQ_PHALIGN_CTRL_j		0500 4188h + formula	0501 4188h + formula
4190h + formula	DEQ_CONCUR_CTRL2_PREG__DEQ_CONCUR_CTRL1_PREG_j		0500 4190h + formula	0501 4190h + formula
4194h + formula	DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j		0500 4194h + formula	0501 4194h + formula
4198h + formula	DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j		0500 4198h + formula	0501 4198h + formula
419Ch + formula	RX_DEQ_COEF_FIFO_PREG__DEQ_FAST_MAIN_T_CYCLES_PREG_j		0500 419Ch + formula	0501 419Ch + formula
41A0h + formula	DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j		0500 41A0h + formula	0501 41A0h + formula
41A4h + formula	CMP_AVR_TIMER_PREG__DEQ_ERRCMPB_OVR_PREG_j		0500 41A4h + formula	0501 41A4h + formula
41B0h + formula	DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j		0500 41B0h + formula	0501 41B0h + formula
41C0h + formula	DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j		0500 41C0h + formula	0501 41C0h + formula
41D0h + formula	DEQ_GLUT1__DEQ_GLUT0_j		0500 41D0h + formula	0501 41D0h + formula
41D4h + formula	DEQ_GLUT3__DEQ_GLUT2_j		0500 41D4h + formula	0501 41D4h + formula
41D8h + formula	DEQ_GLUT5__DEQ_GLUT4_j		0500 41D8h + formula	0501 41D8h + formula
41DCh + formula	DEQ_GLUT7__DEQ_GLUT6_j		0500 41DCh + formula	0501 41DCh + formula
41E0h + formula	DEQ_GLUT9__DEQ_GLUT8_j		0500 41E0h + formula	0501 41E0h + formula
41E4h + formula	DEQ_GLUT11__DEQ_GLUT10_j		0500 41E4h + formula	0501 41E4h + formula
41E8h + formula	DEQ_GLUT13__DEQ_GLUT12_j		0500 41E8h + formula	0501 41E8h + formula
41ECh + formula	DEQ_GLUT15__DEQ_GLUT14_j		0500 41ECh + formula	0501 41ECh + formula
41F0h + formula	DEQ_GLUT17__DEQ_GLUT16_j		0500 41F0h + formula	0501 41F0h + formula
41F4h + formula	DEQ_GLUT19__DEQ_GLUT18_j		0500 41F4h + formula	0501 41F4h + formula

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
41F8h + formula	DEQ_GLUT21__DEQ_GLUT20_j		0500 41F8h + formula	0501 41F8h + formula
41FCh + formula	DEQ_GLUT23__DEQ_GLUT22_j		0500 41FCh + formula	0501 41FCh + formula
4200h + formula	DEQ_GLUT25__DEQ_GLUT24_j		0500 4200h + formula	0501 4200h + formula
4204h + formula	DEQ_GLUT27__DEQ_GLUT26_j		0500 4204h + formula	0501 4204h + formula
4208h + formula	DEQ_GLUT29__DEQ_GLUT28_j		0500 4208h + formula	0501 4208h + formula
420Ch + formula	DEQ_GLUT31__DEQ_GLUT30_j		0500 420Ch + formula	0501 420Ch + formula
4210h + formula	DEQ_ALUT1__DEQ_ALUT0_j		0500 4210h + formula	0501 4210h + formula
4214h + formula	DEQ_ALUT3__DEQ_ALUT2_j		0500 4214h + formula	0501 4214h + formula
4218h + formula	DEQ_ALUT5__DEQ_ALUT4_j		0500 4218h + formula	0501 4218h + formula
421Ch + formula	DEQ_ALUT7__DEQ_ALUT6_j		0500 421Ch + formula	0501 421Ch + formula
4220h + formula	DEQ_ALUT9__DEQ_ALUT8_j		0500 4220h + formula	0501 4220h + formula
4224h + formula	DEQ_ALUT11__DEQ_ALUT10_j		0500 4224h + formula	0501 4224h + formula
4228h + formula	DEQ_ALUT13__DEQ_ALUT12_j		0500 4228h + formula	0501 4228h + formula
422Ch + formula	DEQ_ALUT15__DEQ_ALUT14_j		0500 422Ch + formula	0501 422Ch + formula
4230h + formula	DEQ_ALUT17__DEQ_ALUT16_j		0500 4230h + formula	0501 4230h + formula
4234h + formula	DEQ_ALUT19__DEQ_ALUT18_j		0500 4234h + formula	0501 4234h + formula
4238h + formula	DEQ_ALUT21__DEQ_ALUT20_j		0500 4238h + formula	0501 4238h + formula
423Ch + formula	DEQ_ALUT23__DEQ_ALUT22_j		0500 423Ch + formula	0501 423Ch + formula
4240h + formula	DEQ_ALUT25__DEQ_ALUT24_j		0500 4240h + formula	0501 4240h + formula
4244h + formula	DEQ_ALUT27__DEQ_ALUT26_j		0500 4244h + formula	0501 4244h + formula
4248h + formula	DEQ_ALUT29__DEQ_ALUT28_j		0500 4248h + formula	0501 4248h + formula
424Ch + formula	DEQ_ALUT31__DEQ_ALUT30_j		0500 424Ch + formula	0501 424Ch + formula
4250h + formula	DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j		0500 4250h + formula	0501 4250h + formula
4254h + formula	DEQ_DFETAP1__DEQ_DFETAP0_OVR_j		0500 4254h + formula	0501 4254h + formula
4258h + formula	DEQ_DFETAP2__DEQ_DFETAP1_OVR_j		0500 4258h + formula	0501 4258h + formula
425Ch + formula	DEQ_DFETAP3__DEQ_DFETAP2_OVR_j		0500 425Ch + formula	0501 425Ch + formula
4260h + formula	DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j		0500 4260h + formula	0501 4260h + formula

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
4264h + formula	DATDFE_TAPCAP_THRESH_PREG__DEQ_DFET AP4_OVR_j		0500 4264h + formula	0501 4264h + formula
4268h + formula	DFE_TRAINING_MASK_PREG__DFE_EN_1010_I GNORE_PREG_j		0500 4268h + formula	0501 4268h + formula
426Ch + formula	DFE_EN_1010_IGNORE_DIAG_PREG_j		0500 426Ch + formula	0501 426Ch + formula
4270h + formula	DEQ_PRECUR_PREG_j		0500 4270h + formula	0501 4270h + formula
4280h + formula	DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_ PREG_j		0500 4280h + formula	0501 4280h + formula
4284h + formula	DEQ_POSTCUR_DECR_PREG_j		0500 4284h + formula	0501 4284h + formula
4290h + formula	DEQ_FALSEEYE_CTRL_PREG_j		0500 4290h + formula	0501 4290h + formula
429Ch + formula	DEQ_TAU_CTRL1_FAST_MAINT_PREG_j		0500 429Ch + formula	0501 429Ch + formula
42A0h + formula	DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SL OW_MAINT_PREG_j		0500 42A0h + formula	0501 42A0h + formula
42A4h + formula	DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL 3_PREG_j		0500 42A4h + formula	0501 42A4h + formula
42B0h + formula	DEQ_OPENEYE_CTRL_PREG_j		0500 42B0h + formula	0501 42B0h + formula
42C0h + formula	DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PRE G_j		0500 42C0h + formula	0501 42C0h + formula
42D0h + formula	CPICAL_CAP_STARTCODE_MODE23_PREG__CP ICAL_CTRL_PREG_j		0500 42D0h + formula	0501 42D0h + formula
42D4h + formula	CPICAL_CAP_OVR_PREG__CPICAL_CAP_START CODE_MODE01_PREG_j		0500 42D4h + formula	0501 42D4h + formula
42D8h + formula	CPICAL_CAP_ITERTMR_PREG__CPICAL_CAP_I NITTMR_PREG_j		0500 42D8h + formula	0501 42D8h + formula
42DCh + formula	CPICAL_TMRVAL_MODE2_PREG__CPICAL_TMR VAL_MODE3_PREG_j		0500 42DCh + formula	0501 42DCh + formula
42E0h + formula	CPICAL_TMRVAL_MODE0_PREG__CPICAL_TMR VAL_MODE1_PREG_j		0500 42E0h + formula	0501 42E0h + formula
42E4h + formula	CPICAL_PICNT_MODE2_PREG__CPICAL_PICNT _MODE3_PREG_j		0500 42E4h + formula	0501 42E4h + formula
42E8h + formula	CPICAL_PICNT_MODE0_PREG__CPICAL_PICNT _MODE1_PREG_j		0500 42E8h + formula	0501 42E8h + formula
42ECh + formula	CPICAL_STATUS_PREG_j		0500 42ECh + formula	0501 42ECh + formula
42F0h + formula	CPICAL_OFFSET_PREG_j		0500 42F0h + formula	0501 42F0h + formula
42F8h + formula	CPI_OUTBUF_RATESEL_PREG_j		0500 42F8h + formula	0501 42F8h + formula
42FCh + formula	CPI_TRIM_PREG__CPI_RESBIAS_BIN_PREG_j		0500 42FCh + formula	0501 42FCh + formula
4300h + formula	CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PR EG_j		0500 4300h + formula	0501 4300h + formula
4304h + formula	CPICAL_RES_STARTCODE_MODE23_PREG__CP ICAL_INCR_DECR_PREG_j		0500 4304h + formula	0501 4304h + formula
4308h + formula	CPICAL_RES_INITTMR_PREG__CPICAL_RES_ST ARTCODE_MODE01_PREG_j		0500 4308h + formula	0501 4308h + formula
430Ch + formula	EPI_CTRL_PREG__CPICAL_RES_ITERTMR_PRE G_j		0500 430Ch + formula	0501 430Ch + formula

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
4310h + formula	LFPSFILT_MD_PREG__LFPSDET_SUPPORT_PR EG_j		0500 4310h + formula	0501 4310h + formula
4314h + formula	LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j		0500 4314h + formula	0501 4314h + formula
4318h + formula	LFPSFILT_MP_PREG_j		0500 4318h + formula	0501 4318h + formula
4320h + formula	SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PRE G_j		0500 4320h + formula	0501 4320h + formula
4324h + formula	SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j		0500 4324h + formula	0501 4324h + formula
4328h + formula	SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j		0500 4328h + formula	0501 4328h + formula
432Ch + formula	SDCAL_TUNE_PREG__SDCAL_START_PREG_j		0500 432Ch + formula	0501 432Ch + formula
4330h + formula	SDCAL_ITER_PREG__SDCAL_INIT_PREG_j		0500 4330h + formula	0501 4330h + formula
4338h + formula	RXTERM_ENABLE_PREG__RXTERM_BSCAN_PR EG_j		0500 4338h + formula	0501 4338h + formula
433Ch + formula	RXBUFFER_RCDFECTRL_PREG__RXBUFFER_C TLECTRL_PREG_j		0500 433Ch + formula	0501 433Ch + formula
4340h + formula	RXBUFFER_DFECTRL_PREG_j		0500 4340h + formula	0501 4340h + formula
4348h + formula	DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_C TRL_PREG_j		0500 4348h + formula	0501 4348h + formula
434Ch + formula	DEQ_EYESURF_ACCUMB__DEQ_EYESURF_AC CUMA_j		0500 434Ch + formula	0501 434Ch + formula
4350h + formula	RX_BIST_SYNCNT_PREG__RX_BIST_CONTRO LS_PREG_j		0500 4350h + formula	0501 4350h + formula
4354h + formula	RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PRE G_j		0500 4354h + formula	0501 4354h + formula
4360h + formula	LN_SPARE_REG_PREG_j		0500 4360h + formula	0501 4360h + formula
4370h + formula	PREADAPT_CTRL_PREG_j		0500 4370h + formula	0501 4370h + formula
4380h + formula	LN_CTRL_DIAG_RESET_PREG__LN_FPWRISO_ DIAG_RESET_PREG_j		0500 4380h + formula	0501 4380h + formula
4384h + formula	LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTR L_DIAG_RESET_PREG_j		0500 4384h + formula	0501 4384h + formula
4388h + formula	LN_RXDSYNC_DIAG_RESET_PREG__LN_RXCTR L_DIAG_RESET_PREG_j		0500 4388h + formula	0501 4388h + formula
4390h + formula	LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_ CLK_FREQ_MSMT_CTRL_PREG_j		0500 4390h + formula	0501 4390h + formula
4394h + formula	LN_CLK_FREQ_MSMT_OBS_PREG__LN_CMSMT _TEST_CLK_CNT_VALUE_PREG_j		0500 4394h + formula	0501 4394h + formula
43A0h + formula	RXMGRN_CTRL_PREG_j		0500 43A0h + formula	0501 43A0h + formula
43B0h + formula	SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j		0500 43B0h + formula	0501 43B0h + formula
43B4h + formula	SMPCAL_NUM_WORDS_PREG__SMPCAL_ITER_ PREG_j		0500 43B4h + formula	0501 43B4h + formula
43B8h + formula	SMPCAL_TUNE_PREG__SMPCAL_START_PREG _j		0500 43B8h + formula	0501 43B8h + formula
43BCh + formula	SMPCAL_CALODDCODE_OVR_PREG__SMPCAL _CALEVNCODE_OVR_PREG_j		0500 43BCh + formula	0501 43BCh + formula

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
43C0h + formula	SMPCAL_CALODDCODE_PREG__SMPCAL_CAL EVNCODE_PREG_j		0500 43C0h + formula	0501 43C0h + formula
43C4h + formula	SMPCAL_STATE_PREG_j		0500 43C4h + formula	0501 43C4h + formula
43D0h + formula	DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_T AU_CTRL1_PREG_j		0500 43D0h + formula	0501 43D0h + formula
43D4h + formula	DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_ VTH_PREG_j		0500 43D4h + formula	0501 43D4h + formula
43D8h + formula	DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_ CTRL1_PREG_j		0500 43D8h + formula	0501 43D8h + formula
43DCh + formula	DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_ CTRL3_PREG_j		0500 43DCh + formula	0501 43DCh + formula
6000h + formula	RESERVEDBIT13ADDRESSB_y		0500 6000h + formula	0501 6000h + formula
8000h + formula	RESERVEDSIERRAREP8000_y		0500 8000h + formula	0501 8000h + formula
A000h + formula	RESERVEDBIT13ADDRESSC_y		0500 A000h + formula	0501 A000h + formula
C000h	PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL 1		0500 C000h	0501 C000h
C004h	PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM _LOCK_CFG1		0500 C004h	0501 C004h
C008h	PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_ CFG		0500 C008h	0501 C008h
C00Ch	PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RC V_DET_INH		0500 C00Ch	0501 C00Ch
C010h	PHY_ISO_CMN_CTRL		0500 C010h	0501 C010h
C014h	PHY_STATE_CHG_TIMEOUT		0500 C014h	0501 C014h
C01Ch	PHY_AUTO_CFG_CTRL__PHY_PLL_CFG		0500 C01Ch	0501 C01Ch
C020h	PHY_REFCLK1_DET_THRES_LOW__PHY_REFCL K_DET_THRES_LOW		0500 C020h	0501 C020h
C024h	PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCL LK_DET_THRES_HIGH		0500 C024h	0501 C024h
C028h	PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_ DET_INTERVAL		0500 C028h	0501 C028h
C02Ch	PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_ DET_OP_DELAY		0500 C02Ch	0501 C02Ch
C030h	PHY_REFCLK_DET_ISO_CTRL		0500 C030h	0501 C030h
C034h	PHY_PIPE_LM_CFG0		0500 C034h	0501 C034h
C038h	PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1		0500 C038h	0501 C038h
C03Ch	PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3		0500 C03Ch	0501 C03Ch
C040h	PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE _USB3_GEN2_PRE_CFG0		0500 C040h	0501 C040h
C044h	PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIP E_USB3_GEN2_POST_CFG0		0500 C044h	0501 C044h
D000h + formula	PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_T X_CTRL_j		0500 D000h + formula	0501 D000h + formula
D004h + formula	PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_ TX_LPC_HI_j		0500 D004h + formula	0501 D004h + formula
D008h + formula	PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_D MPH_HI_j		0500 D008h + formula	0501 D008h + formula

Table 11-2. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G0 Physical Address	SERDES_16G1 Physical Address
D00Ch + formula	PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j		0500 D00Ch + formula	0501 D00Ch + formula
D010h + formula	PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j		0500 D010h + formula	0501 D010h + formula
D014h + formula	PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j		0500 D014h + formula	0501 D014h + formula
D018h + formula	PHY_PIPE_ISO_USB_BER_CNT_j		0500 D018h + formula	0501 D018h + formula
D01Ch + formula	PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j		0500 D01Ch + formula	0501 D01Ch + formula
D020h + formula	PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j		0500 D020h + formula	0501 D020h + formula
D024h + formula	PHY_INTERRUPT_STS_j		0500 D024h + formula	0501 D024h + formula
D030h + formula	PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_ISO_LM_CTRL_STS_j		0500 D030h + formula	0501 D030h + formula
D034h + formula	PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j		0500 D034h + formula	0501 D034h + formula
D038h + formula	PHY_PIPE_ISO_LM_PHY2MAC1_j		0500 D038h + formula	0501 D038h + formula
D03Ch + formula	PHY_PIPE_ISO_LM_PHY2MAC_STS_j		0500 D03Ch + formula	0501 D03Ch + formula
E000h	PHY_PMA_CMN_CTRL		0500 E000h	0501 E000h
E008h	PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL		0500 E008h	0501 E008h
E00Ch	PHY_PMA_ISO_RESCAL		0500 E00Ch	0501 E00Ch
E01Ch	PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL		0500 E01Ch	0501 E01Ch
F000h + formula	PHY_PMA_XCVR_CTRL_j		0500 F000h + formula	0501 F000h + formula
F004h + formula	PHY_PMA_ISO_XCVR_CTRL_j		0500 F004h + formula	0501 F004h + formula
F008h + formula	PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX_LPC_LO_j		0500 F008h + formula	0501 F008h + formula
F00Ch + formula	PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j		0500 F00Ch + formula	0501 F00Ch + formula
F010h + formula	PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j		0500 F010h + formula	0501 F010h + formula
F014h + formula	PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j		0500 F014h + formula	0501 F014h + formula
F018h + formula	PHY_PMA_ISO_RX_EQ_CTRL_j		0500 F018h + formula	0501 F018h + formula
F01Ch + formula	PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j		0500 F01Ch + formula	0501 F01Ch + formula
F020h + formula	PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j		0500 F020h + formula	0501 F020h + formula

Table 11-3. SERDES_16G Registers

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
0h	MACRO_ID_REG		0502 0000h	0503 0000h
4h	MACRO_ID_NUMBER_REG		0502 0004h	0503 0004h

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
8h	MACRO_ID_REV_REG		0502 0008h	0503 0008h
10h	MACRO_ID_NODE_REG__MACRO_ID_MFG_REG		0502 0010h	0503 0010h
14h	MACRO_ID_FLAVOR_REG		0502 0014h	0503 0014h
18h	MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG		0502 0018h	0503 0018h
20h	MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG		0502 0020h	0503 0020h
24h	MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG		0502 0024h	0503 0024h
28h	MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG		0502 0028h	0503 0028h
40h	CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG		0502 0040h	0503 0040h
60h	CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BAND_GAP_TMR_PREG		0502 0060h	0503 0060h
64h	CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG		0502 0064h	0503 0064h
68h	CMN_SMCSM_STATE_PREG		0502 0068h	0503 0068h
80h	CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG		0502 0080h	0503 0080h
84h	CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG		0502 0084h	0503 0084h
88h	CMN_PLLLC_DCO_CAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG		0502 0088h	0503 0088h
8Ch	CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG		0502 008Ch	0503 008Ch
90h	CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG		0502 0090h	0503 0090h
94h	CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG		0502 0094h	0503 0094h
98h	CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG		0502 0098h	0503 0098h
9Ch	CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG		0502 009Ch	0503 009Ch
A0h	CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG		0502 00A0h	0503 00A0h
A4h	CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG		0502 00A4h	0503 00A4h
A8h	CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG		0502 00A8h	0503 00A8h
ACCh	CMN_PLLLC_DSMCORR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG		0502 00ACCh	0503 00ACCh
B0h	CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG		0502 00B0h	0503 00B0h
B4h	CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG		0502 00B4h	0503 00B4h
B8h	CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG		0502 00B8h	0503 00B8h
BCh	CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG		0502 00BCh	0503 00BCh
C0h	CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG		0502 00C0h	0503 00C0h

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
C4h	CMN_PLLLC_LOCK_DELAY_CTRL_PREG_CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG		0502 00C4h	0503 00C4h
D0h	SDOSCCAL_CTRL_PREG_CMN_SDOSC_OVRD_PREG		0502 00D0h	0503 00D0h
D4h	SDOSCCAL_INIT_TMR_PREG_SDOSCCAL_OVR_PREG		0502 00D4h	0503 00D4h
D8h	SDOSCCAL_TMR_PREG_SDOSCCAL_ITER_TM_R_PREG		0502 00D8h	0503 00D8h
DCh	SDOSCCAL_START_PREG_SDOSCCAL_CLK_CNT_PREG		0502 00DCh	0503 00DCh
E0h	PROCMON_STATUS_PREG_PROCMON_CTRL_PREG		0502 00E0h	0503 00E0h
E4h	PROCMON_CNTWAIT_PREG_PROCMON_INITWAIT_PREG		0502 00E4h	0503 00E4h
E8h	PROCMON_DIAGNOSTIC_PREG_PROCMON_OVRD_PREG		0502 00E8h	0503 00E8h
100h	CMN_CTRL_DIAG_RESET_PREG_CDB_DIAG_PREG		0502 0100h	0503 0100h
104h	CMN_FUNC_DIAG_RESET_PREG		0502 0104h	0503 0104h
108h	CMN_CMSMT_REF_CLK_TMR_VALUE_PREG_CMN_CLK_FREQ_MSMT_CTRL_PREG		0502 0108h	0503 0108h
10Ch	CMN_CLK_FREQ_MSMT_OBS_PREG_CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG		0502 010Ch	0503 010Ch
110h	CMN_SPARE_REG_PREG		0502 0110h	0503 0110h
120h	CMN_BIAS_TRIM_PREG_CMN_BIAS_EN_OVRD_PREG		0502 0120h	0503 0120h
124h	CMN_BIAS_VREF_TRIM_PREG		0502 0124h	0503 0124h
130h	CMN_PSMCLK_SDOSCCAL_CTRL_PREG_CMN_REFRCV_PREG		0502 0130h	0503 0130h
140h	CMN_RESCAL_CTRLB_PREG_CMN_RESCAL_CTRLA_PREG		0502 0140h	0503 0140h
144h	CMN_RESCAL_STATUS_PREG_CMN_RESCAL_OVRD_PREG		0502 0144h	0503 0144h
150h	CMN_ATB_ADC_PREG_CMN_ATB_CTRL_PREG		0502 0150h	0503 0150h
154h	CMN_CORE_ATB_EN_PREG_CMN_ATB_ADC_EN_TMR_PREG		0502 0154h	0503 0154h
160h	HSRRSM_STATUS_PREG_HSRRSM_CTRL_PREG		0502 0160h	0503 0160h
170h	CMN_REFRCV1_PREG		0502 0170h	0503 0170h
180h	CMN_PLLLC1_STATUS_B_PREG_CMN_PLLLC1_STATUS_A_PREG		0502 0180h	0503 0180h
184h	CMN_PLLLC1_FBDIV_INT_PREG_CMN_PLLLC1_GEN_PREG		0502 0184h	0503 0184h
188h	CMN_PLLLC1_DCOAL_CTRL_PREG_CMN_PLLLC1_FBDIV_FRAC_PREG		0502 0188h	0503 0188h
18Ch	CMN_PLLLC1_ITERTMR_PREG_CMN_PLLLC1_INIT_PREG		0502 018Ch	0503 018Ch
190h	CMN_PLLLC1_LF_COEFF_MODE1_PREG_CMN_PLLLC1_MODE_PREG		0502 0190h	0503 0190h
194h	CMN_PLLLC1_LOCK_CNTSTART_PREG_CMN_PLLLC1_LF_COEFF_MODE0_PREG		0502 0194h	0503 0194h
198h	CMN_PLLLC1_CLK1_PREG_CMN_PLLLC1_LOCK_CNTTHRESH_PREG		0502 0198h	0503 0198h

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
19Ch	CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PL LLC1_CLK0_PREG		0502 019Ch	0503 019Ch
1A0h	CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1 _BWCAL_MODE0_PREG		0502 01A0h	0503 01A0h
1A4h	CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CM N_PLLLC1_SS_PREG		0502 01A4h	0503 01A4h
1A8h	CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLL LC1_SSTWOPT_PREG		0502 01A8h	0503 01A8h
1ACh	CMN_PLLLC1_DSMCORR_OVR_PREG__CMN_PL LLC1_LF_INT_OVR_PREG		0502 01ACh	0503 01ACh
1B0h	CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SST WOPT_OVR_PREG		0502 01B0h	0503 01B0h
1B4h	CMN_PLLLC1_STATUS_PREG__CMN_PLLLC1 _AVDD_PREG		0502 01B4h	0503 01B4h
1B8h	CMN_PLLLC1_PLEN_TMR_PREG__CMN_PL LLCSM1_CTRL_PREG		0502 01B8h	0503 01B8h
1BCh	CMN_PLLLC1_PLLVREF_TMR_PREG__CMN_ PLLLC1_PLLPRE_TMR_PREG		0502 01BCh	0503 01BCh
1C0h	CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1 _CLK2_PREG		0502 01C0h	0503 01C0h
1C4h	CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN _PLLLC1_SS_TIME_STEPSIZE_MODE_PREG		0502 01C4h	0503 01C4h
400h	MOD_VER	Module and Version	0502 0400h	0503 0400h
404h	SERDES_CTRL	Serdes Control	0502 0404h	0503 0404h
408h	SERDES_TOP_CTRL	Serdes Top Level Control	0502 0408h	0503 0408h
40Ch	SERDES_RST	Serdes Reset	0502 040Ch	0503 040Ch
410h	SERDES_TYPEC	Serdes Type C control	0502 0410h	0503 0410h
414h	SERDES_CORE_STATUS	Serdes core power state status	0502 0414h	0503 0414h
480h	LANECTLO	Lane Control 0	0502 0480h	0503 0480h
484h	LANEDIV0	Lane Divider 0	0502 0484h	0503 0484h
488h	LANALIGN0	Lane Align 0	0502 0488h	0503 0488h
48Ch	LANESTS0	Lane Status 0	0502 048Ch	0503 048Ch
4C0h	LANECTL1	Lane Control 1	0502 04C0h	0503 04C0h
4C4h	LANEDIV1	Lane Divider 1	0502 04C4h	0503 04C4h
4C8h	LANALIGN1	Lane Align 1	0502 04C8h	0503 04C8h
4CCh	LANESTS1	Lane Status 1	0502 04CCh	0503 04CCh
5F4h	RES_CAL	Resistor Calibration	0502 05F4h	0503 05F4h
5FCh	DIAG_TEST	Diagnostic Test Register	0502 05FCh	0503 05FCh
2000h + formula	RESERVEDBIT13ADDRESSA_y		0502 2000h + formula	0503 2000h + formula
4000h + formula	DET_STANDEC_B_PREG__DET_STANDEC_A_PR EG_j		0502 4000h + formula	0503 4000h + formula
4004h + formula	DET_STANDEC_D_PREG__DET_STANDEC_C_P REG_j		0502 4004h + formula	0503 4004h + formula
4008h + formula	FPWRISO_OVRD_PREG__DET_STANDEC_E_PR EG_j		0502 4008h + formula	0503 4008h + formula
400Ch + formula	FPWRISO_CTRL_PREG_j		0502 400Ch + formula	0503 400Ch + formula
4010h + formula	PSM_A0IN_TMR_PREG__PSM_LANECAL_DLY_A 1_RESETS_PREG_j		0502 4010h + formula	0503 4010h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
4014h + formula	PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG_j		0502 4014h + formula	0503 4014h + formula
4018h + formula	PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG_j		0502 4018h + formula	0503 4018h + formula
401Ch + formula	PSM_A0OUT_TMR_PREG_j		0502 401Ch + formula	0503 401Ch + formula
4020h + formula	PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_PREG_j		0502 4020h + formula	0503 4020h + formula
4024h + formula	PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_PREG_j		0502 4024h + formula	0503 4024h + formula
4028h + formula	PSM_DIAG_PREG_j		0502 4028h + formula	0503 4028h + formula
402Ch + formula	PSM_STATE_L_PREG__PSM_STATE_H_PREG_j		0502 402Ch + formula	0503 402Ch + formula
4030h + formula	PSTG_STATUS_PREG__PSTG_CTRL_PREG_j		0502 4030h + formula	0503 4030h + formula
4038h + formula	PCSM_STATUS_PREG__PCSM_CTRL_PREG_j		0502 4038h + formula	0503 4038h + formula
4040h + formula	PSC_LN_A1_PREG__PSC_LN_A0_PREG_j		0502 4040h + formula	0503 4040h + formula
4044h + formula	PSC_LN_A3_PREG__PSC_LN_A2_PREG_j		0502 4044h + formula	0503 4044h + formula
4048h + formula	PSC_LN_A5_PREG__PSC_LN_A4_PREG_j		0502 4048h + formula	0503 4048h + formula
404Ch + formula	PSC_LN_IDLE_PREG_j		0502 404Ch + formula	0503 404Ch + formula
4050h + formula	PSC_TX_A1_PREG__PSC_TX_A0_PREG_j		0502 4050h + formula	0503 4050h + formula
4054h + formula	PSC_TX_A3_PREG__PSC_TX_A2_PREG_j		0502 4054h + formula	0503 4054h + formula
4058h + formula	PSC_TX_A5_PREG__PSC_TX_A4_PREG_j		0502 4058h + formula	0503 4058h + formula
405Ch + formula	PSC_TX_IDLE_PREG_j		0502 405Ch + formula	0503 405Ch + formula
4060h + formula	PSC_RX_A1_PREG__PSC_RX_A0_PREG_j		0502 4060h + formula	0503 4060h + formula
4064h + formula	PSC_RX_A3_PREG__PSC_RX_A2_PREG_j		0502 4064h + formula	0503 4064h + formula
4068h + formula	PSC_RX_A5_PREG__PSC_RX_A4_PREG_j		0502 4068h + formula	0503 4068h + formula
406Ch + formula	PSC_RX_IDLE_PREG_j		0502 406Ch + formula	0503 406Ch + formula
4070h + formula	PLLCTRL_FBDIV_MODE01_PREG__PLLCTRL_FBDIV_MODE23_PREG_j		0502 4070h + formula	0503 4070h + formula
4074h + formula	PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j		0502 4074h + formula	0503 4074h + formula
4078h + formula	PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j		0502 4078h + formula	0503 4078h + formula
407Ch + formula	PLLCTRL_CPGAIN_MODE_PREG__PLLCTRL_GEN_D_PREG_j		0502 407Ch + formula	0503 407Ch + formula
4080h + formula	PLLCTRL_PHASE1EN_PREG__LNCTRL_CLKRST_LN_PLLCLK_OVR_PREG_j		0502 4080h + formula	0503 4080h + formula
4084h + formula	PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j		0502 4084h + formula	0503 4084h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
4088h + formula	PLLNC_STATUS_PREG__PLLCTRL_STATUS_PREG_j		0502 4088h + formula	0503 4088h + formula
4090h + formula	LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j		0502 4090h + formula	0503 4090h + formula
4094h + formula	CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j		0502 4094h + formula	0503 4094h + formula
4098h + formula	DFE_BIASTRIM_PREG_j		0502 4098h + formula	0503 4098h + formula
40A0h + formula	BSCAN_LPBKLINE_PREG__LANE_LOOPBACK_CTRL_PREG_j		0502 40A0h + formula	0503 40A0h + formula
40A8h + formula	TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j		0502 40A8h + formula	0503 40A8h + formula
40ACh + formula	TX_LOWLAT_CTRL_PREG_j		0502 40ACh + formula	0503 40ACh + formula
40B0h + formula	TX_ELEC_IDLE_PREG_j		0502 40B0h + formula	0503 40B0h + formula
40B4h + formula	TX_SER_LOADDELAY_PREG_j		0502 40B4h + formula	0503 40B4h + formula
40B8h + formula	TX_HSRISM_STATUS_PREG_j		0502 40B8h + formula	0503 40B8h + formula
40C0h + formula	DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j		0502 40C0h + formula	0503 40C0h + formula
40C4h + formula	DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j		0502 40C4h + formula	0503 40C4h + formula
40C8h + formula	DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j		0502 40C8h + formula	0503 40C8h + formula
40CCh + formula	DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j		0502 40CCh + formula	0503 40CCh + formula
40D0h + formula	DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j		0502 40D0h + formula	0503 40D0h + formula
40D4h + formula	DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j		0502 40D4h + formula	0503 40D4h + formula
40D8h + formula	DRVCTRL_CP1_CV_PREG__DRVCTRL_C0_CV_PREG_j		0502 40D8h + formula	0503 40D8h + formula
40DCh + formula	DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j		0502 40DCh + formula	0503 40DCh + formula
40E0h + formula	LANE_TX_RECEIVER_DETECT_PREG__DRVCTRL_BSCAN_PREG_j		0502 40E0h + formula	0503 40E0h + formula
40E4h + formula	TX_RCVDDET_OVRD_PREG_j		0502 40E4h + formula	0503 40E4h + formula
40E8h + formula	TXCOEF_STATUS_PREG_j		0502 40E8h + formula	0503 40E8h + formula
40F0h + formula	LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROL_PREG_j		0502 40F0h + formula	0503 40F0h + formula
40F8h + formula	TX_LFPGEN_STATUS_PREG_j		0502 40F8h + formula	0503 40F8h + formula
4100h + formula	CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j		0502 4100h + formula	0503 4100h + formula
4108h + formula	RX_CREQ_FLTR_A_MODE3_PREG_j		0502 4108h + formula	0503 4108h + formula
410Ch + formula	RX_CREQ_FLTR_A_MODE1_PREG__RX_CREQ_FLTR_A_MODE2_PREG_j		0502 410Ch + formula	0503 410Ch + formula
4110h + formula	RX_CREQ_FLTR_B_PREG__RX_CREQ_FLTR_A_MODE0_PREG_j		0502 4110h + formula	0503 4110h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
4114h + formula	RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BU MP_PREG_j		0502 4114h + formula	0503 4114h + formula
4118h + formula	CREQ_CCLKDET_MODE23_PREG__CREQ_DCBI ASATTEN_OVR_PREG_j		0502 4118h + formula	0503 4118h + formula
411Ch + formula	RX_CTLE_CAL_PREG__CREQ_CCLKDET_MODE 01_PREG_j		0502 411Ch + formula	0503 411Ch + formula
4120h + formula	RX_CTLE_MAINTENANCE_PREG__RX_CTLE_CT RL_PREG_j		0502 4120h + formula	0503 4120h + formula
4124h + formula	CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_ PREG_j		0502 4124h + formula	0503 4124h + formula
4128h + formula	RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_ PREG_j		0502 4128h + formula	0503 4128h + formula
412Ch + formula	CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_ SPARE_PREG_j		0502 412Ch + formula	0503 412Ch + formula
4130h + formula	CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_ PREG_j		0502 4130h + formula	0503 4130h + formula
4134h + formula	CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_ PREG_j		0502 4134h + formula	0503 4134h + formula
4138h + formula	CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_ PREG_j		0502 4138h + formula	0503 4138h + formula
413Ch + formula	CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_ PREG_j		0502 413Ch + formula	0503 413Ch + formula
4140h + formula	CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_ PREG_j		0502 4140h + formula	0503 4140h + formula
4144h + formula	CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_ PREG_j		0502 4144h + formula	0503 4144h + formula
4148h + formula	CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_ PREG_j		0502 4148h + formula	0503 4148h + formula
414Ch + formula	CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_ PREG_j		0502 414Ch + formula	0503 414Ch + formula
4150h + formula	CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_ PREG_j		0502 4150h + formula	0503 4150h + formula
4154h + formula	CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_ PREG_j		0502 4154h + formula	0503 4154h + formula
4158h + formula	CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_ PREG_j		0502 4158h + formula	0503 4158h + formula
415Ch + formula	CTLELUT_OVR_10B_PREG__CTLELUT_OVR_10 A_PREG_j		0502 415Ch + formula	0503 415Ch + formula
4160h + formula	CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A _PREG_j		0502 4160h + formula	0503 4160h + formula
4164h + formula	CTLELUT_OVR_12B_PREG__CTLELUT_OVR_12 A_PREG_j		0502 4164h + formula	0503 4164h + formula
4168h + formula	CTLELUT_OVR_13B_PREG__CTLELUT_OVR_13 A_PREG_j		0502 4168h + formula	0503 4168h + formula
416Ch + formula	CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14 A_PREG_j		0502 416Ch + formula	0503 416Ch + formula
4170h + formula	CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15 A_PREG_j		0502 4170h + formula	0503 4170h + formula
4180h + formula	DFE_SMP_RATESEL_PREG__DFE_ECMP_RATE SEL_PREG_j		0502 4180h + formula	0503 4180h + formula
4184h + formula	DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j		0502 4184h + formula	0503 4184h + formula
4188h + formula	DEQ_PHALIGN_CTRL_j		0502 4188h + formula	0503 4188h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
4190h + formula	DEQ_CONCUR_CTRL2_PREG__DEQ_CONCUR_CTRL1_PREG_j		0502 4190h + formula	0503 4190h + formula
4194h + formula	DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j		0502 4194h + formula	0503 4194h + formula
4198h + formula	DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j		0502 4198h + formula	0503 4198h + formula
419Ch + formula	RX_DEQ_COEF_FIFO_PREG__DEQ_FAST_MAIN_T_CYCLES_PREG_j		0502 419Ch + formula	0503 419Ch + formula
41A0h + formula	DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j		0502 41A0h + formula	0503 41A0h + formula
41A4h + formula	CMP_AVR_TIMER_PREG__DEQ_ERRCMPB_OVR_PREG_j		0502 41A4h + formula	0503 41A4h + formula
41B0h + formula	DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j		0502 41B0h + formula	0503 41B0h + formula
41C0h + formula	DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j		0502 41C0h + formula	0503 41C0h + formula
41D0h + formula	DEQ_GLUT1__DEQ_GLUT0_j		0502 41D0h + formula	0503 41D0h + formula
41D4h + formula	DEQ_GLUT3__DEQ_GLUT2_j		0502 41D4h + formula	0503 41D4h + formula
41D8h + formula	DEQ_GLUT5__DEQ_GLUT4_j		0502 41D8h + formula	0503 41D8h + formula
41DCh + formula	DEQ_GLUT7__DEQ_GLUT6_j		0502 41DCh + formula	0503 41DCh + formula
41E0h + formula	DEQ_GLUT9__DEQ_GLUT8_j		0502 41E0h + formula	0503 41E0h + formula
41E4h + formula	DEQ_GLUT11__DEQ_GLUT10_j		0502 41E4h + formula	0503 41E4h + formula
41E8h + formula	DEQ_GLUT13__DEQ_GLUT12_j		0502 41E8h + formula	0503 41E8h + formula
41ECh + formula	DEQ_GLUT15__DEQ_GLUT14_j		0502 41ECh + formula	0503 41ECh + formula
41F0h + formula	DEQ_GLUT17__DEQ_GLUT16_j		0502 41F0h + formula	0503 41F0h + formula
41F4h + formula	DEQ_GLUT19__DEQ_GLUT18_j		0502 41F4h + formula	0503 41F4h + formula
41F8h + formula	DEQ_GLUT21__DEQ_GLUT20_j		0502 41F8h + formula	0503 41F8h + formula
41FCh + formula	DEQ_GLUT23__DEQ_GLUT22_j		0502 41FCh + formula	0503 41FCh + formula
4200h + formula	DEQ_GLUT25__DEQ_GLUT24_j		0502 4200h + formula	0503 4200h + formula
4204h + formula	DEQ_GLUT27__DEQ_GLUT26_j		0502 4204h + formula	0503 4204h + formula
4208h + formula	DEQ_GLUT29__DEQ_GLUT28_j		0502 4208h + formula	0503 4208h + formula
420Ch + formula	DEQ_GLUT31__DEQ_GLUT30_j		0502 420Ch + formula	0503 420Ch + formula
4210h + formula	DEQ_ALUT1__DEQ_ALUT0_j		0502 4210h + formula	0503 4210h + formula
4214h + formula	DEQ_ALUT3__DEQ_ALUT2_j		0502 4214h + formula	0503 4214h + formula
4218h + formula	DEQ_ALUT5__DEQ_ALUT4_j		0502 4218h + formula	0503 4218h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
421Ch + formula	DEQ_ALUT7__DEQ_ALUT6_j		0502 421Ch + formula	0503 421Ch + formula
4220h + formula	DEQ_ALUT9__DEQ_ALUT8_j		0502 4220h + formula	0503 4220h + formula
4224h + formula	DEQ_ALUT11__DEQ_ALUT10_j		0502 4224h + formula	0503 4224h + formula
4228h + formula	DEQ_ALUT13__DEQ_ALUT12_j		0502 4228h + formula	0503 4228h + formula
422Ch + formula	DEQ_ALUT15__DEQ_ALUT14_j		0502 422Ch + formula	0503 422Ch + formula
4230h + formula	DEQ_ALUT17__DEQ_ALUT16_j		0502 4230h + formula	0503 4230h + formula
4234h + formula	DEQ_ALUT19__DEQ_ALUT18_j		0502 4234h + formula	0503 4234h + formula
4238h + formula	DEQ_ALUT21__DEQ_ALUT20_j		0502 4238h + formula	0503 4238h + formula
423Ch + formula	DEQ_ALUT23__DEQ_ALUT22_j		0502 423Ch + formula	0503 423Ch + formula
4240h + formula	DEQ_ALUT25__DEQ_ALUT24_j		0502 4240h + formula	0503 4240h + formula
4244h + formula	DEQ_ALUT27__DEQ_ALUT26_j		0502 4244h + formula	0503 4244h + formula
4248h + formula	DEQ_ALUT29__DEQ_ALUT28_j		0502 4248h + formula	0503 4248h + formula
424Ch + formula	DEQ_ALUT31__DEQ_ALUT30_j		0502 424Ch + formula	0503 424Ch + formula
4250h + formula	DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j		0502 4250h + formula	0503 4250h + formula
4254h + formula	DEQ_DFETAP1__DEQ_DFETAP0_OVR_j		0502 4254h + formula	0503 4254h + formula
4258h + formula	DEQ_DFETAP2__DEQ_DFETAP1_OVR_j		0502 4258h + formula	0503 4258h + formula
425Ch + formula	DEQ_DFETAP3__DEQ_DFETAP2_OVR_j		0502 425Ch + formula	0503 425Ch + formula
4260h + formula	DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j		0502 4260h + formula	0503 4260h + formula
4264h + formula	DATDFE_TAPCAP_THRESH_PREG__DEQ_DFETAP4_OVR_j		0502 4264h + formula	0503 4264h + formula
4268h + formula	DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG_j		0502 4268h + formula	0503 4268h + formula
426Ch + formula	DFE_EN_1010_IGNORE_DIAG_PREG_j		0502 426Ch + formula	0503 426Ch + formula
4270h + formula	DEQ_PRECUR_PREG_j		0502 4270h + formula	0503 4270h + formula
4280h + formula	DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j		0502 4280h + formula	0503 4280h + formula
4284h + formula	DEQ_POSTCUR_DECR_PREG_j		0502 4284h + formula	0503 4284h + formula
4290h + formula	DEQ_FALSEEYE_CTRL_PREG_j		0502 4290h + formula	0503 4290h + formula
429Ch + formula	DEQ_TAU_CTRL1_FAST_MAINT_PREG_j		0502 429Ch + formula	0503 429Ch + formula
42A0h + formula	DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j		0502 42A0h + formula	0503 42A0h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
42A4h + formula	DEQ_BLK_TAU_DELTA_PREG_DEQ_TAU_CTRL_3_PREG_j		0502 42A4h + formula	0503 42A4h + formula
42B0h + formula	DEQ_OPENEYE_CTRL_PREG_j		0502 42B0h + formula	0503 42B0h + formula
42C0h + formula	DEQ_PICTRL_PREG_DEQ_PI_OVR_CTRL_PREG_j		0502 42C0h + formula	0503 42C0h + formula
42D0h + formula	CPICAL_CAP_STARTCODE_MODE23_PREG_CPICAL_CTRL_PREG_j		0502 42D0h + formula	0503 42D0h + formula
42D4h + formula	CPICAL_CAP_OVR_PREG_CPICAL_CAP_STARTCODE_MODE01_PREG_j		0502 42D4h + formula	0503 42D4h + formula
42D8h + formula	CPICAL_CAP_ITERTMR_PREG_CPICAL_CAP_INITTMR_PREG_j		0502 42D8h + formula	0503 42D8h + formula
42DCh + formula	CPICAL_TMRVAL_MODE2_PREG_CPICAL_TMRVAL_MODE3_PREG_j		0502 42DCh + formula	0503 42DCh + formula
42E0h + formula	CPICAL_TMRVAL_MODE0_PREG_CPICAL_TMRVAL_MODE1_PREG_j		0502 42E0h + formula	0503 42E0h + formula
42E4h + formula	CPICAL_PICNT_MODE2_PREG_CPICAL_PICNT_MODE3_PREG_j		0502 42E4h + formula	0503 42E4h + formula
42E8h + formula	CPICAL_PICNT_MODE0_PREG_CPICAL_PICNT_MODE1_PREG_j		0502 42E8h + formula	0503 42E8h + formula
42ECh + formula	CPICAL_STATUS_PREG_j		0502 42ECh + formula	0503 42ECh + formula
42F0h + formula	CPICAL_OFFSET_PREG_j		0502 42F0h + formula	0503 42F0h + formula
42F8h + formula	CPI_OUTBUF_RATESEL_PREG_j		0502 42F8h + formula	0503 42F8h + formula
42FCh + formula	CPI_TRIM_PREG_CPI_RESBIAS_BIN_PREG_j		0502 42FCh + formula	0503 42FCh + formula
4300h + formula	CPI_R2DEC_OVR_PREG_CPI_R1DEC_OVR_PREG_j		0502 4300h + formula	0503 4300h + formula
4304h + formula	CPICAL_RES_STARTCODE_MODE23_PREG_CPICAL_INCR_DECR_PREG_j		0502 4304h + formula	0503 4304h + formula
4308h + formula	CPICAL_RES_INITTMR_PREG_CPICAL_RES_STARTCODE_MODE01_PREG_j		0502 4308h + formula	0503 4308h + formula
430Ch + formula	EPI_CTRL_PREG_CPICAL_RES_ITERTMR_PREG_j		0502 430Ch + formula	0503 430Ch + formula
4310h + formula	LFPSFILT_MD_PREG_LFPSDET_SUPPORT_PREG_j		0502 4310h + formula	0503 4310h + formula
4314h + formula	LFPSFILT_RD_PREG_LFPSFILT_NS_PREG_j		0502 4314h + formula	0503 4314h + formula
4318h + formula	LFPSFILT_MP_PREG_j		0502 4318h + formula	0503 4318h + formula
4320h + formula	SDFILT_H2L_A_PREG_SIGDET_SUPPORT_PREG_j		0502 4320h + formula	0503 4320h + formula
4324h + formula	SDFILT_L2H_PREG_SDFILT_H2L_B_PREG_j		0502 4324h + formula	0503 4324h + formula
4328h + formula	SDCAL_OVR_PREG_SDCAL_CTRL_PREG_j		0502 4328h + formula	0503 4328h + formula
432Ch + formula	SDCAL_TUNE_PREG_SDCAL_START_PREG_j		0502 432Ch + formula	0503 432Ch + formula
4330h + formula	SDCAL_ITER_PREG_SDCAL_INIT_PREG_j		0502 4330h + formula	0503 4330h + formula
4338h + formula	RXTERM_ENABLE_PREG_RXTERM_BSCAN_PREG_j		0502 4338h + formula	0503 4338h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
433Ch + formula	RXBUFFER_RCDCTRL_PREG__RXBUFFER_C TCTRL_PREG_j		0502 433Ch + formula	0503 433Ch + formula
4340h + formula	RXBUFFER_DFCTRL_PREG_j		0502 4340h + formula	0503 4340h + formula
4348h + formula	DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_C TRL_PREG_j		0502 4348h + formula	0503 4348h + formula
434Ch + formula	DEQ_EYESURF_ACCUMB__DEQ_EYESURF_AC CUMA_j		0502 434Ch + formula	0503 434Ch + formula
4350h + formula	RX_BIST_SYNCCNT_PREG__RX_BIST_CONTRO LS_PREG_j		0502 4350h + formula	0503 4350h + formula
4354h + formula	RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PRE G_j		0502 4354h + formula	0503 4354h + formula
4360h + formula	LN_SPARE_REG_PREG_j		0502 4360h + formula	0503 4360h + formula
4370h + formula	PREADAPT_CTRL_PREG_j		0502 4370h + formula	0503 4370h + formula
4380h + formula	LN_CTRL_DIAG_RESET_PREG__LN_FPWRISO_ DIAG_RESET_PREG_j		0502 4380h + formula	0503 4380h + formula
4384h + formula	LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTR L_DIAG_RESET_PREG_j		0502 4384h + formula	0503 4384h + formula
4388h + formula	LN_RXDSYNC_DIAG_RESET_PREG__LN_RXCTR L_DIAG_RESET_PREG_j		0502 4388h + formula	0503 4388h + formula
4390h + formula	LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_ CLK_FREQ_MSMT_CTRL_PREG_j		0502 4390h + formula	0503 4390h + formula
4394h + formula	LN_CLK_FREQ_MSMT_OBS_PREG__LN_CMSMT _TEST_CLK_CNT_VALUE_PREG_j		0502 4394h + formula	0503 4394h + formula
43A0h + formula	RXMRGN_CTRL_PREG_j		0502 43A0h + formula	0503 43A0h + formula
43B0h + formula	SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j		0502 43B0h + formula	0503 43B0h + formula
43B4h + formula	SMPCAL_NUM_WORDS_PREG__SMPCAL_ITER_ PREG_j		0502 43B4h + formula	0503 43B4h + formula
43B8h + formula	SMPCAL_TUNE_PREG__SMPCAL_START_PREG _j		0502 43B8h + formula	0503 43B8h + formula
43BCh + formula	SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_ _CALEVNCODE_OVR_PREG_j		0502 43BCh + formula	0503 43BCh + formula
43C0h + formula	SMPCAL_CALODDCODE_PREG__SMPCAL_CAL EVNCODE_PREG_j		0502 43C0h + formula	0503 43C0h + formula
43C4h + formula	SMPCAL_STATE_PREG_j		0502 43C4h + formula	0503 43C4h + formula
43D0h + formula	DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_T AU_CTRL1_PREG_j		0502 43D0h + formula	0503 43D0h + formula
43D4h + formula	DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_ VTH_PREG_j		0502 43D4h + formula	0503 43D4h + formula
43D8h + formula	DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_ CTRL1_PREG_j		0502 43D8h + formula	0503 43D8h + formula
43DCh + formula	DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_ CTRL3_PREG_j		0502 43DCh + formula	0503 43DCh + formula
6000h + formula	RESERVEDBIT13ADDRESSB_y		0502 6000h + formula	0503 6000h + formula
8000h + formula	RESERVEDSIERRAREP8000_y		0502 8000h + formula	0503 8000h + formula
A000h + formula	RESERVEDBIT13ADDRESSC_y		0502 A000h + formula	0503 A000h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
C000h	PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1		0502 C000h	0503 C000h
C004h	PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1		0502 C004h	0503 C004h
C008h	PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG		0502 C008h	0503 C008h
C00Ch	PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RC_V_DET_INH		0502 C00Ch	0503 C00Ch
C010h	PHY_ISO_CMN_CTRL		0502 C010h	0503 C010h
C014h	PHY_STATE_CHG_TIMEOUT		0502 C014h	0503 C014h
C01Ch	PHY_AUTO_CFG_CTRL__PHY_PLL_CFG		0502 C01Ch	0503 C01Ch
C020h	PHY_REFCLK1_DET_THRES_LOW__PHY_REFCLK_DET_THRES_LOW		0502 C020h	0503 C020h
C024h	PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_HIGH		0502 C024h	0503 C024h
C028h	PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_DET_INTERVAL		0502 C028h	0503 C028h
C02Ch	PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_DET_OP_DELAY		0502 C02Ch	0503 C02Ch
C030h	PHY_REFCLK_DET_ISO_CTRL		0502 C030h	0503 C030h
C034h	PHY_PIPE_LM_CFG0		0502 C034h	0503 C034h
C038h	PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1		0502 C038h	0503 C038h
C03Ch	PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3		0502 C03Ch	0503 C03Ch
C040h	PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0		0502 C040h	0503 C040h
C044h	PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0		0502 C044h	0503 C044h
D000h + formula	PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j		0502 D000h + formula	0503 D000h + formula
D004h + formula	PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j		0502 D004h + formula	0503 D004h + formula
D008h + formula	PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j		0502 D008h + formula	0503 D008h + formula
D00Ch + formula	PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j		0502 D00Ch + formula	0503 D00Ch + formula
D010h + formula	PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j		0502 D010h + formula	0503 D010h + formula
D014h + formula	PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j		0502 D014h + formula	0503 D014h + formula
D018h + formula	PHY_PIPE_ISO_USB_BER_CNT_j		0502 D018h + formula	0503 D018h + formula
D01Ch + formula	PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j		0502 D01Ch + formula	0503 D01Ch + formula
D020h + formula	PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j		0502 D020h + formula	0503 D020h + formula
D024h + formula	PHY_INTERRUPT_STS_j		0502 D024h + formula	0503 D024h + formula
D030h + formula	PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j		0502 D030h + formula	0503 D030h + formula
D034h + formula	PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j		0502 D034h + formula	0503 D034h + formula

Table 11-3. SERDES_16G Registers (continued)

Offset	Acronym	Register Name	SERDES_16G2 Physical Address	SERDES_16G3 Physical Address
D038h + formula	PHY_PIPE_ISO_LM_PHY2MAC1_j		0502 D038h + formula	0503 D038h + formula
D03Ch + formula	PHY_PIPE_ISO_LM_PHY2MAC_STS_j		0502 D03Ch + formula	0503 D03Ch + formula
E000h	PHY_PMA_CMN_CTRL		0502 E000h	0503 E000h
E008h	PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_I SO_CMN_CTRL		0502 E008h	0503 E008h
E00Ch	PHY_PMA_ISO_RESCAL		0502 E00Ch	0503 E00Ch
E01Ch	PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_IS OLATION_CTRL		0502 E01Ch	0503 E01Ch
F000h + formula	PHY_PMA_XCVR_CTRL_j		0502 F000h + formula	0503 F000h + formula
F004h + formula	PHY_PMA_ISO_XCVR_CTRL_j		0502 F004h + formula	0503 F004h + formula
F008h + formula	PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX _LPC_LO_j		0502 F008h + formula	0503 F008h + formula
F00Ch + formula	PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_T X_DMPH_LO_j		0502 F00Ch + formula	0503 F00Ch + formula
F010h + formula	PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_F SLF_j		0502 F010h + formula	0503 F010h + formula
F014h + formula	PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_ LINK_MODE_j		0502 F014h + formula	0503 F014h + formula
F018h + formula	PHY_PMA_ISO_RX_EQ_CTRL_j		0502 F018h + formula	0503 F018h + formula
F01Ch + formula	PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA _LO_j		0502 F01Ch + formula	0503 F01Ch + formula
F020h + formula	PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ ISO_LN_MRGN_CTRL_j		0502 F020h + formula	0503 F020h + formula

11.1 MACRO_ID_REG Register (Offset = 0h) [reset = X]

MACRO_ID_REG is shown in [Figure 11-1](#) and described in [Table 11-5](#).

Return to [Summary Table](#).

MACRO_ID_REG

Table 11-4. MACRO_ID_REG Instances

Instance	Physical Address
SERDES_16G0	0500 0000h
SERDES_16G1	0501 0000h
SERDES_16G2	0502 0000h
SERDES_16G3	0503 0000h

Figure 11-1. MACRO_ID_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MACRO_ID_TYPE															
R-X																R-7364h															

LEGEND: R = Read Only; -n = value after reset

Table 11-5. MACRO_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MACRO_ID_TYPE	R	7364h	ASCII representation of sd for SerDes type.

Table 11-6. Register Call Summary for MACRO_ID_REG

16-G SerDes Registers

- [2-L SerDes Registers](#): [0] [1]
- [MACRO_ID_REG Register \(Offset = 0h\) \[reset = X\]](#): [0] [1]

11.2 MACRO_ID_NUMBER_REG Register (Offset = 4h) [reset = X]

MACRO_ID_NUMBER_REG is shown in [Figure 11-2](#) and described in [Table 11-8](#).

Return to [Summary Table](#).

MACRO_ID_NUMBER_REG

Table 11-7. MACRO_ID_NUMBER_REG Instances

Instance	Physical Address
SERDES_16G0	0500 0004h
SERDES_16G1	0501 0004h
SERDES_16G2	0502 0004h
SERDES_16G3	0503 0004h

Figure 11-2. MACRO_ID_NUMBER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACRO_ID_NUMBER																RESERVED															
R-301h																R-X															

LEGEND: R = Read Only; -n = value after reset

Table 11-8. MACRO_ID_NUMBER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MACRO_ID_NUMBER	R	301h	Product family in binary coded decimal.
15-0	RESERVED	R	X	

Table 11-9. Register Call Summary for MACRO_ID_NUMBER_REG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [MACRO_ID_NUMBER_REG Register \(Offset = 4h\) \[reset = X\]: \[0\] \[1\]](#)

11.3 MACRO_ID_REV_REG Register (Offset = 8h) [reset = X]

MACRO_ID_REV_REG is shown in [Figure 11-3](#) and described in [Table 11-11](#).

Return to [Summary Table](#).

Note this read-only field may vary from product to product.

Table 11-10. MACRO_ID_REV_REG Instances

Instance	Physical Address
SERDES_16G0	0500 0008h
SERDES_16G1	0501 0008h
SERDES_16G2	0502 0008h
SERDES_16G3	0503 0008h

Figure 11-3. MACRO_ID_REV_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MACRO_ID_REV															
R-X																R-600h															

LEGEND: R = Read Only; -n = value after reset

Table 11-11. MACRO_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MACRO_ID_REV	R	600h	Revision number in binary coded decimal.

Table 11-12. Register Call Summary for MACRO_ID_REV_REG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [MACRO_ID_REV_REG Register \(Offset = 8h\) \[reset = X\]: \[0\]](#)

11.4 MACRO_ID_NODE_REG__MACRO_ID_MFG_REG Register (Offset = 10h) [reset = 00160074h]

MACRO_ID_NODE_REG__MACRO_ID_MFG_REG is shown in Figure 11-4 and described in Table 11-14.

Return to [Summary Table](#).

Note this read-only field may vary from product to product.

Table 11-13.
MACRO_ID_NODE_REG__MACRO_ID_MFG_REG
Instances

Instance	Physical Address
SERDES_16G0	0500 0010h
SERDES_16G1	0501 0010h
SERDES_16G2	0502 0010h
SERDES_16G3	0503 0010h

Figure 11-4. MACRO_ID_NODE_REG__MACRO_ID_MFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACRO_ID_NODE																MACRO_ID_MFG															
R-16h																R-74h															

LEGEND: R = Read Only; -n = value after reset

Table 11-14. MACRO_ID_NODE_REG__MACRO_ID_MFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MACRO_ID_NODE	R	16h	Technology node in binary coded decimal
15-0	MACRO_ID_MFG	R	74h	ASCII representation of the manufacturer.

Table 11-15. Register Call Summary for MACRO_ID_NODE_REG__MACRO_ID_MFG_REG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [MACRO_ID_NODE_REG__MACRO_ID_MFG_REG Register \(Offset = 10h\) \[reset = 00160074h\]: \[0\]](#)

11.5 MACRO_ID_FLAVOR_REG Register (Offset = 14h) [reset = X]

MACRO_ID_FLAVOR_REG is shown in Figure 11-5 and described in Table 11-17.

Return to [Summary Table](#).

Note this read-only field may vary from product to product.

Table 11-16. MACRO_ID_FLAVOR_REG Instances

Instance	Physical Address
SERDES_16G0	0500 0014h
SERDES_16G1	0501 0014h
SERDES_16G2	0502 0014h
SERDES_16G3	0503 0014h

Figure 11-5. MACRO_ID_FLAVOR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MACRO_ID_FLAVOR															
R-X																R-6663h															

LEGEND: R = Read Only; -n = value after reset

Table 11-17. MACRO_ID_FLAVOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	MACRO_ID_FLAVOR	R	6663h	ASCII representation of fc for finfet compact flavor.

Table 11-18. Register Call Summary for MACRO_ID_FLAVOR_REG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [MACRO_ID_FLAVOR_REG Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)

11.6 MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG Register (Offset = 18h) [reset = X]

MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG is shown in Figure 11-6 and described in Table 11-20.

Return to [Summary Table](#).

Note this read-only field may vary from product to product.

Table 11-19. MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG Instances

Instance	Physical Address
SERDES_16G0	0500 0018h
SERDES_16G1	0501 0018h
SERDES_16G2	0502 0018h
SERDES_16G3	0503 0018h

Figure 11-6. MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACRO_ID_NUM_LANES_LEFT								MACRO_ID_NUM_LANES_RIGHT							
R-1h								R-1h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MACRO_ID_IO_VOLTAGE							
R-X								R-180h							

LEGEND: R = Read Only; -n = value after reset

Table 11-20. MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MACRO_ID_NUM_LANE S_LEFT	R	1h	The number of lanes on the left side of the common module in binary coded decimal.
23-16	MACRO_ID_NUM_LANE S_RIGHT	R	1h	The number of lanes on the right side of the common module in binary coded decimal.
15-10	RESERVED	R	X	
9-0	MACRO_ID_IO_VOLTAGE	R	180h	Product I/O voltage ID in binary coded decimal. Lower byte is voltage right of the decimal. Most-significant byte is voltage left of the decimal.

Table 11-21. Register Call Summary for MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [MACRO_ID_NUM_LANES_REG__MACRO_ID_IO_VOLTAGE_REG Register \(Offset = 18h\) \[reset = X\]: \[0\]](#)

11.7 MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG Register (Offset = 20h) [reset = 214h]

MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG is shown in Figure 11-7 and described in Table 11-23.

Return to [Summary Table](#).

Note this read-only field may vary from product to product.

Table 11-22.
MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG
Instances

Instance	Physical Address
SERDES_16G0	0500 0020h
SERDES_16G1	0501 0020h
SERDES_16G2	0502 0020h
SERDES_16G3	0503 0020h

Figure 11-7. MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACRO_ID_XC				MACRO_ID_XY				MACRO_ID_Y				MACRO_ID_YY			
R-0h				R-0h				R-0h				R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACRO_ID_X				MACRO_ID_XA				MACRO_ID_XD				MACRO_ID_XE			
R-0h				R-2h				R-1h				R-4h			

LEGEND: R = Read Only; -n = value after reset

Table 11-23. MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	MACRO_ID_XC	R	0h	Number xc metals in stack up in binary decimal format.
27-24	MACRO_ID_XY	R	0h	Number xy metals in stack up in binary decimal format.
23-20	MACRO_ID_Y	R	0h	Number y metals in stack up in binary decimal format.
19-16	MACRO_ID_YY	R	0h	Number yy metals in stack up in binary decimal format.
15-12	MACRO_ID_X	R	0h	Number x metals in stack up in binary decimal format.
11-8	MACRO_ID_XA	R	2h	Number xa metals in stack up in binary decimal format.
7-4	MACRO_ID_XD	R	1h	Number xd metals in stack up in binary decimal format.
3-0	MACRO_ID_XE	R	4h	Number xe metals in stack up in binary decimal format.

Table 11-24. Register Call Summary for
MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [MACRO_ID_METAL_LAYERS_1_REG__MACRO_ID_METAL_LAYERS_0_REG Register \(Offset = 20h\) \[reset = 214h\]: \[0\]](#)

11.8 MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG Register (Offset = 24h) [reset = X]

MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG is shown in Figure 11-8 and described in Table 11-26.

Return to [Summary Table](#).

Note this read-only field may vary from product to product.

Table 11-25.
MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG
Instances

Instance	Physical Address
SERDES_16G0	0500 0024h
SERDES_16G1	0501 0024h
SERDES_16G2	0502 0024h
SERDES_16G3	0503 0024h

Figure 11-8. MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MACRO_ID_XD_DIR							
R-X								R-68h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACRO_ID_YZ				MACRO_ID_Z				MACRO_ID_R				MACRO_ID_U			
R-0h				R-0h				R-2h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 11-26. MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	MACRO_ID_XD_DIR	R	68h	Direction of xd metal in ASCII format.
15-12	MACRO_ID_YZ	R	0h	Number yz metals in stack up in binary decimal format.
11-8	MACRO_ID_Z	R	0h	Number z metals in stack up in binary decimal format.
7-4	MACRO_ID_R	R	2h	Number r metals in stack up in binary decimal format.
3-0	MACRO_ID_U	R	0h	Number u metals in stack up in binary decimal format.

Table 11-27. Register Call Summary for
MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [MACRO_ID_METAL_LAYERS_3_REG__MACRO_ID_METAL_LAYERS_2_REG Register \(Offset = 24h\) \[reset = X\]: \[0\]](#)

11.9 MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG Register (Offset = 28h) [reset = 76687668h]

MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG is shown in Figure 11-9 and described in Table 11-29.

Return to [Summary Table](#).

Note this read-only field may vary from product to product.

Table 11-28.
MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG
Instances

Instance	Physical Address
SERDES_16G0	0500 0028h
SERDES_16G1	0501 0028h
SERDES_16G2	0502 0028h
SERDES_16G3	0503 0028h

Figure 11-9. MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACRO_ID_XE3_DIR								MACRO_ID_XE4_DIR							
R-76h								R-68h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACRO_ID_XE1_DIR								MACRO_ID_XE2_DIR							
R-76h								R-68h							

LEGEND: R = Read Only; -n = value after reset

Table 11-29. MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MACRO_ID_XE3_DIR	R	76h	Direction of second highest lowest xe metal in ASCII format.
23-16	MACRO_ID_XE4_DIR	R	68h	Direction of highest xe metal in ASCII format.
15-8	MACRO_ID_XE1_DIR	R	76h	Direction of lowest xe metal in ASCII format.
7-0	MACRO_ID_XE2_DIR	R	68h	Direction of second lowest xe metal in ASCII format.

Table 11-30. Register Call Summary for
MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG

- 16-G SerDes Registers
- [2-L SerDes Registers: \[0\] \[1\]](#)
 - [MACRO_ID_METAL_LAYERS_5_REG__MACRO_ID_METAL_LAYERS_4_REG Register \(Offset = 28h\) \[reset = 76687668h\]: \[0\]](#)

11.10 CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG Register (Offset = 40h) [reset = X]

CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG is shown in Figure 11-10 and described in Table 11-32.

Return to [Summary Table](#).

Common power-gated supply island control register.

Table 11-31. CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0040h
SERDES_16G1	0501 0040h
SERDES_16G2	0502 0040h
SERDES_16G3	0503 0040h

Figure 11-10. CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG Register

31	30	29	28	27	26	25	24
RESERVED			CMN_PWRISO_OVRD_EN_PREG	RESERVED			CMN_PWRISO_ISOLATION_EN_OVRD_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h
23	22	21	20	19	18	17	16
RESERVED			CMN_PWRISO_PHASE2EN_OVRD_PREG	RESERVED			CMN_PWRISO_PHASE1EN_OVRD_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h
15	14	13	12	11	10	9	8
RESERVED	CMN_PWRISO_PWRDN_DISABLE_PREG	RESERVED					
R/W-X	R/W-0h	R/W-X					
7	6	5	4	3	2	1	0
CMN_PWRISO_EN_PH2DLY_PREG				CMN_PWRISO_EN_PH1DLY_PREG			
R/W-1h				R/W-3h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-32. CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28	CMN_PWRISO_OVRD_EN_PREG	R/W	0h	cmn power gate active high override enable: When asserted, cmn_pwriso_isolation_en_ovrd_preg, cmn_pwriso_phase2en_ovrd_preg, and cmn_pwriso_phase1en_ovrd_preg directly control the power-gate enables and associated isolation .
27-25	RESERVED	R/W	X	
24	CMN_PWRISO_ISOLATION_EN_OVRD_PREG	R/W	0h	cmn power gate isolation override: When cmn_pwriso_ovrd_en_preg is asserted, this bit controls the cpwriso_power_isolation_en.
23-21	RESERVED	R/W	X	

**Table 11-32. CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
20	CMN_PWRISO_PHASE2 EN_OVRD_PREG	R/W	0h	cmn power gate phase2en override: When cmn_pwriso_ovrd_en_preg is asserted, this bit controls the phase2en to all cmn power gates.
19-17	RESERVED	R/W	X	
16	CMN_PWRISO_PHASE1 EN_OVRD_PREG	R/W	0h	cmn_pwriso power gate phase1en override: When cmn_pwriso_ovrd_en_preg is asserted, this bit controls the phase1en to all cmn power gates.
15	RESERVED	R/W	X	
14	CMN_PWRISO_PWRDN_ DISABLE_PREG	R/W	0h	Power down disable: Setting this bit to 1'b1 will disable turning off the common power-gated supplies when the macro is in a state that would normally switch the power islands off.
13-8	RESERVED	R/W	X	
7-4	CMN_PWRISO_EN_PH2 DLY_PREG	R/W	1h	Power enable phase 2 timer value: This value + 1 specifies the number of cmn_refclk cycles the Common power island control state machine will wait in the power phase 2 enable state.
3-0	CMN_PWRISO_EN_PH1 DLY_PREG	R/W	3h	Power enable phase 1 timer value: This value + 1 specifies the number of cmn_refclk cycles the Common power island control state machine will wait in the power phase 1 enable state.

Table 11-33. Register Call Summary for CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PWRISO_OVRD_PREG__CMN_PWRISO_CTRL_PREG Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)

11.11 CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BANDGAP_TMR_PREG Register (Offset = 60h) [reset = X]

CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BANDGAP_TMR_PREG is shown in Figure 11-11 and described in Table 11-35.

Return to [Summary Table](#).

Startup State Machine bandgap enable timer register.

Table 11-34.
CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BANDGAP_TMR_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0060h
SERDES_16G1	0501 0060h
SERDES_16G2	0502 0060h
SERDES_16G3	0503 0060h

Figure 11-11. CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BANDGAP_TMR_PREG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CMN_SSM_BIAS_TMR_VAL_PREG											
R/W-X				R/W-5Eh											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CMN_SSM_BANDGAP_TMR_VAL_PREG											
R/W-X				R/W-1h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-35. CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BANDGAP_TMR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_SSM_BIAS_TMR_VAL_PREG	R/W	5Eh	Bias enable state timer value : used for the timer when the startup state machine is in the bias enable state. The value must be 1 or greater. Defaulted to 1 to advance to SSM_PLLEN where bias and PLLcmnlc are be enabled for simultaneous startup.
15-12	RESERVED	R/W	X	
11-0	CMN_SSM_BANDGAP_TMR_VAL_PREG	R/W	1h	Bandgap enable state timer value : The value must be 1 or greater. Note deprecated usage in this Macro.

**Table 11-36. Register Call Summary for
CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BANDGAP_TMR_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_SSM_BIAS_TMR_PREG__CMN_SSM_BANDGAP_TMR_PREG Register \(Offset = 60h\) \[reset = X\]: \[0\]](#)

11.12 CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG Register (Offset = 64h) [reset = X]

CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG is shown in Figure 11-12 and described in Table 11-38.

Return to [Summary Table](#).

Startup State Machine diagnostic register.

Table 11-37.
CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0064h
SERDES_16G1	0501 0064h
SERDES_16G2	0502 0064h
SERDES_16G3	0503 0064h

Figure 11-12. CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG Register

31	30	29	28	27	26	25	24
RESERVED							CMN_SSM_STATE
R/W-X							R-0h
23	22	21	20	19	18	17	16
CMN_SSM_STATE							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CMN_SSM_DIAG_SKIP_AUTO_RECAL_PREG
R/W-X							R/W-1h
7	6	5	4	3	2	1	0
RESERVED							CMN_SSM_DIAG_SKIP_POST_BGEN_RECAL_PREG
R/W-X							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-38. CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	CMN_SSM_STATE	R	0h	Startup state machine current state: This is the current state of the startup state machine. Note this is for diagnostic purposes only.
15-9	RESERVED	R/W	X	
8	CMN_SSM_DIAG_SKIP_AUTO_RECAL_PREG	R/W	1h	Skip auto re-calibration enable : When this bit is active (1'b1), the auto calibration state will be skipped if it was previously run, unless the macro is disabled or reset.
7-1	RESERVED	R/W	X	

Table 11-38. CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMN_SSM_DIAG_SKIP_POST_BGGEN_RECAL_P REG	R/W	1h	Skip post bandgap enable re-calibration : When this bit is active (1'b1), the post bandgap enable calibration state will be skipped if it was previously run, unless the macro is disabled or reset. The bandgap enable calibration state is unnecessary and can always be skipped.

Table 11-39. Register Call Summary for CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_SSM_STATE_PREG__CMN_SSM_DIAG_PREG Register \(Offset = 64h\) \[reset = X\]: \[0\]](#)

11.13 CMN_SMCSM_STATE_PREG Register (Offset = 68h) [reset = X]

CMN_SMCSM_STATE_PREG is shown in Figure 11-13 and described in Table 11-41.

Return to [Summary Table](#).

Startup State Machine Multi-cal State Machine current state register.

Table 11-40. CMN_SMCSM_STATE_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0068h
SERDES_16G1	0501 0068h
SERDES_16G2	0502 0068h
SERDES_16G3	0503 0068h

Figure 11-13. CMN_SMCSM_STATE_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						CMN_SMCSM_STATE	
R-X						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 11-41. CMN_SMCSM_STATE_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1-0	CMN_SMCSM_STATE	R	0h	Startup State Machine Multi-cal State Machine current state register: This is the current state of the startup multi-cal state machine used to control the PLLLC calibration and the resistor calibration. Note this register is for diagnostic purposes only.

Table 11-42. Register Call Summary for CMN_SMCSM_STATE_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_SMCSM_STATE_PREG Register \(Offset = 68h\) \[reset = X\]: \[0\]](#)

11.14 CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG Register (Offset = 80h) [reset = X]

CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG is shown in [Figure 11-14](#) and described in [Table 11-44](#).

Return to [Summary Table](#).

PLLCMNLC status register A.

Table 11-43. CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0080h
SERDES_16G1	0501 0080h
SERDES_16G2	0502 0080h
SERDES_16G3	0503 0080h

Figure 11-14. CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_PLLLC_STATUS_B_SSTW OPT_CODE	
R-X						R-0h	
23	22	21	20	19	18	17	16
CMN_PLLLC_STATUS_B_SSTWOPT_CODE							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		CMN_PLLLC_STATUS_A_DSMMCORR_CODE					
R-X		R-0h					
7	6	5	4	3	2	1	0
CMN_PLLLC_S TATUS_A_LOC KED	CMN_PLLLC_S TATUS_A_DCO CAL_DONE	CMN_PLLLC_STATUS_A_DCOCAL_CODE					
R-0h	R-0h	R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 11-44. CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	CMN_PLLLC_STATUS_B_SSTWOPT_CODE	R	0h	Main PLLLC Spread Spectrum two point value result: Contains the sstwopt result. Note this register field is currently not supported.
15	RESERVED	R	X	
14-8	CMN_PLLLC_STATUS_A_DSMMCORR_CODE	R	0h	PLLCMNLC DSM spur correction code result: Contains the DSM spur correction value in gray code. Note this register is for diagnostic purposes only.
7	CMN_PLLLC_STATUS_A_LOCKED	R	0h	PLLCMNLC locked Status: 1 Locked 0 Not locked

Table 11-44. CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CMN_PLLLC_STATUS_A_DCOCAL_DONE	R	0h	PLLCMNLC DCO calibration status: 1 Calibration complete 0 Calibration has not completed Note this calibration status will deassert upon reset or when calibration starts and stay deasserted until calibration has completed.
5-0	CMN_PLLLC_STATUS_A_DCOCAL_CODE	R	0h	PLLCMNLC DCO calibration code result: Contains the calibration result. Note the contents of this register are not valid until cmn_plllc_status_a_dcocal_done has asserted. Note this register is for diagnostic purposes only.

Table 11-45. Register Call Summary for CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_STATUS_B_PREG__CMN_PLLLC_STATUS_A_PREG Register \(Offset = 80h\) \[reset = X\]: \[0\]](#)

11.15 CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG Register (Offset = 84h) [reset = X]

CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG is shown in Figure 11-15 and described in Table 11-47.

Return to [Summary Table](#).

PLLCMNLC general control register.

Table 11-46. CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0084h
SERDES_16G1	0501 0084h
SERDES_16G2	0502 0084h
SERDES_16G3	0503 0084h

Figure 11-15. CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_PLLLC_FBDIVINT_PREG	
R/W-X						R/W-32h	
23	22	21	20	19	18	17	16
CMN_PLLLC_FBDIVINT_PREG							
R/W-32h							
15	14	13	12	11	10	9	8
RESERVED		CMN_PLLLC_LOCKED_OVRD_EN_PREG	CMN_PLLLC_LOCKED_OVRD_PREG	RESERVED		CMN_PLLLC_PLL_REG_ISO_OVRD_EN_PREG	CMN_PLLLC_PLL_REG_ISO_OVRD_PREG
R/W-X		R/W-0h	R/W-0h	R/W-X		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CMN_PLLLC_LOCK_HOLD_OVRD_EN_PREG	CMN_PLLLC_LOCK_HOLD_OVRD_PREG	CMN_PLLLC_PLL_EN_OVRD_EN_PREG	CMN_PLLLC_PLL_EN_OVRD_PREG	CMN_PLLLC_PLL_RESET_N_OVRD_EN_PREG	CMN_PLLLC_PLL_RESET_N_OVRD_PREG	CMN_PLLLC_PLL_FDCLK1_SEL_PREG	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-47. CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	CMN_PLLLC_FBDIVINT_PREG	R/W	32h	This value sets the mode dependent PLLCMNLC fbdivint value.
15-14	RESERVED	R/W	X	
13	CMN_PLLLC_LOCKED_OVRD_EN_PREG	R/W	0h	PLLCMNLC locked active high override enable: Note this register is for diagnostic purposes only.
12	CMN_PLLLC_LOCKED_OVRD_PREG	R/W	0h	PLLCMNLC locked signal force: When cmn_plllic_locked_ovrd_en_preg is asserted high, this value overrides lock flag from PLLCMNLC. Note this register is for diagnostic purposes only.
11-10	RESERVED	R/W	X	
9	CMN_PLLLC_PLL_REG_ISO_OVRD_EN_PREG	R/W	0h	PLLCMNLC regulator isolation active high override enable Note this register is for diagnostic purposes only.

Table 11-47. CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
8	CMN_PLLLC_PLL_REG_ISO_OVRD_PREG	R/W	0h	When cmn_pll_reg_iso_ovrd_en_preg is asserted high, overrides the state dependent PLLCMNLC regulator isolation value. Note this register is for diagnostic purposes only.
7	CMN_PLLLC_LOCK_HOLD_OVRD_EN_PREG	R/W	0h	Lock detection hold function active high override enable. Note this register is for diagnostic purposes only.
6	CMN_PLLLC_LOCK_HOLD_OVRD_PREG	R/W	0h	When cmn_pll_lock_hold_ovrd_en_preg is asserted high, overrides the state dependent lock detect function value. Note this register is for diagnostic purposes only.
5	CMN_PLLLC_PLL_EN_OVRD_EN_PREG	R/W	0h	PLLCMNLC enable active high override enable. Note this register is for diagnostic purposes only.
4	CMN_PLLLC_PLL_EN_OVRD_PREG	R/W	0h	When cmn_pll_en_ovrd_en_preg is asserted high, overrides the state dependent PLLCMNLC enable value. Note this register is for diagnostic purposes only.
3	CMN_PLLLC_PLL_RESET_N_OVRD_EN_PREG	R/W	0h	PLLCMNLC active high reset override enable. Note this register is for diagnostic purposes only.
2	CMN_PLLLC_PLL_RESET_N_OVRD_PREG	R/W	0h	When cmn_pll_reset_n_ovrd_en_preg is asserted high, overrides the state dependent PLLCMNLC active low reset value. Note this register is for diagnostic purposes only.
1	CMN_PLLLC_PFDCLK1_SEL_PREG	R/W	0h	When asserted the pfdclk1 is used as the reference clock, When deasserted, pfdclk is used.
0	RESERVED	R/W	X	

Table 11-48. Register Call Summary for CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_FBDIV_INT_PREG__CMN_PLLLC_GEN_PREG Register \(Offset = 84h\) \[reset = X\]: \[0\]](#)

11.16 CMN_PLLLC_DCOCAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG Register (Offset = 88h) [reset = X]

CMN_PLLLC_DCOCAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG is shown in Figure 11-16 and described in Table 11-50.

Return to [Summary Table](#).

PLLCMNLC fractional feedback divider register.

Table 11-49.
CMN_PLLLC_DCOCAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0088h
SERDES_16G1	0501 0088h
SERDES_16G2	0502 0088h
SERDES_16G3	0503 0088h

Figure 11-16. CMN_PLLLC_DCOCAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_PLLLC_D COCAL_START _OVRD_EN_P REG	CMN_PLLLC_D COCAL_START _OVRD_PREG
R/W-X						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED		CMN_PLLLC_DCOCAL_STARTVAL_PREG					
R/W-X		R/W-12h					
15	14	13	12	11	10	9	8
CMN_PLLLC_FBDIVFRAC_PREG							
R/W-0h							
7	6	5	4	3	2	1	0
CMN_PLLLC_FBDIVFRAC_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-50. CMN_PLLLC_DCOCAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25	CMN_PLLLC_DCOCAL_S TART_OVRD_EN_PREG	R/W	0h	DCO calibration start active high override enable.
24	CMN_PLLLC_DCOCAL_S TART_OVRD_PREG	R/W	0h	When cmn_pll_cdcocal_start_ovrd_en_preg is asserted high, this value overrides the mode dependent DCO calibration start value.
23-22	RESERVED	R/W	X	
21-16	CMN_PLLLC_DCOCAL_S TARTVAL_PREG	R/W	12h	This value sets the DCO calibration startval value. Note: This must be set to a value that is always at least one step size away from the minimum and maximum calibration codes. For example, if the initial step size is 8 (cmn_pll_cdcocal_initstep_preg = 3'b011), this value must be at least 6'h08 and less than 6'h37.

Table 11-50. CMN_PLLLC_DCOCAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	CMN_PLLLC_FBDIVFRAC_PREG	R/W	0h	This value sets the mode dependent PLLCMNLC fbdivfrac value.

**Table 11-51. Register Call Summary for
CMN_PLLLC_DCOCAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_DCOCAL_CTRL_PREG__CMN_PLLLC_FBDIV_FRAC_PREG Register \(Offset = 88h\) \[reset = X\]: \[0\]](#)

11.17 CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG Register (Offset = 8Ch) [reset = X]

CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG is shown in Figure 11-17 and described in Table 11-53.

Return to [Summary Table](#).

PLLCMNLC DCO calibration initialization register.

Table 11-52. CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 008Ch
SERDES_16G1	0501 008Ch
SERDES_16G2	0502 008Ch
SERDES_16G3	0503 008Ch

Figure 11-17. CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_PLLLC_DCOCAL_ITERTMR_PREG			
R/W-X				R/W-6Eh			
23	22	21	20	19	18	17	16
CMN_PLLLC_DCOCAL_ITERTMR_PREG							
R/W-6Eh							
15	14	13	12	11	10	9	8
RESERVED	CMN_PLLLC_DCOCAL_INITSTEP_PREG			CMN_PLLLC_DCOCAL_INITTMR_PREG			
R/W-X		R/W-3h			R/W-5Ah		
7	6	5	4	3	2	1	0
CMN_PLLLC_DCOCAL_INITTMR_PREG							
R/W-5Ah							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-53. CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLC_DCOCAL_I TERTMR_PREG	R/W	6Eh	This value sets the DCO calibration iteration timer value.
15	RESERVED	R/W	X	
14-12	CMN_PLLLC_DCOCAL_I NITSTEP_PREG	R/W	3h	This value sets the DCO calibration initialization step value. 3'b 000 : 1 step 3'b 001 : 2 step 3'b 010 : 4 step 3'b 011 : 8 step 3'b 100 : 16 step 3'b 101 - 3'b 111 : reserved
11-0	CMN_PLLLC_DCOCAL_I NITTMR_PREG	R/W	5Ah	This value sets the DCO calibration initialization timer value.

Table 11-54. Register Call Summary for CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_ITERTMR_PREG__CMN_PLLLC_INIT_PREG Register \(Offset = 8Ch\) \[reset = X\]: \[0\]](#)

11.18 CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG Register (Offset = 90h) [reset = X]

CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG is shown in Figure 11-18 and described in Table 11-56.

Return to [Summary Table](#).

PLLCMNLC mode register.

Table 11-55.
CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0090h
SERDES_16G1	0501 0090h
SERDES_16G2	0502 0090h
SERDES_16G3	0503 0090h

Figure 11-18. CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG Register

31	30	29	28	27	26	25	24
RESERVED	CMN_PLLLC_LF_PROPCOEFF_MODE1_PREG			RESERVED			CMN_PLLLC_LF_PROPFRAC_MODE1_PREG
R/W-X	R/W-2h			R/W-X			R/W-0h
23	22	21	20	19	18	17	16
CMN_PLLLC_LF_PROPFRAC_MODE1_PREG				CMN_PLLLC_LF_INTCOEFF_MODE1_PREG			
R/W-0h				R/W-5h			
15	14	13	12	11	10	9	8
RESERVED							CMN_PLLLC_INTMODE_PREG
R/W-X							R/W-1h
7	6	5	4	3	2	1	0
RESERVED				CMN_PLLLC_TDCMODE_PREG			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-56. CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	CMN_PLLLC_LF_PROPCOEFF_MODE1_PREG	R/W	2h	This value sets the loop filter proportional coefficient value when cmn_pllnc_mode is asserted.
27-25	RESERVED	R/W	X	
24-20	CMN_PLLLC_LF_PROPFRAC_MODE1_PREG	R/W	0h	This value sets the loop filter fractional coefficient value when cmn_pllnc_mode is asserted.
19-16	CMN_PLLLC_LF_INTCOEFF_MODE1_PREG	R/W	5h	This value sets the loop filter integer coefficient value when cmn_pllnc_mode is asserted.
15-9	RESERVED	R/W	X	
8	CMN_PLLLC_INTMODE_PREG	R/W	1h	This value sets the integer mode value.

Table 11-56. CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	
3-0	CMN_PLLLC_TDCMODE_PREG	R/W	0h	<p>This value sets the TDC mode value.</p> <p>Gain (ps/LSB)</p> <p>0 1</p> <p>1 1.07</p> <p>2 1.14</p> <p>3 1.23</p> <p>4 1.33</p> <p>5 1.45</p> <p>6 1.6</p> <p>7 1.78</p> <p>8 2.0</p> <p>9 2.29</p> <p>10 2.67</p> <p>11 3.2</p> <p>12 4.0</p> <p>13 5.33</p> <p>14 8.0</p> <p>15 16</p>

**Table 11-57. Register Call Summary for
CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_LF_COEFF_MODE1_PREG__CMN_PLLLC_MODE_PREG Register \(Offset = 90h\) \[reset = X\]: \[0\]](#)

11.19 CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG Register (Offset = 94h) [reset = X]

CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG is shown in Figure 11-19 and described in Table 11-59.

Return to [Summary Table](#).

PLLCMNLC loop filter register for mode 0.

Table 11-58.
CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0094h
SERDES_16G1	0501 0094h
SERDES_16G2	0502 0094h
SERDES_16G3	0503 0094h

Figure 11-19. CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_PLLLC_LOCK_CNTSTART_PREG			
R/W-X				R/W-3E8h			
23	22	21	20	19	18	17	16
CMN_PLLLC_LOCK_CNTSTART_PREG							
R/W-3E8h							
15	14	13	12	11	10	9	8
RESERVED	CMN_PLLLC_LF_PROPCOEFF_MODE0_PREG			RESERVED			CMN_PLLLC_LF_PROPFRAC_MODE0_PREG
R/W-X	R/W-3h			R/W-X			R/W-0h
7	6	5	4	3	2	1	0
CMN_PLLLC_LF_PROPFRAC_MODE0_PREG				CMN_PLLLC_LF_INTCOEFF_MODE0_PREG			
R/W-0h				R/W-6h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-59. CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLC_LOCK_CNTSTART_PREG	R/W	3E8h	This value sets the lock counter start value.
15	RESERVED	R/W	X	
14-12	CMN_PLLLC_LF_PROPCOEFF_MODE0_PREG	R/W	3h	This value sets the loop filter proportional coefficient value when cmn_pllcl_mode is deasserted.
11-9	RESERVED	R/W	X	
8-4	CMN_PLLLC_LF_PROPFRAC_MODE0_PREG	R/W	0h	This value sets the loop filter fractional coefficient value when cmn_pllcl_mode is deasserted.
3-0	CMN_PLLLC_LF_INTCOEFF_MODE0_PREG	R/W	6h	This value sets the loop filter integer coefficient value when cmn_pllcl_mode is deasserted.

**Table 11-60. Register Call Summary for
CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_LOCK_CNTSTART_PREG__CMN_PLLLC_LF_COEFF_MODE0_PREG Register \(Offset = 94h\) \[reset = X\]: \[0\]](#)

11.20 CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG Register (Offset = 98h) [reset = X]

CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG is shown in Figure 11-20 and described in Table 11-62.

Return to [Summary Table](#).

PLLCMNLC lock count threshold register.

Table 11-61.
CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0098h
SERDES_16G1	0501 0098h
SERDES_16G2	0502 0098h
SERDES_16G3	0503 0098h

Figure 11-20. CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG Register

31	30	29	28	27	26	25	24
RESERVED			CMN_PLLLC_C LK1_EN_PREG	RESERVED			
R/W-X			R/W-0h	R/W-X			
23	22	21	20	19	18	17	16
RESERVED	CMN_PLLLC_CLK1OUTDIV_PREG						
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				CMN_PLLLC_LOCK_CNTTHRESH_PREG			
R/W-X				R/W-1h			
7	6	5	4	3	2	1	0
CMN_PLLLC_LOCK_CNTTHRESH_PREG							
R/W-1h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-62. CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28	CMN_PLLLC_CLK1_EN_PREG	R/W	0h	This value sets the clock1 enable value.
27-23	RESERVED	R/W	X	
22-16	CMN_PLLLC_CLK1OUTDIV_PREG	R/W	0h	This value sets the clock1 output divider value.
15-12	RESERVED	R/W	X	
11-0	CMN_PLLLC_LOCK_CNTTHRESH_PREG	R/W	1h	PLLCMNLC lock counter threshold value : This value sets the lock count threshold. This is the value used by the PLLCMNLC lock detection logic to determine if the PLL has locked. If the two counters in the PLL lock detection logic differ by less than this value, the PLL is considered locked. Note: this function is deprecated.

**Table 11-63. Register Call Summary for
CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_CLK1_PREG__CMN_PLLLC_LOCK_CNTTHRESH_PREG Register \(Offset = 98h\) \[reset = X\]: \[0\]](#)

11.21 CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG Register (Offset = 9Ch) [reset = X]

CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG is shown in Figure 11-21 and described in Table 11-65.

Return to [Summary Table](#).

PLLCMNLC clock0 register.

Table 11-64.
CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 009Ch
SERDES_16G1	0501 009Ch
SERDES_16G2	0502 009Ch
SERDES_16G3	0503 009Ch

Figure 11-21. CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG Register

31	30	29	28	27	26	25	24
CMN_PLLLC_BWCAL_EN_MODE1_PREG	RESERVED				CMN_PLLLC_BWCAL_THRESH_MODE1_PREG		
R/W-1h	R/W-X				R/W-7h		
23	22	21	20	19	18	17	16
RESERVED			CMN_PLLLC_BWCAL_TMR_MODE1_PREG				
R/W-X			R/W-6h				
15	14	13	12	11	10	9	8
RESERVED			CMN_PLLLC_CLK0_EN_PREG	RESERVED			
R/W-X			R/W-1h	R/W-X			
7	6	5	4	3	2	1	0
RESERVED	CMN_PLLLC_CLK0OUTDIV_PREG						
R/W-X	R/W-1h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-65. CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLLLC_BWCAL_EN_MODE1_PREG	R/W	1h	This value sets the bwcal enable value when cmn_plllic_mode is asserted.
30-28	RESERVED	R/W	X	
27-24	CMN_PLLLC_BWCAL_THRESH_MODE1_PREG	R/W	7h	This value sets the bwcal threshold value when cmn_plllic_mode is asserted.
23-21	RESERVED	R/W	X	
20-16	CMN_PLLLC_BWCAL_TMR_MODE1_PREG	R/W	6h	This value sets the bwcal timer value when cmn_plllic_mode is asserted.
15-13	RESERVED	R/W	X	
12	CMN_PLLLC_CLK0_EN_PREG	R/W	1h	This value sets the clock0 enable value.
11-7	RESERVED	R/W	X	

Table 11-65. CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	CMN_PLLLC_CLK0OUTDIV_PREG	R/W	1h	This value sets the clock0 output divider value.

**Table 11-66. Register Call Summary for
CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_BWCAL_MODE1_PREG__CMN_PLLLC_CLK0_PREG Register \(Offset = 9Ch\) \[reset = X\]: \[0\]](#)

11.22 CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG Register (Offset = A0h) [reset = X]

CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG is shown in Figure 11-22 and described in Table 11-68.

Return to [Summary Table](#).

PLLCMNLC bandwidth cal register for mode 0.

Table 11-67.
CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 00A0h
SERDES_16G1	0501 00A0h
SERDES_16G2	0502 00A0h
SERDES_16G3	0503 00A0h

Figure 11-22. CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG Register

31	30	29	28	27	26	25	24
RESERVED					CMN_PLLLC_DSMCORR_EN_PREG	CMN_PLLLC_DSMCORR_STARTVAL_PREG	
R/W-X					R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
CMN_PLLLC_DSMCORR_STARTVAL_PREG					CMN_PLLLC_DSMCORR_GAIN_PREG		
R/W-0h					R/W-0h		
15	14	13	12	11	10	9	8
CMN_PLLLC_BWCAL_EN_MODE0_PREG	RESERVED			CMN_PLLLC_BWCAL_THRESH_MODE0_PREG			
R/W-1h	R/W-X			R/W-Ah			
7	6	5	4	3	2	1	0
RESERVED			CMN_PLLLC_BWCAL_TMR_MODE0_PREG				
R/W-X			R/W-4h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-68. CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CMN_PLLLC_DSMCORR_EN_PREG	R/W	0h	This value sets the DSM spur correction coefficient enable value.
25-19	CMN_PLLLC_DSMCORR_STARTVAL_PREG	R/W	0h	This value sets the DSM spur correction coefficient startval value.
18-16	CMN_PLLLC_DSMCORR_GAIN_PREG	R/W	0h	This value sets the DSM spur correction coefficient gain value.
15	CMN_PLLLC_BWCAL_EN_MODE0_PREG	R/W	1h	This value sets the bwcal enable value when cmn_plllic_mode is deasserted.
14-12	RESERVED	R/W	X	
11-8	CMN_PLLLC_BWCAL_THRESH_MODE0_PREG	R/W	Ah	This value sets the bwcal threshold value when cmn_plllic_mode is deasserted.
7-5	RESERVED	R/W	X	

Table 11-68. CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CMN_PLLLC_BWCAL_TMR_MODE0_PREG	R/W	4h	This value sets the bwcal timer value when cmn_plllic_mode is deasserted.

**Table 11-69. Register Call Summary for
CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_DSMCORR_PREG__CMN_PLLLC_BWCAL_MODE0_PREG Register \(Offset = A0h\) \[reset = X\]: \[0\]](#)

11.23 CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG Register (Offset = A4h) [reset = X]

CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG is shown in Figure 11-23 and described in Table 11-71.

Return to [Summary Table](#).

PLLCMNLC spread spectrum register.

Table 11-70.

CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00A4h
SERDES_16G1	0501 00A4h
SERDES_16G2	0502 00A4h
SERDES_16G3	0503 00A4h

Figure 11-23. CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_PLLLC_SS_AMP_STEP_SIZE_PREG			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
CMN_PLLLC_SS_AMP_STEP_SIZE_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	CMN_PLLLC_SS_NUM_STEPS_PREG						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
CMN_PLLLC_SS_ENABLE_PREG	RESERVED						
R/W-0h	R/W-X						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-71. CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLC_SS_AMP_STEP_SIZE_PREG	R/W	0h	This value sets the spread spectrum amp step size value.
15	RESERVED	R/W	X	
14-8	CMN_PLLLC_SS_NUM_STEPS_PREG	R/W	0h	This value sets the spread spectrum number of steps value.
7	CMN_PLLLC_SS_ENABLE_PREG	R/W	0h	This value sets the spread spectrum enable value.
6-0	RESERVED	R/W	X	

**Table 11-72. Register Call Summary for
CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG**

16-G SerDes Registers

- 2-L SerDes Registers: [0] [1]
- CMN_PLLLC_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC_SS_PREG Register (Offset = A4h) [reset = X]: [0]

11.24 CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG Register (Offset = A8h) [reset = X]

CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG is shown in Figure 11-24 and described in Table 11-74.

Return to [Summary Table](#).

PLLCMNLC spread spectrum two point register.

Table 11-73.
CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 00A8h
SERDES_16G1	0501 00A8h
SERDES_16G2	0502 00A8h
SERDES_16G3	0503 00A8h

Figure 11-24. CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_PLLLC_LF_PROP_OVR_EN_PREG	CMN_PLLLC_LF_PROP_OVR_VAL_PREG
R/W-X						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CMN_PLLLC_LF_PROP_OVRVAL_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					CMN_PLLLC_SSTWOPT_EN_PREG	CMN_PLLLC_SSTWOPT_STARTVAL_PREG	
R/W-X					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
CMN_PLLLC_SSTWOPT_STARTVAL_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-74. CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25	CMN_PLLLC_LF_PROP_OVREN_PREG	R/W	0h	Drives the lfprop_ovren pin on the PLLCMNLC.
24-16	CMN_PLLLC_LF_PROP_OVRVAL_PREG	R/W	0h	Drives the lfprop_ovrval on the PLLCMNLC.
15-11	RESERVED	R/W	X	
10	CMN_PLLLC_SSTWOPT_EN_PREG	R/W	0h	This value sets the sstwopt_en pin on the PLL.
9-0	CMN_PLLLC_SSTWOPT_STARTVAL_PREG	R/W	0h	This value sets the sstwopt_startval pins on the PLL.

**Table 11-75. Register Call Summary for
CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_LF_PROP_OVR_PREG__CMN_PLLLC_SSTWOPT_PREG Register \(Offset = A8h\) \[reset = X\]: \[0\]](#)

11.25 CMN_PLLLC_DSMCRR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG Register (Offset = ACh) [reset = X]

CMN_PLLLC_DSMCRR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG is shown in Figure 11-25 and described in Table 11-77.

Return to [Summary Table](#).

PLLCMNLC debug and test loop filter integer override register.

Table 11-76.
CMN_PLLLC_DSMCRR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 00ACh
SERDES_16G1	0501 00ACh
SERDES_16G2	0502 00ACh
SERDES_16G3	0503 00ACh

Figure 11-25. CMN_PLLLC_DSMCRR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
CMN_PLLLC_DSMCRR_OVR_PREG	CMN_PLLLC_DSMCRR_OVR_PREG						
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED		CMN_PLLLC_LF_INT_OVR_PREG	CMN_PLLLC_LF_INT_OVR_PREG				
R/W-X		R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
CMN_PLLLC_LF_INT_OVR_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-77. CMN_PLLLC_DSMCRR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	CMN_PLLLC_DSMCRR_OVR_PREG	R/W	0h	Drives the dsmcorr_ovren port on the PLLCMNLC.
22-16	CMN_PLLLC_DSMCRR_OVR_PREG	R/W	0h	Drives the dsmcorr_ovrval port on the PLLCMNLC.
15-14	RESERVED	R/W	X	
13	CMN_PLLLC_LF_INT_OVR_PREG	R/W	0h	Drives the lf_int_ovren pin on the PLLCMNLC.
12-0	CMN_PLLLC_LF_INT_OVR_PREG	R/W	0h	Drives the lf_int_ovrval pin on the PLLCMNLC.

**Table 11-78. Register Call Summary for
CMN_PLLLC_DSMCORR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_DSMCORR_OVR_PREG__CMN_PLLLC_LF_INT_OVR_PREG Register \(Offset = ACh\) \[reset = X\]: \[0\]](#)

11.26 CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG Register (Offset = B0h) [reset = X]

CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG is shown in [Figure 11-26](#) and described in [Table 11-80](#).

Return to [Summary Table](#).

PLLCMNLC debug and test loop Spread Spectrum two point override register.

Table 11-79. CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00B0h
SERDES_16G1	0501 00B0h
SERDES_16G2	0502 00B0h
SERDES_16G3	0503 00B0h

Figure 11-26. CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG Register

31	30	29	28	27	26	25	24
RESERVED	CMN_PLLLC_DCOCAL_OVR_PREG	CMN_PLLLC_DCOCAL_OVR_PREG					
R/W-X	R/W-0h	R/W-0h					
23	22	21	20	19	18	17	16
RESERVED	CMN_PLLLC_DCO_ITRIM_PREG				CMN_PLLLC_ROFFSET_PREG		
R/W-X	R/W-3h				R/W-3h		
15	14	13	12	11	10	9	8
RESERVED					CMN_PLLLC_SSTWOPT_OVR_PREG	CMN_PLLLC_SSTWOPT_OVR_PREG	
R/W-X					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
CMN_PLLLC_SSTWOPT_OVR_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-80. CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	CMN_PLLLC_DCOCAL_OVR_PREG	R/W	0h	When asserted the cmnda_plllc_dcocal_ovren which drives the dcocal_ovren port on the PLLCMNLC is forced high. In addition the cmn_plllc_dcocal_ovrval_preg is forced onto cmnda_plllc_dcocal_ovrval which drives the dcocal_ovrval port on the PLLCMNLC.
29-24	CMN_PLLLC_DCOCAL_OVR_PREG	R/W	0h	When cmnda_plllc_dcocal_ovren is asserted, this value is driven onto cmnda_plllc_dcocal_ovrval which drives the dcocal_ovrval port on the PLLCMNLC.
23-22	RESERVED	R/W	X	
21-19	CMN_PLLLC_DCO_ITRIM_PREG	R/W	3h	Drives the DCO trim current on the PLLCMNLC.
18-16	CMN_PLLLC_ROFFSET_PREG	R/W	3h	DCO tank offset resistor trim.

Table 11-80. CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	RESERVED	R/W	X	
10	CMN_PLLLC_SSTWOPT_OVREN_PREG	R/W	0h	Drives the sstwopt_ovren port on the PLLCMNLC.
9-0	CMN_PLLLC_SSTWOPT_OVRVAL_PREG	R/W	0h	Drives the sstwopt_ovrval port on the PLLCMNLC.

Table 11-81. Register Call Summary for CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_DCO_PREG__CMN_PLLLC_SSTWOPT_OVR_PREG Register \(Offset = B0h\) \[reset = X\]: \[0\]](#)

11.27 CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG Register (Offset = B4h) [reset = X]

CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG is shown in Figure 11-27 and described in Table 11-83.

Return to [Summary Table](#).

PLLCMNLC debug and test avdd register.

Table 11-82. CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00B4h
SERDES_16G1	0501 00B4h
SERDES_16G2	0502 00B4h
SERDES_16G3	0503 00B4h

Figure 11-27. CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG Register

31	30	29	28	27	26	25	24
RESERVED		CMN_PLLLCSM_STATE					
R/W-X		R-B00h					
23	22	21	20	19	18	17	16
CMN_PLLLCSM_STATE							
R-B00h							
15	14	13	12	11	10	9	8
RESERVED				CMN_PLLLC_LFAVDDREG_VTRIM_PREG		CMN_PLLLC_HFAVDDREG_VTRIM_PREG	
R/W-X				R/W-3h		R/W-3h	
7	6	5	4	3	2	1	0
CMN_PLLLC_HFAVDDREG_VTRIM_PREG		CMN_PLLLC_CLK1AVDDREG_VTRIM_PREG			CMN_PLLLC_CLK0AVDDREG_VTRIM_PREG		
R/W-3h		R/W-3h			R/W-3h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-83. CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	CMN_PLLLCSM_STATE	R	B00h	State machine state register.
15-12	RESERVED	R/W	X	
11-9	CMN_PLLLC_LFAVDDREG_VTRIM_PREG	R/W	3h	Drives the lfavddreg_vtrim port on the PLLCMNLC. Voltage 0 0.830 1 0.860 2 0.870 3 0.890 4 0.908 5 0.925 6 0.940 7 0.950

**Table 11-83. CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
8-6	CMN_PLLLC_HFAVDDREG_VTRIM_PREG	R/W	3h	Drives the hfavddreg_vtrim port on the PLLCMNLC. Voltage 0 0.830 1 0.860 2 0.870 3 0.890 4 0.908 5 0.925 6 0.940 7 0.950
5-3	CMN_PLLLC_CLK1AVDDREG_VTRIM_PREG	R/W	3h	Drives the clk1avddreg_vtrim port on the PLLCMNLC. Voltage 0 0.830 1 0.860 2 0.870 3 0.890 4 0.908 5 0.925 6 0.940 7 0.950
2-0	CMN_PLLLC_CLK0AVDDREG_VTRIM_PREG	R/W	3h	Drives the clk0avddreg_vtrim port on the PLLCMNLC. Voltage 0 0.830 1 0.860 2 0.870 3 0.890 4 0.908 5 0.925 6 0.940 7 0.950

Table 11-84. Register Call Summary for CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLCSM_STATUS_PREG__CMN_PLLLC_AVDD_PREG Register \(Offset = B4h\) \[reset = X\]: \[0\]](#)

11.28 CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG Register (Offset = B8h) [reset = X]

CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG is shown in Figure 11-28 and described in Table 11-86.

Return to [Summary Table](#).

PLLCMNLC Control State Machine Control register.

Table 11-85.
CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 00B8h
SERDES_16G1	0501 00B8h
SERDES_16G2	0502 00B8h
SERDES_16G3	0503 00B8h

Figure 11-28. CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_PLLLCSM_PLEN_TMR_VAL_PREG			
R/W-X				R/W-32h			
23	22	21	20	19	18	17	16
CMN_PLLLCSM_PLEN_TMR_VAL_PREG							
R/W-32h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			CMN_PLLLCSM_FORCE_CAL_DONE_PREG	RESERVED			CMN_PLLLCSM_SKIP_PLL_CAL_RECAL_PREG
R/W-X			R/W-0h	R/W-X			R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-86. CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLCSM_PLEN_TMR_VAL_PREG	R/W	32h	PLL enable state timer value : used for the timer when the PLL control state machine is in the PLL phase 1 enable state. The value must be 1 or greater. This timer delay is specified in cmn_refclk periods.
15-5	RESERVED	R/W	X	
4	CMN_PLLLCSM_FORCE_CAL_DONE_PREG	R/W	0h	Asserting this bit immediately advances the State Machine from the PLLSM_CAL state currently in or once entered.
3-1	RESERVED	R/W	X	

Table 11-86. CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMN_PLLLCSM_SKIP_P LL_CAL_RECAL_PREG	R/W	1h	Skip PLL calibration re-calibration enable : When this bit is active (1'b1), the PLL calibration state will be skipped if it was previously run, unless the cmn_pll1c1_en has been deasserted, or the Macro reset.

**Table 11-87. Register Call Summary for
CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLCSM_PLEN_TMR_PREG__CMN_PLLLCSM_CTRL_PREG Register \(Offset = B8h\) \[reset = X\]: \[0\]](#)

11.29 CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG Register (Offset = BCh) [reset = X]

CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG is shown in Figure 11-29 and described in Table 11-89.

Return to [Summary Table](#).

PLLCMNLC Control State Machine PLL pre-charge timer register.

Table 11-88.
CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00BCh
SERDES_16G1	0501 00BCh
SERDES_16G2	0502 00BCh
SERDES_16G3	0503 00BCh

Figure 11-29. CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CMN_PLLLCSM_PLLVREF_TMR_VAL_PREG											
R/W-X				R/W-5h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CMN_PLLLCSM_PLLPRE_TMR_VAL_PREG											
R/W-X				R/W-7Dh											

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-89. CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLCSM_PLLVREF_TMR_VAL_PREG	R/W	5h	PLL pre-charge state timer value : used for the timer when the PLL control state machine is in the PLL vref state which includes releasing the PLLCMNLC reset. The value must be 1 or greater. This timer delay is specified in cmn_refclk periods.
15-12	RESERVED	R/W	X	
11-0	CMN_PLLLCSM_PLLPRE_TMR_VAL_PREG	R/W	7Dh	PLL pre-charge state timer value : used for the timer when the PLL control state machine is in the PLL phase 2 enable state. The value must be 1 or greater. This timer delay is specified in cmn_refclk periods.

**Table 11-90. Register Call Summary for
CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLCSM_PLLVREF_TMR_PREG__CMN_PLLLCSM_PLLPRE_TMR_PREG Register \(Offset = BCh\) \[reset = X\]: \[0\]](#)

11.30 CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG Register (Offset = C0h) [reset = X]

CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG is shown in Figure 11-30 and described in Table 11-92.

Return to [Summary Table](#).

PLLCMNLC clock2 register.

Table 11-91. CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00C0h
SERDES_16G1	0501 00C0h
SERDES_16G2	0502 00C0h
SERDES_16G3	0503 00C0h

Figure 11-30. CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
CMN_PLLLC_STATUS_C_BWCAL_CODE							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			CMN_PLLLC_C LK2_EN_PREG	CMN_PLLLC_CLK2OUTDIVFRAC_PREG			
R/W-X			R/W-0h		R/W-4h		
7	6	5	4	3	2	1	0
RESERVED	CMN_PLLLC_CLK2OUTDIVINT_PREG						
R/W-X				R/W-4h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-92. CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	CMN_PLLLC_STATUS_C_BWCAL_CODE	R	0h	PLLCMNLC Band Width calibration code result: Contains the calibration result. 7:5 If_propcoef[2:0] calibration results 4:0 If_propfrac[4:0] calibration results Note the contents of this register are not valid until cmn_pll_locked Macro output is asserted. Note this register is for diagnostic purposes only.
15-13	RESERVED	R/W	X	
12	CMN_PLLLC_CLK2_EN_PREG	R/W	0h	This value sets the clock2 enable value.

**Table 11-92. CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
11-8	CMN_PLLLC_CLK2OUTDIVFRAC_PREG	R/W	4h	This value sets the clock2 fractional output divider's fraction value: 4'b0000 0 4'b0001 1/2 4'b0010 1/3 4'b0011 2/3 4'b0100 1/4 4'b0101 1/2 4'b0110 reserved 4'b0111 3/4 4'b1000 1/5 4'b1001 reserved 4'b1010 2/5 4'b1011 3/5 4'b1100 reserved 4'b1101 3/5 4'b1110 reserved 4'b1111 4/5
7	RESERVED	R/W	X	
6-0	CMN_PLLLC_CLK2OUTDIVINT_PREG	R/W	4h	This value sets the clock2 fractional output divider's integer value. The overall frequency is determined as: $F_{clk\ 2} = F_{vco} / (cmn_plllc_clk2outdivint_preg + 4 + \text{fraction value})$ where the fractional value is defined above in the description for <code>cmn_plllc_clk2outdivfrac_preg</code> .

Table 11-93. Register Call Summary for CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_STATUS_C_PREG__CMN_PLLLC_CLK2_PREG Register \(Offset = C0h\) \[reset = X\]: \[0\]](#)

11.31 CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG Register (Offset = C4h) [reset = X]

CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG is shown in Figure 11-31 and described in Table 11-95.

Return to [Summary Table](#).

PLLCMNLC spread spectrum Time Step Size Mode register.

Table 11-94.
CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00C4h
SERDES_16G1	0501 00C4h
SERDES_16G2	0502 00C4h
SERDES_16G3	0503 00C4h

Figure 11-31.
CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG Register

31	30	29	28	27	26	25	24
RESERVED							CMN_PLLLC_L OCK_DELAY_P REG
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
CMN_PLLLC_LOCK_DELAY_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	CMN_PLLLC_SS_TIME_STEP_SIZE_MODE1_PREG						
R/W-X	R/W-8h						
7	6	5	4	3	2	1	0
RESERVED	CMN_PLLLC_SS_TIME_STEP_SIZE_MODE0_PREG						
R/W-X	R/W-8h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-95.
CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	CMN_PLLLC_LOCK_DELAY_PREG	R/W	0h	This value sets a delay from internal lock assertion to assertion of cmn_pll_locked. delay = cmn_pll_locked_delay_preg * 256 pfdclk periods.
15	RESERVED	R/W	X	
14-8	CMN_PLLLC_SS_TIME_STEP_SIZE_MODE1_PREG	R/W	8h	This value sets the spread spectrum time step size value when cmn_pll_mode is asserted.
7	RESERVED	R/W	X	

Table 11-95.
CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG Register
Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	CMN_PLLLC_SS_TIME_STEP_SIZE_MODE0_PREG	R/W	8h	This value sets the spread spectrum time step size value when cmn_plllc_mode is deasserted.

Table 11-96. Register Call Summary for
CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC_LOCK_DELAY_CTRL_PREG__CMN_PLLLC_SS_TIME_STEPSIZE_MODE_PREG Register \(Offset = C4h\) \[reset = X\]: \[0\]](#)

11.32 SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG Register (Offset = D0h) [reset = X]

SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG is shown in Figure 11-32 and described in Table 11-98.

Return to [Summary Table](#).

Signal detection oscillator override register

Table 11-97. SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00D0h
SERDES_16G1	0501 00D0h
SERDES_16G2	0502 00D0h
SERDES_16G3	0503 00D0h

Figure 11-32. SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG Register

31	30	29	28	27	26	25	24
SDOSCCAL_RUN_PREG	SDOSCCAL_INITSTEP_PREG			RESERVED			
R/W-0h	R/W-0h			R/W-X			
23	22	21	20	19	18	17	16
RESERVED	SDOSCCAL_DONE	SDOSCCAL_CODE					
R/W-X	R-0h	R-2Ch					
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			CMN_SDOSC_EN_OVRD_EN_PREG	RESERVED			CMN_SDOSC_EN_OVRD_VAL_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-98. SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDOSCCAL_RUN_PREG	R/W	0h	Signal detection oscillator calibration manual initiation active high enable.
30-28	SDOSCCAL_INITSTEP_PREG	R/W	0h	Signal detection oscillator calibration initial step size. 3'b 000 : 1 step 3'b 001 : 2 step 3'b 010 : 4 step 3'b 011 : 8 step 3'b 100 : 16 step 3'b 101 - 3'b 111: reserved
27-23	RESERVED	R/W	X	
22	SDOSCCAL_DONE	R	0h	Signal detection oscillator calibration active high complete flag.
21-16	SDOSCCAL_CODE	R	2Ch	Signal detection oscillator calibration result. Note only valid once cmn_ready has asserted or if re-running manually though the sdosccal_run_preg, once the sdosccal_done has asserted.
15-5	RESERVED	R/W	X	

**Table 11-98. SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	CMN_SDOSC_EN_OVRD_EN_PREG	R/W	0h	Active high override enable for the signal detection oscillator circuit enable.
3-1	RESERVED	R/W	X	
0	CMN_SDOSC_EN_OVRD_VAL_PREG	R/W	0h	When cmn_sdosc_en_ovrd_en_preg is asserted, this value drives the cmnda_sdosc_en circuit enable.

Table 11-99. Register Call Summary for SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDOSCCAL_CTRL_PREG__CMN_SDOSC_OVRD_PREG Register \(Offset = D0h\) \[reset = X\]: \[0\]](#)

11.33 SDOSCCAL_INIT_TMR_PREG__SDOSCCAL_OVR_PREG Register (Offset = D4h) [reset = X]

SDOSCCAL_INIT_TMR_PREG__SDOSCCAL_OVR_PREG is shown in Figure 11-33 and described in Table 11-101.

Return to [Summary Table](#).

Signal detection oscillator calibration override register

Table 11-100. SDOSCCAL_INIT_TMR_PREG__SDOSCCAL_OVR_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00D4h
SERDES_16G1	0501 00D4h
SERDES_16G2	0502 00D4h
SERDES_16G3	0503 00D4h

Figure 11-33. SDOSCCAL_INIT_TMR_PREG__SDOSCCAL_OVR_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
SDOSCCAL_INITTMR_PREG							
R/W-2h							
15	14	13	12	11	10	9	8
SDOSCCAL_OVREN_PREG	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED		SDOSCCAL_OVRVAL_PREG					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-101. SDOSCCAL_INIT_TMR_PREG__SDOSCCAL_OVR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	SDOSCCAL_INITTMR_PREG	R/W	2h	Signal detection calibration initial wait timer to allow the analog circuits to settle on initiation of the calibration sequence. Note this value is in cmn_refclk_gated clock periods.
15	SDOSCCAL_OVREN_PREG	R/W	0h	Signal detection oscillator override active high enable.
14-6	RESERVED	R/W	X	
5-0	SDOSCCAL_OVRVAL_PREG	R/W	0h	When sdosccal_ovren_pregis asserted high, this value is used by the Signal detection oscillator rather than the calibration engine result.

Table 11-102. Register Call Summary for SDOSCCAL_INIT_TMR_PREG__SDOSCCAL_OVR_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDOSCCAL_INIT_TMR_PREG__SDOSCCAL_OVR_PREG Register \(Offset = D4h\) \[reset = X\]: \[0\]](#)

11.34 SDOSCCAL_TMR_PREG__SDOSCCAL_ITER_TMR_PREG Register (Offset = D8h) [reset = X]

SDOSCCAL_TMR_PREG__SDOSCCAL_ITER_TMR_PREG is shown in Figure 11-34 and described in Table 11-104.

Return to [Summary Table](#).

Signal detection oscillator calibration iteration timer register

Table 11-103. SDOSCCAL_TMR_PREG__SDOSCCAL_ITER_TMR_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00D8h
SERDES_16G1	0501 00D8h
SERDES_16G2	0502 00D8h
SERDES_16G3	0503 00D8h

Figure 11-34. SDOSCCAL_TMR_PREG__SDOSCCAL_ITER_TMR_PREG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						SDOSCCAL_TMRVAL_PREG									
R/W-X						R/W-Eh									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SDOSCCAL_ITER_TMR_PREG							
R/W-X								R/W-2h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-104. SDOSCCAL_TMR_PREG__SDOSCCAL_ITER_TMR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	SDOSCCAL_TMRVAL_P REG	R/W	Eh	This value sets the Signal detection oscillator frequency evaluation time. Note this value is in cmn_refclk_gated clock periods.
15-8	RESERVED	R/W	X	
7-0	SDOSCCAL_ITER_TMR_P REG	R/W	2h	Signal detection calibration wait timer to allow the analog circuits to settle to the new frequency after a calibration code change. Note this value is in cmn_refclk_gated clock periods.

Table 11-105. Register Call Summary for SDOSCCAL_TMR_PREG__SDOSCCAL_ITER_TMR_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDOSCCAL_TMR_PREG__SDOSCCAL_ITER_TMR_PREG Register \(Offset = D8h\) \[reset = X\]: \[0\]](#)

11.35 SDOSCCAL_START_PREG__SDOSCCAL_CLK_CNT_PREG Register (Offset = DCh) [reset = X]

SDOSCCAL_START_PREG__SDOSCCAL_CLK_CNT_PREG is shown in Figure 11-35 and described in Table 11-107.

Return to [Summary Table](#).

Signal detection oscillator calibration oscillator clock count target register

Table 11-106. SDOSCCAL_START_PREG__SDOSCCAL_CLK_CNT_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00DCh
SERDES_16G1	0501 00DCh
SERDES_16G2	0502 00DCh
SERDES_16G3	0503 00DCh

Figure 11-35. SDOSCCAL_START_PREG__SDOSCCAL_CLK_CNT_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		SDOSCCAL_STARTVAL_PREG					
R/W-X		R/W-2Ch					
15	14	13	12	11	10	9	8
RESERVED						SDOSCCAL_CLKCNT_PREG	
R/W-X						R/W-12Ch	
7	6	5	4	3	2	1	0
SDOSCCAL_CLKCNT_PREG							
R/W-12Ch							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-107. SDOSCCAL_START_PREG__SDOSCCAL_CLK_CNT_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	SDOSCCAL_STARTVAL_PREG	R/W	2Ch	This value sets the Signal detection oscillator calibration starting code. Note: This must be set to a value that is always at least one step size away from the minimum and maximum calibration codes. For example, if the initial step size is 4 (sdosccal_initstep_preg = 3'b010), this value must be at least 6'h04 and less than 6'h3B.
15-10	RESERVED	R/W	X	
9-0	SDOSCCAL_CLKCNT_PREG	R/W	12Ch	This value sets the Signal detection oscillator expected clock count target.

Table 11-108. Register Call Summary for SDOSCCAL_START_PREG__SDOSCCAL_CLK_CNT_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDOSCCAL_START_PREG__SDOSCCAL_CLK_CNT_PREG Register \(Offset = DCh\) \[reset = X\]: \[0\]](#)

11.36 PROCMON_STATUS_PREG__PROCMON_CTRL_PREG Register (Offset = E0h) [reset = X]

PROCMON_STATUS_PREG__PROCMON_CTRL_PREG is shown in Figure 11-36 and described in Table 11-110.

Return to [Summary Table](#).

Process Monitor control register.

Table 11-109. PROCMON_STATUS_PREG__PROCMON_CTRL_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00E0h
SERDES_16G1	0501 00E0h
SERDES_16G2	0502 00E0h
SERDES_16G3	0503 00E0h

Figure 11-36. PROCMON_STATUS_PREG__PROCMON_CTRL_PREG Register

31	30	29	28	27	26	25	24
PROCMON_D ONE	RESERVED	PROCMON_CN T_OVERNOM	PROCMON_CNT_VAL				
R-0h	R/W-X	R-0h	R-0h				
23	22	21	20	19	18	17	16
PROCMON_CNT_VAL							
R-0h							
15	14	13	12	11	10	9	8
PROCMON_RU N_PREG	PROCMON_ROSEL_PREG		PROCMON_ROCNT_PREG				
R/W-0h	R/W-0h		R/W-BB8h				
7	6	5	4	3	2	1	0
PROCMON_ROCNT_PREG							
R/W-BB8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-110. PROCMON_STATUS_PREG__PROCMON_CTRL_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PROCMON_DONE	R	0h	Active high process monitor ring oscillator count complete flag.
30	RESERVED	R/W	X	
29	PROCMON_CNT_OVER NOM	R	0h	When asserted this bit indicates the process monitor ring oscillator counter reached the value expected for a nominal PVT part, as established by procmon_rocnt_preg. Valid once procmon_done asserts until procmon_run_preg is deasserted.
28-16	PROCMON_CNT_VAL	R	0h	Process monitor ring oscillator counter value. procmon_cnt_val indicates the number of clocks in excess of the procmon_rocnt_preg expected value when procmon_cnt_overnom is asserted. procmon_cnt_val indicates the number of clocks short of the procmon_rocnt_preg expected value when procmon_cnt_overnom is deasserted. Valid once procmon_done asserts until procmon_run_preg is deasserted.

**Table 11-110. PROCMON_STATUS_PREG__PROCMON_CTRL_PREG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15	PROCMON_RUN_PREG	R/W	0h	Active high process monitor counter start. Once this signal is asserted, it should remain asserted until procmon_done asserts. It should not be reasserted until procmon_done deasserts.
14-13	PROCMON_ROSEL_PREG	R/W	0h	Process monitor ring oscillator select: Selects the ring oscillator to enable and count. 2'b 00 : SVT ring oscillator 2'b 01 : LVT ring oscillator 2'b 10 : ULVT ring oscillator 2'b 11 : thick oxide ring oscillator Note this may be set during the same write that asserts procmon_run_preg.
12-0	PROCMON_ROCNT_PREG	R/W	BB8h	Expected oscillator clocks counted for nominal process at typical conditions: Selected ring oscillator 13'h0AD6 SVT 13'h0D39 LVT 13'h1111 ULVT 13'h10B2 thick oxide Note this may be set during the same write that asserts procmon_run_preg.

Table 11-111. Register Call Summary for PROCMON_STATUS_PREG__PROCMON_CTRL_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PROCMON_STATUS_PREG__PROCMON_CTRL_PREG Register \(Offset = E0h\) \[reset = X\]: \[0\]](#)

11.37 PROCMON_CNTWAIT_PREG__PROCMON_INITWAIT_PREG Register (Offset = E4h) [reset = X]

PROCMON_CNTWAIT_PREG__PROCMON_INITWAIT_PREG is shown in Figure 11-37 and described in Table 11-113.

Return to [Summary Table](#).

Process Monitor initial wait timer register.

Table 11-112. PROCMON_CNTWAIT_PREG__PROCMON_INITWAIT_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00E4h
SERDES_16G1	0501 00E4h
SERDES_16G2	0502 00E4h
SERDES_16G3	0503 00E4h

Figure 11-37. PROCMON_CNTWAIT_PREG__PROCMON_INITWAIT_PREG Register

31	30	29	28	27	26	25	24
RESERVED				PROCMON_CNTWAIT_TMRVAL_PREG			
R/W-X				R/W-F9h			
23	22	21	20	19	18	17	16
PROCMON_CNTWAIT_TMRVAL_PREG							
R/W-F9h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					PROCMON_INITWAIT_TMRVAL_PREG		
R/W-X					R/W-3h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-113. PROCMON_CNTWAIT_PREG__PROCMON_INITWAIT_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-16	PROCMON_CNTWAIT_TMRVAL_PREG	R/W	F9h	Time to count the selected ring oscillator clocks. The time to count is: procmon_cntwait_tmrval_preg + 1 cmn_refclk_gated clock periods.
15-3	RESERVED	R/W	X	
2-0	PROCMON_INITWAIT_TMRVAL_PREG	R/W	3h	Nominal number of cmn_refclk_gated clock periods to wait while the analog circuit powers up and the enabled ring oscillator settles.

Table 11-114. Register Call Summary for PROCMON_CNTWAIT_PREG__PROCMON_INITWAIT_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PROCMON_CNTWAIT_PREG__PROCMON_INITWAIT_PREG Register \(Offset = E4h\) \[reset = X\]: \[0\]](#)

11.38 PROCMON_DIAGNOSTIC_PREG__PROCMON_OVRD_PREG Register (Offset = E8h) [reset = X]

PROCMON_DIAGNOSTIC_PREG__PROCMON_OVRD_PREG is shown in Figure 11-38 and described in Table 11-116.

Return to [Summary Table](#).

Process monitor override register.

Table 11-115. PROCMON_DIAGNOSTIC_PREG__PROCMON_OVRD_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 00E8h
SERDES_16G1	0501 00E8h
SERDES_16G2	0502 00E8h
SERDES_16G3	0503 00E8h

Figure 11-38. PROCMON_DIAGNOSTIC_PREG__PROCMON_OVRD_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PROCMON_FSM_STATE					
R/W-X		R-0h					
15	14	13	12	11	10	9	8
RESERVED							PROCMON_OVRD_EN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		PROCMON_OVRD_ISOAVDD_EN_PREG	PROCMON_OVRD_ISOAVDD_FWEN_N_PREG	PROCMON_OVRD_LVT_EN_PREG	PROCMON_OVRD_SVT_EN_PREG	PROCMON_OVRD_THICKOX_EN_PREG	PROCMON_OVRD_ULVT_EN_PREG
R/W-X		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-116. PROCMON_DIAGNOSTIC_PREG__PROCMON_OVRD_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PROCMON_FSM_STATE	R	0h	Process monitor state machine state vector.
15-9	RESERVED	R/W	X	
8	PROCMON_OVRD_EN_PREG	R/W	0h	Active high analog control override enable.
7-6	RESERVED	R/W	X	
5	PROCMON_OVRD_ISOAVDD_EN_PREG	R/W	0h	When procmon_ovrd_en_preg is asserted, this value overrides the analog circuit's power gate enable, cmnda_pmc_isoavdd_en.
4	PROCMON_OVRD_ISOAVDD_FWEN_N_PREG	R/W	0h	When procmon_ovrd_en_preg is asserted, this value overrides the power gate isolation control, cmnda_pmc_isoavdd_fwen_n.
3	PROCMON_OVRD_LVT_EN_PREG	R/W	0h	When procmon_ovrd_en_preg is asserted, this value overrides the analog circuit's LVT ring oscillator enable, cmnda_pmc_lvt_en.
2	PROCMON_OVRD_SVT_EN_PREG	R/W	0h	When procmon_ovrd_en_preg is asserted, this value overrides the analog circuit's SVT ring oscillator enable, cmnda_pmc_svt_en.

**Table 11-116. PROCMON_DIAGNOSTIC_PREG__PROCMON_OVRD_PREG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
1	PROCMON_OVRD_THICKOX_EN_PREG	R/W	0h	When procmon_ovrd_en_preg is asserted, this value overrides the analog circuit's thick oxide ring oscillator enable, cmnda_pmc_thickox_en.
0	PROCMON_OVRD_ULVT_EN_PREG	R/W	0h	When procmon_ovrd_en_preg is asserted, this value overrides the analog circuit's ULVT ring oscillator enable, cmnda_pmc_ulvt_en.

Table 11-117. Register Call Summary for PROCMON_DIAGNOSTIC_PREG__PROCMON_OVRD_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PROCMON_DIAGNOSTIC_PREG__PROCMON_OVRD_PREG Register \(Offset = E8h\) \[reset = X\]: \[0\]](#)

11.39 CMN_CTRL_DIAG_RESET_PREG__CDB_DIAG_PREG Register (Offset = 100h) [reset = X]

CMN_CTRL_DIAG_RESET_PREG__CDB_DIAG_PREG is shown in Figure 11-39 and described in Table 11-119.

Return to [Summary Table](#).

CDB diagnostic register.

Table 11-118. CMN_CTRL_DIAG_RESET_PREG__CDB_DIAG_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0100h
SERDES_16G1	0501 0100h
SERDES_16G2	0502 0100h
SERDES_16G3	0503 0100h

Figure 11-39. CMN_CTRL_DIAG_RESET_PREG__CDB_DIAG_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED				CMN_RESET_SYNC_N	CMNDA_RSTREL_RST_N	CMNDA_PLLLC1_RST_N	CMNDA_PLLLC_RST_N
R-X				R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							CDB_PSLVERR_REG
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-119. CMN_CTRL_DIAG_RESET_PREG__CDB_DIAG_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19	CMN_RESET_SYNC_N	R	0h	Current state of the cmn_reset_sync_n reset.
18	CMNDA_RSTREL_RST_N	R	0h	Current state of the cmnda_rstrel_rst_n reset.
17	CMNDA_PLLLC1_RST_N	R	0h	Current state of the cmnda_plllc1_rst_n reset.
16	CMNDA_PLLLC_RST_N	R	0h	Current state of the cmnda_plllc_rst_n reset.
15-1	RESERVED	R	X	
0	CDB_PSLVERR_REG	R	0h	CDB bus error : Asserted when internal CDB watchdog timer expires. Note: This bit is cleared on read of this register address.

Table 11-120. Register Call Summary for CMN_CTRL_DIAG_RESET_PREG__CDB_DIAG_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_CTRL_DIAG_RESET_PREG__CDB_DIAG_PREG Register \(Offset = 100h\) \[reset = X\]: \[0\]](#)

11.40 CMN_FUNC_DIAG_RESET_PREG Register (Offset = 104h) [reset = X]

CMN_FUNC_DIAG_RESET_PREG is shown in [Figure 11-40](#) and described in [Table 11-122](#).

Return to [Summary Table](#).

Common functions submodule reset diagnostic register.

Table 11-121. CMN_FUNC_DIAG_RESET_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0104h
SERDES_16G1	0501 0104h
SERDES_16G2	0502 0104h
SERDES_16G3	0503 0104h

Figure 11-40. CMN_FUNC_DIAG_RESET_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
CMN_ATBDIG_RST_N	CMN_RESCAL_RST_N	PROCMON_RST_N	SDOSCCAL_RST_N	SDOSCCAL_CNTRST_N	CMN_HSRSM_RST_N	PROCMON_PMC_RST_N	SCANOVDR_ATBADC_RST_N
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-122. CMN_FUNC_DIAG_RESET_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7	CMN_ATBDIG_RST_N	R	0h	Current state of the cmn_atbdig_rst_n reset.
6	CMN_RESCAL_RST_N	R	0h	Current state of the cmn_rescal_rst_n reset.
5	PROCMON_RST_N	R	0h	Current state of the procmon_rst_n reset.
4	SDOSCCAL_RST_N	R	0h	Current state of the sdosccal_rst_n reset.
3	SDOSCCAL_CNTRST_N	R	0h	Current state of the sdosccal_cntrst_n reset.
2	CMN_HSRSM_RST_N	R	0h	Current state of the cmn_hsrsm_rst_n reset.
1	PROCMON_PMC_RST_N	R	0h	Current state of the procmon_pmc_rst_n reset.
0	SCANOVDR_ATBADC_RST_N	R	0h	Current state of the scanovdr_atbadc_rst_n reset.

Table 11-123. Register Call Summary for CMN_FUNC_DIAG_RESET_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_FUNC_DIAG_RESET_PREG Register \(Offset = 104h\) \[reset = X\]: \[0\]](#)

11.41 CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG Register (Offset = 108h) [reset = X]

CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG is shown in Figure 11-41 and described in Table 11-125.

Return to [Summary Table](#).

Common clock frequency measurement control register.

Table 11-124.
CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0108h
SERDES_16G1	0501 0108h
SERDES_16G2	0502 0108h
SERDES_16G3	0503 0108h

Figure 11-41. CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_CMSMT_REF_CLK_TMR_VALUE_PREG			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
CMN_CMSMT_REF_CLK_TMR_VALUE_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				CMN_TEST_CLK_SEL_PREG		CMN_CMSMT_MEASUREMENT_RUN_PREG	
R/W-X				R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-125. CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_CMSMT_REF_CLK_TMR_VALUE_PREG	R/W	0h	Reference clock timer value : This specifies the amount of time, in cmn_refclk periods, to count test clock cycles. This value minus 1 is loaded into the reference clock timer. A value of 0 for this field is not valid when running this function.
15-4	RESERVED	R/W	X	

**Table 11-125. CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG
Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3-1	CMN_TEST_CLK_SEL_PREG	R/W	0h	Test clock selection: cmn_test_clk_sel_preg Test Clock 3'b000 cmnda_refrcv_refclk 3'b001 cmnda_refrcv1_refclk 3'b010 cmnda_pll1c_digclk0 3'b011 cmnda_pll1c_digclk1 3'b100 cmnda_pll1c_digclk2 3'b101 cmnda_pll1c1_digclk1 3'b110 cmnda_pll1c1_digclk2 3'b111 cmnda_sdosc_clk
0	CMN_CMSMT_MEASUREMENT_RUN_PREG	R/W	0h	Test clock measurement active high enable: Asserting this bit will run the test clock measurement process. This bit must remain active until the test clock measurement process is complete, as indicated by the test cmn_cmsmt_measurement_done_preg. To start another measurement process, this bit must first be deasserted then re-asserted. Note: Both of the clocks used to generate the ref_clk and test_clk clocks must be active prior to setting or clearing this bit. Note: The values in the Test clock selection register and Reference clock timer value register must be set prior to activating this bit.

**Table 11-126. Register Call Summary for
CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_CMSMT_REF_CLK_TMR_VALUE_PREG__CMN_CLK_FREQ_MSMT_CTRL_PREG Register \(Offset = 108h\) \[reset = X\]: \[0\]](#)

11.42 CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG Register (Offset = 10Ch) [reset = X]

CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG is shown in Figure 11-42 and described in Table 11-128.

Return to [Summary Table](#).

Common clock frequency measurement result register.

Table 11-127.
CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALU
E_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 010Ch
SERDES_16G1	0501 010Ch
SERDES_16G2	0502 010Ch
SERDES_16G3	0503 010Ch

Figure 11-42. CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							CMN_CMSMT_MEASUREMENT_DONE
R-X							R-0h
15	14	13	12	11	10	9	8
RESERVED				CMN_CMSMT_TEST_CLK_CNT_VALUE			
R-X				R-0h			
7	6	5	4	3	2	1	0
CMN_CMSMT_TEST_CLK_CNT_VALUE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 11-128. CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16	CMN_CMSMT_MEASUREMENT_DONE	R	0h	Test clock measurement done: This bit will be asserted when the test clock measurement process is complete. It will be cleared by the deactivation cmn_cmsmt_measurement_run_preg.
15-12	RESERVED	R	X	

**Table 11-128. CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG
Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
11-0	CMN_CMSMT_TEST_CLK_CNT_VALUE	R	0h	Test clock counter value: When the test clock measurement process is complete, the value in this field specifies the number of test clock cycles that were counted in the time specified by the reference clock timer value. This field is only valid while the cmn_cmsmt_measurement_done_pregbit is asserted.

**Table 11-129. Register Call Summary for
CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_CLK_FREQ_MSMT_OBS_PREG__CMN_CMSMT_TEST_CLK_CNT_VALUE_PREG Register \(Offset = 10Ch\) \[reset = X\]: \[0\]](#)

11.43 CMN_SPARE_REG_PREG Register (Offset = 110h) [reset = X]

CMN_SPARE_REG_PREG is shown in [Figure 11-43](#) and described in [Table 11-131](#).

[Return to Summary Table.](#)

Common spare registers to analog.

Table 11-130. CMN_SPARE_REG_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0110h
SERDES_16G1	0501 0110h
SERDES_16G2	0502 0110h
SERDES_16G3	0503 0110h

Figure 11-43. CMN_SPARE_REG_PREG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SPARE_PREG															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-131. CMN_SPARE_REG_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	SPARE_PREG	R/W	0h	Spare register bits assigned to cmnda_sparecdb.

Table 11-132. Register Call Summary for CMN_SPARE_REG_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_SPARE_REG_PREG Register \(Offset = 110h\) \[reset = X\]: \[0\]](#)

11.44 CMN_BIAS_TRIM_PREG__CMN_BIAS_EN_OVRD_PREG Register (Offset = 120h) [reset = X]

CMN_BIAS_TRIM_PREG__CMN_BIAS_EN_OVRD_PREG is shown in Figure 11-44 and described in Table 11-134.

Return to [Summary Table](#).

Bias diagnostic override register.

Table 11-133. CMN_BIAS_TRIM_PREG__CMN_BIAS_EN_OVRD_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0120h
SERDES_16G1	0501 0120h
SERDES_16G2	0502 0120h
SERDES_16G3	0503 0120h

Figure 11-44. CMN_BIAS_TRIM_PREG__CMN_BIAS_EN_OVRD_PREG Register

31	30	29	28	27	26	25	24
RESERVED		CMN_BIAS_TRIM_PREG					
R/W-X		R/W-7Fh					
23	22	21	20	19	18	17	16
CMN_BIAS_TRIM_PREG							
R/W-7Fh							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						CMN_BIAS_EN_OVRD_EN_P REG	CMN_BIAS_EN_OVRD_VAL_P REG
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-134. CMN_BIAS_TRIM_PREG__CMN_BIAS_EN_OVRD_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	CMN_BIAS_TRIM_PREG	R/W	7Fh	Drives the cmn_ana_bias block's thermometer encoded bus: Bias current 15'h7FFF 31.8uA Max. :: 15'h007F 26.6uA Nominal :: 15'h0000 21.9uA Min.
15-2	RESERVED	R/W	X	
1	CMN_BIAS_EN_OVRD_EN_PREG	R/W	0h	cmn_ana_bias enable active high override enable.
0	CMN_BIAS_EN_OVRD_VAL_PREG	R/W	0h	When cmn_bias_en_ovrd_en_preg is asserted high, this value overrides the normal mission-mode bias enable.

Table 11-135. Register Call Summary for CMN_BIAS_TRIM_PREG__CMN_BIAS_EN_OVRD_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_BIAS_TRIM_PREG__CMN_BIAS_EN_OVRD_PREG Register \(Offset = 120h\) \[reset = X\]: \[0\]](#)

11.45 CMN_BIAS_VREF_TRIM_PREG Register (Offset = 124h) [reset = X]

CMN_BIAS_VREF_TRIM_PREG is shown in Figure 11-45 and described in Table 11-137.

Return to [Summary Table](#).

Bias debug and test voltage reference trim register.

Table 11-136. CMN_BIAS_VREF_TRIM_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0124h
SERDES_16G1	0501 0124h
SERDES_16G2	0502 0124h
SERDES_16G3	0503 0124h

Figure 11-45. CMN_BIAS_VREF_TRIM_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			CMN_BIAS_VREFSEL_PREG	CMN_BIAS_VREFTRIM_PREG			
R/W-X			R/W-0h	R/W-10h			
7	6	5	4	3	2	1	0
CMN_BIAS_VREFTRIM_PREG							
R/W-10h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-137. CMN_BIAS_VREF_TRIM_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12	CMN_BIAS_VREFSEL_PREG	R/W	0h	Drives the cmn_ana_bias block vrefsel to select for voltage reference source: 0 Bandgap 1 Resistor ladder
11-0	CMN_BIAS_VREFTRIM_PREG	R/W	10h	Drives the cmn_ana_bias block's vreftrim setting the resistor ladder voltage reference trim. The bus is one-hot encoded increasing reference voltage from LSB to MSB. 12'h800 748.5mV Max. :: 12'h010 518.6mV Nominal :: 12'h001 377.0mV Min. Note only valid when cmn_bias_vrefsel_preg is 1'b1.

Table 11-138. Register Call Summary for CMN_BIAS_VREF_TRIM_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_BIAS_VREF_TRIM_PREG Register \(Offset = 124h\) \[reset = X\]: \[0\]](#)

11.46 CMN_PSMCLK_SDOSCSSEL_CTRL_PREG__CMN_REFRCV_PREG Register (Offset = 130h) [reset = X]

CMN_PSMCLK_SDOSCSSEL_CTRL_PREG__CMN_REFRCV_PREG is shown in Figure 11-46 and described in Table 11-140.

Return to [Summary Table](#).

Reference clock receiver register.

Table 11-139.

CMN_PSMCLK_SDOSCSSEL_CTRL_PREG__CMN_REFRCV_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0130h
SERDES_16G1	0501 0130h
SERDES_16G2	0502 0130h
SERDES_16G3	0503 0130h

Figure 11-46. CMN_PSMCLK_SDOSCSSEL_CTRL_PREG__CMN_REFRCV_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							CMN_PSMCLK_SDOSCSSEL_PREG
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED	CMN_REFRCV_BWVAL_PREG	CMN_REFRCV_REFCLK_TESTCLKEN_PREG	RESERVED			CMN_REFRCV_REFCLK_PL1LC1EN_PREG	
R/W-X	R/W-1h	R/W-0h	R/W-X			R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							CMN_REFRCV_REFCLK_TERMIN_PREG
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-140. CMN_PSMCLK_SDOSCSSEL_CTRL_PREG__CMN_REFRCV_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	CMN_PSMCLK_SDOSCSSEL_PREG	R/W	0h	cmn_psmclk_out source select. 1'b0 cmnda_sdosc_clk 1'b1 cmnda_refrcv_refclk
15	RESERVED	R/W	X	

Table 11-140. CMN_PSMCLK_SDOSSEL_CTRL_PREG__CMN_REFRCV_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-13	CMN_REFRCV_BWVAL_PREG	R/W	1h	Bus to control the receiver bandwidth. Set to highest setting where reference clock frequency does not exceed published minimum below. Min. frequency (MHz): 00 20 01 50 10 100 11 150 Note this control impacts the settling time.
12	CMN_REFRCV_REFCLK_TESTCLKEN_PREG	R/W	0h	Active high enable for CMOS only path from cmn_refclk_p to the digital.
11-9	RESERVED	R/W	X	
8	CMN_REFRCV_REFCLK_PLLC1EN_PREG	R/W	0h	Active high enable for refclk driver to PLLCMNLC1.
7-1	RESERVED	R/W	X	
0	CMN_REFRCV_REFCLK_TERMEN_PREG	R/W	0h	Active high termination enable for the refclk receiver.

Table 11-141. Register Call Summary for CMN_PSMCLK_SDOSSEL_CTRL_PREG__CMN_REFRCV_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PSMCLK_SDOSSEL_CTRL_PREG__CMN_REFRCV_PREG Register \(Offset = 130h\) \[reset = X\]: \[0\]](#)

11.47 CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG Register (Offset = 140h) [reset = X]

CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG is shown in Figure 11-47 and described in Table 11-143.

Return to [Summary Table](#).

Resistor calibration debug and test control register A.

Table 11-142. CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0140h
SERDES_16G1	0501 0140h
SERDES_16G2	0502 0140h
SERDES_16G3	0503 0140h

Figure 11-47. CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_RESCAL_RXOVREN_P REG	CMN_RESCAL_RXOVRVAL_P REG
R/W-X						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CMN_RESCAL_RXOVRVAL_PREG			CMN_RESCAL_TXOVREN_P REG	CMN_RESCAL_TXOVRVAL_PREG			
R/W-0h			R/W-0h	R/W-0h			
15	14	13	12	11	10	9	8
CMN_RESCAL_DONE	CMN_RESCAL_INITTMR_PREG			CMN_RESCAL_RXOFFSET_PREG			
R-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
CMN_RESCAL_RXOFFSET_P REG		CMN_RESCAL_TXOFFSET_PREG					
R/W-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-143. CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25	CMN_RESCAL_RXOVREN_PREG	R/W	0h	RX resistor calibration LUT value active high override enable.
24-21	CMN_RESCAL_RXOVRVAL_PREG	R/W	0h	When cmn_rescal_rxovren_preg is asserted, this value overrides the RX resistor calibration LUT value. Note this override should not be used to force high impedance on the Lane receiver superspeed pins. The rx_termination_in_{15:0} may be used for this function.
20	CMN_RESCAL_TXOVREN_PREG	R/W	0h	TX resistor calibration LUT value active high override enable.
19-16	CMN_RESCAL_TXOVRVAL_PREG	R/W	0h	When cmn_rescal_txovren_preg is asserted, this value overrides the TX resistor calibration LUT value.
15	CMN_RESCAL_DONE	R	0h	Resistor calibration active high done flag.

Table 11-143. CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	CMN_RESCAL_INITTMR_PREG	R/W	0h	Sets the value of the timer used to allow the clock to settle at startup and before incrementing calibration code. The delay is $2^{(\text{cmn_rescal_inittmr} + 3)} - 1$ cmn_refclk periods.
11-6	CMN_RESCAL_RXOFFS_ET_PREG	R/W	0h	Twos compliment offset to be added to the calibrated resistor code prior to the receive LUT.
5-0	CMN_RESCAL_TXOFFS_ET_PREG	R/W	0h	Twos compliment offset to be added to the calibrated resistor code prior to the transmit LUT.

Table 11-144. Register Call Summary for CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] CMN_RESCAL_CTRLB_PREG__CMN_RESCAL_CTRLA_PREG Register (Offset = 140h) [reset = X]: [0]

11.48 CMN_RESCAL_STATUS_PREG__CMN_RESCAL_OVRD_PREG Register (Offset = 144h) [reset = X]

CMN_RESCAL_STATUS_PREG__CMN_RESCAL_OVRD_PREG is shown in [Figure 11-48](#) and described in [Table 11-146](#).

[Return to Summary Table.](#)

Resistor diagnostic override register.

Table 11-145. CMN_RESCAL_STATUS_PREG__CMN_RESCAL_OVRD_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0144h
SERDES_16G1	0501 0144h
SERDES_16G2	0502 0144h
SERDES_16G3	0503 0144h

Figure 11-48. CMN_RESCAL_STATUS_PREG__CMN_RESCAL_OVRD_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	CMN_RESCAL_STATE						
R/W-X	R-4h						
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			CMN_RESCAL_EN_FORCE_PREG	RESERVED			CMN_RESCAL_RUN_OVRD_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-146. CMN_RESCAL_STATUS_PREG__CMN_RESCAL_OVRD_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	CMN_RESCAL_STATE	R	4h	Resistor calibration FSM state vector.
15-5	RESERVED	R/W	X	
4	CMN_RESCAL_EN_FORCE_PREG	R/W	0h	Resistor calibration analog enable force. When asserted, the cmnda_rescal_en is forced high regardless of the state of the resistor calibration state machine.
3-1	RESERVED	R/W	X	
0	CMN_RESCAL_RUN_OVRD_PREG	R/W	0h	Resistor calibration active high run override.

Table 11-147. Register Call Summary for CMN_RESCAL_STATUS_PREG__CMN_RESCAL_OVRD_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_RESCAL_STATUS_PREG__CMN_RESCAL_OVRD_PREG Register \(Offset = 144h\) \[reset = X\]: \[0\]](#)

11.49 CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG Register (Offset = 150h) [reset = X]

CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG is shown in Figure 11-49 and described in Table 11-149.

Return to [Summary Table](#).

ATB debug and test control register.

Table 11-148.
CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0150h
SERDES_16G1	0501 0150h
SERDES_16G2	0502 0150h
SERDES_16G3	0503 0150h

Figure 11-49. CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG Register

31	30	29	28	27	26	25	24
CMN_ATB_ADC_START_PREG	CMN_ATB_ADC_DONE	CMN_ATB_ADC_MODE_PREG				RESERVED	
R/W-0h	R-0h	R/W-0h				R/W-X	
23	22	21	20	19	18	17	16
CMN_ATB_ADC_CODE							
R-0h							
15	14	13	12	11	10	9	8
CMN_ATB_CTRL_ATBEN_PREG	CMN_ATB_CTRL_BUMP_COEN_PREG	CMN_ATB_CTRL_REGION_SEL_PREG	CMN_ATB_CTRL_LANE_SEL_PREG			CMN_ATB_CTRL_COMPONENT_SEL_PREG	
R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h	
7	6	5	4	3	2	1	0
CMN_ATB_CTRL_COMPONENT_SEL_PREG				CMN_ATB_CTRL_ATBSEL_PREG			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-149. CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_ATB_ADC_START_PREG	R/W	0h	Active high signal that initiates the ADC to convert the ATB analog signal. It should remain high until cmn_atb_adc_done asserts. It must be written low and then high again to trigger another conversion.
30	CMN_ATB_ADC_DONE	R	0h	Active high flag indicating current conversion is complete.

Table 11-149. CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29-27	CMN_ATB_ADC_MODE_PREG	R/W	0h	Drives the mode port on the ADC selecting the input mux configuration as follows: Pos polarity / Neg polarity 3'b000 hiZ / hiZ 3'b001 In_atb0 / local agnd 3'b010 In_atb0 / In_atb1* 3'b011 In_atb1 / local agnd 3'b100 In_atb1 / In_atb0* 3'b101 In_atb0** / local agnd 3'b110 In_atb1** / local agnd 3'b111 In_atb0*** / local agnd * Must be remote agnd. **10KΩ between input and local agnd. *** 10KΩ between input and local cmn_avdd.
26-24	RESERVED	R/W	X	
23-16	CMN_ATB_ADC_CODE	R	0h	Current conversion results of the analog value on the ATB. Note valid only once cmn_atb_adc_done has asserted.
15	CMN_ATB_CTRL_ATBEN_PREG	R/W	0h	Internal ATB active high enable.
14	CMN_ATB_CTRL_BUMP_CON_EN_PREG	R/W	0h	ATB bump connection active high enable.
13	CMN_ATB_CTRL_REGION_SEL_PREG	R/W	0h	ATB region select: Description 0 Common 1 Lane
12-9	CMN_ATB_CTRL_LANE_SEL_PREG	R/W	0h	ATB lane select:
8-4	CMN_ATB_CTRL_COMPONENT_SEL_PREG	R/W	0h	ATB component select: Supported components are defined in tables within the Testability Section's ATB subsection.
3-0	CMN_ATB_CTRL_ATBSEL_PREG	R/W	0h	ATB test point select: Selects a particular test point to be observed within the selected component. Supported components and their associated test points are defined in tables within the Testability Section's ATB subsection.

Table 11-150. Register Call Summary for CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_ATB_ADC_PREG__CMN_ATB_CTRL_PREG Register \(Offset = 150h\) \[reset = X\]: \[0\]](#)

11.50 CMN_CORE_ATB_EN_PREG__CMN_ATB_ADC_EN_TMR_PREG Register (Offset = 154h) [reset = X]

CMN_CORE_ATB_EN_PREG__CMN_ATB_ADC_EN_TMR_PREG is shown in Figure 11-50 and described in Table 11-152.

Return to [Summary Table](#).

ATB debug and test ADC enable and timer register.

Table 11-151. CMN_CORE_ATB_EN_PREG__CMN_ATB_ADC_EN_TMR_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0154h
SERDES_16G1	0501 0154h
SERDES_16G2	0502 0154h
SERDES_16G3	0503 0154h

Figure 11-50. CMN_CORE_ATB_EN_PREG__CMN_ATB_ADC_EN_TMR_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							CMN_CORE_ATBESD_EN_PREG
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED					CMN_ATB_ADC_EN_PREG	CMN_ATB_ADC_EN_TMR_PREG	
R/W-X					R/W-0h	R/W-3Fh	
7	6	5	4	3	2	1	0
CMN_ATB_ADC_EN_TMR_PREG							
R/W-3Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-152. CMN_CORE_ATB_EN_PREG__CMN_ATB_ADC_EN_TMR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	CMN_CORE_ATBESD_EN_PREG	R/W	0h	Core ATB pin connection active high enable.
15-11	RESERVED	R/W	X	
10	CMN_ATB_ADC_EN_PREG	R/W	0h	ADC enable force overriding state dependent enable: Normally the ADC enable is controlled by a state machine that enables it when the cmn_atb_adc_start_preg is written high. This register is ORed with the FSM controlled enable, allowing the user to force the ADC on.
9-0	CMN_ATB_ADC_EN_TMR_PREG	R/W	3Fh	Enable timer value : Number of timer clocks to hold the ATB digitizer control state machine in the A2D En state. This timer delay is specified in 2*(cmn_refclk periods).

Table 11-153. Register Call Summary for CMN_CORE_ATB_EN_PREG__CMN_ATB_ADC_EN_TMR_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_CORE_ATB_EN_PREG__CMN_ATB_ADC_EN_TMR_PREG Register \(Offset = 154h\) \[reset = X\]: \[0\]](#)

11.51 HSRRSM_STATUS_PREG__HSRRSM_CTRL_PREG Register (Offset = 160h) [reset = X]

HSRRSM_STATUS_PREG__HSRRSM_CTRL_PREG is shown in Figure 11-51 and described in Table 11-155.

Return to [Summary Table](#).

High Speed Reset Release State Machine control register.

Table 11-154.
HSRRSM_STATUS_PREG__HSRRSM_CTRL_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0160h
SERDES_16G1	0501 0160h
SERDES_16G2	0502 0160h
SERDES_16G3	0503 0160h

Figure 11-51. HSRRSM_STATUS_PREG__HSRRSM_CTRL_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				HSRRSM_STATE			
R/W-X				R-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				HSRRSM_DELAY_PREG			
R/W-X				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-155. HSRRSM_STATUS_PREG__HSRRSM_CTRL_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	HSRRSM_STATE	R	0h	High Speed Reset Release State Machine state vector.
15-3	RESERVED	R/W	X	
2-0	HSRRSM_DELAY_PREG	R/W	1h	Reset delay : Specifies the number of PSM clock cycles the Common High Speed Reset Release State Machine stays in the delay state. Note the value must be 1 or greater. The delay is hsrrsm_delay_preg +1 clock periods.

Table 11-156. Register Call Summary for HSRRSM_STATUS_PREG__HSRRSM_CTRL_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [HSRRSM_STATUS_PREG__HSRRSM_CTRL_PREG Register \(Offset = 160h\) \[reset = X\]: \[0\]](#)

11.52 CMN_REFRCV1_PREG Register (Offset = 170h) [reset = X]

CMN_REFRCV1_PREG is shown in Figure 11-52 and described in Table 11-158.

Return to [Summary Table](#).

Auxiliary reference clock receiver (refrcv1) register.

Table 11-157. CMN_REFRCV1_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0170h
SERDES_16G1	0501 0170h
SERDES_16G2	0502 0170h
SERDES_16G3	0503 0170h

Figure 11-52. CMN_REFRCV1_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	CMN_REFRCV1_BWVAL_PREG		CMN_REFRCV1_REFCLK_TESTCLKEN_PREG	RESERVED			CMN_REFRCV1_REFCLK_PL LLC1EN_PREG
R/W-X	R/W-1h		R/W-0h	R/W-X			R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CMN_REFRCV1_REFCLK_TEN_PREG
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-158. CMN_REFRCV1_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-13	CMN_REFRCV1_BWVAL_PREG	R/W	1h	Bus to control the receiver bandwidth. Set to highest setting where reference clock frequency does not exceed published minimum below. Minimum clock frequency (MHz) 00 20 01 50 10 100 11 150 Note this control impacts the settling time.
12	CMN_REFRCV1_REFCLK_TESTCLKEN_PREG	R/W	0h	Active high enable for CMOS only path from cmn_refclk1_p to the digital.
11-9	RESERVED	R/W	X	
8	CMN_REFRCV1_REFCLK_PL LC1EN_PREG	R/W	0h	Active high enable for refclk1 driver to PLLCMNLC.
7-1	RESERVED	R/W	X	

Table 11-158. CMN_REFRCV1_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMN_REFRCV1_REFCLK_TERMEN_PREG	R/W	0h	Active high termination enable for the refclk1 receiver.

Table 11-159. Register Call Summary for CMN_REFRCV1_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_REFRCV1_PREG Register \(Offset = 170h\) \[reset = X\]: \[0\]](#)

11.53 CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG Register (Offset = 180h) [reset = X]

CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG is shown in Figure 11-53 and described in Table 11-161.

Return to [Summary Table](#).

PLLCMNLC1 status register A.

Table 11-160.
CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0180h
SERDES_16G1	0501 0180h
SERDES_16G2	0502 0180h
SERDES_16G3	0503 0180h

Figure 11-53. CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_PLLLC1_STATUS_B_SSTWOPT_CODE	
R-X						R-0h	
23	22	21	20	19	18	17	16
CMN_PLLLC1_STATUS_B_SSTWOPT_CODE							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		CMN_PLLLC1_STATUS_A_DSMCORR_CODE					
R-X		R-0h					
7	6	5	4	3	2	1	0
CMN_PLLLC1_STATUS_A_LOCKED	CMN_PLLLC1_STATUS_A_DCOCAL_DONE	CMN_PLLLC1_STATUS_A_DCOCAL_CODE					
R-0h	R-0h	R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 11-161. CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	CMN_PLLLC1_STATUS_B_SSTWOPT_CODE	R	0h	Main PLLLC1 Spread Spectrum two point value result: Contains the sstwopt result. Note this register field is currently not supported.
15	RESERVED	R	X	
14-8	CMN_PLLLC1_STATUS_A_DSMCORR_CODE	R	0h	PLLCMNLC1 DSM spur correction code result: Contains the DSM spur correction value in gray code. Note this register is for diagnostic purposes only.
7	CMN_PLLLC1_STATUS_A_LOCKED	R	0h	PLLCMNLC1 locked Status: Description 1 Locked 0 Not locked

Table 11-161. CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CMN_PLLLC1_STATUS_A_DCOCAL_DONE	R	0h	PLLCMNLC1 DCO calibration status: Description 1 Calibration complete 0 Calibration has not completed Note this calibration status will deassert upon reset or when calibration starts and stay deasserted until calibration has completed.
5-0	CMN_PLLLC1_STATUS_A_DCOCAL_CODE	R	0h	PLLCMNLC1 DCO calibration code result: Contains the calibration result. Note the contents of this register are not valid until cmn_pll_c_status_a_dcocal_done has asserted. Note this register is for diagnostic purposes only.

Table 11-162. Register Call Summary for CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_STATUS_B_PREG__CMN_PLLLC1_STATUS_A_PREG Register \(Offset = 180h\) \[reset = X\]: \[0\]](#)

11.54 CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG Register (Offset = 184h) [reset = X]

CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG is shown in Figure 11-54 and described in Table 11-164.

Return to [Summary Table](#).

PLLCMNLC1 general control register.

Table 11-163. CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0184h
SERDES_16G1	0501 0184h
SERDES_16G2	0502 0184h
SERDES_16G3	0503 0184h

Figure 11-54. CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_PLLLC1_FBDIVINT_PREG	
R/W-X						R/W-32h	
23	22	21	20	19	18	17	16
CMN_PLLLC1_FBDIVINT_PREG							
R/W-32h							
15	14	13	12	11	10	9	8
RESERVED		CMN_PLLLC1_LOCKED_OVRD_EN_PREG	CMN_PLLLC1_LOCKED_OVRD_PREG	RESERVED		CMN_PLLLC1_PLL_REG_ISO_OVRD_EN_PREG	CMN_PLLLC1_PLL_REG_ISO_OVRD_PREG
R/W-X		R/W-0h	R/W-0h	R/W-X		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CMN_PLLLC1_LOCK_HOLD_OVRD_EN_PREG	CMN_PLLLC1_LOCK_HOLD_OVRD_PREG	CMN_PLLLC1_PLL_EN_OVRD_EN_PREG	CMN_PLLLC1_PLL_EN_OVRD_PREG	CMN_PLLLC1_PLL_RESET_N_OVRD_EN_PREG	CMN_PLLLC1_PLL_RESET_N_OVRD_PREG	CMN_PLLLC1_PFDCLK1_SEL_PREG	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-164. CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	CMN_PLLLC1_FBDIVINT_PREG	R/W	32h	This value sets the mode dependent PLLCMNLC1 fbdivint value.
15-14	RESERVED	R/W	X	
13	CMN_PLLLC1_LOCKED_OVRD_EN_PREG	R/W	0h	PLLCMNLC1 locked active high override enable: Note this register is for diagnostic purposes only.
12	CMN_PLLLC1_LOCKED_OVRD_PREG	R/W	0h	PLLCMNLC1 locked signal force: When cmn_plllic1_locked_ovrd_en_preg is asserted high, this value overrides lock flag from PLLCMNLC1. Note this register is for diagnostic purposes only.
11-10	RESERVED	R/W	X	
9	CMN_PLLLC1_PLL_REG_ISO_OVRD_EN_PREG	R/W	0h	PLLCMNLC1 regulator isolation active high override enable Note this register is for diagnostic purposes only.

**Table 11-164. CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
8	CMN_PLLLC1_PLL_REG_ISO_OVRD_PREG	R/W	0h	When cmn_pll1c1_pll_reg_iso_ovrd_en_preg is asserted high, overrides the state dependent PLLCMNLC1 regulator isolation value. Note this register is for diagnostic purposes only.
7	CMN_PLLLC1_LOCK_HOLD_OVRD_EN_PREG	R/W	0h	Lock detection hold function active high override enable. Note this register is for diagnostic purposes only.
6	CMN_PLLLC1_LOCK_HOLD_OVRD_PREG	R/W	0h	When cmn_pll1c1_lock_hold_ovrd_en_preg is asserted high, overrides the state dependent lock detect function value. Note this register is for diagnostic purposes only.
5	CMN_PLLLC1_PLL_EN_OVRD_EN_PREG	R/W	0h	PLLCMNLC1 enable active high override enable. Note this register is for diagnostic purposes only.
4	CMN_PLLLC1_PLL_EN_OVRD_PREG	R/W	0h	When cmn_pll1c1_pll_en_ovrd_en_preg is asserted high, overrides the state dependent PLLCMNLC1 enable value. Note this register is for diagnostic purposes only.
3	CMN_PLLLC1_PLL_RESET_N_OVRD_EN_PREG	R/W	0h	PLLCMNLC1 active high reset override enable. Note this register is for diagnostic purposes only.
2	CMN_PLLLC1_PLL_RESET_N_OVRD_PREG	R/W	0h	When cmn_pll1c1_pll_reset_n_ovrd_en_preg is asserted high, overrides the state dependent PLLCMNLC1 active low reset value. Note this register is for diagnostic purposes only.
1	CMN_PLLLC1_PFDCLK1_SEL_PREG	R/W	0h	When asserted the pfdclk1 is used as the reference clock, When deasserted, pfdclk is used.
0	RESERVED	R/W	X	

Table 11-165. Register Call Summary for CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_FBDIV_INT_PREG__CMN_PLLLC1_GEN_PREG Register \(Offset = 184h\) \[reset = X\]: \[0\]](#)

11.55 CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG Register (Offset = 188h) [reset = X]

CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG is shown in [Figure 11-55](#) and described in [Table 11-167](#).

Return to [Summary Table](#).

PLLCMNLC1 fractional feedback divider register.

Table 11-166.
CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0188h
SERDES_16G1	0501 0188h
SERDES_16G2	0502 0188h
SERDES_16G3	0503 0188h

Figure 11-55. CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_PLLLC1_DCOCAL_STA RT_OVRD_EN _PREG	CMN_PLLLC1_DCOCAL_STA RT_OVRD_PR EG
R/W-X						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED		CMN_PLLLC1_DCOCAL_STARTVAL_PREG					
R/W-X		R/W-12h					
15	14	13	12	11	10	9	8
CMN_PLLLC1_FBDIVFRAC_PREG							
R/W-0h							
7	6	5	4	3	2	1	0
CMN_PLLLC1_FBDIVFRAC_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-167. CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25	CMN_PLLLC1_DCOCAL_START_OVRD_EN_PREG	R/W	0h	DCO calibration start active high override enable.
24	CMN_PLLLC1_DCOCAL_START_OVRD_PREG	R/W	0h	When cmn_pll1c1_dcocal_start_ovrd_en_preg is asserted high, this value overrides the mode dependent DCO calibration start value.
23-22	RESERVED	R/W	X	
21-16	CMN_PLLLC1_DCOCAL_STARTVAL_PREG	R/W	12h	This value sets the DCO calibration startval value. Note: This must be set to a value that is always at least one step size away from the minimum and maximum calibration codes. For example, if the initial step size is 8 (cmn_pll1c1_dcocal_initstep_preg = 3'b011), this value must be at least 6'h08 and less than 6'h37.

Table 11-167. CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	CMN_PLLLC1_FBDIVFRAC_PREG	R/W	0h	This value sets the mode dependent PLLCMNLC1 fbdivfrac value.

**Table 11-168. Register Call Summary for
CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_DCOCAL_CTRL_PREG__CMN_PLLLC1_FBDIV_FRAC_PREG Register \(Offset = 188h\) \[reset = X\]: \[0\]](#)

11.56 CMN_PLLLC1_ITERTMR_PREG__CMN_PLLLC1_INIT_PREG Register (Offset = 18Ch) [reset = X]

CMN_PLLLC1_ITERTMR_PREG__CMN_PLLLC1_INIT_PREG is shown in Figure 11-56 and described in Table 11-170.

Return to [Summary Table](#).

PLLCMNLC1 DCO calibration initialization register.

Table 11-169. CMN_PLLLC1_ITERTMR_PREG__CMN_PLLLC1_INIT_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 018Ch
SERDES_16G1	0501 018Ch
SERDES_16G2	0502 018Ch
SERDES_16G3	0503 018Ch

Figure 11-56. CMN_PLLLC1_ITERTMR_PREG__CMN_PLLLC1_INIT_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_PLLLC1_DCOCAL_ITERTMR_PREG			
R/W-X				R/W-6Eh			
23	22	21	20	19	18	17	16
CMN_PLLLC1_DCOCAL_ITERTMR_PREG							
R/W-6Eh							
15	14	13	12	11	10	9	8
RESERVED	CMN_PLLLC1_DCOCAL_INITSTEP_PREG			CMN_PLLLC1_DCOCAL_INITTMR_PREG			
R/W-X		R/W-3h			R/W-5Ah		
7	6	5	4	3	2	1	0
CMN_PLLLC1_DCOCAL_INITTMR_PREG							
R/W-5Ah							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-170. CMN_PLLLC1_ITERTMR_PREG__CMN_PLLLC1_INIT_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLC1_DCOCAL_ITERTMR_PREG	R/W	6Eh	This value sets the DCO calibration iteration timer value.
15	RESERVED	R/W	X	
14-12	CMN_PLLLC1_DCOCAL_INITSTEP_PREG	R/W	3h	This value sets the DCO calibration initialization step value. 3'b 000 : 1 step 3'b 001 : 2 step 3'b 010 : 4 step 3'b 011 : 8 step 3'b 100 : 16 step 3'b 101 - 3'b 111 : reserved
11-0	CMN_PLLLC1_DCOCAL_INITTMR_PREG	R/W	5Ah	This value sets the DCO calibration initialization timer value.

Table 11-171. Register Call Summary for CMN_PLLLC1_ITERTMR_PREG__CMN_PLLLC1_INIT_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_ITERTMR_PREG__CMN_PLLLC1_INIT_PREG Register \(Offset = 18Ch\) \[reset = X\]: \[0\]](#)

11.57 CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG Register (Offset = 190h) [reset = X]

CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG is shown in Figure 11-57 and described in Table 11-173.

Return to [Summary Table](#).

PLLCMNLC1 mode register.

Table 11-172.
CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0190h
SERDES_16G1	0501 0190h
SERDES_16G2	0502 0190h
SERDES_16G3	0503 0190h

Figure 11-57. CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG Register

31	30	29	28	27	26	25	24
RESERVED	CMN_PLLLC1_LF_PROPCOEFF_MODE1_PREG			RESERVED			CMN_PLLLC1_LF_PROPFRA C_MODE1_PREG
R/W-X	R/W-3h			R/W-X			R/W-0h
23	22	21	20	19	18	17	16
CMN_PLLLC1_LF_PROPFRA C_MODE1_PREG				CMN_PLLLC1_LF_INTCOEFF_MODE1_PREG			
R/W-0h				R/W-6h			
15	14	13	12	11	10	9	8
RESERVED							CMN_PLLLC1_IN TMODE_PREG
R/W-X							R/W-1h
7	6	5	4	3	2	1	0
RESERVED				CMN_PLLLC1_TDCMODE_PREG			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-173. CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	CMN_PLLLC1_LF_PROP COEFF_MODE1_PREG	R/W	3h	This value sets the loop filter proportional coefficient value when cmn_pll1c1_mode is asserted.
27-25	RESERVED	R/W	X	
24-20	CMN_PLLLC1_LF_PROP FRAC_MODE1_PREG	R/W	0h	This value sets the loop filter fractional coefficient value when cmn_pll1c1_mode is asserted.
19-16	CMN_PLLLC1_LF_INTCO EFF_MODE1_PREG	R/W	6h	This value sets the loop filter integer coefficient value when cmn_pll1c1_mode is asserted.
15-9	RESERVED	R/W	X	
8	CMN_PLLLC1_INTMODE _PREG	R/W	1h	This value sets the integer mode value.

Table 11-173. CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	
3-0	CMN_PLLLC1_TDCMODE_PREG	R/W	0h	<p>This value sets the TDC mode value.</p> <p>Gain (ps/LSB)</p> <p>0 1</p> <p>1 1.07</p> <p>2 1.14</p> <p>3 1.23</p> <p>4 1.33</p> <p>5 1.45</p> <p>6 1.6</p> <p>7 1.78</p> <p>8 2.0</p> <p>9 2.29</p> <p>10 2.67</p> <p>11 3.2</p> <p>12 4.0</p> <p>13 5.33</p> <p>14 8.0</p> <p>15 16</p>

**Table 11-174. Register Call Summary for
CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_LF_COEFF_MODE1_PREG__CMN_PLLLC1_MODE_PREG Register \(Offset = 190h\) \[reset = X\]: \[0\]](#)

11.58 CMN_PLLLC1_LOCK_CNTSTART_PREG__CMN_PLLLC1_LF_COEFF_MODE0_PREG Register (Offset = 194h) [reset = X]

CMN_PLLLC1_LOCK_CNTSTART_PREG__CMN_PLLLC1_LF_COEFF_MODE0_PREG is shown in Figure 11-58 and described in Table 11-176.

Return to [Summary Table](#).

PLLCMNLC1 loop filter register for mode 0.

Table 11-175.
CMN_PLLLC1_LOCK_CNTSTART_PREG__CMN_PLLLC1_LF_COEFF_MODE0_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 0194h
SERDES_16G1	0501 0194h
SERDES_16G2	0502 0194h
SERDES_16G3	0503 0194h

Figure 11-58. CMN_PLLLC1_LOCK_CNTSTART_PREG__CMN_PLLLC1_LF_COEFF_MODE0_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_PLLLC1_LOCK_CNTSTART_PREG			
R/W-X				R/W-3E8h			
23	22	21	20	19	18	17	16
CMN_PLLLC1_LOCK_CNTSTART_PREG							
R/W-3E8h							
15	14	13	12	11	10	9	8
RESERVED	CMN_PLLLC1_LF_PROPCOEFF_MODE0_PREG			RESERVED			CMN_PLLLC1_LF_PROPFRAC_MODE0_PREG
R/W-X	R/W-2h			R/W-X			R/W-0h
7	6	5	4	3	2	1	0
CMN_PLLLC1_LF_PROPFRAC_MODE0_PREG				CMN_PLLLC1_LF_INTCOEFF_MODE0_PREG			
R/W-0h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-176. CMN_PLLLC1_LOCK_CNTSTART_PREG__CMN_PLLLC1_LF_COEFF_MODE0_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLC1_LOCK_CNTSTART_PREG	R/W	3E8h	This value sets the lock counter start value.
15	RESERVED	R/W	X	
14-12	CMN_PLLLC1_LF_PROPCOEFF_MODE0_PREG	R/W	2h	This value sets the loop filter proportional coefficient value when cmn_pll1c1_mode is deasserted.
11-9	RESERVED	R/W	X	
8-4	CMN_PLLLC1_LF_PROPFRAC_MODE0_PREG	R/W	0h	This value sets the loop filter fractional coefficient value when cmn_pll1c1_mode is deasserted.
3-0	CMN_PLLLC1_LF_INTCOEFF_MODE0_PREG	R/W	5h	This value sets the loop filter integer coefficient value when cmn_pll1c1_mode is deasserted.

**Table 11-177. Register Call Summary for
CMN_PLLLC1_LOCK_CNTSTART_PREG__CMN_PLLLC1_LF_COEFF_MODE0_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_LOCK_CNTSTART_PREG__CMN_PLLLC1_LF_COEFF_MODE0_PREG Register \(Offset = 194h\) \[reset = X\]: \[0\]](#)

11.59 CMN_PLLLC1_CLK1_PREG__CMN_PLLLC1_LOCK_CNTTHRESH_PREG Register (Offset = 198h) [reset = X]

CMN_PLLLC1_CLK1_PREG__CMN_PLLLC1_LOCK_CNTTHRESH_PREG is shown in Figure 11-59 and described in Table 11-179.

Return to [Summary Table](#).

PLLCMNLC1 lock count threshold register.

Table 11-178.
CMN_PLLLC1_CLK1_PREG__CMN_PLLLC1_LOCK_CNTTHRESH_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 0198h
SERDES_16G1	0501 0198h
SERDES_16G2	0502 0198h
SERDES_16G3	0503 0198h

Figure 11-59. CMN_PLLLC1_CLK1_PREG__CMN_PLLLC1_LOCK_CNTTHRESH_PREG Register

31	30	29	28	27	26	25	24
RESERVED			CMN_PLLLC1_CLK1_EN_PREG	RESERVED			
R/W-X			R/W-0h	R/W-X			
23	22	21	20	19	18	17	16
RESERVED	CMN_PLLLC1_CLK1OUTDIV_PREG						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED				CMN_PLLLC1_LOCK_CNTTHRESH_PREG			
R/W-X				R/W-1h			
7	6	5	4	3	2	1	0
CMN_PLLLC1_LOCK_CNTTHRESH_PREG							
R/W-1h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-179. CMN_PLLLC1_CLK1_PREG__CMN_PLLLC1_LOCK_CNTTHRESH_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28	CMN_PLLLC1_CLK1_EN_PREG	R/W	0h	This value sets the clock1 enable value.
27-23	RESERVED	R/W	X	
22-16	CMN_PLLLC1_CLK1OUTDIV_PREG	R/W	0h	This value sets the clock1 output divider value.
15-12	RESERVED	R/W	X	
11-0	CMN_PLLLC1_LOCK_CNTTHRESH_PREG	R/W	1h	PLLCMNLC1 lock counter threshold value : This value sets the lock count threshold. This is the value used by the PLLCMNLC1 lock detection logic to determine if the PLL has locked. If the two counters in the PLL lock detection logic differ by less than this value, the PLL is considered locked. Note: this function is deprecated.

**Table 11-180. Register Call Summary for
CMN_PLLLC1_CLK1_PREG__CMN_PLLLC1_LOCK_CNTTHRESH_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_CLK1_PREG__CMN_PLLLC1_LOCK_CNTTHRESH_PREG Register \(Offset = 198h\) \[reset = X\]: \[0\]](#)

11.60 CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG Register (Offset = 19Ch) [reset = X]

CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG is shown in Figure 11-60 and described in Table 11-182.

Return to [Summary Table](#).

PLLCMNLC1 clock0 register.

Table 11-181.
CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 019Ch
SERDES_16G1	0501 019Ch
SERDES_16G2	0502 019Ch
SERDES_16G3	0503 019Ch

Figure 11-60. CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG Register

31	30	29	28	27	26	25	24
CMN_PLLLC1_BWCAL_EN_MODE1_PREG	RESERVED				CMN_PLLLC1_BWCAL_THRESH_MODE1_PREG		
R/W-1h	R/W-X				R/W-Ah		
23	22	21	20	19	18	17	16
RESERVED				CMN_PLLLC1_BWCAL_TMR_MODE1_PREG			
R/W-X				R/W-4h			
15	14	13	12	11	10	9	8
RESERVED				CMN_PLLLC1_CLK0_EN_PREG	RESERVED		
R/W-X				R/W-1h	R/W-X		
7	6	5	4	3	2	1	0
RESERVED	CMN_PLLLC1_CLK0OUTDIV_PREG						
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-182. CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLLLC1_BWCAL_EN_MODE1_PREG	R/W	1h	This value sets the bwcal enable value when cmn_pll1c1_mode is asserted.
30-28	RESERVED	R/W	X	
27-24	CMN_PLLLC1_BWCAL_THRESH_MODE1_PREG	R/W	Ah	This value sets the bwcal threshold value when cmn_pll1c1_mode is asserted.
23-21	RESERVED	R/W	X	
20-16	CMN_PLLLC1_BWCAL_TMR_MODE1_PREG	R/W	4h	This value sets the bwcal timer value when cmn_pll1c1_mode is asserted.
15-13	RESERVED	R/W	X	
12	CMN_PLLLC1_CLK0_EN_PREG	R/W	1h	This value sets the clock0 enable value.
11-7	RESERVED	R/W	X	

Table 11-182. CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	CMN_PLLLC1_CLK0OUT DIV_PREG	R/W	1h	This value sets the clock0 output divider value.

**Table 11-183. Register Call Summary for
CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_BWCAL_MODE1_PREG__CMN_PLLLC1_CLK0_PREG Register \(Offset = 19Ch\) \[reset = X\]: \[0\]](#)

11.61 CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG Register (Offset = 1A0h) [reset = X]

CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG is shown in Figure 11-61 and described in Table 11-185.

Return to [Summary Table](#).

PLLCMNLC1 bandwidth cal register for mode 0.

Table 11-184.
CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 01A0h
SERDES_16G1	0501 01A0h
SERDES_16G2	0502 01A0h
SERDES_16G3	0503 01A0h

Figure 11-61. CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG Register

31	30	29	28	27	26	25	24
RESERVED					CMN_PLLLC1_DSMCORR_EN_PREG	CMN_PLLLC1_DSMCORR_STA RTVAL_PREG	
R/W-X					R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
CMN_PLLLC1_DSMCORR_STARTVAL_PREG					CMN_PLLLC1_DSMCORR_GAIN_PREG		
R/W-0h					R/W-0h		
15	14	13	12	11	10	9	8
CMN_PLLLC1_BWCAL_EN_MODE0_PREG	RESERVED			CMN_PLLLC1_BWCAL_THRESH_MODE0_PREG			
R/W-1h	R/W-X			R/W-7h			
7	6	5	4	3	2	1	0
RESERVED			CMN_PLLLC1_BWCAL_TMR_MODE0_PREG				
R/W-X			R/W-6h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-185. CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CMN_PLLLC1_DSMCORR_EN_PREG	R/W	0h	This value sets the DSM spur correction coefficient enable value.
25-19	CMN_PLLLC1_DSMCORR_STARTVAL_PREG	R/W	0h	This value sets the DSM spur correction coefficient startval value.
18-16	CMN_PLLLC1_DSMCORR_GAIN_PREG	R/W	0h	This value sets the DSM spur correction coefficient gain value.
15	CMN_PLLLC1_BWCAL_EN_MODE0_PREG	R/W	1h	This value sets the bwcal enable value when cmn_pll1c1_mode is deasserted.
14-12	RESERVED	R/W	X	
11-8	CMN_PLLLC1_BWCAL_THRESH_MODE0_PREG	R/W	7h	This value sets the bwcal threshold value when cmn_pll1c1_mode is deasserted.
7-5	RESERVED	R/W	X	

Table 11-185. CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CMN_PLLLC1_BWCAL_TMR_MODE0_PREG	R/W	6h	This value sets the bwcal timer value when cmn_pll1c1_mode is deasserted.

**Table 11-186. Register Call Summary for
CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_DSMCORR_PREG__CMN_PLLLC1_BWCAL_MODE0_PREG Register \(Offset = 1A0h\) \[reset = X\]: \[0\]](#)

11.62 CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC1_SS_PREG Register (Offset = 1A4h) [reset = X]

CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC1_SS_PREG is shown in Figure 11-62 and described in Table 11-188.

Return to [Summary Table](#).

PLLCMNLC1 spread spectrum register.

Table 11-187.
CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC1_SS_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 01A4h
SERDES_16G1	0501 01A4h
SERDES_16G2	0502 01A4h
SERDES_16G3	0503 01A4h

Figure 11-62. CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC1_SS_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	CMN_PLLLC1_SS_NUM_STEPS_PREG						
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
CMN_PLLLC1_SS_ENABLE_PREG	RESERVED						
R/W-0h				R/W-X			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-188. CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC1_SS_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG	R/W	0h	This value sets the spread spectrum amp step size value.
15	RESERVED	R/W	X	
14-8	CMN_PLLLC1_SS_NUM_STEPS_PREG	R/W	0h	This value sets the spread spectrum number of steps value.
7	CMN_PLLLC1_SS_ENABLE_PREG	R/W	0h	This value sets the spread spectrum enable value.
6-0	RESERVED	R/W	X	

**Table 11-189. Register Call Summary for
CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC1_SS_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_SS_AMP_STEP_SIZE_PREG__CMN_PLLLC1_SS_PREG Register \(Offset = 1A4h\) \[reset = X\]: \[0\]](#)

11.63 CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLLLC1_SSTWOPT_PREG Register (Offset = 1A8h) [reset = X]

CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLLLC1_SSTWOPT_PREG is shown in Figure 11-63 and described in Table 11-191.

Return to [Summary Table](#).

PLLCMNL1 spread spectrum two point register.

Table 11-190.
CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLLLC1_SSTWOPT_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 01A8h
SERDES_16G1	0501 01A8h
SERDES_16G2	0502 01A8h
SERDES_16G3	0503 01A8h

Figure 11-63. CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLLLC1_SSTWOPT_PREG Register

31	30	29	28	27	26	25	24
RESERVED						CMN_PLLLC1_LF_PROP_OVR_PREG	CMN_PLLLC1_LF_PROP_OVR_PREG
R/W-X						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CMN_PLLLC1_LF_PROP_OVR_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					CMN_PLLLC1_SSTWOPT_EN_PREG	CMN_PLLLC1_SSTWOPT_STA_RTVAL_PREG	
R/W-X					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
CMN_PLLLC1_SSTWOPT_STARTVAL_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-191. CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLLLC1_SSTWOPT_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25	CMN_PLLLC1_LF_PROP_OVR_PREG	R/W	0h	Drives the lfprop_ovren pin on the PLLCMNL1.
24-16	CMN_PLLLC1_LF_PROP_OVR_PREG	R/W	0h	Drives the lfprop_ovrval on the PLLCMNL1.
15-11	RESERVED	R/W	X	
10	CMN_PLLLC1_SSTWOPT_EN_PREG	R/W	0h	This value sets the sstwopt_en pin on the PLL.
9-0	CMN_PLLLC1_SSTWOPT_STARTVAL_PREG	R/W	0h	This value sets the sstwopt_startval pins on the PLL.

**Table 11-192. Register Call Summary for
CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLLLC1_SSTWOPT_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_LF_PROP_OVR_PREG__CMN_PLLLC1_SSTWOPT_PREG Register \(Offset = 1A8h\) \[reset = X\]: \[0\]](#)

11.64 CMN_PLLLC1_DSMCRR_OVR_PREG__CMN_PLLLC1_LF_INT_OVR_PREG Register (Offset = 1ACh) [reset = X]

CMN_PLLLC1_DSMCRR_OVR_PREG__CMN_PLLLC1_LF_INT_OVR_PREG is shown in Figure 11-64 and described in Table 11-194.

Return to [Summary Table](#).

PLLCMNLC1 debug and test loop filter integer override register.

Table 11-193.
CMN_PLLLC1_DSMCRR_OVR_PREG__CMN_PLLLC1_LF_INT_OVR_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 01ACh
SERDES_16G1	0501 01ACh
SERDES_16G2	0502 01ACh
SERDES_16G3	0503 01ACh

Figure 11-64. CMN_PLLLC1_DSMCRR_OVR_PREG__CMN_PLLLC1_LF_INT_OVR_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
CMN_PLLLC1_DSMCRR_OVR_PREG	CMN_PLLLC1_DSMCRR_OVR_PREG						
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED		CMN_PLLLC1_LF_INT_OVR_PREG	CMN_PLLLC1_LF_INT_OVR_PREG				
R/W-X		R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
CMN_PLLLC1_LF_INT_OVR_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-194. CMN_PLLLC1_DSMCRR_OVR_PREG__CMN_PLLLC1_LF_INT_OVR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	CMN_PLLLC1_DSMCRR_OVR_PREG	R/W	0h	Drives the dsmcrr_ovren port on the PLLCMNLC1.
22-16	CMN_PLLLC1_DSMCRR_OVR_PREG	R/W	0h	Drives the dsmcrr_ovrval port on the PLLCMNLC1.
15-14	RESERVED	R/W	X	
13	CMN_PLLLC1_LF_INT_OVR_PREG	R/W	0h	Drives the lf_int_ovren pin on the PLLCMNLC1.
12-0	CMN_PLLLC1_LF_INT_OVR_PREG	R/W	0h	Drives the lf_int_ovrval pin on the PLLCMNLC1.

**Table 11-195. Register Call Summary for
CMN_PLLLC1_DSMCORR_OVR_PREG__CMN_PLLLC1_LF_INT_OVR_PREG**

16-G SerDes Registers
<ul style="list-style-type: none">• 2-L SerDes Registers: [0] [1]• CMN_PLLLC1_DSMCORR_OVR_PREG__CMN_PLLLC1_LF_INT_OVR_PREG Register (Offset = 1ACh) [reset = X]: [0]

11.65 CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG Register (Offset = 1B0h) [reset = X]

CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG is shown in Figure 11-65 and described in Table 11-197.

Return to [Summary Table](#).

PLLCMNLC1 debug and test loop Spread Spectrum two point override register.

Table 11-196.

CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 01B0h
SERDES_16G1	0501 01B0h
SERDES_16G2	0502 01B0h
SERDES_16G3	0503 01B0h

Figure 11-65. CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG Register

31	30	29	28	27	26	25	24
RESERVED	CMN_PLLLC1_DCOCAL_OVR_EN_PREG	CMN_PLLLC1_DCOCAL_OVRVAL_PREG					
R/W-X	R/W-0h	R/W-0h					
23	22	21	20	19	18	17	16
RESERVED	CMN_PLLLC1_DCO_ITRIM_PREG				CMN_PLLLC1_ROFFSET_PREG		
R/W-X	R/W-3h				R/W-3h		
15	14	13	12	11	10	9	8
RESERVED					CMN_PLLLC1_SSTWOPT_OVR_VAL_PREG	CMN_PLLLC1_SSTWOPT_OVR_VAL_PREG	
R/W-X					R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
CMN_PLLLC1_SSTWOPT_OVRVAL_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-197. CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	CMN_PLLLC1_DCOCAL_OVR_EN_PREG	R/W	0h	When asserted the cmnda_pll1c1_dcocal_ovren which drives the dcocal_ovren port on the PLLCMNLC1 is forced high. In addition the cmn_pll1c1_dcocal_ovrval_preg is forced onto cmnda_pll1c1_dcocal_ovrval which drives the dcocal_ovrval port on the PLLCMNLC1.
29-24	CMN_PLLLC1_DCOCAL_OVRVAL_PREG	R/W	0h	When cmnda_pll1c1_dcocal_ovren is asserted, this value is driven onto cmnda_pll1c1_dcocal_ovrval which drives the dcocal_ovrval port on the PLLCMNLC1.
23-22	RESERVED	R/W	X	
21-19	CMN_PLLLC1_DCO_ITRIM_PREG	R/W	3h	Drives the DCO trim current on the PLLCMNLC1.
18-16	CMN_PLLLC1_ROFFSET_PREG	R/W	3h	DCO tank offset resistor trim.

Table 11-197. CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-11	RESERVED	R/W	X	
10	CMN_PLLLC1_SSTWOP T_OVREN_PREG	R/W	0h	Drives the sstwopt_ovren port on the PLLCMNLC1.
9-0	CMN_PLLLC1_SSTWOP T_OVRVAL_PREG	R/W	0h	Drives the sstwopt_ovrval port on the PLLCMNLC1.

**Table 11-198. Register Call Summary for
CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_DCO_PREG__CMN_PLLLC1_SSTWOPT_OVR_PREG Register \(Offset = 1B0h\) \[reset = X\]: \[0\]](#)

11.66 CMN_PLLLCSM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG Register (Offset = 1B4h) [reset = X]

CMN_PLLLCSM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG is shown in Figure 11-66 and described in Table 11-200.

Return to [Summary Table](#).

PLLCMNLC1 debug and test avdd register.

Table 11-199. CMN_PLLLCSM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 01B4h
SERDES_16G1	0501 01B4h
SERDES_16G2	0502 01B4h
SERDES_16G3	0503 01B4h

Figure 11-66. CMN_PLLLCSM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG Register

31	30	29	28	27	26	25	24
RESERVED			CMN_PLLLCSM1_STATE				
R/W-X			R-B00h				
23	22	21	20	19	18	17	16
CMN_PLLLCSM1_STATE							
R-B00h							
15	14	13	12	11	10	9	8
RESERVED				CMN_PLLLC1_LFAVDDREG_VTRIM_PREG		CMN_PLLLC1_HFAVDDREG_VTRIM_PREG	
R/W-X				R/W-3h		R/W-3h	
7	6	5	4	3	2	1	0
CMN_PLLLC1_HFAVDDREG_VTRIM_PREG		CMN_PLLLC1_CLK1AVDDREG_VTRIM_PREG		CMN_PLLLC1_CLK0AVDDREG_VTRIM_PREG			
R/W-3h		R/W-3h		R/W-3h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-200. CMN_PLLLCSM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	CMN_PLLLCSM1_STATE	R	B00h	State machine state register.
15-12	RESERVED	R/W	X	
11-9	CMN_PLLLC1_LFAVDDREG_VTRIM_PREG	R/W	3h	Drives the lfavddreg_vtrim port on the PLLCMNLC1. Voltage 0 0.830 1 0.860 2 0.870 3 0.890 4 0.908 5 0.925 6 0.940 7 0.950

Table 11-200. CMN_PLLLCSM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-6	CMN_PLLLC1_HFAVDDR EG_VTRIM_PREG	R/W	3h	Drives the hfavddreg_vtrim port on the PLLCMNLC1. Voltage 0 0.830 1 0.860 2 0.870 3 0.890 4 0.908 5 0.925 6 0.940 7 0.950
5-3	CMN_PLLLC1_CLK1AVD DREG_VTRIM_PREG	R/W	3h	Drives the clk1avddreg_vtrim port on the PLLCMNLC1. Voltage 0 0.830 1 0.860 2 0.870 3 0.890 4 0.908 5 0.925 6 0.940 7 0.950
2-0	CMN_PLLLC1_CLK0AVD DREG_VTRIM_PREG	R/W	3h	Drives the clk0avddreg_vtrim port on the PLLCMNLC1. Voltage 0 0.830 1 0.860 2 0.870 3 0.890 4 0.908 5 0.925 6 0.940 7 0.950

Table 11-201. Register Call Summary for CMN_PLLLCSM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLCSM1_STATUS_PREG__CMN_PLLLC1_AVDD_PREG Register \(Offset = 1B4h\) \[reset = X\]: \[0\]](#)

11.67 CMN_PLLLCSM1_PLEN_TMR_PREG__CMN_PLLLCSM1_CTRL_PREG Register (Offset = 1B8h) [reset = X]

CMN_PLLLCSM1_PLEN_TMR_PREG__CMN_PLLLCSM1_CTRL_PREG is shown in Figure 11-67 and described in Table 11-203.

Return to [Summary Table](#).

PLLCMNLC1 Control State Machine Control register.

Table 11-202.
CMN_PLLLCSM1_PLEN_TMR_PREG__CMN_PLLLCSM1_CTRL_PREG
Instances

Instance	Physical Address
SERDES_16G0	0500 01B8h
SERDES_16G1	0501 01B8h
SERDES_16G2	0502 01B8h
SERDES_16G3	0503 01B8h

Figure 11-67. CMN_PLLLCSM1_PLEN_TMR_PREG__CMN_PLLLCSM1_CTRL_PREG Register

31	30	29	28	27	26	25	24
RESERVED				CMN_PLLLCSM1_PLEN_TMR_VAL_PREG			
R/W-X				R/W-32h			
23	22	21	20	19	18	17	16
CMN_PLLLCSM1_PLEN_TMR_VAL_PREG							
R/W-32h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			CMN_PLLLCSM1_FORCE_CAL_DONE_PREG	RESERVED			CMN_PLLLCSM1_SKIP_PLL_CAL_RECAL_PREG
R/W-X			R/W-0h	R/W-X			R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-203. CMN_PLLLCSM1_PLEN_TMR_PREG__CMN_PLLLCSM1_CTRL_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLCSM1_PLEN_TMR_VAL_PREG	R/W	32h	PLL enable state timer value : used for the timer when the PLL control state machine is in the PLL phase1 enable state. The value must be 1 or greater. This timer delay is specified in cmn_refclk periods.
15-5	RESERVED	R/W	X	
4	CMN_PLLLCSM1_FORCE_CAL_DONE_PREG	R/W	0h	Asserting this bit immediately advances the State Machine from the PLLSM_CAL state currently in or once entered.
3-1	RESERVED	R/W	X	

Table 11-203. CMN_PLLLCSM1_PLEN_TMR_PREG__CMN_PLLLCSM1_CTRL_PREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMN_PLLLCSM1_SKIP_PLL_CAL_RECAL_PREG	R/W	1h	Skip PLL calibration re-calibration enable : When this bit is active (1'b1), the PLL calibration state will be skipped if it was previously run, unless the cmn_pll_c_en has been deasserted, or the Macro reset.

**Table 11-204. Register Call Summary for
CMN_PLLLCSM1_PLEN_TMR_PREG__CMN_PLLLCSM1_CTRL_PREG**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLCSM1_PLEN_TMR_PREG__CMN_PLLLCSM1_CTRL_PREG Register \(Offset = 1B8h\) \[reset = X\]: \[0\]](#)

11.68 CMN_PLLLCSM1_PLLVREF_TMR_PREG__CMN_PLLLCSM1_PLLPRE_TMR_PREG Register (Offset = 1BCh) [reset = X]

CMN_PLLLCSM1_PLLVREF_TMR_PREG__CMN_PLLLCSM1_PLLPRE_TMR_PREG is shown in Figure 11-68 and described in Table 11-206.

Return to [Summary Table](#).

PLLCMNLC1 Control State Machine PLL pre-charge timer register.

Table 11-205.
CMN_PLLLCSM1_PLLVREF_TMR_PREG__CMN_PLLLCSM1_PLLPRE_TMR_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 01BCh
SERDES_16G1	0501 01BCh
SERDES_16G2	0502 01BCh
SERDES_16G3	0503 01BCh

Figure 11-68. CMN_PLLLCSM1_PLLVREF_TMR_PREG__CMN_PLLLCSM1_PLLPRE_TMR_PREG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CMN_PLLLCSM1_PLLVREF_TMR_VAL_PREG											
R/W-X				R/W-5h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CMN_PLLLCSM1_PLLPRE_TMR_VAL_PREG											
R/W-X				R/W-7Dh											

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-206. CMN_PLLLCSM1_PLLVREF_TMR_PREG__CMN_PLLLCSM1_PLLPRE_TMR_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CMN_PLLLCSM1_PLLVREF_TMR_VAL_PREG	R/W	5h	PLL pre-charge state timer value : used for the timer when the PLL control state machine is in the PLL vref state which includes releasing the PLLCMNLC1 reset. The value must be 1 or greater. This timer delay is specified in cmn_refclk periods.
15-12	RESERVED	R/W	X	
11-0	CMN_PLLLCSM1_PLLPRE_TMR_VAL_PREG	R/W	7Dh	PLL pre-charge state timer value : used for the timer when the PLL control state machine is in the PLL phase2 enable state. The value must be 1 or greater. This timer delay is specified in cmn_refclk periods.

Table 11-207. Register Call Summary for
CMN_PLLLCSM1_PLLVREF_TMR_PREG__CMN_PLLLCSM1_PLLPRE_TMR_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLCSM1_PLLVREF_TMR_PREG__CMN_PLLLCSM1_PLLPRE_TMR_PREG Register \(Offset = 1BCh\) \[reset = X\]: \[0\]](#)

11.69 CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG Register (Offset = 1C0h) [reset = X]

CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG is shown in [Figure 11-69](#) and described in [Table 11-209](#).

Return to [Summary Table](#).

PLLCMNLC1 clock2 register.

Table 11-208. CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 01C0h
SERDES_16G1	0501 01C0h
SERDES_16G2	0502 01C0h
SERDES_16G3	0503 01C0h

Figure 11-69. CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
CMN_PLLLC1_STATUS_C_BWCAL_CODE							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			CMN_PLLLC1_CLK2_EN_PREG	CMN_PLLLC1_CLK2OUTDIVFRAC_PREG			
R/W-X			R/W-0h	R/W-4h			
7	6	5	4	3	2	1	0
RESERVED	CMN_PLLLC1_CLK2OUTDIVINT_PREG						
R/W-X	R/W-4h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-209. CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	CMN_PLLLC1_STATUS_C_BWCAL_CODE	R	0h	PLLCMNLC1 Band Width calibration code result: Contains the calibration result. Bits7:5 - If_propcoef[2:0] calibration results Bits4:0 - If_propfrac[4:0] calibration results Note the contents of this register are not valid until cmn_plllc_locked Macro output is asserted. Note this register is for diagnostic purposes only.
15-13	RESERVED	R/W	X	
12	CMN_PLLLC1_CLK2_EN_PREG	R/W	0h	This value sets the clock2 enable value.

**Table 11-209. CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
11-8	CMN_PLLLC1_CLK2OUT DIVFRAC_PREG	R/W	4h	<p>his value sets the clock2 fractional output divider's fraction value:</p> <p>Fractional Value</p> <p>4'b0000 0</p> <p>4'b0001 1/2</p> <p>4'b0010 1/3</p> <p>4'b0011 2/3</p> <p>4'b0100 1/4</p> <p>4'b0101 1/2</p> <p>4'b0110 reserved</p> <p>4'b0111 3/4</p> <p>4'b1000 1/5</p> <p>4'b1001 reserved</p> <p>4'b1010 2/5</p> <p>4'b1011 3/5</p> <p>4'b1100 reserved</p> <p>4'b1101 3/5</p> <p>4'b1110 reserved</p> <p>4'b1111 4/5</p>
7	RESERVED	R/W	X	
6-0	CMN_PLLLC1_CLK2OUT DIVINT_PREG	R/W	4h	<p>This value sets the clock2 fractional output divider's integer value.</p> <p>The overall frequency is determined as:</p> $F_{clk2} = F_{vco} / (cmn_plllc1_clk2outdivint_preg + 4 + \text{fraction value})$ <p>where the fractional value is defined above in the description for cmn_plllc1_clk2outdivfrac_preg.</p>

Table 11-210. Register Call Summary for CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_STATUS_C_PREG__CMN_PLLLC1_CLK2_PREG Register \(Offset = 1C0h\) \[reset = X\]: \[0\]](#)

11.70 CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG Register (Offset = 1C4h) [reset = X]

CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG is shown in Figure 11-70 and described in Table 11-212.

Return to [Summary Table](#).

PLLCMNLC1 spread spectrum Time Step Size Mode register.

Table 11-211.
CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG Instances

Instance	Physical Address
SERDES_16G0	0500 01C4h
SERDES_16G1	0501 01C4h
SERDES_16G2	0502 01C4h
SERDES_16G3	0503 01C4h

Figure 11-70.

CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG Register

31	30	29	28	27	26	25	24
CMN_PLLLC1_LOCK_DELAY_CTRL_PREG_15_9							CMN_PLLLC1_LOCK_DELAY_PREG
R-0h							R/W-0h
23	22	21	20	19	18	17	16
CMN_PLLLC1_LOCK_DELAY_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	CMN_PLLLC1_SS_TIME_STEP_SIZE_MODE1_PREG						
R/W-X	R/W-8h						
7	6	5	4	3	2	1	0
RESERVED	CMN_PLLLC1_SS_TIME_STEP_SIZE_MODE0_PREG						
R/W-X	R/W-8h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-212.

CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	CMN_PLLLC1_LOCK_DELAY_CTRL_PREG_15_9	R	0h	reserved
24-16	CMN_PLLLC1_LOCK_DELAY_PREG	R/W	0h	This value sets a delay from internal lock assertion to assertion of cmn_pll_c_locked. delay = cmn_pll_c1_lock_delay_preg * 256 pfdclk periods.
15	RESERVED	R/W	X	
14-8	CMN_PLLLC1_SS_TIME_STEP_SIZE_MODE1_PREG	R/W	8h	This value sets the spread spectrum time step size value when cmn_pll_c_mode is asserted.
7	RESERVED	R/W	X	

Table 11-212.
CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG Register
Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	CMN_PLLLC1_SS_TIME_STEP_SIZE_MODE0_PREG	R/W	8h	This value sets the spread spectrum time step size value when cmn_plllic_mode is deasserted.

Table 11-213. Register Call Summary for
CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMN_PLLLC1_LOCK_DELAY_CTRL_PREG__CMN_PLLLC1_SS_TIME_STEPSIZE_MODE_PREG Register \(Offset = 1C4h\) \[reset = X\]: \[0\]](#)

11.71 MOD_VER Register (Offset = 400h) [reset = 69856002h]

MOD_VER is shown in [Figure 11-71](#) and described in [Table 11-215](#).

[Return to Summary Table.](#)

The Module and Version Register identifies the module identifier and revision of the WIZ module.

Table 11-214. MOD_VER Instances

Instance	Physical Address
SERDES_16G0	0500 0400h
SERDES_16G1	0501 0400h
SERDES_16G2	0502 0400h
SERDES_16G3	0503 0400h

Figure 11-71. MOD_VER Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R-1h		R-2h		R-985h			
23	22	21	20	19	18	17	16
MODULE_ID							
R-985h							
15	14	13	12	11	10	9	8
RTL_VERSION					MAJOR_REVISION		
R-Ch					R-0h		
7	6	5	4	3	2	1	0
CUSTOM_REVISION		MINOR_REVISION					
R-0h		R-2h					

LEGEND: R = Read Only; -n = value after reset

Table 11-215. MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Module Scheme
29-28	BU	R	2h	Module BU
27-16	MODULE_ID	R	985h	Module ID.
15-11	RTL_VERSION	R	Ch	RTL Version.
10-8	MAJOR_REVISION	R	0h	Major Revision.
7-6	CUSTOM_REVISION	R	0h	Custom Revision.
5-0	MINOR_REVISION	R	2h	Minor Revision.

Table 11-216. Register Call Summary for MOD_VER

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [MOD_VER Register \(Offset = 400h\) \[reset = 69856002h\]: \[0\]](#)

11.72 SERDES_CTRL Register (Offset = 404h) [reset = X]

SERDES_CTRL is shown in [Figure 11-72](#) and described in [Table 11-218](#).

Return to [Summary Table](#).

Sets the SERDES control state.

Table 11-217. SERDES_CTRL Instances

Instance	Physical Address
SERDES_16G0	0500 0404h
SERDES_16G1	0501 0404h
SERDES_16G2	0502 0404h
SERDES_16G3	0503 0404h

Figure 11-72. SERDES_CTRL Register

31	30	29	28	27	26	25	24
POR_EN	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-218. SERDES_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POR_EN	R/W	0h	The por_en allows the system to place the SERDES in a reset state, Access to the SERDES registers are ignored.
30-0	RESERVED	R/W	X	

Table 11-219. Register Call Summary for SERDES_CTRL

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SERDES_CTRL Register \(Offset = 404h\) \[reset = X\]: \[0\]](#)

11.73 SERDES_TOP_CTRL Register (Offset = 408h) [reset = X]

SERDES_TOP_CTRL is shown in Figure 11-73 and described in Table 11-221.

Return to [Summary Table](#).

The SERDES Top Level Control

Table 11-220. SERDES_TOP_CTRL Instances

Instance	Physical Address
SERDES_16G0	0500 0408h
SERDES_16G1	0501 0408h
SERDES_16G2	0502 0408h
SERDES_16G3	0503 0408h

Figure 11-73. SERDES_TOP_CTRL Register

31	30	29	28	27	26	25	24
PMA_CMN_REFCLK_MODE	PMA_CMN_REFCLK_INT_MODE			PMA_CMN_REFCLK_DIG_DIV		PMA_CMN_REFCLK1_DIG_DIV	
R/W-0h	R/W-0h			R/W-2h		R/W-2h	
23	22	21	20	19	18	17	16
PHY_PMA_SU SPEND_OVER RIDE	RESERVED						
R/W-0h	R/W-X						
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-221. SERDES_TOP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PMA_CMN_REFCLK_MODE	R/W	0h	The PMA common differential reference clock mode - Sets the mode of operation for differential reference clock input. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 2'b 00 - 100 MHz and greater differential reference clock. 2'b 01 - 100 MHz and greater singled ended DC coupled test reference clock. 2'b 10 - Less than 100 MHz differential reference clock. 2'b 11 - Less than 100 MHz single ended DC coupled test reference clock.
29-28	PMA_CMN_REFCLK_INT_MODE	R/W	0h	The PMA common internal reference clock mode - Sets the mode of operation for internal reference clock input. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 2'b 00 - Reserved 2'b 01 - 100 MHz and greater reference clock 2'b 10 - Reserved 2'b 11 - Less than 100 MHz reference clock

Table 11-221. SERDES_TOP_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-26	PMA_CMN_REFCLK_DIG_DIV	R/W	2h	The PMA common reference clock digital divide ratio select - Must be set before the de-assertion of apb_preset_n/phy_reset_n. 2'b 00 - Divide by 1 (set for reference clock in the 19.2 to 27MHz range) 2'b 01 - Divide by 2 (Reserved) 2'b 10 - Divide by 4 (set for 100 MHz reference clock) 2'b 11 - Divide by 8 (set for 156.25MHz reference clock)
25-24	PMA_CMN_REFCLK1_DIG_DIV	R/W	2h	The Alternate reference clock digital divide select - Selects digital divide ratio for alternate reference clock coming from analog (see PMA specification for use) 2'b 00 - Divide by 1 2'b 01 - Divide by 2 2'b 10 - Divide by 4 2'b 11 - Divide by 8
23	PHY_PMA_SUSPEND_OVERRIDE	R/W	0h	The PHY PMA common suspend override enable: 1 = disables suspending the PMA common when all links are in low power state (L1 SS, PCIe P2, USB P3, power down disabled, etc.). 0 = PMA common will be suspended when all links are in low power state. Driving this pin high has no effect if the PMA common is already suspended or is in the process of being suspended (i.e. it will not force the PMA common to resume). It only prevents the start of suspending the PMA common. However, if this pin is de-asserted when all links are in low power state, the PMA common will then be suspended.
22-0	RESERVED	R/W	X	

Table 11-222. Register Call Summary for SERDES_TOP_CTRL

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SERDES_TOP_CTRL Register \(Offset = 408h\) \[reset = X\]: \[0\]](#)

11.74 SERDES_RST Register (Offset = 40Ch) [reset = X]

SERDES_RST is shown in Figure 11-74 and described in Table 11-224.

Return to [Summary Table](#).

The SERDES Reset Register controls the Phy reset and REFCLK selection for the SERDES.

Table 11-223. SERDES_RST Instances

Instance	Physical Address
SERDES_16G0	0500 040Ch
SERDES_16G1	0501 040Ch
SERDES_16G2	0502 040Ch
SERDES_16G3	0503 040Ch

Figure 11-74. SERDES_RST Register

31	30	29	28	27	26	25	24
PHY_RESET_N	PHY_EN_REFCLK	PLL1_REFCLK_SEL	PLL0_REFCLK_SEL	REFCLK_TERM_DIS	RESERVED	REFCLK_DIG_SEL	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h	
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-224. SERDES_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_RESET_N	R/W	0h	The PHY reset : Asserting this signal low will reset all PHY logic for the entire PHY with the exception of the APB registers and TAP controller. Note: Upon de-assertion, all PHY inputs must be driven as described in the PIPE specification for a PIPE reset.
30	PHY_EN_REFCLK	R/W	0h	The PHY reference clock enable: When cmn_refclk_<p/m> is configured as a reference clock output, 1 = glitch-less enable of the reference clock output. 0 = glitch-less turn off reference clock output. Used in L1.x entry/exit protocol. Note: When outputting a derived reference clock from the PLL, it is recommended to drive phy_en_refclk low until the PHY has completed start-up and de-asserted pipe_l*_reset_n for PIPE operation or asserted cmn_ready for Raw SERDES operation.. The clock will not be 'good' until the PHY has completed initial start-up.

Table 11-224. SERDES_RST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	PLL1_REFCLK_SEL	R/W	0h	The PMA common PLL1 reference clock source select - 0 - Selects cmn_refclk1_<m/p> as reference clock source 1 - Selects cmn_refclk1_int as reference clock source. Note: This field is write protected when register field PHY_RESET_N is a '1'.
28	PLL0_REFCLK_SEL	R/W	0h	The PMA common PLL0 reference clock source select - 0 - Selects cmn_refclk_<m/p> as reference clock source 1 - Selects cmn_refclk_int as reference clock source. Note: This field is write protected when register field PHY_RESET_N is a '1'.
27	REFCLK_TERM_DIS	R/W	0h	The PMA common differential reference clock termination disable - enables/disables termination for difference reference clock input (cmn_refclk_<p/m>). Must be set before the de-assertion of apb_preset_n/phy_reset_n. 1 = termination disabled 0 = termination enabled. Note: This field is write protected when register field PHY_RESET_N is a '1'.
26	RESERVED	R/W	X	
25-24	REFCLK_DIG_SEL	R/W	0h	The Reference clock digital source select - Selects the reference clock source for the reference clock used in the PHY and PMA digital logic. 2'b 00 - cmn_refclk_<p/m> 2'b 01 - cmn_refclk_int 2'b 10 - cmn_refclk1_<p/m> 2'b 11 - cmn_refclk1_int. Note: This field is write protected when register field PHY_RESET_N is a '1'.
23-0	RESERVED	R/W	X	

Table 11-225. Register Call Summary for SERDES_RST

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SERDES_RST Register \(Offset = 40Ch\) \[reset = X\]: \[0\]](#)

11.75 SERDES_TYPEC Register (Offset = 410h) [reset = X]

SERDES_TYPEC is shown in [Figure 11-75](#) and described in [Table 11-227](#).

Return to [Summary Table](#).

The SERDES Type C control register allows the external lanes selection to be swapped.

Table 11-226. SERDES_TYPEC Instances

Instance	Physical Address
SERDES_16G0	0500 0410h
SERDES_16G1	0501 0410h
SERDES_16G2	0502 0410h
SERDES_16G3	0503 0410h

Figure 11-75. SERDES_TYPEC Register

31	30	29	28	27	26	25	24
RESERVED	LN10_SWAP	RESERVED					
R/W-X	R/W-0h	R/W-X					
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-227. SERDES_TYPEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	LN10_SWAP	R/W	0h	The LN10_SWAP will swap the lanes 0 and 1. That is all control for lane 0 will apply to lane 1 and vice versa. You cannot set LN10_SWAP to swap lanes in a link. That is, if lanes 0 and 1 are used for a single link of PCIe, the LN10_SWAP must be '0'. Note: This field is write protected when register field PHY_RESET_N is a '1'.
29-0	RESERVED	R/W	X	

Table 11-228. Register Call Summary for SERDES_TYPEC

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SERDES_TYPEC Register \(Offset = 410h\) \[reset = X\]: \[0\]](#)

11.76 SERDES_CORE_STATUS Register (Offset = 414h) [reset = X]

SERDES_CORE_STATUS is shown in Figure 11-76 and described in Table 11-230.

Return to [Summary Table](#).

The contains SERDES core power state status.

Table 11-229. SERDES_CORE_STATUS Instances

Instance	Physical Address
SERDES_16G0	0500 0414h
SERDES_16G1	0501 0414h
SERDES_16G2	0502 0414h
SERDES_16G3	0503 0414h

Figure 11-76. SERDES_CORE_STATUS Register

31	30	29	28	27	26	25	24
MACRO_PWR_EN_ACK	RESERVED						
R-0h				R-X			
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							
R-X							

LEGEND: R = Read Only; -n = value after reset

Table 11-230. SERDES_CORE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MACRO_PWR_EN_ACK	R	0h	SERDES macro_power enable acknowledgment - This signal is asserted high, upon completion of the power on sequence in the SERDES. Upon assertion, digital power islands are enabled and apb_preset_n can be de-asserted. If this stays '0' it may be that there is no REFCLK input based on the REFCLK selection controls.
30-0	RESERVED	R	X	

Table 11-231. Register Call Summary for SERDES_CORE_STATUS

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SERDES_CORE_STATUS Register \(Offset = 414h\) \[reset = X\]: \[0\]](#)

11.77 LANECTLO Register (Offset = 480h) [reset = X]

LANECTLO is shown in [Figure 11-77](#) and described in [Table 11-233](#).

Return to [Summary Table](#).

The Lane Control Register sets the lane specific modes of operation.

Table 11-232. LANECTLO Instances

Instance	Physical Address
SERDES_16G0	0500 0480h
SERDES_16G1	0501 0480h
SERDES_16G2	0502 0480h
SERDES_16G3	0503 0480h

Figure 11-77. LANECTLO Register

31	30	29	28	27	26	25	24
P0_ENABLE	P0_FORCE_ENABLE	P0_ALIGN	P0_RAW_AUTO_START	RESERVED		P0_STANDARD_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h	
23	22	21	20	19	18	17	16
P0_FULLRT_DIV		P0_MAC_SRC_SEL		P0_REFCLK_SEL		P0_OVR_SRC_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RESERVED	P0_OVR_DIV_SEL			P0_SUBCLK_SEL		P0_TXFCLK_SEL	
R/W-X	R/W-0h			R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
P0_RXFCLK_SEL		RESERVED					
R/W-0h		R/W-X					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-233. LANECTLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P0_ENABLE	R/W	0h	The P0_ENABLE is AND'ed with the IPx_LNy_reset_n to enable the lane.
30	P0_FORCE_ENABLE	R/W	0h	The P0_FORCE_ENABLE is OR'ed with the IPx_LNy_reset_n to force enable the lane.
29	P0_ALIGN	R/W	0h	The P0_ALIGN will auto align the RAW interface to 8B10B comma characters.
28	P0_RAW_AUTO_START	R/W	0h	The P0_RAW_AUTO_START will auto sequence the RAW interface according to the configuration settings
27-26	RESERVED	R/W	X	
25-24	P0_STANDARD_MODE	R/W	0h	Standard Mode
23-22	P0_FULLRT_DIV	R/W	0h	Full Rate divider for 2x MAC speed mode. The PMA PLL full rate clock divider select - divide ratio for pma_pllclk_fullrt_in_*. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8

Table 11-233. LANECTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	P0_MAC_SRC_SEL	R/W	0h	MAC clock source select: Selects which PMA clock to use as clock source for pcs_mac_clk*_ln_0 signals. 2'b 00 - cmn_pll1c_digclk2 2'b 01 - cmn_pll1c1_digclk2 2'b 10 - xcvr_pllclk_datart_ln_* (for master lane of link) 2'b 11 - xcvr_pllclk_fullrt_ln_* (for master lane of link)
19-18	P0_REFCLK_SEL	R/W	0h	Refclk Select determines which clocks will be used for the IP refclk signal. 0 - pcs_sub_clk_0 is used. 1 - pcs_mac_clk_ln_0 is used. 2 - pcs_mac_clk_divx0_ln_0 is used. 3 - pcs_mac_clk_divx1_ln_0 is used.
17-16	P0_OVR_SRC_SEL	R/W	0h	Oversample clock source select: Selects which PMA clock to use as clock source for pcs_ovr_clk*_ln_0. 2'b 00 = cmn_pll1c_digclk1 2'b 01 = cmn_pll1c1_digclk1 2'b1x = xcvr_pllclk_fullrt_ln_0 (for master lane of link)
15	RESERVED	R/W	X	
14-12	P0_OVR_DIV_SEL	R/W	0h	Oversample clock divider ratio select: Selects the divider ratio for pcs_ovr_clk_divx_ln_0. 3'd 0: Reserved 3'd 1: Divide by 1 3'd 2: Divide by 2 3'd 3: Divide by 3 ... 3'd 7: Divide by 7
11-10	P0_SUBCLK_SEL	R/W	0h	Selects which clock sources pcs_sub_clk_0. 0 - pma_pllclk_fullrt_ln_0 is used to source pcs_sub_clk_0. 1 - pcs_ovr_clk_ln_0 is used to source pcs_sub_clk_0. 2 - pcs_ovr_clk_divx_ln_0 is used to source pcs_sub_clk_0. 3 - pma_pllclk_fullrt_ln_0 is used to source pcs_sub_clk_0.
9-8	P0_TXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP txfclk signal. 0 - pcs_sub_clk_0 is used. 1 - pcs_mac_clk_ln_0 is used. 2 - pcs_mac_clk_divx0_ln_0 is used. 3 - pcs_mac_clk_divx1_ln_0 is used.
7-6	P0_RXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP rxfclk signal. 0 - pma_rx_rd10_clk_ln_0 is used. 1 - pma_rx_rd_clk_ln_0 is used. 2 - rd_div2_clk0 is used. 3 - rd_div4_clk0 is used.
5-0	RESERVED	R/W	X	

Table 11-234. Register Call Summary for LANECTL0

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANECTL0 Register \(Offset = 480h\) \[reset = X\]: \[0\]](#)

11.78 LANEDIV0 Register (Offset = 484h) [reset = X]

LANEDIV0 is shown in [Figure 11-78](#) and described in [Table 11-236](#).

Return to [Summary Table](#).

The Lane Divider Register sets the lane specific dividers of

Table 11-235. LANEDIV0 Instances

Instance	Physical Address
SERDES_16G0	0500 0484h
SERDES_16G1	0501 0484h
SERDES_16G2	0502 0484h
SERDES_16G3	0503 0484h

Figure 11-78. LANEDIV0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									P0_MAC_DIV_SEL0						
R/W-X									R/W-0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									P0_MAC_DIV_SEL1						
R/W-X									R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-236. LANEDIV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	P0_MAC_DIV_SEL0	R/W	0h	The reg_p0_mac_div_sel0 controls the divider for lane 0 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx0_ln_*. 7'd 0 : Reserved 7'd 1 : Divide by 1 7'd 2 : Divide by 2 7'd 3 : Divide by 3 ... 7'd n : Divide by n n = 127 (maximum)
15-9	RESERVED	R/W	X	
8-0	P0_MAC_DIV_SEL1	R/W	0h	The reg_p0_mac_div_sel1 controls the divider for lane 0 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx1_ln_*. 9'd 0 : Reserved 9'd 1 : Divide by 1 9'd 2 : Divide by 2 9'd 3 : Divide by 3 ... 9'd n : Divide by n n = 511 (maximum)

Table 11-237. Register Call Summary for LANEDIV0

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANEDIV0 Register \(Offset = 484h\) \[reset = X\]: \[0\]](#)

11.79 LANALIGN0 Register (Offset = 488h) [reset = X]

LANALIGN0 is shown in [Figure 11-79](#) and described in [Table 11-239](#).

Return to [Summary Table](#).

The Lane Align reports the 8B10B alignment delay from the Comma aligner when 8B10B protocol is used in RAW mode.

Table 11-238. LANALIGN0 Instances

Instance	Physical Address
SERDES_16G0	0500 0488h
SERDES_16G1	0501 0488h
SERDES_16G2	0502 0488h
SERDES_16G3	0503 0488h

Figure 11-79. LANALIGN0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										P0_ALIGN_RX_DELAY					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 11-239. LANALIGN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	P0_ALIGN_RX_DELAY	R	0h	The reg_p0_align_rx_delay indicates the number of bits that are added to align the data to an 8B10B alignment. This value should be added to the latency of the receiver so that an accurate time of Time Sync packets can be calculated.

Table 11-240. Register Call Summary for LANALIGN0

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANALIGN0 Register \(Offset = 488h\) \[reset = X\]: \[0\]](#)

11.80 LANESTS0 Register (Offset = 48Ch) [reset = X]

LANESTS0 is shown in [Figure 11-80](#) and described in [Table 11-242](#).

Return to [Summary Table](#).

The lane Status reports the lane state information for debug purposes.

Table 11-241. LANESTS0 Instances

Instance	Physical Address
SERDES_16G0	0500 048Ch
SERDES_16G1	0501 048Ch
SERDES_16G2	0502 048Ch
SERDES_16G3	0503 048Ch

Figure 11-80. LANESTS0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						P0_MASTER	P0_PWR_EN_ACK
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-242. LANESTS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	P0_MASTER	R	0h	The reg_p0_master indicates the lane is a base lane for a multi lane link. When '1' Lane is lane 0 of a multi lane link, When '0' lane is part of a multi lane link.
0	P0_PWR_EN_ACK	R	0h	The reg_p0_pwr_en_ack SERDES lane power enable acknowledgment - This signal is asserted high, upon completion of the power on sequence in each PMA transceiver link (per-link/shared signal). Upon assertion, link registers can be written and phy_IX_reset_n can be de-asserted.

Table 11-243. Register Call Summary for LANESTS0

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANESTS0 Register \(Offset = 48Ch\) \[reset = X\]: \[0\]](#)

11.81 LANECTL1 Register (Offset = 4C0h) [reset = X]

LANECTL1 is shown in [Figure 11-81](#) and described in [Table 11-245](#).

Return to [Summary Table](#).

The Lane Control Register sets the lane specific modes of operation.

Table 11-244. LANECTL1 Instances

Instance	Physical Address
SERDES_16G0	0500 04C0h
SERDES_16G1	0501 04C0h
SERDES_16G2	0502 04C0h
SERDES_16G3	0503 04C0h

Figure 11-81. LANECTL1 Register

31	30	29	28	27	26	25	24
P1_ENABLE	P1_FORCE_ENABLE	P1_ALIGN	P1_RAW_AUTO_START	RESERVED		P1_STANDARD_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h	
23	22	21	20	19	18	17	16
P1_FULLRT_DIV		P1_MAC_SRC_SEL		P1_REFCLK_SEL		P1_OVR_SRC_SEL	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RESERVED	P1_OVR_DIV_SEL			P1_SUBCLK_SEL		P1_TXFCLK_SEL	
R/W-X	R/W-0h			R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
P1_RXFCLK_SEL		RESERVED					
R/W-0h		R/W-X					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-245. LANECTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P1_ENABLE	R/W	0h	The p1_enable is AND'd with the IPx_LNy_reset_n to enable the lane.
30	P1_FORCE_ENABLE	R/W	0h	The p1_force_enable is OR'd with the IPx_LNy_reset_n to force enable the lane.
29	P1_ALIGN	R/W	0h	The p1_align will auto align the RAW interface to 8B10B comma characters.
28	P1_RAW_AUTO_START	R/W	0h	The p1_raw_auto_start will auto sequence the RAW interface according to the configuration settings
27-26	RESERVED	R/W	X	
25-24	P1_STANDARD_MODE	R/W	0h	Standard Mode
23-22	P1_FULLRT_DIV	R/W	0h	Full Rate divider for 2x MAC speed mode. The PMA PLL full rate clock divider select - divide ratio for pma_pllclk_fullrt_ln_*. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8

Table 11-245. LANECTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	P1_MAC_SRC_SEL	R/W	0h	MAC clock source select: Selects which PMA clock to use as clock source for pcs_mac_clk*_ln_1 signals. 2'b 00 - cmn_pll1c_digclk2 2'b 01 - cmn_pll1c1_digclk2 2'b 10 - xcvr_pllclk_datart_ln_* (for master lane of link) 2'b 11 - xcvr_pllclk_fullrt_ln_* (for master lane of link)
19-18	P1_REFCLK_SEL	R/W	0h	Refclk Select determines which clocks will be used for the IP refclk signal. 0 - pcs_sub_clk_1 is used. 1 - pcs_mac_clk_ln_1 is used. 2 - pcs_mac_clk_divx0_ln_1 is used. 3 - pcs_mac_clk_divx1_ln_1 is used.
17-16	P1_OVR_SRC_SEL	R/W	0h	Oversample clock source select: Selects which PMA clock to use as clock source for pcs_ovr_clk*_ln_1. 2'b 00 = cmn_pll1c_digclk1 2'b 01 = cmn_pll1c1_digclk1 2'b 1x = xcvr_pllclk_fullrt_ln_1 (for master lane of link)
15	RESERVED	R/W	X	
14-12	P1_OVR_DIV_SEL	R/W	0h	Oversample clock divider ratio select: Selects the divider ratio for pcs_ovr_clk_divx_ln_1. 3'd 0: Reserved 3'd 1: Divide by 1 3'd 2: Divide by 2 3'd 3: Divide by 3 ... 3'd 7: Divide by 7
11-10	P1_SUBCLK_SEL	R/W	0h	Selects which clock sources pcs_sub_clk_1. 0 - pma_pllclk_fullrt_ln_1 is used to source pcs_sub_clk_1. 1 - pcs_ovr_clk_ln_1 is used to source pcs_sub_clk_1. 2 - pcs_ovr_clk_divx_ln_1 is used to source pcs_sub_clk_1. 3 - pma_pllclk_fullrt_ln_1 is used to source pcs_sub_clk_1.
9-8	P1_TXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP txfclk signal. 0 - pcs_sub_clk_1 is used. 1 - pcs_mac_clk_ln_1 is used. 2 - pcs_mac_clk_divx0_ln_1 is used. 3 - pcs_mac_clk_divx1_ln_1 is used.
7-6	P1_RXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP rxfclk signal. 0 - pma_rx_rd10_clk_ln_1 is used. 1 - pma_rx_rd_clk_ln_1 is used. 2 - rd_div2_clk1 is used. 3 - rd_div4_clk1 is used.
5-0	RESERVED	R/W	X	

Table 11-246. Register Call Summary for LANECTL1

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANECTL1 Register \(Offset = 4C0h\) \[reset = X\]: \[0\]](#)

11.82 LANEDIV1 Register (Offset = 4C4h) [reset = X]

LANEDIV1 is shown in [Figure 11-82](#) and described in [Table 11-248](#).

Return to [Summary Table](#).

The Lane Divider Register sets the lane specific dividers of

Table 11-247. LANEDIV1 Instances

Instance	Physical Address
SERDES_16G0	0500 04C4h
SERDES_16G1	0501 04C4h
SERDES_16G2	0502 04C4h
SERDES_16G3	0503 04C4h

Figure 11-82. LANEDIV1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									P1_MAC_DIV_SEL0						
R/W-X									R/W-0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									P1_MAC_DIV_SEL1						
R/W-X									R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-248. LANEDIV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	P1_MAC_DIV_SEL0	R/W	0h	The reg_p1_mac_div_sel0 controls the divider for lane 1 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx0_ln_*. 7'd 0 : Reserved 7'd 1 : Divide by 1 7'd 2 : Divide by 2 7'd 3 : Divide by 3 ... 7'd n : Divide by n n = 127 (maximum)
15-9	RESERVED	R/W	X	
8-0	P1_MAC_DIV_SEL1	R/W	0h	The reg_p1_mac_div_sel1 controls the divider for lane 1 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx1_ln_*. 9'd 0 : Reserved 9'd 1 : Divide by 1 9'd 2 : Divide by 2 9'd 3 : Divide by 3 ... 9'd n : Divide by n n = 511 (maximum)

Table 11-249. Register Call Summary for LANEDIV1

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANEDIV1 Register \(Offset = 4C4h\) \[reset = X\]: \[0\]](#)

11.83 LANALIGN1 Register (Offset = 4C8h) [reset = X]

LANALIGN1 is shown in [Figure 11-83](#) and described in [Table 11-251](#).

Return to [Summary Table](#).

The Lane Align reports the 8B10B alignment delay from the Comma aligner when 8B10B protocol is used in RAW mode.

Table 11-250. LANALIGN1 Instances

Instance	Physical Address
SERDES_16G0	0500 04C8h
SERDES_16G1	0501 04C8h
SERDES_16G2	0502 04C8h
SERDES_16G3	0503 04C8h

Figure 11-83. LANALIGN1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										P1_ALIGN_RX_DELAY					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 11-251. LANALIGN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	P1_ALIGN_RX_DELAY	R	0h	The reg_p1_align_rx_delay indicates the number of bits that are added to align the data to an 8B10B alignment. This value should be added to the latency of the receiver so that an accurate time of Time Sync packets can be calculated.

Table 11-252. Register Call Summary for LANALIGN1

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANALIGN1 Register \(Offset = 4C8h\) \[reset = X\]: \[0\]](#)

11.84 LANESTS1 Register (Offset = 4CCh) [reset = X]

LANESTS1 is shown in [Figure 11-84](#) and described in [Table 11-254](#).

Return to [Summary Table](#).

The lane Status reports the lane state information for debug purposes.

Table 11-253. LANESTS1 Instances

Instance	Physical Address
SERDES_16G0	0500 04CCh
SERDES_16G1	0501 04CCh
SERDES_16G2	0502 04CCh
SERDES_16G3	0503 04CCh

Figure 11-84. LANESTS1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						P1_MASTER	P1_PWR_EN_ACK
R-X						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-254. LANESTS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	P1_MASTER	R	0h	The reg_p1_master indicates the lane is a base lane for a multi lane link. When '1' Lane is lane 0 of a multi lane link, When '0' lane is part of a multi lane link.
0	P1_PWR_EN_ACK	R	0h	The reg_p1_pwr_en_ack SERDES lane power enable acknowledgment - This signal is asserted high, upon completion of the power on sequence in each PMA transceiver link (per-link/shared signal). Upon assertion, link registers can be written and phy_IX_reset_n can be de-asserted.

Table 11-255. Register Call Summary for LANESTS1

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANESTS1 Register \(Offset = 4CCh\) \[reset = X\]: \[0\]](#)

11.85 RES_CAL Register (Offset = 5F4h) [reset = X]

RES_CAL is shown in Figure 11-85 and described in Table 11-257.

Return to [Summary Table](#).

The Resistor Calibration register is used to allow the elimination of the external resistor on multiple macros.

Table 11-256. RES_CAL Instances

Instance	Physical Address
SERDES_16G0	0500 05F4h
SERDES_16G1	0501 05F4h
SERDES_16G2	0502 05F4h
SERDES_16G3	0503 05F4h

Figure 11-85. RES_CAL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PMA_CMN_RESCAL_CODE_OUT					
R/W-X		R-0h					
15	14	13	12	11	10	9	8
RESERVED							PMA_CMN_RESCAL_INSEL
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		PMA_CMN_RESCAL_CODE_IN					
R/W-X		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-257. RES_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PMA_CMN_RESCAL_CODE_OUT	R	0h	This is the current value of the pma_cmn_rescal_code_out from the SERDES, and can be used to set pma_cmn_rescal_code_in for other macros.
15-9	RESERVED	R/W	X	
8	PMA_CMN_RESCAL_INSEL	R/W	0h	Common resistor calibration selection - 0 = the PMA's resistor calibration result is used. 1 = the value on cmn_rescal_code_in is used. Note: This field is write protected when register field PHY_RESET_N is a '1'.
7-6	RESERVED	R/W	X	
5-0	PMA_CMN_RESCAL_CODE_IN	R/W	0h	External common resistor calibration result - Resistor calibration result from another Serdes PCIe PHY. Note: pma_cmn_ready for the driving PHY must be asserted prior to releasing pipe_reset_n. Use of this input eliminates the need for the cmn_rext bump on this PHY. Note: This field is write protected when register field PHY_RESET_N is a '1'.

Table 11-258. Register Call Summary for RES_CAL

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RES_CAL Register \(Offset = 5F4h\) \[reset = X\]: \[0\]](#)

11.86 DIAG_TEST Register (Offset = 5FCh) [reset = 0h]

DIAG_TEST is shown in [Figure 11-86](#) and described in [Table 11-260](#).

Return to [Summary Table](#).

The Diagnostic Test Register allows the system to validate the read and write of all data bits.

Table 11-259. DIAG_TEST Instances

Instance	Physical Address
SERDES_16G0	0500 05FCh
SERDES_16G1	0501 05FCh
SERDES_16G2	0502 05FCh
SERDES_16G3	0503 05FCh

Figure 11-86. DIAG_TEST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIAG_REG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-260. DIAG_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIAG_REG	R/W	0h	Diagnostic register. This register allows full read/write of all data bits to be tested.

Table 11-261. Register Call Summary for DIAG_TEST

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DIAG_TEST Register \(Offset = 5FCh\) \[reset = 0h\]: \[0\]](#)

11.87 RESERVEDBIT13ADDRESSA_y Register (Offset = 2000h + formula) [reset = 0h]

RESERVEDBIT13ADDRESSA_y is shown in [Figure 11-87](#) and described in [Table 11-263](#).

Return to [Summary Table](#).

Reserved Address bit 13 area A

Offset = 2000h + (y * 4h); where y = 0h to 7FFh

Table 11-262. RESERVEDBIT13ADDRESSA_y Instances

Instance	Physical Address
SERDES_16G0	0500 2000h + formula
SERDES_16G1	0501 2000h + formula
SERDES_16G2	0502 2000h + formula
SERDES_16G3	0503 2000h + formula

Figure 11-87. RESERVEDBIT13ADDRESSA_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES_BIT13_ADR_A																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-263. RESERVEDBIT13ADDRESSA_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES_BIT13_ADR_A	R/W	0h	Write only test region A

Table 11-264. Register Call Summary for RESERVEDBIT13ADDRESSA_y

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RESERVEDBIT13ADDRESSA_y Register \(Offset = 2000h + formula\) \[reset = 0h\]: \[0\]](#)

11.88 DET_STANDEC_B_PREG_DET_STANDEC_A_PREG_j Register (Offset = 4000h + formula) [reset = X]

DET_STANDEC_B_PREG_DET_STANDEC_A_PREG_j is shown in Figure 11-88 and described in Table 11-266.

Return to [Summary Table](#).

Standard decoder register A.

Offset = 4000h + (j * 400h); where j = 0h to 1h

Table 11-265. DET_STANDEC_B_PREG_DET_STANDEC_A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4000h + formula
SERDES_16G1	0501 4000h + formula
SERDES_16G2	0502 4000h + formula
SERDES_16G3	0503 4000h + formula

Figure 11-88. DET_STANDEC_B_PREG_DET_STANDEC_A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				DEQ_TXPOST TRAINEN_MO DE3_PREG	DEQ_TXPOST TRAINEN_MO DE2_PREG	DEQ_TXPOST TRAINEN_MO DE1_PREG	DEQ_TXPOST TRAINEN_MO DE0_PREG
R/W-X				R/W-1h	R/W-1h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DEQ_TXPRET RAINEN_MOD E3_PREG	DEQ_TXPRET RAINEN_MOD E2_PREG	DEQ_TXPRET RAINEN_MOD E1_PREG	DEQ_TXPRET RAINEN_MOD E0_PREG	DEQ_CLOSED EYE_SEL_MO DE3_PREG	DEQ_CLOSED EYE_SEL_MO DE2_PREG	DEQ_CLOSED EYE_SEL_MO DE1_PREG	DEQ_CLOSED EYE_SEL_MO DE0_PREG
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DRVCTRL_ED GEBOOST_EN _MODE3_PRE G	DRVCTRL_ED GEBOOST_EN _MODE2_PRE G	DRVCTRL_ED GEBOOST_EN _MODE1_PRE G	DRVCTRL_ED GEBOOST_EN _MODE0_PRE G	TX_DEEMPHA SIS_CTRL_SEL _MODE3_PRE G	TX_DEEMPHA SIS_CTRL_SEL _MODE2_PRE G	TX_DEEMPHA SIS_CTRL_SEL _MODE1_PRE G	TX_DEEMPHA SIS_CTRL_SEL _MODE0_PRE G
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
DRV_IDLE_LO WZ_MODE3_P REG	DRV_IDLE_LO WZ_MODE2_P REG	DRV_IDLE_LO WZ_MODE1_P REG	DRV_IDLE_LO WZ_MODE0_P REG	SER_GT8G_M ODE3_PREG	SER_GT8G_M ODE2_PREG	SER_GT8G_M ODE1_PREG	SER_GT8G_M ODE0_PREG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-266. DET_STANDEC_B_PREG_DET_STANDEC_A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27	DEQ_TXPOSTTRAINEN_MODE3_PREG	R/W	1h	This value sets the deq_txposttrainen from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.
26	DEQ_TXPOSTTRAINEN_MODE2_PREG	R/W	1h	This value sets the deq_txposttrainen from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010.
25	DEQ_TXPOSTTRAINEN_MODE1_PREG	R/W	0h	This value sets the deq_txposttrainen from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001.
24	DEQ_TXPOSTTRAINEN_MODE0_PREG	R/W	0h	This value sets the deq_txposttrainen from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000.

**Table 11-266. DET_STANDEC_B_PREG_DET_STANDEC_A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
23	DEQ_TXPRETRAINEN_MODE3_PREG	R/W	1h	This value sets the deq_txpretrainen from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011.
22	DEQ_TXPRETRAINEN_MODE2_PREG	R/W	1h	This value sets the deq_txpretrainen from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010.
21	DEQ_TXPRETRAINEN_MODE1_PREG	R/W	0h	This value sets the deq_txpretrainen from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001.
20	DEQ_TXPRETRAINEN_MODE0_PREG	R/W	0h	This value sets the deq_txpretrainen from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000.
19	DEQ_CLOSEDEYE_SEL_MODE3_PREG	R/W	1h	This value sets the deq_closedeye_sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011.
18	DEQ_CLOSEDEYE_SEL_MODE2_PREG	R/W	1h	This value sets the deq_closedeye_sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010.
17	DEQ_CLOSEDEYE_SEL_MODE1_PREG	R/W	0h	This value sets the deq_closedeye_sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001.
16	DEQ_CLOSEDEYE_SEL_MODE0_PREG	R/W	0h	This value sets the deq_closedeye_sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000.
15	DRVCTRL_EDGEBOOST_EN_MODE3_PREG	R/W	1h	Active high enable for the transmit driver edgeboost function when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011.
14	DRVCTRL_EDGEBOOST_EN_MODE2_PREG	R/W	1h	Active high enable for the transmit driver edgeboost function when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010.
13	DRVCTRL_EDGEBOOST_EN_MODE1_PREG	R/W	1h	Active high enable for the transmit driver edgeboost function when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001.
12	DRVCTRL_EDGEBOOST_EN_MODE0_PREG	R/W	0h	Active high enable for the transmit driver edgeboost function when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000.
11	TX_DEEMPHASIS_CTRL_SEL_MODE3_PREG	R/W	1h	This value sets the tx_deemphasis_ctrl_sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011.
10	TX_DEEMPHASIS_CTRL_SEL_MODE2_PREG	R/W	1h	This value sets the tx_deemphasis_ctrl_sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010.
9	TX_DEEMPHASIS_CTRL_SEL_MODE1_PREG	R/W	0h	This value sets the tx_deemphasis_ctrl_sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001.
8	TX_DEEMPHASIS_CTRL_SEL_MODE0_PREG	R/W	0h	This value sets the tx_deemphasis_ctrl_sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000.
7	DRV_IDLE_LOWZ_MODE3_PREG	R/W	0h	Asserting this value lowers the impedance of the transmit driver common-mode impedance when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011.
6	DRV_IDLE_LOWZ_MODE2_PREG	R/W	0h	Asserting this value lowers the impedance of the transmit driver common-mode impedance when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010.
5	DRV_IDLE_LOWZ_MODE1_PREG	R/W	0h	Asserting this value lowers the impedance of the transmit driver common-mode impedance when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001.
4	DRV_IDLE_LOWZ_MODE0_PREG	R/W	0h	Asserting this value lowers the impedance of the transmit driver common-mode impedance when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011.
3	SER_GT8G_MODE3_PREG	R/W	1h	This value overrides the ser_gt8g from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011.

**Table 11-266. DET_STANDEC_B_PREG__DET_STANDEC_A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2	SER_GT8G_MODE2_PREG	R/W	0h	This value overrides the ser_gt8g from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010.
1	SER_GT8G_MODE1_PREG	R/W	0h	This value overrides the ser_gt8g from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001.
0	SER_GT8G_MODE0_PREG	R/W	0h	This value overrides the ser_gt8g from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000.

Table 11-267. Register Call Summary for DET_STANDEC_B_PREG__DET_STANDEC_A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DET_STANDEC_B_PREG__DET_STANDEC_A_PREG_j Register \(Offset = 4000h + formula\) \[reset = X\]: \[0\]](#)

11.89 DET_STANDEC_D_PREG__DET_STANDEC_C_PREG_j Register (Offset = 4004h + formula) [reset = 691F00A0h]

DET_STANDEC_D_PREG__DET_STANDEC_C_PREG_j is shown in Figure 11-89 and described in Table 11-269.

Return to [Summary Table](#).

Standard decoder register C.

Offset = 4004h + (j * 400h); where j = 0h to 1h

Table 11-268. DET_STANDEC_D_PREG__DET_STANDEC_C_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4004h + formula
SERDES_16G1	0501 4004h + formula
SERDES_16G2	0502 4004h + formula
SERDES_16G3	0503 4004h + formula

Figure 11-89. DET_STANDEC_D_PREG__DET_STANDEC_C_PREG_j Register

31	30	29	28	27	26	25	24
CLKPATHCTRL_SSCLOCKADJ_MODE3_PREG			CLKPATHCTRL_SSCLOCKADJ_MODE2_PREG			CLKPATHCTRL_SSCLOCKADJ_MODE1_PREG	
R/W-3h			R/W-2h			R/W-2h	
23	22	21	20	19	18	17	16
CLKPATHCTRL_SSCLOCKADJ_MODE1_PREG	CLKPATHCTRL_SSCLOCKADJ_MODE0_PREG			CLKRST_FULL_RT_DIVSEL_MODE3_PREG	CLKRST_FULL_RT_DIVSEL_MODE2_PREG	CLKRST_FULL_RT_DIVSEL_MODE1_PREG	CLKRST_FULL_RT_DIVSEL_MODE0_PREG
R/W-2h	R/W-1h			R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
VGA_TAPSTEPSIZE_MODE3_PREG	VGA_TAPSTEPSIZE_MODE2_PREG		VGA_TAPSTEPSIZE_MODE1_PREG		VGA_TAPSTEPSIZE_MODE0_PREG		
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
DEQ_CLOSEDEYE_MODE_MODE3_PREG	DEQ_CLOSEDEYE_MODE_MODE2_PREG		DEQ_CLOSEDEYE_MODE_MODE1_PREG		DEQ_CLOSEDEYE_MODE_MODE0_PREG		
R/W-2h		R/W-2h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-269. DET_STANDEC_D_PREG__DET_STANDEC_C_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	CLKPATHCTRL_SSCLOCKADJ_MODE3_PREG	R/W	3h	This value sets the clkpathctrl_ssclockadj from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. Divider ratio 3'b000 1 3'b001 2 3'b010 4 3'b011 8 3'b100 16 3'b101 Reserved 3'b110 Reserved 3'b111 Reserved

**Table 11-269. DET_STANDEC_D_PREG_DET_STANDEC_C_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
28-26	CLKPATHCTRL_SSCLOCKADJ_MODE2_PREG	R/W	2h	This value sets the clkpathctrl_sscklockadj from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. Divider ratio 3'b000 1 3'b001 2 3'b010 4 3'b011 8 3'b100 16 3'b101 Reserved 3'b110 Reserved 3'b111 Reserved
25-23	CLKPATHCTRL_SSCLOCKADJ_MODE1_PREG	R/W	2h	This value sets the clkpathctrl_sscklockadj from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Divider ratio 3'b000 1 3'b001 2 3'b010 4 3'b011 8 3'b100 16 3'b101 Reserved 3'b110 Reserved 3'b111 Reserved
22-20	CLKPATHCTRL_SSCLOCKADJ_MODE0_PREG	R/W	1h	This value sets the clkpathctrl_sscklockadj from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. Divider ratio 3'b000 1 3'b001 2 3'b010 4 3'b011 8 3'b100 16 3'b101 Reserved 3'b110 Reserved 3'b111 Reserved
19	CLKRST_FULLRT_DIVSEL_MODE3_PREG	R/W	1h	This value sets the clkrst_fullrt_div2sel from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. Divider ratio 1'b0 1 1'b1 2
18	CLKRST_FULLRT_DIVSEL_MODE2_PREG	R/W	1h	This value sets the clkrst_fullrt_div2sel from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. Divider ratio 1'b0 1 1'b1 2
17	CLKRST_FULLRT_DIVSEL_MODE1_PREG	R/W	1h	This value sets the clkrst_fullrt_div2sel from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Divider ratio 1'b0 1 1'b1 2

**Table 11-269. DET_STANDEC_D_PREG_DET_STANDEC_C_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
16	CLKRST_FULLRT_DIVSEL_MODE0_PREG	R/W	1h	This value sets the clkrst_fullrt_div2sel from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000. Divider ratio 1'b0 1 1'b1 2
15-14	VGA_TAPSTEPSIZE_MODE3_PREG	R/W	0h	Receive data path offset correction current trim when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011: Current Mirror Ratio 2'b11 Lowest 1.00 2'b 10 : 1.33 2'b 01 : 2.00 2'b00 Highest 4.00
13-12	VGA_TAPSTEPSIZE_MODE2_PREG	R/W	0h	Receive data path offset correction current trim when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010: Current Mirror Ratio 2'b11 Lowest 1.00 2'b 10 : 1.33 2'b 01 : 2.00 2'b00 Highest 4.00
11-10	VGA_TAPSTEPSIZE_MODE1_PREG	R/W	0h	Receive data path offset correction current trim when xcvr_standard_mode_in_{15:0}[2:0] is 3'b 001: Current Mirror Ratio 2'b11 Lowest 1.00 2'b 10 : 1.33 2'b 01 : 2.00 2'b00 Highest 4.00
9-8	VGA_TAPSTEPSIZE_MODE0_PREG	R/W	0h	Receive data path offset correction current trim when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000: Current Mirror Ratio 2'b11 Lowest 1.00 2'b 10 : 1.33 2'b 01 : 2.00 2'b00 Highest 4.00
7-6	DEQ_CLOSEDEYE_MODE3_PREG	R/W	2h	This value sets the deq_closedeye_mode from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011. Mode 2'b 00 : Immediate training. 2'b 01: rx_eq_training_in_{15:0} interface. 2'b 10: rx_eq_eval_in_{15:0} interface. 2'b 11: reserved.
5-4	DEQ_CLOSEDEYE_MODE2_PREG	R/W	2h	This value sets the deq_closedeye_mode from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010. Mode 2'b 00 : Immediate training. 2'b 01: rx_eq_training_in_{15:0} interface. 2'b 10: rx_eq_eval_in_{15:0} interface. 2'b 11: reserved.

**Table 11-269. DET_STANDEC_D_PREG__DET_STANDEC_C_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
3-2	DEQ_CLOSED EYE_MODE1_PREG	R/W	0h	This value sets the deq_closedeye_mode from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Mode 2'b 00 : Immediate training. 2'b 01: rx_eq_training_ln_{15:0} interface. 2'b 10: rx_eq_eval_ln_{15:0} interface. 2'b 11: reserved.
1-0	DEQ_CLOSED EYE_MODE0_PREG	R/W	0h	This value sets the deq_closedeye_mode from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. Mode 2'b 00 : Immediate training. 2'b 01: rx_eq_training_ln_{15:0} interface. 2'b 10: rx_eq_eval_ln_{15:0} interface. 2'b 11: reserved.

Table 11-270. Register Call Summary for DET_STANDEC_D_PREG__DET_STANDEC_C_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DET_STANDEC_D_PREG__DET_STANDEC_C_PREG_j Register \(Offset = 4004h + formula\) \[reset = 691F00A0h\]: \[0\]](#)

11.90 FPWRISO_OVRD_PREG_DET_STANDEC_E_PREG_j Register (Offset = 4008h + formula) [reset = X]

FPWRISO_OVRD_PREG_DET_STANDEC_E_PREG_j is shown in Figure 11-90 and described in Table 11-272.

Return to [Summary Table](#).

Standard decoder register E.

Offset = 4008h + (j * 400h); where j = 0h to 1h

Table 11-271. FPWRISO_OVRD_PREG_DET_STANDEC_E_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4008h + formula
SERDES_16G1	0501 4008h + formula
SERDES_16G2	0502 4008h + formula
SERDES_16G3	0503 4008h + formula

Figure 11-90. FPWRISO_OVRD_PREG_DET_STANDEC_E_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED			FPWRISO_OVRD_EN_PREG	RESERVED			FPWRISO_ISOLATION_EN_OVRD_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h
23	22	21	20	19	18	17	16
RESERVED			FPWRISO_PHASE2EN_OVRD_PREG	RESERVED			FPWRISO_PHASE1EN_OVRD_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h
15	14	13	12	11	10	9	8
RESERVED				CLKRST_DATART_DIV_MODE3_PREG			CLKRST_DATART_DIV_MODE2_PREG
R/W-X				R/W-1h			R/W-1h
7	6	5	4	3	2	1	0
CLKRST_DATART_DIV_MODE2_PREG		CLKRST_DATART_DIV_MODE1_PREG			CLKRST_DATART_DIV_MODE0_PREG		
R/W-1h		R/W-2h			R/W-3h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-272. FPWRISO_OVRD_PREG_DET_STANDEC_E_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28	FPWRISO_OVRD_EN_PREG	R/W	0h	Lane power-gated supply island active high override enable: When asserted, cmn_pwriso_isolation_en_ovrd_preg, cmn_pwriso_phase2en_ovrd_preg, and cmn_pwriso_phase1en_ovrd_preg directly control the power-gate enables and associated isolation .
27-25	RESERVED	R/W	X	
24	FPWRISO_ISOLATION_EN_OVRD_PREG	R/W	0h	Lane power-gated supply island isolation override: When fpwriso_ovrd_en_preg is asserted, this bit controls the fpwriso_power_isolation_en.
23-21	RESERVED	R/W	X	

**Table 11-272. FPWRISO_OVRD_PREG__DET_STANDEC_E_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
20	FPWRISO_PHASE2EN_OVRD_PREG	R/W	0h	Lane power-gated supply island phase2en override: When fpwriso_ovrd_en_preg is asserted, this bit controls the phase2en to all lane power gates.
19-17	RESERVED	R/W	X	
16	FPWRISO_PHASE1EN_OVRD_PREG	R/W	0h	Lane power-gated supply island phase1en override: When fpwriso_ovrd_en_preg_preg is asserted, this bit controls the phase1en to all lane power gates.
15-12	RESERVED	R/W	X	
11-9	CLKRST_DATART_DIV_MODE3_PREG	R/W	1h	This value sets the clkrst_datart_divsel from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. Divider ratio 3'b000 1 3'b001 2 3'b010 4 3'b011 8 3'b 100-3'b111 16
8-6	CLKRST_DATART_DIV_MODE2_PREG	R/W	1h	This value sets the clkrst_datart_divsel from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. Divider ratio 3'b000 1 3'b001 2 3'b010 4 3'b011 8 3'b100-3'b111 16
5-3	CLKRST_DATART_DIV_MODE1_PREG	R/W	2h	This value sets the clkrst_datart_divsel from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Divider ratio 3'b000 1 3'b001 2 3'b010 4 3'b011 8 3'b 100-3'b111 16
2-0	CLKRST_DATART_DIV_MODE0_PREG	R/W	3h	This value sets the clkrst_datart_divsel from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. Divider ratio 3'b000 1 3'b001 2 3'b010 4 3'b011 8 3'b100-3'b111 16

Table 11-273. Register Call Summary for FPWRISO_OVRD_PREG__DET_STANDEC_E_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [FPWRISO_OVRD_PREG__DET_STANDEC_E_PREG_j Register \(Offset = 4008h + formula\) \[reset = X\]: \[0\]](#)

11.91 FPWRISO_CTRL_PREG_j Register (Offset = 400Ch + formula) [reset = X]

FPWRISO_CTRL_PREG_j is shown in Figure 11-91 and described in Table 11-275.

Return to [Summary Table](#).

Lane power-gated supply island control register.

Offset = 400Ch + (j * 400h); where j = 0h to 1h

Table 11-274. FPWRISO_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 400Ch + formula
SERDES_16G1	0501 400Ch + formula
SERDES_16G2	0502 400Ch + formula
SERDES_16G3	0503 400Ch + formula

Figure 11-91. FPWRISO_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	FPWRISO_PWRDN_DISABLE_PREG	RESERVED	FPWRISO_STAGGER_DLY_PREG				
R/W-X	R/W-0h	R/W-X	R/W-0h				
23	22	21	20	19	18	17	16
FPWRISO_EN_PH2DLY_PREG				FPWRISO_EN_PH1DLY_PREG			
R/W-0h				R/W-3h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-275. FPWRISO_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	FPWRISO_PWRDN_DISABLE_PREG	R/W	0h	Power down disable: Setting this bit to 1'b1 will disable turning off the Lane power-gated supplies when the macro is in a state that would normally switch the power islands off.
29	RESERVED	R/W	X	
28-24	FPWRISO_STAGGER_DLY_PREG	R/W	0h	Lane to Lane power island enable/disable stagger time: This specifies the number of cmn_refclk cycles between each lane recognizing a change in power island state. The power islands are thus enabled or disabled in a staggered fashion to control in-rush currents. Note: This value must always be the same for all lanes within the Macro.

Table 11-275. FPWRISO_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-20	FPWRISO_EN_PH2DLY_PREG	R/W	0h	Power enable phase 2 timer value: This value + 1 the number of cmn_refclk cycles the Lane power island control state machine will wait in the power phase 2 enable state.
19-16	FPWRISO_EN_PH1DLY_PREG	R/W	3h	Power enable phase 1 timer value: This value + 1 is the number of cmn_refclk cycles the Lane power island control state machine will wait in the power phase 1 enable state.
15-0	RESERVED	R/W	X	

Table 11-276. Register Call Summary for FPWRISO_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [FPWRISO_CTRL_PREG_j Register \(Offset = 400Ch + formula\) \[reset = X\]: \[0\]](#)

11.92 PSM_A0IN_TMR_PREG__PSM_LANECAI_DLY_A1_RESETS_PREG_j Register (Offset = 4010h + formula) [reset = X]

PSM_A0IN_TMR_PREG__PSM_LANECAI_DLY_A1_RESETS_PREG_j is shown in Figure 11-92 and described in Table 11-278.

Return to [Summary Table](#).

Power State Machine lane calibration delay timer and A1 resets register.

Link control register; only valid in master lane.

Offset = 4010h + (j * 400h); where j = 0h to 1h

Table 11-277.
PSM_A0IN_TMR_PREG__PSM_LANECAI_DLY_A1_RESETS_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4010h + formula
SERDES_16G1	0501 4010h + formula
SERDES_16G2	0502 4010h + formula
SERDES_16G3	0503 4010h + formula

Figure 11-92. PSM_A0IN_TMR_PREG__PSM_LANECAI_DLY_A1_RESETS_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PSM_A0IN_TMR_VAL_PREG							
R/W-35h							
15	14	13	12	11	10	9	8
RESERVED			PSM_TX_RESET_ACTIVE_A1_PREG	RESERVED			PSM_RX_RESET_ACTIVE_A1_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h
7	6	5	4	3	2	1	0
PSM_LANECAI_DLY_TMR_VAL_PREG							
R/W-11h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-278. PSM_A0IN_TMR_PREG__PSM_LANECAI_DLY_A1_RESETS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PSM_A0IN_TMR_VAL_PREG	R/W	35h	A0 in delay state timer value : used for the timer when the power state machine is in the A0 in delay state. The value must be 1 or greater and should be 16 * pstg_stagger_dly_preg to allow all lanes to see the staggered power state change. This timer delay is specified in xcvr_psmclk_ln_{15:0} periods. Link control register only valid in master lane.
15-13	RESERVED	R/W	X	
12	PSM_TX_RESET_ACTIVE_A1_PREG	R/W	0h	When asserted, the transmit path resets will be asserted in the A1 power state.

Table 11-278. PSM_A0IN_TMR_PREG__PSM_LANECAL_DLY_A1_RESETS_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	RESERVED	R/W	X	
8	PSM_RX_RESET_ACTIVE_A1_PREG	R/W	0h	When asserted, the receive path resets will be asserted in the A1 power state.
7-0	PSM_LANECAL_DLY_TMR_VAL_PREG	R/W	11h	Lane calibration delay state timer value : The value must be 1 or greater and should be 16 * pstg_stagger_dly_preg to allow all lanes to see the staggered power state change. This timer delay is specified in xcvr_psmclk_ln_{15:0} periods.

Table 11-279. Register Call Summary for PSM_A0IN_TMR_PREG__PSM_LANECAL_DLY_A1_RESETS_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSM_A0IN_TMR_PREG__PSM_LANECAL_DLY_A1_RESETS_PREG_j Register \(Offset = 4010h + formula\) \[reset = X\]: \[0\]](#)

11.93 PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG_j Register (Offset = 4014h + formula) [reset = X]

PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG_j is shown in Figure 11-93 and described in Table 11-281.

Return to [Summary Table](#).

Power State Machine A1 in delay timer register.

Offset = 4014h + (j * 400h); where j = 0h to 1h

Table 11-280. PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4014h + formula
SERDES_16G1	0501 4014h + formula
SERDES_16G2	0502 4014h + formula
SERDES_16G3	0503 4014h + formula

Figure 11-93. PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PSM_A2IN_TMR_VAL_PREG							
R/W-X								R/W-85h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PSM_A1IN_TMR_VAL_PREG							
R/W-X								R/W-1h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-281. PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PSM_A2IN_TMR_VAL_P REG	R/W	85h	A2 in delay state timer value : used for the timer when the power state machine is in the A2 in delay state. The value must be 1 or greater and should be 16 * pstg_stagger_dly_preg to allow all lanes to see the staggered power state change. This timer delay is specified in xcvr_psmclk_ln_{15:0} periods.
15-8	RESERVED	R/W	X	
7-0	PSM_A1IN_TMR_VAL_P REG	R/W	1h	A1 in delay state timer value : used for the timer when the power state machine is in the A1 in delay state. The value must be 1 or greater r and should be 16 * pstg_stagger_dly_preg to allow all lanes to see the staggered power state change. This timer delay is specified in xcvr_psmclk_ln_{15:0} periods.

Table 11-282. Register Call Summary for PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSM_A2IN_TMR_PREG__PSM_A1IN_TMR_PREG_j Register \(Offset = 4014h + formula\) \[reset = X\]: \[0\]](#)

11.94 PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG_j Register (Offset = 4018h + formula) [reset = X]

PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG_j is shown in Figure 11-94 and described in Table 11-284.

Return to [Summary Table](#).

Power State Machine A3 in delay timer register.

Link control register; only valid in master lane.

Offset = 4018h + (j * 400h); where j = 0h to 1h

Table 11-283. PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4018h + formula
SERDES_16G1	0501 4018h + formula
SERDES_16G2	0502 4018h + formula
SERDES_16G3	0503 4018h + formula

Figure 11-94. PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PSM_A4IN_TMR_VAL_PREG							
R/W-X								R/W-1h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PSM_A3IN_TMR_VAL_PREG							
R/W-X								R/W-1h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-284. PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PSM_A4IN_TMR_VAL_P REG	R/W	1h	A4 in delay state timer value : used for the timer when the power state machine is in the A4 in delay state. The value must be 1 or greater. This timer delay is specified in xcvr_psmclk_In_{15:0} periods.
15-8	RESERVED	R/W	X	
7-0	PSM_A3IN_TMR_VAL_P REG	R/W	1h	A3 in delay state timer value : used for the timer when the power state machine is in the A3 in delay state. The value must be 1 or greater and should be 16 * psth_stagger_dly_preg on A4/A5 to A3 transitions to allow all lanes to see the staggered power state change. This timer delay is specified in xcvr_psmclk_In_{15:0} periods.

Table 11-285. Register Call Summary for PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSM_A4IN_TMR_PREG__PSM_A3IN_TMR_PREG_j Register \(Offset = 4018h + formula\) \[reset = X\]: \[0\]](#)

11.95 PSM_A0OUT_TMR_PREG_j Register (Offset = 401Ch + formula) [reset = X]

PSM_A0OUT_TMR_PREG_j is shown in [Figure 11-95](#) and described in [Table 11-287](#).

Return to [Summary Table](#).

Power State Machine A0 out delay timer register.

Link control register; only valid in master lane.

Offset = 401Ch + (j * 400h); where j = 0h to 1h

Table 11-286. PSM_A0OUT_TMR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 401Ch + formula
SERDES_16G1	0501 401Ch + formula
SERDES_16G2	0502 401Ch + formula
SERDES_16G3	0503 401Ch + formula

Figure 11-95. PSM_A0OUT_TMR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PSM_A0OUT_TMR_VAL_PREG			
R/W-X				R/W-1h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-287. PSM_A0OUT_TMR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PSM_A0OUT_TMR_VAL_PREG	R/W	1h	A0 out delay state timer value : used for the timer when the power state machine is in the A0 out delay state. The value must be 1 or greater. This timer delay is specified in xcvr_psmclk_in_{15:0} periods.
15-0	RESERVED	R/W	X	

Table 11-288. Register Call Summary for PSM_A0OUT_TMR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSM_A0OUT_TMR_PREG_j Register \(Offset = 401Ch + formula\) \[reset = X\]: \[0\]](#)

11.96 PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_PREG_j Register (Offset = 4020h + formula) [reset = X]

PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_PREG_j is shown in [Figure 11-96](#) and described in [Table 11-290](#).

Return to [Summary Table](#).

Power State Machine A1 out delay timer register.

Link control register; only valid in master lane.

Offset = 4020h + (j * 400h); where j = 0h to 1h

Table 11-289. PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4020h + formula
SERDES_16G1	0501 4020h + formula
SERDES_16G2	0502 4020h + formula
SERDES_16G3	0503 4020h + formula

Figure 11-96. PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PSM_A2OUT_TMR_VAL_PREG			
R/W-X				R/W-1h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PSM_A1OUT_TMR_VAL_PREG			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-290. PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PSM_A2OUT_TMR_VAL_PREG	R/W	1h	A2 out delay state timer value : used for the timer when the power state machine is in the A2 out delay state. The value must be 1 or greater. This timer delay is specified in xcvr_psmclk_ln_{15:0} periods.
15-4	RESERVED	R/W	X	
3-0	PSM_A1OUT_TMR_VAL_PREG	R/W	1h	A1 out delay state timer value : used for the timer when the power state machine is in the A1 out delay state. The value must be 1 or greater. This timer delay is specified in xcvr_psmclk_ln_{15:0} periods.

Table 11-291. Register Call Summary for PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_PREG_j

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] PSM_A2OUT_TMR_PREG__PSM_A1OUT_TMR_PREG_j Register (Offset = 4020h + formula) [reset = X]: [0]

11.97 PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_PREG_j Register (Offset = 4024h + formula) [reset = X]

PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_PREG_j is shown in [Figure 11-97](#) and described in [Table 11-293](#).

Return to [Summary Table](#).

Power State Machine A3 out delay timer register.

Link control register; only valid in master lane.

Offset = 4024h + (j * 400h); where j = 0h to 1h

Table 11-292. PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4024h + formula
SERDES_16G1	0501 4024h + formula
SERDES_16G2	0502 4024h + formula
SERDES_16G3	0503 4024h + formula

Figure 11-97. PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PSM_A4OUT_TMR_VAL_PREG			
R/W-X				R/W-1h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PSM_A3OUT_TMR_VAL_PREG			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-293. PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PSM_A4OUT_TMR_VAL_PREG	R/W	1h	A4 out delay state timer value : used for the timer when the power state machine is in the A4 out delay state. The value must be 1 or greater. This timer delay is specified in xcvr_psmclk_ln_{15:0} periods.
15-4	RESERVED	R/W	X	
3-0	PSM_A3OUT_TMR_VAL_PREG	R/W	1h	A3 out delay state timer value : used for the timer when the power state machine is in the A3 out delay state. The value must be 1 or greater. This timer delay is specified in xcvr_psmclk_ln_{15:0} periods.

Table 11-294. Register Call Summary for PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSM_A4OUT_TMR_PREG__PSM_A3OUT_TMR_PREG_j](#) Register (Offset = 4024h + formula) [reset = X]: [0]

11.98 PSM_DIAG_PREG_j Register (Offset = 4028h + formula) [reset = X]

PSM_DIAG_PREG_j is shown in [Figure 11-98](#) and described in [Table 11-296](#).

Return to [Summary Table](#).

Power State Machine diagnostic register.

Link control register; only valid in master lane.

Offset = 4028h + (j * 400h); where j = 0h to 1h

Table 11-295. PSM_DIAG_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4028h + formula
SERDES_16G1	0501 4028h + formula
SERDES_16G2	0502 4028h + formula
SERDES_16G3	0503 4028h + formula

Figure 11-98. PSM_DIAG_PREG_j Register

31	30	29	28	27	26	25	24
PSM_SKIP_LANE_RECAL_PREG	PSM_SKIP_RXMEM_RESETPREG	RESERVED	PSM_FORCE_A4_EXIT_ACK_PREG	PSM_FORCE_A3_EXIT_ACK_PREG	PSM_FORCE_A2_EXIT_ACK_PREG	PSM_FORCE_A1_EXIT_ACK_PREG	PSM_FORCE_A0_EXIT_ACK_PREG
R/W-1h	R/W-1h	R/W-X	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
PSM_FORCE_LANE_CAL_CLKEN_ACK_PREG	PSM_FORCE_LANE_CAL_ENTRY_ACK_PREG	PSM_FORCE_A4_ENTRY_ACK_PREG	PSM_FORCE_A3_ENTRY_ACK_PREG	PSM_FORCE_A2_CLKEN_ACK_PREG	PSM_FORCE_A2_ENTRY_ACK_PREG	PSM_FORCE_A1_ENTRY_ACK_PREG	PSM_FORCE_A0_ENTRY_ACK_PREG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-296. PSM_DIAG_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PSM_SKIP_LANE_RECAL_PREG	R/W	1h	Skip lane re-calibration : When this bit is active (1'b1), the lane calibration state will be skipped if it was previously run, unless the macro is disabled or reset or a xcvr_standard_mode change occurs.
30	PSM_SKIP_RXMEM_RESETPREG	R/W	1h	Skip reset of receive clock and data path equalization and offset memories: When this bit is active (1'b1), the lane clock and data path acquisitions will be skipped if it was previously run, unless the macro is disabled or reset, or a xcvr_standard_mode change in the link is requested.
29	RESERVED	R/W	X	
28	PSM_FORCE_A4_EXIT_ACK_PREG	R/W	0h	Force A4 exit acknowledge : Setting this active high bit forces the psm_a4_exit_ack pin of the power state machine active.

Table 11-296. PSM_DIAG_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	PSM_FORCE_A3_EXIT_ACK_PREG	R/W	1h	Force A3 exit acknowledge : Setting this active high bit forces the psm_a3_exit_ack pin of the power state machine active. Note: in the current implementation the default value must be maintained for all standards supporting the A3 power state.
26	PSM_FORCE_A2_EXIT_ACK_PREG	R/W	1h	Force A2 exit acknowledge : Setting active high bit forces the psm_a2_exit_ack pin of the power state machine active. Note: in the current implementation the default value must be maintained for all standards supporting the A2 power state.
25	PSM_FORCE_A1_EXIT_ACK_PREG	R/W	1h	Force A1 exit acknowledge : Setting this active high bit forces the psm_a1_exit_ack pin of the power state machine active. Note: in the current implementation the default value must be maintained for all standards supporting the A1 power state.
24	PSM_FORCE_A0_EXIT_ACK_PREG	R/W	1h	Force A0 exit acknowledge : Setting this active high bit forces the psm_a0_exit_ack pin of the power state machine active. Note: in the current implementation the default value must be maintained.
23	PSM_FORCE_LANE_CAL_CLKEN_ACK_PREG	R/W	0h	Force lane calibration clken acknowledge : Asserting this active high bit forces the psm_lane_cal_clken_ack pin of the power state machine active.
22	PSM_FORCE_LANE_CAL_ENTRY_ACK_PREG	R/W	0h	Force lane calibration entry acknowledge : Asserting this active high bit forces the psm_lane_cal_rdy_ack pin of the power state machine active.
21	PSM_FORCE_A4_ENTRY_ACK_PREG	R/W	0h	Force A4 entry acknowledge : Setting this active high bit forces the psm_a4_entry_ack pin of the power state machine active.
20	PSM_FORCE_A3_ENTRY_ACK_PREG	R/W	0h	Force A3 entry acknowledge : Setting this active high bit forces the psm_a3_entry_ack pin of the power state machine active.
19	PSM_FORCE_A2_CLKEN_ACK_PREG	R/W	0h	Force A2 clken acknowledge : Setting this active high bit forces the psm_a2_clken_ack pin of the power state machine active.
18	PSM_FORCE_A2_ENTRY_ACK_PREG	R/W	0h	Force A2 entry acknowledge : Setting active high bit forces the psm_a2_entry_ack pin of the power state machine active.
17	PSM_FORCE_A1_ENTRY_ACK_PREG	R/W	0h	Force A1 entry acknowledge : Setting this active high bit forces the psm_a1_entry_ack pin of the power state machine active.
16	PSM_FORCE_A0_ENTRY_ACK_PREG	R/W	0h	Force A0 entry acknowledge : Setting this active high bit forces the psm_a0_entry_ack pin of the power state machine active.
15-0	RESERVED	R/W	X	

Table 11-297. Register Call Summary for PSM_DIAG_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSM_DIAG_PREG_j Register \(Offset = 4028h + formula\) \[reset = X\]: \[0\]](#)

11.99 PSM_STATE_L_PREG__PSM_STATE_H_PREG_j Register (Offset = 402Ch + formula) [reset = X]

PSM_STATE_L_PREG__PSM_STATE_H_PREG_j is shown in Figure 11-99 and described in Table 11-299.

Return to [Summary Table](#).

Power State Machine current state register high byte.

Offset = 402Ch + (j * 400h); where j = 0h to 1h

Table 11-298.
PSM_STATE_L_PREG__PSM_STATE_H_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 402Ch + formula
SERDES_16G1	0501 402Ch + formula
SERDES_16G2	0502 402Ch + formula
SERDES_16G3	0503 402Ch + formula

Figure 11-99. PSM_STATE_L_PREG__PSM_STATE_H_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PSM_STATE_L															
R-7h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PSM_STATE_H			
R-X												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 11-299. PSM_STATE_L_PREG__PSM_STATE_H_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PSM_STATE_L	R	7h	Power state machine current state: This is the low byte of the current state of the power state machine: psm_state[15:0]. Note this register is for diagnostic purposes only.
15-4	RESERVED	R	X	
3-0	PSM_STATE_H	R	0h	Power state machine current state: This is the high byte of the current state of the power state machine: psm_state [19:16]. Note this register is for diagnostic purposes only.

Table 11-300. Register Call Summary for PSM_STATE_L_PREG__PSM_STATE_H_PREG_j

16-G SerDes Registers

- PSM_STATE_L_PREG__PSM_STATE_H_PREG_j Register (Offset = 402Ch + formula) [reset = X]: [0]

11.100 PSTG_STATUS_PREG__PSTG_CTRL_PREG_j Register (Offset = 4030h + formula) [reset = X]

PSTG_STATUS_PREG__PSTG_CTRL_PREG_j is shown in [Figure 11-100](#) and described in [Table 11-302](#).

Return to [Summary Table](#).

Power State Token Generator Control Register

Offset = 4030h + (j * 400h); where j = 0h to 1h

Table 11-301.
PSTG_STATUS_PREG__PSTG_CTRL_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4030h + formula
SERDES_16G1	0501 4030h + formula
SERDES_16G2	0502 4030h + formula
SERDES_16G3	0503 4030h + formula

Figure 11-100. PSTG_STATUS_PREG__PSTG_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PSTG_STATE	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PSTG_STAGGER_DLY_PREG			
R/W-X				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-302. PSTG_STATUS_PREG__PSTG_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PSTG_STATE	R	0h	Power State Token Generator FSM state vector.
15-4	RESERVED	R/W	X	
3-0	PSTG_STAGGER_DLY_PREG	R/W	0h	Lane to Lane power state enable/disable stagger time: This specifies the number of cmn_psmclk cycles between each lane recognizing a change in power state. The circuits from lane to lane are thus enabled or disabled in a staggered fashion to control in-rush currents. Note: This value must always be the same for all lanes within the Macro.

Table 11-303. Register Call Summary for PSTG_STATUS_PREG__PSTG_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSTG_STATUS_PREG__PSTG_CTRL_PREG_j Register \(Offset = 4030h + formula\) \[reset = X\]: \[0\]](#)

11.101 PCSM_STATUS_PREG__PCSM_CTRL_PREG_j Register (Offset = 4038h + formula) [reset = X]

PCSM_STATUS_PREG__PCSM_CTRL_PREG_j is shown in Figure 11-101 and described in Table 11-305.

Return to [Summary Table](#).

PLL clock state machine control register

Offset = 4038h + (j * 400h); where j = 0h to 1h

Table 11-304.
PCSM_STATUS_PREG__PCSM_CTRL_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4038h + formula
SERDES_16G1	0501 4038h + formula
SERDES_16G2	0502 4038h + formula
SERDES_16G3	0503 4038h + formula

Figure 11-101. PCSM_STATUS_PREG__PCSM_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PCSM_STATE			
R/W-X				R-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						PCSM_PLLNEN_OVREN_PREG	PCSM_PLLNEN_OVR_PREG
R/W-X						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-305. PCSM_STATUS_PREG__PCSM_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PCSM_STATE	R	0h	PLL clock state machine control state vector.
15-2	RESERVED	R/W	X	
1	PCSM_PLLNEN_OVREN_PREG	R/W	0h	PLLLN active high enable override enable: When asserted, pcsm_pllnen_ovr_preg overrides the pll clock state machine value for the PLLLN enable.
0	PCSM_PLLNEN_OVR_PREG	R/W	0h	PLLLN active high enable override value: When pcsm_pllnen_ovren_preg is asserted, this value overrides the pll clock state machine value for the PLLLN enable.

Table 11-306. Register Call Summary for PCSM_STATUS_PREG__PCSM_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PCSM_STATUS_PREG__PCSM_CTRL_PREG_j Register \(Offset = 4038h + formula\) \[reset = X\]: \[0\]](#)

11.102 PSC_LN_A1_PREG__PSC_LN_A0_PREG_j Register (Offset = 4040h + formula) [reset = X]

PSC_LN_A1_PREG__PSC_LN_A0_PREG_j is shown in [Figure 11-102](#) and described in [Table 11-308](#).

Return to [Summary Table](#).

Lane A0 power state definition register.

Offset = 4040h + (j * 400h); where j = 0h to 1h

Table 11-307.
PSC_LN_A1_PREG__PSC_LN_A0_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4040h + formula
SERDES_16G1	0501 4040h + formula
SERDES_16G2	0502 4040h + formula
SERDES_16G3	0503 4040h + formula

Figure 11-102. PSC_LN_A1_PREG__PSC_LN_A0_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PSC_LN_A1_PREG			
R/W-X				R/W-7h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PSC_LN_A0_PREG			
R/W-X				R/W-7h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-308. PSC_LN_A1_PREG__PSC_LN_A0_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PSC_LN_A1_PREG	R/W	7h	Bit Description 2 psc_biasdist_en 1 psc_slv_pllln_en 0 psc_mstr_pllln_en
15-3	RESERVED	R/W	X	
2-0	PSC_LN_A0_PREG	R/W	7h	Bit Description 2 psc_biasdist_en 1 psc_slv_pllln_en 0 psc_mstr_pllln_en

Table 11-309. Register Call Summary for PSC_LN_A1_PREG__PSC_LN_A0_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_LN_A1_PREG__PSC_LN_A0_PREG_j Register \(Offset = 4040h + formula\) \[reset = X\]: \[0\]](#)

11.103 PSC_LN_A3_PREG__PSC_LN_A2_PREG_j Register (Offset = 4044h + formula) [reset = X]

PSC_LN_A3_PREG__PSC_LN_A2_PREG_j is shown in [Figure 11-103](#) and described in [Table 11-311](#).

Return to [Summary Table](#).

Lane A2 power state definition register.

Offset = 4044h + (j * 400h); where j = 0h to 1h

Table 11-310.
PSC_LN_A3_PREG__PSC_LN_A2_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4044h + formula
SERDES_16G1	0501 4044h + formula
SERDES_16G2	0502 4044h + formula
SERDES_16G3	0503 4044h + formula

Figure 11-103. PSC_LN_A3_PREG__PSC_LN_A2_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PSC_LN_A3_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PSC_LN_A2_PREG			
R/W-X				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-311. PSC_LN_A3_PREG__PSC_LN_A2_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PSC_LN_A3_PREG	R/W	0h	Bit Description 2 psc_biasdist_en 1 psc_slv_pll_en 0 psc_mstr_pll_en
15-3	RESERVED	R/W	X	
2-0	PSC_LN_A2_PREG	R/W	5h	Bit Description 2 psc_biasdist_en 1 psc_slv_pll_en 0 psc_mstr_pll_en

Table 11-312. Register Call Summary for PSC_LN_A3_PREG__PSC_LN_A2_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_LN_A3_PREG__PSC_LN_A2_PREG_j Register \(Offset = 4044h + formula\) \[reset = X\]: \[0\]](#)

11.104 PSC_LN_A5_PREG__PSC_LN_A4_PREG_j Register (Offset = 4048h + formula) [reset = X]

PSC_LN_A5_PREG__PSC_LN_A4_PREG_j is shown in [Figure 11-104](#) and described in [Table 11-314](#).

Return to [Summary Table](#).

Lane A4 power state definition register.

Offset = 4048h + (j * 400h); where j = 0h to 1h

Table 11-313.
PSC_LN_A5_PREG__PSC_LN_A4_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4048h + formula
SERDES_16G1	0501 4048h + formula
SERDES_16G2	0502 4048h + formula
SERDES_16G3	0503 4048h + formula

Figure 11-104. PSC_LN_A5_PREG__PSC_LN_A4_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PSC_LN_A5_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PSC_LN_A4_PREG			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-314. PSC_LN_A5_PREG__PSC_LN_A4_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PSC_LN_A5_PREG	R/W	0h	Bit Description 2 psc_biasdist_en 1 psc_slv_pllln_en 0 psc_mstr_pllln_en
15-3	RESERVED	R/W	X	
2-0	PSC_LN_A4_PREG	R/W	0h	Bit Description 2 psc_biasdist_en 1 psc_slv_pllln_en 0 psc_mstr_pllln_en

Table 11-315. Register Call Summary for PSC_LN_A5_PREG__PSC_LN_A4_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_LN_A5_PREG__PSC_LN_A4_PREG_j Register \(Offset = 4048h + formula\) \[reset = X\]: \[0\]](#)

11.105 PSC_LN_IDLE_PREG_j Register (Offset = 404Ch + formula) [reset = X]

PSC_LN_IDLE_PREG_j is shown in Figure 11-105 and described in Table 11-317.

Return to [Summary Table](#).

Lane idle power state definition register.

Offset = 404Ch + (j * 400h); where j = 0h to 1h

Table 11-316. PSC_LN_IDLE_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 404Ch + formula
SERDES_16G1	0501 404Ch + formula
SERDES_16G2	0502 404Ch + formula
SERDES_16G3	0503 404Ch + formula

Figure 11-105. PSC_LN_IDLE_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					PSC_LN_IDLE_PREG		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-317. PSC_LN_IDLE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	PSC_LN_IDLE_PREG	R/W	0h	Bit Description 2 psc_biasdist_en 1 psc_slv_pllln_en 0 psc_mstr_pllln_en

Table 11-318. Register Call Summary for PSC_LN_IDLE_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_LN_IDLE_PREG_j Register \(Offset = 404Ch + formula\) \[reset = X\]: \[0\]](#)

11.106 PSC_TX_A1_PREG__PSC_TX_A0_PREG_j Register (Offset = 4050h + formula) [reset = X]

PSC_TX_A1_PREG__PSC_TX_A0_PREG_j is shown in [Figure 11-106](#) and described in [Table 11-320](#).

Return to [Summary Table](#).

Transmit A0 power state definition register.

Offset = 4050h + (j * 400h); where j = 0h to 1h

Table 11-319.
PSC_TX_A1_PREG__PSC_TX_A0_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4050h + formula
SERDES_16G1	0501 4050h + formula
SERDES_16G2	0502 4050h + formula
SERDES_16G3	0503 4050h + formula

Figure 11-106. PSC_TX_A1_PREG__PSC_TX_A0_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PSC_TX_A1_PREG				
R/W-X											R/W-6h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PSC_TX_A0_PREG				
R/W-X											R/W-1Eh				

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-320. PSC_TX_A1_PREG__PSC_TX_A0_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PSC_TX_A1_PREG	R/W	6h	Bit Description 4 psc_ser_outavdd_en 3 psc_tx_drv_en 2 psc_tx_clk_en 1 psc_tx_common_mode_en 0 psc_tx_lfpngen_clk_gate_en
15-5	RESERVED	R/W	X	
4-0	PSC_TX_A0_PREG	R/W	1Eh	Bit Description 4 psc_ser_outavdd_en 3 psc_tx_drv_en 2 psc_tx_clk_en 1 psc_tx_common_mode_en 0 psc_tx_lfpngen_clk_gate_en

Table 11-321. Register Call Summary for PSC_TX_A1_PREG__PSC_TX_A0_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_TX_A1_PREG__PSC_TX_A0_PREG_j Register \(Offset = 4050h + formula\) \[reset = X\]: \[0\]](#)

11.107 PSC_TX_A3_PREG__PSC_TX_A2_PREG_j Register (Offset = 4054h + formula) [reset = X]

PSC_TX_A3_PREG__PSC_TX_A2_PREG_j is shown in Figure 11-107 and described in Table 11-323.

Return to [Summary Table](#).

Transmit A2 power state definition register.

Offset = 4054h + (j * 400h); where j = 0h to 1h

Table 11-322.
PSC_TX_A3_PREG__PSC_TX_A2_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4054h + formula
SERDES_16G1	0501 4054h + formula
SERDES_16G2	0502 4054h + formula
SERDES_16G3	0503 4054h + formula

Figure 11-107. PSC_TX_A3_PREG__PSC_TX_A2_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PSC_TX_A3_PREG				
R/W-X											R/W-2h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PSC_TX_A2_PREG				
R/W-X											R/W-2h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-323. PSC_TX_A3_PREG__PSC_TX_A2_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PSC_TX_A3_PREG	R/W	2h	Bit Description 4 psc_ser_outavdd_en 3 psc_tx_drv_en 2 psc_tx_clk_en 1 psc_tx_common_mode_en 0 psc_tx_lfpsgen_clk_gate_en
15-5	RESERVED	R/W	X	
4-0	PSC_TX_A2_PREG	R/W	2h	Bit Description 4 psc_ser_outavdd_en 3 psc_tx_drv_en 2 psc_tx_clk_en 1 psc_tx_common_mode_en 0 psc_tx_lfpsgen_clk_gate_en

Table 11-324. Register Call Summary for PSC_TX_A3_PREG__PSC_TX_A2_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_TX_A3_PREG__PSC_TX_A2_PREG_j Register \(Offset = 4054h + formula\) \[reset = X\]: \[0\]](#)

11.108 PSC_TX_A5_PREG__PSC_TX_A4_PREG_j Register (Offset = 4058h + formula) [reset = X]

PSC_TX_A5_PREG__PSC_TX_A4_PREG_j is shown in [Figure 11-108](#) and described in [Table 11-326](#).

Return to [Summary Table](#).

Transmit A4 power state definition register.

Offset = 4058h + (j * 400h); where j = 0h to 1h

Table 11-325.
PSC_TX_A5_PREG__PSC_TX_A4_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4058h + formula
SERDES_16G1	0501 4058h + formula
SERDES_16G2	0502 4058h + formula
SERDES_16G3	0503 4058h + formula

Figure 11-108. PSC_TX_A5_PREG__PSC_TX_A4_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PSC_TX_A5_PREG				
R/W-X											R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PSC_TX_A4_PREG				
R/W-X											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-326. PSC_TX_A5_PREG__PSC_TX_A4_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PSC_TX_A5_PREG	R/W	0h	Bit Description 4 psc_ser_outavdd_en 3 psc_tx_drv_en 2 psc_tx_clk_en 1 psc_tx_common_mode_en 0 psc_tx_lfpngen_clk_gate_en
15-5	RESERVED	R/W	X	
4-0	PSC_TX_A4_PREG	R/W	0h	Bit Description 4 psc_ser_outavdd_en 3 psc_tx_drv_en 2 psc_tx_clk_en 1 psc_tx_common_mode_en 0 psc_tx_lfpngen_clk_gate_en

Table 11-327. Register Call Summary for PSC_TX_A5_PREG__PSC_TX_A4_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_TX_A5_PREG__PSC_TX_A4_PREG_j Register \(Offset = 4058h + formula\) \[reset = X\]: \[0\]](#)

11.109 PSC_TX_IDLE_PREG_j Register (Offset = 405Ch + formula) [reset = X]

PSC_TX_IDLE_PREG_j is shown in Figure 11-109 and described in Table 11-329.

Return to [Summary Table](#).

Transmit idle power state definition register.

Offset = 405Ch + (j * 400h); where j = 0h to 1h

Table 11-328. PSC_TX_IDLE_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 405Ch + formula
SERDES_16G1	0501 405Ch + formula
SERDES_16G2	0502 405Ch + formula
SERDES_16G3	0503 405Ch + formula

Figure 11-109. PSC_TX_IDLE_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PSC_TX_IDLE_PREG			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-329. PSC_TX_IDLE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	PSC_TX_IDLE_PREG	R/W	0h	Bit Description 4 psc_ser_outavdd_en 3 psc_tx_drv_en 2 psc_tx_clk_en 1 psc_tx_common_mode_en 0 psc_tx_lfpngen_clk_gate_en

Table 11-330. Register Call Summary for PSC_TX_IDLE_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_TX_IDLE_PREG_j Register \(Offset = 405Ch + formula\) \[reset = X\]: \[0\]](#)

11.110 PSC_RX_A1_PREG_PSC_RX_A0_PREG_j Register (Offset = 4060h + formula) [reset = X]

PSC_RX_A1_PREG_PSC_RX_A0_PREG_j is shown in Figure 11-110 and described in Table 11-332.

Return to [Summary Table](#).

Receive A0 power state definition register.

Offset = 4060h + (j * 400h); where j = 0h to 1h

Table 11-331.
PSC_RX_A1_PREG_PSC_RX_A0_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4060h + formula
SERDES_16G1	0501 4060h + formula
SERDES_16G2	0502 4060h + formula
SERDES_16G3	0503 4060h + formula

Figure 11-110. PSC_RX_A1_PREG_PSC_RX_A0_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				PSC_RX_A1_PREG			
R/W-X				R/W-FFEh			
23	22	21	20	19	18	17	16
PSC_RX_A1_PREG							
R/W-FFEh							
15	14	13	12	11	10	9	8
RESERVED				PSC_RX_A0_PREG			
R/W-X				R/W-1FFEh			
7	6	5	4	3	2	1	0
PSC_RX_A0_PREG							
R/W-1FFEh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-332. PSC_RX_A1_PREG_PSC_RX_A0_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PSC_RX_A1_PREG	R/W	FFEh	Bit Description 13 psc_sigdet_ext_mask 12 psc_rxmrgn_en 11 psc_ctleclk_en 10 psc_cksmp_en 9 psc_cpi_en 8 psc_amp_en 7 psc_idac_en 6 psc_sum_en 5 psc_vga_en 4 psc_smp_en 3 psc_dpi_en 2 psc_epi_en 1 psc_rx_sig_det_en 0 psc_rx_lfps_det_en
15-14	RESERVED	R/W	X	

Table 11-332. PSC_RX_A1_PREG__PSC_RX_A0_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-0	PSC_RX_A0_PREG	R/W	1FFEH	Bit Description 13 psc_sigdet_ext_mask 12 psc_rxmrgn_en 11 psc_ctleclk_en 10 psc_cksmp_en 9 psc_cpi_en 8 psc_amp_en 7 psc_idac_en 6 psc_sum_en 5 psc_vga_en 4 psc_smp_en 3 psc_dpi_en 2 psc_epi_en 1 psc_rx_sig_det_en 0 psc_rx_lfps_det_en

Table 11-333. Register Call Summary for PSC_RX_A1_PREG__PSC_RX_A0_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_RX_A1_PREG__PSC_RX_A0_PREG_j Register \(Offset = 4060h + formula\) \[reset = X\]: \[0\]](#)

11.111 PSC_RX_A3_PREG__PSC_RX_A2_PREG_j Register (Offset = 4064h + formula) [reset = X]

PSC_RX_A3_PREG__PSC_RX_A2_PREG_j is shown in Figure 11-111 and described in Table 11-335.

Return to [Summary Table](#).

Receive A2 power state definition register.

Offset = 4064h + (j * 400h); where j = 0h to 1h

Table 11-334.
PSC_RX_A3_PREG__PSC_RX_A2_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4064h + formula
SERDES_16G1	0501 4064h + formula
SERDES_16G2	0502 4064h + formula
SERDES_16G3	0503 4064h + formula

Figure 11-111. PSC_RX_A3_PREG__PSC_RX_A2_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				PSC_RX_A3_PREG			
R/W-X				R/W-2000h			
23	22	21	20	19	18	17	16
PSC_RX_A3_PREG							
R/W-2000h							
15	14	13	12	11	10	9	8
RESERVED				PSC_RX_A2_PREG			
R/W-X				R/W-2h			
7	6	5	4	3	2	1	0
PSC_RX_A2_PREG							
R/W-2h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-335. PSC_RX_A3_PREG__PSC_RX_A2_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PSC_RX_A3_PREG	R/W	2000h	Bit Description 13 psc_sigdet_ext_mask 12 psc_rxmrgn_en 11 psc_ctleclk_en 10 psc_cksmp_en 9 psc_cpi_en 8 psc_amp_en 7 psc_idac_en 6 psc_sum_en 5 psc_vga_en 4 psc_smp_en 3 psc_dpi_en 2 psc_epi_en 1 psc_rx_sig_det_en 0 psc_rx_lfps_det_en
15-14	RESERVED	R/W	X	

Table 11-335. PSC_RX_A3_PREG__PSC_RX_A2_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-0	PSC_RX_A2_PREG	R/W	2h	Bit Description 13 psc_sigdet_ext_mask 12 psc_rxmrgn_en 11 psc_ctleclk_en 10 psc_cksmp_en 9 psc_cpi_en 8 psc_amp_en 7 psc_idac_en 6 psc_sum_en 5 psc_vga_en 4 psc_smp_en 3 psc_dpi_en 2 psc_epi_en 1 psc_rx_sig_det_en 0 psc_rx_lfps_det_en

Table 11-336. Register Call Summary for PSC_RX_A3_PREG__PSC_RX_A2_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_RX_A3_PREG__PSC_RX_A2_PREG_j Register \(Offset = 4064h + formula\) \[reset = X\]: \[0\]](#)

11.112 PSC_RX_A5_PREG__PSC_RX_A4_PREG_j Register (Offset = 4068h + formula) [reset = X]

PSC_RX_A5_PREG__PSC_RX_A4_PREG_j is shown in Figure 11-112 and described in Table 11-338.

Return to [Summary Table](#).

Receive A4 power state definition register.

Offset = 4068h + (j * 400h); where j = 0h to 1h

Table 11-337.
PSC_RX_A5_PREG__PSC_RX_A4_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4068h + formula
SERDES_16G1	0501 4068h + formula
SERDES_16G2	0502 4068h + formula
SERDES_16G3	0503 4068h + formula

Figure 11-112. PSC_RX_A5_PREG__PSC_RX_A4_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				PSC_RX_A5_PREG			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
PSC_RX_A5_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				PSC_RX_A4_PREG			
R/W-X				R/W-2000h			
7	6	5	4	3	2	1	0
PSC_RX_A4_PREG							
R/W-2000h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-338. PSC_RX_A5_PREG__PSC_RX_A4_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PSC_RX_A5_PREG	R/W	0h	Bit Description 13 psc_sigdet_ext_mask 12 psc_rxmrgn_en 11 psc_ctleclk_en 10 psc_cksmp_en 9 psc_cpi_en 8 psc_amp_en 7 psc_idac_en 6 psc_sum_en 5 psc_vga_en 4 psc_smp_en 3 psc_dpi_en 2 psc_epi_en 1 psc_rx_sig_det_en 0 psc_rx_lfps_det_en
15-14	RESERVED	R/W	X	

Table 11-338. PSC_RX_A5_PREG__PSC_RX_A4_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-0	PSC_RX_A4_PREG	R/W	2000h	Bit Description 13 psc_sigdet_ext_mask 12 psc_rxmrgn_en 11 psc_ctleclk_en 10 psc_cksmp_en 9 psc_cpi_en 8 psc_amp_en 7 psc_idac_en 6 psc_sum_en 5 psc_vga_en 4 psc_smp_en 3 psc_dpi_en 2 psc_epi_en 1 psc_rx_sig_det_en 0 psc_rx_lfps_det_en

Table 11-339. Register Call Summary for PSC_RX_A5_PREG__PSC_RX_A4_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_RX_A5_PREG__PSC_RX_A4_PREG_j Register \(Offset = 4068h + formula\) \[reset = X\]: \[0\]](#)

11.113 PSC_RX_IDLE_PREG_j Register (Offset = 406Ch + formula) [reset = X]

PSC_RX_IDLE_PREG_j is shown in Figure 11-113 and described in Table 11-341.

Return to [Summary Table](#).

Receive Idle power state definition register.

Offset = 406Ch + (j * 400h); where j = 0h to 1h

Table 11-340. PSC_RX_IDLE_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 406Ch + formula
SERDES_16G1	0501 406Ch + formula
SERDES_16G2	0502 406Ch + formula
SERDES_16G3	0503 406Ch + formula

Figure 11-113. PSC_RX_IDLE_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PSC_RX_IDLE_PREG													
R/W-X		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-341. PSC_RX_IDLE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	PSC_RX_IDLE_PREG	R/W	0h	Bit Description 13 psc_sigdet_ext_mask 12 psc_rxmrgn_en 11 psc_ctleclk_en 10 psc_cksmp_en 9 psc_cpi_en 8 psc_amp_en 7 psc_idac_en 6 psc_sum_en 5 psc_vga_en 4 psc_smp_en 3 psc_dpi_en 2 psc_epi_en 1 psc_rx_sig_det_en 0 psc_rx_lfps_det_en

Table 11-342. Register Call Summary for PSC_RX_IDLE_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PSC_RX_IDLE_PREG_j Register \(Offset = 406Ch + formula\) \[reset = X\]: \[0\]](#)

11.114 PLLCTRL_FBDIV_MODE01_PREG__PLLCTRL_FBDIV_MODE23_PREG_j Register (Offset = 4070h + formula) [reset = X]

PLLCTRL_FBDIV_MODE01_PREG__PLLCTRL_FBDIV_MODE23_PREG_j is shown in Figure 11-114 and described in Table 11-344.

Return to [Summary Table](#).

PLLLN feedback divider control in standard modes 2 and 3.

Offset = 4070h + (j * 400h); where j = 0h to 1h

Table 11-343.
PLLCTRL_FBDIV_MODE01_PREG__PLLCTRL_FBDIV_MODE23_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4070h + formula
SERDES_16G1	0501 4070h + formula
SERDES_16G2	0502 4070h + formula
SERDES_16G3	0503 4070h + formula

Figure 11-114. PLLCTRL_FBDIV_MODE01_PREG__PLLCTRL_FBDIV_MODE23_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	PLLCTRL_FBDIV_MODE1_PREG						
R/W-X	R/W-1h						
23	22	21	20	19	18	17	16
RESERVED	PLLCTRL_FBDIV_MODE0_PREG						
R/W-X	R/W-1h						
15	14	13	12	11	10	9	8
RESERVED	PLLCTRL_FBDIV_MODE3_PREG						
R/W-X	R/W-4h						
7	6	5	4	3	2	1	0
RESERVED	PLLCTRL_FBDIV_MODE2_PREG						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-344. PLLCTRL_FBDIV_MODE01_PREG__PLLCTRL_FBDIV_MODE23_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PLLCTRL_FBDIV_MODE1_PREG	R/W	1h	This value sets the feedback divider ratio from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001.
23	RESERVED	R/W	X	
22-16	PLLCTRL_FBDIV_MODE0_PREG	R/W	1h	This value sets the feedback divider ratio from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000.
15	RESERVED	R/W	X	
14-8	PLLCTRL_FBDIV_MODE3_PREG	R/W	4h	This value sets the feedback divider ratio from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.
7	RESERVED	R/W	X	
6-0	PLLCTRL_FBDIV_MODE2_PREG	R/W	0h	This value sets the feedback divider ratio from the Lane Standards Decoder when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010.

**Table 11-345. Register Call Summary for
PLLCTRL_FBDIV_MODE01_PREG__PLLCTRL_FBDIV_MODE23_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PLLCTRL_FBDIV_MODE01_PREG__PLLCTRL_FBDIV_MODE23_PREG_j Register \(Offset = 4070h + formula\) \[reset = X\]: \[0\]](#)

11.115 PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j Register (Offset = 4074h + formula) [reset = X]

PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j is shown in Figure 11-115 and described in Table 11-347.

Return to [Summary Table](#).

PLLLN substrate control register.

Offset = 4074h + (j * 400h); where j = 0h to 1h

**Table 11-346. PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4074h + formula
SERDES_16G1	0501 4074h + formula
SERDES_16G2	0502 4074h + formula
SERDES_16G3	0503 4074h + formula

Figure 11-115. PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	PLLCTRL_RST_OVREN_PREG	PLLCTRL_RST_OVR_PREG	RESERVED	RESERVED	RESERVED	RESERVED	PLLCTRL_LOCKOVR_PREG
R/W-X	R/W-0h	R/W-0h	R/W-X	R/W-X	R/W-X	R/W-X	R/W-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	PLLCTRL_PLL_LC1_ANACLK0_SEL_MODE3_PREG	PLLCTRL_PLL_LC1_ANACLK0_SEL_MODE2_PREG	PLLCTRL_PLL_LC1_ANACLK0_SEL_MODE1_PREG	PLLCTRL_PLL_LC1_ANACLK0_SEL_MODE0_PREG
R/W-X	R/W-X	R/W-X	R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	PLLCTRL_SUBRATE_MODE3_PREG	RESERVED	RESERVED	RESERVED	RESERVED	PLLCTRL_SUBRATE_MODE2_PREG	RESERVED
R/W-X	R/W-0h	R/W-X	R/W-X	R/W-X	R/W-X	R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED	PLLCTRL_SUBRATE_MODE1_PREG	RESERVED	RESERVED	RESERVED	RESERVED	PLLCTRL_SUBRATE_MODE0_PREG	RESERVED
R/W-X	R/W-1h	R/W-X	R/W-X	R/W-X	R/W-X	R/W-2h	R/W-X

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-347. PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29	PLLCTRL_RSTOVREN_PREG	R/W	0h	PLLLN reset active high override enable.
28	PLLCTRL_RSTOVR_PREG	R/W	0h	When pllctrl_rstovren_preg is asserted high, this active high bit overrides the reset.
27-25	RESERVED	R/W	X	
24	PLLCTRL_LOCKOVR_PREG	R/W	0h	Forces the lock indication from the PLLIn high as enters into main digital.
23-20	RESERVED	R/W	X	

**Table 11-347. PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19	PLLCTRL_PLLLC1_ANACK0_SEL_MODE3_PREG	R/W	0h	PLLLN reference selection when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011. When asserted pllcl1_anack0 is selected. When deasserted pllcl_anack0 is selected.
18	PLLCTRL_PLLLC1_ANACK0_SEL_MODE2_PREG	R/W	0h	PLLLN reference selection when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010. When asserted pllcl1_anack0 is selected. When deasserted pllcl_anack0 is selected.
17	PLLCTRL_PLLLC1_ANACK0_SEL_MODE1_PREG	R/W	0h	PLLLN reference selection when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001. When asserted pllcl1_anack0 is selected. When deasserted pllcl_anack0 is selected.
16	PLLCTRL_PLLLC1_ANACK0_SEL_MODE0_PREG	R/W	0h	PLLLN reference selection when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000. When asserted pllcl1_anack0 is selected. When deasserted pllcl_anack0 is selected.
15-14	RESERVED	R/W	X	
13-12	PLLCTRL_SUBRATE_MO DE3_PREG	R/W	0h	This value sets the subrate divider ratio from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011. Divider ratio 2'b00 1 2'b01 2 2'b10 4 2'b11 8
11-10	RESERVED	R/W	X	
9-8	PLLCTRL_SUBRATE_MO DE2_PREG	R/W	0h	This value sets the subrate divider ratio from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010. Divider ratio 2'b00 1 2'b01 2 2'b10 4 2'b11 8
7-6	RESERVED	R/W	X	
5-4	PLLCTRL_SUBRATE_MO DE1_PREG	R/W	1h	This value sets the subrate divider ratio from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001. Divider ratio 2'b00 1 2'b01 2 2'b10 4 2'b11 8
3-2	RESERVED	R/W	X	
1-0	PLLCTRL_SUBRATE_MO DE0_PREG	R/W	2h	This value sets the subrate divider ratio from the Lane Standards Decoder when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000. Divider ratio 2'b00 1 2'b01 2 2'b10 4 2'b11 8

Table 11-348. Register Call Summary for PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j

16-G SerDes Registers <ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] PLLCTRL_GEN_A_PREG__PLLCTRL_SUBRATE_PREG_j Register (Offset = 4074h + formula) [reset = X]: [0]
--

11.116 PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j Register (Offset = 4078h + formula) [reset = X]

PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j is shown in [Figure 11-116](#) and described in [Table 11-350](#).

Return to [Summary Table](#).

PLLLN general control register B.

Offset = 4078h + (j * 400h); where j = 0h to 1h

Table 11-349. PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4078h + formula
SERDES_16G1	0501 4078h + formula
SERDES_16G2	0502 4078h + formula
SERDES_16G3	0503 4078h + formula

Figure 11-116. PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	PLLCTRL_DIGDIV_MODE3_PREG						
R/W-X	R/W-4h						
23	22	21	20	19	18	17	16
RESERVED	PLLCTRL_DIGDIV_MODE2_PREG						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
MSTR_PLLN_A AUTORST_ER ROR_FLAG	SLV_PLLN_A UTORST_ERR OR_FLAG	RESERVED	PLLCTRL_AUT ORST_DISABL E_PREG	RESERVED		PLLCTRL_AUTORST_DLY_PRE G	
R-0h	R-0h	R/W-X	R/W-0h	R/W-X		R/W-3h	
7	6	5	4	3	2	1	0
RESERVED	PLLCTRL_AUTORST_REPEAT_PREG			RESERVED	PLLCTRL_MODE_PREG		
R/W-X	R/W-2h			R/W-X	R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-350. PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PLLCTRL_DIGDIV_MOD E3_PREG	R/W	4h	PLLLN digclk divider selection when xcvr_standard_mode_in_{15:0} [2:0] is 3'b011. The divider ratio is 2*(digdiv+4).
23	RESERVED	R/W	X	
22-16	PLLCTRL_DIGDIV_MOD E2_PREG	R/W	0h	PLLLN digclk divider selection when xcvr_standard_mode_in_{15:0} [2:0] is 3'b010. The divider ratio is 2*(digdiv+4).
15	MSTR_PLLN_A AUTORST_ER ROR_FLAG	R	0h	Master lane PLLLN active high auto reset error flag. When asserted, the master lane PLLLN controller has attempted the maximum number reset attempts. This flag is reset low on the next attempt to activate the master lane PLLLN.

**Table 11-350. PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
14	SLV_PLLN_AUTORST_ERROR_FLAG	R	0h	Combined slave lanes PLLN active high auto reset error flag. When asserted, the slave PLLN controller has attempted the maximum number reset attempts. Note if any one of the slave lanes fails to lock, auto resets are forced on all slave lanes. This flag is reset low on the next attempt to activate the PLLN.
13	RESERVED	R/W	X	
12	PLLCTRL_AUTORST_DISABLE_PREG	R/W	0h	PLLN active high auto reset disable. When asserted, the PLLN Controller will not attempt to reset it should it fail to lock in the pllctrl_autorst_dly_preg selected xcvr_psmclk_ln_{15:0} clock periods.
11-10	RESERVED	R/W	X	
9-8	PLLCTRL_AUTORST_DELAY_PREG	R/W	3h	PLLN auto reset delay selection: The delay is $2^{(9+pllctrl_autorst_dly_preg)} - 2$ xcvr_psmclk_ln_{15:0} clock periods. Note this same delay is used for the master Lane PLL and the slave Lane PLLs in the Link.
7	RESERVED	R/W	X	
6-4	PLLCTRL_AUTORST_REPEAT_PREG	R/W	2h	PLLN auto reset maximum attempt selection. Number of auto resets before reporting failure. Note this same value is used for the master Lane PLL and the slave Lane PLLs in the Link.
3	RESERVED	R/W	X	
2-0	PLLCTRL_MODE_PREG	R/W	0h	PLLN operating mode as defined below: Operating mode frclk 3'b 000-3'b101 Normal srdiv 3'b110 Bypass pfdclk 3'b111 Normal srdiv

Table 11-351. Register Call Summary for PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PLLCTRL_GEN_C_PREG__PLLCTRL_GEN_B_PREG_j Register \(Offset = 4078h + formula\) \[reset = X\]: \[0\]](#)

11.117 PLLCTRL_CPGAIN_MODE_PREG__PLLCTRL_GEN_D_PREG_j Register (Offset = 407Ch + formula) [reset = X]

PLLCTRL_CPGAIN_MODE_PREG__PLLCTRL_GEN_D_PREG_j is shown in [Figure 11-117](#) and described in [Table 11-353](#).

Return to [Summary Table](#).

PLLLN general control register D.

Offset = 407Ch + (j * 400h); where j = 0h to 1h

Table 11-352. PLLCTRL_CPGAIN_MODE_PREG__PLLCTRL_GEN_D_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 407Ch + formula
SERDES_16G1	0501 407Ch + formula
SERDES_16G2	0502 407Ch + formula
SERDES_16G3	0503 407Ch + formula

Figure 11-117. PLLCTRL_CPGAIN_MODE_PREG__PLLCTRL_GEN_D_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	PLLCTRL_CPGAIN_MODE3_PREG			RESERVED	PLLCTRL_CPGAIN_MODE2_PREG		
R/W-X	R/W-4h			R/W-X	R/W-2h		
23	22	21	20	19	18	17	16
RESERVED	PLLCTRL_CPGAIN_MODE1_PREG			RESERVED	PLLCTRL_CPGAIN_MODE0_PREG		
R/W-X	R/W-3h			R/W-X	R/W-3h		
15	14	13	12	11	10	9	8
RESERVED	PLLCTRL_DIGDIV_MODE1_PREG						
R/W-X	R/W-1h						
7	6	5	4	3	2	1	0
RESERVED	PLLCTRL_DIGDIV_MODE0_PREG						
R/W-X	R/W-1h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-353. PLLCTRL_CPGAIN_MODE_PREG__PLLCTRL_GEN_D_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PLLCTRL_CPGAIN_MODE3_PREG	R/W	4h	PLLLN charge pump gain when xcvr_standard_mode_in_PLLCTRL_AUTORST_DLY_PREG is 3'b011. Nominal charge pump current (uA) 3'b000 500 3'b001 600 3'b010 700 3'b011 800 3'b100 900 3'b101 1000 3'b110 1100 3'b111 1200
27	RESERVED	R/W	X	

**Table 11-353. PLLCTRL_CPGAIN_MODE_PREG_PLLCTRL_GEN_D_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26-24	PLLCTRL_CPGAIN_MODE_PREG	R/W	2h	PLLLN charge pump gain when xcvr_standard_mode_in_PLLCTRL_AUTORST_DLY_PREG is 3'b010. Nominal charge pump current (uA) 3'b000 500 3'b001 600 3'b010 700 3'b011 800 3'b100 900 3'b101 1000 3'b110 1100 3'b111 1200
23	RESERVED	R/W	X	
22-20	PLLCTRL_CPGAIN_MODE_PREG	R/W	3h	PLLLN charge pump gain when xcvr_standard_mode_in_PLLCTRL_AUTORST_DLY_PREG is 3'b001. Nominal charge pump current (uA) 3'b000 500 3'b001 600 3'b010 700 3'b011 800 3'b100 900 3'b101 1000 3'b110 1100 3'b111 1200
19	RESERVED	R/W	X	
18-16	PLLCTRL_CPGAIN_MODE_PREG	R/W	3h	PLLLN charge pump gain when xcvr_standard_mode_in_PLLCTRL_AUTORST_DLY_PREG is 3'b000. Nominal charge pump current (uA) 3'b000 500 3'b001 600 3'b010 700 3'b011 800 3'b100 900 3'b101 1000 3'b110 1100 3'b111 1200
15	RESERVED	R/W	X	
14-8	PLLCTRL_DIGDIV_MODE_PREG	R/W	1h	PLLLN digclk divider selection when xcvr_standard_mode_in_PLLCTRL_AUTORST_DLY_PREG is 3'b001. The divider ratio is $2^{*(digdiv+4)}$.
7	RESERVED	R/W	X	
6-0	PLLCTRL_DIGDIV_MODE_PREG	R/W	1h	PLLLN digclk divider selection when xcvr_standard_mode_in_PLLCTRL_AUTORST_DLY_PREG is 3'b000. The divider ratio is $2^{*(digdiv+4)}$.

Table 11-354. Register Call Summary for PLLCTRL_CPGAIN_MODE_PREG__PLLCTRL_GEN_D_PREG_j

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] PLLCTRL_CPGAIN_MODE_PREG__PLLCTRL_GEN_D_PREG_j Register (Offset = 407Ch + formula) [reset = X]: [0]

11.118 PLLCTRL_PHASE1EN_PREG__LNCTRL_CLKRST_LN_PLLCLK_OVR_PREG_j Register (Offset = 4080h + formula) [reset = X]

PLLCTRL_PHASE1EN_PREG__LNCTRL_CLKRST_LN_PLLCLK_OVR_PREG_j is shown in Figure 11-118 and described in Table 11-356.

Return to [Summary Table](#).

Diagnostic access to cmn_sdosc_clk

Offset = 4080h + (j * 400h); where j = 0h to 1h

Table 11-355.
PLLCTRL_PHASE1EN_PREG__LNCTRL_CLKRST_LN_PLLCLK_OVR_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4080h + formula
SERDES_16G1	0501 4080h + formula
SERDES_16G2	0502 4080h + formula
SERDES_16G3	0503 4080h + formula

Figure 11-118. PLLCTRL_PHASE1EN_PREG__LNCTRL_CLKRST_LN_PLLCLK_OVR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				PLLCTRL_PHASE1EN_DLY_PREG			
R/W-X				R/W-D4h			
23	22	21	20	19	18	17	16
PLLCTRL_PHASE1EN_DLY_PREG							
R/W-D4h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							LNCTRL_CLKRST_LN_PLLCLK_OVR_EN_PREG
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-356. PLLCTRL_PHASE1EN_PREG__LNCTRL_CLKRST_LN_PLLCLK_OVR_PREG_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PLLCTRL_PHASE1EN_DLY_PREG	R/W	D4h	PLL phase1en delay time in xcvr_psmclk_ln_{15:0} periods: Note the value must be 1 or greater.
15-1	RESERVED	R/W	X	
0	LNCTRL_CLKRST_LN_PLLCLK_OVR_EN_PREG	R/W	0h	When asserted the cmn_sdosc_clk is used to source the ln_pllclk_fullrt. Note this is a diagnostic only feature aimed at providing external access to the ln_sdosc_clk through the xcvr_pllclk_fullrt_ln_{15:0} Macro pin.

**Table 11-357. Register Call Summary for
PLLCTRL_PHASE1EN_PREG__LNCTRL_CLKRST_LN_PLLCLK_OVR_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PLLCTRL_PHASE1EN_PREG__LNCTRL_CLKRST_LN_PLLCLK_OVR_PREG_j Register \(Offset = 4080h + formula\) \[reset = X\]: \[0\]](#)

11.119 PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j Register (Offset = 4084h + formula) [reset = X]

PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j is shown in Figure 11-119 and described in Table 11-359.

Return to [Summary Table](#).

PLLLN phase2 enable delay control register.

Offset = 4084h + (j * 400h); where j = 0h to 1h

Table 11-358. PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4084h + formula
SERDES_16G1	0501 4084h + formula
SERDES_16G2	0502 4084h + formula
SERDES_16G3	0503 4084h + formula

Figure 11-119. PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j Register

31	30	29	28	27	26	25	24
PLLCTRL_LFAVDDREG_VTRIM_PREG			PLLCTRL_LFAVDDREG_FWEN_N_N_PREG	RESERVED			
R/W-4h			R/W-1h	R/W-X			
23	22	21	20	19	18	17	16
RESERVED				PLLCTRL_FRAVDDREG_VTRIM_PREG		PLLCTRL_FRAVDDREG_FWEN_N_N_PREG	
R/W-X				R/W-4h		R/W-1h	
15	14	13	12	11	10	9	8
RESERVED				PLLCTRL_PHASE2EN_DLY_PREG			
R/W-X				R/W-6Ah			
7	6	5	4	3	2	1	0
PLLCTRL_PHASE2EN_DLY_PREG							
R/W-6Ah							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-359. PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	PLLCTRL_LFAVDDREG_VTRIM_PREG	R/W	4h	PLLLN low frequency block regulator voltage trim. Voltage (V) 3'b000 0.830 3'b001 0.860 3'b010 0.870 3'b011 0.890 3'b100 0.908 3'b101 0.925 3'b110 0.940 (Burn-in) 3'b111 0.940
28	PLLCTRL_LFAVDDREG_FWEN_N_N_PREG	R/W	1h	PLLLN active low firewall enable forcing for signal driven from lfavddreg power island. Note this register is for diagnostic purposes only.

**Table 11-359. PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
27-20	RESERVED	R/W	X	
19-17	PLLCTRL_FRAVDDREG_VTRIM_PREG	R/W	4h	PLLLN full rate block regulator voltage trim. Voltage (V) 3'b000 0.830 3'b001 0.860 3'b010 0.870 3'b011 0.890 3'b100 0.908 3'b101 0.925 3'b110 0.940 (Burn-in) 3'b111 0.940
16	PLLCTRL_FRAVDDREG_FWEN_N_PREG	R/W	1h	PLLLN active low firewall enable forcing for signal driven from fravddreg power island. Note this register is for diagnostic purposes only.
15-12	RESERVED	R/W	X	
11-0	PLLCTRL_PHASE2EN_DLY_PREG	R/W	6Ah	PLLLN phase2en delay time in xcvr_psmclk_In_{15:0} periods: Note the value must be 1 or greater.

Table 11-360. Register Call Summary for PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PLLCTRL_AVDDREG_PREG__PLLCTRL_PHASE2EN_PREG_j Register \(Offset = 4084h + formula\) \[reset = X\]: \[0\]](#)

11.120 PLLNC_STATUS_PREG__PLLCTRL_STATUS_PREG_j Register (Offset = 4088h + formula) [reset = X]

PLLNC_STATUS_PREG__PLLCTRL_STATUS_PREG_j is shown in Figure 11-120 and described in Table 11-362.

Return to [Summary Table](#).

PLLNC status register.

Offset = 4088h + (j * 400h); where j = 0h to 1h

Table 11-361. PLLNC_STATUS_PREG__PLLCTRL_STATUS_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4088h + formula
SERDES_16G1	0501 4088h + formula
SERDES_16G2	0502 4088h + formula
SERDES_16G3	0503 4088h + formula

Figure 11-120. PLLNC_STATUS_PREG__PLLCTRL_STATUS_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				SLV_PLLNC_STATE			
R-X				R-0h			
23	22	21	20	19	18	17	16
RESERVED				MSTR_PLLNC_STATE			
R-X				R-0h			
15	14	13	12	11	10	9	8
RESERVED							PLLCTRL_TESTOUT
R-X							R-0h
7	6	5	4	3	2	1	0
RESERVED							PLLCTRL_LOCK
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-362. PLLNC_STATUS_PREG__PLLCTRL_STATUS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-24	SLV_PLLNC_STATE	R	0h	Slave lane PLL control state machine state vector.
23-20	RESERVED	R	X	
19-16	MSTR_PLLNC_STATE	R	0h	Master lane PLL control state machine state vector.
15-9	RESERVED	R	X	
8	PLLCTRL_TESTOUT	R	0h	PLLNC digital debug output. Note this signal is not supported and is tied low.
7-1	RESERVED	R	X	
0	PLLCTRL_LOCK	R	0h	PLLNC active high lock flag.

Table 11-363. Register Call Summary for PLLLNC_STATUS_PREG__PLLCTRL_STATUS_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PLLLNC_STATUS_PREG__PLLCTRL_STATUS_PREG_j Register \(Offset = 4088h + formula\) \[reset = X\]: \[0\]](#)

11.121 LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j Register (Offset = 4090h + formula) [reset = X]

LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j is shown in Figure 11-121 and described in Table 11-365.

Return to [Summary Table](#).

Transmit loopback bias current trim register.

Offset = 4090h + (j * 400h); where j = 0h to 1h

Table 11-364. LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4090h + formula
SERDES_16G1	0501 4090h + formula
SERDES_16G2	0502 4090h + formula
SERDES_16G3	0503 4090h + formula

Figure 11-121. LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	LPBKLINEMUX_BIASTRIM_PREG			RESERVED	LPBKRCCLKMUX1_BIASTRIM_PREG		
R/W-X	R/W-3h			R/W-X	R/W-3h		
23	22	21	20	19	18	17	16
RESERVED	LPBKRCCLKMUX1_BIASTRIM_PREG			RESERVED	LPBKRCCLKMUX2_BIASTRIM_PREG		
R/W-X	R/W-3h			R/W-X	R/W-3h		
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					DRV_LPBK_BIASTRIM_PREG		
R/W-X					R/W-3h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-365. LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	LPBKLINEMUX_BIASTRIM_PREG	R/W	3h	Receive line loopback multiplexor bias current binary encoded trim: Bias current amplitude 3'b111 Lowest :: 3'b000 Highest
27	RESERVED	R/W	X	
26-24	LPBKRCCLKMUX1_BIASTRIM_PREG	R/W	3h	Receive recovered clock loopback clock path stage 1 multiplexor bias current binary encoded trim: Bias current amplitude 3'b111 Lowest :: 3'b000 Highest
23	RESERVED	R/W	X	

**Table 11-365. LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
22-20	LPBKRCCLKMUX1_BIASTRIM_PREG	R/W	3h	Receive recovered clock loopback data path stage 1 multiplexer bias current binary encoded trim: Bias current amplitude 3'b111 Lowest :: 3'b000 Highest
19	RESERVED	R/W	X	
18-16	LPBKRCCLKMUX2_BIASTRIM_PREG	R/W	3h	Receive recovered clock loopback stage 2 multiplexer bias current binary encoded trim: Bias current amplitude 3'b111 Lowest :: 3'b000 Highest
15-3	RESERVED	R/W	X	
2-0	DRV_LPBK_BIASTRIM_PREG	R/W	3h	Transmit bias current binary encoded trim shared for both serial and line/recovered clock loopbacks: Bias current amplitude 3'b111 Lowest :: 3'b000 Highest Note: The nominal setting is valid for line and recovered loopbacks. When using serial loopback, this biastrim should be changed to 3'b000.

Table 11-366. Register Call Summary for LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LOOPBACK_BIASTRIM_PREG__TX_BIASTRIM_PREG_j Register \(Offset = 4090h + formula\) \[reset = X\]: \[0\]](#)

11.122 CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j Register (Offset = 4094h + formula) [reset = X]

CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j is shown in Figure 11-122 and described in Table 11-368.

Return to [Summary Table](#).

Receive front-end bias current trim register

Offset = 4094h + (j * 400h); where j = 0h to 1h

**Table 11-367. CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4094h + formula
SERDES_16G1	0501 4094h + formula
SERDES_16G2	0502 4094h + formula
SERDES_16G3	0503 4094h + formula

Figure 11-122. CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							CTLECLK_MAI NBIASSTRIM_P REG
R/W-X							R/W-4h
23	22	21	20	19	18	17	16
CTLECLK_MAINBIASSTRIM_P REG		CTLECLK_INDBIASSTRIM_PREG			CKSMP_BIASTRIM_PREG		
R/W-4h		R/W-3h			R/W-2h		
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						RXBUFFER_BIASTRIM_PREG	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-368. CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-22	CTLECLK_MAINBIASSTRIM_PREG	R/W	4h	Receive clock path clock CTLE main path bias current binary encoded trim: Bias current amplitude 3'b111 Highest :: 3'b000 Lowest
21-19	CTLECLK_INDBIASSTRIM_PREG	R/W	3h	Receive clock path clock CTLE inductor circuitry bias current binary encoded trim: Bias current amplitude 3'b111 Highest :: 3'b000 Lowest

**Table 11-368. CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
18-16	CKSMP_BIASTRIM_PREG	R/W	2h	Receive clock path clock sampler bias current binary encoded trim: Bias current amplitude 3'b111 Lowest :: 3'b000 Highest
15-2	RESERVED	R/W	X	
1-0	RXBUFFER_BIASTRIM_PREG	R/W	0h	Receive buffer bias current binary encoded trim. This is thermometer encoded before passing to analog as rxda_rxbuffer_biastrim[2:0] as follows: Thermometer encoding Amplitude 2'b00 3'b000 Highest 2'b01 3'b001 : 2'b10 3'b011 : 2'b11 3'b111 Lowest Note: This function has been deprecated. The signal is not connected in the analog.

Table 11-369. Register Call Summary for CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CLKPATH_BIASTRIM_PREG__RXFE_BIASTRIM_PREG_j Register \(Offset = 4094h + formula\) \[reset = X\]: \[0\]](#)

11.123 DFE_BIASTRIM_PREG_j Register (Offset = 4098h + formula) [reset = X]

DFE_BIASTRIM_PREG_j is shown in Figure 11-123 and described in Table 11-371.

Return to [Summary Table](#).

Receive data path DFE bias current trim register.

Offset = 4098h + (j * 400h); where j = 0h to 1h

Table 11-370. DFE_BIASTRIM_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4098h + formula
SERDES_16G1	0501 4098h + formula
SERDES_16G2	0502 4098h + formula
SERDES_16G3	0503 4098h + formula

Figure 11-123. DFE_BIASTRIM_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
SMP_BIASTRIM_PREG				IDAC_BIASTRIM_PREG			
R/W-1h				R/W-5h			
7	6	5	4	3	2	1	0
SUM_BIASTRIM_PREG				AMP_BIASTRIM_PREG			
R/W-5h				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-371. DFE_BIASTRIM_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-12	SMP_BIASTRIM_PREG	R/W	1h	Receive data path DFE sampler bias current binary encoded trim: Bias current amplitude 4'b1111 Lowest :: 4'b0000 Highest
11-8	IDAC_BIASTRIM_PREG	R/W	5h	Receive data path DFE current DAC bias current binary encoded trim: Bias current amplitude 4'b1111 Lowest :: 4'b0000 Highest
7-4	SUM_BIASTRIM_PREG	R/W	5h	Receive data path DFE summer bias current binary encoded trim: Bias current amplitude 4'b1111 Lowest :: 4'b0000 Highest

Table 11-371. DFE_BIASTRIM_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AMP_BIASTRIM_PREG	R/W	1h	Receive data path DFE amplifier bias current binary encoded trim: Bias current amplitude 4'b1111 Lowest :: 4'b0000 Highest

Table 11-372. Register Call Summary for DFE_BIASTRIM_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DFE_BIASTRIM_PREG_j Register \(Offset = 4098h + formula\) \[reset = X\]: \[0\]](#)

11.124 BSCAN_LPBKLINE_PREG_LANE_LOOPBACK_CTRL_PREG_j Register (Offset = 40A0h + formula) [reset = X]

BSCAN_LPBKLINE_PREG_LANE_LOOPBACK_CTRL_PREG_j is shown in Figure 11-124 and described in Table 11-374.

Return to [Summary Table](#).

Local Lane loopback control register.

Offset = 40A0h + (j * 400h); where j = 0h to 1h

Table 11-373. BSCAN_LPBKLINE_PREG_LANE_LOOPBACK_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40A0h + formula
SERDES_16G1	0501 40A0h + formula
SERDES_16G2	0502 40A0h + formula
SERDES_16G3	0503 40A0h + formula

Figure 11-124. BSCAN_LPBKLINE_PREG_LANE_LOOPBACK_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						BSCAN_LPBKLINE_ZTPSEL_PREG	BSCAN_LPBKLINE_EN_PREG
R/W-X						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
LPBKNEPAR_D IGONLY_PREG	LPBKSER_DRVTRIM_PREG			LPBKSERRCV_BIASTRIM_PREG			LPBKLINEMUX_CLKSEL_PREG
R/W-0h	R/W-0h			R/W-3h			R/W-0h
7	6	5	4	3	2	1	0
LPBKRCCLKM UX1_QCLKSEL_PREG	LPBKRCCLKM UX1_EPISSEL_PREG	LPBKRCCLKM UX2_DCLKSEL_PREG	LPBKRCCLKEN_PREG	LPBKLINEEN_PREG	LPBKSEREN_PREG	LPBKNEPAREN_PREG	LPBKFEAREN_PREG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-374. BSCAN_LPBKLINE_PREG_LANE_LOOPBACK_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	BSCAN_LPBKLINE_ZTPSEL_PREG	R/W	0h	Multiplexor selection for which boundary scan receiver is looped back: Receiver looped back 1'b0 rxda_bscan_ztn 1'b1 rxda_bscan_ztp
16	BSCAN_LPBKLINE_EN_PREG	R/W	0h	Active high enable for boundary scan receiver to driver line loopback.

**Table 11-374. BSCAN_LPBKLINE_PREG_LANE_LOOPBACK_CTRL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15	LPBKNEPAR_DIGONLY_PREG	R/W	0h	Active high digital only version of Near-end parallel loopback requiring no analog support other than reference clock reception. Note: This feature is deprecated in PMA revisions R400 and later. In these revisions, this field should remain at the default value of 1'b0.
14-12	LPBKSER_DRVTRIM_PREG	R/W	0h	Trim setting for txana_lpbkser in serial loopback path: drvtrim_preg [2:0] Description 3'b111 Low current:closed-eye : 3'b000 High current:open-eye
11-9	LPBKSERRCV_BIASTRIM_PREG	R/W	3h	Bias trim setting for rxana_lpbkserrcv in serial loopback path: biastrim_preg[2:0] Bias current amplitude 3'b111 Lowest :: 3'b011 Nominal :: 3'b000 Highest
8	LPBKLINEMUX_CLKSEL_PREG	R/W	0h	Line loopback source selection: Path Selected 0 Data path from rxana_dfe_vga 1 Clock path from rxana_ctleclk
7	LPBKRCLKCMUX1_QCLKSEL_PREG	R/W	0h	Recovered clock loopback clock path mux stage 1 selection: Path Selected 0 CPI I clock phase 1 CPI Q clock phase
6	LPBKRCLKDMUX1_EPISSEL_PREG	R/W	0h	Recovered clock loopback data path mux stage 1 selection: Path Selected 0 DPI clock 1 EPI clock
5	LPBKRCLKDMUX2_DCLKSEL_PREG	R/W	0h	Recovered clock loopback mux stage 2 selection: Path Selected 0 clock path mux stage 1 1 data path mux stage 1
4	LPBKRCLKEN_PREG	R/W	0h	Recovered clock loopback active high enable: When asserted the Transmitter drives a selectable version of the receiver recovered clock out on the tx_p/m_In_{15:0} pins.
3	LPBKLINEEN_PREG	R/W	0h	Line side loopback active high enable: When asserted the Transmitter drives a selectable version of the received serial stream prior to clock and data recovery out on the tx_p/m_In_{15:0} pins.
2	LPBKSEREN_PREG	R/W	0h	Serial loopback active high enable: When asserted the receiver path sees the transmitted serial stream rather than rx_p/m_In_{15:0} pins.
1	LPBKNEPAREN_PREG	R/W	0h	Near end parallel loopback active high enable: When asserted the receiver parallel data path is driven by the transmitter parallel data path.

Table 11-374. BSCAN_LPBKLINE_PREG__LANE_LOOPBACK_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LPBKFEPAEN_PREG	R/W	0h	Far end parallel loopback active high enable: When asserted the transmitter parallel data path is driven by the receiver parallel data path.

Table 11-375. Register Call Summary for BSCAN_LPBKLINE_PREG__LANE_LOOPBACK_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [BSCAN_LPBKLINE_PREG__LANE_LOOPBACK_CTRL_PREG_j Register \(Offset = 40A0h + formula\) \[reset = X\]: \[0\]](#)

11.125 TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j Register (Offset = 40A8h + formula) [reset = X]

TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j is shown in Figure 11-125 and described in Table 11-377.

Return to [Summary Table](#).

TX sync FIFO diagnostic control register

Offset = 40A8h + (j * 400h); where j = 0h to 1h

Table 11-376. TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j Instances

Instance	Physical Address
SERDES_16G0	0500 40A8h + formula
SERDES_16G1	0501 40A8h + formula
SERDES_16G2	0502 40A8h + formula
SERDES_16G3	0503 40A8h + formula

Figure 11-125. TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j Register

31	30	29	28	27	26	25	24
RESERVED		TX_SFIFO_ALIGN_SETTLE_DEL_PREG					
R/W-X		R/W-6h					
23	22	21	20	19	18	17	16
RESERVED		TX_SFIFO_ALIGN_DETECT_DEL_PREG					
R/W-X		R/W-Ch					
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
TX_SFIFO_SYNC_REG_MODE_EN_PREG	TX_SFIFO_EROR_STICKY_BIT	TX_SFIFO_EROR_STICKY_BIT_CLR_PREG	TX_SFIFO_ENQ_PTR_BUMP_PREG	TX_SFIFO_EROR	TX_SFIFO_ALIGN_ACK	TX_SFIFO_ALIGN_EN_OVRD_EN_PREG	TX_SFIFO_ALIGN_EN_OVRD_PREG
R/W-0h	R-0h	W-0h	R/W-0h	R-1h	R-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-377. TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	TX_SFIFO_ALIGN_SETTLE_DEL_PREG	R/W	6h	FIFO alignment settle delay: This field specifies the number of clocks to wait for a prior change to the enqueue pointer to complete before initiating the check phase of the alignment procedure in the sync FIFO. It drives the fifo_align_settle_del pin of the FIFO.
23-22	RESERVED	R/W	X	
21-16	TX_SFIFO_ALIGN_DETECT_DEL_PREG	R/W	Ch	FIFO alignment detect delay: This field specifies the number of clocks to wait in the delay state for each phase of the alignment procedure in the sync FIFO. It drives the fifo_align_detect_del pin of the FIFO.
15-8	RESERVED	R/W	X	
7	TX_SFIFO_SYNC_REG_MODE_EN_PREG	R/W	0h	1'b 0 : Normal FIFO operation. 1'b 1 : Sync reg mode, where the FIFO is implemented as a single register clocked by the enq_clk.

Table 11-377. TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TX_SFIFO_ERROR_STICKY_BIT	R	0h	Sticky FIFO alignment error: This bit asserts anytime fifo_error (bit3 below) is asserted and remains set until fifo_error_sticky_bit_clr_preg is written high or the link is reset. Note: When this is observed asserted, it is recommended to clear this bit first and then read again as it may be set during fifo alignment process.
5	TX_SFIFO_ERROR_STICKY_BIT_CLR_PREG	W	0h	Sticky FIFO alignment error clear: Writing this bit high clears the fifo_error_sticky_bit above.
4	TX_SFIFO_ENQ_PTR_BUMP_PREG	R/W	0h	FIFO enqueue pointer bump: This bit can be used to decrement the enqueue pointer relative to the dequeue pointer, for diagnostic purposes. Changing this bit from a value of 1'b0 to 1'b1 will trigger a single decrement of the enqueue pointer.
3	TX_SFIFO_ERROR	R	1h	FIFO alignment error: This bit indicates if a FIFO overflow or FIFO underflow condition currently exists. Note that during the FIFO alignment process, this bit will toggle. This bit is driven directly by the fifo_error pin of the FIFO. Note that this bit is 1'b0 in reset because the FIFO alignment process has not been initiated, and the enqueue and dequeue pointers are set to the same value at this time.
2	TX_SFIFO_ALIGN_ACK	R	0h	FIFO alignment acknowledge: This bit indicates that the FIFO alignment process is complete, as initiated either automatically by the hardware of the FIFO alignment enable override bits in this register. This bit is driven directly by the fifo_align_ack pin of the FIFO.
1	TX_SFIFO_ALIGN_EN_OVERRIDE_PREG	R/W	0h	FIFO alignment enable override enable: This bit enables the FIFO alignment enable override register to drive the fifo_align_en pin of the FIFO directly for diagnostic purposes. 1'b 1: Override enabled 1'b 0: Override disabled
0	TX_SFIFO_ALIGN_EN_OVERRIDE_PREG	R/W	0h	FIFO alignment enable override: When enabled by the FIFO alignment enable override enable bit in this register, this bit directly controls the fifo_align_en pin of the FIFO to provide a means of running the FIFO alignment function for diagnostic purposes.

Table 11-378. Register Call Summary for TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j Register \(Offset = 40A8h + formula\) \[reset = X\]: \[0\]](#)

11.126 TX_LOWLAT_CTRL_PREG_j Register (Offset = 40ACh + formula) [reset = X]

TX_LOWLAT_CTRL_PREG_j is shown in Figure 11-126 and described in Table 11-380.

Return to [Summary Table](#).

Ultra low latency mode control register

Offset = 40ACh + (j * 400h); where j = 0h to 1h

Table 11-379. TX_LOWLAT_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40ACh + formula
SERDES_16G1	0501 40ACh + formula
SERDES_16G2	0502 40ACh + formula
SERDES_16G3	0503 40ACh + formula

Figure 11-126. TX_LOWLAT_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					TX_SER_SLIP4_PREG	RX_LOW_LATE_NCY_PREG	TX_LOW_LATE_NCY_PREG
R/W-X					W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-380. TX_LOWLAT_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2	TX_SER_SLIP4_PREG	W	0h	Serializer slip by 4UI request: Writing a 1 to this field will result in the transmit word clock, tx_td_clk_out_in_{15:0} experiencing a single clock period with 8UI high, 8UI low, effectively slipping by 4UI. This clock will not glitch during this slip. Note: This function is only supported when tx_low_latency_preg is asserted. Note: This function is only supported with xcvr_data_width_in_{15:0} = 3'b101 (20-bit)
1	RX_LOW_LATENCY_PREG	R/W	0h	Receive ultra-low latency mode enable: When asserted, the data path latency would be reduced in the Receive path. Note: This mode is only supported in with xcvr_data_width_in_{15:0} [2:0] = 3'b101.

Table 11-380. TX_LOWLAT_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TX_LOW_LATENCY_PREG	R/W	0h	<p>Transmit ultra-low latency mode enable: When asserted, the data path latency would be reduced in the Transmit path.</p> <p>Note: This mode is only supported in with xcvr_data_width_ln_{15:0}[2:0] = 3'b101.</p> <p>Note: tx_td_ln_{15:0}[19:0] input data for transmit will be synchronous to tx_td_clk_out_ln_{15:0} in this mode.</p>

Table 11-381. Register Call Summary for TX_LOWLAT_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [TX_LOWLAT_CTRL_PREG_j Register \(Offset = 40ACh + formula\) \[reset = X\]: \[0\]](#)

11.127 TX_ELEC_IDLE_PREG_j Register (Offset = 40B0h + formula) [reset = X]

TX_ELEC_IDLE_PREG_j is shown in Figure 11-127 and described in Table 11-383.

Return to [Summary Table](#).

Transmit electrical idle control register.

Offset = 40B0h + (j * 400h); where j = 0h to 1h

Table 11-382. TX_ELEC_IDLE_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40B0h + formula
SERDES_16G1	0501 40B0h + formula
SERDES_16G2	0502 40B0h + formula
SERDES_16G3	0503 40B0h + formula

Figure 11-127. TX_ELEC_IDLE_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED					TX_ELEC_IDLE_ENTRY_DLY_PREG		
R/W-X					R/W-3h		
7	6	5	4	3	2	1	0
TX_ELEC_IDLE_EXIT_DLY_PREG				RESERVED			
R/W-3h				R/W-X			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-383. TX_ELEC_IDLE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-8	TX_ELEC_IDLE_ENTRY_DLY_PREG	R/W	3h	Transmit path electrical idle entry programmable delay: tx_elec_idle_entry_dly_preg controls the amount of additional delay added to the electrical idle signal after the sync FIFO when entering the electrical idle state. tx_td_clk_ln_{15:0} periods 3'b000 0.0 3'b001 0.5 3'b010 1.0 3'b011 1.5 3'b100 2.0 3'b101 2.5 3'b110 3.0 3'b111 3.5

Table 11-383. TX_ELEC_IDLE_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-5	TX_ELEC_IDLE_EXIT_DLY_PREG	R/W	3h	<p>Transmit path electrical idle exit programmable delay: tx_elec_idle_exit_dly_preg controls the amount of additional delay added to the electrical idle signal after the sync FIFO when exiting the electrical idle state.</p> <p>tx_td_clk_ln_{15:0} periods</p> <p>3'b000 0.0</p> <p>3'b001 0.5</p> <p>3'b010 1.0</p> <p>3'b011 1.5</p> <p>3'b100 2.0</p> <p>3'b101 2.5</p> <p>3'b110 3.0</p> <p>3'b111 3.5</p>
4-0	RESERVED	R/W	X	

Table 11-384. Register Call Summary for TX_ELEC_IDLE_PREG_j

- 16-G SerDes Registers
- [2-L SerDes Registers: \[0\] \[1\]](#)
 - [TX_ELEC_IDLE_PREG_j Register \(Offset = 40B0h + formula\) \[reset = X\]: \[0\]](#)

11.128 TX_SER_LOADDELAY_PREG_j Register (Offset = 40B4h + formula) [reset = X]

TX_SER_LOADDELAY_PREG_j is shown in Figure 11-128 and described in Table 11-386.

Return to [Summary Table](#).

Tx serializer load delay control register.

Offset = 40B4h + (j * 400h); where j = 0h to 1h

**Table 11-385. TX_SER_LOADDELAY_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 40B4h + formula
SERDES_16G1	0501 40B4h + formula
SERDES_16G2	0502 40B4h + formula
SERDES_16G3	0503 40B4h + formula

Figure 11-128. TX_SER_LOADDELAY_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			TX_SER_LOAD DELAY_MODE 3_PREG	RESERVED			TX_SER_LOAD DELAY_MODE 2_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h
7	6	5	4	3	2	1	0
RESERVED			TX_SER_LOAD DELAY_MODE 1_PREG	RESERVED			TX_SER_LOAD DELAY_MODE 0_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-386. TX_SER_LOADDELAY_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12	TX_SER_LOADDELAY_M ODE3_PREG	R/W	0h	Analog Serializer parallel data load delay. Asserting this bit is required for word clock rates over 800MHz to meet self-aligning FIFO to Serializer timing. Note that assertion of the bit incurs an additional 4UI of latency through the data path. This value will be selected from the Lane Standards Decoder when xcvr_standard_mode_ln{15:0}[2:0] is 3'b011.
11-9	RESERVED	R/W	X	

Table 11-386. TX_SER_LOADDELAY_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TX_SER_LOADDELAY_MODE2_PREG	R/W	0h	Analog Serializer parallel data load delay. Asserting this bit is required for word clock rates over 800MHz to meet self-aligning FIFO to Serializer timing. Note that assertion of the bit incurs an additional 4UI of latency through the data path. This value will be selected from the Lane Standards Decoder when xcvr_standard_mode_in{15:0}[2:0] is 3'b010.
7-5	RESERVED	R/W	X	
4	TX_SER_LOADDELAY_MODE1_PREG	R/W	0h	Analog Serializer parallel data load delay. Asserting this bit is required for word clock rates over 800MHz to meet self-aligning FIFO to Serializer timing. Note that assertion of the bit incurs an additional 4UI of latency through the data path. This value will be selected from the Lane Standards Decoder when xcvr_standard_mode_in{15:0}[2:0] is 3'b001.
3-1	RESERVED	R/W	X	
0	TX_SER_LOADDELAY_MODE0_PREG	R/W	0h	Analog Serializer parallel data load delay. Asserting this bit is required for word clock rates over 800MHz to meet self-aligning FIFO to Serializer timing. Note that assertion of the bit incurs an additional 4UI of latency through the data path. This value will be selected from the Lane Standards Decoder when xcvr_standard_mode_in{15:0}[2:0] is 3'b000.

Table 11-387. Register Call Summary for TX_SER_LOADDELAY_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [TX_SER_LOADDELAY_PREG_j Register \(Offset = 40B4h + formula\) \[reset = X\]: \[0\]](#)

11.129 TX_HSRSM_STATUS_PREG_j Register (Offset = 40B8h + formula) [reset = X]

TX_HSRSM_STATUS_PREG_j is shown in Figure 11-129 and described in Table 11-389.

Return to [Summary Table](#).

Transmit high speed reset release state machine status register.

Offset = 40B8h + (j * 400h); where j = 0h to 1h

**Table 11-388. TX_HSRSM_STATUS_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 40B8h + formula
SERDES_16G1	0501 40B8h + formula
SERDES_16G2	0502 40B8h + formula
SERDES_16G3	0503 40B8h + formula

Figure 11-129. TX_HSRSM_STATUS_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											TX_HSRSM_STATE				
R-X											R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 11-389. TX_HSRSM_STATUS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	X	
4-0	TX_HSRSM_STATE	R	0h	Transmit high speed reset release state machine state vector

Table 11-390. Register Call Summary for TX_HSRSM_STATUS_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [TX_HSRSM_STATUS_PREG_j Register \(Offset = 40B8h + formula\) \[reset = X\]: \[0\]](#)

11.130 DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j Register (Offset = 40C0h + formula) [reset = X]

DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j is shown in Figure 11-130 and described in Table 11-392.

Return to [Summary Table](#).

Transmit driver local preset pre-emphasis cursor override register.

Offset = 40C0h + (j * 400h); where j = 0h to 1h

Table 11-391.
DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40C0h + formula
SERDES_16G1	0501 40C0h + formula
SERDES_16G2	0502 40C0h + formula
SERDES_16G3	0503 40C0h + formula

Figure 11-130. DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							DRVCTRL_PRESET_C0_OVRD_EN_PREG
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED		DRVCTRL_PRESET_C0_OVRD_VAL_PREG					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED							DRVCTRL_PRESET_CM1_OVRD_EN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		DRVCTRL_PRESET_CM1_OVRD_VAL_PREG					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-392. DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DRVCTRL_PRESET_C0_OVRD_EN_PREG	R/W	0h	Local preset main cursor active high override enable.
23-22	RESERVED	R/W	X	
21-16	DRVCTRL_PRESET_C0_OVRD_VAL_PREG	R/W	0h	When drvctrl_preset_c0_ovrd_en_preg is asserted high, this value overrides the internally generated value for tx_local_tx_preset_coef_ln_{15:0} [11:6] following a tx_get_local_preset_coef_ln_{15:0} request.
15-9	RESERVED	R/W	X	

Table 11-392. DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	DRVCTRL_PRESET_CM1_OVRD_EN_PREG	R/W	0h	Local preset pre-emphasis cursor active high override enable.
7-6	RESERVED	R/W	X	
5-0	DRVCTRL_PRESET_CM1_OVRD_VAL_PREG	R/W	0h	When drvctrl_preset_cm1_ovrd_en_preg is asserted high, this value overrides the internally generated value for tx_local_tx_preset_coef_ln_{15:0} [5:0] following a tx_get_local_preset_coef_ln_{15:0} request.

**Table 11-393. Register Call Summary for
DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j**

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] DRVCTRL_PRESET_C0_OVRD_PREG__DRVCTRL_PRESET_CM1_OVRD_PREG_j Register (Offset = 40C0h + formula) [reset = X]: [0]

11.131 DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j Register (Offset = 40C4h + formula) [reset = X]

DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j is shown in Figure 11-131 and described in Table 11-395.

Return to [Summary Table](#).

Transmit driver local preset post-emphasis cursor override register.

Offset = 40C4h + (j * 400h); where j = 0h to 1h

Table 11-394.
DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 40C4h + formula
SERDES_16G1	0501 40C4h + formula
SERDES_16G2	0502 40C4h + formula
SERDES_16G3	0503 40C4h + formula

Figure 11-131. DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							DRVCTRL_INIT_CM1_OVRD_EN_PREG
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED		DRVCTRL_INIT_CM1_OVRD_VAL_PREG					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED							DRVCTRL_PRESET_CP1_OVRD_EN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		DRVCTRL_PRESET_CP1_OVRD_VAL_PREG					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-395. DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DRVCTRL_INIT_CM1_OVRD_EN_PREG	R/W	0h	Local init pre-emphasis cursor active high override enable.
23-22	RESERVED	R/W	X	
21-16	DRVCTRL_INIT_CM1_OVRD_VAL_PREG	R/W	0h	When drvctrl_init_cm1_ovrd_en_preg is asserted high, this value overrides the internally generated value for tx_local_tx_preset_coef_in_{15:0} [5:0] following a tx_get_local_init_coef_in_{15:0} request.
15-9	RESERVED	R/W	X	
8	DRVCTRL_PRESET_CP1_OVRD_EN_PREG	R/W	0h	Local preset post-emphasis cursor active high override enable.

**Table 11-395. DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j Register
Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	DRVCTRL_PRESET_CP1_OVRD_VAL_PREG	R/W	0h	When drvctrl_preset_cp1_ovrd_en_preg is asserted high, this value overrides the internally generated value for tx_local_tx_preset_coef_ln_{15:0} [17:12] following a tx_get_local_preset_coef_ln_{15:0} request.

**Table 11-396. Register Call Summary for
DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DRVCTRL_INIT_CM1_OVRD_PREG__DRVCTRL_PRESET_CP1_OVRD_PREG_j Register \(Offset = 40C4h + formula\) \[reset = X\]: \[0\]](#)

11.132 DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j Register (Offset = 40C8h + formula) [reset = X]

DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j is shown in Figure 11-132 and described in Table 11-398.

Return to [Summary Table](#).

Transmit driver local init main cursor override register.

Offset = 40C8h + (j * 400h); where j = 0h to 1h

Table 11-397.
DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 40C8h + formula
SERDES_16G1	0501 40C8h + formula
SERDES_16G2	0502 40C8h + formula
SERDES_16G3	0503 40C8h + formula

Figure 11-132. DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							DRVCTRL_INIT_CP1_OVRD_EN_PREG
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED		DRVCTRL_INIT_CP1_OVRD_VAL_PREG					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED							DRVCTRL_INIT_C0_OVRD_EN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		DRVCTRL_INIT_C0_OVRD_VAL_PREG					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-398. DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DRVCTRL_INIT_CP1_OVRD_EN_PREG	R/W	0h	Local init post-emphasis cursor active high override enable.
23-22	RESERVED	R/W	X	
21-16	DRVCTRL_INIT_CP1_OVRD_VAL_PREG	R/W	0h	When drvctrl_init_cp1_ovrd_en_preg is asserted high, this value overrides the internally generated value for tx_local_tx_preset_coef_in_{15:0} [17:12] following a tx_get_local_init_coef_in_{15:0} request.
15-9	RESERVED	R/W	X	
8	DRVCTRL_INIT_C0_OVRD_EN_PREG	R/W	0h	Local init main cursor active high override enable.

Table 11-398. DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	DRVCTRL_INIT_C0_OVRD_VAL_PREG	R/W	0h	When drvctrl_init_c0_ovrd_en_preg is asserted high, this value overrides the internally generated value for tx_local_tx_preset_coef_ln_{15:0} [11:6] following a tx_get_local_init_coef_ln_{15:0} request.

**Table 11-399. Register Call Summary for
DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DRVCTRL_INIT_CP1_OVRD_PREG__DRVCTRL_INIT_C0_OVRD_PREG_j Register \(Offset = 40C8h + formula\) \[reset = X\]: \[0\]](#)

11.133 DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j Register (Offset = 40CCh + formula) [reset = X]

DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j is shown in Figure 11-133 and described in Table 11-401.

Return to [Summary Table](#).

Transmit driver pre-emphasis cursor override register.

Offset = 40CCh + (j * 400h); where j = 0h to 1h

Table 11-400. DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40CCh + formula
SERDES_16G1	0501 40CCh + formula
SERDES_16G2	0502 40CCh + formula
SERDES_16G3	0503 40CCh + formula

Figure 11-133. DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							DRVCTRL_C0_OVRD_EN_PREG
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED	DRVCTRL_C0_OVRD_VAL_PREG						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED							DRVCTRL_CM1_OVRD_EN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	DRVCTRL_CM1_OVRD_VAL_PREG						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-401. DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DRVCTRL_C0_OVRD_EN_PREG	R/W	0h	Main cursor active high override enable.
23	RESERVED	R/W	X	
22-16	DRVCTRL_C0_OVRD_VAL_PREG	R/W	0h	When drvctrl_c0_ovrd_en_preg is asserted high, this value overrides the internally calculated main coefficient sent to the analog transmitter circuit.
15-9	RESERVED	R/W	X	
8	DRVCTRL_CM1_OVRD_EN_PREG	R/W	0h	Pre-emphasis cursor active high override enable.
7	RESERVED	R/W	X	

**Table 11-401. DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
6-0	DRVCTRL_CM1_OVRD_VAL_PREG	R/W	0h	When drvctrl_cm1_ovrd_en_preg is asserted high, this value overrides the internally calculated pre-cursor coefficient sent to the analog transmitter circuit.

Table 11-402. Register Call Summary for DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DRVCTRL_C0_OVRD_PREG__DRVCTRL_CM1_OVRD_PREG_j Register \(Offset = 40CCh + formula\) \[reset = X\]: \[0\]](#)

11.134 DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j Register (Offset = 40D0h + formula) [reset = X]

DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j is shown in Figure 11-134 and described in Table 11-404.

Return to [Summary Table](#).

Transmit driver post-emphasis cursor override register.

Offset = 40D0h + (j * 400h); where j = 0h to 1h

Table 11-403. DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40D0h + formula
SERDES_16G1	0501 40D0h + formula
SERDES_16G2	0502 40D0h + formula
SERDES_16G3	0503 40D0h + formula

Figure 11-134. DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							DRVCTRL_C0M_OVRD_EN_PREG
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED	DRVCTRL_C0M_OVRD_VAL_PREG						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED							DRVCTRL_CP1_OVRD_EN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	DRVCTRL_CP1_OVRD_VAL_PREG						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-404. DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DRVCTRL_C0M_OVRD_EN_PREG	R/W	0h	Margin cursor active high override enable.
23	RESERVED	R/W	X	
22-16	DRVCTRL_C0M_OVRD_VAL_PREG	R/W	0h	When drvctrl_c0m_ovrd_en_preg is asserted high, this value overrides the internally calculated margin coefficient sent to the analog transmitter circuit.
15-9	RESERVED	R/W	X	
8	DRVCTRL_CP1_OVRD_EN_PREG	R/W	0h	Post-emphasis cursor active high override enable.
7	RESERVED	R/W	X	

Table 11-404. DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	DRVCTRL_CP1_OVRD_V AL_PREG	R/W	0h	When drvctrl_cp1_ovrd_en_preg is asserted high, this value overrides the internally calculated post-emphasis coefficient sent to the analog transmitter circuit.

Table 11-405. Register Call Summary for DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DRVCTRL_C0M_OVRD_PREG__DRVCTRL_CP1_OVRD_PREG_j Register \(Offset = 40D0h + formula\) \[reset = X\]: \[0\]](#)

11.135 DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j Register (Offset = 40D4h + formula) [reset = X]

DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j is shown in Figure 11-135 and described in Table 11-407.

Return to [Summary Table](#).

Transmit driver attenuation control register.

Offset = 40D4h + (j * 400h); where j = 0h to 1h

Table 11-406. DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40D4h + formula
SERDES_16G1	0501 40D4h + formula
SERDES_16G2	0502 40D4h + formula
SERDES_16G3	0503 40D4h + formula

Figure 11-135. DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	CM1VAL						
R/W-X	R-0h						
15	14	13	12	11	10	9	8
RESERVED							DRVCTRL_ATT EN_VMARGIN_ SEL_PREG
R/W-X							R/W-1h
7	6	5	4	3	2	1	0
RESERVED				DRVCTRL_ATT EN_OVRD_EN _PREG	DRVCTRL_ATTEN_OVRD_VAL_PREG		
R/W-X				R/W-0h	R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-407. DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	CM1VAL	R	0h	Current pre-emphasis cursor value to analog driver.
15-9	RESERVED	R/W	X	
8	DRVCTRL_ATTEN_VMARGIN_SEL_PREG	R/W	1h	When asserted high, the driver attenuation is controlled through tx_vmarg_in_{15:0}. This is expected to be the case for PCIe operation only. When deasserted low, the driver attenuation is set at 1.0.
7-4	RESERVED	R/W	X	
3	DRVCTRL_ATTEN_OVRD_EN_PREG	R/W	0h	Driver attenuation active high override enable.

**Table 11-407. DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2-0	DRVCTRL_ATTEN_OVRD_VAL_PREG	R/W	0h	When drvctrl_atten_ovrd_en_preg is asserted high, this value overrides the internally calculated attenuation for the transmit driver. Attenuation 3'b000 1.000 3'b001 1.000 3'b010 0.875 3'b011 0.750 3'b100 0.625 3'b101 0.500 3'b110 0.375 3'b111 0.250

Table 11-408. Register Call Summary for DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DRVCTRL_CM1_CV_PREG__DRVCTRL_ATTEN_PREG_j Register \(Offset = 40D4h + formula\) \[reset = X\]: \[0\]](#)

11.136 DRVCTRL_CP1_CV_PREG__DRVCTRL_C0_CV_PREG_j Register (Offset = 40D8h + formula) [reset = X]

DRVCTRL_CP1_CV_PREG__DRVCTRL_C0_CV_PREG_j is shown in Figure 11-136 and described in Table 11-410.

Return to [Summary Table](#).

Transmit driver main cursor status register.

Offset = 40D8h + (j * 400h); where j = 0h to 1h

Table 11-409. DRVCTRL_CP1_CV_PREG__DRVCTRL_C0_CV_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40D8h + formula
SERDES_16G1	0501 40D8h + formula
SERDES_16G2	0502 40D8h + formula
SERDES_16G3	0503 40D8h + formula

Figure 11-136. DRVCTRL_CP1_CV_PREG__DRVCTRL_C0_CV_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CP1VAL								RESERVED								C0VAL							
R-X								R-16h								R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 11-410. DRVCTRL_CP1_CV_PREG__DRVCTRL_C0_CV_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	X	
22-16	CP1VAL	R	16h	Current post-emphasis cursor value to analog driver.
15-7	RESERVED	R	X	
6-0	C0VAL	R	0h	Current main cursor value to analog driver.

Table 11-411. Register Call Summary for DRVCTRL_CP1_CV_PREG__DRVCTRL_C0_CV_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DRVCTRL_CP1_CV_PREG__DRVCTRL_C0_CV_PREG_j Register \(Offset = 40D8h + formula\) \[reset = X\]: \[0\]](#)

11.137 DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j Register (Offset = 40DCh + formula) [reset = X]

DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j is shown in Figure 11-137 and described in Table 11-413.

Return to [Summary Table](#).

Transmit driver margin status register.

Offset = 40DCh + (j * 400h); where j = 0h to 1h

**Table 11-412. DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 40DCh + formula
SERDES_16G1	0501 40DCh + formula
SERDES_16G2	0502 40DCh + formula
SERDES_16G3	0503 40DCh + formula

Figure 11-137. DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j Register

31	30	29	28	27	26	25	24
DRVCTRL_AM PBOOST_EN_ PREG	RESERVED			DRVCTRL_AMPBOOST_OFFAD JUST_PREG	DRVCTRL_AMPBOOST_TUNE_PREG		
R/W-1h	R/W-X			R/W-2h	R/W-4h		
23	22	21	20	19	18	17	16
RESERVED						DRVCTRL_EDGEBOOST_TUNE _PREG	
R/W-X						R/W-2h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	COMVAL						
R/W-X	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-413. DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRVCTRL_AMPBOOST_ EN_PREG	R/W	1h	Amplitude boost active high enable.
30-29	RESERVED	R/W	X	
28-27	DRVCTRL_AMPBOOST_ OFFADJUST_PREG	R/W	2h	When amplitude boost is disabled, the calibrated resistor calibration value is increased by this value, compensating for the boost circuit impedance contribution no longer present.
26-24	DRVCTRL_AMPBOOST_ TUNE_PREG	R/W	4h	Amplitude boost selection: Boost Level 3'b000 Minimum boost :: 3'b111 Maximum boost
23-18	RESERVED	R/W	X	

**Table 11-413. DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
17-16	DRVCTRL_EDGEBOOST_TUNE_PREG	R/W	2h	Edge boost selection: Boost Level 2'b00 Minimum boost :: 2'b11 Maximum boost
15-7	RESERVED	R/W	X	
6-0	C0MVAL	R	0h	Current margin value to analog driver.

Table 11-414. Register Call Summary for DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DRVCTRL_BOOST_PREG__DRVCTRL_C0M_CV_PREG_j Register \(Offset = 40DCh + formula\) \[reset = X\]: \[0\]](#)

11.138 LANE_TX_RECEIVER_DETECT_PREG__DRVCTRL_BSCAN_PREG_j Register (Offset = 40E0h + formula) [reset = X]

LANE_TX_RECEIVER_DETECT_PREG__DRVCTRL_BSCAN_PREG_j is shown in Figure 11-138 and described in Table 11-416.

Return to [Summary Table](#).

Transmit driver boundary scan resistor calibration override register.

Offset = 40E0h + (j * 400h); where j = 0h to 1h

Table 11-415.
LANE_TX_RECEIVER_DETECT_PREG__DRVCTRL_BSCAN_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40E0h + formula
SERDES_16G1	0501 40E0h + formula
SERDES_16G2	0502 40E0h + formula
SERDES_16G3	0503 40E0h + formula

Figure 11-138. LANE_TX_RECEIVER_DETECT_PREG__DRVCTRL_BSCAN_PREG_j Register

31	30	29	28	27	26	25	24
TX_RCVDET_WAIT_TIME_PREG							
R/W-9C4h							
23	22	21	20	19	18	17	16
TX_RCVDET_WAIT_TIME_PREG							
R/W-9C4h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				DRVCTRL_BSCAN_RESCAL_PREG			
R/W-X				R/W-Eh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-416. LANE_TX_RECEIVER_DETECT_PREG__DRVCTRL_BSCAN_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_RCVDET_WAIT_TIME_PREG	R/W	9C4h	Receiver detection wait time: Number of cmn_refclk periods to wait before the receiver detection state machine evaluates the results from the analog circuit. Note the required wait time is 100us.
15-4	RESERVED	R/W	X	
3-0	DRVCTRL_BSCAN_RESCAL_PREG	R/W	Eh	Transmit driver resistor calibration level used in boundary scan operation.

**Table 11-417. Register Call Summary for
LANE_TX_RECEIVER_DETECT_PREG__DRVCTRL_BSCAN_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANE_TX_RECEIVER_DETECT_PREG__DRVCTRL_BSCAN_PREG_j Register \(Offset = 40E0h + formula\) \[reset = X\]: \[0\]](#)

11.139 TX_RCVDET_OVRD_PREG_j Register (Offset = 40E4h + formula) [reset = X]

TX_RCVDET_OVRD_PREG_j is shown in Figure 11-139 and described in Table 11-419.

Return to [Summary Table](#).

Transmit driver receiver detection analog override

Offset = 40E4h + (j * 400h); where j = 0h to 1h

**Table 11-418. TX_RCVDET_OVRD_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 40E4h + formula
SERDES_16G1	0501 40E4h + formula
SERDES_16G2	0502 40E4h + formula
SERDES_16G3	0503 40E4h + formula

Figure 11-139. TX_RCVDET_OVRD_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TX_RCVDET_OVRD_EN_PREG	TX_RCVDET_OVRD_PREG
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-419. TX_RCVDET_OVRD_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TX_RCVDET_OVRD_EN_PREG	R/W	0h	Receiver detection analog override enable: When asserted, the value of tx_rcvdet_ovrd_preg overrides the txda_rcv_detected_n value from the analog.
0	TX_RCVDET_OVRD_PREG	R/W	0h	Receiver detection analog override: When tx_rcvdet_ovrd_en_preg is asserted high, this value overrides the txda_rcv_detected_n value from the analog.

Table 11-420. Register Call Summary for TX_RCVDET_OVRD_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [TX_RCVDET_OVRD_PREG_j Register \(Offset = 40E4h + formula\) \[reset = X\]: \[0\]](#)

11.140 TXCOEF_STATUS_PREG_j Register (Offset = 40E8h + formula) [reset = X]

TXCOEF_STATUS_PREG_j is shown in [Figure 11-140](#) and described in [Table 11-422](#).

Return to [Summary Table](#).

Transmit coefficient calculator status register.

Offset = 40E8h + (j * 400h); where j = 0h to 1h

Table 11-421. TXCOEF_STATUS_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40E8h + formula
SERDES_16G1	0501 40E8h + formula
SERDES_16G2	0502 40E8h + formula
SERDES_16G3	0503 40E8h + formula

Figure 11-140. TXCOEF_STATUS_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED					TXCOEF_STATE		
R-X					R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 11-422. TXCOEF_STATUS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	X	
2-0	TXCOEF_STATE	R	0h	Transmit coefficient calculator state vector.

Table 11-423. Register Call Summary for TXCOEF_STATUS_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [TXCOEF_STATUS_PREG_j Register \(Offset = 40E8h + formula\) \[reset = X\]: \[0\]](#)

11.141 LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROLS_PREG_j Register (Offset = 40F0h + formula) [reset = X]

LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROLS_PREG_j is shown in Figure 11-141 and described in Table 11-425.

Return to [Summary Table](#).

Transmit BIST control register.

Offset = 40F0h + (j * 400h); where j = 0h to 1h

Table 11-424. LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROLS_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 40F0h + formula
SERDES_16G1	0501 40F0h + formula
SERDES_16G2	0502 40F0h + formula
SERDES_16G3	0503 40F0h + formula

Figure 11-141. LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROLS_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED						TX_UDD_FIFO_WR_DATA	
R/W-X						W-0h	
23	22	21	20	19	18	17	16
TX_UDD_FIFO_WR_DATA							
W-0h							
15	14	13	12	11	10	9	8
RESERVED						TX_BIST_UDD _WR_CLEAR_ PREG	TX_BIST_FOR CE_ERROR_P REG
R/W-X						R/W-0h	W-0h
7	6	5	4	3	2	1	0
TX_BIST_PRBS_SEED_PREG			TX_BIST_MODE_PREG				TX_BIST_EN_P REG
R/W-0h			R/W-0h				R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-425. LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROLS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	

**Table 11-425. LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROLS_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
25-16	TX_UDD_FIFO_WR_DATA	W	0h	Transmit BIST user defined data: Writing a data word to this field will result in that data word being placed in the next available position in the transmitter BIST user defined data FIFO. Note: xcvr_data_width_in_{15:0}=16bit data: Only bits [7:0] used. Two FIFO words consumed per clock period. xcvr_data_width_in_{15:0}=20bit data: All bits used. Two FIFO words consumed per clock period. xcvr_data_width_in_{15:0}=32bit data: Only bits [7:0] used. Four FIFO words consumed per clock period.
15-10	RESERVED	R/W	X	
9	TX_BIST_UDD_WR_CLEAR_PREG	R/W	0h	Transmit BIST User Defined Data (UDD) FIFO write pointer clear: Writing a logic 1 resets the FIFO write pointer to 0. Note it does not clear the content of the user defined data FIFO. Note this register bit must be written back low for BIST operation.
8	TX_BIST_FORCE_ERROR_PREG	W	0h	Transmit BIST force error toggle bit: When written high, the transmit BIST controller will force a single bit error to be transmitted from the BIST logic. Writing it low does not trigger an error. Note due to the nature of this (T)oggle bit, writing the bit is not retained, and there is no requirement to write this bit back low.
7-5	TX_BIST_PRBS_SEED_PREG	R/W	0h	Transmit BIST PRBS seed: When the transmit BIST is in PRBS mode, this field provides a seed for the PRBS LFSR.
4-1	TX_BIST_MODE_PREG	R/W	0h	Transmit BIST mode: Selects which pattern the BIST will generate. Pattern 4'b0000 User Defined Data (UDD) FIFO 4'b0001 - 4'b0111 Reserved 4'b1000 27 order PRBS (Polynomial x^7+x^6+1) 4'b1001 215 bit PRBS (Polynomial $x^{15}+x^{14}+1$) 4'b1010 223 bit PRBS (Polynomial $x^{23}+x^{18}+1$) 4'b1011 231 bit PRBS (Polynomial $x^{31}+x^{28}+1$) 4'b 1100 - 4'b1111 Reserved Note the value must match the corresponding field for the receive BIST controller.
0	TX_BIST_EN_PREG	R/W	0h	Transmit BIST active high enable.

Table 11-426. Register Call Summary for LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROLS_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LANE_TX_BIST_UDD_PREG__TX_BIST_CONTROLS_PREG_j Register \(Offset = 40F0h + formula\) \[reset = X\]: \[0\]](#)

11.142 TX_LFPSGEN_STATUS_PREG_j Register (Offset = 40F8h + formula) [reset = X]

TX_LFPSGEN_STATUS_PREG_j is shown in Figure 11-142 and described in Table 11-428.

Return to [Summary Table](#).

Transmit LFPS generator status register.

Offset = 40F8h + (j * 400h); where j = 0h to 1h

**Table 11-427. TX_LFPSGEN_STATUS_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 40F8h + formula
SERDES_16G1	0501 40F8h + formula
SERDES_16G2	0502 40F8h + formula
SERDES_16G3	0503 40F8h + formula

Figure 11-142. TX_LFPSGEN_STATUS_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				TX_LFPSGEN_STATE			
R-X				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 11-428. TX_LFPSGEN_STATUS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3-0	TX_LFPSGEN_STATE	R	0h	Transmit LFPS generator state vector.

Table 11-429. Register Call Summary for TX_LFPSGEN_STATUS_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [TX_LFPSGEN_STATUS_PREG_j Register \(Offset = 40F8h + formula\) \[reset = X\]: \[0\]](#)

11.143 CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j Register (Offset = 4100h + formula) [reset = X]

CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j is shown in Figure 11-143 and described in Table 11-431.

Return to [Summary Table](#).

Receive clock path controller override register.

Offset = 4100h + (j * 400h); where j = 0h to 1h

Table 11-430. CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4100h + formula
SERDES_16G1	0501 4100h + formula
SERDES_16G2	0502 4100h + formula
SERDES_16G3	0503 4100h + formula

Figure 11-143. CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j Register

31	30	29	28	27	26	25	24
CLKPATHCTRL_SSCEN_PREG	RESERVED				CLKPATHCTRL_SSCTMRVAL_PREG		
R/W-0h	R/W-X				R/W-1h		
23	22	21	20	19	18	17	16
CLKPATHCTRL_NOSSCTMRVAL_PREG							
R/W-3Eh							
15	14	13	12	11	10	9	8
RESERVED						CLKPATHCTRL_RDYOVREN_PREG	CLKPATHCTRL_RDYOVRRVAL_PREG
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-431. CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLKPATHCTRL_SSCEN_PREG	R/W	0h	Receive clock recovery timer selection 0 short lock timer using clkpathctrl_nossctmrval_preg selected 1 long lock timer using clkpathctrl_ssctmrval_preg selected
30-27	RESERVED	R/W	X	
26-24	CLKPATHCTRL_SSCTMRVAL_PREG	R/W	1h	Receive clock recovery lock timer with spread spectrum system Lock time is: $2^{\text{clkpathctrl_ssclockadj}[1:0]} * (750 + (\text{clkpathctrl_ssctmrval} * 256))$ rx_rd_clk_ln_{15:0} periods

Table 11-431. CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	CLKPATHCTRL_NOSSCTMRVAL_PREG	R/W	3Eh	Receive clock recovery lock timer without spread spectrum system Lock time for 16 / 20 bit wide data is: clkpathctrl_nossctmrval[7:0] rx_rd_clk_ln_{15:0} periods Lock time for 32 bit wide data is: 0.5 * clkpathctrl_nossctmrval[7:0] rx_rd_clk_ln_{15:0} periods
15-10	RESERVED	R/W	X	
9	CLKPATHCTRL_RDYOVR EN_PREG	R/W	0h	Receive clock path ready signal to data path (deq_clkpathrdy) active high override enable.
8	CLKPATHCTRL_RDYOVR VAL_PREG	R/W	0h	When clkpathctrl_rdyovren_preg is asserted high, this value will override the clock path controller generated ready signal (deq_clkpathrdy).
7-0	RESERVED	R/W	X	

Table 11-432. Register Call Summary for CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CLKPATHCTRL_TMR_PREG__CLKPATHCTRL_OVR_PREG_j Register \(Offset = 4100h + formula\) \[reset = X\]: \[0\]](#)

11.144 RX_CREQ_FLTR_A_MODE3_PREG_j Register (Offset = 4108h + formula) [reset = X]

RX_CREQ_FLTR_A_MODE3_PREG_j is shown in Figure 11-144 and described in Table 11-434.

Return to [Summary Table](#).

RX_CREQ_FLTR_A_MODE3_PREG

Offset = 4108h + (j * 400h); where j = 0h to 1h

**Table 11-433. RX_CREQ_FLTR_A_MODE3_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4108h + formula
SERDES_16G1	0501 4108h + formula
SERDES_16G2	0502 4108h + formula
SERDES_16G3	0503 4108h + formula

Figure 11-144. RX_CREQ_FLTR_A_MODE3_PREG_j Register

31	30	29	28	27	26	25	24
CREQ_CRFLTR_RSTACCUM2ONSAT_MODE3_PREG	CREQ_CRFLTR_CRHOLD_MODE3_PREG	RESERVED		CREQ_CRFLTR_SUBSUMINV_MODE3_PREG	CREQ_CRFLTR_LEAKFREQ_MODE3_PREG		
R/W-1h	R/W-0h	R/W-X		R/W-0h	R/W-0h		
23	22	21	20	19	18	17	16
CREQ_CRFLTR_GAIN1_MODE3_PREG		CREQ_CRFLTR_GAIN2_MODE3_PREG			CREQ_CRFLTR_ACCUMSAT2_MODE3_PREG		CREQ_CRFLTR_HIRES_MODE3_PREG
R/W-2h		R/W-3h			R/W-1h		R/W-1h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-434. RX_CREQ_FLTR_A_MODE3_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CREQ_CRFLTR_RSTACCUM2ONSAT_MODE3_PREG	R/W	1h	Clock recovery filter 's integral path accumulator reset on saturation control when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. 1'b0 Integral path reset on CTLE LUT change. 1'b1 Integral path reset when saturation reached.
30	CREQ_CRFLTR_CRHOLD_MODE3_PREG	R/W	0h	Clock recovery hold active high enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.
29-28	RESERVED	R/W	X	
27	CREQ_CRFLTR_SUBSUMINV_MODE3_PREG	R/W	0h	Clock recovery filter inversion active high enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. When asserted, the sumsub node in the clock recovery filter is inverted. Note this bit is for diagnostic purposes only.

Table 11-434. RX_CREQ_FLTR_A_MODE3_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-24	CREQ_CRFLTR_LEAKFR EQ_MODE3_PREG	R/W	0h	<p>Clock recovery integral path leak frequency when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.</p> <p>An integrator leak of +/- 1 is applied every N cycles. When the accumulated value is positive, the leak is -1 and when it is negative, the leak is +1.</p> <p>Cycles per leak (N)</p> <p>3'b000 Off</p> <p>3'b001 16</p> <p>3'b010 64</p> <p>3'b011 256</p> <p>3'b100 1024</p> <p>3'b101 4096</p> <p>3'b110 1 (Continuous)</p> <p>3'b111 1 (Continuous)</p>
23-22	CREQ_CRFLTR_GAIN1_ MODE3_PREG	R/W	2h	<p>Clock recovery combined proportional and integral path gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.</p> <p>Gain</p> <p>2'b00 1/2</p> <p>2'b01 1</p> <p>2'b10 2</p> <p>2'b11 2</p> <p>Note: Use of the Gain setting value of 2 (gain1_preg=2'b1X) requires the creq_crfltr_accum2sat_preg to be limiting at or less than +4095/-4096.</p>
21-19	CREQ_CRFLTR_GAIN2_ MODE3_PREG	R/W	3h	<p>Clock recovery integral path gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.</p> <p>Gain</p> <p>3'b000 1/32</p> <p>3'b001 1/64</p> <p>3'b010 1/128</p> <p>3'b011 1/256</p> <p>3'b1XX 0 (Integral path disabled.)</p>
18-17	CREQ_CRFLTR_ACCUM SAT2_MODE3_PREG	R/W	1h	<p>Clock Recovery integral path accumulator saturation level when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.</p> <p>Limit</p> <p>2'b00 +1023/-1024</p> <p>2'b01 +2047/-2048</p> <p>2'b10 +4095/-4096</p> <p>2'b11 +8191/-8192</p>
16	CREQ_CRFLTR_HIRES_ MODE3_PREG	R/W	1h	<p>CPI high resolution enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.</p> <p>Interpolation steps per UI</p> <p>1'b0 32</p> <p>1'b1 64</p>
15-0	RESERVED	R/W	X	

Table 11-435. Register Call Summary for RX_CREQ_FLTR_A_MODE3_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_CREQ_FLTR_A_MODE3_PREG_j Register \(Offset = 4108h + formula\) \[reset = X\]: \[0\]](#)

11.145 RX_CREQ_FLTR_A_MODE1_PREG_RX_CREQ_FLTR_A_MODE2_PREG_j Register (Offset = 410Ch + formula) [reset = X]

RX_CREQ_FLTR_A_MODE1_PREG_RX_CREQ_FLTR_A_MODE2_PREG_j is shown in Figure 11-145 and described in Table 11-437.

Return to [Summary Table](#).

RX_CREQ_FLTR_A_MODE1_PREG_RX_CREQ_FLTR_A_MODE2_PREG

Offset = 410Ch + (j * 400h); where j = 0h to 1h

Table 11-436.
RX_CREQ_FLTR_A_MODE1_PREG_RX_CREQ_FLTR_A_MODE2_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 410Ch + formula
SERDES_16G1	0501 410Ch + formula
SERDES_16G2	0502 410Ch + formula
SERDES_16G3	0503 410Ch + formula

Figure 11-145. RX_CREQ_FLTR_A_MODE1_PREG_RX_CREQ_FLTR_A_MODE2_PREG_j Register

31	30	29	28	27	26	25	24
CREQ_CRFLT R_RSTACCUM 2ONSAT_MOD E1_PREG	CREQ_CRFLT R_CRHOLD_M ODE1_PREG	RESERVED		CREQ_CRFLT R_SUBSUMINV _MODE1_PRE G	CREQ_CRFLTR_LEAKFREQ_MODE1_PREG		
R/W-1h	R/W-0h	R/W-X		R/W-0h	R/W-4h		
23	22	21	20	19	18	17	16
CREQ_CRFLTR_GAIN1_MODE1_PREG		CREQ_CRFLTR_GAIN2_MODE1_PREG			CREQ_CRFLTR_ACCUMSAT2_MODE1_PREG		CREQ_CRFLT R_HIRES_MOD E1_PREG
R/W-2h		R/W-1h			R/W-0h		R/W-1h
15	14	13	12	11	10	9	8
CREQ_CRFLT R_RSTACCUM 2ONSAT_MOD E2_PREG	CREQ_CRFLT R_CRHOLD_M ODE2_PREG	RESERVED		CREQ_CRFLT R_SUBSUMINV _MODE2_PRE G	CREQ_CRFLTR_LEAKFREQ_MODE2_PREG		
R/W-1h	R/W-0h	R/W-X		R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
CREQ_CRFLTR_GAIN1_MODE2_PREG		CREQ_CRFLTR_GAIN2_MODE2_PREG			CREQ_CRFLTR_ACCUMSAT2_MODE2_PREG		CREQ_CRFLT R_HIRES_MOD E2_PREG
R/W-2h		R/W-3h			R/W-1h		R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-437. RX_CREQ_FLTR_A_MODE1_PREG_RX_CREQ_FLTR_A_MODE2_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CREQ_CRFLTR_RSTACCUM2ONSAT_MODE1_PREG	R/W	1h	Clock recovery filter 's integral path accumulator reset on saturation control when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. 1'b0 Integral path reset on CTLE LUT change. 1'b1 Integral path reset when saturation reached.
30	CREQ_CRFLTR_CRHOLD_MODE1_PREG	R/W	0h	Clock recovery hold active high enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001.

Table 11-437. RX_CREQ_FLTR_A_MODE1_PREG_RX_CREQ_FLTR_A_MODE2_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29-28	RESERVED	R/W	X	
27	CREQ_CRFLTR_SUBSU MINV_MODE1_PREG	R/W	0h	Clock recovery filter inversion active high enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. When asserted, the sumsub node in the clock recovery filter is inverted. Note this bit is for diagnostic purposes only.
26-24	CREQ_CRFLTR_LEAKFR EQ_MODE1_PREG	R/W	4h	Clock recovery integral path leak frequency when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. An integrator leak of +/- 1 is applied every N cycles. When the accumulated value is positive, the leak is -1 and when it is negative, the leak is +1. Cycles per leak (N) 3'b000 Off 3'b001 16 3'b010 64 3'b011 256 3'b100 1024 2'b101 4096 3'b110 1 (Continuous) 3'b111 1 (Continuous)
23-22	CREQ_CRFLTR_GAIN1_ MODE1_PREG	R/W	2h	Clock recovery combined proportional and integral path gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Gain 2'b00 1/2 2'b01 1 2'b10 2 2'b11 2 Note: Use of the Gain setting value of 2 (gain1_preg=2'b1X) requires the creq_crfltr_accum2sat_preg to be limiting at or less than +4095/-4096.
21-19	CREQ_CRFLTR_GAIN2_ MODE1_PREG	R/W	1h	Clock recovery integral path gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Gain 3'b000 1/32 3'b001 1/64 3'b010 1/128 3'b011 1/256 3'b1XX 0 (Integral path disabled.)
18-17	CREQ_CRFLTR_ACCUM SAT2_MODE1_PREG	R/W	0h	Clock Recovery integral path accumulator saturation level when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Limit 2'b00 +1023/-1024 2'b01 +2047/-2047 2'b10 +4095/-4096 2'b11 +8191/-8192
16	CREQ_CRFLTR_HIRES_ MODE1_PREG	R/W	1h	CPI high resolution enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Interpolation steps per UI 1'b0 32 1'b1 64

Table 11-437. RX_CREQ_FLTR_A_MODE1_PREG_RX_CREQ_FLTR_A_MODE2_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	CREQ_CRFLTR_RSTACCUM2ONSAT_MODE2_PREG	R/W	1h	Clock recovery filter 's integral path accumulator reset on saturation control when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. 1'b0 Integral path reset on CTLE LUT change. 1'b1 Integral path reset when saturation reached.
14	CREQ_CRFLTR_CRHOLD_MODE2_PREG	R/W	0h	Clock recovery hold active high enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010.
13-12	RESERVED	R/W	X	
11	CREQ_CRFLTR_SUBSUMINV_MODE2_PREG	R/W	0h	Clock recovery filter inversion active high enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. When asserted, the sumsub node in the clock recovery filter is inverted. Note this bit is for diagnostic purposes only.
10-8	CREQ_CRFLTR_LEAKFREQUENCY_MODE2_PREG	R/W	0h	Clock recovery integral path leak frequency when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. An integrator leak of +/- 1 is applied every N cycles. When the accumulated value is positive, the leak is -1 and when it is negative, the leak is +1. Cycles per leak (N) 3'b000 Off 3'b001 16 3'b010 64 3'b011 256 3'b100 1024 3'b101 4096 3'b110 1 (Continuous) 3'b111 1 (Continuous)
7-6	CREQ_CRFLTR_GAIN1_MODE2_PREG	R/W	2h	Clock recovery combined proportional and integral path gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. Gain 2'b00 1/2 2'b01 1 2'b10 2 2'b11 2 Note: Use of the Gain setting value of 2 (gain1_preg=2'b1X) requires the creq_crfltr_accum2sat_preg to be limiting at or less than +4095/-4096.
5-3	CREQ_CRFLTR_GAIN2_MODE2_PREG	R/W	3h	Clock recovery integral path gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. Gain 3'b000 1/32 3'b001 1/64 3'b010 1/128 3'b011 1/256 3'b1XX 0 (Integral path disabled.)
2-1	CREQ_CRFLTR_ACCUMSAT2_MODE2_PREG	R/W	1h	Clock Recovery integral path accumulator saturation level when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. Limit 2'b00 +1023/-1024 2'b01 +2047/-2047 2'b10 +4095/-4096 2'b11 +8191/-8192

Table 11-437. RX_CREQ_FLTR_A_MODE1_PREG__RX_CREQ_FLTR_A_MODE2_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CREQ_CRFLTR_HIRES_MODE2_PREG	R/W	1h	CPI high resolution enable when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010. Interpolation steps per UI 1'b0 32 1'b1 64

**Table 11-438. Register Call Summary for
RX_CREQ_FLTR_A_MODE1_PREG__RX_CREQ_FLTR_A_MODE2_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_CREQ_FLTR_A_MODE1_PREG__RX_CREQ_FLTR_A_MODE2_PREG_j Register \(Offset = 410Ch + formula\) \[reset = X\]: \[0\]](#)

11.146 RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j Register (Offset = 4110h + formula) [reset = X]

RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j is shown in Figure 11-146 and described in Table 11-440.

Return to [Summary Table](#).

Receive clock recovery filter control register A.

Offset = 4110h + (j * 400h); where j = 0h to 1h

Table 11-439.
RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4110h + formula
SERDES_16G1	0501 4110h + formula
SERDES_16G2	0502 4110h + formula
SERDES_16G3	0503 4110h + formula

Figure 11-146. RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED			CREQ_CRFLTR_LOWLATENCYEN_MODE3_PREG	RESERVED		CREQ_CRFLTR_LOWLATENCYEN_MODE2_PREG	
R/W-X			R/W-0h	R/W-X		R/W-1h	
23	22	21	20	19	18	17	16
RESERVED			CREQ_CRFLTR_LOWLATENCYEN_MODE1_PREG	RESERVED		CREQ_CRFLTR_LOWLATENCYEN_MODE0_PREG	
R/W-X			R/W-1h	R/W-X		R/W-1h	
15	14	13	12	11	10	9	8
CREQ_CRFLTR_RSTACCUM2ONSTAT_MODE0_PREG	CREQ_CRFLTR_CRHOLD_MODE0_PREG	RESERVED		CREQ_CRFLTR_SUBSUMINV_MODE0_PREG	CREQ_CRFLTR_LEAKFREQ_MODE0_PREG		
R/W-1h	R/W-0h	R/W-X		R/W-0h	R/W-0h		
7	6	5	4	3	2	1	0
CREQ_CRFLTR_GAIN1_MODE0_PREG		CREQ_CRFLTR_GAIN2_MODE0_PREG			CREQ_CRFLTR_ACCUMSAT2_MODE0_PREG		CREQ_CRFLTR_HIRES_MODE0_PREG
R/W-3h		R/W-1h			R/W-0h		R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-440. RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28	CREQ_CRFLTR_LOWLATENCYEN_MODE3_PREG	R/W	0h	This value sets the low latency mode enable from the Lane Standards Decoder when xcvr_standard_mode_in{15:0}[2:0] is 3'b011.
27-25	RESERVED	R/W	X	

Table 11-440. RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	CREQ_CRFLTR_LOWLATENCYEN_MODE2_PREG	R/W	1h	This value sets the low latency mode enable from the Lane Standards Decoder when xcvr_standard_mode_ln{15:0}[2:0] is 3'b010.
23-21	RESERVED	R/W	X	
20	CREQ_CRFLTR_LOWLATENCYEN_MODE1_PREG	R/W	1h	This value sets the low latency mode enable from the Lane Standards Decoder when xcvr_standard_mode_ln{15:0}[2:0] is 3'b001.
19-17	RESERVED	R/W	X	
16	CREQ_CRFLTR_LOWLATENCYEN_MODE0_PREG	R/W	1h	This value sets the low latency mode enable from the Lane Standards Decoder when xcvr_standard_mode_ln{15:0}[2:0] is 3'b000.
15	CREQ_CRFLTR_RSTACCUM2ONSAT_MODE0_PREG	R/W	1h	Clock recovery filter 's integral path accumulator reset on saturation control when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. 1'b0 Integral path reset on CTLE LUT change. 1'b1 Integral path reset when saturation reached.
14	CREQ_CRFLTR_CRHOLD_MODE0_PREG	R/W	0h	Clock recovery hold active high enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000.
13-12	RESERVED	R/W	X	
11	CREQ_CRFLTR_SUBSUMINV_MODE0_PREG	R/W	0h	Clock recovery filter inversion active high enable when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. When asserted, the sumsub node in the clock recovery filter is inverted. Note this bit is for diagnostic purposes only.
10-8	CREQ_CRFLTR_LEAKFREQUENCY_MODE0_PREG	R/W	0h	Clock recovery integral path leak frequency when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. An integrator leak of +/- 1 is applied every N cycles. When the accumulated value is positive, the leak is -1 and when it is negative, the leak is +1. Cycles per leak (N) 3'b000 Off 3'b001 16 3'b010 64 3'b011 256 3'b100 1024 3'b101 4096 3'b110 1 (Continuous) 3'b111 1 (Continuous)
7-6	CREQ_CRFLTR_GAIN1_MODE0_PREG	R/W	3h	Clock recovery combined proportional and integral path gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. Gain 2'b00 1/2 2'b01 1 2'b10 2 2'b11 2 Note: Use of the Gain setting value of 2 (gain1_preg=2'b1X) requires the creq_crfltr_accum2sat_preg to be limiting at or less than +4095/-4096.

Table 11-440. RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-3	CREQ_CRFLTR_GAIN2_MODE0_PREG	R/W	1h	Clock recovery integral path gain when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000. Gain 3'b000 1/32 3'b001 1/64 3'b010 1/128 3'b011 1/256 3'b1XX 0 (Integral path disabled.)
2-1	CREQ_CRFLTR_ACCUM SAT2_MODE0_PREG	R/W	0h	Clock Recovery integral path accumulator saturation level: Limit 2'b00 +1023/-1024 2'b01 +2047/-2047 2'b10 +4095/-4096 2'b11 +8191/-8192
0	CREQ_CRFLTR_HIRES_MODE0_PREG	R/W	1h	CPI high resolution enable when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000. Interpolation steps per UI 1'b0 32 1'b1 64

Table 11-441. Register Call Summary for RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_CREQ_FLTR_B_PREG_RX_CREQ_FLTR_A_MODE0_PREG_j Register \(Offset = 4110h + formula\) \[reset = X\]: \[0\]](#)

11.147 RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BUMP_PREG_j Register (Offset = 4114h + formula) [reset = X]

RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BUMP_PREG_j is shown in Figure 11-147 and described in Table 11-443.

Return to [Summary Table](#).

Receive clock recovery bump feature control register.

NOTE: The bump feature is deprecated. rxda_creq_crfltr_bumpen_preg should not be written high.

Offset = 4114h + (j * 400h); where j = 0h to 1h

Table 11-442. RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BUMP_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4114h + formula
SERDES_16G1	0501 4114h + formula
SERDES_16G2	0502 4114h + formula
SERDES_16G3	0503 4114h + formula

Figure 11-147. RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BUMP_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
CREQ_CPI_OVREN_PREG	CREQ_CPI_OVR_PREG						
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	RXDA_CREQ_CRFLTR_BUMPEN_PREG	RXDA_CREQ_CRFLTR_INACTIVTHRESHOLD_PREG					
R/W-X		R/W-0h		R/W-Ah			
7	6	5	4	3	2	1	0
RXDA_CREQ_CRFLTR_INACTIVTHRESHOLD_PREG	RXDA_CREQ_CRFLTR_BUMPTHRESHOLD_PREG						
R/W-Ah				R/W-7Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-443. RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BUMP_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	CREQ_CPI_OVREN_PREG	R/W	0h	CPI phase active high override enable.
22-16	CREQ_CPI_OVR_PREG	R/W	0h	When creq_cpi_ovren_preg is asserted high, this value will override the clock recovery filter CPI binary phase. Increasing binary values advance the output clock phase relative to the input.
15	RESERVED	R/W	X	
14	RXDA_CREQ_CRFLTR_BUMPEN_PREG	R/W	0h	Clock recover bump feature active high enable.

**Table 11-443. RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BUMP_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
13-7	RXDA_CREQ_CRFLTR_I NACTIVTHRESHOLD_PREG	R/W	Ah	Clock recover bump feature inactivity threshold: Used to determine receive input inactivity when bump feature is enabled. After an inactive period greater than or equal to this number of 1/8th serial data rate clock periods has been observed, bump insertions are discontinued until activity resumes.
6-0	RXDA_CREQ_CRFLTR_B UMPTHRESHOLD_PREG	R/W	7Fh	Clock recover bump feature bump threshold: If the CPI phase has been static for this number of 1/8 serial data rate clock periods, a bump is inserted.

Table 11-444. Register Call Summary for RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BUMP_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_CPI_OVERRIDE_PREG__RX_CREQ_CR_BUMP_PREG_j Register \(Offset = 4114h + formula\) \[reset = X\]: \[0\]](#)

11.148 CREQ_CCLKDET_MODE23_PREG__CREQ_DCBIASATTEN_OVR_PREG_j Register (Offset = 4118h + formula) [reset = X]

CREQ_CCLKDET_MODE23_PREG__CREQ_DCBIASATTEN_OVR_PREG_j is shown in Figure 11-148 and described in Table 11-446.

Return to [Summary Table](#).

Receive clock path DC bias attenuation override register.

Offset = 4118h + (j * 400h); where j = 0h to 1h

Table 11-445.
CREQ_CCLKDET_MODE23_PREG__CREQ_DCBIASATTEN_OVR_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4118h + formula
SERDES_16G1	0501 4118h + formula
SERDES_16G2	0502 4118h + formula
SERDES_16G3	0503 4118h + formula

Figure 11-148. CREQ_CCLKDET_MODE23_PREG__CREQ_DCBIASATTEN_OVR_PREG_j Register

31	30	29	28	27	26	25	24
CREQ_CLKDET_TIMERVAL_MODE3_PREG							
R/W-C6h							
23	22	21	20	19	18	17	16
CREQ_CLKDET_TIMERVAL_MODE2_PREG							
R/W-62h							
15	14	13	12	11	10	9	8
RESERVED			CREQ_CLKDETEN_FORCE_PREG	RESERVED			
R/W-X			R/W-0h	R/W-X			
7	6	5	4	3	2	1	0
RESERVED						CREQ_DCBIASATTEN_OVR_N_PREG	CREQ_DCBIASATTEN_OVRVA_L_PREG
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-446. CREQ_CCLKDET_MODE23_PREG__CREQ_DCBIASATTEN_OVR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CREQ_CLKDET_TIMERVAL_MODE3_PREG	R/W	C6h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_{15:0}[2:0] is 3'b011. Note time is delineated in 1/8 data rate clock periods.
23-16	CREQ_CLKDET_TIMERVAL_MODE2_PREG	R/W	62h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_{15:0}[2:0] is 3'b010. Note time is delineated in 1/8 data rate clock periods.
15-13	RESERVED	R/W	X	
12	CREQ_CLKDETEN_FORCE_PREG	R/W	0h	When asserted, the ctcleclk_clkdeten output of rxana_creq is forced high. This is useful when monitoring the related ATB points.
11-2	RESERVED	R/W	X	

Table 11-446. CREQ_CCLKDET_MODE23_PREG__CREQ_DCBIASATTEN_OVR_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CREQ_DCBIASATTEN_OVREN_PREG	R/W	0h	Clock path CTLE DC bias attenuation active high override enable.
0	CREQ_DCBIASATTEN_OVRVAL_PREG	R/W	0h	When creq_dcbiasatten_ovren_preg is asserted high, this value overrides the internally generated control to ctleck_dcbiasatten.

**Table 11-447. Register Call Summary for
CREQ_CCLKDET_MODE23_PREG__CREQ_DCBIASATTEN_OVR_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CREQ_CCLKDET_MODE23_PREG__CREQ_DCBIASATTEN_OVR_PREG_j Register \(Offset = 4118h + formula\) \[reset = X\]: \[0\]](#)

11.149 RX_CTL_ECAL_PREG_CREQ_CCLKDET_MODE01_PREG_j Register (Offset = 411Ch + formula) [reset = X]

RX_CTL_ECAL_PREG_CREQ_CCLKDET_MODE01_PREG_j is shown in Figure 11-149 and described in Table 11-449.

Return to [Summary Table](#).

Receive clock path CTLE clock detection register for standard modes 0 and 1.

Offset = 411Ch + (j * 400h); where j = 0h to 1h

Table 11-448. RX_CTL_ECAL_PREG_CREQ_CCLKDET_MODE01_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 411Ch + formula
SERDES_16G1	0501 411Ch + formula
SERDES_16G2	0502 411Ch + formula
SERDES_16G3	0503 411Ch + formula

Figure 11-149. RX_CTL_ECAL_PREG_CREQ_CCLKDET_MODE01_PREG_j Register

31	30	29	28	27	26	25	24
CREQ_CTRL_EQOVREN_PREG	CREQ_CTL_EQOVR_PREG				RESERVED	CREQ_CTL_OSEN_PREG	RESERVED
R/W-0h	R/W-0h				R/W-X	R/W-0h	R/W-X
23	22	21	20	19	18	17	16
CREQ_CTL_OFFSET_OVR_PREG	RESERVED	CREQ_CTL_OFFSET_OVR_PREG					
R/W-0h	R/W-X	R/W-0h					
15	14	13	12	11	10	9	8
CREQ_CLKDET_TIMERVAL_MODE1_PREG							
R/W-3Ch							
7	6	5	4	3	2	1	0
CREQ_CLKDET_TIMERVAL_MODE0_PREG							
R/W-1Dh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-449. RX_CTL_ECAL_PREG_CREQ_CCLKDET_MODE01_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CREQ_CTRL_EQOVREN_PREG	R/W	0h	Receive clock path CTLE equalization pointer active high override enable.
30-27	CREQ_CTL_EQOVR_PREG	R/W	0h	When creq_ctrl_eqovren_preg is asserted high, this value overrides rxda_creq_eqptr in selecting the appropriate CTLE LUT entry.
26	RESERVED	R/W	X	
25	CREQ_CTL_OSEN_PREG	R/W	0h	Receive clock path CTLE offset calibration algorithm active low maintenance enable.
24	RESERVED	R/W	X	
23	CREQ_CTL_OFFSET_OVR_PREG	R/W	0h	Receive clock path CTLE offset calibration active high override enable.
22	RESERVED	R/W	X	

**Table 11-449. RX_CTL_E_CAL_PREG__CREQ_CCLKDET_MODE01_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
21-16	CREQ_CTL_E_OFFSET_OVR_PREG	R/W	0h	When creq_ctl_e_offsetovren_preg is asserted high, this value overrides the calibration algorithm binary data. Bit Field Description [5] Sign bit applied to ctleclk_posoffset [4:0] Amplitude applied to ctleclk_offcal
15-8	CREQ_CLKDET_TIMERVAL_MODE1_PREG	R/W	3Ch	This value sets the Lane Standards Decoder value when xcvr_standard_mode_{15:0}[2:0] is 3'b001. Note time is delineated in 1/8 data rate clock periods.
7-0	CREQ_CLKDET_TIMERVAL_MODE0_PREG	R/W	1Dh	This value sets the Lane Standards Decoder value when xcvr_standard_mode_{15:0}[2:0] is 3'b000. Note time is delineated in 1/8 data rate clock periods.

Table 11-450. Register Call Summary for RX_CTL_E_CAL_PREG__CREQ_CCLKDET_MODE01_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_CTL_E_CAL_PREG__CREQ_CCLKDET_MODE01_PREG_j Register \(Offset = 411Ch + formula\) \[reset = X\]: \[0\]](#)

11.150 RX_CTLTLE_MAINTENANCE_PREG__RX_CTLTLE_CTRL_PREG_j Register (Offset = 4120h + formula) [reset = X]

RX_CTLTLE_MAINTENANCE_PREG__RX_CTLTLE_CTRL_PREG_j is shown in Figure 11-150 and described in Table 11-452.

Return to [Summary Table](#).

Receive clock path CTLE Control register.

Offset = 4120h + (j * 400h); where j = 0h to 1h

Table 11-451. RX_CTLTLE_MAINTENANCE_PREG__RX_CTLTLE_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4120h + formula
SERDES_16G1	0501 4120h + formula
SERDES_16G2	0502 4120h + formula
SERDES_16G3	0503 4120h + formula

Figure 11-150. RX_CTLTLE_MAINTENANCE_PREG__RX_CTLTLE_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED						CREQ_FSM_EQMAINTAVEDLY_PREG	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED		CREQ_FSM_OSMWAIT_PREG		CREQ_FSM_FULL_SCALE_SEL_PREG		CREQ_FSM_OSMWAITAVEDLY_PREG	
R/W-X		R/W-3h		R/W-3h		R/W-0h	
15	14	13	12	11	10	9	8
RESERVED		CREQ_CTLES_TART_OVRVAL_PREG	CREQ_CTLES_TART_OVRVAL_PREG	RESERVED		CREQ_CTLES_TART_ACK_OVRVAL_PREG	CREQ_CTLES_TART_ACK_OVRVAL_PREG
R/W-X		R/W-0h	R/W-0h	R/W-X		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			CREQ_CTLEH_OLD_FORCE_PREG	RESERVED		CREQ_CTLEH_OLD_ACK_OVRVAL_PREG	CREQ_CTLEH_OLD_ACK_OVRVAL_PREG
R/W-X			R/W-0h	R/W-X		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-452. RX_CTLTLE_MAINTENANCE_PREG__RX_CTLTLE_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	CREQ_FSM_EQMAINTAVEDLY_PREG	R/W	0h	Receive clock path CTLE equalization maintenance averaging timer: Delay 2'b00 32 fsmclk periods 2'b01 512 fsmclk periods 2'b10 768 fsmclk periods 2'b11 1024 fsmclk periods where: (8*creq_fsmclk_sel_preg ratio) fsmclks=1UI.
23-22	RESERVED	R/W	X	

**Table 11-452. RX_CTL_E_MAINTENANCE_PREG_RX_CTL_E_CTRL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
21-20	CREQ_FSM_OSMaintW AIT_PREG	R/W	3h	Receive clock path CTLE offset calibration maintenance hold off timer: N such that hold off time is $2(N+21)$ fsmclk clock periods where: ($8 \cdot \text{creq_fsmclk_sel_preg}$ ratio) fsmclks=1UI.
19-18	CREQ_FSM_FULL_SCAL E_SEL_PREG	R/W	3h	Offset maintenance filter threshold. Corrections occur only when the absolute value of the average number of 1's or 0's recovered at the Q sampling point exceeds this value. Threshold 2'b00 greater than 2 2'b01 greater than 4 2'b10 greater than 8 2'b11 greater than 16
17-16	CREQ_FSM_OSMaintAV EDLY_PREG	R/W	0h	Receive clock path CTLE offset calibration maintenance =averaging timer: N such that averaging period is $2(N+5)$ fsmclk clock periods where: ($8 \cdot \text{creq_fsmclk_sel_preg}$ ratio) fsmclks=1UI.
15-14	RESERVED	R/W	X	
13	CREQ_CTLSTART_OVR VAL_PREG	R/W	0h	When creq_ctlstart_ovren_preg is asserted this value overrides the receive clock path CTLE FSM start signal from the clock path controller.
12	CREQ_CTLSTART_OVR EN_PREG	R/W	0h	Receive clock path CTLE start active high override enable.
11-10	RESERVED	R/W	X	
9	CREQ_CTLSTART_ACK _OVRVAL_PREG	R/W	0h	When creq_ctlstart_ack_ovren_preg is asserted this value overrides the receive clock path CTLE FSM start signal acknowledge to the clock path controller.
8	CREQ_CTLSTART_ACK _OVRN_PREG	R/W	0h	Receive clock path CTLE start acknowledge active high override enable.
7-5	RESERVED	R/W	X	
4	CREQ_CTLHOLD_FOR CE_PREG	R/W	0h	Receive clock path CTLE FSM hold active high force: When asserted, a CREQ CTLE hold condition will be forced in the regardless of the clock path controller FSM state.
3-2	RESERVED	R/W	X	
1	CREQ_CTLHOLD_ACK _OVRVAL_PREG	R/W	0h	Receive clock path CTLE FSM hold acknowledge active high override value: When creq_ctlhold_ack_ovren_preg is asserted, this value will be used in Clock Path Controller regardless of the CREQ Offset and Equalization FSM state.
0	CREQ_CTLHOLD_ACK _OVRN_PREG	R/W	0h	Receive clock path CTLE FSM hold acknowledge active high override enable: When asserted, a CREQ CTLE hold acknowledge condition will take the creq_ctlhold_ack_ovrval_preg value regardless of the CREQ Offset and Equalization FSM state.

Table 11-453. Register Call Summary for RX_CTLE_MAINTENANCE_PREG__RX_CTLE_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_CTLE_MAINTENANCE_PREG__RX_CTLE_CTRL_PREG_j Register \(Offset = 4120h + formula\) \[reset = X\]: \[0\]](#)

11.151 CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j Register (Offset = 4124h + formula) [reset = X]

CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j is shown in [Figure 11-151](#) and described in [Table 11-455](#).

Return to [Summary Table](#).

Receive clock recovery and equalization (CREQ) state machine clock division register.

Offset = 4124h + (j * 400h); where j = 0h to 1h

Table 11-454. CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4124h + formula
SERDES_16G1	0501 4124h + formula
SERDES_16G2	0502 4124h + formula
SERDES_16G3	0503 4124h + formula

Figure 11-151. CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED		CREQ_HS_IQ_HISTORY_PREG		RESERVED		CREQ_HS_EQ_BIAS_PREG	
R/W-X		R/W-0h		R/W-X		R/W-1h	
23	22	21	20	19	18	17	16
RESERVED				CREQ_FSM_O PEN_EYE_STA NDARD_MODE 3_PREG	CREQ_FSM_O PEN_EYE_STA NDARD_MODE 2_PREG	CREQ_FSM_O PEN_EYE_STA NDARD_MODE 1_PREG	CREQ_FSM_O PEN_EYE_STA NDARD_MODE 0_PREG
R/W-X				R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED		CREQ_FSMCLK_SEL_MODE3_ PREG		RESERVED		CREQ_FSMCLK_SEL_MODE2_ PREG	
R/W-X		R/W-3h		R/W-X		R/W-2h	
7	6	5	4	3	2	1	0
RESERVED		CREQ_FSMCLK_SEL_MODE1_ PREG		RESERVED		CREQ_FSMCLK_SEL_MODE0_ PREG	
R/W-X		R/W-2h		R/W-X		R/W-1h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-455. CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-28	CREQ_HS_IQ_HISTORY_PREG	R/W	0h	Lookback history selection for Undereq/Overeq function. Values represents number of UI in past from current cursor. Lookback (UI) 2'b00 2 2'b01 3 2'b10 4 2'b11 Reserved
27-26	RESERVED	R/W	X	

**Table 11-455. CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
25-24	CREQ_HS_EQ_BIAS_PREG	R/W	1h	Programmable bias control where larger values provides more equalization. Factor 2'b00 1X 2'b01 2X 2'b10 4X 2'b11 Reserved
23-20	RESERVED	R/W	X	
19	CREQ_FSM_OPEN_EYE_STANDARD_MODE3_PREG	R/W	0h	When asserted, clock path equalization will not be performed when xcvr_standard_mode_ln{15:0}[2:0] is 3'b011.
18	CREQ_FSM_OPEN_EYE_STANDARD_MODE2_PREG	R/W	0h	When asserted, clock path equalization will not be performed when xcvr_standard_mode_ln{15:0}[2:0] is 3'b010.
17	CREQ_FSM_OPEN_EYE_STANDARD_MODE1_PREG	R/W	0h	When asserted, clock path equalization will not be performed when xcvr_standard_mode_ln{15:0}[2:0] is 3'b001.
16	CREQ_FSM_OPEN_EYE_STANDARD_MODE0_PREG	R/W	0h	When asserted, clock path equalization will not be performed when xcvr_standard_mode_ln{15:0}[2:0] is 3'b000.
15-14	RESERVED	R/W	X	
13-12	CREQ_FSMCLK_SEL_MODE3_PREG	R/W	3h	This value sets the Clock recovery and equalization (CREQ) state machine clock, fsmclk, division ratio from the Lane Standards Decoder when xcvr_standard_mode_ln{15:0} [2:0] is 3'b011. Division Ratio 2'b00 8 2'b01 16 2'b10 32 2'b11 64
11-10	RESERVED	R/W	X	
9-8	CREQ_FSMCLK_SEL_MODE2_PREG	R/W	2h	This value sets the Clock recovery and equalization (CREQ) state machine clock, fsmclk, division ratio from the Lane Standards Decoder when xcvr_standard_mode_ln{15:0} [2:0] is 3'b010. Division Ratio 2'b00 8 2'b01 16 2'b10 32 2'b11 64
7-6	RESERVED	R/W	X	
5-4	CREQ_FSMCLK_SEL_MODE1_PREG	R/W	2h	This value sets the Clock recovery and equalization (CREQ) state machine clock, fsmclk, division ratio from the Lane Standards Decoder when xcvr_standard_mode_ln{15:0} [2:0] is 3'b001. Division Ratio 2'b00 8 2'b01 16 2'b10 32 2'b11 64
3-2	RESERVED	R/W	X	

**Table 11-455. CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
1-0	CREQ_FSMCLK_SEL_M ODE0_PREG	R/W	1h	This value sets the Clock recovery and equalization (CREQ) state machine clock, fsmclk, division ratio from the Lane Standards Decoder when xcvr_standard_mode_In{15:0} [2:0] is 3'b000. Division Ratio 2'b00 8 2'b01 16 2'b10 32 2'b11 64

Table 11-456. Register Call Summary for CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CREQ_EQ_CTRL_PREG__CREQ_FSMCLK_SEL_PREG_j Register \(Offset = 4124h + formula\) \[reset = X\]: \[0\]](#)

11.152 RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_PREG_j Register (Offset = 4128h + formula) [reset = X]

RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_PREG_j is shown in Figure 11-152 and described in Table 11-458.

Return to [Summary Table](#).

Receive clock recovery and equalization (CREQ) diagnostic bus control register.

Offset = 4128h + (j * 400h); where j = 0h to 1h

**Table 11-457. RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4128h + formula
SERDES_16G1	0501 4128h + formula
SERDES_16G2	0502 4128h + formula
SERDES_16G3	0503 4128h + formula

Figure 11-152. RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_PREG_j Register

31	30	29	28	27	26	25	24
CREQ_DIAG_DATA							
R-0h							
23	22	21	20	19	18	17	16
CREQ_DIAG_DATA							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					RXDA_CREQ_DIAGCAPT_PREG	CREQ_CR_ACCUM2_STICKY_CLR_PREG	CREQ_HS_RESULT_STICKY_CLR_PREG
R/W-X					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CREQ_DIAGSEL_PREG							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-458. RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CREQ_DIAG_DATA	R	0h	Clock recovery and equalization (CREQ) diagnostic bus.
15-11	RESERVED	R/W	X	
10	RXDA_CREQ_DIAGCAPT_PREG	R/W	0h	Clock recovery and equalization (CREQ) diagnostic bus active high capture signal: Writing this bit from low to high will initiate capture of the currently selected diagnostic bus observation point into a register for subsequent read out.
9	CREQ_CR_ACCUM2_STICKY_CLR_PREG	R/W	0h	Clock recovery integral path accumulator sticky saturation clear: Writing this bit to the value opposite the current value triggers clearing of all positive and negative saturation sticky bits available to the diagnostic bus from the clock recovery integral path accumulator.

**Table 11-458. RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
8	CREQ_HS_RESULT_STICKY_CLR_PREG	R/W	0h	Clock path equalization high-speed circuit result sticky saturation clear: Writing this bit to the value opposite the current value triggers clearing of all positive and negative saturation sticky bits available to the diagnostic bus from the Clock path equalization high-speed circuit.
7-0	CREQ_DIAGSEL_PREG	R/W	0h	Clock recovery and equalization (CREQ) diagnostic bus selection: This bus controls what internal signals are read out in diagnostic bus. Note see the rxana_creq Digital Diagnostic Bus Mapping Table for detailed mapping of diagnostic select to test points.

Table 11-459. Register Call Summary for RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_CREQ_DIAG_READ__RX_CREQ_DIAG_SEL_PREG_j Register \(Offset = 4128h + formula\) \[reset = X\]: \[0\]](#)

11.153 CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_SPARE_PREG_j Register (Offset = 412Ch + formula) [reset = X]

CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_SPARE_PREG_j is shown in Figure 11-153 and described in Table 11-461.

Return to [Summary Table](#).

CREQ spare and speedup register

Offset = 412Ch + (j * 400h); where j = 0h to 1h

Table 11-460.

CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_SPARE_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 412Ch + formula
SERDES_16G1	0501 412Ch + formula
SERDES_16G2	0502 412Ch + formula
SERDES_16G3	0503 412Ch + formula

Figure 11-153. CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_SPARE_PREG_j Register

31	30	29	28	27	26	25	24
CREQ_EQ_OPEN_EYE_THRESH_SEL_MODE3_PREG				CREQ_EQ_OPEN_EYE_THRESH_SEL_MODE2_PREG			
R/W-Ch				R/W-Ch			
23	22	21	20	19	18	17	16
CREQ_EQ_OPEN_EYE_THRESH_SEL_MODE1_PREG				CREQ_EQ_OPEN_EYE_THRESH_SEL_MODE0_PREG			
R/W-Ch				R/W-Ch			
15	14	13	12	11	10	9	8
CREQ_SPEED UP_PREG	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
RESERVED						CREQ_SPARE_PREG	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-461. CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_SPARE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CREQ_EQ_OPEN_EYE_THRESH_SEL_MODE3_PREG	R/W	Ch	<p>Selects number of ctle_open_eye (bad codes) to declare a CTLE LUT setting invalid when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.</p> <p>Bad code count</p> <p>4'b0000 Greater than or equal to 1023</p> <p>4'b0001 Greater than or equal to 767</p> <p>4'b0010 Greater than or equal to 511</p> <p>4'b0011 Greater than or equal to 384</p> <p>4'b0100 Greater than or equal to 255</p> <p>4'b0101 Greater than or equal to 191</p> <p>4'b0110 Greater than or equal to 127</p> <p>4'b0111 Greater than or equal to 95</p> <p>4'b1000 Greater than or equal to 63</p> <p>4'b1001 Greater than or equal to 47</p> <p>4'b1010 Greater than or equal to 31</p> <p>4'b1011 Greater than or equal to 23</p> <p>4'b1100 Greater than or equal to 15</p> <p>4'b1101 Greater than or equal to 11</p> <p>4'b1110 Greater than or equal to 7</p> <p>4'b1111 Greater than or equal to 3</p>
27-24	CREQ_EQ_OPEN_EYE_THRESH_SEL_MODE2_PREG	R/W	Ch	<p>Selects number of ctle_open_eye (bad codes) to declare a CTLE LUT setting invalid when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010.</p> <p>Bad code count</p> <p>4'b0000 Greater than or equal to 1023</p> <p>4'b0001 Greater than or equal to 767</p> <p>4'b0010 Greater than or equal to 511</p> <p>4'b0011 Greater than or equal to 384</p> <p>4'b0100 Greater than or equal to 255</p> <p>4'b0101 Greater than or equal to 191</p> <p>4'b0110 Greater than or equal to 127</p> <p>4'b0111 Greater than or equal to 95</p> <p>4'b1000 Greater than or equal to 63</p> <p>4'b1001 Greater than or equal to 47</p> <p>4'b1010 Greater than or equal to 31</p> <p>4'b1011 Greater than or equal to 23</p> <p>4'b1100 Greater than or equal to 15</p> <p>4'b1101 Greater than or equal to 11</p> <p>4'b1110 Greater than or equal to 7</p> <p>4'b1111 Greater than or equal to 3</p>

Table 11-461. CREQ_EQ_OPEN_EYE_THRESH_PREG_CREQ_SPARE_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-20	CREQ_EQ_OPEN_EYE_THRESH_SEL_MODE1_PREG	R/W	Ch	<p>Selects number of ctle_open_eye (bad codes) to declare a CTLE LUT setting invalid when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001.</p> <p>Bad code count</p> <p>4'b0000 Greater than or equal to 1023</p> <p>4'b0001 Greater than or equal to 767</p> <p>4'b0010 Greater than or equal to 511</p> <p>4'b0011 Greater than or equal to 384</p> <p>4'b0100 Greater than or equal to 255</p> <p>4'b0101 Greater than or equal to 191</p> <p>4'b0110 Greater than or equal to 127</p> <p>4'b0111 Greater than or equal to 95</p> <p>4'b1000 Greater than or equal to 63</p> <p>4'b1001 Greater than or equal to 47</p> <p>4'b1010 Greater than or equal to 31</p> <p>4'b1011 Greater than or equal to 23</p> <p>4'b1100 Greater than or equal to 15</p> <p>4'b1101 Greater than or equal to 11</p> <p>4'b1110 Greater than or equal to 7</p> <p>4'b1111 Greater than or equal to 3</p>
19-16	CREQ_EQ_OPEN_EYE_THRESH_SEL_MODE0_PREG	R/W	Ch	<p>Selects number of ctle_open_eye (bad codes) to declare a CTLE LUT setting invalid when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000.</p> <p>Bad code count</p> <p>4'b0000 Greater than or equal to 1023</p> <p>4'b0001 Greater than or equal to 767</p> <p>4'b0010 Greater than or equal to 511</p> <p>4'b0011 Greater than or equal to 384</p> <p>4'b0100 Greater than or equal to 255</p> <p>4'b0101 Greater than or equal to 191</p> <p>4'b0110 Greater than or equal to 127</p> <p>4'b0111 Greater than or equal to 95</p> <p>4'b1000 Greater than or equal to 63</p> <p>4'b1001 Greater than or equal to 47</p> <p>4'b1010 Greater than or equal to 31</p> <p>4'b1011 Greater than or equal to 23</p> <p>4'b1100 Greater than or equal to 15</p> <p>4'b1101 Greater than or equal to 11</p> <p>4'b1110 Greater than or equal to 7</p> <p>4'b1111 Greater than or equal to 3</p>
15	CREQ_SPEEDUP_PREG	R/W	0h	<p>Caution: This register bit must be left at reset value.</p> <p>CREQ active high simulation only speedup enable:</p> <p>When asserted, several CREQ functions are changed to provide simulation only speedups.</p> <p>Note: This bit may only be asserted for simulation where actual CREQ offset and equalization acquisition are not supported or required.</p>
14-2	RESERVED	R/W	X	
1-0	CREQ_SPARE_PREG	R/W	0h	Spare register bits assigned to rxda_creq_spare[1:0].

**Table 11-462. Register Call Summary for
CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_SPARE_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CREQ_EQ_OPEN_EYE_THRESH_PREG__CREQ_SPARE_PREG_j Register \(Offset = 412Ch + formula\) \[reset = X\]: \[0\]](#)

11.154 CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_PREG_j Register (Offset = 4130h + formula) [reset = X]

CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_PREG_j is shown in Figure 11-154 and described in Table 11-464.

Return to [Summary Table](#).

Receive clock Path CTLE LUT control register.

Offset = 4130h + (j * 400h); where j = 0h to 1h

**Table 11-463. CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4130h + formula
SERDES_16G1	0501 4130h + formula
SERDES_16G2	0502 4130h + formula
SERDES_16G3	0503 4130h + formula

Figure 11-154. CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
CTLELUT_OVR EN_PREG	RESERVED						
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CTLELUT_SEL_MODE3_PREG				CTLELUT_SEL_MODE2_PREG			
R/W-8h				R/W-4h			
7	6	5	4	3	2	1	0
CTLELUT_SEL_MODE1_PREG				CTLELUT_SEL_MODE0_PREG			
R/W-2h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-464. CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CTLELUT_OVREN_PREG	R/W	0h	Receive clock Path CTLE LUT active high override table enable: When asserted the following CDB based override LUT table is used rather than the Lane Standards Decoder tables.
30-16	RESERVED	R/W	X	
15-12	CTLELUT_SEL_MODE3_PREG	R/W	8h	Selects the CTLE LUT from the Lane Standards Decoder to use when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011.
11-8	CTLELUT_SEL_MODE2_PREG	R/W	4h	Selects the CTLE LUT from the Lane Standards Decoder to use when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010.
7-4	CTLELUT_SEL_MODE1_PREG	R/W	2h	Selects the CTLE LUT from the Lane Standards Decoder to use when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001.
3-0	CTLELUT_SEL_MODE0_PREG	R/W	0h	Selects the CTLE LUT from the Lane Standards Decoder to use when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000.

Table 11-465. Register Call Summary for CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVRDCTRL_PREG__CTLELUT_CTRL_PREG_j Register \(Offset = 4130h + formula\) \[reset = X\]: \[0\]](#)

11.155 CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_PREG_j Register (Offset = 4134h + formula) [reset = X]

CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_PREG_j is shown in Figure 11-155 and described in Table 11-467.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 0 register.

Offset = 4134h + (j * 400h); where j = 0h to 1h

**Table 11-466. CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4134h + formula
SERDES_16G1	0501 4134h + formula
SERDES_16G2	0502 4134h + formula
SERDES_16G3	0503 4134h + formula

Figure 11-155. CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_0_PR EG	CTLELUT_IND EN2OVR_0_PR EG	CTLELUT_IND EN3OVR_0_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_0_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_0_PREG			RESERVED	CTLELUT_RATESEL2OVR_0_PREG		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_0_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_0_ PREG
R/W-X	R/W-0h			R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-467. CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_0_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 0
25	CTLELUT_INDEN2OVR_0_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 0
24	CTLELUT_INDEN3OVR_0_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 0
23-20	RESERVED	R/W	X	

**Table 11-467. CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_0_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 0 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_0_PREG	R/W	0h	Clock Path CTLE LUT ratesel1 Override Value, Entry 0 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_0_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 0 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_0_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 0 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_0_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 0 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-468. Register Call Summary for CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_0B_PREG__CTLELUT_OVR_0A_PREG_j Register \(Offset = 4134h + formula\) \[reset = X\]: \[0\]](#)

11.156 CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_PREG_j Register (Offset = 4138h + formula) [reset = X]

CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_PREG_j is shown in Figure 11-156 and described in Table 11-470.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 1 register.

Offset = 4138h + (j * 400h); where j = 0h to 1h

Table 11-469. CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4138h + formula
SERDES_16G1	0501 4138h + formula
SERDES_16G2	0502 4138h + formula
SERDES_16G3	0503 4138h + formula

Figure 11-156. CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_1_PR EG	CTLELUT_IND EN2OVR_1_PR EG	CTLELUT_IND EN3OVR_1_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_1_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_1_PREG			RESERVED	CTLELUT_RATESEL2OVR_1_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_1_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_1_ PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-470. CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_1_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 1
25	CTLELUT_INDEN2OVR_1_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 1
24	CTLELUT_INDEN3OVR_1_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 1
23-20	RESERVED	R/W	X	

**Table 11-470. CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_1_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 1 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_1_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 1 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_1_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 1 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_1_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 1 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_1_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 1 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-471. Register Call Summary for CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_1B_PREG__CTLELUT_OVR_1A_PREG_j Register \(Offset = 4138h + formula\) \[reset = X\]: \[0\]](#)

11.157 CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_PREG_j Register (Offset = 413Ch + formula) [reset = X]

CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_PREG_j is shown in Figure 11-157 and described in Table 11-473.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 2 register.

Offset = 413Ch + (j * 400h); where j = 0h to 1h

**Table 11-472. CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 413Ch + formula
SERDES_16G1	0501 413Ch + formula
SERDES_16G2	0502 413Ch + formula
SERDES_16G3	0503 413Ch + formula

Figure 11-157. CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_2_PR EG	CTLELUT_IND EN2OVR_2_PR EG	CTLELUT_IND EN3OVR_2_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_2_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_2_PREG			RESERVED	CTLELUT_RATESEL2OVR_2_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_2_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_2_ PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-473. CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_2_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 2
25	CTLELUT_INDEN2OVR_2_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 2
24	CTLELUT_INDEN3OVR_2_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 2
23-20	RESERVED	R/W	X	

**Table 11-473. CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_2_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 2 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_2_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 2 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_2_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 2 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_2_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 2 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_2_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 2 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-474. Register Call Summary for CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_2B_PREG__CTLELUT_OVR_2A_PREG_j Register \(Offset = 413Ch + formula\) \[reset = X\]: \[0\]](#)

11.158 CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_PREG_j Register (Offset = 4140h + formula) [reset = X]

CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_PREG_j is shown in Figure 11-158 and described in Table 11-476.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 3 register.

Offset = 4140h + (j * 400h); where j = 0h to 1h

Table 11-475. CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4140h + formula
SERDES_16G1	0501 4140h + formula
SERDES_16G2	0502 4140h + formula
SERDES_16G3	0503 4140h + formula

Figure 11-158. CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_3_PR EG	CTLELUT_IND EN2OVR_3_PR EG	CTLELUT_IND EN3OVR_3_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_3_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_3_PREG			RESERVED	CTLELUT_RATESEL2OVR_3_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_3_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_3_ PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-476. CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_3_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 3
25	CTLELUT_INDEN2OVR_3_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 3
24	CTLELUT_INDEN3OVR_3_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 3
23-20	RESERVED	R/W	X	

**Table 11-476. CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_3_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 3 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_3_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 3 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_3_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 3 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_3_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 3 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_3_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 3 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-477. Register Call Summary for CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_3B_PREG__CTLELUT_OVR_3A_PREG_j Register \(Offset = 4140h + formula\) \[reset = X\]: \[0\]](#)

11.159 CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_PREG_j Register (Offset = 4144h + formula) [reset = X]

CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_PREG_j is shown in Figure 11-159 and described in Table 11-479.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 4 register.

Offset = 4144h + (j * 400h); where j = 0h to 1h

**Table 11-478. CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4144h + formula
SERDES_16G1	0501 4144h + formula
SERDES_16G2	0502 4144h + formula
SERDES_16G3	0503 4144h + formula

Figure 11-159. CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_4_PR EG	CTLELUT_IND EN2OVR_4_PR EG	CTLELUT_IND EN3OVR_4_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_4_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_4_PREG			RESERVED	CTLELUT_RATESEL2OVR_4_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_4_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_4_ PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-479. CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_4_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 4
25	CTLELUT_INDEN2OVR_4_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 4
24	CTLELUT_INDEN3OVR_4_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 4
23-20	RESERVED	R/W	X	

**Table 11-479. CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_4_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 4 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_4_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 4 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_4_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 4 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_4_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 4 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_4_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 4 1'b0 Minimum 1'b1 Maximum

Table 11-480. Register Call Summary for CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_4B_PREG__CTLELUT_OVR_4A_PREG_j Register \(Offset = 4144h + formula\) \[reset = X\]: \[0\]](#)

11.160 CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_PREG_j Register (Offset = 4148h + formula) [reset = X]

CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_PREG_j is shown in Figure 11-160 and described in Table 11-482.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 5 register.

Offset = 4148h + (j * 400h); where j = 0h to 1h

Table 11-481. CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4148h + formula
SERDES_16G1	0501 4148h + formula
SERDES_16G2	0502 4148h + formula
SERDES_16G3	0503 4148h + formula

Figure 11-160. CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_5_PR EG	CTLELUT_IND EN2OVR_5_PR EG	CTLELUT_IND EN3OVR_5_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_5_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_5_PREG			RESERVED	CTLELUT_RATESEL2OVR_5_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_5_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_5_ PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-482. CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_5_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 5
25	CTLELUT_INDEN2OVR_5_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 5
24	CTLELUT_INDEN3OVR_5_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 5
23-20	RESERVED	R/W	X	

**Table 11-482. CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_5_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 5 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_5_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 5 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_5_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 5 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_5_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 5 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_5_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 5 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-483. Register Call Summary for CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_5B_PREG__CTLELUT_OVR_5A_PREG_j Register \(Offset = 4148h + formula\) \[reset = X\]: \[0\]](#)

11.161 CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_PREG_j Register (Offset = 414Ch + formula) [reset = X]

CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_PREG_j is shown in Figure 11-161 and described in Table 11-485.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 6 register.

Offset = 414Ch + (j * 400h); where j = 0h to 1h

Table 11-484. CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 414Ch + formula
SERDES_16G1	0501 414Ch + formula
SERDES_16G2	0502 414Ch + formula
SERDES_16G3	0503 414Ch + formula

Figure 11-161. CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_6_PR EG	CTLELUT_IND EN2OVR_6_PR EG	CTLELUT_IND EN3OVR_6_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_6_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_6_PREG			RESERVED	CTLELUT_RATESEL2OVR_6_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_6_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_6_ PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-485. CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_6_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 6
25	CTLELUT_INDEN2OVR_6_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 6
24	CTLELUT_INDEN3OVR_6_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 6
23-20	RESERVED	R/W	X	

**Table 11-485. CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_6_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 6 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_6_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 6 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_6_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 6 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_6_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 6 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_6_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 6 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-486. Register Call Summary for CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_6B_PREG__CTLELUT_OVR_6A_PREG_j Register \(Offset = 414Ch + formula\) \[reset = X\]: \[0\]](#)

11.162 CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_PREG_j Register (Offset = 4150h + formula) [reset = X]

CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_PREG_j is shown in Figure 11-162 and described in Table 11-488.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 7 register.

Offset = 4150h + (j * 400h); where j = 0h to 1h

**Table 11-487. CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4150h + formula
SERDES_16G1	0501 4150h + formula
SERDES_16G2	0502 4150h + formula
SERDES_16G3	0503 4150h + formula

Figure 11-162. CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_7_PR EG	CTLELUT_IND EN2OVR_7_PR EG	CTLELUT_IND EN3OVR_7_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_7_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_7_PREG			RESERVED	CTLELUT_RATESEL2OVR_7_PREG		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_7_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_7_ PREG
R/W-X	R/W-0h			R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-488. CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_7_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 7
25	CTLELUT_INDEN2OVR_7_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 7
24	CTLELUT_INDEN3OVR_7_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 7
23-20	RESERVED	R/W	X	

**Table 11-488. CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_7_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 7 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_7_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 7 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_7_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 7 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_7_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 7 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_7_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 7 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-489. Register Call Summary for CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_7B_PREG__CTLELUT_OVR_7A_PREG_j Register \(Offset = 4150h + formula\) \[reset = X\]: \[0\]](#)

11.163 CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_PREG_j Register (Offset = 4154h + formula) [reset = X]

CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_PREG_j is shown in Figure 11-163 and described in Table 11-491.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 8 register.

Offset = 4154h + (j * 400h); where j = 0h to 1h

**Table 11-490. CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4154h + formula
SERDES_16G1	0501 4154h + formula
SERDES_16G2	0502 4154h + formula
SERDES_16G3	0503 4154h + formula

Figure 11-163. CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_8_PR EG	CTLELUT_IND EN2OVR_8_PR EG	CTLELUT_IND EN3OVR_8_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_8_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_8_PREG			RESERVED	CTLELUT_RATESEL2OVR_8_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_8_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_8_ PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-491. CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_8_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 8
25	CTLELUT_INDEN2OVR_8_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 8
24	CTLELUT_INDEN3OVR_8_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 8
23-20	RESERVED	R/W	X	

**Table 11-491. CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_8_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 8 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_8_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 8 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_8_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 8 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_8_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 8 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_8_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 8 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-492. Register Call Summary for CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_8B_PREG__CTLELUT_OVR_8A_PREG_j Register \(Offset = 4154h + formula\) \[reset = X\]: \[0\]](#)

11.164 CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_PREG_j Register (Offset = 4158h + formula) [reset = X]

CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_PREG_j is shown in Figure 11-164 and described in Table 11-494.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 9 register.

Offset = 4158h + (j * 400h); where j = 0h to 1h

Table 11-493. CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4158h + formula
SERDES_16G1	0501 4158h + formula
SERDES_16G2	0502 4158h + formula
SERDES_16G3	0503 4158h + formula

Figure 11-164. CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_9_PR EG	CTLELUT_IND EN2OVR_9_PR EG	CTLELUT_IND EN3OVR_9_PR EG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_9_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_9_PREG			RESERVED	CTLELUT_RATESEL2OVR_9_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_9_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_9_ PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-494. CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_9_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 9
25	CTLELUT_INDEN2OVR_9_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 9
24	CTLELUT_INDEN3OVR_9_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 9
23-20	RESERVED	R/W	X	

**Table 11-494. CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_9_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 9 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_9_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 9 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_9_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 9 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_9_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 9 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_9_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 9 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-495. Register Call Summary for CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_9B_PREG__CTLELUT_OVR_9A_PREG_j Register \(Offset = 4158h + formula\) \[reset = X\]: \[0\]](#)

11.165 CTLELUT_OVR_10B_PREG_CTLELUT_OVR_10A_PREG_j Register (Offset = 415Ch + formula) [reset = X]

CTLELUT_OVR_10B_PREG_CTLELUT_OVR_10A_PREG_j is shown in Figure 11-165 and described in Table 11-497.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 10 register.

Offset = 415Ch + (j * 400h); where j = 0h to 1h

**Table 11-496. CTLELUT_OVR_10B_PREG_CTLELUT_OVR_10A_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 415Ch + formula
SERDES_16G1	0501 415Ch + formula
SERDES_16G2	0502 415Ch + formula
SERDES_16G3	0503 415Ch + formula

Figure 11-165. CTLELUT_OVR_10B_PREG_CTLELUT_OVR_10A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_10_P REG	CTLELUT_IND EN2OVR_10_P REG	CTLELUT_IND EN3OVR_10_P REG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_10_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_10_PREG			RESERVED	CTLELUT_RATESEL2OVR_10_PREG		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_10_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_10 _PREG
R/W-X	R/W-0h			R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-497. CTLELUT_OVR_10B_PREG_CTLELUT_OVR_10A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_10_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 10
25	CTLELUT_INDEN2OVR_10_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 10
24	CTLELUT_INDEN3OVR_10_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 10
23-20	RESERVED	R/W	X	

**Table 11-497. CTLELUT_OVR_10B_PREG__CTLELUT_OVR_10A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_10_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 10 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_10_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 10 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_10_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 10 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_10_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 10 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_10_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 10 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-498. Register Call Summary for CTLELUT_OVR_10B_PREG__CTLELUT_OVR_10A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_10B_PREG__CTLELUT_OVR_10A_PREG_j Register \(Offset = 415Ch + formula\) \[reset = X\]: \[0\]](#)

11.166 CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j Register (Offset = 4160h + formula) [reset = X]

CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j is shown in Figure 11-166 and described in Table 11-500.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 11 register.

Offset = 4160h + (j * 400h); where j = 0h to 1h

Table 11-499. CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4160h + formula
SERDES_16G1	0501 4160h + formula
SERDES_16G2	0502 4160h + formula
SERDES_16G3	0503 4160h + formula

Figure 11-166. CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_11_P REG	CTLELUT_IND EN2OVR_11_P REG	CTLELUT_IND EN3OVR_11_P REG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_11_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_11_PREG			RESERVED	CTLELUT_RATESEL2OVR_11_PREG		
R/W-X		R/W-0h		R/W-X		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_11_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_11 _PREG
R/W-X		R/W-0h		R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-500. CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_11_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 11
25	CTLELUT_INDEN2OVR_11_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 11
24	CTLELUT_INDEN3OVR_11_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 11
23-20	RESERVED	R/W	X	

**Table 11-500. CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_11_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 11 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_11_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 11 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_11_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 11 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_11_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 11 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_11_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 11 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-501. Register Call Summary for CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_11B_PREG__CTLELUT_OVR_11A_PREG_j Register \(Offset = 4160h + formula\) \[reset = X\]: \[0\]](#)

11.167 CTLELUT_OVR_12B_PREG_CTLELUT_OVR_12A_PREG_j Register (Offset = 4164h + formula) [reset = X]

CTLELUT_OVR_12B_PREG_CTLELUT_OVR_12A_PREG_j is shown in [Figure 11-167](#) and described in [Table 11-503](#).

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 12 register.

Offset = 4164h + (j * 400h); where j = 0h to 1h

Table 11-502. CTLELUT_OVR_12B_PREG_CTLELUT_OVR_12A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4164h + formula
SERDES_16G1	0501 4164h + formula
SERDES_16G2	0502 4164h + formula
SERDES_16G3	0503 4164h + formula

Figure 11-167. CTLELUT_OVR_12B_PREG_CTLELUT_OVR_12A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_12_P REG	CTLELUT_IND EN2OVR_12_P REG	CTLELUT_IND EN3OVR_12_P REG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_12_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_12_PREG			RESERVED	CTLELUT_RATESEL2OVR_12_PREG		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_12_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_12 _PREG
R/W-X	R/W-0h			R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-503. CTLELUT_OVR_12B_PREG_CTLELUT_OVR_12A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_12_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 12
25	CTLELUT_INDEN2OVR_12_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 12
24	CTLELUT_INDEN3OVR_12_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 12
23-20	RESERVED	R/W	X	

**Table 11-503. CTLELUT_OVR_12B_PREG__CTLELUT_OVR_12A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_12_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 12 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_12_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 12 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_12_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 12 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_12_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 12 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_12_PREG	R/W	0h	Clock Path CTLE LUT stage 4 tdata rate per bandwidth selection override, Entry 12 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-504. Register Call Summary for CTLELUT_OVR_12B_PREG__CTLELUT_OVR_12A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_12B_PREG__CTLELUT_OVR_12A_PREG_j Register \(Offset = 4164h + formula\) \[reset = X\]: \[0\]](#)

11.168 CTLELUT_OVR_13B_PREG_CTLELUT_OVR_13A_PREG_j Register (Offset = 4168h + formula) [reset = X]

CTLELUT_OVR_13B_PREG_CTLELUT_OVR_13A_PREG_j is shown in [Figure 11-168](#) and described in [Table 11-506](#).

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 13 register.

Offset = 4168h + (j * 400h); where j = 0h to 1h

Table 11-505. CTLELUT_OVR_13B_PREG_CTLELUT_OVR_13A_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4168h + formula
SERDES_16G1	0501 4168h + formula
SERDES_16G2	0502 4168h + formula
SERDES_16G3	0503 4168h + formula

Figure 11-168. CTLELUT_OVR_13B_PREG_CTLELUT_OVR_13A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_13_P REG	CTLELUT_IND EN2OVR_13_P REG	CTLELUT_IND EN3OVR_13_P REG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_13_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_13_PREG			RESERVED	CTLELUT_RATESEL2OVR_13_PREG		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_13_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_13 _PREG
R/W-X	R/W-0h			R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-506. CTLELUT_OVR_13B_PREG_CTLELUT_OVR_13A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_13_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 13
25	CTLELUT_INDEN2OVR_13_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 13
24	CTLELUT_INDEN3OVR_13_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 13
23-20	RESERVED	R/W	X	

**Table 11-506. CTLELUT_OVR_13B_PREG__CTLELUT_OVR_13A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_13_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 13 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_13_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 13 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_13_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 13 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_13_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 13 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_13_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 13 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-507. Register Call Summary for CTLELUT_OVR_13B_PREG__CTLELUT_OVR_13A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_13B_PREG__CTLELUT_OVR_13A_PREG_j Register \(Offset = 4168h + formula\) \[reset = X\]: \[0\]](#)

11.169 CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j Register (Offset = 416Ch + formula) [reset = X]

CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j is shown in Figure 11-169 and described in Table 11-509.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 14 register.

Offset = 416Ch + (j * 400h); where j = 0h to 1h

**Table 11-508. CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 416Ch + formula
SERDES_16G1	0501 416Ch + formula
SERDES_16G2	0502 416Ch + formula
SERDES_16G3	0503 416Ch + formula

Figure 11-169. CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_14_P REG	CTLELUT_IND EN2OVR_14_P REG	CTLELUT_IND EN3OVR_14_P REG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_14_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_14_PREG			RESERVED	CTLELUT_RATESEL2OVR_14_PREG		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_14_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_14 _PREG
R/W-X	R/W-0h			R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-509. CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_14_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 14
25	CTLELUT_INDEN2OVR_14_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 14
24	CTLELUT_INDEN3OVR_14_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 14
23-20	RESERVED	R/W	X	

**Table 11-509. CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_14_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 14 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_14_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 14 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_14_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 14 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_14_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 14 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_14_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 14 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-510. Register Call Summary for CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_14B_PREG__CTLELUT_OVR_14A_PREG_j Register \(Offset = 416Ch + formula\) \[reset = X\]: \[0\]](#)

11.170 CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j Register (Offset = 4170h + formula) [reset = X]

CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j is shown in Figure 11-170 and described in Table 11-512.

Return to [Summary Table](#).

Receive clock path CTLE LUT ratesel override, entry 15 register.

Offset = 4170h + (j * 400h); where j = 0h to 1h

**Table 11-511. CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4170h + formula
SERDES_16G1	0501 4170h + formula
SERDES_16G2	0502 4170h + formula
SERDES_16G3	0503 4170h + formula

Figure 11-170. CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED					CTLELUT_IND EN1OVR_15_P REG	CTLELUT_IND EN2OVR_15_P REG	CTLELUT_IND EN3OVR_15_P REG
R/W-X					R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CTLELUT_CSELOVR_15_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	CTLELUT_RATESEL1OVR_15_PREG			RESERVED	CTLELUT_RATESEL2OVR_15_PREG		
R/W-X	R/W-0h			R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	CTLELUT_RATESEL3OVR_15_PREG			RESERVED			CTLELUT_RAT ESEL4OVR_15 _PREG
R/W-X	R/W-0h			R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-512. CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26	CTLELUT_INDEN1OVR_15_PREG	R/W	0h	Clock Path CTLE LUT stage 1 active high inductor enable override, Entry 15
25	CTLELUT_INDEN2OVR_15_PREG	R/W	0h	Clock Path CTLE LUT stage 2 active high inductor enable override, Entry 15
24	CTLELUT_INDEN3OVR_15_PREG	R/W	0h	Clock Path CTLE LUT stage 3 active high inductor enable override, Entry 15
23-20	RESERVED	R/W	X	

**Table 11-512. CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
19-16	CTLELUT_CSELOVR_15_PREG	R/W	0h	Clock Path CTLE LUT binary encoded boost / peaking control override, Entry 15 Boost amount 4'b0000 Minimum :: 4'b1111 Maximum
15	RESERVED	R/W	X	
14-12	CTLELUT_RATESEL1OVR_15_PREG	R/W	0h	Clock Path CTLE LUT stage 1 thermometer encoded data rate per bandwidth selection override, Entry 15 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
11	RESERVED	R/W	X	
10-8	CTLELUT_RATESEL2OVR_15_PREG	R/W	0h	Clock Path CTLE LUT stage 2 thermometer encoded data rate per bandwidth selection override, Entry 15 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
7	RESERVED	R/W	X	
6-4	CTLELUT_RATESEL3OVR_15_PREG	R/W	0h	Clock Path CTLE LUT stage 3 thermometer encoded data rate per bandwidth selection override, Entry 15 Data rate / BW 3'b000 Minimum 3'b001 Lower Mid-range 3'b011 Upper Mid-range 3'b111 Maximum
3-1	RESERVED	R/W	X	
0	CTLELUT_RATESEL4OVR_15_PREG	R/W	0h	Clock Path CTLE LUT stage 4 data rate per bandwidth selection override, Entry 15 Data rate / BW 1'b0 Minimum 1'b1 Maximum

Table 11-513. Register Call Summary for CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CTLELUT_OVR_15B_PREG__CTLELUT_OVR_15A_PREG_j Register \(Offset = 4170h + formula\) \[reset = X\]: \[0\]](#)

11.171 DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j Register (Offset = 4180h + formula) [reset = X]

DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j is shown in [Figure 11-171](#) and described in [Table 11-515](#).

Return to [Summary Table](#).

Receive data path DFE error comparator rate selection register.

Offset = 4180h + (j * 400h); where j = 0h to 1h

Table 11-514. DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4180h + formula
SERDES_16G1	0501 4180h + formula
SERDES_16G2	0502 4180h + formula
SERDES_16G3	0503 4180h + formula

Figure 11-171. DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	SMP_RATESEL_MODE3_PREG			RESERVED	SMP_RATESEL_MODE2_PREG		
R/W-X	R/W-4h			R/W-X	R/W-1h		
23	22	21	20	19	18	17	16
RESERVED	SMP_RATESEL_MODE1_PREG			RESERVED	SMP_RATESEL_MODE0_PREG		
R/W-X	R/W-1h			R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED	ECMP_RATESEL_MODE3_PREG			RESERVED	ECMP_RATESEL_MODE2_PREG		
R/W-X	R/W-4h			R/W-X	R/W-1h		
7	6	5	4	3	2	1	0
RESERVED	ECMP_RATESEL_MODE1_PREG			RESERVED	ECMP_RATESEL_MODE0_PREG		
R/W-X	R/W-1h			R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-515. DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	SMP_RATESEL_MODE3_PREG	R/W	4h	This value sets the receive data path DFE sampler rate selection when xcvr_standard_mode_in_{15:0}[2:0] is 3'b011. Data rate 3'b000 less than 5Gbps 3'b001 less than or equal to 8Gbps and greater than or equal to 5Gbps 3'b010 less than or equal to 12.5Gbps and greater than or equal to 10.3Gbps 3'b100 less than or equal to 16Gbps and greater than or equal to 15Gbps
27	RESERVED	R/W	X	

**Table 11-515. DFE_SMP_RATESEL_PREG_DFE_ECMP_RATESEL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26-24	SMP_RATESEL_MODE2_PREG	R/W	1h	This value sets the receive data path DFE sampler rate selection when <code>xcvr_standard_mode_in_{15:0}[2:0]</code> is 3'b010. Data rate 3'b000 less than 5Gbps 3'b001 less than or equal to 8Gbps and greater than or equal to 5Gbps 3'b010 less than or equal to 12.5Gbps and greater than or equal to 10.3Gbps 3'b100 less than or equal to 16Gbps and greater than or equal to 15Gbps
23	RESERVED	R/W	X	
22-20	SMP_RATESEL_MODE1_PREG	R/W	1h	This value sets the receive data path DFE sampler rate selection when <code>xcvr_standard_mode_in_{15:0}[2:0]</code> is 3'b001. Data rate 3'b000 less than 5Gbps 3'b001 less than or equal to 8Gbps and greater than or equal to 5Gbps 3'b010 less than or equal to 12.5Gbps and greater than or equal to 10.3Gbps 3'b100 less than or equal to 16Gbps and greater than or equal to 15Gbps
19	RESERVED	R/W	X	
18-16	SMP_RATESEL_MODE0_PREG	R/W	0h	This value sets the receive data path DFE sampler rate selection when <code>xcvr_standard_mode_in_{15:0}[2:0]</code> is 3'b000. Data rate 3'b000 less than 5Gbps 3'b001 less than or equal to 8Gbps and greater than or equal to 5Gbps 3'b010 less than or equal to 12.5Gbps and greater than or equal to 10.3Gbps 3'b100 less than or equal to 16Gbps and greater than or equal to 15Gbps
15	RESERVED	R/W	X	
14-12	ECMP_RATESEL_MODE3_PREG	R/W	4h	This value sets the Lane Standards Decoder driven value for receive data path DFE error comparator rate selection when <code>xcvr_standard_mode_in_{15:0}[2:0]</code> is 3'b011. Data rate 3'b000 less than 5Gbps 3'b001 less than or equal to 8Gbps and greater than or equal to 5Gbps 3'b010 less than or equal to 12.5Gbps and greater than or equal to 10.3Gbps 3'b100 less than or equal to 16Gbps and greater than or equal to 15Gbps
11	RESERVED	R/W	X	

**Table 11-515. DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
10-8	ECMP_RATESEL_MODE 2_PREG	R/W	1h	This value sets the Lane Standards Decoder driven value for receive data path DFE error comparator rate selection when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010. Data rate 3'b000 less than 5Gbps 3'b001 less than or equal to 8Gbps and greater than or equal to 5Gbps 3'b010 less than or equal to 12.5Gbps and greater than or equal to 10.3Gbps 3'b100 less than or equal to 16Gbps and greater than or equal to 15Gbps
7	RESERVED	R/W	X	
6-4	ECMP_RATESEL_MODE 1_PREG	R/W	1h	This value sets the Lane Standards Decoder driven value for receive data path DFE error comparator rate selection when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001. Data rate 3'b000 less than 5Gbps 3'b001 less than or equal to 8Gbps and greater than or equal to 5Gbps 3'b010 less than or equal to 12.5Gbps and greater than or equal to 10.3Gbps 3'b100 less than or equal to 16Gbps and greater than or equal to 15Gbps
3	RESERVED	R/W	X	
2-0	ECMP_RATESEL_MODE 0_PREG	R/W	0h	This value sets the Lane Standards Decoder driven value for receive data path DFE error comparator rate selection when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000. Data rate 3'b000 less than 5Gbps 3'b001 less than or equal to 8Gbps and greater than or equal to 5Gbps 3'b010 less than or equal to 12.5Gbps and greater than or equal to 10.3Gbps 3'b100 less than or equal to 16Gbps and greater than or equal to 15Gbps

Table 11-516. Register Call Summary for DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DFE_SMP_RATESEL_PREG__DFE_ECMP_RATESEL_PREG_j Register \(Offset = 4180h + formula\) \[reset = X\]: \[0\]](#)

11.172 DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j Register (Offset = 4184h + formula) [reset = X]

DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j is shown in [Figure 11-172](#) and described in [Table 11-518](#).

Return to [Summary Table](#).

Receive data path equalization (DEQ) diagnostic bus control register.

Offset = 4184h + (j * 400h); where j = 0h to 1h

Table 11-517.
DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4184h + formula
SERDES_16G1	0501 4184h + formula
SERDES_16G2	0502 4184h + formula
SERDES_16G3	0503 4184h + formula

Figure 11-172. DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DEQ_DIAG_DATA															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEQ_DIAG_SEL_PREG							
R/W-X								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-518. DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DEQ_DIAG_DATA	R	0h	Receive data path equalization (DEQ) diagnostic bus.
15-8	RESERVED	R/W	X	
7-0	DEQ_DIAG_SEL_PREG	R/W	0h	Receive data path equalization (DEQ) diagnostic bus selection: This bus controls what internal signals are read out in diagnostic bus. See the Receive Data Path Digital Diganostic Bus Mapping Table for a detailed listing of test points.

Table 11-519. Register Call Summary for DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_DIAG_READ__DEQ_DIAG_SEL_PREG_j Register \(Offset = 4184h + formula\) \[reset = X\]: \[0\]](#)

11.173 DEQ_PHALIGN_CTRL_j Register (Offset = 4188h + formula) [reset = X]

DEQ_PHALIGN_CTRL_j is shown in Figure 11-173 and described in Table 11-521.

Return to [Summary Table](#).

Receive data path phase alignment control register

Offset = 4188h + (j * 400h); where j = 0h to 1h

Table 11-520. DEQ_PHALIGN_CTRL_j Instances

Instance	Physical Address
SERDES_16G0	0500 4188h + formula
SERDES_16G1	0501 4188h + formula
SERDES_16G2	0502 4188h + formula
SERDES_16G3	0503 4188h + formula

Figure 11-173. DEQ_PHALIGN_CTRL_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DEQ_PHALIGN_SAMP SIZE_PREG	
R/W-X						R/W-3h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-521. DEQ_PHALIGN_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	DEQ_PHALIGN_SAMP SIZE_PREG	R/W	3h	Selection of sample size used to determine the position of the ecmp_clk_n rising edge in the ST_B1_EVAL state of the rxana_deq_phalign FSM: Sample size 2'b11 63 2'b10 31 2'b01 15 2'b00 7

Table 11-522. Register Call Summary for DEQ_PHALIGN_CTRL_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_PHALIGN_CTRL_j Register \(Offset = 4188h + formula\) \[reset = X\]: \[0\]](#)

11.174 DEQ_CONCUR_CTRL2_PREG__DEQ_CONCUR_CTRL1_PREG_j Register (Offset = 4190h + formula) [reset = 52242A20h]

DEQ_CONCUR_CTRL2_PREG__DEQ_CONCUR_CTRL1_PREG_j is shown in Figure 11-174 and described in Table 11-524.

Return to [Summary Table](#).

Receive data path concurrent equalization control register 1.

Offset = 4190h + (j * 400h); where j = 0h to 1h

Table 11-523. DEQ_CONCUR_CTRL2_PREG__DEQ_CONCUR_CTRL1_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4190h + formula
SERDES_16G1	0501 4190h + formula
SERDES_16G2	0502 4190h + formula
SERDES_16G3	0503 4190h + formula

Figure 11-174. DEQ_CONCUR_CTRL2_PREG__DEQ_CONCUR_CTRL1_PREG_j Register

31	30	29	28	27	26	25	24
CONCUR_TIME_SPEEDUP_PREG	CONCUR_TXACK_TIMEOUT_PREG			CONCUR_TIME_MNT_PREG			
R/W-0h	R/W-5h			R/W-2h			
23	22	21	20	19	18	17	16
CONCUR_TIME_ACQ_PREG				CONCUR_TXACKITER_PREG			
R/W-2h				R/W-4h			
15	14	13	12	11	10	9	8
DEQ_CLEARSTATFLAGS_PREG	CONCUR_MINITER_PREG						
W-0h	R/W-A8h						
7	6	5	4	3	2	1	0
CONCUR_MINITER_PREG		CONCUR_MAXTXREQ_PREG					
R/W-A8h		R/W-20h					

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-524. DEQ_CONCUR_CTRL2_PREG__DEQ_CONCUR_CTRL1_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CONCUR_TIME_SPEEDUP_PREG	R/W	0h	Concurrent equalization active high simulation speedup enable: When asserted, several CREQ functions are changed to provide simulation only speedups. In particular, the he concur_time_mnt_preg, concur_time_acq_preg, the concur_txack_timeout_preg, and the concur_txack_timeout_preg timer delays are shortened. Note: This bit may only be asserted for simulation where actual data equalization acquisition and maintenance are not supported or required.

Table 11-524. DEQ_CONCUR_CTRL2_PREG_DEQ_CONCUR_CTRL1_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30-28	CONCUR_TXACK_TIME_OUT_PREG	R/W	5h	Receive closed-eye data path equalization timeout waiting for next rx_eq_eval assertion. If this timeout is reached, the equalization is declared done. The time is $2^{(\text{concur_txack_timeout_preg}+16)}_1$ rx_rd_clk_ln_{15:0} periods.
27-24	CONCUR_TIME_MNT_PREG	R/W	2h	Receive closed-eye data path equalization concurrent process time during maintenance. The time is $2^{(\text{concur_time_mnt_preg}+7)}_1$ rx_rd_clk_ln_{15:0} periods.
23-20	CONCUR_TIME_ACQ_PREG	R/W	2h	Receive closed-eye data path equalization concurrent process time during acquisition. The time is $2^{(\text{concur_time_acq_preg}+7)}_1$ rx_rd_clk_ln_{15:0} periods.
19-16	CONCUR_TXACKITER_PREG	R/W	4h	Receive closed-eye data path equalization minimum iterations of concur and tau processes after a far-end transmit equalization acknowledgement before a new far-end transmit request can be made. Note: The value must be 1 or greater. Note: this field is read at each new request.
15	DEQ_CLEARSTFLGSPREG	W	0h	Toggle style bit which when written high clears the equalization saturation flags of all concurrent algorithms.
14-6	CONCUR_MINITER_PREG	R/W	A8h	Receive closed-eye data path equalization minimum iterations of concur and tau processes during acquisition. Note: iteration minimum is concur_miniter_preg + 1. The value must be 1 or greater.
5-0	CONCUR_MAXTXREQ_PREG	R/W	20h	Receive closed-eye data path equalization maximum far-end transmit equalization requests. The value must be 1 or greater.

Table 11-525. Register Call Summary for DEQ_CONCUR_CTRL2_PREG_DEQ_CONCUR_CTRL1_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_CONCUR_CTRL2_PREG_DEQ_CONCUR_CTRL1_PREG_j Register \(Offset = 4190h + formula\) \[reset = 52242A20h\]: \[0\]](#)

11.175 DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j Register (Offset = 4194h + formula) [reset = X]

DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j is shown in [Figure 11-175](#) and described in [Table 11-527](#).

Return to [Summary Table](#).

Receive data path equalization (DEQ) and EPI control register.

Offset = 4194h + (j * 400h); where j = 0h to 1h

Table 11-526. DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4194h + formula
SERDES_16G1	0501 4194h + formula
SERDES_16G2	0502 4194h + formula
SERDES_16G3	0503 4194h + formula

Figure 11-175. DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							RX_DEQ_CLK_FORCE_PREG
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED					DEQ_PHALIGN_DONE_FORCE_PREG	CREQ_EQ_ACK_OVREN_PREG	CREQ_EQ_ACK_OVRVAL_PREG
R/W-X					R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
DEQ_CLOSED_EYE_MAINT_DISSABLE_PREG	RESERVED					EPION_TIME_PREG	
R/W-0h	R/W-X					R/W-190h	
7	6	5	4	3	2	1	0
EPION_TIME_PREG							
R/W-190h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-527. DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RX_DEQ_CLK_FORCE_PREG	R/W	0h	When asserted, rx_deq_clk remains on when ln_rxctrl_deq_fsm whenever rxdatclk is on.
23-19	RESERVED	R/W	X	
18	DEQ_PHALIGN_DONE_FORCE_PREG	R/W	0h	rxda_deq_phalign_done force. When asserted, rxda_deq_phalign_done to the ln_rxctrl_deq_fsm is forced high regardless of the state of the signal being received from rxana_deq.
17	CREQ_EQ_ACK_OVREN_PREG	R/W	0h	rxda_creq_eq_req acknowledgement override enable. When asserted, creq_eq_ack_ovrval_preg is used rather than the rxda_creq_eq_ack back from rxana_creq.

**Table 11-527. DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
16	CREQ_EQ_ACK_OVRVAL_PREG	R/W	0h	rxda_creq_eq_req acknowledgement override value. When creq_eq_ack_ovren_preg is asserted, this value is used rather than the rxda_creq_eq_ack back from rxana_creq.
15	DEQ_CLOSED EYE_MAIN_T_DISABLE_PREG	R/W	0h	Receive data path closed-eye equalization active high disable.
14-10	RESERVED	R/W	X	
9-0	EPION_TIME_PREG	R/W	190h	Receive data path equalization EPI power on settling time. The time is epion_time_preg rx_rd_clk_ln_{15:0} periods.

Table 11-528. Register Call Summary for DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_FSM_OVR_PREG__DEQ_EPIPWR_CTRL_PREG_j Register \(Offset = 4194h + formula\) \[reset = X\]: \[0\]](#)

11.176 DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j Register (Offset = 4198h + formula) [reset = X]

DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j is shown in Figure 11-176 and described in Table 11-530.

Return to [Summary Table](#).

DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG

Offset = 4198h + (j * 400h); where j = 0h to 1h

Table 11-529.
DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4198h + formula
SERDES_16G1	0501 4198h + formula
SERDES_16G2	0502 4198h + formula
SERDES_16G3	0503 4198h + formula

Figure 11-176. DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED						FAST_MAINT_TIME_PREG	
R/W-X						R/W-Ah	
23	22	21	20	19	18	17	16
FAST_MAINT_TIME_PREG				SLOW_MAINT_TIME_PREG			
R/W-Ah				R/W-Eh			
15	14	13	12	11	10	9	8
RESERVED						CONCUR_PREEVAL_MINITER_CTRL_PREG	
R/W-X						R/W-A8h	
7	6	5	4	3	2	1	0
CONCUR_PREEVAL_MINITER_CTRL_PREG							
R/W-A8h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-530. DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-21	FAST_MAINT_TIME_PREG	R/W	Ah	Receive data path closed-eye equalization fast maintenance cycle hold off time. The time is $2^{(\text{maint_time_preg}+9)} \cdot 1$ rx_rd_clk_ln_{15:0} periods.
20-16	SLOW_MAINT_TIME_PREG	R/W	Eh	Receive data path closed-eye equalization slow maintenance cycle hold off time. The time is $2^{(\text{maint_time_preg}+9)} \cdot 1$ rx_rd_clk_ln_{15:0} periods.
15-9	RESERVED	R/W	X	

Table 11-530. DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-0	CONCUR_PREEVAL_MINITER_PREG	R/W	A8h	Receive closed-eye data path equalization minimum iterations of concur and tau processes during the acquisition phase prior to the initial rx_eq_eval assertion when deq_closedeye_mode = 2'b10. Note iteration minimum is concur_miniter_preg + 1. Note a value of 9'd0 will allow infinite iterations during this state prior to the initial rx_eq_eval assertion.

Table 11-531. Register Call Summary for DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_EPIPWR_CTRL2_PREG__CONCUR_PREEVAL_MINITER_CTRL_PREG_j Register \(Offset = 4198h + formula\) \[reset = X\]: \[0\]](#)

11.177 RX_DEQ_COEF_FIFO_PREG_DEQ_FAST_MAINT_CYCLES_PREG_j Register (Offset = 419Ch + formula) [reset = X]

RX_DEQ_COEF_FIFO_PREG_DEQ_FAST_MAINT_CYCLES_PREG_j is shown in Figure 11-177 and described in Table 11-533.

Return to [Summary Table](#).

Receive data path equalization (DEQ) fast maintainance cycles register

Offset = 419Ch + (j * 400h); where j = 0h to 1h

Table 11-532.
RX_DEQ_COEF_FIFO_PREG_DEQ_FAST_MAINT_CYCLES_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 419Ch + formula
SERDES_16G1	0501 419Ch + formula
SERDES_16G2	0502 419Ch + formula
SERDES_16G3	0503 419Ch + formula

Figure 11-177. RX_DEQ_COEF_FIFO_PREG_DEQ_FAST_MAINT_CYCLES_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				RX_DEQ_COEF_FIFO_OUTDAT			
R/W-X				R-0h			
23	22	21	20	19	18	17	16
RX_DEQ_COEF_FIFO_EMPTY	RX_DEQ_COEF_FIFO_OVRD_EN_PREG	RX_DEQ_COEF_FIFO_ENQ_CLR	RX_DEQ_COEF_FIFO_ENQ_EN	RX_DEQ_COEF_FIFO_ENQ_DATA			
R-1h	R/W-0h	W-0h	W-0h	W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
DEQ_FAST_MAINT_CYCLES_PREG							
R/W-48h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-533. RX_DEQ_COEF_FIFO_PREG_DEQ_FAST_MAINT_CYCLES_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	RX_DEQ_COEF_FIFO_OUTDAT	R	0h	Receive data path equalization emulation mode FIFO output data: Current dequeued data from the emulation FIFO. bit [3] - pre cursor increment bit [2] - pre cursor decrement bit [1] - post cursor increment bit [0] - post cursor decrement Note: Not valid when rx_deq_coef_fifo_empty is asserted.
23	RX_DEQ_COEF_FIFO_EMPTY	R	1h	Receive data path equalization emulation mode FIFO empty : Indicates that the FIFO is empty. Note: This signal is valid only when rx_deq_coef_fifo_ovrd_en_preg is asserted.

Table 11-533. RX_DEQ_COEF_FIFO_PREG_DEQ_FAST_MAINT_CYCLES_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RX_DEQ_COEF_FIFO_OVRD_EN_PREG	R/W	0h	Receive data path equalization emulation mode FIFO output active high enable: Asserting this bit enables emulation data to be dequeued from the FIFO onto the rx_eq_eval interface. Note: This bit should be asserted only after emulation FIFO has been loaded. Note: When current emulation run is complete, i.e. all emulation FIFO contents have been dequeued, and the rx_deq_coef_fifo_empty is asserted, this bit should be deasserted before reloading the emulation FIFO.
21	RX_DEQ_COEF_FIFO_ENQ_CLR	W	0h	Receive data path equalization emulation mode FIFO enqueue pointer clear: Writing a 1 to this toggle bit resets the enqueue pointer to zero.
20	RX_DEQ_COEF_FIFO_ENQ_EN	W	0h	Receive data path equalization emulation mode FIFO enqueue enable : Writing a 1 to this bit will result in the rx_deq_coef_fifo_enq_data_preg field being enqueued into the next FIFO pointer position.
19-16	RX_DEQ_COEF_FIFO_ENQ_DATA	W	0h	Receive data path equalization emulation mode FIFO write data : The emulation data which will be enqueued to the FIFO if rx_deq_coef_fifo_enq_en_preg is written high. The order of the data is bit [3] - pre cursor increment bit [2] - pre cursor decrement bit [1] - post cursor increment bit [0] - post cursor decrement Note: All emulation data should be loaded into the FIFO (maximum of 8 entries) prior to asserting rx_deq_coef_fifo_ovrd_en_preg.
15-8	RESERVED	R/W	X	
7-0	DEQ_FAST_MAINT_CYCLES_PREG	R/W	48h	Receive data path equalization (deq) fast maintenance cycle count: This field determines the number of deq maintenance periods which use the fast_maint_time_preg cycle hold off and associated fast TAU iterations supported out of the deq_tau_ctrl1_fast_maint_preg register. Note: If set to a value of 0, no fast cycles are performed. Slow maintenance begins immediately after acquisition.

Table 11-534. Register Call Summary for RX_DEQ_COEF_FIFO_PREG_DEQ_FAST_MAINT_CYCLES_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_DEQ_COEF_FIFO_PREG_DEQ_FAST_MAINT_CYCLES_PREG_j Register \(Offset = 419Ch + formula\) \[reset = X\]: \[0\]](#)

11.178 DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j Register (Offset = 41A0h + formula) [reset = X]

DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j is shown in Figure 11-178 and described in Table 11-536.

Return to [Summary Table](#).

Receive data path error comparator control register.

Offset = 41A0h + (j * 400h); where j = 0h to 1h

Table 11-535. DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 41A0h + formula
SERDES_16G1	0501 41A0h + formula
SERDES_16G2	0502 41A0h + formula
SERDES_16G3	0503 41A0h + formula

Figure 11-178. DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
CMPA_OFF_O VREN_PREG	CMPA_OFFFM_OVR_PREG						
R/W-0h	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	CMPA_OFFFP_OVR_PREG						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	CMPB_VTH_PREG						
R/W-X	R/W-50h						
7	6	5	4	3	2	1	0
RESERVED	CMPA_VTH_PREG						
R/W-X	R/W-50h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-536. DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMPA_OFF_OVREN_PREG	R/W	0h	Receive data path error comparator error comparator A offset override active high enable.
30-24	CMPA_OFFFM_OVR_PREG	R/W	0h	When cmpa_off_ovren_preg is asserted high, this active high binary encoded value will override the A comparator negative polarity DAC input which introduces a negative offset. Each step is nominally 3mV.
23	RESERVED	R/W	X	
22-16	CMPA_OFFFP_OVR_PREG	R/W	0h	When cmpa_off_ovren_preg is asserted high, this active high binary encoded value will override the A comparator positive polarity DAC input which introduces a positive offset. Each step is nominally 3mV.
15	RESERVED	R/W	X	
14-8	CMPB_VTH_PREG	R/W	50h	Receive data path error comparator error comparator B target level, binary encoded. Each step is nominally 3mV.

Table 11-536. DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	
6-0	CMPA_VTH_PREG	R/W	50h	Receive data path error comparator error comparator A target level, binary encoded. Each step is nominally 3mV.

Table 11-537. Register Call Summary for DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ERRCMPA_OVR_PREG__DEQ_ERRCMP_CTRL_PREG_j Register \(Offset = 41A0h + formula\) \[reset = X\]: \[0\]](#)

11.179 CMP_AVR_TIMER_PREG_DEQ_ERRCMPB_OVR_PREG_j Register (Offset = 41A4h + formula) [reset = X]

CMP_AVR_TIMER_PREG_DEQ_ERRCMPB_OVR_PREG_j is shown in Figure 11-179 and described in Table 11-539.

Return to [Summary Table](#).

Receive data path error comparator B override register.

Offset = 41A4h + (j * 400h); where j = 0h to 1h

Table 11-538. CMP_AVR_TIMER_PREG_DEQ_ERRCMPB_OVR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 41A4h + formula
SERDES_16G1	0501 41A4h + formula
SERDES_16G2	0502 41A4h + formula
SERDES_16G3	0503 41A4h + formula

Figure 11-179. CMP_AVR_TIMER_PREG_DEQ_ERRCMPB_OVR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
CMP_AVR_TIMER_PREG							
R/W-F9h							
15	14	13	12	11	10	9	8
CMPB_OFF_O VREN_PREG	CMPB_OFFFM_OVR_PREG						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	CMPB_OFFFP_OVR_PREG						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-539. CMP_AVR_TIMER_PREG_DEQ_ERRCMPB_OVR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	CMP_AVR_TIMER_PREG	R/W	F9h	Receive data path error comparators A and B average timer value. Number of rx_rd_clk clock periods to average the error comparator offset data over during offset calibration.
15	CMPB_OFF_OVREN_PREG	R/W	0h	Receive data path error comparator error comparator B offset override active high enable.
14-8	CMPB_OFFFM_OVR_PREG	R/W	0h	When cmpa_off_ovren_preg is asserted high, this active high binary encoded value will override the B comparator negative polarity DAC input which introduces a negative offset. Each step is nominally 3mV.
7	RESERVED	R/W	X	

**Table 11-539. CMP_AVR_TIMER_PREG__DEQ_ERRCMPB_OVR_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
6-0	CMPB_OFFFP_OVR_PREG	R/W	0h	When cmpa_off_ovren_preg is asserted high, this active high binary encoded value will override the B comparator positive polarity DAC input which introduces a positive offset. Each step is nominally 3mV.

Table 11-540. Register Call Summary for CMP_AVR_TIMER_PREG__DEQ_ERRCMPB_OVR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CMP_AVR_TIMER_PREG__DEQ_ERRCMPB_OVR_PREG_j Register \(Offset = 41A4h + formula\) \[reset = X\]: \[0\]](#)

11.180 DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j Register (Offset = 41B0h + formula) [reset = X]

DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j is shown in Figure 11-180 and described in Table 11-542.

Return to [Summary Table](#).

Receive data path offset control register.

Offset = 41B0h + (j * 400h); where j = 0h to 1h

Table 11-541.

DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 41B0h + formula
SERDES_16G1	0501 41B0h + formula
SERDES_16G2	0502 41B0h + formula
SERDES_16G3	0503 41B0h + formula

Figure 11-180. DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							DATOFF_OVR_EN_PREG
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
DATOFF_OVR_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				DATOFF_THRESH_OE_PREG			
R/W-X				R/W-2h			
7	6	5	4	3	2	1	0
DATOFF_THRESH_MNT_PREG				DATOFF_THRESH_ACQ_PREG			
R/W-Ah				R/W-7h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-542. DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DATOFF_OVREN_PREG	R/W	0h	Receive data path offset active high override enable.
23-16	DATOFF_OVR_PREG	R/W	0h	When datoff_ovren_preg is asserted high, this value overrides the data offset. Value is { sign bit, 7-bit magnitude }
15-12	RESERVED	R/W	X	
11-8	DATOFF_THRESH_OE_PREG	R/W	2h	Receive data path offset accumulator threshold for open-eye standards. Threshold = $2^{\text{datoff_thresh_oe_preg}}$
7-4	DATOFF_THRESH_MNT_PREG	R/W	Ah	Receive data path offset accumulator threshold for maintenance. Threshold = $2^{\text{datoff_thresh_oe_preg}}$
3-0	DATOFF_THRESH_ACQ_PREG	R/W	7h	Receive data path offset accumulator threshold for acquisition. Threshold = $2^{\text{datoff_thresh_oe_preg}}$

**Table 11-543. Register Call Summary for
DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_OFFSET_OVR_CTRL_PREG__DEQ_OFFSET_CTRL_PREG_j Register \(Offset = 41B0h + formula\) \[reset = X\]: \[0\]](#)

11.181 DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j Register (Offset = 41C0h + formula) [reset = X]

DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j is shown in Figure 11-181 and described in Table 11-545.

Return to [Summary Table](#).

Receive data path gain and attenuation control register.

Offset = 41C0h + (j * 400h); where j = 0h to 1h

Table 11-544. DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 41C0h + formula
SERDES_16G1	0501 41C0h + formula
SERDES_16G2	0502 41C0h + formula
SERDES_16G3	0503 41C0h + formula

Figure 11-181. DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
VGA_VGA2TUNE_N_MODE3_P REG	VGA_VGA2TUNE_N_MODE2_P REG	VGA_VGA2TUNE_N_MODE1_P REG	VGA_VGA2TUNE_N_MODE0_P REG				
R/W-2h	R/W-2h	R/W-1h	R/W-0h				
23	22	21	20	19	18	17	16
VGA_VGA1TUNE_N_MODE3_P REG	VGA_VGA1TUNE_N_MODE2_P REG	VGA_VGA1TUNE_N_MODE1_P REG	VGA_VGA1TUNE_N_MODE0_P REG				
R/W-2h	R/W-2h	R/W-1h	R/W-0h				
15	14	13	12	11	10	9	8
RESERVED		DATGAIN_OVR EN_PREG	DATGAIN_THRESH_OE_PREG				
R/W-X		R/W-0h	R/W-2h				
7	6	5	4	3	2	1	0
DATGAIN_THRESH_MNT_PREG		DATGAIN_THRESH_ACQ_PREG					
R/W-Ah		R/W-7h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-545. DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	VGA_VGA2TUNE_N_MODE3_PREG	R/W	2h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. Zero frequency 2'b11 Reserved 2'b10 Highest 2'b01 Medium 2'b00 Lowest
29-28	VGA_VGA2TUNE_N_MODE2_PREG	R/W	2h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. Zero frequency 2'b11 Reserved 2'b10 Highest 2'b01 Medium 2'b00 Lowest

**Table 11-545. DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
27-26	VGA_VGA2TUNE_N_MO DE1_PREG	R/W	1h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Zero frequency 2'b11 Reserved 2'b10 Highest 2'b01 Medium 2'b00 Lowest
25-24	VGA_VGA2TUNE_N_MO DE0_PREG	R/W	0h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. Zero frequency 2'b11 Reserved 2'b10 Highest 2'b01 Medium 2'b00 Lowest
23-22	VGA_VGA1TUNE_N_MO DE3_PREG	R/W	2h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. Zero frequency 2'b11 Reserved 2'b10 Highest 2'b01 Medium 2'b00 Lowest
21-20	VGA_VGA1TUNE_N_MO DE2_PREG	R/W	2h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010. Zero frequency 2'b11 Reserved 2'b10 Highest 2'b01 Medium 2'b00 Lowest
19-18	VGA_VGA1TUNE_N_MO DE1_PREG	R/W	1h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001. Zero frequency 2'b11 Reserved 2'b10 Highest 2'b01 Medium 2'b00 Lowest
17-16	VGA_VGA1TUNE_N_MO DE0_PREG	R/W	0h	This value sets the Lane Standards Decoder value when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000. Zero frequency 2'b11 Reserved 2'b10 Highest 2'b01 Medium 2'b00 Lowest
15-13	RESERVED	R/W	X	
12	DATGAIN_OVREN_PREG	R/W	0h	Receive data path gain and attenuation look-up table pointer active high override enable. When asserted high, the pointer is forced to entry 0.
11-8	DATGAIN_THRESH_OE_PREG	R/W	2h	Receive data path gain accumulator threshold for open-eye standards. Threshold = 2 ^{datgain_thresh_oe_preg}

**Table 11-545. DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
7-4	DATGAIN_THRESH_MNT_PREG	R/W	Ah	Receive data path gain accumulator threshold for maintenance. Threshold = $2^{\text{datgain_thresh_mnt_preg}}$
3-0	DATGAIN_THRESH_ACQ_PREG	R/W	7h	Receive data path gain accumulator threshold for acquisition. Threshold = $2^{\text{datgain_thresh_acq_preg}}$

Table 11-546. Register Call Summary for DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_VGATUNE_CTRL_PREG__DEQ_GAIN_CTRL_PREG_j Register \(Offset = 41C0h + formula\) \[reset = X\]: \[0\]](#)

11.182 DEQ_GLUT1__DEQ_GLUT0_j Register (Offset = 41D0h + formula) [reset = X]

DEQ_GLUT1__DEQ_GLUT0_j is shown in Figure 11-182 and described in Table 11-548.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 0 register.

Offset = 41D0h + (j * 400h); where j = 0h to 1h

**Table 11-547. DEQ_GLUT1__DEQ_GLUT0_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41D0h + formula
SERDES_16G1	0501 41D0h + formula
SERDES_16G2	0502 41D0h + formula
SERDES_16G3	0503 41D0h + formula

Figure 11-182. DEQ_GLUT1__DEQ_GLUT0_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_1_PREG			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_1_PREG		DATGAIN_VGA1GAIN_1_PREG					
R/W-0h		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_0_PREG			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_0_PREG		DATGAIN_VGA1GAIN_0_PREG					
R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-548. DEQ_GLUT1__DEQ_GLUT0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_1_PREG	R/W	0h	Receive data path equalization LUT VGA2 peaking control, entry 1 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_1_PREG	R/W	0h	Receive data path equalization LUT VGA1 peaking control, entry 1 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-548. DEQ_GLUT1__DEQ_GLUT0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_0_PREG	R/W	0h	Receive data path equalization LUT VGA2 peaking control, entry 0 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_0_PREG	R/W	0h	Receive data path equalization LUT VGA1 peaking control, entry 0 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-549. Register Call Summary for DEQ_GLUT1__DEQ_GLUT0_j

16-G SerDes Registers
<ul style="list-style-type: none"> • 2-L SerDes Registers: [0] [1] • DEQ_GLUT1__DEQ_GLUT0_j Register (Offset = 41D0h + formula) [reset = X]: [0]

11.183 DEQ_GLUT3__DEQ_GLUT2_j Register (Offset = 41D4h + formula) [reset = X]

DEQ_GLUT3__DEQ_GLUT2_j is shown in Figure 11-183 and described in Table 11-551.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 2 register.

Offset = 41D4h + (j * 400h); where j = 0h to 1h

**Table 11-550. DEQ_GLUT3__DEQ_GLUT2_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41D4h + formula
SERDES_16G1	0501 41D4h + formula
SERDES_16G2	0502 41D4h + formula
SERDES_16G3	0503 41D4h + formula

Figure 11-183. DEQ_GLUT3__DEQ_GLUT2_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_3_PREG			
R/W-X				R/W-2h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_3_PREG		DATGAIN_VGA1GAIN_3_PREG					
R/W-2h		R/W-2h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_2_PREG			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_2_PREG		DATGAIN_VGA1GAIN_2_PREG					
R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-551. DEQ_GLUT3__DEQ_GLUT2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_3_PREG	R/W	2h	Receive data path equalization LUT VGA2 peaking control, entry 3 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_3_PREG	R/W	2h	Receive data path equalization LUT VGA1 peaking control, entry 3 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-551. DEQ_GLUT3__DEQ_GLUT2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_2_PREG	R/W	0h	Receive data path equalization LUT VGA2 peaking control, entry 2 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_2_PREG	R/W	0h	Receive data path equalization LUT VGA1 peaking control, entry 2 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-552. Register Call Summary for DEQ_GLUT3__DEQ_GLUT2_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT3__DEQ_GLUT2_j Register \(Offset = 41D4h + formula\) \[reset = X\]: \[0\]](#)

11.184 DEQ_GLUT5__DEQ_GLUT4_j Register (Offset = 41D8h + formula) [reset = X]

DEQ_GLUT5__DEQ_GLUT4_j is shown in Figure 11-184 and described in Table 11-554.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 4 register.

Offset = 41D8h + (j * 400h); where j = 0h to 1h

**Table 11-553. DEQ_GLUT5__DEQ_GLUT4_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41D8h + formula
SERDES_16G1	0501 41D8h + formula
SERDES_16G2	0502 41D8h + formula
SERDES_16G3	0503 41D8h + formula

Figure 11-184. DEQ_GLUT5__DEQ_GLUT4_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_5_PREG			
R/W-X				R/W-6h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_5_PREG		DATGAIN_VGA1GAIN_5_PREG					
R/W-6h		R/W-6h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_4_PREG			
R/W-X				R/W-2h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_4_PREG		DATGAIN_VGA1GAIN_4_PREG					
R/W-2h		R/W-2h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-554. DEQ_GLUT5__DEQ_GLUT4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_5_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 5 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_5_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 5 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-554. DEQ_GLUT5__DEQ_GLUT4_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_4_PREG	R/W	2h	Receive data path equalization LUT VGA2 peaking control, entry 4 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_4_PREG	R/W	2h	Receive data path equalization LUT VGA1 peaking control, entry 4 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-555. Register Call Summary for DEQ_GLUT5__DEQ_GLUT4_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT5__DEQ_GLUT4_j Register \(Offset = 41D8h + formula\) \[reset = X\]: \[0\]](#)

11.185 DEQ_Glut7__DEQ_Glut6_j Register (Offset = 41DCh + formula) [reset = X]

DEQ_Glut7__DEQ_Glut6_j is shown in Figure 11-185 and described in Table 11-557.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 6 register.

Offset = 41DCh + (j * 400h); where j = 0h to 1h

**Table 11-556. DEQ_Glut7__DEQ_Glut6_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41DCh + formula
SERDES_16G1	0501 41DCh + formula
SERDES_16G2	0502 41DCh + formula
SERDES_16G3	0503 41DCh + formula

Figure 11-185. DEQ_Glut7__DEQ_Glut6_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_7_PREG			
R/W-X				R/W-6h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_7_PREG		DATGAIN_VGA1GAIN_7_PREG					
R/W-6h		R/W-6h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_6_PREG			
R/W-X				R/W-6h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_6_PREG		DATGAIN_VGA1GAIN_6_PREG					
R/W-6h		R/W-6h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-557. DEQ_Glut7__DEQ_Glut6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_7_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 7 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_7_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 7 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-557. DEQ_GLUT7__DEQ_GLUT6_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_6_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 6 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_6_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 6 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-558. Register Call Summary for DEQ_GLUT7__DEQ_GLUT6_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT7__DEQ_GLUT6_j Register \(Offset = 41DCh + formula\) \[reset = X\]: \[0\]](#)

11.186 DEQ_GLUT9__DEQ_GLUT8_j Register (Offset = 41E0h + formula) [reset = X]

DEQ_GLUT9__DEQ_GLUT8_j is shown in Figure 11-186 and described in Table 11-560.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 8 register.

Offset = 41E0h + (j * 400h); where j = 0h to 1h

**Table 11-559. DEQ_GLUT9__DEQ_GLUT8_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41E0h + formula
SERDES_16G1	0501 41E0h + formula
SERDES_16G2	0502 41E0h + formula
SERDES_16G3	0503 41E0h + formula

Figure 11-186. DEQ_GLUT9__DEQ_GLUT8_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_9_PREG			
R/W-X				R/W-6h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_9_PREG		DATGAIN_VGA1GAIN_9_PREG					
R/W-6h		R/W-6h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_8_PREG			
R/W-X				R/W-6h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_8_PREG		DATGAIN_VGA1GAIN_8_PREG					
R/W-6h		R/W-6h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-560. DEQ_GLUT9__DEQ_GLUT8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_9_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 9 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_9_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 9 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-560. DEQ_GLUT9__DEQ_GLUT8_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_8_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 8 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_8_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 8 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-561. Register Call Summary for DEQ_GLUT9__DEQ_GLUT8_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT9__DEQ_GLUT8_j Register \(Offset = 41E0h + formula\) \[reset = X\]: \[0\]](#)

11.187 DEQ_GLUT11__DEQ_GLUT10_j Register (Offset = 41E4h + formula) [reset = X]

DEQ_GLUT11__DEQ_GLUT10_j is shown in Figure 11-187 and described in Table 11-563.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 10 register.

Offset = 41E4h + (j * 400h); where j = 0h to 1h

**Table 11-562. DEQ_GLUT11__DEQ_GLUT10_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41E4h + formula
SERDES_16G1	0501 41E4h + formula
SERDES_16G2	0502 41E4h + formula
SERDES_16G3	0503 41E4h + formula

Figure 11-187. DEQ_GLUT11__DEQ_GLUT10_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_11_PREG			
R/W-X				R/W-6h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_11_PREG		DATGAIN_VGA1GAIN_11_PREG					
R/W-6h		R/W-6h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_10_PREG			
R/W-X				R/W-6h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_10_PREG		DATGAIN_VGA1GAIN_10_PREG					
R/W-6h		R/W-6h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-563. DEQ_GLUT11__DEQ_GLUT10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_11_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 11 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_11_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 11 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-563. DEQ_GLUT11__DEQ_GLUT10_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_10_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 10 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_10_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 10 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-564. Register Call Summary for DEQ_GLUT11__DEQ_GLUT10_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT11__DEQ_GLUT10_j Register \(Offset = 41E4h + formula\) \[reset = X\]: \[0\]](#)

11.188 DEQ_GLUT13__DEQ_GLUT12_j Register (Offset = 41E8h + formula) [reset = X]

DEQ_GLUT13__DEQ_GLUT12_j is shown in Figure 11-188 and described in Table 11-566.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 12 register.

Offset = 41E8h + (j * 400h); where j = 0h to 1h

**Table 11-565. DEQ_GLUT13__DEQ_GLUT12_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41E8h + formula
SERDES_16G1	0501 41E8h + formula
SERDES_16G2	0502 41E8h + formula
SERDES_16G3	0503 41E8h + formula

Figure 11-188. DEQ_GLUT13__DEQ_GLUT12_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_13_PREG			
R/W-X				R/W-6h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_13_PREG		DATGAIN_VGA1GAIN_13_PREG					
R/W-6h		R/W-6h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_12_PREG			
R/W-X				R/W-6h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_12_PREG		DATGAIN_VGA1GAIN_12_PREG					
R/W-6h		R/W-6h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-566. DEQ_GLUT13__DEQ_GLUT12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_13_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 13 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_13_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 13 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-566. DEQ_GLUT13__DEQ_GLUT12_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_12_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 12 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_12_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 12 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-567. Register Call Summary for DEQ_GLUT13__DEQ_GLUT12_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT13__DEQ_GLUT12_j Register \(Offset = 41E8h + formula\) \[reset = X\]: \[0\]](#)

11.189 DEQ_GLUT15__DEQ_GLUT14_j Register (Offset = 41ECh + formula) [reset = X]

DEQ_GLUT15__DEQ_GLUT14_j is shown in Figure 11-189 and described in Table 11-569.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 14 register.

Offset = 41ECh + (j * 400h); where j = 0h to 1h

**Table 11-568. DEQ_GLUT15__DEQ_GLUT14_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41ECh + formula
SERDES_16G1	0501 41ECh + formula
SERDES_16G2	0502 41ECh + formula
SERDES_16G3	0503 41ECh + formula

Figure 11-189. DEQ_GLUT15__DEQ_GLUT14_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_15_PREG			
R/W-X				R/W-6h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_15_PREG		DATGAIN_VGA1GAIN_15_PREG					
R/W-6h		R/W-6h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_14_PREG			
R/W-X				R/W-6h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_14_PREG		DATGAIN_VGA1GAIN_14_PREG					
R/W-6h		R/W-6h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-569. DEQ_GLUT15__DEQ_GLUT14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_15_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 15 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_15_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 15 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-569. DEQ_GLUT15__DEQ_GLUT14_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_14_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 14 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_14_PREG	R/W	6h	Receive data path equalization LUT VGA1 peaking control, entry 14 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-570. Register Call Summary for DEQ_GLUT15__DEQ_GLUT14_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT15__DEQ_GLUT14_j Register \(Offset = 41ECh + formula\) \[reset = X\]: \[0\]](#)

11.190 DEQ_GLUT17__DEQ_GLUT16_j Register (Offset = 41F0h + formula) [reset = X]

DEQ_GLUT17__DEQ_GLUT16_j is shown in Figure 11-190 and described in Table 11-572.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 16 register.

Offset = 41F0h + (j * 400h); where j = 0h to 1h

**Table 11-571. DEQ_GLUT17__DEQ_GLUT16_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41F0h + formula
SERDES_16G1	0501 41F0h + formula
SERDES_16G2	0502 41F0h + formula
SERDES_16G3	0503 41F0h + formula

Figure 11-190. DEQ_GLUT17__DEQ_GLUT16_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_17_PREG			
R/W-X				R/W-8h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_17_PREG		DATGAIN_VGA1GAIN_17_PREG					
R/W-8h		R/W-8h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_16_PREG			
R/W-X				R/W-6h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_16_PREG		DATGAIN_VGA1GAIN_16_PREG					
R/W-6h		R/W-8h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-572. DEQ_GLUT17__DEQ_GLUT16_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_17_PREG	R/W	8h	Receive data path equalization LUT VGA2 peaking control, entry 17 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_17_PREG	R/W	8h	Receive data path equalization LUT VGA1 peaking control, entry 17 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-572. DEQ_GLUT17__DEQ_GLUT16_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_16_PREG	R/W	6h	Receive data path equalization LUT VGA2 peaking control, entry 16 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_16_PREG	R/W	8h	Receive data path equalization LUT VGA1 peaking control, entry 16 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-573. Register Call Summary for DEQ_GLUT17__DEQ_GLUT16_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT17__DEQ_GLUT16_j Register \(Offset = 41F0h + formula\) \[reset = X\]: \[0\]](#)

11.191 DEQ_GLUT19__DEQ_GLUT18_j Register (Offset = 41F4h + formula) [reset = X]

DEQ_GLUT19__DEQ_GLUT18_j is shown in Figure 11-191 and described in Table 11-575.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 18 register.

Offset = 41F4h + (j * 400h); where j = 0h to 1h

**Table 11-574. DEQ_GLUT19__DEQ_GLUT18_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41F4h + formula
SERDES_16G1	0501 41F4h + formula
SERDES_16G2	0502 41F4h + formula
SERDES_16G3	0503 41F4h + formula

Figure 11-191. DEQ_GLUT19__DEQ_GLUT18_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_19_PREG			
R/W-X				R/W-Ah			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_19_PREG		DATGAIN_VGA1GAIN_19_PREG					
R/W-Ah				R/W-Ah			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_18_PREG			
R/W-X				R/W-8h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_18_PREG		DATGAIN_VGA1GAIN_18_PREG					
R/W-8h				R/W-Ah			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-575. DEQ_GLUT19__DEQ_GLUT18_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_19_PREG	R/W	Ah	Receive data path equalization LUT VGA2 peaking control, entry 19 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_19_PREG	R/W	Ah	Receive data path equalization LUT VGA1 peaking control, entry 19 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-575. DEQ_GLUT19__DEQ_GLUT18_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_18_PREG	R/W	8h	Receive data path equalization LUT VGA2 peaking control, entry 18 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_18_PREG	R/W	Ah	Receive data path equalization LUT VGA1 peaking control, entry 18 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-576. Register Call Summary for DEQ_GLUT19__DEQ_GLUT18_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT19__DEQ_GLUT18_j Register \(Offset = 41F4h + formula\) \[reset = X\]: \[0\]](#)

11.192 DEQ_GLUT21__DEQ_GLUT20_j Register (Offset = 41F8h + formula) [reset = X]

DEQ_GLUT21__DEQ_GLUT20_j is shown in Figure 11-192 and described in Table 11-578.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 20 register.

Offset = 41F8h + (j * 400h); where j = 0h to 1h

**Table 11-577. DEQ_GLUT21__DEQ_GLUT20_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41F8h + formula
SERDES_16G1	0501 41F8h + formula
SERDES_16G2	0502 41F8h + formula
SERDES_16G3	0503 41F8h + formula

Figure 11-192. DEQ_GLUT21__DEQ_GLUT20_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_21_PREG			
R/W-X				R/W-Ch			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_21_PREG		DATGAIN_VGA1GAIN_21_PREG					
R/W-Ch				R/W-Ch			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_20_PREG			
R/W-X				R/W-Ah			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_20_PREG		DATGAIN_VGA1GAIN_20_PREG					
R/W-Ah				R/W-Ch			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-578. DEQ_GLUT21__DEQ_GLUT20_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_21_PREG	R/W	Ch	Receive data path equalization LUT VGA2 peaking control, entry 21 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_21_PREG	R/W	Ch	Receive data path equalization LUT VGA1 peaking control, entry 21 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-578. DEQ_GLUT21__DEQ_GLUT20_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_20_PREG	R/W	Ah	Receive data path equalization LUT VGA2 peaking control, entry 20 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_20_PREG	R/W	Ch	Receive data path equalization LUT VGA1 peaking control, entry 20 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-579. Register Call Summary for DEQ_GLUT21__DEQ_GLUT20_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT21__DEQ_GLUT20_j Register \(Offset = 41F8h + formula\) \[reset = X\]: \[0\]](#)

11.193 DEQ_GLUT23__DEQ_GLUT22_j Register (Offset = 41FCh + formula) [reset = X]

DEQ_GLUT23__DEQ_GLUT22_j is shown in Figure 11-193 and described in Table 11-581.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 22 register.

Offset = 41FCh + (j * 400h); where j = 0h to 1h

**Table 11-580. DEQ_GLUT23__DEQ_GLUT22_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 41FCh + formula
SERDES_16G1	0501 41FCh + formula
SERDES_16G2	0502 41FCh + formula
SERDES_16G3	0503 41FCh + formula

Figure 11-193. DEQ_GLUT23__DEQ_GLUT22_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_23_PREG			
R/W-X				R/W-Eh			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_23_PREG		DATGAIN_VGA1GAIN_23_PREG					
R/W-Eh				R/W-Eh			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_22_PREG			
R/W-X				R/W-Ch			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_22_PREG		DATGAIN_VGA1GAIN_22_PREG					
R/W-Ch				R/W-Eh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-581. DEQ_GLUT23__DEQ_GLUT22_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_23_PREG	R/W	Eh	Receive data path equalization LUT VGA2 peaking control, entry 23 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_23_PREG	R/W	Eh	Receive data path equalization LUT VGA1 peaking control, entry 23 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-581. DEQ_GLUT23__DEQ_GLUT22_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_22_PREG	R/W	Ch	Receive data path equalization LUT VGA2 peaking control, entry 22 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_22_PREG	R/W	Eh	Receive data path equalization LUT VGA1 peaking control, entry 22 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-582. Register Call Summary for DEQ_GLUT23__DEQ_GLUT22_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT23__DEQ_GLUT22_j Register \(Offset = 41FCh + formula\) \[reset = X\]: \[0\]](#)

11.194 DEQ_GLUT25__DEQ_GLUT24_j Register (Offset = 4200h + formula) [reset = X]

DEQ_GLUT25__DEQ_GLUT24_j is shown in Figure 11-194 and described in Table 11-584.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 24 register.

Offset = 4200h + (j * 400h); where j = 0h to 1h

**Table 11-583. DEQ_GLUT25__DEQ_GLUT24_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4200h + formula
SERDES_16G1	0501 4200h + formula
SERDES_16G2	0502 4200h + formula
SERDES_16G3	0503 4200h + formula

Figure 11-194. DEQ_GLUT25__DEQ_GLUT24_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_25_PREG			
R/W-X				R/W-11h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_25_PREG		DATGAIN_VGA1GAIN_25_PREG					
R/W-11h				R/W-11h			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_24_PREG			
R/W-X				R/W-Eh			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_24_PREG		DATGAIN_VGA1GAIN_24_PREG					
R/W-Eh				R/W-11h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-584. DEQ_GLUT25__DEQ_GLUT24_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_25_PREG	R/W	11h	Receive data path equalization LUT VGA2 peaking control, entry 25 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_25_PREG	R/W	11h	Receive data path equalization LUT VGA1 peaking control, entry 25 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-584. DEQ_GLUT25__DEQ_GLUT24_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_24_PREG	R/W	Eh	Receive data path equalization LUT VGA2 peaking control, entry 24 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_24_PREG	R/W	11h	Receive data path equalization LUT VGA1 peaking control, entry 24 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-585. Register Call Summary for DEQ_GLUT25__DEQ_GLUT24_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT25__DEQ_GLUT24_j Register \(Offset = 4200h + formula\) \[reset = X\]: \[0\]](#)

11.195 DEQ_GLUT27__DEQ_GLUT26_j Register (Offset = 4204h + formula) [reset = X]

DEQ_GLUT27__DEQ_GLUT26_j is shown in Figure 11-195 and described in Table 11-587.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 26 register.

Offset = 4204h + (j * 400h); where j = 0h to 1h

**Table 11-586. DEQ_GLUT27__DEQ_GLUT26_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4204h + formula
SERDES_16G1	0501 4204h + formula
SERDES_16G2	0502 4204h + formula
SERDES_16G3	0503 4204h + formula

Figure 11-195. DEQ_GLUT27__DEQ_GLUT26_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_27_PREG			
R/W-X				R/W-14h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_27_PREG		DATGAIN_VGA1GAIN_27_PREG					
R/W-14h				R/W-14h			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_26_PREG			
R/W-X				R/W-11h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_26_PREG		DATGAIN_VGA1GAIN_26_PREG					
R/W-11h				R/W-14h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-587. DEQ_GLUT27__DEQ_GLUT26_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_27_PREG	R/W	14h	Receive data path equalization LUT VGA2 peaking control, entry 27 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_27_PREG	R/W	14h	Receive data path equalization LUT VGA1 peaking control, entry 27 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-587. DEQ_GLUT27__DEQ_GLUT26_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_26_PREG	R/W	11h	Receive data path equalization LUT VGA2 peaking control, entry 26 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_26_PREG	R/W	14h	Receive data path equalization LUT VGA1 peaking control, entry 26 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-588. Register Call Summary for DEQ_GLUT27__DEQ_GLUT26_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT27__DEQ_GLUT26_j Register \(Offset = 4204h + formula\) \[reset = X\]: \[0\]](#)

11.196 DEQ_GLUT29__DEQ_GLUT28_j Register (Offset = 4208h + formula) [reset = X]

DEQ_GLUT29__DEQ_GLUT28_j is shown in Figure 11-196 and described in Table 11-590.

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 28 register.

Offset = 4208h + (j * 400h); where j = 0h to 1h

**Table 11-589. DEQ_GLUT29__DEQ_GLUT28_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4208h + formula
SERDES_16G1	0501 4208h + formula
SERDES_16G2	0502 4208h + formula
SERDES_16G3	0503 4208h + formula

Figure 11-196. DEQ_GLUT29__DEQ_GLUT28_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_29_PREG			
R/W-X				R/W-18h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_29_PREG		DATGAIN_VGA1GAIN_29_PREG					
R/W-18h				R/W-18h			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_28_PREG			
R/W-X				R/W-14h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_28_PREG		DATGAIN_VGA1GAIN_28_PREG					
R/W-14h				R/W-18h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-590. DEQ_GLUT29__DEQ_GLUT28_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_29_PREG	R/W	18h	Receive data path equalization LUT VGA2 peaking control, entry 29 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_29_PREG	R/W	18h	Receive data path equalization LUT VGA1 peaking control, entry 29 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-590. DEQ_GLUT29__DEQ_GLUT28_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_28_PREG	R/W	14h	Receive data path equalization LUT VGA2 peaking control, entry 28 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_28_PREG	R/W	18h	Receive data path equalization LUT VGA1 peaking control, entry 28 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-591. Register Call Summary for DEQ_GLUT29__DEQ_GLUT28_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT29__DEQ_GLUT28_j Register \(Offset = 4208h + formula\) \[reset = X\]: \[0\]](#)

11.197 DEQ_GLUT31__DEQ_GLUT30_j Register (Offset = 420Ch + formula) [reset = X]

DEQ_GLUT31__DEQ_GLUT30_j is shown in [Figure 11-197](#) and described in [Table 11-593](#).

Return to [Summary Table](#).

Receive data path equalization LUT gain, entry 30 register.

Offset = 420Ch + (j * 400h); where j = 0h to 1h

**Table 11-592. DEQ_GLUT31__DEQ_GLUT30_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 420Ch + formula
SERDES_16G1	0501 420Ch + formula
SERDES_16G2	0502 420Ch + formula
SERDES_16G3	0503 420Ch + formula

Figure 11-197. DEQ_GLUT31__DEQ_GLUT30_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2GAIN_31_PREG			
R/W-X				R/W-1Dh			
23	22	21	20	19	18	17	16
DATGAIN_VGA2GAIN_31_PREG		DATGAIN_VGA1GAIN_31_PREG					
R/W-1Dh				R/W-1Dh			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2GAIN_30_PREG			
R/W-X				R/W-18h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2GAIN_30_PREG		DATGAIN_VGA1GAIN_30_PREG					
R/W-18h				R/W-1Dh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-593. DEQ_GLUT31__DEQ_GLUT30_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2GAIN_31_PREG	R/W	1Dh	Receive data path equalization LUT VGA2 peaking control, entry 31 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1GAIN_31_PREG	R/W	1Dh	Receive data path equalization LUT VGA1 peaking control, entry 31 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
15-12	RESERVED	R/W	X	

Table 11-593. DEQ_GLUT31__DEQ_GLUT30_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-6	DATGAIN_VGA2GAIN_30_PREG	R/W	18h	Receive data path equalization LUT VGA2 peaking control, entry 30 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1GAIN_30_PREG	R/W	1Dh	Receive data path equalization LUT VGA1 peaking control, entry 30 Gain 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-594. Register Call Summary for DEQ_GLUT31__DEQ_GLUT30_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_GLUT31__DEQ_GLUT30_j Register \(Offset = 420Ch + formula\) \[reset = X\]: \[0\]](#)

11.198 DEQ_ALUT1__DEQ_ALUT0_j Register (Offset = 4210h + formula) [reset = X]

DEQ_ALUT1__DEQ_ALUT0_j is shown in [Figure 11-198](#) and described in [Table 11-596](#).

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 0 register.

Offset = 4210h + (j * 400h); where j = 0h to 1h

**Table 11-595. DEQ_ALUT1__DEQ_ALUT0_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4210h + formula
SERDES_16G1	0501 4210h + formula
SERDES_16G2	0502 4210h + formula
SERDES_16G3	0503 4210h + formula

Figure 11-198. DEQ_ALUT1__DEQ_ALUT0_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_1_PREG			
R/W-X				R/W-24h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_1_PREG		DATGAIN_VGA1ATTEN_1_PREG					
R/W-24h				R/W-24h			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_0_PREG			
R/W-X				R/W-26h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_0_PREG		DATGAIN_VGA1ATTEN_0_PREG					
R/W-26h				R/W-26h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-596. DEQ_ALUT1__DEQ_ALUT0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_1_PREG	R/W	24h	Receive data path equalization LUT VGA2 attenuation control, entry 1 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_1_PREG	R/W	24h	Receive data path equalization LUT VGA1 attenuation control, entry 1 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-596. DEQ_ALUT1__DEQ_ALUT0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_0_PREG	R/W	26h	Receive data path equalization LUT VGA2 attenuation control, entry 0 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_0_PREG	R/W	26h	Receive data path equalization LUT VGA1 attenuation control, entry 0 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-597. Register Call Summary for DEQ_ALUT1__DEQ_ALUT0_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT1__DEQ_ALUT0_j Register \(Offset = 4210h + formula\) \[reset = X\]: \[0\]](#)

11.199 DEQ_ALUT3__DEQ_ALUT2_j Register (Offset = 4214h + formula) [reset = X]

DEQ_ALUT3__DEQ_ALUT2_j is shown in Figure 11-199 and described in Table 11-599.

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 2 register.

Offset = 4214h + (j * 400h); where j = 0h to 1h

**Table 11-598. DEQ_ALUT3__DEQ_ALUT2_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4214h + formula
SERDES_16G1	0501 4214h + formula
SERDES_16G2	0502 4214h + formula
SERDES_16G3	0503 4214h + formula

Figure 11-199. DEQ_ALUT3__DEQ_ALUT2_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_3_PREG			
R/W-X				R/W-22h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_3_PREG		DATGAIN_VGA1ATTEN_3_PREG					
R/W-22h				R/W-22h			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_2_PREG			
R/W-X				R/W-23h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_2_PREG		DATGAIN_VGA1ATTEN_2_PREG					
R/W-23h				R/W-23h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-599. DEQ_ALUT3__DEQ_ALUT2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_3_PREG	R/W	22h	Receive data path equalization LUT VGA2 attenuation control, entry 3 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_3_PREG	R/W	22h	Receive data path equalization LUT VGA1 attenuation control, entry 3 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-599. DEQ_ALUT3__DEQ_ALUT2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_2_PREG	R/W	23h	Receive data path equalization LUT VGA2 attenuation control, entry 2 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_2_PREG	R/W	23h	Receive data path equalization LUT VGA1 attenuation control, entry 2 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-600. Register Call Summary for DEQ_ALUT3__DEQ_ALUT2_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT3__DEQ_ALUT2_j Register \(Offset = 4214h + formula\) \[reset = X\]: \[0\]](#)

11.200 DEQ_ALUT5__DEQ_ALUT4_j Register (Offset = 4218h + formula) [reset = X]

DEQ_ALUT5__DEQ_ALUT4_j is shown in Figure 11-200 and described in Table 11-602.

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 4 register.

Offset = 4218h + (j * 400h); where j = 0h to 1h

**Table 11-601. DEQ_ALUT5__DEQ_ALUT4_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4218h + formula
SERDES_16G1	0501 4218h + formula
SERDES_16G2	0502 4218h + formula
SERDES_16G3	0503 4218h + formula

Figure 11-200. DEQ_ALUT5__DEQ_ALUT4_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_5_PREG			
R/W-X				R/W-1Fh			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_5_PREG		DATGAIN_VGA1ATTEN_5_PREG					
R/W-1Fh				R/W-1Fh			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_4_PREG			
R/W-X				R/W-21h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_4_PREG		DATGAIN_VGA1ATTEN_4_PREG					
R/W-21h				R/W-21h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-602. DEQ_ALUT5__DEQ_ALUT4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_5_PREG	R/W	1Fh	Receive data path equalization LUT VGA2 attenuation control, entry 5 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_5_PREG	R/W	1Fh	Receive data path equalization LUT VGA1 attenuation control, entry 5 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-602. DEQ_ALUT5__DEQ_ALUT4_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_4_PREG	R/W	21h	Receive data path equalization LUT VGA2 attenuation control, entry 4 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_4_PREG	R/W	21h	Receive data path equalization LUT VGA1 attenuation control, entry 4 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-603. Register Call Summary for DEQ_ALUT5__DEQ_ALUT4_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT5__DEQ_ALUT4_j Register \(Offset = 4218h + formula\) \[reset = X\]: \[0\]](#)

11.201 DEQ_ALUT7__DEQ_ALUT6_j Register (Offset = 421Ch + formula) [reset = X]

DEQ_ALUT7__DEQ_ALUT6_j is shown in Figure 11-201 and described in Table 11-605.

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 6 register.

Offset = 421Ch + (j * 400h); where j = 0h to 1h

**Table 11-604. DEQ_ALUT7__DEQ_ALUT6_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 421Ch + formula
SERDES_16G1	0501 421Ch + formula
SERDES_16G2	0502 421Ch + formula
SERDES_16G3	0503 421Ch + formula

Figure 11-201. DEQ_ALUT7__DEQ_ALUT6_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_7_PREG			
R/W-X				R/W-19h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_7_PREG		DATGAIN_VGA1ATTEN_7_PREG					
R/W-19h				R/W-19h			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_6_PREG			
R/W-X				R/W-1Ch			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_6_PREG		DATGAIN_VGA1ATTEN_6_PREG					
R/W-1Ch				R/W-1Ch			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-605. DEQ_ALUT7__DEQ_ALUT6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_7_PREG	R/W	19h	Receive data path equalization LUT VGA2 attenuation control, entry 7 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_7_PREG	R/W	19h	Receive data path equalization LUT VGA1 attenuation control, entry 7 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-605. DEQ_ALUT7__DEQ_ALUT6_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_6_PREG	R/W	1Ch	Receive data path equalization LUT VGA2 attenuation control, entry 6 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_6_PREG	R/W	1Ch	Receive data path equalization LUT VGA1 attenuation control, entry 6 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-606. Register Call Summary for DEQ_ALUT7__DEQ_ALUT6_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT7__DEQ_ALUT6_j Register \(Offset = 421Ch + formula\) \[reset = X\]: \[0\]](#)

11.202 DEQ_ALUT9__DEQ_ALUT8_j Register (Offset = 4220h + formula) [reset = X]

DEQ_ALUT9__DEQ_ALUT8_j is shown in Figure 11-202 and described in Table 11-608.

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 8 register.

Offset = 4220h + (j * 400h); where j = 0h to 1h

**Table 11-607. DEQ_ALUT9__DEQ_ALUT8_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4220h + formula
SERDES_16G1	0501 4220h + formula
SERDES_16G2	0502 4220h + formula
SERDES_16G3	0503 4220h + formula

Figure 11-202. DEQ_ALUT9__DEQ_ALUT8_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_9_PREG			
R/W-X				R/W-14h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_9_PREG		DATGAIN_VGA1ATTEN_9_PREG					
R/W-14h				R/W-14h			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_8_PREG			
R/W-X				R/W-16h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_8_PREG		DATGAIN_VGA1ATTEN_8_PREG					
R/W-16h				R/W-16h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-608. DEQ_ALUT9__DEQ_ALUT8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_9_PREG	R/W	14h	Receive data path equalization LUT VGA2 attenuation control, entry 9 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_9_PREG	R/W	14h	Receive data path equalization LUT VGA1 attenuation control, entry 9 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-608. DEQ_ALUT9__DEQ_ALUT8_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_8_PREG	R/W	16h	Receive data path equalization LUT VGA2 attenuation control, entry 8 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_8_PREG	R/W	16h	Receive data path equalization LUT VGA1 attenuation control, entry 8 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-609. Register Call Summary for DEQ_ALUT9__DEQ_ALUT8_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT9__DEQ_ALUT8_j Register \(Offset = 4220h + formula\) \[reset = X\]: \[0\]](#)

11.203 DEQ_ALUT11__DEQ_ALUT10_j Register (Offset = 4224h + formula) [reset = X]

DEQ_ALUT11__DEQ_ALUT10_j is shown in Figure 11-203 and described in Table 11-611.

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 10 register.

Offset = 4224h + (j * 400h); where j = 0h to 1h

**Table 11-610. DEQ_ALUT11__DEQ_ALUT10_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4224h + formula
SERDES_16G1	0501 4224h + formula
SERDES_16G2	0502 4224h + formula
SERDES_16G3	0503 4224h + formula

Figure 11-203. DEQ_ALUT11__DEQ_ALUT10_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_11_PREG			
R/W-X				R/W-10h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_11_PREG		DATGAIN_VGA1ATTEN_11_PREG					
R/W-10h		R/W-10h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_10_PREG			
R/W-X				R/W-12h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_10_PREG		DATGAIN_VGA1ATTEN_10_PREG					
R/W-12h		R/W-12h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-611. DEQ_ALUT11__DEQ_ALUT10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_11_PREG	R/W	10h	Receive data path equalization LUT VGA2 attenuation control, entry 11 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_11_PREG	R/W	10h	Receive data path equalization LUT VGA1 attenuation control, entry 11 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-611. DEQ_ALUT11__DEQ_ALUT10_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_10_PREG	R/W	12h	Receive data path equalization LUT VGA2 attenuation control, entry 10 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_10_PREG	R/W	12h	Receive data path equalization LUT VGA1 attenuation control, entry 10 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-612. Register Call Summary for DEQ_ALUT11__DEQ_ALUT10_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT11__DEQ_ALUT10_j Register \(Offset = 4224h + formula\) \[reset = X\]: \[0\]](#)

11.204 DEQ_ALUT13__DEQ_ALUT12_j Register (Offset = 4228h + formula) [reset = X]

DEQ_ALUT13__DEQ_ALUT12_j is shown in [Figure 11-204](#) and described in [Table 11-614](#).

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 12 register.

Offset = 4228h + (j * 400h); where j = 0h to 1h

**Table 11-613. DEQ_ALUT13__DEQ_ALUT12_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4228h + formula
SERDES_16G1	0501 4228h + formula
SERDES_16G2	0502 4228h + formula
SERDES_16G3	0503 4228h + formula

Figure 11-204. DEQ_ALUT13__DEQ_ALUT12_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_13_PREG			
R/W-X				R/W-Ch			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_13_PREG		DATGAIN_VGA1ATTEN_13_PREG					
R/W-Ch				R/W-Ch			
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_12_PREG			
R/W-X				R/W-Eh			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_12_PREG		DATGAIN_VGA1ATTEN_12_PREG					
R/W-Eh				R/W-Eh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-614. DEQ_ALUT13__DEQ_ALUT12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_13_PREG	R/W	Ch	Receive data path equalization LUT VGA2 attenuation control, entry 13 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_13_PREG	R/W	Ch	Receive data path equalization LUT VGA1 attenuation control, entry 13 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-614. DEQ_ALUT13__DEQ_ALUT12_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_12_PREG	R/W	Eh	Receive data path equalization LUT VGA2 attenuation control, entry 12 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_12_PREG	R/W	Eh	Receive data path equalization LUT VGA1 attenuation control, entry 12 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-615. Register Call Summary for DEQ_ALUT13__DEQ_ALUT12_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT13__DEQ_ALUT12_j Register \(Offset = 4228h + formula\) \[reset = X\]: \[0\]](#)

11.205 DEQ_ALUT15__DEQ_ALUT14_j Register (Offset = 422Ch + formula) [reset = X]

DEQ_ALUT15__DEQ_ALUT14_j is shown in [Figure 11-205](#) and described in [Table 11-617](#).

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 14 register.

Offset = 422Ch + (j * 400h); where j = 0h to 1h

**Table 11-616. DEQ_ALUT15__DEQ_ALUT14_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 422Ch + formula
SERDES_16G1	0501 422Ch + formula
SERDES_16G2	0502 422Ch + formula
SERDES_16G3	0503 422Ch + formula

Figure 11-205. DEQ_ALUT15__DEQ_ALUT14_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_15_PREG			
R/W-X				R/W-9h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_15_PREG		DATGAIN_VGA1ATTEN_15_PREG					
R/W-9h		R/W-9h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_14_PREG			
R/W-X				R/W-Ah			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_14_PREG		DATGAIN_VGA1ATTEN_14_PREG					
R/W-Ah		R/W-Ah					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-617. DEQ_ALUT15__DEQ_ALUT14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_15_PREG	R/W	9h	Receive data path equalization LUT VGA2 attenuation control, entry 15 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_15_PREG	R/W	9h	Receive data path equalization LUT VGA1 attenuation control, entry 15 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-617. DEQ_ALUT15__DEQ_ALUT14_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_14_PREG	R/W	Ah	Receive data path equalization LUT VGA2 attenuation control, entry 14 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_14_PREG	R/W	Ah	Receive data path equalization LUT VGA1 attenuation control, entry 14 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-618. Register Call Summary for DEQ_ALUT15__DEQ_ALUT14_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT15__DEQ_ALUT14_j Register \(Offset = 422Ch + formula\) \[reset = X\]: \[0\]](#)

11.206 DEQ_ALUT17__DEQ_ALUT16_j Register (Offset = 4230h + formula) [reset = X]

DEQ_ALUT17__DEQ_ALUT16_j is shown in Figure 11-206 and described in Table 11-620.

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 16 register.

Offset = 4230h + (j * 400h); where j = 0h to 1h

**Table 11-619. DEQ_ALUT17__DEQ_ALUT16_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4230h + formula
SERDES_16G1	0501 4230h + formula
SERDES_16G2	0502 4230h + formula
SERDES_16G3	0503 4230h + formula

Figure 11-206. DEQ_ALUT17__DEQ_ALUT16_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_17_PREG			
R/W-X				R/W-7h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_17_PREG		DATGAIN_VGA1ATTEN_17_PREG					
R/W-7h		R/W-7h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_16_PREG			
R/W-X				R/W-8h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_16_PREG		DATGAIN_VGA1ATTEN_16_PREG					
R/W-8h		R/W-8h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-620. DEQ_ALUT17__DEQ_ALUT16_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_17_PREG	R/W	7h	Receive data path equalization LUT VGA2 attenuation control, entry 17 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_17_PREG	R/W	7h	Receive data path equalization LUT VGA1 attenuation control, entry 17 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-620. DEQ_ALUT17__DEQ_ALUT16_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_16_PREG	R/W	8h	Receive data path equalization LUT VGA2 attenuation control, entry 16 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_16_PREG	R/W	8h	Receive data path equalization LUT VGA1 attenuation control, entry 16 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-621. Register Call Summary for DEQ_ALUT17__DEQ_ALUT16_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT17__DEQ_ALUT16_j Register \(Offset = 4230h + formula\) \[reset = X\]: \[0\]](#)

11.207 DEQ_ALUT19__DEQ_ALUT18_j Register (Offset = 4234h + formula) [reset = X]

DEQ_ALUT19__DEQ_ALUT18_j is shown in [Figure 11-207](#) and described in [Table 11-623](#).

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 18 register.

Offset = 4234h + (j * 400h); where j = 0h to 1h

**Table 11-622. DEQ_ALUT19__DEQ_ALUT18_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4234h + formula
SERDES_16G1	0501 4234h + formula
SERDES_16G2	0502 4234h + formula
SERDES_16G3	0503 4234h + formula

Figure 11-207. DEQ_ALUT19__DEQ_ALUT18_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_19_PREG			
R/W-X				R/W-6h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_19_PREG		DATGAIN_VGA1ATTEN_19_PREG					
R/W-6h		R/W-6h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_18_PREG			
R/W-X				R/W-6h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_18_PREG		DATGAIN_VGA1ATTEN_18_PREG					
R/W-6h		R/W-7h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-623. DEQ_ALUT19__DEQ_ALUT18_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_19_PREG	R/W	6h	Receive data path equalization LUT VGA2 attenuation control, entry 19 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_19_PREG	R/W	6h	Receive data path equalization LUT VGA1 attenuation control, entry 19 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-623. DEQ_ALUT19__DEQ_ALUT18_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_18_PREG	R/W	6h	Receive data path equalization LUT VGA2 attenuation control, entry 18 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_18_PREG	R/W	7h	Receive data path equalization LUT VGA1 attenuation control, entry 18 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-624. Register Call Summary for DEQ_ALUT19__DEQ_ALUT18_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT19__DEQ_ALUT18_j Register \(Offset = 4234h + formula\) \[reset = X\]: \[0\]](#)

11.208 DEQ_ALUT21__DEQ_ALUT20_j Register (Offset = 4238h + formula) [reset = X]

DEQ_ALUT21__DEQ_ALUT20_j is shown in Figure 11-208 and described in Table 11-626.

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 20 register.

Offset = 4238h + (j * 400h); where j = 0h to 1h

**Table 11-625. DEQ_ALUT21__DEQ_ALUT20_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4238h + formula
SERDES_16G1	0501 4238h + formula
SERDES_16G2	0502 4238h + formula
SERDES_16G3	0503 4238h + formula

Figure 11-208. DEQ_ALUT21__DEQ_ALUT20_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_21_PREG			
R/W-X				R/W-5h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_21_PREG		DATGAIN_VGA1ATTEN_21_PREG					
R/W-5h		R/W-5h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_20_PREG			
R/W-X				R/W-5h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_20_PREG		DATGAIN_VGA1ATTEN_20_PREG					
R/W-5h		R/W-6h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-626. DEQ_ALUT21__DEQ_ALUT20_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_21_PREG	R/W	5h	Receive data path equalization LUT VGA2 attenuation control, entry 21 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_21_PREG	R/W	5h	Receive data path equalization LUT VGA1 attenuation control, entry 21 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-626. DEQ_ALUT21__DEQ_ALUT20_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_20_PREG	R/W	5h	Receive data path equalization LUT VGA2 attenuation control, entry 20 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_20_PREG	R/W	6h	Receive data path equalization LUT VGA1 attenuation control, entry 20 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-627. Register Call Summary for DEQ_ALUT21__DEQ_ALUT20_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT21__DEQ_ALUT20_j Register \(Offset = 4238h + formula\) \[reset = X\]: \[0\]](#)

11.209 DEQ_ALUT23__DEQ_ALUT22_j Register (Offset = 423Ch + formula) [reset = X]

DEQ_ALUT23__DEQ_ALUT22_j is shown in [Figure 11-209](#) and described in [Table 11-629](#).

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 22 register.

Offset = 423Ch + (j * 400h); where j = 0h to 1h

**Table 11-628. DEQ_ALUT23__DEQ_ALUT22_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 423Ch + formula
SERDES_16G1	0501 423Ch + formula
SERDES_16G2	0502 423Ch + formula
SERDES_16G3	0503 423Ch + formula

Figure 11-209. DEQ_ALUT23__DEQ_ALUT22_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_23_PREG			
R/W-X				R/W-4h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_23_PREG		DATGAIN_VGA1ATTEN_23_PREG					
R/W-4h		R/W-4h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_22_PREG			
R/W-X				R/W-4h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_22_PREG		DATGAIN_VGA1ATTEN_22_PREG					
R/W-4h		R/W-5h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-629. DEQ_ALUT23__DEQ_ALUT22_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_23_PREG	R/W	4h	Receive data path equalization LUT VGA2 attenuation control, entry 23 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_23_PREG	R/W	4h	Receive data path equalization LUT VGA1 attenuation control, entry 23 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-629. DEQ_ALUT23__DEQ_ALUT22_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_2_2_PREG	R/W	4h	Receive data path equalization LUT VGA2 attenuation control, entry 22 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_2_2_PREG	R/W	5h	Receive data path equalization LUT VGA1 attenuation control, entry 22 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-630. Register Call Summary for DEQ_ALUT23__DEQ_ALUT22_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT23__DEQ_ALUT22_j Register \(Offset = 423Ch + formula\) \[reset = X\]: \[0\]](#)

11.210 DEQ_ALUT25__DEQ_ALUT24_j Register (Offset = 4240h + formula) [reset = X]

DEQ_ALUT25__DEQ_ALUT24_j is shown in [Figure 11-210](#) and described in [Table 11-632](#).

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 24 register.

Offset = 4240h + (j * 400h); where j = 0h to 1h

**Table 11-631. DEQ_ALUT25__DEQ_ALUT24_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4240h + formula
SERDES_16G1	0501 4240h + formula
SERDES_16G2	0502 4240h + formula
SERDES_16G3	0503 4240h + formula

Figure 11-210. DEQ_ALUT25__DEQ_ALUT24_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_25_PREG			
R/W-X				R/W-3h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_25_PREG		DATGAIN_VGA1ATTEN_25_PREG					
R/W-3h		R/W-3h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_24_PREG			
R/W-X				R/W-3h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_24_PREG		DATGAIN_VGA1ATTEN_24_PREG					
R/W-3h		R/W-4h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-632. DEQ_ALUT25__DEQ_ALUT24_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_25_PREG	R/W	3h	Receive data path equalization LUT VGA2 attenuation control, entry 25 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_25_PREG	R/W	3h	Receive data path equalization LUT VGA1 attenuation control, entry 25 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-632. DEQ_ALUT25__DEQ_ALUT24_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_24_PREG	R/W	3h	Receive data path equalization LUT VGA2 attenuation control, entry 24 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_24_PREG	R/W	4h	Receive data path equalization LUT VGA1 attenuation control, entry 24 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-633. Register Call Summary for DEQ_ALUT25__DEQ_ALUT24_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT25__DEQ_ALUT24_j Register \(Offset = 4240h + formula\) \[reset = X\]: \[0\]](#)

11.211 DEQ_ALUT27__DEQ_ALUT26_j Register (Offset = 4244h + formula) [reset = X]

DEQ_ALUT27__DEQ_ALUT26_j is shown in [Figure 11-211](#) and described in [Table 11-635](#).

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 26 register.

Offset = 4244h + (j * 400h); where j = 0h to 1h

**Table 11-634. DEQ_ALUT27__DEQ_ALUT26_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4244h + formula
SERDES_16G1	0501 4244h + formula
SERDES_16G2	0502 4244h + formula
SERDES_16G3	0503 4244h + formula

Figure 11-211. DEQ_ALUT27__DEQ_ALUT26_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_27_PREG			
R/W-X				R/W-2h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_27_PREG		DATGAIN_VGA1ATTEN_27_PREG					
R/W-2h		R/W-2h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_26_PREG			
R/W-X				R/W-2h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_26_PREG		DATGAIN_VGA1ATTEN_26_PREG					
R/W-2h		R/W-3h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-635. DEQ_ALUT27__DEQ_ALUT26_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_27_PREG	R/W	2h	Receive data path equalization LUT VGA2 attenuation control, entry 27 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_27_PREG	R/W	2h	Receive data path equalization LUT VGA1 attenuation control, entry 27 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-635. DEQ_ALUT27__DEQ_ALUT26_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_26_PREG	R/W	2h	Receive data path equalization LUT VGA2 attenuation control, entry 26 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_26_PREG	R/W	3h	Receive data path equalization LUT VGA1 attenuation control, entry 26 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-636. Register Call Summary for DEQ_ALUT27__DEQ_ALUT26_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT27__DEQ_ALUT26_j Register \(Offset = 4244h + formula\) \[reset = X\]: \[0\]](#)

11.212 DEQ_ALUT29__DEQ_ALUT28_j Register (Offset = 4248h + formula) [reset = X]

DEQ_ALUT29__DEQ_ALUT28_j is shown in [Figure 11-212](#) and described in [Table 11-638](#).

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 28 register.

Offset = 4248h + (j * 400h); where j = 0h to 1h

**Table 11-637. DEQ_ALUT29__DEQ_ALUT28_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4248h + formula
SERDES_16G1	0501 4248h + formula
SERDES_16G2	0502 4248h + formula
SERDES_16G3	0503 4248h + formula

Figure 11-212. DEQ_ALUT29__DEQ_ALUT28_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_29_PREG			
R/W-X				R/W-1h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_29_PREG		DATGAIN_VGA1ATTEN_29_PREG					
R/W-1h		R/W-1h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_28_PREG			
R/W-X				R/W-1h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_28_PREG		DATGAIN_VGA1ATTEN_28_PREG					
R/W-1h		R/W-2h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-638. DEQ_ALUT29__DEQ_ALUT28_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_29_PREG	R/W	1h	Receive data path equalization LUT VGA2 attenuation control, entry 29 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_29_PREG	R/W	1h	Receive data path equalization LUT VGA1 attenuation control, entry 29 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-638. DEQ_ALUT29__DEQ_ALUT28_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_28_PREG	R/W	1h	Receive data path equalization LUT VGA2 attenuation control, entry 28 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_28_PREG	R/W	2h	Receive data path equalization LUT VGA1 attenuation control, entry 28 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-639. Register Call Summary for DEQ_ALUT29__DEQ_ALUT28_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT29__DEQ_ALUT28_j Register \(Offset = 4248h + formula\) \[reset = X\]: \[0\]](#)

11.213 DEQ_ALUT31__DEQ_ALUT30_j Register (Offset = 424Ch + formula) [reset = X]

DEQ_ALUT31__DEQ_ALUT30_j is shown in Figure 11-213 and described in Table 11-641.

Return to [Summary Table](#).

Receive data path equalization LUT attenuation, entry 30 register.

Offset = 424Ch + (j * 400h); where j = 0h to 1h

**Table 11-640. DEQ_ALUT31__DEQ_ALUT30_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 424Ch + formula
SERDES_16G1	0501 424Ch + formula
SERDES_16G2	0502 424Ch + formula
SERDES_16G3	0503 424Ch + formula

Figure 11-213. DEQ_ALUT31__DEQ_ALUT30_j Register

31	30	29	28	27	26	25	24
RESERVED				DATGAIN_VGA2ATTEN_31_PREG			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
DATGAIN_VGA2ATTEN_31_PREG		DATGAIN_VGA1ATTEN_31_PREG					
R/W-0h		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED				DATGAIN_VGA2ATTEN_30_PREG			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
DATGAIN_VGA2ATTEN_30_PREG		DATGAIN_VGA1ATTEN_30_PREG					
R/W-0h		R/W-1h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-641. DEQ_ALUT31__DEQ_ALUT30_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-22	DATGAIN_VGA2ATTEN_31_PREG	R/W	0h	Receive data path equalization LUT VGA2 attenuation control, entry 31 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
21-16	DATGAIN_VGA1ATTEN_31_PREG	R/W	0h	Receive data path equalization LUT VGA1 attenuation control, entry 31 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-641. DEQ_ALUT31__DEQ_ALUT30_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	X	
11-6	DATGAIN_VGA2ATTEN_30_PREG	R/W	0h	Receive data path equalization LUT VGA2 attenuation control, entry 30 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest
5-0	DATGAIN_VGA1ATTEN_30_PREG	R/W	1h	Receive data path equalization LUT VGA1 attenuation control, entry 30 Attenuation 6'b11_1111 Highest :: 6'b00_0110 Nominal :: 6'b00_0000 Lowest

Table 11-642. Register Call Summary for DEQ_ALUT31__DEQ_ALUT30_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_ALUT31__DEQ_ALUT30_j Register \(Offset = 424Ch + formula\) \[reset = X\]: \[0\]](#)

11.214 DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j Register (Offset = 4250h + formula) [reset = X]

DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j is shown in Figure 11-214 and described in Table 11-644.

Return to [Summary Table](#).

Receive data path DFE tap control register.

Offset = 4250h + (j * 400h); where j = 0h to 1h

Table 11-643.
DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4250h + formula
SERDES_16G1	0501 4250h + formula
SERDES_16G2	0502 4250h + formula
SERDES_16G3	0503 4250h + formula

Figure 11-214. DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DATDFE_TAP0_THRESH_MNT_PREG				DATDFE_TAP0_THRESH_ACQ_PREG			
R/W-Ah				R/W-Bh			
15	14	13	12	11	10	9	8
RESERVED						SUM_TAP4STEPSIZE_PREG	
R/W-X						R/W-3h	
7	6	5	4	3	2	1	0
SUM_TAP3STEPSIZE_PREG		SUM_TAP2STEPSIZE_PREG		SUM_TAP1STEPSIZE_PREG		SUM_TAP0STEPSIZE_PREG	
R/W-3h		R/W-3h		R/W-1h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-644. DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-20	DATDFE_TAP0_THRESH_MNT_PREG	R/W	Ah	Receive data path DFE tap 0 accumulator threshold for maintenance. Threshold = $2^{\text{datdfe_tap0_thresh_mnt_preg}}$
19-16	DATDFE_TAP0_THRESH_ACQ_PREG	R/W	Bh	Receive data path DFE tap 0 accumulator threshold for acquisition. Threshold = $2^{\text{datdfe_tap0_thresh_acq_preg}}$
15-10	RESERVED	R/W	X	
9-8	SUM_TAP4STEPSIZE_PREG	R/W	3h	Receive data path DFE tap 4 feedback current trim: Current Mirror Ratio 2'b11 Lowest 1.00 2'b10 : 1.33 2'b01 : 2.00 2'b00 Highest 4.00

Table 11-644. DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	SUM_TAP3STEPSIZE_P REG	R/W	3h	Receive data path DFE tap 3 feedback current trim: Current Mirror Ratio 2'b11 Lowest 1.00 2'b 10 : 1.33 2'b 01 : 2.00 2'b00 Highest 4.00
5-4	SUM_TAP2STEPSIZE_P REG	R/W	3h	Receive data path DFE tap 2 feedback current trim: Current Mirror Ratio 2'b11 Lowest 1.00 2'b 10 : 1.33 2'b 01 : 2.00 2'b00 Highest 4.00
3-2	SUM_TAP1STEPSIZE_P REG	R/W	1h	Receive data path DFE tap 1 feedback current trim: Current Mirror Ratio 2'b11 Lowest 1.00 2'b 10 : 1.33 2'b 01 : 2.00 2'b00 Highest 4.00
1-0	SUM_TAP0STEPSIZE_P REG	R/W	0h	Receive data path DFE tap 0 feedback current trim: Current Mirror Ratio 2'b11 Lowest 1.00 2'b 10 : 1.33 2'b 01 : 2.00 2'b00 Highest 4.00

Table 11-645. Register Call Summary for DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_DFETAP0__DEQ_DFETAP_CTRL_PREG_j Register \(Offset = 4250h + formula\) \[reset = X\]: \[0\]](#)

11.215 DEQ_DFETAP1__DEQ_DFETAP0_OVR_j Register (Offset = 4254h + formula) [reset = X]

DEQ_DFETAP1__DEQ_DFETAP0_OVR_j is shown in Figure 11-215 and described in Table 11-647.

Return to [Summary Table](#).

Receive data path DFE tap 0 override register.

Offset = 4254h + (j * 400h); where j = 0h to 1h

Table 11-646.
DEQ_DFETAP1__DEQ_DFETAP0_OVR_j Instances

Instance	Physical Address
SERDES_16G0	0500 4254h + formula
SERDES_16G1	0501 4254h + formula
SERDES_16G2	0502 4254h + formula
SERDES_16G3	0503 4254h + formula

Figure 11-215. DEQ_DFETAP1__DEQ_DFETAP0_OVR_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DATDFE_TAP1_THRESH_MNT_PREG				DATDFE_TAP1_THRESH_ACQ_PREG			
R/W-Ah				R/W-Bh			
15	14	13	12	11	10	9	8
RESERVED							DATDFE_TAP0_OVREN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
DATDFE_TAP0_OVR_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-647. DEQ_DFETAP1__DEQ_DFETAP0_OVR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-20	DATDFE_TAP1_THRESH_MNT_PREG	R/W	Ah	Receive data path DFE tap 1 accumulator threshold for maintenance. Threshold = $2^{\text{datdfe_tap1_thresh_mnt_preg}}$
19-16	DATDFE_TAP1_THRESH_ACQ_PREG	R/W	Bh	Receive data path DFE tap 1 accumulator threshold for acquisition. Threshold = $2^{\text{datdfe_tap1_thresh_acq_preg}}$
15-9	RESERVED	R/W	X	
8	DATDFE_TAP0_OVREN_PREG	R/W	0h	Receive data path DFE tap 0 weight active high override enable.
7-0	DATDFE_TAP0_OVR_PREG	R/W	0h	When datdfe_tap0_ovren_preg is asserted high, this value overrides the tap 0 weight. Value is { sign bit, 7-bit magnitude }

Table 11-648. Register Call Summary for DEQ_DFETAP1__DEQ_DFETAP0_OVR_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_DFETAP1__DEQ_DFETAP0_OVR_j Register \(Offset = 4254h + formula\) \[reset = X\]: \[0\]](#)

11.216 DEQ_DFETAP2__DEQ_DFETAP1_OVR_j Register (Offset = 4258h + formula) [reset = X]

DEQ_DFETAP2__DEQ_DFETAP1_OVR_j is shown in Figure 11-216 and described in Table 11-650.

Return to [Summary Table](#).

Receive data path DFE tap 1 override register.

Offset = 4258h + (j * 400h); where j = 0h to 1h

Table 11-649.
DEQ_DFETAP2__DEQ_DFETAP1_OVR_j Instances

Instance	Physical Address
SERDES_16G0	0500 4258h + formula
SERDES_16G1	0501 4258h + formula
SERDES_16G2	0502 4258h + formula
SERDES_16G3	0503 4258h + formula

Figure 11-216. DEQ_DFETAP2__DEQ_DFETAP1_OVR_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DATDFE_TAP2_THRESH_MNT_PREG				DATDFE_TAP2_THRESH_ACQ_PREG			
R/W-Ah				R/W-Bh			
15	14	13	12	11	10	9	8
RESERVED							DATDFE_TAP1_OVREN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
DATDFE_TAP1_OVR_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-650. DEQ_DFETAP2__DEQ_DFETAP1_OVR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-20	DATDFE_TAP2_THRESH_MNT_PREG	R/W	Ah	Receive data path DFE tap 2 accumulator threshold for maintenance. Threshold = $2^{\text{datdfe_tap2_thresh_mnt_preg}}$
19-16	DATDFE_TAP2_THRESH_ACQ_PREG	R/W	Bh	Receive data path DFE tap 2 accumulator threshold for acquisition. Threshold = $2^{\text{datdfe_tap2_thresh_acq_preg}}$
15-9	RESERVED	R/W	X	
8	DATDFE_TAP1_OVREN_PREG	R/W	0h	Receive data path DFE tap 1 weight active high override enable.
7-0	DATDFE_TAP1_OVR_PREG	R/W	0h	When datdfe_tap1_ovren_preg is asserted high, this value overrides the tap 1 weight. Value is { sign bit, 7-bit magnitude }

Table 11-651. Register Call Summary for DEQ_DFETAP2__DEQ_DFETAP1_OVR_j

<div>16-G SerDes Registers</div> <ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] DEQ_DFETAP2__DEQ_DFETAP1_OVR_j Register (Offset = 4258h + formula) [reset = X]: [0]

11.217 DEQ_DFETAP3__DEQ_DFETAP2_OVR_j Register (Offset = 425Ch + formula) [reset = X]

DEQ_DFETAP3__DEQ_DFETAP2_OVR_j is shown in [Figure 11-217](#) and described in [Table 11-653](#).

Return to [Summary Table](#).

Receive data path DFE tap 2 override register.

Offset = 425Ch + (j * 400h); where j = 0h to 1h

Table 11-652.
DEQ_DFETAP3__DEQ_DFETAP2_OVR_j Instances

Instance	Physical Address
SERDES_16G0	0500 425Ch + formula
SERDES_16G1	0501 425Ch + formula
SERDES_16G2	0502 425Ch + formula
SERDES_16G3	0503 425Ch + formula

Figure 11-217. DEQ_DFETAP3__DEQ_DFETAP2_OVR_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DATDFE_TAP3_THRESH_MNT_PREG				DATDFE_TAP3_THRESH_ACQ_PREG			
R/W-Ah				R/W-Bh			
15	14	13	12	11	10	9	8
RESERVED							DATDFE_TAP2_OVREN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
DATDFE_TAP2_OVR_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-653. DEQ_DFETAP3__DEQ_DFETAP2_OVR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-20	DATDFE_TAP3_THRESH_MNT_PREG	R/W	Ah	Receive data path DFE tap 3 accumulator threshold for maintenance. Threshold = $2^{\text{datdfe_tap3_thresh_mnt_preg}}$
19-16	DATDFE_TAP3_THRESH_ACQ_PREG	R/W	Bh	Receive data path DFE tap 3 accumulator threshold for acquisition. Threshold = $2^{\text{datdfe_tap3_thresh_acq_preg}}$
15-9	RESERVED	R/W	X	
8	DATDFE_TAP2_OVREN_PREG	R/W	0h	Receive data path DFE tap 2 weight active high override enable.
7-0	DATDFE_TAP2_OVR_PREG	R/W	0h	When datdfe_tap2_ovren_preg is asserted high, this value overrides the tap 2 weight. Value is { sign bit, 7-bit magnitude }

Table 11-654. Register Call Summary for DEQ_DFETAP3__DEQ_DFETAP2_OVR_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_DFETAP3__DEQ_DFETAP2_OVR_j Register \(Offset = 425Ch + formula\) \[reset = X\]: \[0\]](#)

11.218 DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j Register (Offset = 4260h + formula) [reset = X]

DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j is shown in [Figure 11-218](#) and described in [Table 11-656](#).

Return to [Summary Table](#).

Receive data path DFE tap 3 override register.

Offset = 4260h + (j * 400h); where j = 0h to 1h

Table 11-655.
DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4260h + formula
SERDES_16G1	0501 4260h + formula
SERDES_16G2	0502 4260h + formula
SERDES_16G3	0503 4260h + formula

Figure 11-218. DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DATDFE_TAP4_THRESH_MNT_PREG				DATDFE_TAP4_THRESH_ACQ_PREG			
R/W-Ah				R/W-Bh			
15	14	13	12	11	10	9	8
RESERVED							DATDFE_TAP3_OVREN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
DATDFE_TAP3_OVR_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-656. DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-20	DATDFE_TAP4_THRESH_MNT_PREG	R/W	Ah	Receive data path DFE tap 4 accumulator threshold for maintenance. Threshold = $2^{\text{datdfe_tap4_thresh_mnt_preg}}$
19-16	DATDFE_TAP4_THRESH_ACQ_PREG	R/W	Bh	Receive data path DFE tap 4 accumulator threshold for acquisition. Threshold = $2^{\text{datdfe_tap4_thresh_acq_preg}}$
15-9	RESERVED	R/W	X	
8	DATDFE_TAP3_OVREN_PREG	R/W	0h	Receive data path DFE tap 3 weight active high override enable.
7-0	DATDFE_TAP3_OVR_PREG	R/W	0h	When datdfe_tap3_ovren_preg is asserted high, this value overrides the tap 3 weight. Value is { sign bit, 7-bit magnitude }

Table 11-657. Register Call Summary for DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_DFETAP4_PREG__DEQ_DFETAP3_OVR_j Register \(Offset = 4260h + formula\) \[reset = X\]: \[0\]](#)

11.219 DATDFE_TAPCAP_THRESH_PREG__DEQ_DFETAP4_OVR_j Register (Offset = 4264h + formula) [reset = X]

DATDFE_TAPCAP_THRESH_PREG__DEQ_DFETAP4_OVR_j is shown in Figure 11-219 and described in Table 11-659.

Return to [Summary Table](#).

Receive data path DFE tap 4 override register.

Offset = 4264h + (j * 400h); where j = 0h to 1h

Table 11-658. DATDFE_TAPCAP_THRESH_PREG__DEQ_DFETAP4_OVR_j Instances

Instance	Physical Address
SERDES_16G0	0500 4264h + formula
SERDES_16G1	0501 4264h + formula
SERDES_16G2	0502 4264h + formula
SERDES_16G3	0503 4264h + formula

Figure 11-219. DATDFE_TAPCAP_THRESH_PREG__DEQ_DFETAP4_OVR_j Register

31	30	29	28	27	26	25	24
RESERVED				DATDFE_TAPCAP_THRESH_PREG			
R/W-X				R/W-FFFh			
23	22	21	20	19	18	17	16
DATDFE_TAPCAP_THRESH_PREG							
R/W-FFFh							
15	14	13	12	11	10	9	8
RESERVED							DATDFE_TAP4_OVREN_PREG
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
DATDFE_TAP4_OVR_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-659. DATDFE_TAPCAP_THRESH_PREG__DEQ_DFETAP4_OVR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	DATDFE_TAPCAP_THRESH_PREG	R/W	FFFh	Threshold for capping the sum of the receive data path DFE tap magnitudes.
15-9	RESERVED	R/W	X	
8	DATDFE_TAP4_OVREN_PREG	R/W	0h	Receive data path DFE tap 4 weight active high override enable.
7-0	DATDFE_TAP4_OVR_PREG	R/W	0h	When datdfe_tap4_ovren_preg is asserted high, this value overrides the tap 4 weight. Value is { sign bit, 7-bit magnitude }

Table 11-660. Register Call Summary for DATDFE_TAPCAP_THRESH_PREG__DEQ_DFETAP4_OVR_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DATDFE_TAPCAP_THRESH_PREG__DEQ_DFETAP4_OVR_j Register \(Offset = 4264h + formula\) \[reset = X\]: \[0\]](#)

11.220 DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG_j Register (Offset = 4268h + formula) [reset = X]

DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG_j is shown in Figure 11-220 and described in Table 11-662.

Return to [Summary Table](#).

DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG

Offset = 4268h + (j * 400h); where j = 0h to 1h

Table 11-661. DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4268h + formula
SERDES_16G1	0501 4268h + formula
SERDES_16G2	0502 4268h + formula
SERDES_16G3	0503 4268h + formula

Figure 11-220. DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED						DFE_TAU_TRAINING_MASK_PREG	DFE_DATGAIN_TRAINING_MASK_PREG
R/W-X						R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
DFE_DATOFF_TRAINING_MASK_PREG	DFE_DATDFE4_TRAINING_MASK_PREG	DFE_DATDFE3_TRAINING_MASK_PREG	DFE_DATDFE2_TRAINING_MASK_PREG	DFE_DATDFE1_TRAINING_MASK_PREG	DFE_DATDFE0_TRAINING_MASK_PREG	DFE_PRECUR_TRAINING_MASK_PREG	DFE_FALSEEYE_TRAINING_MASK_PREG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED			DFE_EN_1010_IGNORE_MODE3_PREG	RESERVED			DFE_EN_1010_IGNORE_MODE2_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h
7	6	5	4	3	2	1	0
RESERVED			DFE_EN_1010_IGNORE_MODE1_PREG	RESERVED			DFE_EN_1010_IGNORE_MODE0_PREG
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-662. DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25	DFE_TAU_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the tau training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted.
24	DFE_DATGAIN_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the data path gain training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted.

Table 11-662. DFE_TRAINING_MASK_PREG_DFE_EN_1010_IGNORE_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	DFE_DATOFF_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the data path offset training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted.
22	DFE_DATDFE4_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the DFE tap 4 training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted.
21	DFE_DATDFE3_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the DFE tap 3 training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted.
20	DFE_DATDFE2_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the DFE tap 2 training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted.
19	DFE_DATDFE1_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the DFE tap 1 training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted. This should be programmed same as dfe_datdfe0_training_mask_preg as both Tap1 and Tap0 will be used by postcur module
18	DFE_DATDFE0_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the DFE tap 0 training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted. This should be programmed same as dfe_datdfe1_training_mask_preg as both Tap1 and Tap0 will be used by postcur module
17	DFE_PRECUR_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, the far-end transmit pre cursor training will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted.
16	DFE_FALSEEYE_TRAINING_MASK_PREG	R/W	0h	When set to 1'b0, false eye detection will be paused during rx_eq_training_data_valid deassertion and during detection of 1010 pattern occurs with dfe_en_1010_ignore_modeX_preg is asserted.
15-13	RESERVED	R/W	X	
12	DFE_EN_1010_IGNORE_MODE3_PREG	R/W	0h	Active high enable for the DFE ignore 1010 function when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011.
11-9	RESERVED	R/W	X	
8	DFE_EN_1010_IGNORE_MODE2_PREG	R/W	0h	Active high enable for the DFE ignore 1010 function when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b010.
7-5	RESERVED	R/W	X	
4	DFE_EN_1010_IGNORE_MODE1_PREG	R/W	0h	Active high enable for the DFE ignore 1010 function when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b001
3-1	RESERVED	R/W	X	
0	DFE_EN_1010_IGNORE_MODE0_PREG	R/W	0h	Active high enable for the DFE ignore 1010 function when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b000.

**Table 11-663. Register Call Summary for
DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DFE_TRAINING_MASK_PREG__DFE_EN_1010_IGNORE_PREG_j Register \(Offset = 4268h + formula\) \[reset = X\]: \[0\]](#)

11.221 DFE_EN_1010_IGNORE_DIAG_PREG_j Register (Offset = 426Ch + formula) [reset = X]

DFE_EN_1010_IGNORE_DIAG_PREG_j is shown in Figure 11-221 and described in Table 11-665.

Return to [Summary Table](#).

DFE_EN_1010_IGNORE_DIAG_PREG

Offset = 426Ch + (j * 400h); where j = 0h to 1h

Table 11-664.
DFE_EN_1010_IGNORE_DIAG_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 426Ch + formula
SERDES_16G1	0501 426Ch + formula
SERDES_16G2	0502 426Ch + formula
SERDES_16G3	0503 426Ch + formula

Figure 11-221. DFE_EN_1010_IGNORE_DIAG_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
DFE_1010_DIAGCNTR_VAL							DFE_1010_DIAGCNTR_EN_PREG
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-665. DFE_EN_1010_IGNORE_DIAG_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-1	DFE_1010_DIAGCNTR_VAL	R	0h	Indicates how many 1010.. or 0101.. pattern words are detected
0	DFE_1010_DIAGCNTR_EN_PREG	R/W	0h	Level sensitive diagnostic bit: When de-asserted, counter will be cleared and will not advance. When asserted, counter increments every time 1010 pattern is detected.

Table 11-666. Register Call Summary for DFE_EN_1010_IGNORE_DIAG_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DFE_EN_1010_IGNORE_DIAG_PREG_j Register \(Offset = 426Ch + formula\) \[reset = X\]: \[0\]](#)

11.222 DEQ_PRECUR_PREG_j Register (Offset = 4270h + formula) [reset = X]

DEQ_PRECUR_PREG_j is shown in [Figure 11-222](#) and described in [Table 11-668](#).

Return to [Summary Table](#).

Receive data path far-end transmit precursor equalization control register.

Offset = 4270h + (j * 400h); where j = 0h to 1h

Table 11-667. DEQ_PRECUR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4270h + formula
SERDES_16G1	0501 4270h + formula
SERDES_16G2	0502 4270h + formula
SERDES_16G3	0503 4270h + formula

Figure 11-222. DEQ_PRECUR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PRECUR_THRESH_PREG			
R/W-X				R/W-8h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-668. DEQ_PRECUR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PRECUR_THRESH_PREG	R/W	8h	Receive data path far-end transmit precursor equalization accumulator threshold. Threshold = $2^{\text{precur_thresh_preg}}$

Table 11-669. Register Call Summary for DEQ_PRECUR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_PRECUR_PREG_j Register \(Offset = 4270h + formula\) \[reset = X\]: \[0\]](#)

11.223 DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j Register (Offset = 4280h + formula) [reset = X]

DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j is shown in Figure 11-223 and described in Table 11-671.

Return to [Summary Table](#).

Receive data path far-end transmit postcursor equalization control register.

Offset = 4280h + (j * 400h); where j = 0h to 1h

Table 11-670. DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4280h + formula
SERDES_16G1	0501 4280h + formula
SERDES_16G2	0502 4280h + formula
SERDES_16G3	0503 4280h + formula

Figure 11-223. DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j Register

31	30	29	28	27	26	25	24
POSTCUR_INCR_TAP0SGN_PREG	POSTCUR_INCR_TAP0MAG_PREG						
R/W-1h				R/W-40h			
23	22	21	20	19	18	17	16
POSTCUR_INCR_TAP1SGN_PREG	POSTCUR_INCR_TAP1MAG_PREG						
R/W-0h				R/W-3h			
15	14	13	12	11	10	9	8
RESERVED						POSTCUR_INCR_GAIN_PREG	
R/W-X						R/W-14h	
7	6	5	4	3	2	1	0
POSTCUR_INCR_GAIN_PREG				POSTCUR_DECR_GAIN_PREG			
R/W-14h				R/W-1Bh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-671. DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POSTCUR_INCR_TAP0SGN_PREG	R/W	1h	Receive data path far-end transmit postcursor equalization increment request tap 0 threshold sign.
30-24	POSTCUR_INCR_TAP0MAG_PREG	R/W	40h	Receive data path far-end transmit postcursor equalization increment request tap 0 threshold unsigned binary encoded magnitude. Note the current internal data path tap0 value must be less than { postcur_incr_tap0sgn_preg, postcur_incr_tap0mag_preg } for an increment request to be made.
23	POSTCUR_INCR_TAP1SGN_PREG	R/W	0h	Receive data path far-end transmit postcursor equalization increment request tap 1 threshold sign.

**Table 11-671. DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
22-16	POSTCUR_INCR_TAP1MAG_PREG	R/W	3h	Receive data path far-end transmit postcursor equalization increment request tap 1 threshold unsigned binary encoded magnitude. Note the current internal data path tap1 value must be less than { postcur_incr_tap1sgn_preg, postcur_incr_tap1mag_preg } for an increment request to be made.
15-10	RESERVED	R/W	X	
9-5	POSTCUR_INCR_GAIN_PREG	R/W	14h	Receive data path far-end transmit postcursor equalization increment request gain threshold. Note the current internal data path gain must be less than this value for an increment request to be made.
4-0	POSTCUR_DECR_GAIN_PREG	R/W	1Bh	Receive data path far-end transmit postcursor equalization decrement request gain threshold. Note the current internal data path gain must be greater than this value for an decrement request to be made.

Table 11-672. Register Call Summary for DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_POSTCUR_INCR_PREG__DEQ_POSTCUR_PREG_j Register \(Offset = 4280h + formula\) \[reset = X\]: \[0\]](#)

11.224 DEQ_POSTCUR_DECR_PREG_j Register (Offset = 4284h + formula) [reset = X]

DEQ_POSTCUR_DECR_PREG_j is shown in [Figure 11-224](#) and described in [Table 11-674](#).

Return to [Summary Table](#).

Receive data path far-end transmit postcursor equalization decrement control register.

Offset = 4284h + (j * 400h); where j = 0h to 1h

Table 11-673. DEQ_POSTCUR_DECR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4284h + formula
SERDES_16G1	0501 4284h + formula
SERDES_16G2	0502 4284h + formula
SERDES_16G3	0503 4284h + formula

Figure 11-224. DEQ_POSTCUR_DECR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
POSTCUR_DE CR_TAP0SGN_ PREG	POSTCUR_DECR_TAP0MAG_PREG						
R/W-1h				R/W-1h			
7	6	5	4	3	2	1	0
POSTCUR_DE CR_TAP1SGN_ PREG	POSTCUR_DECR_TAP1MAG_PREG						
R/W-0h				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-674. DEQ_POSTCUR_DECR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	POSTCUR_DECR_TAP0SGN_PREG	R/W	1h	Receive data path far-end transmit postcursor equalization decrement request tap 0 threshold sign.
14-8	POSTCUR_DECR_TAP0MAG_PREG	R/W	1h	Receive data path far-end transmit postcursor equalization decrement request tap 0 threshold unsigned binary encoded magnitude. Note the current internal data path tap0 value must be greater than { postcur_decr_tap0sgn_preg, postcur_decr_tap0mag_preg } for an decrement request to be made.
7	POSTCUR_DECR_TAP1SGN_PREG	R/W	0h	Receive data path far-end transmit postcursor equalization decrement request tap 1 threshold sign.

Table 11-674. DEQ_POSTCUR_DECR_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	POSTCUR_DECR_TAP1 MAG_PREG	R/W	5h	Receive data path far-end transmit postcursor equalization decrement request tap 1 threshold unsigned binary encoded magnitude. Note the current internal data path tap1 value must be greater than { postcur_decr_tap1sgn_preg, postcur_decr_tap1mag_preg } for an decrement request to be made.

Table 11-675. Register Call Summary for DEQ_POSTCUR_DECR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_POSTCUR_DECR_PREG_j Register \(Offset = 4284h + formula\) \[reset = X\]: \[0\]](#)

11.225 DEQ_FALSEEYE_CTRL_PREG_j Register (Offset = 4290h + formula) [reset = X]

DEQ_FALSEEYE_CTRL_PREG_j is shown in [Figure 11-225](#) and described in [Table 11-677](#).

Return to [Summary Table](#).

Receive data path equalization (DEQ) false eye control register.

Offset = 4290h + (j * 400h); where j = 0h to 1h

**Table 11-676. DEQ_FALSEEYE_CTRL_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4290h + formula
SERDES_16G1	0501 4290h + formula
SERDES_16G2	0502 4290h + formula
SERDES_16G3	0503 4290h + formula

Figure 11-225. DEQ_FALSEEYE_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED		FALSEEYE_KICKVAL_PREG					
R/W-X		R/W-20h					
7	6	5	4	3	2	1	0
FALSEEYE_DISABLE_PREG	FALSEEYE_BW_PREG		FALSEEYE_THRESH_PREG				
R/W-0h		R/W-2h		R/W-Ch			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-677. DEQ_FALSEEYE_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-8	FALSEEYE_KICKVAL_PREG	R/W	20h	Receive data path equalization (DEQ) false eye detection phase kick amplitude. This field represents the DPI/EPI (hires) adjustment to be made in response to a false eye detection event. The value is unsigned and will always advance the Pis in the positive direction. Note the default 6'h20 is 1/2UI.
7	FALSEEYE_DISABLE_PREG	R/W	0h	Receive data path equalization (DEQ) false eye detection active high disable.
6-5	FALSEEYE_BW_PREG	R/W	2h	Receive data path equalization (DEQ) false eye detection bandwidth selection. Increasing values incur increasing bandwidth.
4-0	FALSEEYE_THRESH_PREG	R/W	Ch	Receive data path equalization (DEQ) false eye detection binary encoded threshold.

Table 11-678. Register Call Summary for DEQ_FALSEEYE_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_FALSEEYE_CTRL_PREG_j Register \(Offset = 4290h + formula\) \[reset = X\]: \[0\]](#)

11.226 DEQ_TAU_CTRL1_FAST_MAINT_PREG_j Register (Offset = 429Ch + formula) [reset = X]

DEQ_TAU_CTRL1_FAST_MAINT_PREG_j is shown in Figure 11-226 and described in Table 11-680.

Return to [Summary Table](#).

Receive data path equalization (DEQ) fast maintenance tau training control register 1.

Offset = 429Ch + (j * 400h); where j = 0h to 1h

Table 11-679.
DEQ_TAU_CTRL1_FAST_MAINT_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 429Ch + formula
SERDES_16G1	0501 429Ch + formula
SERDES_16G2	0502 429Ch + formula
SERDES_16G3	0503 429Ch + formula

Figure 11-226. DEQ_TAU_CTRL1_FAST_MAINT_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	TAU_DISABLE_FAST_MAINT_PREG	TAU_FAST_MAINT_TIME_PREG				TAU_FAST_MAINT_THRESH_PREG	
R/W-X	R/W-0h	R/W-3h				R/W-1h	
23	22	21	20	19	18	17	16
TAU_FAST_MAINT_THRESH_PREG							
R/W-1h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-680. DEQ_TAU_CTRL1_FAST_MAINT_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	TAU_DISABLE_FAST_MAINT_PREG	R/W	0h	Receive data path equalization (DEQ) fast maintenance tau algorithm active high disable. The tau algorithm will be skipped during calls from the data path equalization state machine when in the fast maintenance period.
29-26	TAU_FAST_MAINT_TIME_PREG	R/W	3h	Receive data path equalization (DEQ) fast maintenance tau algorithm accumulation time. The delay is $2^{(\text{tau_fast_maint_time_preg} + 1)}$ rx_rd_clk_in_{15:0} periods.
25-16	TAU_FAST_MAINT_THRESH_PREG	R/W	1h	Receive data path equalization (DEQ) fast maintenance tau algorithm accumulation threshold.
15-0	RESERVED	R/W	X	

Table 11-681. Register Call Summary for DEQ_TAU_CTRL1_FAST_MAINT_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_TAU_CTRL1_FAST_MAINT_PREG_j Register \(Offset = 429Ch + formula\) \[reset = X\]: \[0\]](#)

11.227 DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j Register (Offset = 42A0h + formula) [reset = X]

DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j is shown in Figure 11-227 and described in Table 11-683.

Return to [Summary Table](#).

Receive data path equalization (DEQ) slow maintenance tau training control register 1.

Offset = 42A0h + (j * 400h); where j = 0h to 1h

Table 11-682.
DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 42A0h + formula
SERDES_16G1	0501 42A0h + formula
SERDES_16G2	0502 42A0h + formula
SERDES_16G3	0503 42A0h + formula

Figure 11-227. DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				TAU_DELTAMAX_PREG			
R/W-X				R/W-1Ch			
23	22	21	20	19	18	17	16
RESERVED				TAU_DELTAMIN_PREG			
R/W-X				R/W-4h			
15	14	13	12	11	10	9	8
RESERVED	TAU_DISABLE_SLOW_MAINT_PREG	TAU_SLOW_MAINT_TIME_PREG				TAU_SLOW_MAINT_THRESH_PREG	
R/W-X	R/W-0h	R/W-Fh				R/W-40h	
7	6	5	4	3	2	1	0
TAU_SLOW_MAINT_THRESH_PREG							
R/W-40h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-683. DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	TAU_DELTAMAX_PREG	R/W	1Ch	Receive data path equalization (DEQ) tau algorithm maximum delta from EPI to DPI.
23-22	RESERVED	R/W	X	
21-16	TAU_DELTAMIN_PREG	R/W	4h	Receive data path equalization (DEQ) tau algorithm minimum delta from EPI to DPI.
15	RESERVED	R/W	X	
14	TAU_DISABLE_SLOW_MAINT_PREG	R/W	0h	Receive data path equalization (DEQ) slow maintenance tau algorithm active high disable. The tau algorithm will be skipped during calls from the data path equalization state machine when in the slow maintenance period.

Table 11-683. DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-10	TAU_SLOW_MAINT_TIME_PREG	R/W	Fh	Receive data path equalization (DEQ) slow maintenance tau algorithm accumulation time The delay is $2^{(\text{tau_slow_maint_time_preg} + 1)}$ rx_rd_clk_ln_{15:0} periods.
9-0	TAU_SLOW_MAINT_THRESHOLD_PREG	R/W	40h	Receive data path equalization (DEQ) slow maintenance tau algorithm accumulation threshold.

Table 11-684. Register Call Summary for DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_TAU_CTRL2_PREG__DEQ_TAU_CTRL1_SLOW_MAINT_PREG_j Register \(Offset = 42A0h + formula\) \[reset = X\]: \[0\]](#)

11.228 DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG_j Register (Offset = 42A4h + formula) [reset = X]

DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG_j is shown in Figure 11-228 and described in Table 11-686.

Return to [Summary Table](#).

DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG

Offset = 42A4h + (j * 400h); where j = 0h to 1h

Table 11-685. DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 42A4h + formula
SERDES_16G1	0501 42A4h + formula
SERDES_16G2	0502 42A4h + formula
SERDES_16G3	0503 42A4h + formula

Figure 11-228. DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				BLK_TAU_DELTAMAX_PREG			
R/W-X				R/W-Eh			
23	22	21	20	19	18	17	16
RESERVED				BLK_TAU_DELTAMIN_PREG			
R/W-X				R/W-2h			
15	14	13	12	11	10	9	8
TAU_MODE_PREG				RESERVED			
R/W-0h				R/W-X			
				MV_DPI_ACCUM_EQ_PREG			
				R/W-0h			
7	6	5	4	3	2	1	0
CONCURRENT_EPIOFFSET_PREG				TAU_EPIOFFSET_PREG			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-686. DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	BLK_TAU_DELTAMAX_PREG	R/W	Eh	Receive data path equalization (DEQ) tau algorithm's maximum delta from EPI to DPI used for block TAU acquisition and apparent center.
23-22	RESERVED	R/W	X	
21-16	BLK_TAU_DELTAMIN_PREG	R/W	2h	Receive data path equalization (DEQ) tau algorithm's minimum delta from EPI to DPI used for block TAU acquisition and apparent center.
15-14	TAU_MODE_PREG	R/W	0h	TAU mode register Mode 2'b00 Classic TAU 2'b01 Bumper TAU algorithm 2'b10 Block TAU algorithm 2'b11 Block TAU algorithm for acquisition, bumper TAU for maintenance
13-9	RESERVED	R/W	X	

**Table 11-686. DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
8	MV_DPI_ACCUM_EQ_PREG	R/W	0h	Move DPI to the left if (r_accum_a is equal to r_accum_b) and (r_delta is less than equal to tau_deltamin_preg) if this bit is set to 1'b1, else don't move DPI.
7-4	CONCURRENT_EPIOFFSET_PREG	R/W	0h	Receive data path equalization (DEQ) tau algorithm 4 bit signed offset for EPI used in concurrent, eyesurf, and rx margining.
3-0	TAU_EPIOFFSET_PREG	R/W	0h	Receive data path equalization (DEQ) tau algorithm 4 bit signed offset for EPI used tau operations.

Table 11-687. Register Call Summary for DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_BLK_TAU_DELTA_PREG__DEQ_TAU_CTRL3_PREG_j Register \(Offset = 42A4h + formula\) \[reset = X\]: \[0\]](#)

11.229 DEQ_OPENEYE_CTRL_PREG_j Register (Offset = 42B0h + formula) [reset = X]

DEQ_OPENEYE_CTRL_PREG_j is shown in Figure 11-229 and described in Table 11-689.

Return to [Summary Table](#).

Receive data path equalization (DEQ) open eye algorithms control register.

Offset = 42B0h + (j * 400h); where j = 0h to 1h

**Table 11-688. DEQ_OPENEYE_CTRL_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 42B0h + formula
SERDES_16G1	0501 42B0h + formula
SERDES_16G2	0502 42B0h + formula
SERDES_16G3	0503 42B0h + formula

Figure 11-229. DEQ_OPENEYE_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	OPENEYE_DATA TABLANKEN_P REG	OPENEYE_DISABLE_P REG	OPENEYE_TAU_SARCN TSEL_PREG		OPENEYE_TAU_PICNTSEL_PR EG		OPENEYE_GAIN_ITERC NT_PREG
R/W-X	R/W-1h	R/W-0h	R/W-2h		R/W-2h		R/W-3Fh
7	6	5	4	3	2	1	0
OPENEYE_GAIN_ITERC NT_PREG					OPENEYE_GAIN_TIME_P REG		
R/W-3Fh					R/W-5h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-689. DEQ_OPENEYE_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14	OPENEYE_DATA TABLANKEN_P REG	R/W	1h	Receive data path equalization (DEQ) open eye data blank active high enable. rx_rd_in_{15:0} data will be all zero until data path acquisition is complete when asserted.
13	OPENEYE_DISABLE_P REG	R/W	0h	Receive data path equalization (DEQ) open eye tau algorithm active high disable. The open eye tau algorithm will be skipped during calls from the data path equalization state machine.
12-11	OPENEYE_TAU_SARCN TSEL_PREG	R/W	2h	Receive data path equalization (DEQ) open eye tau algorithm SAR count selection. Number of SAR iterations 0 6 1 5 2 4 3 3

Table 11-689. DEQ_OPENEYE_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-9	OPENEYE_TAU_PICNTSEL_PREG	R/W	2h	Receive data path equalization (DEQ) open eye tau algorithm PI step count selection. Steps taken = $2^{(5-\text{openeye_tau_picntsel_preg})}$
8-3	OPENEYE_GAIN_ITERCNT_PREG	R/W	3Fh	Open eye gain iteration count
2-0	OPENEYE_GAIN_TIME_PREG	R/W	5h	Open eye gain accumulation time. The time is $2^{(\text{openeye_gain_time_preg}+1)}$ rx_rd_clk_ln_{15:0} periods.

Table 11-690. Register Call Summary for DEQ_OPENEYE_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_OPENEYE_CTRL_PREG_j Register \(Offset = 42B0h + formula\) \[reset = X\]: \[0\]](#)

11.230 DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PREG_j Register (Offset = 42C0h + formula) [reset = X]

DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PREG_j is shown in Figure 11-230 and described in Table 11-692.

Return to [Summary Table](#).

Receive data path equalization (DEQ) PI override register.

Offset = 42C0h + (j * 400h); where j = 0h to 1h

Table 11-691. DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 42C0h + formula
SERDES_16G1	0501 42C0h + formula
SERDES_16G2	0502 42C0h + formula
SERDES_16G3	0503 42C0h + formula

Figure 11-230. DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PICTRL_HIRES_PREG	PICTRL_STEPSIZE_PREG		PICTRL_SETTLE_PREG		
R/W-X		R/W-1h	R/W-0h		R/W-3h		
15	14	13	12	11	10	9	8
EPI_OVREN_P REG	EPI_OVR_PREG						
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
DPI_OVREN_P REG	DPI_OVR_PREG						
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-692. DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21	PICTRL_HIRES_PREG	R/W	1h	DPI and EPI high resolution enable: Interpolation steps per UI 0 32 1 64
20-19	PICTRL_STEPSIZE_PREG	R/W	0h	DPI and EPI step size selection. PI steps taken 00 2 01 4 10 6 11 8
18-16	PICTRL_SETTLE_PREG	R/W	3h	DPI and EPI control settling time. Note this value is in rx_rd_clk_ln_{15:0} clock periods.

**Table 11-692. DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15	EPI_OVREN_PREG	R/W	0h	EPI phase active high override enable. Note that rx_deq_clk clock must be active for this override to take affect. These clocks are active whenever the data path adaptation or maintenance is active.
14-8	EPI_OVR_PREG	R/W	0h	When epi_ovren_preg is asserted high, this value will override the data path EPI binary phase. Increasing binary values advance the output clock phase relative to the input.
7	DPI_OVREN_PREG	R/W	0h	DPI phase active high override enable. Note that rx_deq_clk clock must be active for this override to take affect. These clocks are active whenever the data path adaptation or maintenance is active.
6-0	DPI_OVR_PREG	R/W	0h	When dpi_ovren_preg is asserted high, this value will override the data path DPI binary phase. Increasing binary values advance the output clock phase relative to the input.

Table 11-693. Register Call Summary for DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_PICTRL_PREG__DEQ_PI_OVR_CTRL_PREG_j Register \(Offset = 42C0h + formula\) \[reset = X\]: \[0\]](#)

11.231 CPICAL_CAP_STARTCODE_MODE23_PREG__CPICAL_CTRL_PREG_j Register (Offset = 42D0h + formula) [reset = X]

CPICAL_CAP_STARTCODE_MODE23_PREG__CPICAL_CTRL_PREG_j is shown in Figure 11-231 and described in Table 11-695.

Return to [Summary Table](#).

CPI calibration control and status register.

Offset = 42D0h + (j * 400h); where j = 0h to 1h

Table 11-694.
CPICAL_CAP_STARTCODE_MODE23_PREG__CPICAL_CTRL_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 42D0h + formula
SERDES_16G1	0501 42D0h + formula
SERDES_16G2	0502 42D0h + formula
SERDES_16G3	0503 42D0h + formula

Figure 11-231. CPICAL_CAP_STARTCODE_MODE23_PREG__CPICAL_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	CPICAL_CAP_STARTCODE_MODE3_PREG						
R/W-X	R/W-27h						
23	22	21	20	19	18	17	16
RESERVED	CPICAL_CAP_STARTCODE_MODE2_PREG						
R/W-X	R/W-27h						
15	14	13	12	11	10	9	8
CPICAL_RUN_PREG	RESERVED			CPICAL_CLKB UFEN_OVRVAL _PREG	CPICAL_CLKB UFEN_OVRVAL _PREG	RESERVED	CPICAL_CALE N_FORCE_PR EG
R/W-0h	R/W-X			R/W-0h	R/W-0h	R/W-X	R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-695. CPICAL_CAP_STARTCODE_MODE23_PREG__CPICAL_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	CPICAL_CAP_STARTCODE_MODE3_PREG	R/W	27h	This value is used as the starting code for subsequent CPI calibrations (capacitor) when xcvr_standard_mode_in{15:0}[2:0] is 3'b011.
23	RESERVED	R/W	X	
22-16	CPICAL_CAP_STARTCODE_MODE2_PREG	R/W	27h	This value is used as the starting code for subsequent CPI calibrations(capacitor) when xcvr_standard_mode_in{15:0}[2:0] is 3'b010.
15	CPICAL_RUN_PREG	R/W	0h	CPI calibration manual initiation active high enable.
14-12	RESERVED	R/W	X	
11	CPICAL_CLKBUFEN_OVRVAL_PREG	R/W	0h	override enable for cpi cal clock buf enable

Table 11-695. CPICAL_CAP_STARTCODE_MODE23_PREG__CPICAL_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	CPICAL_CLKBUFEN_OVRVAL_PREG	R/W	0h	override value for cpi cal clock buf enable
9	RESERVED	R/W	X	
8	CPICAL_CALEN_FORCE_PREG	R/W	0h	CPI analog module calen force. Asserting this bit will force rxd_cpi_calen and rxd_creq_cpicalen high, thus placing the CPI injection loop in free-running mode.
7-0	RESERVED	R/W	X	

**Table 11-696. Register Call Summary for
CPICAL_CAP_STARTCODE_MODE23_PREG__CPICAL_CTRL_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPICAL_CAP_STARTCODE_MODE23_PREG__CPICAL_CTRL_PREG_j Register \(Offset = 42D0h + formula\) \[reset = X\]: \[0\]](#)

11.232 CPICAL_CAP_OVR_PREG__CPICAL_CAP_STARTCODE_MODE01_PREG_j Register (Offset = 42D4h + formula) [reset = X]

CPICAL_CAP_OVR_PREG__CPICAL_CAP_STARTCODE_MODE01_PREG_j is shown in Figure 11-232 and described in Table 11-698.

Return to [Summary Table](#).

CPI calibration (capacitor) starting code register for xcvr_standard_mode 0 and 1.

Offset = 42D4h + (j * 400h); where j = 0h to 1h

Table 11-697.
CPICAL_CAP_OVR_PREG__CPICAL_CAP_STARTCODE_MODE01_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 42D4h + formula
SERDES_16G1	0501 42D4h + formula
SERDES_16G2	0502 42D4h + formula
SERDES_16G3	0503 42D4h + formula

Figure 11-232. CPICAL_CAP_OVR_PREG__CPICAL_CAP_STARTCODE_MODE01_PREG_j Register

31	30	29	28	27	26	25	24
CPICAL_CAP_OVREN_PREG	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED	CPICAL_CAP_OVRVAL_PREG						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	CPICAL_CAP_STARTCODE_MODE1_PREG						
R/W-X	R/W-27h						
7	6	5	4	3	2	1	0
RESERVED	CPICAL_CAP_STARTCODE_MODE0_PREG						
R/W-X	R/W-27h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-698. CPICAL_CAP_OVR_PREG__CPICAL_CAP_STARTCODE_MODE01_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CPICAL_CAP_OVREN_PREG	R/W	0h	CPI calibration (capacitor) override active high enable.
30-23	RESERVED	R/W	X	
22-16	CPICAL_CAP_OVRVAL_PREG	R/W	0h	When cpical_cap_ovren_preg is asserted high, this value is used by the CPI rather than the calibration engine result.
15	RESERVED	R/W	X	
14-8	CPICAL_CAP_STARTCODE_MODE1_PREG	R/W	27h	This value is used as the starting code for subsequent CPI calibrations(capacitor) when xcvr_standard_mode_ln{15:0}[2:0] is 3'b001.
7	RESERVED	R/W	X	

Table 11-698. CPICAL_CAP_OVR_PREG__CPICAL_CAP_STARTCODE_MODE01_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	CPICAL_CAP_STARTCODE_MODE0_PREG	R/W	27h	This value is used as the starting code for subsequent CPI calibrations(capacitor) when xcvr_standard_mode_ln{15:0}[2:0] is 3'b000.

Table 11-699. Register Call Summary for CPICAL_CAP_OVR_PREG__CPICAL_CAP_STARTCODE_MODE01_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPICAL_CAP_OVR_PREG__CPICAL_CAP_STARTCODE_MODE01_PREG_j Register \(Offset = 42D4h + formula\) \[reset = X\]: \[0\]](#)

11.233 CPICAL_CAP_ITERTMR_PREG__CPICAL_CAP_INITTMR_PREG_j Register (Offset = 42D8h + formula) [reset = X]

CPICAL_CAP_ITERTMR_PREG__CPICAL_CAP_INITTMR_PREG_j is shown in Figure 11-233 and described in Table 11-701.

Return to [Summary Table](#).

CPI calibration(capacitor) initial delay register.

Offset = 42D8h + (j * 400h); where j = 0h to 1h

Table 11-700.
CPICAL_CAP_ITERTMR_PREG__CPICAL_CAP_INITTMR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 42D8h + formula
SERDES_16G1	0501 42D8h + formula
SERDES_16G2	0502 42D8h + formula
SERDES_16G3	0503 42D8h + formula

Figure 11-233. CPICAL_CAP_ITERTMR_PREG__CPICAL_CAP_INITTMR_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPICAL_CAP_ITERTMR_PREG											
R/W-X				R/W-80h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CPICAL_CAP_INITTMR_PREG											
R/W-X				R/W-2EEh											

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-701. CPICAL_CAP_ITERTMR_PREG__CPICAL_CAP_INITTMR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CPICAL_CAP_ITERTMR_PREG	R/W	80h	CPI calibration(capacitor) iteration wait timer to allow the analog circuits to settle to the new frequency after a calibration code change. Note this value is in ln_pllclk_fullrt clock periods. Note the actual wait time is cpical_cap_ittertmr_preg + 1 clock periods.
15-12	RESERVED	R/W	X	
11-0	CPICAL_CAP_INITTMR_PREG	R/W	2EEh	CPI calibration(capacitor) initial wait timer to allow the analog circuits to settle on initiation of the calibration sequence. Note this value is in ln_pllclk_fullrt clock periods.

**Table 11-702. Register Call Summary for
CPICAL_CAP_ITERTMR_PREG__CPICAL_CAP_INITTMR_PREG_j**

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] CPICAL_CAP_ITERTMR_PREG__CPICAL_CAP_INITTMR_PREG_j Register (Offset = 42D8h + formula) [reset = X]: [0]

11.234 CPICAL_TMRVAL_MODE2_PREG__CPICAL_TMRVAL_MODE3_PREG_j Register (Offset = 42DCh + formula) [reset = X]

CPICAL_TMRVAL_MODE2_PREG__CPICAL_TMRVAL_MODE3_PREG_j is shown in Figure 11-234 and described in Table 11-704.

Return to [Summary Table](#).

CPI calibration mode3 evaluation time register

Offset = 42DCh + (j * 400h); where j = 0h to 1h

Table 11-703.
CPICAL_TMRVAL_MODE2_PREG__CPICAL_TMRVAL_MODE3_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 42DCh + formula
SERDES_16G1	0501 42DCh + formula
SERDES_16G2	0502 42DCh + formula
SERDES_16G3	0503 42DCh + formula

Figure 11-234. CPICAL_TMRVAL_MODE2_PREG__CPICAL_TMRVAL_MODE3_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPICAL_TMRVAL_MODE2_PREG											
R/W-X				R/W-800h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CPICAL_TMRVAL_MODE3_PREG											
R/W-X				R/W-400h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-704. CPICAL_TMRVAL_MODE2_PREG__CPICAL_TMRVAL_MODE3_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-16	CPICAL_TMRVAL_MODE2_PREG	R/W	800h	This value sets the Lane Standards Decoder frequency evaluation time. Power of 2 scaling is applied in the Lane Standards Decoder based on xcvr_standard_mode_ln_{15:0}. Note this value is in ln_pllclk_fullrt clock periods.
15-13	RESERVED	R/W	X	
12-0	CPICAL_TMRVAL_MODE3_PREG	R/W	400h	This value sets the Lane Standards Decoder frequency evaluation time. Power of 2 scaling is applied in the Lane Standards Decoder based on xcvr_standard_mode_ln_{15:0}. Note this value is in ln_pllclk_fullrt clock periods.

Table 11-705. Register Call Summary for
CPICAL_TMRVAL_MODE2_PREG__CPICAL_TMRVAL_MODE3_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPICAL_TMRVAL_MODE2_PREG__CPICAL_TMRVAL_MODE3_PREG_j Register \(Offset = 42DCh + formula\) \[reset = X\]: \[0\]](#)

11.235 CPICAL_TMRVAL_MODE0_PREG__CPICAL_TMRVAL_MODE1_PREG_j Register (Offset = 42E0h + formula) [reset = X]

CPICAL_TMRVAL_MODE0_PREG__CPICAL_TMRVAL_MODE1_PREG_j is shown in Figure 11-235 and described in Table 11-707.

Return to [Summary Table](#).

CPI calibration mode1 evaluation time register

Offset = 42E0h + (j * 400h); where j = 0h to 1h

Table 11-706.
CPICAL_TMRVAL_MODE0_PREG__CPICAL_TMRVAL_MODE1_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 42E0h + formula
SERDES_16G1	0501 42E0h + formula
SERDES_16G2	0502 42E0h + formula
SERDES_16G3	0503 42E0h + formula

Figure 11-235. CPICAL_TMRVAL_MODE0_PREG__CPICAL_TMRVAL_MODE1_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPICAL_TMRVAL_MODE0_PREG											
R/W-X				R/W-CC0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CPICAL_TMRVAL_MODE1_PREG											
R/W-X				R/W-660h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-707. CPICAL_TMRVAL_MODE0_PREG__CPICAL_TMRVAL_MODE1_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-16	CPICAL_TMRVAL_MODE0_PREG	R/W	CC0h	This value sets the Lane Standards Decoder frequency evaluation time. Power of 2 scaling is applied in the Lane Standards Decoder based on xcvr_standard_mode_ln_{15:0}. Note this value is in ln_pllclk_fullrt clock periods.
15-13	RESERVED	R/W	X	
12-0	CPICAL_TMRVAL_MODE1_PREG	R/W	660h	This value sets the Lane Standards Decoder frequency evaluation time. Power of 2 scaling is applied in the Lane Standards Decoder based on xcvr_standard_mode_ln_{15:0}. Note this value is in ln_pllclk_fullrt clock periods.

Table 11-708. Register Call Summary for
CPICAL_TMRVAL_MODE0_PREG__CPICAL_TMRVAL_MODE1_PREG_j

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] CPICAL_TMRVAL_MODE0_PREG__CPICAL_TMRVAL_MODE1_PREG_j Register (Offset = 42E0h + formula) [reset = X]: [0]

11.236 CPICAL_PICNT_MODE2_PREG__CPICAL_PICNT_MODE3_PREG_j Register (Offset = 42E4h + formula) [reset = X]

CPICAL_PICNT_MODE2_PREG__CPICAL_PICNT_MODE3_PREG_j is shown in Figure 11-236 and described in Table 11-710.

Return to [Summary Table](#).

CPI calibration PI clock cnt, mode 3 register.

Offset = 42E4h + (j * 400h); where j = 0h to 1h

Table 11-709.

CPICAL_PICNT_MODE2_PREG__CPICAL_PICNT_MODE3_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 42E4h + formula
SERDES_16G1	0501 42E4h + formula
SERDES_16G2	0502 42E4h + formula
SERDES_16G3	0503 42E4h + formula

Figure 11-236. CPICAL_PICNT_MODE2_PREG__CPICAL_PICNT_MODE3_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPICAL_PICNT_MODE2_PREG											
R/W-X				R/W-1FFh											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CPICAL_PICNT_MODE3_PREG											
R/W-X				R/W-1FFh											

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-710. CPICAL_PICNT_MODE2_PREG__CPICAL_PICNT_MODE3_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CPICAL_PICNT_MODE2_PREG	R/W	1FFh	This value sets the Lane Standards Decoder PI clock counter expected value when xcvr_standard_mode_ln{15:0}[2:0] is 3'b010.
15-12	RESERVED	R/W	X	
11-0	CPICAL_PICNT_MODE3_PREG	R/W	1FFh	This value sets the Lane Standards Decoder PI clock counter expected value when xcvr_standard_mode_ln{15:0}[2:0] is 3'b011.

Table 11-711. Register Call Summary for CPICAL_PICNT_MODE2_PREG__CPICAL_PICNT_MODE3_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPICAL_PICNT_MODE2_PREG__CPICAL_PICNT_MODE3_PREG_j Register \(Offset = 42E4h + formula\) \[reset = X\]: \[0\]](#)

11.237 CPICAL_PICNT_MODE0_PREG__CPICAL_PICNT_MODE1_PREG_j Register (Offset = 42E8h + formula) [reset = X]

CPICAL_PICNT_MODE0_PREG__CPICAL_PICNT_MODE1_PREG_j is shown in Figure 11-237 and described in Table 11-713.

Return to [Summary Table](#).

CPI calibration PI clock cnt, mode 1 register.

Offset = 42E8h + (j * 400h); where j = 0h to 1h

Table 11-712.
CPICAL_PICNT_MODE0_PREG__CPICAL_PICNT_MODE1_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 42E8h + formula
SERDES_16G1	0501 42E8h + formula
SERDES_16G2	0502 42E8h + formula
SERDES_16G3	0503 42E8h + formula

Figure 11-237. CPICAL_PICNT_MODE0_PREG__CPICAL_PICNT_MODE1_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CPICAL_PICNT_MODE0_PREG											
R/W-X				R/W-1FDh											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CPICAL_PICNT_MODE1_PREG											
R/W-X				R/W-1FDh											

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-713. CPICAL_PICNT_MODE0_PREG__CPICAL_PICNT_MODE1_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CPICAL_PICNT_MODE0_PREG	R/W	1FDh	This value sets the Lane Standards Decoder PI clock counter expected value when xcvr_standard_mode_ln{15:0}[2:0] is 3'b000.
15-12	RESERVED	R/W	X	
11-0	CPICAL_PICNT_MODE1_PREG	R/W	1FDh	This value sets the Lane Standards Decoder PI clock counter expected value when xcvr_standard_mode_ln{15:0}[2:0] is 3'b001.

Table 11-714. Register Call Summary for CPICAL_PICNT_MODE0_PREG__CPICAL_PICNT_MODE1_PREG_j

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] CPICAL_PICNT_MODE0_PREG__CPICAL_PICNT_MODE1_PREG_j Register (Offset = 42E8h + formula) [reset = X]: [0]

11.238 CPICAL_STATUS_PREG_j Register (Offset = 42ECh + formula) [reset = X]

CPICAL_STATUS_PREG_j is shown in Figure 11-238 and described in Table 11-716.

Return to [Summary Table](#).

Fine PI calibration control and status register

Offset = 42ECh + (j * 400h); where j = 0h to 1h

Table 11-715. CPICAL_STATUS_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 42ECh + formula
SERDES_16G1	0501 42ECh + formula
SERDES_16G2	0502 42ECh + formula
SERDES_16G3	0503 42ECh + formula

Figure 11-238. CPICAL_STATUS_PREG_j Register

31	30	29	28	27	26	25	24
CPICAL_RES_CODE							
R-19h							
23	22	21	20	19	18	17	16
CPICAL_CAP_CODE							CPICAL_DONE
R-27h							R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							
R-X							

LEGEND: R = Read Only; -n = value after reset

Table 11-716. CPICAL_STATUS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CPICAL_RES_CODE	R	19h	CPI calibration resistor code. Note: Only valid once A0 power state has been acknowledged or, if rerunning through the cpical_run_preg, once cpical_done has asserted.
23-17	CPICAL_CAP_CODE	R	27h	CPI calibration capacitor code. Note: Only valid once A0 power state has been acknowledged or, if rerunning through the cpical_run_preg, once cpical_done has asserted.
16	CPICAL_DONE	R	0h	CPI calibration active high complete flag. This done flag will deassert once the auto calibration is complete, thus it may not be observed high in normal operation. When using the cpical_run_preg to manually re-run the calibration, this flag may be polled to observe it transitions high, at which point the re-calibration is complete and the cpical_run_preg may be deasserted.
15-0	RESERVED	R	X	

Table 11-717. Register Call Summary for CPICAL_STATUS_PREG_j

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] CPICAL_STATUS_PREG_j Register (Offset = 42ECh + formula) [reset = X]: [0]

11.239 CPICAL_OFFSET_PREG_j Register (Offset = 42F0h + formula) [reset = X]

CPICAL_OFFSET_PREG_j is shown in Figure 11-239 and described in Table 11-719.

Return to [Summary Table](#).

CPI calibration offset register(resistor and capacitor)

Offset = 42F0h + (j * 400h); where j = 0h to 1h

Table 11-718. CPICAL_OFFSET_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 42F0h + formula
SERDES_16G1	0501 42F0h + formula
SERDES_16G2	0502 42F0h + formula
SERDES_16G3	0503 42F0h + formula

Figure 11-239. CPICAL_OFFSET_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CPICAL_RES_OFFSET_PREG					RESERVED		
R/W-0h					R/W-X		
7	6	5	4	3	2	1	0
RESERVED		CPICAL_CAP_OFFSET_WR_TOGGLE_PREG		CPICAL_CAP_OFFSET_PREG			
R/W-X		W-0h		R/W-0h			

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-719. CPICAL_OFFSET_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-11	CPICAL_RES_OFFSET_PREG	R/W	0h	Twos compliment offset to be added to the calibrated course code sent to the CPI .
10-6	RESERVED	R/W	X	
5	CPICAL_CAP_OFFSET_WR_TOGGLE_PREG	W	0h	Cal (cap)Offset write toggle bit
4-0	CPICAL_CAP_OFFSET_PREG	R/W	0h	Twos compliment offset to be added to the calibrated course code sent to the CPI.

Table 11-720. Register Call Summary for CPICAL_OFFSET_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPICAL_OFFSET_PREG_j Register \(Offset = 42F0h + formula\) \[reset = X\]: \[0\]](#)

11.240 CPI_OUTBUF_RATESEL_PREG_j Register (Offset = 42F8h + formula) [reset = X]

CPI_OUTBUF_RATESEL_PREG_j is shown in Figure 11-240 and described in Table 11-722.

Return to [Summary Table](#).

CPI output buffers BW control

Offset = 42F8h + (j * 400h); where j = 0h to 1h

**Table 11-721. CPI_OUTBUF_RATESEL_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 42F8h + formula
SERDES_16G1	0501 42F8h + formula
SERDES_16G2	0502 42F8h + formula
SERDES_16G3	0503 42F8h + formula

Figure 11-240. CPI_OUTBUF_RATESEL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
CPI_OUTBUF_RATESEL_MODE 3_PREG		CPI_OUTBUF_RATESEL_MODE 2_PREG		CPI_OUTBUF_RATESEL_MODE 1_PREG		CPI_OUTBUF_RATESEL_MODE 0_PREG	
R/W-3h		R/W-1h		R/W-1h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-722. CPI_OUTBUF_RATESEL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	CPI_OUTBUF_RATESEL_MODE3_PREG	R/W	3h	CPI output buffers BW control when xcvr_standard_mode_in{15:0} [2:0] is 3'b011. PI clock rate supported 00 625MHz to 1.56GHz 01 2.5GHz to 4GHz 10 5GHz to 6.25GHz 11 7.5GHz to 8GHz.
5-4	CPI_OUTBUF_RATESEL_MODE2_PREG	R/W	1h	CPI output buffers BW control when xcvr_standard_mode_in{15:0} [2:0] is 3'b010. PI clock rate supported 00 625MHz to 1.56GHz 01 2.5GHz to 4GHz 10 5GHz to 6.25GHz 11 7.5GHz to 8GHz.

Table 11-722. CPI_OUTBUF_RATESEL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	CPI_OUTBUF_RATESEL_MODE1_PREG	R/W	1h	CPI output buffers BW control when xcvr_standard_mode_in{15:0} [2:0] is 3'b001. PI clock rate supported 00 625MHz to 1.56GHz 01 2.5GHz to 4GHz 10 5GHz to 6.25GHz 11 7.5GHz to 8GHz.
1-0	CPI_OUTBUF_RATESEL_MODE0_PREG	R/W	0h	CPI output buffers BW control when xcvr_standard_mode_in{15:0} [2:0] is 3'b000. PI clock rate supported 00 625MHz to 1.56GHz 01 2.5GHz to 4GHz 10 5GHz to 6.25GHz 11 7.5GHz to 8GHz.

Table 11-723. Register Call Summary for CPI_OUTBUF_RATESEL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPI_OUTBUF_RATESEL_PREG_j Register \(Offset = 42F8h + formula\) \[reset = X\]: \[0\]](#)

11.241 CPI_TRIM_PREG__CPI_RESBIAS_BIN_PREG_j Register (Offset = 42FCh + formula) [reset = X]

CPI_TRIM_PREG__CPI_RESBIAS_BIN_PREG_j is shown in Figure 11-241 and described in Table 11-725.

Return to [Summary Table](#).

CPI res bias

Offset = 42FCh + (j * 400h); where j = 0h to 1h

Table 11-724.
CPI_TRIM_PREG__CPI_RESBIAS_BIN_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 42FCh + formula
SERDES_16G1	0501 42FCh + formula
SERDES_16G2	0502 42FCh + formula
SERDES_16G3	0503 42FCh + formula

Figure 11-241. CPI_TRIM_PREG__CPI_RESBIAS_BIN_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		CPI_IDIVTRIM_PREG			CPI_IPTATTRIM_PREG		
R/W-X		R/W-3h			R/W-5h		
15	14	13	12	11	10	9	8
RESERVED				CPI_RESBIAS_BIN_MODE3_PREG		CPI_RESBIAS_BIN_MODE2_PREG	
R/W-X				R/W-5h		R/W-4h	
7	6	5	4	3	2	1	0
CPI_RESBIAS_BIN_MODE2_PREG		CPI_RESBIAS_BIN_MODE1_PREG			CPI_RESBIAS_BIN_MODE0_PREG		
R/W-4h		R/W-4h			R/W-4h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-725. CPI_TRIM_PREG__CPI_RESBIAS_BIN_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-19	CPI_IDIVTRIM_PREG	R/W	3h	bias current magnitude controll
18-16	CPI_IPTATTRIM_PREG	R/W	5h	ptat percentage control
15-12	RESERVED	R/W	X	
11-9	CPI_RESBIAS_BIN_MOD E3_PREG	R/W	5h	CPI res bias when xcvr_standard_mode_in{15:0}[2:0] is 3'b011.
8-6	CPI_RESBIAS_BIN_MOD E2_PREG	R/W	4h	CPI res bias when xcvr_standard_mode_in{15:0}[2:0] is 3'b010.
5-3	CPI_RESBIAS_BIN_MOD E1_PREG	R/W	4h	CPI res bias when xcvr_standard_mode_in{15:0}[2:0] is 3'b001.
2-0	CPI_RESBIAS_BIN_MOD E0_PREG	R/W	4h	CPI res bias when xcvr_standard_mode_in{15:0}[2:0] is 3'b000.

Table 11-726. Register Call Summary for CPI_TRIM_PREG__CPI_RESBIAS_BIN_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPI_TRIM_PREG__CPI_RESBIAS_BIN_PREG_j Register \(Offset = 42FCh + formula\) \[reset = X\]: \[0\]](#)

11.242 CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PREG_j Register (Offset = 4300h + formula) [reset = X]

CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PREG_j is shown in Figure 11-242 and described in Table 11-728.

Return to [Summary Table](#).

CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PREG

Offset = 4300h + (j * 400h); where j = 0h to 1h

Table 11-727. CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4300h + formula
SERDES_16G1	0501 4300h + formula
SERDES_16G2	0502 4300h + formula
SERDES_16G3	0503 4300h + formula

Figure 11-242. CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				CPICAL_R2DEC_OVR_VAL_PREG			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
CPICAL_R2DEC_OVR_VAL_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
CPICAL_RDEC_OVR_EN_PREG	RESERVED			CPICAL_R1DEC_OVR_VAL_PREG			
R/W-0h	R/W-X			R/W-0h			
7	6	5	4	3	2	1	0
CPICAL_R1DEC_OVR_VAL_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-728. CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CPICAL_R2DEC_OVR_VAL_PREG	R/W	0h	Override value for cpi cal resistor decoder 2 output
15	CPICAL_RDEC_OVR_EN_PREG	R/W	0h	Override enable for cpi cal resistor decoder 1 /2 (r1dec and r2dec) outputs.
14-12	RESERVED	R/W	X	
11-0	CPICAL_R1DEC_OVR_VAL_PREG	R/W	0h	Override value for cpi cal resistor decoder 1 output

Table 11-729. Register Call Summary for CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPI_R2DEC_OVR_PREG__CPI_R1DEC_OVR_PREG_j Register \(Offset = 4300h + formula\) \[reset = X\]: \[0\]](#)

11.243 CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG_j Register (Offset = 4304h + formula) [reset = X]

CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG_j is shown in Figure 11-243 and described in Table 11-731.

Return to [Summary Table](#).

CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG

Offset = 4304h + (j * 400h); where j = 0h to 1h

Table 11-730.
CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4304h + formula
SERDES_16G1	0501 4304h + formula
SERDES_16G2	0502 4304h + formula
SERDES_16G3	0503 4304h + formula

Figure 11-243. CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG_j Register

31	30	29	28	27	26	25	24
CPICAL_RES_STARTCODE_MODE3_PREG							
R/W-32h							
23	22	21	20	19	18	17	16
CPICAL_RES_STARTCODE_MODE2_PREG							
R/W-32h							
15	14	13	12	11	10	9	8
CPICAL_RES_INCR_PREG				CPICAL_RES_DECR_PREG			
R/W-4h				R/W-1h			
7	6	5	4	3	2	1	0
RESERVED				CPICAL_CAP_DECR_PREG			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-731. CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CPICAL_RES_STARTCODE_MODE3_PREG	R/W	32h	This value is used as the starting code for subsequent CPI calibrations (resistor) when xcvr_standard_mode_in{15:0}[2:0] is 3'b011.
23-16	CPICAL_RES_STARTCODE_MODE2_PREG	R/W	32h	This value is used as the starting code for subsequent CPI calibrations(resistor) when xcvr_standard_mode_in{15:0}[2:0] is 3'b010.
15-12	CPICAL_RES_INCR_PREG	R/W	4h	CPI calibration Resistor code steps up by this value while incrementing the code. This is for diagnostic purpose only. Should be fixed to 4'd4 for normal operation.
11-8	CPICAL_RES_DECR_PREG	R/W	1h	CPI calibration Resistor code steps down by this value while decrementing the code. This is for diagnostic purpose only. Should be fixed to 4'd1 for normal operation.

Table 11-731. CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	X	
3-0	CPICAL_CAP_DECR_PREG	R/W	1h	CPI calibration Capacitor code steps down by this value while decrementing the code. This is for diagnostic purpose only. Should be fixed to 4'd1 for normal operation.

Table 11-732. Register Call Summary for CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPICAL_RES_STARTCODE_MODE23_PREG__CPICAL_INCR_DECR_PREG_j Register \(Offset = 4304h + formula\) \[reset = X\]: \[0\]](#)

11.244 CPICAL_RES_INITTMR_PREG__CPICAL_RES_STARTCODE_MODE01_PREG_j Register (Offset = 4308h + formula) [reset = X]

CPICAL_RES_INITTMR_PREG__CPICAL_RES_STARTCODE_MODE01_PREG_j is shown in Figure 11-244 and described in Table 11-734.

Return to [Summary Table](#).

CPI calibration (resistor) starting code register for xcvr_standard_mode 0 and 1.

Offset = 4308h + (j * 400h); where j = 0h to 1h

Table 11-733.
CPICAL_RES_INITTMR_PREG__CPICAL_RES_STARTCODE_MODE01_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4308h + formula
SERDES_16G1	0501 4308h + formula
SERDES_16G2	0502 4308h + formula
SERDES_16G3	0503 4308h + formula

Figure 11-244. CPICAL_RES_INITTMR_PREG__CPICAL_RES_STARTCODE_MODE01_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				CPICAL_RES_INITTMR_PREG			
R/W-X				R/W-2EEh			
23	22	21	20	19	18	17	16
CPICAL_RES_INITTMR_PREG							
R/W-2EEh							
15	14	13	12	11	10	9	8
CPICAL_RES_STARTCODE_MODE1_PREG							
R/W-32h							
7	6	5	4	3	2	1	0
CPICAL_RES_STARTCODE_MODE0_PREG							
R/W-32h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-734. CPICAL_RES_INITTMR_PREG__CPICAL_RES_STARTCODE_MODE01_PREG_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	CPICAL_RES_INITTMR_PREG	R/W	2EEh	CPI calibration(resistor) initial wait timer to allow the analog circuits to settle on initiation of the calibration sequence. Note this value is in ln_pllclk_fullrt clock periods.
15-8	CPICAL_RES_STARTCODE_MODE1_PREG	R/W	32h	This value is used as the starting code for subsequent CPI calibrations (resistor) when xcvr_standard_mode_ln{15:0}[2:0] is 3'b0001
7-0	CPICAL_RES_STARTCODE_MODE0_PREG	R/W	32h	This value is used as the starting code for subsequent CPI calibrations(resistor) when xcvr_standard_mode_ln{15:0}[2:0] is 3'b0000.

**Table 11-735. Register Call Summary for
CPICAL_RES_INITTMR_PREG__CPICAL_RES_STARTCODE_MODE01_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [CPICAL_RES_INITTMR_PREG__CPICAL_RES_STARTCODE_MODE01_PREG_j Register \(Offset = 4308h + formula\) \[reset = X\]: \[0\]](#)

11.245 EPI_CTRL_PREG__CPICAL_RES_ITERTMR_PREG_j Register (Offset = 430Ch + formula) [reset = X]

EPI_CTRL_PREG__CPICAL_RES_ITERTMR_PREG_j is shown in Figure 11-245 and described in Table 11-737.

Return to [Summary Table](#).

CPI calibration(resistor)iteration delay register.

Offset = 430Ch + (j * 400h); where j = 0h to 1h

Table 11-736. EPI_CTRL_PREG__CPICAL_RES_ITERTMR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 430Ch + formula
SERDES_16G1	0501 430Ch + formula
SERDES_16G2	0502 430Ch + formula
SERDES_16G3	0503 430Ch + formula

Figure 11-245. EPI_CTRL_PREG__CPICAL_RES_ITERTMR_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						EPIDEC_EN_OVR_PREG	EPATHPWISO_EN_PREG
R/W-X						R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED				CPICAL_RES_ITERTMR_PREG			
R/W-X				R/W-80h			
7	6	5	4	3	2	1	0
CPICAL_RES_ITERTMR_PREG							
R/W-80h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-737. EPI_CTRL_PREG__CPICAL_RES_ITERTMR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17	EPIDEC_EN_OVR_PREG	R/W	1h	EPI IDDQ style PSC enable override: When asserted high, the rxda_epidec_en follows the rxda_epathpwiso_en such the EPI will turn off in A0 during the equalization maintenance wait period. When deasserted, rxda_epidec_en is driven from the associated PSC bit.
16	EPATHPWISO_EN_PREG	R/W	0h	EPI power island manual active high enable.
15-12	RESERVED	R/W	X	
11-0	CPICAL_RES_ITERTMR_PREG	R/W	80h	CPI calibration(resistor) iteration wait timer to allow the analog circuits to settle to the new frequency after a calibration code change. Note this value is in ln_pllclk_fullrt clock periods. Note the actual wait time is cpical_res_ittertmr_preg + 1 clock periods.

Table 11-738. Register Call Summary for EPI_CTRL_PREG__CPICAL_RES_ITERTMR_PREG_j

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] EPI_CTRL_PREG__CPICAL_RES_ITERTMR_PREG_j Register (Offset = 430Ch + formula) [reset = X]: [0]

11.246 LFPSFILT_MD_PREG_LFPSDET_SUPPORT_PREG_j Register (Offset = 4310h + formula) [reset = X]

LFPSFILT_MD_PREG_LFPSDET_SUPPORT_PREG_j is shown in Figure 11-246 and described in Table 11-740.

Return to [Summary Table](#).

LFPS Detector Support Register

Offset = 4310h + (j * 400h); where j = 0h to 1h

Table 11-739. LFPSFILT_MD_PREG_LFPSDET_SUPPORT_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4310h + formula
SERDES_16G1	0501 4310h + formula
SERDES_16G2	0502 4310h + formula
SERDES_16G3	0503 4310h + formula

Figure 11-246. LFPSFILT_MD_PREG_LFPSDET_SUPPORT_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED			LFPSFILT_MD_COUNT_PREG				
R/W-X			R/W-5h				
15	14	13	12	11	10	9	8
RESERVED			LFPSFILT_DISABLE_PULSE_NONE_MD_CHK_PREG	RESERVED		LFPSDET_OVR_EN_PREG	LFPSDET_OVR_VAL_PREG
R/W-X			R/W-0h	R/W-X		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED					LFPSDET_VTHRESH_PREG		
R/W-X					R/W-3h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-740. LFPSFILT_MD_PREG_LFPSDET_SUPPORT_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	LFPSFILT_MD_COUNT_PREG	R/W	5h	Minimum pulse distance counter value (MD): Specifies the minimum pulse distance for a valid LFPS sequence. MD usually represents the minimum number of cycles between two rising edges of the same type (i.e., high or low). MD is equal to lfpsfilt_md_count_preg + 2. Note that MD is usually set to a value that is greater than MP, unless it would be desired to ignore MD for debugging purposes. The minimum value for lfpsfilt_md_count_preg is 0 (MD = 2) and the maximum is 31 (MD = 33). A value of 5 thus requires 7 cycles between rising edges.
15-13	RESERVED	R/W	X	
12	LFPSFILT_DISABLE_PULSE_NONE_MD_CHK_PREG	R/W	0h	When asserted the MD check using pulse_none is disabled.

**Table 11-740. LFPSFILT_MD_PREG__LFPSDET_SUPPORT_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
11-10	RESERVED	R/W	X	
9	LFPSDET_OVREN_PREG	R/W	0h	LFPS detect active high analog override enable.
8	LFPSDET_OVRVAL_PREG	R/W	0h	When lfpsdet_ovren_preg is asserted high, this value drives the filter rather than the analog circuit result.
7-3	RESERVED	R/W	X	
2-0	LFPSDET_VTHRESH_PREG	R/W	3h	Voltage threshold control. Nominal Trip Point (mVpp) 3'b111 153 3'b110 134 3'b101 115 3'b100 96 3'b011 78 3'b010 59 3'b001 40 3'b000 21

Table 11-741. Register Call Summary for LFPSFILT_MD_PREG__LFPSDET_SUPPORT_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LFPSFILT_MD_PREG__LFPSDET_SUPPORT_PREG_j Register \(Offset = 4310h + formula\) \[reset = X\]: \[0\]](#)

11.247 LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j Register (Offset = 4314h + formula) [reset = X]

LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j is shown in Figure 11-247 and described in Table 11-743.

Return to [Summary Table](#).

LFPS Detection Filter No Signal Counter Register

Offset = 4314h + (j * 400h); where j = 0h to 1h

Table 11-742.
LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4314h + formula
SERDES_16G1	0501 4314h + formula
SERDES_16G2	0502 4314h + formula
SERDES_16G3	0503 4314h + formula

Figure 11-247. LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				LFPSFILT_RD_COUNT_PREG			
R/W-X				R/W-7h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				LFPSFILT_NS_COUNT_PREG			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-743. LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	

Table 11-743. LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	LFPSFILT_RD_COUNT_P REG	R/W	7h	<p>Ramp down counter value (RD):</p> <p>Specifies the number of clock cycles that are used in the LFPS detect ramp down process.</p> <p>To reduce LFPS distortion, RD should correspond to MD-1.</p> <p>RD is equal to lfpsfilt_rd_count_preg, which means that lfpsfilt_rd_count_preg should correspond to lfpsfilt_md_count_preg+1.</p> <p>The default value (7) is thus meant to make the detected output 1 cycle longer for normal cases, to compensate for analog distortion in the comparator and samplers.</p> <p>It is still possible to get a detected output smaller than the analog duration of the LFPS signal, if the beginning of the LFPS signal is truncated in such a way that it prevents its immediate detection due to failure of MP or MD, or if long no-signal gaps appear at its beginning or at its end.</p> <p>Note that the actual ramp down time starts on the first cycle without a pulse_high or pulse_low signal.</p> <p>Ramp down also assumes that the illegal pattern happened at the very end of the faulty cycle, favoring the</p>
15-4	RESERVED	R/W	X	
3-0	LFPSFILT_NS_COUNT_P REG	R/W	0h	<p>No signal counter value (NS):</p> <p>Specifies the number of clock cycles where pulse_high and pulse_low are inactive before declaring no signal.</p> <p>NS is equal to lfpsfilt_ns_count_preg + 1.</p> <p>The minimum value for lfpsfilt_ns_count_preg is -1 (4'b1111, 0xF, NS = 0) and the maximum is +14 (4'b1110, NS = 15).</p> <p>The minimum value of -1 (0xF, NS = 0) allows no cycle.</p>

Table 11-744. Register Call Summary for LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LFPSFILT_RD_PREG__LFPSFILT_NS_PREG_j Register \(Offset = 4314h + formula\) \[reset = X\]: \[0\]](#)

11.248 LFPSFILT_MP_PREG_j Register (Offset = 4318h + formula) [reset = X]

LFPSFILT_MP_PREG_j is shown in Figure 11-248 and described in Table 11-746.

Return to [Summary Table](#).

LFPS Detection Filter Minimum Pulse Duration Counter Register

Offset = 4318h + (j * 400h); where j = 0h to 1h

Table 11-745. LFPSFILT_MP_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4318h + formula
SERDES_16G1	0501 4318h + formula
SERDES_16G2	0502 4318h + formula
SERDES_16G3	0503 4318h + formula

Figure 11-248. LFPSFILT_MP_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					LFPSFILT_MP_COUNT_PREG		
R/W-X					R/W-7h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-746. LFPSFILT_MP_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	LFPSFILT_MP_COUNT_P REG	R/W	7h	<p>Minimum pulse duration (MP): Specifies the minimum number of clock cycles required for a given LFPS pulse to be driven active to be considered part of a valid LFPS burst.</p> <p>MP is equal to lfpsfilt_mp_count_preg + 2.</p> <p>The minimum value for lfpsfilt_mp_count_preg is -1 (0x7, MP = 1), while the maximum is +6 (0x6, MP = 8).</p> <p>Note that MP is usually set to a smaller value than MD.</p> <p>Note that when MP=1 (lfpsfilt_mp_count_preg = -1, i.e., 0x7), MP check is effectively disabled since all pulses will be accepted.</p>

Table 11-747. Register Call Summary for LFPSFILT_MP_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LFPSFILT_MP_PREG_j Register \(Offset = 4318h + formula\) \[reset = X\]: \[0\]](#)

11.249 SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PREG_j Register (Offset = 4320h + formula) [reset = X]

SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PREG_j is shown in Figure 11-249 and described in Table 11-749.

Return to [Summary Table](#).

Receive signal detection support register.

Offset = 4320h + (j * 400h); where j = 0h to 1h

Table 11-748. SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4320h + formula
SERDES_16G1	0501 4320h + formula
SERDES_16G2	0502 4320h + formula
SERDES_16G3	0503 4320h + formula

Figure 11-249. SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PREG_j Register

31	30	29	28	27	26	25	24
SDFILT_H2LSEL_PREG	SDFILT_H2L_DLY_TMR_PREG						
R/W-1h	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	SDFILT_H2L_FILTER_TMR_PREG						
R/W-X	R/W-Ch						
15	14	13	12	11	10	9	8
RESERVED	SIGDET_VTHRESH_PREG			RESERVED		SIGDET_OVREN_PREG	SIGDET_OVRVAL_PREG
R/W-X	R/W-6h			R/W-X		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED		SIGDET_STRESSPROT_PREG		RESERVED	SIGDET_BIASTRIM_PREG		
R/W-X		R/W-1h		R/W-X	R/W-3h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-749. SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDFILT_H2LSEL_PREG	R/W	1h	Receive signal detect high to low filter select value: Assertion of this bit selects the result of the high to low filter as the rx_signal_detect_in_{15:0} output. Otherwise the high to low filter is bypassed and the output of the low to high filter is used directly.
30-24	SDFILT_H2L_DLY_TMR_PREG	R/W	0h	Receive signal detect high to low filter delay timer value: Delays the assertion of the filter output to suppress time distortion of the output relative to the signal at the high-speed pins. Note this value is in cmn_sdosc_clk clock periods of nominally 2ns.
23	RESERVED	R/W	X	
22-16	SDFILT_H2L_FILTER_TMR_PREG	R/W	Ch	Receive signal detect high to low filter timer value: Used to remove glitches in raw analog signal detection result. Note this value is in cmn_sdosc_clk clock periods of nominally 2ns.
15	RESERVED	R/W	X	

**Table 11-749. SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
14-12	SIGDET_VTHRESH_PREG	R/W	6h	Receive signal detection voltage threshold binary encoded selection: At the 0dB setting below and a -12dB channel, 175mVppd is always detected and 65mVppd is never detected. Attenuation (dB) 3'b111 +2.43 3'b110 +1.19 3'b101 0 3'b 100 -1.6 3'b 011 -3.5 3'b 010 -6.0 3'b 001 -9.5 3'b 000 -15.5
11-10	RESERVED	R/W	X	
9	SIGDET_OVREN_PREG	R/W	0h	Receive signal detect active high analog override enable.
8	SIGDET_OVRVAL_PREG	R/W	0h	When sigdet_ovren_preg is asserted high, this value drives the filter rather than the analog circuit result.
7-6	RESERVED	R/W	X	
5-4	SIGDET_STRESSPROT_PREG	R/W	1h	Receive signal detection analog device protection binary encoded selection: Protection 2'b11 Highest :: 2'b00 Nominal
3	RESERVED	R/W	X	
2-0	SIGDET_BIASTRIM_PREG	R/W	3h	Receive signal detection bias current binary encoded trim: Bias current amplitude 3'b111 Lowest :: 3'b000 Highest

Table 11-750. Register Call Summary for SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDFILT_H2L_A_PREG__SIGDET_SUPPORT_PREG_j Register \(Offset = 4320h + formula\) \[reset = X\]: \[0\]](#)

11.250 SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j Register (Offset = 4324h + formula) [reset = X]

SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j is shown in Figure 11-250 and described in Table 11-752.

Return to [Summary Table](#).

Receive signal detection high to low filter control register B.

Offset = 4324h + (j * 400h); where j = 0h to 1h

Table 11-751.
SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4324h + formula
SERDES_16G1	0501 4324h + formula
SERDES_16G2	0502 4324h + formula
SERDES_16G3	0503 4324h + formula

Figure 11-250. SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j Register

31	30	29	28	27	26	25	24
SDFILT_L2HSEL_L_PREG	SDFILT_L2H_MIN_TMR_PREG						
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED	SDFILT_L2H_FILTER_TMR_PREG						
R/W-X				R/W-4h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	SDFILT_H2L_MIN_TMR_PREG						
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-752. SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDFILT_L2HSEL_PREG	R/W	0h	Receive signal detect low to high filter select value: Assertion of this bit selects the result of the low to high filter to be used in the rx_signal_detect generation, either directly if sdfilt_h2lssel_preg is low, or as the input to the high to low filter if sdfilt_h2lssel_preg is high. If this bit is low, the low to high filter is bypassed altogether.
30-24	SDFILT_L2H_MIN_TMR_PREG	R/W	0h	Receive signal detect low to high filter minimum timer value: Stretches the filter output assertions to a minimum time. Note this value is in cmn_sdosc_clk clock periods of nominally 2ns.
23	RESERVED	R/W	X	
22-16	SDFILT_L2H_FILTER_TMR_PREG	R/W	4h	Receive signal detect low to high filter timer value: Used to remove glitches in raw analog signal detection result. Note this value is in cmn_sdosc_clk clock periods of nominally 2ns.
15-7	RESERVED	R/W	X	

Table 11-752. SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	SDFILT_H2L_MIN_TMR_PREG	R/W	0h	Receive signal detect high to low filter minimum timer value: Stretches the filter output assertions to a minimum time. Note this value is in cmn_sdosc_clk clock periods of nominally 2ns.

Table 11-753. Register Call Summary for SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDFILT_L2H_PREG__SDFILT_H2L_B_PREG_j Register \(Offset = 4324h + formula\) \[reset = X\]: \[0\]](#)

11.251 SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j Register (Offset = 4328h + formula) [reset = X]

SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j is shown in [Figure 11-251](#) and described in [Table 11-755](#).

Return to [Summary Table](#).

Receive signal detection calibration control register.

Offset = 4328h + (j * 400h); where j = 0h to 1h

Table 11-754.
SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4328h + formula
SERDES_16G1	0501 4328h + formula
SERDES_16G2	0502 4328h + formula
SERDES_16G3	0503 4328h + formula

Figure 11-251. SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
SDCAL_OVREN_PREG	RESERVED						
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED				SDCAL_OVRVAL_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
SDCAL_RUN_PREG	SDCAL_DONE	SDCAL_NO_ANA_RESP	SDCAL_VALID	RESERVED			SDCAL_VALID_OVR_PREG
R/W-0h	R-0h	R-0h	R-0h	R/W-X			R/W-0h
7	6	5	4	3	2	1	0
RESERVED				SDCAL_CODE			
R/W-X				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-755. SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDCAL_OVREN_PREG	R/W	0h	Receive signal detect code active high override enable.
30-21	RESERVED	R/W	X	
20-16	SDCAL_OVRVAL_PREG	R/W	0h	When sdcal_ovren_preg is asserted high, this value overrides the internally signal detection calibration code from the calibration circuit.
15	SDCAL_RUN_PREG	R/W	0h	Receive signal detection calibration manual start signal: Note the user must write this bit from low to high to initiate a new calibration sequence.
14	SDCAL_DONE	R	0h	Receive signal detection calibration active high complete flag. Note this flag deasserts with the deassertion of either sdcal_run_preg or the Lane calibration sdcal_run.
13	SDCAL_NO_ANA_RESP	R	0h	Receive sigdet detection calibration no analog response flag.

Table 11-755. SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SDCAL_VALID	R	0h	Receive signal detection calibration has completed flag. Note this flag asserts with the completion of calibration and remains high until a link / macro reset or until a manual re-calibration is requested with sdcal_run_preg. After a manual recalibration completes, it will reassert.
11-9	RESERVED	R/W	X	
8	SDCAL_VALID_OVR_PREG	R/W	0h	Receive signal detection calibration has completed override. When asserted, forces the sdcal_valid flag high. This results in the signal detection filter not being gated off prior to calibration complete.
7-5	RESERVED	R/W	X	
4-0	SDCAL_CODE	R	0h	Receive signal detection calibration code. Note only valid once A0 power state has been acknowledged or, if rerunning through the sdcal_run_preg, once sdcal_done has asserted.

Table 11-756. Register Call Summary for SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDCAL_OVR_PREG__SDCAL_CTRL_PREG_j Register \(Offset = 4328h + formula\) \[reset = X\]: \[0\]](#)

11.252 SDCAL_TUNE_PREG__SDCAL_START_PREG_j Register (Offset = 432Ch + formula) [reset = X]

SDCAL_TUNE_PREG__SDCAL_START_PREG_j is shown in Figure 11-252 and described in Table 11-758.

Return to [Summary Table](#).

Receive signal detection calibration starting code register.

Offset = 432Ch + (j * 400h); where j = 0h to 1h

Table 11-757.
SDCAL_TUNE_PREG__SDCAL_START_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 432Ch + formula
SERDES_16G1	0501 432Ch + formula
SERDES_16G2	0502 432Ch + formula
SERDES_16G3	0503 432Ch + formula

Figure 11-252. SDCAL_TUNE_PREG__SDCAL_START_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				SDCAL_TUNE_PREG			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				SDCAL_START_PREG			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-758. SDCAL_TUNE_PREG__SDCAL_START_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	SDCAL_TUNE_PREG	R/W	0h	Receive signal detection mission mode amplitude threshold binary encoded selection. Threshold 5'b1_1111 Highest : 5'b0_0000 Lowest Note the threshold resolution is nominally 5mV per code. Note this function is deprecated. The signal detection amplitude is now set using sigdet_vthresh_preg[2:0].
15-5	RESERVED	R/W	X	
4-0	SDCAL_START_PREG	R/W	0h	Receive signal detect calibration start code when the calibration sequence begins.

Table 11-759. Register Call Summary for SDCAL_TUNE_PREG__SDCAL_START_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDCAL_TUNE_PREG__SDCAL_START_PREG_j Register \(Offset = 432Ch + formula\) \[reset = X\]: \[0\]](#)

11.253 SDCAL_ITER_PREG__SDCAL_INIT_PREG_j Register (Offset = 4330h + formula) [reset = X]

SDCAL_ITER_PREG__SDCAL_INIT_PREG_j is shown in Figure 11-253 and described in Table 11-761.

Return to [Summary Table](#).

Receive signal detection calibration initialization timer register.

Offset = 4330h + (j * 400h); where j = 0h to 1h

Table 11-760.
SDCAL_ITER_PREG__SDCAL_INIT_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4330h + formula
SERDES_16G1	0501 4330h + formula
SERDES_16G2	0502 4330h + formula
SERDES_16G3	0503 4330h + formula

Figure 11-253. SDCAL_ITER_PREG__SDCAL_INIT_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SDCAL_ITER_WAIT_PREG							
R/W-X								R/W-4h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SDCAL_INIT_WAIT_PREG							
R/W-X								R/W-12h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-761. SDCAL_ITER_PREG__SDCAL_INIT_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	SDCAL_ITER_WAIT_PREG	R/W	4h	Receive signal detect calibration iteration wait timer providing delay for settling between each offset adjustment level change. Note this value is in cmn_refclk clock periods. The delay is sdcal_iter_wait_preg + 1 cmn_refclk periods.
15-9	RESERVED	R/W	X	
8-0	SDCAL_INIT_WAIT_PREG	R/W	12h	Receive signal detect calibration initial wait timer providing a circuit settling period at the initiation of the calibration sequence. Note this value is in cmn_refclk clock periods. The delay is sdcal_init_wait_preg + 1 cmn_refclk periods.

Table 11-762. Register Call Summary for SDCAL_ITER_PREG__SDCAL_INIT_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SDCAL_ITER_PREG__SDCAL_INIT_PREG_j Register \(Offset = 4330h + formula\) \[reset = X\]: \[0\]](#)

11.254 RXTERM_ENABLE_PREG__RXTERM_BSCAN_PREG_j Register (Offset = 4338h + formula) [reset = X]

RXTERM_ENABLE_PREG__RXTERM_BSCAN_PREG_j is shown in Figure 11-254 and described in Table 11-764.

Return to [Summary Table](#).

Receiver termination boundary scan support register

Offset = 4338h + (j * 400h); where j = 0h to 1h

Table 11-763. RXTERM_ENABLE_PREG__RXTERM_BSCAN_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4338h + formula
SERDES_16G1	0501 4338h + formula
SERDES_16G2	0502 4338h + formula
SERDES_16G3	0503 4338h + formula

Figure 11-254. RXTERM_ENABLE_PREG__RXTERM_BSCAN_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED			RX_TERM_GN DRESSEL_PR EG	RESERVED		RXTERM_EN_ OVRVAL_PRE G	RXTERM_EN_ OVREN_PREG
R/W-X			R/W-1h	R/W-X		R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				RXTERM_BSCAN_RESCAL_PREG			
R/W-X				R/W-9h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-764. RXTERM_ENABLE_PREG__RXTERM_BSCAN_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20	RX_TERM_GNDRESSEL_PREG	R/W	1h	Receive termination configuration select. All termination resistors are grounded when asserted. Some resistors are differential between rx_p/m when deasserted. Mode 1'b0 Grounded/differential combination 1'b1 Grounded resistors
19-18	RESERVED	R/W	X	
17	RXTERM_EN_OVRVAL_PREG	R/W	0h	Receive termination enable override value
16	RXTERM_EN_OVREN_PREG	R/W	0h	Receive termination enable override enable
15-4	RESERVED	R/W	X	

**Table 11-764. RXTERM_ENABLE_PREG__RXTERM_BSCAN_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
3-0	RXTERM_BSCAN_RESCAL_PREG	R/W	9h	Receive termination resistor calibration level used in boundary scan operation.

Table 11-765. Register Call Summary for RXTERM_ENABLE_PREG__RXTERM_BSCAN_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RXTERM_ENABLE_PREG__RXTERM_BSCAN_PREG_j Register \(Offset = 4338h + formula\) \[reset = X\]: \[0\]](#)

11.255 RXBUFFER_RCDFECTRL_PREG__RXBUFFER_CTLECTRL_PREG_j Register (Offset = 433Ch + formula) [reset = X]

RXBUFFER_RCDFECTRL_PREG__RXBUFFER_CTLECTRL_PREG_j is shown in Figure 11-255 and described in Table 11-767.

Return to [Summary Table](#).

RX buffer CTLE control register

Offset = 433Ch + (j * 400h); where j = 0h to 1h

Table 11-766.
RXBUFFER_RCDFECTRL_PREG__RXBUFFER_CTLECTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 433Ch + formula
SERDES_16G1	0501 433Ch + formula
SERDES_16G2	0502 433Ch + formula
SERDES_16G3	0503 433Ch + formula

Figure 11-255. RXBUFFER_RCDFECTRL_PREG__RXBUFFER_CTLECTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	RXBUFFER_RCTRIMDFE_MODE3_PREG			RESERVED	RXBUFFER_RCTRIMDFE_MODE2_PREG		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	RXBUFFER_RCTRIMDFE_MODE1_PREG			RESERVED	RXBUFFER_RCTRIMDFE_MODE0_PREG		
R/W-X	R/W-0h			R/W-X	R/W-2h		
15	14	13	12	11	10	9	8
RESERVED	RXBUFFER_RCTRIMCTLE_DCBIASATTEN1_PREG			RESERVED	RXBUFFER_RCTRIMCTLE_DCBIASATTEN0_PREG		
R/W-X	R/W-0h			R/W-X	R/W-1h		
7	6	5	4	3	2	1	0
RESERVED	RXBUFFER_TRIMCTLE_DCBIASATTEN1_PREG			RESERVED	RXBUFFER_TRIMCTLE_DCBIASATTEN0_PREG		
R/W-X	R/W-0h			R/W-X	R/W-2h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-767. RXBUFFER_RCDFECTRL_PREG__RXBUFFER_CTLECTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	RXBUFFER_RCTRIMDFE_MODE3_PREG	R/W	0h	Trim for rxana_dfe path high frequency gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_rctrimdfef[3:0]: Thermometer Encoding 3'b000 4'b0000 3'b001 4'b0001 3'b010 4'b0011 3'b011 4'b0111 3'b100 4'b1111 3'b101 4'b1111 3'b110 4'b1111 3'b111 4'b1111
27	RESERVED	R/W	X	

Table 11-767. RXBUFFER_RCDFECTRL_PREG_RXBUFFER_CTLECTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-24	RXBUFFER_RCTRIMDFE_MODE2_PREG	R/W	0h	Trim for rxana_dfe path high frequency gain when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_rctrimdfe[3:0]: Thermometer Encoding 3'b000 4'b0000 3'b001 4'b0001 3'b010 4'b0011 3'b011 4'b0111 3'b100 4'b1111 3'b101 4'b1111 3'b110 4'b1111 3'b111 4'b1111
23	RESERVED	R/W	X	
22-20	RXBUFFER_RCTRIMDFE_MODE1_PREG	R/W	0h	Trim for rxana_dfe path high frequency gain when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_rctrimdfe[3:0]: Thermometer Encoding 3'b000 4'b0000 3'b001 4'b0001 3'b010 4'b0011 3'b011 4'b0111 3'b100 4'b1111 3'b101 4'b1111 3'b110 4'b1111 3'b111 4'b1111
19	RESERVED	R/W	X	
18-16	RXBUFFER_RCTRIMDFE_MODE0_PREG	R/W	2h	Trim for rxana_dfe path high frequency gain when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_rctrimdfe[3:0]: Thermometer Encoding 3'b000 4'b0000 3'b001 4'b0001 3'b010 4'b0011 3'b011 4'b0111 3'b100 4'b1111 3'b101 4'b1111 3'b110 4'b1111 3'b111 4'b1111
15	RESERVED	R/W	X	

Table 11-767. RXBUFFER_RCDFECTRL_PREG_RXBUFFER_CTLECTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	RXBUFFER_RCTRIMCTLE_DCBIASATTEN1_PREG	R/W	0h	Trim for rxana_ctleclk path high frequency gain when ctleclk_dcbiasatten is 1'b1. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_rctrimctle_dcbiasatten1[3:0]: Thermometer Encoding Gain 3'b000 4'b0000 Lowest 3'b001 4'b 0001 : 3'b010 4'b 0011 : 3'b011 4'b 0111 : 3'b100 4'b1111 Highest 3'b101 4'b1111 Highest 3'b110 4'b1111 Highest 3'b111 4'b1111 Highest
11	RESERVED	R/W	X	
10-8	RXBUFFER_RCTRIMCTLE_DCBIASATTEN0_PREG	R/W	1h	Trim for rxana_ctleclk path high frequency gain when ctleclk_dcbiasatten is 1'b0. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_rctrimctle_dcbiasatten0[3:0]: Thermometer Encoding Gain 3'b000 4'b0000 Lowest 3'b001 4'b 0001 : 3'b010 4'b 0011 : 3'b011 4'b 0111 : 3'b100 4'b1111 Highest 3'b101 4'b1111 Highest 3'b110 4'b1111 Highest 3'b111 4'b1111 Highest
7	RESERVED	R/W	X	
6-4	RXBUFFER_TRIMCTLE_DCBIASATTEN1_PREG	R/W	0h	Trim for rxana_ctleclk path DC gain when ctleclk_dcbiasatten is 1'b1. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_trimctle_dcbiasatten1[6:0]: Thermometer Encoding Gain 3'b000 7'b000_0000 Lowest 3'b001 7'b000_0001 : 3'b010 7'b000_0011 : 3'b011 7'b000_0111 : 3'b100 7'b000_1111 : 3'b101 7'b001_1111 : 3'b110 7'b011_1111 : 3'b111 7'b111_1111 Highest
3	RESERVED	R/W	X	

Table 11-767. RXBUFFER_RCDFECTRL_PREG__RXBUFFER_CTLECTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	RXBUFFER_TRIMCTLE_DCBIASATTEN0_PREG	R/W	2h	Trim for rxana_ctleclk path DC gain when ctleclk_dcbiasatten is 1'b0. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_trimctle_dcbiasatten0 [6:0]: Thermometer Encoding Gain 3'b000 7'b000_0000 Lowest 3'b001 7'b000_0001 : 3'b010 7'b000_0011 : 3'b011 7'b000_0111 : 3'b100 7'b000_1111 : 3'b101 7'b001_1111 : 3'b110 7'b011_1111 : 3'b111 7'b111_1111 Highest

Table 11-768. Register Call Summary for RXBUFFER_RCDFECTRL_PREG__RXBUFFER_CTLECTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RXBUFFER_RCDFECTRL_PREG__RXBUFFER_CTLECTRL_PREG_j Register \(Offset = 433Ch + formula\) \[reset = X\]: \[0\]](#)

11.256 RXBUFFER_DFECTRL_PREG_j Register (Offset = 4340h + formula) [reset = X]

RXBUFFER_DFECTRL_PREG_j is shown in Figure 11-256 and described in Table 11-770.

Return to [Summary Table](#).

RX buffer DFE control register

Offset = 4340h + (j * 400h); where j = 0h to 1h

**Table 11-769. RXBUFFER_DFECTRL_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4340h + formula
SERDES_16G1	0501 4340h + formula
SERDES_16G2	0502 4340h + formula
SERDES_16G3	0503 4340h + formula

Figure 11-256. RXBUFFER_DFECTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	RXBUFFER_TRIMDFE_MODE3_PREG			RESERVED	RXBUFFER_TRIMDFE_MODE2_PREG		
R/W-X	R/W-4h			R/W-X	R/W-2h		
7	6	5	4	3	2	1	0
RESERVED	RXBUFFER_TRIMDFE_MODE1_PREG			RESERVED	RXBUFFER_TRIMDFE_MODE0_PREG		
R/W-X	R/W-3h			R/W-X	R/W-3h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-770. RXBUFFER_DFECTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-12	RXBUFFER_TRIMDFE_M ODE3_PREG	R/W	4h	Trim for rxana_dfe path DC gain when xcvr_standard_mode_ln_{15:0}[2:0] is 3'b011. This binary value is thermometer encoded as follows before passing onto analog as rxda_rxbuffer_trimdfe[3:0]: Thermometer Encoding 3'b000 4'b0000 3'b001 4'b0001 3'b010 4'b0011 3'b011 4'b0111 3'b100 4'b1111 3'b101 4'b1111 3'b110 4'b1111 3'b111 4'b1111
11	RESERVED	R/W	X	

Table 11-770. RXBUFFER_DFECTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	RXBUFFER_TRIMDFE_M ODE2_PREG	R/W	2h	Trim for rxana_dfe path DC gain when xcvr_standard_mode_in_{15:0}[2:0] is 3'b010. This binary value is thermometer encoded as follows before passing onto analog as rxd_rxbuffer_trimdfe[3:0]: Thermometer Encoding 3'b000 4'b0000 3'b001 4'b0001 3'b010 4'b0011 3'b011 4'b0111 3'b100 4'b1111 3'b101 4'b1111 3'b110 4'b1111 3'b111 4'b1111
7	RESERVED	R/W	X	
6-4	RXBUFFER_TRIMDFE_M ODE1_PREG	R/W	3h	Trim for rxana_dfe path DC gain when xcvr_standard_mode_in_{15:0}[2:0] is 3'b001. This binary value is thermometer encoded as follows before passing onto analog as rxd_rxbuffer_trimdfe[3:0]: Thermometer Encoding 3'b000 4'b0000 3'b001 4'b0001 3'b010 4'b0011 3'b011 4'b0111 3'b100 4'b1111 3'b101 4'b1111 3'b110 4'b1111 3'b111 4'b1111
3	RESERVED	R/W	X	
2-0	RXBUFFER_TRIMDFE_M ODE0_PREG	R/W	3h	Trim for rxana_dfe path DC gain when xcvr_standard_mode_in_{15:0}[2:0] is 3'b000. This binary value is thermometer encoded as follows before passing onto analog as rxd_rxbuffer_trimdfe[3:0]: Thermometer Encoding 3'b000 4'b0000 3'b001 4'b0001 3'b010 4'b0011 3'b011 4'b0111 3'b100 4'b1111 3'b101 4'b1111 3'b110 4'b1111 3'b111 4'b1111

Table 11-771. Register Call Summary for RXBUFFER_DFECTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RXBUFFER_DFECTRL_PREG_j Register \(Offset = 4340h + formula\) \[reset = X\]: \[0\]](#)

11.257 DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_CTRL_PREG_j Register (Offset = 4348h + formula) [reset = X]

DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_CTRL_PREG_j is shown in [Figure 11-257](#) and described in [Table 11-773](#).

Return to [Summary Table](#).

Receive data path eye surf control register.

Offset = 4348h + (j * 400h); where j = 0h to 1h

**Table 11-772. DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_CTRL_PREG_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 4348h + formula
SERDES_16G1	0501 4348h + formula
SERDES_16G2	0502 4348h + formula
SERDES_16G3	0503 4348h + formula

Figure 11-257. DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	EYESURF_ECMPVTH_PREG						
R/W-X	R/W-64h						
15	14	13	12	11	10	9	8
EYESURF_TIME_PREG				EYESURF_VAL ID	EYESURF_STA RT_PREG	EYESURF_MO DE_PREG	RESERVED
R/W-Fh				R-0h	R/W-0h	R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED	EYESURF_EPIADJ_PREG						
R/W-X	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-773. DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	EYESURF_ECMPVTH_P REG	R/W	64h	Receive data path eye surf comparator voltage binary encoded threshold selection. Each step is nominally 3mV.
15-12	EYESURF_TIME_PREG	R/W	Fh	Receive data path eye surf accumulation time. The delay is 2(eyesurf_time_preg+ 1) rx_rd_clk_In_{15:0} periods. Note: For use of eye surf with Receiver Margining, this range of this field should be from 4'hB to 4'hF. When using the eye surf feature standalone, the full range from 4'h0 to 4'hF may be used.
11	EYESURF_VALID	R	0h	Receive data path eye surf accumulation period active high complete flag. At the assertion of this signal, eyesurf_accuma and eyesurf_accumb are valid.
10	EYESURF_START_PREG	R/W	0h	Receive data path eye surf active high start sequence enable

Table 11-773. DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EYESURF_MODE_PREG	R/W	0h	Receive data path eye surf active high mode enable.
8-7	RESERVED	R/W	X	
6-0	EYESURF_EPIADJ_PREG	R/W	0h	Receive data path eye surf EPI position shift control. This is a signed value representing the binary number of PI steps to adjust from the current EPI position, maintained with the DPI position nominally in the center of the eye through tau algorithms. Note the EPI is returned to its original position once eyesurf_valid asserts.

Table 11-774. Register Call Summary for DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_EYESURF_VTH_PREG__DEQ_EYESURF_CTRL_PREG_j Register \(Offset = 4348h + formula\) \[reset = X\]: \[0\]](#)

11.258 DEQ_EYESURF_ACCUMB__DEQ_EYESURF_ACCUMA_j Register (Offset = 434Ch + formula) [reset = X]

DEQ_EYESURF_ACCUMB__DEQ_EYESURF_ACCUMA_j is shown in [Figure 11-258](#) and described in [Table 11-776](#).

Return to [Summary Table](#).

Receive data path eye surf accumulator A status register.

Offset = 434Ch + (j * 400h); where j = 0h to 1h

Table 11-775. DEQ_EYESURF_ACCUMB__DEQ_EYESURF_ACCUMA_j Instances

Instance	Physical Address
SERDES_16G0	0500 434Ch + formula
SERDES_16G1	0501 434Ch + formula
SERDES_16G2	0502 434Ch + formula
SERDES_16G3	0503 434Ch + formula

Figure 11-258. DEQ_EYESURF_ACCUMB__DEQ_EYESURF_ACCUMA_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						EYESURF_ACCUMB									
R-X						R-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						EYESURF_ACCUMA									
R-X						R-0h									

LEGEND: R = Read Only; -n = value after reset

Table 11-776. DEQ_EYESURF_ACCUMB__DEQ_EYESURF_ACCUMA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	EYESURF_ACCUMB	R	0h	Receive data path eye surf accumulator B result. This represents accumulations at the negative voltage threshold. This result is valid only after eyesurf_valid has asserted.
15-10	RESERVED	R	X	
9-0	EYESURF_ACCUMA	R	0h	Receive data path eye surf accumulator A result. This represents accumulations at the positive voltage threshold. This result is valid only after eyesurf_valid has asserted.

Table 11-777. Register Call Summary for DEQ_EYESURF_ACCUMB__DEQ_EYESURF_ACCUMA_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_EYESURF_ACCUMB__DEQ_EYESURF_ACCUMA_j Register \(Offset = 434Ch + formula\) \[reset = X\]: \[0\]](#)

11.259 RX_BIST_SYNCNT_PREG__RX_BIST_CONTROLS_PREG_j Register (Offset = 4350h + formula) [reset = X]

RX_BIST_SYNCNT_PREG__RX_BIST_CONTROLS_PREG_j is shown in Figure 11-259 and described in Table 11-779.

Return to [Summary Table](#).

Receive BIST control register.

Offset = 4350h + (j * 400h); where j = 0h to 1h

Table 11-778. RX_BIST_SYNCNT_PREG__RX_BIST_CONTROLS_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4350h + formula
SERDES_16G1	0501 4350h + formula
SERDES_16G2	0502 4350h + formula
SERDES_16G3	0503 4350h + formula

Figure 11-259. RX_BIST_SYNCNT_PREG__RX_BIST_CONTROLS_PREG_j Register

31	30	29	28	27	26	25	24
RX_BIST_SYNC_COUNT_PREG							
R/W-0h							
23	22	21	20	19	18	17	16
RX_BIST_SYNC_COUNT_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				RX_BIST_MODE_PREG			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED			RX_BIST_ERR_RESET_PREG	RESERVED		RX_BIST_UDD_WR_CLEAR_PREG	RX_BIST_EN_PREG
R/W-X			W-0h	R/W-X		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-779. RX_BIST_SYNCNT_PREG__RX_BIST_CONTROLS_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_BIST_SYNC_COUNT_PREG	R/W	0h	Receive BIST synchronization count: Number of clock periods the received data must match the expected BIST data to achieve rx_bist_sync_In_{15:0} assertion.
15-12	RESERVED	R/W	X	

**Table 11-779. RX_BIST_SYNCCNT_PREG__RX_BIST_CONTROLS_PREG_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
11-8	RX_BIST_MODE_PREG	R/W	0h	Receive BIST mode: Selects which pattern to which the BIST will align and compare. Pattern 4'b0000 User Defined Data (UDD) FIFO 4'b 0001 - 4'b0111 Reserved 4'b1000 27 order PRBS (Polynomial x^7+x^6+1) 4'b1001 215 bit PRBS (Polynomial $x^{15}+x^{14}+1$) 4'b1010 223 bit PRBS (Polynomial $x^{23}+x^{18}+1$) 4'b1011 231 bit PRBS (Polynomial $x^{31}+x^{28}+1$) 4'b 1100 - 4'b1111 Reserved Note the value must match the corresponding field for the transmit BIST controller.
7-5	RESERVED	R/W	X	
4	RX_BIST_ERR_RESET_PREG	W	0h	Receive BIST error clear: Writing this bit high will clear any rx_bist_status_in_{15:0} assertion and any rx_bist_err_count_preg accumulations.
3-2	RESERVED	R/W	X	
1	RX_BIST_UDD_WR_CLEAR_PREG	R/W	0h	Receive BIST User Defined Data (UDD) FIFO write pointer clear: Writing a logic 1 resets the FIFO write pointer to 0. Note it does not clear the content of the user defined data FIFO. Note this register bit must be written back low for BIST operation.
0	RX_BIST_EN_PREG	R/W	0h	Receive BIST active high enable.

Table 11-780. Register Call Summary for RX_BIST_SYNCCNT_PREG__RX_BIST_CONTROLS_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_BIST_SYNCCNT_PREG__RX_BIST_CONTROLS_PREG_j Register \(Offset = 4350h + formula\) \[reset = X\]: \[0\]](#)

11.260 RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PREG_j Register (Offset = 4354h + formula) [reset = X]

RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PREG_j is shown in Figure 11-260 and described in Table 11-782.

Return to [Summary Table](#).

Receive BIST user defined data (UDD) FIFO definition register.

Offset = 4354h + (j * 400h); where j = 0h to 1h

Table 11-781. RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4354h + formula
SERDES_16G1	0501 4354h + formula
SERDES_16G2	0502 4354h + formula
SERDES_16G3	0503 4354h + formula

Figure 11-260. RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_BIST_ERR_COUNT															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						RX_UDD_FIFO_WR_DATA									
R/W-X						W-0h									

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-782. RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_BIST_ERR_COUNT	R	0h	Receive BIST accumulated error count.
15-10	RESERVED	R/W	X	
9-0	RX_UDD_FIFO_WR_DATA	W	0h	Receive BIST user defined data: Writing a data word to this field will result in that data word being placed in the next available position in the receive BIST user defined data FIFO. Note: xcvr_data_width_in_{15:0}=16-bit data: Only bits [7:0] used. Two FIFO words consumed per clock period. xcvr_data_width_in_{15:0}=20-bit data: All bits used. Two FIFO words consumed per clock period. xcvr_data_width_in_{15:0}=32-bit data : Only bits [7:0] used. Four FIFO words consumed per clock period.

Table 11-783. Register Call Summary for RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RX_BIST_ERRCNT_PREG__RX_BIST_UDD_PREG_j Register \(Offset = 4354h + formula\) \[reset = X\]: \[0\]](#)

11.261 LN_SPARE_REG_PREG_j Register (Offset = 4360h + formula) [reset = X]

LN_SPARE_REG_PREG_j is shown in [Figure 11-261](#) and described in [Table 11-785](#).

Return to [Summary Table](#).

Local Lane spare register.

Offset = 4360h + (j * 400h); where j = 0h to 1h

Table 11-784. LN_SPARE_REG_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4360h + formula
SERDES_16G1	0501 4360h + formula
SERDES_16G2	0502 4360h + formula
SERDES_16G3	0503 4360h + formula

Figure 11-261. LN_SPARE_REG_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SPARE_PREG															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-785. LN_SPARE_REG_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	SPARE_PREG	R/W	0h	Spare register bits assigned to Inda_sparecdb. Bits Definition [15:2] Unused [1] LFPS det sampler clock edge selection for pulse_none: 0 : falling edge 1 : rising edge [0] Unused

Table 11-786. Register Call Summary for LN_SPARE_REG_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LN_SPARE_REG_PREG_j Register \(Offset = 4360h + formula\) \[reset = X\]: \[0\]](#)

11.262 PREADAPT_CTRL_PREG_j Register (Offset = 4370h + formula) [reset = X]

PREADAPT_CTRL_PREG_j is shown in [Figure 11-262](#) and described in [Table 11-788](#).

Return to [Summary Table](#).

Pre-adaptation control register.

Offset = 4370h + (j * 400h); where j = 0h to 1h

Table 11-787. PREADAPT_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4370h + formula
SERDES_16G1	0501 4370h + formula
SERDES_16G2	0502 4370h + formula
SERDES_16G3	0503 4370h + formula

Figure 11-262. PREADAPT_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			PREADAPT_EN_PREG	RESERVED		PREADAPT_STANDARD_MODE_SEL_PREG	
R/W-X			R/W-0h	R/W-X		R/W-2h	
7	6	5	4	3	2	1	0
PREADAPT_STATE							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-788. PREADAPT_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12	PREADAPT_EN_PREG	R/W	0h	Active high pre-adaptation enable.
11-10	RESERVED	R/W	X	
9-8	PREADAPT_STANDARD_MODE_SEL_PREG	R/W	2h	Pre-adaptation xcvr_standard_mode selection: Pre-adaptation run on 2'b00 xcvr_standard_mode=0 only. 2'b01 xcvr_standard_mode=0 and 1. 2'b10 xcvr_standard_mode=0,1 and 2. 2'b11 xcvr_standard_mode=0,1,2 and 3.
7-0	PREADAPT_STATE	R	0h	Pre-adaptation current state: Note this register is for diagnostic purposes only.

Table 11-789. Register Call Summary for PREADAPT_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PREADAPT_CTRL_PREG_j Register \(Offset = 4370h + formula\) \[reset = X\]: \[0\]](#)

11.263 LN_CTRL_DIAG_RESET_PREG_LN_FPWRISO_DIAG_RESET_PREG_j Register (Offset = 4380h + formula) [reset = X]

LN_CTRL_DIAG_RESET_PREG_LN_FPWRISO_DIAG_RESET_PREG_j is shown in Figure 11-263 and described in Table 11-791.

Return to [Summary Table](#).

Lane fpwriso reset diagnostic register

Offset = 4380h + (j * 400h); where j = 0h to 1h

Table 11-790.
LN_CTRL_DIAG_RESET_PREG_LN_FPWRISO_DIAG_RESET_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4380h + formula
SERDES_16G1	0501 4380h + formula
SERDES_16G2	0502 4380h + formula
SERDES_16G3	0503 4380h + formula

Figure 11-263. LN_CTRL_DIAG_RESET_PREG_LN_FPWRISO_DIAG_RESET_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED				LN_PSMRST_N	PSTG_RST_N	CMN_RESET_SYNCED_LN_PLLCLK_N	SCANOVRD_P_LLLN_RST_N
R-X				R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LNDA_RSTGEN_RST_N
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-791. LN_CTRL_DIAG_RESET_PREG_LN_FPWRISO_DIAG_RESET_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19	LN_PSMRST_N	R	0h	Current state of the ln_psmrst_n reset.
18	PSTG_RST_N	R	0h	Current state of the pstg_rst_n reset.
17	CMN_RESET_SYNCED_LN_PLLCLK_N	R	0h	Current state of the cmn_reset_synced_ln_pllclk_n reset.
16	SCANOVRD_P_LLLN_RST_N	R	0h	Current state of the scanovrd_pll_n rst_n reset.
15-1	RESERVED	R	X	
0	LNDA_RSTGEN_RST_N	R	0h	Current state of the lnda_rstgen_rst_n reset.

**Table 11-792. Register Call Summary for
LN_CTRL_DIAG_RESET_PREG__LN_FPWRISO_DIAG_RESET_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LN_CTRL_DIAG_RESET_PREG__LN_FPWRISO_DIAG_RESET_PREG_j Register \(Offset = 4380h + formula\) \[reset = X\]: \[0\]](#)

11.264 LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTRL_DIAG_RESET_PREG_j Register (Offset = 4384h + formula) [reset = X]

LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTRL_DIAG_RESET_PREG_j is shown in Figure 11-264 and described in Table 11-794.

Return to [Summary Table](#).

Lane Tx control reset diagnostic register

Offset = 4384h + (j * 400h); where j = 0h to 1h

Table 11-793.
LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTRL_DIAG_RESET_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4384h + formula
SERDES_16G1	0501 4384h + formula
SERDES_16G2	0502 4384h + formula
SERDES_16G3	0503 4384h + formula

Figure 11-264. LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTRL_DIAG_RESET_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED						TX_SYNC_FIFO_RD_RESET_N	TX_SYNC_FIFO_WR_RESET_N
R-X						R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED					CMN_RESET_SYNCED_TX_REFCLK_GATED_N	TX_LFPSGEN_RST_N	TX_BIST_RST_N
R-X					R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-794. LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTRL_DIAG_RESET_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17	TX_SYNC_FIFO_RD_RESET_N	R	0h	Current state of the tx_sync_fifo_rd_reset_n reset.
16	TX_SYNC_FIFO_WR_RESET_N	R	0h	Current state of the tx_sync_fifo_wr_reset_n reset.
15-3	RESERVED	R	X	
2	CMN_RESET_SYNCED_TX_REFCLK_GATED_N	R	0h	Current state of the cmn_reset_synced_tx_refclk_gated_n reset.
1	TX_LFPSGEN_RST_N	R	0h	Current state of the tx_lfpsgen_rst_n reset.
0	TX_BIST_RST_N	R	0h	Current state of the tx_bist_rst_n reset.

**Table 11-795. Register Call Summary for
LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTRL_DIAG_RESET_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LN_TXDSYNC_DIAG_RESET_PREG__LN_TXCTRL_DIAG_RESET_PREG_j Register \(Offset = 4384h + formula\) \[reset = X\]: \[0\]](#)

11.265 LN_RXDSYNC_DIAG_RESET_PREG__LN_RXCTRL_DIAG_RESET_PREG_j Register (Offset = 4388h + formula) [reset = X]

LN_RXDSYNC_DIAG_RESET_PREG__LN_RXCTRL_DIAG_RESET_PREG_j is shown in Figure 11-265 and described in Table 11-797.

Return to [Summary Table](#).

Lane Rx control reset diagnostic register

Offset = 4388h + (j * 400h); where j = 0h to 1h

Table 11-796.
LN_RXDSYNC_DIAG_RESET_PREG__LN_RXCTRL_DIAG_RESET_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 4388h + formula
SERDES_16G1	0501 4388h + formula
SERDES_16G2	0502 4388h + formula
SERDES_16G3	0503 4388h + formula

Figure 11-265. LN_RXDSYNC_DIAG_RESET_PREG__LN_RXCTRL_DIAG_RESET_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED				TX_TD_FE_LP BK_RST_N	RXDA_DEQ_R ST_N	RXDATRST_N	RXMEMRST_N
R-X				R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED		CMN_RESET_ SYNCED_RX_ REFCLK_GATE_ D_N	CMN_RESET_ SYNCED_LN_P LLCLK_FULLR T_N	CMN_RESET_ SYNCED_CMN_ SDOSC_CLK_ N	CPICAL_CNTR ST_N	RXDA_ECMP_ RST_N	RXDA_SMP_R ST_N
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-797. LN_RXDSYNC_DIAG_RESET_PREG__LN_RXCTRL_DIAG_RESET_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19	TX_TD_FE_LPBK_RST_N	R	0h	Current state of the tx_td_fe_lpbk_rst_n reset.
18	RXDA_DEQ_RST_N	R	0h	Current state of the rxda_deq_rst_n reset.
17	RXDATRST_N	R	0h	Current state of the rxdatrst_n reset.
16	RXMEMRST_N	R	0h	Current state of the rxmemrst_n reset.
15-6	RESERVED	R	X	
5	CMN_RESET_SYNCED_RX_REFCLK_GATED_N	R	0h	Current state of the cmn_reset_synced_rx_refclk_gated_n reset.
4	CMN_RESET_SYNCED_LN_PLLCLK_FULLRT_N	R	0h	Current state of the cmn_reset_synced_ln_pllclk_fullrt_n reset.

Table 11-797. LN_RXDSYNC_DIAG_RESET_PREG_LN_RXCTRL_DIAG_RESET_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMN_RESET_SYNCED_CMN_SDOSC_CLK_N	R	0h	Current state of the cmn_reset_synced_cmn_sdosc_clk_n reset.
2	CPICAL_CNTRST_N	R	0h	Current state of the cpical_cntrst_n reset.
1	RXDA_ECMP_RST_N	R	0h	Current state of the rxda_ecmp_rst_n reset.
0	RXDA_SMP_RST_N	R	0h	Current state of the rxda_smp_rst_n reset.

Table 11-798. Register Call Summary for LN_RXDSYNC_DIAG_RESET_PREG_LN_RXCTRL_DIAG_RESET_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LN_RXDSYNC_DIAG_RESET_PREG_LN_RXCTRL_DIAG_RESET_PREG_j Register \(Offset = 4388h + formula\) \[reset = X\]: \[0\]](#)

11.266 LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_CLK_FREQ_MSMT_CTRL_PREG_j Register (Offset = 4390h + formula) [reset = X]

LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_CLK_FREQ_MSMT_CTRL_PREG_j is shown in Figure 11-266 and described in Table 11-800.

Return to [Summary Table](#).

Register For Controlling Clock Frequency Measurement Module.

Offset = 4390h + (j * 400h); where j = 0h to 1h

Table 11-799.
LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_CLK_FREQ_MSMT_CTRL_P
REG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4390h + formula
SERDES_16G1	0501 4390h + formula
SERDES_16G2	0502 4390h + formula
SERDES_16G3	0503 4390h + formula

Figure 11-266. LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_CLK_FREQ_MSMT_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED				LN_CMSMT_REF_CLK_TMR_VALUE_PREG			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
LN_CMSMT_REF_CLK_TMR_VALUE_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				LN_TEST_CLK_SEL_PREG		LN_CMSMT_MEASUREMENT_RUN_PREG	
R/W-X				R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-800. LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_CLK_FREQ_MSMT_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	LN_CMSMT_REF_CLK_TMR_VALUE_PREG	R/W	0h	Reference clock Timer Value
15-4	RESERVED	R/W	X	
3-1	LN_TEST_CLK_SEL_PREG	R/W	0h	Select Line For Clock Signal Muxing
0	LN_CMSMT_MEASUREMENT_RUN_PREG	R/W	0h	Clock Frequency Measurement Enabln Signal.

**Table 11-801. Register Call Summary for
LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_CLK_FREQ_MSMT_CTRL_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LN_CMSMT_REF_CLK_TMR_VALUE_PREG__LN_CLK_FREQ_MSMT_CTRL_PREG_j Register \(Offset = 4390h + formula\) \[reset = X\]: \[0\]](#)

11.267 LN_CLK_FREQ_MSMT_OBS_PREG_LN_CMSMT_TEST_CLK_CNT_VALUE_PREG_j Register (Offset = 4394h + formula) [reset = X]

LN_CLK_FREQ_MSMT_OBS_PREG_LN_CMSMT_TEST_CLK_CNT_VALUE_PREG_j is shown in Figure 11-267 and described in Table 11-803.

Return to [Summary Table](#).

Status Register Indicating the test clock count value from Clock Frequency Measurement Module.

Offset = 4394h + (j * 400h); where j = 0h to 1h

Table 11-802.
LN_CLK_FREQ_MSMT_OBS_PREG_LN_CMSMT_TEST_CLK_CNT_VALUE_P
REG_j Instances

Instance	Physical Address
SERDES_16G0	0500 4394h + formula
SERDES_16G1	0501 4394h + formula
SERDES_16G2	0502 4394h + formula
SERDES_16G3	0503 4394h + formula

Figure 11-267. LN_CLK_FREQ_MSMT_OBS_PREG_LN_CMSMT_TEST_CLK_CNT_VALUE_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							LN_CMSMT_MEASUREMENT_DONE
R-X							R-0h
15	14	13	12	11	10	9	8
RESERVED				LN_CMSMT_TEST_CLK_CNT_VALUE			
R-X				R-0h			
7	6	5	4	3	2	1	0
LN_CMSMT_TEST_CLK_CNT_VALUE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 11-803. LN_CLK_FREQ_MSMT_OBS_PREG_LN_CMSMT_TEST_CLK_CNT_VALUE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16	LN_CMSMT_MEASUREMENT_DONE	R	0h	Clock Frequency Measurement Done Output.
15-12	RESERVED	R	X	
11-0	LN_CMSMT_TEST_CLK_CNT_VALUE	R	0h	Test Clock Count value Output

**Table 11-804. Register Call Summary for
LN_CLK_FREQ_MSMT_OBS_PREG_LN_CMSMT_TEST_CLK_CNT_VALUE_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [LN_CLK_FREQ_MSMT_OBS_PREG_LN_CMSMT_TEST_CLK_CNT_VALUE_PREG_j Register \(Offset = 4394h + formula\) \[reset = X\]: \[0\]](#)

11.268 RXMRGN_CTRL_PREG_j Register (Offset = 43A0h + formula) [reset = X]

RXMRGN_CTRL_PREG_j is shown in [Figure 11-268](#) and described in [Table 11-806](#).

Return to [Summary Table](#).

RX margining control and status register

Offset = 43A0h + (j * 400h); where j = 0h to 1h

Table 11-805. RXMRGN_CTRL_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 43A0h + formula
SERDES_16G1	0501 43A0h + formula
SERDES_16G2	0502 43A0h + formula
SERDES_16G3	0503 43A0h + formula

Figure 11-268. RXMRGN_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RXMRGN_FSM_STATE				RESERVED			
R-0h				R/W-X			
7	6	5	4	3	2	1	0
RESERVED							RXMRGN_CLK_FORCE_PREG
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-806. RXMRGN_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-12	RXMRGN_FSM_STATE	R	0h	In_rxctrl_rxmrngn FSM state vector
11-1	RESERVED	R/W	X	
0	RXMRGN_CLK_FORCE_PREG	R/W	0h	When asserted,rxmrngb_clk remains on when whenever rxdatclk is on in power state where psc_rxmrngn_en is asserted.

Table 11-807. Register Call Summary for RXMRGN_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RXMRGN_CTRL_PREG_j Register \(Offset = 43A0h + formula\) \[reset = X\]: \[0\]](#)

11.269 SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j Register (Offset = 43B0h + formula) [reset = X]

SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j is shown in Figure 11-269 and described in Table 11-809.

Return to [Summary Table](#).

Data path sampler offset calibration control register.

Offset = 43B0h + (j * 400h); where j = 0h to 1h

Table 11-808.
SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 43B0h + formula
SERDES_16G1	0501 43B0h + formula
SERDES_16G2	0502 43B0h + formula
SERDES_16G3	0503 43B0h + formula

Figure 11-269. SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED						SMPCAL_INIT_WAIT_PREG	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
SMPCAL_INIT_WAIT_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
SMPCAL_RUN_PREG	SMPCALMEM_POSOFF_INVERT	SMPCAL_NO_ANA_RESP	SMPCAL_ERROR	RESERVED			
R/W-0h	R/W-0h	R-0h	R-0h	R/W-X			
7	6	5	4	3	2	1	0
RESERVED		SMPCAL_SCALE_PREG		RESERVED	SMPCAL_DON_E_OVR_PREG	SMPCAL_EN_OVR_PREG	SMPCAL_EN_OVRVAL_PREG
R/W-X		R/W-0h		R/W-X	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-809. SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	SMPCAL_INIT_WAIT_PREG	R/W	0h	Data path sampler offset calibration initial wait timer. Provides a analog circuit settling period at the initiation of the calibration sequence for both even and odd slicers. Note: This value is in rx_rd_clk clock periods. Note: The delay is smpcal_init_wait_preg + 1 rx_rd_clk periods. Note: The same value is applied to both even and odd slicers.
15	SMPCAL_RUN_PREG	R/W	0h	Data path sampler offset calibration manual start signal. Note: The user must write this bit from low to high to initiate a new calibration sequence.
14	SMPCALMEM_POSOFF_INVERT	R/W	0h	Data path sampler offset calibration positive offset correction inversion. Note: This bit is for diagnostic purposes only.

Table 11-809. SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SMPCAL_NO_ANA_RESP	R	0h	Data path sampler offset calibration no analog response flag. Indicates that the odd slicer calibration function has exhausted the entire offset correction range and concluded with no data greater or equal to 25% ones. Note: This signal is valid when smpcal_odddone is asserted, and cleared when smpcal_run or smpcal_run_preg is asserted.
12	SMPCAL_ERROR	R	0h	Data path sampler offset calibration error flag. This error status bit will be asserted if the captured data is not all zeroes when the even and odd comparators are set to their maximum positive offset correction values. Note: This signal is valid when smpcal_odddone is asserted, and cleared when smpcal_run or smpcal_run_preg is asserted.
11-6	RESERVED	R/W	X	
5-4	SMPCAL_SCALE_PREG	R/W	0h	Data path sampler offset calibration scale register. Setting this register to a non-zero value will reduce the number of offset correction codes by forcing the LSBs to zero. 2'b 00: Max. 8-bit signed correction code 2'b 01: Correction code LSB zeroed out 2'b 10: Correction code 2 LSBs zeroed out 2'b 11: Correction code 3 LSBs zeroed out Note: The smpcal_start_preg value will be right-shift by smpcal_scale_preg to shorten the calibration accordingly. Note: The same value is applied to both even and odd slicers.
3	RESERVED	R/W	X	
2	SMPCAL_DONE_OVR_PREG	R/W	0h	Data path sampler offset calibration done override. When this is asserted, the calibration process will be skipped, and the smpcal_done pulse to the PSM will be asserted.
1	SMPCAL_EN_OVR_PREG	R/W	0h	Data path sampler offset calibration enable active high override enable. When asserted, forces the smpcal_en_ovrval_preg value on rxda_smp_calen.
0	SMPCAL_EN_OVRVAL_PREG	R/W	0h	Data path sampler offset calibration enable active high override value. When smpcal_en_ovr_preg is asserted high, this value drives out on rxda_smp_calen.

Table 11-810. Register Call Summary for SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SMPCAL_INIT_PREG__SMPCAL_CTRL_PREG_j Register \(Offset = 43B0h + formula\) \[reset = X\]: \[0\]](#)

11.270 SMPCAL_NUM_WORDS_PREG__SMPICAL_ITER_PREG_j Register (Offset = 43B4h + formula) [reset = X]

SMPCAL_NUM_WORDS_PREG__SMPICAL_ITER_PREG_j is shown in Figure 11-270 and described in Table 11-812.

Return to [Summary Table](#).

Data path sampler offset calibration iteration timer register.

Offset = 43B4h + (j * 400h); where j = 0h to 1h

Table 11-811. SMPCAL_NUM_WORDS_PREG__SMPICAL_ITER_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 43B4h + formula
SERDES_16G1	0501 43B4h + formula
SERDES_16G2	0502 43B4h + formula
SERDES_16G3	0503 43B4h + formula

Figure 11-270. SMPCAL_NUM_WORDS_PREG__SMPICAL_ITER_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						SMPCAL_NUM_WORDS_PREG									
R/W-X						R/W-100h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SMPICAL_ITER_WAIT_PREG									
R/W-X						R/W-4h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-812. SMPCAL_NUM_WORDS_PREG__SMPICAL_ITER_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	SMPCAL_NUM_WORDS_PREG	R/W	100h	Data path sampler offset calibration accumulation period timer. Sets the time period to accumulate measurement data before making a decision about the current offset correction code. Note: This value is delineated in 16-bit or 20 bit words. If 32-bit data mode is selected using xcvr_data_width, this value will be internally halved to correspond to 16-bit words. Note: The same value is applied to both even and odd slicers.
15-10	RESERVED	R/W	X	
9-0	SMPICAL_ITER_WAIT_PREG	R/W	4h	Data path sampler offset calibration iteration wait timer. Provides delay for analog settling between each offset adjustment level change. Note: This value is in rx_rd_clk clock periods. Note: The delay is smpcal_iter_wait_preg + 1 rx_rd_clk periods. Note: The same value is applied to both even and odd slicers.

Table 11-813. Register Call Summary for SMPCAL_NUM_WORDS_PREG__SMPICAL_ITER_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SMPCAL_NUM_WORDS_PREG__SMPICAL_ITER_PREG_j Register \(Offset = 43B4h + formula\) \[reset = X\]: \[0\]](#)

11.271 SMPCAL_TUNE_PREG__SMPCAL_START_PREG_j Register (Offset = 43B8h + formula) [reset = X]

SMPCAL_TUNE_PREG__SMPCAL_START_PREG_j is shown in Figure 11-271 and described in Table 11-815.

Return to [Summary Table](#).

Data path sampler offset calibration starting code register.

Offset = 43B8h + (j * 400h); where j = 0h to 1h

Table 11-814.
SMPCAL_TUNE_PREG__SMPCAL_START_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 43B8h + formula
SERDES_16G1	0501 43B8h + formula
SERDES_16G2	0502 43B8h + formula
SERDES_16G3	0503 43B8h + formula

Figure 11-271. SMPCAL_TUNE_PREG__SMPCAL_START_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								SMPCAL_TUNE_PREG							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPCAL_START_PREG							
R/W-X								R/W-7Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-815. SMPCAL_TUNE_PREG__SMPCAL_START_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	SMPCAL_TUNE_PREG	R/W	0h	Data path sampler offset calibration tuning offset. This signed value is applied both even and odd slicer offset correction codes once the calibration of both is complete.
15-8	RESERVED	R/W	X	
7-0	SMPCAL_START_PREG	R/W	7Fh	Data path sampler offset calibration start code. Note: The same code is applied to both even and odd slicers.

Table 11-816. Register Call Summary for SMPCAL_TUNE_PREG__SMPCAL_START_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SMPCAL_TUNE_PREG__SMPCAL_START_PREG_j Register \(Offset = 43B8h + formula\) \[reset = X\]: \[0\]](#)

11.272 SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_CALEVNCODE_OVR_PREG_j Register (Offset = 43BCh + formula) [reset = X]

SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_CALEVNCODE_OVR_PREG_j is shown in Figure 11-272 and described in Table 11-818.

Return to [Summary Table](#).

Data path sampler offset calibration even code override register.

Offset = 43BCh + (j * 400h); where j = 0h to 1h

Table 11-817.
SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_CALEVNCODE_OVR_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 43BCh + formula
SERDES_16G1	0501 43BCh + formula
SERDES_16G2	0502 43BCh + formula
SERDES_16G3	0503 43BCh + formula

Figure 11-272. SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_CALEVNCODE_OVR_PREG_j Register

31	30	29	28	27	26	25	24
SMPCALMEM_CALODDCODE_OVREN_PREG	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
SMPCALMEM_CALODDCODE_OVRVAL_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
SMPCALMEM_CALEVNCODE_OVREN_PREG	RESERVED						
R/W-0h	R/W-X						
7	6	5	4	3	2	1	0
SMPCALMEM_CALEVNCODE_OVRVAL_PREG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-818. SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_CALEVNCODE_OVR_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SMPCALMEM_CALODDCODE_OVREN_PREG	R/W	0h	Data path sampler offset calibration odd code active high override enable.
30-24	RESERVED	R/W	X	
23-16	SMPCALMEM_CALODDCODE_OVRVAL_PREG	R/W	0h	When smpcalmem_calodddcode_ovren_preg is asserted high, this value overrides the rxda_smp_caloddmag and rxda_smp_caloddposoff analog controls as follows: rxda_smp_caloddposoff = calodddcode_ovren_preg[7] rxda_smp_caloddmag = calodddcode_ovren_preg [6:0]

Table 11-818. SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_CALEVNCODE_OVR_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	SMPCALMEM_CALEVNCODE_OVREN_PREG	R/W	0h	Data path sampler offset calibration even code active high override enable.
14-8	RESERVED	R/W	X	
7-0	SMPCALMEM_CALEVNCODE_OVRVAL_PREG	R/W	0h	When smpcalmem_calevncode_ovren_preg is asserted high, this value overrides the rxd_smp_calevnmag and rxd_smp_calevnposoff analog controls as follows: rxd_smp_calevnposoff = calevncode_ovren_preg[7] rxd_smp_calevnmag = calevncode_ovren_preg[6:0]

Table 11-819. Register Call Summary for SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_CALEVNCODE_OVR_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SMPCAL_CALODDCODE_OVR_PREG__SMPCAL_CALEVNCODE_OVR_PREG_j Register \(Offset = 43BCh + formula\) \[reset = X\]: \[0\]](#)

11.273 SMPCAL_CALODDCODE_PREG__SMPCAL_CALEVNCODE_PREG_j Register (Offset = 43C0h + formula) [reset = X]

SMPCAL_CALODDCODE_PREG__SMPCAL_CALEVNCODE_PREG_j is shown in Figure 11-273 and described in Table 11-821.

Return to [Summary Table](#).

Data path sampler offset calibration even slicer status register.

Offset = 43C0h + (j * 400h); where j = 0h to 1h

Table 11-820.

SMPCAL_CALODDCODE_PREG__SMPCAL_CALEVNCODE_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 43C0h + formula
SERDES_16G1	0501 43C0h + formula
SERDES_16G2	0502 43C0h + formula
SERDES_16G3	0503 43C0h + formula

Figure 11-273. SMPCAL_CALODDCODE_PREG__SMPCAL_CALEVNCODE_PREG_j Register

31	30	29	28	27	26	25	24
SMPCAL_ODD DONE	RESERVED						
R-0h	R-X						
23	22	21	20	19	18	17	16
SMPCAL_CALODDCODE							
R-0h							
15	14	13	12	11	10	9	8
SMPCAL_EVN DONE	RESERVED						
R-0h	R-X						
7	6	5	4	3	2	1	0
SMPCAL_CALEVNCODE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 11-821. SMPCAL_CALODDCODE_PREG__SMPCAL_CALEVNCODE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SMPCAL_ODDDONE	R	0h	Data path sampler offset odd calibration active high complete flag. Note that this calibration status bit is sticky in nature. This bit, once set will remain asserted until another calibration starts or until reset is asserted.
30-24	RESERVED	R	X	
23-16	SMPCAL_CALODDCODE	R	0h	Data path sampler offset calibration odd calibration result. Note: This is a signed binary value. Note: This result is valid when smpcal_odddone is asserted.
15	SMPCAL_EVNDONE	R	0h	Data path sampler offset even calibration active high complete flag. Note: This calibration status bit is sticky in nature. This bit, once set will remain asserted until another offset calibration starts or until a link or macro is asserted.
14-8	RESERVED	R	X	

Table 11-821. SMPCAL_CALODDCODE_PREG__SMPCAL_CALEVNCODE_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SMPCAL_CALEVNCODE	R	0h	Data path sampler offset calibration even calibration result. Note: This is a signed binary value. Note: This result is valid when smpcal_evndone is asserted.

**Table 11-822. Register Call Summary for
SMPCAL_CALODDCODE_PREG__SMPCAL_CALEVNCODE_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SMPCAL_CALODDCODE_PREG__SMPCAL_CALEVNCODE_PREG_j Register \(Offset = 43C0h + formula\) \[reset = X\]: \[0\]](#)

11.274 SMPCAL_STATE_PREG_j Register (Offset = 43C4h + formula) [reset = X]

SMPCAL_STATE_PREG_j is shown in Figure 11-274 and described in Table 11-824.

Return to [Summary Table](#).

Data path sampler offset calibration master state machine state vector status register.

Offset = 43C4h + (j * 400h); where j = 0h to 1h

Table 11-823. SMPCAL_STATE_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 43C4h + formula
SERDES_16G1	0501 43C4h + formula
SERDES_16G2	0502 43C4h + formula
SERDES_16G3	0503 43C4h + formula

Figure 11-274. SMPCAL_STATE_PREG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SMPCAL_STATE							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 11-824. SMPCAL_STATE_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	SMPCAL_STATE	R	0h	Data path sampler offset calibration master state machine state vector. Note: This is used for diagnostic purposes only. FSM State smpcal_state CAL_IDLE 10'b0000000000 CAL_SHORT_LA 10'b0000000001 CAL_INIT_EVN 10'b0000000011 CAL_WAIT_EVN 10'b0000010111 CAL_CAPTURE_EVN 10'b0000100111 CAL_STORE_EVN 10'b0001000101 CAL_INIT_ODD 10'b1000000011 CAL_WAIT_ODD 10'b0000011011 CAL_CAPTURE_ODD 10'b0000101011 CAL_STORE_ODD 10'b0010001001 CAL_DONE 10'b0100000000

Table 11-825. Register Call Summary for SMPCAL_STATE_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [SMPCAL_STATE_PREG_j Register \(Offset = 43C4h + formula\) \[reset = X\]: \[0\]](#)

11.275 DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_TAU_CTRL1_PREG_j Register (Offset = 43D0h + formula) [reset = X]

DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_TAU_CTRL1_PREG_j is shown in Figure 11-275 and described in Table 11-827.

Return to [Summary Table](#).

Receive data path equalization (DEQ) bumper TAU algorithm control register 1

Offset = 43D0h + (j * 400h); where j = 0h to 1h

Table 11-826.
DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_TAU_CTRL1_PREG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 43D0h + formula
SERDES_16G1	0501 43D0h + formula
SERDES_16G2	0502 43D0h + formula
SERDES_16G3	0503 43D0h + formula

Figure 11-275. DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_TAU_CTRL1_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED						BMPR_TAU_ERROR_THRESH_PREG	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
BMPR_TAU_ERROR_THRESH_PREG							
R/W-0h							
15	14	13	12	11	10	9	8
BMPR_TAU_DIR_PREG	RESERVED	BMPR_TAU_PING_PONG_EN_PREG		RESERVED			
R/W-0h	R/W-X	R/W-0h		R/W-X			
7	6	5	4	3	2	1	0
RESERVED				BMPR_TAU_EPIOFFSET_PREG			
R/W-X				R/W-5h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-827. DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_TAU_CTRL1_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	BMPR_TAU_ERROR_THRESH_PREG	R/W	0h	Bumper TAU algorithm error accumulation threshold.
15	BMPR_TAU_DIR_PREG	R/W	0h	Bumper TAU algorithm EPI initial direction control. Direction 1'b0 The EPI will initially shift to the right. 1'b1 The EPI will initially shift to the left.
14	RESERVED	R/W	X	

Table 11-827. DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_TAU_CTRL1_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	BMPR_TAU_PING_PONG_EN_PREG	R/W	0h	Bumper TAU ping pong enable register. Direction 2'b0x Ping pong mode disabled. The bumper TAU algorithm will always start shifting in the direction set by bmpr_tau_dir_preg. 2'b10 Ping pong alternate mode. If the bumper TAU algorithm does not find any errors that surpass the threshold in both ST_BMPR_TAU_ACCUM_A and ST_BMPR_TAU_ACCUM_B states, the initial direction of the algorithm will swap in the subsequent bumper TAU iteration. 2'b11 Ping pong always mode. The initial direction of the algorithm will always swap in the subsequent bumper TAU iteration.
11-4	RESERVED	R/W	X	
3-0	BMPR_TAU_EPIOFFSET_PREG	R/W	5h	Bumper TAU algorithm 4 bit signed offset for EPI.

Table 11-828. Register Call Summary for DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_TAU_CTRL1_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_BMPR_TAU_CTRL2_PREG__DEQ_BMPR_TAU_CTRL1_PREG_j Register \(Offset = 43D0h + formula\) \[reset = X\]: \[0\]](#)

11.276 DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_VTH_PREG_j Register (Offset = 43D4h + formula) [reset = X]

DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_VTH_PREG_j is shown in [Figure 11-276](#) and described in [Table 11-830](#).

Return to [Summary Table](#).

Receive data path equalization (DEQ) TAU algorithm acquisition voltage threshold control register

Offset = 43D4h + (j * 400h); where j = 0h to 1h

Table 11-829. DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_VTH_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 43D4h + formula
SERDES_16G1	0501 43D4h + formula
SERDES_16G2	0502 43D4h + formula
SERDES_16G3	0503 43D4h + formula

Figure 11-276. DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_VTH_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	TAU_MAITECMPA_VTH_PREG						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	TAU_MAITECMPB_VTH_PREG						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	TAU_ECMPA_VTH_PREG						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	TAU_ECMPB_VTH_PREG						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-830. DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_VTH_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	TAU_MAITECMPA_VTH_PREG	R/W	0h	TAU algorithm voltage threshold control register for both error comparators A and B, binary encoded, used for maintenance for bumper TAU during ST_BMPR_TAU_ACCUM_A, and for apparent center and maintenace for block TAU during ST_BLK_TAU_ACCUM_A. Each step is nominally 3mV.
23	RESERVED	R/W	X	
22-16	TAU_MAITECMPB_VTH_PREG	R/W	0h	TAU algorithm voltage threshold control register for both error comparators A and B, binary encoded, used for maintenance for bumper TAU during ST_BMPR_TAU_ACCUM_B, and for apparent center and maintenace for block TAU during ST_BLK_TAU_ACCUM_B. Each step is nominally 3mV.
15	RESERVED	R/W	X	

Table 11-830. DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_VTH_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-8	TAU_ECMPA_VTH_PREG	R/W	0h	TAU algorithm voltage threshold control register for both error comparators A and B, binary encoded, used for initial acquisition for bumper TAU during ST_BMPR_TAU_ACCUM_A, and block TAU during ST_BLK_TAU_ACCUM_A. Each step is nominally 3mV.
7	RESERVED	R/W	X	
6-0	TAU_ECMPB_VTH_PREG	R/W	0h	TAU algorithm voltage threshold control register for both error comparators A and B, binary encoded, used for initial acquisition for bumper TAU during ST_BMPR_TAU_ACCUM_B, and block TAU during ST_BLK_TAU_ACCUM_B. Each step is nominally 3mV.

Table 11-831. Register Call Summary for DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_VTH_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_TAU_MAINT_VTH_PREG__DEQ_TAU_ACQ_VTH_PREG_j Register \(Offset = 43D4h + formula\) \[reset = X\]: \[0\]](#)

11.277 DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_CTRL1_PREG_j Register (Offset = 43D8h + formula) [reset = X]

DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_CTRL1_PREG_j is shown in Figure 11-277 and described in Table 11-833.

Return to [Summary Table](#).

Receive data path equalization (DEQ) block TAU algorithm control register 1

Offset = 43D8h + (j * 400h); where j = 0h to 1h

Table 11-832. DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_CTRL1_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 43D8h + formula
SERDES_16G1	0501 43D8h + formula
SERDES_16G2	0502 43D8h + formula
SERDES_16G3	0503 43D8h + formula

Figure 11-277. DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_CTRL1_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED	BLK_TAU_EPISHIFT_OPTCENT						
R/W-X	R-0h						
23	22	21	20	19	18	17	16
BLK_TAU_EPISHIFT_OPTCENT_OVRD_PREG	BLK_TAU_EPISHIFT_OPTCENT_OVRD_PREG						
R/W-0h	R/W-0h						
15	14	13	12	11	10	9	8
BLK_TAU_EPIOFFSETA_PREG				BLK_TAU_EPIOFFSETB_PREG			
R/W-2h				R/W-Eh			
7	6	5	4	3	2	1	0
BLK_TAU_MAINT_EPIOFFSETA_PREG				BLK_TAU_MAINT_EPIOFFSETB_PREG			
R/W-2h				R/W-Eh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-833. DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_CTRL1_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	BLK_TAU_EPISHIFT_OPTCENT	R	0h	Block TAU algorithm optimal EPI phase shift obtained from AC_TAU
23	BLK_TAU_EPISHIFT_OPTCENT_OVRD_PREG	R/W	0h	Block TAU algorithm EPI phase shift override enable used for maintenance
22-16	BLK_TAU_EPISHIFT_OPTCENT_OVRD_PREG	R/W	0h	Block TAU algorithm EPI phase shift override value used for maintenance
15-12	BLK_TAU_EPIOFFSETA_PREG	R/W	2h	Block TAU algorithm 4 bit signed offset for EPI, used for accumulation during ST_TAU3_ACCUM_A during initial acquisition.
11-8	BLK_TAU_EPIOFFSETB_PREG	R/W	Eh	Block TAU algorithm 4 bit signed offset for EPI, used for accumulation during ST_TAU3_ACCUM_B during initial acquisition.

Table 11-833. DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_CTRL1_PREG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	BLK_TAU_MAINT_EPIOF_FSETA_PREG	R/W	2h	Block TAU algorithm 4 bit signed offset for EPI, used for accumulation during ST_TAU3_ACCUM_A during AC_TAU and maintenance.
3-0	BLK_TAU_MAINT_EPIOF_FSETB_PREG	R/W	Eh	Block TAU algorithm 4 bit signed offset for EPI, used for accumulation during ST_TAU3_ACCUM_B during AC_TAU and maintenance.

Table 11-834. Register Call Summary for DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_CTRL1_PREG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_BLK_TAU_CTRL2_PREG__DEQ_BLK_TAU_CTRL1_PREG_j Register \(Offset = 43D8h + formula\) \[reset = X\]: \[0\]](#)

11.278 DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_CTRL3_PREG_j Register (Offset = 43DCh + formula) [reset = X]

DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_CTRL3_PREG_j is shown in [Figure 11-278](#) and described in [Table 11-836](#).

Return to [Summary Table](#).

Receive data path equalization (DEQ) block TAU algorithm control register 3

Offset = 43DCh + (j * 400h); where j = 0h to 1h

Table 11-835. DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_CTRL3_PREG_j Instances

Instance	Physical Address
SERDES_16G0	0500 43DCh + formula
SERDES_16G1	0501 43DCh + formula
SERDES_16G2	0502 43DCh + formula
SERDES_16G3	0503 43DCh + formula

Figure 11-278. DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_CTRL3_PREG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	BLK_TAU_DPI_OPTCENT						
R/W-X				R-0h			
15	14	13	12	11	10	9	8
RESERVED		BLK_TAU_PATTERN_MASK_PREG				BLK_TAU_AC_BYPASS_CONCUR_PREG	BLK_TAU_AC_MINITER_PREG
R/W-X		R/W-0h				R/W-0h	R/W-A8h
7	6	5	4	3	2	1	0
BLK_TAU_AC_MINITER_PREG							
R/W-A8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-836. DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_CTRL3_PREG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	BLK_TAU_DPI_OPTCENT	R	0h	Block TAU algorithm optimal DPI phase obtained from initial acquisition
15-14	RESERVED	R/W	X	
13-10	BLK_TAU_PATTERN_MASK_PREG	R/W	0h	Block TAU algorithm pattern filter mask.
9	BLK_TAU_AC_BYPASS_CONCUR_PREG	R/W	0h	Block TAU algorithm bypass concur register. When enabled, the concur processes during the apparent center states will be bypassed.
8-0	BLK_TAU_AC_MINITER_PREG	R/W	A8h	Block TAU algorithm minimum iterations of AC_TAU and concur processes during the apparent center states.

**Table 11-837. Register Call Summary for
DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_CTRL3_PREG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [DEQ_BLK_TAU_CTRL4_PREG__DEQ_BLK_TAU_CTRL3_PREG_j Register \(Offset = 43DCh + formula\) \[reset = X\]: \[0\]](#)

11.279 RESERVEDBIT13ADDRESSB_y Register (Offset = 6000h + formula) [reset = 0h]

RESERVEDBIT13ADDRESSB_y is shown in Figure 11-279 and described in Table 11-839.

Return to [Summary Table](#).

Reserved Address bit 13 area B

Offset = 6000h + (y * 4h); where y = 0h to 7FFh

**Table 11-838. RESERVEDBIT13ADDRESSB_y
Instances**

Instance	Physical Address
SERDES_16G0	0500 6000h + formula
SERDES_16G1	0501 6000h + formula
SERDES_16G2	0502 6000h + formula
SERDES_16G3	0503 6000h + formula

Figure 11-279. RESERVEDBIT13ADDRESSB_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES_BIT13_ADR_B																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-839. RESERVEDBIT13ADDRESSB_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES_BIT13_ADR_B	R/W	0h	Write only test region B

Table 11-840. Register Call Summary for RESERVEDBIT13ADDRESSB_y

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RESERVEDBIT13ADDRESSB_y Register \(Offset = 6000h + formula\) \[reset = 0h\]: \[0\]](#)

11.280 RESERVEDSerdesREP8000_y Register (Offset = 8000h + formula) [reset = 0h]

RESERVEDSIERRAREP8000_y is shown in Figure 11-280 and described in Table 11-842.

Return to [Summary Table](#).

Reserved region aliases region 0x0000-0x0400

Offset = 8000h + (y * 4h); where y = 0h to FFh

**Table 11-841. RESERVEDSerdesREP8000_y
Instances**

Instance	Physical Address
SERDES_16G0	0500 8000h + formula
SERDES_16G1	0501 8000h + formula
SERDES_16G2	0502 8000h + formula
SERDES_16G3	0503 8000h + formula

Figure 11-280. RESERVEDSerdesREP8000_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES_DUP_REGION_A																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-842. RESERVEDSerdesREP8000_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES_DUP_REGION_A	R/W	0h	Duplicate region

Table 11-843. Register Call Summary for RESERVEDSerdesREP8000_y

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RESERVEDSIERRAREP8000_y Register \(Offset = 8000h + formula\) \[reset = 0h\]: \[0\]](#)

11.281 RESERVEDBIT13ADDRESSC_y Register (Offset = A000h + formula) [reset = 0h]

RESERVEDBIT13ADDRESSC_y is shown in [Figure 11-281](#) and described in [Table 11-845](#).

Return to [Summary Table](#).

Reserved Address bit 13 area C

Offset = A000h + (y * 4h); where y = 0h to 7FFh

**Table 11-844. RESERVEDBIT13ADDRESSC_y
Instances**

Instance	Physical Address
SERDES_16G0	0500 A000h + formula
SERDES_16G1	0501 A000h + formula
SERDES_16G2	0502 A000h + formula
SERDES_16G3	0503 A000h + formula

Figure 11-281. RESERVEDBIT13ADDRESSC_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES_BIT13_ADR_C																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-845. RESERVEDBIT13ADDRESSC_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES_BIT13_ADR_C	R/W	0h	Write only test region C

Table 11-846. Register Call Summary for RESERVEDBIT13ADDRESSC_y

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [RESERVEDBIT13ADDRESSC_y Register \(Offset = A000h + formula\) \[reset = 0h\]: \[0\]](#)

11.282 PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register (Offset = C000h) [reset = BD510400h]

PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 is shown in Figure 11-282 and described in Table 11-848.

Return to [Summary Table](#).

PIPE common control1 register

Table 11-847. PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Instances

Instance	Physical Address
SERDES_16G0	0500 C000h
SERDES_16G1	0501 C000h
SERDES_16G2	0502 C000h
SERDES_16G3	0503 C000h

Figure 11-282. PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register

31	30	29	28	27	26	25	24
PHY_PIPE_CMN_CTRL2_15_12				PHY_PIPE_CMN_CTRL2_11_8			
R/W-Bh				R/W-Dh			
23	22	21	20	19	18	17	16
PHY_PIPE_CMN_CTRL2_7	PHY_PIPE_CMN_CTRL2_6	PHY_PIPE_CMN_CTRL2_5	PHY_PIPE_CMN_CTRL2_4	PHY_PIPE_CMN_CTRL2_3	PHY_PIPE_CMN_CTRL2_2	PHY_PIPE_CMN_CTRL2_1	PHY_PIPE_CMN_CTRL2_0
R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
PHY_PIPE_CMN_CTRL1_15_13			PHY_PIPE_CMN_CTRL1_12	PHY_PIPE_CMN_CTRL1_11	PHY_PIPE_CMN_CTRL1_10	PHY_PIPE_CMN_CTRL1_9	PHY_PIPE_CMN_CTRL1_8
R-0h			RC-0h	R-0h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PHY_PIPE_CMN_CTRL1_7	PHY_PIPE_CMN_CTRL1_6	PHY_PIPE_CMN_CTRL1_5_4		PHY_PIPE_CMN_CTRL1_3_0			
R/W-0h	R/W-0h	R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; RC = Read to Clear; -n = value after reset

Table 11-848. PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PHY_PIPE_CMN_CTRL2_15_12	R/W	Bh	USB SuperSpeed Tx LFPS Stretch: Minimum number of data rate clock cycles in which PMA tx_lfps_en signal is asserted for USB SuperSpeed rate. Number of data rate clock cycles must be X 1 PMA RefClk cycle.
27-24	PHY_PIPE_CMN_CTRL2_11_8	R/W	Dh	USB SuperSpeedPlus Tx LFPS Stretch: Minimum number of data rate clock cycles in which PMA tx_lfps_en signal is asserted for USB SuperSpeedPlus rate. Number of data rate clock cycles must be X 1 PMA RefClk cycle.
23	PHY_PIPE_CMN_CTRL2_7	R/W	0h	PCIe PIPE Gen 4 Rx mode: 0 = PCIe Gen4 v0.7 mode, 1 = PCIe Gen4 v0.5 mode. Selects the EIEOS format used for block alignment performed. 0.7 = 0x0000, 0xFFFF, 0x0000, 0xFFFF... 0.5 = 0xFF00, 0xFF00,...
22	PHY_PIPE_CMN_CTRL2_6	R/W	1h	TX electrical idle pre release: When this bit is set, the TX electrical idle release to the PMA is advanced 1 cycle to allow the adjustment of the data path timing

Table 11-848. PHY_PIPE_CMN_CTRL2_PHY_PIPE_CMN_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	PHY_PIPE_CMN_CTRL2_5	R/W	0h	RX equalizer complete mask: When this bit is cleared, the PHY will return direction change of 0 when PMA indicates evaluation complete. Subsequent evaluation requests would clear the PMA iteration counters. When set high, the PMA equalization complete signal is ignored.
20	PHY_PIPE_CMN_CTRL2_4	R/W	1h	PCIe Gen 1/2 EIOS cycle error mask: When this bit is enabled and the pipe rx interface is outputting a PCIe Gen 1/2 EIOS symbol, decode errors will be masked out.
19	PHY_PIPE_CMN_CTRL2_3	R/W	0h	USB Gen 2 Bit Error Correction Disable: When this bit is high, bit error correction on SKP and SDS symbols is disabled.
18	PHY_PIPE_CMN_CTRL2_2	R/W	0h	USB PIPE3 Compatibility Mode enable: When this bit is set to 1, USB PIPE3 compatibility mode is enabled. In this mode, when operating in nominal empty Elasticity Buffer mode, when the EB buffer goes empty, instead of de-asserting PIPE RxDataValid, a USB SKIP OS is inserted into the data stream. This is the behavior as defined in PIPE version 3. When this bit is low, PIPE RxDataValid is de-asserted when the EB buffer goes empty, as recommended by PIPE version 4.
17	PHY_PIPE_CMN_CTRL2_1	R/W	0h	USB Loopback Slave Error Count disable: When this bit is set to 1, disables the error count for US loopback slave, such that the error count is not inserted into the BCNT OS.
16	PHY_PIPE_CMN_CTRL2_0	R/W	1h	USB Elasticity Buffer Re-align enable: When this bit is set to 1, when Rx for a USB link is initially started, the elasticity buffer is re-aligned to its idle point upon seeing 3 consecutive COMMAAs (i.e. from TS1/TS2s) in the same relative bit position. The purpose of this is to re-align the elasticity buffer (i.e. CTC) after receiving the TSEQ data, which contains no SKIP OSs.
15-13	PHY_PIPE_CMN_CTRL1_15_13	R	0h	Reserved
12	PHY_PIPE_CMN_CTRL1_12	RC	0h	PHY APB access timeout: When set, an APB read/write request to PHY registers failed (i.e. timed out). When set, this bit is cleared upon read.
11	PHY_PIPE_CMN_CTRL1_11	R	0h	Reserved
10	PHY_PIPE_CMN_CTRL1_10	R/W	1h	Comma realign: This field controls the comma alignment state machine to re-align to new bit position without going to loss of sync state for Gen1/2. The requirement of the new bit position should meet the number of COM as per Symbol lock count register definition. When new bit position is identified the comma alignment state machine remains in sync state with the alignment now locked to the new bit position. This field needs to be programmed during the PHY initialization routine before training sequences are received.
9	PHY_PIPE_CMN_CTRL1_9	R/W	0h	Block alignment clear on EIOS Gen4: When this bit is enabled and the Gen 3/4 block alignment sees an EIOS, then the block alignment will automatically reset regardless of signal detect from the PMA.

Table 11-848. PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	PHY_PIPE_CMN_CTRL1_8	R/W	0h	Comma alignment clear on EIOS Gen2: When this bit is enabled and the Gen 1/2 comma alignment sees an EIOS, then the COMMA alignment will automatically reset regardless of signal detect from the PMA.
7	PHY_PIPE_CMN_CTRL1_7	R/W	0h	Block alignment ignore rx_sigdetect Gen4: When this signal is enabled, the PCS receive path block alignment will not clear due to loss of signal detection from the PMA in Gen 3/4 mode.
6	PHY_PIPE_CMN_CTRL1_6	R/W	0h	Comma alignment ignore rx_sigdetect Gen2: When this signal is enabled, the PCS receive path COMMA alignment will not clear due to loss of signal detection from the PMA in Gen 1/2 mode.
5-4	PHY_PIPE_CMN_CTRL1_5_4	R/W	0h	RX signal detect delay: Controls how much delay to add to the PMA signal detect to delay when the bit alignment blocks should be reset after losing signal.
3-0	PHY_PIPE_CMN_CTRL1_3_0	R	0h	Reserved

Table 11-849. Register Call Summary for PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register \(Offset = C000h\) \[reset = BD510400h\]: \[0\]](#)

11.283 PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Register (Offset = C004h) [reset = 44444400h]

PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 is shown in [Figure 11-283](#) and described in [Table 11-851](#).

[Return to Summary Table.](#)

PIPE comma lock configuration1 register ()

Table 11-850. PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Instances

Instance	Physical Address
SERDES_16G0	0500 C004h
SERDES_16G1	0501 C004h
SERDES_16G2	0502 C004h
SERDES_16G3	0503 C004h

Figure 11-283. PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Register

31	30	29	28	27	26	25	24
PHY_PIPE_COM_LOCK_CFG2_15_8							
R/W-44h							
23	22	21	20	19	18	17	16
PHY_PIPE_COM_LOCK_CFG2_7_0							
R/W-44h							
15	14	13	12	11	10	9	8
PHY_PIPE_COM_LOCK_CFG1_15_12				PHY_PIPE_COM_LOCK_CFG1_11_0			
R/W-4h				R/W-400h			
7	6	5	4	3	2	1	0
PHY_PIPE_COM_LOCK_CFG1_11_0							
R/W-400h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-851. PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_COM_LOCK_CFG2_15_8	R/W	44h	comma lock count fast: The number of COMMA symbols that needs to be seen in the same bit position for the comma state machine to lock for Gen1/2. This field is used while the PCS is in P0 state after an EIOS has been seen, ie detecting FTS.
23-16	PHY_PIPE_COM_LOCK_CFG2_7_0	R/W	44h	comma lock count: The number of COMMA symbols that needs to be seen in the same bit position for the comma state machine to lock for Gen1/2. This field is used while the PCS is transitioning out of a power state and not performing a rate change.
15-12	PHY_PIPE_COM_LOCK_CFG1_15_12	R/W	4h	Symbol unlock count: The number of COMMA symbols that needs to be seen in the wrong bit position before the comma alignment state machine will transition to RESYNC or LOS state for Gen1/2.
11-0	PHY_PIPE_COM_LOCK_CFG1_11_0	R/W	400h	comma full lock count: The number of COMMA symbols that needs to be seen in the same bit position for the comma alignment state machine to lock for Gen1/2. The field is used for initial reset lock or lock after a rate change

Table 11-852. Register Call Summary for PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Register \(Offset = C004h\) \[reset = 44444400h\]: \[0\]](#)

11.284 PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register (Offset = C008h) [reset = 137Fh]

PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG is shown in Figure 11-284 and described in Table 11-854.

Return to [Summary Table](#).

PIPE EIEOS lock configuration register ()

Table 11-853. PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Instances

Instance	Physical Address
SERDES_16G0	0500 C008h
SERDES_16G1	0501 C008h
SERDES_16G2	0502 C008h
SERDES_16G3	0503 C008h

Figure 11-284. PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register

31	30	29	28	27	26	25	24
PHY_PIPE_LANE_DSBL_15_0							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_PIPE_LANE_DSBL_15_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_PIPE_EIE_LOCK_CFG_15_12				PHY_PIPE_EIE_LOCK_CFG_11_8			
R/W-1h				R/W-3h			
7	6	5	4	3	2	1	0
PHY_PIPE_EIE_LOCK_CFG_7_0							
R/W-7Fh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-854. PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_PIPE_LANE_DSBL_15_0	R/W	0h	lane disable: When set the appropriate lane is disabled. Lanes that are disabled will transmit electrical idle and will not return any data on the PIPE RX interface
15-12	PHY_PIPE_EIE_LOCK_CFG_15_12	R/W	1h	EIE lock count fast: The number of EIEOS blocks that need to be seen in the same bit position for the alignment state machine to lock for Gen3/4. The field is used while the PCS is in P0 state after an EIEOS has been seen
11-8	PHY_PIPE_EIE_LOCK_CFG_11_8	R/W	3h	EIE lock count: The number of EIEOS blocks that need to be seen in the same bit position for the alignment state machine to lock for Gen3/4. The field is used while the PCS is transitioning out of a power state change and not performing a rate change
7-0	PHY_PIPE_EIE_LOCK_CFG_7_0	R/W	7Fh	EIE full lock count: The number of EIEOS blocks that need to be seen in the same bit position for the alignment state machine to lock for Gen3/4. The field is used for initial after reset lock or lock after a rate change

Table 11-855. Register Call Summary for PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register \(Offset = C008h\) \[reset = 137Fh\]: \[0\]](#)

11.285 PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register (Offset = C00Ch) [reset = 3C963D09h]

PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH is shown in Figure 11-285 and described in Table 11-857.

Return to [Summary Table](#).

PIPE receiver detect inhibit register ()

Table 11-856. PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Instances

Instance	Physical Address
SERDES_16G0	0500 C00Ch
SERDES_16G1	0501 C00Ch
SERDES_16G2	0502 C00Ch
SERDES_16G3	0503 C00Ch

Figure 11-285. PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register

31	30	29	28	27	26	25	24
PHY_PIPE_RX_ELEC_IDLE_DLY_15_10						PHY_PIPE_RX_ELEC_IDLE_DLY_9_0	
R/W-Fh						R/W-96h	
23	22	21	20	19	18	17	16
PHY_PIPE_RX_ELEC_IDLE_DLY_9_0							
R/W-96h							
15	14	13	12	11	10	9	8
PHY_PIPE_RCV_DET_INH_15_0							
R/W-3D09h							
7	6	5	4	3	2	1	0
PHY_PIPE_RCV_DET_INH_15_0							
R/W-3D09h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-857. PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	PHY_PIPE_RX_ELEC_IDLE_DLY_15_10	R/W	Fh	L1.x exit Rx electrical idle force fast count: Counter load value to hold PIPE Rx Electrical Idle high upon exit from L1.x. Counter is loaded and starts counting down after phy_l*_rx_elec_idle_det_en is asserted high. Default is 500 nsec. This counter runs on cmn_refclk_gated PMA output and accounts for time to power on just the analog Rx signal detect block.
25-16	PHY_PIPE_RX_ELEC_IDLE_DLY_9_0	R/W	96h	L1.x exit Rx electrical idle force full count: Counter load value to hold PIPE Rx Electrical Idle high upon exit from L1.x when the PMA common was powered down. Counter is loaded and starts counting down upon de-assertion of PMA cmn_ref_clk_disable (triggered by de-assertion of phy_l*_ent_l1_x for first link to signal exit from L1.x). Default is 6 usec. This counter accounts for time to power on the bias and decap and only takes effect if the PMA had been suspended.

Table 11-857. PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
15-0	PHY_PIPE_RCV_DET_INH_15_0	R/W	3D09h	<p>Receiver Detect Inhibit Counter Load Value: Counter load value to delay receiver detection request to PMA until PMA common mode is within the required range.</p> <p>The timer (running on divided reference clock from PMA) starts once the PMA common has completed startup.</p> <p>If receiver detect request is received while timer has not expired, the PCS will wait until the timer expires before signaling the request to the PMA.</p> <p>Load value is specified in multiples of 4x the divided reference clock period (typically 40 nsec for 100 MHz reference clock frequency) for a 2.5 msec inhibit time.</p>

Table 11-858. Register Call Summary for PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register \(Offset = C00Ch\) \[reset = 3C963D09h\]: \[0\]](#)

11.286 PHY_ISO_CMN_CTRL Register (Offset = C010h) [reset = X]

PHY_ISO_CMN_CTRL is shown in [Figure 11-286](#) and described in [Table 11-860](#).

Return to [Summary Table](#).

PHY common control signal isolation register

Table 11-859. PHY_ISO_CMN_CTRL Instances

Instance	Physical Address
SERDES_16G0	0500 C010h
SERDES_16G1	0501 C010h
SERDES_16G2	0502 C010h
SERDES_16G3	0503 C010h

Figure 11-286. PHY_ISO_CMN_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_ISO_CMN_CTRL_15_1							
R-0h							
7	6	5	4	3	2	1	0
PHY_ISO_CMN_CTRL_15_1							PHY_ISO_CMN_CTRL_0
R-0h							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-860. PHY_ISO_CMN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-1	PHY_ISO_CMN_CTRL_15_1	R	0h	Reserved
0	PHY_ISO_CMN_CTRL_0	R/W	1h	Drives the phy_reset_n PHY input when in PHY macro and PMA isolation modes.

Table 11-861. Register Call Summary for PHY_ISO_CMN_CTRL

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_ISO_CMN_CTRL Register \(Offset = C010h\) \[reset = X\]: \[0\]](#)

11.287 PHY_STATE_CHG_TIMEOUT Register (Offset = C014h) [reset = X]

PHY_STATE_CHG_TIMEOUT is shown in [Figure 11-287](#) and described in [Table 11-863](#).

Return to [Summary Table](#).

PHY state change monitor timeout

Table 11-862. PHY_STATE_CHG_TIMEOUT Instances

Instance	Physical Address
SERDES_16G0	0500 C014h
SERDES_16G1	0501 C014h
SERDES_16G2	0502 C014h
SERDES_16G3	0503 C014h

Figure 11-287. PHY_STATE_CHG_TIMEOUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_STATE_CHG_TIMEOUT_15_0															
R/W-30D4h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-863. PHY_STATE_CHG_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PHY_STATE_CHG_TIMEOUT_15_0	R/W	30D4h	<p>State change timeout: Bits [19:4] of the state change timeout (bits [3:0] are zero).</p> <p>The timeout is the maximum number of APB clock cycles (abp_pclk) that are allowed for completion of a PHY power state change for the link.</p> <p>If the timeout expires, phy_interrupt_In_XX for the associated lane is asserted and interrupt status register bit is set.</p> <p>For maximum allowed APB clock frequency, this provides 5.2 msec maximum timeout.</p> <p>Default is set for 1 msec for the maximum APB clock frequency.</p>

Table 11-864. Register Call Summary for PHY_STATE_CHG_TIMEOUT

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_STATE_CHG_TIMEOUT Register \(Offset = C014h\) \[reset = X\]: \[0\]](#)

11.288 PHY_AUTO_CFG_CTRL__PHY_PLL_CFG Register (Offset = C01Ch) [reset = 11h]

PHY_AUTO_CFG_CTRL__PHY_PLL_CFG is shown in Figure 11-288 and described in Table 11-866.

Return to [Summary Table](#).

PHY PLL configuration register

Table 11-865.
PHY_AUTO_CFG_CTRL__PHY_PLL_CFG Instances

Instance	Physical Address
SERDES_16G0	0500 C01Ch
SERDES_16G1	0501 C01Ch
SERDES_16G2	0502 C01Ch
SERDES_16G3	0503 C01Ch

Figure 11-288. PHY_AUTO_CFG_CTRL__PHY_PLL_CFG Register

31	30	29	28	27	26	25	24
PHY_AUTO_CFG_CTRL_15_4							
R-0h							
23	22	21	20	19	18	17	16
PHY_AUTO_CFG_CTRL_15_4				PHY_AUTO_C FG_CTRL_3	PHY_AUTO_C FG_CTRL_2	PHY_AUTO_C FG_CTRL_1	PHY_AUTO_C FG_CTRL_0
R-0h				R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
PHY_PLL_CFG_15_10						PHY_PLL_CFG _9	PHY_PLL_CFG _8
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PHY_PLL_CFG_7_4				PHY_PLL_CFG _3	PHY_PLL_CFG _2	PHY_PLL_CFG _1	PHY_PLL_CFG _0
R/W-1h				R-0h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-866. PHY_AUTO_CFG_CTRL__PHY_PLL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PHY_AUTO_CFG_CTRL_15_4	R	0h	Reserved
19	PHY_AUTO_CFG_CTRL_3	R	0h	Auto-configuration complete: 1 = auto-configuration is complete, 0 = not complete. This bit is only functional when PHY is configured to include the auto-configuration logic. Otherwise, this bit is reserved

Table 11-866. PHY_AUTO_CFG_CTRL_PHY_PLL_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	PHY_AUTO_CFG_CTRL_2	R/W	0h	Auto-configuration stall: 1 = .upon completion of PHY auto-configuration, release (de-assertion) of cmn_reset_n to the PMA is prevented until this bit is cleared. This allows registers to be written after auto-configuration has completed as indicated by bit [3]. 0 = reset to PMA is released. Do not set high is bit [0] = 1. This bit is only functional when PHY is configured to include the auto-configuration logic. Otherwise, this bit is reserved.
17	PHY_AUTO_CFG_CTRL_1	R	0h	Reserved
16	PHY_AUTO_CFG_CTRL_0	R/W	0h	Auto-configuration disable: 1 = disables the PHY auto-configuration logic, such that register writes are not performed. 0 = normal operatoin of PHY auto-configuration logic. This bit is only functional when PHY is configured to include the auto-configuration logic. Otherwise, this bit is reserved
15-10	PHY_PLL_CFG_15_10	R	0h	Reserved
9	PHY_PLL_CFG_9	R/W	0h	RefClk1 disable override: When set to 1, overrides asserting cmn_refclk1_disable to the PMA high when the PMA is suspended (i.e. all links in low power state). 0 = normal operation.
8	PHY_PLL_CFG_8	R/W	0h	RefClk disable override: When set to 1, overrides asserting cmn_refclk_disable to the PMA high when the PMA is suspended (i.e. all links in low power state). 0 = normal operation.
7-4	PHY_PLL_CFG_7_4	R/W	1h	Dual port mode port 1 lane number: When configured for dual port mode, this field selects the master lane for port/link 1. (The master lane for port/link 0 is fixed to be lane 0.) Only valid with bit [2] is set.
3	PHY_PLL_CFG_3	R	0h	Reserved
2	PHY_PLL_CFG_2	R/W	0h	Dual port mode enable: 1 = PHY configured for dual port mode. 0 = PHY configured for normal operation (i.e. non-dual port mode).
1	PHY_PLL_CFG_1	R/W	0h	PLL LC only: 0 = PHY configured to only use PLL LC. PLL LC1 disabled. 1 = PHY configured to use both PLL LC and LC1.
0	PHY_PLL_CFG_0	R/W	1h	Single link PCIe configuration: 1 = PHY configured such that there is only 1 PCIe link (1xN). All other links are not PCIe and do not use PLL LC. 0 = All other PHY configurations. Static configuration. Can only be changed while PHY is in reset.

Table 11-867. Register Call Summary for PHY_AUTO_CFG_CTRL__PHY_PLL_CFG

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_AUTO_CFG_CTRL__PHY_PLL_CFG Register \(Offset = C01Ch\) \[reset = 11h\]: \[0\]](#)

11.289 PHY_REFCLK1_DET_THRES_LOW__PHY_REFCLK_DET_THRES_LOW Register (Offset = C020h) [reset = 01C201C2h]

PHY_REFCLK1_DET_THRES_LOW__PHY_REFCLK_DET_THRES_LOW is shown in Figure 11-289 and described in Table 11-869.

Return to [Summary Table](#).

PHY external reference clock detect low threshold register

Table 11-868.
PHY_REFCLK1_DET_THRES_LOW__PHY_REFCLK_DET_THRES_LOW
Instances

Instance	Physical Address
SERDES_16G0	0500 C020h
SERDES_16G1	0501 C020h
SERDES_16G2	0502 C020h
SERDES_16G3	0503 C020h

Figure 11-289. PHY_REFCLK1_DET_THRES_LOW__PHY_REFCLK_DET_THRES_LOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_REFCLK1_DET_THRES_LOW_15_0															
R/W-1C2h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_REFCLK_DET_THRES_LOW_15_0															
R/W-1C2h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-869. PHY_REFCLK1_DET_THRES_LOW__PHY_REFCLK_DET_THRES_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_REFCLK1_DET_THRES_LOW_15_0	R/W	1C2h	External Reference Clock1 Active Detect Low Threshold: This is the minimum number of external reference clock cycles (on cmn_refclk1_p/m) which must be counted during the measurement interval to indicate a valid clock detected. The default value is based on 100MHz reference clock external frequency and 200 MHz (max) apb_pclk frequency.
15-0	PHY_REFCLK_DET_THRES_LOW_15_0	R/W	1C2h	External Reference Clock Active Detect Low Threshold: This is the minimum number of external reference clock cycles (on cmn_refclk_p/m) which must be counted during the measurement interval to indicate a valid clock detected. The default value is based on 100MHz reference clock external frequency and 200 MHz (max) apb_pclk frequency.

Table 11-870. Register Call Summary for
PHY_REFCLK1_DET_THRES_LOW__PHY_REFCLK_DET_THRES_LOW

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_REFCLK1_DET_THRES_LOW__PHY_REFCLK_DET_THRES_LOW Register \(Offset = C020h\) \[reset = 01C201C2h\]: \[0\]](#)

11.290 PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_HIGH Register (Offset = C024h) [reset = 27422742h]

PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_HIGH is shown in [Figure 11-290](#) and described in [Table 11-872](#).

Return to [Summary Table](#).

PHY external reference clock detect high threshold register

Table 11-871.
PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_HIGH
Instances

Instance	Physical Address
SERDES_16G0	0500 C024h
SERDES_16G1	0501 C024h
SERDES_16G2	0502 C024h
SERDES_16G3	0503 C024h

Figure 11-290. PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_HIGH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_REFCLK1_DET_THRES_HIGH_15_0															
R/W-2742h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_REFCLK_DET_THRES_HIGH_15_0															
R/W-2742h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-872. PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_REFCLK1_DET_THRES_HIGH_15_0	R/W	2742h	External Reference Clock1 Active Detect High Threshold: This is the maximum number of external reference clock cycles (on cmn_refclk1_p/m) which must be counted during the measurement interval to indicate a valid clock detected. The default value is based on 100MHz reference clock frequency and 10 MHz apb_pclk frequency.
15-0	PHY_REFCLK_DET_THRES_HIGH_15_0	R/W	2742h	External Reference Clock Active Detect High Threshold: This is the maximum number of external reference clock cycles (on cmn_refclk_p/m) which must be counted during the measurement interval to indicate a valid clock detected. The default value is based on 100MHz reference clock frequency and 10 MHz apb_pclk frequency.

Table 11-873. Register Call Summary for
PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_HIGH

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_REFCLK1_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_HIGH Register \(Offset = C024h\) \[reset = 27422742h\]: \[0\]](#)

11.291 PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_DET_INTERVAL Register (Offset = C028h) [reset = 03E803E8h]

PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_DET_INTERVAL is shown in Figure 11-291 and described in Table 11-875.

Return to [Summary Table](#).

PHY external reference clock detect measurement interval register

Table 11-874.

PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_DET_INTERVAL Instances

Instance	Physical Address
SERDES_16G0	0500 C028h
SERDES_16G1	0501 C028h
SERDES_16G2	0502 C028h
SERDES_16G3	0503 C028h

Figure 11-291. PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_DET_INTERVAL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_REFCLK1_DET_INTERVAL_15_0															
R/W-3E8h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_REFCLK_DET_INTERVAL_15_0															
R/W-3E8h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-875. PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_DET_INTERVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_REFCLK1_DET_INTERVAL_15_0	R/W	3E8h	External Reference Clock1 Active Detect Measurement Interval: This is the number of apb_pclk cycles in which to count external reference clock cycles (on cmn_refclk1_p/m). The default corresponds to 5 us for 200 MHz apb_clk and 100 us for 10 MHz apb_clock.
15-0	PHY_REFCLK_DET_INTERVAL_15_0	R/W	3E8h	External Reference Clock Active Detect Measurement Interval: This is the number of apb_pclk cycles in which to count external reference clock cycles (on cmn_refclk_p/m). The default corresponds to 5 us for 200 MHz apb_clk and 100 us for 10 MHz apb_clock.

**Table 11-876. Register Call Summary for
PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_DET_INTERVAL**

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] PHY_REFCLK1_DET_INTERVAL__PHY_REFCLK_DET_INTERVAL Register (Offset = C028h) [reset = 03E803E8h]: [0]

11.292 PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_DET_OP_DELAY Register (Offset = C02Ch) [reset = 10641064h]

PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_DET_OP_DELAY is shown in Figure 11-292 and described in Table 11-878.

Return to [Summary Table](#).

PHY external reference clock detect delay register

Table 11-877.

PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_DET_OP_DELAY Instances

Instance	Physical Address
SERDES_16G0	0500 C02Ch
SERDES_16G1	0501 C02Ch
SERDES_16G2	0502 C02Ch
SERDES_16G3	0503 C02Ch

Figure 11-292. PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_DET_OP_DELAY Register

31	30	29	28	27	26	25	24
PHY_REFCLK1_DET_OP_DELAY_15_8							
R/W-10h							
23	22	21	20	19	18	17	16
PHY_REFCLK1_DET_OP_DELAY_7_0							
R/W-64h							
15	14	13	12	11	10	9	8
PHY_REFCLK_DET_OP_DELAY_15_8							
R/W-10h							
7	6	5	4	3	2	1	0
PHY_REFCLK_DET_OP_DELAY_7_0							
R/W-64h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-878. PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_DET_OP_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_REFCLK1_DET_OP_DELAY_15_8	R/W	10h	External Reference Clock1 Active Detect End Delay: This is the number of apb_pclk cycles to wait upon completion of measurement interval before capturing the result (accounts for synchronization delays) for measurement on cmn_refclk1_p/m.
23-16	PHY_REFCLK1_DET_OP_DELAY_7_0	R/W	64h	External Reference Clock1 Active Detect Start Delay: This is the number of apb_pclk cycles to wait prior to start of measurement interval (accounts for enable delay of reference clock in PMA) for measurement on cmn_refclk1_p/m.
15-8	PHY_REFCLK_DET_OP_DELAY_15_8	R/W	10h	External Reference Clock Active Detect End Delay: This is the number of apb_pclk cycles to wait upon completion of measurement interval before capturing the result (accounts for synchronization delays) for measurement on cmn_refclk_p/m.
7-0	PHY_REFCLK_DET_OP_DELAY_7_0	R/W	64h	External Reference Clock Active Detect Start Delay: This is the number of apb_pclk cycles to wait prior to start of measurement interval (accounts for enable delay of reference clock in PMA) for measurement on cmn_refclk_p/m.

**Table 11-879. Register Call Summary for
PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_DET_OP_DELAY**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_REFCLK1_DET_OP_DELAY__PHY_REFCLK_DET_OP_DELAY Register \(Offset = C02Ch\) \[reset = 10641064h\]: \[0\]](#)

11.293 PHY_REFCLK_DET_ISO_CTRL Register (Offset = C030h) [reset = X]

PHY_REFCLK_DET_ISO_CTRL is shown in [Figure 11-293](#) and described in [Table 11-881](#).

Return to [Summary Table](#).

PHY external reference clock detect isolation control register

**Table 11-880. PHY_REFCLK_DET_ISO_CTRL
Instances**

Instance	Physical Address
SERDES_16G0	0500 C030h
SERDES_16G1	0501 C030h
SERDES_16G2	0502 C030h
SERDES_16G3	0503 C030h

Figure 11-293. PHY_REFCLK_DET_ISO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_REFCLK_DET_ISO_CTRL_15_14	PHY_REFCLK_DET_ISO_CTRL_L_13	PHY_REFCLK_DET_ISO_CTRL_L_12	PHY_REFCLK_DET_ISO_CTRL_L_11	PHY_REFCLK_DET_ISO_CTRL_L_10	PHY_REFCLK_DET_ISO_CTRL_L_9	PHY_REFCLK_DET_ISO_CTRL_L_8	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PHY_REFCLK_DET_ISO_CTRL_7_2						PHY_REFCLK_DET_ISO_CTRL_L_1	PHY_REFCLK_DET_ISO_CTRL_L_0
R-0h						W-0h	W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 11-881. PHY_REFCLK_DET_ISO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	PHY_REFCLK_DET_ISO_CTRL_15_14	R	0h	Reserved
13	PHY_REFCLK_DET_ISO_CTRL_13	R	0h	Captures the current value of the pma_cm_n_ext_refclk1_detected_cfg PHY input.
12	PHY_REFCLK_DET_ISO_CTRL_12	R	0h	Captures the current value of the pma_cm_n_ext_refclk1_detected_cfg PHY input.
11	PHY_REFCLK_DET_ISO_CTRL_11	R	0h	Current value of pma_cm_n_ext_refclk1_detected PHY output.
10	PHY_REFCLK_DET_ISO_CTRL_10	R	0h	Current value of pma_cm_n_ext_refclk1_detected_valid PHY output.
9	PHY_REFCLK_DET_ISO_CTRL_9	R	0h	Current value of pma_cm_n_ext_refclk1_detected PHY output.
8	PHY_REFCLK_DET_ISO_CTRL_8	R	0h	Current value of pma_cm_n_ext_refclk1_detected_valid PHY output.
7-2	PHY_REFCLK_DET_ISO_CTRL_7_2	R	0h	Reserved

Table 11-881. PHY_REFCLK_DET_ISO_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PHY_REFCLK_DET_ISO_CTRL_1	W	0h	External Reference Clock1 Active Detect Start: Write with 1 to initiate an external reference clock active detect operation on cmn_refclk1_p/m. Any previous operation must have completed prior to writing with 1.
0	PHY_REFCLK_DET_ISO_CTRL_0	W	0h	External Reference Clock Active Detect Start: Write with 1 to initiate an external reference clock active detect operation on cmn_refclk_p/m. Any previous operation must have completed prior to writing with 1.

Table 11-882. Register Call Summary for PHY_REFCLK_DET_ISO_CTRL

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_REFCLK_DET_ISO_CTRL Register \(Offset = C030h\) \[reset = X\]: \[0\]](#)

11.294 PHY_PIPE_LM_CFG0 Register (Offset = C034h) [reset = X]

PHY_PIPE_LM_CFG0 is shown in [Figure 11-294](#) and described in [Table 11-884](#).

Return to [Summary Table](#).

PHY PIPE lane margining configuration 0 register (#)

Table 11-883. PHY_PIPE_LM_CFG0 Instances

Instance	Physical Address
SERDES_16G0	0500 C034h
SERDES_16G1	0501 C034h
SERDES_16G2	0502 C034h
SERDES_16G3	0503 C034h

Figure 11-294. PHY_PIPE_LM_CFG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_PIPE_LM_CFG0_15_8								PHY_PIPE_LM_CFG0_7_0							
R-0h								R/W-4Bh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-X															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-884. PHY_PIPE_LM_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_LM_CFG0_15_8	R	0h	Reserved
23-16	PHY_PIPE_LM_CFG0_7_0	R/W	4Bh	Lane margining direction configuration: Maps the PIPE margin direction encoding to the PMA margin direction encoding:
15-0	RESERVED	R/W	X	

Table 11-885. Register Call Summary for PHY_PIPE_LM_CFG0

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_LM_CFG0 Register \(Offset = C034h\) \[reset = X\]: \[0\]](#)

11.295 PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1 Register (Offset = C038h) [reset = 817F0336h]

PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1 is shown in [Figure 11-295](#) and described in [Table 11-887](#).

Return to [Summary Table](#).

PHY PIPE lane margining configuration 1 register (#)

Table 11-886.
PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1
Instances

Instance	Physical Address
SERDES_16G0	0500 C038h
SERDES_16G1	0501 C038h
SERDES_16G2	0502 C038h
SERDES_16G3	0503 C038h

Figure 11-295. PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1 Register

31	30	29	28	27	26	25	24
PHY_PIPE_LM_CFG2_15_8							
R/W-81h							
23	22	21	20	19	18	17	16
PHY_PIPE_LM_CFG2_7_0							
R/W-7Fh							
15	14	13	12	11	10	9	8
PHY_PIPE_LM_CFG1_15_12				PHY_PIPE_LM_CFG1_11_8			
R-0h				R/W-3h			
7	6	5	4	3	2	1	0
PHY_PIPE_LM_CFG1_7_6		PHY_PIPE_LM_CFG1_5_0					
R-0h		R/W-36h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-887. PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_LM_CFG2_15_8	R/W	81h	Lane margining sample count threshold: This is the sample count saturation point.
23-16	PHY_PIPE_LM_CFG2_7_0	R/W	7Fh	Lane margining sample count maximum: This is sample count value reported whenever total sample count value X= sample count threshold (bits [15:8]).
15-12	PHY_PIPE_LM_CFG1_15_12	R	0h	Reserved
11-8	PHY_PIPE_LM_CFG1_11_8	R/W	3h	Lane margining wait time: This is wait time at PMA interface between setting PMA inputs rx_mrgn_offset and rx_mrgn_dir before asserting rx_mrgn_req.
7-6	PHY_PIPE_LM_CFG1_7_6	R	0h	Reserved
5-0	PHY_PIPE_LM_CFG1_5_0	R/W	36h	Lane margining sample count 3 logn value: This is the value of 3 * logn (number of samples per PMA eye surf iteration).

Table 11-888. Register Call Summary for PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_LM_CFG2__PHY_PIPE_LM_CFG1 Register \(Offset = C038h\) \[reset = 817F0336h\]: \[0\]](#)

11.296 PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3 Register (Offset = C03Ch) [reset = 7F203F3Fh]

PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3 is shown in [Figure 11-296](#) and described in [Table 11-890](#).

Return to [Summary Table](#).

PHY PIPE lane margining configuration 3 register (#)

Table 11-889.
PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3
Instances

Instance	Physical Address
SERDES_16G0	0500 C03Ch
SERDES_16G1	0501 C03Ch
SERDES_16G2	0502 C03Ch
SERDES_16G3	0503 C03Ch

Figure 11-296. PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3 Register

31	30	29	28	27	26	25	24
PHY_PIPE_LM_CFG4_15	PHY_PIPE_LM_CFG4_14_8						
R-0h				R/W-7Fh			
23	22	21	20	19	18	17	16
PHY_PIPE_LM_CFG4_7_6		PHY_PIPE_LM_CFG4_5_0					
R-0h				R/W-20h			
15	14	13	12	11	10	9	8
PHY_PIPE_LM_CFG3_15_14		PHY_PIPE_LM_CFG3_13_8					
R-0h				R/W-3Fh			
7	6	5	4	3	2	1	0
PHY_PIPE_LM_CFG3_7_6		PHY_PIPE_LM_CFG3_5_0					
R-0h				R/W-3Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-890. PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PIPE_LM_CFG4_15	R	0h	Reserved
30-24	PHY_PIPE_LM_CFG4_14_8	R/W	7Fh	Lane margining maximum voltage offset: This is the maximum voltage offset supported by the PMA.
23-22	PHY_PIPE_LM_CFG4_7_6	R	0h	Reserved
21-16	PHY_PIPE_LM_CFG4_5_0	R/W	20h	Lane margining maximum timing offset: This is the maximum timing offset supported by the PMA
15-14	PHY_PIPE_LM_CFG3_15_14	R	0h	Reserved
13-8	PHY_PIPE_LM_CFG3_13_8	R/W	3Fh	Lane margining error count threshold: Maximum total error count. Error count reported saturates at this value.
7-6	PHY_PIPE_LM_CFG3_7_6	R	0h	Reserved
5-0	PHY_PIPE_LM_CFG3_5_0	R/W	3Fh	Lane margining error count maximum: This is the error count reported, whenever the total error count value X= error count threshold (bits [13:8]).

Table 11-891. Register Call Summary for PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_LM_CFG4__PHY_PIPE_LM_CFG3 Register \(Offset = C03Ch\) \[reset = 7F203F3Fh\]: \[0\]](#)

11.297 PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0 Register (Offset = C040h) [reset = 1010h]

PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0 is shown in Figure 11-297 and described in Table 11-893.

Return to [Summary Table](#).

PHY USB3 Gen 2 pre-shoot configuration 0 register ()

Table 11-892.
PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0
Instances

Instance	Physical Address
SERDES_16G0	0500 C040h
SERDES_16G1	0501 C040h
SERDES_16G2	0502 C040h
SERDES_16G3	0503 C040h

Figure 11-297. PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0 Register

31	30	29	28	27	26	25	24
PHY_PIPE_USB3_GEN2_PRE_CFG1_15_8							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_PIPE_USB3_GEN2_PRE_CFG1_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_PIPE_USB3_GEN2_PRE_CFG0_15_8							
R/W-10h							
7	6	5	4	3	2	1	0
PHY_PIPE_USB3_GEN2_PRE_CFG0_7_0							
R/W-10h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-893. PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_USB3_GEN2_PRE_CFG1_15_8	R/W	0h	USB3 Gen 2 transmit pre-shoot multiplier configuration 3: For a lane configured for USB3 mode at Gen 3 data rate, sets the multiplier configuration for the Tx de-emphasis pre-shoot (C-1) when pipe_IXX_tx_deemphasis [1:0] == 0b11 for the associated lane. Default: 0.
23-16	PHY_PIPE_USB3_GEN2_PRE_CFG1_7_0	R/W	0h	USB3 Gen 2 transmit pre-shoot multiplier configuration 2: For a lane configured for USB3 mode at Gen 3 data rate, sets the multiplier configuration for the Tx de-emphasis pre-shoot (C1) when pipe_IXX_tx_deemphasis [1:0] == 0b10 for the associated lane. Default: 0.

Table 11-893. PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	PHY_PIPE_USB3_GEN2_PRE_CFG0_15_8	R/W	10h	USB3 Gen 2 transmit pre-shoot multiplier configuration 1: For a lane configured for USB3 mode at Gen 3 data rate, sets the multiplier configuration for the Tx de-emphasis pre-shoot (C-1) when pipe_IXX_tx_deemphasis [1:0] == 0b01 for the associated lane. Default: 1/8.
7-0	PHY_PIPE_USB3_GEN2_PRE_CFG0_7_0	R/W	10h	USB3 Gen 2 transmit pre-shoot multiplier configuration 0: For a lane configured for USB3 mode at Gen 3 data rate, sets the multiplier configuration for the Tx de-emphasis pre-shoot (C-1) when pipe_IXX_tx_deemphasis [1:0] == 0b00 for the associated lane. The multiplier is set based on: Default: 1/8.

**Table 11-894. Register Call Summary for
PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_USB3_GEN2_PRE_CFG1__PHY_PIPE_USB3_GEN2_PRE_CFG0 Register \(Offset = C040h\) \[reset = 1010h\]: \[0\]](#)

11.298 PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0 Register (Offset = C044h) [reset = 000A0A00h]

PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0 is shown in Figure 11-298 and described in Table 11-896.

Return to [Summary Table](#).

PHY USB3 Gen 2 de-emphasis configuration 0 register ()

Table 11-895.
PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0
Instances

Instance	Physical Address
SERDES_16G0	0500 C044h
SERDES_16G1	0501 C044h
SERDES_16G2	0502 C044h
SERDES_16G3	0503 C044h

Figure 11-298. PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0 Register

31	30	29	28	27	26	25	24
PHY_PIPE_USB3_GEN2_POST_CFG1_15_8							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_PIPE_USB3_GEN2_POST_CFG1_7_0							
R/W-Ah							
15	14	13	12	11	10	9	8
PHY_PIPE_USB3_GEN2_POST_CFG0_15_8							
R/W-Ah							
7	6	5	4	3	2	1	0
PHY_PIPE_USB3_GEN2_POST_CFG0_7_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-896. PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0 Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_USB3_GEN2_POST_CFG1_15_8	R/W	0h	USB3 Gen 2 transmit pre-shoot multiplier configuration 3: For a lane configured for USB3 mode at Gen 3 data rate, sets the multiplier configuration for the Tx de-emphasis (C1) when pipe_IXX_tx_deemphasis[1:0] == 0b11 for the associated lane. Default: 0.
23-16	PHY_PIPE_USB3_GEN2_POST_CFG1_7_0	R/W	Ah	USB3 Gen 2 transmit pre-shoot multiplier configuration 2: For a lane configured for USB3 mode at Gen 3 data rate, sets the multiplier configuration for the Tx de-emphasis (C1) when pipe_IXX_tx_deemphasis[1:0] == 0b10 for the associated lane. Default: 5/64.
15-8	PHY_PIPE_USB3_GEN2_POST_CFG0_15_8	R/W	Ah	USB3 Gen 2 transmit pre-shoot multiplier configuration 1: For a lane configured for USB3 mode at Gen 3 data rate, sets the multiplier configuration for the Tx de-emphasis (C1) when pipe_IXX_tx_deemphasis[1:0] == 0b01 for the associated lane. Default: 5/64.

**Table 11-896. PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0 Register
Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
7-0	PHY_PIPE_USB3_GEN2_POST_CFG0_7_0	R/W	0h	USB3 Gen 2 transmit pre-shoot multiplier configuration 0: For a lane configured for USB3 mode at Gen 3 data rate, sets the multiplier configuration for the Tx de-emphasis (C1) when pipe_IXX_tx_deemphasis[1:0] == 0b00 for the associated lane. Default: 0.

**Table 11-897. Register Call Summary for
PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_USB3_GEN2_POST_CFG1__PHY_PIPE_USB3_GEN2_POST_CFG0 Register \(Offset = C044h\) \[reset = 000A0A00h\]: \[0\]](#)

11.299 PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register (Offset = D000h + formula) [reset = 0h]

PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j is shown in Figure 11-299 and described in Table 11-899.

Return to [Summary Table](#).

PIPE TX control signal isolation register ()

Offset = D000h + (j * 200h); where j = 0h to 1h

Table 11-898. PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Instances

Instance	Physical Address
SERDES_16G0	0500 D000h + formula
SERDES_16G1	0501 D000h + formula
SERDES_16G2	0502 D000h + formula
SERDES_16G3	0503 D000h + formula

Figure 11-299. PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_TX_LPC_LO_1_5_14		PHY_PIPE_ISO_TX_LPC_LO_13_8					
R-0h		R-0h					
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_TX_LPC_LO_7_6		PHY_PIPE_ISO_TX_LPC_LO_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_TX_CTRL_15_12				PHY_PIPE_ISO_TX_CTRL_11_9		PHY_PIPE_ISO_TX_CTRL_8	
R/W-0h				R-0h		R/W-0h	
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_TX_CTRL_7_5			PHY_PIPE_ISO_TX_CTRL_4	PHY_PIPE_ISO_TX_CTRL_3	PHY_PIPE_ISO_TX_CTRL_2	PHY_PIPE_ISO_TX_CTRL_1_0	
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-899. PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PIPE_ISO_TX_LPC_LO_15_14	R	0h	Reserved
29-24	PHY_PIPE_ISO_TX_LPC_LO_13_8	R	0h	Current value of pipe_tx_local_tx_preset_coefficients[11:6] for the associated lane when PHY_PCS_ISO_TX_LPC_HI[15] == 1. Otherwise, 0.
23-22	PHY_PIPE_ISO_TX_LPC_LO_7_6	R	0h	Reserved
21-16	PHY_PIPE_ISO_TX_LPC_LO_5_0	R	0h	Current value of pipe_tx_local_tx_preset_coefficients[5:0] for the associated lane when PHY_PCS_ISO_TX_LPC_HI[15] == 1. Otherwise, 0.
15-12	PHY_PIPE_ISO_TX_CTRL_15_12	R/W	0h	Drives pipe_tx_data_k PHY input for the associated lane when in PHY macro and PMA isolation modes.

**Table 11-899. PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
11-9	PHY_PIPE_ISO_TX_CTR L_11_9	R	0h	Reserved
8	PHY_PIPE_ISO_TX_CTR L_8	R/W	0h	Drives pipe_tx_ones_zeros input for the associated lane when in PHY macro and PMA isolation modes.
7-5	PHY_PIPE_ISO_TX_CTR L_7_5	R	0h	Reserved
4	PHY_PIPE_ISO_TX_CTR L_4	R/W	0h	Drives pipe_tx_elec_idle PHY input for the associated lane when in PHY macro and PMA isolation modes.
3	PHY_PIPE_ISO_TX_CTR L_3	R/W	0h	Drives pipe_tx_128b_enc_byp PHY input for the associated lane when in PHY macro and PMA isolation modes.
2	PHY_PIPE_ISO_TX_CTR L_2	R/W	0h	Drives pipe_tx_compliance PHY input for the associated lane when in PHY macro and PMA isolation modes.
1-0	PHY_PIPE_ISO_TX_CTR L_1_0	R/W	0h	Drives pipe_tx_pattern PHY input for the associated lane when in PHY macro and PMA isolation modes.

Table 11-900. Register Call Summary for PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register \(Offset = D000h + formula\) \[reset = 0h\]: \[0\]](#)

11.300 PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register (Offset = D004h + formula) [reset = 0h]

PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j is shown in Figure 11-300 and described in Table 11-902.

Return to [Summary Table](#).

PIPE TX local preset coefficients high isolation register ()

Offset = D004h + (j * 200h); where j = 0h to 1h

Table 11-901. PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Instances

Instance	Physical Address
SERDES_16G0	0500 D004h + formula
SERDES_16G1	0501 D004h + formula
SERDES_16G2	0502 D004h + formula
SERDES_16G3	0503 D004h + formula

Figure 11-300. PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_TX_DMPH_LO_15_14		PHY_PIPE_ISO_TX_DMPH_LO_13_8					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_TX_DMPH_LO_7_6		PHY_PIPE_ISO_TX_DMPH_LO_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_TX_LPC_HI_1_5	PHY_PIPE_ISO_TX_LPC_HI_1_4	PHY_PIPE_ISO_TX_LPC_HI_1_3	PHY_PIPE_ISO_TX_LPC_HI_12_8				
R-0h	R-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_TX_LPC_HI_7_6		PHY_PIPE_ISO_TX_LPC_HI_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-902. PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PIPE_ISO_TX_DMPH_LO_15_14	R	0h	Reserved
29-24	PHY_PIPE_ISO_TX_DMPH_LO_13_8	R/W	0h	Drives pipe_tx_deemph[11:6] PHY input for the associated lane when in PHY macro and PMA isolation modes.
23-22	PHY_PIPE_ISO_TX_DMPH_LO_7_6	R	0h	Reserved
21-16	PHY_PIPE_ISO_TX_DMPH_LO_5_0	R/W	0h	Drives pipe_tx_deemph[5:0] PHY input for the associated lane when in PHY macro and PMA isolation modes.
15	PHY_PIPE_ISO_TX_LPC_HI_15	R	0h	Set upon assertion of pipe_tx_local_tx_coeff_vld PHY output for the associated lane. Cleared upon writing PHY_PCS_ISO_TX_LPC_HI[13] with a 0.

**Table 11-902. PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
14	PHY_PIPE_ISO_TX_LPC_HI_14	R	0h	Reserved
13	PHY_PIPE_ISO_TX_LPC_HI_13	R/W	0h	Drives pipe_tx_get_local_preset_coef PHY output for the associated lane when in PHY macro and PMA isolation modes
12-8	PHY_PIPE_ISO_TX_LPC_HI_12_8	R/W	0h	Drives pipe_tx_local_preset_index PHY output for the associated lane when in PHY macro and PMA isolation modes.
7-6	PHY_PIPE_ISO_TX_LPC_HI_7_6	R	0h	Reserved
5-0	PHY_PIPE_ISO_TX_LPC_HI_5_0	R	0h	Current value of pipe_tx_local_tx_preset_coefficients[17:12] for the associated lane when PHY_PCS_ISO_TX_LPC_HI[15] == 1. Otherwise, 0.

Table 11-903. Register Call Summary for PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register \(Offset = D004h + formula\) \[reset = 0h\]: \[0\]](#)

11.301 PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Register (Offset = D008h + formula) [reset = 0h]

PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j is shown in Figure 11-301 and described in Table 11-905.

Return to [Summary Table](#).

PIPE TX deemphasis isolation register ()

Offset = D008h + (j * 200h); where j = 0h to 1h

Table 11-904. PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Instances

Instance	Physical Address
SERDES_16G0	0500 D008h + formula
SERDES_16G1	0501 D008h + formula
SERDES_16G2	0502 D008h + formula
SERDES_16G3	0503 D008h + formula

Figure 11-301. PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_TX_FSLF_15_14		PHY_PIPE_ISO_TX_FSLF_13_8					
R-0h		R-0h					
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_TX_FSLF_7_6		PHY_PIPE_ISO_TX_FSLF_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_TX_DMPH_HI_15_6							
R-0h							
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_TX_DMPH_HI_15_6		PHY_PIPE_ISO_TX_DMPH_HI_5_0					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-905. PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PIPE_ISO_TX_FSLF_15_14	R	0h	Reserved
29-24	PHY_PIPE_ISO_TX_FSLF_13_8	R	0h	Current value of pipe_tx_local_fs PHY output for the associated lane. (Not re-synchronized to apb_pclk)
23-22	PHY_PIPE_ISO_TX_FSLF_7_6	R	0h	Reserved
21-16	PHY_PIPE_ISO_TX_FSLF_5_0	R	0h	Current value of pipe_tx_local_if PHY output for the associated lane. (Not re-synchronized to apb_pclk)
15-6	PHY_PIPE_ISO_TX_DMPH_HI_15_6	R	0h	Reserved
5-0	PHY_PIPE_ISO_TX_DMPH_HI_5_0	R/W	0h	Drives pipe_tx_deemph[17:12] PHY input for the associated lane when in PHY macro and PMA isolation modes.

Table 11-906. Register Call Summary for PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Register \(Offset = D008h + formula\) \[reset = 0h\]: \[0\]](#)

11.302 PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j Register (Offset = D00Ch + formula) [reset = 0h]

PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j is shown in Figure 11-302 and described in Table 11-908.

Return to [Summary Table](#).

PIPE TX data lower isolation register ()

Offset = D00Ch + (j * 200h); where j = 0h to 1h

Table 11-907. PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j Instances

Instance	Physical Address
SERDES_16G0	0500 D00Ch + formula
SERDES_16G1	0501 D00Ch + formula
SERDES_16G2	0502 D00Ch + formula
SERDES_16G3	0503 D00Ch + formula

Figure 11-302. PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_PIPE_ISO_TX_DATA_HI_15_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PIPE_ISO_TX_DATA_LO_15_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-908. PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_PIPE_ISO_TX_DATA_HI_15_0	R/W	0h	Drives pipe_tx_data[31:16] PHY input for the associated lane when in PHY macro and PMA isolation modes.
15-0	PHY_PIPE_ISO_TX_DATA_LO_15_0	R/W	0h	Drives pipe_tx_data[15:0] PHY input for the associated lane when in PHY macro and PMA isolation modes.

Table 11-909. Register Call Summary for PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] PHY_PIPE_ISO_TX_DATA_HI__PHY_PIPE_ISO_TX_DATA_LO_j Register (Offset = D00Ch + formula) [reset = 0h]: [0]

11.303 PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j Register (Offset = D010h + formula) [reset = 00400010h]

PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j is shown in Figure 11-303 and described in Table 11-911.

Return to [Summary Table](#).

PIPE RX control signal isolation register ()

Offset = D010h + (j * 200h); where j = 0h to 1h

**Table 11-910. PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 D010h + formula
SERDES_16G1	0501 D010h + formula
SERDES_16G2	0502 D010h + formula
SERDES_16G3	0503 D010h + formula

Figure 11-303. PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_RX_EQ_EVAL_15_13			PHY_PIPE_ISO_RX_EQ_EVAL_12	PHY_PIPE_ISO_RX_EQ_EVAL_11	PHY_PIPE_ISO_RX_EQ_EVAL_10	PHY_PIPE_ISO_RX_EQ_EVAL_9	PHY_PIPE_ISO_RX_EQ_EVAL_8
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_RX_EQ_EVAL_7	PHY_PIPE_ISO_RX_EQ_EVAL_6	PHY_PIPE_ISO_RX_EQ_EVAL_5_0					
R-0h	R-1h	R-0h					
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_RX_CTRL_15_12				PHY_PIPE_ISO_RX_CTRL_11_10	PHY_PIPE_ISO_RX_CTRL_9	PHY_PIPE_ISO_RX_CTRL_8	
R-0h				R-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_RX_CTRL_7	PHY_PIPE_ISO_RX_CTRL_6	PHY_PIPE_ISO_RX_CTRL_5	PHY_PIPE_ISO_RX_CTRL_4	PHY_PIPE_ISO_RX_CTRL_3	PHY_PIPE_ISO_RX_CTRL_2_0		
R/W-0h	R-0h	R-0h	R-1h	R-0h	R-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-911. PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	PHY_PIPE_ISO_RX_EQ_EVAL_15_13	R	0h	Reserved
28	PHY_PIPE_ISO_RX_EQ_EVAL_12	R/W	0h	Drives pipe_rx_invalid_request PHY input for the associated lane when in PHY macro and PMA isolation modes.
27	PHY_PIPE_ISO_RX_EQ_EVAL_11	R/W	0h	pipe_link_eval_dir_change[5:4] bit reversal enable. When low, no bit reversal. When high, the bit positions for pipe_link_eval_dir_change[5:4] PHY output for the associated lane are reversed.

**Table 11-911. PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26	PHY_PIPE_ISO_RX_EQ_EVAL_10	R/W	0h	pipe_link_eval_dir_change[3:2] bit reversal enable. When low, no bit reversal. When high, the bit positions for pipe_link_eval_dir_change[3:2] PHY output for the associated lane are reversed.
25	PHY_PIPE_ISO_RX_EQ_EVAL_9	R/W	0h	pipe_link_eval_dir_change[1:0] bit reversal enable. When low, no bit reversal. When high, the bit positions for pipe_link_eval_dir_change[1:0] PHY output for the associated lane are reversed.]
24	PHY_PIPE_ISO_RX_EQ_EVAL_8	R/W	0h	Drives pipe_rx_eval PHY input for the associated lane when in PHY macro and PMA isolation modes.
23	PHY_PIPE_ISO_RX_EQ_EVAL_7	R	0h	Reserved
22	PHY_PIPE_ISO_RX_EQ_EVAL_6	R	1h	Captures pipe_phy_status for Rx equalization evaluation PHY output for the associated lane (does not include power state change signaling). Set when pipe_phy_status is high. Cleared upon read.
21-16	PHY_PIPE_ISO_RX_EQ_EVAL_5_0	R	0h	pipe_link_eval_dir_change PHY output for the associated lane (prior to bit reversal logic) upon completion of Rx equalization evaluation. Captured upon assertion of Rx equalization eval pipe_phy_status when PHY_PCS_ISO_RX_EQ_EVAL[8] == 1. Cleared upon de-assertion of PHY_PCS_ISO_RX_EQ_EVAL[8]. (Not re-synchronized to apb_pclk)
15-12	PHY_PIPE_ISO_RX_CTRL_15_12	R	0h	Current value of pipe_rx_data_k PHY output for the associated lane, when PHY_PCS_ISO_RX_CTRL[6] == 1. Otherwise, 0. (Not re-synchronized to apb_pclk)
11-10	PHY_PIPE_ISO_RX_CTRL_11_10	R	0h	Reserved
9	PHY_PIPE_ISO_RX_CTRL_9	R/W	0h	Drives pipe_rx_eq_training PHY input for the associated lane when in PHY macro and PMA isolation modes.
8	PHY_PIPE_ISO_RX_CTRL_8	R/W	0h	Drives pipe_rx_termination PHY input for the associated lane when in PHY macro and PMA isolation modes.
7	PHY_PIPE_ISO_RX_CTRL_7	R/W	0h	Drives pipe_rx_polarity PHY output for the associated lane when in PHY macro and PMA isolation modes.
6	PHY_PIPE_ISO_RX_CTRL_6	R	0h	Reserved
5	PHY_PIPE_ISO_RX_CTRL_5	R	0h	Current value of pipe_rx_valid PHY output for the associated lane.
4	PHY_PIPE_ISO_RX_CTRL_4	R	1h	Current value of pipe_rx_elec_idle PHY output for the associated lane.
3	PHY_PIPE_ISO_RX_CTRL_3	R	0h	Captures pipe_align_detect for PHY output for the associated lane. Set when pipe_align_detect is high. Clear upon read.
2-0	PHY_PIPE_ISO_RX_CTRL_2_0	R	0h	Current value of pipe_rx_status PHY output for the associated lane. Holds the highest priority pipe_rx_status value seen, since the last register read. Clear upon read.

Table 11-912. Register Call Summary for PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PIPE_ISO_RX_CTRL_j Register \(Offset = D010h + formula\) \[reset = 00400010h\]: \[0\]](#)

11.304 PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register (Offset = D014h + formula) [reset = 00230000h]

PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j is shown in Figure 11-304 and described in Table 11-914.

Return to [Summary Table](#).

PHY Link configuration isolation register

Offset = D014h + (j * 200h); where j = 0h to 1h

Table 11-913.
PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j
Instances

Instance	Physical Address
SERDES_16G0	0500 D014h + formula
SERDES_16G1	0501 D014h + formula
SERDES_16G2	0502 D014h + formula
SERDES_16G3	0503 D014h + formula

Figure 11-304. PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register

31	30	29	28	27	26	25	24
PHY_ISO_LINK_CTRL_15	PHY_ISO_LINK_CTRL_14	PHY_ISO_LINK_CTRL_13	PHY_ISO_LINK_CTRL_12	PHY_ISO_LINK_CTRL_11	PHY_ISO_LINK_CTRL_10	PHY_ISO_LINK_CTRL_9_8	
R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	
23	22	21	20	19	18	17	16
PHY_ISO_LINK_CTRL_7	PHY_ISO_LINK_CTRL_6_4			PHY_ISO_LINK_CTRL_3	PHY_ISO_LINK_CTRL_2	PHY_ISO_LINK_CTRL_1	PHY_ISO_LINK_CTRL_0
R-0h	R/W-2h			R-0h	R/W-0h	R-1h	R/W-1h
15	14	13	12	11	10	9	8
PHY_ISO_LINK_CFG_15	PHY_ISO_LINK_CFG_14_13		PHY_ISO_LINK_CFG_12	PHY_ISO_LINK_CFG_11_6			
R/W-0h	R-0h		R/W-0h	R-0h			
7	6	5	4	3	2	1	0
PHY_ISO_LINK_CFG_11_6		PHY_ISO_LINK_CFG_5	PHY_ISO_LINK_CFG_4	PHY_ISO_LINK_CFG_3	PHY_ISO_LINK_CFG_2	PHY_ISO_LINK_CFG_1_0	
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-914. PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_ISO_LINK_CTRL_15	R	0h	Current value of pma_l{nnnn}_pwr_en_ack PHY output.
30	PHY_ISO_LINK_CTRL_14	R/W	0h	Drives pma_l{nnnn}_pwr_en PHY input when in PHY macro and PMA isolation modes.
29	PHY_ISO_LINK_CTRL_13	R	0h	Current value of phy_l{nnnn}_ack_l1_x PHY output.
28	PHY_ISO_LINK_CTRL_12	R/W	0h	Drives phy_l{nnnn}_ent_l1_x PHY input when in PHY macro and PMA isolation modes.
27	PHY_ISO_LINK_CTRL_11	R/W	0h	Drives phy_l{nnnn}_rx_elec_idle_det_en PHY input when in PHY macro and PMA isolation modes.
26	PHY_ISO_LINK_CTRL_10	R/W	0h	Drives phy_l{nnnn}_tx_cm_n_mode_en PHY input when in PHY macro and PMA isolation modes.

Table 11-914. PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-24	PHY_ISO_LINK_CTRL_9_8	R/W	0h	Drives pipe_l{nnnn}_rate PHY input when in PHY macro and PMA isolation modes.
23	PHY_ISO_LINK_CTRL_7	R	0h	Reserved
22-20	PHY_ISO_LINK_CTRL_6_4	R/W	2h	Drives pipe_l{nnnn}_powerdown PHY input when in PHY macro and PMA isolation modes.
19	PHY_ISO_LINK_CTRL_3	R	0h	Reserved
18	PHY_ISO_LINK_CTRL_2	R/W	0h	Drives pipe_l{nnnn}_tx_det_rx_lpbk PHY input when in PHY macro and PMA isolation modes.
17	PHY_ISO_LINK_CTRL_1	R	1h	Captures pipe_l{nnnn}_phy_status for power state change PHY output (does not include Rx equalization signaling). Set when pipe_phy_status is high and cleared upon read if pipe_phy_status is low.
16	PHY_ISO_LINK_CTRL_0	R/W	1h	Drives phy_l{nnnn}_reset_n PHY input when in PHY macro and PMA isolation modes.
15	PHY_ISO_LINK_CFG_15	R/W	0h	Drives phy_link_cfg_ln_{nnnn} PHY input when in PHY macro and PMA isolation modes.
14-13	PHY_ISO_LINK_CFG_14_13	R	0h	Reserved
12	PHY_ISO_LINK_CFG_12	R/W	0h	Drives pipe_l{nnnn}_32bit_sel PHY input when in PHY macro and PMA isolation modes.
11-6	PHY_ISO_LINK_CFG_11_6	R	0h	Reserved
5	PHY_ISO_LINK_CFG_5	R/W	0h	Drives phy_l{nnnn}_pcie_l1_ss_sel PHY input when in PHY macro and PMA isolation modes.
4	PHY_ISO_LINK_CFG_4	R/W	0h	Drives pipe_l{nnnn}_eb_mode PHY input when in PHY macro and PMA isolation modes.
3	PHY_ISO_LINK_CFG_3	R/W	0h	Drives phy_eth_mode PHY input for the associated lane when in PHY macro and PMA isolation modes.
2	PHY_ISO_LINK_CFG_2	R/W	0h	Drives phy_eth_mode_en PHY input for the associated lane when in PHY macro and PMA isolation modes.
1-0	PHY_ISO_LINK_CFG_1_0	R/W	0h	Drives phy_l{nnnn}_mode PHY input when in PHY macro and PMA isolation modes.

Table 11-915. Register Call Summary for PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register \(Offset = D014h + formula\) \[reset = 00230000h\]: \[0\]](#)

11.305 PHY_PIPE_ISO_USB_BER_CNT_j Register (Offset = D018h + formula) [reset = X]

PHY_PIPE_ISO_USB_BER_CNT_j is shown in Figure 11-305 and described in Table 11-917.

Return to [Summary Table](#).

PIPE USB loopback slave BER count register ()

Offset = D018h + (j * 200h); where j = 0h to 1h

Table 11-916. PHY_PIPE_ISO_USB_BER_CNT_j Instances

Instance	Physical Address
SERDES_16G0	0500 D018h + formula
SERDES_16G1	0501 D018h + formula
SERDES_16G2	0502 D018h + formula
SERDES_16G3	0503 D018h + formula

Figure 11-305. PHY_PIPE_ISO_USB_BER_CNT_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_USB_BER_CNT_15_8							
R-0h							
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_USB_BER_CNT_7_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 11-917. PHY_PIPE_ISO_USB_BER_CNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-8	PHY_PIPE_ISO_USB_BER_CNT_15_8	R	0h	Reserved
7-0	PHY_PIPE_ISO_USB_BER_CNT_7_0	R	0h	Current value of USB 3.0 loopback slave Bit Error Count from the PCS.

Table 11-918. Register Call Summary for PHY_PIPE_ISO_USB_BER_CNT_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_USB_BER_CNT_j Register \(Offset = D018h + formula\) \[reset = X\]: \[0\]](#)

11.306 PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j Register (Offset = D01Ch + formula) [reset = 0h]

PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j is shown in Figure 11-306 and described in Table 11-920.

Return to [Summary Table](#).

PIPE RX data low isolation register ()

Offset = D01Ch + (j * 200h); where j = 0h to 1h

Table 11-919. PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j Instances

Instance	Physical Address
SERDES_16G0	0500 D01Ch + formula
SERDES_16G1	0501 D01Ch + formula
SERDES_16G2	0502 D01Ch + formula
SERDES_16G3	0503 D01Ch + formula

Figure 11-306. PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_PIPE_ISO_RX_DATA_HI_15_0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PIPE_ISO_RX_DATA_LO_15_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 11-920. PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_PIPE_ISO_RX_DATA_HI_15_0	R	0h	Current value of pipe_rx_data[31:16] PHY output for the associated lane. (Not re-synchronized to apb_pclk)
15-0	PHY_PIPE_ISO_RX_DATA_LO_15_0	R	0h	Current value of pipe_rx_data[15:0] PHY output for the associated lane. (Not re-synchronized to apb_pclk)

Table 11-921. Register Call Summary for PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_RX_DATA_HI__PHY_PIPE_ISO_RX_DATA_LO_j Register \(Offset = D01Ch + formula\) \[reset = 0h\]: \[0\]](#)

11.307 PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register (Offset = D020h + formula) [reset = 00810000h]

PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j is shown in Figure 11-307 and described in Table 11-923.

Return to [Summary Table](#).

Ethernet MAC clock configuration isolation register

Offset = D020h + (j * 200h); where j = 0h to 1h

Table 11-922.
PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Instances

Instance	Physical Address
SERDES_16G0	0500 D020h + formula
SERDES_16G1	0501 D020h + formula
SERDES_16G2	0502 D020h + formula
SERDES_16G3	0503 D020h + formula

Figure 11-307. PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register

31	30	29	28	27	26	25	24
PHY_ETH_ISO_MAC_CLK_DIV_15_7							
R/W-1h							
23	22	21	20	19	18	17	16
PHY_ETH_ISO_MAC_CLK_DIV_15_7	PHY_ETH_ISO_MAC_CLK_DIV_6_0						
R/W-1h	R/W-1h						
15	14	13	12	11	10	9	8
PHY_ETH_ISO_MAC_CLK_CFG_15_10						PHY_ETH_ISO_MAC_CLK_CFG_9_8	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
PHY_ETH_ISO_MAC_CLK_CFG_7_6	PHY_ETH_ISO_MAC_CLK_CFG_5_4		PHY_ETH_ISO_MAC_CLK_CFG_3	PHY_ETH_ISO_MAC_CLK_CFG_2_0			
R-0h	R/W-0h		R-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-923. PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	PHY_ETH_ISO_MAC_CLK_DIV_15_7	R/W	1h	Drives mac_div_sel1 PHY input for the associated lane when in PHY macro and PMA isolation mode.
22-16	PHY_ETH_ISO_MAC_CLK_DIV_6_0	R/W	1h	Drives mac_div_sel0 PHY input for the associated lane when in PHY macro and PMA isolation mode.
15-10	PHY_ETH_ISO_MAC_CLK_CFG_15_10	R	0h	Reserved
9-8	PHY_ETH_ISO_MAC_CLK_CFG_9_8	R/W	0h	Drives mac_src_sel PHY input for the associated lane when in PHY macro and PMA isolation mode.
7-6	PHY_ETH_ISO_MAC_CLK_CFG_7_6	R	0h	Reserved

Table 11-923. PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	PHY_ETH_ISO_MAC_CLK_CFG_5_4	R/W	0h	Drives ovr_src_sel PHY input for the associated lane when in PHY macro and PMA isolation mode.
3	PHY_ETH_ISO_MAC_CLK_CFG_3	R	0h	Reserved
2-0	PHY_ETH_ISO_MAC_CLK_CFG_2_0	R/W	0h	Drives ovr_div_sel PHY input for the associated lane when in PHY macro and PMA isolation mode.

**Table 11-924. Register Call Summary for
PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register \(Offset = D020h + formula\) \[reset = 00810000h\]: \[0\]](#)

11.308 PHY_INTERRUPT_STS_j Register (Offset = D024h + formula) [reset = X]

PHY_INTERRUPT_STS_j is shown in [Figure 11-308](#) and described in [Table 11-926](#).

Return to [Summary Table](#).

PHY interrupt status register

Offset = D024h + (j * 200h); where j = 0h to 1h

Table 11-925. PHY_INTERRUPT_STS_j Instances

Instance	Physical Address
SERDES_16G0	0500 D024h + formula
SERDES_16G1	0501 D024h + formula
SERDES_16G2	0502 D024h + formula
SERDES_16G3	0503 D024h + formula

Figure 11-308. PHY_INTERRUPT_STS_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_INTERRUPT_STS_15	PHY_INTERRUPT_STS_14_11				PHY_INTERRUPT_STS_10_8		
R/W-0h	R-0h				R-0h		
7	6	5	4	3	2	1	0
PHY_INTERRUPT_STS_7	PHY_INTERRUPT_STS_6_4			PHY_INTERRUPT_STS_3_2		PHY_INTERRUPT_STS_1	PHY_INTERRUPT_STS_0
R-0h	R-0h			R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-926. PHY_INTERRUPT_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	PHY_INTERRUPT_STS_15	R/W	0h	State change monitor enable - 1 = state change monitor enabled, 0 = state change monitor disabled. Note: Only the master lane's state change monitor for a link is enabled. The state change monitor for a slave lane is disabled regardless of the state of this bit.
14-11	PHY_INTERRUPT_STS_14_11	R	0h	Reserved
10-8	PHY_INTERRUPT_STS_10_8	R	0h	Next power state/data rate - Only valid when one of the interrupt status bits is set. Indicates the requested power state or data rate for the state change failure. For PIPE requests, loaded based on the following: For Raw SerDes power state change requests, loaded based on following: 3'b 111 = PLL clock enable de-asserted

Table 11-926. PHY_INTERRUPT_STS_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	PHY_INTERRUPT_STS_7	R	0h	Reserved
6-4	PHY_INTERRUPT_STS_6_4	R	0h	Current power state/data rate - Only valid when one of the interrupt status bits is set. Indicates the starting power state or data rate for the state change failure. For PIPE requests, loaded based on the following: For Raw SerDes power state change requests, loaded based on following: 3'b 111 = PLL clock enable de-asserted
3-2	PHY_INTERRUPT_STS_3_2	R	0h	Reserved
1	PHY_INTERRUPT_STS_1	R/W	0h	Data rate state change interrupt status - Set to 1 upon data rate change timeout. Cleared upon read. Bit is writeable to allow the interrupt to be set manually for test purposes. Only set high by data rate change timeout if bit [0] == 0.
0	PHY_INTERRUPT_STS_0	R/W	0h	Power state change interrupt status - Set to 1 upon power state change timeout. Cleared upon read. Bit is writeable to allow the interrupt to set manually for test purposes. Only set high by power state change timeout if bit[1] == 0.

Table 11-927. Register Call Summary for PHY_INTERRUPT_STS_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_INTERRUPT_STS_j Register \(Offset = D024h + formula\) \[reset = X\]: \[0\]](#)

11.309 PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j Register (Offset = D030h + formula) [reset = 0h]

PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j is shown in Figure 11-309 and described in Table 11-929.

Return to [Summary Table](#).

PHY PIPE lane margining control and status register (#)

Offset = D030h + (j * 200h); where j = 0h to 1h

Table 11-928. PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j Instances

Instance	Physical Address
SERDES_16G0	0500 D030h + formula
SERDES_16G1	0501 D030h + formula
SERDES_16G2	0502 D030h + formula
SERDES_16G3	0503 D030h + formula

Figure 11-309. PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_LM_MAC2PHY0_15_8							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_LM_MAC2PHY0_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_PIPE_LM_CTRL_STS_15_12				PHY_PIPE_LM_CTRL_STS_11	PHY_PIPE_LM_CTRL_STS_10	PHY_PIPE_LM_CTRL_STS_9	PHY_PIPE_LM_CTRL_STS_8
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PHY_PIPE_LM_CTRL_STS_7_6	PHY_PIPE_LM_CTRL_STS_5	PHY_PIPE_LM_CTRL_STS_4	PHY_PIPE_LM_CTRL_STS_3	PHY_PIPE_LM_CTRL_STS_2	PHY_PIPE_LM_CTRL_STS_1	PHY_PIPE_LM_CTRL_STS_0	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-929. PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_ISO_LM_MAC2PHY0_15_8	R/W	0h	When in PHY isolation mode, this field provides the data for the 2nd cycle of a MAC-to-PHY register interface operation (for operations that require 2 or more cycle). Contains the low order register address bits. Set to zero for single cycle operations.
23-16	PHY_PIPE_ISO_LM_MAC2PHY0_7_0	R/W	0h	When in PHY isolation mode, this field provides the data for the 1st cycle of a MAC-to-PHY register interface operation. Contains the command + high order register address bits.
15-12	PHY_PIPE_LM_CTRL_STS_15_12	R	0h	Reserved
11	PHY_PIPE_LM_CTRL_STS_11	R	0h	Error count saturated flag: When set to 1, the error counter for the associated lane has saturated. Cleared upon read.

Table 11-929. PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	PHY_PIPE_LM_CTRL_STS_10	R	0h	Sample count saturated flag: When set to 1, the sample counter for the associated lane has saturated. Cleared upon read.
9	PHY_PIPE_LM_CTRL_STS_9	R	0h	Committed write invalid address error: When set to 1, an invalid register address was received on the PIPE MAC-to-PHY register interface for a committed write operation for the associated lane. Cleared upon read.
8	PHY_PIPE_LM_CTRL_STS_8	R	0h	Uncommitted write invalid address error: When set to 1, an invalid register address was received on the PIPE MAC-to-PHY register interface for an uncommitted write operation for the associated lane. Cleared upon read.
7-6	PHY_PIPE_LM_CTRL_STS_7_6	R	0h	Reserved
5	PHY_PIPE_LM_CTRL_STS_5	R/W	0h	Lane margining enable: 1 = lane margining logic is enabled regardless of PHY data rate or power state. 0 = lane margining logic is only enabled when link is in Gen 4 data rate and P0 power state.
4	PHY_PIPE_LM_CTRL_STS_4	R/W	0h	Lane margining controller soft reset: Soft reset to the associated lane's lane margining controller block (i.e. MAC-XPHY).
3	PHY_PIPE_LM_CTRL_STS_3	R/W	0h	Lane margining PMA I/F soft reset: Soft reset to the associated lane's lane margining PMA interface block (i.e. MAC-XPHY).
2	PHY_PIPE_LM_CTRL_STS_2	R/W	0h	Lane margining PIPE Tx I/F soft reset: Soft reset to the associated lane's lane margining PIPE transmit block (i.e. MAC-XPHY).
1	PHY_PIPE_LM_CTRL_STS_1	R/W	0h	Lane margining PIPE Rx I/F soft reset: Soft reset to the associated lane's lane margining PIPE receive block (i.e. MAC-XPHY).
0	PHY_PIPE_LM_CTRL_STS_0	R/W	0h	Lane margining soft reset: Soft reset to the associated lane's lane margining logic.

Table 11-930. Register Call Summary for PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_LM_MAC2PHY0__PHY_PIPE_LM_CTRL_STS_j Register \(Offset = D030h + formula\) \[reset = 0h\]: \[0\]](#)

11.310 PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j Register (Offset = D034h + formula) [reset = 0h]

PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j is shown in Figure 11-310 and described in Table 11-932.

Return to [Summary Table](#).

PHY PIPE lane margining MAC-to-PHY isolation register 1 (#)

Offset = D034h + (j * 200h); where j = 0h to 1h

Table 11-931.
PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j Instances

Instance	Physical Address
SERDES_16G0	0500 D034h + formula
SERDES_16G1	0501 D034h + formula
SERDES_16G2	0502 D034h + formula
SERDES_16G3	0503 D034h + formula

Figure 11-310. PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_LM_PHY2MAC0_15_8							
R-0h							
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_LM_PHY2MAC0_7_0							
R-0h							
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_LM_MAC2PHY1_15_9							PHY_PIPE_ISO_LM_MAC2PHY1_8
R-0h							R/W-0h
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_LM_MAC2PHY1_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-932. PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_ISO_LM_PHY2MAC0_15_8	R	0h	Captures the data from a PHY-to-MAC write (committed or uncommitted) operation to address 1. Once captured, a new write operation to address 1 will not overwrite this field this register has been read.
23-16	PHY_PIPE_ISO_LM_PHY2MAC0_7_0	R	0h	Captures the data from a PHY-to-MAC write (committed or uncommitted) operation to address 0. Once captured, a new write operation to address 0 will not overwrite this field until this register has been read.
15-9	PHY_PIPE_ISO_LM_MAC2PHY1_15_9	R	0h	Reserved
8	PHY_PIPE_ISO_LM_MAC2PHY1_8	R/W	0h	When in PHY isolation mode, write a 1 to this bit to initiate a MAC-to-PHY register interface operation. (self-clearing).

Table 11-932. PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	PHY_PIPE_ISO_LM_MAC2PHY1_7_0	R/W	0h	When in PHY isolation mode, this field provides the data for the 3rd cycle of a MAC-to-PHY register interface operation. Contains the register data. Set to zero for 1 and 2 cycle operations.

Table 11-933. Register Call Summary for PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_LM_PHY2MAC0__PHY_PIPE_ISO_LM_MAC2PHY1_j Register \(Offset = D034h + formula\) \[reset = 0h\]: \[0\]](#)

11.311 PHY_PIPE_ISO_LM_PHY2MAC1_j Register (Offset = D038h + formula) [reset = X]

PHY_PIPE_ISO_LM_PHY2MAC1_j is shown in Figure 11-311 and described in Table 11-935.

Return to [Summary Table](#).

PHY PIPE lane margining PHY-to-MAC isolation register 1 (#)

Offset = D038h + (j * 200h); where j = 0h to 1h

Table 11-934. PHY_PIPE_ISO_LM_PHY2MAC1_j Instances

Instance	Physical Address
SERDES_16G0	0500 D038h + formula
SERDES_16G1	0501 D038h + formula
SERDES_16G2	0502 D038h + formula
SERDES_16G3	0503 D038h + formula

Figure 11-311. PHY_PIPE_ISO_LM_PHY2MAC1_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_LM_PHY2MAC1_15_8							
R-0h							
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_LM_PHY2MAC1_7_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 11-935. PHY_PIPE_ISO_LM_PHY2MAC1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-8	PHY_PIPE_ISO_LM_PHY2MAC1_15_8	R	0h	Captures the data from a PHY-to-MAC read completion operation. Once captured, a new read completion operation will not overwrite this field until this register has been read.
7-0	PHY_PIPE_ISO_LM_PHY2MAC1_7_0	R	0h	Captures the data from a PHY-to-MAC write (committed or uncommitted) operation to address 2. Once captured, a new write operation to address 2 will not overwrite this field until this register has been read.

Table 11-936. Register Call Summary for PHY_PIPE_ISO_LM_PHY2MAC1_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_LM_PHY2MAC1_j Register \(Offset = D038h + formula\) \[reset = X\]: \[0\]](#)

11.312 PHY_PIPE_ISO_LM_PHY2MAC_STS_j Register (Offset = D03Ch + formula) [reset = X]

PHY_PIPE_ISO_LM_PHY2MAC_STS_j is shown in Figure 11-312 and described in Table 11-938.

Return to [Summary Table](#).

PHY PIPE lane margining PHY-to-MAC status isolation register 1 (#)

Offset = D03Ch + (j * 200h); where j = 0h to 1h

**Table 11-937. PHY_PIPE_ISO_LM_PHY2MAC_STS_j
Instances**

Instance	Physical Address
SERDES_16G0	0500 D03Ch + formula
SERDES_16G1	0501 D03Ch + formula
SERDES_16G2	0502 D03Ch + formula
SERDES_16G3	0503 D03Ch + formula

Figure 11-312. PHY_PIPE_ISO_LM_PHY2MAC_STS_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_LM_PHY2MAC_STS_15_12				PHY_PIPE_ISO_LM_PHY2MAC_STS_11	PHY_PIPE_ISO_LM_PHY2MAC_STS_10	PHY_PIPE_ISO_LM_PHY2MAC_STS_9	PHY_PIPE_ISO_LM_PHY2MAC_STS_8
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_LM_PHY2MAC_STS_7	PHY_PIPE_ISO_LM_PHY2MAC_STS_6	PHY_PIPE_ISO_LM_PHY2MAC_STS_5	PHY_PIPE_ISO_LM_PHY2MAC_STS_4	PHY_PIPE_ISO_LM_PHY2MAC_STS_3	PHY_PIPE_ISO_LM_PHY2MAC_STS_2	PHY_PIPE_ISO_LM_PHY2MAC_STS_1	PHY_PIPE_ISO_LM_PHY2MAC_STS_0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 11-938. PHY_PIPE_ISO_LM_PHY2MAC_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-12	PHY_PIPE_ISO_LM_PHY2MAC_STS_15_12	R	0h	Reserved
11	PHY_PIPE_ISO_LM_PHY2MAC_STS_11	R	0h	Set upon receiving a PHY-to-MAC read completion. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC1.
10	PHY_PIPE_ISO_LM_PHY2MAC_STS_10	R	0h	Set upon receiving a PHY-to-MAC write acknowledgment.
9	PHY_PIPE_ISO_LM_PHY2MAC_STS_9	R	0h	Set upon receiving a PHY-to-MAC committed write to an unsupported address. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC1.
8	PHY_PIPE_ISO_LM_PHY2MAC_STS_8	R	0h	Reserved
7	PHY_PIPE_ISO_LM_PHY2MAC_STS_7	R	0h	Set upon receiving a PHY-to-MAC committed write to address 2. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC1.

Table 11-938. PHY_PIPE_ISO_LM_PHY2MAC_STS_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PHY_PIPE_ISO_LM_PHY2MAC_STS_6	R	0h	Set upon receiving a PHY-to-MAC committed write to address 1. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC0.
5	PHY_PIPE_ISO_LM_PHY2MAC_STS_5	R	0h	Set upon receiving a PHY-to-MAC committed write to address 0. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC0.
4	PHY_PIPE_ISO_LM_PHY2MAC_STS_4	R	0h	Set upon receiving a PHY-to-MAC uncommitted write to an unsupported address. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC1.
3	PHY_PIPE_ISO_LM_PHY2MAC_STS_3	R	0h	Reserved
2	PHY_PIPE_ISO_LM_PHY2MAC_STS_2	R	0h	Set upon receiving a PHY-to-MAC uncommitted write to address 2. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC1.
1	PHY_PIPE_ISO_LM_PHY2MAC_STS_1	R	0h	Set upon receiving a PHY-to-MAC uncommitted write to address 1. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC0.
0	PHY_PIPE_ISO_LM_PHY2MAC_STS_0	R	0h	Set upon receiving a PHY-to-MAC uncommitted write to address 0. Cleared upon reading PHY_PIPE_ISO_LM_PHY2MAC0.

Table 11-939. Register Call Summary for PHY_PIPE_ISO_LM_PHY2MAC_STS_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PIPE_ISO_LM_PHY2MAC_STS_j Register \(Offset = D03Ch + formula\) \[reset = X\]: \[0\]](#)

11.313 PHY_PMA_CMN_CTRL Register (Offset = E000h) [reset = X]

PHY_PMA_CMN_CTRL is shown in Figure 11-313 and described in Table 11-941.

Return to [Summary Table](#).

PMA common control register

Table 11-940. PHY_PMA_CMN_CTRL Instances

Instance	Physical Address
SERDES_16G0	0500 E000h
SERDES_16G1	0501 E000h
SERDES_16G2	0502 E000h
SERDES_16G3	0503 E000h

Figure 11-313. PHY_PMA_CMN_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_PMA_CMN_CTRL_15_14	PHY_PMA_CM_N_CTRL_13	PHY_PMA_CM_N_CTRL_12	PHY_PMA_CM_N_CTRL_11	PHY_PMA_CM_N_CTRL_10	PHY_PMA_CMN_CTRL_9_8		
R/W-0h	R-1h	R-1h	R-0h	R-0h	R-0h		
7	6	5	4	3	2	1	0
PHY_PMA_CM_N_CTRL_7	PHY_PMA_CM_N_CTRL_6	PHY_PMA_CM_N_CTRL_5	PHY_PMA_CM_N_CTRL_4	PHY_PMA_CM_N_CTRL_3	PHY_PMA_CM_N_CTRL_2	PHY_PMA_CM_N_CTRL_1	PHY_PMA_CM_N_CTRL_0
R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-941. PHY_PMA_CMN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	PHY_PMA_CMN_CTRL_15_14	R/W	0h	Drives cmn_psmclk_dig_div PMA input
13	PHY_PMA_CMN_CTRL_13	R	1h	Current value of cmn_pll1c1_disabled PMA output
12	PHY_PMA_CMN_CTRL_12	R	1h	Current value of cmn_pll1c_disabled PMA output
11	PHY_PMA_CMN_CTRL_11	R	0h	Current value of cmn_pll1c1_ready PMA output
10	PHY_PMA_CMN_CTRL_10	R	0h	Current value of cmn_pll1c_ready PMA output
9-8	PHY_PMA_CMN_CTRL_9_8	R	0h	Reserved
7	PHY_PMA_CMN_CTRL_7	R/W	0h	Drives cmn_refclk1_rcv_out_en PMA input
6	PHY_PMA_CMN_CTRL_6	R/W	0h	Drives cmn_refclk_rcv_out_en PMA input
5	PHY_PMA_CMN_CTRL_5	R	0h	Current value of cmn_refclk1_active PMA output
4	PHY_PMA_CMN_CTRL_4	R	0h	Current value of cmn_refclk_active PMA output
3	PHY_PMA_CMN_CTRL_3	R	0h	Current value of cmn_pll1c1_locked PMA output.

Table 11-941. PHY_PMA_CMN_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PHY_PMA_CMN_CTRL_2	R	0h	Current value of cmn_pll_locked PMA output
1	PHY_PMA_CMN_CTRL_1	R	0h	Current value of cmn_macro_suspend_ack PMA output
0	PHY_PMA_CMN_CTRL_0	R	0h	Current value of cmn_ready PMA output

Table 11-942. Register Call Summary for PHY_PMA_CMN_CTRL

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_CMN_CTRL Register \(Offset = E000h\) \[reset = X\]: \[0\]](#)

11.314 PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL Register (Offset = E008h) [reset = 201h]

PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL is shown in Figure 11-314 and described in Table 11-944.

Return to [Summary Table](#).

PMA common control signal isolation register

Table 11-943.

PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL Instances

Instance	Physical Address
SERDES_16G0	0500 E008h
SERDES_16G1	0501 E008h
SERDES_16G2	0502 E008h
SERDES_16G3	0503 E008h

Figure 11-314. PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_CMN_PLLLC_CTRL_15_6							
R-0h							
23	22	21	20	19	18	17	16
PHY_PMA_ISO_CMN_PLLLC_CTRL_15_6	PHY_PMA_ISO_CMN_PLLLC_CTRL_5	PHY_PMA_ISO_CMN_PLLLC_CTRL_4	PHY_PMA_ISO_CMN_PLLLC_CTRL_3	PHY_PMA_ISO_CMN_PLLLC_CTRL_2	PHY_PMA_ISO_CMN_PLLLC_CTRL_1	PHY_PMA_ISO_CMN_PLLLC_CTRL_0	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PHY_PMA_ISO_CMN_CTRL_15_14	PHY_PMA_ISO_CMN_CTRL_13_12	PHY_PMA_ISO_CMN_CTRL_11_10	PHY_PMA_ISO_CMN_CTRL_9	PHY_PMA_ISO_CMN_CTRL_8			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-1h	R/W-0h		
7	6	5	4	3	2	1	0
PHY_PMA_ISO_CMN_CTRL_7	PHY_PMA_ISO_CMN_CTRL_6	PHY_PMA_ISO_CMN_CTRL_5	PHY_PMA_ISO_CMN_CTRL_4	PHY_PMA_ISO_CMN_CTRL_3	PHY_PMA_ISO_CMN_CTRL_2	PHY_PMA_ISO_CMN_CTRL_1	PHY_PMA_ISO_CMN_CTRL_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-944. PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	PHY_PMA_ISO_CMN_PLLLC_CTRL_15_6	R	0h	Reserved
21	PHY_PMA_ISO_CMN_PLLLC_CTRL_5	R/W	0h	Drives cmn_pll1_suspend PMA input when in PMA isolation mode.
20	PHY_PMA_ISO_CMN_PLLLC_CTRL_4	R/W	0h	Drives cmn_pll1_suspend PMA input when in PMA isolation mode.
19	PHY_PMA_ISO_CMN_PLLLC_CTRL_3	R/W	0h	Drives cmn_pll1_mode PMA input when in PMA isolation mode.
18	PHY_PMA_ISO_CMN_PLLLC_CTRL_2	R/W	0h	Drives cmn_pll1_mode PMA input when in PMA isolation mode.
17	PHY_PMA_ISO_CMN_PLLLC_CTRL_1	R/W	0h	Drives cmn_pll1_en PMA input when in PMA isolation mode.
16	PHY_PMA_ISO_CMN_PLLLC_CTRL_0	R/W	0h	Drives cmn_pll1_en PMA input when in PMA isolation mode.

Table 11-944. PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	PHY_PMA_ISO_CMN_CTL_15_14	R/W	0h	Drives cmn_refclk1_dig_div PMA input when in PHY macro or PMA isolation mode.
13-12	PHY_PMA_ISO_CMN_CTL_13_12	R/W	0h	Drives cmn_refclk_dig_div PMA input when in PHY macro or PMA isolation mode.
11-10	PHY_PMA_ISO_CMN_CTL_11_10	R/W	0h	Drives cmn_refclk_dig_sel PMA input when in PHY macro or PMA isolation mode.
9	PHY_PMA_ISO_CMN_CTL_9	R	1h	Current value of cmn_macro_pwr_en_ack PMA output.
8	PHY_PMA_ISO_CMN_CTL_8	R/W	0h	Drives cmn_macro_pwr_en PMA input when in PHY macro and PMA isolation mode.
7	PHY_PMA_ISO_CMN_CTL_7	R/W	0h	Drives cmn_refclk1_sel PMA input when in PHY macro and PMA isolation mode.
6	PHY_PMA_ISO_CMN_CTL_6	R/W	0h	Drives cmn_refclk_sel PMA input when in PHY macro and PMA isolation mode.
5	PHY_PMA_ISO_CMN_CTL_5	R/W	0h	Drives cmn_refclk1_disable PMA input when in PMA isolation mode.
4	PHY_PMA_ISO_CMN_CTL_4	R/W	0h	Drives cmn_refclk_disable PMA input when in PMA isolation mode.
3	PHY_PMA_ISO_CMN_CTL_3	R	0h	Reserved
2	PHY_PMA_ISO_CMN_CTL_2	R/W	0h	Drives macro_suspend_req PMA input when in PMA isolation mode.
1	PHY_PMA_ISO_CMN_CTL_1	R/W	0h	Drives cmn_macro_en PMA input when in PMA isolation mode.
0	PHY_PMA_ISO_CMN_CTL_0	R/W	1h	Drives cmn_reset_n PMA input when in PMA isolation mode.

Table 11-945. Register Call Summary for PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_CMN_PLLLC_CTRL__PHY_PMA_ISO_CMN_CTRL Register \(Offset = E008h\) \[reset = 201h\]: \[0\]](#)

11.315 PHY_PMA_ISO_RESCAL Register (Offset = E00Ch) [reset = X]

PHY_PMA_ISO_RESCAL is shown in [Figure 11-315](#) and described in [Table 11-947](#).

Return to [Summary Table](#).

PMA Isolation resistor calibration code register

Table 11-946. PHY_PMA_ISO_RESCAL Instances

Instance	Physical Address
SERDES_16G0	0500 E00Ch
SERDES_16G1	0501 E00Ch
SERDES_16G2	0502 E00Ch
SERDES_16G3	0503 E00Ch

Figure 11-315. PHY_PMA_ISO_RESCAL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_PMA_ISO_RESCAL_15_14		PHY_PMA_ISO_RESCAL_13_8					
R-0h		R-1Dh					
7	6	5	4	3	2	1	0
PHY_PMA_ISO_RESCAL_7	PHY_PMA_ISO_RESCAL_6	PHY_PMA_ISO_RESCAL_5_0					
R/W-0h	R-0h	R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-947. PHY_PMA_ISO_RESCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	PHY_PMA_ISO_RESCAL_15_14	R	0h	Reserved.
13-8	PHY_PMA_ISO_RESCAL_13_8	R	1Dh	Current value cmn_rescal_code_out PMA output.
7	PHY_PMA_ISO_RESCAL_7	R/W	0h	Drives cmn_rescal_insel PMA input in PMA isolation mode.
6	PHY_PMA_ISO_RESCAL_6	R	0h	Reserved
5-0	PHY_PMA_ISO_RESCAL_5_0	R/W	0h	Drives cmn_rescal_code_in PMA input in PMA isolation mode.

Table 11-948. Register Call Summary for PHY_PMA_ISO_RESCAL

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_RESCAL Register \(Offset = E00Ch\) \[reset = X\]: \[0\]](#)

11.316 PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL Register (Offset = E01Ch) [reset = 0h]

PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL is shown in Figure 11-316 and described in Table 11-950.

Return to [Summary Table](#).

PMA Lane Isolation control register

Table 11-949. PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL Instances

Instance	Physical Address
SERDES_16G0	0500 E01Ch
SERDES_16G1	0501 E01Ch
SERDES_16G2	0502 E01Ch
SERDES_16G3	0503 E01Ch

Figure 11-316. PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO LATION_CTRL _15	PHY_PMA_ISO LATION_CTRL _14	PHY_PMA_ISO LATION_CTRL _13	PHY_PMA_ISO LATION_CTRL _12	PHY_PMA_ISOLATION_CTRL_11_0			
R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
PHY_PMA_ISOLATION_CTRL_11_0							
R-0h							
15	14	13	12	11	10	9	8
PHY_PMA_LN_ISOLATION_CTRL_15_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_PMA_LN_ISOLATION_CTRL_15_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-950. PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PMA_ISOLATION_C TRL_15	R/W	0h	PHY/PMA isolation enable (isolation_en) - When set, enables isolation (PHY or PMA).
30	PHY_PMA_ISOLATION_C TRL_14	R/W	0h	PHY/PMA common isolation enable (cmn_isolation_en) - When in PHY Macro Isolation Mode, the PHY common isolation register(s) are selected. When in PMA Isolation Mode, the PMA common isolation register(s) are selected.
29	PHY_PMA_ISOLATION_C TRL_13	R	0h	Reserved
28	PHY_PMA_ISOLATION_C TRL_12	R/W	0h	PHY/PMA isolation mode select (isolation_mode_sel) - When isolation_en is set, this bit selects between PHY isolation mode and PMA isolation mode. 0 = PHY Macro isolation mode 1 = PMA isolation mode.

Table 11-950. PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-16	PHY_PMA_ISOLATION_CTRL_11_0	R	0h	Reserved
15-0	PHY_PMA_LN_ISOLATION_CTRL_15_0	R/W	0h	PHY/PMA lane isolation enable (ln_isolation_en) - When in PHY Macro Isolation Mode, the selected PHY lane(s) isolation registers are selected. When in PMA Isolation Mode, the selected PMA lane(s).

**Table 11-951. Register Call Summary for
PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISOLATION_CTRL__PHY_PMA_LN_ISOLATION_CTRL Register \(Offset = E01Ch\) \[reset = 0h\]: \[0\]](#)

11.317 PHY_PMA_XCVR_CTRL_j Register (Offset = F000h + formula) [reset = X]

PHY_PMA_XCVR_CTRL_j is shown in Figure 11-317 and described in Table 11-953.

Return to [Summary Table](#).

PMA transceiver control register

Offset = F000h + (j * 200h); where j = 0h to 1h

Table 11-952. PHY_PMA_XCVR_CTRL_j Instances

Instance	Physical Address
SERDES_16G0	0500 F000h + formula
SERDES_16G1	0501 F000h + formula
SERDES_16G2	0502 F000h + formula
SERDES_16G3	0503 F000h + formula

Figure 11-317. PHY_PMA_XCVR_CTRL_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_PMA_XCVR_CTRL_15	PHY_PMA_XCVR_CTRL_14	PHY_PMA_XCVR_CTRL_13	PHY_PMA_XCVR_CTRL_12	PHY_PMA_XCVR_CTRL_11_10		PHY_PMA_XCVR_CTRL_9	PHY_PMA_XCVR_CTRL_8
R/W-1h	R-0h	R-0h	R-1h	R-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PHY_PMA_XCVR_CTRL_7_6		PHY_PMA_XCVR_CTRL_5	PHY_PMA_XCVR_CTRL_4	PHY_PMA_XCVR_CTRL_3	PHY_PMA_XCVR_CTRL_2	PHY_PMA_XCVR_CTRL_1	PHY_PMA_XCVR_CTRL_0
R-0h		R-0h	R/W-0h	R-0h	R-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-953. PHY_PMA_XCVR_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	PHY_PMA_XCVR_CTRL_15	R/W	1h	Drives rx_termination PMA input for the associated lane when the lane is configured for Ethernet.
14	PHY_PMA_XCVR_CTRL_14	R	0h	Reserved
13	PHY_PMA_XCVR_CTRL_13	R	0h	Current value of xcvr_pll_clk_en_ack PMA output for the associated lane.
12	PHY_PMA_XCVR_CTRL_12	R	1h	Current value of xcvr_lane_en_ack PMA output for the associated lane.
11-10	PHY_PMA_XCVR_CTRL_11_10	R	0h	Reserved
9	PHY_PMA_XCVR_CTRL_9	R/W	0h	Drives the tx_bist_hold PMA input for all lanes in the associated link (for the master lane) - synchronized to the Tx data rate clock for the link. The bit associated with the master lane of the link drives PMA inputs for all lanes in the link after synchronization to the Tx data rate clock.

Table 11-953. PHY_PMA_XCVR_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	PHY_PMA_XCVR_CTRL_8	R/W	0h	Drives the tx_differential_invert PMA input for the associated lane.
7-6	PHY_PMA_XCVR_CTRL_7_6	R	0h	Reserved
5	PHY_PMA_XCVR_CTRL_5	R	0h	Current value of ln_plln_locked PMA output for the associated lane
4	PHY_PMA_XCVR_CTRL_4	R/W	0h	Drives rx_rd10_clken PMA input for the associated lane
3	PHY_PMA_XCVR_CTRL_3	R	0h	Current value of rx_bist_status PMA output for the associated lane.
2	PHY_PMA_XCVR_CTRL_2	R	0h	Current value of rx_bist_err_toggle PMA output for the associated lane.
1	PHY_PMA_XCVR_CTRL_1	R	0h	Current value of rx_bist_sync PMA output for the associated lane.
0	PHY_PMA_XCVR_CTRL_0	R/W	0h	Drives the rx_differential_invert PMA input for the associated lane.

Table 11-954. Register Call Summary for PHY_PMA_XCVR_CTRL_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_XCVR_CTRL_j Register \(Offset = F000h + formula\) \[reset = X\]: \[0\]](#)

11.318 PHY_PMA_ISO_XCVR_CTRL_j Register (Offset = F004h + formula) [reset = X]

PHY_PMA_ISO_XCVR_CTRL_j is shown in Figure 11-318 and described in Table 11-956.

Return to [Summary Table](#).

PMA Isolation Transceiver control register

Offset = F004h + (j * 200h); where j = 0h to 1h

Table 11-955. PHY_PMA_ISO_XCVR_CTRL_j Instances

Instance	Physical Address
SERDES_16G0	0500 F004h + formula
SERDES_16G1	0501 F004h + formula
SERDES_16G2	0502 F004h + formula
SERDES_16G3	0503 F004h + formula

Figure 11-318. PHY_PMA_ISO_XCVR_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_XCVR_CTRL_15	PHY_PMA_ISO_XCVR_CTRL_14	PHY_PMA_ISO_XCVR_CTRL_13	PHY_PMA_ISO_XCVR_CTRL_12	PHY_PMA_ISO_XCVR_CTRL_11	PHY_PMA_ISO_XCVR_CTRL_10	PHY_PMA_ISO_XCVR_CTRL_9	PHY_PMA_ISO_XCVR_CTRL_8
R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PHY_PMA_ISO_XCVR_CTRL_7	PHY_PMA_ISO_XCVR_CTRL_6	PHY_PMA_ISO_XCVR_CTRL_5	PHY_PMA_ISO_XCVR_CTRL_4	PHY_PMA_ISO_XCVR_CTRL_3	PHY_PMA_ISO_XCVR_CTRL_2	PHY_PMA_ISO_XCVR_CTRL_1	PHY_PMA_ISO_XCVR_CTRL_0
R/W-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-956. PHY_PMA_ISO_XCVR_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PMA_ISO_XCVR_CTRL_15	R/W	0h	Drives tx_high_z PMA input for the associated lane when in PMA isolation mode.
30	PHY_PMA_ISO_XCVR_CTRL_14	R	0h	Reserved.
29	PHY_PMA_ISO_XCVR_CTRL_13	R/W	0h	Drives tx_ifps_en PMA input for the associated lane when in PMA isolation mode.
28	PHY_PMA_ISO_XCVR_CTRL_12	R/W	0h	Drives tx_elec_idle PMA input for the associated lane when in PMA isolation mode.
27	PHY_PMA_ISO_XCVR_CTRL_11	R	0h	Current value of tx_rcv_detected PMA output for the associated lane when PHY_PMA_ISO_XCVR_CTRL[9] == 1 and PHY_PMA_ISO_XCVR_CTRL[10] == 1. (Not re-synchronized to apb_pclk)
26	PHY_PMA_ISO_XCVR_CTRL_10	R	0h	Current value of tx_rcv_detect_done PMA output for the associated lane.

Table 11-956. PHY_PMA_ISO_XCVR_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	PHY_PMA_ISO_XCVR_CTRL_9	R/W	0h	Drives tx_rcv_detect_en PMA input for the associated lane when in PMA isolation mode.
24	PHY_PMA_ISO_XCVR_CTRL_8	R/W	0h	Drives xcvr_link_reset_n PMA input for the associated lane when in PMA isolation mode.
23	PHY_PMA_ISO_XCVR_CTRL_7	R/W	0h	Drives xcvr_pllclk_en PMA input for the associated lane when in PMA isolation mode.
22	PHY_PMA_ISO_XCVR_CTRL_6	R	0h	Reserved
21	PHY_PMA_ISO_XCVR_CTRL_5	R/W	0h	Drives xcvr_lane_suspend PMA input for the associated lane when in PMA isolation mode.
20	PHY_PMA_ISO_XCVR_CTRL_4	R	0h	Current value of rx_lfps_detect PMA output for the associated lane.
19	PHY_PMA_ISO_XCVR_CTRL_3	R	0h	Current value of rx_signal_detect PMA output for the associated lane.
18	PHY_PMA_ISO_XCVR_CTRL_2	R	0h	Reserved
17	PHY_PMA_ISO_XCVR_CTRL_1	R/W	0h	Drives rx_termination PMA input for the associated lane when in PMA isolation mode.
16	PHY_PMA_ISO_XCVR_CTRL_0	R/W	0h	Drives xcvr_lane_en PMA input for the associated lane when in PMA isolation mode.
15-0	RESERVED	R/W	X	

Table 11-957. Register Call Summary for PHY_PMA_ISO_XCVR_CTRL_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_XCVR_CTRL_j Register \(Offset = F004h + formula\) \[reset = X\]: \[0\]](#)

11.319 PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j Register (Offset = F008h + formula) [reset = 0h]

PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j is shown in Figure 11-319 and described in Table 11-959.

Return to [Summary Table](#).

PMA Isolation transmitter local preset coefficient register

Offset = F008h + (j * 200h); where j = 0h to 1h

Table 11-958. PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j Instances

Instance	Physical Address
SERDES_16G0	0500 F008h + formula
SERDES_16G1	0501 F008h + formula
SERDES_16G2	0502 F008h + formula
SERDES_16G3	0503 F008h + formula

Figure 11-319. PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_TX_LPC_HI_1_5	PHY_PMA_ISO_TX_LPC_HI_1_4	PHY_PMA_ISO_TX_LPC_HI_1_3	PHY_PMA_ISO_TX_LPC_HI_1_2	PHY_PMA_ISO_TX_LPC_HI_11_8			
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h			
23	22	21	20	19	18	17	16
PHY_PMA_ISO_TX_LPC_HI_7_6	PHY_PMA_ISO_TX_LPC_HI_5_0						
R-0h				R-0h			
15	14	13	12	11	10	9	8
PHY_PMA_ISO_TX_LPC_LO_15_14	PHY_PMA_ISO_TX_LPC_LO_13_8						
R-0h				R-0h			
7	6	5	4	3	2	1	0
PHY_PMA_ISO_TX_LPC_LO_7_6	PHY_PMA_ISO_TX_LPC_LO_5_0						
R-0h				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-959. PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PMA_ISO_TX_LPC_HI_15	R	0h	Current value of tx_local_preset_coeff_valid PMA output for the associated lane.
30	PHY_PMA_ISO_TX_LPC_HI_14	R	0h	Reserved
29	PHY_PMA_ISO_TX_LPC_HI_13	R/W	0h	Drives tx_get_local_init_coef PMA input for the associated lane when in PMA isolation mode.
28	PHY_PMA_ISO_TX_LPC_HI_12	R/W	0h	Drives tx_get_local_preset_coef PMA input for the associated lane when in PMA isolation mode.
27-24	PHY_PMA_ISO_TX_LPC_HI_11_8	R/W	0h	Drives tx_local_preset_index PMA input for the associated lane when in PMA isolation mode.
23-22	PHY_PMA_ISO_TX_LPC_HI_7_6	R	0h	Reserved

**Table 11-959. PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX_LPC_LO_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
21-16	PHY_PMA_ISO_TX_LPC_HI_5_0	R	0h	Current value of tx_local_tx_preset_coef[17:12] PMA output for the associated lane when (PHY_PMA_ISO_TX_LPC_HI[12] == 1 or PHY_PMA_ISO_TX_LPC_HI[13] == 1) and PHY_PMA_ISO_TX_LPC_HI[15] == 1.
15-14	PHY_PMA_ISO_TX_LPC_LO_15_14	R	0h	Reserved
13-8	PHY_PMA_ISO_TX_LPC_LO_13_8	R	0h	Current value of tx_local_tx_preset_coef[11:6] PMA output for the associated lane when (PHY_PMA_ISO_TX_LPC_HI[12] == 1 or PHY_PMA_ISO_TX_LPC_HI[13] == 1) and PHY_PMA_ISO_TX_LPC_HI[15] == 1.
7-6	PHY_PMA_ISO_TX_LPC_LO_7_6	R	0h	Reserved
5-0	PHY_PMA_ISO_TX_LPC_LO_5_0	R	0h	Current value of tx_local_tx_preset_coef[5:0] PMA output for the associated lane when (PHY_PMA_ISO_TX_LPC_HI[12] == 1 or PHY_PMA_ISO_TX_LPC_HI[13] == 1) and PHY_PMA_ISO_TX_LPC_HI[15] == 1.

Table 11-960. Register Call Summary for PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX_LPC_LO_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX_LPC_LO_j Register \(Offset = F008h + formula\) \[reset = 0h\]: \[0\]](#)

11.320 PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Register (Offset = F00Ch + formula) [reset = 0h]

PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j is shown in Figure 11-320 and described in Table 11-962.

Return to [Summary Table](#).

PMA TX de-emphasis low isolation register

Offset = F00Ch + (j * 200h); where j = 0h to 1h

Table 11-961. PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Instances

Instance	Physical Address
SERDES_16G0	0500 F00Ch + formula
SERDES_16G1	0501 F00Ch + formula
SERDES_16G2	0502 F00Ch + formula
SERDES_16G3	0503 F00Ch + formula

Figure 11-320. PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_TX_DMPH_HI_15_6							
R-0h							
23	22	21	20	19	18	17	16
PHY_PMA_ISO_TX_DMPH_HI_15_6	PHY_PMA_ISO_TX_DMPH_HI_5_0						
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
PHY_PMA_ISO_TX_DMPH_LO_15_14	PHY_PMA_ISO_TX_DMPH_LO_13_8						
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
PHY_PMA_ISO_TX_DMPH_LO_7_6	PHY_PMA_ISO_TX_DMPH_LO_5_0						
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-962. PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	PHY_PMA_ISO_TX_DMPH_HI_15_6	R	0h	Reserved
21-16	PHY_PMA_ISO_TX_DMPH_HI_5_0	R/W	0h	Drives tx_deemphasis[17:12] PMA input for the associated lane when in PMA isolation mode
15-14	PHY_PMA_ISO_TX_DMPH_LO_15_14	R	0h	Reserved
13-8	PHY_PMA_ISO_TX_DMPH_LO_13_8	R/W	0h	Drives tx_deemphasis[11:6] PMA input for the associated lane when in PMA isolation mode
7-6	PHY_PMA_ISO_TX_DMPH_LO_7_6	R	0h	Reserved
5-0	PHY_PMA_ISO_TX_DMPH_LO_5_0	R/W	0h	Drives tx_deemphasis[5:0] PMA input for the associated lane when in PMA isolation mode

Table 11-963. Register Call Summary for PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Register \(Offset = F00Ch + formula\) \[reset = 0h\]: \[0\]](#)

11.321 PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Register (Offset = F010h + formula) [reset = 2D0Fh]

PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j is shown in Figure 11-321 and described in Table 11-965.

Return to [Summary Table](#).

PMA TX FS LF isolation register

Offset = F010h + (j * 200h); where j = 0h to 1h

Table 11-964. PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Instances

Instance	Physical Address
SERDES_16G0	0500 F010h + formula
SERDES_16G1	0501 F010h + formula
SERDES_16G2	0502 F010h + formula
SERDES_16G3	0503 F010h + formula

Figure 11-321. PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_TX_MGN_15_9							PHY_PMA_ISO_TX_MGN_8
R-0h							R/W-0h
23	22	21	20	19	18	17	16
PHY_PMA_ISO_TX_MGN_7_3					PHY_PMA_ISO_TX_MGN_2_0		
R-0h					R/W-0h		
15	14	13	12	11	10	9	8
PHY_PMA_ISO_TX_FSLF_15_14		PHY_PMA_ISO_TX_FSLF_13_8					
R-0h		R-2Dh					
7	6	5	4	3	2	1	0
PHY_PMA_ISO_TX_FSLF_7_6		PHY_PMA_ISO_TX_FSLF_5_0					
R-0h		R-Fh					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-965. PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	PHY_PMA_ISO_TX_MGN_15_9	R	0h	Reserved
24	PHY_PMA_ISO_TX_MGN_8	R/W	0h	Drives tx_low_power_swing_en PMA input for the associated lane when in PHY macro and PMA isolation mode.
23-19	PHY_PMA_ISO_TX_MGN_7_3	R	0h	Reserved
18-16	PHY_PMA_ISO_TX_MGN_2_0	R/W	0h	Drives tx_vmargin PMA input for the associated lane when in PHY macro and PMA isolation mode.
15-14	PHY_PMA_ISO_TX_FSLF_15_14	R	0h	Reserved
13-8	PHY_PMA_ISO_TX_FSLF_13_8	R	2Dh	Current value of tx_local_fs PMA output for the associated lane. (Not re-synchronized to apb_pclk)
7-6	PHY_PMA_ISO_TX_FSLF_7_6	R	0h	Reserved

**Table 11-965. PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
5-0	PHY_PMA_ISO_TX_FSLF_5_0	R	Fh	Current value of tx_local_if PMA output for the associated lane. (Not re-synchronized to app_pclk)

Table 11-966. Register Call Summary for PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Register \(Offset = F010h + formula\) \[reset = 2D0Fh\]: \[0\]](#)

11.322 PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register (Offset = F014h + formula) [reset = 1000h]

PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j is shown in Figure 11-322 and described in Table 11-968.

Return to [Summary Table](#).

PMA Isolation mode control register

Offset = F014h + (j * 200h); where j = 0h to 1h

Table 11-967. PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Instances

Instance	Physical Address
SERDES_16G0	0500 F014h + formula
SERDES_16G1	0501 F014h + formula
SERDES_16G2	0502 F014h + formula
SERDES_16G3	0503 F014h + formula

Figure 11-322. PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_PWRST_CTRL_15_15	PHY_PMA_ISO_PWRST_CTRL_14_14	PHY_PMA_ISO_PWRST_CTRL_13_8					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
PHY_PMA_ISO_PWRST_CTRL_7_6	PHY_PMA_ISO_PWRST_CTRL_5_0						
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
PHY_PMA_ISO_LINK_MODE_15_13			PHY_PMA_ISO_LINK_MODE_12_12	PHY_PMA_ISO_LINK_MODE_11_7			
R-0h			R/W-1h	R-0h			
7	6	5	4	3	2	1	0
PHY_PMA_ISO_LINK_MODE_11_7	PHY_PMA_ISO_LINK_MODE_6_4			PHY_PMA_ISO_LINK_MODE_3_3	PHY_PMA_ISO_LINK_MODE_2_0		
R-0h	R/W-0h			R-0h	R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-968. PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PMA_ISO_PWRST_CTRL_15	R/W	0h	Drives rx_sig_det_en_ext_in_{nnnn} PMA input when in PMA isolation mode.
30	PHY_PMA_ISO_PWRST_CTRL_14	R/W	0h	Drives tx_common_mode_en_ext_in_{nnnn} PMA input when in PMA isolation mode.
29-24	PHY_PMA_ISO_PWRST_CTRL_13_8	R	0h	Current value of xcvr_power_state_ack_in_{nnnn} PMA output.
23-22	PHY_PMA_ISO_PWRST_CTRL_7_6	R	0h	Reserved
21-16	PHY_PMA_ISO_PWRST_CTRL_5_0	R/W	0h	Drives xcvr_power_state_req_in_{nnnn} PMA input when in PMA isolation mode.

Table 11-968. PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	PHY_PMA_ISO_LINK_M ODE_15_13	R	0h	Reserved
12	PHY_PMA_ISO_LINK_M ODE_12	R/W	1h	Drives xcvr_master_in_{nnnn} PMA input when in PMA isolation mode.
11-7	PHY_PMA_ISO_LINK_M ODE_11_7	R	0h	Reserved
6-4	PHY_PMA_ISO_LINK_M ODE_6_4	R/W	0h	Drives xcvr_standard_mode_in_{nnnn} PMA input when in PMA isolation mode.
3	PHY_PMA_ISO_LINK_M ODE_3	R	0h	Reserved
2-0	PHY_PMA_ISO_LINK_M ODE_2_0	R/W	0h	Drives xcvr_data_width_in_{nnnn} PMA input when in PMA isolation mode.

Table 11-969. Register Call Summary for PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register \(Offset = F014h + formula\) \[reset = 1000h\]: \[0\]](#)

11.323 PHY_PMA_ISO_RX_EQ_CTRL_j Register (Offset = F018h + formula) [reset = X]

PHY_PMA_ISO_RX_EQ_CTRL_j is shown in Figure 11-323 and described in Table 11-971.

Return to [Summary Table](#).

PMA RX equalization control isolation register

Offset = F018h + (j * 200h); where j = 0h to 1h

Table 11-970. PHY_PMA_ISO_RX_EQ_CTRL_j Instances

Instance	Physical Address
SERDES_16G0	0500 F018h + formula
SERDES_16G1	0501 F018h + formula
SERDES_16G2	0502 F018h + formula
SERDES_16G3	0503 F018h + formula

Figure 11-323. PHY_PMA_ISO_RX_EQ_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_RX_EQ_CTRL_15_14	PHY_PMA_ISO_RX_EQ_CTRL_13	PHY_PMA_ISO_RX_EQ_CTRL_12	PHY_PMA_ISO_RX_EQ_CTRL_11	PHY_PMA_ISO_RX_EQ_CTRL_10	PHY_PMA_ISO_RX_EQ_CTRL_9_4		
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R-0h		
23	22	21	20	19	18	17	16
PHY_PMA_ISO_RX_EQ_CTRL_9_4				PHY_PMA_ISO_RX_EQ_CTRL_3	PHY_PMA_ISO_RX_EQ_CTRL_2	PHY_PMA_ISO_RX_EQ_CTRL_1	PHY_PMA_ISO_RX_EQ_CTRL_0
R-0h				R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-971. PHY_PMA_ISO_RX_EQ_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PMA_ISO_RX_EQ_CTRL_15_14	R	0h	Reserved
29	PHY_PMA_ISO_RX_EQ_CTRL_13	R/W	0h	Drives rx_eq_training_data_valid PMA input for the associated lane when in PMA isolation mode.
28	PHY_PMA_ISO_RX_EQ_CTRL_12	R/W	0h	Drives rx_eq_training PMA input for the associated lane when in PMA isolation mode.
27	PHY_PMA_ISO_RX_EQ_CTRL_11	R/W	0h	Drives rx_eq_eval_cnt_rst PMA input for the associated lane when in PMA isolation mode.
26	PHY_PMA_ISO_RX_EQ_CTRL_10	R	0h	Reserved
25-20	PHY_PMA_ISO_RX_EQ_CTRL_9_4	R	0h	Current value of rx_link_eval_fb_dir_change PMA output for the associated lane, when PHY_PMA_ISO_RX_EQ_CTRL[0] == 1 and PHY_PMA_ISO_RX_EQ_CTRL[1] == 1. Otherwise, 0. (Not re-synchronized to apb_pclk)

Table 11-971. PHY_PMA_ISO_RX_EQ_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	PHY_PMA_ISO_RX_EQ_CTRL_3	R	0h	Current value of rx_eq_eval_complete PMA output for the associated lane, when PHY_PMA_ISO_RX_EQ_CTRL[0] == 1 and PHY_PMA_ISO_RX_EQ_CTRL[1] == 1. Otherwise, 0. (Not re-synchronized to apb_pclk)
18	PHY_PMA_ISO_RX_EQ_CTRL_2	R/W	0h	Drives rx_invalid_request PMA input for the associated lane when in PMA isolation mode.
17	PHY_PMA_ISO_RX_EQ_CTRL_1	R	0h	Current value of rx_eq_eval_status PMA output for the associated lane.
16	PHY_PMA_ISO_RX_EQ_CTRL_0	R/W	0h	Drives rx_eq_eval PMA input for the associated lane when in PMA isolation mode.
15-0	RESERVED	R/W	X	

Table 11-972. Register Call Summary for PHY_PMA_ISO_RX_EQ_CTRL_j

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_RX_EQ_CTRL_j Register \(Offset = F018h + formula\) \[reset = X\]: \[0\]](#)

11.324 PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Register (Offset = F01Ch + formula) [reset = 0h]

PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j is shown in Figure 11-324 and described in Table 11-974.

Return to [Summary Table](#).

PMA low data isolation register

Offset = F01Ch + (j * 200h); where j = 0h to 1h

Table 11-973. PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Instances

Instance	Physical Address
SERDES_16G0	0500 F01Ch + formula
SERDES_16G1	0501 F01Ch + formula
SERDES_16G2	0502 F01Ch + formula
SERDES_16G3	0503 F01Ch + formula

Figure 11-324. PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_PMA_ISO_DATA_HI_15_0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PMA_ISO_DATA_LO_15_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 11-974. PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_PMA_ISO_DATA_HI_15_0	R	0h	Current value of rx_rd[31:16] PMA output for the current lane. (Not re-synchronized to apb_pclk). This register can be written and the value will drive tx_td[31:16] for the associated lane when in PMA isolation mode.
15-0	PHY_PMA_ISO_DATA_LO_15_0	R	0h	Current value of rx_rd[15:0] PMA output for the current lane. (Not re-synchronized to apb_pclk). This register can be written and the value will drive tx_td[15:0] for the associated lane when in PMA isolation mode.

Table 11-975. Register Call Summary for PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j

16-G SerDes Registers
<ul style="list-style-type: none"> 2-L SerDes Registers: [0] [1] PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Register (Offset = F01Ch + formula) [reset = 0h]: [0]

11.325 PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j Register (Offset = F020h + formula) [reset = 0h]

PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j is shown in Figure 11-325 and described in Table 11-977.

Return to [Summary Table](#).

PMA RX lane margining control isolation register

Offset = F020h + (j * 200h); where j = 0h to 1h

Table 11-976.
PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j
Instances

Instance	Physical Address
SERDES_16G0	0500 F020h + formula
SERDES_16G1	0501 F020h + formula
SERDES_16G2	0502 F020h + formula
SERDES_16G3	0503 F020h + formula

Figure 11-325. PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_LN_MRGN_RESULT_15_6							
R-0h							
23	22	21	20	19	18	17	16
PHY_PMA_ISO_LN_MRGN_RESULT_15_6		PHY_PMA_ISO_LN_MRGN_RESULT_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
PHY_PMA_ISO_LN_MRGN_CTRL_15		PHY_PMA_ISO_LN_MRGN_CTRL_14_8					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
PHY_PMA_ISO_LN_MRGN_CTRL_7_6		PHY_PMA_ISO_LN_MRGN_CTRL_5_4		PHY_PMA_ISO_LN_MRGN_CTRL_3_2		PHY_PMA_ISO_LN_MRGN_CTRL_1	PHY_PMA_ISO_LN_MRGN_CTRL_0
R-0h		R/W-0h		R-0h		R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-977. PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	PHY_PMA_ISO_LN_MRGN_RESULT_15_6	R	0h	Reserved
21-16	PHY_PMA_ISO_LN_MRGN_RESULT_5_0	R	0h	Captures rx_mrgn_errcnt PMA output for the associated lane.
15	PHY_PMA_ISO_LN_MRGN_CTRL_15	R	0h	Reserved
14-8	PHY_PMA_ISO_LN_MRGN_CTRL_14_8	R/W	0h	Drives rx_mrgn_offset PMA input for the associated lane when in PMA isolation mode.
7-6	PHY_PMA_ISO_LN_MRGN_CTRL_7_6	R	0h	Reserved

Table 11-977. PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	PHY_PMA_ISO_LN_MRGN_CTRL_5_4	R/W	0h	Drives rx_mrgn_dir PMA input for the associated lane when in PMA isolation mode.
3-2	PHY_PMA_ISO_LN_MRGN_CTRL_3_2	R	0h	Reserved
1	PHY_PMA_ISO_LN_MRGN_CTRL_1	R	0h	Captures rx_mrgn_valid PMA output for the associated lane.
0	PHY_PMA_ISO_LN_MRGN_CTRL_0	R/W	0h	Drives rx_mrgn_req PMA input for the associated lane when in PMA isolation mode.

**Table 11-978. Register Call Summary for
PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j**

16-G SerDes Registers

- [2-L SerDes Registers: \[0\] \[1\]](#)
- [PHY_PMA_ISO_LN_MRGN_RESULT__PHY_PMA_ISO_LN_MRGN_CTRL_j Register \(Offset = F020h + formula\) \[reset = 0h\]: \[0\]](#)

12 4-L SerDes Registers

Table 12-2 lists the memory-mapped registers for the SERDES_10G registers. All register offset addresses not listed in Table 12-2 should be considered as reserved locations and the register contents should not be modified.

The WIZ registers are overlayed starting at offset 0x400.

Table 12-1. SERDES_10G Instances

Instance	Base Address
SERDES_10G0	0505 0000h

Table 12-2. SERDES_10G Registers

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
0h	CMN_PID_TYPE		0505 0000h
4h	CMN_PID_NUM		0505 0004h
8h	CMN_PID_REV		0505 0008h
10h	CMN_PID_NODE__CMN_PID_MFG		0505 0010h
14h	CMN_PID_FLV1__CMN_PID_FLV0		0505 0014h
18h	CMN_PID_LANES__CMN_PID_IOV		0505 0018h
20h	CMN_PID_METAL1__CMN_PID_METAL0		0505 0020h
24h	CMN_PID_METAL3__CMN_PID_METAL2		0505 0024h
28h	CMN_PID_METALD		0505 0028h
40h	CMN_SSM_BANDGAP_TMR__CMN_SSM_SM_CTRL		0505 0040h
44h	CMN_SSM_BIAS_TMR		0505 0044h
4Ch	CMN_SSM_USER_DEF_CTRL		0505 004Ch
50h	CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL		0505 0050h
54h	CMN_PLLSM0_PLLVREF_TMR__CMN_PLLSM0_PLLPRE_TMR		0505 0054h
58h	CMN_PLLSM0_PLLCLKDIS_TMR__CMN_PLLSM0_PLLOCK_TMR		0505 0058h
5Ch	CMN_PLLSM0_USER_DEF_CTRL		0505 005Ch
60h	CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL		0505 0060h
64h	CMN_PLLSM1_PLLVREF_TMR__CMN_PLLSM1_PLLPRE_TMR		0505 0064h
68h	CMN_PLLSM1_PLLCLKDIS_TMR__CMN_PLLSM1_PLLOCK_TMR		0505 0068h
6Ch	CMN_PLLSM1_USER_DEF_CTRL		0505 006Ch
80h	CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR		0505 0080h
84h	CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT		0505 0084h
88h	CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT		0505 0088h
8Ch	CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT		0505 008Ch
90h	CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT		0505 0090h
94h	CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT		0505 0094h
98h	CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD		0505 0098h
9Ch	CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL		0505 009Ch
A0h	CMN_CDIAG_REFCLK_DRV0_CTRL		0505 00A0h

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
B8h	CMN_CDIAG_RST_DIAG_CMN_CDIAG_CDB_DIAG		0505 00B8h
BCh	CMN_CDIAG_DCYA		0505 00BCh
C0h	CMN_BGCAL_OVRD_CMN_BGCAL_CTRL		0505 00C0h
C4h	CMN_BGCAL_TUNE_CMN_BGCAL_START		0505 00C4h
C8h	CMN_BGCAL_ITER_TMR_CMN_BGCAL_INIT_TMR		0505 00C8h
E0h	CMN_IBCAL_OVRD_CMN_IBCAL_CTRL		0505 00E0h
E4h	CMN_IBCAL_TUNE_CMN_IBCAL_START		0505 00E4h
E8h	CMN_IBCAL_ITER_TMR_CMN_IBCAL_INIT_TMR		0505 00E8h
100h	CMN_PLL0_VCOCAL_START_CMN_PLL0_VCOCAL_C TRL		0505 0100h
104h	CMN_PLL0_VCOCAL_OVRD_CMN_PLL0_VCOCAL_TC TRL		0505 0104h
108h	CMN_PLL0_VCOCAL_ITER_TMR_CMN_PLL0_VCOCA L_INIT_TMR		0505 0108h
10Ch	CMN_PLL0_VCOCAL_REFTIM_START		0505 010Ch
110h	CMN_PLL0_VCOCAL_PLLCNT_START		0505 0110h
120h	CMN_PLL0_FRACDIVL_M0_CMN_PLL0_INTDIV_M0		0505 0120h
124h	CMN_PLL0_HIGH_THR_M0_CMN_PLL0_FRACDIVH_M 0		0505 0124h
128h	CMN_PLL0_DSM_FBH_OVRD_M0_CMN_PLL0_DSM_ DIAG_M0		0505 0128h
12Ch	CMN_PLL0_DSM_FBL_OVRD_M0		0505 012Ch
130h	CMN_PLL0_SS_CTRL2_M0_CMN_PLL0_SS_CTRL1_M 0		0505 0130h
134h	CMN_PLL0_SS_CTRL4_M0_CMN_PLL0_SS_CTRL3_M 0		0505 0134h
138h	CMN_PLL0_LOCK_REFCNT_IDLE_CMN_PLL0_LOCK_ REFCNT_START		0505 0138h
13Ch	CMN_PLL0_LOCK_PLLCNT_THR_CMN_PLL0_LOCK_ PLLCNT_START		0505 013Ch
140h	CMN_PLL0_FRACDIVL_M1_CMN_PLL0_INTDIV_M1		0505 0140h
144h	CMN_PLL0_HIGH_THR_M1_CMN_PLL0_FRACDIVH_M 1		0505 0144h
148h	CMN_PLL0_DSM_FBH_OVRD_M1_CMN_PLL0_DSM_ DIAG_M1		0505 0148h
14Ch	CMN_PLL0_DSM_FBL_OVRD_M1		0505 014Ch
150h	CMN_PLL0_SS_CTRL2_M1_CMN_PLL0_SS_CTRL1_M 1		0505 0150h
154h	CMN_PLL0_SS_CTRL4_M1_CMN_PLL0_SS_CTRL3_M 1		0505 0154h
180h	CMN_PLL1_VCOCAL_START_CMN_PLL1_VCOCAL_C TRL		0505 0180h
184h	CMN_PLL1_VCOCAL_OVRD_CMN_PLL1_VCOCAL_TC TRL		0505 0184h
188h	CMN_PLL1_VCOCAL_ITER_TMR_CMN_PLL1_VCOCA L_INIT_TMR		0505 0188h
18Ch	CMN_PLL1_VCOCAL_REFTIM_START		0505 018Ch
190h	CMN_PLL1_VCOCAL_PLLCNT_START		0505 0190h
1A0h	CMN_PLL1_FRACDIVL_M0_CMN_PLL1_INTDIV_M0		0505 01A0h
1A4h	CMN_PLL1_HIGH_THR_M0_CMN_PLL1_FRACDIVH_M 0		0505 01A4h

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
1A8h	CMN_PLL1_DSM_FBH_OVRD_M0_CMN_PLL1_DSM_DIAG_M0		0505 01A8h
1ACh	CMN_PLL1_DSM_FBL_OVRD_M0		0505 01ACh
1B0h	CMN_PLL1_SS_CTRL2_M0_CMN_PLL1_SS_CTRL1_M0		0505 01B0h
1B4h	CMN_PLL1_SS_CTRL4_M0_CMN_PLL1_SS_CTRL3_M0		0505 01B4h
1B8h	CMN_PLL1_LOCK_REFCNT_IDLE_CMN_PLL1_LOCK_REFCNT_START		0505 01B8h
1BCh	CMN_PLL1_LOCK_PLLCNT_THR_CMN_PLL1_LOCK_PLLCNT_START		0505 01BCh
200h	CMN_TXPUCAL_OVRD_CMN_TXPUCAL_CTRL		0505 0200h
204h	CMN_TXPUCAL_TUNE_CMN_TXPUCAL_START		0505 0204h
208h	CMN_TXPUCAL_ITER_TMR_CMN_TXPUCAL_INIT_TMR		0505 0208h
210h	CMN_TXPDCAL_OVRD_CMN_TXPDCAL_CTRL		0505 0210h
214h	CMN_TXPDCAL_TUNE_CMN_TXPDCAL_START		0505 0214h
218h	CMN_TXPDCAL_ITER_TMR_CMN_TXPDCAL_INIT_TMR		0505 0218h
220h	CMN_RXCAL_OVRD_CMN_RXCAL_CTRL		0505 0220h
224h	CMN_RXCAL_TUNE_CMN_RXCAL_START		0505 0224h
228h	CMN_RXCAL_ITER_TMR_CMN_RXCAL_INIT_TMR		0505 0228h
240h	CMN_SD_CAL_START_CMN_SD_CAL_CTRL		0505 0240h
244h	CMN_SD_CAL_OVRD_CMN_SD_CAL_TCTRL		0505 0244h
248h	CMN_SD_CAL_ITER_TMR_CMN_SD_CAL_INIT_TMR		0505 0248h
24Ch	CMN_SD_CAL_REFTIM_START		0505 024Ch
250h	CMN_SD_CAL_PLLCNT_START		0505 0250h
300h	CMN_CMSMT_TEST_CLK_SEL_CMN_CMSMT_CLK_F REQ_MSMT_CTRL		0505 0300h
304h	CMN_CMSMT_TEST_CLK_CNT_VALUE_CMN_CMSMT _REF_CLK_TMR_VALUE		0505 0304h
340h	CMN_PDIAG_PLL0_CLK_SEL_M0_CMN_PDIAG_PLL0 _CTRL_M0		0505 0340h
344h	CMN_PDIAG_PLL0_ITRIM_M0_CMN_PDIAG_PLL0_OV RD_M0		0505 0344h
348h	CMN_PDIAG_PLL0_CP_IADJ_M0_CMN_PDIAG_PLL0 _CP_PADJ_M0		0505 0348h
34Ch	CMN_PDIAG_PLL0_CP_TUNE_M0_CMN_PDIAG_PLL0 _FILT_PADJ_M0		0505 034Ch
360h	CMN_PDIAG_PLL0_CLK_SEL_M1_CMN_PDIAG_PLL0 _CTRL_M1		0505 0360h
364h	CMN_PDIAG_PLL0_ITRIM_M1_CMN_PDIAG_PLL0_OV RD_M1		0505 0364h
368h	CMN_PDIAG_PLL0_CP_IADJ_M1_CMN_PDIAG_PLL0 _CP_PADJ_M1		0505 0368h
36Ch	CMN_PDIAG_PLL0_CP_TUNE_M1_CMN_PDIAG_PLL0 _FILT_PADJ_M1		0505 036Ch
380h	CMN_PDIAG_PLL1_CLK_SEL_M0_CMN_PDIAG_PLL1 _CTRL_M0		0505 0380h
384h	CMN_PDIAG_PLL1_ITRIM_M0_CMN_PDIAG_PLL1_OV RD_M0		0505 0384h

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
388h	CMN_PDIAG_PLL1_CP_IADJ_M0_CMN_PDIAG_PLL1_CP_PADJ_M0		0505 0388h
38Ch	CMN_PDIAG_PLL1_CP_TUNE_M0_CMN_PDIAG_PLL1_FILT_PADJ_M0		0505 038Ch
3C0h	CMN_DIAG_BIAS_OVRD1_CMN_DIAG_BANDGAP_OVRD		0505 03C0h
3C4h	CMN_DIAG_VREG_CTRL_CMN_DIAG_BIAS_OVRD2		0505 03C4h
3C8h	CMN_DIAG_SH_BANDGAP_CMN_DIAG_PM_CTRL		0505 03C8h
3CCh	CMN_DIAG_SH_SDCLK_CMN_DIAG_SH_RESISTOR		0505 03CCh
3D0h	CMN_DIAG_ATB_CTRL2_CMN_DIAG_ATB_CTRL1		0505 03D0h
3D4h	CMN_DIAG_ATB_ADC_CTRL1_CMN_DIAG_ATB_ADC_CTRL0		0505 03D4h
3D8h	CMN_DIAG_RST_DIAG_CMN_DIAG_HSRSM_CTRL		0505 03D8h
3DCh	CMN_DIAG_ACYA_CMN_DIAG_DCYA		0505 03DCh
400h	MOD_VER	Module and Version	0505 0400h
404h	SERDES_CTRL	Serdes Control	0505 0404h
408h	SERDES_TOP_CTRL	Serdes Top Level Control	0505 0408h
40Ch	SERDES_RST	Serdes reset	0505 040Ch
410h	SERDES_TYPEC	Serdes Type C control	0505 0410h
480h	LANECTL0	Lane Control 0	0505 0480h
484h	LANEDIV0	Lane Divider 0	0505 0484h
488h	LANALIGN0	Lane Align 0	0505 0488h
48Ch	LANESTS0	Lane Status 0	0505 048Ch
4C0h	LANECTL1	Lane Control 1	0505 04C0h
4C4h	LANEDIV1	Lane Divider 1	0505 04C4h
4C8h	LANALIGN1	Lane Align 1	0505 04C8h
4CCh	LANESTS1	Lane Status 1	0505 04CCh
500h	LANECTL2	Lane Control 2	0505 0500h
504h	LANEDIV2	Lane Divider 2	0505 0504h
508h	LANALIGN2	Lane Align 2	0505 0508h
50Ch	LANESTS2	Lane Status 2	0505 050Ch
540h	LANECTL3	Lane Control 3	0505 0540h
544h	LANEDIV3	Lane Divider 3	0505 0544h
548h	LANALIGN3	Lane Align 3	0505 0548h
54Ch	LANESTS3	Lane Status 3	0505 054Ch
5F8h	DTB_MUX_SEL	Digital Test Bus Mux Select	0505 05F8h
5FCh	DIAG_TEST	Diagnostic Test Register	0505 05FCh
2000h + formula	RESERVEDBIT13ADDRESSA_y		0505 2000h + formula
4000h + formula	XCVR_PSM_RCTRL_XCVR_PSM_CTRL_j		0505 4000h + formula
4004h + formula	XCVR_PSM_A0IN_TMR_XCVR_PSM_CALIN_TMR_j		0505 4004h + formula
4008h + formula	XCVR_PSM_A1IN_TMR_XCVR_PSM_A0BYP_TMR_j		0505 4008h + formula
400Ch + formula	XCVR_PSM_A3IN_TMR_XCVR_PSM_A2IN_TMR_j		0505 400Ch + formula
4010h + formula	XCVR_PSM_A5IN_TMR_XCVR_PSM_A4IN_TMR_j		0505 4010h + formula

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
4014h + formula	XCVR_PSM_A0OUT_TMR_XCVR_PSM_CALOUT_TMR_j		0505 4014h + formula
4018h + formula	XCVR_PSM_A2OUT_TMR_XCVR_PSM_A1OUT_TMR_j		0505 4018h + formula
401Ch + formula	XCVR_PSM_A4OUT_TMR_XCVR_PSM_A3OUT_TMR_j		0505 401Ch + formula
4020h + formula	XCVR_PSM_RDY_TMR_XCVR_PSM_A5OUT_TMR_j		0505 4020h + formula
4024h + formula	XCVR_PSM_ST_0_XCVR_PSM_DIAG_j		0505 4024h + formula
4028h + formula	XCVR_PSM_ST_1_j		0505 4028h + formula
403Ch + formula	XCVR_PSM_USER_DEF_CTRL_j		0505 403Ch + formula
4080h + formula	TX_TXCC_PRE_OVRD_TX_TXCC_CTRL_j		0505 4080h + formula
4084h + formula	TX_TXCC_POST_OVRD_TX_TXCC_MAIN_OVRD_j		0505 4084h + formula
4088h + formula	TX_TXCC_MAIN_CVAL_TX_TXCC_PRE_CVAL_j		0505 4088h + formula
408Ch + formula	TX_TXCC_LF_MULT_TX_TXCC_POST_CVAL_j		0505 408Ch + formula
4090h + formula	TX_TXCC_CPRE_MULT_01_TX_TXCC_CPRE_MULT_0_0_j		0505 4090h + formula
4094h + formula	TX_TXCC_CPRE_MULT_11_TX_TXCC_CPRE_MULT_1_0_j		0505 4094h + formula
4098h + formula	TX_TXCC_CPOST_MULT_01_TX_TXCC_CPOST_MULT_00_j		0505 4098h + formula
409Ch + formula	TX_TXCC_CPOST_MULT_11_TX_TXCC_CPOST_MULT_10_j		0505 409Ch + formula
40A0h + formula	TX_TXCC_MGNFS_MULT_001_TX_TXCC_MGNFS_MULT_000_j		0505 40A0h + formula
40A4h + formula	TX_TXCC_MGNFS_MULT_011_TX_TXCC_MGNFS_MULT_010_j		0505 40A4h + formula
40A8h + formula	TX_TXCC_MGNFS_MULT_101_TX_TXCC_MGNFS_MULT_100_j		0505 40A8h + formula
40ACh + formula	TX_TXCC_MGNFS_MULT_111_TX_TXCC_MGNFS_MULT_110_j		0505 40ACh + formula
40B0h + formula	TX_TXCC_MGNHS_MULT_001_TX_TXCC_MGNHS_MULT_000_j		0505 40B0h + formula
40B4h + formula	TX_TXCC_MGNHS_MULT_011_TX_TXCC_MGNHS_MULT_010_j		0505 40B4h + formula
40B8h + formula	TX_TXCC_MGNHS_MULT_101_TX_TXCC_MGNHS_MULT_100_j		0505 40B8h + formula
40BCh + formula	TX_TXCC_MGNHS_MULT_111_TX_TXCC_MGNHS_MULT_110_j		0505 40BCh + formula
40C0h + formula	TX_TXCC_P1PRE_COEF_MULT_TX_TXCC_P0PRE_COEF_MULT_j		0505 40C0h + formula
40C4h + formula	TX_TXCC_P3PRE_COEF_MULT_TX_TXCC_P2PRE_COEF_MULT_j		0505 40C4h + formula
40C8h + formula	TX_TXCC_P5PRE_COEF_MULT_TX_TXCC_P4PRE_COEF_MULT_j		0505 40C8h + formula
40CCh + formula	TX_TXCC_P7PRE_COEF_MULT_TX_TXCC_P6PRE_COEF_MULT_j		0505 40CCh + formula

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
40D0h + formula	TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_C_OEF_MULT_j		0505 40D0h + formula
40E0h + formula	TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j		0505 40E0h + formula
40E4h + formula	TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j		0505 40E4h + formula
40E8h + formula	TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j		0505 40E8h + formula
40ECh + formula	TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j		0505 40ECh + formula
40F0h + formula	TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j		0505 40F0h + formula
4180h + formula	DRV_DIAG_LANE_FCM_EN_SWAIT_TMR__DRV_DIAG_LANE_FCM_EN_TO_j		0505 4180h + formula
4184h + formula	DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j		0505 4184h + formula
4188h + formula	DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j		0505 4188h + formula
418Ch + formula	DRV_DIAG_TX_DRV_j		0505 418Ch + formula
41C0h + formula	XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j		0505 41C0h + formula
41C4h + formula	XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j		0505 41C4h + formula
41C8h + formula	XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j		0505 41C8h + formula
41CCh + formula	XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j		0505 41CCh + formula
41D0h + formula	XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j		0505 41D0h + formula
41D4h + formula	XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j		0505 41D4h + formula
41D8h + formula	XCVR_DIAG_XCVR_CLK_CTRL__XCVR_DIAG_RST_DIAG_j		0505 41D8h + formula
41DCh + formula	XCVR_DIAG_DCYA_j		0505 41DCh + formula
4200h + formula	TX_PSC_A1__TX_PSC_A0_j		0505 4200h + formula
4204h + formula	TX_PSC_A3__TX_PSC_A2_j		0505 4204h + formula
4208h + formula	TX_PSC_A5__TX_PSC_A4_j		0505 4208h + formula
420Ch + formula	TX_PSC_RDY__TX_PSC_CAL_j		0505 420Ch + formula
4240h + formula	TX_RCVDET_OVRD__TX_RCVDET_CTRL_j		0505 4240h + formula
4244h + formula	TX_RCVDET_ST_TMR__TX_RCVDET_EN_TMR_j		0505 4244h + formula
4280h + formula	TX_BIST_UDDWR__TX_BIST_CTRL_j		0505 4280h + formula
4284h + formula	TX_BIST_SEED1__TX_BIST_SEED0_j		0505 4284h + formula
43C0h + formula	TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j		0505 43C0h + formula

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
43C4h + formula	TX_DIAG_ELEC_IDLE_j		0505 43C4h + formula
43C8h + formula	TX_DIAG_RST_DIAG_j		0505 43C8h + formula
43CCh + formula	TX_DIAG_ACYA__TX_DIAG_DCYA_j		0505 43CCh + formula
6000h + formula	RESERVEDBIT13ADDRESSB_y		0505 6000h + formula
8000h + formula	RX_PSC_A1__RX_PSC_A0_j		0505 8000h + formula
8004h + formula	RX_PSC_A3__RX_PSC_A2_j		0505 8004h + formula
8008h + formula	RX_PSC_A5__RX_PSC_A4_j		0505 8008h + formula
800Ch + formula	RX_PSC_RDY__RX_PSC_CAL_j		0505 800Ch + formula
8080h + formula	RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j		0505 8080h + formula
8084h + formula	RX_SDCAL0_TUNE__RX_SDCAL0_START_j		0505 8084h + formula
8088h + formula	RX_SDCAL0_ITER_TMR__RX_SDCAL0_INIT_TMR_j		0505 8088h + formula
8090h + formula	RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j		0505 8090h + formula
8094h + formula	RX_SDCAL1_TUNE__RX_SDCAL1_START_j		0505 8094h + formula
8098h + formula	RX_SDCAL1_ITER_TMR__RX_SDCAL1_INIT_TMR_j		0505 8098h + formula
80B0h + formula	RX_SAMP_DAC_CTRL_j		0505 80B0h + formula
80C0h + formula	RX_SLC_IPP_STAT__RX_SLC_CTRL_j		0505 80C0h + formula
80C4h + formula	RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j		0505 80C4h + formula
80C8h + formula	RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j		0505 80C8h + formula
80CCh + formula	RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j		0505 80CCh + formula
80D0h + formula	RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j		0505 80D0h + formula
80D4h + formula	RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j		0505 80D4h + formula
80D8h + formula	RX_SLC_INIT_TMR__RX_SLC_EPM_OVRD_j		0505 80D8h + formula
80DCh + formula	RX_SLC_DIAG_CTRL__RX_SLC_RUN_TMR_j		0505 80DCh + formula
80E0h + formula	RX_SLC_DIS_j		0505 80E0h + formula
8100h + formula	RX_CDRLF_CNFG2__RX_CDRLF_CNFG_j		0505 8100h + formula
8104h + formula	RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j		0505 8104h + formula
8108h + formula	RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j		0505 8108h + formula

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
8120h + formula	RX_SIGDET_HL_DLY_TMR__RX_SIGDET_HL_FILT_TM R_j		0505 8120h + formula
8124h + formula	RX_SIGDET_HL_INIT_TMR__RX_SIGDET_HL_MIN_TM R_j		0505 8124h + formula
8128h + formula	RX_SIGDET_LH_DLY_TMR__RX_SIGDET_LH_FILT_TM R_j		0505 8128h + formula
812Ch + formula	RX_SIGDET_LH_INIT_TMR__RX_SIGDET_LH_MIN_TM R_j		0505 812Ch + formula
8130h + formula	RX_LFPSDET_NS_CNT__RX_LFPSDET_MD_CNT_j		0505 8130h + formula
8134h + formula	RX_LFPSDET_MP_CNT__RX_LFPSDET_RD_CNT_j		0505 8134h + formula
8138h + formula	RX_LFPSDET_DIAG_CTRL_j		0505 8138h + formula
8140h + formula	RX_EYESURF_CTRL_j		0505 8140h + formula
8148h + formula	RX_EYESURF_TMR_DELHIGH__RX_EYESURF_TMR_D ELLOW_j		0505 8148h + formula
814Ch + formula	RX_EYESURF_TMR_TESTHIGH__RX_EYESURF_TMR_ TESTLOW_j		0505 814Ch + formula
8150h + formula	RX_EYESURF_EW_COORD__RX_EYESURF_NS_COO RD_j		0505 8150h + formula
8154h + formula	RX_EYESURF_ERRCNT_j		0505 8154h + formula
8160h + formula	RX_BIST_SYNCCNT__RX_BIST_CTRL_j		0505 8160h + formula
8164h + formula	RX_BIST_ERRCNT__RX_BIST_UDDWR_j		0505 8164h + formula
8200h + formula	RX_REE_PTSEQSM_EQENM_EVAL__RX_REE_PTSEQ SM_CTRL_j		0505 8200h + formula
8204h + formula	RX_REE_PTSEQSM_PEVAL_TMR__RX_REE_PTSEQS M_EQENM_PEVAL_j		0505 8204h + formula
8208h + formula	RX_REE_PTSEQSM_MAX_EVAL_CNT__RX_REE_PTXE QSM_TIMEOUT_TMR_j		0505 8208h + formula
8210h + formula	RX_REE_GCSM1_EQENM_PH1__RX_REE_GCSM1_CT RL_j		0505 8210h + formula
8214h + formula	RX_REE_GCSM1_START_TMR__RX_REE_GCSM1_EQ ENM_PH2_j		0505 8214h + formula
8218h + formula	RX_REE_GCSM1_RUN_PH2_TMR__RX_REE_GCSM1_ RUN_PH1_TMR_j		0505 8218h + formula
8220h + formula	RX_REE_GCSM2_EQENM_PH1__RX_REE_GCSM2_CT RL_j		0505 8220h + formula
8224h + formula	RX_REE_GCSM2_START_TMR__RX_REE_GCSM2_EQ ENM_PH2_j		0505 8224h + formula
8228h + formula	RX_REE_GCSM2_RUN_PH2_TMR__RX_REE_GCSM2_ RUN_PH1_TMR_j		0505 8228h + formula
8230h + formula	RX_REE_PERGCSM_EQENM_PH1__RX_REE_PERGC SM_CTRL_j		0505 8230h + formula
8234h + formula	RX_REE_PERGCSM_START_TMR__RX_REE_PERGCS M_EQENM_PH2_j		0505 8234h + formula
8238h + formula	RX_REE_PERGCSM_RUN_PH2_TMR__RX_REE_PERG CSM_RUN_PH1_TMR_j		0505 8238h + formula
8240h + formula	RX_REE_U3GCSM_EQENM_PH1__RX_REE_U3GCSM_ CTRL_j		0505 8240h + formula

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
8244h + formula	RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j		0505 8244h + formula
8248h + formula	RX_REE_U3GCSM_RUN_PH2_TMR_RX_REE_U3GCSM_RUN_PH1_TMR_j		0505 8248h + formula
8250h + formula	RX_REE_ANAENSM_DEL_TMR_j		0505 8250h + formula
8260h + formula	RX_REE_TXPOST_CODE_CTRL_RX_REE_TXPOST_CTRL_j		0505 8260h + formula
8264h + formula	RX_REE_TXPOST_LTHR_RX_REE_TXPOST_UTHR_j		0505 8264h + formula
8268h + formula	RX_REE_TXPOST_COVRD0_RX_REE_TXPOST_IOVRD_j		0505 8268h + formula
826Ch + formula	RX_REE_TXPOST_DIAG_RX_REE_TXPOST_COVRD1_j		0505 826Ch + formula
8270h + formula	RX_REE_TXPRE_OVRD_RX_REE_TXPRE_CTRL_j		0505 8270h + formula
8274h + formula	RX_REE_TXPRE_DIAG_j		0505 8274h + formula
8280h + formula	RX_REE_PEAK_CODE_CTRL_RX_REE_PEAK_CTRL_j		0505 8280h + formula
8284h + formula	RX_REE_PEAK_LTHR_RX_REE_PEAK_UTHR_j		0505 8284h + formula
8288h + formula	RX_REE_PEAK_COVRD0_RX_REE_PEAK_IOVRD_j		0505 8288h + formula
828Ch + formula	RX_REE_PEAK_DIAG_RX_REE_PEAK_COVRD1_j		0505 828Ch + formula
8290h + formula	RX_REE_ATTEN_THR_RX_REE_ATTEN_CTRL_j		0505 8290h + formula
8294h + formula	RX_REE_ATTEN_OVRD_RX_REE_ATTEN_CNT_j		0505 8294h + formula
8298h + formula	RX_REE_ATTEN_DIAG_j		0505 8298h + formula
82A0h + formula	RX_REE_TAP1_OVRD_RX_REE_TAP1_CTRL_j		0505 82A0h + formula
82A4h + formula	RX_REE_TAP1_DIAG_j		0505 82A4h + formula
82A8h + formula	RX_REE_TAP2_OVRD_RX_REE_TAP2_CTRL_j		0505 82A8h + formula
82ACh + formula	RX_REE_TAP2_DIAG_j		0505 82ACh + formula
82B0h + formula	RX_REE_TAP3_OVRD_RX_REE_TAP3_CTRL_j		0505 82B0h + formula
82B4h + formula	RX_REE_TAP3_DIAG_j		0505 82B4h + formula
82B8h + formula	RX_REE_LFEQ_OVRD_RX_REE_LFEQ_CTRL_j		0505 82B8h + formula
82BCh + formula	RX_REE_LFEQ_DIAG_j		0505 82BCh + formula
82C0h + formula	RX_REE_VGA_GAIN_OVRD_RX_REE_VGA_GAIN_CTRL_j		0505 82C0h + formula
82C4h + formula	RX_REE_VGA_GAIN_TGT_DIAG_RX_REE_VGA_GAIN_DIAG_j		0505 82C4h + formula
82C8h + formula	RX_REE_OFF_COR_OVRD_RX_REE_OFF_COR_CTRL_j		0505 82C8h + formula

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
82CCh + formula	RX_REE_OFF_COR_DIAG_j		0505 82CCh + formula
82D0h + formula	RX_REE_SC_COR_TCNT__RX_REE_SC_COR_WCNT_j		0505 82D0h + formula
82E0h + formula	RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j		0505 82E0h + formula
82E4h + formula	RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLI_P_j		0505 82E4h + formula
82E8h + formula	RX_REE_DIAG_CTRL__RX_REE_FIFO_DIAG_j		0505 82E8h + formula
82ECh + formula	RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j		0505 82ECh + formula
82F0h + formula	RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j		0505 82F0h + formula
82F4h + formula	RX_REE_TXEQEVAL_POST_j		0505 82F4h + formula
8380h + formula	XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j		0505 8380h + formula
8384h + formula	XCVR_CMSMT_TEST_CLK_CNT_VALUE__XCVR_CMSMT_REF_CLK_TMR_VALUE_j		0505 8384h + formula
83C0h + formula	RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j		0505 83C0h + formula
83C4h + formula	RX_DIAG_DFE_AMP_TUNE_3__RX_DIAG_DFE_AMP_TUNE_2_j		0505 83C4h + formula
83C8h + formula	RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j		0505 83C8h + formula
83CCh + formula	RX_DIAG_LFEQ_TUNE_j		0505 83CCh + formula
83D0h + formula	RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j		0505 83D0h + formula
83D4h + formula	RX_DIAG_SD_TEST_j		0505 83D4h + formula
83D8h + formula	RX_DIAG_SH_SLC_IPP__RX_DIAG_SAMP_CTRL_j		0505 83D8h + formula
83DCh + formula	RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j		0505 83DCh + formula
83E0h + formula	RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j		0505 83E0h + formula
83E4h + formula	RX_DIAG_SH_SLC_EPM_j		0505 83E4h + formula
83E8h + formula	RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j		0505 83E8h + formula
83ECh + formula	RX_DIAG_PI_TUNE_j		0505 83ECh + formula
83F0h + formula	RX_DIAG_RST_DIAG__RX_DIAG_LPBK_CTRL_j		0505 83F0h + formula
83FCh + formula	RX_DIAG_ACYA__RX_DIAG_DCYA_j		0505 83FCh + formula
A000h + formula	RESERVEDBIT13ADDRESSC_y		0505 A000h + formula
C000h	PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1		0505 C000h
C004h	PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1		0505 C004h
C008h	PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG		0505 C008h

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
C00Ch	PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DE T_INH		0505 C00Ch
C010h	PHY_ISO_CMN_CTRL		0505 C010h
C014h	PHY_STATE_CHG_TIMEOUT		0505 C014h
C01Ch	PHY_AUTO_CFG_SPDUP		0505 C01Ch
C020h	PHY_REFCLK_DET_THRES_HIGH__PHY_REFCLK_DE T_THRES_LOW		0505 C020h
C024h	PHY_REFCLK_DET_OP_DELAY__PHY_REFCLK_DET_I NTERVAL		0505 C024h
C028h	PHY_REFCLK_DET_ISO_CTRL		0505 C028h
D000h + formula	PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTR L_j		0505 D000h + formula
D004h + formula	PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LP C_HI_j		0505 D004h + formula
D008h + formula	PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_ HI_j		0505 D008h + formula
D00Ch + formula	PHY_PCS_ISO_TX_DATA_HI__PHY_PCS_ISO_TX_DAT A_LO_j		0505 D00Ch + formula
D010h + formula	PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CT RL_j		0505 D010h + formula
D014h + formula	PHY_PCS_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j		0505 D014h + formula
D018h + formula	PHY_PIPE_ISO_USB_BER_CNT_j		0505 D018h + formula
D01Ch + formula	PHY_PCS_ISO_RX_DATA_HI__PHY_PCS_ISO_RX DAT A_LO_j		0505 D01Ch + formula
D020h + formula	PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_ CLK_CFG_j		0505 D020h + formula
D024h + formula	PHY_INTERRUPT_STS_j		0505 D024h + formula
E000h	PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1		0505 E000h
E004h	PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE		0505 E004h
E008h	PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CT RL		0505 E008h
E00Ch	PHY_PMA_ISO_PLL_CTRL1		0505 E00Ch
E014h	PHY_PMA_PLL0_SM_STATE		0505 E014h
E018h	PHY_PMA_PLL1_SM_STATE		0505 E018h
E01Ch	PHY_PMA_ISOLATION_CTRL		0505 E01Ch
F000h + formula	PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j		0505 F000h + formula
F004h + formula	PHY_PMA_ISO_XCVR_CTRL_j		0505 F004h + formula
F008h + formula	PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX_LPC_ LO_j		0505 F008h + formula
F00Ch + formula	PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DM PH_LO_j		0505 F00Ch + formula
F010h + formula	PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j		0505 F010h + formula
F014h + formula	PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_ MODE_j		0505 F014h + formula
F018h + formula	PHY_PMA_ISO_RX_EQ_CTRL_j		0505 F018h + formula

Table 12-2. SERDES_10G Registers (continued)

Offset	Acronym	Register Name	SERDES_10G0 Physical Address
F01Ch + formula	PHY_PMA_ISO_DATA_HI_PHY_PMA_ISO_DATA_LO_j		0505 F01Ch + formula
F020h + formula	PHY_PMA_PSM_STATE_HI_PHY_PMA_PSM_STATE_LO_j		0505 F020h + formula

12.1 CMN_PID_TYPE Register (Offset = 0h) [reset = X]

CMN_PID_TYPE is shown in [Figure 12-1](#) and described in [Table 12-4](#).

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Product type ID register

Table 12-3. CMN_PID_TYPE Instances

Instance	Physical Address
SERDES_10G0	0505 0000h

Figure 12-1. CMN_PID_TYPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMN_PID_TYPE_15_0															
R-7364h															

LEGEND: R = Read Only; -n = value after reset

Table 12-4. CMN_PID_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	CMN_PID_TYPE_15_0	R	7364h	Product type : This field contains the ASCII codes that represent the product type sd for SerDes.

Table 12-5. Register Call Summary for CMN_PID_TYPE

10-G SerDes Registers

- [CMN_PID_TYPE Register \(Offset = 0h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.2 CMN_PID_NUM Register (Offset = 4h) [reset = X]

CMN_PID_NUM is shown in [Figure 12-2](#) and described in [Table 12-7](#).

Return to [Summary Table](#).

Product number ID register

Table 12-6. CMN_PID_NUM Instances

Instance	Physical Address
SERDES_10G0	0505 0004h

Figure 12-2. CMN_PID_NUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMN_PID_NUM_15_0																RESERVED															
R-801h																R-X															

LEGEND: R = Read Only; -n = value after reset

Table 12-7. CMN_PID_NUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMN_PID_NUM_15_0	R	801h	Product number : This field contains the binary coded decimal numbers that represent the product number.
15-0	RESERVED	R	X	

Table 12-8. Register Call Summary for CMN_PID_NUM

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PID_NUM Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)

12.3 CMN_PID_REV Register (Offset = 8h) [reset = X]

CMN_PID_REV is shown in Figure 12-3 and described in Table 12-10.

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Product revision ID register

Table 12-9. CMN_PID_REV Instances

Instance	Physical Address
SERDES_10G0	0505 0008h

Figure 12-3. CMN_PID_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMN_PID_REV_15_0															
R-X																R-120h															

LEGEND: R = Read Only; -n = value after reset

Table 12-10. CMN_PID_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	CMN_PID_REV_15_0	R	120h	Product revision : This field contains the binary coded decimal numbers that represent the product revision.

Table 12-11. Register Call Summary for CMN_PID_REV

10-G SerDes Registers

- [CMN_PID_REV Register \(Offset = 8h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.4 CMN_PID_NODE__CMN_PID_MFG Register (Offset = 10h) [reset = 00160074h]

CMN_PID_NODE__CMN_PID_MFG is shown in [Figure 12-4](#) and described in [Table 12-13](#).

Return to [Summary Table](#).

Product technology manufacturer ID register

Table 12-12. CMN_PID_NODE__CMN_PID_MFG Instances

Instance	Physical Address
SERDES_10G0	0505 0010h

Figure 12-4. CMN_PID_NODE__CMN_PID_MFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMN_PID_NODE_15_0															
R-16h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMN_PID_MFG_15_0															
R-74h															

LEGEND: R = Read Only; -n = value after reset

Table 12-13. CMN_PID_NODE__CMN_PID_MFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMN_PID_NODE_15_0	R	16h	Product technology process node : This field contains the binary coded decimal numbers that represent the product technology node
15-0	CMN_PID_MFG_15_0	R	74h	Product technology manufacturer : This field contains the ASCII codes that represent the product technology manufacturer t for TSMC.

Table 12-14. Register Call Summary for CMN_PID_NODE__CMN_PID_MFG

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PID_NODE__CMN_PID_MFG Register \(Offset = 10h\) \[reset = 00160074h\]: \[0\]](#)

12.5 CMN_PID_FLV1__CMN_PID_FLV0 Register (Offset = 14h) [reset = 63006666h]

CMN_PID_FLV1__CMN_PID_FLV0 is shown in [Figure 12-5](#) and described in [Table 12-16](#).

Return to [Summary Table](#).

Product technology process flavor ID register 0

**Table 12-15. CMN_PID_FLV1__CMN_PID_FLV0
Instances**

Instance	Physical Address
SERDES_10G0	0505 0014h

Figure 12-5. CMN_PID_FLV1__CMN_PID_FLV0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMN_PID_FLV1_15_0															
R-6300h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMN_PID_FLV0_15_0															
R-6666h															

LEGEND: R = Read Only; -n = value after reset

Table 12-16. CMN_PID_FLV1__CMN_PID_FLV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMN_PID_FLV1_15_0	R	6300h	Product technology flavor : This field contains the ASCII codes that represent the second two characters of the product technology flavor. In this case, the second two characters are c .
15-0	CMN_PID_FLV0_15_0	R	6666h	Product technology flavor : This field contains the ASCII codes that represent the first two characters of the product technology flavor. In this case, the first two characters are ff .

Table 12-17. Register Call Summary for CMN_PID_FLV1__CMN_PID_FLV0

10-G SerDes Registers
<ul style="list-style-type: none"> 10-G SerDes Registers: [0] CMN_PID_FLV1__CMN_PID_FLV0 Register (Offset = 14h) [reset = 63006666h]: [0]

12.6 CMN_PID_LANES__CMN_PID_IOV Register (Offset = 18h) [reset = 02020120h]

CMN_PID_LANES__CMN_PID_IOV is shown in Figure 12-6 and described in Table 12-19.

Return to [Summary Table](#).

Product I/O voltage ID register

Table 12-18. CMN_PID_LANES__CMN_PID_IOV Instances

Instance	Physical Address
SERDES_10G0	0505 0018h

Figure 12-6. CMN_PID_LANES__CMN_PID_IOV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMN_PID_LANES_15_8								CMN_PID_LANES_7_0							
R-2h								R-2h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMN_PID_IOV_15_0															
R-120h															

LEGEND: R = Read Only; -n = value after reset

Table 12-19. CMN_PID_LANES__CMN_PID_IOV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PID_LANES_15_8	R	2h	Product SerDes lanes left of common : This field contains the binary coded decimal numbers that represent the number of lanes implemented in this SerDes product on the left side of the common module.
23-16	CMN_PID_LANES_7_0	R	2h	Product SerDes lanes right of common : This field contains the binary coded decimal numbers that represent the number of lanes implemented in this SerDes product on the right side of the common module.
15-0	CMN_PID_IOV_15_0	R	120h	Product I/O voltage : This field contains the binary coded decimal numbers that represent the product I/O voltage. The most significant byte represents the value to the left of the decimal point, and the least significant byte represents the value to the right of the decimal point. For example, 1.5V is represented as 0x0150.

Table 12-20. Register Call Summary for CMN_PID_LANES__CMN_PID_IOV

10-G SerDes Registers

- [CMN_PID_LANES__CMN_PID_IOV Register \(Offset = 18h\) \[reset = 02020120h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.7 CMN_PID_METAL1__CMN_PID_METAL0 Register (Offset = 20h) [reset = 00041020h]

CMN_PID_METAL1__CMN_PID_METAL0 is shown in [Figure 12-7](#) and described in [Table 12-22](#).

Return to [Summary Table](#).

Product metal layers ID register 0

Table 12-21.
CMN_PID_METAL1__CMN_PID_METAL0 Instances

Instance	Physical Address
SERDES_10G0	0505 0020h

Figure 12-7. CMN_PID_METAL1__CMN_PID_METAL0 Register

31	30	29	28	27	26	25	24
CMN_PID_METAL1_15_12				CMN_PID_METAL1_11_8			
R-0h				R-0h			
23	22	21	20	19	18	17	16
CMN_PID_METAL1_7_4				CMN_PID_METAL1_3_0			
R-0h				R-4h			
15	14	13	12	11	10	9	8
CMN_PID_METAL0_15_12				CMN_PID_METAL0_11_8			
R-1h				R-0h			
7	6	5	4	3	2	1	0
CMN_PID_METAL0_7_4				CMN_PID_METAL0_3_0			
R-2h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 12-22. CMN_PID_METAL1__CMN_PID_METAL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_PID_METAL1_15_12	R	0h	Reserved
27-24	CMN_PID_METAL1_11_8	R	0h	Reserved
23-20	CMN_PID_METAL1_7_4	R	0h	Product xy metal layers : This field contains the binary coded decimal number that represent the number of xy metal layers used for this product.
19-16	CMN_PID_METAL1_3_0	R	4h	Product xe metal layers : This field contains the binary coded decimal number that represent the number of xe metal layers used for this product.
15-12	CMN_PID_METAL0_15_12	R	1h	Product xd metal layers : This field contains the binary coded decimal number that represent the number of xd metal layers used for this product.
11-8	CMN_PID_METAL0_11_8	R	0h	Product xc metal layers : This field contains the binary coded decimal number that represent the number of xc metal layers used for this product.
7-4	CMN_PID_METAL0_7_4	R	2h	Product xa metal layers : This field contains the binary coded decimal number that represent the number of xa metal layers used for this product.
3-0	CMN_PID_METAL0_3_0	R	0h	Product x metal layers : This field contains the binary coded decimal number that represent the number of x metal layers used for this product.

Table 12-23. Register Call Summary for CMN_PID_METAL1__CMN_PID_METAL0

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PID_METAL1__CMN_PID_METAL0 Register \(Offset = 20h\) \[reset = 00041020h\]: \[0\]](#)

12.8 CMN_PID_METAL3__CMN_PID_METAL2 Register (Offset = 24h) [reset = 00200000h]

CMN_PID_METAL3__CMN_PID_METAL2 is shown in [Figure 12-8](#) and described in [Table 12-25](#).

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Product metal layers ID register 2

Table 12-24.
CMN_PID_METAL3__CMN_PID_METAL2 Instances

Instance	Physical Address
SERDES_10G0	0505 0024h

Figure 12-8. CMN_PID_METAL3__CMN_PID_METAL2 Register

31	30	29	28	27	26	25	24
CMN_PID_METAL3_15_12				CMN_PID_METAL3_11_8			
R-0h				R-0h			
23	22	21	20	19	18	17	16
CMN_PID_METAL3_7_4				CMN_PID_METAL3_3_0			
R-2h				R-0h			
15	14	13	12	11	10	9	8
CMN_PID_METAL2_15_12				CMN_PID_METAL2_11_8			
R-0h				R-0h			
7	6	5	4	3	2	1	0
CMN_PID_METAL2_7_4				CMN_PID_METAL2_3_0			
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 12-25. CMN_PID_METAL3__CMN_PID_METAL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_PID_METAL3_15_12	R	0h	Product yz metal layers : This field contains the binary coded decimal number that represent the number of yz metal layers used for this product.
27-24	CMN_PID_METAL3_11_8	R	0h	Product u metal layers : This field contains the binary coded decimal number that represent the number of u metal layers used for this product.
23-20	CMN_PID_METAL3_7_4	R	2h	Product r metal layers : This field contains the binary coded decimal number that represent the number of r metal layers used for this product.
19-16	CMN_PID_METAL3_3_0	R	0h	Product z metal layers : This field contains the binary coded decimal number that represent the number of z metal layers used for this product.
15-12	CMN_PID_METAL2_15_12	R	0h	Product yz metal layers : This field contains the binary coded decimal number that represent the number of yz metal layers used for this product.
11-8	CMN_PID_METAL2_11_8	R	0h	Product yy metal layers : This field contains the binary coded decimal number that represent the number of yy metal layers used for this product.
7-4	CMN_PID_METAL2_7_4	R	0h	Product ya metal layers : This field contains the binary coded decimal number that represent the number of ya metal layers used for this product.

Table 12-25. CMN_PID_METAL3__CMN_PID_METAL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CMN_PID_METAL2_3_0	R	0h	Product y metal layers : This field contains the binary coded decimal number that represent the number of y metal layers used for this product.

Table 12-26. Register Call Summary for CMN_PID_METAL3__CMN_PID_METAL2

10-G SerDes Registers

- [CMN_PID_METAL3__CMN_PID_METAL2 Register \(Offset = 24h\) \[reset = 00200000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.9 CMN_PID_METALD Register (Offset = 28h) [reset = X]

CMN_PID_METALD is shown in [Figure 12-9](#) and described in [Table 12-28](#).

[Return to Summary Table.](#)

Product metal layer direction ID register

Table 12-27. CMN_PID_METALD Instances

Instance	Physical Address
SERDES_10G0	0505 0028h

Figure 12-9. CMN_PID_METALD Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
CMN_PID_MET ALD_15	CMN_PID_MET ALD_14	CMN_PID_MET ALD_13	CMN_PID_MET ALD_12	CMN_PID_MET ALD_11	CMN_PID_MET ALD_10	CMN_PID_MET ALD_9	CMN_PID_MET ALD_8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h
7	6	5	4	3	2	1	0
CMN_PID_MET ALD_7	CMN_PID_MET ALD_6	CMN_PID_MET ALD_5	CMN_PID_MET ALD_4	CMN_PID_MET ALD_3	CMN_PID_MET ALD_2	CMN_PID_MET ALD_1	CMN_PID_MET ALD_0
R-0h	R-1h	R-0h	R-1h	R-0h	R-1h	R-0h	R-1h

LEGEND: R = Read Only; -n = value after reset

Table 12-28. CMN_PID_METALD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15	CMN_PID_METALD_15	R	0h	Reserved
14	CMN_PID_METALD_14	R	0h	Reserved
13	CMN_PID_METALD_13	R	0h	Reserved
12	CMN_PID_METALD_12	R	0h	Reserved
11	CMN_PID_METALD_11	R	0h	Metal 11 direction (when used) : 0 = Vertical, 1 = Horizontal
10	CMN_PID_METALD_10	R	0h	Metal 10 direction (when used) : 0 = Vertical, 1 = Horizontal
9	CMN_PID_METALD_9	R	0h	Metal 9 direction (when used) : 0 = Vertical, 1 = Horizontal
8	CMN_PID_METALD_8	R	1h	Metal 8 direction : 0 = Vertical, 1 = Horizontal
7	CMN_PID_METALD_7	R	0h	Metal 7 direction : 0 = Vertical, 1 = Horizontal

Table 12-28. CMN_PID_METALD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CMN_PID_METALD_6	R	1h	Metal 6 direction : 0 = Vertical, 1 = Horizontal
5	CMN_PID_METALD_5	R	0h	Metal 5 direction : 0 = Vertical, 1 = Horizontal
4	CMN_PID_METALD_4	R	1h	Metal 4 direction : 0 = Vertical, 1 = Horizontal
3	CMN_PID_METALD_3	R	0h	Metal 3 direction : 0 = Vertical, 1 = Horizontal
2	CMN_PID_METALD_2	R	1h	Metal 2 direction : 0 = Vertical, 1 = Horizontal
1	CMN_PID_METALD_1	R	0h	Metal 1 direction : 0 = Vertical, 1 = Horizontal
0	CMN_PID_METALD_0	R	1h	Metal 0 direction : This layer does not have a direction associated with it.

Table 12-29. Register Call Summary for CMN_PID_METALD

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PID_METALD Register \(Offset = 28h\) \[reset = X\]: \[0\]](#)

12.10 CMN_SSM_BANDGAP_TMR_CMN_SSM_SM_CTRL Register (Offset = 40h) [reset = 00010003h]

CMN_SSM_BANDGAP_TMR_CMN_SSM_SM_CTRL is shown in Figure 12-10 and described in Table 12-31.

Return to [Summary Table](#).

Startup state machine control register

Table 12-30.
CMN_SSM_BANDGAP_TMR_CMN_SSM_SM_CTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 0040h

Figure 12-10. CMN_SSM_BANDGAP_TMR_CMN_SSM_SM_CTRL Register

31	30	29	28	27	26	25	24
CMN_SSM_BANDGAP_TMR_15_5							
R-0h							
23	22	21	20	19	18	17	16
CMN_SSM_BANDGAP_TMR_15_5				CMN_SSM_BANDGAP_TMR_4_0			
R-0h				R/W-1h			
15	14	13	12	11	10	9	8
CMN_SSM_SM_CTRL_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_SSM_SM_CTRL_7	CMN_SSM_SM_CTRL_6	CMN_SSM_SM_CTRL_5	CMN_SSM_SM_CTRL_4	CMN_SSM_SM_CTRL_3_2		CMN_SSM_SM_CTRL_1	CMN_SSM_SM_CTRL_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-31. CMN_SSM_BANDGAP_TMR_CMN_SSM_SM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	CMN_SSM_BANDGAP_TMR_15_5	R	0h	Reserved
20-16	CMN_SSM_BANDGAP_TMR_4_0	R/W	1h	Bandgap enable state timer value : Value used for the timer when the startup state machine is in the bandgap enable state. This timer delay is specified as the number of reference clocks to count. This value creates a delay of 40 nSec. Note, when exiting common suspend mode, a total of 1000 nSec is required for the bandgap to be enabled. This total delay is what is ultimately used to determine what the delay needs to be in the bandgap enable state. Of this total time, 960 nSec of this time is accounted for in the suspend recovery state. The remainder is accounted for here.
15-8	CMN_SSM_SM_CTRL_15_8	R	0h	Reserved
7	CMN_SSM_SM_CTRL_7	R/W	0h	Bandgap enable override enable : When active (1'b1), the bandgap enable override bit in this register will drive the ssmda_bandgap_en pin from the SSM directly.

Table 12-31. CMN_SSM_BANDGAP_TMR__CMN_SSM_SM_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CMN_SSM_SM_CTRL_6	R/W	0h	Bandgap enable override : When enabled by the bandgap enable override enable bit in this register, this bit will drive the ssmda_bandgap_en pin from the SSM directly. Note: The bandgap enable hold enable bit in the Startup state machine user defined control register on page 69 must also be set to 1'b0 in order for this register to function correctly.
5	CMN_SSM_SM_CTRL_5	R/W	0h	Bias enable override enable : When active (1'b1), the bias enable override bit in this register will drive the ssmda_bias_en pin from the SSM directly.
4	CMN_SSM_SM_CTRL_4	R/W	0h	Bias enable override : When enabled by the bias enable override enable bit in this register, this bit will drive the ssmda_bias_en pin from the SSM directly.
3-2	CMN_SSM_SM_CTRL_3_2	R	0h	Reserved
1	CMN_SSM_SM_CTRL_1	R/W	1h	Skip post bandgap enable re-calibration : When this bit is active (1'b1), the post bandgap enable calibration state will be skipped if it was previously run, unless the macro is disabled or reset.
0	CMN_SSM_SM_CTRL_0	R/W	1h	Skip auto re-calibration : When this bit is active (1'b1), the auto calibration state will be skipped if it was previously run, unless the macro is disabled or reset.

Table 12-32. Register Call Summary for CMN_SSM_BANDGAP_TMR__CMN_SSM_SM_CTRL

10-G SerDes Registers

- [CMN_SSM_BANDGAP_TMR__CMN_SSM_SM_CTRL Register \(Offset = 40h\) \[reset = 00010003h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.11 CMN_SSM_BIAS_TMR Register (Offset = 44h) [reset = X]

CMN_SSM_BIAS_TMR is shown in [Figure 12-11](#) and described in [Table 12-34](#).

Return to [Summary Table](#).

Bias enable timer register

Table 12-33. CMN_SSM_BIAS_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0044h

Figure 12-11. CMN_SSM_BIAS_TMR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMN_SSM_BIAS_TMR_15_7								CMN_SSM_BIAS_TMR_6_0							
R-0h								R/W-19h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-34. CMN_SSM_BIAS_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-7	CMN_SSM_BIAS_TMR_15_7	R	0h	Reserved
6-0	CMN_SSM_BIAS_TMR_6_0	R/W	19h	Bias enable state timer value : Value used for the timer when the startup state machine is in the bias enable state. This timer delay is specified as the number of reference clocks to count. This value creates a delay of 1 uSec.

Table 12-35. Register Call Summary for CMN_SSM_BIAS_TMR

10-G SerDes Registers

- [CMN_SSM_BIAS_TMR Register \(Offset = 44h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.12 CMN_SSM_USER_DEF_CTRL Register (Offset = 4Ch) [reset = X]

CMN_SSM_USER_DEF_CTRL is shown in [Figure 12-12](#) and described in [Table 12-37](#).

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Startup state machine user defined control register

Table 12-36. CMN_SSM_USER_DEF_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 004Ch

Figure 12-12. CMN_SSM_USER_DEF_CTRL Register

31	30	29	28	27	26	25	24
CMN_SSM_USER_DEF_CTRL_15_8							
R-0h							
23	22	21	20	19	18	17	16
CMN_SSM_USER_DEF_CTRL_7_2						CMN_SSM_US ER_DEF_CTRL _1	CMN_SSM_US ER_DEF_CTRL _0
R/W-0h						R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-37. CMN_SSM_USER_DEF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_SSM_USER_DEF_CTRL_15_8	R	0h	Reserved
23-18	CMN_SSM_USER_DEF_CTRL_7_2	R/W	0h	Reserved - spare
17	CMN_SSM_USER_DEF_CTRL_1	R/W	0h	Force SSM gated clock on: Setting this bit to 1'b1 will force the SSM gated clock on, independent of the internal SSM state machine clock gate controls.
16	CMN_SSM_USER_DEF_CTRL_0	R/W	1h	Bandgap enable hold enable: This bit enables the bandgap enable hold function, which holds the bandgap enable active in the common suspend state until the signal detect function is switched off.
15-0	RESERVED	R/W	X	

Table 12-38. Register Call Summary for CMN_SSM_USER_DEF_CTRL

10-G SerDes Registers

- [CMN_SSM_USER_DEF_CTRL Register \(Offset = 4Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.13 CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL Register (Offset = 50h) [reset = 00040001h]

CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL is shown in Figure 12-13 and described in Table 12-40.

Return to [Summary Table](#).

PLL 0 control state machine control register

Table 12-39. CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 0050h

Figure 12-13. CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL Register

31	30	29	28	27	26	25	24
CMN_PLLSM0_PLEN_TMR_15_4							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLLSM0_PLEN_TMR_15_4				CMN_PLLSM0_PLEN_TMR_3_0			
R-0h				R/W-4h			
15	14	13	12	11	10	9	8
CMN_PLLSM0_SM_CTRL_15_10						CMN_PLLSM0_SM_CTRL_9	CMN_PLLSM0_SM_CTRL_8
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CMN_PLLSM0_SM_CTRL_7	CMN_PLLSM0_SM_CTRL_6	CMN_PLLSM0_SM_CTRL_5	CMN_PLLSM0_SM_CTRL_4	CMN_PLLSM0_SM_CTRL_3_1			CMN_PLLSM0_SM_CTRL_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-40. CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	CMN_PLLSM0_PLEN_TMR_15_4	R	0h	Reserved
19-16	CMN_PLLSM0_PLEN_TMR_3_0	R/W	4h	PLL enable state timer value : Value used for the timer when the startup state machine is in the PLL enable state. This timer delay is specified as the number of reference clocks to count.
15-10	CMN_PLLSM0_SM_CTRL_15_10	R	0h	Reserved
9	CMN_PLLSM0_SM_CTRL_9	R/W	0h	PLL enable override enable : When active (1'b1), the PLL enable override bit in this register will drive the pllsmda_pll_en pin from the PLLSM directly.
8	CMN_PLLSM0_SM_CTRL_8	R/W	0h	PLL enable override : When enabled by the PLL enable override enable bit in this register, this bit will drive the pllsmda_pll_en pin from the PLLSM directly.
7	CMN_PLLSM0_SM_CTRL_7	R/W	0h	PLL reset override enable : When active (1'b1), the PLL reset override bit in this register will drive the pllsmda_pll_rst_n pin from the PLLSM directly.
6	CMN_PLLSM0_SM_CTRL_6	R/W	0h	PLL reset override : When enabled by the PLL reset override enable bit in this register, this bit will drive the pllsmda_pll_rst_n pin from the PLLSM directly.

**Table 12-40. CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
5	CMN_PLLSM0_SM_CTRL_5	R/W	0h	PLL pre charge override enable : When active (1'b1), the PLL pre charge override bit in this register will drive the pllsmda_pll_pre_charge pin from the PLLSM directly.
4	CMN_PLLSM0_SM_CTRL_4	R/W	0h	PLL pre charge override : When enabled by the PLL pre charge override enable bit in this register, this bit will drive the pllsmda_pll_pre_charge pin from the PLLSM directly.
3-1	CMN_PLLSM0_SM_CTRL_3_1	R	0h	Reserved
0	CMN_PLLSM0_SM_CTRL_0	R/W	1h	Skip PLL re-calibration : When this bit is active (1'b1), the PLL calibration state will be skipped if it was previously run, unless the PLL is disabled or resetting the state machine.

Table 12-41. Register Call Summary for CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL

10-G SerDes Registers

- [CMN_PLLSM0_PLEN_TMR__CMN_PLLSM0_SM_CTRL Register \(Offset = 50h\) \[reset = 00040001h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.14 CMN_PLLSM0_PLLVREF_TMR__CMN_PLLSM0_PLLPRE_TMR Register (Offset = 54h) [reset = 00010032h]

CMN_PLLSM0_PLLVREF_TMR__CMN_PLLSM0_PLLPRE_TMR is shown in Figure 12-14 and described in Table 12-43.

Return to [Summary Table](#).

PLL 0 pre-charge timer register

Table 12-42. CMN_PLLSM0_PLLVREF_TMR__CMN_PLLSM0_PLLPRE_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0054h

Figure 12-14. CMN_PLLSM0_PLLVREF_TMR__CMN_PLLSM0_PLLPRE_TMR Register

31	30	29	28	27	26	25	24
CMN_PLLSM0_PLLVREF_TMR_15_4							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLLSM0_PLLVREF_TMR_15_4				CMN_PLLSM0_PLLVREF_TMR_3_0			
R-0h				R/W-1h			
15	14	13	12	11	10	9	8
CMN_PLLSM0_PLLPRE_TMR_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLLSM0_PLLPRE_TMR_7_0							
R/W-32h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-43. CMN_PLLSM0_PLLVREF_TMR__CMN_PLLSM0_PLLPRE_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	CMN_PLLSM0_PLLVREF_TMR_15_4	R	0h	Reserved
19-16	CMN_PLLSM0_PLLVREF_TMR_3_0	R/W	1h	PLL VREF delay state timer value : Value used for the timer when the startup state machine is in the PLL VREF delay state. This timer delay is specified as the number of reference clocks to count.
15-8	CMN_PLLSM0_PLLPRE_TMR_15_8	R	0h	Reserved
7-0	CMN_PLLSM0_PLLPRE_TMR_7_0	R/W	32h	PLL pre-charge state timer value : Value used for the timer when the startup state machine is in the PLL pre-charge state. This timer delay is specified as the number of reference clocks to count. This value creates a delay of 2 uSec.

Table 12-44. Register Call Summary for CMN_PLLSM0_PLLVREF_TMR__CMN_PLLSM0_PLLPRE_TMR

10-G SerDes Registers

- [CMN_PLLSM0_PLLVREF_TMR__CMN_PLLSM0_PLLPRE_TMR Register \(Offset = 54h\) \[reset = 00010032h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.15 CMN_PLLSM0_PLLCLKDIS_TMR_CMN_PLLSM0_PLLLOCK_TMR Register (Offset = 58h) [reset = 000100D1h]

CMN_PLLSM0_PLLCLKDIS_TMR_CMN_PLLSM0_PLLLOCK_TMR is shown in Figure 12-15 and described in Table 12-46.

Return to [Summary Table](#).

PLL 0 lock delay timer register

Table 12-45.
CMN_PLLSM0_PLLCLKDIS_TMR_CMN_PLLSM0_PLLLOCK_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0058h

Figure 12-15. CMN_PLLSM0_PLLCLKDIS_TMR_CMN_PLLSM0_PLLLOCK_TMR Register

31	30	29	28	27	26	25	24
CMN_PLLSM0_PLLCLKDIS_TMR_15_2							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLLSM0_PLLCLKDIS_TMR_15_2						CMN_PLLSM0_PLLCLKDIS_TM R_1_0	
R-0h						R/W-1h	
15	14	13	12	11	10	9	8
CMN_PLLSM0_PLLLOCK_TMR_15_10						CMN_PLLSM0_PLLLOCK_TMR_ 9_0	
R-0h						R/W-D1h	
7	6	5	4	3	2	1	0
CMN_PLLSM0_PLLLOCK_TMR_9_0							
R/W-D1h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-46. CMN_PLLSM0_PLLCLKDIS_TMR_CMN_PLLSM0_PLLLOCK_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	CMN_PLLSM0_PLLCLKDIS_TMR_15_2	R	0h	Reserved
17-16	CMN_PLLSM0_PLLCLKDIS_TMR_1_0	R/W	1h	PLL clock disable delay state timer value : Value used for the timer when the startup state machine is in the PLL clock disable delay state. This timer delay is specified as the number of reference clocks to count.
15-10	CMN_PLLSM0_PLLLOCK_TMR_15_10	R	0h	Reserved
9-0	CMN_PLLSM0_PLLLOCK_TMR_9_0	R/W	D1h	PLL lock delay state timer value : Value used for the timer when the startup state machine is in the PLL lock delay state. This timer delay is specified as the number of reference clocks to count. This value creates a delay of 8.36 uSec.

**Table 12-47. Register Call Summary for
CMN_PLLSM0_PLLCLKDIS_TMR__CMN_PLLSM0_PLLLOCK_TMR**

10-G SerDes Registers

- [CMN_PLLSM0_PLLCLKDIS_TMR__CMN_PLLSM0_PLLLOCK_TMR Register \(Offset = 58h\) \[reset = 000100D1h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.16 CMN_PLLSM0_USER_DEF_CTRL Register (Offset = 5Ch) [reset = X]

CMN_PLLSM0_USER_DEF_CTRL is shown in [Figure 12-16](#) and described in [Table 12-49](#).

Return to [Summary Table](#).

PLL 0 control state machine user defined control register

Table 12-48. CMN_PLLSM0_USER_DEF_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 005Ch

Figure 12-16. CMN_PLLSM0_USER_DEF_CTRL Register

31	30	29	28	27	26	25	24
CMN_PLLSM0_USER_DEF_CTRL_15_8							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLLSM0_USER_DEF_CTRL_7_1							CMN_PLLSM0_USER_DEF_CTRL_0
R/W-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-49. CMN_PLLSM0_USER_DEF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PLLSM0_USER_DEF_CTRL_15_8	R	0h	Reserved
23-17	CMN_PLLSM0_USER_DEF_CTRL_7_1	R/W	0h	Reserved - spare
16	CMN_PLLSM0_USER_DEF_CTRL_0	R/W	0h	PLL lock override: When active (1'b1), this bit will force the PLL lock indication active.
15-0	RESERVED	R/W	X	

Table 12-50. Register Call Summary for CMN_PLLSM0_USER_DEF_CTRL

10-G SerDes Registers

- [CMN_PLLSM0_USER_DEF_CTRL Register \(Offset = 5Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.17 CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL Register (Offset = 60h) [reset = 00040001h]

CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL is shown in Figure 12-17 and described in Table 12-52.

Return to [Summary Table](#).

PLL 1 control state machine control register

Table 12-51. CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 0060h

Figure 12-17. CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL Register

31	30	29	28	27	26	25	24
CMN_PLLSM1_PLEN_TMR_15_4							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLLSM1_PLEN_TMR_15_4				CMN_PLLSM1_PLEN_TMR_3_0			
R-0h				R/W-4h			
15	14	13	12	11	10	9	8
CMN_PLLSM1_SM_CTRL_15_10						CMN_PLLSM1_SM_CTRL_9	CMN_PLLSM1_SM_CTRL_8
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CMN_PLLSM1_SM_CTRL_7	CMN_PLLSM1_SM_CTRL_6	CMN_PLLSM1_SM_CTRL_5	CMN_PLLSM1_SM_CTRL_4	CMN_PLLSM1_SM_CTRL_3_1			CMN_PLLSM1_SM_CTRL_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-52. CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	CMN_PLLSM1_PLEN_TMR_15_4	R	0h	Reserved
19-16	CMN_PLLSM1_PLEN_TMR_3_0	R/W	4h	PLL enable state timer value : Value used for the timer when the startup state machine is in the PLL enable state. This timer delay is specified as the number of reference clocks to count.
15-10	CMN_PLLSM1_SM_CTRL_15_10	R	0h	Reserved
9	CMN_PLLSM1_SM_CTRL_9	R/W	0h	PLL enable override enable : When active (1'b1), the PLL enable override bit in this register will drive the pllsmda_pll_en pin from the PLLSM directly.
8	CMN_PLLSM1_SM_CTRL_8	R/W	0h	PLL enable override : When enabled by the PLL enable override enable bit in this register, this bit will drive the pllsmda_pll_en pin from the PLLSM directly.
7	CMN_PLLSM1_SM_CTRL_7	R/W	0h	PLL reset override enable : When active (1'b1), the PLL reset override bit in this register will drive the pllsmda_pll_rst_n pin from the PLLSM directly.
6	CMN_PLLSM1_SM_CTRL_6	R/W	0h	PLL reset override : When enabled by the PLL reset override enable bit in this register, this bit will drive the pllsmda_pll_rst_n pin from the PLLSM directly.

**Table 12-52. CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
5	CMN_PLLSM1_SM_CTRL_5	R/W	0h	PLL pre charge override enable : When active (1'b1), the PLL pre charge override bit in this register will drive the pllsmda_pll_pre_charge pin from the PLLSM directly.
4	CMN_PLLSM1_SM_CTRL_4	R/W	0h	PLL pre charge override : When enabled by the PLL pre charge override enable bit in this register, this bit will drive the pllsmda_pll_pre_charge pin from the PLLSM directly.
3-1	CMN_PLLSM1_SM_CTRL_3_1	R	0h	Reserved
0	CMN_PLLSM1_SM_CTRL_0	R/W	1h	Skip PLL re-calibration : When this bit is active (1'b1), the PLL calibration state will be skipped if it was previously run, unless the PLL is disabled or resetting the state machine.

Table 12-53. Register Call Summary for CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL

10-G SerDes Registers

- [CMN_PLLSM1_PLEN_TMR__CMN_PLLSM1_SM_CTRL Register \(Offset = 60h\) \[reset = 00040001h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.18 CMN_PLLSM1_PLLVREF_TMR__CMN_PLLSM1_PLLPRE_TMR Register (Offset = 64h) [reset = 00010032h]

CMN_PLLSM1_PLLVREF_TMR__CMN_PLLSM1_PLLPRE_TMR is shown in Figure 12-18 and described in Table 12-55.

Return to [Summary Table](#).

PLL 1 pre-charge timer register

Table 12-54. CMN_PLLSM1_PLLVREF_TMR__CMN_PLLSM1_PLLPRE_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0064h

Figure 12-18. CMN_PLLSM1_PLLVREF_TMR__CMN_PLLSM1_PLLPRE_TMR Register

31	30	29	28	27	26	25	24
CMN_PLLSM1_PLLVREF_TMR_15_4							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLLSM1_PLLVREF_TMR_15_4				CMN_PLLSM1_PLLVREF_TMR_3_0			
R-0h				R/W-1h			
15	14	13	12	11	10	9	8
CMN_PLLSM1_PLLPRE_TMR_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLLSM1_PLLPRE_TMR_7_0							
R/W-32h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-55. CMN_PLLSM1_PLLVREF_TMR__CMN_PLLSM1_PLLPRE_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	CMN_PLLSM1_PLLVREF_TMR_15_4	R	0h	Reserved
19-16	CMN_PLLSM1_PLLVREF_TMR_3_0	R/W	1h	PLL VREF delay state timer value : Value used for the timer when the startup state machine is in the PLL VREF delay state. This timer delay is specified as the number of reference clocks to count.
15-8	CMN_PLLSM1_PLLPRE_TMR_15_8	R	0h	Reserved
7-0	CMN_PLLSM1_PLLPRE_TMR_7_0	R/W	32h	PLL pre-charge state timer value : Value used for the timer when the startup state machine is in the PLL pre-charge state. This timer delay is specified as the number of reference clocks to count. This value creates a delay of 2 uSec.

Table 12-56. Register Call Summary for CMN_PLLSM1_PLLVREF_TMR__CMN_PLLSM1_PLLPRE_TMR

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLLSM1_PLLVREF_TMR__CMN_PLLSM1_PLLPRE_TMR Register \(Offset = 64h\) \[reset = 00010032h\]: \[0\]](#)

12.19 CMN_PLLSM1_PLLCLKDIS_TMR_CMN_PLLSM1_PLLLOCK_TMR Register (Offset = 68h) [reset = 000100D1h]

CMN_PLLSM1_PLLCLKDIS_TMR_CMN_PLLSM1_PLLLOCK_TMR is shown in Figure 12-19 and described in Table 12-58.

Return to [Summary Table](#).

PLL 1 lock delay timer register

Table 12-57.
CMN_PLLSM1_PLLCLKDIS_TMR_CMN_PLLSM1_PLLLOCK_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0068h

Figure 12-19. CMN_PLLSM1_PLLCLKDIS_TMR_CMN_PLLSM1_PLLLOCK_TMR Register

31	30	29	28	27	26	25	24
CMN_PLLSM1_PLLCLKDIS_TMR_15_2							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLLSM1_PLLCLKDIS_TMR_15_2						CMN_PLLSM1_PLLCLKDIS_TMR_1_0	
R-0h						R/W-1h	
15	14	13	12	11	10	9	8
CMN_PLLSM1_PLLLOCK_TMR_15_10						CMN_PLLSM1_PLLLOCK_TMR_9_0	
R-0h						R/W-D1h	
7	6	5	4	3	2	1	0
CMN_PLLSM1_PLLLOCK_TMR_9_0							
R/W-D1h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-58. CMN_PLLSM1_PLLCLKDIS_TMR_CMN_PLLSM1_PLLLOCK_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	CMN_PLLSM1_PLLCLKDIS_TMR_15_2	R	0h	Reserved
17-16	CMN_PLLSM1_PLLCLKDIS_TMR_1_0	R/W	1h	PLL clock disable delay state timer value : Value used for the timer when the startup state machine is in the PLL clock disable delay state. This timer delay is specified as the number of reference clocks to count.
15-10	CMN_PLLSM1_PLLLOCK_TMR_15_10	R	0h	Reserved
9-0	CMN_PLLSM1_PLLLOCK_TMR_9_0	R/W	D1h	PLL lock delay state timer value : Value used for the timer when the startup state machine is in the PLL lock delay state. This timer delay is specified as the number of reference clocks to count. This value creates a delay of 8.36 uSec.

Table 12-59. Register Call Summary for
CMN_PLLSM1_PLLCLKDIS_TMR__CMN_PLLSM1_PLLLOCK_TMR

10-G SerDes Registers <ul style="list-style-type: none"> CMN_PLLSM1_PLLCLKDIS_TMR__CMN_PLLSM1_PLLLOCK_TMR Register (Offset = 68h) [reset = 000100D1h]: [0] 10-G SerDes Registers: [0]

12.20 CMN_PLLSM1_USER_DEF_CTRL Register (Offset = 6Ch) [reset = X]

CMN_PLLSM1_USER_DEF_CTRL is shown in [Figure 12-20](#) and described in [Table 12-61](#).

Return to [Summary Table](#).

PLL 1 control state machine user defined control register

Table 12-60. CMN_PLLSM1_USER_DEF_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 006Ch

Figure 12-20. CMN_PLLSM1_USER_DEF_CTRL Register

31	30	29	28	27	26	25	24
CMN_PLLSM1_USER_DEF_CTRL_15_8							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLLSM1_USER_DEF_CTRL_7_1							CMN_PLLSM1_USER_DEF_CTRL_0
R/W-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-61. CMN_PLLSM1_USER_DEF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PLLSM1_USER_DEF_CTRL_15_8	R	0h	Reserved
23-17	CMN_PLLSM1_USER_DEF_CTRL_7_1	R/W	0h	Reserved - spare
16	CMN_PLLSM1_USER_DEF_CTRL_0	R/W	0h	PLL lock override: When active (1'b1), this bit will force the PLL lock indication active.
15-0	RESERVED	R/W	X	

Table 12-62. Register Call Summary for CMN_PLLSM1_USER_DEF_CTRL

10-G SerDes Registers

- [CMN_PLLSM1_USER_DEF_CTRL Register \(Offset = 6Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.21 CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR Register (Offset = 80h) [reset = 01240101h]

CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR is shown in Figure 12-21 and described in Table 12-64.

Return to [Summary Table](#).

Common power island control timer register

Table 12-63. CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0080h

Figure 12-21. CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR Register

31	30	29	28	27	26	25	24
CMN_CDIAG_CDB_PWRI_OVRD_15	CMN_CDIAG_CDB_PWRI_OVRD_14	CMN_CDIAG_CDB_PWRI_OVRD_13_12		CMN_CDIAG_CDB_PWRI_OVRD_11	CMN_CDIAG_CDB_PWRI_OVRD_10	CMN_CDIAG_CDB_PWRI_OVRD_9	CMN_CDIAG_CDB_PWRI_OVRD_8
R/W-0h	R/W-0h	R-0h		R/W-0h	R-0h	R/W-0h	R-1h
23	22	21	20	19	18	17	16
CMN_CDIAG_CDB_PWRI_OVRD_7_0							
R/W-24h							
15	14	13	12	11	10	9	8
CMN_CDIAG_PWRI_TMR_15_11					CMN_CDIAG_PWRI_TMR_10_8		
R-0h					R/W-1h		
7	6	5	4	3	2	1	0
CMN_CDIAG_PWRI_TMR_7_3					CMN_CDIAG_PWRI_TMR_2_0		
R-0h					R/W-1h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-64. CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_CDIAG_CDB_PWRI_OVRD_15	R/W	0h	Power island controller input override enable: When enabled, the power island control state machine input override bits in this register will drive the power island control state machine directly, and override any control from other state machines in the macro. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 0: Override disabled 1: Override enabled
30	CMN_CDIAG_CDB_PWRI_OVRD_14	R/W	0h	Power island controller output override enable: When enabled, the power island control state machine output override bits in this register will drive the power island control state machine outputs, and override any control from power island control state machine. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 0: Override disabled 1: Override enabled
29-28	CMN_CDIAG_CDB_PWRI_OVRD_13_12	R	0h	Reserved

**Table 12-64. CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
27	CMN_CDIAG_CDB_PWRI_OVRD_11	R/W	0h	Power suspend request override: When enabled, this bit will override the power_suspend_req input of the power island control state machine. Note that, whenever changing the state of this bit, no other CDB register access should be initiated for 1 uSec, to keep the CDB clock off while the power island state change transition is in progress.
26	CMN_CDIAG_CDB_PWRI_OVRD_10	R	0h	Power suspend acknowledge: This is the current state of the power_suspend_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
25	CMN_CDIAG_CDB_PWRI_OVRD_9	R/W	0h	Power recover request override: When enabled, this bit will override the power_recover_req input of the power island control state machine. Note that, whenever changing the state of this bit, no other CDB register access should be initiated for 1 uSec, to keep the CDB clock off while the power island state change transition is in progress.
24	CMN_CDIAG_CDB_PWRI_OVRD_8	R	1h	Power recover acknowledge: This is the current state of the power_recover_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
23-16	CMN_CDIAG_CDB_PWRI_OVRD_7_0	R/W	24h	Power island controller output override: When enabled, the bits in this field will override the output signals from the power island control state machine. The following are the power island control state machine output signals, and the bits in this field that they are associated with. Bit 7: state_sandh Bit 6: state_ret_save Bit 5: state_ret_restore (active low) Bit 4: power_en_ph_1 Bit 3: power_en_ph_2 Bit 2: power_isolation Bit 1: power_por_reset_n Bit 0: power_rstr_reset_n The default value of the bits in this register are such that the power island is not forced to be switched on when the power island controller output override enable bit in this register is enabled. When using this register to switch this power island on and off, the bits in this field are required to change in a specific order with individual register writes. The writes must happen in the order specified below. 8'b00100100 : Power island is not being forced on 8'b10100100
15-11	CMN_CDIAG_PWRI_TMR_15_11	R	0h	Reserved

**Table 12-64. CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
10-8	CMN_CDIAG_PWRI_TMR_10_8	R/W	1h	Power enable phase 2 timer value: This specifies the number of reference clock cycles the power island control state machines in common will wait in the power phase 2 enable states, in order to allow enough time for the second phase of the switched domain to power up, before deactivating the isolation functions. The default value of this register corresponds to a delay of 40 nSec. Note that a value of 0 in this field is not valid, and will result in a delay of 1 clock cycle.
7-3	CMN_CDIAG_PWRI_TMR_7_3	R	0h	Reserved
2-0	CMN_CDIAG_PWRI_TMR_2_0	R/W	1h	Power enable phase 1 timer value: This specifies the number of reference clock cycles the power island control state machines in common will wait in the power phase 1 enable states, in order to allow enough time for the first phase of the switched domain to power up, before enabling the second phase of the power up. The default value of this register corresponds to a delay of 40 nSec. Note that a value of 0 in this field is not valid, and will result in a delay of 1 clock cycle.

Table 12-65. Register Call Summary for CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR

10-G SerDes Registers

- [CMN_CDIAG_CDB_PWRI_OVRD__CMN_CDIAG_PWRI_TMR Register \(Offset = 80h\) \[reset = 01240101h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.22 CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT Register (Offset = 84h) [reset = 0424003Bh]

CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT is shown in Figure 12-22 and described in Table 12-67.

Return to [Summary Table](#).

Common CDB power island control status register

Table 12-66.
CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT Instances

Instance	Physical Address
SERDES_10G0	0505 0084h

Figure 12-22. CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT Register

31	30	29	28	27	26	25	24
CMN_CDIAG_P LLC_PWRI_OV RD_15	CMN_CDIAG_P LLC_PWRI_OV RD_14	CMN_CDIAG_PLLC_PWRI_OVR D_13_12		CMN_CDIAG_P LLC_PWRI_OV RD_11	CMN_CDIAG_P LLC_PWRI_OV RD_10	CMN_CDIAG_P LLC_PWRI_OV RD_9	CMN_CDIAG_P LLC_PWRI_OV RD_8
R/W-0h	R/W-0h	R-0h		R/W-0h	R-1h	R/W-0h	R-0h
23	22	21	20	19	18	17	16
CMN_CDIAG_PLLC_PWRI_OVRD_7_0							
R/W-24h							
15	14	13	12	11	10	9	8
CMN_CDIAG_CDB_PWRI_STAT_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_CDIAG_CDB_PWRI_STAT_7_0							
R-3Bh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-67. CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_CDIAG_PLLC_PWRI_OVRD_15	R/W	0h	Power island controller input override enable: When enabled, the power island control state machine input override bits in this register will drive the power island control state machine directly, and override any control from other state machines in the macro. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 0: Override disabled 1: Override enabled
30	CMN_CDIAG_PLLC_PWRI_OVRD_14	R/W	0h	Power island controller output override enable: When enabled, the power island control state machine output override bits in this register will drive the power island control state machine outputs, and override any control from power island control state machine. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 0: Override disabled 1: Override enabled
29-28	CMN_CDIAG_PLLC_PWRI_OVRD_13_12	R	0h	Reserved

Table 12-67. CMN_CDIAG_PLLC_PWRI_OVRD_CMN_CDIAG_CDB_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMN_CDIAG_PLLC_PWRI_OVRD_11	R/W	0h	Power suspend request override: When enabled, this bit will override the power_suspend_req input of the power island control state machine.
26	CMN_CDIAG_PLLC_PWRI_OVRD_10	R	1h	Power suspend acknowledge: This is the current state of the power_suspend_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
25	CMN_CDIAG_PLLC_PWRI_OVRD_9	R/W	0h	Power recover request override: When enabled, this bit will override the power_recover_req input of the power island control state machine.
24	CMN_CDIAG_PLLC_PWRI_OVRD_8	R	0h	Power recover acknowledge: This is the current state of the power_recover_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
23-16	CMN_CDIAG_PLLC_PWRI_OVRD_7_0	R/W	24h	Power island controller output override: When enabled, the bits in this field will override the output signals from the power island control state machine. The following are the power island control state machine output signals, and the bits in this field that they are associated with. Bit 7: state_sandh Bit 6: state_ret_save Bit 5: state_ret_restore (active low) Bit 4: power_en_ph_1 Bit 3: power_en_ph_2 Bit 2: power_isolation Bit 1: power_por_reset_n Bit 0: power_rstr_reset_n The default value of the bits in this register are such that the power island is not forced to be switched on when the power island controller output override enable bit in this register is enabled. When using this register to switch this power island on and off, the bits in this field are required to change in a specific order with individual register writes. The writes must happen in the order specified below. 8'b 00100100 : Power island is not being forced on 8'b10100100
15-8	CMN_CDIAG_CDB_PWRI_STAT_15_8	R	0h	Reserved

Table 12-67. CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CMN_CDIAG_CDB_PWRI_STAT_7_0	R	3Bh	<p>Power island controller output status: This field indicates the current state of the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p>

Table 12-68. Register Call Summary for CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_CDIAG_PLLC_PWRI_OVRD__CMN_CDIAG_CDB_PWRI_STAT Register \(Offset = 84h\) \[reset = 0424003Bh\]: \[0\]](#)

12.23 CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT Register (Offset = 88h) [reset = 04240024h]

CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT is shown in Figure 12-23 and described in Table 12-70.

Return to [Summary Table](#).

Common PLL controller power island control status register

Table 12-69.
CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT
Instances

Instance	Physical Address
SERDES_10G0	0505 0088h

Figure 12-23. CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT Register

31	30	29	28	27	26	25	24
CMN_CDIAG_CCAL_PWRI_OVRD_15	CMN_CDIAG_CCAL_PWRI_OVRD_14	CMN_CDIAG_CCAL_PWRI_OVRD_13_12	CMN_CDIAG_CCAL_PWRI_OVRD_11	CMN_CDIAG_CCAL_PWRI_OVRD_10	CMN_CDIAG_CCAL_PWRI_OVRD_9	CMN_CDIAG_CCAL_PWRI_OVRD_8	
R/W-0h	R/W-0h	R-0h	R/W-0h	R-1h	R/W-0h	R-0h	
23	22	21	20	19	18	17	16
CMN_CDIAG_CCAL_PWRI_OVRD_7_0							
R/W-24h							
15	14	13	12	11	10	9	8
CMN_CDIAG_PLLC_PWRI_STAT_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_CDIAG_PLLC_PWRI_STAT_7_0							
R-24h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-70. CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_CDIAG_CCAL_PWRI_OVRD_15	R/W	0h	Power island controller input override enable: When enabled, the power island control state machine input override bits in this register will drive the power island control state machine directly, and override any control from other state machines in the macro. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 1'b 0: Override disabled 1'b 1: Override enabled
30	CMN_CDIAG_CCAL_PWRI_OVRD_14	R/W	0h	Power island controller output override enable: When enabled, the power island control state machine output override bits in this register will drive the power island control state machine outputs, and override any control from power island control state machine. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 1'b 0: Override disabled 1'b 1: Override enabled
29-28	CMN_CDIAG_CCAL_PWRI_OVRD_13_12	R	0h	Reserved

Table 12-70. CMN_CDIAG_CCAL_PWRI_OVRD_CMN_CDIAG_PLLC_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMN_CDIAG_CCAL_PWRI_OVRD_11	R/W	0h	Power suspend request override: When enabled, this bit will override the power_suspend_req input of the power island control state machine.
26	CMN_CDIAG_CCAL_PWRI_OVRD_10	R	1h	Power suspend acknowledge: This is the current state of the power_suspend_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
25	CMN_CDIAG_CCAL_PWRI_OVRD_9	R/W	0h	Power recover request override: When enabled, this bit will override the power_recover_req input of the power island control state machine.
24	CMN_CDIAG_CCAL_PWRI_OVRD_8	R	0h	Power recover acknowledge: This is the current state of the power_recover_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
23-16	CMN_CDIAG_CCAL_PWRI_OVRD_7_0	R/W	24h	Power island controller output override: When enabled, the bits in this field will override the output signals from the power island control state machine. The following are the power island control state machine output signals, and the bits in this field that they are associated with. Bit 7: state_sandh Bit 6: state_ret_save Bit 5: state_ret_restore (active low) Bit 4: power_en_ph_1 Bit 3: power_en_ph_2 Bit 2: power_isolation Bit 1: power_por_reset_n Bit 0: power_rstr_reset_n The default value of the bits in this register are such that the power island is not forced to be switched on when the power island controller output override enable bit in this register is enabled. When using this register to switch this power island on and off, the bits in this field are required to change in a specific order with individual register writes. The writes must happen in the order specified below. 8'b 00100100 : Power island is not being forced on 8'b10100100
15-8	CMN_CDIAG_PLLC_PWRI_STAT_15_8	R	0h	Reserved

Table 12-70. CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CMN_CDIAG_PLLC_PWRI_STAT_7_0	R	24h	<p>Power island controller output status: This field indicates the current state of the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p>

Table 12-71. Register Call Summary for CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_CDIAG_CCAL_PWRI_OVRD__CMN_CDIAG_PLLC_PWRI_STAT Register \(Offset = 88h\) \[reset = 04240024h\]: \[0\]](#)

12.24 CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT Register (Offset = 8Ch) [reset = 04240024h]

CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT is shown in Figure 12-24 and described in Table 12-73.

Return to [Summary Table](#).

Common common calibration power island control status register

Table 12-72.
CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT
Instances

Instance	Physical Address
SERDES_10G0	0505 008Ch

Figure 12-24. CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT Register

31	30	29	28	27	26	25	24
CMN_CDIAG_XCVRC_PWRI_OVRD_15	CMN_CDIAG_XCVRC_PWRI_OVRD_14	CMN_CDIAG_XCVRC_PWRI_OVRD_13_12	CMN_CDIAG_XCVRC_PWRI_OVRD_11	CMN_CDIAG_XCVRC_PWRI_OVRD_10	CMN_CDIAG_XCVRC_PWRI_OVRD_9	CMN_CDIAG_XCVRC_PWRI_OVRD_8	
R/W-0h	R/W-0h	R-0h	R/W-0h	R-1h	R/W-0h	R-0h	
23	22	21	20	19	18	17	16
CMN_CDIAG_XCVRC_PWRI_OVRD_7_0							
R/W-24h							
15	14	13	12	11	10	9	8
CMN_CDIAG_CCAL_PWRI_STAT_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_CDIAG_CCAL_PWRI_STAT_7_0							
R-24h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-73. CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_CDIAG_XCVRC_PWRI_OVRD_15	R/W	0h	Power island controller input override enable: When enabled, the power island control state machine input override bits in this register will drive the power island control state machine directly, and override any control from other state machines in the macro. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 1'b 0: Override disabled 1'b 1: Override enabled
30	CMN_CDIAG_XCVRC_PWRI_OVRD_14	R/W	0h	Power island controller output override enable: When enabled, the power island control state machine output override bits in this register will drive the power island control state machine outputs, and override any control from power island control state machine. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 1'b 0: Override disabled 1'b 1: Override enabled
29-28	CMN_CDIAG_XCVRC_PWRI_OVRD_13_12	R	0h	Reserved

Table 12-73. CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMN_CDIAG_XCVRC_PWRI_OVRD_11	R/W	0h	Power suspend request override: When enabled, this bit will override the power_suspend_req input of the power island control state machine.
26	CMN_CDIAG_XCVRC_PWRI_OVRD_10	R	1h	Power suspend acknowledge: This is the current state of the power_suspend_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
25	CMN_CDIAG_XCVRC_PWRI_OVRD_9	R/W	0h	Power recover request override: When enabled, this bit will override the power_recover_req input of the power island control state machine.
24	CMN_CDIAG_XCVRC_PWRI_OVRD_8	R	0h	Power recover acknowledge: This is the current state of the power_recover_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
23-16	CMN_CDIAG_XCVRC_PWRI_OVRD_7_0	R/W	24h	Power island controller output override: When enabled, the bits in this field will override the output signals from the power island control state machine. The following are the power island control state machine output signals, and the bits in this field that they are associated with. Bit 7: state_sandh Bit 6: state_ret_save Bit 5: state_ret_restore (active low) Bit 4: power_en_ph_1 Bit 3: power_en_ph_2 Bit 2: power_isolation Bit 1: power_por_reset_n Bit 0: power_rstr_reset_n The default value of the bits in this register are such that the power island is not forced to be switched on when the power island controller output override enable bit in this register is enabled. When using this register to switch this power island on and off, the bits in this field are required to change in a specific order with individual register writes. The writes must happen in the order specified below. 8'b 00100100 : Power island is not being forced on 8'b1010010
15-8	CMN_CDIAG_CCAL_PWRI_STAT_15_8	R	0h	Reserved

Table 12-73. CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CMN_CDIAG_CCAL_PWRI_STAT_7_0	R	24h	<p>Power island controller output status: This field indicates the current state of the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p>

Table 12-74. Register Call Summary for CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT

10-G SerDes Registers

- [CMN_CDIAG_XCVRC_PWRI_OVRD__CMN_CDIAG_CCAL_PWRI_STAT Register \(Offset = 8Ch\) \[reset = 04240024h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.25 CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT Register (Offset = 90h) [reset = 04240024h]

CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT is shown in Figure 12-25 and described in Table 12-76.

Return to [Summary Table](#).

Common transceiver controller power island control status register

Table 12-75.
CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT
Instances

Instance	Physical Address
SERDES_10G0	0505 0090h

Figure 12-25. CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT Register

31	30	29	28	27	26	25	24
CMN_CDIAG_DIAG_PWRI_OVRD_15	CMN_CDIAG_DIAG_PWRI_OVRD_14	CMN_CDIAG_DIAG_PWRI_OVRD_13_12		CMN_CDIAG_DIAG_PWRI_OVRD_11	CMN_CDIAG_DIAG_PWRI_OVRD_10	CMN_CDIAG_DIAG_PWRI_OVRD_9	CMN_CDIAG_DIAG_PWRI_OVRD_8
R/W-0h	R/W-0h	R-0h		R/W-0h	R-1h	R/W-0h	R-0h
23	22	21	20	19	18	17	16
CMN_CDIAG_DIAG_PWRI_OVRD_7_0							
R/W-24h							
15	14	13	12	11	10	9	8
CMN_CDIAG_XCVRC_PWRI_STAT_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_CDIAG_XCVRC_PWRI_STAT_7_0							
R-24h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-76. CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_CDIAG_DIAG_PWRI_OVRD_15	R/W	0h	Power island controller input override enable: When enabled, the power island control state machine input override bits in this register will drive the power island control state machine directly, and override any control from other state machines in the macro. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 1'b 0: Override disabled 1'b 1: Override enabled
30	CMN_CDIAG_DIAG_PWRI_OVRD_14	R/W	0h	Power island controller output override enable: When enabled, the power island control state machine output override bits in this register will drive the power island control state machine outputs, and override any control from power island control state machine. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. 1'b 0: Override disabled 1'b 1: Override enabled
29-28	CMN_CDIAG_DIAG_PWRI_OVRD_13_12	R	0h	Reserved

Table 12-76. CMN_CDIAG_DIAG_PWRI_OVRD_CMN_CDIAG_XCVRC_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	CMN_CDIAG_DIAG_PWRI_OVRD_11	R/W	0h	Power suspend request override: When enabled, this bit will override the power_suspend_req input of the power island control state machine.
26	CMN_CDIAG_DIAG_PWRI_OVRD_10	R	1h	Power suspend acknowledge: This is the current state of the power_suspend_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
25	CMN_CDIAG_DIAG_PWRI_OVRD_9	R/W	0h	Power recover request override: When enabled, this bit will override the power_recover_req input of the power island control state machine.
24	CMN_CDIAG_DIAG_PWRI_OVRD_8	R	0h	Power recover acknowledge: This is the current state of the power_recover_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
23-16	CMN_CDIAG_DIAG_PWRI_OVRD_7_0	R/W	24h	Power island controller output override: When enabled, the bits in this field will override the output signals from the power island control state machine. The following are the power island control state machine output signals, and the bits in this field that they are associated with. Bit 7: state_sandh Bit 6: state_ret_save Bit 5: state_ret_restore (active low) Bit 4: power_en_ph_1 Bit 3: power_en_ph_2 Bit 2: power_isolation Bit 1: power_por_reset_n Bit 0: power_rstr_reset_n The default value of the bits in this register are such that the power island is not forced to be switched on when the power island controller output override enable bit in this register is enabled. When using this register to switch this power island on and off, the bits in this field are required to change in a specific order with individual register writes. The writes must happen in the order specified below. 8'b 00100100 : Power island is not being forced on 8'b10100100
15-8	CMN_CDIAG_XCVRC_PWRI_STAT_15_8	R	0h	Reserved

Table 12-76. CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CMN_CDIAG_XCVRC_PWRI_STAT_7_0	R	24h	<p>Power island controller output status: This field indicates the current state of the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p>

Table 12-77. Register Call Summary for CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT

10-G SerDes Registers

- [CMN_CDIAG_DIAG_PWRI_OVRD__CMN_CDIAG_XCVRC_PWRI_STAT Register \(Offset = 90h\) \[reset = 04240024h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.26 CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT Register (Offset = 94h) [reset = A4h]

CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT is shown in Figure 12-26 and described in Table 12-79.

Return to [Summary Table](#).

Common diagnostic power island control status register

Table 12-78.
CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT Instances

Instance	Physical Address
SERDES_10G0	0505 0094h

Figure 12-26. CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT Register

31	30	29	28	27	26	25	24
CMN_CDIAG_PRATECLK_CTRL_15_2							
R-0h							
23	22	21	20	19	18	17	16
CMN_CDIAG_PRATECLK_CTRL_15_2						CMN_CDIAG_P RATECLK_CTR L_1	CMN_CDIAG_P RATECLK_CTR L_0
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CMN_CDIAG_DIAG_PWRI_STAT_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_CDIAG_DIAG_PWRI_STAT_7_0							
R-A4h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-79. CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	CMN_CDIAG_PRATECLK_CTRL_15_2	R	0h	Reserved
17	CMN_CDIAG_PRATECLK_CTRL_1	R/W	0h	Common PLL 1 full rate and data rate source clock select: Selects the PLL source clock to use when generating the cmn_pll1_clk_fullrt, cmn_pll1_clk_datart0, and cmn_pll1_clk_datart1 clocks. 1'b 0 : cmnda_pll1_clk_0 1'b 1 : cmnda_pll1_clk_1
16	CMN_CDIAG_PRATECLK_CTRL_0	R/W	0h	Common PLL 0 full rate and data rate source clock select: Selects the PLL source clock to use when generating the cmn_pll0_clk_fullrt, cmn_pll0_clk_datart0, and cmn_pll0_clk_datart1 clocks. 1'b 0 : cmnda_pll0_clk_0 1'b 1 : cmnda_pll0_clk_1
15-8	CMN_CDIAG_DIAG_PWRI_STAT_15_8	R	0h	Reserved

Table 12-79. CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	CMN_CDIAG_DIAG_PWR I_STAT_7_0	R	A4h	<p>Power island controller output status: This field indicates the current state of the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p>

**Table 12-80. Register Call Summary for
CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT**

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_CDIAG_PRATECLK_CTRL__CMN_CDIAG_DIAG_PWRI_STAT Register \(Offset = 94h\) \[reset = A4h\]: \[0\]](#)

12.27 CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD Register (Offset = 98h) [reset = 108h]

CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD is shown in Figure 12-27 and described in Table 12-82.

Return to [Summary Table](#).

Reference clock receiver override register

Table 12-81. CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD Instances

Instance	Physical Address
SERDES_10G0	0505 0098h

Figure 12-27. CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD Register

31	30	29	28	27	26	25	24
CMN_CDIAG_REFCLK_TEST_15_10						CMN_CDIAG_REFCLK_TEST_9_8	
R-0h						R/W-0h	
23	22	21	20	19	18	17	16
CMN_CDIAG_REFCLK_TEST_7_6	CMN_CDIAG_REFCLK_TEST_5	CMN_CDIAG_REFCLK_TEST_4	CMN_CDIAG_REFCLK_TEST_3	CMN_CDIAG_REFCLK_TEST_2	CMN_CDIAG_REFCLK_TEST_1	CMN_CDIAG_REFCLK_TEST_0	
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R-0h	
15	14	13	12	11	10	9	8
CMN_CDIAG_REFCLK_OVRD_15_13			CMN_CDIAG_REFCLK_OVRD_12	CMN_CDIAG_REFCLK_OVRD_11_10		CMN_CDIAG_REFCLK_OVRD_9_8	
R-0h			R/W-0h	R-0h		R/W-1h	
7	6	5	4	3	2	1	0
CMN_CDIAG_REFCLK_OVRD_7	CMN_CDIAG_REFCLK_OVRD_6	CMN_CDIAG_REFCLK_OVRD_5	CMN_CDIAG_REFCLK_OVRD_4	CMN_CDIAG_REFCLK_OVRD_3_2		CMN_CDIAG_REFCLK_OVRD_1	CMN_CDIAG_REFCLK_OVRD_0
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-2h		R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-82. CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	CMN_CDIAG_REFCLK_TEST_15_10	R	0h	Reserved
25-24	CMN_CDIAG_REFCLK_TEST_9_8	R/W	0h	Reserved - spare
23-22	CMN_CDIAG_REFCLK_TEST_7_6	R	0h	Reserved
21	CMN_CDIAG_REFCLK_TEST_5	R/W	0h	Reference clock driver 0 test mode enable: Enables the reference clock driver DC test mode, by controlling the cmnda_ref_clk0_drv_test_en signal going into the analog.
20	CMN_CDIAG_REFCLK_TEST_4	R/W	0h	Reference clock driver 0 test mode value: When enabled by the reference clock driver 0 test mode enable bit in this register, the value in this bit will be driven by the reference clock driver, by controlling the cmnda_ref_clk0_drv_test_val signal going into the analog.
19	CMN_CDIAG_REFCLK_TEST_3	R	0h	Reserved

**Table 12-82. CMN_CDIAG_REFCLK_TEST_CMN_CDIAG_REFCLK_OVRD Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
18	CMN_CDIAG_REFCLK_TEST_2	R/W	0h	Reference clock receiver test mode enable: Enables the reference clock receiver DC test mode, by controlling the cmnda_ref_clk_rcv_test_en signal going into the analog.
17	CMN_CDIAG_REFCLK_TEST_1	R	0h	Reference clock receiver test mode PLL value: When enabled by the reference clock receiver test mode enable bit in this register, the value in this bit will be the value present on the PLL reference clock receiver. This bit is driven by the cmnda_ref_clk_rcv_test_pll_val signal driven from the analog.
16	CMN_CDIAG_REFCLK_TEST_0	R	0h	Reference clock receiver test mode digital value: When enabled by the reference clock receiver test mode enable bit in this register, the value in this bit will be the value present on the digital reference clock receiver. This bit is driven by the cmnda_ref_clk_rcv_test_dig_val signal driven from the analog.
15-13	CMN_CDIAG_REFCLK_OVRD_15_13	R	0h	Reserved
12	CMN_CDIAG_REFCLK_OVRD_12	R/W	0h	Derived reference clock source select: Selects which PLL is the source for the derived reference clock, by driving the cmnda_ref_clk_der_src_sel signal to the analog. 1'b 0: PLL 0 1'b 1: PLL 1
11-10	CMN_CDIAG_REFCLK_OVRD_11_10	R	0h	Reserved
9-8	CMN_CDIAG_REFCLK_OVRD_9_8	R/W	1h	Digital reference clock receiver hysteresis adjust: Control the amount of hysteresis used for the digital reference clock receiver, by driving the cmnda_ref_clk_dig_hyst_adj signal to the analog. 2'b 00: -1X nominal 2'b 01: Nominal 2'b 10: +1X nominal 2'b 11: +2X nominal
7	CMN_CDIAG_REFCLK_OVRD_7	R	0h	Reserved
6	CMN_CDIAG_REFCLK_OVRD_6	R/W	0h	Analog reference clock enable override: This bit can be used to force the cmnda_ref_clk_en signal going to the analog to the active state. 1'b 0 : No effect on the state of the cmnda_ref_clk_en signal. 1'b 1 : The cmnda_ref_clk_en is forced to the active state.
5	CMN_CDIAG_REFCLK_OVRD_5	R/W	0h	Reference clock AC coupling cap bypass: Controls the bypassing of the AC coupling caps in the differential receiver. 1'b 0: AC coupling caps not bypassed. 1'b 1: AC coupling caps bypassed.
4	CMN_CDIAG_REFCLK_OVRD_4	R/W	0h	Derived reference clock enable: Enables the derived reference clock function, by driving the cmnda_ref_clk_der_en signal to the analog. Note that the option of using this clock is only intended to be for PCIe modes of operation. 1'b 0: Derived clock function disabled. 1'b 1: Derived clock function enabled.

**Table 12-82. CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
3-2	CMN_CDIAG_REFCLK_OVRD_3_2	R/W	2h	Reference clock high pass filter control: Controls the cutoff frequency of the high pass filter in the reference clock receiver input. This controls this function by controlling the cmnda_ref_clk_filt_ctrl signal going into the analog. The following are the valid settings for this field and the corresponding cut off frequencies. 2'b 00 : 20 - 49 MHz 2'b 01 : 50 - 99 MHz 2'b 10 : 100 - 149 MHz 2'b 11 : 150 - 166 MHz
1	CMN_CDIAG_REFCLK_OVRD_1	R	0h	Reserved
0	CMN_CDIAG_REFCLK_OVRD_0	R/W	0h	Reference clock receiver circuit clock control: 1'b 0 : The analog reference clock receiver circuit for the digital drives the cmn_ref_clk_rcv pin. 1'b 1 : The analog reference clock receiver circuit for the PLL drives the cmn_ref_clk_rcv pin.

Table 12-83. Register Call Summary for CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD

10-G SerDes Registers

- [CMN_CDIAG_REFCLK_TEST__CMN_CDIAG_REFCLK_OVRD Register \(Offset = 98h\) \[reset = 108h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.28 CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL Register (Offset = 9Ch) [reset = 5h]

CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL is shown in Figure 12-28 and described in Table 12-85.

Return to [Summary Table](#).

Power state machine clock receiver control register

Table 12-84. CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 009Ch

Figure 12-28. CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL Register

31	30	29	28	27	26	25	24
CMN_CDIAG_SDOSC_CTRL_15_2							
R-0h							
23	22	21	20	19	18	17	16
CMN_CDIAG_SDOSC_CTRL_15_2						CMN_CDIAG_S DOSC_CTRL_1	CMN_CDIAG_S DOSC_CTRL_0
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CMN_CDIAG_PSMCLK_CTRL_15_4							
R-0h							
7	6	5	4	3	2	1	0
CMN_CDIAG_PSMCLK_CTRL_15_4				CMN_CDIAG_PSMCLK_CTRL_3_0			
R-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-85. CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	CMN_CDIAG_SDOSC_CTRL_15_2	R	0h	Reserved
17	CMN_CDIAG_SDOSC_CTRL_1	R/W	0h	Oscillator Enable Override Enable: This bit enables the oscillator enable override bit in this register to directly control the signal detect oscillator. 1'b 0 : Override disabled. 1'b 1 : Override enabled
16	CMN_CDIAG_SDOSC_CTRL_0	R/W	0h	Oscillator Enable Override: When enabled by the oscillator enable override enable bit in this register, this bit can be used to directly control the enable of the signal detect oscillator. 1'b 0 : Disabled. 1'b 1 : Enabled
15-4	CMN_CDIAG_PSMCLK_CTRL_15_4	R	0h	Reserved

Table 12-85. CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
3-0	CMN_CDIAG_PSMCLK_CTRL_3_0	R/W	5h	<p>PSM clock divider value: The value of this field is used to control the divider setting of the PSM clock divider.</p> <p>The following are the encoded value for this field.</p> <p>4'b 0000 : Reserved</p> <p>4'b 0001 : Divide by 1</p> <p>4'b 0010 : Divide by 2</p> <p>4'b 0011 : Divide by 3</p> <p>...</p> <p>4'b 1111 : Divide by 15</p>

Table 12-86. Register Call Summary for CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_CDIAG_SDOSC_CTRL__CMN_CDIAG_PSMCLK_CTRL Register \(Offset = 9Ch\) \[reset = 5h\]: \[0\]](#)

12.29 CMN_CDIAG_REFCLK_DRV0_CTRL Register (Offset = A0h) [reset = X]

CMN_CDIAG_REFCLK_DRV0_CTRL is shown in Figure 12-29 and described in Table 12-88.

Return to [Summary Table](#).

Reference clock bump driver 0 control register

Table 12-87. CMN_CDIAG_REFCLK_DRV0_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 00A0h

Figure 12-29. CMN_CDIAG_REFCLK_DRV0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_CDIAG_REFCLK_DRV0_CTRL_15_10						CMN_CDIAG_REFCLK_DRV0_CTRL_9_8	
R-0h						R/W-2h	
7	6	5	4	3	2	1	0
CMN_CDIAG_REFCLK_DRV0_CTRL_7	CMN_CDIAG_REFCLK_DRV0_CTRL_6	CMN_CDIAG_REFCLK_DRV0_CTRL_5	CMN_CDIAG_REFCLK_DRV0_CTRL_4	CMN_CDIAG_REFCLK_DRV0_CTRL_3	CMN_CDIAG_REFCLK_DRV0_CTRL_2	CMN_CDIAG_REFCLK_DRV0_CTRL_1	CMN_CDIAG_REFCLK_DRV0_CTRL_0
R-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-88. CMN_CDIAG_REFCLK_DRV0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	CMN_CDIAG_REFCLK_DRV0_CTRL_15_10	R	0h	Reserved
9-8	CMN_CDIAG_REFCLK_DRV0_CTRL_9_8	R/W	2h	Clock driver drive current tune: Controls the amplitude of the reference clock driver, by controlling the cmnda_ref_clk0_itune signal going to the analog. The following is the encoding of this field. 2'b 00: 300mV pk-pk differential 2'b 01: 350mV pk-pk differential 2'b 10: 400mV pk-pk differential 2'b 11: 450mV pk-pk differential
7	CMN_CDIAG_REFCLK_DRV0_CTRL_7	R	0h	Reserved
6	CMN_CDIAG_REFCLK_DRV0_CTRL_6	R/W	1h	Reference clock driver high Z: When the reference clock driver is disabled, this controls if the driver outputs are high Z or pulled low, by controlling the cmnda_ref_clk0_drv_highz signal going to the analog. 1'b 0: Driver outputs pulled low 1'b 1: Driver outputs high Z

Table 12-88. CMN_CDIAG_REFCLK_DRV0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CMN_CDIAG_REFCLK_D RV0_CTRL_5	R/W	0h	Clock driver termination: Enables the termination in the reference clock driver, by controlling the cmnda_ref_clk0_termination signal going to the analog. 1'b 0: Disabled 1'b 1: Enabled
4	CMN_CDIAG_REFCLK_D RV0_CTRL_4	R/W	0h	Clock select: Selects which reference clock that will be driven by the reference clock driver, by controlling the cmnda_ref_clk0_clk_select signal going to the analog. 1'b 0: Received reference clock 1'b 1: Derived reference clock
3	CMN_CDIAG_REFCLK_D RV0_CTRL_3	R/W	0h	Clock gate enable override enable: This bit enables the clock gate enable override bit in this register to override the clock gate of the reference clock driver.
2	CMN_CDIAG_REFCLK_D RV0_CTRL_2	R/W	0h	Clock gate enable override: When enabled by the clock gate enable override enable bit in this register, this bit can be used to directly control the clock gate enable of the reference clock driver by controlling the cmnda_ref_clk0_clk_gate_en signal going to the analog.
1	CMN_CDIAG_REFCLK_D RV0_CTRL_1	R/W	1h	Driver enable override enable: This bit enables the driver enable override bit in this register to override the enable of the reference clock driver. Note that this driver must not be enabled when a reference clock signal is being driven to the reference clock 0 bumps.
0	CMN_CDIAG_REFCLK_D RV0_CTRL_0	R/W	0h	Driver enable override: When enabled by the driver enable override enable bit in this register, this bit can be used to directly control the enable of the reference clock driver by controlling the cmnda_ref_clk0_drv_en signal going to the analog. Note that this driver must not be enabled when a reference clock signal is being driven to the reference clock 0 bumps.

Table 12-89. Register Call Summary for CMN_CDIAG_REFCLK_DRV0_CTRL

10-G SerDes Registers

- [CMN_CDIAG_REFCLK_DRV0_CTRL Register \(Offset = A0h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.30 CMN_CDIAG_RST_DIAG__CMN_CDIAG_CDB_DIAG Register (Offset = B8h) [reset = 0h]

CMN_CDIAG_RST_DIAG__CMN_CDIAG_CDB_DIAG is shown in Figure 12-30 and described in Table 12-91.

Return to [Summary Table](#).

Common control CDB diagnostic register

Table 12-90. CMN_CDIAG_RST_DIAG__CMN_CDIAG_CDB_DIAG Instances

Instance	Physical Address
SERDES_10G0	0505 00B8h

Figure 12-30. CMN_CDIAG_RST_DIAG__CMN_CDIAG_CDB_DIAG Register

31	30	29	28	27	26	25	24
CMN_CDIAG_RST_DIAG_15_2							
R-0h							
23	22	21	20	19	18	17	16
CMN_CDIAG_RST_DIAG_15_2						CMN_CDIAG_RST_DIAG_1	CMN_CDIAG_RST_DIAG_0
R-0h						R-0h	R-0h
15	14	13	12	11	10	9	8
CMN_CDIAG_CDB_DIAG_15_1							
R-0h							
7	6	5	4	3	2	1	0
CMN_CDIAG_CDB_DIAG_15_1						CMN_CDIAG_CDB_DIAG_0	
R-0h						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 12-91. CMN_CDIAG_RST_DIAG__CMN_CDIAG_CDB_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	CMN_CDIAG_RST_DIAG_15_2	R	0h	Reserved
17	CMN_CDIAG_RST_DIAG_1	R	0h	Current state of the cdb_isl_ctrl_sm_reset_n reset.
16	CMN_CDIAG_RST_DIAG_0	R	0h	Current state of the cmn_reset_sync_n reset.
15-1	CMN_CDIAG_CDB_DIAG_15_1	R	0h	Reserved
0	CMN_CDIAG_CDB_DIAG_0	R	0h	CDB bus error: This bit will be set when the internal CDB watchdog timer expires. It is automatically cleared on a read of this register.

Table 12-92. Register Call Summary for CMN_CDIAG_RST_DIAG__CMN_CDIAG_CDB_DIAG

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_CDIAG_RST_DIAG__CMN_CDIAG_CDB_DIAG Register \(Offset = B8h\) \[reset = 0h\]: \[0\]](#)

12.31 CMN_CDIAG_DCYA Register (Offset = BCh) [reset = X]

CMN_CDIAG_DCYA is shown in [Figure 12-31](#) and described in [Table 12-94](#).

Return to [Summary Table](#).

Common control cover your alternatives register

Table 12-93. CMN_CDIAG_DCYA Instances

Instance	Physical Address
SERDES_10G0	0505 00BCh

Figure 12-31. CMN_CDIAG_DCYA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMN_CDIAG_DCYA_15_8								CMN_CDIAG_DCYA_7_0							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-X															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-94. CMN_CDIAG_DCYA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_CDIAG_DCYA_15_8	R	0h	Reserved
23-16	CMN_CDIAG_DCYA_7_0	R/W	0h	Reserved - spare
15-0	RESERVED	R/W	X	

Table 12-95. Register Call Summary for CMN_CDIAG_DCYA

10-G SerDes Registers

- [CMN_CDIAG_DCYA Register \(Offset = BCh\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.32 CMN_BGCAL_OVRD__CMN_BGCAL_CTRL Register (Offset = C0h) [reset = 0h]

CMN_BGCAL_OVRD__CMN_BGCAL_CTRL is shown in [Figure 12-32](#) and described in [Table 12-97](#).

Return to [Summary Table](#).

Bandgap calibration control register

Table 12-96.
CMN_BGCAL_OVRD__CMN_BGCAL_CTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 00C0h

Figure 12-32. CMN_BGCAL_OVRD__CMN_BGCAL_CTRL Register

31	30	29	28	27	26	25	24
CMN_BGCAL_OVRD_15	CMN_BGCAL_OVRD_14	CMN_BGCAL_OVRD_13_6					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
CMN_BGCAL_OVRD_13_6		CMN_BGCAL_OVRD_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
CMN_BGCAL_CTRL_15	CMN_BGCAL_CTRL_14	CMN_BGCAL_CTRL_13	CMN_BGCAL_CTRL_12	CMN_BGCAL_CTRL_11_6			
R/W-0h	R-0h	R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
CMN_BGCAL_CTRL_11_6		CMN_BGCAL_CTRL_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-97. CMN_BGCAL_OVRD__CMN_BGCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_BGCAL_OVRD_15	R/W	0h	Bandgap code override enable: Activation (1'b1) of this register bit allows the bandgap codes determined during the automatic calibration process to be overridden. The override value is specified using the bandgap code override value field of this register. Note: The value of this field must not be changed while the calibration function is running.
30	CMN_BGCAL_OVRD_14	R/W	0h	Analog calibration enable override: Activation (1'b1) of this register bit will force the analog calibration circuits to be enabled by activating the cmnda_bias_bgcal_en enable. Note: The value of this field must not be changed while the calibration function is running.
29-22	CMN_BGCAL_OVRD_13_6	R	0h	Reserved

Table 12-97. CMN_BGCAL_OVRD__CMN_BGCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	CMN_BGCAL_OVRD_5_0	R/W	0h	<p>Bandgap code override value: These bits are used to override the bandgap code determined during the automatic calibration process. The code written to these bits is valid when the bandgap code override enable bit in this register is active.</p> <p>The codes in this field correspond to those described in the bandgap calibration code field in the Bandgap calibration control register on page 91.</p> <p>Note: The value of this field must not be changed while the calibration function is running.</p>
15	CMN_BGCAL_CTRL_15	R/W	0h	<p>Start bandgap calibration: Activating (1'b1) this bit will start the bandgap calibration process.</p> <p>This signal must remain active until the calibration process is complete.</p> <p>To start another calibration process, this register must first be set inactive (1'b0) until the bandgap calibration process done bit in this register is cleared.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the startup state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	CMN_BGCAL_CTRL_14	R	0h	<p>Bandgap calibration process done: This bit will be set to 1'b1 when the bandgap calibration process is complete.</p> <p>It will be cleared by cmn_reset_n, or by the deactivation of the start bandgap calibration bit in this register after calibration is complete.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p> <p>Note: Three cmn_ref_clk cycles are required after the start of the calibration process to clear this signal.</p>
13	CMN_BGCAL_CTRL_13	R	0h	<p>No analog calibration response : This signal indicates that the calibration function has gone through the entire calibration process, reached the final calibration value, and the analog has not responded indicating that a valid calibration value has been reached.</p> <p>Note: Due to the nature of the calibration process, it is not possible to determine if the analog responded or not for the lowest code of 5'b10001.</p> <p>The reason for this is, when sequencing to lower codes, the calibration function is looking for the analog response to transition from 1'b1 to 1'b0.</p> <p>If the lowest calibration code is the correct code, the analog will respond with 1'b1, and the algorithm can't sequence to a lower code to look for the transition from 1'b1 to 1'b0.</p> <p>Similarly, if the analog is not responding, it is not possible to sequence to a lower code to detect this.</p> <p>Therefore, even when the calibration function selects this calibration code as valid, this bit will be set.</p>

Table 12-97. CMN_BGCAL_OVRD__CMN_BGCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CMN_BGCAL_CTRL_12	R	0h	Current analog comparator response: This is the current state of the analog comparator response signal (cmnda_bias_bgcal_comp). This signal is not synchronized, and is provided for diagnostic purposes only.
11-6	CMN_BGCAL_CTRL_11_6	R	0h	Reserved
5-0	CMN_BGCAL_CTRL_5_0	R	0h	<p>Bandgap calibration code: This is the calibration code that was determined by the bandgap calibration process.</p> <p>The following indicates how this encoding maps to the cmnda_bias_bgcal_up and cmnda_bias_bgcal_azel signals going to the analog bandgap function.</p> <p>The 6 bit value on the left is the value of this field.</p> <p>The 1 bit value on the right corresponds to the value of cmnda_bias_bgcal_up.</p> <p>The 5 bit field corresponds to the value of cmnda_bias_bgcal_azel.</p> <p>6'b 011111 : 1'b1, 5'b11111</p> <p>6'b 011110 : 1'b1, 5'b11110</p> <p>...</p> <p>6'b 000010 : 1'b1, 5'b00010</p> <p>6'b 000001 : 1'b1, 5'b00001</p> <p>6'b 000000 : 1'b1, 5'b00000</p> <p>6'b 111111 : 1'b0, 5'b00001</p> <p>6'b 111110 : 1'b0, 5'b00010</p> <p>...</p> <p>6'b 100010 : 1'b0, 5'b11110</p> <p>6'b 100001 : 1'b0, 5'b11111</p>

Table 12-98. Register Call Summary for CMN_BGCAL_OVRD__CMN_BGCAL_CTRL

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_BGCAL_OVRD__CMN_BGCAL_CTRL Register \(Offset = C0h\) \[reset = 0h\]: \[0\]](#)

12.33 CMN_BGCAL_TUNE__CMN_BGCAL_START Register (Offset = C4h) [reset = 0h]

CMN_BGCAL_TUNE__CMN_BGCAL_START is shown in Figure 12-33 and described in Table 12-100.

Return to [Summary Table](#).

Bandgap calibration start register

Table 12-99.
CMN_BGCAL_TUNE__CMN_BGCAL_START
Instances

Instance	Physical Address
SERDES_10G0	0505 00C4h

Figure 12-33. CMN_BGCAL_TUNE__CMN_BGCAL_START Register

31	30	29	28	27	26	25	24
CMN_BGCAL_TUNE_15_6							
R-0h							
23	22	21	20	19	18	17	16
CMN_BGCAL_TUNE_15_6				CMN_BGCAL_TUNE_5_0			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CMN_BGCAL_START_15		CMN_BGCAL_START_14_6					
R/W-0h		R-0h					
7	6	5	4	3	2	1	0
CMN_BGCAL_START_14_6				CMN_BGCAL_START_5_0			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-100. CMN_BGCAL_TUNE__CMN_BGCAL_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	CMN_BGCAL_TUNE_15_6	R	0h	Reserved
21-16	CMN_BGCAL_TUNE_5_0	R/W	0h	Bandgap calibration tune value: The value of this field is added to the automatically calibrated code, or the override code if override is enabled. Note that this value is a twos complement value, so the calibrated code can be increased or decreased.
15	CMN_BGCAL_START_15	R/W	0h	Bandgap calibration direction: This controls the direction that the automatic calibration process steps the calibration codes in. 1'b 0 : From 4'b1001 to 4'b0111. 1'b 1 : From 4'b0111 to 4'b0000.
14-6	CMN_BGCAL_START_14_6	R	0h	Reserved
5-0	CMN_BGCAL_START_5_0	R/W	0h	Start bandgap calibration code: This is the calibration code that the calibration process starts with when automatic calibration is run. The codes in this field correspond to those described in the bandgap calibration code field in the Bandgap calibration control register on page 91.

Table 12-101. Register Call Summary for CMN_BGCAL_TUNE__CMN_BGCAL_START

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_BGCAL_TUNE__CMN_BGCAL_START Register \(Offset = C4h\) \[reset = 0h\]: \[0\]](#)

12.34 CMN_BGCAL_ITER_TMR__CMN_BGCAL_INIT_TMR Register (Offset = C8h) [reset = 007D007Dh]

CMN_BGCAL_ITER_TMR__CMN_BGCAL_INIT_TMR is shown in Figure 12-34 and described in Table 12-103.

Return to [Summary Table](#).

Bandgap calibration initialization timer register

Table 12-102. CMN_BGCAL_ITER_TMR__CMN_BGCAL_INIT_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 00C8h

Figure 12-34. CMN_BGCAL_ITER_TMR__CMN_BGCAL_INIT_TMR Register

31	30	29	28	27	26	25	24
CMN_BGCAL_ITER_TMR_15_9							CMN_BGCAL_I TER_TMR_8_0
R-0h							R/W-7Dh
23	22	21	20	19	18	17	16
CMN_BGCAL_ITER_TMR_8_0							
R/W-7Dh							
15	14	13	12	11	10	9	8
CMN_BGCAL_INIT_TMR_15_9							CMN_BGCAL_I NIT_TMR_8_0
R-0h							R/W-7Dh
7	6	5	4	3	2	1	0
CMN_BGCAL_INIT_TMR_8_0							
R/W-7Dh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-103. CMN_BGCAL_ITER_TMR__CMN_BGCAL_INIT_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	CMN_BGCAL_ITER_TMR_15_9	R	0h	Reserved
24-16	CMN_BGCAL_ITER_TMR_8_0	R/W	7Dh	Iteration wait timer value: This is the number of cmn_ref_clk clocks to wait between when a value is placed on the bandgap calibration signals going to the analog, and when the comparator value coming from the analog circuits can be checked. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 5 uSec. Note that this should never be set to a value of less than 3.
15-9	CMN_BGCAL_INIT_TMR_15_9	R	0h	Reserved
8-0	CMN_BGCAL_INIT_TMR_8_0	R/W	7Dh	Initialization wait timer value: This is the number of cmn_ref_clk clocks to wait between when the analog bandgap calibration circuits are enabled, and when the first values are placed on the bandgap calibration signals going to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 5 uSec. Note that this should never be set to a value of less than 1.

Table 12-104. Register Call Summary for CMN_BGCAL_ITER_TMR__CMN_BGCAL_INIT_TMR

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_BGCAL_ITER_TMR__CMN_BGCAL_INIT_TMR Register \(Offset = C8h\) \[reset = 007D007Dh\]: \[0\]](#)

12.35 CMN_IBCAL_OVRD__CMN_IBCAL_CTRL Register (Offset = E0h) [reset = 0h]

CMN_IBCAL_OVRD__CMN_IBCAL_CTRL is shown in Figure 12-35 and described in Table 12-106.

Return to [Summary Table](#).

External bias current calibration control register

Table 12-105.
CMN_IBCAL_OVRD__CMN_IBCAL_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 00E0h

Figure 12-35. CMN_IBCAL_OVRD__CMN_IBCAL_CTRL Register

31	30	29	28	27	26	25	24
CMN_IBCAL_OVRD_15	CMN_IBCAL_OVRD_14	CMN_IBCAL_OVRD_13_7					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
CMN_IBCAL_OVRD_13_7	CMN_IBCAL_OVRD_6_0						
R-0h	R/W-0h						
15	14	13	12	11	10	9	8
CMN_IBCAL_CTRL_15	CMN_IBCAL_CTRL_14	CMN_IBCAL_CTRL_13	CMN_IBCAL_CTRL_12	CMN_IBCAL_CTRL_11_7			
R/W-0h	R-0h	R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
CMN_IBCAL_CTRL_11_7	CMN_IBCAL_CTRL_6_0						
R-0h	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-106. CMN_IBCAL_OVRD__CMN_IBCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_IBCAL_OVRD_15	R/W	0h	Calibration code override enable: Activation (1'b1) of this register bit allows the calibration code determined during the automatic resistor calibration process to be overridden. The override value is specified using the calibration code override value field of this register.
30	CMN_IBCAL_OVRD_14	R/W	0h	Analog calibration enable override: Activation (1'b1) of this register bit will force the analog calibration circuits to be enabled by activating the cmnda_ibiascal_en enable and the cmnda_ibiascal_clk clock.
29-23	CMN_IBCAL_OVRD_13_7	R	0h	Reserved

Table 12-106. CMN_IBCAL_OVRD__CMN_IBCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-16	CMN_IBCAL_OVRD_6_0	R/W	0h	<p>Calibration code override value: These bits are used to override the calibration code determined during the automatic resistor calibration process.</p> <p>The code written to these bits is valid when the calibration code override enable bit in this register is active.</p> <p>The following are the values for the code:</p> <p>7'b 0000000: Minimum value.</p> <p>7'b0000001</p> <p>7'b0000010</p> <p>7'b0000011</p> <p>...</p> <p>7'b0111110</p> <p>7'b 0111111: Maximum value.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>
15	CMN_IBCAL_CTRL_15	R/W	0h	<p>Start calibration: Activating (1'b1) this bit will start the calibration process.</p> <p>This signal must remain active until the calibration process is complete.</p> <p>To start another calibration process, this register must first be set inactive (1'b0) until the calibration process done bit in this register is cleared.</p> <p>Note: This signal is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the startup state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	CMN_IBCAL_CTRL_14	R	0h	<p>Calibration process done: This bit will be set to 1'b1 when the calibration process is complete.</p> <p>It will be cleared by cmn_reset_n, or by the deactivation of the start calibration bit in this register after calibration is complete.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p> <p>Note: Three cmn_ref_clk cycles are required after the start of the resistor calibration process to clear this signal.</p>

Table 12-106. CMN_IBCAL_OVRD__CMN_IBCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CMN_IBCAL_CTRL_13	R	0h	<p>No analog calibration response : This signal indicates that the calibration function has gone through the entire calibration process, reached the final calibration value, and the analog has not responded indicating that a valid calibration value has been reached. Note: Due to the nature of the calibration process, it is not possible to determine if the analog responded or not for the lowest code of 7'b000000.</p> <p>The reason for this is, when sequencing to lower codes, the calibration function is looking for the analog response to transition from 1'b1 to 1'b0.</p> <p>If the lowest calibration code is the correct code, the analog will respond with 1'b1, and the algorithm can't sequence to a lower code to look for the transition from 1'b1 to 1'b0.</p> <p>Similarly, if the analog is not responding, it is not possible to sequence to a lower code to detect this.</p> <p>Therefore, even when the calibration function selects this calibration code as valid, this bit will be set.</p>
12	CMN_IBCAL_CTRL_12	R	0h	<p>Current analog comparator response: This is the current state of the analog comparator response signal (cmnda_ibiascal_comp). This signal is not synchronized, and is provided for diagnostic purposes only.</p>
11-7	CMN_IBCAL_CTRL_11_7	R	0h	Reserved
6-0	CMN_IBCAL_CTRL_6_0	R	0h	<p>Calibration code: This is the calibration code that was determined by the calibration process.</p> <p>The following are the values for the code:</p> <p>7'b 0000000: Minimum value.</p> <p>7'b0000001</p> <p>7'b0000010</p> <p>7'b0000011</p> <p>...</p> <p>7'b0111110</p> <p>7'b 0111111: Maximum value.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p> <p>Note: The reset value for this field is with the common calibration power island switched off.</p> <p>In cases where this power island is switched on, the reset value be 7'b0011111.</p>

Table 12-107. Register Call Summary for CMN_IBCAL_OVRD__CMN_IBCAL_CTRL

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_IBCAL_OVRD__CMN_IBCAL_CTRL Register \(Offset = E0h\) \[reset = 0h\]: \[0\]](#)

12.36 CMN_IBCAL_TUNE__CMN_IBCAL_START Register (Offset = E4h) [reset = 1Fh]

CMN_IBCAL_TUNE__CMN_IBCAL_START is shown in Figure 12-36 and described in Table 12-109.

Return to [Summary Table](#).

External bias current calibration start register

Table 12-108.
CMN_IBCAL_TUNE__CMN_IBCAL_START Instances

Instance	Physical Address
SERDES_10G0	0505 00E4h

Figure 12-36. CMN_IBCAL_TUNE__CMN_IBCAL_START Register

31	30	29	28	27	26	25	24
CMN_IBCAL_TUNE_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_IBCAL_TUNE_15_7	CMN_IBCAL_TUNE_6_0						
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CMN_IBCAL_START_15	CMN_IBCAL_START_14_7						
R/W-0h				R-0h			
7	6	5	4	3	2	1	0
CMN_IBCAL_START_14_7	CMN_IBCAL_START_6_0						
R-0h				R/W-1Fh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-109. CMN_IBCAL_TUNE__CMN_IBCAL_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_IBCAL_TUNE_15_7	R	0h	Reserved
22-16	CMN_IBCAL_TUNE_6_0	R/W	0h	Calibration tune value: The value of this field is added to the automatically calibrated code, or the override code if override is enabled. Note that this value is a twos complement value, so the calibrated code can be increased or decreased.
15	CMN_IBCAL_START_15	R/W	0h	Calibration direction: This controls the direction that the automatic calibration process steps the calibration codes in. 1'b 0 : From 7'b00000000 to 7'b01111111. 1'b 1 : From 7'b01111111 to 7'b00000000.
14-7	CMN_IBCAL_START_14_7	R	0h	Reserved

Table 12-109. CMN_IBCAL_TUNE__CMN_IBCAL_START Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	CMN_IBCAL_START_6_0	R/W	1Fh	<p>Start resistor calibration code: This is the calibration code that the resistor calibration process starts with when automatic calibration is run.</p> <p>The following are the values for the code.</p> <p>7'b 0000000: Minimum value.</p> <p>7'b0000001</p> <p>7'b0000010</p> <p>7'b0000011</p> <p>...</p> <p>7'b0111110</p> <p>7'b 0111111: Maximum value.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>

Table 12-110. Register Call Summary for CMN_IBCAL_TUNE__CMN_IBCAL_START

10-G SerDes Registers

- [CMN_IBCAL_TUNE__CMN_IBCAL_START Register \(Offset = E4h\) \[reset = 1Fh\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.37 CMN_IBCAL_ITER_TMR__CMN_IBCAL_INIT_TMR Register (Offset = E8h) [reset = 00070019h]

CMN_IBCAL_ITER_TMR__CMN_IBCAL_INIT_TMR is shown in Figure 12-37 and described in Table 12-112.

Return to [Summary Table](#).

External bias current calibration initialization timer register

Table 12-111. CMN_IBCAL_ITER_TMR__CMN_IBCAL_INIT_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 00E8h

Figure 12-37. CMN_IBCAL_ITER_TMR__CMN_IBCAL_INIT_TMR Register

31	30	29	28	27	26	25	24
CMN_IBCAL_ITER_TMR_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_IBCAL_ITER_TMR_15_7	CMN_IBCAL_ITER_TMR_6_0						
R-0h				R/W-7h			
15	14	13	12	11	10	9	8
CMN_IBCAL_INIT_TMR_15_7							
R-0h							
7	6	5	4	3	2	1	0
CMN_IBCAL_INIT_TMR_15_7	CMN_IBCAL_INIT_TMR_6_0						
R-0h				R/W-19h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-112. CMN_IBCAL_ITER_TMR__CMN_IBCAL_INIT_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_IBCAL_ITER_TMR_15_7	R	0h	Reserved
22-16	CMN_IBCAL_ITER_TMR_6_0	R/W	7h	Iteration wait timer value: This is the number of cmn_ref_clk clocks to wait between when a value is placed on the calibration selection bus going to the analog, and when the comparator value coming from the analog circuits can be checked. Note that this should never be set to a value of less than 3.
15-7	CMN_IBCAL_INIT_TMR_15_7	R	0h	Reserved
6-0	CMN_IBCAL_INIT_TMR_6_0	R/W	19h	Initialization wait timer value: This is the number of cmn_ref_clk clocks to wait between when the analog calibration circuits are enabled, and when the first calibration selection value is placed on the calibration code bus, going to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 1 uSec. Note that this should never be set to a value of less than 1.

Table 12-113. Register Call Summary for CMN_IBCAL_ITER_TMR__CMN_IBCAL_INIT_TMR

10-G SerDes Registers

- [CMN_IBCAL_ITER_TMR__CMN_IBCAL_INIT_TMR Register \(Offset = E8h\) \[reset = 00070019h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.38 CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL Register (Offset = 100h) [reset = 20280000h]

CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL is shown in Figure 12-38 and described in Table 12-115.

Return to [Summary Table](#).

PLL 0 VCO calibration control register

Table 12-114. CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 0100h

Figure 12-38. CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL Register

31	30	29	28	27	26	25	24
CMN_PLL0_VCOCAL_START_15	CMN_PLL0_VCOCAL_START_14_12			CMN_PLL0_VCOCAL_START_11_8			
R-0h	R/W-2h			R-0h			
23	22	21	20	19	18	17	16
CMN_PLL0_VCOCAL_START_7_0							
R/W-28h							
15	14	13	12	11	10	9	8
CMN_PLL0_VCOCAL_CTRL_15	CMN_PLL0_VCOCAL_CTRL_14	CMN_PLL0_VCOCAL_CTRL_13_8					
R/W-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
CMN_PLL0_VCOCAL_CTRL_7_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-115. CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLL0_VCOCAL_START_15	R	0h	Reserved
30-28	CMN_PLL0_VCOCAL_START_14_12	R/W	2h	VCO calibration initial step size control: This field specifies the initial step size for the VCO calibration state machine. The following are the values that can be used in this field, and the corresponding step sizes. 3'b 000 : 1 3'b 001 : 2 3'b 010 : 4 3'b 011 : 8 3'b 100 : 16 3'b 101 - 3'b 111 : Reserved
27-24	CMN_PLL0_VCOCAL_START_11_8	R	0h	Reserved

**Table 12-115. CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
23-16	CMN_PLL0_VCOCAL_START_7_0	R/W	28h	<p>VCO calibration code starting point value: This field specifies the starting VCO code that is used by the VCO calibration state machine.</p> <p>The purpose of this value is such that the VCO calibration process starts at a point that is, on average, relatively close to the final calibration point.</p> <p>This allows the calibration time to be reduced, on average.</p> <p>The encoding of this field is the same as what is described in the VCO calibration control register.</p> <p>Note: This field is intended to be for diagnostics purposes only.</p> <p>Note : This field must be set to a value that is always at least one step size away from the minimum and maximum calibration codes, and is a function of the step size specified in this register.</p> <p>For example, if the initial step size is 4, this value must be at least 4 greater than the minimum calibration code or 4 less than the maximum calibration code.</p>
15	CMN_PLL0_VCOCAL_CTRL_15	R/W	0h	<p>Start VCO calibration: Activating (1'b1) this bit will start a VCO calibration process.</p> <p>This bit must remain active until the VCO calibration process is complete (as indicated by the VCO calibration process done bit in this register).</p> <p>To start another VCO calibration process, the VCO calibration process done bit must have gone inactive from any prior calibration process.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the PLL control state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	CMN_PLL0_VCOCAL_CTRL_14	R	0h	<p>VCO calibration process done: This bit will be set to 1'b1 when the VCO calibration process is complete.</p> <p>It will be cleared by the deactivation of the Start VCO calibration bit in this register.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p>
13-8	CMN_PLL0_VCOCAL_CTRL_13_8	R	0h	Reserved

**Table 12-115. CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
7-0	CMN_PLL0_VCOCAL_CTRL_7_0	R	0h	<p>VCO calibration code: This is the calibration code that was determined by the VCO calibration process.</p> <p>This signal is valid when the VCO calibration process is complete.</p> <p>The values of this field correspond to different frequency bands the VCO will operate in.</p> <p>The frequency bands are controlled by the number of capacitors that are switched in the VCO analog circuit.</p> <p>This field specifies the number of capacitors that are switched in.</p> <p>The following are the values for this code:</p> <p>8'b 00000000: 0 Capacitors activated</p> <p>8'b 00000001: 1 Capacitor activated</p> <p>8'b 00000010: 2 Capacitors activated</p> <p>8'b 00000011: 3 Capacitors activated</p> <p>...</p> <p>8'b 11111110: 254 Capacitors activated</p> <p>8'b 11111111: 255 Capacitors activated</p> <p>Note: This register is intended to be for diagnostics purposes only.</p> <p>Note: The reset value for this field is with the PLL controller power island switched off.</p> <p>In cases where this power island is switched on, the reset value be 8'h28.</p>

Table 12-116. Register Call Summary for CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL

10-G SerDes Registers

- [CMN_PLL0_VCOCAL_START__CMN_PLL0_VCOCAL_CTRL Register \(Offset = 100h\) \[reset = 20280000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.39 CMN_PLL0_VCOCAL_OVRD__CMN_PLL0_VCOCAL_TCTRL Register (Offset = 104h) [reset = 4h]

CMN_PLL0_VCOCAL_OVRD__CMN_PLL0_VCOCAL_TCTRL is shown in Figure 12-39 and described in Table 12-118.

Return to [Summary Table](#).

PLL 0 VCO calibration timer control register

Table 12-117. CMN_PLL0_VCOCAL_OVRD__CMN_PLL0_VCOCAL_TCTRL Instances

Instance	Physical Address
SERDES_10G0	0505 0104h

Figure 12-39. CMN_PLL0_VCOCAL_OVRD__CMN_PLL0_VCOCAL_TCTRL Register

31	30	29	28	27	26	25	24
CMN_PLL0_VCOCAL_OVRD_15	CMN_PLL0_VCOCAL_OVRD_14_8						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
CMN_PLL0_VCOCAL_OVRD_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL0_VCOCAL_TCTRL_15_3							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL0_VCOCAL_TCTRL_15_3					CMN_PLL0_VCOCAL_TCTRL_2_0		
R-0h					R/W-4h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-118. CMN_PLL0_VCOCAL_OVRD__CMN_PLL0_VCOCAL_TCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLL0_VCOCAL_OVRD_15	R/W	0h	VCO calibration code override enable: Activating (1'b1) this bit allows the VCO code determined during the automatic VCO calibration process to be overridden by the value driven by the VCO calibration code override value field in this register. Note: This bit is intended to be for diagnostics purposes only.
30-24	CMN_PLL0_VCOCAL_OVRD_14_8	R	0h	Reserved
23-16	CMN_PLL0_VCOCAL_OVRD_7_0	R/W	0h	VCO calibration code override value: This field is used to override the VCO code determined during the automatic VCO calibration process. The VCO code driven on this field is valid when the VCO calibration code override enable bit in this register is active. The encoding of this field is the same as what is described in the VCO calibration control register.
15-3	CMN_PLL0_VCOCAL_TCTRL_15_3	R	0h	Reserved

**Table 12-118. CMN_PLL0_VCOCAL_OVRD__CMN_PLL0_VCOCAL_TCTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2-0	CMN_PLL0_VCOCAL_TCTRL_2_0	R/W	4h	<p>VCO calibration initial time scale control: This field specifies the calibration start time scaling factor applied to the VCO calibration when running the initial step size for the calibration code if not set to 1.</p> <p>Setting this value to a value other than 1 will reduce the calibration measurement time by the amount specified below.</p> <p>Then when the final calibration steps are made the full calibration time will be used to get the appropriate amount of resolution.</p> <p>3'b 000 : Div 1 3'b 001 : Div 2 3'b 010 : Div 4 3'b 011 : Div 8 3'b 100 : Div 16 3'b 101 : Div 32 3'b 110 : Div 64 3'b 111 : Div 128</p>

Table 12-119. Register Call Summary for CMN_PLL0_VCOCAL_OVRD__CMN_PLL0_VCOCAL_TCTRL

10-G SerDes Registers

- [CMN_PLL0_VCOCAL_OVRD__CMN_PLL0_VCOCAL_TCTRL Register \(Offset = 104h\) \[reset = 4h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.40 CMN_PLL0_VCOCAL_ITER_TMR__CMN_PLL0_VCOCAL_INIT_TMR Register (Offset = 108h) [reset = 001003E8h]

CMN_PLL0_VCOCAL_ITER_TMR__CMN_PLL0_VCOCAL_INIT_TMR is shown in Figure 12-40 and described in Table 12-121.

Return to [Summary Table](#).

PLL 0 VCO calibration initialization timer register

Table 12-120.

CMN_PLL0_VCOCAL_ITER_TMR__CMN_PLL0_VCOCAL_INIT_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0108h

Figure 12-40. CMN_PLL0_VCOCAL_ITER_TMR__CMN_PLL0_VCOCAL_INIT_TMR Register

31	30	29	28	27	26	25	24
CMN_PLL0_VCOCAL_ITER_TMR_15_14		CMN_PLL0_VCOCAL_ITER_TMR_13_0					
R-0h		R/W-10h					
23	22	21	20	19	18	17	16
CMN_PLL0_VCOCAL_ITER_TMR_13_0							
R/W-10h							
15	14	13	12	11	10	9	8
CMN_PLL0_VCOCAL_INIT_TMR_15_14		CMN_PLL0_VCOCAL_INIT_TMR_13_0					
R-0h		R/W-3E8h					
7	6	5	4	3	2	1	0
CMN_PLL0_VCOCAL_INIT_TMR_13_0							
R/W-3E8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-121. CMN_PLL0_VCOCAL_ITER_TMR__CMN_PLL0_VCOCAL_INIT_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	CMN_PLL0_VCOCAL_ITER_TMR_15_14	R	0h	Reserved
29-16	CMN_PLL0_VCOCAL_ITER_TMR_13_0	R/W	10h	Iteration wait timer value: This is the number of clocks to wait between when a calibration code is driven to the analog, and when the clock rates are measured.
15-14	CMN_PLL0_VCOCAL_INIT_TMR_15_14	R	0h	Reserved
13-0	CMN_PLL0_VCOCAL_INIT_TMR_13_0	R/W	3E8h	Initialization wait timer value: This is the number of clocks to wait between when the analog VCO calibration circuits are enabled, and when the first calibration code is driven to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 10 uSec.

Table 12-122. Register Call Summary for CMN_PLL0_VCOCAL_ITER_TMR__CMN_PLL0_VCOCAL_INIT_TMR

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL0_VCOCAL_ITER_TMR__CMN_PLL0_VCOCAL_INIT_TMR Register \(Offset = 108h\) \[reset = 001003E8h\]: \[0\]](#)

12.41 CMN_PLL0_VCOCAL_REFTIM_START Register (Offset = 10Ch) [reset = X]

CMN_PLL0_VCOCAL_REFTIM_START is shown in Figure 12-41 and described in Table 12-124.

Return to [Summary Table](#).

PLL 0 VCO calibration reference clock timer start value register

Table 12-123. CMN_PLL0_VCOCAL_REFTIM_START Instances

Instance	Physical Address
SERDES_10G0	0505 010Ch

Figure 12-41. CMN_PLL0_VCOCAL_REFTIM_START Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_PLL0_VCOCAL_REFTIM_START_15_14		CMN_PLL0_VCOCAL_REFTIM_START_13_0					
R-0h		R/W-C5Fh					
7	6	5	4	3	2	1	0
CMN_PLL0_VCOCAL_REFTIM_START_13_0							
R/W-C5Fh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-124. CMN_PLL0_VCOCAL_REFTIM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	CMN_PLL0_VCOCAL_REFTIM_START_15_14	R	0h	Reserved
13-0	CMN_PLL0_VCOCAL_REFTIM_START_13_0	R/W	C5Fh	PLL VCO calibration reference clock timer start value : This is the value that is loaded into the reference clock timer as the starting point for that timer, when running VCO calibration. The value in this field must correspond to a time that is approximately one full spread spectrum cycle long (31.67 uSec) Note that the actual number of clocks counted is one larger than what is specified by this field.

Table 12-125. Register Call Summary for CMN_PLL0_VCOCAL_REFTIM_START

10-G SerDes Registers

- [CMN_PLL0_VCOCAL_REFTIM_START Register \(Offset = 10Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.42 CMN_PLL0_VCOCAL_PLLCNT_START Register (Offset = 110h) [reset = X]

CMN_PLL0_VCOCAL_PLLCNT_START is shown in Figure 12-42 and described in Table 12-127.

Return to [Summary Table](#).

PLL 0 VCO calibration PLL clock counter start value register

Table 12-126. CMN_PLL0_VCOCAL_PLLCNT_START Instances

Instance	Physical Address
SERDES_10G0	0505 0110h

Figure 12-42. CMN_PLL0_VCOCAL_PLLCNT_START Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_PLL0_VCOCAL_PLLCNT_START_15_14		CMN_PLL0_VCOCAL_PLLCNT_START_13_0					
R-0h		R/W-C5Fh					
7	6	5	4	3	2	1	0
CMN_PLL0_VCOCAL_PLLCNT_START_13_0							
R/W-C5Fh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-127. CMN_PLL0_VCOCAL_PLLCNT_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	CMN_PLL0_VCOCAL_PL LCNT_START_15_14	R	0h	Reserved
13-0	CMN_PLL0_VCOCAL_PL LCNT_START_13_0	R/W	C5Fh	PLL VCO calibration PLL clock counter start value : This is the value that is loaded into the PLL clock counter as the starting point for that counter, when running VCO calibration. When programming this register, it is important to understand how the frequency of the cmnda_pll0_fb_divider_clk is calculated relative to the reference clock. This is described in section 10.4 Dual VCO PLL on page 422. Note that the actual number of clocks counted is one larger than what is specified by this field.

Table 12-128. Register Call Summary for CMN_PLL0_VCOCAL_PLLCNT_START

10-G SerDes Registers

- [CMN_PLL0_VCOCAL_PLLCNT_START Register \(Offset = 110h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.43 CMN_PLL0_FRACDIVL_M0__CMN_PLL0_INTDIV_M0 Register (Offset = 120h) [reset = 0h]

CMN_PLL0_FRACDIVL_M0__CMN_PLL0_INTDIV_M0 is shown in Figure 12-43 and described in Table 12-130.

Return to [Summary Table](#).

PLL 0 feedback divider integer register mode 0

Table 12-129. CMN_PLL0_FRACDIVL_M0__CMN_PLL0_INTDIV_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0120h

Figure 12-43. CMN_PLL0_FRACDIVL_M0__CMN_PLL0_INTDIV_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL0_FRACDIVL_M0_15_0							
R/W-0h							
23	22	21	20	19	18	17	16
CMN_PLL0_FRACDIVL_M0_15_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL0_INTDIV_M0_15_9							CMN_PLL0_IN TDIV_M0_8_0
R-0h							R/W-0h
7	6	5	4	3	2	1	0
CMN_PLL0_INTDIV_M0_8_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-130. CMN_PLL0_FRACDIVL_M0__CMN_PLL0_INTDIV_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMN_PLL0_FRACDIVL_M0_15_0	R/W	0h	pll_fb_div_fractional: Value of the pll_fb_div_fractional[15:0] signal.
15-9	CMN_PLL0_INTDIV_M0_15_9	R	0h	Reserved
8-0	CMN_PLL0_INTDIV_M0_8_0	R/W	0h	pll_fb_div_integer value: Value of the pll_fb_div_integer signal.

Table 12-131. Register Call Summary for CMN_PLL0_FRACDIVL_M0__CMN_PLL0_INTDIV_M0

10-G SerDes Registers

- [CMN_PLL0_FRACDIVL_M0__CMN_PLL0_INTDIV_M0 Register \(Offset = 120h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.44 CMN_PLL0_HIGH_THR_M0__CMN_PLL0_FRACDIVH_M0 Register (Offset = 124h) [reset = 0h]

CMN_PLL0_HIGH_THR_M0__CMN_PLL0_FRACDIVH_M0 is shown in [Figure 12-44](#) and described in [Table 12-133](#).

Return to [Summary Table](#).

PLL 0 feedback divider fractional high register mode 0

Table 12-132. CMN_PLL0_HIGH_THR_M0__CMN_PLL0_FRACDIVH_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0124h

Figure 12-44. CMN_PLL0_HIGH_THR_M0__CMN_PLL0_FRACDIVH_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL0_HIGH_THR_M0_15_9							CMN_PLL0_HI GH_THR_M0_8 _0
R-0h							R/W-0h
23	22	21	20	19	18	17	16
CMN_PLL0_HIGH_THR_M0_8_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL0_FRACDIVH_M0_15_3							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL0_FRACDIVH_M0_15_3					CMN_PLL0_FRACDIVH_M0_2_0		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-133. CMN_PLL0_HIGH_THR_M0__CMN_PLL0_FRACDIVH_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	CMN_PLL0_HIGH_THR_M0_15_9	R	0h	Reserved
24-16	CMN_PLL0_HIGH_THR_M0_8_0	R/W	0h	pll_fb_div_high_theshold: Value of the pll_fb_div_high_threshold signal. The value of this register should be 2/3 the value of the combined integer and fractional divider values, and rounded up to the next even number.
15-3	CMN_PLL0_FRACDIVH_M0_15_3	R	0h	Reserved
2-0	CMN_PLL0_FRACDIVH_M0_2_0	R/W	0h	pll_fb_div_fractional: Value of the pll_fb_div_fractional[18:16] signal.

Table 12-134. Register Call Summary for CMN_PLL0_HIGH_THR_M0__CMN_PLL0_FRACDIVH_M0

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL0_HIGH_THR_M0__CMN_PLL0_FRACDIVH_M0 Register \(Offset = 124h\) \[reset = 0h\]: \[0\]](#)

12.45 CMN_PLL0_DSM_FBH_OVRD_M0__CMN_PLL0_DSM_DIAG_M0 Register (Offset = 128h) [reset = 001E4004h]

CMN_PLL0_DSM_FBH_OVRD_M0__CMN_PLL0_DSM_DIAG_M0 is shown in Figure 12-45 and described in Table 12-136.

Return to [Summary Table](#).

PLL 0 delta sigma modulator diagnostics register mode 0

Table 12-135. CMN_PLL0_DSM_FBH_OVRD_M0__CMN_PLL0_DSM_DIAG_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0128h

Figure 12-45. CMN_PLL0_DSM_FBH_OVRD_M0__CMN_PLL0_DSM_DIAG_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL0_DSM_FBH_OVRD_M0_15_9							CMN_PLL0_DS M_FBH_OVRD _M0_8_0
R-0h							R/W-1Eh
23	22	21	20	19	18	17	16
CMN_PLL0_DSM_FBH_OVRD_M0_8_0							
R/W-1Eh							
15	14	13	12	11	10	9	8
CMN_PLL0_DS M_DIAG_M0_1 5	CMN_PLL0_DS M_DIAG_M0_1 4	CMN_PLL0_DSM_DIAG_M0_13_4					
R/W-0h	R/W-1h	R-0h					
7	6	5	4	3	2	1	0
CMN_PLL0_DSM_DIAG_M0_13_4				CMN_PLL0_DSM_DIAG_M0_3_0			
R-0h				R/W-4h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-136. CMN_PLL0_DSM_FBH_OVRD_M0__CMN_PLL0_DSM_DIAG_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	CMN_PLL0_DSM_FBH_OVRD_M0_15_9	R	0h	Reserved
24-16	CMN_PLL0_DSM_FBH_OVRD_M0_8_0	R/W	1Eh	PLL feedback divider high override value : When enabled by the PLL feedback divider override enable bit in the PLL 0 delta sigma modulator diagnostics register mode 0 on page 102, the value in this field will be used to override the value on the cmnda_pll0_fb_div_high signal.
15	CMN_PLL0_DSM_DIAG_M0_15	R/W	0h	Delta sigma bypass enable: When set to 1'b1, the delta sigma modulator will be bypassed, and the output will be the value specified for the internal pll_fb_div_integer signal.
14	CMN_PLL0_DSM_DIAG_M0_14	R/W	1h	PLL feedback divider override enable : When active (1'b1), the feedback divider low and high override values in the PLL 0 delta sigma modulator feedback divider value high override register mode 0 on page 102 and PLL 0 delta sigma modulator feedback divider value low override register mode 0 on page 102 registers will be used to override the feedback divider values driven to the analog.

Table 12-136. CMN_PLL0_DSM_FBH_OVRD_M0__CMN_PLL0_DSM_DIAG_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-4	CMN_PLL0_DSM_DIAG_M0_13_4	R	0h	Reserved
3-0	CMN_PLL0_DSM_DIAG_M0_3_0	R/W	4h	PLL feedback divider latency adjustment: This signal specifies a value to be subtracted from the feedback divider settings before they are output on the cmnda_pll0_fb_div_high and cmnda_pll0_fb_div_low signals.

Table 12-137. Register Call Summary for CMN_PLL0_DSM_FBH_OVRD_M0__CMN_PLL0_DSM_DIAG_M0

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL0_DSM_FBH_OVRD_M0__CMN_PLL0_DSM_DIAG_M0 Register \(Offset = 128h\) \[reset = 001E4004h\]: \[0\]](#)

12.46 CMN_PLL0_DSM_FBL_OVRD_M0 Register (Offset = 12Ch) [reset = X]

CMN_PLL0_DSM_FBL_OVRD_M0 is shown in [Figure 12-46](#) and described in [Table 12-139](#).

Return to [Summary Table](#).

PLL 0 delta sigma modulator feedback divider value low override register mode 0

Table 12-138. CMN_PLL0_DSM_FBL_OVRD_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 012Ch

Figure 12-46. CMN_PLL0_DSM_FBL_OVRD_M0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_PLL0_DSM_FBL_OVRD_M0_15_9						CMN_PLL0_DS M_FBL_OVRD_ M0_8_0	
R-0h						R/W-Ch	
7	6	5	4	3	2	1	0
CMN_PLL0_DSM_FBL_OVRD_M0_8_0							
R/W-Ch							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-139. CMN_PLL0_DSM_FBL_OVRD_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-9	CMN_PLL0_DSM_FBL_OVRD_M0_15_9	R	0h	Reserved
8-0	CMN_PLL0_DSM_FBL_OVRD_M0_8_0	R/W	Ch	PLL feedback divider low override value : When enabled by the PLL feedback divider override enable bit in the PLL 0 delta sigma modulator diagnostics register mode 0 on page 102, the value in this field will be used to override the value on the cmnda_pll0_fb_div_low signal.

Table 12-140. Register Call Summary for CMN_PLL0_DSM_FBL_OVRD_M0

10-G SerDes Registers

- [CMN_PLL0_DSM_FBL_OVRD_M0 Register \(Offset = 12Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.47 CMN_PLL0_SS_CTRL2_M0__CMN_PLL0_SS_CTRL1_M0 Register (Offset = 130h) [reset = 2h]

CMN_PLL0_SS_CTRL2_M0__CMN_PLL0_SS_CTRL1_M0 is shown in Figure 12-47 and described in Table 12-142.

Return to [Summary Table](#).

PLL 0 spread spectrum control register 1 mode 0

Table 12-141. CMN_PLL0_SS_CTRL2_M0__CMN_PLL0_SS_CTRL1_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0130h

Figure 12-47. CMN_PLL0_SS_CTRL2_M0__CMN_PLL0_SS_CTRL1_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL0_SS_CTRL2_M0_1_5	CMN_PLL0_SS_CTRL2_M0_14_0						
R-0h	R/W-0h						
23	22	21	20	19	18	17	16
CMN_PLL0_SS_CTRL2_M0_14_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL0_SS_CTRL1_M0_15_2							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL0_SS_CTRL1_M0_15_2						CMN_PLL0_SS_CTRL1_M0_1	CMN_PLL0_SS_CTRL1_M0_0
R-0h						R/W-1h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-142. CMN_PLL0_SS_CTRL2_M0__CMN_PLL0_SS_CTRL1_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLL0_SS_CTRL2_M0_15	R	0h	Reserved
30-16	CMN_PLL0_SS_CTRL2_M0_14_0	R/W	0h	Amplitude step size: Value of the amplitude_step_size pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.
15-2	CMN_PLL0_SS_CTRL1_M0_15_2	R	0h	Reserved
1	CMN_PLL0_SS_CTRL1_M0_1	R/W	1h	Spread spectrum waveform generator disable: Setting this bit to a 1'b1 will disable the spread spectrum waveform generator.
0	CMN_PLL0_SS_CTRL1_M0_0	R/W	0h	Spread spectrum enable during VCO calibration : Setting this bit to a 1'b1 will enable the spread spectrum function while VCO calibration is taking place.

Table 12-143. Register Call Summary for CMN_PLL0_SS_CTRL2_M0__CMN_PLL0_SS_CTRL1_M0

10-G SerDes Registers

- [CMN_PLL0_SS_CTRL2_M0__CMN_PLL0_SS_CTRL1_M0 Register \(Offset = 130h\) \[reset = 2h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.48 CMN_PLL0_SS_CTRL4_M0__CMN_PLL0_SS_CTRL3_M0 Register (Offset = 134h) [reset = 0h]

CMN_PLL0_SS_CTRL4_M0__CMN_PLL0_SS_CTRL3_M0 is shown in Figure 12-48 and described in Table 12-145.

Return to [Summary Table](#).

PLL 0 spread spectrum control register 3 mode 0

Table 12-144. CMN_PLL0_SS_CTRL4_M0__CMN_PLL0_SS_CTRL3_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0134h

Figure 12-48. CMN_PLL0_SS_CTRL4_M0__CMN_PLL0_SS_CTRL3_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL0_SS_CTRL4_M0_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLL0_SS_CTRL4_M0_15_7	CMN_PLL0_SS_CTRL4_M0_6_0						
R-0h	R/W-0h						
15	14	13	12	11	10	9	8
CMN_PLL0_SS_CTRL3_M0_15_7							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL0_SS_CTRL3_M0_15_7	CMN_PLL0_SS_CTRL3_M0_6_0						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-145. CMN_PLL0_SS_CTRL4_M0__CMN_PLL0_SS_CTRL3_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_PLL0_SS_CTRL4_M0_15_7	R	0h	Reserved
22-16	CMN_PLL0_SS_CTRL4_M0_6_0	R/W	0h	Time step size: Value for the time_step_size pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.
15-7	CMN_PLL0_SS_CTRL3_M0_15_7	R	0h	Reserved
6-0	CMN_PLL0_SS_CTRL3_M0_6_0	R/W	0h	Number of steps: Value of the num_steps pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.

Table 12-146. Register Call Summary for CMN_PLL0_SS_CTRL4_M0__CMN_PLL0_SS_CTRL3_M0

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL0_SS_CTRL4_M0__CMN_PLL0_SS_CTRL3_M0 Register \(Offset = 134h\) \[reset = 0h\]: \[0\]](#)

12.49 CMN_PLL0_LOCK_REFCNT_IDLE__CMN_PLL0_LOCK_REFCNT_START Register (Offset = 138h) [reset = 000400C8h]

CMN_PLL0_LOCK_REFCNT_IDLE__CMN_PLL0_LOCK_REFCNT_START is shown in Figure 12-49 and described in Table 12-148.

Return to [Summary Table](#).

PLL 0 lock reference counter start value register

Table 12-147.
CMN_PLL0_LOCK_REFCNT_IDLE__CMN_PLL0_LOCK_REFCNT_START
Instances

Instance	Physical Address
SERDES_10G0	0505 0138h

Figure 12-49. CMN_PLL0_LOCK_REFCNT_IDLE__CMN_PLL0_LOCK_REFCNT_START Register

31	30	29	28	27	26	25	24
CMN_PLL0_LOCK_REFCNT_IDLE_15_12				CMN_PLL0_LOCK_REFCNT_IDLE_11_0			
R-0h				R/W-4h			
23	22	21	20	19	18	17	16
CMN_PLL0_LOCK_REFCNT_IDLE_11_0							
R/W-4h							
15	14	13	12	11	10	9	8
CMN_PLL0_LOCK_REFCNT_START_15_12				CMN_PLL0_LOCK_REFCNT_START_11_0			
R-0h				R/W-C8h			
7	6	5	4	3	2	1	0
CMN_PLL0_LOCK_REFCNT_START_11_0							
R/W-C8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-148. CMN_PLL0_LOCK_REFCNT_IDLE__CMN_PLL0_LOCK_REFCNT_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_PLL0_LOCK_REFCNT_IDLE_15_12	R	0h	Reserved
27-16	CMN_PLL0_LOCK_REFCNT_IDLE_11_0	R/W	4h	PLL lock reference counter idle value : This is the value used by the PLL lock detection logic to specify the number of reference clocks between each phase of counting PLL clocks.
15-12	CMN_PLL0_LOCK_REFCNT_START_15_12	R	0h	Reserved
11-0	CMN_PLL0_LOCK_REFCNT_START_11_0	R/W	C8h	PLL lock reference counter start value : This is the value that is loaded into the PLL lock detect reference counter as the starting point for that counter, when checking for PLL lock. This is set to 200 clocks by default.

Table 12-149. Register Call Summary for
CMN_PLL0_LOCK_REFCNT_IDLE__CMN_PLL0_LOCK_REFCNT_START

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL0_LOCK_REFCNT_IDLE__CMN_PLL0_LOCK_REFCNT_START Register \(Offset = 138h\) \[reset = 000400C8h\]: \[0\]](#)

12.50 CMN_PLL0_LOCK_PLLCNT_THR__CMN_PLL0_LOCK_PLLCNT_START Register (Offset = 13Ch) [reset = 000300C8h]

CMN_PLL0_LOCK_PLLCNT_THR__CMN_PLL0_LOCK_PLLCNT_START is shown in Figure 12-50 and described in Table 12-151.

Return to [Summary Table](#).

PLL 0 lock PLL counter start value register

Table 12-150.
CMN_PLL0_LOCK_PLLCNT_THR__CMN_PLL0_LOCK_PLLCNT_START
Instances

Instance	Physical Address
SERDES_10G0	0505 013Ch

Figure 12-50. CMN_PLL0_LOCK_PLLCNT_THR__CMN_PLL0_LOCK_PLLCNT_START Register

31	30	29	28	27	26	25	24
CMN_PLL0_LOCK_PLLCNT_THR_15_12				CMN_PLL0_LOCK_PLLCNT_THR_11_0			
R-0h				R/W-3h			
23	22	21	20	19	18	17	16
CMN_PLL0_LOCK_PLLCNT_THR_11_0							
R/W-3h							
15	14	13	12	11	10	9	8
CMN_PLL0_LOCK_PLLCNT_START_15_12				CMN_PLL0_LOCK_PLLCNT_START_11_0			
R-0h				R/W-C8h			
7	6	5	4	3	2	1	0
CMN_PLL0_LOCK_PLLCNT_START_11_0							
R/W-C8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-151. CMN_PLL0_LOCK_PLLCNT_THR__CMN_PLL0_LOCK_PLLCNT_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_PLL0_LOCK_PLLCNT_THR_15_12	R	0h	Reserved
27-16	CMN_PLL0_LOCK_PLLCNT_THR_11_0	R/W	3h	PLL lock counter threshold value : This is the value used by the PLL lock detection logic to determine if the PLL has locked. If the two counters in the PLL lock detection logic differ by less than this value, the PLL is considered locked. For a 100 MHz feedback divider clock, this should be set to 3. For other clock rates, this value should scale proportionally to that ratio.
15-12	CMN_PLL0_LOCK_PLLCNT_START_15_12	R	0h	Reserved
11-0	CMN_PLL0_LOCK_PLLCNT_START_11_0	R/W	C8h	PLL lock PLL counter start value : This is the value that is loaded into the PLL lock detect PLL counter as the starting point for that counter, when checking for PLL lock. When programming this register, it is important to understand how the frequency of the cmnda_pll0_fb_divider_clk is calculated relative to the reference clock. This is described in section 10.4 Dual VCO PLL on page 422.

**Table 12-152. Register Call Summary for
CMN_PLL0_LOCK_PLLCNT_THR__CMN_PLL0_LOCK_PLLCNT_START**

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL0_LOCK_PLLCNT_THR__CMN_PLL0_LOCK_PLLCNT_START Register \(Offset = 13Ch\) \[reset = 000300C8h\]: \[0\]](#)

12.51 CMN_PLL0_FRACDIVL_M1__CMN_PLL0_INTDIV_M1 Register (Offset = 140h) [reset = 0h]

CMN_PLL0_FRACDIVL_M1__CMN_PLL0_INTDIV_M1 is shown in Figure 12-51 and described in Table 12-154.

Return to [Summary Table](#).

PLL 0 feedback divider integer register mode 1

Table 12-153. CMN_PLL0_FRACDIVL_M1__CMN_PLL0_INTDIV_M1 Instances

Instance	Physical Address
SERDES_10G0	0505 0140h

Figure 12-51. CMN_PLL0_FRACDIVL_M1__CMN_PLL0_INTDIV_M1 Register

31	30	29	28	27	26	25	24
CMN_PLL0_FRACDIVL_M1_15_0							
R/W-0h							
23	22	21	20	19	18	17	16
CMN_PLL0_FRACDIVL_M1_15_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL0_INTDIV_M1_15_9							CMN_PLL0_IN TDIV_M1_8_0
R-0h							R/W-0h
7	6	5	4	3	2	1	0
CMN_PLL0_INTDIV_M1_8_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-154. CMN_PLL0_FRACDIVL_M1__CMN_PLL0_INTDIV_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMN_PLL0_FRACDIVL_M1_15_0	R/W	0h	pll_fb_div_fractional: Value of the pll_fb_div_fractional[15:0] signal.
15-9	CMN_PLL0_INTDIV_M1_15_9	R	0h	Reserved
8-0	CMN_PLL0_INTDIV_M1_8_0	R/W	0h	pll_fb_div_integer value: Value of the pll_fb_div_integer signal.

Table 12-155. Register Call Summary for CMN_PLL0_FRACDIVL_M1__CMN_PLL0_INTDIV_M1

10-G SerDes Registers

- [CMN_PLL0_FRACDIVL_M1__CMN_PLL0_INTDIV_M1 Register \(Offset = 140h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.52 CMN_PLL0_HIGH_THR_M1__CMN_PLL0_FRACDIVH_M1 Register (Offset = 144h) [reset = 0h]

CMN_PLL0_HIGH_THR_M1__CMN_PLL0_FRACDIVH_M1 is shown in Figure 12-52 and described in Table 12-157.

Return to [Summary Table](#).

PLL 0 feedback divider fractional high register mode 1

Table 12-156. CMN_PLL0_HIGH_THR_M1__CMN_PLL0_FRACDIVH_M1 Instances

Instance	Physical Address
SERDES_10G0	0505 0144h

Figure 12-52. CMN_PLL0_HIGH_THR_M1__CMN_PLL0_FRACDIVH_M1 Register

31	30	29	28	27	26	25	24
CMN_PLL0_HIGH_THR_M1_15_9							CMN_PLL0_HI GH_THR_M1_8 _0
R-0h							R/W-0h
23	22	21	20	19	18	17	16
CMN_PLL0_HIGH_THR_M1_8_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL0_FRACDIVH_M1_15_3							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL0_FRACDIVH_M1_15_3					CMN_PLL0_FRACDIVH_M1_2_0		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-157. CMN_PLL0_HIGH_THR_M1__CMN_PLL0_FRACDIVH_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	CMN_PLL0_HIGH_THR_M1_15_9	R	0h	Reserved
24-16	CMN_PLL0_HIGH_THR_M1_8_0	R/W	0h	pll_fb_div_high_theshold: Value of the pll_fb_div_high_threshold signal. The value of this register should be 2/3 the value of the combined integer and fractional divider values, and rounded up to the next even number.
15-3	CMN_PLL0_FRACDIVH_M1_15_3	R	0h	Reserved
2-0	CMN_PLL0_FRACDIVH_M1_2_0	R/W	0h	pll_fb_div_fractional: Value of the pll_fb_div_fractional[18:16] signal.

Table 12-158. Register Call Summary for CMN_PLL0_HIGH_THR_M1__CMN_PLL0_FRACDIVH_M1

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL0_HIGH_THR_M1__CMN_PLL0_FRACDIVH_M1 Register \(Offset = 144h\) \[reset = 0h\]: \[0\]](#)

12.53 CMN_PLL0_DSM_FBH_OVRD_M1__CMN_PLL0_DSM_DIAG_M1 Register (Offset = 148h) [reset = 00104004h]

CMN_PLL0_DSM_FBH_OVRD_M1__CMN_PLL0_DSM_DIAG_M1 is shown in Figure 12-53 and described in Table 12-160.

Return to [Summary Table](#).

PLL 0 delta sigma modulator diagnostics register mode 1

Table 12-159. CMN_PLL0_DSM_FBH_OVRD_M1__CMN_PLL0_DSM_DIAG_M1 Instances

Instance	Physical Address
SERDES_10G0	0505 0148h

Figure 12-53. CMN_PLL0_DSM_FBH_OVRD_M1__CMN_PLL0_DSM_DIAG_M1 Register

31	30	29	28	27	26	25	24
CMN_PLL0_DSM_FBH_OVRD_M1_15_9							CMN_PLL0_DS M_FBH_OVRD _M1_8_0
R-0h							R/W-10h
23	22	21	20	19	18	17	16
CMN_PLL0_DSM_FBH_OVRD_M1_8_0							
R/W-10h							
15	14	13	12	11	10	9	8
CMN_PLL0_DS M_DIAG_M1_1 5	CMN_PLL0_DS M_DIAG_M1_1 4	CMN_PLL0_DSM_DIAG_M1_13_4					
R/W-0h	R/W-1h	R-0h					
7	6	5	4	3	2	1	0
CMN_PLL0_DSM_DIAG_M1_13_4				CMN_PLL0_DSM_DIAG_M1_3_0			
R-0h				R/W-4h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-160. CMN_PLL0_DSM_FBH_OVRD_M1__CMN_PLL0_DSM_DIAG_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	CMN_PLL0_DSM_FBH_OVRD_M1_15_9	R	0h	Reserved
24-16	CMN_PLL0_DSM_FBH_OVRD_M1_8_0	R/W	10h	PLL feedback divider high override value : When enabled by the PLL feedback divider override enable bit in the PLL 0 delta sigma modulator diagnostics register mode 0 on page 102, the value in this field will be used to override the value on the cmnda_pll0_fb_div_high signal.
15	CMN_PLL0_DSM_DIAG_M1_15	R/W	0h	Delta sigma bypass enable: When set to 1'b1, the delta sigma modulator will be bypassed, and the output will be the value specified for the internal pll_fb_div_integer signal.
14	CMN_PLL0_DSM_DIAG_M1_14	R/W	1h	PLL feedback divider override enable : When active (1'b1), the feedback divider low and high override values in the PLL 0 delta sigma modulator feedback divider value high override register mode 0 on page 102 and PLL 0 delta sigma modulator feedback divider value low override register mode 0 on page 102 registers will be used to override the feedback divider values driven to the analog.

Table 12-160. CMN_PLL0_DSM_FBH_OVRD_M1__CMN_PLL0_DSM_DIAG_M1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-4	CMN_PLL0_DSM_DIAG_M1_13_4	R	0h	Reserved
3-0	CMN_PLL0_DSM_DIAG_M1_3_0	R/W	4h	PLL feedback divider latency adjustment: This signal specifies a value to be subtracted from the feedback divider settings before they are output on the cmnda_pll0_fb_div_high and cmnda_pll0_fb_div_low signals.

Table 12-161. Register Call Summary for CMN_PLL0_DSM_FBH_OVRD_M1__CMN_PLL0_DSM_DIAG_M1

10-G SerDes Registers

- [CMN_PLL0_DSM_FBH_OVRD_M1__CMN_PLL0_DSM_DIAG_M1 Register \(Offset = 148h\) \[reset = 00104004h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.54 CMN_PLL0_DSM_FBL_OVRD_M1 Register (Offset = 14Ch) [reset = X]

CMN_PLL0_DSM_FBL_OVRD_M1 is shown in [Figure 12-54](#) and described in [Table 12-163](#).

Return to [Summary Table](#).

PLL 0 delta sigma modulator feedback divider value low override register mode 1

Table 12-162. CMN_PLL0_DSM_FBL_OVRD_M1 Instances

Instance	Physical Address
SERDES_10G0	0505 014Ch

Figure 12-54. CMN_PLL0_DSM_FBL_OVRD_M1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_PLL0_DSM_FBL_OVRD_M1_15_9						CMN_PLL0_DS M_FBL_OVRD_ M1_8_0	
R-0h						R/W-10h	
7	6	5	4	3	2	1	0
CMN_PLL0_DSM_FBL_OVRD_M1_8_0							
R/W-10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-163. CMN_PLL0_DSM_FBL_OVRD_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-9	CMN_PLL0_DSM_FBL_OVRD_M1_15_9	R	0h	Reserved
8-0	CMN_PLL0_DSM_FBL_OVRD_M1_8_0	R/W	10h	PLL feedback divider low override value : When enabled by the PLL feedback divider override enable bit in the PLL 0 delta sigma modulator diagnostics register mode 0 on page 102, the value in this field will be used to override the value on the cmnda_pll0_fb_div_low signal.

Table 12-164. Register Call Summary for CMN_PLL0_DSM_FBL_OVRD_M1

10-G SerDes Registers
<ul style="list-style-type: none"> 10-G SerDes Registers: [0] CMN_PLL0_DSM_FBL_OVRD_M1 Register (Offset = 14Ch) [reset = X]: [0]

12.55 CMN_PLL0_SS_CTRL2_M1__CMN_PLL0_SS_CTRL1_M1 Register (Offset = 150h) [reset = 2h]

CMN_PLL0_SS_CTRL2_M1__CMN_PLL0_SS_CTRL1_M1 is shown in Figure 12-55 and described in Table 12-166.

Return to [Summary Table](#).

PLL 0 spread spectrum control register 1 mode 1

Table 12-165. CMN_PLL0_SS_CTRL2_M1__CMN_PLL0_SS_CTRL1_M1 Instances

Instance	Physical Address
SERDES_10G0	0505 0150h

Figure 12-55. CMN_PLL0_SS_CTRL2_M1__CMN_PLL0_SS_CTRL1_M1 Register

31	30	29	28	27	26	25	24
CMN_PLL0_SS_CTRL2_M1_1_5		CMN_PLL0_SS_CTRL2_M1_14_0					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
CMN_PLL0_SS_CTRL2_M1_14_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL0_SS_CTRL1_M1_15_2							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL0_SS_CTRL1_M1_15_2						CMN_PLL0_SS_CTRL1_M1_1	CMN_PLL0_SS_CTRL1_M1_0
R-0h						R/W-1h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-166. CMN_PLL0_SS_CTRL2_M1__CMN_PLL0_SS_CTRL1_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLL0_SS_CTRL2_M1_15	R	0h	Reserved
30-16	CMN_PLL0_SS_CTRL2_M1_14_0	R/W	0h	Amplitude step size: Value of the amplitude_step_size pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.
15-2	CMN_PLL0_SS_CTRL1_M1_15_2	R	0h	Reserved
1	CMN_PLL0_SS_CTRL1_M1_1	R/W	1h	Spread spectrum waveform generator disable: Setting this bit to a 1'b1 will disable the spread spectrum waveform generator.
0	CMN_PLL0_SS_CTRL1_M1_0	R/W	0h	Spread spectrum enable during VCO calibration : Setting this bit to a 1'b1 will enable the spread spectrum function while VCO calibration is taking place.

Table 12-167. Register Call Summary for CMN_PLL0_SS_CTRL2_M1__CMN_PLL0_SS_CTRL1_M1

10-G SerDes Registers

- [CMN_PLL0_SS_CTRL2_M1__CMN_PLL0_SS_CTRL1_M1 Register \(Offset = 150h\) \[reset = 2h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.56 CMN_PLL0_SS_CTRL4_M1__CMN_PLL0_SS_CTRL3_M1 Register (Offset = 154h) [reset = 0h]

CMN_PLL0_SS_CTRL4_M1__CMN_PLL0_SS_CTRL3_M1 is shown in Figure 12-56 and described in Table 12-169.

Return to [Summary Table](#).

PLL 0 spread spectrum control register 3 mode 1

Table 12-168. CMN_PLL0_SS_CTRL4_M1__CMN_PLL0_SS_CTRL3_M1 Instances

Instance	Physical Address
SERDES_10G0	0505 0154h

Figure 12-56. CMN_PLL0_SS_CTRL4_M1__CMN_PLL0_SS_CTRL3_M1 Register

31	30	29	28	27	26	25	24
CMN_PLL0_SS_CTRL4_M1_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLL0_SS_CTRL4_M1_1_5_7	CMN_PLL0_SS_CTRL4_M1_6_0						
R-0h	R/W-0h						
15	14	13	12	11	10	9	8
CMN_PLL0_SS_CTRL3_M1_15_7							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL0_SS_CTRL3_M1_1_5_7	CMN_PLL0_SS_CTRL3_M1_6_0						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-169. CMN_PLL0_SS_CTRL4_M1__CMN_PLL0_SS_CTRL3_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_PLL0_SS_CTRL4_M1_15_7	R	0h	Reserved
22-16	CMN_PLL0_SS_CTRL4_M1_6_0	R/W	0h	Time step size: Value for the time_step_size pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.
15-7	CMN_PLL0_SS_CTRL3_M1_15_7	R	0h	Reserved
6-0	CMN_PLL0_SS_CTRL3_M1_6_0	R/W	0h	Number of steps: Value of the num_steps pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.

Table 12-170. Register Call Summary for CMN_PLL0_SS_CTRL4_M1__CMN_PLL0_SS_CTRL3_M1

10-G SerDes Registers

- [CMN_PLL0_SS_CTRL4_M1__CMN_PLL0_SS_CTRL3_M1 Register \(Offset = 154h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.57 CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL Register (Offset = 180h) [reset = 20280000h]

CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL is shown in Figure 12-57 and described in Table 12-172.

Return to [Summary Table](#).

PLL 1 VCO calibration control register

Table 12-171. CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 0180h

Figure 12-57. CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL Register

31	30	29	28	27	26	25	24
CMN_PLL1_VCOCAL_START_15	CMN_PLL1_VCOCAL_START_14_12			CMN_PLL1_VCOCAL_START_11_8			
R-0h	R/W-2h			R-0h			
23	22	21	20	19	18	17	16
CMN_PLL1_VCOCAL_START_7_0							
R/W-28h							
15	14	13	12	11	10	9	8
CMN_PLL1_VCOCAL_CTRL_15	CMN_PLL1_VCOCAL_CTRL_14	CMN_PLL1_VCOCAL_CTRL_13_8					
R/W-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
CMN_PLL1_VCOCAL_CTRL_7_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-172. CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLL1_VCOCAL_START_15	R	0h	Reserved
30-28	CMN_PLL1_VCOCAL_START_14_12	R/W	2h	VCO calibration initial step size control: This field specifies the initial step size for the VCO calibration state machine. The following are the values that can be used in this field, and the corresponding step sizes. 3'b 000 : 1 3'b 001 : 2 3'b 010 : 4 3'b 011 : 8 3'b 100 : 16 3'b 101 - 3'b 111 : Reserved Note: This field is intended to be for diagnostics purposes only.
27-24	CMN_PLL1_VCOCAL_START_11_8	R	0h	Reserved

**Table 12-172. CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
23-16	CMN_PLL1_VCOCAL_START_7_0	R/W	28h	<p>VCO calibration code starting point value: This field specifies the starting VCO code that is used by the VCO calibration state machine.</p> <p>The purpose of this value is such that the VCO calibration process starts at a point that is, on average, relatively close to the final calibration point.</p> <p>This allows the calibration time to be reduced, on average.</p> <p>The encoding of this field is the same as what is described in the VCO calibration control register.</p> <p>Note: This field is intended to be for diagnostics purposes only.</p> <p>Note : This field must be set to a value that is always at least one step size away from the minimum and maximum calibration codes, and is a function of the step size specified in this register.</p> <p>For example, if the initial step size is 4, this value must be at least 4 greater than the minimum calibration code or 4 less than the maximum calibration code.</p>
15	CMN_PLL1_VCOCAL_CTRL_15	R/W	0h	<p>Start VCO calibration: Activating (1'b1) this bit will start a VCO calibration process.</p> <p>This bit must remain active until the VCO calibration process is complete (as indicated by the VCO calibration process done bit in this register).</p> <p>To start another VCO calibration process, the VCO calibration process done bit must have gone inactive from any prior calibration process.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the PLL control state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	CMN_PLL1_VCOCAL_CTRL_14	R	0h	<p>VCO calibration process done: This bit will be set to 1'b1 when the VCO calibration process is complete.</p> <p>It will be cleared by the deactivation of the Start VCO calibration bit in this register.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p>
13-8	CMN_PLL1_VCOCAL_CTRL_13_8	R	0h	Reserved

**Table 12-172. CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
7-0	CMN_PLL1_VCOCAL_CTRL_7_0	R	0h	<p>VCO calibration code: This is the calibration code that was determined by the VCO calibration process.</p> <p>This signal is valid when the VCO calibration process is complete.</p> <p>The values of this field correspond to different frequency bands the VCO will operate in.</p> <p>The frequency bands are controlled by the number of capacitors that are switched in the VCO analog circuit.</p> <p>This field specifies the number of capacitors that are switched in.</p> <p>The following are the values for this code:</p> <p>8'b 00000000: 0 Capacitors activated</p> <p>8'b 00000001: 1 Capacitor activated</p> <p>8'b 00000010: 2 Capacitors activated</p> <p>8'b 00000011: 3 Capacitors activated</p> <p>...</p> <p>8'b 11111110: 254 Capacitors activated</p> <p>8'b 11111111: 255 Capacitors activated</p> <p>Note: This register is intended to be for diagnostics purposes only.</p> <p>Note: The reset value for this field is with the PLL controller power island switched off.</p> <p>In cases where this power island is switched on, the reset value be 8'h28.</p>

Table 12-173. Register Call Summary for CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL

10-G SerDes Registers

- [CMN_PLL1_VCOCAL_START__CMN_PLL1_VCOCAL_CTRL Register \(Offset = 180h\) \[reset = 20280000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.58 CMN_PLL1_VCOCAL_OVRD__CMN_PLL1_VCOCAL_TCTRL Register (Offset = 184h) [reset = 4h]

CMN_PLL1_VCOCAL_OVRD__CMN_PLL1_VCOCAL_TCTRL is shown in Figure 12-58 and described in Table 12-175.

Return to [Summary Table](#).

PLL 1 VCO calibration timer control register

Table 12-174. CMN_PLL1_VCOCAL_OVRD__CMN_PLL1_VCOCAL_TCTRL Instances

Instance	Physical Address
SERDES_10G0	0505 0184h

Figure 12-58. CMN_PLL1_VCOCAL_OVRD__CMN_PLL1_VCOCAL_TCTRL Register

31	30	29	28	27	26	25	24
CMN_PLL1_VCOCAL_OVRD_15	CMN_PLL1_VCOCAL_OVRD_14_8						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
CMN_PLL1_VCOCAL_OVRD_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL1_VCOCAL_TCTRL_15_3							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL1_VCOCAL_TCTRL_15_3					CMN_PLL1_VCOCAL_TCTRL_2_0		
R-0h					R/W-4h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-175. CMN_PLL1_VCOCAL_OVRD__CMN_PLL1_VCOCAL_TCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLL1_VCOCAL_OVRD_15	R/W	0h	VCO calibration code override enable: Activating (1'b1) this bit allows the VCO code determined during the automatic VCO calibration process to be overridden by the value driven by the VCO calibration code override value field in this register. Note: This bit is intended to be for diagnostics purposes only. Note: This bit should not be activated while a calibration is currently in progress.
30-24	CMN_PLL1_VCOCAL_OVRD_14_8	R	0h	Reserved
23-16	CMN_PLL1_VCOCAL_OVRD_7_0	R/W	0h	VCO calibration code override value: This field is used to override the VCO code determined during the automatic VCO calibration process. The VCO code driven on this field is valid when the VCO calibration code override enable bit in this register is active. The encoding of this field is the same as what is described in the VCO calibration control register. Note: This field is intended to be for diagnostics purposes only.
15-3	CMN_PLL1_VCOCAL_TCTRL_15_3	R	0h	Reserved

**Table 12-175. CMN_PLL1_VCOCAL_OVRD__CMN_PLL1_VCOCAL_TCTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2-0	CMN_PLL1_VCOCAL_TCTRL_2_0	R/W	4h	<p>VCO calibration initial time scale control: This field specifies the calibration start time scaling factor applied to the VCO calibration when running the initial step size for the calibration code if not set to 1.</p> <p>Setting this value to a value other than 1 will reduce the calibration measurement time by the amount specified below.</p> <p>Then when the final calibration steps are made the full calibration time will be used to get the appropriate amount of resolution.</p> <p>3'b 000 : Div 1 3'b 001 : Div 2 3'b 010 : Div 4 3'b 011 : Div 8 3'b 100 : Div 16 3'b 101 : Div 32 3'b 110 : Div 64 3'b 111 : Div 128</p>

Table 12-176. Register Call Summary for CMN_PLL1_VCOCAL_OVRD__CMN_PLL1_VCOCAL_TCTRL

10-G SerDes Registers

- [CMN_PLL1_VCOCAL_OVRD__CMN_PLL1_VCOCAL_TCTRL Register \(Offset = 184h\) \[reset = 4h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.59 CMN_PLL1_VCOCAL_ITER_TMR__CMN_PLL1_VCOCAL_INIT_TMR Register (Offset = 188h) [reset = 001003E8h]

CMN_PLL1_VCOCAL_ITER_TMR__CMN_PLL1_VCOCAL_INIT_TMR is shown in Figure 12-59 and described in Table 12-178.

Return to [Summary Table](#).

PLL 1 VCO calibration initialization timer register

Table 12-177.

CMN_PLL1_VCOCAL_ITER_TMR__CMN_PLL1_VCOCAL_INIT_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0188h

Figure 12-59. CMN_PLL1_VCOCAL_ITER_TMR__CMN_PLL1_VCOCAL_INIT_TMR Register

31	30	29	28	27	26	25	24
CMN_PLL1_VCOCAL_ITER_TMR_15_14		CMN_PLL1_VCOCAL_ITER_TMR_13_0					
R-0h		R/W-10h					
23	22	21	20	19	18	17	16
CMN_PLL1_VCOCAL_ITER_TMR_13_0							
R/W-10h							
15	14	13	12	11	10	9	8
CMN_PLL1_VCOCAL_INIT_TMR_15_14		CMN_PLL1_VCOCAL_INIT_TMR_13_0					
R-0h		R/W-3E8h					
7	6	5	4	3	2	1	0
CMN_PLL1_VCOCAL_INIT_TMR_13_0							
R/W-3E8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-178. CMN_PLL1_VCOCAL_ITER_TMR__CMN_PLL1_VCOCAL_INIT_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	CMN_PLL1_VCOCAL_ITER_TMR_15_14	R	0h	Reserved
29-16	CMN_PLL1_VCOCAL_ITER_TMR_13_0	R/W	10h	Iteration wait timer value: This is the number of clocks to wait between when a calibration code is driven to the analog, and when the clock rates are measured.
15-14	CMN_PLL1_VCOCAL_INIT_TMR_15_14	R	0h	Reserved
13-0	CMN_PLL1_VCOCAL_INIT_TMR_13_0	R/W	3E8h	Initialization wait timer value: This is the number of clocks to wait between when the analog VCO calibration circuits are enabled, and when the first calibration code is driven to the analog. Note that the reset value for this field corresponds to a time of 10 uSec.

Table 12-179. Register Call Summary for CMN_PLL1_VCOCAL_ITER_TMR__CMN_PLL1_VCOCAL_INIT_TMR

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL1_VCOCAL_ITER_TMR__CMN_PLL1_VCOCAL_INIT_TMR Register \(Offset = 188h\) \[reset = 001003E8h\]: \[0\]](#)

12.60 CMN_PLL1_VCOCAL_REFTIM_START Register (Offset = 18Ch) [reset = X]

CMN_PLL1_VCOCAL_REFTIM_START is shown in Figure 12-60 and described in Table 12-181.

Return to [Summary Table](#).

PLL 1 VCO calibration reference clock timer start value register

Table 12-180. CMN_PLL1_VCOCAL_REFTIM_START Instances

Instance	Physical Address
SERDES_10G0	0505 018Ch

Figure 12-60. CMN_PLL1_VCOCAL_REFTIM_START Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_PLL1_VCOCAL_REFTIM_START_15_14		CMN_PLL1_VCOCAL_REFTIM_START_13_0					
R-0h		R/W-C5Fh					
7	6	5	4	3	2	1	0
CMN_PLL1_VCOCAL_REFTIM_START_13_0							
R/W-C5Fh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-181. CMN_PLL1_VCOCAL_REFTIM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	CMN_PLL1_VCOCAL_REFTIM_START_15_14	R	0h	Reserved
13-0	CMN_PLL1_VCOCAL_REFTIM_START_13_0	R/W	C5Fh	PLL VCO calibration reference clock timer start value : This is the value that is loaded into the reference clock timer as the starting point for that timer, when running VCO calibration. The value in this field must correspond to a time that is approximately one full spread spectrum cycle long (31.67 uSec) Note that the actual number of clocks counted is one larger than what is specified by this field.

Table 12-182. Register Call Summary for CMN_PLL1_VCOCAL_REFTIM_START

10-G SerDes Registers

- [CMN_PLL1_VCOCAL_REFTIM_START Register \(Offset = 18Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.61 CMN_PLL1_VCOCAL_PLLCNT_START Register (Offset = 190h) [reset = X]

CMN_PLL1_VCOCAL_PLLCNT_START is shown in Figure 12-61 and described in Table 12-184.

Return to [Summary Table](#).

PLL 1 VCO calibration PLL clock counter start value register

Table 12-183. CMN_PLL1_VCOCAL_PLLCNT_START Instances

Instance	Physical Address
SERDES_10G0	0505 0190h

Figure 12-61. CMN_PLL1_VCOCAL_PLLCNT_START Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_PLL1_VCOCAL_PLLCNT_START_15_14		CMN_PLL1_VCOCAL_PLLCNT_START_13_0					
R-0h		R/W-C5Fh					
7	6	5	4	3	2	1	0
CMN_PLL1_VCOCAL_PLLCNT_START_13_0							
R/W-C5Fh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-184. CMN_PLL1_VCOCAL_PLLCNT_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-14	CMN_PLL1_VCOCAL_PL LCNT_START_15_14	R	0h	Reserved
13-0	CMN_PLL1_VCOCAL_PL LCNT_START_13_0	R/W	C5Fh	PLL VCO calibration PLL clock counter start value : This is the value that is loaded into the PLL clock counter as the starting point for that counter, when running VCO calibration. When programming this register, it is important to understand how the frequency of the cmnda_pll1_fb_divider_clk is calculated relative to the reference clock. Note that the actual number of clocks counted is one larger than what is specified by this field.

Table 12-185. Register Call Summary for CMN_PLL1_VCOCAL_PLLCNT_START

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL1_VCOCAL_PLLCNT_START Register \(Offset = 190h\) \[reset = X\]: \[0\]](#)

12.62 CMN_PLL1_FRACDIVL_M0__CMN_PLL1_INTDIV_M0 Register (Offset = 1A0h) [reset = 0h]

CMN_PLL1_FRACDIVL_M0__CMN_PLL1_INTDIV_M0 is shown in [Figure 12-62](#) and described in [Table 12-187](#).

Return to [Summary Table](#).

PLL 1 feedback divider integer register mode 0

Table 12-186. CMN_PLL1_FRACDIVL_M0__CMN_PLL1_INTDIV_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 01A0h

Figure 12-62. CMN_PLL1_FRACDIVL_M0__CMN_PLL1_INTDIV_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL1_FRACDIVL_M0_15_0							
R/W-0h							
23	22	21	20	19	18	17	16
CMN_PLL1_FRACDIVL_M0_15_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL1_INTDIV_M0_15_9							CMN_PLL1_IN TDIV_M0_8_0
R-0h							R/W-0h
7	6	5	4	3	2	1	0
CMN_PLL1_INTDIV_M0_8_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-187. CMN_PLL1_FRACDIVL_M0__CMN_PLL1_INTDIV_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CMN_PLL1_FRACDIVL_M0_15_0	R/W	0h	pll_fb_div_fractional: Value of the pll_fb_div_fractional[15:0] signal.
15-9	CMN_PLL1_INTDIV_M0_15_9	R	0h	Reserved
8-0	CMN_PLL1_INTDIV_M0_8_0	R/W	0h	pll_fb_div_integer value: Value of the pll_fb_div_integer signal.

Table 12-188. Register Call Summary for CMN_PLL1_FRACDIVL_M0__CMN_PLL1_INTDIV_M0

10-G SerDes Registers

- [CMN_PLL1_FRACDIVL_M0__CMN_PLL1_INTDIV_M0 Register \(Offset = 1A0h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.63 CMN_PLL1_HIGH_THR_M0__CMN_PLL1_FRACDIVH_M0 Register (Offset = 1A4h) [reset = 0h]

CMN_PLL1_HIGH_THR_M0__CMN_PLL1_FRACDIVH_M0 is shown in Figure 12-63 and described in Table 12-190.

Return to [Summary Table](#).

PLL 1 feedback divider fractional high register mode 0

Table 12-189. CMN_PLL1_HIGH_THR_M0__CMN_PLL1_FRACDIVH_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 01A4h

Figure 12-63. CMN_PLL1_HIGH_THR_M0__CMN_PLL1_FRACDIVH_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL1_HIGH_THR_M0_15_9							CMN_PLL1_HI GH_THR_M0_8 _0
R-0h							R/W-0h
23	22	21	20	19	18	17	16
CMN_PLL1_HIGH_THR_M0_8_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL1_FRACDIVH_M0_15_3							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL1_FRACDIVH_M0_15_3					CMN_PLL1_FRACDIVH_M0_2_0		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-190. CMN_PLL1_HIGH_THR_M0__CMN_PLL1_FRACDIVH_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	CMN_PLL1_HIGH_THR_M0_15_9	R	0h	Reserved
24-16	CMN_PLL1_HIGH_THR_M0_8_0	R/W	0h	pll_fb_div_high_theshold: Value of the pll_fb_div_high_threshold signal. The value of this register should be 2/3 the value of the combined integer and fractional divider values, and rounded up to the next even number.
15-3	CMN_PLL1_FRACDIVH_M0_15_3	R	0h	Reserved
2-0	CMN_PLL1_FRACDIVH_M0_2_0	R/W	0h	pll_fb_div_fractional: Value of the pll_fb_div_fractional[18:16] signal.

Table 12-191. Register Call Summary for CMN_PLL1_HIGH_THR_M0__CMN_PLL1_FRACDIVH_M0

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL1_HIGH_THR_M0__CMN_PLL1_FRACDIVH_M0 Register \(Offset = 1A4h\) \[reset = 0h\]: \[0\]](#)

12.64 CMN_PLL1_DSM_FBH_OVRD_M0__CMN_PLL1_DSM_DIAG_M0 Register (Offset = 1A8h) [reset = 00104004h]

CMN_PLL1_DSM_FBH_OVRD_M0__CMN_PLL1_DSM_DIAG_M0 is shown in Figure 12-64 and described in Table 12-193.

Return to [Summary Table](#).

PLL 1 delta sigma modulator diagnostics register mode 0

Table 12-192. CMN_PLL1_DSM_FBH_OVRD_M0__CMN_PLL1_DSM_DIAG_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 01A8h

Figure 12-64. CMN_PLL1_DSM_FBH_OVRD_M0__CMN_PLL1_DSM_DIAG_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL1_DSM_FBH_OVRD_M0_15_9							CMN_PLL1_DS M_FBH_OVRD _M0_8_0
R-0h							R/W-10h
23	22	21	20	19	18	17	16
CMN_PLL1_DSM_FBH_OVRD_M0_8_0							
R/W-10h							
15	14	13	12	11	10	9	8
CMN_PLL1_DS M_DIAG_M0_1 5	CMN_PLL1_DS M_DIAG_M0_1 4	CMN_PLL1_DSM_DIAG_M0_13_4					
R/W-0h	R/W-1h	R-0h					
7	6	5	4	3	2	1	0
CMN_PLL1_DSM_DIAG_M0_13_4				CMN_PLL1_DSM_DIAG_M0_3_0			
R-0h				R/W-4h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-193. CMN_PLL1_DSM_FBH_OVRD_M0__CMN_PLL1_DSM_DIAG_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	CMN_PLL1_DSM_FBH_OVRD_M0_15_9	R	0h	Reserved
24-16	CMN_PLL1_DSM_FBH_OVRD_M0_8_0	R/W	10h	PLL feedback divider high override value : When enabled by the PLL feedback divider override enable bit in the PLL 1 delta sigma modulator diagnostics register mode 0 on page 111, the value in this field will be used to override the value on the cmnda_pll1_fb_div_high signal.
15	CMN_PLL1_DSM_DIAG_M0_15	R/W	0h	Delta sigma bypass enable: When set to 1'b1, the delta sigma modulator will be bypassed, and the output will be the value specified for the internal pll_fb_div_integer signal.
14	CMN_PLL1_DSM_DIAG_M0_14	R/W	1h	PLL feedback divider override enable : When active (1'b1), the feedback divider low and high override values in the PLL 1 delta sigma modulator feedback divider value high override register mode 0 on page 111 and PLL 1 delta sigma modulator feedback divider value low override register mode 0 on page 111 registers will be used to override the feedback divider values driven to the analog.

Table 12-193. CMN_PLL1_DSM_FBH_OVRD_M0__CMN_PLL1_DSM_DIAG_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-4	CMN_PLL1_DSM_DIAG_M0_13_4	R	0h	Reserved
3-0	CMN_PLL1_DSM_DIAG_M0_3_0	R/W	4h	PLL feedback divider latency adjustment: This signal specifies a value to be subtracted from the feedback divider settings before they are output on the cmnda_pll1_fb_div_high and cmnda_pll1_fb_div_low signals.

Table 12-194. Register Call Summary for CMN_PLL1_DSM_FBH_OVRD_M0__CMN_PLL1_DSM_DIAG_M0

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL1_DSM_FBH_OVRD_M0__CMN_PLL1_DSM_DIAG_M0 Register \(Offset = 1A8h\) \[reset = 00104004h\]: \[0\]](#)

12.65 CMN_PLL1_DSM_FBL_OVRD_M0 Register (Offset = 1ACh) [reset = X]

CMN_PLL1_DSM_FBL_OVRD_M0 is shown in [Figure 12-65](#) and described in [Table 12-196](#).

Return to [Summary Table](#).

PLL 1 delta sigma modulator feedback divider value low override register mode 0

**Table 12-195. CMN_PLL1_DSM_FBL_OVRD_M0
Instances**

Instance	Physical Address
SERDES_10G0	0505 01ACh

Figure 12-65. CMN_PLL1_DSM_FBL_OVRD_M0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_PLL1_DSM_FBL_OVRD_M0_15_9						CMN_PLL1_DS M_FBL_OVRD_ M0_8_0	
R-0h						R/W-10h	
7	6	5	4	3	2	1	0
CMN_PLL1_DSM_FBL_OVRD_M0_8_0							
R/W-10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-196. CMN_PLL1_DSM_FBL_OVRD_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-9	CMN_PLL1_DSM_FBL_OVRD_M0_15_9	R	0h	Reserved
8-0	CMN_PLL1_DSM_FBL_OVRD_M0_8_0	R/W	10h	PLL feedback divider low override value : When enabled by the PLL feedback divider override enable bit in the PLL 1 delta sigma modulator diagnostics register mode 0 on page 111, the value in this field will be used to override the value on the cmnda_pll1_fb_div_low signal.

Table 12-197. Register Call Summary for CMN_PLL1_DSM_FBL_OVRD_M0

10-G SerDes Registers

- [CMN_PLL1_DSM_FBL_OVRD_M0 Register \(Offset = 1ACh\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.66 CMN_PLL1_SS_CTRL2_M0__CMN_PLL1_SS_CTRL1_M0 Register (Offset = 1B0h) [reset = 2h]

CMN_PLL1_SS_CTRL2_M0__CMN_PLL1_SS_CTRL1_M0 is shown in Figure 12-66 and described in Table 12-199.

Return to [Summary Table](#).

PLL 1 spread spectrum control register 1 mode 0

Table 12-198. CMN_PLL1_SS_CTRL2_M0__CMN_PLL1_SS_CTRL1_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 01B0h

Figure 12-66. CMN_PLL1_SS_CTRL2_M0__CMN_PLL1_SS_CTRL1_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL1_SS_CTRL2_M0_1_5	CMN_PLL1_SS_CTRL2_M0_14_0						
R-0h	R/W-0h						
23	22	21	20	19	18	17	16
CMN_PLL1_SS_CTRL2_M0_14_0							
R/W-0h							
15	14	13	12	11	10	9	8
CMN_PLL1_SS_CTRL1_M0_15_2							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL1_SS_CTRL1_M0_15_2						CMN_PLL1_SS_CTRL1_M0_1	CMN_PLL1_SS_CTRL1_M0_0
R-0h						R/W-1h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-199. CMN_PLL1_SS_CTRL2_M0__CMN_PLL1_SS_CTRL1_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PLL1_SS_CTRL2_M0_15	R	0h	Reserved
30-16	CMN_PLL1_SS_CTRL2_M0_14_0	R/W	0h	Amplitude step size: Value of the amplitude_step_size pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.
15-2	CMN_PLL1_SS_CTRL1_M0_15_2	R	0h	Reserved
1	CMN_PLL1_SS_CTRL1_M0_1	R/W	1h	Spread spectrum waveform generator disable: Setting this bit to a 1'b1 will disable the spread spectrum waveform generator.
0	CMN_PLL1_SS_CTRL1_M0_0	R/W	0h	Spread spectrum enable during VCO calibration : Setting this bit to a 1'b1 will enable the spread spectrum function while VCO calibration is taking place.

Table 12-200. Register Call Summary for CMN_PLL1_SS_CTRL2_M0__CMN_PLL1_SS_CTRL1_M0

10-G SerDes Registers

- [CMN_PLL1_SS_CTRL2_M0__CMN_PLL1_SS_CTRL1_M0 Register \(Offset = 1B0h\) \[reset = 2h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.67 CMN_PLL1_SS_CTRL4_M0__CMN_PLL1_SS_CTRL3_M0 Register (Offset = 1B4h) [reset = 0h]

CMN_PLL1_SS_CTRL4_M0__CMN_PLL1_SS_CTRL3_M0 is shown in Figure 12-67 and described in Table 12-202.

Return to [Summary Table](#).

PLL 1 spread spectrum control register 3 mode 0

Table 12-201. CMN_PLL1_SS_CTRL4_M0__CMN_PLL1_SS_CTRL3_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 01B4h

Figure 12-67. CMN_PLL1_SS_CTRL4_M0__CMN_PLL1_SS_CTRL3_M0 Register

31	30	29	28	27	26	25	24
CMN_PLL1_SS_CTRL4_M0_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_PLL1_SS_CTRL4_M0_15_7	CMN_PLL1_SS_CTRL4_M0_6_0						
R-0h	R/W-0h						
15	14	13	12	11	10	9	8
CMN_PLL1_SS_CTRL3_M0_15_7							
R-0h							
7	6	5	4	3	2	1	0
CMN_PLL1_SS_CTRL3_M0_15_7	CMN_PLL1_SS_CTRL3_M0_6_0						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-202. CMN_PLL1_SS_CTRL4_M0__CMN_PLL1_SS_CTRL3_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_PLL1_SS_CTRL4_M0_15_7	R	0h	Reserved
22-16	CMN_PLL1_SS_CTRL4_M0_6_0	R/W	0h	Time step size: Value for the time_step_size pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.
15-7	CMN_PLL1_SS_CTRL3_M0_15_7	R	0h	Reserved
6-0	CMN_PLL1_SS_CTRL3_M0_6_0	R/W	0h	Number of steps: Value of the num_steps pin on the spread spectrum waveform generator. Note that this field should not be set to 0 when spread spectrum is enabled.

Table 12-203. Register Call Summary for CMN_PLL1_SS_CTRL4_M0__CMN_PLL1_SS_CTRL3_M0

10-G SerDes Registers

- [CMN_PLL1_SS_CTRL4_M0__CMN_PLL1_SS_CTRL3_M0 Register \(Offset = 1B4h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.68 CMN_PLL1_LOCK_REFCNT_IDLE__CMN_PLL1_LOCK_REFCNT_START Register (Offset = 1B8h) [reset = 000400C8h]

CMN_PLL1_LOCK_REFCNT_IDLE__CMN_PLL1_LOCK_REFCNT_START is shown in Figure 12-68 and described in Table 12-205.

Return to [Summary Table](#).

PLL 1 lock reference counter start value register

Table 12-204.
CMN_PLL1_LOCK_REFCNT_IDLE__CMN_PLL1_LOCK_REFCNT_START
Instances

Instance	Physical Address
SERDES_10G0	0505 01B8h

Figure 12-68. CMN_PLL1_LOCK_REFCNT_IDLE__CMN_PLL1_LOCK_REFCNT_START Register

31	30	29	28	27	26	25	24
CMN_PLL1_LOCK_REFCNT_IDLE_15_12				CMN_PLL1_LOCK_REFCNT_IDLE_11_0			
R-0h				R/W-4h			
23	22	21	20	19	18	17	16
CMN_PLL1_LOCK_REFCNT_IDLE_11_0							
R/W-4h							
15	14	13	12	11	10	9	8
CMN_PLL1_LOCK_REFCNT_START_15_12				CMN_PLL1_LOCK_REFCNT_START_11_0			
R-0h				R/W-C8h			
7	6	5	4	3	2	1	0
CMN_PLL1_LOCK_REFCNT_START_11_0							
R/W-C8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-205. CMN_PLL1_LOCK_REFCNT_IDLE__CMN_PLL1_LOCK_REFCNT_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_PLL1_LOCK_REFCNT_IDLE_15_12	R	0h	Reserved
27-16	CMN_PLL1_LOCK_REFCNT_IDLE_11_0	R/W	4h	PLL lock reference counter idle value : This is the value used by the PLL lock detection logic to specify the number of reference clocks between each phase of counting PLL clocks.
15-12	CMN_PLL1_LOCK_REFCNT_START_15_12	R	0h	Reserved
11-0	CMN_PLL1_LOCK_REFCNT_START_11_0	R/W	C8h	PLL lock reference counter start value : This is the value that is loaded into the PLL lock detect reference counter as the starting point for that counter, when checking for PLL lock. This register is provided for simulation speedup and diagnostic purposes only.

Table 12-206. Register Call Summary for
CMN_PLL1_LOCK_REFCNT_IDLE__CMN_PLL1_LOCK_REFCNT_START

10-G SerDes Registers

- [CMN_PLL1_LOCK_REFCNT_IDLE__CMN_PLL1_LOCK_REFCNT_START Register \(Offset = 1B8h\) \[reset = 000400C8h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.69 CMN_PLL1_LOCK_PLLCNT_THR__CMN_PLL1_LOCK_PLLCNT_START Register (Offset = 1BCh) [reset = 000300C8h]

CMN_PLL1_LOCK_PLLCNT_THR__CMN_PLL1_LOCK_PLLCNT_START is shown in Figure 12-69 and described in Table 12-208.

Return to [Summary Table](#).

PLL 1 lock PLL counter start value register

Table 12-207.
CMN_PLL1_LOCK_PLLCNT_THR__CMN_PLL1_LOCK_PLLCNT_START
Instances

Instance	Physical Address
SERDES_10G0	0505 01BCh

Figure 12-69. CMN_PLL1_LOCK_PLLCNT_THR__CMN_PLL1_LOCK_PLLCNT_START Register

31	30	29	28	27	26	25	24
CMN_PLL1_LOCK_PLLCNT_THR_15_12				CMN_PLL1_LOCK_PLLCNT_THR_11_0			
R-0h				R/W-3h			
23	22	21	20	19	18	17	16
CMN_PLL1_LOCK_PLLCNT_THR_11_0							
R/W-3h							
15	14	13	12	11	10	9	8
CMN_PLL1_LOCK_PLLCNT_START_15_12				CMN_PLL1_LOCK_PLLCNT_START_11_0			
R-0h				R/W-C8h			
7	6	5	4	3	2	1	0
CMN_PLL1_LOCK_PLLCNT_START_11_0							
R/W-C8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-208. CMN_PLL1_LOCK_PLLCNT_THR__CMN_PLL1_LOCK_PLLCNT_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_PLL1_LOCK_PLLCNT_THR_15_12	R	0h	Reserved
27-16	CMN_PLL1_LOCK_PLLCNT_THR_11_0	R/W	3h	PLL lock counter threshold value : This is the value used by the PLL lock detection logic to determine if the PLL has locked. If the two counters in the PLL lock detection logic differ by less than this value, the PLL is considered locked. For a 100 MHz feedback divider clock, this should be set to 3. For other clock rates, this value should scale proportionally to that ratio.
15-12	CMN_PLL1_LOCK_PLLCNT_START_15_12	R	0h	Reserved
11-0	CMN_PLL1_LOCK_PLLCNT_START_11_0	R/W	C8h	PLL lock PLL counter start value : This is the value that is loaded into the PLL lock detect PLL counter as the starting point for that counter, when checking for PLL lock. When programming this register, it is important to understand how the frequency of the cmnda_pll1_fb_divider_clk is calculated relative to the reference clock. This is described in section 10.4 Dual VCO PLL on page 422.

**Table 12-209. Register Call Summary for
CMN_PLL1_LOCK_PLLCNT_THR__CMN_PLL1_LOCK_PLLCNT_START**

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PLL1_LOCK_PLLCNT_THR__CMN_PLL1_LOCK_PLLCNT_START Register \(Offset = 1BCh\) \[reset = 000300C8h\]: \[0\]](#)

12.70 CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL Register (Offset = 200h) [reset = 0h]

CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL is shown in Figure 12-70 and described in Table 12-211.

Return to [Summary Table](#).

TX pull-up resistor calibration control register

Table 12-210.
CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 0200h

Figure 12-70. CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL Register

31	30	29	28	27	26	25	24
CMN_TXPUCAL_OVRD_15	CMN_TXPUCAL_OVRD_14	CMN_TXPUCAL_OVRD_13_7					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
CMN_TXPUCAL_OVRD_13_7	CMN_TXPUCAL_OVRD_6_0						
R-0h	R/W-0h						
15	14	13	12	11	10	9	8
CMN_TXPUCAL_CTRL_15	CMN_TXPUCAL_CTRL_14	CMN_TXPUCAL_CTRL_13	CMN_TXPUCAL_CTRL_12	CMN_TXPUCAL_CTRL_11_7			
R/W-0h	R-0h	R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
CMN_TXPUCAL_CTRL_11_7	CMN_TXPUCAL_CTRL_6_0						
R-0h	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-211. CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_TXPUCAL_OVRD_15	R/W	0h	Resistor code override enable: Activation (1'b1) of this register bit allows the resistor codes determined during the automatic resistor calibration process to be overridden. The override value is specified using the resistor code override value field of this register.
30	CMN_TXPUCAL_OVRD_14	R/W	0h	Analog calibration enable override: Activation (1'b1) of this register bit will force the analog calibration circuits to be enabled by activating the cmnda_rescal_en_tx_useg enable and the cmnda_rescal_clk_tx_useg clock.
29-23	CMN_TXPUCAL_OVRD_13_7	R	0h	Reserved

Table 12-211. CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-16	CMN_TXPUCAL_OVRD_6_0	R/W	0h	<p>Resistor code override value: These bits are used to override the resistor code determined during the automatic resistor calibration process.</p> <p>The resistor code written to these bits is valid when the resistor code override enable bit in this register is active.</p> <p>The following are the values for the code.</p> <p>7'b 0000000: No resistors active.</p> <p>7'b 0000001: 1 resistor active.</p> <p>7'b 0000010: 2 resistors active.</p> <p>7'b 0000011: 3 resistors active.</p> <p>7'b 0000100: 4 resistors active.</p> <p>...</p> <p>7'b 0111100: 60 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>
15	CMN_TXPUCAL_CTRL_15	R/W	0h	<p>Start resistor calibration: Activating (1'b1) this bit will start the resistor calibration process.</p> <p>This signal must remain active until the resistor calibration process is complete.</p> <p>To start another resistor calibration process, this register must first be set inactive (1'b0) until the resistor calibration process done bit in this register is cleared.</p> <p>Note: This signal is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the startup state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	CMN_TXPUCAL_CTRL_14	R	0h	<p>Resistor calibration process done: This bit will be set to 1'b1 when the resistor calibration process is complete.</p> <p>It will be cleared by cmn_reset_n, or by the deactivation of the start resistor calibration bit in this register after calibration is complete.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p> <p>Note: Three cmn_ref_clk cycles are required after the start of the resistor calibration process to clear this signal.</p>

Table 12-211. CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CMN_TXPUCAL_CTRL_1_3	R	0h	<p>No analog calibration response : This signal indicates that the calibration function has gone through the entire calibration process, reached the final calibration value, and the analog has not responded indicating that a valid calibration value has been reached. Note: Due to the nature of the calibration process, it is not possible to determine if the analog responded or not for the lowest code of 7'b00000000.</p> <p>The reason for this is, when sequencing to lower codes, the calibration function is looking for the analog response to transition from 1'b1 to 1'b0.</p> <p>If the lowest calibration code is the correct code, the analog will respond with 1'b1, and the algorithm can't sequence to a lower code to look for the transition from 1'b1 to 1'b0.</p> <p>Similarly, if the analog is not responding, it is not possible to sequence to a lower code to detect this.</p> <p>Therefore, even when the calibration function selects this calibration code as valid, this bit will be set.</p>
12	CMN_TXPUCAL_CTRL_1_2	R	0h	<p>Current analog comparator response: This is the current state of the analog comparator response signal (cmnda_rescal_comp_tx_useg). This signal is not synchronized, and is provided for diagnostic purposes only.</p>
11-7	CMN_TXPUCAL_CTRL_1_1_7	R	0h	Reserved
6-0	CMN_TXPUCAL_CTRL_6_0	R	0h	<p>Resistor calibration code: This is the calibration code that was determined by the resistor calibration process.</p> <p>The following are the values for the code.</p> <p>7'b 0000000: No resistors active.</p> <p>7'b 0000001: 1 resistor active.</p> <p>7'b 0000010: 2 resistors active.</p> <p>7'b 0000011: 3 resistors active.</p> <p>7'b 0000100: 4 resistors active.</p> <p>...</p> <p>7'b 0111100: 60 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p> <p>Note: The reset value for this field is with the common calibration power island switched off.</p> <p>In cases where this power island is switched on, the reset value be 7'b0101101.</p>

Table 12-212. Register Call Summary for CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL

10-G SerDes Registers

- [CMN_TXPUCAL_OVRD__CMN_TXPUCAL_CTRL Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.71 CMN_TXPUCAL_TUNE__CMN_TXPUCAL_START Register (Offset = 204h) [reset = 2Dh]

CMN_TXPUCAL_TUNE__CMN_TXPUCAL_START is shown in Figure 12-71 and described in Table 12-214.

Return to [Summary Table](#).

TX pull-up resistor calibration start register

Table 12-213.
CMN_TXPUCAL_TUNE__CMN_TXPUCAL_START
Instances

Instance	Physical Address
SERDES_10G0	0505 0204h

Figure 12-71. CMN_TXPUCAL_TUNE__CMN_TXPUCAL_START Register

31	30	29	28	27	26	25	24
CMN_TXPUCAL_TUNE_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_TXPUCAL_TUNE_15_7	CMN_TXPUCAL_TUNE_6_0						
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CMN_TXPUCAL_START_15	CMN_TXPUCAL_START_14_7						
R/W-0h				R-0h			
7	6	5	4	3	2	1	0
CMN_TXPUCAL_START_14_7	CMN_TXPUCAL_START_6_0						
R-0h				R/W-2Dh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-214. CMN_TXPUCAL_TUNE__CMN_TXPUCAL_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_TXPUCAL_TUNE_15_7	R	0h	Reserved
22-16	CMN_TXPUCAL_TUNE_6_0	R/W	0h	Resistor calibration tune value: The value of this field is added to the automatically calibrated code, or the override code if override is enabled. Note that this value is a twos complement value, so the calibrated code can be increased or decreased.
15	CMN_TXPUCAL_START_15	R/W	0h	Resistor calibration direction: This controls the direction that the automatic calibration process steps the calibration codes in. 1'b 0 : From 7'b00000000 to 7'b0111100. 1'b 1 : From 7'b0111100 to 7'b00000000.
14-7	CMN_TXPUCAL_START_14_7	R	0h	Reserved

Table 12-214. CMN_TXPUCAL_TUNE__CMN_TXPUCAL_START Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	CMN_TXPUCAL_START_6_0	R/W	2Dh	<p>Start resistor calibration code: This is the calibration code that the resistor calibration process starts with when automatic calibration is run.</p> <p>The following are the values for the code.</p> <p>7'b 0000000: No resistors active.</p> <p>7'b 0000001: 1 resistor active.</p> <p>7'b 0000010: 2 resistors active.</p> <p>7'b 0000011: 3 resistors active.</p> <p>7'b 0000100: 4 resistors active.</p> <p>...</p> <p>7'b 0111100: 60 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>

Table 12-215. Register Call Summary for CMN_TXPUCAL_TUNE__CMN_TXPUCAL_START

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_TXPUCAL_TUNE__CMN_TXPUCAL_START Register \(Offset = 204h\) \[reset = 2Dh\]: \[0\]](#)

12.72 CMN_TXPUCAL_ITER_TMR__CMN_TXPUCAL_INIT_TMR Register (Offset = 208h) [reset = 0006001Eh]

CMN_TXPUCAL_ITER_TMR__CMN_TXPUCAL_INIT_TMR is shown in Figure 12-72 and described in Table 12-217.

Return to [Summary Table](#).

TX pull-up resistor calibration initialization timer register

Table 12-216. CMN_TXPUCAL_ITER_TMR__CMN_TXPUCAL_INIT_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0208h

Figure 12-72. CMN_TXPUCAL_ITER_TMR__CMN_TXPUCAL_INIT_TMR Register

31	30	29	28	27	26	25	24
CMN_TXPUCAL_ITER_TMR_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_TXPUCAL_ITER_TMR_15_7	CMN_TXPUCAL_ITER_TMR_6_0						
R-0h	R/W-6h						
15	14	13	12	11	10	9	8
CMN_TXPUCAL_INIT_TMR_15_7							
R-0h							
7	6	5	4	3	2	1	0
CMN_TXPUCAL_INIT_TMR_15_7	CMN_TXPUCAL_INIT_TMR_6_0						
R-0h	R/W-1Eh						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-217. CMN_TXPUCAL_ITER_TMR__CMN_TXPUCAL_INIT_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_TXPUCAL_ITER_TMR_15_7	R	0h	Reserved
22-16	CMN_TXPUCAL_ITER_TMR_6_0	R/W	6h	Iteration wait timer value: This is the number of cmn_ref_clk clocks to wait between when a value is placed on the resistor selection bus going to the analog, and when the comparator value coming from the analog circuits can be checked. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 240 nSec. Note that this should never be set to a value of less than 3.
15-7	CMN_TXPUCAL_INIT_TMR_15_7	R	0h	Reserved
6-0	CMN_TXPUCAL_INIT_TMR_6_0	R/W	1Eh	Initialization wait timer value: This is the number of cmn_ref_clk clocks to wait between when the analog resistor calibration circuits are enabled, and when the first resistor selection values are placed on the resistor selection bus, going to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 1.2 uSec. Note that this should never be set to a value of less than 1.

Table 12-218. Register Call Summary for CMN_TXPUCAL_ITER_TMR__CMN_TXPUCAL_INIT_TMR

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_TXPUCAL_ITER_TMR__CMN_TXPUCAL_INIT_TMR Register \(Offset = 208h\) \[reset = 0006001Eh\]: \[0\]](#)

12.73 CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL Register (Offset = 210h) [reset = 0h]

CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL is shown in Figure 12-73 and described in Table 12-220.

Return to [Summary Table](#).

TX pull-down resistor calibration control register

Table 12-219.
CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 0210h

Figure 12-73. CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL Register

31	30	29	28	27	26	25	24
CMN_TXPDCA L_OVRD_15	CMN_TXPDCA L_OVRD_14	CMN_TXPDCAL_OVRD_13_7					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
CMN_TXPDCA L_OVRD_13_7	CMN_TXPDCAL_OVRD_6_0						
R-0h	R/W-0h						
15	14	13	12	11	10	9	8
CMN_TXPDCA L_CTRL_15	CMN_TXPDCA L_CTRL_14	CMN_TXPDCA L_CTRL_13	CMN_TXPDCA L_CTRL_12	CMN_TXPDCAL_CTRL_11_7			
R/W-0h	R-0h	R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
CMN_TXPDCA L_CTRL_11_7	CMN_TXPDCAL_CTRL_6_0						
R-0h	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-220. CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_TXPDCAL_OVRD_15	R/W	0h	Resistor code override enable: Activation (1'b1) of this register bit allows the resistor codes determined during the automatic resistor calibration process to be overridden. The override value is specified using the resistor code override value field of this register.
30	CMN_TXPDCAL_OVRD_14	R/W	0h	Analog calibration enable override: Activation (1'b1) of this register bit will force the analog calibration circuits to be enabled by activating the cmnda_rescal_en_tx_dseq enable and the cmnda_rescal_clk_tx_dseq clock.
29-23	CMN_TXPDCAL_OVRD_13_7	R	0h	Reserved

Table 12-220. CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-16	CMN_TXPDCAL_OVRD_6_0	R/W	0h	<p>Resistor code override value: These bits are used to override the resistor code determined during the automatic resistor calibration process.</p> <p>The resistor code written to these bits is valid when the resistor code override enable bit in this register is active.</p> <p>The following are the values for the code.</p> <p>7'b 0000000: No resistors active.</p> <p>7'b 0000001: 1 resistor active.</p> <p>7'b 0000010: 2 resistors active.</p> <p>7'b 0000011: 3 resistors active.</p> <p>7'b 0000100: 4 resistors active.</p> <p>...</p> <p>7'b 0111100: 60 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>
15	CMN_TXPDCAL_CTRL_15	R/W	0h	<p>Start resistor calibration: Activating (1'b1) this bit will start the resistor calibration process.</p> <p>This signal must remain active until the resistor calibration process is complete.</p> <p>To start another resistor calibration process, this register must first be set inactive (1'b0) until the resistor calibration process done bit in this register is cleared.</p> <p>Note: This signal is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the startup state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	CMN_TXPDCAL_CTRL_14	R	0h	<p>Resistor calibration process done: This bit will be set to 1'b1 when the resistor calibration process is complete.</p> <p>It will be cleared by cmn_reset_n, or by the deactivation of the start resistor calibration bit in this register after calibration is complete.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p> <p>Note: Three cmn_ref_clk cycles are required after the start of the resistor calibration process to clear this signal.</p>

Table 12-220. CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CMN_TXPDCAL_CTRL_1_3	R	0h	<p>No analog calibration response : This signal indicates that the calibration function has gone through the entire calibration process, reached the final calibration value, and the analog has not responded indicating that a valid calibration value has been reached. Note: Due to the nature of the calibration process, it is not possible to determine if the analog responded or not for the lowest code of 7'b00000000.</p> <p>The reason for this is, when sequencing to lower codes, the calibration function is looking for the analog response to transition from 1'b1 to 1'b0.</p> <p>If the lowest calibration code is the correct code, the analog will respond with 1'b1, and the algorithm can't sequence to a lower code to look for the transition from 1'b1 to 1'b0.</p> <p>Similarly, if the analog is not responding, it is not possible to sequence to a lower code to detect this.</p> <p>Therefore, even when the calibration function selects this calibration code as valid, this bit will be set.</p>
12	CMN_TXPDCAL_CTRL_1_2	R	0h	<p>Current analog comparator response: This is the current state of the analog comparator response signal (cmnda_rescal_comp_tx_dseg). This signal is not synchronized, and is provided for diagnostic purposes only.</p>
11-7	CMN_TXPDCAL_CTRL_1_1_7	R	0h	Reserved
6-0	CMN_TXPDCAL_CTRL_6_0	R	0h	<p>Resistor calibration code: This is the calibration code that was determined by the resistor calibration process.</p> <p>The following are the values for the code.</p> <p>7'b 0000000: No resistors active.</p> <p>7'b 0000001: 1 resistor active.</p> <p>7'b 0000010: 2 resistors active.</p> <p>7'b 0000011: 3 resistors active.</p> <p>7'b 0000100: 4 resistors active.</p> <p>...</p> <p>7'b 0111100: 60 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p> <p>Note: The reset value for this field is with the common calibration power island switched off.</p> <p>In cases where this power island is switched on, the reset value be 7'b0101101.</p>

Table 12-221. Register Call Summary for CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL

10-G SerDes Registers

- [CMN_TXPDCAL_OVRD__CMN_TXPDCAL_CTRL Register \(Offset = 210h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.74 CMN_TXPDCAL_TUNE__CMN_TXPDCAL_START Register (Offset = 214h) [reset = 802Dh]

CMN_TXPDCAL_TUNE__CMN_TXPDCAL_START is shown in Figure 12-74 and described in Table 12-223.

Return to [Summary Table](#).

TX pull-down resistor calibration start register

Table 12-222.
CMN_TXPDCAL_TUNE__CMN_TXPDCAL_START
Instances

Instance	Physical Address
SERDES_10G0	0505 0214h

Figure 12-74. CMN_TXPDCAL_TUNE__CMN_TXPDCAL_START Register

31	30	29	28	27	26	25	24
CMN_TXPDCAL_TUNE_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_TXPDCA L_TUNE_15_7	CMN_TXPDCAL_TUNE_6_0						
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CMN_TXPDCA L_START_15	CMN_TXPDCAL_START_14_7						
R/W-1h				R-0h			
7	6	5	4	3	2	1	0
CMN_TXPDCA L_START_14_7	CMN_TXPDCAL_START_6_0						
R-0h				R/W-2Dh			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-223. CMN_TXPDCAL_TUNE__CMN_TXPDCAL_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_TXPDCAL_TUNE_15_7	R	0h	Reserved
22-16	CMN_TXPDCAL_TUNE_6_0	R/W	0h	Resistor calibration tune value: The value of this field is added to the automatically calibrated code, or the override code if override is enabled. Note that this value is a twos complement value, so the calibrated code can be increased or decreased.
15	CMN_TXPDCAL_START_15	R/W	1h	Resistor calibration direction: This controls the direction that the automatic calibration process steps the calibration codes in. 1'b 0 : From 7'b00000000 to 7'b0111100. 1'b 1 : From 7'b0111100 to 7'b00000000.
14-7	CMN_TXPDCAL_START_14_7	R	0h	Reserved

Table 12-223. CMN_TXPDCAL_TUNE__CMN_TXPDCAL_START Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	CMN_TXPDCAL_START_6_0	R/W	2Dh	<p>Start resistor calibration code: This is the calibration code that the resistor calibration process starts with when automatic calibration is run.</p> <p>The following are the values for the code.</p> <p>7'b 0000000: No resistors active.</p> <p>7'b 0000001: 1 resistor active.</p> <p>7'b 0000010: 2 resistors active.</p> <p>7'b 0000011: 3 resistors active.</p> <p>7'b 0000100: 4 resistors active.</p> <p>...</p> <p>7'b 0111100: 60 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>

Table 12-224. Register Call Summary for CMN_TXPDCAL_TUNE__CMN_TXPDCAL_START

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_TXPDCAL_TUNE__CMN_TXPDCAL_START Register \(Offset = 214h\) \[reset = 802Dh\]: \[0\]](#)

12.75 CMN_TXPDCAL_ITER_TMR__CMN_TXPDCAL_INIT_TMR Register (Offset = 218h) [reset = 0006001Eh]

CMN_TXPDCAL_ITER_TMR__CMN_TXPDCAL_INIT_TMR is shown in Figure 12-75 and described in Table 12-226.

Return to [Summary Table](#).

TX pull-down resistor calibration initialization timer register

Table 12-225. CMN_TXPDCAL_ITER_TMR__CMN_TXPDCAL_INIT_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0218h

Figure 12-75. CMN_TXPDCAL_ITER_TMR__CMN_TXPDCAL_INIT_TMR Register

31	30	29	28	27	26	25	24
CMN_TXPDCAL_ITER_TMR_15_7							
R-0h							
23	22	21	20	19	18	17	16
CMN_TXPDCAL_ITER_TMR_15_7	CMN_TXPDCAL_ITER_TMR_6_0						
R-0h	R/W-6h						
15	14	13	12	11	10	9	8
CMN_TXPDCAL_INIT_TMR_15_7							
R-0h							
7	6	5	4	3	2	1	0
CMN_TXPDCAL_INIT_TMR_15_7	CMN_TXPDCAL_INIT_TMR_6_0						
R-0h	R/W-1Eh						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-226. CMN_TXPDCAL_ITER_TMR__CMN_TXPDCAL_INIT_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	CMN_TXPDCAL_ITER_TMR_15_7	R	0h	Reserved
22-16	CMN_TXPDCAL_ITER_TMR_6_0	R/W	6h	Iteration wait timer value: This is the number of cmn_ref_clk clocks to wait between when a value is placed on the resistor selection bus going to the analog, and when the comparator value coming from the analog circuits can be checked. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 240 nSec. Note that this should never be set to a value of less than 3.
15-7	CMN_TXPDCAL_INIT_TMR_15_7	R	0h	Reserved
6-0	CMN_TXPDCAL_INIT_TMR_6_0	R/W	1Eh	Initialization wait timer value: This is the number of cmn_ref_clk clocks to wait between when the analog resistor calibration circuits are enabled, and when the first resistor selection values are placed on the resistor selection bus, going to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 1.2 uSec. Note that this should never be set to a value of less than 1.

Table 12-227. Register Call Summary for CMN_TXPDCAL_ITER_TMR__CMN_TXPDCAL_INIT_TMR

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_TXPDCAL_ITER_TMR__CMN_TXPDCAL_INIT_TMR Register \(Offset = 218h\) \[reset = 0006001Eh\]: \[0\]](#)

12.76 CMN_RXCAL_OVRD__CMN_RXCAL_CTRL Register (Offset = 220h) [reset = 0h]

CMN_RXCAL_OVRD__CMN_RXCAL_CTRL is shown in [Figure 12-76](#) and described in [Table 12-229](#).

Return to [Summary Table](#).

RX resistor calibration control register

Table 12-228.
CMN_RXCAL_OVRD__CMN_RXCAL_CTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 0220h

Figure 12-76. CMN_RXCAL_OVRD__CMN_RXCAL_CTRL Register

31	30	29	28	27	26	25	24
CMN_RXCAL_OVRD_15	CMN_RXCAL_OVRD_14	CMN_RXCAL_OVRD_13_5					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
CMN_RXCAL_OVRD_13_5			CMN_RXCAL_OVRD_4_0				
R-0h			R/W-0h				
15	14	13	12	11	10	9	8
CMN_RXCAL_CTRL_15	CMN_RXCAL_CTRL_14	CMN_RXCAL_CTRL_13	CMN_RXCAL_CTRL_12	CMN_RXCAL_CTRL_11_5			
R/W-0h	R-0h	R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
CMN_RXCAL_CTRL_11_5			CMN_RXCAL_CTRL_4_0				
R-0h			R-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-229. CMN_RXCAL_OVRD__CMN_RXCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_RXCAL_OVRD_15	R/W	0h	Resistor code override enable: Activation (1'b1) of this register bit allows the resistor codes determined during the automatic resistor calibration process to be overridden. The override value is specified using the resistor code override value field of this register.
30	CMN_RXCAL_OVRD_14	R/W	0h	Analog calibration enable override: Activation (1'b1) of this register bit will force the analog calibration circuits to be enabled by activating the cmnda_rescal_en_rx enable and the cmnda_rescal_clk_rx clock.
29-21	CMN_RXCAL_OVRD_13_5	R	0h	Reserved

Table 12-229. CMN_RXCAL_OVRD__CMN_RXCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	CMN_RXCAL_OVRD_4_0	R/W	0h	<p>Resistor code override value: These bits are used to override the resistor code determined during the automatic resistor calibration process.</p> <p>The resistor code written to these bits is valid when the resistor code override enable bit in this register is active.</p> <p>The following are the values for the code:</p> <p>5'b 00000: No resistors active</p> <p>5'b 00001: 1 resistor active</p> <p>5'b 00010: 2 resistors active</p> <p>5'b 00011: 3 resistors active</p> <p>...</p> <p>5'b 01110: 14 resistors active.</p> <p>5'b 01111: 15 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>
15	CMN_RXCAL_CTRL_15	R/W	0h	<p>Start resistor calibration: Activating (1'b1) this bit will start the resistor calibration process.</p> <p>This signal must remain active until the resistor calibration process is complete.</p> <p>To start another resistor calibration process, this register must first be set inactive (1'b0) until the resistor calibration process done bit in this register is cleared.</p> <p>Note: This signal is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the startup state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	CMN_RXCAL_CTRL_14	R	0h	<p>Resistor calibration process done: This bit will be set to 1'b1 when the resistor calibration process is complete.</p> <p>It will be cleared by cmn_reset_n, or by the deactivation of the start resistor calibration bit in this register after calibration is complete.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p> <p>Note: Three cmn_ref_clk cycles are required after the start of the resistor calibration process to clear this signal.</p>

Table 12-229. CMN_RXCAL_OVRD__CMN_RXCAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CMN_RXCAL_CTRL_13	R	0h	<p>No analog calibration response : This signal indicates that the calibration function has gone through the entire calibration process, reached the final calibration value, and the analog has not responded indicating that a valid calibration value has been reached. Note: Due to the nature of the calibration process, it is not possible to determine if the analog responded or not for the lowest code of 5'b00000.</p> <p>The reason for this is, when sequencing to lower codes, the calibration function is looking for the analog response to transition from 1'b1 to 1'b0.</p> <p>If the lowest calibration code is the correct code, the analog will respond with 1'b1, and the algorithm can't sequence to a lower code to look for the transition from 1'b1 to 1'b0.</p> <p>Similarly, if the analog is not responding, it is not possible to sequence to a lower code to detect this.</p> <p>Therefore, even when the calibration function selects this calibration code as valid, this bit will be set.</p>
12	CMN_RXCAL_CTRL_12	R	0h	<p>Current analog comparator response: This is the current state of the analog comparator response signal (cmnda_rescal_comp_rx). This signal is not synchronized, and is provided for diagnostic purposes only.</p>
11-5	CMN_RXCAL_CTRL_11_5	R	0h	Reserved
4-0	CMN_RXCAL_CTRL_4_0	R	0h	<p>Resistor calibration code: This is the calibration code that was determined by the resistor calibration process.</p> <p>The following are the values for the code:</p> <p>5'b 00000: No resistors active</p> <p>5'b 00001: 1 resistor active</p> <p>5'b 00010: 2 resistors active</p> <p>5'b 00011: 3 resistors active</p> <p>...</p> <p>5'b 01110: 14 resistors active.</p> <p>5'b 01111: 15 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>

Table 12-230. Register Call Summary for CMN_RXCAL_OVRD__CMN_RXCAL_CTRL

10-G SerDes Registers

- [CMN_RXCAL_OVRD__CMN_RXCAL_CTRL Register \(Offset = 220h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.77 CMN_RXCAL_TUNE__CMN_RXCAL_START Register (Offset = 224h) [reset = 8h]

CMN_RXCAL_TUNE__CMN_RXCAL_START is shown in Figure 12-77 and described in Table 12-232.

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RX resistor calibration start register

Table 12-231.
CMN_RXCAL_TUNE__CMN_RXCAL_START
Instances

Instance	Physical Address
SERDES_10G0	0505 0224h

Figure 12-77. CMN_RXCAL_TUNE__CMN_RXCAL_START Register

31	30	29	28	27	26	25	24
CMN_RXCAL_TUNE_15_5							
R-0h							
23	22	21	20	19	18	17	16
CMN_RXCAL_TUNE_15_5				CMN_RXCAL_TUNE_4_0			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CMN_RXCAL_START_15	CMN_RXCAL_START_14_5						
R/W-0h				R-0h			
7	6	5	4	3	2	1	0
CMN_RXCAL_START_14_5				CMN_RXCAL_START_4_0			
R-0h				R/W-8h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-232. CMN_RXCAL_TUNE__CMN_RXCAL_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	CMN_RXCAL_TUNE_15_5	R	0h	Reserved
20-16	CMN_RXCAL_TUNE_4_0	R/W	0h	Resistor calibration tune value: The value of this field is added to the automatically calibrated code, or the override code if override is enabled. Note that this value is a twos complement value, so the calibrated code can be increased or decreased.
15	CMN_RXCAL_START_15	R/W	0h	Resistor calibration direction: This controls the direction that the automatic calibration process steps the calibration codes in. 1'b 0 : From 4'b0000 to 4'b0111. 1'b 1 : From 4'b0111 to 4'b0000.
14-5	CMN_RXCAL_START_14_5	R	0h	Reserved

Table 12-232. CMN_RXCAL_TUNE__CMN_RXCAL_START Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CMN_RXCAL_START_4_0	R/W	8h	<p>Start resistor calibration code: This is the calibration code that the resistor calibration process starts with when automatic calibration is run.</p> <p>The following are the values for the code.</p> <p>5'b 00000: No resistors active</p> <p>5'b 00001: 1 resistor active</p> <p>5'b 00010: 2 resistors active</p> <p>5'b 00011: 3 resistors active</p> <p>...</p> <p>5'b 01110: 14 resistors active.</p> <p>5'b 01111: 15 resistors active.</p> <p>Note that the most significant bit is the calibration code sign bit, and is always 1'b0 in this application.</p>

Table 12-233. Register Call Summary for CMN_RXCAL_TUNE__CMN_RXCAL_START

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_RXCAL_TUNE__CMN_RXCAL_START Register \(Offset = 224h\) \[reset = 8h\]: \[0\]](#)

12.78 CMN_RXCAL_ITER_TMR__CMN_RXCAL_INIT_TMR Register (Offset = 228h) [reset = 000602EEh]

CMN_RXCAL_ITER_TMR__CMN_RXCAL_INIT_TMR is shown in Figure 12-78 and described in Table 12-235.

Return to [Summary Table](#).

RX resistor calibration initialization timer register

Table 12-234. CMN_RXCAL_ITER_TMR__CMN_RXCAL_INIT_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0228h

Figure 12-78. CMN_RXCAL_ITER_TMR__CMN_RXCAL_INIT_TMR Register

31	30	29	28	27	26	25	24
CMN_RXCAL_ITER_TMR_15_12				CMN_RXCAL_ITER_TMR_11_0			
R-0h				R/W-6h			
23	22	21	20	19	18	17	16
CMN_RXCAL_ITER_TMR_11_0							
R/W-6h							
15	14	13	12	11	10	9	8
CMN_RXCAL_INIT_TMR_15_12				CMN_RXCAL_INIT_TMR_11_0			
R-0h				R/W-2EEh			
7	6	5	4	3	2	1	0
CMN_RXCAL_INIT_TMR_11_0							
R/W-2EEh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-235. CMN_RXCAL_ITER_TMR__CMN_RXCAL_INIT_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_RXCAL_ITER_TMR_15_12	R	0h	Reserved
27-16	CMN_RXCAL_ITER_TMR_11_0	R/W	6h	Iteration wait timer value: This is the number of cmn_ref_clk clocks to wait between when a value is placed on the resistor selection bus going to the analog, and when the comparator value coming from the analog circuits can be checked. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 240 nSec. Note that this should never be set to a value of less than 3.
15-12	CMN_RXCAL_INIT_TMR_15_12	R	0h	Reserved
11-0	CMN_RXCAL_INIT_TMR_11_0	R/W	2EEh	Initialization wait timer value: This is the number of cmn_ref_clk clocks to wait between when the analog resistor calibration circuits are enabled, and when the first resistor selection values are placed on the resistor selection bus, going to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 30 uSec. Note that this should never be set to a value of less than 1.

Table 12-236. Register Call Summary for CMN_RXCAL_ITER_TMR__CMN_RXCAL_INIT_TMR

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_RXCAL_ITER_TMR__CMN_RXCAL_INIT_TMR Register \(Offset = 228h\) \[reset = 000602EEh\]: \[0\]](#)

12.79 CMN_SD_CAL_START__CMN_SD_CAL_CTRL Register (Offset = 240h) [reset = 101E0000h]

CMN_SD_CAL_START__CMN_SD_CAL_CTRL is shown in Figure 12-79 and described in Table 12-238.

Return to [Summary Table](#).

Signal detect clock calibration control register

Table 12-237.
CMN_SD_CAL_START__CMN_SD_CAL_CTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 0240h

Figure 12-79. CMN_SD_CAL_START__CMN_SD_CAL_CTRL Register

31	30	29	28	27	26	25	24
CMN_SD_CAL_START_15	CMN_SD_CAL_START_14_12			CMN_SD_CAL_START_11_5			
R-0h	R/W-1h			R-0h			
23	22	21	20	19	18	17	16
CMN_SD_CAL_START_11_5			CMN_SD_CAL_START_4_0				
R-0h			R/W-1Eh				
15	14	13	12	11	10	9	8
CMN_SD_CAL_CTRL_15	CMN_SD_CAL_CTRL_14	CMN_SD_CAL_CTRL_13_5					
R/W-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
CMN_SD_CAL_CTRL_13_5			CMN_SD_CAL_CTRL_4_0				
R-0h			R-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-238. CMN_SD_CAL_START__CMN_SD_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_SD_CAL_START_15	R	0h	Reserved
30-28	CMN_SD_CAL_START_14_12	R/W	1h	Calibration initial step size control: This field specifies the initial step size for the calibration state machine. The following are the values that can be used in this field, and the corresponding step sizes. 3'b 000 : 1 3'b 001 : 2 3'b 010 : 4 3'b 011 : 8 3'b 100 : 16 3'b 101 - 3'b 111 : Reserved
27-21	CMN_SD_CAL_START_11_5	R	0h	Reserved

Table 12-238. CMN_SD_CAL_START__CMN_SD_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	CMN_SD_CAL_START_4_0	R/W	1Eh	<p>Calibration code starting point value: This field specifies the starting code that is used by the calibration state machine.</p> <p>The purpose of this value is such that the calibration process starts at a point that is, on average, relatively close to the final calibration point.</p> <p>This allows the calibration time to be reduced, on average.</p> <p>The following are the values for this code:</p> <p>5'b 00000: 0 Capacitors activated</p> <p>5'b 00001: 1 Capacitor activated</p> <p>5'b 00010: 2 Capacitors activated</p> <p>5'b 00011: 3 Capacitors activated</p> <p>...</p> <p>5'b 11110: 30 Capacitors activated</p> <p>5'b 11111: 31 Capacitors activated</p> <p>Note: This field is intended to be for diagnostics purposes only.</p> <p>Note : This field must be set to a value that is always at least one step size away from the minimum and maximum calibration codes, and is a function of the step size specified in this register.</p> <p>For example, if the initial step size is 4, this value must be at least 4 greater than the minimum calibration code or 4 l</p>
15	CMN_SD_CAL_CTRL_15	R/W	0h	<p>Start calibration: Activating (1'b1) this bit will start a calibration process.</p> <p>This bit must remain active until the calibration process is complete (as indicated by the calibration process done bit in this register).</p> <p>To start another calibration process, the calibration process done bit must have gone inactive from any prior calibration process.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the startup state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	CMN_SD_CAL_CTRL_14	R	0h	<p>Calibration process done: This bit will be set to 1'b1 when the calibration process is complete.</p> <p>It will be cleared by the deactivation of the Start calibration bit in this register.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p>
13-5	CMN_SD_CAL_CTRL_13_5	R	0h	Reserved

Table 12-238. CMN_SD_CAL_START__CMN_SD_CAL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CMN_SD_CAL_CTRL_4_0	R	0h	<p>Calibration code: This is the calibration code that was determined by the calibration process.</p> <p>This signal is valid when the calibration process is complete.</p> <p>The values of this field correspond to different frequency bands the will operate in.</p> <p>The frequency bands are controlled by the number of capacitors that are switched in the analog circuit.</p> <p>This field specifies the number of capacitors that are switched in.</p> <p>The following are the values for this code:</p> <p>5'b 00000: 0 Capacitors activated</p> <p>5'b 00001: 1 Capacitor activated</p> <p>5'b 00010: 2 Capacitors activated</p> <p>5'b 00011: 3 Capacitors activated</p> <p>...</p> <p>5'b 11110: 30 Capacitors activated</p> <p>5'b 11111: 31 Capacitors activated</p> <p>Note: This signal is intended to be for diagnostics purposes only.</p> <p>Note: The reset value for this field is with the common calibration power island switched off.</p> <p>In cases where this power island is switched on, the reset value be 5'b11110</p>

Table 12-239. Register Call Summary for CMN_SD_CAL_START__CMN_SD_CAL_CTRL

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_SD_CAL_START__CMN_SD_CAL_CTRL Register \(Offset = 240h\) \[reset = 101E0000h\]: \[0\]](#)

12.80 CMN_SD_CAL_OVRD__CMN_SD_CAL_TCTRL Register (Offset = 244h) [reset = 1h]

CMN_SD_CAL_OVRD__CMN_SD_CAL_TCTRL is shown in Figure 12-80 and described in Table 12-241.

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Signal detect clock calibration timer control register

Table 12-240.
CMN_SD_CAL_OVRD__CMN_SD_CAL_TCTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 0244h

Figure 12-80. CMN_SD_CAL_OVRD__CMN_SD_CAL_TCTRL Register

31	30	29	28	27	26	25	24
CMN_SD_CAL_OVRD_15	CMN_SD_CAL_OVRD_14_5						
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
CMN_SD_CAL_OVRD_14_5				CMN_SD_CAL_OVRD_4_0			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CMN_SD_CAL_TCTRL_15_3							
R-0h							
7	6	5	4	3	2	1	0
CMN_SD_CAL_TCTRL_15_3				CMN_SD_CAL_TCTRL_2_0			
R-0h				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-241. CMN_SD_CAL_OVRD__CMN_SD_CAL_TCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_SD_CAL_OVRD_15	R/W	0h	Calibration code override enable: Activating (1'b1) this bit allows the code determined during the automatic calibration process to be overridden by the value driven by the calibration code override value field in this register. Note: This bit is intended to be for diagnostics purposes only. Note: This bit should not be activated while a calibration is currently in progress.
30-21	CMN_SD_CAL_OVRD_14_5	R	0h	Reserved

Table 12-241. CMN_SD_CAL_OVRD__CMN_SD_CAL_TCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	CMN_SD_CAL_OVRD_4_0	R/W	0h	<p>Calibration code override value: This field is used to override the code determined during the automatic calibration process. The code driven on this field is valid when the calibration code override enable bit in this register is active.</p> <p>The following are the values for this code:</p> <p>5'b 00000: 0 Capacitors activated</p> <p>5'b 00001: 1 Capacitor activated</p> <p>5'b 00010: 2 Capacitors activated</p> <p>5'b 00011: 3 Capacitors activated</p> <p>...</p> <p>5'b 11110: 30 Capacitors activated</p> <p>5'b 11111: 31 Capacitors activated</p> <p>Note: This field is intended to be for diagnostics purposes only.</p> <p>Note: The value of this field must not be changed while the calibration function is running.</p>
15-3	CMN_SD_CAL_TCTRL_15_3	R	0h	Reserved
2-0	CMN_SD_CAL_TCTRL_2_0	R/W	1h	<p>Calibration initial time scale control: This field specifies the calibration start time scaling factor applied to the calibration when running the initial step size for the calibration code is not set to 1. Setting this value to a value other than 1 will reduce the calibration measurement time by the amount specified below.</p> <p>Then when the final calibration steps are made the full calibration time will be used to get the appropriate amount of resolution.</p> <p>3'b 000 : Div 1</p> <p>3'b 001 : Div 2</p> <p>3'b 010 : Div 4</p> <p>3'b 011 : Div 8</p> <p>3'b 100 : Div 16</p> <p>3'b 101 : Div 32</p> <p>3'b 110 : Div 64</p> <p>3'b 111 : Div 128</p>

Table 12-242. Register Call Summary for CMN_SD_CAL_OVRD__CMN_SD_CAL_TCTRL

10-G SerDes Registers

- [CMN_SD_CAL_OVRD__CMN_SD_CAL_TCTRL Register \(Offset = 244h\) \[reset = 1h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.81 CMN_SD_CAL_ITER_TMR__CMN_SD_CAL_INIT_TMR Register (Offset = 248h) [reset = 00020006h]

CMN_SD_CAL_ITER_TMR__CMN_SD_CAL_INIT_TMR is shown in [Figure 12-81](#) and described in [Table 12-244](#).

Return to [Summary Table](#).

Signal detect clock calibration initialization timer register

Table 12-243. CMN_SD_CAL_ITER_TMR__CMN_SD_CAL_INIT_TMR Instances

Instance	Physical Address
SERDES_10G0	0505 0248h

Figure 12-81. CMN_SD_CAL_ITER_TMR__CMN_SD_CAL_INIT_TMR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMN_SD_CAL_ITER_TMR_15_8								CMN_SD_CAL_ITER_TMR_7_0							
R-0h								R/W-2h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMN_SD_CAL_INIT_TMR_15_8								CMN_SD_CAL_INIT_TMR_7_0							
R-0h								R/W-6h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-244. CMN_SD_CAL_ITER_TMR__CMN_SD_CAL_INIT_TMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_SD_CAL_ITER_TMR_15_8	R	0h	Reserved
23-16	CMN_SD_CAL_ITER_TMR_7_0	R/W	2h	Iteration wait timer value: This is the number of clocks to wait between when a calibration code is driven to the analog, and when the clock rates are measured. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 80 nSec.
15-8	CMN_SD_CAL_INIT_TMR_15_8	R	0h	Reserved
7-0	CMN_SD_CAL_INIT_TMR_7_0	R/W	6h	Initialization wait timer value: This is the number of clocks to wait between when the analog calibration circuits are enabled, and when the first calibration code is driven to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 80 nSec for the analog plus four reference clocks for the digital clock gating to be enabled.

Table 12-245. Register Call Summary for CMN_SD_CAL_ITER_TMR__CMN_SD_CAL_INIT_TMR

10-G SerDes Registers

- [CMN_SD_CAL_ITER_TMR__CMN_SD_CAL_INIT_TMR Register \(Offset = 248h\) \[reset = 00020006h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.82 CMN_SD_CAL_REFTIM_START Register (Offset = 24Ch) [reset = X]

CMN_SD_CAL_REFTIM_START is shown in [Figure 12-82](#) and described in [Table 12-247](#).

Return to [Summary Table](#).

Signal detect clock calibration reference clock timer start value register

**Table 12-246. CMN_SD_CAL_REFTIM_START
Instances**

Instance	Physical Address
SERDES_10G0	0505 024Ch

Figure 12-82. CMN_SD_CAL_REFTIM_START Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_SD_CAL_REFTIM_START_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_SD_CAL_REFTIM_START_7_0							
R/W-Eh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-247. CMN_SD_CAL_REFTIM_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	CMN_SD_CAL_REFTIM_START_15_8	R	0h	Reserved
7-0	CMN_SD_CAL_REFTIM_START_7_0	R/W	Eh	Calibration reference clock timer start value : This is the value that is loaded into the reference clock timer as the starting point for that timer, when running calibration. Note that the actual number of clocks counted is one larger than what is specified by this field.

Table 12-248. Register Call Summary for CMN_SD_CAL_REFTIM_START

10-G SerDes Registers

- [CMN_SD_CAL_REFTIM_START Register \(Offset = 24Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.83 CMN_SD_CAL_PLLCNT_START Register (Offset = 250h) [reset = X]

CMN_SD_CAL_PLLCNT_START is shown in [Figure 12-83](#) and described in [Table 12-250](#).

Return to [Summary Table](#).

Signal detect clock calibration PLL clock counter start value register

Table 12-249. CMN_SD_CAL_PLLCNT_START Instances

Instance	Physical Address
SERDES_10G0	0505 0250h

Figure 12-83. CMN_SD_CAL_PLLCNT_START Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CMN_SD_CAL_PLLCNT_START_15_10						CMN_SD_CAL_PLLCNT_START_9_0	
R-0h						R/W-12Bh	
7	6	5	4	3	2	1	0
CMN_SD_CAL_PLLCNT_START_9_0							
R/W-12Bh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-250. CMN_SD_CAL_PLLCNT_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-10	CMN_SD_CAL_PLLCNT_START_15_10	R	0h	Reserved
9-0	CMN_SD_CAL_PLLCNT_START_9_0	R/W	12Bh	Calibration feedback clock counter start value : This is the value that is loaded into the PLL clock counter as the starting point for that counter, when running calibration. Note that the actual number of clocks counted is one larger than what is specified by this field.

Table 12-251. Register Call Summary for CMN_SD_CAL_PLLCNT_START

10-G SerDes Registers

- [CMN_SD_CAL_PLLCNT_START Register \(Offset = 250h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.84 CMN_CMSMT_TEST_CLK_SEL__CMN_CMSMT_CLK_FREQ_MSMT_CTRL Register (Offset = 300h) [reset = 0h]

CMN_CMSMT_TEST_CLK_SEL__CMN_CMSMT_CLK_FREQ_MSMT_CTRL is shown in Figure 12-84 and described in Table 12-253.

Return to [Summary Table](#).

Clock frequency measurement control register

Table 12-252.
CMN_CMSMT_TEST_CLK_SEL__CMN_CMSMT_CLK_FREQ_MSMT_CTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 0300h

Figure 12-84. CMN_CMSMT_TEST_CLK_SEL__CMN_CMSMT_CLK_FREQ_MSMT_CTRL Register

31	30	29	28	27	26	25	24
CMN_CMSMT_TEST_CLK_SEL_15_3							
R-0h							
23	22	21	20	19	18	17	16
CMN_CMSMT_TEST_CLK_SEL_15_3				CMN_CMSMT_TEST_CLK_SEL_2_0			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
CMN_CMSMT_CLK_FREQ_MSMT_CTRL_15	CMN_CMSMT_CLK_FREQ_MSMT_CTRL_14	CMN_CMSMT_CLK_FREQ_MSMT_CTRL_13_0					
R/W-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
CMN_CMSMT_CLK_FREQ_MSMT_CTRL_13_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-253. CMN_CMSMT_TEST_CLK_SEL__CMN_CMSMT_CLK_FREQ_MSMT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	CMN_CMSMT_TEST_CLK_SEL_15_3	R	0h	Reserved
18-16	CMN_CMSMT_TEST_CLK_SEL_2_0	R/W	0h	Test clock select: This field drives the test_clk_select pin, in order to control an external MUX for selecting between multiple test clocks to measure. The following is the encoding for this field, and the clock each value selects. 3'b 000 : PLL 0 reference clock 3'b 001 : PLL 0 feedback divider clock 3'b 010 : PLL 0 full rate clock 3'b 011 : PLL 1 reference clock 3'b 100 : PLL 1 feedback divider clock 3'b 101 : PLL 1 full rate clock 3'b 110 : Process monitor clock 3'b 111 : Signal detect clock

Table 12-253. CMN_CMSMT_TEST_CLK_SEL__CMN_CMSMT_CLK_FREQ_MSMT_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	CMN_CMSMT_CLK_FREQ_MSMT_CTRL_15	R/W	0h	Run test clock measurement: Activating (1'b1) this bit will run the test clock measurement process. This bit must remain active until the test clock measurement process is complete, as indicated by the test clock measurement done bit in this register. To start another measurement process, this bit must first be driven inactive then driven active again. Note: Both of the clocks used to generate the ref_clk and test_clk clocks must be active prior to setting or clearing this bit. Note: The values in the Test clock selection register and Reference clock timer value register must be set prior to activating this bit.
14	CMN_CMSMT_CLK_FREQ_MSMT_CTRL_14	R	0h	Test clock measurement done: This bit will be set to 1'b1 when the test clock measurement process is complete. It will be cleared by the deactivation of the start test clock measurement bit in this register.
13-0	CMN_CMSMT_CLK_FREQ_MSMT_CTRL_13_0	R	0h	Reserved

**Table 12-254. Register Call Summary for
CMN_CMSMT_TEST_CLK_SEL__CMN_CMSMT_CLK_FREQ_MSMT_CTRL**

10-G SerDes Registers

- [CMN_CMSMT_TEST_CLK_SEL__CMN_CMSMT_CLK_FREQ_MSMT_CTRL Register \(Offset = 300h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.85 CMN_CMSMT_TEST_CLK_CNT_VALUE__CMN_CMSMT_REF_CLK_TMR_VALUE Register (Offset = 304h) [reset = 0h]

CMN_CMSMT_TEST_CLK_CNT_VALUE__CMN_CMSMT_REF_CLK_TMR_VALUE is shown in Figure 12-85 and described in Table 12-256.

Return to [Summary Table](#).

Reference clock timer value register

Table 12-255.
CMN_CMSMT_TEST_CLK_CNT_VALUE__CMN_CMSMT_REF_CLK_TMR_VAL
UE Instances

Instance	Physical Address
SERDES_10G0	0505 0304h

Figure 12-85. CMN_CMSMT_TEST_CLK_CNT_VALUE__CMN_CMSMT_REF_CLK_TMR_VALUE Register

31	30	29	28	27	26	25	24
CMN_CMSMT_TEST_CLK_CNT_VALUE_15_12				CMN_CMSMT_TEST_CLK_CNT_VALUE_11_0			
R-0h				R-0h			
23	22	21	20	19	18	17	16
CMN_CMSMT_TEST_CLK_CNT_VALUE_11_0							
R-0h							
15	14	13	12	11	10	9	8
CMN_CMSMT_REF_CLK_TMR_VALUE_15_12				CMN_CMSMT_REF_CLK_TMR_VALUE_11_0			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
CMN_CMSMT_REF_CLK_TMR_VALUE_11_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-256. CMN_CMSMT_TEST_CLK_CNT_VALUE__CMN_CMSMT_REF_CLK_TMR_VALUE Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_CMSMT_TEST_CLK_CNT_VALUE_15_12	R	0h	Reserved
27-16	CMN_CMSMT_TEST_CLK_CNT_VALUE_11_0	R	0h	Test clock counter value: When the test clock measurement process is complete, the value in this field specifies the number of test clock cycles that were counted in the time specified by the reference clock timer value. This field is only valid while the test clock measurement done bit in the Clock frequency measurement control register is active.
15-12	CMN_CMSMT_REF_CLK_TMR_VALUE_15_12	R	0h	Reserved
11-0	CMN_CMSMT_REF_CLK_TMR_VALUE_11_0	R/W	0h	Reference clock timer value : This specifies the amount of time, in reference clock cycles, to count test clock cycles. This value minus 1 is loaded into the reference clock timer. A value of 0 for this field is not valid when running this function.

**Table 12-257. Register Call Summary for
CMN_CMSMT_TEST_CLK_CNT_VALUE__CMN_CMSMT_REF_CLK_TMR_VALUE**

10-G SerDes Registers

- [CMN_CMSMT_TEST_CLK_CNT_VALUE__CMN_CMSMT_REF_CLK_TMR_VALUE](#) Register (Offset = 304h) [reset = 0h]: [0]
- 10-G SerDes Registers: [0]

12.86 CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0 Register (Offset = 340h) [reset = 06011012h]

CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0 is shown in Figure 12-86 and described in Table 12-259.

Return to [Summary Table](#).

PLL 0 control register mode 0

Table 12-258.
CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0340h

Figure 12-86. CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_P LL0_CLK_SEL_ M0_15	CMN_PDIAG_PLL0_CLK_SEL_M0_14_12			CMN_PDIAG_PLL0_CLK_SEL_M0_11_8			
R/W-0h	R/W-0h			R/W-6h			
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL0_CLK_SEL_M0_7_2						CMN_PDIAG_PLL0_CLK_SEL_ M0_1_0	
R-0h						R/W-1h	
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL0_CTRL_M0_15_12				CMN_PDIAG_PLL0_CTRL_M0_11_9			CMN_PDIAG_P LL0_CTRL_M0 _8
R/W-1h				R-0h			R/W-0h
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL0_CTRL_M0_ 7_6	CMN_PDIAG_P LL0_CTRL_M0 _5		CMN_PDIAG_P LL0_CTRL_M0 _4	CMN_PDIAG_PLL0_CTRL_M0_ 3_2		CMN_PDIAG_PLL0_CTRL_M0_ 1_0	
R-0h	R/W-0h		R/W-1h	R-0h		R/W-2h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-259. CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PDIAG_PLL0_CLK_SEL_M0_15	R/W	0h	PLL 0 clock 1 divider enable: This bit enables the divider used to generate the cmnda_pll0_clk_1, from the PLL high speed clock.
30-28	CMN_PDIAG_PLL0_CLK_SEL_M0_14_12	R/W	0h	PLL 0 clock 1 divider select: This field selects the divider value used to generate the cmnda_pll0_clk_1, from the PLL high speed clock, by driving the cmnda_pll0_clk_1_div_sel signal to the analog. The encoding of this signal is as follows. All codes currently result in divide by 16.
27-24	CMN_PDIAG_PLL0_CLK_SEL_M0_11_8	R/W	6h	PLL 0 clock 0 and derived reference clock divider select: This field selects the divider value used to generate the cmnda_pll0_clk_0 and derived reference clock, from the PLL high speed clock, by driving the cmnda_pll0_clk_0_div_sel signal to the analog. The encoding of this signal is as follows. Note that there are different divider values per bit for associated with each clock.

Table 12-259. CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-18	CMN_PDIAG_PLL0_CLK_SEL_M0_7_2	R	0h	Reserved
17-16	CMN_PDIAG_PLL0_CLK_SEL_M0_1_0	R/W	1h	PLL 0 clock select: This field selects one of 3 possible high speed output clocks from PLL 0, to drive on the high speed analog clock 0, by driving the cmnda_pll0_clk_sel signal to the analog. The encoding for this is as follows. 2'b 00: Divide by 1 2'b 01: Divide by 2 2'b 10: Divide by 4 2'b 11: Reserved
15-12	CMN_PDIAG_PLL0_CTRL_M0_15_12	R/W	1h	This field controls the Ring VCO Frequency drift with temperature. It controls the mix of vtref bias and external bias to keep the temperature drift for the ring low, by driving the cmnda_pll0_vco_ring_cmos_sel signal going into the common analog.
11-9	CMN_PDIAG_PLL0_CTRL_M0_11_9	R	0h	Reserved
8	CMN_PDIAG_PLL0_CTRL_M0_8	R/W	0h	PLL VCO select: Selects the VCO mode of operation, by driving the cmnda_pll0_vco_sel signal going into the common analog. 1'b 0: LC tank mode 1'b 1: Ring oscillator mode
7-6	CMN_PDIAG_PLL0_CTRL_M0_7_6	R	0h	Reserved
5	CMN_PDIAG_PLL0_CTRL_M0_5	R/W	0h	PLL feedback divider clock select: This signal selects which internal PLL clock will be used to drive the cmnda_pll0_fb_divider_clk, by driving the cmnda_pll0_fb_divider_clk_sel signal going into the common analog. 1'b 0: Feedback divider clock 1'b 1: PLL digital rate clock
4	CMN_PDIAG_PLL0_CTRL_M0_4	R/W	1h	PLL feedback divider pre-scale: controls the feedback divider pre-scale, by driving the cmnda_pll0_div24_sel signal going into the common analog. One should read the description of the PLL in section 10.4 Dual VCO PLL on page 422 for detailed information about the function of this divider control. 1'b 0: Divide by 2 - When using the delta sigma modulator, this setting results in lower noise on the PLL output clock, but higher power. 1'b 1: Divide by 4 - When using the delta sigma modulator, this setting results in higher noise on the PLL output clock, but lower power. This setting is ideal for cases when the delta sigma modulator is not used, because it results in both lower noise and lower power.
3-2	CMN_PDIAG_PLL0_CTRL_M0_3_2	R	0h	Reserved

Table 12-259. CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	CMN_PDIAG_PLL0_CTRL_M0_1_0	R/W	2h	<p>PLL PFD reset delay: Controls the minimum reset pulse width for the PFD.</p> <p>This drives the cmnda_pll0_pfd_rst_dly signal going into the common analog.</p> <p>The following lists the reset pulse width values for typical conditions for each of the possible values for this field.</p> <p>2'b 00 : Delay = 257.5 pSec (minimum)</p> <p>2'b 01 : Delay = 337.4 pSec</p> <p>2'b 10 : Delay = 415.2 pSec</p> <p>2'b 11 : Delay = 493.2 pSec (maximum)</p>

**Table 12-260. Register Call Summary for
CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0**

10-G SerDes Registers

- [CMN_PDIAG_PLL0_CLK_SEL_M0__CMN_PDIAG_PLL0_CTRL_M0 Register \(Offset = 340h\) \[reset = 06011012h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.87 CMN_PDIAG_PLL0_ITRIM_M0__CMN_PDIAG_PLL0_OVRD_M0 Register (Offset = 344h) [reset = 000F0000h]

CMN_PDIAG_PLL0_ITRIM_M0__CMN_PDIAG_PLL0_OVRD_M0 is shown in Figure 12-87 and described in Table 12-262.

Return to [Summary Table](#).

PLL 0 override register mode 0

Table 12-261. CMN_PDIAG_PLL0_ITRIM_M0__CMN_PDIAG_PLL0_OVRD_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0344h

Figure 12-87. CMN_PDIAG_PLL0_ITRIM_M0__CMN_PDIAG_PLL0_OVRD_M0 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL0_ITRIM_M0_15_8							
R-0h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL0_ITRIM_M0_7_0							
R/W-Fh							
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL0_OVRD_M0_15_4							
R-0h							
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL0_OVRD_M0_15_4				CMN_PDIAG_P LL0_OVRD_M0 _3	CMN_PDIAG_P LL0_OVRD_M0 _2	CMN_PDIAG_P LL0_OVRD_M0 _1	CMN_PDIAG_P LL0_OVRD_M0 _0
R-0h				R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-262. CMN_PDIAG_PLL0_ITRIM_M0__CMN_PDIAG_PLL0_OVRD_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PDIAG_PLL0_ITRIM_M0_15_8	R	0h	Reserved
23-16	CMN_PDIAG_PLL0_ITRIM_M0_7_0	R/W	Fh	PLL VCO bias current trim code: Controls the tank currents in the PLL LC tank circuit. This field drives the cmnda_pll0_vco_bias_current_trim signal going to the analog.
15-4	CMN_PDIAG_PLL0_OVRD_M0_15_4	R	0h	Reserved
3	CMN_PDIAG_PLL0_OVRD_M0_3	R/W	0h	PLL VCO calibration enable override enable: When active (1'b1), the PLL VCO calibration enable override bit in this register, can be used to directly control the enable of the VCO calibration function in the PLL (instead of the VCO calibration module).
2	CMN_PDIAG_PLL0_OVRD_M0_2	R/W	0h	PLL VCO calibration enable override: When enabled by the PLL VCO calibration enable override enable bit in this register, this bit will directly control the enable of the VCO calibration function in the PLL.
1	CMN_PDIAG_PLL0_OVRD_M0_1	R/W	0h	PLL phase lock detect enable : Enables the diagnostic PLL phase lock detect function in the analog. This activates the cmnda_pll0_ph_lock_en signal going into the analog.

Table 12-262. CMN_PDIAG_PLL0_ITRIM_M0__CMN_PDIAG_PLL0_OVRD_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMN_PDIAG_PLL0_OVRD_M0_0	R	0h	PLL phase lock detected : When enabled by the PLL phase lock detect enable bit in this register, this bit indicates that a PLL phase lock has been detected. This is the current value of the cmnda_pll0_ph_lock_detect signal coming from the analog.

Table 12-263. Register Call Summary for CMN_PDIAG_PLL0_ITRIM_M0__CMN_PDIAG_PLL0_OVRD_M0

10-G SerDes Registers

- [CMN_PDIAG_PLL0_ITRIM_M0__CMN_PDIAG_PLL0_OVRD_M0 Register \(Offset = 344h\) \[reset = 000F0000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.88 CMN_PDIAG_PLL0_CP_IADJ_M0__CMN_PDIAG_PLL0_CP_PADJ_M0 Register (Offset = 348h) [reset = 08080028h]

CMN_PDIAG_PLL0_CP_IADJ_M0__CMN_PDIAG_PLL0_CP_PADJ_M0 is shown in Figure 12-88 and described in Table 12-265.

Return to [Summary Table](#).

PLL 0 charge pump proportional path adjust register mode 0

Table 12-264.
CMN_PDIAG_PLL0_CP_IADJ_M0__CMN_PDIAG_PLL0_CP_PADJ_M0
Instances

Instance	Physical Address
SERDES_10G0	0505 0348h

Figure 12-88. CMN_PDIAG_PLL0_CP_IADJ_M0__CMN_PDIAG_PLL0_CP_PADJ_M0 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL0_CP_IADJ_M0_15_8							
R/W-8h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL0_CP_IADJ_M0_7_0							
R/W-8h							
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL0_CP_PADJ_M0_15_8							
R/W-0h							
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL0_CP_PADJ_M0_7_0							
R/W-28h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-265. CMN_PDIAG_PLL0_CP_IADJ_M0__CMN_PDIAG_PLL0_CP_PADJ_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PDIAG_PLL0_CP_IADJ_M0_15_8	R/W	8h	PLL charge pump integral path capacitance adjust: Adjusts the charge pump integral path capacitance, by driving the cmnda_pll0_cp_int_cap_adj signal going to the analog.
23-16	CMN_PDIAG_PLL0_CP_IADJ_M0_7_0	R/W	8h	PLL charge pump integral path current adjust: Adjusts the charge pump integral path current, by driving the cmnda_pll0_cp_int_cur_adj signal going to the analog.
15-8	CMN_PDIAG_PLL0_CP_PADJ_M0_15_8	R/W	0h	PLL charge pump proportional path capacitance adjust: Adjusts the charge pump proportional path capacitance, by driving the cmnda_pll0_cp_prop_cap_adj signal going to the analog.
7-0	CMN_PDIAG_PLL0_CP_PADJ_M0_7_0	R/W	28h	PLL charge pump proportional path current adjust: Adjusts the charge pump proportional path current, by driving the cmnda_pll0_cp_prop_cur_adj signal going to the analog.

Table 12-266. Register Call Summary for
CMN_PDIAG_PLL0_CP_IADJ_M0__CMN_PDIAG_PLL0_CP_PADJ_M0

10-G SerDes Registers

- [CMN_PDIAG_PLL0_CP_IADJ_M0__CMN_PDIAG_PLL0_CP_PADJ_M0 Register \(Offset = 348h\) \[reset = 08080028h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.89 CMN_PDIAG_PLL0_CP_TUNE_M0__CMN_PDIAG_PLL0_FILT_PADJ_M0 Register (Offset = 34Ch) [reset = 00010000h]

CMN_PDIAG_PLL0_CP_TUNE_M0__CMN_PDIAG_PLL0_FILT_PADJ_M0 is shown in Figure 12-89 and described in Table 12-268.

Return to [Summary Table](#).

PLL 0 proportional path filter adjust register mode 0

Table 12-267.
CMN_PDIAG_PLL0_CP_TUNE_M0__CMN_PDIAG_PLL0_FILT_PADJ_M0
Instances

Instance	Physical Address
SERDES_10G0	0505 034Ch

Figure 12-89. CMN_PDIAG_PLL0_CP_TUNE_M0__CMN_PDIAG_PLL0_FILT_PADJ_M0 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL0_CP_TUNE_M0_15_2							
R-0h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL0_CP_TUNE_M0_15_2						CMN_PDIAG_PLL0_CP_TUNE_M0_1_0	
R-0h						R/W-1h	
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL0_FILT_PADJ_M0_15_12				CMN_PDIAG_PLL0_FILT_PADJ_M0_11_8			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL0_FILT_PADJ_M0_7_4				CMN_PDIAG_PLL0_FILT_PADJ_M0_3_0			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-268. CMN_PDIAG_PLL0_CP_TUNE_M0__CMN_PDIAG_PLL0_FILT_PADJ_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	CMN_PDIAG_PLL0_CP_TUNE_M0_15_2	R	0h	Reserved
17-16	CMN_PDIAG_PLL0_CP_TUNE_M0_1_0	R/W	1h	PLL charge pump calibration reference voltage tune: Adjusts the charge pump calibration reference voltage, by driving the cmnda_pll0_cp_vref_tune signal going to the analog. 2'b 00 : minimum 2'b01 2'b10 2'b11 maximum
15-12	CMN_PDIAG_PLL0_FILT_PADJ_M0_15_12	R	0h	Reserved
11-8	CMN_PDIAG_PLL0_FILT_PADJ_M0_11_8	R/W	0h	PLL proportional path filter capacitance adjust: Adjusts the proportional path filter capacitance, by driving the cmnda_pll0_filt_c_adj signal going to the analog.
7-4	CMN_PDIAG_PLL0_FILT_PADJ_M0_7_4	R	0h	Reserved

Table 12-268. CMN_PDIAG_PLL0_CP_TUNE_M0__CMN_PDIAG_PLL0_FILT_PADJ_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CMN_PDIAG_PLL0_FILT_PADJ_M0_3_0	R/W	0h	PLL proportional path filter resistance adjust: Adjusts the proportional path filter resistance, by driving the cmnda_pll0_filt_r_adj signal going to the analog.

**Table 12-269. Register Call Summary for
CMN_PDIAG_PLL0_CP_TUNE_M0__CMN_PDIAG_PLL0_FILT_PADJ_M0**

10-G SerDes Registers

- [CMN_PDIAG_PLL0_CP_TUNE_M0__CMN_PDIAG_PLL0_FILT_PADJ_M0 Register \(Offset = 34Ch\) \[reset = 00010000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.90 CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1 Register (Offset = 360h) [reset = 04001012h]

CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1 is shown in Figure 12-90 and described in Table 12-271.

Return to [Summary Table](#).

PLL 0 control register mode 1

Table 12-270.

CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1 Instances

Instance	Physical Address
SERDES_10G0	0505 0360h

Figure 12-90. CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_P LL0_CLK_SEL_ M1_15	CMN_PDIAG_PLL0_CLK_SEL_M1_14_12			CMN_PDIAG_PLL0_CLK_SEL_M1_11_8			
R/W-0h	R/W-0h			R/W-4h			
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL0_CLK_SEL_M1_7_2						CMN_PDIAG_PLL0_CLK_SEL_ M1_1_0	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL0_CTRL_M1_15_12				CMN_PDIAG_PLL0_CTRL_M1_11_9			CMN_PDIAG_P LL0_CTRL_M1 _8
R/W-1h				R-0h			R/W-0h
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL0_CTRL_M1_ 7_6	CMN_PDIAG_P LL0_CTRL_M1 _5		CMN_PDIAG_P LL0_CTRL_M1 _4	CMN_PDIAG_PLL0_CTRL_M1_ 3_2		CMN_PDIAG_PLL0_CTRL_M1_ 1_0	
R-0h	R/W-0h		R/W-1h	R-0h		R/W-2h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-271. CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PDIAG_PLL0_CLK_SEL_M1_15	R/W	0h	PLL 0 clock 1 divider enable: This bit enables the divider used to generate the cmnda_pll0_clk_1, from the PLL high speed clock.
30-28	CMN_PDIAG_PLL0_CLK_SEL_M1_14_12	R/W	0h	PLL 0 clock 1 divider select: This field selects the divider value used to generate the cmnda_pll0_clk_1, from the PLL high speed clock, by driving the cmnda_pll0_clk_1_div_sel signal to the analog. The encoding of this signal is as follows. All codes currently result in divide by 16.
27-24	CMN_PDIAG_PLL0_CLK_SEL_M1_11_8	R/W	4h	PLL 0 clock 0 and derived reference clock divider select: This field selects the divider value used to generate the cmnda_pll0_clk_0 and derived reference clock, from the PLL high speed clock, by driving the cmnda_pll0_clk_0_div_sel signal to the analog. The encoding of this signal is as follows. Note that there are different divider values per bit for associated with each clock.

Table 12-271. CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-18	CMN_PDIAG_PLL0_CLK_SEL_M1_7_2	R	0h	Reserved
17-16	CMN_PDIAG_PLL0_CLK_SEL_M1_1_0	R/W	0h	PLL 0 clock select: This field selects one of 3 possible high speed output clocks from PLL 0, to drive on the high speed analog clock 0, by driving the cmnda_pll0_clk_sel signal to the analog. The encoding for this is as follows. 2'b 00: Divide by 1 2'b 01: Divide by 2 2'b 10: Divide by 4 2'b 11: Reserved
15-12	CMN_PDIAG_PLL0_CTRL_M1_15_12	R/W	1h	This field controls the Ring VCO Frequency drift with temperature. It controls the mix of vtref bias and external bias to keep the temperature drift for the ring low, by driving the cmnda_pll0_vco_ring_cmos_sel signal going into the common analog.
11-9	CMN_PDIAG_PLL0_CTRL_M1_11_9	R	0h	Reserved
8	CMN_PDIAG_PLL0_CTRL_M1_8	R/W	0h	PLL VCO select: Selects the VCO mode of operation, by driving the cmnda_pll0_vco_sel signal going into the common analog. 1'b 0: LC tank mode 1'b 1: Ring oscillator mode
7-6	CMN_PDIAG_PLL0_CTRL_M1_7_6	R	0h	Reserved
5	CMN_PDIAG_PLL0_CTRL_M1_5	R/W	0h	PLL feedback divider clock select: This signal selects which internal PLL clock will be used to drive the cmnda_pll0_fb_divider_clk, driving the cmnda_pll0_fb_divider_clk_sel signal going into the common analog. 1'b 0: Feedback divider clock 1'b 1: PLL digital rate clock
4	CMN_PDIAG_PLL0_CTRL_M1_4	R/W	1h	PLL feedback divider pre-scale: controls the feedback divider pre-scale, by driving the cmnda_pll0_div24_sel signal going into the common analog. One should read the description of the PLL in section 10.4 Dual VCO PLL on page 422 for detailed information about the function of this divider control. 1'b 0: Divide by 2 - When using the delta sigma modulator, this setting results in lower noise on the PLL output clock, but higher power. 1'b 1: Divide by 4 - When using the delta sigma modulator, this setting results in higher noise on the PLL output clock, but lower power. This setting is ideal for cases when the delta sigma modulator is not used, because it results in both lower noise and lower power.
3-2	CMN_PDIAG_PLL0_CTRL_M1_3_2	R	0h	Reserved

Table 12-271. CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	CMN_PDIAG_PLL0_CTRL_M1_1_0	R/W	2h	<p>PLL PFD reset delay: Controls the minimum reset pulse width for the PFD.</p> <p>This drives the cmnda_pll0_pfd_rst_dly signal going into the common analog.</p> <p>The following lists the reset pulse width values for typical conditions for each of the possible values for this field.</p> <p>2'b 00 : Delay = 257.5 pSec (minimum)</p> <p>2'b 01 : Delay = 337.4 pSec</p> <p>2'b 10 : Delay = 415.2 pSec</p> <p>2'b 11 : Delay = 493.2 pSec (maximum)</p>

**Table 12-272. Register Call Summary for
CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1**

10-G SerDes Registers

- [CMN_PDIAG_PLL0_CLK_SEL_M1__CMN_PDIAG_PLL0_CTRL_M1 Register \(Offset = 360h\) \[reset = 04001012h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.91 CMN_PDIAG_PLL0_ITRIM_M1__CMN_PDIAG_PLL0_OVRD_M1 Register (Offset = 364h) [reset = 000F0000h]

CMN_PDIAG_PLL0_ITRIM_M1__CMN_PDIAG_PLL0_OVRD_M1 is shown in Figure 12-91 and described in Table 12-274.

Return to [Summary Table](#).

PLL 0 override register mode 1

Table 12-273. CMN_PDIAG_PLL0_ITRIM_M1__CMN_PDIAG_PLL0_OVRD_M1 Instances

Instance	Physical Address
SERDES_10G0	0505 0364h

Figure 12-91. CMN_PDIAG_PLL0_ITRIM_M1__CMN_PDIAG_PLL0_OVRD_M1 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL0_ITRIM_M1_15_8							
R-0h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL0_ITRIM_M1_7_0							
R/W-Fh							
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL0_OVRD_M1_15_4							
R-0h							
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL0_OVRD_M1_15_4				CMN_PDIAG_P LL0_OVRD_M1 _3	CMN_PDIAG_P LL0_OVRD_M1 _2	CMN_PDIAG_P LL0_OVRD_M1 _1	CMN_PDIAG_P LL0_OVRD_M1 _0
R-0h				R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-274. CMN_PDIAG_PLL0_ITRIM_M1__CMN_PDIAG_PLL0_OVRD_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PDIAG_PLL0_ITRIM_M1_15_8	R	0h	Reserved
23-16	CMN_PDIAG_PLL0_ITRIM_M1_7_0	R/W	Fh	PLL VCO bias current trim code: Controls the tank currents in the PLL LC tank circuit. This field drives the cmnda_pll0_vco_bias_current_trim signal going to the analog.
15-4	CMN_PDIAG_PLL0_OVRD_M1_15_4	R	0h	Reserved
3	CMN_PDIAG_PLL0_OVRD_M1_3	R/W	0h	PLL VCO calibration enable override enable: When active (1'b1), the PLL VCO calibration enable override bit in this register, can be used to directly control the enable of the VCO calibration function in the PLL (instead of the VCO calibration module).
2	CMN_PDIAG_PLL0_OVRD_M1_2	R/W	0h	PLL VCO calibration enable override: When enabled by the PLL VCO calibration enable override enable bit in this register, this bit will directly control the enable of the VCO calibration function in the PLL.
1	CMN_PDIAG_PLL0_OVRD_M1_1	R/W	0h	PLL phase lock detect enable : Enables the diagnostic PLL phase lock detect function in the analog. This activates the cmnda_pll0_ph_lock_en signal going into the analog.

Table 12-274. CMN_PDIAG_PLL0_ITRIM_M1__CMN_PDIAG_PLL0_OVRD_M1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMN_PDIAG_PLL0_OVRD_M1_0	R	0h	PLL phase lock detected : When enabled by the PLL phase lock detect enable bit in this register, this bit indicates that a PLL phase lock has been detected. This is the current value of the cmnda_pll0_ph_lock_detect signal coming from the analog.

Table 12-275. Register Call Summary for CMN_PDIAG_PLL0_ITRIM_M1__CMN_PDIAG_PLL0_OVRD_M1

10-G SerDes Registers

- [CMN_PDIAG_PLL0_ITRIM_M1__CMN_PDIAG_PLL0_OVRD_M1 Register \(Offset = 364h\) \[reset = 000F0000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.92 CMN_PDIAG_PLL0_CP_IADJ_M1__CMN_PDIAG_PLL0_CP_PADJ_M1 Register (Offset = 368h) [reset = 08080128h]

CMN_PDIAG_PLL0_CP_IADJ_M1__CMN_PDIAG_PLL0_CP_PADJ_M1 is shown in Figure 12-92 and described in Table 12-277.

Return to [Summary Table](#).

PLL 0 charge pump proportional path adjust register mode 1

Table 12-276.
CMN_PDIAG_PLL0_CP_IADJ_M1__CMN_PDIAG_PLL0_CP_PADJ_M1
Instances

Instance	Physical Address
SERDES_10G0	0505 0368h

Figure 12-92. CMN_PDIAG_PLL0_CP_IADJ_M1__CMN_PDIAG_PLL0_CP_PADJ_M1 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL0_CP_IADJ_M1_15_8							
R/W-8h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL0_CP_IADJ_M1_7_0							
R/W-8h							
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL0_CP_PADJ_M1_15_8							
R/W-1h							
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL0_CP_PADJ_M1_7_0							
R/W-28h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-277. CMN_PDIAG_PLL0_CP_IADJ_M1__CMN_PDIAG_PLL0_CP_PADJ_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PDIAG_PLL0_CP_IADJ_M1_15_8	R/W	8h	PLL charge pump integral path capacitance adjust: Adjusts the charge pump integral path capacitance, by driving the cmnda_pll0_cp_int_cap_adj signal going to the analog.
23-16	CMN_PDIAG_PLL0_CP_IADJ_M1_7_0	R/W	8h	PLL charge pump integral path current adjust: Adjusts the charge pump integral path current, by driving the cmnda_pll0_cp_int_cur_adj signal going to the analog.
15-8	CMN_PDIAG_PLL0_CP_PADJ_M1_15_8	R/W	1h	PLL charge pump proportional path capacitance adjust: Adjusts the charge pump proportional path capacitance, by driving the cmnda_pll0_cp_prop_cap_adj signal going to the analog.
7-0	CMN_PDIAG_PLL0_CP_PADJ_M1_7_0	R/W	28h	PLL charge pump proportional path current adjust: Adjusts the charge pump proportional path current, by driving the cmnda_pll0_cp_prop_cur_adj signal going to the analog.

Table 12-278. Register Call Summary for
CMN_PDIAG_PLL0_CP_IADJ_M1__CMN_PDIAG_PLL0_CP_PADJ_M1

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PDIAG_PLL0_CP_IADJ_M1__CMN_PDIAG_PLL0_CP_PADJ_M1 Register \(Offset = 368h\) \[reset = 08080128h\]: \[0\]](#)

12.93 CMN_PDIAG_PLL0_CP_TUNE_M1__CMN_PDIAG_PLL0_FILT_PADJ_M1 Register (Offset = 36Ch) [reset = 00010000h]

CMN_PDIAG_PLL0_CP_TUNE_M1__CMN_PDIAG_PLL0_FILT_PADJ_M1 is shown in Figure 12-93 and described in Table 12-280.

Return to [Summary Table](#).

PLL 0 proportional path filter adjust register mode 1

Table 12-279.
CMN_PDIAG_PLL0_CP_TUNE_M1__CMN_PDIAG_PLL0_FILT_PADJ_M1
Instances

Instance	Physical Address
SERDES_10G0	0505 036Ch

Figure 12-93. CMN_PDIAG_PLL0_CP_TUNE_M1__CMN_PDIAG_PLL0_FILT_PADJ_M1 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL0_CP_TUNE_M1_15_2							
R-0h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL0_CP_TUNE_M1_15_2						CMN_PDIAG_PLL0_CP_TUNE_M1_1_0	
R-0h						R/W-1h	
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL0_FILT_PADJ_M1_15_12				CMN_PDIAG_PLL0_FILT_PADJ_M1_11_8			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL0_FILT_PADJ_M1_7_4				CMN_PDIAG_PLL0_FILT_PADJ_M1_3_0			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-280. CMN_PDIAG_PLL0_CP_TUNE_M1__CMN_PDIAG_PLL0_FILT_PADJ_M1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	CMN_PDIAG_PLL0_CP_TUNE_M1_15_2	R	0h	Reserved
17-16	CMN_PDIAG_PLL0_CP_TUNE_M1_1_0	R/W	1h	PLL charge pump calibration reference voltage tune: Adjusts the charge pump calibration reference voltage, by driving the cmnda_pll0_cp_vref_tune signal going to the analog. 2'b 00 : minimum 2'b01 2'b10 2'b11 maximum
15-12	CMN_PDIAG_PLL0_FILT_PADJ_M1_15_12	R	0h	Reserved
11-8	CMN_PDIAG_PLL0_FILT_PADJ_M1_11_8	R/W	0h	PLL proportional path filter capacitance adjust: Adjusts the proportional path filter capacitance, by driving the cmnda_pll0_filt_c_adj signal going to the analog.
7-4	CMN_PDIAG_PLL0_FILT_PADJ_M1_7_4	R	0h	Reserved

Table 12-280. CMN_PDIAG_PLL0_CP_TUNE_M1__CMN_PDIAG_PLL0_FILT_PADJ_M1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CMN_PDIAG_PLL0_FILT_PADJ_M1_3_0	R/W	0h	PLL proportional path filter resistance adjust: Adjusts the proportional path filter resistance, by driving the cmnda_pll0_filt_r_adj signal going to the analog.

**Table 12-281. Register Call Summary for
CMN_PDIAG_PLL0_CP_TUNE_M1__CMN_PDIAG_PLL0_FILT_PADJ_M1**

10-G SerDes Registers

- [CMN_PDIAG_PLL0_CP_TUNE_M1__CMN_PDIAG_PLL0_FILT_PADJ_M1 Register \(Offset = 36Ch\) \[reset = 00010000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.94 CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0 Register (Offset = 380h) [reset = 04001012h]

CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0 is shown in Figure 12-94 and described in Table 12-283.

Return to [Summary Table](#).

PLL 1 control register mode 0

Table 12-282.

CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0380h

Figure 12-94. CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_P LL1_CLK_SEL_ M0_15	CMN_PDIAG_PLL1_CLK_SEL_M0_14_12			CMN_PDIAG_PLL1_CLK_SEL_M0_11_8			
R/W-0h	R/W-0h			R/W-4h			
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL1_CLK_SEL_M0_7_2						CMN_PDIAG_PLL1_CLK_SEL_ M0_1_0	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL1_CTRL_M0_15_12				CMN_PDIAG_PLL1_CTRL_M0_11_9			CMN_PDIAG_P LL1_CTRL_M0 _8
R/W-1h				R-0h			R/W-0h
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL1_CTRL_M0_ 7_6	CMN_PDIAG_P LL1_CTRL_M0 _5		CMN_PDIAG_P LL1_CTRL_M0 _4	CMN_PDIAG_PLL1_CTRL_M0_ 3_2		CMN_PDIAG_PLL1_CTRL_M0_ 1_0	
R-0h	R/W-0h		R/W-1h	R-0h		R/W-2h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-283. CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_PDIAG_PLL1_CLK_SEL_M0_15	R/W	0h	PLL 1 clock 1 divider enable: This bit enables the divider used to generate the cmnda_pll1_clk_1, from the PLL high speed clock.
30-28	CMN_PDIAG_PLL1_CLK_SEL_M0_14_12	R/W	0h	PLL 1 clock 1 divider select: This field selects the divider value used to generate the cmnda_pll1_clk_1, from the PLL high speed clock, by driving the cmnda_pll1_clk_1_div_sel signal to the analog. The encoding of this signal is as follows. All codes currently result in divide by 16.
27-24	CMN_PDIAG_PLL1_CLK_SEL_M0_11_8	R/W	4h	PLL 1 clock 0 and derived reference clock divider select: This field selects the divider value used to generate the cmnda_pll1_clk_0 and derived reference clock, from the PLL high speed clock, by driving the cmnda_pll1_clk_0_div_sel signal to the analog. The encoding of this signal is as follows. Note that there are different divider values per bit for associated with each clock.

Table 12-283. CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-18	CMN_PDIAG_PLL1_CLK_SEL_M0_7_2	R	0h	Reserved
17-16	CMN_PDIAG_PLL1_CLK_SEL_M0_1_0	R/W	0h	PLL 1 clock select: This field selects one of 3 possible high speed output clocks from PLL 1, to drive on the high speed analog clock 1, by driving the cmnda_pll1_clk_sel signal to the analog. The encoding for this is as follows. 2'b 00: Divide by 1 2'b 01: Divide by 2 2'b 10: Divide by 4 2'b 11: Reserved
15-12	CMN_PDIAG_PLL1_CTRL_M0_15_12	R/W	1h	This field controls the Ring VCO Frequency drift with temperature. It controls the mix of vtref bias and external bias to keep the temperature drift for the ring low, by driving the cmnda_pll1_vco_ring_cmos_sel signal going into the common analog.
11-9	CMN_PDIAG_PLL1_CTRL_M0_11_9	R	0h	Reserved
8	CMN_PDIAG_PLL1_CTRL_M0_8	R/W	0h	PLL VCO select: Selects the VCO mode of operation, by driving the cmnda_pll1_vco_sel signal going into the common analog. 1'b 0: LC tank mode 1'b 1: Ring oscillator mode
7-6	CMN_PDIAG_PLL1_CTRL_M0_7_6	R	0h	Reserved
5	CMN_PDIAG_PLL1_CTRL_M0_5	R/W	0h	PLL feedback divider clock select: This signal selects which internal PLL clock will be used to drive the cmnda_pll1_fb_divider_clk, driving the cmnda_pll1_fb_divider_clk_sel signal going into the common analog. 1'b 0: Feedback divider clock 1'b 1: PLL digital rate clock
4	CMN_PDIAG_PLL1_CTRL_M0_4	R/W	1h	PLL feedback divider pre-scale: controls the feedback divider pre-scale, by driving the cmnda_pll1_div24_sel signal going into the common analog. One should read the description of the PLL in section 10.4 Dual VCO PLL on page 422 for detailed information about the function of this divider control. 1'b 0: Divide by 2 - When using the delta sigma modulator, this setting results in lower noise on the PLL output clock, but higher power. 1'b 1: Divide by 4 - When using the delta sigma modulator, this setting results in higher noise on the PLL output clock, but lower power. This setting is ideal for cases when the delta sigma modulator is not used, because it results in both lower noise and lower power.
3-2	CMN_PDIAG_PLL1_CTRL_M0_3_2	R	0h	Reserved

Table 12-283. CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	CMN_PDIAG_PLL1_CTRL_M0_1_0	R/W	2h	<p>PLL PFD reset delay: Controls the minimum reset pulse width for the PFD.</p> <p>This drives the cmnda_pll1_pfd_rst_dly signal going into the common analog.</p> <p>The following lists the reset pulse width values for typical conditions for each of the possible values for this field.</p> <p>2'b 00 : Delay = 257.5 pSec (minimum)</p> <p>2'b 01 : Delay = 337.4 pSec</p> <p>2'b 10 : Delay = 415.2 pSec</p> <p>2'b 11 : Delay = 493.2 pSec (maximum)</p>

**Table 12-284. Register Call Summary for
CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0**

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [CMN_PDIAG_PLL1_CLK_SEL_M0__CMN_PDIAG_PLL1_CTRL_M0 Register \(Offset = 380h\) \[reset = 04001012h\]: \[0\]](#)

12.95 CMN_PDIAG_PLL1_ITRIM_M0__CMN_PDIAG_PLL1_OVRD_M0 Register (Offset = 384h) [reset = 000F0000h]

CMN_PDIAG_PLL1_ITRIM_M0__CMN_PDIAG_PLL1_OVRD_M0 is shown in Figure 12-95 and described in Table 12-286.

Return to [Summary Table](#).

PLL 1 override register mode 0

Table 12-285. CMN_PDIAG_PLL1_ITRIM_M0__CMN_PDIAG_PLL1_OVRD_M0 Instances

Instance	Physical Address
SERDES_10G0	0505 0384h

Figure 12-95. CMN_PDIAG_PLL1_ITRIM_M0__CMN_PDIAG_PLL1_OVRD_M0 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL1_ITRIM_M0_15_8							
R-0h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL1_ITRIM_M0_7_0							
R/W-Fh							
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL1_OVRD_M0_15_4							
R-0h							
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL1_OVRD_M0_15_4				CMN_PDIAG_P LL1_OVRD_M0 _3	CMN_PDIAG_P LL1_OVRD_M0 _2	CMN_PDIAG_P LL1_OVRD_M0 _1	CMN_PDIAG_P LL1_OVRD_M0 _0
R-0h				R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-286. CMN_PDIAG_PLL1_ITRIM_M0__CMN_PDIAG_PLL1_OVRD_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PDIAG_PLL1_ITRIM_M0_15_8	R	0h	Reserved
23-16	CMN_PDIAG_PLL1_ITRIM_M0_7_0	R/W	Fh	PLL VCO bias current trim code: Controls the tank currents in the PLL LC tank circuit. This field drives the cmnda_pll1_vco_bias_current_trim signal going to the analog.
15-4	CMN_PDIAG_PLL1_OVRD_M0_15_4	R	0h	Reserved
3	CMN_PDIAG_PLL1_OVRD_M0_3	R/W	0h	PLL VCO calibration enable override enable: When active (1'b1), the PLL VCO calibration enable override bit in this register, can be used to directly control the enable of the VCO calibration function in the PLL (instead of the VCO calibration module).
2	CMN_PDIAG_PLL1_OVRD_M0_2	R/W	0h	PLL VCO calibration enable override: When enabled by the PLL VCO calibration enable override enable bit in this register, this bit will directly control the enable of the VCO calibration function in the PLL.
1	CMN_PDIAG_PLL1_OVRD_M0_1	R/W	0h	PLL phase lock detect enable : Enables the diagnostic PLL phase lock detect function in the analog. This activates the cmnda_pll1_ph_lock_en signal going into the analog.

Table 12-286. CMN_PDIAG_PLL1_ITRIM_M0__CMN_PDIAG_PLL1_OVRD_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CMN_PDIAG_PLL1_OVRD_M0_0	R	0h	PLL phase lock detected : When enabled by the PLL phase lock detect enable bit in this register, this bit indicates that a PLL phase lock has been detected. This is the current value of the cmnda_pll1_ph_lock_detect signal coming from the analog.

Table 12-287. Register Call Summary for CMN_PDIAG_PLL1_ITRIM_M0__CMN_PDIAG_PLL1_OVRD_M0

10-G SerDes Registers

- [CMN_PDIAG_PLL1_ITRIM_M0__CMN_PDIAG_PLL1_OVRD_M0 Register \(Offset = 384h\) \[reset = 000F0000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.96 CMN_PDIAG_PLL1_CP_IADJ_M0__CMN_PDIAG_PLL1_CP_PADJ_M0 Register (Offset = 388h) [reset = 08080128h]

CMN_PDIAG_PLL1_CP_IADJ_M0__CMN_PDIAG_PLL1_CP_PADJ_M0 is shown in Figure 12-96 and described in Table 12-289.

Return to [Summary Table](#).

PLL 1 charge pump proportional path adjust register mode 0

Table 12-288.
CMN_PDIAG_PLL1_CP_IADJ_M0__CMN_PDIAG_PLL1_CP_PADJ_M0
Instances

Instance	Physical Address
SERDES_10G0	0505 0388h

Figure 12-96. CMN_PDIAG_PLL1_CP_IADJ_M0__CMN_PDIAG_PLL1_CP_PADJ_M0 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL1_CP_IADJ_M0_15_8							
R/W-8h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL1_CP_IADJ_M0_7_0							
R/W-8h							
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL1_CP_PADJ_M0_15_8							
R/W-1h							
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL1_CP_PADJ_M0_7_0							
R/W-28h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-289. CMN_PDIAG_PLL1_CP_IADJ_M0__CMN_PDIAG_PLL1_CP_PADJ_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_PDIAG_PLL1_CP_IADJ_M0_15_8	R/W	8h	PLL charge pump integral path capacitance adjust: Adjusts the charge pump integral path capacitance, by driving the cmnda_pll1_cp_int_cap_adj signal going to the analog.
23-16	CMN_PDIAG_PLL1_CP_IADJ_M0_7_0	R/W	8h	PLL charge pump integral path current adjust: Adjusts the charge pump integral path current, by driving the cmnda_pll1_cp_int_cur_adj signal going to the analog.
15-8	CMN_PDIAG_PLL1_CP_PADJ_M0_15_8	R/W	1h	PLL charge pump proportional path capacitance adjust: Adjusts the charge pump proportional path capacitance, by driving the cmnda_pll1_cp_prop_cap_adj signal going to the analog.
7-0	CMN_PDIAG_PLL1_CP_PADJ_M0_7_0	R/W	28h	PLL charge pump proportional path current adjust: Adjusts the charge pump proportional path current, by driving the cmnda_pll1_cp_prop_cur_adj signal going to the analog.

Table 12-290. Register Call Summary for
CMN_PDIAG_PLL1_CP_IADJ_M0__CMN_PDIAG_PLL1_CP_PADJ_M0

10-G SerDes Registers

- [CMN_PDIAG_PLL1_CP_IADJ_M0__CMN_PDIAG_PLL1_CP_PADJ_M0 Register \(Offset = 388h\) \[reset = 08080128h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.97 CMN_PDIAG_PLL1_CP_TUNE_M0__CMN_PDIAG_PLL1_FILT_PADJ_M0 Register (Offset = 38Ch) [reset = 00010000h]

CMN_PDIAG_PLL1_CP_TUNE_M0__CMN_PDIAG_PLL1_FILT_PADJ_M0 is shown in Figure 12-97 and described in Table 12-292.

Return to [Summary Table](#).

PLL 1 proportional path filter adjust register mode 0

Table 12-291.
CMN_PDIAG_PLL1_CP_TUNE_M0__CMN_PDIAG_PLL1_FILT_PADJ_M0
Instances

Instance	Physical Address
SERDES_10G0	0505 038Ch

Figure 12-97. CMN_PDIAG_PLL1_CP_TUNE_M0__CMN_PDIAG_PLL1_FILT_PADJ_M0 Register

31	30	29	28	27	26	25	24
CMN_PDIAG_PLL1_CP_TUNE_M0_15_2							
R-0h							
23	22	21	20	19	18	17	16
CMN_PDIAG_PLL1_CP_TUNE_M0_15_2						CMN_PDIAG_PLL1_CP_TUNE_M0_1_0	
R-0h						R/W-1h	
15	14	13	12	11	10	9	8
CMN_PDIAG_PLL1_FILT_PADJ_M0_15_12				CMN_PDIAG_PLL1_FILT_PADJ_M0_11_8			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
CMN_PDIAG_PLL1_FILT_PADJ_M0_7_4				CMN_PDIAG_PLL1_FILT_PADJ_M0_3_0			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-292. CMN_PDIAG_PLL1_CP_TUNE_M0__CMN_PDIAG_PLL1_FILT_PADJ_M0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	CMN_PDIAG_PLL1_CP_TUNE_M0_15_2	R	0h	Reserved
17-16	CMN_PDIAG_PLL1_CP_TUNE_M0_1_0	R/W	1h	PLL charge pump calibration reference voltage tune: Adjusts the charge pump calibration reference voltage, by driving the cmnda_pll1_cp_vref_tune signal going to the analog. 2'b 00 : minimum 2'b01 2'b10 2'b11 maximum
15-12	CMN_PDIAG_PLL1_FILT_PADJ_M0_15_12	R	0h	Reserved
11-8	CMN_PDIAG_PLL1_FILT_PADJ_M0_11_8	R/W	0h	PLL proportional path filter capacitance adjust: Adjusts the proportional path filter capacitance, by driving the cmnda_pll1_filt_c_adj signal going to the analog.
7-4	CMN_PDIAG_PLL1_FILT_PADJ_M0_7_4	R	0h	Reserved

Table 12-292. CMN_PDIAG_PLL1_CP_TUNE_M0__CMN_PDIAG_PLL1_FILT_PADJ_M0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CMN_PDIAG_PLL1_FILT_PADJ_M0_3_0	R/W	0h	PLL proportional path filter resistance adjust: Adjusts the proportional path filter resistance, by driving the cmnda_pll1_filt_r_adj signal going to the analog.

**Table 12-293. Register Call Summary for
CMN_PDIAG_PLL1_CP_TUNE_M0__CMN_PDIAG_PLL1_FILT_PADJ_M0**

10-G SerDes Registers

- [CMN_PDIAG_PLL1_CP_TUNE_M0__CMN_PDIAG_PLL1_FILT_PADJ_M0 Register \(Offset = 38Ch\) \[reset = 00010000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.98 CMN_DIAG_BIAS_OVRD1__CMN_DIAG_BANDGAP_OVRD Register (Offset = 3C0h) [reset = 36000005h]

CMN_DIAG_BIAS_OVRD1__CMN_DIAG_BANDGAP_OVRD is shown in Figure 12-98 and described in Table 12-295.

Return to [Summary Table](#).

Bandgap override register

Table 12-294. CMN_DIAG_BIAS_OVRD1__CMN_DIAG_BANDGAP_OVRD Instances

Instance	Physical Address
SERDES_10G0	0505 03C0h

Figure 12-98. CMN_DIAG_BIAS_OVRD1__CMN_DIAG_BANDGAP_OVRD Register

31	30	29	28	27	26	25	24
CMN_DIAG_BIAS_OVRD1_15	CMN_DIAG_BIAS_OVRD1_14_12			CMN_DIAG_BIAS_OVRD1_11	CMN_DIAG_BIAS_OVRD1_10_8		
R-0h	R/W-3h			R-0h	R/W-6h		
23	22	21	20	19	18	17	16
CMN_DIAG_BIAS_OVRD1_7_4				CMN_DIAG_BIAS_OVRD1_3_1		CMN_DIAG_BIAS_OVRD1_0	
R/W-0h				R-0h		R/W-0h	
15	14	13	12	11	10	9	8
CMN_DIAG_BANDGAP_OVRD_15_12				CMN_DIAG_BANDGAP_OVRD_11_8			
R-0h				R-0h			
7	6	5	4	3	2	1	0
CMN_DIAG_BANDGAP_OVRD_7_5			CMN_DIAG_BANDGAP_OVRD_4	CMN_DIAG_BANDGAP_OVRD_3_2		CMN_DIAG_BANDGAP_OVRD_1_0	
R-0h			R/W-0h	R/W-1h		R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-295. CMN_DIAG_BIAS_OVRD1__CMN_DIAG_BANDGAP_OVRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CMN_DIAG_BIAS_OVRD1_15	R	0h	Reserved
30-28	CMN_DIAG_BIAS_OVRD1_14_12	R/W	3h	Receiver resistor calibration current adjust: This field is used to adjust the receiver resistor calibration bias current. It drives the cmnda_bias_rx_rescal_adj signal going to the analog. The following list shows the encoding of this field. 3'b 000 : 110.72 uA 3'b 001 : 112.50 uA 3'b 010 : 114.29 uA 3'b 011 : 116.07 uA 3'b 100 : 117.86 uA 3'b 101 : 119.64 uA 3'b 110 : 121.43 uA 3'b 111 : 123.22 uA
27	CMN_DIAG_BIAS_OVRD1_11	R	0h	Reserved

**Table 12-295. CMN_DIAG_BIAS_OVRD1_CMN_DIAG_BANDGAP_OVRD Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26-24	CMN_DIAG_BIAS_OVRD1_10_8	R/W	6h	Transmitter resistor calibration current adjust: This field is used to adjust the transmitter resistor calibration bias current. It drives the cmnda_bias_tx_rescal_adj signal going to the analog. The following list shows the encoding of this field. 3'b 000 : 110.72 uA 3'b 001 : 112.50 uA 3'b 010 : 114.29 uA 3'b 011 : 116.07 uA 3'b 100 : 117.86 uA 3'b 101 : 119.64 uA 3'b 110 : 121.43 uA 3'b 111 : 123.22 uA
23-20	CMN_DIAG_BIAS_OVRD1_7_4	R/W	0h	Reserved - spare
19-17	CMN_DIAG_BIAS_OVRD1_3_1	R	0h	Reserved
16	CMN_DIAG_BIAS_OVRD1_0	R/W	0h	Reserved - spare
15-12	CMN_DIAG_BANDGAP_OVRD_15_12	R	0h	Reserved
11-8	CMN_DIAG_BANDGAP_OVRD_11_8	R	0h	Bandgap startup circuit startup count : Identifies the status of the bandgap startup counter. This bit is driven by the cmnda_bias_bg_start_count signal coming from the analog.
7-5	CMN_DIAG_BANDGAP_OVRD_7_5	R	0h	Reserved
4	CMN_DIAG_BANDGAP_OVRD_4	R/W	0h	Bandgap startup circuit select : Selects the startup circuit to be used for the bias / bandgap circuits, by driving the cmnda_bias_bg_start_sel signal going to the analog. 1'b 0: Analog comparator startup circuit 1'b 1: Ring oscillator startup circuit
3-2	CMN_DIAG_BANDGAP_OVRD_3_2	R/W	1h	Bandgap startup circuit sense voltage adjust : This field is used to adjust the bandgap startup circuit sense voltage, by driving the cmnda_bias_bg_start_adj signal to the analog. The following list shows the encoding of this field. 2'b 00 : 543.0 mV 2'b 01 : 558.5 mV 2'b 10 : 574.0 mV 2'b 11 : Reserved
1-0	CMN_DIAG_BANDGAP_OVRD_1_0	R/W	1h	Bandgap voltage adjust : This field is used to adjust the bandgap voltage, by driving the cmnda_bias_bg_adj signal to the analog. The following list shows the encoding of this field. 2'b 00 : 414.7 mV 2'b 01 : 440.7 mV 2'b 10 : 446.7 mV 2'b 11 : 446.7 mV

Table 12-296. Register Call Summary for CMN_DIAG_BIAS_OVRD1__CMN_DIAG_BANDGAP_OVRD

10-G SerDes Registers

- [CMN_DIAG_BIAS_OVRD1__CMN_DIAG_BANDGAP_OVRD Register \(Offset = 3C0h\) \[reset = 36000005h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.99 CMN_DIAG_VREG_CTRL_CMN_DIAG_BIAS_OVRD2 Register (Offset = 3C4h) [reset = 0h]

CMN_DIAG_VREG_CTRL_CMN_DIAG_BIAS_OVRD2 is shown in Figure 12-99 and described in Table 12-298.

Return to [Summary Table](#).

Bias override register 2

Table 12-297. CMN_DIAG_VREG_CTRL_CMN_DIAG_BIAS_OVRD2 Instances

Instance	Physical Address
SERDES_10G0	0505 03C4h

Figure 12-99. CMN_DIAG_VREG_CTRL_CMN_DIAG_BIAS_OVRD2 Register

31	30	29	28	27	26	25	24
CMN_DIAG_VREG_CTRL_15_1							
R-0h							
23	22	21	20	19	18	17	16
CMN_DIAG_VREG_CTRL_15_1							CMN_DIAG_VREG_CTRL_0
R-0h							R/W-0h
15	14	13	12	11	10	9	8
CMN_DIAG_BIAS_OVRD2_15_6							
R-0h							
7	6	5	4	3	2	1	0
CMN_DIAG_BIAS_OVRD2_15_6	CMN_DIAG_BIAS_OVRD2_5	CMN_DIAG_BIAS_OVRD2_4	CMN_DIAG_BIAS_OVRD2_3_2	CMN_DIAG_BIAS_OVRD2_1_0			
R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-298. CMN_DIAG_VREG_CTRL_CMN_DIAG_BIAS_OVRD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	CMN_DIAG_VREG_CTRL_15_1	R	0h	Reserved
16	CMN_DIAG_VREG_CTRL_0	R/W	0h	Voltage regulator reference voltage select: Selects the reference voltage used for the voltage regulator in common, by driving the cmnda_vreg_ref_sel signal to the analog. 1'b 0: Bandgap supply 1'b 1: Core supply
15-6	CMN_DIAG_BIAS_OVRD2_15_6	R	0h	Reserved
5	CMN_DIAG_BIAS_OVRD2_5	R/W	0h	Bias filter bypass enable override enable: When active (1'b1), the bias filter bypass enable override bit in this register, can be used to directly control the bias filter bypass enable function.
4	CMN_DIAG_BIAS_OVRD2_4	R/W	0h	Bias filter bypass enable override: When enabled by the bias filter bypass enable override enable bit in this register, this bit will directly control the bias filter bypass enable function.
3-2	CMN_DIAG_BIAS_OVRD2_3_2	R	0h	Reserved

**Table 12-298. CMN_DIAG_VREG_CTRL__CMN_DIAG_BIAS_OVRD2 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
1-0	CMN_DIAG_BIAS_OVRD2_1_0	R/W	0h	Regulator bandgap reference voltage adjust: This field is used to adjust the regulator bandgap reference voltage, by driving the cmnda_bias_vreg_adj signal to the analog. The encoding of this field is as follows. 2'b 00 : 850 mV 2'b 01 : 830 mV 2'b 10 : 810 mV 2'b 11 : Reserved

Table 12-299. Register Call Summary for CMN_DIAG_VREG_CTRL__CMN_DIAG_BIAS_OVRD2

10-G SerDes Registers

- [CMN_DIAG_VREG_CTRL__CMN_DIAG_BIAS_OVRD2 Register \(Offset = 3C4h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.100 CMN_DIAG_SH_BANDGAP__CMN_DIAG_PM_CTRL Register (Offset = 3C8h) [reset = 0h]

CMN_DIAG_SH_BANDGAP__CMN_DIAG_PM_CTRL is shown in Figure 12-100 and described in Table 12-301.

Return to [Summary Table](#).

Common process monitor control register

Table 12-300.
CMN_DIAG_SH_BANDGAP__CMN_DIAG_PM_CTRL
Instances

Instance	Physical Address
SERDES_10G0	0505 03C8h

Figure 12-100. CMN_DIAG_SH_BANDGAP__CMN_DIAG_PM_CTRL Register

31	30	29	28	27	26	25	24
CMN_DIAG_SH_BANDGAP_15_6							
R-0h							
23	22	21	20	19	18	17	16
CMN_DIAG_SH_BANDGAP_15_6	CMN_DIAG_SH_BANDGAP_5	CMN_DIAG_SH_BANDGAP_4_0					
R-0h	R-0h	R-0h					
15	14	13	12	11	10	9	8
CMN_DIAG_PM_CTRL_15_5							
R-0h							
7	6	5	4	3	2	1	0
CMN_DIAG_PM_CTRL_15_5	CMN_DIAG_PM_CTRL_4	CMN_DIAG_PM_CTRL_3	CMN_DIAG_PM_CTRL_2_0				
R-0h	R/W-0h	R-0h	R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-301. CMN_DIAG_SH_BANDGAP__CMN_DIAG_PM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	CMN_DIAG_SH_BANDGAP_15_6	R	0h	Reserved
21	CMN_DIAG_SH_BANDGAP_5	R	0h	Bandgap up value: Bandgap calibration up signal value, as it is currently captured in the sample and hold latches.
20-16	CMN_DIAG_SH_BANDGAP_4_0	R	0h	Bandgap auto zero select value: Bandgap calibration auto zero select signal value, as it is currently captured in the sample and hold latches.
15-5	CMN_DIAG_PM_CTRL_15_5	R	0h	Reserved
4	CMN_DIAG_PM_CTRL_4	R/W	0h	Process monitor enable: Enables the analog process monitor, by driving the cmnda_pcm_en signal to the analog. 1'b 0: Disabled 1'b 1: Enabled
3	CMN_DIAG_PM_CTRL_3	R	0h	Reserved

**Table 12-301. CMN_DIAG_SH_BANDGAP__CMN_DIAG_PM_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2-0	CMN_DIAG_PM_CTRL_2_0	R/W	0h	Process monitor mode select: Selects the mode of the analog process monitor, by driving the cmnda_pcm_sel signal to the analog. 000 : SVT 11nm oscillator, 001 : LVT 11nm oscillator, 010 : ULVT 11nm oscillator, 011 : IO oscillator, 100 : SVT 36nm oscillator, 101 : LVT 36nm oscillator, 110 : ULVT 36nm oscillator, 111 : Reserved

Table 12-302. Register Call Summary for CMN_DIAG_SH_BANDGAP__CMN_DIAG_PM_CTRL

10-G SerDes Registers

- [CMN_DIAG_SH_BANDGAP__CMN_DIAG_PM_CTRL Register \(Offset = 3C8h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.101 CMN_DIAG_SH_SDCLK__CMN_DIAG_SH_RESISTOR Register (Offset = 3CCh) [reset = 0h]

CMN_DIAG_SH_SDCLK__CMN_DIAG_SH_RESISTOR is shown in Figure 12-101 and described in Table 12-304.

Return to [Summary Table](#).

Sample and hold resistor calibration code register

Table 12-303. CMN_DIAG_SH_SDCLK__CMN_DIAG_SH_RESISTOR Instances

Instance	Physical Address
SERDES_10G0	0505 03CCh

Figure 12-101. CMN_DIAG_SH_SDCLK__CMN_DIAG_SH_RESISTOR Register

31	30	29	28	27	26	25	24
CMN_DIAG_SH_SDCLK_15_5							
R-0h							
23	22	21	20	19	18	17	16
CMN_DIAG_SH_SDCLK_15_5				CMN_DIAG_SH_SDCLK_4_0			
R-0h				R-0h			
15	14	13	12	11	10	9	8
CMN_DIAG_SH_RESISTOR_15_14		CMN_DIAG_SH_RESISTOR_13_8					
R-0h		R-0h					
7	6	5	4	3	2	1	0
CMN_DIAG_SH_RESISTOR_7_4				CMN_DIAG_SH_RESISTOR_3_0			
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 12-304. CMN_DIAG_SH_SDCLK__CMN_DIAG_SH_RESISTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	CMN_DIAG_SH_SDCLK_15_5	R	0h	Reserved
20-16	CMN_DIAG_SH_SDCLK_4_0	R	0h	Signal detect clock code: Signal detect clock calibration code signal value, as it is currently captured in the sample and hold latches.
15-14	CMN_DIAG_SH_RESISTOR_15_14	R	0h	Reserved
13-8	CMN_DIAG_SH_RESISTOR_13_8	R	0h	TX resistor code: TX resistor calibration code signal value, as it is currently captured in the sample and hold latches.
7-4	CMN_DIAG_SH_RESISTOR_7_4	R	0h	Reserved
3-0	CMN_DIAG_SH_RESISTOR_3_0	R	0h	RX resistor code: RX resistor calibration code signal value, as it is currently captured in the sample and hold latches.

Table 12-305. Register Call Summary for CMN_DIAG_SH_SDCLK__CMN_DIAG_SH_RESISTOR

10-G SerDes Registers

- [CMN_DIAG_SH_SDCLK__CMN_DIAG_SH_RESISTOR Register \(Offset = 3CCh\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.102 CMN_DIAG_ATB_CTRL2__CMN_DIAG_ATB_CTRL1 Register (Offset = 3D0h) [reset = 0h]

CMN_DIAG_ATB_CTRL2__CMN_DIAG_ATB_CTRL1 is shown in Figure 12-102 and described in Table 12-307.

Return to [Summary Table](#).

ATB control register 1

Table 12-306. CMN_DIAG_ATB_CTRL2__CMN_DIAG_ATB_CTRL1 Instances

Instance	Physical Address
SERDES_10G0	0505 03D0h

Figure 12-102. CMN_DIAG_ATB_CTRL2__CMN_DIAG_ATB_CTRL1 Register

31	30	29	28	27	26	25	24
CMN_DIAG_ATB_CTRL2_15_13			CMN_DIAG_ATB_CTRL2_12_11			CMN_DIAG_ATB_CTRL2_10_6	
R-0h			R/W-0h			R/W-0h	
23	22	21	20	19	18	17	16
CMN_DIAG_ATB_CTRL2_10_6		CMN_DIAG_ATB_CTRL2_5_0					
R/W-0h		R/W-0h					
15	14	13	12	11	10	9	8
CMN_DIAG_ATB_CTRL1_15_2							
R-0h							
7	6	5	4	3	2	1	0
CMN_DIAG_ATB_CTRL1_15_2						CMN_DIAG_ATB_CTRL1_1	CMN_DIAG_ATB_CTRL1_0
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-307. CMN_DIAG_ATB_CTRL2__CMN_DIAG_ATB_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	CMN_DIAG_ATB_CTRL2_15_13	R	0h	Reserved
28-27	CMN_DIAG_ATB_CTRL2_12_11	R/W	0h	ATB component type select: These bits specify which component type is currently selected by the ATB, as specified below. 2'b 00: Common 2'b 01: Transmitter 2'b 10: Receiver 2'b 11: Reserved
26-22	CMN_DIAG_ATB_CTRL2_10_6	R/W	0h	ATB component sub address: Specifies the sub address of the component being selected. In this design, the sub address must be 0 when accessing the common, and the lane number when accessing a transmitter or receiver.
21-16	CMN_DIAG_ATB_CTRL2_5_0	R/W	0h	ATB test point address: Specifies the exact point in the selected analog component to be observed.
15-2	CMN_DIAG_ATB_CTRL1_15_2	R	0h	Reserved
1	CMN_DIAG_ATB_CTRL1_1	R/W	0h	Core side ATB enable: When active (1'b) and the ATB enable bit in this register is also active, the ATB signals will be driven on the core side ATB signals.
0	CMN_DIAG_ATB_CTRL1_0	R/W	0h	ATB enable: When active (1'b1), the ATB test function is enabled.

Table 12-308. Register Call Summary for CMN_DIAG_ATB_CTRL2__CMN_DIAG_ATB_CTRL1

10-G SerDes Registers <ul style="list-style-type: none"> CMN_DIAG_ATB_CTRL2__CMN_DIAG_ATB_CTRL1 Register (Offset = 3D0h) [reset = 0h]: [0] 10-G SerDes Registers: [0]

12.103 CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0 Register (Offset = 3D4h) [reset = 0h]

CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0 is shown in Figure 12-103 and described in Table 12-310.

Return to [Summary Table](#).

ATB ADC control register 0

Table 12-309. CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0 Instances

Instance	Physical Address
SERDES_10G0	0505 03D4h

Figure 12-103. CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0 Register

31	30	29	28	27	26	25	24
CMN_DIAG_ATB_ADC_CTRL1_15_14	CMN_DIAG_ATB_ADC_CTRL1_13	CMN_DIAG_ATB_ADC_CTRL1_12	CMN_DIAG_ATB_ADC_CTRL1_11	CMN_DIAG_ATB_ADC_CTRL1_10_9	CMN_DIAG_ATB_ADC_CTRL1_8_4	CMN_DIAG_ATB_ADC_CTRL1_3_0	CMN_DIAG_ATB_ADC_CTRL1_2_0
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
CMN_DIAG_ATB_ADC_CTRL1_8_4	CMN_DIAG_ATB_ADC_CTRL1_3_0	CMN_DIAG_ATB_ADC_CTRL1_2_0	CMN_DIAG_ATB_ADC_CTRL1_1_0	CMN_DIAG_ATB_ADC_CTRL1_0_0	CMN_DIAG_ATB_ADC_CTRL1_0_0	CMN_DIAG_ATB_ADC_CTRL1_0_0	CMN_DIAG_ATB_ADC_CTRL1_0_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
CMN_DIAG_ATB_ADC_CTRL0_15	CMN_DIAG_ATB_ADC_CTRL0_14	CMN_DIAG_ATB_ADC_CTRL0_13	CMN_DIAG_ATB_ADC_CTRL0_12_8	CMN_DIAG_ATB_ADC_CTRL0_12_8	CMN_DIAG_ATB_ADC_CTRL0_12_8	CMN_DIAG_ATB_ADC_CTRL0_12_8	CMN_DIAG_ATB_ADC_CTRL0_12_8
R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CMN_DIAG_ATB_ADC_CTRL0_7_0	CMN_DIAG_ATB_ADC_CTRL0_7_0	CMN_DIAG_ATB_ADC_CTRL0_7_0	CMN_DIAG_ATB_ADC_CTRL0_7_0	CMN_DIAG_ATB_ADC_CTRL0_7_0	CMN_DIAG_ATB_ADC_CTRL0_7_0	CMN_DIAG_ATB_ADC_CTRL0_7_0	CMN_DIAG_ATB_ADC_CTRL0_7_0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-310. CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	CMN_DIAG_ATB_ADC_CTRL1_15_14	R	0h	Reserved
29	CMN_DIAG_ATB_ADC_CTRL1_13	R/W	0h	ATB ADC offset correction enable : Enables internal auto generated offset correction mode, by driving the cmnda_atba2d_en_off_cor signal to the analog. 1'b 0: Disabled 1'b 1: Enabled
28	CMN_DIAG_ATB_ADC_CTRL1_12	R/W	0h	ATB ADC force cap values : Forces a positive or negative voltage on the internal cap, by driving the cmnda_atba2d_frc_val signal to the analog. 1'b 0: Forces a negative voltage on the cap. 1'b 1: Forces a positive voltage on the cap.
27	CMN_DIAG_ATB_ADC_CTRL1_11	R/W	0h	ATB ADC enable manual offset correction : When this signal is active, the value in the ATB ADC manual offset correction value field of this register is used to manually control the offset correction, by driving the cmnda_atba2d_off_byp_en signal to the analog. 1'b 0: Disabled 1'b 1: Enabled

**Table 12-310. CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26-25	CMN_DIAG_ATB_ADC_CTRL1_10_9	R	0h	Reserved
24-20	CMN_DIAG_ATB_ADC_CTRL1_8_4	R/W	0h	ATB ADC manual offset correction value : When the ATB ADC enable manual offset correction bit in this register is active, this field is used to manually control the offset correction, by driving the cmnda_atba2d_off_adj_byp signal to the analog.
19-16	CMN_DIAG_ATB_ADC_CTRL1_3_0	R/W	0h	<p>ATB ADC mode : This field indicates the mode the analog to digital converter is in.</p> <p>This field directly controls the cmnda_atba2d_adcmode signal going to the analog.</p> <p>For current mode measurements (ATB analog to digital converter mode == 3'b101), the current is equal to (Code/256)*0.6901/10.5K uA.</p> <p>The following list describes each of the modes, and the value used to select it.</p> <p>4'b 0000: Hi-Z Mode</p> <p>4'b 0001: atb0 and local gnd</p> <p>4'b 0010: atb0 assumed remote gnd</p> <p>4'b 0011: atb1 and local gnd</p> <p>4'b 0100: atb1 assumed remote gnd</p> <p>4'b 0101: 10K between atb0 and agnd</p> <p>4'b 0110: Offset Measure Mode volt offset</p> <p>4'b 0111: Offset Measure Mode current offset</p> <p>4'b 1000: BIST mode - force cap 1 polarity based on the ADC force cap values bit in this register.</p> <p>4'b 1001: BIST mode - force cap 2 polarity based on the ADC force cap values bit in this register.</p> <p>4'b 1010: BIST mode - force cap 3 polarity based on the ADC force cap values bit in this register.</p> <p>4'b 1011: BIST mode - force</p>
15	CMN_DIAG_ATB_ADC_CTRL0_15	R/W	0h	<p>ATB analog ADC enable: This enables the analog ADC function, by driving the cmnda_atba2d_en signal to the analog.</p> <p>This bit must be set to the enabled state before starting an ATB ADC process using the other bits in this register.</p> <p>1'b 0: ADC disabled</p> <p>1'b 1: ADC enabled</p>
14	CMN_DIAG_ATB_ADC_CTRL0_14	R/W	0h	<p>Start ATB ADC process: Activating (1'b1) this bit will start the ATB ADC process.</p> <p>This signal must remain active until the ATB ADC process is complete, as indicated by the ATB ADC process done bit in this register.</p> <p>To start another ATB ADC process, this bit must first be deactivated until the ATB ADC process done bit in this register is also cleared.</p> <p>This bit drives the cmnda_atba2d_start signal to the analog.</p>
13	CMN_DIAG_ATB_ADC_CTRL0_13	R	0h	<p>ATB ADC process done: This bit will be set to 1'b1 when the ATB ADC process is complete, and the data in the ATB ADC code field of this register is considered valid.</p> <p>Once set to 1'b1, it will remain set until the Start ATB ADC process bit in this register is set to 1'b0.</p> <p>This bit is driven by the cmnda_atba2d_dvalid signal from the analog.</p>

**Table 12-310. CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
12-8	CMN_DIAG_ATB_ADC_C TRL0_12_8	R	0h	Reserved
7-0	CMN_DIAG_ATB_ADC_C TRL0_7_0	R	0h	ATB ADC data code: This is the digital code representing the level of the analog ATB signal that was digitized by the analog ADC. This code is only valid when the ATB ADC process done bit in this register is active (1'b1). The voltage represented by this value is equal to $\text{code}/256 \times 0.94$.

Table 12-311. Register Call Summary for CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0

10-G SerDes Registers

- [CMN_DIAG_ATB_ADC_CTRL1__CMN_DIAG_ATB_ADC_CTRL0 Register \(Offset = 3D4h\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.104 CMN_DIAG_RST_DIAG__CMN_DIAG_HSRSM_CTRL Register (Offset = 3D8h) [reset = 11h]

CMN_DIAG_RST_DIAG__CMN_DIAG_HSRSM_CTRL is shown in Figure 12-104 and described in Table 12-313.

Return to [Summary Table](#).

Common high speed reset release state machine control register

Table 12-312. CMN_DIAG_RST_DIAG__CMN_DIAG_HSRSM_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 03D8h

Figure 12-104. CMN_DIAG_RST_DIAG__CMN_DIAG_HSRSM_CTRL Register

31	30	29	28	27	26	25	24
CMN_DIAG_RST_DIAG_15_12				CMN_DIAG_RST_DIAG_11	CMN_DIAG_RST_DIAG_10	CMN_DIAG_RST_DIAG_9	CMN_DIAG_RST_DIAG_8
R-0h				R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
CMN_DIAG_RST_DIAG_7	CMN_DIAG_RST_DIAG_6	CMN_DIAG_RST_DIAG_5	CMN_DIAG_RST_DIAG_4	CMN_DIAG_RST_DIAG_3	CMN_DIAG_RST_DIAG_2	CMN_DIAG_RST_DIAG_1	CMN_DIAG_RST_DIAG_0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
CMN_DIAG_HSRSM_CTRL_15_7							
R-0h							
7	6	5	4	3	2	1	0
CMN_DIAG_HSRSM_CTRL_5_7	CMN_DIAG_HSRSM_CTRL_6_4			CMN_DIAG_HSRSM_CTRL_3	CMN_DIAG_HSRSM_CTRL_2_0		
R-0h	R/W-1h			R-0h	R/W-1h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-313. CMN_DIAG_RST_DIAG__CMN_DIAG_HSRSM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	CMN_DIAG_RST_DIAG_15_12	R	0h	Reserved
27	CMN_DIAG_RST_DIAG_11	R	0h	Current state of the cmn_sd_clk_cal_fb_clk_reset_n reset.
26	CMN_DIAG_RST_DIAG_10	R	0h	Current state of the cmn_sd_clk_cal_ref_clk_reset_n reset.
25	CMN_DIAG_RST_DIAG_9	R	0h	Current state of the cmn_pll1_dsm_reset_n reset.
24	CMN_DIAG_RST_DIAG_8	R	0h	Current state of the cmn_pll0_dsm_reset_n reset.
23	CMN_DIAG_RST_DIAG_7	R	0h	Current state of the cmn_pll1_vco_cal_fbdiv_clk_reset_n reset.
22	CMN_DIAG_RST_DIAG_6	R	0h	Current state of the cmn_pll1_lock_det_fbdiv_clk_reset_n reset.
21	CMN_DIAG_RST_DIAG_5	R	0h	Current state of the cmn_pll1_vco_cal_ref_clk_reset_n reset.
20	CMN_DIAG_RST_DIAG_4	R	0h	Current state of the cmn_pll1_lock_det_ref_clk_reset_n reset.
19	CMN_DIAG_RST_DIAG_3	R	0h	Current state of the cmn_pll0_vco_cal_fbdiv_clk_reset_n reset.

**Table 12-313. CMN_DIAG_RST_DIAG__CMN_DIAG_HSRSM_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
18	CMN_DIAG_RST_DIAG_2	R	0h	Current state of the cmn_pll0_lock_det_fbdiv_clk_reset_n reset.
17	CMN_DIAG_RST_DIAG_1	R	0h	Current state of the cmn_pll0_vco_cal_ref_clk_reset_n reset.
16	CMN_DIAG_RST_DIAG_0	R	0h	Current state of the cmn_pll0_lock_det_ref_clk_reset_n reset.
15-7	CMN_DIAG_HSRSM_CTRL_15_7	R	0h	Reserved
6-4	CMN_DIAG_HSRSM_CTRL_6_4	R/W	1h	Transceiver reset delay : Species the number of PSM clock cycles the transceiver common high speed reset state machine stays in the delay state.
3	CMN_DIAG_HSRSM_CTRL_3	R	0h	Reserved
2-0	CMN_DIAG_HSRSM_CTRL_2_0	R/W	1h	Transmitter reset delay : Species the number of PSM clock cycles the transmitter common high speed reset state machine stays in the delay state.

Table 12-314. Register Call Summary for CMN_DIAG_RST_DIAG__CMN_DIAG_HSRSM_CTRL

10-G SerDes Registers

- [CMN_DIAG_RST_DIAG__CMN_DIAG_HSRSM_CTRL Register \(Offset = 3D8h\) \[reset = 11h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.105 CMN_DIAG_ACYA__CMN_DIAG_DCYA Register (Offset = 3DCh) [reset = 0h]

CMN_DIAG_ACYA__CMN_DIAG_DCYA is shown in [Figure 12-105](#) and described in [Table 12-316](#).

Return to [Summary Table](#).

Common digital functions cover your alternatives register

Table 12-315. CMN_DIAG_ACYA__CMN_DIAG_DCYA Instances

Instance	Physical Address
SERDES_10G0	0505 03DCh

Figure 12-105. CMN_DIAG_ACYA__CMN_DIAG_DCYA Register

31	30	29	28	27	26	25	24
CMN_DIAG_ACYA_15_8							
R-0h							
23	22	21	20	19	18	17	16
CMN_DIAG_ACYA_7_4				CMN_DIAG_ACYA_3_0			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
CMN_DIAG_DCYA_15_8							
R-0h							
7	6	5	4	3	2	1	0
CMN_DIAG_DCYA_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-316. CMN_DIAG_ACYA__CMN_DIAG_DCYA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMN_DIAG_ACYA_15_8	R	0h	Reserved
23-20	CMN_DIAG_ACYA_7_4	R/W	0h	Reserved - spare
19-16	CMN_DIAG_ACYA_3_0	R/W	0h	PLL charge pump proportional gain adjust: Adjusts the charge pump gain for the PLLs to help manage bandwidth. The following is the encoding of this field. 4'b 0000: vctrip + 0 mV 4'b 0001: vctrip + 15 mV 4'b 0011: vctrip + 30 mV 4'b 0111: vctrip + 45 mV 4'b 1111: vctrip + 60 mV
15-8	CMN_DIAG_DCYA_15_8	R	0h	Reserved
7-0	CMN_DIAG_DCYA_7_0	R/W	0h	Reserved - spare

Table 12-317. Register Call Summary for CMN_DIAG_ACYA__CMN_DIAG_DCYA

10-G SerDes Registers

- [CMN_DIAG_ACYA__CMN_DIAG_DCYA Register \(Offset = 3DCh\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.106 MOD_VER Register (Offset = 400h) [reset = 698A6002h]

MOD_VER is shown in [Figure 12-106](#) and described in [Table 12-319](#).

Return to [Summary Table](#).

The Module and Version Register identifies the module identifier and revision of the WIZmodule.

Table 12-318. MOD_VER Instances

Instance	Physical Address
SERDES_10G0	0505 0400h

Figure 12-106. MOD_VER Register

31	30	29	28	27	26	25	24
SCHEME		BU		MODULE_ID			
R-1h		R-2h		R-98Ah			
23	22	21	20	19	18	17	16
MODULE_ID							
R-98Ah							
15	14	13	12	11	10	9	8
RTL_VERSION					MAJOR_REVISION		
R-Ch					R-0h		
7	6	5	4	3	2	1	0
CUSTOM_REVISION		MINOR_REVISION					
R-0h		R-2h					

LEGEND: R = Read Only; -n = value after reset

Table 12-319. MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Module Scheme
29-28	BU	R	2h	Module BU
27-16	MODULE_ID	R	98Ah	Module ID.
15-11	RTL_VERSION	R	Ch	RTL Version.
10-8	MAJOR_REVISION	R	0h	Major Revision.
7-6	CUSTOM_REVISION	R	0h	Custom Revision.
5-0	MINOR_REVISION	R	2h	Minor Revision.

Table 12-320. Register Call Summary for MOD_VER

10-G SerDes Registers

- [MOD_VER Register \(Offset = 400h\) \[reset = 698A6002h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.107 SERDES_CTRL Register (Offset = 404h) [reset = X]

SERDES_CTRL is shown in [Figure 12-107](#) and described in [Table 12-322](#).

Return to [Summary Table](#).

Sets the SERDES control state.

Table 12-321. SERDES_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 0404h

Figure 12-107. SERDES_CTRL Register

31	30	29	28	27	26	25	24
POR_EN	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-322. SERDES_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POR_EN	R/W	0h	The POR_EN allows the system to place the SERDES in a reset state, Access to the SERDES registers are ignored.
30-0	RESERVED	R/W	X	

Table 12-323. Register Call Summary for SERDES_CTRL

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [SERDES_CTRL Register \(Offset = 404h\) \[reset = X\]: \[0\]](#)

12.108 SERDES_TOP_CTRL Register (Offset = 408h) [reset = X]

SERDES_TOP_CTRL is shown in Figure 12-108 and described in Table 12-325.

Return to [Summary Table](#).

The SERDES Top Level Control

Table 12-324. SERDES_TOP_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 0408h

Figure 12-108. SERDES_TOP_CTRL Register

31	30	29	28	27	26	25	24
PMA_CMN_REFCLK_MODE	PMA_CMN_REFCLK_INT_MODE			PMA_CMN_REFCLK_DIG_DIV		RESERVED	
R/W-0h	R/W-0h			R/W-2h		R/W-X	
23	22	21	20	19	18	17	16
PHY_PMA_SU SPEND_OVER RIDE				RESERVED			
R/W-0h				R/W-X			
15	14	13	12	11	10	9	8
				RESERVED			
				R/W-X			
7	6	5	4	3	2	1	0
				RESERVED			
				R/W-X			

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-325. SERDES_TOP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PMA_CMN_REFCLK_MODE	R/W	0h	The PMA common differential reference clock mode - Sets the mode of operation for differential reference clock input. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 2'b 00 - 100 MHz and greater differential reference clock. 2'b 01 - 100 MHz and greater singled ended DC coupled test reference clock. 2'b 10 - Less than 100 MHz differential reference clock. 2'b 11 - Less than 100 MHz single ended DC coupled test reference clock.
29-28	PMA_CMN_REFCLK_INT_MODE	R/W	0h	The PMA common internal reference clock mode - Sets the mode of operation for internal reference clock input. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 2'b 00 - Reserved 2'b 01 - 100 MHz and greater reference clock 2'b 10 - Reserved 2'b 11 - Less than 100 MHz reference clock

Table 12-325. SERDES_TOP_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-26	PMA_CMN_REFCLK_DIG_DIV	R/W	2h	The PMA common reference clock digital divide ratio select - Must be set before the de-assertion of apb_preset_n/phy_reset_n. 2'b 00 - Divide by 1 (set for reference clock in the 19.2 to 27MHz range) 2'b 01 - Divide by 2 (Reserved) 2'b 10 - Divide by 4 (set for 100 MHz reference clock) 2'b 11 - Divide by 8 (set for 156.25MHz reference clock)
25-24	RESERVED	R/W	X	
23	PHY_PMA_SUSPEND_OVERRIDE	R/W	0h	The PHY PMA common suspend override enable: 1 = disables suspending the PMA common when all links are in low power state (L1 SS, PCIe P2, USB P3, power down disabled, etc.). 0 = PMA common will be suspended when all links are in low power state. Driving this pin high has no effect if the PMA common is already suspended or is in the process of being suspended (i.e. it will not force the PMA common to resume). It only prevents the start of suspending the PMA common. However, if this pin is de-asserted when all links are in low power state, the PMA common will then be suspended.
22-0	RESERVED	R/W	X	

Table 12-326. Register Call Summary for SERDES_TOP_CTRL

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [SERDES_TOP_CTRL Register \(Offset = 408h\) \[reset = X\]: \[0\]](#)

12.109 SERDES_RST Register (Offset = 40Ch) [reset = X]

SERDES_RST is shown in Figure 12-109 and described in Table 12-328.

Return to [Summary Table](#).

The SERDES Reset Register controls the Phy reset and REFCLK selection for the SERDES.

Table 12-327. SERDES_RST Instances

Instance	Physical Address
SERDES_10G0	0505 040Ch

Figure 12-109. SERDES_RST Register

31	30	29	28	27	26	25	24
PHY_RESET_N	PHY_EN_REFCLK	PLL1_REFCLK_SEL	PLL0_REFCLK_SEL	REFCLK_TERM_DIS	RESERVED		REFCLK_DIG_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-328. SERDES_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_RESET_N	R/W	0h	The PHY reset : Asserting this signal low will reset all PHY logic for the entire PHY with the exception of the APB registers and TAP controller. Note: Upon de-assertion, all PHY inputs must be driven as described in the PIPE specification for a PIPE reset.
30	PHY_EN_REFCLK	R/W	0h	The PHY reference clock enable: When cmn_refclk_<p/m> is configured as a reference clock output, 1 = glitch-less enable of the reference clock output. 0 = glitch-less turn off reference clock output. Used in L1.x entry/exit protocol. Note: When outputting a derived reference clock from the PLL, it is recommended to drive phy_en_refclk low until the PHY has completed start-up and de-asserted pipe_l*_reset_n for PIPE operation or asserted cmn_ready for Raw SERDES operation.. The clock will not be 'good' until the PHY has completed initial start-up.
29	PLL1_REFCLK_SEL	R/W	0h	The PMA common PLL1 reference clock source select - 0 - Selects cmn_refclk_<m/p> as reference clock source 1 - Selects pma_cmn_refclk_int as reference clock source. Note: This field is write protected when register field ~iphy_reset_n is a '1'.

Table 12-328. SERDES_RST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	PLL0_REFCLK_SEL	R/W	0h	The PMA common PLL0 reference clock source select - 0 - Selects cmn_refclk_<m/p> as reference clock source 1 - Selects pma_cmn_refclk_int as reference clock source. Note: This field is write protected when register field ~iphy_reset_n is a '1'.
27	REFCLK_TERM_DIS	R/W	0h	The PMA common differential reference clock termination disable - enables/disables termination for difference reference clock input (cmn_refclk_<p/m>). Must be set before the de-assertion of apb_preset_n/phy_reset_n. 1 = termination disabled 0 = termination enabled. Note: This field is write protected when register field ~iphy_reset_n is a '1'.
26-25	RESERVED	R/W	X	
24	REFCLK_DIG_SEL	R/W	0h	The PMA common reference clock select - Selects the reference clock source for the digital logic between cmn_refclk_<p/m> and pma_cmn_refclk_int. Must be set before the de-assertion of apb_preset_n/phy_reset_n. 0 - cmn_refclk_<p/m> 1 - pma_cmn_refclk_int. Note: This field is write protected when register field ~iphy_reset_n is a '1'.
23-0	RESERVED	R/W	X	

Table 12-329. Register Call Summary for SERDES_RST

10-G SerDes Registers

- [SERDES_RST Register \(Offset = 40Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.110 SERDES_TYPEC Register (Offset = 410h) [reset = X]

SERDES_TYPEC is shown in [Figure 12-110](#) and described in [Table 12-331](#).

Return to [Summary Table](#).

The SERDES Type C control register allows the external lanes selection to be swapped.

Table 12-330. SERDES_TYPEC Instances

Instance	Physical Address
SERDES_10G0	0505 0410h

Figure 12-110. SERDES_TYPEC Register

31	30	29	28	27	26	25	24
LN23_SWAP	LN10_SWAP	RESERVED					
R/W-0h	R/W-0h	R/W-X					
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-331. SERDES_TYPEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LN23_SWAP	R/W	0h	The ~iln23_swap will swap the lanes 2 and 3. That is all control for lane 2 will apply to lane 3 and vice versa. You cannot set ~iln23_swap to swap lanes in a link. That is If lanes 2 and 3 are used for a single link of PCIe, the ~iln23_swap must be '0'. Note: This field is write protected when register field ~iphy_reset_n is a '1'.
30	LN10_SWAP	R/W	0h	The ~iln10_swap will swap the lanes 0 and 1. That is all control for lane 0 will apply to lane 1 and vice versa. You cannot set ~iln10_swap to swap lanes in a link. That is If lanes 0 and 1 are used for a single link of PCIe, the ~iln10_swap must be '0'. Note: This field is write protected when register field ~iphy_reset_n is a '1'.
29-0	RESERVED	R/W	X	

Table 12-332. Register Call Summary for SERDES_TYPEC

10-G SerDes Registers

- [SERDES_TYPEC Register \(Offset = 410h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.111 LANECTLO Register (Offset = 480h) [reset = X]

LANECTLO is shown in [Figure 12-111](#) and described in [Table 12-334](#).

Return to [Summary Table](#).

The Lane Control Register sets the lane specific modes of operation.

Table 12-333. LANECTLO Instances

Instance	Physical Address
SERDES_10G0	0505 0480h

Figure 12-111. LANECTLO Register

31	30	29	28	27	26	25	24
P0_ENABLE	P0_FORCE_ENABLE	P0_ALIGN	P0_RAW_AUTO_START	RESERVED		P0_STANDARD_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h	
23	22	21	20	19	18	17	16
P0_FULLRT_DIV		P0_MAC_SRC_SEL		P0_REFCLK_SEL		RESERVED	
R/W-0h		R/W-0h		R/W-0h		R/W-X	
15	14	13	12	11	10	9	8
RESERVED						P0_TXFCLK_SEL	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
P0_RXFCLK_SEL		RESERVED					
R/W-0h		R/W-X					

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-334. LANECTLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P0_ENABLE	R/W	0h	The p0_enable is AND'd with the IPx_LNy_reset_n to enable the lane.
30	P0_FORCE_ENABLE	R/W	0h	The p0_force_enable is OR'd with the IPx_LNy_reset_n to force enable the lane.
29	P0_ALIGN	R/W	0h	The p0_align will auto align the RAW interface to 8B10B comma characters.
28	P0_RAW_AUTO_START	R/W	0h	The p0_raw_auto_start will auto sequence the RAW interface according to the configuration settings
27-26	RESERVED	R/W	X	
25-24	P0_STANDARD_MODE	R/W	0h	Standard Mode
23-22	P0_FULLRT_DIV	R/W	0h	Full Rate divider for 2x MAC speed mode. The PMA PLL full rate clock divider select - divide ratio for pma_pllclk_fullrt_in_*. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8

Table 12-334. LANECTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	P0_MAC_SRC_SEL	R/W	0h	MAC clock source select : Selects which PMA clock to use as clock source for pcs_mac_clk*_ln_*. 2'b 00 - PMA output xcvr_pll_clk_datart_ln_* for the associated lane. 2'b 01 - PMA output xcvr_pll_clk_fullrt_ln_* for the associated lane. 2'b 10 - PMA output cmn_ref_clk_rcv. 2'b 11 - Reserved
19-18	P0_REFCLK_SEL	R/W	0h	Refclk Select determines which clocks will be used for the IP refclk signal. 0 - pma_pllclk_fullrt_ln_0 is used. 1 - pcs_mac_clk_ln_0 is used. 2 - pcs_mac_clk_divx0_ln_0 is used. 3 - pcs_mac_clk_divx1_ln_0 is used.
17-10	RESERVED	R/W	X	
9-8	P0_TXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP txfclk signal. 0 - pma_pllclk_fullrt_ln_0 is used. 1 - pcs_mac_clk_ln_0 is used. 2 - pcs_mac_clk_divx0_ln_0 is used. 3 - pcs_mac_clk_divx1_ln_0 is used.
7-6	P0_RXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP rxfclk signal. 0 - pma_rx_rd_clk2x_ln_0 is used. 1 - pma_rx_rd_clk_ln_0 is used. 2 - rd_div2_clk0 is used. 3 - rd_div4_clk0 is used.
5-0	RESERVED	R/W	X	

Table 12-335. Register Call Summary for LANECTL0

10-G SerDes Registers

- [LANECTL0 Register \(Offset = 480h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.112 LANEDIV0 Register (Offset = 484h) [reset = X]

LANEDIV0 is shown in Figure 12-112 and described in Table 12-337.

Return to [Summary Table](#).

The Lane Divider Register sets the lane specific dividers of

Table 12-336. LANEDIV0 Instances

Instance	Physical Address
SERDES_10G0	0505 0484h

Figure 12-112. LANEDIV0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									P0_MAC_DIV_SEL0						
R/W-X									R/W-0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									P0_MAC_DIV_SEL1						
R/W-X									R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-337. LANEDIV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	P0_MAC_DIV_SEL0	R/W	0h	The reg_p0_mac_div_sel0 controls the divider for lane 0 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx0_in_*. 7'd 0 : Reserved 7'd 1 : Divide by 1 7'd 2 : Divide by 2 7'd 3 : Divide by 3 ... 7'd n : Divide by n, n = 127 (maximum)
15-9	RESERVED	R/W	X	
8-0	P0_MAC_DIV_SEL1	R/W	0h	The reg_p0_mac_div_sel1 controls the divider for lane 0 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx1_in_*. 9'd 0 : Reserved 9'd 1 : Divide by 1 9'd 2 : Divide by 2 9'd 3 : Divide by 3 ... 9'd n : Divide by n, n = 511 (maximum)

Table 12-338. Register Call Summary for LANEDIV0

10-G SerDes Registers

- [LANEDIV0 Register \(Offset = 484h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.113 LANALIGN0 Register (Offset = 488h) [reset = X]

LANALIGN0 is shown in [Figure 12-113](#) and described in [Table 12-340](#).

Return to [Summary Table](#).

The Lane Align reports the 8B10B alignment delay from the Comma aligner when 8B10B protocol is used in RAW mode.

Table 12-339. LANALIGN0 Instances

Instance	Physical Address
SERDES_10G0	0505 0488h

Figure 12-113. LANALIGN0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										P0_ALIGN_RX_DELAY					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 12-340. LANALIGN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	P0_ALIGN_RX_DELAY	R	0h	The reg_p0_align_rx_delay indicates the number of bits that are added to align the data to an 8B10B alignment. This value should be added to the latency of the receiver so that an accurate time of Time Sync packets can be calculated.

Table 12-341. Register Call Summary for LANALIGN0

10-G SerDes Registers

- [LANALIGN0 Register \(Offset = 488h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.114 LANESTS0 Register (Offset = 48Ch) [reset = X]

LANESTS0 is shown in [Figure 12-114](#) and described in [Table 12-343](#).

Return to [Summary Table](#).

The lane Status reports the lane state information for debug purposes.

Table 12-342. LANESTS0 Instances

Instance	Physical Address
SERDES_10G0	0505 048Ch

Figure 12-114. LANESTS0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						P0_MASTER	RESERVED
R-X						R-0h	R-X

LEGEND: R = Read Only; -n = value after reset

Table 12-343. LANESTS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	P0_MASTER	R	0h	The reg_p0_master indicates the lane is a base lane for a multi lane link. When '1' Lane is lane 0 of a multi lane link, When '0' lane is part of a multi lane link.
0	RESERVED	R	X	

Table 12-344. Register Call Summary for LANESTS0

10-G SerDes Registers

- [LANESTS0 Register \(Offset = 48Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.115 LANECTL1 Register (Offset = 4C0h) [reset = X]

LANECTL1 is shown in [Figure 12-115](#) and described in [Table 12-346](#).

Return to [Summary Table](#).

The Lane Control Register sets the lane specific modes of operation.

Table 12-345. LANECTL1 Instances

Instance	Physical Address
SERDES_10G0	0505 04C0h

Figure 12-115. LANECTL1 Register

31	30	29	28	27	26	25	24
P1_ENABLE	P1_FORCE_ENABLE	P1_ALIGN	P1_RAW_AUTO_START	RESERVED		P1_STANDARD_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h	
23	22	21	20	19	18	17	16
P1_FULLRT_DIV		P1_MAC_SRC_SEL		P1_REFCLK_SEL		RESERVED	
R/W-0h		R/W-0h		R/W-0h		R/W-X	
15	14	13	12	11	10	9	8
RESERVED						P1_TXFCLK_SEL	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
P1_RXFCLK_SEL		RESERVED					
R/W-0h		R/W-X					

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-346. LANECTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P1_ENABLE	R/W	0h	The p1_enable is AND'd with the IPx_LNy_reset_n to enable the lane.
30	P1_FORCE_ENABLE	R/W	0h	The p1_force_enable is OR'd with the IPx_LNy_reset_n to force enable the lane.
29	P1_ALIGN	R/W	0h	The p1_align will auto align the RAW interface to 8B10B comma characters.
28	P1_RAW_AUTO_START	R/W	0h	The p1_raw_auto_start will auto sequence the RAW interface according to the configuration settings
27-26	RESERVED	R/W	X	
25-24	P1_STANDARD_MODE	R/W	0h	Standard Mode
23-22	P1_FULLRT_DIV	R/W	0h	Full Rate divider for 2x MAC speed mode. The PMA PLL full rate clock divider select - divide ratio for pma_pllclk_fullrt_in_*. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8

Table 12-346. LANECTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	P1_MAC_SRC_SEL	R/W	0h	MAC clock source select : Selects which PMA clock to use as clock source for pcs_mac_clk*_ln_*. 2'b 00 - PMA output xcvr_pll_clk_datart_ln_* for the associated lane. 2'b 01 - PMA output xcvr_pll_clk_fullrt_ln_* for the associated lane. 2'b 10 - PMA output cmn_ref_clk_rcv. 2'b 11 - Reserved
19-18	P1_REFCLK_SEL	R/W	0h	Refclk Select determines which clocks will be used for the IP refclk signal. 0 - pma_pllclk_fullrt_ln_1 is used. 1 - pcs_mac_clk_ln_1 is used. 2 - pcs_mac_clk_divx0_ln_1 is used. 3 - pcs_mac_clk_divx1_ln_1 is used.
17-10	RESERVED	R/W	X	
9-8	P1_TXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP txfclk signal. 0 - pma_pllclk_fullrt_ln_1 is used. 1 - pcs_mac_clk_ln_1 is used. 2 - pcs_mac_clk_divx0_ln_1 is used. 3 - pcs_mac_clk_divx1_ln_1 is used.
7-6	P1_RXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP rxfclk signal. 0 - pma_rx_rd_clk2x_ln_1 is used. 1 - pma_rx_rd_clk_ln_1 is used. 2 - rd_div2_clk1 is used. 3 - rd_div4_clk1 is used.
5-0	RESERVED	R/W	X	

Table 12-347. Register Call Summary for LANECTL1

10-G SerDes Registers

- [LANECTL1 Register \(Offset = 4C0h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.116 LANEDIV1 Register (Offset = 4C4h) [reset = X]

LANEDIV1 is shown in [Figure 12-116](#) and described in [Table 12-349](#).

Return to [Summary Table](#).

The Lane Divider Register sets the lane specific dividers of

Table 12-348. LANEDIV1 Instances

Instance	Physical Address
SERDES_10G0	0505 04C4h

Figure 12-116. LANEDIV1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										P1_MAC_DIV_SEL0					
R/W-X										R/W-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										P1_MAC_DIV_SEL1					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-349. LANEDIV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	P1_MAC_DIV_SEL0	R/W	0h	The reg_p1_mac_div_sel0 controls the divider for lane 1 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx0_in_*. 7'd 0 : Reserved 7'd 1 : Divide by 1 7'd 2 : Divide by 2 7'd 3 : Divide by 3 ... 7'd n : Divide by n, n = 127 (maximum)
15-9	RESERVED	R/W	X	
8-0	P1_MAC_DIV_SEL1	R/W	0h	The reg_p1_mac_div_sel1 controls the divider for lane 1 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx1_in_*. 9'd 0 : Reserved 9'd 1 : Divide by 1 9'd 2 : Divide by 2 9'd 3 : Divide by 3 ... 9'd n : Divide by n, n = 511 (maximum)

Table 12-350. Register Call Summary for LANEDIV1

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [LANEDIV1 Register \(Offset = 4C4h\) \[reset = X\]: \[0\]](#)

12.117 LANALIGN1 Register (Offset = 4C8h) [reset = X]

LANALIGN1 is shown in [Figure 12-117](#) and described in [Table 12-352](#).

Return to [Summary Table](#).

The Lane Align reports the 8B10B alignment delay from the Comma aligner when 8B10B protocol is used in RAW mode.

Table 12-351. LANALIGN1 Instances

Instance	Physical Address
SERDES_10G0	0505 04C8h

Figure 12-117. LANALIGN1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										P1_ALIGN_RX_DELAY					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 12-352. LANALIGN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	P1_ALIGN_RX_DELAY	R	0h	The reg_p1_align_rx_delay indicates the number of bits that are added to align the data to an 8B10B alignment. This value should be added to the latency of the receiver so that an accurate time of Time Sync packets can be calculated.

Table 12-353. Register Call Summary for LANALIGN1

10-G SerDes Registers

- [LANALIGN1 Register \(Offset = 4C8h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.118 LANESTS1 Register (Offset = 4CCh) [reset = X]

LANESTS1 is shown in [Figure 12-118](#) and described in [Table 12-355](#).

Return to [Summary Table](#).

The lane Status reports the lane state information for debug purposes.

Table 12-354. LANESTS1 Instances

Instance	Physical Address
SERDES_10G0	0505 04CCh

Figure 12-118. LANESTS1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						P1_MASTER	RESERVED
R-X						R-0h	R-X

LEGEND: R = Read Only; -n = value after reset

Table 12-355. LANESTS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	P1_MASTER	R	0h	The reg_p1_master indicates the lane is a base lane for a multi lane link. When '1' Lane is lane 0 of a multi lane link, When '0' lane is part of a multi lane link.
0	RESERVED	R	X	

Table 12-356. Register Call Summary for LANESTS1

10-G SerDes Registers

- [LANESTS1 Register \(Offset = 4CCh\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.119 LANECTL2 Register (Offset = 500h) [reset = X]

LANECTL2 is shown in [Figure 12-119](#) and described in [Table 12-358](#).

Return to [Summary Table](#).

The Lane Control Register sets the lane specific modes of operation.

Table 12-357. LANECTL2 Instances

Instance	Physical Address
SERDES_10G0	0505 0500h

Figure 12-119. LANECTL2 Register

31	30	29	28	27	26	25	24
P2_ENABLE	P2_FORCE_ENABLE	P2_ALIGN	P2_RAW_AUTO_START	RESERVED		P2_STANDARD_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h	
23	22	21	20	19	18	17	16
P2_FULLRT_DIV		P2_MAC_SRC_SEL		P2_REFCLK_SEL		RESERVED	
R/W-0h		R/W-0h		R/W-0h		R/W-X	
15	14	13	12	11	10	9	8
RESERVED						P2_TXFCLK_SEL	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
P2_RXFCLK_SEL		RESERVED					
R/W-0h		R/W-X					

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-358. LANECTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P2_ENABLE	R/W	0h	The p2_enable is AND'd with the IPx_LNy_reset_n to enable the lane.
30	P2_FORCE_ENABLE	R/W	0h	The p2_force_enable is OR'd with the IPx_LNy_reset_n to force enable the lane.
29	P2_ALIGN	R/W	0h	The p2_align will auto align the RAW interface to 8B10B comma characters.
28	P2_RAW_AUTO_START	R/W	0h	The p2_raw_auto_start will auto sequence the RAW interface according to the configuration settings
27-26	RESERVED	R/W	X	
25-24	P2_STANDARD_MODE	R/W	0h	Standard Mode
23-22	P2_FULLRT_DIV	R/W	0h	Full Rate divider for 2x MAC speed mode. The PMA PLL full rate clock divider select - divide ratio for pma_pllclk_fullrt_in_*. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8

Table 12-358. LANECTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	P2_MAC_SRC_SEL	R/W	0h	MAC clock source select : Selects which PMA clock to use as clock source for pcs_mac_clk*_ln_*. 2'b 00 - PMA output xcvr_pll_clk_datart_ln_* for the associated lane. 2'b 01 - PMA output xcvr_pll_clk_fullrt_ln_* for the associated lane. 2'b 10 - PMA output cmn_ref_clk_rcv. 2'b 11 - Reserved
19-18	P2_REFCLK_SEL	R/W	0h	Refclk Select determines which clocks will be used for the IP refclk signal. 0 - pma_pllclk_fullrt_ln_2 is used. 1 - pcs_mac_clk_ln_2 is used. 2 - pcs_mac_clk_divx0_ln_2 is used. 3 - pcs_mac_clk_divx1_ln_2 is used.
17-10	RESERVED	R/W	X	
9-8	P2_TXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP txfclk signal. 0 - pma_pllclk_fullrt_ln_2 is used. 1 - pcs_mac_clk_ln_2 is used. 2 - pcs_mac_clk_divx0_ln_2 is used. 3 - pcs_mac_clk_divx1_ln_2 is used.
7-6	P2_RXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP rxfclk signal. 0 - pma_rx_rd_clk2x_ln_2 is used. 1 - pma_rx_rd_clk_ln_2 is used. 2 - rd_div2_clk2 is used. 3 - rd_div4_clk2 is used.
5-0	RESERVED	R/W	X	

Table 12-359. Register Call Summary for LANECTL2

10-G SerDes Registers

- [LANECTL2 Register \(Offset = 500h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.120 LANEDIV2 Register (Offset = 504h) [reset = X]

LANEDIV2 is shown in Figure 12-120 and described in Table 12-361.

Return to [Summary Table](#).

The Lane Divider Register sets the lane specific dividers of

Table 12-360. LANEDIV2 Instances

Instance	Physical Address
SERDES_10G0	0505 0504h

Figure 12-120. LANEDIV2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									P2_MAC_DIV_SEL0						
R/W-X									R/W-0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									P2_MAC_DIV_SEL1						
R/W-X									R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-361. LANEDIV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	P2_MAC_DIV_SEL0	R/W	0h	The reg_p2_mac_div_sel0 controls the divider for lane 2 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx0_in_*. 7'd 0 : Reserved 7'd 1 : Divide by 1 7'd 2 : Divide by 2 7'd 3 : Divide by 3 ... 7'd n : Divide by n n = 127 (maximum)
15-9	RESERVED	R/W	X	
8-0	P2_MAC_DIV_SEL1	R/W	0h	The reg_p2_mac_div_sel1 controls the divider for lane 2 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx1_in_*. 9'd 0 : Reserved 9'd 1 : Divide by 1 9'd 2 : Divide by 2 9'd 3 : Divide by 3 ... 9'd n : Divide by n n = 511 (maximum)

Table 12-362. Register Call Summary for LANEDIV2

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [LANEDIV2 Register \(Offset = 504h\) \[reset = X\]: \[0\]](#)

12.121 LANALIGN2 Register (Offset = 508h) [reset = X]

LANALIGN2 is shown in [Figure 12-121](#) and described in [Table 12-364](#).

Return to [Summary Table](#).

The Lane Align reports the 8B10B alignment delay from the Comma aligner when 8B10B protocol is used in RAW mode.

Table 12-363. LANALIGN2 Instances

Instance	Physical Address
SERDES_10G0	0505 0508h

Figure 12-121. LANALIGN2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										P2_ALIGN_RX_DELAY					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 12-364. LANALIGN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	P2_ALIGN_RX_DELAY	R	0h	The reg_p2_align_rx_delay indicates the number of bits that are added to align the data to an 8B10B alignment. This value should be added to the latency of the receiver so that an accurate time of Time Sync packets can be calculated.

Table 12-365. Register Call Summary for LANALIGN2

10-G SerDes Registers

- [LANALIGN2 Register \(Offset = 508h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.122 LANESTS2 Register (Offset = 50Ch) [reset = X]

LANESTS2 is shown in [Figure 12-122](#) and described in [Table 12-367](#).

Return to [Summary Table](#).

The lane Status reports the lane state information for debug purposes.

Table 12-366. LANESTS2 Instances

Instance	Physical Address
SERDES_10G0	0505 050Ch

Figure 12-122. LANESTS2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						P2_MASTER	RESERVED
R-X						R-0h	R-X

LEGEND: R = Read Only; -n = value after reset

Table 12-367. LANESTS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	P2_MASTER	R	0h	The reg_p2_master indicates the lane is a base lane for a multi lane link. When '1' Lane is lane 0 of a multi lane link, When '0' lane is part of a multi lane link.
0	RESERVED	R	X	

Table 12-368. Register Call Summary for LANESTS2

10-G SerDes Registers

- [LANESTS2 Register \(Offset = 50Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.123 LANECTL3 Register (Offset = 540h) [reset = X]

LANECTL3 is shown in [Figure 12-123](#) and described in [Table 12-370](#).

Return to [Summary Table](#).

The Lane Control Register sets the lane specific modes of operation.

Table 12-369. LANECTL3 Instances

Instance	Physical Address
SERDES_10G0	0505 0540h

Figure 12-123. LANECTL3 Register

31	30	29	28	27	26	25	24
P3_ENABLE	P3_FORCE_ENABLE	P3_ALIGN	P3_RAW_AUTO_START	RESERVED		P3_STANDARD_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X		R/W-0h	
23	22	21	20	19	18	17	16
P3_FULLRT_DIV		P3_MAC_SRC_SEL		P3_REFCLK_SEL		RESERVED	
R/W-0h		R/W-0h		R/W-0h		R/W-X	
15	14	13	12	11	10	9	8
RESERVED						P3_TXFCLK_SEL	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
P3_RXFCLK_SEL		RESERVED					
R/W-0h		R/W-X					

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-370. LANECTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	P3_ENABLE	R/W	0h	The p3_enable is AND'd with the IPx_LNy_reset_n to enable the lane.
30	P3_FORCE_ENABLE	R/W	0h	The p3_force_enable is OR'd with the IPx_LNy_reset_n to force enable the lane.
29	P3_ALIGN	R/W	0h	The p3_align will auto align the RAW interface to 8B10B comma characters.
28	P3_RAW_AUTO_START	R/W	0h	The p3_raw_auto_start will auto sequence the RAW interface according to the configuration settings
27-26	RESERVED	R/W	X	
25-24	P3_STANDARD_MODE	R/W	0h	Standard Mode
23-22	P3_FULLRT_DIV	R/W	0h	Full Rate divider for 2x MAC speed mode. The PMA PLL full rate clock divider select - divide ratio for pma_pllclk_fullrt_in_*. 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8

Table 12-370. LANECTL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-20	P3_MAC_SRC_SEL	R/W	0h	MAC clock source select : Selects which PMA clock to use as clock source for pcs_mac_clk*_ln_*. 2'b 00 - PMA output xcvr_pll_clk_datart_ln_* for the associated lane. 2'b 01 - PMA output xcvr_pll_clk_fullrt_ln_* for the associated lane. 2'b 10 - PMA output cmn_ref_clk_rcv. 2'b 11 - Reserved
19-18	P3_REFCLK_SEL	R/W	0h	Refclk Select determines which clocks will be used for the IP refclk signal. 0 - pma_pllclk_fullrt_ln_3 is used. 1 - pcs_mac_clk_ln_3 is used. 2 - pcs_mac_clk_divx0_ln_3 is used. 3 - pcs_mac_clk_divx1_ln_3 is used.
17-10	RESERVED	R/W	X	
9-8	P3_TXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP txfclk signal. 0 - pma_pllclk_fullrt_ln_3 is used. 1 - pcs_mac_clk_ln_3 is used. 2 - pcs_mac_clk_divx0_ln_3 is used. 3 - pcs_mac_clk_divx1_ln_3 is used.
7-6	P3_RXFCLK_SEL	R/W	0h	Fclk Select determines which clocks will be used for the IP rxfclk signal. 0 - pma_rx_rd_clk2x_ln_3 is used. 1 - pma_rx_rd_clk_ln_3 is used. 2 - rd_div2_clk3 is used. 3 - rd_div4_clk3 is used.
5-0	RESERVED	R/W	X	

Table 12-371. Register Call Summary for LANECTL3

10-G SerDes Registers

- [LANECTL3 Register \(Offset = 540h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.124 LANEDIV3 Register (Offset = 544h) [reset = X]

LANEDIV3 is shown in [Figure 12-124](#) and described in [Table 12-373](#).

Return to [Summary Table](#).

The Lane Divider Register sets the lane specific dividers of

Table 12-372. LANEDIV3 Instances

Instance	Physical Address
SERDES_10G0	0505 0544h

Figure 12-124. LANEDIV3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									P3_MAC_DIV_SEL0						
R/W-X									R/W-0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									P3_MAC_DIV_SEL1						
R/W-X									R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-373. LANEDIV3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	P3_MAC_DIV_SEL0	R/W	0h	The reg_p3_mac_div_sel0 controls the divider for lane 3 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx0_in_*. 7'd 0 : Reserved 7'd 1 : Divide by 1 7'd 2 : Divide by 2 7'd 3 : Divide by 3 ... 7'd n : Divide by n n = 127 (maximum)
15-9	RESERVED	R/W	X	
8-0	P3_MAC_DIV_SEL1	R/W	0h	The reg_p3_mac_div_sel1 controls the divider for lane 3 MAC clock divider ratio select : Selects the divider ratio for pcs_mac_clk_divx1_in_*. 9'd 0 : Reserved 9'd 1 : Divide by 1 9'd 2 : Divide by 2 9'd 3 : Divide by 3 ... 9'd n : Divide by n n = 511 (maximum)

Table 12-374. Register Call Summary for LANEDIV3

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [LANEDIV3 Register \(Offset = 544h\) \[reset = X\]: \[0\]](#)

12.125 LANALIGN3 Register (Offset = 548h) [reset = X]

LANALIGN3 is shown in [Figure 12-125](#) and described in [Table 12-376](#).

Return to [Summary Table](#).

The Lane Align reports the 8B10B alignment delay from the Comma aligner when 8B10B protocol is used in RAW mode.

Table 12-375. LANALIGN3 Instances

Instance	Physical Address
SERDES_10G0	0505 0548h

Figure 12-125. LANALIGN3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										P3_ALIGN_RX_DELAY					
R-X										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 12-376. LANALIGN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	P3_ALIGN_RX_DELAY	R	0h	The reg_p3_align_rx_delay indicates the number of bits that are added to align the data to an 8B10B alignment. This value should be added to the latency of the receiver so that an accurate time of Time Sync packets can be calculated.

Table 12-377. Register Call Summary for LANALIGN3

10-G SerDes Registers

- [LANALIGN3 Register \(Offset = 548h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.126 LANESTS3 Register (Offset = 54Ch) [reset = X]

LANESTS3 is shown in [Figure 12-126](#) and described in [Table 12-379](#).

Return to [Summary Table](#).

The lane Status reports the lane state information for debug purposes.

Table 12-378. LANESTS3 Instances

Instance	Physical Address
SERDES_10G0	0505 054Ch

Figure 12-126. LANESTS3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						P3_MASTER	RESERVED
R-X						R-0h	R-X

LEGEND: R = Read Only; -n = value after reset

Table 12-379. LANESTS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1	P3_MASTER	R	0h	The reg_p3_master indicates the lane is a base lane for a multi lane link. When '1' Lane is lane 0 of a multi lane link, When '0' lane is part of a multi lane link.
0	RESERVED	R	X	

Table 12-380. Register Call Summary for LANESTS3

10-G SerDes Registers

- [LANESTS3 Register \(Offset = 54Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.127 DTB_MUX_SEL Register (Offset = 5F8h) [reset = X]

DTB_MUX_SEL is shown in [Figure 12-127](#) and described in [Table 12-382](#).

Return to [Summary Table](#).

The digital test bus mux select determines the value on the test bus.

Table 12-381. DTB_MUX_SEL Instances

Instance	Physical Address
SERDES_10G0	0505 05F8h

Figure 12-127. DTB_MUX_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												DTB_MUX_SEL			
R/W-X												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-382. DTB_MUX_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	DTB_MUX_SEL	R/W	0h	

Table 12-383. Register Call Summary for DTB_MUX_SEL

10-G SerDes Registers

- [DTB_MUX_SEL Register \(Offset = 5F8h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.128 DIAG_TEST Register (Offset = 5FCh) [reset = 0h]

DIAG_TEST is shown in [Figure 12-128](#) and described in [Table 12-385](#).

Return to [Summary Table](#).

The Diagnostic Test Register allows the system to validate the read and write of all data bits.

Table 12-384. DIAG_TEST Instances

Instance	Physical Address
SERDES_10G0	0505 05FCh

Figure 12-128. DIAG_TEST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIAG_REG																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-385. DIAG_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIAG_REG	R/W	0h	Diagnostic register. This register allows full read/write of all data bits to be tested.

Table 12-386. Register Call Summary for DIAG_TEST

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [DIAG_TEST Register \(Offset = 5FCh\) \[reset = 0h\]: \[0\]](#)

12.129 RESERVEDBIT13ADDRESSA_y Register (Offset = 2000h + formula) [reset = 0h]

RESERVEDBIT13ADDRESSA_y is shown in Figure 12-129 and described in Table 12-388.

Return to [Summary Table](#).

Reserved Address bit 13 area A

Offset = 2000h + (y * 4h); where y = 0h to 7FFh

**Table 12-387. RESERVEDBIT13ADDRESSA_y
Instances**

Instance	Physical Address
SERDES_10G0	0505 2000h + formula

Figure 12-129. RESERVEDBIT13ADDRESSA_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES_BIT13_ADR_A																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-388. RESERVEDBIT13ADDRESSA_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES_BIT13_ADR_A	R/W	0h	Write only test region A

Table 12-389. Register Call Summary for RESERVEDBIT13ADDRESSA_y

10-G SerDes Registers

- [RESERVEDBIT13ADDRESSA_y Register \(Offset = 2000h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.130 XCVR_PSM_RCTRL_XCVR_PSM_CTRL_j Register (Offset = 4000h + formula) [reset = BCFC0201h]

XCVR_PSM_RCTRL_XCVR_PSM_CTRL_j is shown in Figure 12-130 and described in Table 12-391.

Return to [Summary Table](#).

Power state machine control register

Offset = 4000h + (j * 400h); where j = 0h to 3h

Table 12-390.
XCVR_PSM_RCTRL_XCVR_PSM_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 4000h + formula

Figure 12-130. XCVR_PSM_RCTRL_XCVR_PSM_CTRL_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_R_CTRL_15	XCVR_PSM_R_CTRL_14	XCVR_PSM_R_CTRL_13	XCVR_PSM_R_CTRL_12	XCVR_PSM_R_CTRL_11	XCVR_PSM_R_CTRL_10	XCVR_PSM_R_CTRL_9	XCVR_PSM_R_CTRL_8
R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
XCVR_PSM_R_CTRL_7	XCVR_PSM_R_CTRL_6	XCVR_PSM_R_CTRL_5	XCVR_PSM_R_CTRL_4	XCVR_PSM_R_CTRL_3	XCVR_PSM_R_CTRL_2	XCVR_PSM_R_CTRL_1	XCVR_PSM_R_CTRL_0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
XCVR_PSM_C_TRL_15	XCVR_PSM_C_TRL_14	XCVR_PSM_C_TRL_13	XCVR_PSM_C_TRL_12	XCVR_PSM_C_TRL_11	XCVR_PSM_C_TRL_10	XCVR_PSM_C_TRL_9	XCVR_PSM_C_TRL_8
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R-0h
7	6	5	4	3	2	1	0
XCVR_PSM_CTRL_7_1							XCVR_PSM_C_TRL_0
R-0h							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-391. XCVR_PSM_RCTRL_XCVR_PSM_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	XCVR_PSM_RCTRL_15	R/W	1h	RX reset active ready : Controls the state the receiver reset is changed to when in the ready power state. 1'b 0: Reset not active 1'b 1: Reset active
30	XCVR_PSM_RCTRL_14	R/W	0h	RX reset active calibration : Controls the state the receiver reset is changed to when in the calibration power state. 1'b 0: Reset not active 1'b 1: Reset active
29	XCVR_PSM_RCTRL_13	R/W	1h	RX reset active A5 : Controls the state the receiver reset is changed to when in the A5 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
28	XCVR_PSM_RCTRL_12	R/W	1h	RX reset active A4 : Controls the state the receiver reset is changed to when in the A4 entry power state. 1'b 0: Reset not active 1'b 1: Reset active

Table 12-391. XCVR_PSM_RCTRL_XCVR_PSM_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	XCVR_PSM_RCTRL_11	R/W	1h	RX reset active A3 : Controls the state the receiver reset is changed to when in the A3 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
26	XCVR_PSM_RCTRL_10	R/W	1h	RX reset active A2 : Controls the state the receiver reset is changed to when in the A2 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
25	XCVR_PSM_RCTRL_9	R/W	0h	RX reset active A1 : Controls the state the receiver reset is changed to when in the A1 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
24	XCVR_PSM_RCTRL_8	R/W	0h	RX reset active A0 : Controls the state the receiver reset is changed to when in the A0 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
23	XCVR_PSM_RCTRL_7	R/W	1h	TX reset active ready : Controls the state the transmitter reset is changed to when in the ready power state. 1'b 0: Reset not active 1'b 1: Reset active
22	XCVR_PSM_RCTRL_6	R/W	1h	TX reset active calibration : Controls the state the transmitter reset is changed to when in the calibration power state. 1'b 0: Reset not active 1'b 1: Reset active
21	XCVR_PSM_RCTRL_5	R/W	1h	TX reset active A5 : Controls the state the transmitter reset is changed to when in the A5 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
20	XCVR_PSM_RCTRL_4	R/W	1h	TX reset active A4 : Controls the state the transmitter reset is changed to when in the A4 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
19	XCVR_PSM_RCTRL_3	R/W	1h	TX reset active A3 : Controls the state the transmitter reset is changed to when in the A3 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
18	XCVR_PSM_RCTRL_2	R/W	1h	TX reset active A2 : Controls the state the transmitter reset is changed to when in the A2 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
17	XCVR_PSM_RCTRL_1	R/W	0h	TX reset active A1 : Controls the state the transmitter reset is changed to when in the A1 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
16	XCVR_PSM_RCTRL_0	R/W	0h	TX reset active A0 : Controls the state the transmitter reset is changed to when in the A0 entry power state. 1'b 0: Reset not active 1'b 1: Reset active
15	XCVR_PSM_CTRL_15	R	0h	Reserved

Table 12-391. XCVR_PSM_RCTRL_XCVR_PSM_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	XCVR_PSM_CTRL_14	R/W	0h	<p>Bypass A0 in delay from PSM ready : When this bit is active (1'b1), the A0 input delay is bypassed when transitioning from the PSM ready state to the A0 power state.</p> <p>The result of this is the amount of time spent in the A0 in delay state is the value specified in the A0 in bypass timer register.</p> <p>The intention of this bit is to bypass the delay for cases when the required analog components being controlled are already enabled in the ready power state, and no additional delay is required when transitioning to the A0 power state.</p>
13	XCVR_PSM_CTRL_13	R/W	0h	<p>Bypass A0 in delay from A5 : When this bit is active (1'b1), the A0 input delay is bypassed when transitioning from the A5 to the A0 power state.</p> <p>The result of this is the amount of time spent in the A0 in delay state is the value specified in the A0 in bypass timer register.</p> <p>The intention of this bit is to bypass the delay for cases when the required analog components being controlled are already enabled in the A5 power state, and no additional delay is required when transitioning to the A0 power state.</p>
12	XCVR_PSM_CTRL_12	R/W	0h	<p>Bypass A0 in delay from A4 : When this bit is active (1'b1), the A0 input delay is bypassed when transitioning from the A4 to the A0 power state.</p> <p>The result of this is the amount of time spent in the A0 in delay state is the value specified in the A0 in bypass timer register.</p> <p>The intention of this bit is to bypass the delay for cases when the required analog components being controlled are already enabled in the A4 power state, and no additional delay is required when transitioning to the A0 power state.</p>
11	XCVR_PSM_CTRL_11	R/W	0h	<p>Bypass A0 in delay from A3 : When this bit is active (1'b1), the A0 input delay is bypassed when transitioning from the A3 to the A0 power state.</p> <p>The result of this is the amount of time spent in the A0 in delay state is the value specified in the A0 in bypass timer register.</p> <p>The intention of this bit is to bypass the delay for cases when the required analog components being controlled are already enabled in the A3 power state, and no additional delay is required when transitioning to the A0 power state.</p>
10	XCVR_PSM_CTRL_10	R/W	0h	<p>Bypass A0 in delay from A2 : When this bit is active (1'b1), the A0 input delay is bypassed when transitioning from the A2 to the A0 power state.</p> <p>The result of this is the amount of time spent in the A0 in delay state is the value specified in the A0 in bypass timer register.</p> <p>The intention of this bit is to bypass the delay for cases when the required analog components being controlled are already enabled in the A2 power state, and no additional delay is required when transitioning to the A0 power state.</p>

Table 12-391. XCVR_PSM_RCTRL__XCVR_PSM_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	XCVR_PSM_CTRL_9	R/W	1h	Bypass A0 in delay from A1 : When this bit is active (1'b1), the A0 input delay is bypassed when transitioning from the A1 to the A0 power state. The result of this is the amount of time spent in the A0 in delay state is the value specified in the A0 in bypass timer register. The intention of this bit is to bypass the delay for cases when the required analog components being controlled are already enabled in the A1 power state, and no additional delay is required when transitioning to the A0 power state.
8	XCVR_PSM_CTRL_8	R	0h	Reserved
7-1	XCVR_PSM_CTRL_7_1	R	0h	Reserved
0	XCVR_PSM_CTRL_0	R/W	1h	Reserved - spare (must remain set to 1'b1).

Table 12-392. Register Call Summary for XCVR_PSM_RCTRL__XCVR_PSM_CTRL_j

10-G SerDes Registers

- [XCVR_PSM_RCTRL__XCVR_PSM_CTRL_j Register \(Offset = 4000h + formula\) \[reset = BCFC0201h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.131 XCVR_PSM_A0IN_TMR_XCVR_PSM_CALIN_TMR_j Register (Offset = 4004h + formula) [reset = 00960096h]

XCVR_PSM_A0IN_TMR_XCVR_PSM_CALIN_TMR_j is shown in Figure 12-131 and described in Table 12-394.

Return to [Summary Table](#).

PSM calibration in delay timer register

Offset = 4004h + (j * 400h); where j = 0h to 3h

Table 12-393. XCVR_PSM_A0IN_TMR_XCVR_PSM_CALIN_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 4004h + formula

Figure 12-131. XCVR_PSM_A0IN_TMR_XCVR_PSM_CALIN_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_A0IN_TMR_15_12				XCVR_PSM_A0IN_TMR_11_0			
R-0h				R/W-96h			
23	22	21	20	19	18	17	16
XCVR_PSM_A0IN_TMR_11_0							
R/W-96h							
15	14	13	12	11	10	9	8
XCVR_PSM_CALIN_TMR_15_12				XCVR_PSM_CALIN_TMR_11_0			
R-0h				R/W-96h			
7	6	5	4	3	2	1	0
XCVR_PSM_CALIN_TMR_11_0							
R/W-96h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-394. XCVR_PSM_A0IN_TMR_XCVR_PSM_CALIN_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	XCVR_PSM_A0IN_TMR_15_12	R	0h	Reserved
27-16	XCVR_PSM_A0IN_TMR_11_0	R/W	96h	A0 in delay state timer value : Value used for the timer when the power state machine is in the A0 in delay state, unless the timer is bypassed under the control of the bypass A0 bits in the Power state machine control register. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A0_in_del. Note, the smallest value this field is allowed to be is 12'h001. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.
15-12	XCVR_PSM_CALIN_TMR_15_12	R	0h	Reserved

Table 12-394. XCVR_PSM_A0IN_TMR__XCVR_PSM_CALIN_TMR_j Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
11-0	XCVR_PSM_CALIN_TMR_11_0	R/W	96h	<p>PSM calibration in delay state timer value : Value used for the timer when the power state machine is in the PSM calibration in delay state.</p> <p>This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_lane_cal_in_del.</p> <p>Note, the smallest value this field is allowed to be is 12'h001.</p> <p>With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.</p>

Table 12-395. Register Call Summary for XCVR_PSM_A0IN_TMR__XCVR_PSM_CALIN_TMR_j

10-G SerDes Registers

- [XCVR_PSM_A0IN_TMR__XCVR_PSM_CALIN_TMR_j Register \(Offset = 4004h + formula\) \[reset = 00960096h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.132 XCVR_PSM_A1IN_TMR_XCVR_PSM_A0BYP_TMR_j Register (Offset = 4008h + formula) [reset = 0010000Ah]

XCVR_PSM_A1IN_TMR_XCVR_PSM_A0BYP_TMR_j is shown in Figure 12-132 and described in Table 12-397.

Return to [Summary Table](#).

A0 in bypass timer register

Offset = 4008h + (j * 400h); where j = 0h to 3h

Table 12-396. XCVR_PSM_A1IN_TMR_XCVR_PSM_A0BYP_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 4008h + formula

Figure 12-132. XCVR_PSM_A1IN_TMR_XCVR_PSM_A0BYP_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_A1IN_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_A1IN_TMR_15_6		XCVR_PSM_A1IN_TMR_5_0					
R-0h		R/W-10h					
15	14	13	12	11	10	9	8
XCVR_PSM_A0BYP_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
XCVR_PSM_A0BYP_TMR_15_6		XCVR_PSM_A0BYP_TMR_5_0					
R-0h		R/W-Ah					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-397. XCVR_PSM_A1IN_TMR_XCVR_PSM_A0BYP_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	XCVR_PSM_A1IN_TMR_15_6	R	0h	Reserved
21-16	XCVR_PSM_A1IN_TMR_5_0	R/W	10h	A1 in delay state timer value : Value used for the timer when the power state machine is in the A1 in delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A1_in_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.
15-6	XCVR_PSM_A0BYP_TMR_15_6	R	0h	Reserved
5-0	XCVR_PSM_A0BYP_TMR_5_0	R/W	Ah	A0 in delay state bypass timer value : Value used for the timer when the power state machine is in the A0 in delay state and the timer is bypassed under the control of the bypass A0 bits in the Power state machine control register. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A0_in_byp. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.

Table 12-398. Register Call Summary for XCVR_PSM_A1IN_TMR__XCVR_PSM_A0BYP_TMR_j

10-G SerDes Registers

- [XCVR_PSM_A1IN_TMR__XCVR_PSM_A0BYP_TMR_j](#) Register (Offset = 4008h + formula) [reset = 0010000Ah]: [0]
- 10-G SerDes Registers: [0]

12.133 XCVR_PSM_A3IN_TMR_XCVR_PSM_A2IN_TMR_j Register (Offset = 400Ch + formula) [reset = 00100010h]

XCVR_PSM_A3IN_TMR_XCVR_PSM_A2IN_TMR_j is shown in Figure 12-133 and described in Table 12-400.

Return to [Summary Table](#).

A2 in delay timer register

Offset = 400Ch + (j * 400h); where j = 0h to 3h

Table 12-399. XCVR_PSM_A3IN_TMR_XCVR_PSM_A2IN_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 400Ch + formula

Figure 12-133. XCVR_PSM_A3IN_TMR_XCVR_PSM_A2IN_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_A3IN_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_A3IN_TMR_15_6		XCVR_PSM_A3IN_TMR_5_0					
R-0h		R/W-10h					
15	14	13	12	11	10	9	8
XCVR_PSM_A2IN_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
XCVR_PSM_A2IN_TMR_15_6		XCVR_PSM_A2IN_TMR_5_0					
R-0h		R/W-10h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-400. XCVR_PSM_A3IN_TMR_XCVR_PSM_A2IN_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	XCVR_PSM_A3IN_TMR_15_6	R	0h	Reserved
21-16	XCVR_PSM_A3IN_TMR_5_0	R/W	10h	A3 in delay state timer value : Value used for the timer when the power state machine is in the A3 in delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A3_in_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.
15-6	XCVR_PSM_A2IN_TMR_15_6	R	0h	Reserved
5-0	XCVR_PSM_A2IN_TMR_5_0	R/W	10h	A2 in delay state timer value : Value used for the timer when the power state machine is in the A2 in delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A2_in_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.

Table 12-401. Register Call Summary for XCVR_PSM_A3IN_TMR__XCVR_PSM_A2IN_TMR_j

10-G SerDes Registers

- [XCVR_PSM_A3IN_TMR__XCVR_PSM_A2IN_TMR_j](#) Register (Offset = 400Ch + formula) [reset = 00100010h]: [0]
- [10-G SerDes Registers](#): [0]

12.134 XCVR_PSM_A5IN_TMR_XCVR_PSM_A4IN_TMR_j Register (Offset = 4010h + formula) [reset = 00100010h]

XCVR_PSM_A5IN_TMR_XCVR_PSM_A4IN_TMR_j is shown in Figure 12-134 and described in Table 12-403.

Return to [Summary Table](#).

A4 in delay timer register

Offset = 4010h + (j * 400h); where j = 0h to 3h

Table 12-402. XCVR_PSM_A5IN_TMR_XCVR_PSM_A4IN_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 4010h + formula

Figure 12-134. XCVR_PSM_A5IN_TMR_XCVR_PSM_A4IN_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_A5IN_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_A5IN_TMR_15_6		XCVR_PSM_A5IN_TMR_5_0					
R-0h		R/W-10h					
15	14	13	12	11	10	9	8
XCVR_PSM_A4IN_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
XCVR_PSM_A4IN_TMR_15_6		XCVR_PSM_A4IN_TMR_5_0					
R-0h		R/W-10h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-403. XCVR_PSM_A5IN_TMR_XCVR_PSM_A4IN_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	XCVR_PSM_A5IN_TMR_15_6	R	0h	Reserved
21-16	XCVR_PSM_A5IN_TMR_5_0	R/W	10h	A5 in delay state timer value : Value used for the timer when the power state machine is in the A5 in delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A5_in_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.
15-6	XCVR_PSM_A4IN_TMR_15_6	R	0h	Reserved
5-0	XCVR_PSM_A4IN_TMR_5_0	R/W	10h	A4 in delay state timer value : Value used for the timer when the power state machine is in the A4 in delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A4_in_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.

Table 12-404. Register Call Summary for XCVR_PSM_A5IN_TMR__XCVR_PSM_A4IN_TMR_j

10-G SerDes Registers

- [XCVR_PSM_A5IN_TMR__XCVR_PSM_A4IN_TMR_j](#) Register (Offset = 4010h + formula) [reset = 00100010h]: [0]
- [10-G SerDes Registers](#): [0]

12.135 XCVR_PSM_A0OUT_TMR__XCVR_PSM_CALOUT_TMR_j Register (Offset = 4014h + formula) [reset = 00010001h]

XCVR_PSM_A0OUT_TMR__XCVR_PSM_CALOUT_TMR_j is shown in Figure 12-135 and described in Table 12-406.

Return to [Summary Table](#).

PSM calibration out delay timer register

Offset = 4014h + (j * 400h); where j = 0h to 3h

Table 12-405. XCVR_PSM_A0OUT_TMR__XCVR_PSM_CALOUT_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 4014h + formula

Figure 12-135. XCVR_PSM_A0OUT_TMR__XCVR_PSM_CALOUT_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_A0OUT_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_A0OUT_TMR_15_6				XCVR_PSM_A0OUT_TMR_5_0			
R-0h				R/W-1h			
15	14	13	12	11	10	9	8
XCVR_PSM_CALOUT_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
XCVR_PSM_CALOUT_TMR_15_6				XCVR_PSM_CALOUT_TMR_5_0			
R-0h				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-406. XCVR_PSM_A0OUT_TMR__XCVR_PSM_CALOUT_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	XCVR_PSM_A0OUT_TM R_15_6	R	0h	Reserved
21-16	XCVR_PSM_A0OUT_TM R_5_0	R/W	1h	A0 out delay state timer value : Value used for the timer when the power state machine is in the A0 out delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A0_out_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.
15-6	XCVR_PSM_CALOUT_T MR_15_6	R	0h	Reserved
5-0	XCVR_PSM_CALOUT_T MR_5_0	R/W	1h	PSM calibration out delay state timer value : Value used for the timer when the power state machine is in the PSM calibration out delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_lane_cal_out_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.

Table 12-407. Register Call Summary for XCVR_PSM_A0OUT_TMR__XCVR_PSM_CALOUT_TMR_j

10-G SerDes Registers <ul style="list-style-type: none"> 10-G SerDes Registers: [0] XCVR_PSM_A0OUT_TMR__XCVR_PSM_CALOUT_TMR_j Register (Offset = 4014h + formula) [reset = 00010001h]: [0]
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12.136 XCVR_PSM_A2OUT_TMR_XCVR_PSM_A1OUT_TMR_j Register (Offset = 4018h + formula) [reset = 00010001h]

XCVR_PSM_A2OUT_TMR_XCVR_PSM_A1OUT_TMR_j is shown in Figure 12-136 and described in Table 12-409.

Return to [Summary Table](#).

A1 out delay timer register

Offset = 4018h + (j * 400h); where j = 0h to 3h

Table 12-408. XCVR_PSM_A2OUT_TMR_XCVR_PSM_A1OUT_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 4018h + formula

Figure 12-136. XCVR_PSM_A2OUT_TMR_XCVR_PSM_A1OUT_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_A2OUT_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_A2OUT_TMR_15_6				XCVR_PSM_A2OUT_TMR_5_0			
R-0h				R/W-1h			
15	14	13	12	11	10	9	8
XCVR_PSM_A1OUT_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
XCVR_PSM_A1OUT_TMR_15_6				XCVR_PSM_A1OUT_TMR_5_0			
R-0h				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-409. XCVR_PSM_A2OUT_TMR_XCVR_PSM_A1OUT_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	XCVR_PSM_A2OUT_TM_R_15_6	R	0h	Reserved
21-16	XCVR_PSM_A2OUT_TM_R_5_0	R/W	1h	A2 out delay state timer value : Value used for the timer when the power state machine is in the A2 out delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A2_out_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.
15-6	XCVR_PSM_A1OUT_TM_R_15_6	R	0h	Reserved
5-0	XCVR_PSM_A1OUT_TM_R_5_0	R/W	1h	A1 out delay state timer value : Value used for the timer when the power state machine is in the A1 out delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A1_out_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.

Table 12-410. Register Call Summary for XCVR_PSM_A2OUT_TMR__XCVR_PSM_A1OUT_TMR_j

10-G SerDes Registers

- [XCVR_PSM_A2OUT_TMR__XCVR_PSM_A1OUT_TMR_j](#) Register (Offset = 4018h + formula) [reset = 00010001h]: [0]
- 10-G SerDes Registers: [0]

12.137 XCVR_PSM_A4OUT_TMR_XCVR_PSM_A3OUT_TMR_j Register (Offset = 401Ch + formula) [reset = 00010001h]

XCVR_PSM_A4OUT_TMR_XCVR_PSM_A3OUT_TMR_j is shown in [Figure 12-137](#) and described in [Table 12-412](#).

Return to [Summary Table](#).

A3 out delay timer register

Offset = 401Ch + (j * 400h); where j = 0h to 3h

Table 12-411. XCVR_PSM_A4OUT_TMR_XCVR_PSM_A3OUT_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 401Ch + formula

Figure 12-137. XCVR_PSM_A4OUT_TMR_XCVR_PSM_A3OUT_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_A4OUT_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_A4OUT_TMR_15_6				XCVR_PSM_A4OUT_TMR_5_0			
R-0h				R/W-1h			
15	14	13	12	11	10	9	8
XCVR_PSM_A3OUT_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
XCVR_PSM_A3OUT_TMR_15_6				XCVR_PSM_A3OUT_TMR_5_0			
R-0h				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-412. XCVR_PSM_A4OUT_TMR_XCVR_PSM_A3OUT_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	XCVR_PSM_A4OUT_TM_R_15_6	R	0h	Reserved
21-16	XCVR_PSM_A4OUT_TM_R_5_0	R/W	1h	A4 out delay state timer value : Value used for the timer when the power state machine is in the A4 out delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A4_out_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.
15-6	XCVR_PSM_A3OUT_TM_R_15_6	R	0h	Reserved
5-0	XCVR_PSM_A3OUT_TM_R_5_0	R/W	1h	A3 out delay state timer value : Value used for the timer when the power state machine is in the A3 out delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A3_out_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.

Table 12-413. Register Call Summary for XCVR_PSM_A4OUT_TMR__XCVR_PSM_A3OUT_TMR_j

10-G SerDes Registers

- [XCVR_PSM_A4OUT_TMR__XCVR_PSM_A3OUT_TMR_j](#) Register (Offset = 401Ch + formula) [reset = 00010001h]: [0]
- 10-G SerDes Registers: [0]

12.138 XCVR_PSM_RDY_TMR__XCVR_PSM_A5OUT_TMR_j Register (Offset = 4020h + formula) [reset = 00100001h]

XCVR_PSM_RDY_TMR__XCVR_PSM_A5OUT_TMR_j is shown in [Figure 12-138](#) and described in [Table 12-415](#).

Return to [Summary Table](#).

A5 out delay timer register

Offset = 4020h + (j * 400h); where j = 0h to 3h

Table 12-414. XCVR_PSM_RDY_TMR__XCVR_PSM_A5OUT_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 4020h + formula

Figure 12-138. XCVR_PSM_RDY_TMR__XCVR_PSM_A5OUT_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_RDY_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_RDY_TMR_15_6		XCVR_PSM_RDY_TMR_5_0					
R-0h		R/W-10h					
15	14	13	12	11	10	9	8
XCVR_PSM_A5OUT_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
XCVR_PSM_A5OUT_TMR_15_6		XCVR_PSM_A5OUT_TMR_5_0					
R-0h		R/W-1h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-415. XCVR_PSM_RDY_TMR__XCVR_PSM_A5OUT_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	XCVR_PSM_RDY_TMR_15_6	R	0h	Reserved
21-16	XCVR_PSM_RDY_TMR_5_0	R/W	10h	Ready delay state timer value : Value used for the timer when the power state machine is in the ready state. This timer delay is specified as the number of PSM clocks to count to implement the minimum time (tpsm_rdy_out_del.) required to remain in this state. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.
15-6	XCVR_PSM_A5OUT_TMR_15_6	R	0h	Reserved
5-0	XCVR_PSM_A5OUT_TMR_5_0	R/W	1h	A5 out delay state timer value : Value used for the timer when the power state machine is in the A5 out delay state. This timer delay is specified as the number of PSM clocks to count to implement the time required for tpsm_A5_out_del. Note, the smallest value this field is allowed to be is 6'h01. With that said, setting this field to a value smaller than the reset value will likely result in incorrect function.

Table 12-416. Register Call Summary for XCVR_PSM_RDY_TMR__XCVR_PSM_A5OUT_TMR_j

<div> 10-G SerDes Registers <ul style="list-style-type: none"> XCVR_PSM_RDY_TMR__XCVR_PSM_A5OUT_TMR_j Register (Offset = 4020h + formula) [reset = 00100001h]: [0] 10-G SerDes Registers: [0] </div>
--

12.139 XCVR_PSM_ST_0__XCVR_PSM_DIAG_j Register (Offset = 4024h + formula) [reset = 0h]

XCVR_PSM_ST_0__XCVR_PSM_DIAG_j is shown in Figure 12-139 and described in Table 12-418.

Return to [Summary Table](#).

Power state machine diagnostic register

Offset = 4024h + (j * 400h); where j = 0h to 3h

Table 12-417.
XCVR_PSM_ST_0__XCVR_PSM_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 4024h + formula

Figure 12-139. XCVR_PSM_ST_0__XCVR_PSM_DIAG_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_ST_0_15_0							
R-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_ST_0_15_0							
R-0h							
15	14	13	12	11	10	9	8
XCVR_PSM_DI AG_15	XCVR_PSM_DI AG_14	XCVR_PSM_DI AG_13	XCVR_PSM_DI AG_12	XCVR_PSM_DI AG_11	XCVR_PSM_DI AG_10	XCVR_PSM_DI AG_9	XCVR_PSM_DI AG_8
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
XCVR_PSM_DI AG_7	XCVR_PSM_DI AG_6	XCVR_PSM_DI AG_5	XCVR_PSM_DI AG_4	XCVR_PSM_DI AG_3	XCVR_PSM_DI AG_2	XCVR_PSM_DI AG_1	XCVR_PSM_DI AG_0
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-418. XCVR_PSM_ST_0__XCVR_PSM_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	XCVR_PSM_ST_0_15_0	R	0h	PSM current state [15:0] : Indicates bits 15:0 of the current state of the power state machine.
15	XCVR_PSM_DIAG_15	R	0h	Reserved
14	XCVR_PSM_DIAG_14	R/W	0h	Force calibration exit acknowledge : Setting this bit to 1'b1 forces the psm_cal_exit_ack pin of the power state machine active.
13	XCVR_PSM_DIAG_13	R/W	0h	Force A5 exit acknowledge : Setting this bit to 1'b1 forces the psm_a5_exit_ack pin of the power state machine active.
12	XCVR_PSM_DIAG_12	R/W	0h	Force A4 exit acknowledge : Setting this bit to 1'b1 forces the psm_a4_exit_ack pin of the power state machine active.
11	XCVR_PSM_DIAG_11	R/W	0h	Force A3 exit acknowledge : Setting this bit to 1'b1 forces the psm_a3_exit_ack pin of the power state machine active.
10	XCVR_PSM_DIAG_10	R/W	0h	Force A2 exit acknowledge : Setting this bit to 1'b1 forces the psm_a2_exit_ack pin of the power state machine active.
9	XCVR_PSM_DIAG_9	R/W	0h	Force A1 exit acknowledge : Setting this bit to 1'b1 forces the psm_a1_exit_ack pin of the power state machine active.
8	XCVR_PSM_DIAG_8	R/W	0h	Force A0 exit acknowledge : Setting this bit to 1'b1 forces the psm_a0_exit_ack pin of the power state machine active.
7	XCVR_PSM_DIAG_7	R	0h	Reserved

Table 12-418. XCVR_PSM_ST_0__XCVR_PSM_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	XCVR_PSM_DIAG_6	R/W	0h	Force calibration entry acknowledge : Setting this bit to 1'b1 forces the psm_cal_entry_ack pin of the power state machine active.
5	XCVR_PSM_DIAG_5	R/W	0h	Force A5 entry acknowledge : Setting this bit to 1'b1 forces the psm_a5_entry_ack pin of the power state machine active.
4	XCVR_PSM_DIAG_4	R/W	0h	Force A4 entry acknowledge : Setting this bit to 1'b1 forces the psm_a4_entry_ack pin of the power state machine active.
3	XCVR_PSM_DIAG_3	R/W	0h	Force A3 entry acknowledge : Setting this bit to 1'b1 forces the psm_a3_entry_ack pin of the power state machine active.
2	XCVR_PSM_DIAG_2	R/W	0h	Force A2 entry acknowledge : Setting this bit to 1'b1 forces the psm_a2_entry_ack pin of the power state machine active.
1	XCVR_PSM_DIAG_1	R/W	0h	Force A1 entry acknowledge : Setting this bit to 1'b1 forces the psm_a1_entry_ack pin of the power state machine active.
0	XCVR_PSM_DIAG_0	R/W	0h	Force A0 entry acknowledge : Setting this bit to 1'b1 forces the psm_a0_entry_ack pin of the power state machine active.

Table 12-419. Register Call Summary for XCVR_PSM_ST_0__XCVR_PSM_DIAG_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [XCVR_PSM_ST_0__XCVR_PSM_DIAG_j Register \(Offset = 4024h + formula\) \[reset = 0h\]: \[0\]](#)

12.140 XCVR_PSM_ST_1_j Register (Offset = 4028h + formula) [reset = X]

XCVR_PSM_ST_1_j is shown in [Figure 12-140](#) and described in [Table 12-421](#).

Return to [Summary Table](#).

PSM current state register 1

Offset = 4028h + (j * 400h); where j = 0h to 3h

Table 12-420. XCVR_PSM_ST_1_j Instances

Instance	Physical Address
SERDES_10G0	0505 4028h + formula

Figure 12-140. XCVR_PSM_ST_1_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
XCVR_PSM_ST_1_15_10						XCVR_PSM_ST_1_9_0	
R-0h						R-0h	
7	6	5	4	3	2	1	0
XCVR_PSM_ST_1_9_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 12-421. XCVR_PSM_ST_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-10	XCVR_PSM_ST_1_15_10	R	0h	Reserved
9-0	XCVR_PSM_ST_1_9_0	R	0h	PSM current state [25:16] : Indicates bits 25:16 of the current state of the power state machine.

Table 12-422. Register Call Summary for XCVR_PSM_ST_1_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [XCVR_PSM_ST_1_j Register \(Offset = 4028h + formula\) \[reset = X\]: \[0\]](#)

12.141 XCVR_PSM_USER_DEF_CTRL_j Register (Offset = 403Ch + formula) [reset = X]

XCVR_PSM_USER_DEF_CTRL_j is shown in [Figure 12-141](#) and described in [Table 12-424](#).

Return to [Summary Table](#).

Power state machine user defined control register

Offset = 403Ch + (j * 400h); where j = 0h to 3h

**Table 12-423. XCVR_PSM_USER_DEF_CTRL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 403Ch + formula

Figure 12-141. XCVR_PSM_USER_DEF_CTRL_j Register

31	30	29	28	27	26	25	24
XCVR_PSM_USER_DEF_CTRL_15_5							
R/W-0h							
23	22	21	20	19	18	17	16
XCVR_PSM_USER_DEF_CTRL_15_5			XCVR_PSM_U SER_DEF_CTR L_4	XCVR_PSM_USER_DEF_CTRL_3_0			
R/W-0h			R/W-0h	R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-424. XCVR_PSM_USER_DEF_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	XCVR_PSM_USER_DEF_CTRL_15_5	R/W	0h	Reserved - spare
20	XCVR_PSM_USER_DEF_CTRL_4	R/W	0h	Force PSM gated clock on: Setting this bit to 1'b1 will force the PSM gated clock on, independent of the internal PSM state machine clock gate controls.
19-16	XCVR_PSM_USER_DEF_CTRL_3_0	R/W	0h	Reserved - spare
15-0	RESERVED	R/W	X	

Table 12-425. Register Call Summary for XCVR_PSM_USER_DEF_CTRL_j

10-G SerDes Registers

- [XCVR_PSM_USER_DEF_CTRL_j Register \(Offset = 403Ch + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.142 TX_TXCC_PRE_OVRD__TX_TXCC_CTRL_j Register (Offset = 4080h + formula) [reset = 2A84h]

TX_TXCC_PRE_OVRD__TX_TXCC_CTRL_j is shown in Figure 12-142 and described in Table 12-427.

Return to [Summary Table](#).

TX coefficient controller control register

Offset = 4080h + (j * 400h); where j = 0h to 3h

Table 12-426.
TX_TXCC_PRE_OVRD__TX_TXCC_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 4080h + formula

Figure 12-142. TX_TXCC_PRE_OVRD__TX_TXCC_CTRL_j Register

31	30	29	28	27	26	25	24
TX_TXCC_PRE_OVRD_15_9							TX_TXCC_PRE_OVRD_8
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TX_TXCC_PRE_OVRD_7_6		TX_TXCC_PRE_OVRD_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
TX_TXCC_CTRL_15_14		TX_TXCC_CTRL_13_12		TX_TXCC_CTRL_11_10		TX_TXCC_CTRL_9_8	
R-0h		R/W-2h		R/W-2h		R/W-2h	
7	6	5	4	3	2	1	0
TX_TXCC_CTRL_7_6		TX_TXCC_CTRL_5_4		TX_TXCC_CTRL_L_3	TX_TXCC_CTRL_L_2	TX_TXCC_CTRL_L_1	TX_TXCC_CTRL_L_0
R/W-2h		R/W-0h		R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-427. TX_TXCC_PRE_OVRD__TX_TXCC_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	TX_TXCC_PRE_OVRD_15_9	R	0h	Reserved
24	TX_TXCC_PRE_OVRD_8	R/W	0h	Pre-cursor override enable: When enabled, the pre-cursor field in this register is used to override the pre-cursor value.
23-22	TX_TXCC_PRE_OVRD_7_6	R	0h	Reserved

Table 12-427. TX_TXCC_PRE_OVRD_TX_TXCC_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	TX_TXCC_PRE_OVRD_5_0	R/W	0h	<p>Pre-cursor override value: When enabled by the pre-cursor override enable bit in this register, the value in this field is used to override the pre-cursor value.</p> <p>Note that this field is 6 bits wide, to match the pre-cursor data input width on the tx_deemphasis input pin, only the least significant 5 bits are used to actually drive the H bridge driver controller.</p> <p>In the calculated modes, this will override the calculated pre-cursor value.</p> <p>Note : This register is for diagnostic purposes only.</p> <p>When this field is used, one must make sure that the value does not result in the H bridge driver controller input pin restrictions being violated.</p> <p>These restrictions are documented in the pin list of H bridge driver controller specification.</p>
15-14	TX_TXCC_CTRL_15_14	R	0h	Reserved
13-12	TX_TXCC_CTRL_13_12	R/W	2h	<p>Margin multiplier rounding control: This field controls the rounding function on the margin multiplier.</p> <p>2'b 00 : Round to nearest integer</p> <p>2'b 01 : Floor</p> <p>2'b 10 : Ceiling</p>
11-10	TX_TXCC_CTRL_11_10	R/W	2h	<p>LF value multiplier rounding control: This field controls the rounding function on the LF value multiplier.</p> <p>2'b 00 : Round to nearest integer</p> <p>2'b 01 : Floor</p> <p>2'b 10 : Ceiling</p>
9-8	TX_TXCC_CTRL_9_8	R/W	2h	<p>Calculated post-emphasis multiplier rounding control: This field controls the rounding function on the calculated post-emphasis multiplier.</p> <p>2'b 00 : Round to nearest integer</p> <p>2'b 01 : Floor</p> <p>2'b 10 : Ceiling</p>
7-6	TX_TXCC_CTRL_7_6	R/W	2h	<p>Calculated pre-emphasis multiplier rounding control: This field controls the rounding function on the pre-emphasis multiplier.</p> <p>2'b 00 : Round to nearest integer</p> <p>2'b 01 : Floor</p> <p>2'b 10 : Ceiling</p>
5-4	TX_TXCC_CTRL_5_4	R/W	0h	<p>Coefficient calculator multiplier rounding control: This field controls the rounding function on the coefficient calculator multiplier.</p> <p>2'b 00 : Round to nearest integer</p> <p>2'b 01 : Floor</p> <p>2'b 10 : Ceiling</p>
3	TX_TXCC_CTRL_3	R/W	0h	<p>De-emphasis control standard mode 3 value: This bit controls the de-emphasis mode when the xcvr_standard_mode is set to 2'b11.</p> <p>1'b 0 : Use the calculated de-emphasis values based on the 2 least significant bits of the top level tx_deemphasis signal.</p> <p>1'b 1 : Use the coefficient values on all 18 bits of the top level tx_deemphasis signal.</p>

Table 12-427. TX_TXCC_PRE_OVRD__TX_TXCC_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TX_TXCC_CTRL_2	R/W	1h	De-emphasis control standard mode 2 value: This bit controls the de-emphasis mode when the xcvr_standard_mode is set to 2'b10. 1'b 0 : Use the calculated de-emphasis values based on the 2 least significant bits of the top level tx_deemphasis signal. 1'b 1 : Use the coefficient values on all 18 bits of the top level tx_deemphasis signal.
1	TX_TXCC_CTRL_1	R/W	0h	De-emphasis control standard mode 1 value: This bit controls the de-emphasis mode when the xcvr_standard_mode is set to 2'b01. 1'b 0 : Use the calculated de-emphasis values based on the 2 least significant bits of the top level tx_deemphasis signal. 1'b 1 : Use the coefficient values on all 18 bits of the top level tx_deemphasis signal.
0	TX_TXCC_CTRL_0	R/W	0h	De-emphasis control standard mode 0 value: This bit controls the de-emphasis mode when the xcvr_standard_mode is set to 2'b00. 1'b 0 : Use the calculated de-emphasis values based on the 2 least significant bits of the top level tx_deemphasis signal. 1'b 1 : Use the coefficient values on all 18 bits of the top level tx_deemphasis signal.

Table 12-428. Register Call Summary for TX_TXCC_PRE_OVRD__TX_TXCC_CTRL_j

10-G SerDes Registers

- [TX_TXCC_PRE_OVRD__TX_TXCC_CTRL_j Register \(Offset = 4080h + formula\) \[reset = 2A84h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.143 TX_TXCC_POST_OVRD__TX_TXCC_MAIN_OVRD_j Register (Offset = 4084h + formula) [reset = 0h]

TX_TXCC_POST_OVRD__TX_TXCC_MAIN_OVRD_j is shown in Figure 12-143 and described in Table 12-430.

Return to [Summary Table](#).

TX main-cursor override register

Offset = 4084h + (j * 400h); where j = 0h to 3h

Table 12-429. TX_TXCC_POST_OVRD__TX_TXCC_MAIN_OVRD_j Instances

Instance	Physical Address
SERDES_10G0	0505 4084h + formula

Figure 12-143. TX_TXCC_POST_OVRD__TX_TXCC_MAIN_OVRD_j Register

31	30	29	28	27	26	25	24
TX_TXCC_POST_OVRD_15_9							TX_TXCC_POS T_OVRD_8
R-0h							R/W-0h
23	22	21	20	19	18	17	16
TX_TXCC_POST_OVRD_7_6		TX_TXCC_POST_OVRD_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
TX_TXCC_MAIN_OVRD_15_9							TX_TXCC_MAI N_OVRD_8
R-0h							R/W-0h
7	6	5	4	3	2	1	0
TX_TXCC_MAIN_OVRD_7_6		TX_TXCC_MAIN_OVRD_5_0					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-430. TX_TXCC_POST_OVRD__TX_TXCC_MAIN_OVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	TX_TXCC_POST_OVRD_15_9	R	0h	Reserved
24	TX_TXCC_POST_OVRD_8	R/W	0h	Post-cursor override enable: When enabled, the post-cursor field in this register is used to override the post-cursor value.
23-22	TX_TXCC_POST_OVRD_7_6	R	0h	Reserved

Table 12-430. TX_TXCC_POST_OVRD__TX_TXCC_MAIN_OVRD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	TX_TXCC_POST_OVRD_5_0	R/W	0h	<p>Post-cursor override value: When enabled by the post-cursor override enable bit in this register, the value in this field is used to override the post-cursor value.</p> <p>Note that this field is 6 bits wide, to match the post-cursor data input width on the tx_deemphasis input pin, only the least significant 5 bits are used to actually drive the H bridge driver controller.</p> <p>In the calculated modes, this will override the calculated post-cursor value.</p> <p>Note : This register is for diagnostic purposes only.</p> <p>When this field is used, one must make sure that the value does not result in the H bridge driver controller input pin restrictions being violated.</p> <p>These restrictions are documented in the pin list of H bridge driver controller specification.</p>
15-9	TX_TXCC_MAIN_OVRD_15_9	R	0h	Reserved
8	TX_TXCC_MAIN_OVRD_8	R/W	0h	Main-cursor override enable: When enabled, the main-cursor field in this register is used to override the main-cursor value.
7-6	TX_TXCC_MAIN_OVRD_7_6	R	0h	Reserved
5-0	TX_TXCC_MAIN_OVRD_5_0	R/W	0h	<p>Main-cursor override value: When enabled by the main-cursor override enable bit in this register, the value in this field is used to override the main-cursor value.</p> <p>Note that this field is 6 bits wide, to match the main-cursor data input width on the tx_deemphasis input pin, only the least significant 5 bits are used to actually drive the H bridge driver controller.</p> <p>In the calculated modes, this will override the calculated main-cursor value.</p> <p>Note : This register is for diagnostic purposes only.</p> <p>When this field is used, one must make sure that the value does not result in the H bridge driver controller input pin restrictions being violated.</p> <p>These restrictions are documented in the pin list of H bridge driver controller specification.</p>

Table 12-431. Register Call Summary for TX_TXCC_POST_OVRD__TX_TXCC_MAIN_OVRD_j

10-G SerDes Registers

- [TX_TXCC_POST_OVRD__TX_TXCC_MAIN_OVRD_j Register \(Offset = 4084h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.144 TX_TXCC_MAIN_CVAL__TX_TXCC_PRE_CVAL_j Register (Offset = 4088h + formula) [reset = 0h]

TX_TXCC_MAIN_CVAL__TX_TXCC_PRE_CVAL_j is shown in Figure 12-144 and described in Table 12-433.

Return to [Summary Table](#).

TX pre-cursor current value register

Offset = 4088h + (j * 400h); where j = 0h to 3h

Table 12-432.
TX_TXCC_MAIN_CVAL__TX_TXCC_PRE_CVAL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 4088h + formula

Figure 12-144. TX_TXCC_MAIN_CVAL__TX_TXCC_PRE_CVAL_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MAIN_CVAL_15_6							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MAIN_CVAL_15_6		TX_TXCC_MAIN_CVAL_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
TX_TXCC_PRE_CVAL_15_6							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_PRE_CVAL_15_6		TX_TXCC_PRE_CVAL_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 12-433. TX_TXCC_MAIN_CVAL__TX_TXCC_PRE_CVAL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	TX_TXCC_MAIN_CVAL_15_6	R	0h	Reserved
21-16	TX_TXCC_MAIN_CVAL_5_0	R	0h	<p>Main-cursor value: The value in this field indicates the current value of the main-cursor (C0) coefficient.</p> <p>The value of this field can be any of the following, depending on the current mode of operation.</p> <p>The override value when override is enabled, under the control of the TX main-cursor override register</p> <p>The main-cursor data on the tx_deemphasis input pin when the calculated de-emphasis values are disabled, under the control of the TX coefficient controller control register .</p> <p>All 0s when the calculated de-emphasis values are enabled, under the control of the TX coefficient controller control register .</p> <p>Note: The value of this is a function of input values and internal logic. Therefore, there is not a fixed reset value.</p>
15-6	TX_TXCC_PRE_CVAL_15_6	R	0h	Reserved

Table 12-433. TX_TXCC_MAIN_CVAL__TX_TXCC_PRE_CVAL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	TX_TXCC_PRE_CVAL_5_0	R	0h	<p>Pre-cursor value: The value in this field indicates the current value of the pre-cursor (C-1) coefficient.</p> <p>The value of this field can be any of the following, depending on the current mode of operation.</p> <p>The override value when override is enabled, under the control of the TX pre-cursor override register</p> <p>The pre-cursor data on the tx_deemphasis input pin when the calculated de-emphasis values are disabled, under the control of the TX coefficient controller control register .</p> <p>The internally calculated pre-cursor value when the calculated de-emphasis values are enabled, under the control of the TX coefficient controller control register .</p> <p>Note: The value of this is a function of input values and internal logic. Therefore, there is not a fixed reset value.</p>

Table 12-434. Register Call Summary for TX_TXCC_MAIN_CVAL__TX_TXCC_PRE_CVAL_j

10-G SerDes Registers

- [TX_TXCC_MAIN_CVAL__TX_TXCC_PRE_CVAL_j Register \(Offset = 4088h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.145 TX_TXCC_LF_MULT__TX_TXCC_POST_CVAL_j Register (Offset = 408Ch + formula) [reset = 002A0000h]

TX_TXCC_LF_MULT__TX_TXCC_POST_CVAL_j is shown in [Figure 12-145](#) and described in [Table 12-436](#).

Return to [Summary Table](#).

TX post-cursor current value register

Offset = 408Ch + (j * 400h); where j = 0h to 3h

Table 12-435.
TX_TXCC_LF_MULT__TX_TXCC_POST_CVAL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 408Ch + formula

Figure 12-145. TX_TXCC_LF_MULT__TX_TXCC_POST_CVAL_j Register

31	30	29	28	27	26	25	24
TX_TXCC_LF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_LF_MULT_7_0							
R/W-2Ah							
15	14	13	12	11	10	9	8
TX_TXCC_POST_CVAL_15_6							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_POST_CVAL_15_6				TX_TXCC_POST_CVAL_5_0			
R-0h				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-436. TX_TXCC_LF_MULT__TX_TXCC_POST_CVAL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_LF_MULT_15_8	R	0h	Reserved
23-16	TX_TXCC_LF_MULT_7_0	R/W	2Ah	<p>LF multiplier value: The value in this field specifies the multiplier value used to generate the LF value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000</p> <p>Bit 6 : 64/ 128 = 0.500000</p> <p>Bit 5 : 32/ 128 = 0.250000</p> <p>Bit 4 : 16/ 128 = 0.125000</p> <p>Bit 3 : 8/ 128 = 0.062500</p> <p>Bit 2 : 4/ 128 = 0.031250</p> <p>Bit 1 : 2/ 128 = 0.015625</p> <p>Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-436. TX_TXCC_LF_MULT__TX_TXCC_POST_CVAL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-6	TX_TXCC_POST_CVAL_15_6	R	0h	Reserved
5-0	TX_TXCC_POST_CVAL_5_0	R	0h	<p>Post-cursor value: The value in this field indicates the current value of the post-cursor (C+1) coefficient.</p> <p>The value of this field can be any of the following, depending on the current mode of operation.</p> <p>The override value when override is enabled, under the control of the TX post-cursor override register</p> <p>The post-cursor data on the tx_deemphasis input pin when the calculated de-emphasis values are disabled, under the control of the TX coefficient controller control register .</p> <p>The internally calculated post-cursor value when the calculated de-emphasis values are enabled, under the control of the TX coefficient controller control register .</p> <p>Note: The value of this is a function of input values and internal logic. Therefore, there is not a fixed reset value.</p>

Table 12-437. Register Call Summary for TX_TXCC_LF_MULT__TX_TXCC_POST_CVAL_j

10-G SerDes Registers

- [TX_TXCC_LF_MULT__TX_TXCC_POST_CVAL_j Register \(Offset = 408Ch + formula\) \[reset = 002A0000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.146 TX_TXCC_CPRES_MULT_01__TX_TXCC_CPRES_MULT_00_j Register (Offset = 4090h + formula) [reset = 0h]

TX_TXCC_CPRES_MULT_01__TX_TXCC_CPRES_MULT_00_j is shown in Figure 12-146 and described in Table 12-439.

Return to [Summary Table](#).

Calculated pre emphasis multiplier value 00 register

Offset = 4090h + (j * 400h); where j = 0h to 3h

**Table 12-438. TX_TXCC_CPRES_MULT_01__TX_TXCC_CPRES_MULT_00_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 4090h + formula

Figure 12-146. TX_TXCC_CPRES_MULT_01__TX_TXCC_CPRES_MULT_00_j Register

31	30	29	28	27	26	25	24
TX_TXCC_CPRES_MULT_01_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_CPRES_MULT_01_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_TXCC_CPRES_MULT_00_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_CPRES_MULT_00_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-439. TX_TXCC_CPRES_MULT_01__TX_TXCC_CPRES_MULT_00_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_CPRES_MULT_01_15_8	R	0h	Reserved
23-16	TX_TXCC_CPRES_MULT_01_7_0	R/W	0h	<p>Calculated pre emphasis multiplier value 01: The value in this field specifies the multiplier value used to generate the calculated pre emphasis value from the FS value when tx_deemphasis[1:0] = 2'b01. The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

**Table 12-439. TX_TXCC_CPRES_MULT_01__TX_TXCC_CPRES_MULT_00_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15-8	TX_TXCC_CPRES_MULT_00_15_8	R	0h	Reserved
7-0	TX_TXCC_CPRES_MULT_00_7_0	R/W	0h	<p>Calculated pre emphasis multiplier value 00: The value in this field specifies the multiplier value used to generate the calculated pre emphasis value from the FS value when tx_deemphasis[1:0] = 2'b00. The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-440. Register Call Summary for TX_TXCC_CPRES_MULT_01__TX_TXCC_CPRES_MULT_00_j

10-G SerDes Registers

- [TX_TXCC_CPRES_MULT_01__TX_TXCC_CPRES_MULT_00_j Register \(Offset = 4090h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.147 TX_TXCC_CPRES_MULT_11_TX_TXCC_CPRES_MULT_10_j Register (Offset = 4094h + formula) [reset = 0h]

TX_TXCC_CPRES_MULT_11_TX_TXCC_CPRES_MULT_10_j is shown in Figure 12-147 and described in Table 12-442.

Return to [Summary Table](#).

Calculated pre emphasis multiplier value 10 register

Offset = 4094h + (j * 400h); where j = 0h to 3h

**Table 12-441. TX_TXCC_CPRES_MULT_11_TX_TXCC_CPRES_MULT_10_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 4094h + formula

Figure 12-147. TX_TXCC_CPRES_MULT_11_TX_TXCC_CPRES_MULT_10_j Register

31	30	29	28	27	26	25	24
TX_TXCC_CPRES_MULT_11_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_CPRES_MULT_11_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_TXCC_CPRES_MULT_10_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_CPRES_MULT_10_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-442. TX_TXCC_CPRES_MULT_11_TX_TXCC_CPRES_MULT_10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_CPRES_MULT_11_15_8	R	0h	Reserved
23-16	TX_TXCC_CPRES_MULT_11_7_0	R/W	0h	<p>Calculated pre emphasis multiplier value 11: The value in this field specifies the multiplier value used to generate the calculated pre emphasis value from the FS value when tx_deemphasis[1:0] = 2'b11. The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

**Table 12-442. TX_TXCC_CPRES_MULT_11__TX_TXCC_CPRES_MULT_10_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15-8	TX_TXCC_CPRES_MULT_10_15_8	R	0h	Reserved
7-0	TX_TXCC_CPRES_MULT_10_7_0	R/W	0h	<p>Calculated pre emphasis multiplier value 10: The value in this field specifies the multiplier value used to generate the calculated pre emphasis value from the FS value when tx_deemphasis[1:0] = 2'b10. The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-443. Register Call Summary for TX_TXCC_CPRES_MULT_11__TX_TXCC_CPRES_MULT_10_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_TXCC_CPRES_MULT_11__TX_TXCC_CPRES_MULT_10_j Register \(Offset = 4094h + formula\) \[reset = 0h\]: \[0\]](#)

12.148 TX_TXCC_CPOST_MULT_01__TX_TXCC_CPOST_MULT_00_j Register (Offset = 4098h + formula) [reset = 0011001Ch]

TX_TXCC_CPOST_MULT_01__TX_TXCC_CPOST_MULT_00_j is shown in Figure 12-148 and described in Table 12-445.

Return to [Summary Table](#).

Calculated post emphasis multiplier value 00 register

Offset = 4098h + (j * 400h); where j = 0h to 3h

Table 12-444. TX_TXCC_CPOST_MULT_01__TX_TXCC_CPOST_MULT_00_j Instances

Instance	Physical Address
SERDES_10G0	0505 4098h + formula

Figure 12-148. TX_TXCC_CPOST_MULT_01__TX_TXCC_CPOST_MULT_00_j Register

31	30	29	28	27	26	25	24
TX_TXCC_CPOST_MULT_01_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_CPOST_MULT_01_7_0							
R/W-11h							
15	14	13	12	11	10	9	8
TX_TXCC_CPOST_MULT_00_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_CPOST_MULT_00_7_0							
R/W-1Ch							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-445. TX_TXCC_CPOST_MULT_01__TX_TXCC_CPOST_MULT_00_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_CPOST_MULT_01_15_8	R	0h	Reserved

**Table 12-445. TX_TXCC_CPOST_MULT_01__TX_TXCC_CPOST_MULT_00_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_CPOST_MULT_01_7_0	R/W	11h	<p>Calculated post emphasis multiplier value 01: The value in this field specifies the multiplier value used to generate the calculated post emphasis value from the FS value when tx_deemphasis [1:0] = 2'b01.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_CPOST_MULT_00_15_8	R	0h	Reserved
7-0	TX_TXCC_CPOST_MULT_00_7_0	R/W	1Ch	<p>Calculated post emphasis multiplier value 00: The value in this field specifies the multiplier value used to generate the calculated post emphasis value from the FS value when tx_deemphasis [1:0] = 2'b00.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-446. Register Call Summary for TX_TXCC_CPOST_MULT_01__TX_TXCC_CPOST_MULT_00_j

10-G SerDes Registers

- [TX_TXCC_CPOST_MULT_01__TX_TXCC_CPOST_MULT_00_j Register \(Offset = 4098h + formula\) \[reset = 0011001Ch\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.149 TX_TXCC_CPOST_MULT_11__TX_TXCC_CPOST_MULT_10_j Register (Offset = 409Ch + formula) [reset = 0h]

TX_TXCC_CPOST_MULT_11__TX_TXCC_CPOST_MULT_10_j is shown in Figure 12-149 and described in Table 12-448.

Return to [Summary Table](#).

Calculated post emphasis multiplier value 10 register

Offset = 409Ch + (j * 400h); where j = 0h to 3h

Table 12-447. TX_TXCC_CPOST_MULT_11__TX_TXCC_CPOST_MULT_10_j Instances

Instance	Physical Address
SERDES_10G0	0505 409Ch + formula

Figure 12-149. TX_TXCC_CPOST_MULT_11__TX_TXCC_CPOST_MULT_10_j Register

31	30	29	28	27	26	25	24
TX_TXCC_CPOST_MULT_11_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_CPOST_MULT_11_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_TXCC_CPOST_MULT_10_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_CPOST_MULT_10_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-448. TX_TXCC_CPOST_MULT_11__TX_TXCC_CPOST_MULT_10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_CPOST_MULT_11_15_8	R	0h	Reserved

**Table 12-448. TX_TXCC_CPOST_MULT_11__TX_TXCC_CPOST_MULT_10_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_CPOST_MULT_11_7_0	R/W	0h	<p>Calculated post emphasis multiplier value 11: The value in this field specifies the multiplier value used to generate the calculated post emphasis value from the FS value when tx_deemphasis [1:0] = 2'b11.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_CPOST_MULT_10_15_8	R	0h	Reserved
7-0	TX_TXCC_CPOST_MULT_10_7_0	R/W	0h	<p>Calculated post emphasis multiplier value 10: The value in this field specifies the multiplier value used to generate the calculated post emphasis value from the FS value when tx_deemphasis [1:0] = 2'b10.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-449. Register Call Summary for TX_TXCC_CPOST_MULT_11__TX_TXCC_CPOST_MULT_10_j

10-G SerDes Registers

- [TX_TXCC_CPOST_MULT_11__TX_TXCC_CPOST_MULT_10_j Register \(Offset = 409Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.150 TX_TXCC_MGNFS_MULT_001__TX_TXCC_MGNFS_MULT_000_j Register (Offset = 40A0h + formula) [reset = 0h]

TX_TXCC_MGNFS_MULT_001__TX_TXCC_MGNFS_MULT_000_j is shown in Figure 12-150 and described in Table 12-451.

Return to [Summary Table](#).

Margin full swing multiplier value 000 register

Offset = 40A0h + (j * 400h); where j = 0h to 3h

Table 12-450. TX_TXCC_MGNFS_MULT_001__TX_TXCC_MGNFS_MULT_000_j Instances

Instance	Physical Address
SERDES_10G0	0505 40A0h + formula

Figure 12-150. TX_TXCC_MGNFS_MULT_001__TX_TXCC_MGNFS_MULT_000_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MGNFS_MULT_001_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MGNFS_MULT_001_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_TXCC_MGNFS_MULT_000_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_MGNFS_MULT_000_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-451. TX_TXCC_MGNFS_MULT_001__TX_TXCC_MGNFS_MULT_000_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_MGNFS_MULT_001_15_8	R	0h	Reserved

Table 12-451. TX_TXCC_MGNFS_MULT_001__TX_TXCC_MGNFS_MULT_000_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_MGNFS_MULT_001_7_0	R/W	0h	<p>Margin full swing multiplier value 001: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b001 and tx_low_power_swing_en = 1'b0.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_MGNFS_MULT_000_15_8	R	0h	Reserved
7-0	TX_TXCC_MGNFS_MULT_000_7_0	R/W	0h	<p>Margin full swing multiplier value 000: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b000 and tx_low_power_swing_en = 1'b0.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-452. Register Call Summary for TX_TXCC_MGNFS_MULT_001__TX_TXCC_MGNFS_MULT_000_j

10-G SerDes Registers
<ul style="list-style-type: none"> TX_TXCC_MGNFS_MULT_001__TX_TXCC_MGNFS_MULT_000_j Register (Offset = 40A0h + formula) [reset = 0h]: [0] 10-G SerDes Registers: [0]

12.151 TX_TXCC_MGNFS_MULT_011__TX_TXCC_MGNFS_MULT_010_j Register (Offset = 40A4h + formula) [reset = 000F0007h]

TX_TXCC_MGNFS_MULT_011__TX_TXCC_MGNFS_MULT_010_j is shown in Figure 12-151 and described in Table 12-454.

Return to [Summary Table](#).

Margin full swing multiplier value 010 register

Offset = 40A4h + (j * 400h); where j = 0h to 3h

Table 12-453. TX_TXCC_MGNFS_MULT_011__TX_TXCC_MGNFS_MULT_010_j Instances

Instance	Physical Address
SERDES_10G0	0505 40A4h + formula

Figure 12-151. TX_TXCC_MGNFS_MULT_011__TX_TXCC_MGNFS_MULT_010_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MGNFS_MULT_011_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MGNFS_MULT_011_7_0							
R/W-Fh							
15	14	13	12	11	10	9	8
TX_TXCC_MGNFS_MULT_010_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_MGNFS_MULT_010_7_0							
R/W-7h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-454. TX_TXCC_MGNFS_MULT_011__TX_TXCC_MGNFS_MULT_010_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_MGNFS_MULT_011_15_8	R	0h	Reserved

Table 12-454. TX_TXCC_MGNFS_MULT_011__TX_TXCC_MGNFS_MULT_010_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_MGNFS_MULT_011_7_0	R/W	Fh	<p>Margin full swing multiplier value 011: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_vmargin = 3'b011 and tx_low_power_swing_en = 1'b0.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_MGNFS_MULT_010_15_8	R	0h	Reserved
7-0	TX_TXCC_MGNFS_MULT_010_7_0	R/W	7h	<p>Margin full swing multiplier value 010: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_vmargin = 3'b010 and tx_low_power_swing_en = 1'b0.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-455. Register Call Summary for TX_TXCC_MGNFS_MULT_011__TX_TXCC_MGNFS_MULT_010_j

10-G SerDes Registers
<ul style="list-style-type: none"> 10-G SerDes Registers: [0] TX_TXCC_MGNFS_MULT_011__TX_TXCC_MGNFS_MULT_010_j Register (Offset = 40A4h + formula) [reset = 000F0007h]: [0]

12.152 TX_TXCC_MGNFS_MULT_101__TX_TXCC_MGNFS_MULT_100_j Register (Offset = 40A8h + formula) [reset = 001C0015h]

TX_TXCC_MGNFS_MULT_101__TX_TXCC_MGNFS_MULT_100_j is shown in Figure 12-152 and described in Table 12-457.

Return to [Summary Table](#).

Margin full swing multiplier value 100 register

Offset = 40A8h + (j * 400h); where j = 0h to 3h

Table 12-456. TX_TXCC_MGNFS_MULT_101__TX_TXCC_MGNFS_MULT_100_j Instances

Instance	Physical Address
SERDES_10G0	0505 40A8h + formula

Figure 12-152. TX_TXCC_MGNFS_MULT_101__TX_TXCC_MGNFS_MULT_100_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MGNFS_MULT_101_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MGNFS_MULT_101_7_0							
R/W-1Ch							
15	14	13	12	11	10	9	8
TX_TXCC_MGNFS_MULT_100_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_MGNFS_MULT_100_7_0							
R/W-15h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-457. TX_TXCC_MGNFS_MULT_101__TX_TXCC_MGNFS_MULT_100_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_MGNFS_MULT_101_15_8	R	0h	Reserved

Table 12-457. TX_TXCC_MGNFS_MULT_101__TX_TXCC_MGNFS_MULT_100_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_MGNFS_MULT_101_7_0	R/W	1Ch	<p>Margin full swing multiplier value 101: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_vmargin = 3'b101 and tx_low_power_swing_en = 1'b0.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_MGNFS_MULT_100_15_8	R	0h	Reserved
7-0	TX_TXCC_MGNFS_MULT_100_7_0	R/W	15h	<p>Margin full swing multiplier value 100: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_vmargin = 3'b100 and tx_low_power_swing_en = 1'b0.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-458. Register Call Summary for TX_TXCC_MGNFS_MULT_101__TX_TXCC_MGNFS_MULT_100_j

10-G SerDes Registers
<ul style="list-style-type: none"> 10-G SerDes Registers: [0] TX_TXCC_MGNFS_MULT_101__TX_TXCC_MGNFS_MULT_100_j Register (Offset = 40A8h + formula) [reset = 001C0015h]: [0]

12.153 TX_TXCC_MGNFS_MULT_111__TX_TXCC_MGNFS_MULT_110_j Register (Offset = 40ACh + formula) [reset = 002A0023h]

TX_TXCC_MGNFS_MULT_111__TX_TXCC_MGNFS_MULT_110_j is shown in Figure 12-153 and described in Table 12-460.

Return to [Summary Table](#).

Margin full swing multiplier value 110 register

Offset = 40ACh + (j * 400h); where j = 0h to 3h

Table 12-459. TX_TXCC_MGNFS_MULT_111__TX_TXCC_MGNFS_MULT_110_j Instances

Instance	Physical Address
SERDES_10G0	0505 40ACh + formula

Figure 12-153. TX_TXCC_MGNFS_MULT_111__TX_TXCC_MGNFS_MULT_110_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MGNFS_MULT_111_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MGNFS_MULT_111_7_0							
R/W-2Ah							
15	14	13	12	11	10	9	8
TX_TXCC_MGNFS_MULT_110_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_MGNFS_MULT_110_7_0							
R/W-23h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-460. TX_TXCC_MGNFS_MULT_111__TX_TXCC_MGNFS_MULT_110_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_MGNFS_MULT_111_15_8	R	0h	Reserved

Table 12-460. TX_TXCC_MGNFS_MULT_111__TX_TXCC_MGNFS_MULT_110_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_MGNFS_MULT_111_7_0	R/W	2Ah	<p>Margin full swing multiplier value 111: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_vmargin = 3'b111 and tx_low_power_swing_en = 1'b0.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_MGNFS_MULT_110_15_8	R	0h	Reserved
7-0	TX_TXCC_MGNFS_MULT_110_7_0	R/W	23h	<p>Margin full swing multiplier value 110: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_vmargin = 3'b110 and tx_low_power_swing_en = 1'b0.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-461. Register Call Summary for TX_TXCC_MGNFS_MULT_111__TX_TXCC_MGNFS_MULT_110_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_TXCC_MGNFS_MULT_111__TX_TXCC_MGNFS_MULT_110_j Register \(Offset = 40ACh + formula\) \[reset = 002A0023h\]: \[0\]](#)

12.154 TX_TXCC_MGNHS_MULT_001__TX_TXCC_MGNHS_MULT_000_j Register (Offset = 40B0h + formula) [reset = 001C001Ch]

TX_TXCC_MGNHS_MULT_001__TX_TXCC_MGNHS_MULT_000_j is shown in Figure 12-154 and described in Table 12-463.

Return to [Summary Table](#).

Margin half swing multiplier value 000 register

Offset = 40B0h + (j * 400h); where j = 0h to 3h

Table 12-462. TX_TXCC_MGNHS_MULT_001__TX_TXCC_MGNHS_MULT_000_j Instances

Instance	Physical Address
SERDES_10G0	0505 40B0h + formula

Figure 12-154. TX_TXCC_MGNHS_MULT_001__TX_TXCC_MGNHS_MULT_000_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MGNHS_MULT_001_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MGNHS_MULT_001_7_0							
R/W-1Ch							
15	14	13	12	11	10	9	8
TX_TXCC_MGNHS_MULT_000_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_MGNHS_MULT_000_7_0							
R/W-1Ch							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-463. TX_TXCC_MGNHS_MULT_001__TX_TXCC_MGNHS_MULT_000_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_MGNHS_MULT_001_15_8	R	0h	Reserved

Table 12-463. TX_TXCC_MGNHS_MULT_001__TX_TXCC_MGNHS_MULT_000_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_MGNHS_MULT_001_7_0	R/W	1Ch	<p>Margin half swing multiplier value 001: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b001 and tx_low_power_swing_en = 1'b1.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_MGNHS_MULT_000_15_8	R	0h	Reserved
7-0	TX_TXCC_MGNHS_MULT_000_7_0	R/W	1Ch	<p>Margin half swing multiplier value 000: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b000 and tx_low_power_swing_en = 1'b1.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-464. Register Call Summary for TX_TXCC_MGNHS_MULT_001__TX_TXCC_MGNHS_MULT_000_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_TXCC_MGNHS_MULT_001__TX_TXCC_MGNHS_MULT_000_j Register \(Offset = 40B0h + formula\) \[reset = 001C001Ch\]: \[0\]](#)

12.155 TX_TXCC_MGNHS_MULT_011__TX_TXCC_MGNHS_MULT_010_j Register (Offset = 40B4h + formula) [reset = 00240020h]

TX_TXCC_MGNHS_MULT_011__TX_TXCC_MGNHS_MULT_010_j is shown in Figure 12-155 and described in Table 12-466.

Return to [Summary Table](#).

Margin half swing multiplier value 010 register

Offset = 40B4h + (j * 400h); where j = 0h to 3h

Table 12-465. TX_TXCC_MGNHS_MULT_011__TX_TXCC_MGNHS_MULT_010_j Instances

Instance	Physical Address
SERDES_10G0	0505 40B4h + formula

Figure 12-155. TX_TXCC_MGNHS_MULT_011__TX_TXCC_MGNHS_MULT_010_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MGNHS_MULT_011_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MGNHS_MULT_011_7_0							
R/W-24h							
15	14	13	12	11	10	9	8
TX_TXCC_MGNHS_MULT_010_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_MGNHS_MULT_010_7_0							
R/W-20h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-466. TX_TXCC_MGNHS_MULT_011__TX_TXCC_MGNHS_MULT_010_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_MGNHS_MULT_011_15_8	R	0h	Reserved

Table 12-466. TX_TXCC_MGNHS_MULT_011__TX_TXCC_MGNHS_MULT_010_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_MGNHS_MULT_011_7_0	R/W	24h	<p>Margin half swing multiplier value 011: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b011 and tx_low_power_swing_en = 1'b1.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_MGNHS_MULT_010_15_8	R	0h	Reserved
7-0	TX_TXCC_MGNHS_MULT_010_7_0	R/W	20h	<p>Margin half swing multiplier value 010: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b010 and tx_low_power_swing_en = 1'b1.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-467. Register Call Summary for TX_TXCC_MGNHS_MULT_011__TX_TXCC_MGNHS_MULT_010_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_TXCC_MGNHS_MULT_011__TX_TXCC_MGNHS_MULT_010_j Register \(Offset = 40B4h + formula\) \[reset = 00240020h\]: \[0\]](#)

12.156 TX_TXCC_MGNHS_MULT_101__TX_TXCC_MGNHS_MULT_100_j Register (Offset = 40B8h + formula) [reset = 002C0028h]

TX_TXCC_MGNHS_MULT_101__TX_TXCC_MGNHS_MULT_100_j is shown in Figure 12-156 and described in Table 12-469.

Return to [Summary Table](#).

Margin half swing multiplier value 100 register

Offset = 40B8h + (j * 400h); where j = 0h to 3h

Table 12-468. TX_TXCC_MGNHS_MULT_101__TX_TXCC_MGNHS_MULT_100_j Instances

Instance	Physical Address
SERDES_10G0	0505 40B8h + formula

Figure 12-156. TX_TXCC_MGNHS_MULT_101__TX_TXCC_MGNHS_MULT_100_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MGNHS_MULT_101_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MGNHS_MULT_101_7_0							
R/W-2Ch							
15	14	13	12	11	10	9	8
TX_TXCC_MGNHS_MULT_100_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_MGNHS_MULT_100_7_0							
R/W-28h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-469. TX_TXCC_MGNHS_MULT_101__TX_TXCC_MGNHS_MULT_100_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_MGNHS_MULT_101_15_8	R	0h	Reserved

Table 12-469. TX_TXCC_MGNHS_MULT_101__TX_TXCC_MGNHS_MULT_100_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_MGNHS_MULT_101_7_0	R/W	2Ch	<p>Margin half swing multiplier value 101: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b101 and tx_low_power_swing_en = 1'b1.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_MGNHS_MULT_100_15_8	R	0h	Reserved
7-0	TX_TXCC_MGNHS_MULT_100_7_0	R/W	28h	<p>Margin half swing multiplier value 100: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b100 and tx_low_power_swing_en = 1'b1.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-470. Register Call Summary for TX_TXCC_MGNHS_MULT_101__TX_TXCC_MGNHS_MULT_100_j

10-G SerDes Registers

- [TX_TXCC_MGNHS_MULT_101__TX_TXCC_MGNHS_MULT_100_j Register \(Offset = 40B8h + formula\) \[reset = 002C0028h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.157 TX_TXCC_MGNHS_MULT_111__TX_TXCC_MGNHS_MULT_110_j Register (Offset = 40BCh + formula) [reset = 00360033h]

TX_TXCC_MGNHS_MULT_111__TX_TXCC_MGNHS_MULT_110_j is shown in Figure 12-157 and described in Table 12-472.

Return to [Summary Table](#).

Margin half swing multiplier value 110 register

Offset = 40BCh + (j * 400h); where j = 0h to 3h

Table 12-471. TX_TXCC_MGNHS_MULT_111__TX_TXCC_MGNHS_MULT_110_j Instances

Instance	Physical Address
SERDES_10G0	0505 40BCh + formula

Figure 12-157. TX_TXCC_MGNHS_MULT_111__TX_TXCC_MGNHS_MULT_110_j Register

31	30	29	28	27	26	25	24
TX_TXCC_MGNHS_MULT_111_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_MGNHS_MULT_111_7_0							
R/W-36h							
15	14	13	12	11	10	9	8
TX_TXCC_MGNHS_MULT_110_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_MGNHS_MULT_110_7_0							
R/W-33h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-472. TX_TXCC_MGNHS_MULT_111__TX_TXCC_MGNHS_MULT_110_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_MGNHS_MULT_111_15_8	R	0h	Reserved

Table 12-472. TX_TXCC_MGNHS_MULT_111__TX_TXCC_MGNHS_MULT_110_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_MGNHS_MULT_111_7_0	R/W	36h	<p>Margin half swing multiplier value 111: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b111 and tx_low_power_swing_en = 1'b1.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_MGNHS_MULT_110_15_8	R	0h	Reserved
7-0	TX_TXCC_MGNHS_MULT_110_7_0	R/W	33h	<p>Margin half swing multiplier value 110: The value in this field specifies the multiplier value used to generate the margin value from the resistor calibration value when tx_ymargin = 3'b110 and tx_low_power_swing_en = 1'b1.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : 128/ 128 = 1.000000 Bit 6 : 64/ 128 = 0.500000 Bit 5 : 32/ 128 = 0.250000 Bit 4 : 16/ 128 = 0.125000 Bit 3 : 8/ 128 = 0.062500 Bit 2 : 4/ 128 = 0.031250 Bit 1 : 2/ 128 = 0.015625 Bit 0 : 1/ 128 = 0.0078125</p> <p>Note that the largest value this is allowed to be set to is 54/128. Note that the output of the multiplier is 6 bits wide. It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value. In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-473. Register Call Summary for TX_TXCC_MGNHS_MULT_111__TX_TXCC_MGNHS_MULT_110_j

10-G SerDes Registers
<ul style="list-style-type: none"> 10-G SerDes Registers: [0] TX_TXCC_MGNHS_MULT_111__TX_TXCC_MGNHS_MULT_110_j Register (Offset = 40BCh + formula) [reset = 00360033h]: [0]

12.158 TX_TXCC_P1PRE_COEF_MULT__TX_TXCC_P0PRE_COEF_MULT_j Register (Offset = 40C0h + formula) [reset = 0h]

TX_TXCC_P1PRE_COEF_MULT__TX_TXCC_P0PRE_COEF_MULT_j is shown in Figure 12-158 and described in Table 12-475.

Return to [Summary Table](#).

Preset 0 pre emphasis coefficient multiplier value register

Offset = 40C0h + (j * 400h); where j = 0h to 3h

Table 12-474.

TX_TXCC_P1PRE_COEF_MULT__TX_TXCC_P0PRE_COEF_MULT_j Instances

Instance	Physical Address
SERDES_10G0	0505 40C0h + formula

Figure 12-158. TX_TXCC_P1PRE_COEF_MULT__TX_TXCC_P0PRE_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P1PRE_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P1PRE_COEF_MULT_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_TXCC_P0PRE_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P0PRE_COEF_MULT_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-475. TX_TXCC_P1PRE_COEF_MULT__TX_TXCC_P0PRE_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P1PRE_COEF_MULT_15_8	R	0h	Reserved

Table 12-475. TX_TXCC_P1PRE_COEF_MULT__TX_TXCC_P0PRE_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P1PRE_COEF_MULT_7_0	R/W	0h	<p>Preset 1 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 1 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P0PRE_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P0PRE_COEF_MULT_7_0	R/W	0h	<p>Preset 0 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 0 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-476. Register Call Summary for TX_TXCC_P1PRE_COEF_MULT__TX_TXCC_P0PRE_COEF_MULT_j

10-G SerDes Registers

- [TX_TXCC_P1PRE_COEF_MULT__TX_TXCC_P0PRE_COEF_MULT_j Register \(Offset = 40C0h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.159 TX_TXCC_P3PRE_COEF_MULT__TX_TXCC_P2PRE_COEF_MULT_j Register (Offset = 40C4h + formula) [reset = 0h]

TX_TXCC_P3PRE_COEF_MULT__TX_TXCC_P2PRE_COEF_MULT_j is shown in Figure 12-159 and described in Table 12-478.

Return to [Summary Table](#).

Preset 2 pre emphasis coefficient multiplier value register

Offset = 40C4h + (j * 400h); where j = 0h to 3h

Table 12-477.

TX_TXCC_P3PRE_COEF_MULT__TX_TXCC_P2PRE_COEF_MULT_j Instances

Instance	Physical Address
SERDES_10G0	0505 40C4h + formula

Figure 12-159. TX_TXCC_P3PRE_COEF_MULT__TX_TXCC_P2PRE_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P3PRE_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P3PRE_COEF_MULT_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_TXCC_P2PRE_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P2PRE_COEF_MULT_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-478. TX_TXCC_P3PRE_COEF_MULT__TX_TXCC_P2PRE_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P3PRE_COEF_MULT_15_8	R	0h	Reserved

Table 12-478. TX_TXCC_P3PRE_COEF_MULT__TX_TXCC_P2PRE_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P3PRE_COEF_MULT_7_0	R/W	0h	<p>Preset 3 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 3 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P2PRE_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P2PRE_COEF_MULT_7_0	R/W	0h	<p>Preset 2 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 2 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-479. Register Call Summary for TX_TXCC_P3PRE_COEF_MULT__TX_TXCC_P2PRE_COEF_MULT_j

10-G SerDes Registers

- [TX_TXCC_P3PRE_COEF_MULT__TX_TXCC_P2PRE_COEF_MULT_j Register \(Offset = 40C4h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.160 TX_TXCC_P5PRE_COEF_MULT__TX_TXCC_P4PRE_COEF_MULT_j Register (Offset = 40C8h + formula) [reset = 000D0000h]

TX_TXCC_P5PRE_COEF_MULT__TX_TXCC_P4PRE_COEF_MULT_j is shown in Figure 12-160 and described in Table 12-481.

Return to [Summary Table](#).

Preset 4 pre emphasis coefficient multiplier value register

Offset = 40C8h + (j * 400h); where j = 0h to 3h

Table 12-480.

TX_TXCC_P5PRE_COEF_MULT__TX_TXCC_P4PRE_COEF_MULT_j Instances

Instance	Physical Address
SERDES_10G0	0505 40C8h + formula

Figure 12-160. TX_TXCC_P5PRE_COEF_MULT__TX_TXCC_P4PRE_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P5PRE_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P5PRE_COEF_MULT_7_0							
R/W-Dh							
15	14	13	12	11	10	9	8
TX_TXCC_P4PRE_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P4PRE_COEF_MULT_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-481. TX_TXCC_P5PRE_COEF_MULT__TX_TXCC_P4PRE_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P5PRE_COEF_MULT_15_8	R	0h	Reserved

Table 12-481. TX_TXCC_P5PRE_COEF_MULT__TX_TXCC_P4PRE_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P5PRE_COEF_MULT_7_0	R/W	Dh	<p>Preset 5 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 5 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P4PRE_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P4PRE_COEF_MULT_7_0	R/W	0h	<p>Preset 4 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 4 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-482. Register Call Summary for TX_TXCC_P5PRE_COEF_MULT__TX_TXCC_P4PRE_COEF_MULT_j

10-G SerDes Registers

- [TX_TXCC_P5PRE_COEF_MULT__TX_TXCC_P4PRE_COEF_MULT_j Register \(Offset = 40C8h + formula\) \[reset = 000D0000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.161 TX_TXCC_P7PRE_COEF_MULT__TX_TXCC_P6PRE_COEF_MULT_j Register (Offset = 40CCh + formula) [reset = 000D0010h]

TX_TXCC_P7PRE_COEF_MULT__TX_TXCC_P6PRE_COEF_MULT_j is shown in Figure 12-161 and described in Table 12-484.

Return to [Summary Table](#).

Preset 6 pre emphasis coefficient multiplier value register

Offset = 40CCh + (j * 400h); where j = 0h to 3h

Table 12-483.

TX_TXCC_P7PRE_COEF_MULT__TX_TXCC_P6PRE_COEF_MULT_j Instances

Instance	Physical Address
SERDES_10G0	0505 40CCh + formula

Figure 12-161. TX_TXCC_P7PRE_COEF_MULT__TX_TXCC_P6PRE_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P7PRE_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P7PRE_COEF_MULT_7_0							
R/W-Dh							
15	14	13	12	11	10	9	8
TX_TXCC_P6PRE_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P6PRE_COEF_MULT_7_0							
R/W-10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-484. TX_TXCC_P7PRE_COEF_MULT__TX_TXCC_P6PRE_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P7PRE_COEF_MULT_15_8	R	0h	Reserved

Table 12-484. TX_TXCC_P7PRE_COEF_MULT__TX_TXCC_P6PRE_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P7PRE_COEF_MULT_7_0	R/W	Dh	<p>Preset 7 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 7 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P6PRE_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P6PRE_COEF_MULT_7_0	R/W	10h	<p>Preset 6 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 6 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-485. Register Call Summary for TX_TXCC_P7PRE_COEF_MULT__TX_TXCC_P6PRE_COEF_MULT_j

10-G SerDes Registers

- [TX_TXCC_P7PRE_COEF_MULT__TX_TXCC_P6PRE_COEF_MULT_j Register \(Offset = 40CCh + formula\) \[reset = 000D0010h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.162 TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_COEF_MULT_j Register (Offset = 40D0h + formula) [reset = 00160010h]

TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_COEF_MULT_j is shown in Figure 12-162 and described in Table 12-487.

Return to [Summary Table](#).

Preset 8 pre emphasis coefficient multiplier value register

Offset = 40D0h + (j * 400h); where j = 0h to 3h

Table 12-486.

TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_COEF_MULT_j Instances

Instance	Physical Address
SERDES_10G0	0505 40D0h + formula

Figure 12-162. TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P9PRE_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P9PRE_COEF_MULT_7_0							
R/W-16h							
15	14	13	12	11	10	9	8
TX_TXCC_P8PRE_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P8PRE_COEF_MULT_7_0							
R/W-10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-487. TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P9PRE_COEF_MULT_15_8	R	0h	Reserved

Table 12-487. TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P9PRE_COEF_MULT_7_0	R/W	16h	<p>Preset 9 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 9 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P8PRE_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P8PRE_COEF_MULT_7_0	R/W	10h	<p>Preset 8 pre emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 8 pre emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-488. Register Call Summary for TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_COEF_MULT_j

10-G SerDes Registers

- [TX_TXCC_P9PRE_COEF_MULT__TX_TXCC_P8PRE_COEF_MULT_j Register \(Offset = 40D0h + formula\) \[reset = 00160010h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.163 TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j Register (Offset = 40E0h + formula) [reset = 00160022h]

TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j is shown in Figure 12-163 and described in Table 12-490.

Return to [Summary Table](#).

Preset 0 post emphasis coefficient multiplier value register

Offset = 40E0h + (j * 400h); where j = 0h to 3h

Table 12-489.
TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j
Instances

Instance	Physical Address
SERDES_10G0	0505 40E0h + formula

Figure 12-163. TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P1POST_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P1POST_COEF_MULT_7_0							
R/W-16h							
15	14	13	12	11	10	9	8
TX_TXCC_P0POST_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P0POST_COEF_MULT_7_0							
R/W-22h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-490. TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P1POST_COEF_MULT_15_8	R	0h	Reserved

Table 12-490. TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P1POST_COEF_MULT_7_0	R/W	16h	<p>Preset 1 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 1 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P0POST_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P0POST_COEF_MULT_7_0	R/W	22h	<p>Preset 0 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 0 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-491. Register Call Summary for TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j

10-G SerDes Registers

- [TX_TXCC_P1POST_COEF_MULT__TX_TXCC_P0POST_COEF_MULT_j Register \(Offset = 40E0h + formula\) \[reset = 00160022h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.164 TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j Register (Offset = 40E4h + formula) [reset = 0010001Bh]

TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j is shown in Figure 12-164 and described in Table 12-493.

Return to [Summary Table](#).

Preset 2 post emphasis coefficient multiplier value register

Offset = 40E4h + (j * 400h); where j = 0h to 3h

Table 12-492.
TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j
Instances

Instance	Physical Address
SERDES_10G0	0505 40E4h + formula

Figure 12-164. TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P3POST_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P3POST_COEF_MULT_7_0							
R/W-10h							
15	14	13	12	11	10	9	8
TX_TXCC_P2POST_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P2POST_COEF_MULT_7_0							
R/W-1Bh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-493. TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P3POST_COEF_MULT_15_8	R	0h	Reserved

Table 12-493. TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P3POST_COEF_MULT_7_0	R/W	10h	<p>Preset 3 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 3 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P2POST_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P2POST_COEF_MULT_7_0	R/W	1Bh	<p>Preset 2 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 2 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-494. Register Call Summary for TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_TXCC_P3POST_COEF_MULT__TX_TXCC_P2POST_COEF_MULT_j Register \(Offset = 40E4h + formula\) \[reset = 0010001Bh\]: \[0\]](#)

12.165 TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j Register (Offset = 40E8h + formula) [reset = 0h]

TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j is shown in Figure 12-165 and described in Table 12-496.

Return to [Summary Table](#).

Preset 4 post emphasis coefficient multiplier value register

Offset = 40E8h + (j * 400h); where j = 0h to 3h

Table 12-495.
TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j
Instances

Instance	Physical Address
SERDES_10G0	0505 40E8h + formula

Figure 12-165. TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P5POST_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P5POST_COEF_MULT_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_TXCC_P4POST_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P4POST_COEF_MULT_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-496. TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P5POST_COEF_MULT_15_8	R	0h	Reserved

Table 12-496. TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P5POST_COEF_MULT_7_0	R/W	0h	<p>Preset 5 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 5 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P4POST_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P4POST_COEF_MULT_7_0	R/W	0h	<p>Preset 4 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 4 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-497. Register Call Summary for TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j

10-G SerDes Registers

- [TX_TXCC_P5POST_COEF_MULT__TX_TXCC_P4POST_COEF_MULT_j Register \(Offset = 40E8h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.166 TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j Register (Offset = 40ECh + formula) [reset = 001B0000h]

TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j is shown in Figure 12-166 and described in Table 12-499.

Return to [Summary Table](#).

Preset 6 post emphasis coefficient multiplier value register

Offset = 40ECh + (j * 400h); where j = 0h to 3h

Table 12-498.
TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j
Instances

Instance	Physical Address
SERDES_10G0	0505 40ECh + formula

Figure 12-166. TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P7POST_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P7POST_COEF_MULT_7_0							
R/W-1Bh							
15	14	13	12	11	10	9	8
TX_TXCC_P6POST_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P6POST_COEF_MULT_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-499. TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P7POST_COEF_MULT_15_8	R	0h	Reserved

Table 12-499. TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P7POST_COEF_MULT_7_0	R/W	1Bh	<p>Preset 7 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 7 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P6POST_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P6POST_COEF_MULT_7_0	R/W	0h	<p>Preset 6 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 6 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-500. Register Call Summary for TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_TXCC_P7POST_COEF_MULT__TX_TXCC_P6POST_COEF_MULT_j Register \(Offset = 40ECh + formula\) \[reset = 001B0000h\]: \[0\]](#)

12.167 TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j Register (Offset = 40F0h + formula) [reset = 10h]

TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j is shown in Figure 12-167 and described in Table 12-502.

Return to [Summary Table](#).

Preset 8 post emphasis coefficient multiplier value register

Offset = 40F0h + (j * 400h); where j = 0h to 3h

Table 12-501.
TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j
Instances

Instance	Physical Address
SERDES_10G0	0505 40F0h + formula

Figure 12-167. TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j Register

31	30	29	28	27	26	25	24
TX_TXCC_P9POST_COEF_MULT_15_8							
R-0h							
23	22	21	20	19	18	17	16
TX_TXCC_P9POST_COEF_MULT_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_TXCC_P8POST_COEF_MULT_15_8							
R-0h							
7	6	5	4	3	2	1	0
TX_TXCC_P8POST_COEF_MULT_7_0							
R/W-10h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-502. TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TX_TXCC_P9POST_COEF_MULT_15_8	R	0h	Reserved

Table 12-502. TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TX_TXCC_P9POST_COEF_MULT_7_0	R/W	0h	<p>Preset 9 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 9 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>
15-8	TX_TXCC_P8POST_COEF_MULT_15_8	R	0h	Reserved
7-0	TX_TXCC_P8POST_COEF_MULT_7_0	R/W	10h	<p>Preset 8 post emphasis coefficient multiplier value : The value in this field specifies the multiplier value used to generate the preset 8 post emphasis coefficient value from the FS value.</p> <p>The following describes the multiplier value each bit in this field corresponds to.</p> <p>Bit 7 : $128 / 128 = 1.000000$ Bit 6 : $64 / 128 = 0.500000$ Bit 5 : $32 / 128 = 0.250000$ Bit 4 : $16 / 128 = 0.125000$ Bit 3 : $8 / 128 = 0.062500$ Bit 2 : $4 / 128 = 0.031250$ Bit 1 : $2 / 128 = 0.015625$ Bit 0 : $1 / 128 = 0.0078125$</p> <p>Note that the output of the multiplier is 6 bits wide.</p> <p>It is possible to set the multiplier value here to a sufficiently large value to cause the multiplier result to be such that it can't be represented by a 6 bit value.</p> <p>In such a case, the multiplier output will be driven to 6'b111111.</p>

Table 12-503. Register Call Summary for TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j

10-G SerDes Registers

- [TX_TXCC_P9POST_COEF_MULT__TX_TXCC_P8POST_COEF_MULT_j Register \(Offset = 40F0h + formula\) \[reset = 10h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.168 DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_DRV_DIAG_LANE_FCM_EN_TO_j Register (Offset = 4180h + formula) [reset = 000601F4h]

DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_DRV_DIAG_LANE_FCM_EN_TO_j is shown in Figure 12-168 and described in Table 12-505.

Return to [Summary Table](#).

Lane fast common mode enable timeout register

Offset = 4180h + (j * 400h); where j = 0h to 3h

Table 12-504.
DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_DRV_DIAG_LANE_FCM_EN_TO_j
Instances

Instance	Physical Address
SERDES_10G0	0505 4180h + formula

Figure 12-168. DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_DRV_DIAG_LANE_FCM_EN_TO_j Register

31	30	29	28	27	26	25	24
DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_15_4							
R-0h							
23	22	21	20	19	18	17	16
DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_15_4				DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_3_0			
R-0h				R/W-6h			
15	14	13	12	11	10	9	8
DRV_DIAG_LANE_FCM_EN_TO_15	DRV_DIAG_LANE_FCM_EN_TO_14_12			DRV_DIAG_LANE_FCM_EN_TO_11_0			
R/W-0h		R-0h		R/W-1F4h			
7	6	5	4	3	2	1	0
DRV_DIAG_LANE_FCM_EN_TO_11_0							
R/W-1F4h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-505. DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_DRV_DIAG_LANE_FCM_EN_TO_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-20	DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_15_4	R	0h	Reserved
19-16	DRV_DIAG_LANE_FCM_EN_SWAIT_TMR_3_0	R/W	6h	Lane fast common mode enable sample wait timer value: This specifies the number of reference clock cycles the fast establishment of common mode process will wait between changing the state of the signals controlling the analog common mode sense circuits, and testing the results of the new state.
15	DRV_DIAG_LANE_FCM_EN_TO_15	R/W	0h	Bypass fast establishment of common mode enable: When enabled, the fast establishment of common mode function will be bypassed. When bypassed, the lane fast common mode enable timeout value field in this register can be used to implement a programmable delay between when fast establishment of common mode is normally initiated, and when it will complete.
14-12	DRV_DIAG_LANE_FCM_EN_TO_14_12	R	0h	Reserved

Table 12-505. DRV_DIAG_LANE_FCM_EN_SWAIT_TMR__DRV_DIAG_LANE_FCM_EN_TO_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	DRV_DIAG_LANE_FCM_EN_TO_11_0	R/W	1F4h	<p>Lane fast common mode enable timeout value: The usage of the value of this field is a function of the state of the bypass fast establishment of common mode enable bit in this register.</p> <p>Bypass disabled (normal operation): This specifies the maximum number of reference clock cycles the fast establishment of common mode process will wait for the tx_{p,m} signals to be reported as above the reference voltage, before timing out.</p> <p>The default value of this register corresponds to a delay of 20 uSec.</p> <p>Bypass enabled: This can be used to specify the number of reference clock cycles between when fast establishment of common mode would normally be initiated, and when it is acknowledged to have been completed.</p>

**Table 12-506. Register Call Summary for
DRV_DIAG_LANE_FCM_EN_SWAIT_TMR__DRV_DIAG_LANE_FCM_EN_TO_j**

10-G SerDes Registers

- [DRV_DIAG_LANE_FCM_EN_SWAIT_TMR__DRV_DIAG_LANE_FCM_EN_TO_j Register \(Offset = 4180h + formula\) \[reset = 000601F4h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.169 DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j Register (Offset = 4184h + formula) [reset = 08C40096h]

DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j is shown in Figure 12-169 and described in Table 12-508.

Return to [Summary Table](#).

Lane fast common mode enable margin timer register

Offset = 4184h + (j * 400h); where j = 0h to 3h

Table 12-507.
DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 4184h + formula

Figure 12-169. DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j Register

31	30	29	28	27	26	25	24
DRV_DIAG_LANE_FCM_EN_TUNE_15_12				DRV_DIAG_LANE_FCM_EN_TUNE_11_8			
R-0h				R/W-8h			
23	22	21	20	19	18	17	16
DRV_DIAG_LANE_FCM_EN_TUNE_7_4				DRV_DIAG_LANE_FCM_EN_TUNE_3_0			
R/W-Ch				R/W-4h			
15	14	13	12	11	10	9	8
DRV_DIAG_LANE_FCM_EN_MGN_TMR_15_12				DRV_DIAG_LANE_FCM_EN_MGN_TMR_11_0			
R-0h				R/W-96h			
7	6	5	4	3	2	1	0
DRV_DIAG_LANE_FCM_EN_MGN_TMR_11_0							
R/W-96h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-508. DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-28	DRV_DIAG_LANE_FCM_EN_TUNE_15_12	R	0h	Reserved
27-24	DRV_DIAG_LANE_FCM_EN_TUNE_11_8	R/W	8h	Common mode sense reference DAC voltage initial test: This field sets the common mode detect reference voltage for the common mode detect comparator, when the fast establishment of common mode function is checking the initial state of the txda_cm_sense_comp_out signal. This field drives the txda_cm_sense_vref_dac signal going to the analog, and it is only driven when the fast establishment of common mode function is enabled. 4'b 0000 : Minimum ... 4'b 1111 : Maximum

**Table 12-508. DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j Register
Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
23-20	DRV_DIAG_LANE_FCM_EN_TUNE_7_4	R/W	Ch	Common mode sense reference DAC voltage high test: This field sets the common mode detect reference voltage for the common mode detect comparator, when the fast establishment of common mode function is waiting for the txdac_cm_sense_comp_out signal from the analog to be driven high. This field drives the txdac_cm_sense_vref_dac signal going to the analog, and it is only driven when the fast establishment of common mode function is enabled. 4'b 0000 : Minimum ... 4'b 1111 : Maximum
19-16	DRV_DIAG_LANE_FCM_EN_TUNE_3_0	R/W	4h	Common mode sense reference DAC voltage low test: This field sets the common mode detect reference voltage for the common mode detect comparator, when the fast establishment of common mode function is waiting for the txdac_cm_sense_comp_out signal from the analog to be driven low. This field drives the txdac_cm_sense_vref_dac signal going to the analog, and it is only driven when the fast establishment of common mode function is enabled. 4'b 0000 : Minimum ... 4'b 1111 : Maximum
15-12	DRV_DIAG_LANE_FCM_EN_MGN_TMR_15_12	R	0h	Reserved
11-0	DRV_DIAG_LANE_FCM_EN_MGN_TMR_11_0	R/W	96h	Lane fast common mode enable margin timer value: This specifies the number of reference clock cycles the fast establishment of common mode process will enable all the margin segments for. The default value of this register corresponds to a delay of 6 uSec.

**Table 12-509. Register Call Summary for
DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j**

10-G SerDes Registers

- [DRV_DIAG_LANE_FCM_EN_TUNE__DRV_DIAG_LANE_FCM_EN_MGN_TMR_j Register \(Offset = 4184h + formula\) \[reset = 08C40096h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.170 DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j Register (Offset = 4188h + formula) [reset = 000C000Fh]

DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j is shown in Figure 12-170 and described in Table 12-511.

Return to [Summary Table](#).

Transmitter LFPS control register

Offset = 4188h + (j * 400h); where j = 0h to 3h

Table 12-510. DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 4188h + formula

Figure 12-170. DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j Register

31	30	29	28	27	26	25	24
DRV_DIAG_RCVDET_TUNE_15_5							
R-0h							
23	22	21	20	19	18	17	16
DRV_DIAG_RCVDET_TUNE_15_5			DRV_DIAG_RCVDET_TUNE_4	DRV_DIAG_RCVDET_TUNE_3_0			
R-0h			R/W-0h	R/W-Ch			
15	14	13	12	11	10	9	8
DRV_DIAG_LFPS_CTRL_15_8							
R-0h							
7	6	5	4	3	2	1	0
DRV_DIAG_LFPS_CTRL_7_0							
R/W-Fh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-511. DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	DRV_DIAG_RCVDET_TUNE_15_5	R	0h	Reserved
20	DRV_DIAG_RCVDET_TUNE_4	R/W	0h	Receiver detect comparators output and or control: This bit controls how the receiver detect comparators are used to drive the txda_rcvdet_detected_n signal to the digital. This bit drives the txda_rcvdet_and_orb signal going to the analog. 1'b 0: Comparator outputs are ORed to drive txda_rcvdet_detected_n. 1'b 1: Comparator outputs are ANDed to drive txda_rcvdet_detected_n.
19-16	DRV_DIAG_RCVDET_TUNE_3_0	R/W	Ch	Receiver detect reference DAC voltage: This field sets the receiver detect reference voltage for the receiver detect comparator. This field drives the txda_rcvdet_vref_dac signal going to the analog. 4'b 0000 : Minimum ... 4'b 1111 : Maximum
15-8	DRV_DIAG_LFPS_CTRL_15_8	R	0h	Reserved

**Table 12-511. DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
7-0	DRV_DIAG_LFPS_CTRL_7_0	R/W	Fh	LFPS half period clocks: Specifies the number of clock cycles required to implement one half of a LFPS period, by the transmitter LFPS controller.

Table 12-512. Register Call Summary for DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [DRV_DIAG_RCVDET_TUNE__DRV_DIAG_LFPS_CTRL_j Register \(Offset = 4188h + formula\) \[reset = 000C00Fh\]: \[0\]](#)

12.171 DRV_DIAG_TX_DRV_j Register (Offset = 418Ch + formula) [reset = X]

DRV_DIAG_TX_DRV_j is shown in [Figure 12-171](#) and described in [Table 12-514](#).

Return to [Summary Table](#).

TX driver diagnostic register

Offset = 418Ch + (j * 400h); where j = 0h to 3h

Table 12-513. DRV_DIAG_TX_DRV_j Instances

Instance	Physical Address
SERDES_10G0	0505 418Ch + formula

Figure 12-171. DRV_DIAG_TX_DRV_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
DRV_DIAG_TX_DRV_15_8							
R-0h							
7	6	5	4	3	2	1	0
DRV_DIAG_TX_DRV_7	DRV_DIAG_TX_DRV_6	DRV_DIAG_TX_DRV_5_4		DRV_DIAG_TX_DRV_3_2		DRV_DIAG_TX_DRV_1	DRV_DIAG_TX_DRV_0
R/W-1h	R-0h	R/W-2h		R-0h		R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-514. DRV_DIAG_TX_DRV_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	DRV_DIAG_TX_DRV_15_8	R	0h	Reserved
7	DRV_DIAG_TX_DRV_7	R/W	1h	TX boost enable: Increases the transmitter amplitude for fast data transitions, by controlling the txda_drv_boost_en signal going to the analog.
6	DRV_DIAG_TX_DRV_6	R	0h	Reserved
5-4	DRV_DIAG_TX_DRV_5_4	R/W	2h	TX boost tune: Controls the transmitter boost amplitude when the transmitter boost function is enabled using the TX boost enable bit in this register, by controlling the txda_drv_boost_tune signal going to the analog. The following specifies the encoding of this field. 2'b 00: Minimum Boost 2'b 01: 2'b 10: 2'b 11: Maximum Boost
3-2	DRV_DIAG_TX_DRV_3_2	R	0h	Reserved

Table 12-514. DRV_DIAG_TX_DRV_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DRV_DIAG_TX_DRV_1	R/W	1h	TX pre-driver pull up control: When the pre-driver is disabled, this bit controls the state of the pre-driver output, by controlling the txd_drv_predrv_pullup signal going to the analog. 1'b 0 : Pulled low 1'b 1 : Pulled high
0	DRV_DIAG_TX_DRV_0	R/W	1h	TX driver margin type: Selects the margining type the driver will operate in, by controlling the txd_drv_margin_type signal going to the analog. 1'b 0 : Classical margining - High power margining that complies with the driver differential and common-mode output impedance specs. 1'b 1 : Low-Power margining - Low power margining that complies with the driver differential output impedance spec. However, this violates the driver common-mode output impedance spec to save power whenever a reduced swing driver configuration is used. Note that when fast establishment of common mode is active, the analog signal that this drives will be forced to 1'b0.

Table 12-515. Register Call Summary for DRV_DIAG_TX_DRV_j

10-G SerDes Registers

- [DRV_DIAG_TX_DRV_j Register \(Offset = 418Ch + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.172 XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j Register (Offset = 41C0h + formula) [reset = 04240505h]

XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j is shown in Figure 12-172 and described in Table 12-517.

Return to [Summary Table](#).

Transceiver power island control timer register

Offset = 41C0h + (j * 400h); where j = 0h to 3h

Table 12-516. XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 41C0h + formula

Figure 12-172. XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j Register

31	30	29	28	27	26	25	24
XCVR_DIAG_XCAL_PWRI_OVRD_15	XCVR_DIAG_XCAL_PWRI_OVRD_14	XCVR_DIAG_XCAL_PWRI_OVRD_13_12		XCVR_DIAG_XCAL_PWRI_OVRD_11	XCVR_DIAG_XCAL_PWRI_OVRD_10	XCVR_DIAG_XCAL_PWRI_OVRD_9	XCVR_DIAG_XCAL_PWRI_OVRD_8
R/W-0h	R/W-0h	R-0h		R/W-0h	R-1h	R/W-0h	R-0h
23	22	21	20	19	18	17	16
XCVR_DIAG_XCAL_PWRI_OVRD_7_0							
R/W-24h							
15	14	13	12	11	10	9	8
XCVR_DIAG_PWRI_TMR_15_13			XCVR_DIAG_PWRI_TMR_12_8				
R-0h			R/W-5h				
7	6	5	4	3	2	1	0
XCVR_DIAG_PWRI_TMR_7_5			XCVR_DIAG_PWRI_TMR_4_0				
R-0h			R/W-5h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-517. XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	XCVR_DIAG_XCAL_PWRI_OVRD_15	R/W	0h	Power island controller input override enable: When enabled, the power island control state machine input override bits in this register will drive the power island control state machine directly, and override any control from other state machines in the macro. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. Note that the value of this field must be the same for all lanes that make up a link. 1'b 0: Override disabled 1'b 1: Override enabled

**Table 12-517. XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
30	XCVR_DIAG_XCAL_PWRI_OVRD_14	R/W	0h	Power island controller output override enable: When enabled, the power island control state machine output override bits in this register will drive the power island control state machine outputs, and override any control from power island control state machine. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. Note that the value of this field must be the same for all lanes that make up a link. 1'b 0: Override disabled 1'b 1: Override enabled
29-28	XCVR_DIAG_XCAL_PWRI_OVRD_13_12	R	0h	Reserved
27	XCVR_DIAG_XCAL_PWRI_OVRD_11	R/W	0h	Power suspend request override: When enabled, this bit will override the power_suspend_req input of the power island control state machine. Note that the value of this field must be the same for all lanes that make up a link.
26	XCVR_DIAG_XCAL_PWRI_OVRD_10	R	1h	Power suspend acknowledge: This is the current state of the power_suspend_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
25	XCVR_DIAG_XCAL_PWRI_OVRD_9	R/W	0h	Power recover request override: When enabled, this bit will override the power_recover_req input of the power island control state machine. Note that the value of this field must be the same for all lanes that make up a link.
24	XCVR_DIAG_XCAL_PWRI_OVRD_8	R	0h	Power recover acknowledge: This is the current state of the power_recover_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.

Table 12-517. XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	XCVR_DIAG_XCAL_PWRI_OVRD_7_0	R/W	24h	<p>Power island controller output override: When enabled, the bits in this field will override the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p> <p>The default value of the bits in this register are such that the power island is not forced to be switched on when the power island controller output override enable bit in this register is enabled.</p> <p>When using this register to switch this power island on and off, the bits in this field are required to change in a specific order with individual register writes.</p> <p>The writes must happen in the order specified below.</p> <p>8'b 00100100 : Power island is not being forced on 8'b1010010</p>
15-13	XCVR_DIAG_PWRI_TMR_15_13	R	0h	Reserved
12-8	XCVR_DIAG_PWRI_TMR_12_8	R/W	5h	<p>Power enable phase 2 timer value: This specifies the number of PSM clock cycles the power island control state machines in the transceiver will wait in the power phase 2 enable states, in order to allow enough time for the second phase of the switched domain to power up, before deactivating the isolation functions.</p> <p>The default value of this register corresponds to a delay of 40 nSec.</p> <p>Note that a value of 0 in this field is not valid, and will result in a delay of 1 clock cycle.</p> <p>Note that the value of this field must be the same for all lanes that make up a link.</p>
7-5	XCVR_DIAG_PWRI_TMR_7_5	R	0h	Reserved
4-0	XCVR_DIAG_PWRI_TMR_4_0	R/W	5h	<p>Power enable phase 1 timer value: This specifies the number of PSM clock cycles the power island control state machines in the transceiver will wait in the power phase 1 enable states, in order to allow enough time for the first phase of the switched domain to power up, before enabling the second phase of the power up.</p> <p>The default value of this register corresponds to a delay of 40 nSec.</p> <p>Note that a value of 0 in this field is not valid, and will result in a delay of 1 clock cycle.</p> <p>Note that the value of this field must be the same for all lanes that make up a link.</p>

Table 12-518. Register Call Summary for XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [XCVR_DIAG_XCAL_PWRI_OVRD__XCVR_DIAG_PWRI_TMR_j Register \(Offset = 41C0h + formula\) \[reset = 04240505h\]: \[0\]](#)

12.173 XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j Register (Offset = 41C4h + formula) [reset = 04240024h]

XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j is shown in Figure 12-173 and described in Table 12-520.

Return to [Summary Table](#).

Transceiver transceiver calibration power island control status register

Offset = 41C4h + (j * 400h); where j = 0h to 3h

Table 12-519.
XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j Instances

Instance	Physical Address
SERDES_10G0	0505 41C4h + formula

Figure 12-173. XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j Register

31	30	29	28	27	26	25	24
XCVR_DIAG_XDP_PWRI_OVRD_15	XCVR_DIAG_XDP_PWRI_OVRD_14	XCVR_DIAG_XDP_PWRI_OVRD_13_12		XCVR_DIAG_XDP_PWRI_OVRD_11	XCVR_DIAG_XDP_PWRI_OVRD_10	XCVR_DIAG_XDP_PWRI_OVRD_9	XCVR_DIAG_XDP_PWRI_OVRD_8
R/W-0h	R/W-0h	R-0h		R/W-0h	R-1h	R/W-0h	R-0h
23	22	21	20	19	18	17	16
XCVR_DIAG_XDP_PWRI_OVRD_7_0							
R/W-24h							
15	14	13	12	11	10	9	8
XCVR_DIAG_XCAL_PWRI_STAT_15_8							
R-0h							
7	6	5	4	3	2	1	0
XCVR_DIAG_XCAL_PWRI_STAT_7_0							
R-24h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-520. XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	XCVR_DIAG_XDP_PWRI_OVRD_15	R/W	0h	Power island controller input override enable: When enabled, the power island control state machine input override bits in this register will drive the power island control state machine directly, and override any control from other state machines in the macro. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. Note that the value of this field must be the same for all lanes that make up a link. 1'b 0: Override disabled 1'b 1: Override enabled

Table 12-520. XCVR_DIAG_XDP_PWRI_OVRD_XCVR_DIAG_XCAL_PWRI_STAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	XCVR_DIAG_XDP_PWRI_OVRD_14	R/W	0h	Power island controller output override enable: When enabled, the power island control state machine output override bits in this register will drive the power island control state machine outputs, and override any control from power island control state machine. Note that this bit must never change state in the same register write that any of the override bits it controls in this register are changed. Note that the value of this field must be the same for all lanes that make up a link. 1'b 0: Override disabled 1'b 1: Override enabled
29-28	XCVR_DIAG_XDP_PWRI_OVRD_13_12	R	0h	Reserved
27	XCVR_DIAG_XDP_PWRI_OVRD_11	R/W	0h	Power suspend request override: When enabled, this bit will override the power_suspend_req input of the power island control state machine. Note that the value of this field must be the same for all lanes that make up a link.
26	XCVR_DIAG_XDP_PWRI_OVRD_10	R	1h	Power suspend acknowledge: This is the current state of the power_suspend_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 after the power island is enabled, as a function of the power island controller input override enable bit in this register.
25	XCVR_DIAG_XDP_PWRI_OVRD_9	R/W	0h	Power recover request override: When enabled, this bit will override the power_recover_req input of the power island control state machine. Note that the value of this field must be the same for all lanes that make up a link.
24	XCVR_DIAG_XDP_PWRI_OVRD_8	R	0h	Power recover acknowledge: This is the current state of the power_recover_ack output from the power island control state machine. Note that this bit will always be set to 1'b1 when the power island controller input override enable bit in this register.

Table 12-520. XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	XCVR_DIAG_XDP_PWRI_OVRD_7_0	R/W	24h	<p>Power island controller output override: When enabled, the bits in this field will override the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p> <p>The default value of the bits in this register are such that the power island is not forced to be switched on when the power island controller output override enable bit in this register is enabled.</p> <p>When using this register to switch this power island on and off, the bits in this field are required to change in a specific order with individual register writes.</p> <p>The writes must happen in the order specified below.</p> <p>8'b 00100100 : Power island is not being forced on 8'b10100100</p>
15-8	XCVR_DIAG_XCAL_PWRI_STAT_15_8	R	0h	Reserved
7-0	XCVR_DIAG_XCAL_PWRI_STAT_7_0	R	24h	<p>Power island controller output status: This field indicates the current state of the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p>

Table 12-521. Register Call Summary for XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j

10-G SerDes Registers

- [XCVR_DIAG_XDP_PWRI_OVRD__XCVR_DIAG_XCAL_PWRI_STAT_j Register \(Offset = 41C4h + formula\) \[reset = 04240024h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.174 XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j Register (Offset = 41C8h + formula) [reset = 00120024h]

XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j is shown in Figure 12-174 and described in Table 12-523.

Return to [Summary Table](#).

Transceiver transceiver data path power island control status register

Offset = 41C8h + (j * 400h); where j = 0h to 3h

Table 12-522. XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j Instances

Instance	Physical Address
SERDES_10G0	0505 41C8h + formula

Figure 12-174. XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j Register

31	30	29	28	27	26	25	24
XCVR_DIAG_PLLDRC_CTRL_1_5_14	XCVR_DIAG_PLLDRC_CTRL_1_3_12	XCVR_DIAG_PLLDRC_CTRL_1_1_10	XCVR_DIAG_PLLDRC_CTRL_1_9_8				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
23	22	21	20	19	18	17	16
XCVR_DIAG_PLLDRC_CTRL_7_6	XCVR_DIAG_PLLDRC_CTRL_5_4	XCVR_DIAG_PLLDRC_CTRL_3_2	XCVR_DIAG_PLLDRC_CTRL_1_0				
R/W-0h	R/W-1h	R/W-0h	R/W-2h				
15	14	13	12	11	10	9	8
XCVR_DIAG_XDP_PWRI_STAT_15_8							
R-0h							
7	6	5	4	3	2	1	0
XCVR_DIAG_XDP_PWRI_STAT_7_0							
R-24h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-523. XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	XCVR_DIAG_PLLDRC_CTRL_15_14	R/W	0h	Digital PLL clock select standard mode 3: This bit controls which full rate PLL clock is selected, when xcvr_standard_mode is set to 2'b11. 2'b 00 : PLL clock 0 from the PLL 0. 2'b 01 : PLL clock 1 from the PLL 0. 2'b 10 : PLL clock 0 from the PLL 1. 2'b 11 : PLL clock 1 from the PLL 1.
29-28	XCVR_DIAG_PLLDRC_CTRL_13_12	R/W	0h	Digital PLL data rate divider standard mode 3 value: This field will directly control the xcvr_pll_clk_datart_div signal, which controls which divided clock is selected when generating the xcvr_pll_clk_datart clock, when xcvr_standard_mode is set to 2'b11. 2'b 00 : Divide by 1. 2'b 01 : Divide by 2. 2'b 10 : Divide by 4. 2'b 11 : Divide by 8.

Table 12-523. XCVR_DIAG_PLLDRC_CTRL_XCVR_DIAG_XDP_PWRI_STAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27-26	XCVR_DIAG_PLLDRC_CTRL_11_10	R/W	0h	Digital PLL clock select standard mode 2: This bit controls which full rate PLL clock is selected, when xcvr_standard_mode is set to 2'b10. 2'b 00 : PLL clock 0 from the PLL 0. 2'b 01 : PLL clock 1 from the PLL 0. 2'b 10 : PLL clock 0 from the PLL 1. 2'b 11 : PLL clock 1 from the PLL 1.
25-24	XCVR_DIAG_PLLDRC_CTRL_9_8	R/W	0h	Digital PLL data rate divider standard mode 2 value: This field will directly control the xcvr_pll_clk_datart_div signal, which controls which divided clock is selected when generating the xcvr_pll_clk_datart clock, when xcvr_standard_mode is set to 2'b10. 2'b 00 : Divide by 1. 2'b 01 : Divide by 2. 2'b 10 : Divide by 4. 2'b 11 : Divide by 8.
23-22	XCVR_DIAG_PLLDRC_CTRL_7_6	R/W	0h	Digital PLL clock select standard mode 1: This bit controls which full rate PLL clock is selected, when xcvr_standard_mode is set to 2'b01. 2'b 00 : PLL clock 0 from the PLL 0. 2'b 01 : PLL clock 1 from the PLL 0. 2'b 10 : PLL clock 0 from the PLL 1. 2'b 11 : PLL clock 1 from the PLL 1.
21-20	XCVR_DIAG_PLLDRC_CTRL_5_4	R/W	1h	Digital PLL data rate divider standard mode 1 value: This field will directly control the xcvr_pll_clk_datart_div signal, which controls which divided clock is selected when generating the xcvr_pll_clk_datart clock, when xcvr_standard_mode is set to 2'b01. 2'b 00 : Divide by 1. 2'b 01 : Divide by 2. 2'b 10 : Divide by 4. 2'b 11 : Divide by 8.
19-18	XCVR_DIAG_PLLDRC_CTRL_3_2	R/W	0h	Digital PLL clock select standard mode 0: This bit controls which full rate PLL clock is selected, when xcvr_standard_mode is set to 2'b00. 2'b 00 : PLL clock 0 from the PLL 0. 2'b 01 : PLL clock 1 from the PLL 0. 2'b 10 : PLL clock 0 from the PLL 1. 2'b 11 : PLL clock 1 from the PLL 1.
17-16	XCVR_DIAG_PLLDRC_CTRL_1_0	R/W	2h	Digital PLL data rate divider standard mode 0 value: This field will directly control the xcvr_pll_clk_datart_div signal, which controls which divided clock is selected when generating the xcvr_pll_clk_datart clock, when xcvr_standard_mode is set to 2'b00. 2'b 00 : Divide by 1. 2'b 01 : Divide by 2. 2'b 10 : Divide by 4. 2'b 11 : Divide by 8.
15-8	XCVR_DIAG_XDP_PWRI_STAT_15_8	R	0h	Reserved

Table 12-523. XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	XCVR_DIAG_XDP_PWRI_STAT_7_0	R	24h	<p>Power island controller output status: This field indicates the current state of the output signals from the power island control state machine.</p> <p>The following are the power island control state machine output signals, and the bits in this field that they are associated with.</p> <p>Bit 7: state_sandh</p> <p>Bit 6: state_ret_save</p> <p>Bit 5: state_ret_restore (active low)</p> <p>Bit 4: power_en_ph_1</p> <p>Bit 3: power_en_ph_2</p> <p>Bit 2: power_isolation</p> <p>Bit 1: power_por_reset_n</p> <p>Bit 0: power_rstr_reset_n</p>

Table 12-524. Register Call Summary for XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j

10-G SerDes Registers

- [XCVR_DIAG_PLLDRC_CTRL__XCVR_DIAG_XDP_PWRI_STAT_j Register \(Offset = 41C8h + formula\) \[reset = 00120024h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.175 XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j Register (Offset = 41CCh + formula) [reset = 00010000h]

XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j is shown in Figure 12-175 and described in Table 12-526.

Return to [Summary Table](#).

Transceiver high speed clock select register

Offset = 41CCh + (j * 400h); where j = 0h to 3h

**Table 12-525. XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 41CCh + formula

Figure 12-175. XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j Register

31	30	29	28	27	26	25	24
XCVR_DIAG_H SCLK_DIV_15	XCVR_DIAG_HSCLK_DIV_14_12			XCVR_DIAG_H SCLK_DIV_11	XCVR_DIAG_HSCLK_DIV_10_8		
R-0h	R/W-0h			R-0h	R/W-0h		
23	22	21	20	19	18	17	16
XCVR_DIAG_H SCLK_DIV_7	XCVR_DIAG_HSCLK_DIV_6_4			XCVR_DIAG_H SCLK_DIV_3	XCVR_DIAG_HSCLK_DIV_2_0		
R-0h	R/W-0h			R-0h	R/W-1h		
15	14	13	12	11	10	9	8
XCVR_DIAG_HSCLK_SEL_15_1 4	XCVR_DIAG_HSCLK_SEL_13_1 2		XCVR_DIAG_HSCLK_SEL_11_1 0		XCVR_DIAG_HSCLK_SEL_9_8		
R-0h	R/W-0h		R-0h		R/W-0h		
7	6	5	4	3	2	1	0
XCVR_DIAG_HSCLK_SEL_7_6	XCVR_DIAG_HSCLK_SEL_5_4		XCVR_DIAG_HSCLK_SEL_3_2		XCVR_DIAG_HSCLK_SEL_1_0		
R-0h	R/W-0h		R-0h		R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-526. XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	XCVR_DIAG_HSCLK_DIV_15	R	0h	Reserved
30-28	XCVR_DIAG_HSCLK_DIV_14_12	R/W	0h	Transceiver clock divider select standard mode 3: This field selects the divider value used to divide the selected analog high speed clock by when generating the transmit and receive clocks, when xcvr_standard_mode is set to 2'b11, by driving the xcvrda_xcvr_clk_div_sel signal to the analog, as specified below. 3'b 000: Div 1 3'b 001: Div 2 3'b 010: Div 3 3'b 011: Div 4 3'b 100: Div 5 3'b 101: Div 6 3'b 110: Div 7 3'b 111: Div 8
27	XCVR_DIAG_HSCLK_DIV_11	R	0h	Reserved

**Table 12-526. XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26-24	XCVR_DIAG_HSCLK_DIV_10_8	R/W	0h	Transceiver clock divider select standard mode 2: This field selects the divider value used to divide the selected analog high speed clock by when generating the transmit and receive clocks, when xcvr_standard_mode is set to 2'b10, by driving the xcvrda_xcwr_clk_div_sel signal to the analog, as specified below. 3'b 000: Div 1 3'b 001: Div 2 3'b 010: Div 3 3'b 011: Div 4 3'b 100: Div 5 3'b 101: Div 6 3'b 110: Div 7 3'b 111: Div 8
23	XCVR_DIAG_HSCLK_DIV_7	R	0h	Reserved
22-20	XCVR_DIAG_HSCLK_DIV_6_4	R/W	0h	Transceiver clock divider select standard mode 1: This field selects the divider value used to divide the selected analog high speed clock by when generating the transmit and receive clocks, when xcvr_standard_mode is set to 2'b01, by driving the xcvrda_xcwr_clk_div_sel signal to the analog, as specified below. 3'b 000: Div 1 3'b 001: Div 2 3'b 010: Div 3 3'b 011: Div 4 3'b 100: Div 5 3'b 101: Div 6 3'b 110: Div 7 3'b 111: Div 8
19	XCVR_DIAG_HSCLK_DIV_3	R	0h	Reserved
18-16	XCVR_DIAG_HSCLK_DIV_2_0	R/W	1h	Transceiver clock divider select standard mode 0: This field selects the divider value used to divide the selected analog high speed clock by when generating the transmit and receive clocks, when xcvr_standard_mode is set to 2'b00, by driving the xcvrda_xcwr_clk_div_sel signal to the analog, as specified below. 3'b 000: Div 1 3'b 001: Div 2 3'b 010: Div 3 3'b 011: Div 4 3'b 100: Div 5 3'b 101: Div 6 3'b 110: Div 7 3'b 111: Div 8
15-14	XCVR_DIAG_HSCLK_SEL_15_14	R	0h	Reserved

**Table 12-526. XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
13-12	XCVR_DIAG_HSCLK_SE L_13_12	R/W	0h	High speed clock select standard mode 3: This specifies which analog high speed clock is selected when xcvr_standard_mode is set to 2'b11, by driving the xcvrda_clk_sel signal to the analog, as specified below. 2'b 00 : clock 0. 2'b 01 : clock 1. 2'b 10 : Reserved. 2'b 11 : Reserved.
11-10	XCVR_DIAG_HSCLK_SE L_11_10	R	0h	Reserved
9-8	XCVR_DIAG_HSCLK_SE L_9_8	R/W	0h	High speed clock select standard mode 2: This specifies which analog high speed clock is selected when xcvr_standard_mode is set to 2'b10, by driving the xcvrda_clk_sel signal to the analog, as specified below. 2'b 00 : clock 0. 2'b 01 : clock 1. 2'b 10 : Reserved. 2'b 11 : Reserved.
7-6	XCVR_DIAG_HSCLK_SE L_7_6	R	0h	Reserved
5-4	XCVR_DIAG_HSCLK_SE L_5_4	R/W	0h	High speed clock select standard mode 1: This specifies which analog high speed clock is selected when xcvr_standard_mode is set to 2'b01, by driving the xcvrda_clk_sel signal to the analog, as specified below. 2'b 00 : clock 0. 2'b 01 : clock 1. 2'b 10 : Reserved. 2'b 11 : Reserved.
3-2	XCVR_DIAG_HSCLK_SE L_3_2	R	0h	Reserved
1-0	XCVR_DIAG_HSCLK_SE L_1_0	R/W	0h	High speed clock select standard mode 0: This specifies which analog high speed clock is selected when xcvr_standard_mode is set to 2'b00, by driving the xcvrda_clk_sel signal to the analog, as specified below. 2'b 00 : clock 0. 2'b 01 : clock 1. 2'b 10 : Reserved. 2'b 11 : Reserved.

Table 12-527. Register Call Summary for XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j

10-G SerDes Registers

- [XCVR_DIAG_HSCLK_DIV__XCVR_DIAG_HSCLK_SEL_j Register \(Offset = 41CCh + formula\) \[reset = 00010000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.176 XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j Register (Offset = 41D0h + formula) [reset = 0h]

XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j is shown in Figure 12-176 and described in Table 12-529.

Return to [Summary Table](#).

TX clock control register

Offset = 41D0h + (j * 400h); where j = 0h to 3h

Table 12-528. XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 41D0h + formula

Figure 12-176. XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j Register

31	30	29	28	27	26	25	24
XCVR_DIAG_RXCLK_CTRL_1_5	XCVR_DIAG_RXCLK_CTRL_1_4	XCVR_DIAG_RXCLK_CTRL_1_3	XCVR_DIAG_RXCLK_CTRL_12_8				
R/W-0h	R/W-0h	R/W-0h	R-0h				
23	22	21	20	19	18	17	16
XCVR_DIAG_RXCLK_CTRL_7	XCVR_DIAG_RXCLK_CTRL_6	XCVR_DIAG_RXCLK_CTRL_5	XCVR_DIAG_RXCLK_CTRL_4	XCVR_DIAG_RXCLK_CTRL_3_0			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
15	14	13	12	11	10	9	8
XCVR_DIAG_TXCLK_CTRL_1_5	XCVR_DIAG_TXCLK_CTRL_14_0						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
XCVR_DIAG_TXCLK_CTRL_14_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-529. XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	XCVR_DIAG_RXCLK_CTRL_15	R/W	0h	RX deserializer clock invert: This bit is used to optionally invert the deserializer clock (rxda_des_clk) for diagnostic purposes.
30	XCVR_DIAG_RXCLK_CTRL_14	R/W	0h	RX 2x clock enable: This bit enables the receiver 2x clock function, by driving the rxda_des_clk_2x_en signal going to the analog. Note that this clock is only designed to be used in modes where the data width is 20 bits. 1'b 0 : Disabled 1'b 1 : Enabled
29	XCVR_DIAG_RXCLK_CTRL_13	R/W	0h	RX PI E path clock select: Controls which PI clock drives the E path clocks, by driving the rxda_pi_i_drv_e_en signal going to the analog. 1'b 0: E PI clock 1'b 1: IQ PI clock
28-24	XCVR_DIAG_RXCLK_CTRL_12_8	R	0h	Reserved

**Table 12-529. XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
23	XCVR_DIAG_RXCLK_CTRL_7	R/W	0h	PI output clock divider enable standard mode 3: This bit controls the rxda_pi_out_clk_div_en to enable the PI output clock divider, when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled
22	XCVR_DIAG_RXCLK_CTRL_6	R/W	0h	PI output clock divider enable standard mode 2: This bit controls the rxda_pi_out_clk_div_en to enable the PI output clock divider, when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled
21	XCVR_DIAG_RXCLK_CTRL_5	R/W	0h	PI output clock divider enable standard mode 1: This bit controls the rxda_pi_out_clk_div_en to enable the PI output clock divider, when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
20	XCVR_DIAG_RXCLK_CTRL_4	R/W	0h	PI output clock divider enable standard mode 0: This bit controls the rxda_pi_out_clk_div_en to enable the PI output clock divider, when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled
19-16	XCVR_DIAG_RXCLK_CTRL_3_0	R	0h	Reserved
15	XCVR_DIAG_TXCLK_CTRL_15	R/W	0h	TX serializer clock invert: This bit is used to optionally invert the serializer clock (txda_ser_clk) for diagnostic purposes.
14-0	XCVR_DIAG_TXCLK_CTRL_14_0	R	0h	Reserved

Table 12-530. Register Call Summary for XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [XCVR_DIAG_RXCLK_CTRL__XCVR_DIAG_TXCLK_CTRL_j Register \(Offset = 41D0h + formula\) \[reset = 0h\]: \[0\]](#)

12.177 XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j Register (Offset = 41D4h + formula) [reset = 000600FFh]

XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j is shown in Figure 12-177 and described in Table 12-532.

Return to [Summary Table](#).

Transceiver bidirectional control register

Offset = 41D4h + (j * 400h); where j = 0h to 3h

Table 12-531. XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 41D4h + formula

Figure 12-177. XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j Register

31	30	29	28	27	26	25	24
XCVR_DIAG_PSC_OVRD_15_4							
R-0h							
23	22	21	20	19	18	17	16
XCVR_DIAG_PSC_OVRD_15_4				XCVR_DIAG_PSC_OVRD_3	XCVR_DIAG_PSC_OVRD_2	XCVR_DIAG_PSC_OVRD_1	XCVR_DIAG_PSC_OVRD_0
R-0h				R/W-0h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
XCVR_DIAG_BIDI_CTRL_15_8							
R-0h							
7	6	5	4	3	2	1	0
XCVR_DIAG_BIDI_CTRL_7	XCVR_DIAG_BIDI_CTRL_6	XCVR_DIAG_BIDI_CTRL_5	XCVR_DIAG_BIDI_CTRL_4	XCVR_DIAG_BIDI_CTRL_3	XCVR_DIAG_BIDI_CTRL_2	XCVR_DIAG_BIDI_CTRL_1	XCVR_DIAG_BIDI_CTRL_0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-532. XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	XCVR_DIAG_PSC_OVRD_15_4	R	0h	Reserved
19	XCVR_DIAG_PSC_OVRD_3	R/W	0h	Receiver DFE enable mask value standard mode 3: This bit will controls the rx_dfe_eq_enable_std_mask digital signal, which can be used to mask off the rxda_dfe_eq_enable signal coming from the power state controller and going into the analog, when xcvr_standard_mode is set to 2'b11. 1'b 0 : The signal will be masked off. 1'b 1 : The signal to pass through unchanged.
18	XCVR_DIAG_PSC_OVRD_2	R/W	1h	Receiver DFE enable mask value standard mode 2: This bit will controls the rx_dfe_eq_enable_std_mask digital signal, which can be used to mask off the rxda_dfe_eq_enable signal coming from the power state controller and going into the analog, when xcvr_standard_mode is set to 2'b10. 1'b 0 : The signal will be masked off. 1'b 1 : The signal to pass through unchanged.

**Table 12-532. XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
17	XCVR_DIAG_PSC_OVRD_1	R/W	1h	Receiver DFE enable mask value standard mode 1: This bit will controls the rx_dfe_eq_enable_std_mask digital signal, which can be used to mask off the rxd_dfe_eq_enable signal coming from the power state controller and going into the analog, when xcvr_standard_mode is set to 2'b01. 1'b 0 : The signal will be masked off. 1'b 1 : The signal to pass through unchanged.
16	XCVR_DIAG_PSC_OVRD_0	R/W	0h	Receiver DFE enable mask value standard mode 0: This bit will controls the rx_dfe_eq_enable_std_mask digital signal, which can be used to mask off the rxd_dfe_eq_enable signal coming from the power state controller and going into the analog, when xcvr_standard_mode is set to 2'b00. 1'b 0 : The signal will be masked off. 1'b 1 : The signal to pass through unchanged.
15-8	XCVR_DIAG_BIDI_CTRL_15_8	R	0h	Reserved
7	XCVR_DIAG_BIDI_CTRL_7	R/W	1h	Receiver enable standard mode 3: When bidirectional bumps are implemented in the transceiver, this bit is a global enable for the receiver function, when xcvr_standard_mode is set to 2'b11. When bidirectional bumps are not implemented, this bit will be reset to 1'b1, and should not be changed. When bidirectional bumps are implemented in the transceiver, this bit and the corresponding transmitter enable bit must not be set to 1'b1 at the same time. 1'b 0 : RX disabled 1'b 1 : RX enabled
6	XCVR_DIAG_BIDI_CTRL_6	R/W	1h	Receiver enable standard mode 2: When bidirectional bumps are implemented in the transceiver, this bit is a global enable for the receiver function, when xcvr_standard_mode is set to 2'b10. When bidirectional bumps are not implemented, this bit will be reset to 1'b1, and should not be changed. When bidirectional bumps are implemented in the transceiver, this bit and the corresponding transmitter enable bit must not be set to 1'b1 at the same time. 1'b 0 : RX disabled 1'b 1 : RX enabled
5	XCVR_DIAG_BIDI_CTRL_5	R/W	1h	Receiver enable standard mode 1: When bidirectional bumps are implemented in the transceiver, this bit is a global enable for the receiver function, when xcvr_standard_mode is set to 2'b01. When bidirectional bumps are not implemented, this bit will be reset to 1'b1, and should not be changed. When bidirectional bumps are implemented in the transceiver, this bit and the corresponding transmitter enable bit must not be set to 1'b1 at the same time. 1'b 0 : RX disabled 1'b 1 : RX enabled

**Table 12-532. XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	XCVR_DIAG_BIDI_CTRL_4	R/W	1h	Receiver enable standard mode 0: When bidirectional bumps are implemented in the transceiver, this bit is a global enable for the receiver function, when xcvr_standard_mode is set to 2'b00. When bidirectional bumps are not implemented, this bit will be reset to 1'b1, and should not be changed. When bidirectional bumps are implemented in the transceiver, this bit and the corresponding transmitter enable bit must not be set to 1'b1 at the same time. 1'b 0 : RX disabled 1'b 1 : RX enabled
3	XCVR_DIAG_BIDI_CTRL_3	R/W	1h	Transmitter enable standard mode 3: When bidirectional bumps are implemented in the transceiver, this bit is a global enable for the transmitter function, when xcvr_standard_mode is set to 2'b11. When bidirectional bumps are not implemented, this bit will be reset to 1'b1, and should not be changed. When bidirectional bumps are implemented in the transceiver, this bit and the corresponding receiver enable bit must not be set to 1'b1 at the same time. 1'b 0 : TX disabled 1'b 1 : TX enabled
2	XCVR_DIAG_BIDI_CTRL_2	R/W	1h	Transmitter enable standard mode 2: When bidirectional bumps are implemented in the transceiver, this bit is a global enable for the transmitter function, when xcvr_standard_mode is set to 2'b10. When bidirectional bumps are not implemented, this bit will be reset to 1'b1, and should not be changed. When bidirectional bumps are implemented in the transceiver, this bit and the corresponding receiver enable bit must not be set to 1'b1 at the same time. 1'b 0 : TX disabled 1'b 1 : TX enabled
1	XCVR_DIAG_BIDI_CTRL_1	R/W	1h	Transmitter enable standard mode 1: When bidirectional bumps are implemented in the transceiver, this bit is a global enable for the transmitter function, when xcvr_standard_mode is set to 2'b01. When bidirectional bumps are not implemented, this bit will be reset to 1'b1, and should not be changed. When bidirectional bumps are implemented in the transceiver, this bit and the corresponding receiver enable bit must not be set to 1'b1 at the same time. 1'b 0 : TX disabled 1'b 1 : TX enabled
0	XCVR_DIAG_BIDI_CTRL_0	R/W	1h	Transmitter enable standard mode 0: When bidirectional bumps are implemented in the transceiver, this bit is a global enable for the transmitter function, when xcvr_standard_mode is set to 2'b00. When bidirectional bumps are not implemented, this bit will be reset to 1'b1, and should not be changed. When bidirectional bumps are implemented in the transceiver, this bit and the corresponding receiver enable bit must not be set to 1'b1 at the same time. 1'b 0 : TX disabled 1'b 1 : TX enabled

Table 12-533. Register Call Summary for XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j

10-G SerDes Registers

- [XCVR_DIAG_PSC_OVRD__XCVR_DIAG_BIDI_CTRL_j](#) Register (Offset = 41D4h + formula) [reset = 000600FFh]: [0]
- 10-G SerDes Registers: [0]

12.178 XCVR_DIAG_XCVR_CLK_CTRL__XCVR_DIAG_RST_DIAG_j Register (Offset = 41D8h + formula) [reset = 000D0000h]

XCVR_DIAG_XCVR_CLK_CTRL__XCVR_DIAG_RST_DIAG_j is shown in Figure 12-178 and described in Table 12-535.

Return to [Summary Table](#).

Transceiver control reset diagnostic register

Offset = 41D8h + (j * 400h); where j = 0h to 3h

Table 12-534. XCVR_DIAG_XCVR_CLK_CTRL__XCVR_DIAG_RST_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 41D8h + formula

Figure 12-178. XCVR_DIAG_XCVR_CLK_CTRL__XCVR_DIAG_RST_DIAG_j Register

31	30	29	28	27	26	25	24
XCVR_DIAG_XCVR_CLK_CTRL_15_6							
R-0h							
23	22	21	20	19	18	17	16
XCVR_DIAG_XCVR_CLK_CTRL_15_6		XCVR_DIAG_XCVR_CLK_CTRL_5_0					
R-0h		R/W-Dh					
15	14	13	12	11	10	9	8
XCVR_DIAG_RST_DIAG_15_3							
R-0h							
7	6	5	4	3	2	1	0
XCVR_DIAG_RST_DIAG_15_3				XCVR_DIAG_RST_DIAG_2		XCVR_DIAG_RST_DIAG_1	XCVR_DIAG_RST_DIAG_0
R-0h				R-0h		R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-535. XCVR_DIAG_XCVR_CLK_CTRL__XCVR_DIAG_RST_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	XCVR_DIAG_XCVR_CLK_CTRL_15_6	R	0h	Reserved
21-16	XCVR_DIAG_XCVR_CLK_CTRL_5_0	R/W	Dh	Transceiver clock enable delay timer value: This specifies the number of xcvr_psm_clk clock cycles that the transceiver high speed clock reset release state machine will wait between when it drives the analog transceiver clock enable signal active, and when it will initiate the process to release the reset for this clock. The default value of this register corresponds to a delay of at least 100 nSec.
15-3	XCVR_DIAG_RST_DIAG_15_3	R	0h	Reserved
2	XCVR_DIAG_RST_DIAG_2	R	0h	Current state of the tx_coef_calc_reset_n reset.
1	XCVR_DIAG_RST_DIAG_1	R	0h	Current state of the xcvr_psm_reset_n reset.
0	XCVR_DIAG_RST_DIAG_0	R	0h	Current state of the xcvr_ref_clk_reset_n reset.

Table 12-536. Register Call Summary for XCVR_DIAG_XCVR_CLK_CTRL__XCVR_DIAG_RST_DIAG_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [XCVR_DIAG_XCVR_CLK_CTRL__XCVR_DIAG_RST_DIAG_j Register \(Offset = 41D8h + formula\) \[reset = 000D0000h\]: \[0\]](#)

12.179 XCVR_DIAG_DCYA_j Register (Offset = 41DCh + formula) [reset = X]

XCVR_DIAG_DCYA_j is shown in Figure 12-179 and described in Table 12-538.

Return to [Summary Table](#).

Transceiver digital cover your alternatives register

Offset = 41DCh + (j * 400h); where j = 0h to 3h

Table 12-537. XCVR_DIAG_DCYA_j Instances

Instance	Physical Address
SERDES_10G0	0505 41DCh + formula

Figure 12-179. XCVR_DIAG_DCYA_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
XCVR_DIAG_DCYA_15_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-X															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-538. XCVR_DIAG_DCYA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	XCVR_DIAG_DCYA_15_0	R/W	0h	Reserved - spare
15-0	RESERVED	R/W	X	

Table 12-539. Register Call Summary for XCVR_DIAG_DCYA_j

10-G SerDes Registers

- [XCVR_DIAG_DCYA_j Register \(Offset = 41DCh + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.180 TX_PSC_A1__TX_PSC_A0_j Register (Offset = 4200h + formula) [reset = 04AF00FFh]

TX_PSC_A1__TX_PSC_A0_j is shown in Figure 12-180 and described in Table 12-541.

Return to [Summary Table](#).

Transmitter A0 power state definition register

Offset = 4200h + (j * 400h); where j = 0h to 3h

Table 12-540. TX_PSC_A1__TX_PSC_A0_j Instances

Instance	Physical Address
SERDES_10G0	0505 4200h + formula

Figure 12-180. TX_PSC_A1__TX_PSC_A0_j Register

31	30	29	28	27	26	25	24
TX_PSC_A1_15_12				TX_PSC_A1_1_1	TX_PSC_A1_1_0	TX_PSC_A1_9	TX_PSC_A1_8
R-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TX_PSC_A1_7	TX_PSC_A1_6	TX_PSC_A1_5	TX_PSC_A1_4	TX_PSC_A1_3	TX_PSC_A1_2	TX_PSC_A1_1	TX_PSC_A1_0
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
TX_PSC_A0_15_12				TX_PSC_A0_1_1	TX_PSC_A0_1_0	TX_PSC_A0_9	TX_PSC_A0_8
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TX_PSC_A0_7	TX_PSC_A0_6	TX_PSC_A0_5	TX_PSC_A0_4	TX_PSC_A0_3	TX_PSC_A0_2	TX_PSC_A0_1	TX_PSC_A0_0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-541. TX_PSC_A1__TX_PSC_A0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TX_PSC_A1_15_12	R	0h	Reserved
27	TX_PSC_A1_11	R/W	0h	TX driver common mode enable extend control
26	TX_PSC_A1_10	R/W	1h	Force txda_lfps_sel active
25	TX_PSC_A1_9	R/W	0h	LFPS clock gate enable
24	TX_PSC_A1_8	R/W	0h	Reserved - spare
23	TX_PSC_A1_7	R/W	1h	Transmitter low current mode
22	TX_PSC_A1_6	R/W	0h	Transmitter mission mode enable
21	TX_PSC_A1_5	R/W	1h	TX driver common mode enable
20	TX_PSC_A1_4	R/W	0h	TX driver enable
19	TX_PSC_A1_3	R/W	1h	TX post-emphasis enable (C+1)
18	TX_PSC_A1_2	R/W	1h	TX pre-emphasis enable (C-1)
17	TX_PSC_A1_1	R/W	1h	TX pre-driver enable
16	TX_PSC_A1_0	R/W	1h	TX serializer enable
15-12	TX_PSC_A0_15_12	R	0h	Reserved

Table 12-541. TX_PSC_A1__TX_PSC_A0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TX_PSC_A0_11	R/W	0h	TX driver common mode enable extend control: Specifies which power states the tx_cm_n_mode_en_ext signal is considered valid in and can be used to force the driver to continue to be in the common mode state.
10	TX_PSC_A0_10	R/W	0h	Force txda_lfps_sel active: Setting this bit forces the txda_lfps_sel signal going to the analog to be driven active. Note that this function is implemented for additional power savings. In the analog, this signal controls a MUX select associated with the driver. Setting this bit to 1'b1 will force the MUX to select the LFPS data path. By selecting this path in low power states, instead of the serializer path, the driver inputs will be driven to 1'b0, instead of having the potential to toggle.
9	TX_PSC_A0_9	R/W	0h	LFPS clock gate enable: Enables the LFPS clock gate when an LFPS clock is required.
8	TX_PSC_A0_8	R/W	0h	Reserved - spare
7	TX_PSC_A0_7	R/W	1h	Transmitter low current mode: Enables a low current consumption mode within the common mode voltage circuit in the driver, via the txda_drv_idle_lowi_en signal going to the analog.
6	TX_PSC_A0_6	R/W	1h	Transmitter mission mode enable: Enables the analog circuits in the driver required to run in mission mode, via the txda_drv_mission_en signal going to the analog.
5	TX_PSC_A0_5	R/W	1h	TX driver common mode enable: Enables the common mode voltage circuits in the driver.
4	TX_PSC_A0_4	R/W	1h	TX driver enable: Enables the transmitter driver, via the H bridge driver controller.
3	TX_PSC_A0_3	R/W	1h	TX post-emphasis enable (C+1): Enables the transmitter circuits related to the post-emphasis function.
2	TX_PSC_A0_2	R/W	1h	TX pre-emphasis enable (C-1): Enables the transmitter circuits related to the pre-emphasis function.
1	TX_PSC_A0_1	R/W	1h	TX pre-driver enable: Enables the transmitter pre-driver, driver data selection MUX, and receiver detect.
0	TX_PSC_A0_0	R/W	1h	TX serializer enable: Enables the serializer and related clock divider circuits.

Table 12-542. Register Call Summary for TX_PSC_A1__TX_PSC_A0_j

10-G SerDes Registers

- [TX_PSC_A1__TX_PSC_A0_j Register \(Offset = 4200h + formula\) \[reset = 04AF00FFh\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.181 TX_PSC_A3__TX_PSC_A2_j Register (Offset = 4204h + formula) [reset = 04AE04AEh]

TX_PSC_A3__TX_PSC_A2_j is shown in Figure 12-181 and described in Table 12-544.

Return to [Summary Table](#).

Transmitter A2 power state definition register

Offset = 4204h + (j * 400h); where j = 0h to 3h

Table 12-543. TX_PSC_A3__TX_PSC_A2_j Instances

Instance	Physical Address
SERDES_10G0	0505 4204h + formula

Figure 12-181. TX_PSC_A3__TX_PSC_A2_j Register

31	30	29	28	27	26	25	24
TX_PSC_A3_15_12				TX_PSC_A3_1_1	TX_PSC_A3_1_0	TX_PSC_A3_9	TX_PSC_A3_8
R-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TX_PSC_A3_7	TX_PSC_A3_6	TX_PSC_A3_5	TX_PSC_A3_4	TX_PSC_A3_3	TX_PSC_A3_2	TX_PSC_A3_1	TX_PSC_A3_0
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
TX_PSC_A2_15_12				TX_PSC_A2_1_1	TX_PSC_A2_1_0	TX_PSC_A2_9	TX_PSC_A2_8
R-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TX_PSC_A2_7	TX_PSC_A2_6	TX_PSC_A2_5	TX_PSC_A2_4	TX_PSC_A2_3	TX_PSC_A2_2	TX_PSC_A2_1	TX_PSC_A2_0
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-544. TX_PSC_A3__TX_PSC_A2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TX_PSC_A3_15_12	R	0h	Reserved
27	TX_PSC_A3_11	R/W	0h	TX driver common mode enable extend control
26	TX_PSC_A3_10	R/W	1h	Force txda_lfps_sel active
25	TX_PSC_A3_9	R/W	0h	LFPS clock gate enable
24	TX_PSC_A3_8	R/W	0h	Reserved - spare
23	TX_PSC_A3_7	R/W	1h	Transmitter low current mode
22	TX_PSC_A3_6	R/W	0h	Transmitter mission mode enable
21	TX_PSC_A3_5	R/W	1h	TX driver common mode enable
20	TX_PSC_A3_4	R/W	0h	TX driver enable
19	TX_PSC_A3_3	R/W	1h	TX post-emphasis enable (C+1)
18	TX_PSC_A3_2	R/W	1h	TX pre-emphasis enable (C-1)
17	TX_PSC_A3_1	R/W	1h	TX pre-driver enable
16	TX_PSC_A3_0	R/W	0h	TX serializer enable
15-12	TX_PSC_A2_15_12	R	0h	Reserved
11	TX_PSC_A2_11	R/W	0h	TX driver common mode enable extend control
10	TX_PSC_A2_10	R/W	1h	Force txda_lfps_sel active

Table 12-544. TX_PSC_A3__TX_PSC_A2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	TX_PSC_A2_9	R/W	0h	LFPS clock gate enable
8	TX_PSC_A2_8	R/W	0h	Reserved - spare
7	TX_PSC_A2_7	R/W	1h	Transmitter low current mode
6	TX_PSC_A2_6	R/W	0h	Transmitter mission mode enable
5	TX_PSC_A2_5	R/W	1h	TX driver common mode enable
4	TX_PSC_A2_4	R/W	0h	TX driver enable
3	TX_PSC_A2_3	R/W	1h	TX post-emphasis enable (C+1)
2	TX_PSC_A2_2	R/W	1h	TX pre-emphasis enable (C-1)
1	TX_PSC_A2_1	R/W	1h	TX pre-driver enable
0	TX_PSC_A2_0	R/W	0h	TX serializer enable

Table 12-545. Register Call Summary for TX_PSC_A3__TX_PSC_A2_j

10-G SerDes Registers

- [TX_PSC_A3__TX_PSC_A2_j Register \(Offset = 4204h + formula\) \[reset = 04AE04AEh\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.182 TX_PSC_A5__TX_PSC_A4_j Register (Offset = 4208h + formula) [reset = 880h]

TX_PSC_A5__TX_PSC_A4_j is shown in Figure 12-182 and described in Table 12-547.

Return to [Summary Table](#).

Transmitter A4 power state definition register

Offset = 4208h + (j * 400h); where j = 0h to 3h

Table 12-546. TX_PSC_A5__TX_PSC_A4_j Instances

Instance	Physical Address
SERDES_10G0	0505 4208h + formula

Figure 12-182. TX_PSC_A5__TX_PSC_A4_j Register

31	30	29	28	27	26	25	24
TX_PSC_A5_15_12				TX_PSC_A5_11	TX_PSC_A5_10	TX_PSC_A5_9	TX_PSC_A5_8
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TX_PSC_A5_7	TX_PSC_A5_6	TX_PSC_A5_5	TX_PSC_A5_4	TX_PSC_A5_3	TX_PSC_A5_2	TX_PSC_A5_1	TX_PSC_A5_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TX_PSC_A4_15_12				TX_PSC_A4_11	TX_PSC_A4_10	TX_PSC_A4_9	TX_PSC_A4_8
R-0h				R/W-1h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TX_PSC_A4_7	TX_PSC_A4_6	TX_PSC_A4_5	TX_PSC_A4_4	TX_PSC_A4_3	TX_PSC_A4_2	TX_PSC_A4_1	TX_PSC_A4_0
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-547. TX_PSC_A5__TX_PSC_A4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TX_PSC_A5_15_12	R	0h	Reserved
27	TX_PSC_A5_11	R/W	0h	TX driver common mode enable extend control
26	TX_PSC_A5_10	R/W	0h	Force txd_a_lfps_sel active
25	TX_PSC_A5_9	R/W	0h	LFPS clock gate enable
24	TX_PSC_A5_8	R/W	0h	Reserved - spare
23	TX_PSC_A5_7	R/W	0h	Transmitter low current mode
22	TX_PSC_A5_6	R/W	0h	Transmitter mission mode enable
21	TX_PSC_A5_5	R/W	0h	TX driver common mode enable
20	TX_PSC_A5_4	R/W	0h	TX driver enable
19	TX_PSC_A5_3	R/W	0h	TX post-emphasis enable (C+1)
18	TX_PSC_A5_2	R/W	0h	TX pre-emphasis enable (C-1)
17	TX_PSC_A5_1	R/W	0h	TX pre-driver enable
16	TX_PSC_A5_0	R/W	0h	TX serializer enable
15-12	TX_PSC_A4_15_12	R	0h	Reserved
11	TX_PSC_A4_11	R/W	1h	TX driver common mode enable extend control
10	TX_PSC_A4_10	R/W	0h	Force txd_a_lfps_sel active

Table 12-547. TX_PSC_A5__TX_PSC_A4_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	TX_PSC_A4_9	R/W	0h	LFPS clock gate enable
8	TX_PSC_A4_8	R/W	0h	Reserved - spare
7	TX_PSC_A4_7	R/W	1h	Transmitter low current mode
6	TX_PSC_A4_6	R/W	0h	Transmitter mission mode enable
5	TX_PSC_A4_5	R/W	0h	TX driver common mode enable
4	TX_PSC_A4_4	R/W	0h	TX driver enable
3	TX_PSC_A4_3	R/W	0h	TX post-emphasis enable (C+1)
2	TX_PSC_A4_2	R/W	0h	TX pre-emphasis enable (C-1)
1	TX_PSC_A4_1	R/W	0h	TX pre-driver enable
0	TX_PSC_A4_0	R/W	0h	TX serializer enable

Table 12-548. Register Call Summary for TX_PSC_A5__TX_PSC_A4_j

10-G SerDes Registers

- [TX_PSC_A5__TX_PSC_A4_j Register \(Offset = 4208h + formula\) \[reset = 880h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.183 TX_PSC_RDY__TX_PSC_CAL_j Register (Offset = 420Ch + formula) [reset = 00A000A0h]

TX_PSC_RDY__TX_PSC_CAL_j is shown in Figure 12-183 and described in Table 12-550.

Return to [Summary Table](#).

Transmitter calibration power state definition register

Offset = 420Ch + (j * 400h); where j = 0h to 3h

**Table 12-549. TX_PSC_RDY__TX_PSC_CAL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 420Ch + formula

Figure 12-183. TX_PSC_RDY__TX_PSC_CAL_j Register

31	30	29	28	27	26	25	24
TX_PSC_RDY_15_12				TX_PSC_RDY_11	TX_PSC_RDY_10	TX_PSC_RDY_9	TX_PSC_RDY_8
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
TX_PSC_RDY_7	TX_PSC_RDY_6	TX_PSC_RDY_5	TX_PSC_RDY_4	TX_PSC_RDY_3	TX_PSC_RDY_2	TX_PSC_RDY_1	TX_PSC_RDY_0
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
TX_PSC_CAL_15_12				TX_PSC_CAL_11	TX_PSC_CAL_10	TX_PSC_CAL_9	TX_PSC_CAL_8
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TX_PSC_CAL_7	TX_PSC_CAL_6	TX_PSC_CAL_5	TX_PSC_CAL_4	TX_PSC_CAL_3	TX_PSC_CAL_2	TX_PSC_CAL_1	TX_PSC_CAL_0
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-550. TX_PSC_RDY__TX_PSC_CAL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TX_PSC_RDY_15_12	R	0h	Reserved
27	TX_PSC_RDY_11	R/W	0h	TX driver common mode enable extend control
26	TX_PSC_RDY_10	R/W	0h	Force txda_lfps_sel active
25	TX_PSC_RDY_9	R/W	0h	LFPS clock gate enable
24	TX_PSC_RDY_8	R/W	0h	Reserved - spare
23	TX_PSC_RDY_7	R/W	1h	Transmitter low current mode
22	TX_PSC_RDY_6	R/W	0h	Transmitter mission mode enable
21	TX_PSC_RDY_5	R/W	1h	TX driver common mode enable
20	TX_PSC_RDY_4	R/W	0h	TX driver enable
19	TX_PSC_RDY_3	R/W	0h	TX post-emphasis enable (C+1)
18	TX_PSC_RDY_2	R/W	0h	TX pre-emphasis enable (C-1)
17	TX_PSC_RDY_1	R/W	0h	TX pre-driver enable
16	TX_PSC_RDY_0	R/W	0h	TX serializer enable
15-12	TX_PSC_CAL_15_12	R	0h	Reserved

Table 12-550. TX_PSC_RDY__TX_PSC_CAL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TX_PSC_CAL_11	R/W	0h	TX driver common mode enable extend control
10	TX_PSC_CAL_10	R/W	0h	Force txda_lfps_sel active
9	TX_PSC_CAL_9	R/W	0h	LFPS clock gate enable
8	TX_PSC_CAL_8	R/W	0h	Reserved - spare
7	TX_PSC_CAL_7	R/W	1h	Transmitter low current mode
6	TX_PSC_CAL_6	R/W	0h	Transmitter mission mode enable
5	TX_PSC_CAL_5	R/W	1h	TX driver common mode enable
4	TX_PSC_CAL_4	R/W	0h	TX driver enable
3	TX_PSC_CAL_3	R/W	0h	TX post-emphasis enable (C+1)
2	TX_PSC_CAL_2	R/W	0h	TX pre-emphasis enable (C-1)
1	TX_PSC_CAL_1	R/W	0h	TX pre-driver enable
0	TX_PSC_CAL_0	R/W	0h	TX serializer enable

Table 12-551. Register Call Summary for TX_PSC_RDY__TX_PSC_CAL_j

10-G SerDes Registers

- [TX_PSC_RDY__TX_PSC_CAL_j Register \(Offset = 420Ch + formula\) \[reset = 00A000A0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.184 TX_RCVDET_OVRD__TX_RCVDET_CTRL_j Register (Offset = 4240h + formula) [reset = 0h]

TX_RCVDET_OVRD__TX_RCVDET_CTRL_j is shown in Figure 12-184 and described in Table 12-553.

Return to [Summary Table](#).

Transmit receiver detect control register

Offset = 4240h + (j * 400h); where j = 0h to 3h

Table 12-552.
TX_RCVDET_OVRD__TX_RCVDET_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 4240h + formula

Figure 12-184. TX_RCVDET_OVRD__TX_RCVDET_CTRL_j Register

31	30	29	28	27	26	25	24
TX_RCVDET_OVRD_15	TX_RCVDET_OVRD_14	TX_RCVDET_OVRD_13_0					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
TX_RCVDET_OVRD_13_0							
R-0h							
15	14	13	12	11	10	9	8
TX_RCVDET_CTRL_15	TX_RCVDET_CTRL_14	TX_RCVDET_CTRL_13	TX_RCVDET_CTRL_12_0				
R/W-0h	R-0h	R-0h	R-0h				
7	6	5	4	3	2	1	0
TX_RCVDET_CTRL_12_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-553. TX_RCVDET_OVRD__TX_RCVDET_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_RCVDET_OVRD_15	R/W	0h	Receiver detect override enable: Activation (1'b1) of this register bit enables the tx_rcv_detected output from the receiver detect state machine to be driven directly by the receiver detect override bit in this register.
30	TX_RCVDET_OVRD_14	R/W	0h	Receiver detect override: When the receiver detect override enable bit in this register is active (1'b1), this bit will directly control the tx_rcv_detected output from the receiver detect state machine.
29-16	TX_RCVDET_OVRD_13_0	R	0h	Reserved

Table 12-553. TX_RCVDET_OVRD__TX_RCVDET_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	TX_RCVDET_CTRL_15	R/W	0h	<p>Start receiver detect: Activating (1'b1) this bit will start the receiver detect process.</p> <p>This bit must remain active until the receiver detect process is complete, as indicated by the receiver detect process done bit in this register.</p> <p>To start another receiver detect process, this register must first be set inactive (1'b0) until the receiver detect process done bit in this register is cleared.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>The receiver detect process must not be under the control of the top level tx_rcv_detect_en pin when attempting to initiate the process using this register.</p>
14	TX_RCVDET_CTRL_14	R	0h	<p>Receiver detect process done: This bit will be set to 1'b1 when the receiver detect process is complete.</p> <p>It will be cleared by cmn_reset_n, or by the deactivation of the start receiver detect bit in this register.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p>
13	TX_RCVDET_CTRL_13	R	0h	<p>Receiver detected: When the receiver detect process is complete, this register bit will indicate the current state of the tx_rcv_detected pin.</p>
12-0	TX_RCVDET_CTRL_12_0	R	0h	Reserved

Table 12-554. Register Call Summary for TX_RCVDET_OVRD__TX_RCVDET_CTRL_j

10-G SerDes Registers

- [TX_RCVDET_OVRD__TX_RCVDET_CTRL_j Register \(Offset = 4240h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.185 TX_RCVDET_ST_TMR__TX_RCVDET_EN_TMR_j Register (Offset = 4244h + formula) [reset = 09C40000h]

TX_RCVDET_ST_TMR__TX_RCVDET_EN_TMR_j is shown in Figure 12-185 and described in Table 12-556.

Return to [Summary Table](#).

Transmit receiver detect enable timer register

Offset = 4244h + (j * 400h); where j = 0h to 3h

Table 12-555.
TX_RCVDET_ST_TMR__TX_RCVDET_EN_TMR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 4244h + formula

Figure 12-185. TX_RCVDET_ST_TMR__TX_RCVDET_EN_TMR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_RCVDET_ST_TMR_15_0															
R/W-9C4h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_RCVDET_EN_TMR_15_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-556. TX_RCVDET_ST_TMR__TX_RCVDET_EN_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_RCVDET_ST_TMR_15_0	R/W	9C4h	Start wait time value: This is the number of clocks the receiver detect state machine waits between driving the txda_rcvdet_start signal active and checking the results on the txda_rcvdet_detected_n signal coming from the analog. The default required wait time is 100us.
15-0	TX_RCVDET_EN_TMR_15_0	R/W	0h	Enable wait time value: This is the number of clocks the receiver detect state machine waits between driving the txda_rcvdet_en signal active and driving the txda_rcvdet_start signal active going to the analog.

Table 12-557. Register Call Summary for TX_RCVDET_ST_TMR__TX_RCVDET_EN_TMR_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_RCVDET_ST_TMR__TX_RCVDET_EN_TMR_j Register \(Offset = 4244h + formula\) \[reset = 09C40000h\]: \[0\]](#)

12.186 TX_BIST_UDDWR__TX_BIST_CTRL_j Register (Offset = 4280h + formula) [reset = 0h]

TX_BIST_UDDWR__TX_BIST_CTRL_j is shown in [Figure 12-186](#) and described in [Table 12-559](#).

Return to [Summary Table](#).

Transmit BIST control register

Offset = 4280h + (j * 400h); where j = 0h to 3h

**Table 12-558. TX_BIST_UDDWR__TX_BIST_CTRL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 4280h + formula

Figure 12-186. TX_BIST_UDDWR__TX_BIST_CTRL_j Register

31	30	29	28	27	26	25	24
TX_BIST_UDDWR_15_10						TX_BIST_UDDWR_9_0	
R-0h						W-0h	
23	22	21	20	19	18	17	16
TX_BIST_UDDWR_9_0							
W-0h							
15	14	13	12	11	10	9	8
TX_BIST_CTRL_15_12				TX_BIST_CTRL_11_8			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
TX_BIST_CTRL_7_5			TX_BIST_CTRL_4	TX_BIST_CTRL_3_2		TX_BIST_CTRL_1	TX_BIST_CTRL_0
R-0h			R/W-0h	R-0h		W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 12-559. TX_BIST_UDDWR__TX_BIST_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	TX_BIST_UDDWR_15_10	R	0h	Reserved
25-16	TX_BIST_UDDWR_9_0	W	0h	Transmitter BIST user defined data: Writing a data word to this field will result in that data word being placed in the next available position in the transmitter BIST user defined data FIFO. Note, when in 20 bit mode, all 10 of these bits are used. When in 16 bit mode, only the least significant 8 bits are used. Note that the FIFO in this implementation is 18 words deep. It is up to the user to not write more than 18 words of data into this FIFO. Exceeding this amount of data will generate unpredictable results.
15-12	TX_BIST_CTRL_15_12	R	0h	Reserved

Table 12-559. TX_BIST_UDDWR_TX_BIST_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	TX_BIST_CTRL_11_8	R/W	0h	Transmitter BIST mode: Controls which mode the BIST will operate in. The value of this field must match the corresponding field for the receive BIST controller. The following are the values used for this field, and what BIST mode they correspond to. 4'b 0000 : User defined data FIFO 4'b 0001 - 4'b 0111 : Reserved 4'b 1000 : PRBS 7 : 7 bit LFSR 4'b 1001 : PRBS 15 : 15 bit LFSR 4'b 1010 : PRBS 23 : 23 bit LFSR 4'b 1011 : PRBS 31 : 31 bit LFSR 4'b 1100 - 4'b 1111 : Reserved
7-5	TX_BIST_CTRL_7_5	R	0h	Reserved
4	TX_BIST_CTRL_4	R/W	0h	Transmitter BIST force error: When this bit transitions from 1'b0 to 1'b1, the transmit BIST controller will force an error to be transmitted from the BIST logic, by inverting one of the parallel data bits.
3-2	TX_BIST_CTRL_3_2	R	0h	Reserved
1	TX_BIST_CTRL_1	W	0h	Transmitter BIST user defined data FIFO clear: Writing a 1'b1 to this bit will clear the transmitter BIST user defined data FIFO. Note : This bit is automatically cleared after it is written to. Note : This clear function simply resets the FIFO pointers. It does not clear the contents of the FIFO.
0	TX_BIST_CTRL_0	R/W	0h	Transmitter BIST enable: This bit enables the transmitter BIST function. Note : The remaining bits in this register must be stable when changing this bit. Therefore, it is best to enable and disable this function using a read / modify / write of this bit.

Table 12-560. Register Call Summary for TX_BIST_UDDWR_TX_BIST_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_BIST_UDDWR_TX_BIST_CTRL_j Register \(Offset = 4280h + formula\) \[reset = 0h\]: \[0\]](#)

12.187 TX_BIST_SEED1__TX_BIST_SEED0_j Register (Offset = 4284h + formula) [reset = 1h]

TX_BIST_SEED1__TX_BIST_SEED0_j is shown in [Figure 12-187](#) and described in [Table 12-562](#).

Return to [Summary Table](#).

Transmit BIST PRBS seed 0 register

Offset = 4284h + (j * 400h); where j = 0h to 3h

**Table 12-561. TX_BIST_SEED1__TX_BIST_SEED0_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 4284h + formula

Figure 12-187. TX_BIST_SEED1__TX_BIST_SEED0_j Register

31	30	29	28	27	26	25	24
TX_BIST_SEE D1_15	TX_BIST_SEED1_14_0						
R-0h	R/W-0h						
23	22	21	20	19	18	17	16
TX_BIST_SEED1_14_0							
R/W-0h							
15	14	13	12	11	10	9	8
TX_BIST_SEED0_15_0							
R/W-1h							
7	6	5	4	3	2	1	0
TX_BIST_SEED0_15_0							
R/W-1h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-562. TX_BIST_SEED1__TX_BIST_SEED0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TX_BIST_SEED1_15	R	0h	Reserved
30-16	TX_BIST_SEED1_14_0	R/W	0h	Transmitter BIST PRBS seed (30:16): When the BIST is in PRBS mode, this field provides a seed for the PRBS, such that different lanes can have different BIST patterns. Note that this field contains the most significant 15 bits of the full 31 bit seed value. Note: When combined, this register and the Transmit BIST PRBS seed 0 register on page 214 must never be all 0s.
15-0	TX_BIST_SEED0_15_0	R/W	1h	Transmitter BIST PRBS seed (15:0): When the BIST is in PRBS mode, this field provides a seed for the PRBS, such that different lanes can have different BIST patterns. Note that this field contains the least significant 16 bits of the full 31 bit seed value. Note: When combined, this register and the Transmit BIST PRBS seed 1 register on page 214 must never be all 0s.

Table 12-563. Register Call Summary for TX_BIST_SEED1__TX_BIST_SEED0_j

10-G SerDes Registers

- [TX_BIST_SEED1__TX_BIST_SEED0_j Register \(Offset = 4284h + formula\) \[reset = 1h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.188 TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j Register (Offset = 43C0h + formula) [reset = 060C0000h]

TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j is shown in Figure 12-188 and described in Table 12-565.

Return to [Summary Table](#).

TX sync FIFO diagnostic control register

Offset = 43C0h + (j * 400h); where j = 0h to 3h

Table 12-564. TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 43C0h + formula

Figure 12-188. TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j Register

31	30	29	28	27	26	25	24
TX_DIAG_SFIFO_TMR_15_14		TX_DIAG_SFIFO_TMR_13_8					
R-0h		R/W-6h					
23	22	21	20	19	18	17	16
TX_DIAG_SFIFO_TMR_7_6		TX_DIAG_SFIFO_TMR_5_0					
R-0h		R/W-Ch					
15	14	13	12	11	10	9	8
TX_DIAG_SFIFO_CTRL_15_5							
R-0h							
7	6	5	4	3	2	1	0
TX_DIAG_SFIFO_CTRL_15_5			TX_DIAG_SFIFO_CTRL_4	TX_DIAG_SFIFO_CTRL_3	TX_DIAG_SFIFO_CTRL_2	TX_DIAG_SFIFO_CTRL_1	TX_DIAG_SFIFO_CTRL_0
R-0h			R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-565. TX_DIAG_SFIFO_TMR_TX_DIAG_SFIFO_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	TX_DIAG_SFIFO_TMR_15_14	R	0h	Reserved
29-24	TX_DIAG_SFIFO_TMR_13_8	R/W	6h	FIFO alignment settle delay: This field specifies the number of clocks to wait for a prior change to the enqueue pointer to complete before initiating the check phase of the alignment procedure in the sync FIFO. It drives the fifo_align_settle_del pin of the FIFO.
23-22	TX_DIAG_SFIFO_TMR_7_6	R	0h	Reserved
21-16	TX_DIAG_SFIFO_TMR_5_0	R/W	Ch	FIFO alignment detect delay: This field specifies the number of clocks to wait in the delay state for each phase of the alignment procedure in the sync FIFO. It drives the fifo_align_detect_del pin of the FIFO.
15-5	TX_DIAG_SFIFO_CTRL_15_5	R	0h	Reserved
4	TX_DIAG_SFIFO_CTRL_4	R/W	0h	FIFO enqueue pointer bump: This bit can be used to decrement the enqueue pointer relative to the dequeue pointer, for diagnostic purposes. Changing this bit from a value of 1'b0 to 1'b1 will trigger a single decrement of the enqueue pointer.

Table 12-565. TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TX_DIAG_SFIFO_CTRL_3	R	0h	<p>FIFO pointers overlapping: This bit indicates that the current enqueue and dequeue pointers have been detected as overlapping. This is not necessarily an error condition.</p> <p>For example, the pointers could be overlapping but the enqueue pointer could be skewed later in time relative to the dequeue pointer. In this scenario, the actual enqueue would take place after the dequeue.</p> <p>The intention of this bit is to be used with the FIFO enqueue pointer bump bit in this register to move the pointers around and determine their relative positions.</p> <p>Note: The reset value for this field is with the transceiver data path power island switched off.</p> <p>In cases where this power island is switched on, the reset value be 1'b1</p>
2	TX_DIAG_SFIFO_CTRL_2	R	0h	<p>FIFO alignment acknowledge: This bit indicates that the FIFO alignment process is complete, as initiated either automatically by the hardware of the FIFO alignment enable override bits in this register.</p> <p>This bit is driven directly by the fifo_align_ack pin of the FIFO.</p>
1	TX_DIAG_SFIFO_CTRL_1	R/W	0h	<p>FIFO alignment enable override enable: This bit enables the FIFO alignment enable override register to drive the fifo_align_en pin of the FIFO directly for diagnostic purposes.</p> <p>1'b 0: Override disabled 1'b 1: Override enabled.</p>
0	TX_DIAG_SFIFO_CTRL_0	R/W	0h	<p>FIFO alignment enable override: When enabled by the FIFO alignment enable override enable bit in this register, this bit directly controls the fifo_align_en pin of the FIFO to provide a means of running the FIFO alignment function for diagnostic purposes.</p>

Table 12-566. Register Call Summary for TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j

10-G SerDes Registers

- [TX_DIAG_SFIFO_TMR__TX_DIAG_SFIFO_CTRL_j Register \(Offset = 43C0h + formula\) \[reset = 060C0000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.189 TX_DIAG_ELEC_IDLE_j Register (Offset = 43C4h + formula) [reset = X]

TX_DIAG_ELEC_IDLE_j is shown in Figure 12-189 and described in Table 12-568.

Return to [Summary Table](#).

TX electrical idle diagnostic register

Offset = 43C4h + (j * 400h); where j = 0h to 3h

Table 12-567. TX_DIAG_ELEC_IDLE_j Instances

Instance	Physical Address
SERDES_10G0	0505 43C4h + formula

Figure 12-189. TX_DIAG_ELEC_IDLE_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
TX_DIAG_ELEC_IDLE_15_12				TX_DIAG_ELEC_IDLE_11_8			
R/W-4h				R/W-4h			
7	6	5	4	3	2	1	0
TX_DIAG_ELEC_IDLE_7_4				TX_DIAG_ELEC_IDLE_3_0			
R/W-3h				R/W-3h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-568. TX_DIAG_ELEC_IDLE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-12	TX_DIAG_ELEC_IDLE_15_12	R/W	4h	TX electrical idle exit delay 16 bit data width : This field controls the amount of additional delay added to the electrical idle signal after the sync FIFO, when exiting the electrical idle state for 16 bit data width modes. The valid values that can be used for this field are the same as those in the TX electrical idle entry delay 20 bit data width field of this register.
11-8	TX_DIAG_ELEC_IDLE_11_8	R/W	4h	TX electrical idle entry delay 16 bit data width : This field controls the amount of additional delay added to the electrical idle signal after the sync FIFO, when entering the electrical idle state for 16 bit data width modes. The valid values that can be used for this field are the same as those in the TX electrical idle entry delay 20 bit data width field of this register.
7-4	TX_DIAG_ELEC_IDLE_7_4	R/W	3h	TX electrical idle exit delay 20 bit data width : This field controls the amount of additional delay added to the electrical idle signal after the sync FIFO, when exiting the electrical idle state for 20 bit data width modes. The valid values that can be used for this field are the same as those in the TX electrical idle entry delay 20 bit data width field of this register.

Table 12-568. TX_DIAG_ELEC_IDLE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	TX_DIAG_ELEC_IDLE_3_0	R/W	3h	<p>TX electrical idle entry delay 20 bit data width : This field controls the amount of additional delay added to the electrical idle signal after the sync FIFO, when entering the electrical idle state for 20 bit data width modes.</p> <p>The following are the valid values that can be used for this field, and the corresponding delays.</p> <p>Note that in the cases of 1/2 clock cycle delays, this is implemented on the falling edge of the clock, so the result is a function of the duty cycle of the clock.</p> <p>4'b 0000 : Reserved.</p> <p>4'b 0001 : Reserved.</p> <p>4'b 0010 : 1.0 clock delays.</p> <p>4'b 0011 : 1.5 clock delays.</p> <p>4'b 0100 : 2.0 clock delays.</p> <p>4'b 0101 : 2.5 clock delays.</p> <p>4'b 0110 : 3.0 clock delays.</p> <p>4'b 0111 : 3.5 clock delays.</p> <p>4'b 1000 : 4.0 clock delays.</p> <p>4'b 1001 : 4.5 clock delays.</p> <p>4'b 1010 : 5.0 clock delays.</p> <p>4'b 1011 : 5.5 clock delays.</p> <p>4'b 1100 : 6.0 clock delays.</p> <p>4'b 1101 : 6.5 clock delays.</p> <p>4'b 1110 : 7.0 clock delays.</p> <p>4'b 1111 : 7.5 clock delays.</p>

Table 12-569. Register Call Summary for TX_DIAG_ELEC_IDLE_j

10-G SerDes Registers

- [TX_DIAG_ELEC_IDLE_j Register \(Offset = 43C4h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.190 TX_DIAG_RST_DIAG_j Register (Offset = 43C8h + formula) [reset = X]

TX_DIAG_RST_DIAG_j is shown in [Figure 12-190](#) and described in [Table 12-571](#).

Return to [Summary Table](#).

Transmitter control reset diagnostic register

Offset = 43C8h + (j * 400h); where j = 0h to 3h

Table 12-570. TX_DIAG_RST_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 43C8h + formula

Figure 12-190. TX_DIAG_RST_DIAG_j Register

31	30	29	28	27	26	25	24
TX_DIAG_RST_DIAG_15_5							
R-0h							
23	22	21	20	19	18	17	16
TX_DIAG_RST_DIAG_15_5			TX_DIAG_RST_DIAG_4	TX_DIAG_RST_DIAG_3	TX_DIAG_RST_DIAG_2	TX_DIAG_RST_DIAG_1	TX_DIAG_RST_DIAG_0
R-0h			R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							
R-X							

LEGEND: R = Read Only; -n = value after reset

Table 12-571. TX_DIAG_RST_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	TX_DIAG_RST_DIAG_15_5	R	0h	Reserved
20	TX_DIAG_RST_DIAG_4	R	0h	Current state of the txda_tx_clk_reset_n reset.
19	TX_DIAG_RST_DIAG_3	R	0h	Current state of the tx_dig_reset_n reset.
18	TX_DIAG_RST_DIAG_2	R	0h	Current state of the tx_sync_fifo_deq_rst_n reset.
17	TX_DIAG_RST_DIAG_1	R	0h	Current state of the tx_sync_fifo_enq_rst_n reset.
16	TX_DIAG_RST_DIAG_0	R	0h	Current state of the tx_lfps_reset_n reset.
15-0	RESERVED	R	X	

Table 12-572. Register Call Summary for TX_DIAG_RST_DIAG_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [TX_DIAG_RST_DIAG_j Register \(Offset = 43C8h + formula\) \[reset = X\]: \[0\]](#)

12.191 TX_DIAG_ACYA__TX_DIAG_DCYA_j Register (Offset = 43CCCh + formula) [reset = 0h]

TX_DIAG_ACYA__TX_DIAG_DCYA_j is shown in Figure 12-191 and described in Table 12-574.

Return to [Summary Table](#).

Transmitter digital cover your alternatives register

Offset = 43CCCh + (j * 400h); where j = 0h to 3h

**Table 12-573. TX_DIAG_ACYA__TX_DIAG_DCYA_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 43CCCh + formula

Figure 12-191. TX_DIAG_ACYA__TX_DIAG_DCYA_j Register

31	30	29	28	27	26	25	24
TX_DIAG_ACYA_15_1							
R/W-0h							
23	22	21	20	19	18	17	16
TX_DIAG_ACYA_15_1							TX_DIAG_ACYA_0
R/W-0h							R/W-0h
15	14	13	12	11	10	9	8
TX_DIAG_DCYA_15_0							
R/W-0h							
7	6	5	4	3	2	1	0
TX_DIAG_DCYA_15_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-574. TX_DIAG_ACYA__TX_DIAG_DCYA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	TX_DIAG_ACYA_15_1	R/W	0h	Reserved - spare
16	TX_DIAG_ACYA_0	R/W	0h	HBDC latch control: Controls the state of the latches associated with the H bridge driver controller related signals in the H bridge driver encoder logic digital in the transmitter analog, as well as the boost enable and level control signals. These latches can be closed to hold the current state of these signals. While closed, the signals that drive the latch inputs can be changed by writing the registers that control them, and not effect the state of the driver. Once such register writes are complete, the latches can be made transparent again to apply the changes. 1'b 0: Latches transparent 1'b 1: Latches gated
15-0	TX_DIAG_DCYA_15_0	R/W	0h	Reserved - spare

Table 12-575. Register Call Summary for TX_DIAG_ACYA__TX_DIAG_DCYA_j

10-G SerDes Registers

- TX_DIAG_ACYA__TX_DIAG_DCYA_j Register (Offset = 43CCCh + formula) [reset = 0h]: [0]
- 10-G SerDes Registers: [0]

12.192 RESERVEDBIT13ADDRESSB_y Register (Offset = 6000h + formula) [reset = 0h]

RESERVEDBIT13ADDRESSB_y is shown in Figure 12-192 and described in Table 12-577.

Return to [Summary Table](#).

Reserved Address bit 13 area B

Offset = 6000h + (y * 4h); where y = 0h to 7FFh

**Table 12-576. RESERVEDBIT13ADDRESSB_y
Instances**

Instance	Physical Address
SERDES_10G0	0505 6000h + formula

Figure 12-192. RESERVEDBIT13ADDRESSB_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES_BIT13_ADR_B																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-577. RESERVEDBIT13ADDRESSB_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES_BIT13_ADR_B	R/W	0h	Write only test region B

Table 12-578. Register Call Summary for RESERVEDBIT13ADDRESSB_y

10-G SerDes Registers

- [RESERVEDBIT13ADDRESSB_y Register \(Offset = 6000h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.193 RX_PSC_A1__RX_PSC_A0_j Register (Offset = 8000h + formula) [reset = 091D091Dh]

RX_PSC_A1__RX_PSC_A0_j is shown in Figure 12-193 and described in Table 12-580.

Return to [Summary Table](#).

Receiver A0 power state definition register

Offset = 8000h + (j * 400h); where j = 0h to 3h

**Table 12-579. RX_PSC_A1__RX_PSC_A0_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 8000h + formula

Figure 12-193. RX_PSC_A1__RX_PSC_A0_j Register

31	30	29	28	27	26	25	24
RX_PSC_A1_15_13			RX_PSC_A1_1_2	RX_PSC_A1_1_1	RX_PSC_A1_1_0	RX_PSC_A1_9	RX_PSC_A1_8
R-0h			R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h
23	22	21	20	19	18	17	16
RX_PSC_A1_7_5			RX_PSC_A1_4	RX_PSC_A1_3	RX_PSC_A1_2	RX_PSC_A1_1	RX_PSC_A1_0
R/W-0h			R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
RX_PSC_A0_15_13			RX_PSC_A0_1_2	RX_PSC_A0_1_1	RX_PSC_A0_1_0	RX_PSC_A0_9	RX_PSC_A0_8
R-0h			R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RX_PSC_A0_7_5			RX_PSC_A0_4	RX_PSC_A0_3	RX_PSC_A0_2	RX_PSC_A0_1	RX_PSC_A0_0
R/W-0h			R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-580. RX_PSC_A1__RX_PSC_A0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RX_PSC_A1_15_13	R	0h	Reserved
28	RX_PSC_A1_12	R/W	0h	RX signal detect enable extend control
27	RX_PSC_A1_11	R/W	1h	RX signal detect filter enable
26	RX_PSC_A1_10	R/W	0h	RX LFPS detect filter enable
25	RX_PSC_A1_9	R/W	0h	Reserved - spare
24	RX_PSC_A1_8	R/W	1h	RX signal detect enable
23-21	RX_PSC_A1_7_5	R/W	0h	Reserved - spare
20	RX_PSC_A1_4	R/W	1h	RX equalizer engine enable
19	RX_PSC_A1_3	R/W	1h	RX DFE equalization enable.
18	RX_PSC_A1_2	R/W	1h	RX PI enable
17	RX_PSC_A1_1	R/W	0h	RX e path enable (calibration and eye surf only)
16	RX_PSC_A1_0	R/W	1h	RX enable
15-13	RX_PSC_A0_15_13	R	0h	Reserved
12	RX_PSC_A0_12	R/W	0h	RX signal detect enable extend control: Specifies which power states the rx_sig_det_en_ext signal is considered valid in and can be used to force the signal detect functions to remain on.

Table 12-580. RX_PSC_A1__RX_PSC_A0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_PSC_A0_11	R/W	1h	RX signal detect filter enable: Enables the receiver signal detect filter function in the digital receiver controller.
10	RX_PSC_A0_10	R/W	0h	RX LFPS detect filter enable: Enables the receiver LFPS detect filter function in the digital receiver controller.
9	RX_PSC_A0_9	R/W	0h	Reserved - spare
8	RX_PSC_A0_8	R/W	1h	RX signal detect enable: Enables the receiver signal detect function. This drives the rxda_sd_en signal going to the analog. Note that this bit needs to be active for LFPS detect functions to work, because these functions share the same analog circuits.
7-5	RX_PSC_A0_7_5	R/W	0h	Reserved - spare
4	RX_PSC_A0_4	R/W	1h	RX equalizer engine enable: Specifies which power state the REE runs in. 1'b 0: Disabled 1'b 1: Enabled
3	RX_PSC_A0_3	R/W	1h	RX DFE equalization enable: Enables the receiver DFE equalization circuits, via the rxda_dfe_eq_enable signal.
2	RX_PSC_A0_2	R/W	1h	RX PI enable: Enables the receiver circuits related to the PI and associated clocking components.
1	RX_PSC_A0_1	R/W	0h	RX e path enable (calibration and eye surf only) : Enables the receiver circuits related to the eye plot PI and e path deserializer for calibration and eye surf.
0	RX_PSC_A0_0	R/W	1h	RX enable: Enables the receiver circuits related to the CDRLF, Sampler, FE, and Deserializer.

Table 12-581. Register Call Summary for RX_PSC_A1__RX_PSC_A0_j

10-G SerDes Registers

- [RX_PSC_A1__RX_PSC_A0_j Register \(Offset = 8000h + formula\) \[reset = 091D091Dh\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.194 RX_PSC_A3__RX_PSC_A2_j Register (Offset = 8004h + formula) [reset = 900h]

RX_PSC_A3__RX_PSC_A2_j is shown in [Figure 12-194](#) and described in [Table 12-583](#).

Return to [Summary Table](#).

Receiver A2 power state definition register

Offset = 8004h + (j * 400h); where j = 0h to 3h

**Table 12-582. RX_PSC_A3__RX_PSC_A2_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 8004h + formula

Figure 12-194. RX_PSC_A3__RX_PSC_A2_j Register

31	30	29	28	27	26	25	24
RX_PSC_A3_15_13			RX_PSC_A3_12	RX_PSC_A3_11	RX_PSC_A3_10	RX_PSC_A3_9	RX_PSC_A3_8
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RX_PSC_A3_7_5			RX_PSC_A3_4	RX_PSC_A3_3	RX_PSC_A3_2	RX_PSC_A3_1	RX_PSC_A3_0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_PSC_A2_15_13			RX_PSC_A2_12	RX_PSC_A2_11	RX_PSC_A2_10	RX_PSC_A2_9	RX_PSC_A2_8
R-0h			R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RX_PSC_A2_7_5			RX_PSC_A2_4	RX_PSC_A2_3	RX_PSC_A2_2	RX_PSC_A2_1	RX_PSC_A2_0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-583. RX_PSC_A3__RX_PSC_A2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RX_PSC_A3_15_13	R	0h	Reserved
28	RX_PSC_A3_12	R/W	0h	RX signal detect enable extend control
27	RX_PSC_A3_11	R/W	0h	RX signal detect filter enable
26	RX_PSC_A3_10	R/W	0h	RX LFPS detect filter enable
25	RX_PSC_A3_9	R/W	0h	Reserved - spare
24	RX_PSC_A3_8	R/W	0h	RX signal detect enable
23-21	RX_PSC_A3_7_5	R/W	0h	Reserved - spare
20	RX_PSC_A3_4	R/W	0h	RX equalizer engine enable
19	RX_PSC_A3_3	R/W	0h	RX DFE equalization enable.
18	RX_PSC_A3_2	R/W	0h	RX PI enable
17	RX_PSC_A3_1	R/W	0h	RX e path enable (calibration and eye surf only)
16	RX_PSC_A3_0	R/W	0h	RX enable
15-13	RX_PSC_A2_15_13	R	0h	Reserved
12	RX_PSC_A2_12	R/W	0h	RX signal detect enable extend control
11	RX_PSC_A2_11	R/W	1h	RX signal detect filter enable

Table 12-583. RX_PSC_A3__RX_PSC_A2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_PSC_A2_10	R/W	0h	RX LFPS detect filter enable
9	RX_PSC_A2_9	R/W	0h	Reserved - spare
8	RX_PSC_A2_8	R/W	1h	RX signal detect enable
7-5	RX_PSC_A2_7_5	R/W	0h	Reserved - spare
4	RX_PSC_A2_4	R/W	0h	RX equalizer engine enable
3	RX_PSC_A2_3	R/W	0h	RX DFE equalization enable.
2	RX_PSC_A2_2	R/W	0h	RX PI enable
1	RX_PSC_A2_1	R/W	0h	RX e path enable (calibration and eye surf only)
0	RX_PSC_A2_0	R/W	0h	RX enable

Table 12-584. Register Call Summary for RX_PSC_A3__RX_PSC_A2_j

10-G SerDes Registers

- [RX_PSC_A3__RX_PSC_A2_j Register \(Offset = 8004h + formula\) \[reset = 900h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.195 RX_PSC_A5_RX_PSC_A4_j Register (Offset = 8008h + formula) [reset = 1000h]

RX_PSC_A5_RX_PSC_A4_j is shown in Figure 12-195 and described in Table 12-586.

Return to [Summary Table](#).

Receiver A4 power state definition register

Offset = 8008h + (j * 400h); where j = 0h to 3h

Table 12-585. RX_PSC_A5_RX_PSC_A4_j Instances

Instance	Physical Address
SERDES_10G0	0505 8008h + formula

Figure 12-195. RX_PSC_A5_RX_PSC_A4_j Register

31	30	29	28	27	26	25	24
RX_PSC_A5_15_13			RX_PSC_A5_12	RX_PSC_A5_11	RX_PSC_A5_10	RX_PSC_A5_9	RX_PSC_A5_8
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RX_PSC_A5_7_5			RX_PSC_A5_4	RX_PSC_A5_3	RX_PSC_A5_2	RX_PSC_A5_1	RX_PSC_A5_0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_PSC_A4_15_13			RX_PSC_A4_12	RX_PSC_A4_11	RX_PSC_A4_10	RX_PSC_A4_9	RX_PSC_A4_8
R-0h			R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_PSC_A4_7_5			RX_PSC_A4_4	RX_PSC_A4_3	RX_PSC_A4_2	RX_PSC_A4_1	RX_PSC_A4_0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-586. RX_PSC_A5_RX_PSC_A4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RX_PSC_A5_15_13	R	0h	Reserved
28	RX_PSC_A5_12	R/W	0h	RX signal detect enable extend control
27	RX_PSC_A5_11	R/W	0h	RX signal detect filter enable
26	RX_PSC_A5_10	R/W	0h	RX LFPS detect filter enable
25	RX_PSC_A5_9	R/W	0h	Reserved - spare
24	RX_PSC_A5_8	R/W	0h	RX signal detect enable
23-21	RX_PSC_A5_7_5	R/W	0h	Reserved - spare
20	RX_PSC_A5_4	R/W	0h	RX equalizer engine enable
19	RX_PSC_A5_3	R/W	0h	RX DFE equalization enable.
18	RX_PSC_A5_2	R/W	0h	RX PI enable
17	RX_PSC_A5_1	R/W	0h	RX e path enable (calibration and eye surf only)
16	RX_PSC_A5_0	R/W	0h	RX enable
15-13	RX_PSC_A4_15_13	R	0h	Reserved
12	RX_PSC_A4_12	R/W	1h	RX signal detect enable extend control
11	RX_PSC_A4_11	R/W	0h	RX signal detect filter enable

Table 12-586. RX_PSC_A5__RX_PSC_A4_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_PSC_A4_10	R/W	0h	RX LFPS detect filter enable
9	RX_PSC_A4_9	R/W	0h	Reserved - spare
8	RX_PSC_A4_8	R/W	0h	RX signal detect enable
7-5	RX_PSC_A4_7_5	R/W	0h	Reserved - spare
4	RX_PSC_A4_4	R/W	0h	RX equalizer engine enable
3	RX_PSC_A4_3	R/W	0h	RX DFE equalization enable.
2	RX_PSC_A4_2	R/W	0h	RX PI enable
1	RX_PSC_A4_1	R/W	0h	RX e path enable (calibration and eye surf only)
0	RX_PSC_A4_0	R/W	0h	RX enable

Table 12-587. Register Call Summary for RX_PSC_A5__RX_PSC_A4_j

10-G SerDes Registers

- [RX_PSC_A5__RX_PSC_A4_j Register \(Offset = 8008h + formula\) \[reset = 1000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.196 RX_PSC_RDY__RX_PSC_CAL_j Register (Offset = 800Ch + formula) [reset = 10Fh]

RX_PSC_RDY__RX_PSC_CAL_j is shown in [Figure 12-196](#) and described in [Table 12-589](#).

Return to [Summary Table](#).

Receiver calibration power state definition register

Offset = 800Ch + (j * 400h); where j = 0h to 3h

**Table 12-588. RX_PSC_RDY__RX_PSC_CAL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 800Ch + formula

Figure 12-196. RX_PSC_RDY__RX_PSC_CAL_j Register

31	30	29	28	27	26	25	24
RX_PSC_RDY_15_13			RX_PSC_RDY_12	RX_PSC_RDY_11	RX_PSC_RDY_10	RX_PSC_RDY_9	RX_PSC_RDY_8
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RX_PSC_RDY_7_5			RX_PSC_RDY_4	RX_PSC_RDY_3	RX_PSC_RDY_2	RX_PSC_RDY_1	RX_PSC_RDY_0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_PSC_CAL_15_13			RX_PSC_CAL_12	RX_PSC_CAL_11	RX_PSC_CAL_10	RX_PSC_CAL_9	RX_PSC_CAL_8
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RX_PSC_CAL_7_5			RX_PSC_CAL_4	RX_PSC_CAL_3	RX_PSC_CAL_2	RX_PSC_CAL_1	RX_PSC_CAL_0
R/W-0h			R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-589. RX_PSC_RDY__RX_PSC_CAL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RX_PSC_RDY_15_13	R	0h	Reserved
28	RX_PSC_RDY_12	R/W	0h	RX signal detect enable extend control
27	RX_PSC_RDY_11	R/W	0h	RX signal detect filter enable
26	RX_PSC_RDY_10	R/W	0h	RX LFPS detect filter enable
25	RX_PSC_RDY_9	R/W	0h	Reserved - spare
24	RX_PSC_RDY_8	R/W	0h	RX signal detect enable
23-21	RX_PSC_RDY_7_5	R/W	0h	Reserved - spare
20	RX_PSC_RDY_4	R/W	0h	RX equalizer engine enable
19	RX_PSC_RDY_3	R/W	0h	RX DFE equalization enable.
18	RX_PSC_RDY_2	R/W	0h	RX PI enable
17	RX_PSC_RDY_1	R/W	0h	RX e path enable (calibration and eye surf only)
16	RX_PSC_RDY_0	R/W	0h	RX enable
15-13	RX_PSC_CAL_15_13	R	0h	Reserved
12	RX_PSC_CAL_12	R/W	0h	RX signal detect enable extend control

Table 12-589. RX_PSC_RDY__RX_PSC_CAL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_PSC_CAL_11	R/W	0h	RX signal detect filter enable
10	RX_PSC_CAL_10	R/W	0h	RX LFPS detect filter enable
9	RX_PSC_CAL_9	R/W	0h	Reserved - spare
8	RX_PSC_CAL_8	R/W	1h	RX signal detect enable
7-5	RX_PSC_CAL_7_5	R/W	0h	Reserved - spare
4	RX_PSC_CAL_4	R/W	0h	RX equalizer engine enable
3	RX_PSC_CAL_3	R/W	1h	RX DFE equalization enable.
2	RX_PSC_CAL_2	R/W	1h	RX PI enable
1	RX_PSC_CAL_1	R/W	1h	RX e path enable (calibration and eye surf only)
0	RX_PSC_CAL_0	R/W	1h	RX enable

Table 12-590. Register Call Summary for RX_PSC_RDY__RX_PSC_CAL_j

10-G SerDes Registers

- [RX_PSC_RDY__RX_PSC_CAL_j Register \(Offset = 800Ch + formula\) \[reset = 10Fh\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.197 RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j Register (Offset = 8080h + formula) [reset = 0h]

RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j is shown in Figure 12-197 and described in Table 12-592.

Return to [Summary Table](#).

Signal detect calibration 0 control register

Offset = 8080h + (j * 400h); where j = 0h to 3h

Table 12-591.
RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8080h + formula

Figure 12-197. RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j Register

31	30	29	28	27	26	25	24
RX_SDCAL0_OVRD_15	RX_SDCAL0_OVRD_14	RX_SDCAL0_OVRD_13_5					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
RX_SDCAL0_OVRD_13_5			RX_SDCAL0_OVRD_4_0				
R-0h			R/W-0h				
15	14	13	12	11	10	9	8
RX_SDCAL0_CTRL_15	RX_SDCAL0_CTRL_14	RX_SDCAL0_CTRL_13	RX_SDCAL0_CTRL_12	RX_SDCAL0_CTRL_11_5			
R/W-0h	R-0h	R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
RX_SDCAL0_CTRL_11_5			RX_SDCAL0_CTRL_4_0				
R-0h			R-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-592. RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SDCAL0_OVRD_15	R/W	0h	Calibration code override enable: Activation (1'b1) of this register bit allows the codes determined during the automatic calibration process to be overridden. The override value is specified using the calibration code override value field of this register.
30	RX_SDCAL0_OVRD_14	R/W	0h	Analog calibration enable override: Activation (1'b1) of this register bit will force the analog calibration circuits to be enabled by activating the rxda_sd_cal_0_en enable and the rxda_sd_cal_0_clk clock.
29-21	RX_SDCAL0_OVRD_13_5	R	0h	Reserved
20-16	RX_SDCAL0_OVRD_4_0	R/W	0h	Calibration code override value: These bits are used to override the calibration code determined during the automatic calibration process. The code written to these bits is valid when the calibration code override enable bit in this register is active. The codes in this field correspond to those described in the calibration code field in the Signal detect calibration 0 control register on page 222.

Table 12-592. RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RX_SDCAL0_CTRL_15	R/W	0h	<p>Start calibration: Activating (1'b1) this bit will start the calibration process.</p> <p>This signal must remain active until the calibration process is complete.</p> <p>To start another calibration process, this register must first be set inactive (1'b0) until the bandbap calibration process done bit in this register is cleared.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the power state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	RX_SDCAL0_CTRL_14	R	0h	<p>Calibration process done: This bit will be set to 1'b1 when the calibration process is complete.</p> <p>It will be cleared by cmn_reset_n, or by the deactivation of the start calibration bit in this register after calibration is complete.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p> <p>Note: Three cmn_ref_clk cycles are required after the start of the calibration process to clear this signal.</p>
13	RX_SDCAL0_CTRL_13	R	0h	<p>No analog calibration response : This signal indicates that the calibration function has gone through the entire calibration process, reached the final calibration value, and the analog has not responded indicating that a valid calibration value has been reached.</p> <p>Note: Due to the nature of the calibration process, it is not possible to determine if the analog responded or not for the lowest code of 4'b1001.</p> <p>The reason for this is, when sequencing to lower codes, the calibration function is looking for the analog response to transition from 1'b1 to 1'b0.</p> <p>If the lowest calibration code is the correct code, the analog will respond with 1'b1, and the algorithm can't sequence to a lower code to look for the transition from 1'b1 to 1'b0.</p> <p>Similarly, if the analog is not responding, it is not possible to sequence to a lower code to detect this.</p> <p>Therefore, even when the calibration function selects this calibration code as valid, this bit will be set.</p>
12	RX_SDCAL0_CTRL_12	R	0h	<p>Current analog comparator response: This is the current state of the analog comparator response signal (rxda_sd_cal_0_comp).</p> <p>This signal is not synchronized, and is provided for diagnostic purposes only.</p>
11-5	RX_SDCAL0_CTRL_11_5	R	0h	Reserved

Table 12-592. RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	RX_SDCAL0_CTRL_4_0	R	0h	<p>Calibration code: This is the calibration code that was determined by the calibration process.</p> <p>The following indicates how this encoding maps to the rxda_sd_cal_0_up and rxda_sd_cal_0_code signals going to the analog function.</p> <p>The five bit value on the left is the value of this field.</p> <p>The one bit value on the right corresponds to the value of rxda_sd_cal_0_up.</p> <p>The four bit field corresponds to the value of rxda_sd_cal_0_code.</p> <p>5'b 01111 : 1'b1, 4'b1111</p> <p>5'b 01110 : 1'b1, 4'b1110</p> <p>...</p> <p>5'b 00010 : 1'b1, 4'b0010</p> <p>5'b 00001 : 1'b1, 4'b0001</p> <p>5'b 00000 : 1'b1, 4'b0000</p> <p>5'b 11111 : 1'b0, 4'b0001</p> <p>5'b 11110 : 1'b0, 4'b0010</p> <p>...</p> <p>5'b 10010 : 1'b0, 4'b1110</p> <p>5'b 10001 : 1'b0, 4'b1111</p>

Table 12-593. Register Call Summary for RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_SDCAL0_OVRD__RX_SDCAL0_CTRL_j Register \(Offset = 8080h + formula\) \[reset = 0h\]: \[0\]](#)

12.198 RX_SDCAL0_TUNE__RX_SDCAL0_START_j Register (Offset = 8084h + formula) [reset = 0h]

RX_SDCAL0_TUNE__RX_SDCAL0_START_j is shown in Figure 12-198 and described in Table 12-595.

Return to [Summary Table](#).

Signal detect calibration 0 start register

Offset = 8084h + (j * 400h); where j = 0h to 3h

Table 12-594.
RX_SDCAL0_TUNE__RX_SDCAL0_START_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8084h + formula

Figure 12-198. RX_SDCAL0_TUNE__RX_SDCAL0_START_j Register

31	30	29	28	27	26	25	24
RX_SDCAL0_TUNE_15_5							
R-0h							
23	22	21	20	19	18	17	16
RX_SDCAL0_TUNE_15_5				RX_SDCAL0_TUNE_4_0			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
RX_SDCAL0_S TART_15	RX_SDCAL0_START_14_5						
R/W-0h				R-0h			
7	6	5	4	3	2	1	0
RX_SDCAL0_START_14_5				RX_SDCAL0_START_4_0			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-595. RX_SDCAL0_TUNE__RX_SDCAL0_START_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RX_SDCAL0_TUNE_15_5	R	0h	Reserved
20-16	RX_SDCAL0_TUNE_4_0	R/W	0h	Calibration tune value: The value of this field is added to the automatically calibrated code, or the override code if override is enabled. Note that this value is a twos complement value, so the calibrated code can be increased or decreased.
15	RX_SDCAL0_START_15	R/W	0h	Calibration direction: This controls the direction that the automatic calibration process steps the calibration codes in. 1'b 0 : From 5'b10001 to 5'b01111. 1'b 1 : From 5'b01111 to 5'b00000.
14-5	RX_SDCAL0_START_14_5	R	0h	Reserved
4-0	RX_SDCAL0_START_4_0	R/W	0h	Start calibration code: This is the calibration code that the calibration process starts with when automatic calibration is run. The codes in this field correspond to those described in the calibration code field in the Signal detect calibration 0 control register on page 222.

Table 12-596. Register Call Summary for RX_SDCAL0_TUNE__RX_SDCAL0_START_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_SDCAL0_TUNE__RX_SDCAL0_START_j Register \(Offset = 8084h + formula\) \[reset = 0h\]: \[0\]](#)

12.199 RX_SDCAL0_ITER_TMR__RX_SDCAL0_INIT_TMR_j Register (Offset = 8088h + formula) [reset = 007D0019h]

RX_SDCAL0_ITER_TMR__RX_SDCAL0_INIT_TMR_j is shown in Figure 12-199 and described in Table 12-598.

Return to [Summary Table](#).

Signal detect calibration 0 initialization timer register

Offset = 8088h + (j * 400h); where j = 0h to 3h

Table 12-597. RX_SDCAL0_ITER_TMR__RX_SDCAL0_INIT_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 8088h + formula

Figure 12-199. RX_SDCAL0_ITER_TMR__RX_SDCAL0_INIT_TMR_j Register

31	30	29	28	27	26	25	24
RX_SDCAL0_ITER_TMR_15_9							RX_SDCAL0_I TER_TMR_8_0
R-0h							R/W-7Dh
23	22	21	20	19	18	17	16
RX_SDCAL0_ITER_TMR_8_0							
R/W-7Dh							
15	14	13	12	11	10	9	8
RX_SDCAL0_INIT_TMR_15_9							RX_SDCAL0_I NIT_TMR_8_0
R-0h							R/W-19h
7	6	5	4	3	2	1	0
RX_SDCAL0_INIT_TMR_8_0							
R/W-19h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-598. RX_SDCAL0_ITER_TMR__RX_SDCAL0_INIT_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RX_SDCAL0_ITER_TMR_15_9	R	0h	Reserved
24-16	RX_SDCAL0_ITER_TMR_8_0	R/W	7Dh	Iteration wait timer value: This is the number of cmn_ref_clk clocks to wait between when a value is placed on the calibration code signals going to the analog, and when the comparator value coming from the analog circuits can be checked. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 5 uSec. Note that this should never be set to a value of less than 3.
15-9	RX_SDCAL0_INIT_TMR_15_9	R	0h	Reserved
8-0	RX_SDCAL0_INIT_TMR_8_0	R/W	19h	Initialization wait timer value: This is the number of cmn_ref_clk clocks to wait between when the analog calibration circuits are enabled, and when the first values are placed on the calibration code signals going to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 1 uSec. Note that this should never be set to a value of less than 1.

Table 12-599. Register Call Summary for RX_SDCAL0_ITER_TMR__RX_SDCAL0_INIT_TMR_j

<div> 10-G SerDes Registers <ul style="list-style-type: none"> RX_SDCAL0_ITER_TMR__RX_SDCAL0_INIT_TMR_j Register (Offset = 8088h + formula) [reset = 007D0019h]: [0] 10-G SerDes Registers: [0] </div>
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12.200 RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j Register (Offset = 8090h + formula) [reset = 0h]

RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j is shown in Figure 12-200 and described in Table 12-601.

Return to [Summary Table](#).

Signal detect calibration 1 control register

Offset = 8090h + (j * 400h); where j = 0h to 3h

Table 12-600.
RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8090h + formula

Figure 12-200. RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j Register

31	30	29	28	27	26	25	24
RX_SDCAL1_OVRD_15	RX_SDCAL1_OVRD_14	RX_SDCAL1_OVRD_13_5					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
RX_SDCAL1_OVRD_13_5			RX_SDCAL1_OVRD_4_0				
R-0h			R/W-0h				
15	14	13	12	11	10	9	8
RX_SDCAL1_CTRL_15	RX_SDCAL1_CTRL_14	RX_SDCAL1_CTRL_13	RX_SDCAL1_CTRL_12	RX_SDCAL1_CTRL_11_5			
R/W-0h	R-0h	R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
RX_SDCAL1_CTRL_11_5			RX_SDCAL1_CTRL_4_0				
R-0h			R-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-601. RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SDCAL1_OVRD_15	R/W	0h	Calibration code override enable: Activation (1'b1) of this register bit allows the calibration code determined during the automatic calibration process to be overridden. The override value is specified using the calibration code override value field of this register.
30	RX_SDCAL1_OVRD_14	R/W	0h	Analog calibration enable override: Activation (1'b1) of this register bit will force the analog calibration circuits to be enabled by activating the rxda_sd_cal_1_en enable and the rxda_sd_cal_1_clk clock.
29-21	RX_SDCAL1_OVRD_13_5	R	0h	Reserved
20-16	RX_SDCAL1_OVRD_4_0	R/W	0h	Calibration code override value: These bits are used to override the calibration code determined during the automatic calibration process. The code written to these bits is valid when the calibration code override enable bit in this register is active. The codes in this field correspond to those described in the calibration code field in the Signal detect calibration 1 control register on page 225.

Table 12-601. RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RX_SDCAL1_CTRL_15	R/W	0h	<p>Start calibration: Activating (1'b1) this bit will start the calibration process.</p> <p>This signal must remain active until the calibration process is complete.</p> <p>To start another calibration process, this register must first be set inactive (1'b0) until the bandbap calibration process done bit in this register is cleared.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally by the power state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	RX_SDCAL1_CTRL_14	R	0h	<p>Calibration process done: This bit will be set to 1'b1 when the calibration process is complete.</p> <p>It will be cleared by cmn_reset_n, or by the deactivation of the start calibration bit in this register after calibration is complete.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p> <p>Note: Three cmn_ref_clk cycles are required after the start of the calibration process to clear this signal.</p>
13	RX_SDCAL1_CTRL_13	R	0h	<p>No analog calibration response : This signal indicates that the calibration function has gone through the entire calibration process, reached the final calibration value, and the analog has not responded indicating that a valid calibration value has been reached.</p> <p>Note: Due to the nature of the calibration process, it is not possible to determine if the analog responded or not for the lowest code of 4'b1001.</p> <p>The reason for this is, when sequencing to lower codes, the calibration function is looking for the analog response to transition from 1'b1 to 1'b0.</p> <p>If the lowest calibration code is the correct code, the analog will respond with 1'b1, and the algorithm can't sequence to a lower code to look for the transition from 1'b1 to 1'b0.</p> <p>Similarly, if the analog is not responding, it is not possible to sequence to a lower code to detect this.</p> <p>Therefore, even when the calibration function selects this calibration code as valid, this bit will be set.</p>
12	RX_SDCAL1_CTRL_12	R	0h	<p>Current analog comparator response: This is the current state of the analog comparator response signal (rxda_sd_cal_0_comp).</p> <p>This signal is not synchronized, and is provided for diagnostic purposes only.</p>
11-5	RX_SDCAL1_CTRL_11_5	R	0h	Reserved

Table 12-601. RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	RX_SDCAL1_CTRL_4_0	R	0h	<p>Calibration code: This is the calibration code that was determined by the calibration process.</p> <p>The following indicates how this encoding maps to the rxda_sd_cal_1_up and rxda_sd_cal_1_code signals going to the analog calibration function.</p> <p>The five bit value on the left is the value of this field.</p> <p>The one bit value on the right corresponds to the value of rxda_sd_cal_1_up.</p> <p>The four bit field corresponds to the value of rxda_sd_cal_1_code.</p> <p>5'b 01111 : 1'b1, 4'b1111</p> <p>5'b 01110 : 1'b1, 4'b1110</p> <p>...</p> <p>5'b 00010 : 1'b1, 4'b0010</p> <p>5'b 00001 : 1'b1, 4'b0001</p> <p>5'b 00000 : 1'b1, 4'b0000</p> <p>5'b 11111 : 1'b0, 4'b0001</p> <p>5'b 11110 : 1'b0, 4'b0010</p> <p>...</p> <p>5'b 10010 : 1'b0, 4'b1110</p> <p>5'b 10001 : 1'b0, 4'b1111</p>

Table 12-602. Register Call Summary for RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j

10-G SerDes Registers

- [RX_SDCAL1_OVRD__RX_SDCAL1_CTRL_j Register \(Offset = 8090h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.201 RX_SDCAL1_TUNE__RX_SDCAL1_START_j Register (Offset = 8094h + formula) [reset = 0h]

RX_SDCAL1_TUNE__RX_SDCAL1_START_j is shown in Figure 12-201 and described in Table 12-604.

Return to [Summary Table](#).

Signal detect calibration 1 start register

Offset = 8094h + (j * 400h); where j = 0h to 3h

Table 12-603.
RX_SDCAL1_TUNE__RX_SDCAL1_START_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8094h + formula

Figure 12-201. RX_SDCAL1_TUNE__RX_SDCAL1_START_j Register

31	30	29	28	27	26	25	24
RX_SDCAL1_TUNE_15_5							
R-0h							
23	22	21	20	19	18	17	16
RX_SDCAL1_TUNE_15_5				RX_SDCAL1_TUNE_4_0			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
RX_SDCAL1_S TART_15	RX_SDCAL1_START_14_5						
R/W-0h				R-0h			
7	6	5	4	3	2	1	0
RX_SDCAL1_START_14_5				RX_SDCAL1_START_4_0			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-604. RX_SDCAL1_TUNE__RX_SDCAL1_START_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RX_SDCAL1_TUNE_15_5	R	0h	Reserved
20-16	RX_SDCAL1_TUNE_4_0	R/W	0h	Calibration tune value: The value of this field is added to the automatically calibrated code, or the override code if override is enabled. Note that this value is a twos complement value, so the calibrated code can be increased or decreased.
15	RX_SDCAL1_START_15	R/W	0h	Calibration direction: This controls the direction that the automatic calibration process steps the calibration codes in. 1'b 0 : From 5'b10001 to 5'b01111. 1'b 1 : From 5'b01111 to 5'b00000.
14-5	RX_SDCAL1_START_14_5	R	0h	Reserved
4-0	RX_SDCAL1_START_4_0	R/W	0h	Start calibration code: This is the calibration code that the calibration process starts with when automatic calibration is run. The codes in this field correspond to those described in the calibration code field in the Signal detect calibration 1 control register on page 225.

Table 12-605. Register Call Summary for RX_SDCAL1_TUNE__RX_SDCAL1_START_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_SDCAL1_TUNE__RX_SDCAL1_START_j Register \(Offset = 8094h + formula\) \[reset = 0h\]: \[0\]](#)

12.202 RX_SDCAL1_ITER_TMR__RX_SDCAL1_INIT_TMR_j Register (Offset = 8098h + formula) [reset = 007D0019h]

RX_SDCAL1_ITER_TMR__RX_SDCAL1_INIT_TMR_j is shown in Figure 12-202 and described in Table 12-607.

Return to [Summary Table](#).

Signal detect calibration 1 initialization timer register

Offset = 8098h + (j * 400h); where j = 0h to 3h

Table 12-606. RX_SDCAL1_ITER_TMR__RX_SDCAL1_INIT_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 8098h + formula

Figure 12-202. RX_SDCAL1_ITER_TMR__RX_SDCAL1_INIT_TMR_j Register

31	30	29	28	27	26	25	24
RX_SDCAL1_ITER_TMR_15_9							RX_SDCAL1_I TER_TMR_8_0
R-0h							R/W-7Dh
23	22	21	20	19	18	17	16
RX_SDCAL1_ITER_TMR_8_0							
R/W-7Dh							
15	14	13	12	11	10	9	8
RX_SDCAL1_INIT_TMR_15_9							RX_SDCAL1_I NIT_TMR_8_0
R-0h							R/W-19h
7	6	5	4	3	2	1	0
RX_SDCAL1_INIT_TMR_8_0							
R/W-19h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-607. RX_SDCAL1_ITER_TMR__RX_SDCAL1_INIT_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RX_SDCAL1_ITER_TMR_15_9	R	0h	Reserved
24-16	RX_SDCAL1_ITER_TMR_8_0	R/W	7Dh	Iteration wait timer value: This is the number of cmn_ref_clk clocks to wait between when a value is placed on the calibration code signals going to the analog, and when the comparator value coming from the analog circuits can be checked. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 5 uSec. Note that this should never be set to a value of less than 3.
15-9	RX_SDCAL1_INIT_TMR_15_9	R	0h	Reserved
8-0	RX_SDCAL1_INIT_TMR_8_0	R/W	19h	Initialization wait timer value: This is the number of cmn_ref_clk clocks to wait between when the analog calibration circuits are enabled, and when the first values are placed on the calibration code signals going to the analog. Note that this results in the minimum number of cmn_ref_clk clocks required to wait 1 uSec. Note that this should never be set to a value of less than 1.

Table 12-608. Register Call Summary for RX_SDCAL1_ITER_TMR__RX_SDCAL1_INIT_TMR_j

10-G SerDes Registers

- [RX_SDCAL1_ITER_TMR__RX_SDCAL1_INIT_TMR_j](#) Register (Offset = 8098h + formula) [reset = 007D0019h]: [0]
- 10-G SerDes Registers: [0]

12.203 RX_SAMP_DAC_CTRL_j Register (Offset = 80B0h + formula) [reset = X]

RX_SAMP_DAC_CTRL_j is shown in Figure 12-203 and described in Table 12-610.

Return to [Summary Table](#).

Sampler error DAC control register

Offset = 80B0h + (j * 400h); where j = 0h to 3h

Table 12-609. RX_SAMP_DAC_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 80B0h + formula

Figure 12-203. RX_SAMP_DAC_CTRL_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_SAMP_DAC_CTRL_15_6							
R-0h							
7	6	5	4	3	2	1	0
RX_SAMP_DAC_CTRL_15_6				RX_SAMP_DAC_CTRL_5_0			
R-0h				R/W-14h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-610. RX_SAMP_DAC_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-6	RX_SAMP_DAC_CTRL_15_6	R	0h	Reserved
5-0	RX_SAMP_DAC_CTRL_5_0	R/W	14h	<p>Sampler error DAC value: Specifies the input value to the sampler error DAC.</p> <p>This value is a twos complement binary number, with the range specified below.</p> <p>6'b 011111: Maximum.</p> <p>6'b 000000: Center point of the data eye.</p> <p>6'b 100001: Minimum.</p> <p>Note : Even though this register can be set to as low as 6'b100001, it should never be set below the value of 6'b000000 when the VGA gain target adjustment algorithm is enabled in the REE. Doing so can result in an underflow condition.</p>

Table 12-611. Register Call Summary for RX_SAMP_DAC_CTRL_j

10-G SerDes Registers

- [RX_SAMP_DAC_CTRL_j Register \(Offset = 80B0h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.204 RX_SLC_IPP_STAT__RX_SLC_CTRL_j Register (Offset = 80C0h + formula) [reset = 1h]

RX_SLC_IPP_STAT__RX_SLC_CTRL_j is shown in Figure 12-204 and described in Table 12-613.

Return to [Summary Table](#).

RX sampler latch calibration control register

Offset = 80C0h + (j * 400h); where j = 0h to 3h

**Table 12-612. RX_SLC_IPP_STAT__RX_SLC_CTRL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 80C0h + formula

Figure 12-204. RX_SLC_IPP_STAT__RX_SLC_CTRL_j Register

31	30	29	28	27	26	25	24
RX_SLC_IPP_STAT_15	RX_SLC_IPP_STAT_14_8						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RX_SLC_IPP_STAT_7	RX_SLC_IPP_STAT_6_0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
RX_SLC_CTRL_15	RX_SLC_CTRL_14	RX_SLC_CTRL_13_2					
R/W-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
RX_SLC_CTRL_13_2						RX_SLC_CTRL_1_0	
R-0h						R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-613. RX_SLC_IPP_STAT__RX_SLC_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SLC_IPP_STAT_15	R	0h	Reserved
30-24	RX_SLC_IPP_STAT_14_8	R	0h	I even latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the I even latch in the analog sampler component.
23	RX_SLC_IPP_STAT_7	R	0h	Reserved
22-16	RX_SLC_IPP_STAT_6_0	R	0h	I odd latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the I odd latch in the analog sampler component.

Table 12-613. RX_SLC_IPP_STAT__RX_SLC_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RX_SLC_CTRL_15	R/W	0h	<p>Start RX sampler latch calibration: Activating (1'b1) this bit will start the RX sampler latch calibration process.</p> <p>This bit should remain active until the RX sampler latch calibration process is complete.</p> <p>To start another RX sampler latch calibration process, this bit must first be inactive (1'b0) until the RX sampler latch calibration done bit goes inactive.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>This calibration process is automatically activated internally, by the power state machine.</p> <p>When using this bit, the user must wait until after the internally activated process completes.</p>
14	RX_SLC_CTRL_14	R	0h	<p>RX sampler latch calibration process done: This bit will be set to 1'b1 when the RX sampler latch calibration process is complete.</p> <p>It will be cleared by cmn_reset_n, or by clearing the start RX sampler latch process bit.</p> <p>Note: This bit is intended to be for diagnostics purposes only.</p> <p>Note: This bit is not likely to be observed as being set after internal automatic calibration is complete, because the internally generated run signal will be driven inactive immediately after the done signal is activated, and therefore the internal done signal will be cleared.</p>
13-2	RX_SLC_CTRL_13_2	R	0h	Reserved
1-0	RX_SLC_CTRL_1_0	R/W	1h	<p>RX sampler latch calibration scaler: This field specifies the scaler value used for the input data accumulator.</p> <p>The following is the encoding used for this signal.</p>

Table 12-614. Register Call Summary for RX_SLC_IPP_STAT__RX_SLC_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_SLC_IPP_STAT__RX_SLC_CTRL_j Register \(Offset = 80C0h + formula\) \[reset = 1h\]: \[0\]](#)

12.205 RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j Register (Offset = 80C4h + formula) [reset = 0h]

RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j is shown in [Figure 12-205](#) and described in [Table 12-616](#).

Return to [Summary Table](#).

RX sampler latch calibration I predictive positive override register

Offset = 80C4h + (j * 400h); where j = 0h to 3h

Table 12-615.
RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j
Instances

Instance	Physical Address
SERDES_10G0	0505 80C4h + formula

Figure 12-205. RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j Register

31	30	29	28	27	26	25	24
RX_SLC_IPM_STAT_15	RX_SLC_IPM_STAT_14_8						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RX_SLC_IPM_STAT_7	RX_SLC_IPM_STAT_6_0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
RX_SLC_IPP_OVRD_15	RX_SLC_IPP_OVRD_14_8						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RX_SLC_IPP_OVRD_7	RX_SLC_IPP_OVRD_6_0						
R/W-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-616. RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SLC_IPM_STAT_15	R	0h	Reserved
30-24	RX_SLC_IPM_STAT_14_8	R	0h	I even latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the I even latch in the analog sampler component.
23	RX_SLC_IPM_STAT_7	R	0h	Reserved
22-16	RX_SLC_IPM_STAT_6_0	R	0h	I odd latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the I odd latch in the analog sampler component.
15	RX_SLC_IPP_OVRD_15	R/W	0h	I even latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the I even latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the I even sampler latch.

Table 12-616. RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-8	RX_SLC_IPP_OVRD_14_8	R/W	0h	I even latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the I even sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.
7	RX_SLC_IPP_OVRD_7	R/W	0h	I odd latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the I odd latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the I odd sampler latch.
6-0	RX_SLC_IPP_OVRD_6_0	R/W	0h	I odd latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the I odd sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.

Table 12-617. Register Call Summary for RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j

10-G SerDes Registers

- [RX_SLC_IPM_STAT__RX_SLC_IPP_OVRD_j Register \(Offset = 80C4h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.206 RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j Register (Offset = 80C8h + formula) [reset = 0h]

RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j is shown in [Figure 12-206](#) and described in [Table 12-619](#).

Return to [Summary Table](#).

RX sampler latch calibration I predictive negative override register

Offset = 80C8h + (j * 400h); where j = 0h to 3h

Table 12-618.
RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j
Instances

Instance	Physical Address
SERDES_10G0	0505 80C8h + formula

Figure 12-206. RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j Register

31	30	29	28	27	26	25	24
RX_SLC_QPP_STAT_15	RX_SLC_QPP_STAT_14_8						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RX_SLC_QPP_STAT_7	RX_SLC_QPP_STAT_6_0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
RX_SLC_IPM_OVRD_15	RX_SLC_IPM_OVRD_14_8						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RX_SLC_IPM_OVRD_7	RX_SLC_IPM_OVRD_6_0						
R/W-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-619. RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SLC_QPP_STAT_15	R	0h	Reserved
30-24	RX_SLC_QPP_STAT_14_8	R	0h	Q even latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the Q even latch in the analog sampler component.
23	RX_SLC_QPP_STAT_7	R	0h	Reserved
22-16	RX_SLC_QPP_STAT_6_0	R	0h	Q odd latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the Q odd latch in the analog sampler component.
15	RX_SLC_IPM_OVRD_15	R/W	0h	I eve latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the I even latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the I even sampler latch.

Table 12-619. RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-8	RX_SLC_IPM_OVRD_14_8	R/W	0h	I even latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the I even sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.
7	RX_SLC_IPM_OVRD_7	R/W	0h	I odd latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the I odd latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the I odd sampler latch.
6-0	RX_SLC_IPM_OVRD_6_0	R/W	0h	I odd latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the I odd sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.

Table 12-620. Register Call Summary for RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_SLC_QPP_STAT__RX_SLC_IPM_OVRD_j Register \(Offset = 80C8h + formula\) \[reset = 0h\]: \[0\]](#)

12.207 RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j Register (Offset = 80CCh + formula) [reset = 0h]

[RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j](#) is shown in [Figure 12-207](#) and described in [Table 12-622](#).

Return to [Summary Table](#).

RX sampler latch calibration Q predictive positive override register

Offset = 80CCh + (j * 400h); where j = 0h to 3h

Table 12-621.
RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j
Instances

Instance	Physical Address
SERDES_10G0	0505 80CCh + formula

Figure 12-207. RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j Register

31	30	29	28	27	26	25	24
RX_SLC_QPM_STAT_15	RX_SLC_QPM_STAT_14_8						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RX_SLC_QPM_STAT_7	RX_SLC_QPM_STAT_6_0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
RX_SLC_QPP_OVRD_15	RX_SLC_QPP_OVRD_14_8						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RX_SLC_QPP_OVRD_7	RX_SLC_QPP_OVRD_6_0						
R/W-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-622. RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SLC_QPM_STAT_15	R	0h	Reserved
30-24	RX_SLC_QPM_STAT_14_8	R	0h	Q even latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the Q even latch in the analog sampler component.
23	RX_SLC_QPM_STAT_7	R	0h	Reserved
22-16	RX_SLC_QPM_STAT_6_0	R	0h	Q odd latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the Q odd latch in the analog sampler component.
15	RX_SLC_QPP_OVRD_15	R/W	0h	Q even latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the Q even latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the Q even sampler latch.

Table 12-622. RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-8	RX_SLC_QPP_OVRD_14_8	R/W	0h	Q even latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the Q even sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.
7	RX_SLC_QPP_OVRD_7	R/W	0h	Q odd latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the Q odd latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the Q odd sampler latch.
6-0	RX_SLC_QPP_OVRD_6_0	R/W	0h	Q odd latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the Q odd sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.

Table 12-623. Register Call Summary for RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j

10-G SerDes Registers

- [RX_SLC_QPM_STAT__RX_SLC_QPP_OVRD_j Register \(Offset = 80CCh + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.208 RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j Register (Offset = 80D0h + formula) [reset = 0h]

[RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j](#) is shown in [Figure 12-208](#) and described in [Table 12-625](#).

Return to [Summary Table](#).

RX sampler latch calibration Q predictive negative override register

Offset = 80D0h + (j * 400h); where j = 0h to 3h

Table 12-624.
RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j
Instances

Instance	Physical Address
SERDES_10G0	0505 80D0h + formula

Figure 12-208. RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j Register

31	30	29	28	27	26	25	24
RX_SLC_EPP_STAT_15	RX_SLC_EPP_STAT_14_8						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RX_SLC_EPP_STAT_7	RX_SLC_EPP_STAT_6_0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
RX_SLC_QPM_OVRD_15	RX_SLC_QPM_OVRD_14_8						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RX_SLC_QPM_OVRD_7	RX_SLC_QPM_OVRD_6_0						
R/W-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-625. RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SLC_EPP_STAT_15	R	0h	Reserved
30-24	RX_SLC_EPP_STAT_14_8	R	0h	e even latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the e even latch in the analog sampler component.
23	RX_SLC_EPP_STAT_7	R	0h	Reserved
22-16	RX_SLC_EPP_STAT_6_0	R	0h	e odd latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the e odd latch in the analog sampler component.
15	RX_SLC_QPM_OVRD_15	R/W	0h	Q even latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the Q even latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the Q even sampler latch.

Table 12-625. RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-8	RX_SLC_QPM_OVRD_14_8	R/W	0h	Q even latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the Q even sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.
7	RX_SLC_QPM_OVRD_7	R/W	0h	Q odd latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the Q odd latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the Q odd sampler latch.
6-0	RX_SLC_QPM_OVRD_6_0	R/W	0h	Q odd latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the Q odd sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.

Table 12-626. Register Call Summary for RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j

10-G SerDes Registers

- [RX_SLC_EPP_STAT__RX_SLC_QPM_OVRD_j Register \(Offset = 80D0h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.209 RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j Register (Offset = 80D4h + formula) [reset = 0h]

RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j is shown in Figure 12-209 and described in Table 12-628.

Return to [Summary Table](#).

RX sampler latch calibration e predictive positive override register

Offset = 80D4h + (j * 400h); where j = 0h to 3h

Table 12-627.
RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j
Instances

Instance	Physical Address
SERDES_10G0	0505 80D4h + formula

Figure 12-209. RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j Register

31	30	29	28	27	26	25	24
RX_SLC_EPM_STAT_15	RX_SLC_EPM_STAT_14_8						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RX_SLC_EPM_STAT_7	RX_SLC_EPM_STAT_6_0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
RX_SLC_EPP_OVRD_15	RX_SLC_EPP_OVRD_14_8						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
RX_SLC_EPP_OVRD_7	RX_SLC_EPP_OVRD_6_0						
R/W-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-628. RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SLC_EPM_STAT_15	R	0h	Reserved
30-24	RX_SLC_EPM_STAT_14_8	R	0h	e even latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the e even latch in the analog sampler component.
23	RX_SLC_EPM_STAT_7	R	0h	Reserved
22-16	RX_SLC_EPM_STAT_6_0	R	0h	e odd latch receiver sampler calibration DAC value: This field contains the current value that the RX sampler latch calibration module has calculated to drive to the DAC that controls the offset for the e odd latch in the analog sampler component.
15	RX_SLC_EPP_OVRD_15	R/W	0h	e even latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the e even latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the e even sampler latch.

Table 12-628. RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-8	RX_SLC_EPP_OVRD_14_8	R/W	0h	e even latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the e even sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.
7	RX_SLC_EPP_OVRD_7	R/W	0h	e odd latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the e odd latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the e odd sampler latch.
6-0	RX_SLC_EPP_OVRD_6_0	R/W	0h	e odd latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the e odd sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.

Table 12-629. Register Call Summary for RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j

10-G SerDes Registers

- [RX_SLC_EPM_STAT__RX_SLC_EPP_OVRD_j Register \(Offset = 80D4h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.210 RX_SLC_INIT_TMR_RX_SLC_EPM_OVRD_j Register (Offset = 80D8h + formula) [reset = 00100000h]

[RX_SLC_INIT_TMR_RX_SLC_EPM_OVRD_j](#) is shown in [Figure 12-210](#) and described in [Table 12-631](#).

Return to [Summary Table](#).

RX sampler latch calibration e predictive negative override register

Offset = 80D8h + (j * 400h); where j = 0h to 3h

Table 12-630.
RX_SLC_INIT_TMR_RX_SLC_EPM_OVRD_j
Instances

Instance	Physical Address
SERDES_10G0	0505 80D8h + formula

Figure 12-210. RX_SLC_INIT_TMR_RX_SLC_EPM_OVRD_j Register

31	30	29	28	27	26	25	24
RX_SLC_INIT_TMR_15_0							
R/W-10h							
23	22	21	20	19	18	17	16
RX_SLC_INIT_TMR_15_0							
R/W-10h							
15	14	13	12	11	10	9	8
RX_SLC_EPM_OVRD_15	RX_SLC_EPM_OVRD_14_8						
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RX_SLC_EPM_OVRD_7	RX_SLC_EPM_OVRD_6_0						
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-631. RX_SLC_INIT_TMR_RX_SLC_EPM_OVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_SLC_INIT_TMR_15_0	R/W	10h	RX sampler latch calibration initialization timer value : This is the value that will be used for the RX sampler latch calibration initialization timer, which controls the time the rxda_sampler_latch_cal_en is held active prior to the individual calibration processes being kicked off. Note that this register should not be set to 16'h0000.
15	RX_SLC_EPM_OVRD_15	R/W	0h	e even latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the e even latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the e even sampler latch.
14-8	RX_SLC_EPM_OVRD_14_8	R/W	0h	e even latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the e even sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.

Table 12-631. RX_SLC_INIT_TMR__RX_SLC_EPM_OVRD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RX_SLC_EPM_OVRD_7	R/W	0h	e odd latch receiver sampler calibration DAC override enable: When this bit is active (1'b1), the value in the e odd latch receiver sampler calibration DAC override value field of this register will override the calibrated value for the e odd sampler latch.
6-0	RX_SLC_EPM_OVRD_6_0	R/W	0h	e odd latch receiver sampler calibration DAC override value: This field contains the value that can be used to override the calibrated value for the e odd sampler latch. Note that the value of this field is a signed magnitude number with a range of 5'b11111 (min) to 5'b01111 (max). A value of 5'b10000 (-0) is not valid.

Table 12-632. Register Call Summary for RX_SLC_INIT_TMR__RX_SLC_EPM_OVRD_j

10-G SerDes Registers

- [RX_SLC_INIT_TMR__RX_SLC_EPM_OVRD_j Register \(Offset = 80D8h + formula\) \[reset = 00100000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.211 RX_SLC_DIAG_CTRL__RX_SLC_RUN_TMR_j Register (Offset = 80DCh + formula) [reset = A000h]

RX_SLC_DIAG_CTRL__RX_SLC_RUN_TMR_j is shown in [Figure 12-211](#) and described in [Table 12-634](#).

Return to [Summary Table](#).

RX sampler latch calibration run timer value register

Offset = 80DCh + (j * 400h); where j = 0h to 3h

Table 12-633.
RX_SLC_DIAG_CTRL__RX_SLC_RUN_TMR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 80DCh + formula

Figure 12-211. RX_SLC_DIAG_CTRL__RX_SLC_RUN_TMR_j Register

31	30	29	28	27	26	25	24
RX_SLC_DIAG_CTRL_15	RX_SLC_DIAG_CTRL_14_7						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RX_SLC_DIAG_CTRL_14_7	RX_SLC_DIAG_CTRL_6	RX_SLC_DIAG_CTRL_5	RX_SLC_DIAG_CTRL_4	RX_SLC_DIAG_CTRL_3_0			
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			
15	14	13	12	11	10	9	8
RX_SLC_RUN_TMR_15_0							
R/W-A000h							
7	6	5	4	3	2	1	0
RX_SLC_RUN_TMR_15_0							
R/W-A000h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-634. RX_SLC_DIAG_CTRL__RX_SLC_RUN_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_SLC_DIAG_CTRL_15	R/W	0h	Diagnostic control enable : This bit enables the selected RX sampler latch calibration data sub module for diagnostic purposes. Note that the diagnostic control override select field must be set to select the desired RX sampler latch calibration data sub module when this bit is set. This bit MUST also be cleared before changing the value of the diagnostic control override select field. Note that when these diagnostic features are used, the user must disable the respective automatic calibration functions in the RX sampler latch calibration disable register on page 238. Due to the way this is implemented, if a given i sampler latch calibration function is being controlled by the diagnostic features here, all of the i sampler calibration functions must be disabled in the RX sampler latch calibration disable register on page 238. The same is required for both the e and q sampler latch calibration functions.
30-23	RX_SLC_DIAG_CTRL_14_7	R	0h	Reserved

Table 12-634. RX_SLC_DIAG_CTRL_RX_SLC_RUN_TMR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	RX_SLC_DIAG_CTRL_6	R/W	0h	<p>Voter override neg : When enabled using the voter override enable bit in this register, writing a 1'b1 in this register bit will force the voter in the selected RX sampler latch calibration data sub module to activate the voter neg signal for a single clock cycle.</p> <p>Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit.</p> <p>Note : It is not valid to activate both the voter override neg and voter override pos at the same time.</p>
21	RX_SLC_DIAG_CTRL_5	R/W	0h	<p>Voter override pos : When enabled using the voter override enable bit in this register, writing a 1'b1 in this register bit will force the voter in the selected RX sampler latch calibration data sub module to activate the voter pos signal for a single clock cycle.</p> <p>Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit.</p> <p>Note : It is not valid to activate both the voter override neg and voter override pos at the same time.</p>
20	RX_SLC_DIAG_CTRL_4	R/W	0h	<p>Voter override enable : Setting this bit to a 1'b1 will enable the voter override function in the selected RX sampler latch calibration data sub module.</p> <p>Note : This function is intended to be for diagnostic and verification purposes only.</p> <p>Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.</p>
19-16	RX_SLC_DIAG_CTRL_3_0	R/W	0h	<p>Diagnostic control override select : Selects the RX sampler latch calibration data sub module to enable for diagnostic and verification purposes.</p> <p>This field also selects which sub module's rx_sampler_latch_cal_diag output port will be routed to the top level rx_sampler_latch_cal_diag output port.</p> <p>The following are the values used to select the required RX sampler latch calibration data sub module.</p> <p>4'b 0000 : i odd positive coefficient.</p> <p>4'b 0001 : q odd positive coefficient.</p> <p>4'b 0010 : e odd positive coefficient.</p> <p>4'b 0011 : Reserved.</p> <p>4'b 0100 : i odd negative coefficient.</p> <p>4'b 0101 : q odd negative coefficient.</p> <p>4'b 0110 : e odd negative coefficient.</p> <p>4'b 0111 : Reserved.</p> <p>4'b 1000 : i even positive coefficient.</p> <p>4'b 1001 : q even positive coefficient.</p> <p>4'b 1010 : e even positive coefficient.</p> <p>4'b 1011 : Reserved.</p> <p>4'b 1100 : i even negative coefficient.</p> <p>4'b 1101 : q even negative coefficient.</p> <p>4'b 1110 : e even negative coefficient.</p> <p>4'b 1111 : Reserved.</p>
15-0	RX_SLC_RUN_TMR_15_0	R/W	A000h	<p>RX sampler latch calibration run timer value : This is the value that will be used for the RX sampler latch calibration run timer, which controls the run time for each calibration process.</p> <p>Note that this register should not be set to 16'h0000.</p>

Table 12-635. Register Call Summary for RX_SLC_DIAG_CTRL__RX_SLC_RUN_TMR_j

10-G SerDes Registers

- [RX_SLC_DIAG_CTRL__RX_SLC_RUN_TMR_j](#) Register (Offset = 80DCh + formula) [reset = A000h]: [0]
- 10-G SerDes Registers: [0]

12.212 RX_SLC_DIS_j Register (Offset = 80E0h + formula) [reset = X]

RX_SLC_DIS_j is shown in [Figure 12-212](#) and described in [Table 12-637](#).

Return to [Summary Table](#).

RX sampler latch calibration disable register

Offset = 80E0h + (j * 400h); where j = 0h to 3h

Table 12-636. RX_SLC_DIS_j Instances

Instance	Physical Address
SERDES_10G0	0505 80E0h + formula

Figure 12-212. RX_SLC_DIS_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_SLC_DIS_1 5	RX_SLC_DIS_1 4	RX_SLC_DIS_1 3	RX_SLC_DIS_1 2	RX_SLC_DIS_1 1	RX_SLC_DIS_1 0	RX_SLC_DIS_9	RX_SLC_DIS_8
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_SLC_DIS_7	RX_SLC_DIS_6	RX_SLC_DIS_5	RX_SLC_DIS_4	RX_SLC_DIS_3	RX_SLC_DIS_2	RX_SLC_DIS_1	RX_SLC_DIS_0
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-637. RX_SLC_DIS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RX_SLC_DIS_15	R	0h	Reserved
14	RX_SLC_DIS_14	R/W	0h	e even negative coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the e even negative coefficient RX sampler latch calibration data sub module.
13	RX_SLC_DIS_13	R/W	0h	q even negative coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the q even negative coefficient RX sampler latch calibration data sub module.
12	RX_SLC_DIS_12	R/W	0h	i even negative coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the i even negative coefficient RX sampler latch calibration data sub module.
11	RX_SLC_DIS_11	R	0h	Reserved
10	RX_SLC_DIS_10	R/W	0h	e even positive coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the e even positive coefficient RX sampler latch calibration data sub module.
9	RX_SLC_DIS_9	R/W	0h	q even positive coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the q even positive coefficient RX sampler latch calibration data sub module.

Table 12-637. RX_SLC_DIS_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RX_SLC_DIS_8	R/W	0h	i even positive coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the i even positive coefficient RX sampler latch calibration data sub module.
7	RX_SLC_DIS_7	R	0h	Reserved
6	RX_SLC_DIS_6	R/W	0h	e odd negative coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the e odd negative coefficient RX sampler latch calibration data sub module.
5	RX_SLC_DIS_5	R/W	0h	q odd negative coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the q odd negative coefficient RX sampler latch calibration data sub module.
4	RX_SLC_DIS_4	R/W	0h	i odd negative coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the i odd negative coefficient RX sampler latch calibration data sub module.
3	RX_SLC_DIS_3	R	0h	Reserved
2	RX_SLC_DIS_2	R/W	0h	e odd positive coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the e odd positive coefficient RX sampler latch calibration data sub module.
1	RX_SLC_DIS_1	R/W	0h	q odd positive coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the q odd positive coefficient RX sampler latch calibration data sub module.
0	RX_SLC_DIS_0	R/W	0h	i odd positive coefficient disable : Writing a 1'b1 to this bit will disable auto calibration for the i odd positive coefficient RX sampler latch calibration data sub module.

Table 12-638. Register Call Summary for RX_SLC_DIS_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_SLC_DIS_j Register \(Offset = 80E0h + formula\) \[reset = X\]: \[0\]](#)

12.213 RX_CDRLF_CNFG2__RX_CDRLF_CNFG_j Register (Offset = 8100h + formula) [reset = 0A33018Ch]

RX_CDRLF_CNFG2__RX_CDRLF_CNFG_j is shown in Figure 12-213 and described in Table 12-640.

Return to [Summary Table](#).

CDRLF configuration register

Offset = 8100h + (j * 400h); where j = 0h to 3h

Table 12-639.
RX_CDRLF_CNFG2__RX_CDRLF_CNFG_j Instances

Instance	Physical Address
SERDES_10G0	0505 8100h + formula

Figure 12-213. RX_CDRLF_CNFG2__RX_CDRLF_CNFG_j Register

31	30	29	28	27	26	25	24
RX_CDRLF_C NFG2_15	RX_CDRLF_C NFG2_14	RX_CDRLF_C NFG2_13	RX_CDRLF_C NFG2_12	RX_CDRLF_C NFG2_11	RX_CDRLF_C NFG2_10	RX_CDRLF_C NFG2_9	RX_CDRLF_C NFG2_8
R-0h	R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h
23	22	21	20	19	18	17	16
RX_CDRLF_CNFG2_7_6		RX_CDRLF_CNFG2_5_0					
R-0h		R/W-33h					
15	14	13	12	11	10	9	8
RX_CDRLF_C NFG_15	RX_CDRLF_CNFG_14_12			RX_CDRLF_C NFG_11	RX_CDRLF_CNFG_10_6		
R/W-0h	R/W-0h			R/W-0h	R/W-6h		
7	6	5	4	3	2	1	0
RX_CDRLF_CNFG_10_6		RX_CDRLF_C NFG_5	RX_CDRLF_CNFG_4_0				
R/W-6h		R/W-0h	R/W-Ch				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-640. RX_CDRLF_CNFG2__RX_CDRLF_CNFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_CDRLF_CNFG2_15	R	0h	Reserved
30	RX_CDRLF_CNFG2_14	R/W	0h	CDRLF second order loop integrator max clear enable: This signal enables the function in the CDRLF where the second order loop integrator is cleared when it reaches the maximum value.
29	RX_CDRLF_CNFG2_13	R	0h	CDRLF fast phase lock locked detected: This register bit is the current status of the fphl_locked pin on the CDRLF, and indicates the fast phase lock process is complete.
28	RX_CDRLF_CNFG2_12	R/W	0h	CDRLF fast phase lock diagnostic enable: This register bit can control the fphl_start pin on the CDRLF. for diagnostic purposes. If the CDRLF fast phase lock enabled by signal detect bit in this register is enabled, then either signal detect or this bit will activate the fphl_start pin.
27	RX_CDRLF_CNFG2_11	R/W	1h	CDRLF fast phase lock enabled by signal detect: When active, signal detect will control the fphl_start pin on the CDRLF. This will cause fast phase lock to be enabled whenever the macro detects a transition from electrical idle to high speed data.

Table 12-640. RX_CDRLF_CNFG2_RX_CDRLF_CNFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	RX_CDRLF_CNFG2_10	R/W	0h	CDRLF reset on CDRLF PM Accumulator Max: Activating (1'b1) this bit will force the CDRLF to be reset when the PM accumulator in the CDRLF reaches is maximum absolute value (the largest positive or negative value).
25	RX_CDRLF_CNFG2_9	R/W	1h	CDRLF freeze on electrical idle detect: Activating (1'b1) this bit will force the CDRLF to be freeze in its current state when the receiver signal detect detects an electrical idle. When high speed data is detected, the freeze will be released.
24	RX_CDRLF_CNFG2_8	R/W	0h	CDRLF reset on electrical idle detect: Activating (1'b1) this bit will force the CDRLF to be reset when the receiver signal detect detects an electrical idle. When high speed data is detected, the reset will be released.
23-22	RX_CDRLF_CNFG2_7_6	R	0h	Reserved
21-16	RX_CDRLF_CNFG2_5_0	R/W	33h	CDRLF second order loop integrator threshold : This value is the maximum magnitude the CDRLF second order loop integrator will be allowed to go to. Note that this field must never be set to a value less than 2 (6'b000010).
15	RX_CDRLF_CNFG_15	R/W	0h	CDRLF reset hold: When active (1'b1), the CDRLF will be held in reset beyond the time that it would normally be released by its asynchronous release signals. The CDRLF will be held in reset until this bit is deactivated (1'b0). Note: This signal is intended be for verification purposes only. It should be set to 1'b0 for normal operation.
14-12	RX_CDRLF_CNFG_14_12	R/W	0h	CDRLF diagnostic mode control: This field controls the information driven on the rx_pi_val_ln_{15:0}[7:0] signal, when in diagnostics mode.
11	RX_CDRLF_CNFG_11	R/W	0h	CDRLF second order loop disable: Activating (1'b1) this bit will disable the CDRLF second order loop. Note: This signal is intended be for verification purposes only. It should be set to 1'b0 for normal operation.
10-6	RX_CDRLF_CNFG_10_6	R/W	6h	CDRLF second order loop sigma delta update rate: This is the value that is added to or subtracted from the second order loop accumulator register when the serial data sample clock is detected as being out of phase with the serial data on a given parallel data word cycle. This is part of the CDRLF averaging function.
5	RX_CDRLF_CNFG_5	R/W	0h	CDRLF first order loop disable: Activating (1'b1) this bit will disable the CDRLF first order loop. Note: This signal is intended to be for verification purposes only. It should be set to 1'b0 for normal operation.
4-0	RX_CDRLF_CNFG_4_0	R/W	Ch	CDRLF first order loop sigma delta update rate: This is the value that is added to or subtracted from the first order loop accumulator register when the serial data sample clock is detected as being out of phase with the serial data on a given parallel data word cycle. This is part of the CDRLF averaging function.

Table 12-641. Register Call Summary for RX_CDRLF_CNFG2__RX_CDRLF_CNFG_j

10-G SerDes Registers

- [RX_CDRLF_CNFG2__RX_CDRLF_CNFG_j](#) Register (Offset = 8100h + formula) [reset = 0A33018Ch]: [0]
- 10-G SerDes Registers: [0]

12.214 RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j Register (Offset = 8104h + formula) [reset = 3h]

RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j is shown in Figure 12-214 and described in Table 12-643.

Return to [Summary Table](#).

CDRLF configuration register 3

Offset = 8104h + (j * 400h); where j = 0h to 3h

Table 12-642.
RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8104h + formula

Figure 12-214. RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j Register

31	30	29	28	27	26	25	24
RX_CDRLF_MGN_DIAG_15_3							
R-0h							
23	22	21	20	19	18	17	16
RX_CDRLF_MGN_DIAG_15_3					RX_CDRLF_MGN_DIAG_2	RX_CDRLF_MGN_DIAG_1	RX_CDRLF_MGN_DIAG_0
R-0h					W-0h	W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_CDRLF_CNFG3_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_CDRLF_CNFG3_15_4				RX_CDRLF_CNFG3_3	RX_CDRLF_CNFG3_2	RX_CDRLF_CNFG3_1	RX_CDRLF_CNFG3_0
R-0h				R/W-0h	R/W-0h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 12-643. RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RX_CDRLF_MGN_DIAG_15_3	R	0h	Reserved
18	RX_CDRLF_MGN_DIAG_2	W	0h	CDRLF PI override down : When the CDRLF PI override enable function is enabled, writing a 1'b1 to this bit will force a down to be generated in the CDRLF PI interface logic. Note : This bit will be automatically cleared after the down request has been sent to the CDRLF PI interface logic. The down request is generated by changing the state of the cdrif_pi_down_in signal in the CDRLF.
17	RX_CDRLF_MGN_DIAG_1	W	0h	CDRLF PI override up : When the CDRLF PI override enable function is enabled, writing a 1'b1 to this bit will force an up to be generated in the CDRLF PI interface logic. Note : This bit will be automatically cleared after the up request has been sent to the CDRLF PI interface logic. The up request is generated by changing the state of the cdrif_pi_up_in signal in the CDRLF.

Table 12-643. RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	RX_CDRLF_MGN_DIAG_0	R/W	0h	CDRLF PI override enable : Setting this bit to 1'b1 will enable the CDRLF PI override function, which will allow ups and downs to be forced to the CDRLF PI interface logic from the up and down override bits in this register. Note : This bit must be set to 1'b1 before the CDRLF PI override up and down bits in this register are changed.
15-4	RX_CDRLF_CNFG3_15_4	R	0h	Reserved
3	RX_CDRLF_CNFG3_3	R/W	0h	CDRLF data filter enable standard mode 3 : Enables the filter function for the data that feeds into the CDRLF from the deserializer, using the rxda_cdrif_data_filter_en_n signal, when xcvr_standard_mode is set to 2'b11. 1'b 0 : Enable filter of 1010 patterns from the CDRLF. 1'b 1 : No CDRLF data filter function enabled.
2	RX_CDRLF_CNFG3_2	R/W	0h	CDRLF data filter enable standard mode 2 : Enables the filter function for the data that feeds into the CDRLF from the deserializer, using the rxda_cdrif_data_filter_en_n signal, when xcvr_standard_mode is set to 2'b10. 1'b 0 : Enable filter of 1010 patterns from the CDRLF. 1'b 1 : No CDRLF data filter function enabled.
1	RX_CDRLF_CNFG3_1	R/W	1h	CDRLF data filter enable standard mode 1 : Enables the filter function for the data that feeds into the CDRLF from the deserializer, using the rxda_cdrif_data_filter_en_n signal, when xcvr_standard_mode is set to 2'b01. 1'b 0 : Enable filter of 1010 patterns from the CDRLF. 1'b 1 : No CDRLF data filter function enabled.
0	RX_CDRLF_CNFG3_0	R/W	1h	CDRLF data filter enable standard mode 0 : Enables the filter function for the data that feeds into the CDRLF from the deserializer, using the rxda_cdrif_data_filter_en_n signal, when xcvr_standard_mode is set to 2'b00. 1'b 0 : Enable filter of 1010 patterns from the CDRLF. 1'b 1 : No CDRLF data filter function enabled.

Table 12-644. Register Call Summary for RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_CDRLF_MGN_DIAG__RX_CDRLF_CNFG3_j Register \(Offset = 8104h + formula\) \[reset = 3h\]: \[0\]](#)

12.215 RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j Register (Offset = 8108h + formula) [reset = 07310071h]

RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j is shown in Figure 12-215 and described in Table 12-646.

Return to [Summary Table](#).

CDRLF fast phase lock timer value register 0

Offset = 8108h + (j * 400h); where j = 0h to 3h

Table 12-645. RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j Instances

Instance	Physical Address
SERDES_10G0	0505 8108h + formula

Figure 12-215. RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j Register

31	30	29	28	27	26	25	24
RX_CDRLF_FPL_TMR1_15_12				RX_CDRLF_FPL_TMR1_11_8			
R-0h				R/W-7h			
23	22	21	20	19	18	17	16
RX_CDRLF_FPL_TMR1_7_4				RX_CDRLF_FPL_TMR1_3_0			
R/W-3h				R/W-1h			
15	14	13	12	11	10	9	8
RX_CDRLF_FPL_TMR0_15_8							
R-0h							
7	6	5	4	3	2	1	0
RX_CDRLF_FPL_TMR0_7_4				RX_CDRLF_FPL_TMR0_3_0			
R/W-7h				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-646. RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RX_CDRLF_FPL_TMR1_15_12	R	0h	Reserved
27-24	RX_CDRLF_FPL_TMR1_11_8	R/W	7h	Fast phase lock timer trigger 1 state time value : Specifies the number of clock cycles minus 1 that the fast phase lock state machine will remain in the trigger state the first time it is in that state. The recommended value for this is the number of PI steps required to move the PI 1/4 UI.
23-20	RX_CDRLF_FPL_TMR1_7_4	R/W	3h	Fast phase lock timer trigger 2 state time value : Specifies the number of clock cycles minus 1 that the fast phase lock state machine will remain in the trigger state the second time it is in that state. The recommended value for this is the number of PI steps required to move the PI 1/8 UI.
19-16	RX_CDRLF_FPL_TMR1_3_0	R/W	1h	Fast phase lock timer trigger 3 state time value : Specifies the number of clock cycles minus 1 that the fast phase lock state machine will remain in the trigger state the third time it is in that state. The recommended value for this is the number of PI steps required to move the PI 1/16 UI.
15-8	RX_CDRLF_FPL_TMR0_15_8	R	0h	Reserved

Table 12-646. RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	RX_CDRLF_FPL_TMR0_7_4	R/W	7h	Fast phase lock timer accumulate state time value : Specifies the number of clock cycles minus 1 that the fast phase lock state machine will remain in the accumulate state.
3-0	RX_CDRLF_FPL_TMR0_3_0	R/W	1h	Fast phase lock timer delay state time value : Specifies the number of clock cycles minus 1 that the fast phase lock state machine will remain in the delay state.

Table 12-647. Register Call Summary for RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_CDRLF_FPL_TMR1__RX_CDRLF_FPL_TMR0_j Register \(Offset = 8108h + formula\) \[reset = 07310071h\]: \[0\]](#)

12.216 RX_SIGDET_HL_DLY_TMR__RX_SIGDET_HL_FILT_TMR_j Register (Offset = 8120h + formula) [reset = Ch]

RX_SIGDET_HL_DLY_TMR__RX_SIGDET_HL_FILT_TMR_j is shown in Figure 12-216 and described in Table 12-649.

Return to [Summary Table](#).

Receiver signal detect filter high to low filter timer register

Offset = 8120h + (j * 400h); where j = 0h to 3h

Table 12-648. RX_SIGDET_HL_DLY_TMR__RX_SIGDET_HL_FILT_TMR_j Instances

Instance	Physical Address
SERDES_10G0	0505 8120h + formula

Figure 12-216. RX_SIGDET_HL_DLY_TMR__RX_SIGDET_HL_FILT_TMR_j Register

31	30	29	28	27	26	25	24
RX_SIGDET_HL_DLY_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
RX_SIGDET_HL_DLY_TMR_15_6		RX_SIGDET_HL_DLY_TMR_5_0					
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
RX_SIGDET_HL_FILT_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
RX_SIGDET_HL_FILT_TMR_15_6		RX_SIGDET_HL_FILT_TMR_5_0					
R-0h				R/W-Ch			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-649. RX_SIGDET_HL_DLY_TMR__RX_SIGDET_HL_FILT_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RX_SIGDET_HL_DLY_TMR_15_6	R	0h	Reserved
21-16	RX_SIGDET_HL_DLY_TMR_5_0	R/W	0h	Signal detect filter high to low delay timer value: This is the value loaded into the delay timer in the signal detect high to low filter circuit.
15-6	RX_SIGDET_HL_FILT_TMR_15_6	R	0h	Reserved
5-0	RX_SIGDET_HL_FILT_TMR_5_0	R/W	Ch	Signal detect filter high to low filter timer value: This is the value loaded into the filter timer in the signal detect high to low filter circuit.

Table 12-650. Register Call Summary for RX_SIGDET_HL_DLY_TMR__RX_SIGDET_HL_FILT_TMR_j

10-G SerDes Registers

- [RX_SIGDET_HL_DLY_TMR__RX_SIGDET_HL_FILT_TMR_j Register \(Offset = 8120h + formula\) \[reset = Ch\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.217 RX_SIGDET_HL_INIT_TMR__RX_SIGDET_HL_MIN_TMR_j Register (Offset = 8124h + formula) [reset = 00280000h]

RX_SIGDET_HL_INIT_TMR__RX_SIGDET_HL_MIN_TMR_j is shown in Figure 12-217 and described in Table 12-652.

Return to [Summary Table](#).

Receiver signal detect filter high to low min timer register

Offset = 8124h + (j * 400h); where j = 0h to 3h

**Table 12-651. RX_SIGDET_HL_INIT_TMR__RX_SIGDET_HL_MIN_TMR_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 8124h + formula

Figure 12-217. RX_SIGDET_HL_INIT_TMR__RX_SIGDET_HL_MIN_TMR_j Register

31	30	29	28	27	26	25	24
RX_SIGDET_HL_INIT_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
RX_SIGDET_HL_INIT_TMR_15_6		RX_SIGDET_HL_INIT_TMR_5_0					
R-0h		R/W-28h					
15	14	13	12	11	10	9	8
RX_SIGDET_HL_MIN_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
RX_SIGDET_HL_MIN_TMR_15_6		RX_SIGDET_HL_MIN_TMR_5_0					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-652. RX_SIGDET_HL_INIT_TMR__RX_SIGDET_HL_MIN_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RX_SIGDET_HL_INIT_TMR_15_6	R	0h	Reserved
21-16	RX_SIGDET_HL_INIT_TMR_5_0	R/W	28h	Signal detect init timer value: This is the value loaded into the initialization timer in the signal detect filter high to low filter circuit.
15-6	RX_SIGDET_HL_MIN_TMR_15_6	R	0h	Reserved
5-0	RX_SIGDET_HL_MIN_TMR_5_0	R/W	0h	Signal detect filter high to low min timer value: This is the value loaded into the min timer in the signal detect high to low filter circuit.

Table 12-653. Register Call Summary for RX_SIGDET_HL_INIT_TMR__RX_SIGDET_HL_MIN_TMR_j

10-G SerDes Registers

- [RX_SIGDET_HL_INIT_TMR__RX_SIGDET_HL_MIN_TMR_j Register \(Offset = 8124h + formula\) \[reset = 00280000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.218 RX_SIGDET_LH_DLY_TMR__RX_SIGDET_LH_FILT_TMR_j Register (Offset = 8128h + formula) [reset = 4h]

RX_SIGDET_LH_DLY_TMR__RX_SIGDET_LH_FILT_TMR_j is shown in Figure 12-218 and described in Table 12-655.

Return to [Summary Table](#).

Receiver signal detect filter low to high filter timer register

Offset = 8128h + (j * 400h); where j = 0h to 3h

**Table 12-654. RX_SIGDET_LH_DLY_TMR__RX_SIGDET_LH_FILT_TMR_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 8128h + formula

Figure 12-218. RX_SIGDET_LH_DLY_TMR__RX_SIGDET_LH_FILT_TMR_j Register

31	30	29	28	27	26	25	24
RX_SIGDET_LH_DLY_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
RX_SIGDET_LH_DLY_TMR_15_6		RX_SIGDET_LH_DLY_TMR_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
RX_SIGDET_LH_FILT_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
RX_SIGDET_LH_FILT_TMR_15_6		RX_SIGDET_LH_FILT_TMR_5_0					
R-0h		R/W-4h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-655. RX_SIGDET_LH_DLY_TMR__RX_SIGDET_LH_FILT_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RX_SIGDET_LH_DLY_TMR_15_6	R	0h	Reserved
21-16	RX_SIGDET_LH_DLY_TMR_5_0	R/W	0h	Signal detect filter low to high min timer value: This is the value loaded into the min timer in the signal detect low to high filter circuit.
15-6	RX_SIGDET_LH_FILT_TMR_15_6	R	0h	Reserved
5-0	RX_SIGDET_LH_FILT_TMR_5_0	R/W	4h	Signal detect filter low to high filter timer value: This is the value loaded into the filter timer in the signal detect low to high filter circuit. This should be set to 5 less than the number of clocks of desired filter time. This takes into account the synchronizing of the signal to be filtered (4 clocks) and the time to load the filter timer (1 clock). Therefore, the smallest granularity of filtering available here is 5 clocks. This is more of an issue of latency through the filter circuit as the signal initially rises.

Table 12-656. Register Call Summary for RX_SIGDET_LH_DLY_TMR__RX_SIGDET_LH_FILT_TMR_j

10-G SerDes Registers <ul style="list-style-type: none"> RX_SIGDET_LH_DLY_TMR__RX_SIGDET_LH_FILT_TMR_j Register (Offset = 8128h + formula) [reset = 4h]: [0] 10-G SerDes Registers: [0]

12.219 RX_SIGDET_LH_INIT_TMR__RX_SIGDET_LH_MIN_TMR_j Register (Offset = 812Ch + formula) [reset = 00280000h]

RX_SIGDET_LH_INIT_TMR__RX_SIGDET_LH_MIN_TMR_j is shown in Figure 12-219 and described in Table 12-658.

Return to [Summary Table](#).

Receiver signal detect filter low to high min timer register

Offset = 812Ch + (j * 400h); where j = 0h to 3h

**Table 12-657. RX_SIGDET_LH_INIT_TMR__RX_SIGDET_LH_MIN_TMR_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 812Ch + formula

Figure 12-219. RX_SIGDET_LH_INIT_TMR__RX_SIGDET_LH_MIN_TMR_j Register

31	30	29	28	27	26	25	24
RX_SIGDET_LH_INIT_TMR_15_6							
R-0h							
23	22	21	20	19	18	17	16
RX_SIGDET_LH_INIT_TMR_15_6		RX_SIGDET_LH_INIT_TMR_5_0					
R-0h		R/W-28h					
15	14	13	12	11	10	9	8
RX_SIGDET_LH_MIN_TMR_15_6							
R-0h							
7	6	5	4	3	2	1	0
RX_SIGDET_LH_MIN_TMR_15_6		RX_SIGDET_LH_MIN_TMR_5_0					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-658. RX_SIGDET_LH_INIT_TMR__RX_SIGDET_LH_MIN_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RX_SIGDET_LH_INIT_TMR_15_6	R	0h	Reserved
21-16	RX_SIGDET_LH_INIT_TMR_5_0	R/W	28h	Signal detect init timer value: This is the value loaded into the initialization timer in the signal detect filter high to low filter circuit.
15-6	RX_SIGDET_LH_MIN_TMR_15_6	R	0h	Reserved
5-0	RX_SIGDET_LH_MIN_TMR_5_0	R/W	0h	Signal detect filter high to low min timer value: This is the value loaded into the min timer in the signal detect high to low filter circuit.

Table 12-659. Register Call Summary for RX_SIGDET_LH_INIT_TMR__RX_SIGDET_LH_MIN_TMR_j

10-G SerDes Registers

- [RX_SIGDET_LH_INIT_TMR__RX_SIGDET_LH_MIN_TMR_j Register \(Offset = 812Ch + formula\) \[reset = 00280000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.220 RX_LFPSDET_NS_CNT__RX_LFPSDET_MD_CNT_j Register (Offset = 8130h + formula) [reset = 5h]

[RX_LFPSDET_NS_CNT__RX_LFPSDET_MD_CNT_j](#) is shown in [Figure 12-220](#) and described in [Table 12-661](#).

Return to [Summary Table](#).

Receiver LFPS detect minimum pulse distance counter register

Offset = 8130h + (j * 400h); where j = 0h to 3h

Table 12-660. RX_LFPSDET_NS_CNT__RX_LFPSDET_MD_CNT_j Instances

Instance	Physical Address
SERDES_10G0	0505 8130h + formula

Figure 12-220. RX_LFPSDET_NS_CNT__RX_LFPSDET_MD_CNT_j Register

31	30	29	28	27	26	25	24
RX_LFPSDET_NS_CNT_15_2							
R-0h							
23	22	21	20	19	18	17	16
RX_LFPSDET_NS_CNT_15_2						RX_LFPSDET_NS_CNT_1_0	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
RX_LFPSDET_MD_CNT_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_LFPSDET_MD_CNT_15_4				RX_LFPSDET_MD_CNT_3_0			
R-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-661. RX_LFPSDET_NS_CNT__RX_LFPSDET_MD_CNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RX_LFPSDET_NS_CNT_15_2	R	0h	Reserved
17-16	RX_LFPSDET_NS_CNT_1_0	R/W	0h	No signal counter value (NS): Specifies the number of clock cycles where pulse_high and pulse_low are inactive before declaring no signal. Note: a value of 2'b00 is not a valid value for this field.
15-4	RX_LFPSDET_MD_CNT_15_4	R	0h	Reserved
3-0	RX_LFPSDET_MD_CNT_3_0	R/W	5h	Minimum pulse distance counter value (MD): Specifies the minimum pulse distance for a valid LFPS sequence. Note that MD must be set to a value that is greater than MP.

Table 12-662. Register Call Summary for RX_LFPSDET_NS_CNT__RX_LFPSDET_MD_CNT_j

10-G SerDes Registers

- [RX_LFPSDET_NS_CNT__RX_LFPSDET_MD_CNT_j Register \(Offset = 8130h + formula\) \[reset = 5h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.221 RX_LFPSDET_MP_CNT_RX_LFPSDET_RD_CNT_j Register (Offset = 8134h + formula) [reset = 00070007h]

[RX_LFPSDET_MP_CNT_RX_LFPSDET_RD_CNT_j](#) is shown in [Figure 12-221](#) and described in [Table 12-664](#).

Return to [Summary Table](#).

Receiver LFPS detect ramp down counter register

Offset = 8134h + (j * 400h); where j = 0h to 3h

Table 12-663. RX_LFPSDET_MP_CNT_RX_LFPSDET_RD_CNT_j Instances

Instance	Physical Address
SERDES_10G0	0505 8134h + formula

Figure 12-221. RX_LFPSDET_MP_CNT_RX_LFPSDET_RD_CNT_j Register

31	30	29	28	27	26	25	24
RX_LFPSDET_MP_CNT_15_3							
R-0h							
23	22	21	20	19	18	17	16
RX_LFPSDET_MP_CNT_15_3				RX_LFPSDET_MP_CNT_2_0			
R-0h				R/W-7h			
15	14	13	12	11	10	9	8
RX_LFPSDET_RD_CNT_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_LFPSDET_RD_CNT_15_4				RX_LFPSDET_RD_CNT_3_0			
R-0h				R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-664. RX_LFPSDET_MP_CNT_RX_LFPSDET_RD_CNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RX_LFPSDET_MP_CNT_15_3	R	0h	Reserved
18-16	RX_LFPSDET_MP_CNT_2_0	R/W	7h	Minimum pulse duration (MP): Specifies the minimum number of clock cycles required for a given LFPS pulse to be driven active to be considered part of a valid LFPS burst.
15-4	RX_LFPSDET_RD_CNT_15_4	R	0h	Reserved
3-0	RX_LFPSDET_RD_CNT_3_0	R/W	7h	Ramp down counter value (RD): Species the number of clock cycles that are used in the LFPS detect ramp down process. This signal should correspond to the MD, to reduce LFPS distortion. Note that the actual ramp down time is a function of the detection of no signal when lfps_detected is driven active. If no signal is detected, the ramp down time is the value in this field minus the value of the no signal counter value field in the RX_LFPSDET_NS_CNT register. Otherwise, the value in this field is used as is.

Table 12-665. Register Call Summary for RX_LFPSDET_MP_CNT_RX_LFPSDET_RD_CNT_j

10-G SerDes Registers

- [RX_LFPSDET_MP_CNT_RX_LFPSDET_RD_CNT_j Register \(Offset = 8134h + formula\) \[reset = 00070007h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.222 RX_LFPSDET_DIAG_CTRL_j Register (Offset = 8138h + formula) [reset = X]

RX_LFPSDET_DIAG_CTRL_j is shown in Figure 12-222 and described in Table 12-667.

Return to [Summary Table](#).

Receiver LFPS detect diagnostic control register

Offset = 8138h + (j * 400h); where j = 0h to 3h

**Table 12-666. RX_LFPSDET_DIAG_CTRL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 8138h + formula

Figure 12-222. RX_LFPSDET_DIAG_CTRL_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_LFPSDET_DIAG_CTRL_15_3							
R-0h							
7	6	5	4	3	2	1	0
RX_LFPSDET_DIAG_CTRL_15_3					RX_LFPSDET_DIAG_CTRL_2	RX_LFPSDET_DIAG_CTRL_1	RX_LFPSDET_DIAG_CTRL_0
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-667. RX_LFPSDET_DIAG_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-3	RX_LFPSDET_DIAG_CTRL_15_3	R	0h	Reserved
2	RX_LFPSDET_DIAG_CTRL_2	R/W	0h	Disable pulse none MD check: When active (1'b1), the check that tests if pulse_none is driven inactive while the MD check is being performed will be disabled.
1	RX_LFPSDET_DIAG_CTRL_1	R/W	0h	LFPS detect override enable: When active (1'b1), the LFPS detect override bit in this register will drive the LFPS detect output directly.
0	RX_LFPSDET_DIAG_CTRL_0	R/W	0h	LFPS detect override: When enabled by the LFPS detect override enable bit in this register, this bit will drive the LFPS detect output directly.

Table 12-668. Register Call Summary for RX_LFPSDET_DIAG_CTRL_j

10-G SerDes Registers

- [RX_LFPSDET_DIAG_CTRL_j Register \(Offset = 8138h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.223 RX_EYESURF_CTRL_j Register (Offset = 8140h + formula) [reset = X]

RX_EYESURF_CTRL_j is shown in Figure 12-223 and described in Table 12-670.

Return to [Summary Table](#).

Eye surf control register

Offset = 8140h + (j * 400h); where j = 0h to 3h

Table 12-669. RX_EYESURF_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8140h + formula

Figure 12-223. RX_EYESURF_CTRL_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_EYESURF_CTRL_15	RX_EYESURF_CTRL_14	RX_EYESURF_CTRL_13_0					
R/W-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
RX_EYESURF_CTRL_13_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-670. RX_EYESURF_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RX_EYESURF_CTRL_15	R/W	0h	Eye surf run: Setting this bit to 1'b1 will initiate the eye surf process. This bit must remain set to 1'b1 until the eye surf done bit is set.
14	RX_EYESURF_CTRL_14	R	0h	Eye surf done: When this bit is set to 1'b1, the eye surf process has completed. This bit will be cleared after the eye surf run bit is cleared.
13-0	RX_EYESURF_CTRL_13_0	R	0h	Reserved

Table 12-671. Register Call Summary for RX_EYESURF_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_EYESURF_CTRL_j Register \(Offset = 8140h + formula\) \[reset = X\]: \[0\]](#)

12.224 RX_EYESURF_TMR_DELHIGH__RX_EYESURF_TMR_DELOW_j Register (Offset = 8148h + formula) [reset = 0h]

[RX_EYESURF_TMR_DELHIGH__RX_EYESURF_TMR_DELOW_j](#) is shown in [Figure 12-224](#) and described in [Table 12-673](#).

Return to [Summary Table](#).

Eye surf timer delay low register

Offset = 8148h + (j * 400h); where j = 0h to 3h

Table 12-672. RX_EYESURF_TMR_DELHIGH__RX_EYESURF_TMR_DELOW_j Instances

Instance	Physical Address
SERDES_10G0	0505 8148h + formula

Figure 12-224. RX_EYESURF_TMR_DELHIGH__RX_EYESURF_TMR_DELOW_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_EYESURF_TMR_DELHIGH_15_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_EYESURF_TMR_DELOW_15_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-673. RX_EYESURF_TMR_DELHIGH__RX_EYESURF_TMR_DELOW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_EYESURF_TMR_DELHIGH_15_0	R/W	0h	Most significant 16 bits of the delay time: The delay time specifies the number of clock cycles to wait between when a coordinate test point is set, and when to start testing the i and e data. Note : It is not valid to set the total eye surf timer delay value to 0.
15-0	RX_EYESURF_TMR_DELOW_15_0	R/W	0h	Least significant 16 bits of the delay time: The delay time specifies the number of clock cycles to wait between when a coordinate test point is set, and when to start testing the i and e data. Note : It is not valid to set the total eye surf timer delay value to 0.

Table 12-674. Register Call Summary for RX_EYESURF_TMR_DELHIGH__RX_EYESURF_TMR_DELOW_j

10-G SerDes Registers
<ul style="list-style-type: none"> RX_EYESURF_TMR_DELHIGH__RX_EYESURF_TMR_DELOW_j Register (Offset = 8148h + formula) [reset = 0h]: [0] 10-G SerDes Registers: [0]

12.225 RX_EYESURF_TMR_TESTHIGH__RX_EYESURF_TMR_TESTLOW_j Register (Offset = 814Ch + formula) [reset = 0h]

[RX_EYESURF_TMR_TESTHIGH__RX_EYESURF_TMR_TESTLOW_j](#) is shown in [Figure 12-225](#) and described in [Table 12-676](#).

Return to [Summary Table](#).

Eye surf timer test low register

Offset = 814Ch + (j * 400h); where j = 0h to 3h

Table 12-675.

RX_EYESURF_TMR_TESTHIGH__RX_EYESURF_TMR_TESTLOW_j Instances

Instance	Physical Address
SERDES_10G0	0505 814Ch + formula

Figure 12-225. RX_EYESURF_TMR_TESTHIGH__RX_EYESURF_TMR_TESTLOW_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_EYESURF_TMR_TESTHIGH_15_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_EYESURF_TMR_TESTLOW_15_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-676. RX_EYESURF_TMR_TESTHIGH__RX_EYESURF_TMR_TESTLOW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_EYESURF_TMR_TESTHIGH_15_0	R/W	0h	Most significant 16 bits of the test time: The test time specifies the number of clock cycles to test the i and e data at a given coordinate test point. Note : It is not valid to set the total eye surf timer test value to 0.
15-0	RX_EYESURF_TMR_TESTLOW_15_0	R/W	0h	Least significant 16 bits of the test time: The test time specifies the number of clock cycles to test the i and e data at a given coordinate test point. Note : It is not valid to set the total eye surf timer test value to 0.

**Table 12-677. Register Call Summary for
RX_EYESURF_TMR_TESTHIGH__RX_EYESURF_TMR_TESTLOW_j**

10-G SerDes Registers
<ul style="list-style-type: none"> RX_EYESURF_TMR_TESTHIGH__RX_EYESURF_TMR_TESTLOW_j Register (Offset = 814Ch + formula) [reset = 0h]: [0] 10-G SerDes Registers: [0]

12.226 RX_EYESURF_EW_COORD__RX_EYESURF_NS_COORD_j Register (Offset = 8150h + formula) [reset = 0h]

RX_EYESURF_EW_COORD__RX_EYESURF_NS_COORD_j is shown in Figure 12-226 and described in Table 12-679.

Return to [Summary Table](#).

Eye surf north south test point coordinate register

Offset = 8150h + (j * 400h); where j = 0h to 3h

Table 12-678. RX_EYESURF_EW_COORD__RX_EYESURF_NS_COORD_j Instances

Instance	Physical Address
SERDES_10G0	0505 8150h + formula

Figure 12-226. RX_EYESURF_EW_COORD__RX_EYESURF_NS_COORD_j Register

31	30	29	28	27	26	25	24
RX_EYESURF_EW_COORD_15_9							RX_EYESURF_EW_COORD_8
R-0h							R/W-0h
23	22	21	20	19	18	17	16
RX_EYESURF_EW_COORD_7_5			RX_EYESURF_EW_COORD_4_0				
R-0h			R/W-0h				
15	14	13	12	11	10	9	8
RX_EYESURF_NS_COORD_15_9							RX_EYESURF_NS_COORD_8
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RX_EYESURF_NS_COORD_7	RX_EYESURF_NS_COORD_6_0						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-679. RX_EYESURF_EW_COORD__RX_EYESURF_NS_COORD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RX_EYESURF_EW_COORD_15_9	R	0h	Reserved
24	RX_EYESURF_EW_COORD_8	R/W	0h	Test point coordinate east west direction : Indicates whether the desired test point is in the east or the west direction relative to the origin. 1 : East 0 : West
23-21	RX_EYESURF_EW_COORD_7_5	R	0h	Reserved
20-16	RX_EYESURF_EW_COORD_4_0	R/W	0h	Test point coordinate east west offset : Indicates how many steps in the east or west direction the desired test point is relative to the origin.
15-9	RX_EYESURF_NS_COORD_15_9	R	0h	Reserved

**Table 12-679. RX_EYESURF_EW_COORD__RX_EYESURF_NS_COORD_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
8	RX_EYESURF_NS_COORD_8	R/W	0h	Test point coordinate north south direction : Indicates whether the desired test point is in the north or the south direction relative to the origin. 1 : North 0 : South
7	RX_EYESURF_NS_COORD_7	R	0h	Reserved
6-0	RX_EYESURF_NS_COORD_6_0	R/W	0h	Test point coordinate north south offset : Indicates how many steps in the north or south direction the desired test point is relative to the origin. Note that in this implementation, only 5 least significant bits are used to control the sampler error DAC. Therefore, the most significant bits of this field are not used.

Table 12-680. Register Call Summary for RX_EYESURF_EW_COORD__RX_EYESURF_NS_COORD_j

10-G SerDes Registers

- [RX_EYESURF_EW_COORD__RX_EYESURF_NS_COORD_j Register \(Offset = 8150h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.227 RX_EYESURF_ERRCNT_j Register (Offset = 8154h + formula) [reset = X]

RX_EYESURF_ERRCNT_j is shown in Figure 12-227 and described in Table 12-682.

Return to [Summary Table](#).

Eye surf bit error count register

Offset = 8154h + (j * 400h); where j = 0h to 3h

Table 12-681. RX_EYESURF_ERRCNT_j Instances

Instance	Physical Address
SERDES_10G0	0505 8154h + formula

Figure 12-227. RX_EYESURF_ERRCNT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_EYESURF_ERRCNT_15_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 12-682. RX_EYESURF_ERRCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	RX_EYESURF_ERRCNT_15_0	R	0h	Test point bit error count : The total number of bit errors that were detected for a given run of the eye surf function. This register is only valid after the eye surf done bit in the Eye surf control register on page 290 is active, and will be cleared when the done bit is cleared in response to the run bit being cleared.

Table 12-683. Register Call Summary for RX_EYESURF_ERRCNT_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_EYESURF_ERRCNT_j Register \(Offset = 8154h + formula\) \[reset = X\]: \[0\]](#)

12.228 RX_BIST_SYNCCNT__RX_BIST_CTRL_j Register (Offset = 8160h + formula) [reset = 0h]

RX_BIST_SYNCCNT__RX_BIST_CTRL_j is shown in Figure 12-228 and described in Table 12-685.

Return to [Summary Table](#).

Receiver BIST control register

Offset = 8160h + (j * 400h); where j = 0h to 3h

Table 12-684.
RX_BIST_SYNCCNT__RX_BIST_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8160h + formula

Figure 12-228. RX_BIST_SYNCCNT__RX_BIST_CTRL_j Register

31	30	29	28	27	26	25	24
RX_BIST_SYNCCNT_15_0							
R/W-0h							
23	22	21	20	19	18	17	16
RX_BIST_SYNCCNT_15_0							
R/W-0h							
15	14	13	12	11	10	9	8
RX_BIST_CTRL_15_12				RX_BIST_CTRL_11_8			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RX_BIST_CTRL_7_5			RX_BIST_CTR L_4	RX_BIST_CTRL_3_2		RX_BIST_CTR L_1	RX_BIST_CTR L_0
R-0h			R/W-0h	R-0h		W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 12-685. RX_BIST_SYNCCNT__RX_BIST_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_BIST_SYNCCNT_15_0	R/W	0h	Receiver BIST sync count: This field controls the value of the RX BIST sync count. The sync count indicates the number of consecutive received data words with no BIST bit errors that must be received in order for the RX BIST module to be considered synced to the input data stream. It is recommended that, when using a clean channel, this register be set to 16'h00FA. This will require the RX BIST to receive 250 consecutive words of data to confirm a BIST sync, which is enough time to allow the CDRLF to lock.
15-12	RX_BIST_CTRL_15_12	R	0h	Reserved

Table 12-685. RX_BIST_SYNCCNT__RX_BIST_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	RX_BIST_CTRL_11_8	R/W	0h	Receiver BIST mode: Controls which mode the BIST will operate in. The value of this field must match the corresponding field for the receive BIST controller. The following are the values used for this field, and what BIST mode they correspond to. 4'b 0000 : User defined data FIFO 4'b 0001 - 4'b 0111 : Reserved 4'b 1000 : PRBS7 : 7 bit LFSR 4'b 1001 : PRBS15 : 15 bit LFSR 4'b 1010 : PRBS23 : 23 bit LFSR 4'b 1011 : PRBS31 : 31 bit LFSR 4'b 1100 - 4'b 1111 : Reserved
7-5	RX_BIST_CTRL_7_5	R	0h	Reserved
4	RX_BIST_CTRL_4	R/W	0h	Receiver BIST error reset: Writing this bit is set to a 1'b1 will hold the error indicators in the receive BIST logic in reset. When this signal goes active, the rx_bist_status pin, rx_bist_err_toggle pin, and receive BIST error count field in this register will be cleared. When this bit is cleared, these error indicators will be released from reset and operate normally.
3-2	RX_BIST_CTRL_3_2	R	0h	Reserved
1	RX_BIST_CTRL_1	W	0h	Receiver BIST user defined data FIFO clear: Writing a 1'b1 to this bit will clear the receiver BIST user defined data FIFO. Note : This bit is automatically cleared after it is written to. Note : This clear function simply resets the FIFO pointers. It does not clear the contents of the FIFO.
0	RX_BIST_CTRL_0	R/W	0h	Receiver BIST enable: This bit enables the receiver BIST function. Note : The remaining bits in this register must be stable when changing this bit. Therefore, it is best to enable and disable this function using a read / modify / write of this bit.

Table 12-686. Register Call Summary for RX_BIST_SYNCCNT__RX_BIST_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_BIST_SYNCCNT__RX_BIST_CTRL_j Register \(Offset = 8160h + formula\) \[reset = 0h\]: \[0\]](#)

12.229 RX_BIST_ERRCNT__RX_BIST_UDDWR_j Register (Offset = 8164h + formula) [reset = 0h]

RX_BIST_ERRCNT__RX_BIST_UDDWR_j is shown in Figure 12-229 and described in Table 12-688.

Return to [Summary Table](#).

Receiver BIST user defined data write register

Offset = 8164h + (j * 400h); where j = 0h to 3h

Table 12-687.
RX_BIST_ERRCNT__RX_BIST_UDDWR_j Instances

Instance	Physical Address
SERDES_10G0	0505 8164h + formula

Figure 12-229. RX_BIST_ERRCNT__RX_BIST_UDDWR_j Register

31	30	29	28	27	26	25	24
RX_BIST_ERRCNT_15_0							
R-0h							
23	22	21	20	19	18	17	16
RX_BIST_ERRCNT_15_0							
R-0h							
15	14	13	12	11	10	9	8
RX_BIST_UDDWR_15_10						RX_BIST_UDDWR_9_0	
R-0h						W-0h	
7	6	5	4	3	2	1	0
RX_BIST_UDDWR_9_0							
W-0h							

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 12-688. RX_BIST_ERRCNT__RX_BIST_UDDWR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_BIST_ERRCNT_15_0	R	0h	Receiver BIST error count: Indicates the number of BIST errors that have been observed by the receive BIST logic, since the last time the BIST error indicator logic was reset or restarted. This counter increments up to a maximum value of 16'hFFFF. Note : Due to the nature of the BIST PRBS error detection logic, when a bit error occurs in PRBS mode, two or three errors will be counted.
15-10	RX_BIST_UDDWR_15_10	R	0h	Reserved
9-0	RX_BIST_UDDWR_9_0	W	0h	Receiver BIST user defined data: Writing a data word to this field will result in that data word being placed in the next available position in the receiver BIST user defined data FIFO. Note, when in 20 bit mode, all 10 of these bits are used. When in 16 bit mode, only the least significant 8 bits are used. Note that the FIFO in this implementation is 18 words deep. It is up to the user to not write more than 18 words of data into this FIFO. Exceeding this amount of data will generate unpredictable results.

Table 12-689. Register Call Summary for RX_BIST_ERRCNT_RX_BIST_UDDWR_j

10-G SerDes Registers <ul style="list-style-type: none"> RX_BIST_ERRCNT_RX_BIST_UDDWR_j Register (Offset = 8164h + formula) [reset = 0h]: [0] 10-G SerDes Registers: [0]
--

12.230 RX_REE_PTxEQSM_EQENM_EVAL__RX_REE_PTxEQSM_CTRL_j Register (Offset = 8200h + formula) [reset = 3BC70000h]

[RX_REE_PTxEQSM_EQENM_EVAL__RX_REE_PTxEQSM_CTRL_j](#) is shown in [Figure 12-230](#) and described in [Table 12-691](#).

Return to [Summary Table](#).

REE PCIe TX equalization control state machine control register

Offset = 8200h + (j * 400h); where j = 0h to 3h

Table 12-690.
RX_REE_PTxEQSM_EQENM_EVAL__RX_REE_PTxEQSM_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8200h + formula

Figure 12-230. RX_REE_PTxEQSM_EQENM_EVAL__RX_REE_PTxEQSM_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_PTxEQSM_EQENM_EVAL_15	RX_REE_PTxEQSM_EQENM_EVAL_14	RX_REE_PTxEQSM_EQENM_EVAL_13	RX_REE_PTxEQSM_EQENM_EVAL_12	RX_REE_PTxEQSM_EQENM_EVAL_11	RX_REE_PTxEQSM_EQENM_EVAL_10	RX_REE_PTxEQSM_EQENM_EVAL_9	RX_REE_PTxEQSM_EQENM_EVAL_8
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
RX_REE_PTxEQSM_EQENM_EVAL_7	RX_REE_PTxEQSM_EQENM_EVAL_6	RX_REE_PTxEQSM_EQENM_EVAL_5	RX_REE_PTxEQSM_EQENM_EVAL_4	RX_REE_PTxEQSM_EQENM_EVAL_3	RX_REE_PTxEQSM_EQENM_EVAL_2	RX_REE_PTxEQSM_EQENM_EVAL_1	RX_REE_PTxEQSM_EQENM_EVAL_0
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
RX_REE_PTxEQSM_CTRL_15_0							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_PTxEQSM_CTRL_15_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-691. RX_REE_PTxEQSM_EQENM_EVAL__RX_REE_PTxEQSM_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_PTxEQSM_EQENM_EVAL_15	R/W	0h	Reserved - spare
30	RX_REE_PTxEQSM_EQENM_EVAL_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
29	RX_REE_PTxEQSM_EQENM_EVAL_13	R/W	1h	TX equalization evaluator : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
28	RX_REE_PTxEQSM_EQENM_EVAL_12	R/W	1h	TX post cursor control : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
27	RX_REE_PTxEQSM_EQENM_EVAL_11	R/W	1h	TX pre cursor control : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.

Table 12-691. RX_REE_PTSEQSM_EQENM_EVAL_RX_REE_PTSEQSM_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	RX_REE_PTSEQSM_EQENM_EVAL_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the TX equalization general control state machine is controlling the REE.
25	RX_REE_PTSEQSM_EQENM_EVAL_9	R/W	1h	RX attenuation : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
24	RX_REE_PTSEQSM_EQENM_EVAL_8	R/W	1h	RX VGA gain : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
23	RX_REE_PTSEQSM_EQENM_EVAL_7	R/W	1h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
22	RX_REE_PTSEQSM_EQENM_EVAL_6	R/W	1h	RX peaking amp gain : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
21	RX_REE_PTSEQSM_EQENM_EVAL_5	R/W	0h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
20	RX_REE_PTSEQSM_EQENM_EVAL_4	R/W	0h	Reserved - spare
19	RX_REE_PTSEQSM_EQENM_EVAL_3	R/W	0h	Reserved - spare
18	RX_REE_PTSEQSM_EQENM_EVAL_2	R/W	1h	RX tap3 : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
17	RX_REE_PTSEQSM_EQENM_EVAL_1	R/W	1h	RX tap2 : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
16	RX_REE_PTSEQSM_EQENM_EVAL_0	R/W	1h	RX tap1 : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
15-0	RX_REE_PTSEQSM_CTRL_15_0	R	0h	Reserved

Table 12-692. Register Call Summary for RX_REE_PTSEQSM_EQENM_EVAL_RX_REE_PTSEQSM_CTRL_j

10-G SerDes Registers

- [RX_REE_PTSEQSM_EQENM_EVAL_RX_REE_PTSEQSM_CTRL_j Register \(Offset = 8200h + formula\) \[reset = 3BC70000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.231 RX_REE_PTxEQSM_PEVAL_TMR_RX_REE_PTxEQSM_EQENM_PEVAL_j Register (Offset = 8204h + formula) [reset = 0h]

[RX_REE_PTxEQSM_PEVAL_TMR_RX_REE_PTxEQSM_EQENM_PEVAL_j](#) is shown in [Figure 12-231](#) and described in [Table 12-694](#).

Return to [Summary Table](#).

REE PCIe TX equalization control state machine equalization enable mask for PCIe post evaluation equalization register

Offset = 8204h + (j * 400h); where j = 0h to 3h

Table 12-693.
RX_REE_PTxEQSM_PEVAL_TMR_RX_REE_PTxEQSM_EQENM_PEVAL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8204h + formula

Figure 12-231. RX_REE_PTxEQSM_PEVAL_TMR_RX_REE_PTxEQSM_EQENM_PEVAL_j Register

31	30	29	28	27	26	25	24
RX_REE_PTxEQSM_PEVAL_TMR_15_0							
R/W-0h							
23	22	21	20	19	18	17	16
RX_REE_PTxEQSM_PEVAL_TMR_15_0							
R/W-0h							
15	14	13	12	11	10	9	8
RX_REE_PTxEQSM_EQENM_PEVAL_15	RX_REE_PTxEQSM_EQENM_PEVAL_14	RX_REE_PTxEQSM_EQENM_PEVAL_13	RX_REE_PTxEQSM_EQENM_PEVAL_12	RX_REE_PTxEQSM_EQENM_PEVAL_11	RX_REE_PTxEQSM_EQENM_PEVAL_10	RX_REE_PTxEQSM_EQENM_PEVAL_9	RX_REE_PTxEQSM_EQENM_PEVAL_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_REE_PTxEQSM_EQENM_PEVAL_7	RX_REE_PTxEQSM_EQENM_PEVAL_6	RX_REE_PTxEQSM_EQENM_PEVAL_5	RX_REE_PTxEQSM_EQENM_PEVAL_4	RX_REE_PTxEQSM_EQENM_PEVAL_3	RX_REE_PTxEQSM_EQENM_PEVAL_2	RX_REE_PTxEQSM_EQENM_PEVAL_1	RX_REE_PTxEQSM_EQENM_PEVAL_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-694. RX_REE_PTxEQSM_PEVAL_TMR_RX_REE_PTxEQSM_EQENM_PEVAL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_PTxEQSM_PEVAL_TMR_15_0	R/W	0h	Run post evaluation equalization timer value : This specifies number of clock cycles the state machine will wait in the Post Evaluation Equalization state.
15	RX_REE_PTxEQSM_EQENM_PEVAL_15	R/W	0h	Reserved - spare
14	RX_REE_PTxEQSM_EQENM_PEVAL_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
13	RX_REE_PTxEQSM_EQENM_PEVAL_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.

Table 12-694. RX_REE_PTxEQSM_PEVAL_TMR_RX_REE_PTxEQSM_EQENM_PEVAL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_PTxEQSM_EQENM_PEVAL_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
11	RX_REE_PTxEQSM_EQENM_PEVAL_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
10	RX_REE_PTxEQSM_EQENM_PEVAL_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the TX equalization general control state machine is controlling the REE.
9	RX_REE_PTxEQSM_EQENM_PEVAL_9	R/W	0h	RX attenuation : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
8	RX_REE_PTxEQSM_EQENM_PEVAL_8	R/W	0h	RX VGA gain : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
7	RX_REE_PTxEQSM_EQENM_PEVAL_7	R/W	0h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
6	RX_REE_PTxEQSM_EQENM_PEVAL_6	R/W	0h	RX peaking amp gain : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
5	RX_REE_PTxEQSM_EQENM_PEVAL_5	R/W	0h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
4	RX_REE_PTxEQSM_EQENM_PEVAL_4	R/W	0h	Reserved - spare
3	RX_REE_PTxEQSM_EQENM_PEVAL_3	R/W	0h	Reserved - spare
2	RX_REE_PTxEQSM_EQENM_PEVAL_2	R/W	0h	RX tap 3 : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
1	RX_REE_PTxEQSM_EQENM_PEVAL_1	R/W	0h	RX tap 2 : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.
0	RX_REE_PTxEQSM_EQENM_PEVAL_0	R/W	0h	RX tap 1 : When set to 1'b1, this function is enabled when the PCIe TX equalization control state machine is controlling the REE.

Table 12-695. Register Call Summary for RX_REE_PTxEQSM_PEVAL_TMR_RX_REE_PTxEQSM_EQENM_PEVAL_j

10-G SerDes Registers

- [RX_REE_PTxEQSM_PEVAL_TMR_RX_REE_PTxEQSM_EQENM_PEVAL_j Register \(Offset = 8204h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.232 RX_REE_PTSEQSM_MAX_EVAL_CNT__RX_REE_PTSEQSM_TIMEOUT_TMR_j Register (Offset = 8208h + formula) [reset = 003F30D4h]

[RX_REE_PTSEQSM_MAX_EVAL_CNT__RX_REE_PTSEQSM_TIMEOUT_TMR_j](#) is shown in [Figure 12-232](#) and described in [Table 12-697](#).

Return to [Summary Table](#).

REE PCIe TX equalization control state machine time-out timer value register

Offset = 8208h + (j * 400h); where j = 0h to 3h

Table 12-696.
RX_REE_PTSEQSM_MAX_EVAL_CNT__RX_REE_PTSEQSM_TIMEOUT_TMR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8208h + formula

Figure 12-232. RX_REE_PTSEQSM_MAX_EVAL_CNT__RX_REE_PTSEQSM_TIMEOUT_TMR_j Register

31	30	29	28	27	26	25	24
RX_REE_PTSEQSM_MAX_EVAL_CNT_15_6							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_PTSEQSM_MAX_EVAL_CNT_15_6		RX_REE_PTSEQSM_MAX_EVAL_CNT_5_0					
R-0h				R/W-3Fh			
15	14	13	12	11	10	9	8
RX_REE_PTSEQSM_TIMEOUT_TMR_15_0							
R/W-30D4h							
7	6	5	4	3	2	1	0
RX_REE_PTSEQSM_TIMEOUT_TMR_15_0							
R/W-30D4h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-697. RX_REE_PTSEQSM_MAX_EVAL_CNT__RX_REE_PTSEQSM_TIMEOUT_TMR_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RX_REE_PTSEQSM_MAX_EVAL_CNT_15_6	R	0h	Reserved
21-16	RX_REE_PTSEQSM_MAX_EVAL_CNT_5_0	R/W	3Fh	Incremental evaluation counter load value: This is the maximum number of incremental evaluations that will be performed plus one. When the number of incremental evaluations specified here minus one are performed, the state machine will indicate that no further equalization processes are required.
15-0	RX_REE_PTSEQSM_TIMEOUT_TMR_15_0	R/W	30D4h	Time-out timer load value: This specifies the number of clocks to run a PCIe evaluation before a time-out is indicated. If a time-out takes place, the state machine will indicate that no further equalization processes are required. Note that this value is shifted left 4 bits when loading the timer, the actual time is 16X this value.

**Table 12-698. Register Call Summary for
RX_REE_PTSEQSM_MAX_EVAL_CNT_RX_REE_PTSEQSM_TIMEOUT_TMR_j**

10-G SerDes Registers

- [RX_REE_PTSEQSM_MAX_EVAL_CNT_RX_REE_PTSEQSM_TIMEOUT_TMR_j](#) Register (Offset = 8208h + formula) [reset = 003F30D4h]: [0]
- 10-G SerDes Registers: [0]

**12.233 RX_REE_GCSM1_EQENM_PH1_RX_REE_GCSM1_CTRL_j Register (Offset = 8210h + formula)
[reset = 03E70009h]**

[RX_REE_GCSM1_EQENM_PH1_RX_REE_GCSM1_CTRL_j](#) is shown in [Figure 12-233](#) and described in [Table 12-700](#).

Return to [Summary Table](#).

REE general control state machine 1 control register

Offset = 8210h + (j * 400h); where j = 0h to 3h

**Table 12-699. RX_REE_GCSM1_EQENM_PH1_RX_REE_GCSM1_CTRL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 8210h + formula

Figure 12-233. RX_REE_GCSM1_EQENM_PH1_RX_REE_GCSM1_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_GCSM1_EQENM_PH1_15	RX_REE_GCSM1_EQENM_PH1_14	RX_REE_GCSM1_EQENM_PH1_13	RX_REE_GCSM1_EQENM_PH1_12	RX_REE_GCSM1_EQENM_PH1_11	RX_REE_GCSM1_EQENM_PH1_10	RX_REE_GCSM1_EQENM_PH1_9	RX_REE_GCSM1_EQENM_PH1_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
RX_REE_GCSM1_EQENM_PH1_7	RX_REE_GCSM1_EQENM_PH1_6	RX_REE_GCSM1_EQENM_PH1_5	RX_REE_GCSM1_EQENM_PH1_4	RX_REE_GCSM1_EQENM_PH1_3	RX_REE_GCSM1_EQENM_PH1_2	RX_REE_GCSM1_EQENM_PH1_1	RX_REE_GCSM1_EQENM_PH1_0
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
RX_REE_GCSM1_CTRL_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_GCSM1_CTRL_15_4				RX_REE_GCSM1_CTRL_3	RX_REE_GCSM1_CTRL_2	RX_REE_GCSM1_CTRL_1	RX_REE_GCSM1_CTRL_0
R-0h				R/W-1h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-700. RX_REE_GCSM1_EQENM_PH1_RX_REE_GCSM1_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_GCSM1_EQENM_PH1_15	R/W	0h	Reserved - spare
30	RX_REE_GCSM1_EQENM_PH1_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
29	RX_REE_GCSM1_EQENM_PH1_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
28	RX_REE_GCSM1_EQENM_PH1_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
27	RX_REE_GCSM1_EQENM_PH1_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
26	RX_REE_GCSM1_EQENM_PH1_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
25	RX_REE_GCSM1_EQENM_PH1_9	R/W	1h	RX attenuation : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.

**Table 12-700. RX_REE_GCSM1_EQENM_PH1__RX_REE_GCSM1_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
24	RX_REE_GCSM1_EQENM_PH1_8	R/W	1h	RX VGA gain : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
23	RX_REE_GCSM1_EQENM_PH1_7	R/W	1h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
22	RX_REE_GCSM1_EQENM_PH1_6	R/W	1h	RX peaking amp gain : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
21	RX_REE_GCSM1_EQENM_PH1_5	R/W	1h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
20	RX_REE_GCSM1_EQENM_PH1_4	R/W	0h	Reserved - spare
19	RX_REE_GCSM1_EQENM_PH1_3	R/W	0h	Reserved - spare
18	RX_REE_GCSM1_EQENM_PH1_2	R/W	1h	RX tap 3 : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
17	RX_REE_GCSM1_EQENM_PH1_1	R/W	1h	RX tap 2 : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
16	RX_REE_GCSM1_EQENM_PH1_0	R/W	1h	RX tap 1 : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
15-4	RX_REE_GCSM1_CTRL_15_4	R	0h	Reserved
3	RX_REE_GCSM1_CTRL_3	R/W	1h	Equalization function reset enable: Enables the reset of the functions controlled by this state machine, using the rx_ree_fcn_reset_n signal, when the equalization mode changes. 1'b 1 : Enabled 1'b 0 : Disabled
2	RX_REE_GCSM1_CTRL_2	R/W	0h	Loop enable: Controls when the equalization functions in this state machine are run one time or loop continuously.
1	RX_REE_GCSM1_CTRL_1	R/W	0h	Force run equalization: Setting this bit to a 1'b1, will force the general control state machine to run, independent of the macro functions that normally run the equalization.
0	RX_REE_GCSM1_CTRL_0	R/W	1h	Enable: This bit enables the general control state machine function. 1'b 1 : Enabled 1'b 0 : Disabled

Table 12-701. Register Call Summary for RX_REE_GCSM1_EQENM_PH1__RX_REE_GCSM1_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_GCSM1_EQENM_PH1__RX_REE_GCSM1_CTRL_j Register \(Offset = 8210h + formula\) \[reset = 03E70009h\]: \[0\]](#)

12.234 RX_REE_GCSM1_START_TMR_RX_REE_GCSM1_EQENM_PH2_j Register (Offset = 8214h + formula) [reset = 1E7h]

RX_REE_GCSM1_START_TMR_RX_REE_GCSM1_EQENM_PH2_j is shown in Figure 12-234 and described in Table 12-703.

Return to [Summary Table](#).

REE general control state machine 1 phase 2 equalization enable mask register

Offset = 8214h + (j * 400h); where j = 0h to 3h

Table 12-702.
RX_REE_GCSM1_START_TMR_RX_REE_GCSM1_EQENM_PH2_j Instances

Instance	Physical Address
SERDES_10G0	0505 8214h + formula

Figure 12-234. RX_REE_GCSM1_START_TMR_RX_REE_GCSM1_EQENM_PH2_j Register

31	30	29	28	27	26	25	24
RX_REE_GCSM1_START_TMR_15_0							
R/W-0h							
23	22	21	20	19	18	17	16
RX_REE_GCSM1_START_TMR_15_0							
R/W-0h							
15	14	13	12	11	10	9	8
RX_REE_GCSM1_EQENM_P_H2_15	RX_REE_GCSM1_EQENM_P_H2_14	RX_REE_GCSM1_EQENM_P_H2_13	RX_REE_GCSM1_EQENM_P_H2_12	RX_REE_GCSM1_EQENM_P_H2_11	RX_REE_GCSM1_EQENM_P_H2_10	RX_REE_GCSM1_EQENM_P_H2_9	RX_REE_GCSM1_EQENM_P_H2_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RX_REE_GCSM1_EQENM_P_H2_7	RX_REE_GCSM1_EQENM_P_H2_6	RX_REE_GCSM1_EQENM_P_H2_5	RX_REE_GCSM1_EQENM_P_H2_4	RX_REE_GCSM1_EQENM_P_H2_3	RX_REE_GCSM1_EQENM_P_H2_2	RX_REE_GCSM1_EQENM_P_H2_1	RX_REE_GCSM1_EQENM_P_H2_0
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-703. RX_REE_GCSM1_START_TMR_RX_REE_GCSM1_EQENM_PH2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_GCSM1_START_TMR_15_0	R/W	0h	Start timer value : The number of clock cycles the state machine will wait in the Start Delay state. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.
15	RX_REE_GCSM1_EQENM_PH2_15	R/W	0h	Reserved - spare
14	RX_REE_GCSM1_EQENM_PH2_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
13	RX_REE_GCSM1_EQENM_PH2_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
12	RX_REE_GCSM1_EQENM_PH2_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
11	RX_REE_GCSM1_EQENM_PH2_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.

Table 12-703. RX_REE_GCSM1_START_TMR_RX_REE_GCSM1_EQENM_PH2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_REE_GCSM1_EQENM_PH2_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
9	RX_REE_GCSM1_EQENM_PH2_9	R/W	0h	RX attenuation : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
8	RX_REE_GCSM1_EQENM_PH2_8	R/W	1h	RX VGA gain : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
7	RX_REE_GCSM1_EQENM_PH2_7	R/W	1h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
6	RX_REE_GCSM1_EQENM_PH2_6	R/W	1h	RX peaking amp gain : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
5	RX_REE_GCSM1_EQENM_PH2_5	R/W	1h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
4	RX_REE_GCSM1_EQENM_PH2_4	R/W	0h	Reserved - spare
3	RX_REE_GCSM1_EQENM_PH2_3	R/W	0h	Reserved - spare
2	RX_REE_GCSM1_EQENM_PH2_2	R/W	1h	RX tap 3 : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
1	RX_REE_GCSM1_EQENM_PH2_1	R/W	1h	RX tap 2 : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.
0	RX_REE_GCSM1_EQENM_PH2_0	R/W	1h	RX tap 1 : When set to 1'b1, this function is enabled when the general control state machine 1 is controlling the REE.

Table 12-704. Register Call Summary for RX_REE_GCSM1_START_TMR_RX_REE_GCSM1_EQENM_PH2_j

10-G SerDes Registers

- [RX_REE_GCSM1_START_TMR_RX_REE_GCSM1_EQENM_PH2_j Register \(Offset = 8214h + formula\) \[reset = 1E7h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.235 RX_REE_GCSM1_RUN_PH2_TMR_RX_REE_GCSM1_RUN_PH1_TMR_j Register (Offset = 8218h + formula) [reset = 009D0F43h]

[RX_REE_GCSM1_RUN_PH2_TMR_RX_REE_GCSM1_RUN_PH1_TMR_j](#) is shown in [Figure 12-235](#) and described in [Table 12-706](#).

Return to [Summary Table](#).

REE general control state machine 1 run phase 1 timer value register

Offset = 8218h + (j * 400h); where j = 0h to 3h

Table 12-705.
RX_REE_GCSM1_RUN_PH2_TMR_RX_REE_GCSM1_RUN_PH1_TMR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8218h + formula

Figure 12-235. RX_REE_GCSM1_RUN_PH2_TMR_RX_REE_GCSM1_RUN_PH1_TMR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_REE_GCSM1_RUN_PH2_TMR_15_0															
R/W-9Dh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_REE_GCSM1_RUN_PH1_TMR_15_0															
R/W-F43h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-706. RX_REE_GCSM1_RUN_PH2_TMR_RX_REE_GCSM1_RUN_PH1_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_GCSM1_RUN_PH2_TMR_15_0	R/W	9Dh	Run phase 2 timer value : This specifies the number of clock cycles the state machine will wait in the Run Equalization Phase 2 state. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.
15-0	RX_REE_GCSM1_RUN_PH1_TMR_15_0	R/W	F43h	Run phase 1 timer value : This specifies the number of clock cycles the state machine will wait in the Run Equalization Phase 1 state. If this register is set to all 1s, the run in the Run Equalization Phase 1 state indefinitely. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.

Table 12-707. Register Call Summary for
RX_REE_GCSM1_RUN_PH2_TMR_RX_REE_GCSM1_RUN_PH1_TMR_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_GCSM1_RUN_PH2_TMR_RX_REE_GCSM1_RUN_PH1_TMR_j Register \(Offset = 8218h + formula\) \[reset = 009D0F43h\]: \[0\]](#)

12.236 RX_REE_GCSM2_EQENM_PH1_RX_REE_GCSM2_CTRL_j Register (Offset = 8220h + formula) [reset = 00800009h]

RX_REE_GCSM2_EQENM_PH1_RX_REE_GCSM2_CTRL_j is shown in Figure 12-236 and described in Table 12-709.

Return to [Summary Table](#).

REE general control state machine 2 control register

Offset = 8220h + (j * 400h); where j = 0h to 3h

Table 12-708. RX_REE_GCSM2_EQENM_PH1_RX_REE_GCSM2_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8220h + formula

Figure 12-236. RX_REE_GCSM2_EQENM_PH1_RX_REE_GCSM2_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_GCSM2_EQENM_P_H1_15	RX_REE_GCSM2_EQENM_P_H1_14	RX_REE_GCSM2_EQENM_P_H1_13	RX_REE_GCSM2_EQENM_P_H1_12	RX_REE_GCSM2_EQENM_P_H1_11	RX_REE_GCSM2_EQENM_P_H1_10	RX_REE_GCSM2_EQENM_P_H1_9	RX_REE_GCSM2_EQENM_P_H1_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RX_REE_GCSM2_EQENM_P_H1_7	RX_REE_GCSM2_EQENM_P_H1_6	RX_REE_GCSM2_EQENM_P_H1_5	RX_REE_GCSM2_EQENM_P_H1_4	RX_REE_GCSM2_EQENM_P_H1_3	RX_REE_GCSM2_EQENM_P_H1_2	RX_REE_GCSM2_EQENM_P_H1_1	RX_REE_GCSM2_EQENM_P_H1_0
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_REE_GCSM2_CTRL_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_GCSM2_CTRL_15_4				RX_REE_GCSM2_CTRL_3	RX_REE_GCSM2_CTRL_2	RX_REE_GCSM2_CTRL_1	RX_REE_GCSM2_CTRL_0
R-0h				R/W-1h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-709. RX_REE_GCSM2_EQENM_PH1_RX_REE_GCSM2_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_GCSM2_EQENM_PH1_15	R/W	0h	Reserved - spare
30	RX_REE_GCSM2_EQENM_PH1_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
29	RX_REE_GCSM2_EQENM_PH1_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
28	RX_REE_GCSM2_EQENM_PH1_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
27	RX_REE_GCSM2_EQENM_PH1_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
26	RX_REE_GCSM2_EQENM_PH1_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
25	RX_REE_GCSM2_EQENM_PH1_9	R/W	0h	RX attenuation : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.

**Table 12-709. RX_REE_GCSM2_EQENM_PH1__RX_REE_GCSM2_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
24	RX_REE_GCSM2_EQENM_PH1_8	R/W	0h	RX VGA gain : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
23	RX_REE_GCSM2_EQENM_PH1_7	R/W	1h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
22	RX_REE_GCSM2_EQENM_PH1_6	R/W	0h	RX peaking amp gain : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
21	RX_REE_GCSM2_EQENM_PH1_5	R/W	0h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
20	RX_REE_GCSM2_EQENM_PH1_4	R/W	0h	Reserved - spare
19	RX_REE_GCSM2_EQENM_PH1_3	R/W	0h	Reserved - spare
18	RX_REE_GCSM2_EQENM_PH1_2	R/W	0h	RX tap 3 : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
17	RX_REE_GCSM2_EQENM_PH1_1	R/W	0h	RX tap 2 : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
16	RX_REE_GCSM2_EQENM_PH1_0	R/W	0h	RX tap 1 : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
15-4	RX_REE_GCSM2_CTRL_15_4	R	0h	Reserved
3	RX_REE_GCSM2_CTRL_3	R/W	1h	Equalization function reset enable: Enables the reset of the functions controlled by this state machine, using the rx_ree_fcn_reset_n signal, when the equalization mode changes. 1'b 1 : Enabled 1'b 0 : Disabled
2	RX_REE_GCSM2_CTRL_2	R/W	0h	Loop enable: Controls when the equalization functions in this state machine are run one time or loop continuously.
1	RX_REE_GCSM2_CTRL_1	R/W	0h	Force run equalization: Setting this bit to a 1'b1, will force the general control state machine to run, independent of the macro functions that normally run the equalization.
0	RX_REE_GCSM2_CTRL_0	R/W	1h	Enable: This bit enables the general control state machine function. 1'b 1 : Enabled 1'b 0 : Disabled

Table 12-710. Register Call Summary for RX_REE_GCSM2_EQENM_PH1__RX_REE_GCSM2_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_GCSM2_EQENM_PH1__RX_REE_GCSM2_CTRL_j Register \(Offset = 8220h + formula\) \[reset = 00800009h\]: \[0\]](#)

12.237 RX_REE_GCSM2_START_TMR__RX_REE_GCSM2_EQENM_PH2_j Register (Offset = 8224h + formula) [reset = 0h]

RX_REE_GCSM2_START_TMR__RX_REE_GCSM2_EQENM_PH2_j is shown in Figure 12-237 and described in Table 12-712.

Return to [Summary Table](#).

REE general control state machine 2 phase 2 equalization enable mask register

Offset = 8224h + (j * 400h); where j = 0h to 3h

Table 12-711.
RX_REE_GCSM2_START_TMR__RX_REE_GCSM2_EQENM_PH2_j Instances

Instance	Physical Address
SERDES_10G0	0505 8224h + formula

Figure 12-237. RX_REE_GCSM2_START_TMR__RX_REE_GCSM2_EQENM_PH2_j Register

31	30	29	28	27	26	25	24
RX_REE_GCSM2_START_TMR_15_0							
R/W-0h							
23	22	21	20	19	18	17	16
RX_REE_GCSM2_START_TMR_15_0							
R/W-0h							
15	14	13	12	11	10	9	8
RX_REE_GCSM2_EQENM_P_H2_15	RX_REE_GCSM2_EQENM_P_H2_14	RX_REE_GCSM2_EQENM_P_H2_13	RX_REE_GCSM2_EQENM_P_H2_12	RX_REE_GCSM2_EQENM_P_H2_11	RX_REE_GCSM2_EQENM_P_H2_10	RX_REE_GCSM2_EQENM_P_H2_9	RX_REE_GCSM2_EQENM_P_H2_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_REE_GCSM2_EQENM_P_H2_7	RX_REE_GCSM2_EQENM_P_H2_6	RX_REE_GCSM2_EQENM_P_H2_5	RX_REE_GCSM2_EQENM_P_H2_4	RX_REE_GCSM2_EQENM_P_H2_3	RX_REE_GCSM2_EQENM_P_H2_2	RX_REE_GCSM2_EQENM_P_H2_1	RX_REE_GCSM2_EQENM_P_H2_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-712. RX_REE_GCSM2_START_TMR__RX_REE_GCSM2_EQENM_PH2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_GCSM2_START_TMR_15_0	R/W	0h	Start timer value : The number of clock cycles the state machine will wait in the Start Delay state. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.
15	RX_REE_GCSM2_EQENM_PH2_15	R/W	0h	Reserved - spare
14	RX_REE_GCSM2_EQENM_PH2_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
13	RX_REE_GCSM2_EQENM_PH2_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
12	RX_REE_GCSM2_EQENM_PH2_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
11	RX_REE_GCSM2_EQENM_PH2_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.

Table 12-712. RX_REE_GCSM2_START_TMR_RX_REE_GCSM2_EQENM_PH2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_REE_GCSM2_EQENM_PH2_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
9	RX_REE_GCSM2_EQENM_PH2_9	R/W	0h	RX attenuation : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
8	RX_REE_GCSM2_EQENM_PH2_8	R/W	0h	RX VGA gain : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
7	RX_REE_GCSM2_EQENM_PH2_7	R/W	0h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
6	RX_REE_GCSM2_EQENM_PH2_6	R/W	0h	RX peaking amp gain : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
5	RX_REE_GCSM2_EQENM_PH2_5	R/W	0h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
4	RX_REE_GCSM2_EQENM_PH2_4	R/W	0h	Reserved - spare
3	RX_REE_GCSM2_EQENM_PH2_3	R/W	0h	Reserved - spare
2	RX_REE_GCSM2_EQENM_PH2_2	R/W	0h	RX tap 3 : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
1	RX_REE_GCSM2_EQENM_PH2_1	R/W	0h	RX tap 2 : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.
0	RX_REE_GCSM2_EQENM_PH2_0	R/W	0h	RX tap 1 : When set to 1'b1, this function is enabled when the general control state machine 2 is controlling the REE.

Table 12-713. Register Call Summary for RX_REE_GCSM2_START_TMR_RX_REE_GCSM2_EQENM_PH2_j

10-G SerDes Registers

- [RX_REE_GCSM2_START_TMR_RX_REE_GCSM2_EQENM_PH2_j Register \(Offset = 8224h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.238 RX_REE_GCSM2_RUN_PH2_TMR_RX_REE_GCSM2_RUN_PH1_TMR_j Register (Offset = 8228h + formula) [reset = FFFFh]

[RX_REE_GCSM2_RUN_PH2_TMR_RX_REE_GCSM2_RUN_PH1_TMR_j](#) is shown in [Figure 12-238](#) and described in [Table 12-715](#).

Return to [Summary Table](#).

REE general control state machine 2 run phase 1 timer value register

Offset = 8228h + (j * 400h); where j = 0h to 3h

Table 12-714.
RX_REE_GCSM2_RUN_PH2_TMR_RX_REE_GCSM2_RUN_PH1_TMR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8228h + formula

Figure 12-238. RX_REE_GCSM2_RUN_PH2_TMR_RX_REE_GCSM2_RUN_PH1_TMR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_REE_GCSM2_RUN_PH2_TMR_15_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_REE_GCSM2_RUN_PH1_TMR_15_0															
R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-715. RX_REE_GCSM2_RUN_PH2_TMR_RX_REE_GCSM2_RUN_PH1_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_GCSM2_RUN_PH2_TMR_15_0	R/W	0h	Run phase 2 timer value : This specifies the number of clock cycles the state machine will wait in the Run Equalization Phase 2 state. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.
15-0	RX_REE_GCSM2_RUN_PH1_TMR_15_0	R/W	FFFFh	Run phase 1 timer value : This specifies the number of clock cycles the state machine will wait in the Run Equalization Phase 1 state. If this register is set to all 1s, the run in the Run Equalization Phase 1 state indefinitely. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.

Table 12-716. Register Call Summary for
RX_REE_GCSM2_RUN_PH2_TMR_RX_REE_GCSM2_RUN_PH1_TMR_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_GCSM2_RUN_PH2_TMR_RX_REE_GCSM2_RUN_PH1_TMR_j Register \(Offset = 8228h + formula\) \[reset = FFFFh\]: \[0\]](#)

12.239 RX_REE_PERGCSM_EQENM_PH1__RX_REE_PERGCSM_CTRL_j Register (Offset = 8230h + formula) [reset = 03C7000Dh]

RX_REE_PERGCSM_EQENM_PH1__RX_REE_PERGCSM_CTRL_j is shown in Figure 12-239 and described in Table 12-718.

Return to [Summary Table](#).

REE periodic general control state machine control register

Offset = 8230h + (j * 400h); where j = 0h to 3h

Table 12-717.
RX_REE_PERGCSM_EQENM_PH1__RX_REE_PERGCSM_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8230h + formula

Figure 12-239. RX_REE_PERGCSM_EQENM_PH1__RX_REE_PERGCSM_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_PERGCSM_EQENM_PH1_15	RX_REE_PERGCSM_EQENM_PH1_14	RX_REE_PERGCSM_EQENM_PH1_13	RX_REE_PERGCSM_EQENM_PH1_12	RX_REE_PERGCSM_EQENM_PH1_11	RX_REE_PERGCSM_EQENM_PH1_10	RX_REE_PERGCSM_EQENM_PH1_9	RX_REE_PERGCSM_EQENM_PH1_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
RX_REE_PERGCSM_EQENM_PH1_7	RX_REE_PERGCSM_EQENM_PH1_6	RX_REE_PERGCSM_EQENM_PH1_5	RX_REE_PERGCSM_EQENM_PH1_4	RX_REE_PERGCSM_EQENM_PH1_3	RX_REE_PERGCSM_EQENM_PH1_2	RX_REE_PERGCSM_EQENM_PH1_1	RX_REE_PERGCSM_EQENM_PH1_0
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
RX_REE_PERGCSM_CTRL_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_PERGCSM_CTRL_15_4				RX_REE_PERGCSM_CTRL_3	RX_REE_PERGCSM_CTRL_2	RX_REE_PERGCSM_CTRL_1	RX_REE_PERGCSM_CTRL_0
R-0h				R/W-1h	R/W-1h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-718. RX_REE_PERGCSM_EQENM_PH1__RX_REE_PERGCSM_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_PERGCSM_EQENM_PH1_15	R/W	0h	Reserved - spare
30	RX_REE_PERGCSM_EQENM_PH1_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
29	RX_REE_PERGCSM_EQENM_PH1_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
28	RX_REE_PERGCSM_EQENM_PH1_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
27	RX_REE_PERGCSM_EQENM_PH1_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.

Table 12-718. RX_REE_PERGCSM_EQENM_PH1_RX_REE_PERGCSM_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	RX_REE_PERGCSM_EQENM_PH1_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
25	RX_REE_PERGCSM_EQENM_PH1_9	R/W	1h	RX attenuation : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
24	RX_REE_PERGCSM_EQENM_PH1_8	R/W	1h	RX VGA gain : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
23	RX_REE_PERGCSM_EQENM_PH1_7	R/W	1h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
22	RX_REE_PERGCSM_EQENM_PH1_6	R/W	1h	RX peaking amp gain : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
21	RX_REE_PERGCSM_EQENM_PH1_5	R/W	0h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
20	RX_REE_PERGCSM_EQENM_PH1_4	R/W	0h	Reserved - spare
19	RX_REE_PERGCSM_EQENM_PH1_3	R/W	0h	Reserved - spare
18	RX_REE_PERGCSM_EQENM_PH1_2	R/W	1h	RX tap 3 : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
17	RX_REE_PERGCSM_EQENM_PH1_1	R/W	1h	RX tap 2 : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
16	RX_REE_PERGCSM_EQENM_PH1_0	R/W	1h	RX tap 1 : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
15-4	RX_REE_PERGCSM_CTL_15_4	R	0h	Reserved
3	RX_REE_PERGCSM_CTL_3	R/W	1h	Equalization function reset enable: Enables the reset of the functions controlled by this state machine, using the rx_ree_fcn_reset_n pin, when the equalization mode changes. 1'b 1 : Enabled 1'b 0 : Disabled
2	RX_REE_PERGCSM_CTL_2	R/W	1h	Loop enable: Controls when the equalization functions in this state machine are run one time or loop continuously.
1	RX_REE_PERGCSM_CTL_1	R/W	0h	Force run equalization: Setting this bit to a 1'b1, will force the general control state machine to run, independent of the macro functions that normally run the equalization.
0	RX_REE_PERGCSM_CTL_0	R/W	1h	Enable: This bit enables the general control state machine function. 1'b 1 : Enabled 1'b 0 : Disabled

Table 12-719. Register Call Summary for RX_REE_PERGCSM_EQENM_PH1_RX_REE_PERGCSM_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_PERGCSM_EQENM_PH1_RX_REE_PERGCSM_CTRL_j Register \(Offset = 8230h + formula\) \[reset = 03C7000Dh\]: \[0\]](#)

12.240 RX_REE_PERGCSM_START_TMR_RX_REE_PERGCSM_EQENM_PH2_j Register (Offset = 8234h + formula) [reset = 1E8501C7h]

RX_REE_PERGCSM_START_TMR_RX_REE_PERGCSM_EQENM_PH2_j is shown in Figure 12-240 and described in Table 12-721.

Return to [Summary Table](#).

REE periodic general control state machine phase 2 equalization enable mask register

Offset = 8234h + (j * 400h); where j = 0h to 3h

Table 12-720.
RX_REE_PERGCSM_START_TMR_RX_REE_PERGCSM_EQENM_PH2_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8234h + formula

Figure 12-240. RX_REE_PERGCSM_START_TMR_RX_REE_PERGCSM_EQENM_PH2_j Register

31	30	29	28	27	26	25	24
RX_REE_PERGCSM_START_TMR_15_0							
R/W-1E85h							
23	22	21	20	19	18	17	16
RX_REE_PERGCSM_START_TMR_15_0							
R/W-1E85h							
15	14	13	12	11	10	9	8
RX_REE_PERGCSM_EQENM_PH2_15	RX_REE_PERGCSM_EQENM_PH2_14	RX_REE_PERGCSM_EQENM_PH2_13	RX_REE_PERGCSM_EQENM_PH2_12	RX_REE_PERGCSM_EQENM_PH2_11	RX_REE_PERGCSM_EQENM_PH2_10	RX_REE_PERGCSM_EQENM_PH2_9	RX_REE_PERGCSM_EQENM_PH2_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RX_REE_PERGCSM_EQENM_PH2_7	RX_REE_PERGCSM_EQENM_PH2_6	RX_REE_PERGCSM_EQENM_PH2_5	RX_REE_PERGCSM_EQENM_PH2_4	RX_REE_PERGCSM_EQENM_PH2_3	RX_REE_PERGCSM_EQENM_PH2_2	RX_REE_PERGCSM_EQENM_PH2_1	RX_REE_PERGCSM_EQENM_PH2_0
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-721. RX_REE_PERGCSM_START_TMR_RX_REE_PERGCSM_EQENM_PH2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_PERGCSM_START_TMR_15_0	R/W	1E85h	Start timer value : The number of clock cycles the state machine will wait in the Start Delay state. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.
15	RX_REE_PERGCSM_EQENM_PH2_15	R/W	0h	Reserved - spare
14	RX_REE_PERGCSM_EQENM_PH2_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
13	RX_REE_PERGCSM_EQENM_PH2_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.

Table 12-721. RX_REE_PERGCSM_START_TMR_RX_REE_PERGCSM_EQENM_PH2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_PERGCSM_EQENM_PH2_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
11	RX_REE_PERGCSM_EQENM_PH2_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
10	RX_REE_PERGCSM_EQENM_PH2_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
9	RX_REE_PERGCSM_EQENM_PH2_9	R/W	0h	RX attenuation : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
8	RX_REE_PERGCSM_EQENM_PH2_8	R/W	1h	RX VGA gain : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
7	RX_REE_PERGCSM_EQENM_PH2_7	R/W	1h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
6	RX_REE_PERGCSM_EQENM_PH2_6	R/W	1h	RX peaking amp gain : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
5	RX_REE_PERGCSM_EQENM_PH2_5	R/W	0h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
4	RX_REE_PERGCSM_EQENM_PH2_4	R/W	0h	Reserved - spare
3	RX_REE_PERGCSM_EQENM_PH2_3	R/W	0h	Reserved - spare
2	RX_REE_PERGCSM_EQENM_PH2_2	R/W	1h	RX tap 3 : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
1	RX_REE_PERGCSM_EQENM_PH2_1	R/W	1h	RX tap 2 : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.
0	RX_REE_PERGCSM_EQENM_PH2_0	R/W	1h	RX tap 1 : When set to 1'b1, this function is enabled when the periodic general control state machine is controlling the REE.

Table 12-722. Register Call Summary for RX_REE_PERGCSM_START_TMR_RX_REE_PERGCSM_EQENM_PH2_j

10-G SerDes Registers

- [RX_REE_PERGCSM_START_TMR_RX_REE_PERGCSM_EQENM_PH2_j Register \(Offset = 8234h + formula\) \[reset = 1E8501C7h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.241 RX_REE_PERGCSM_RUN_PH2_TMR_RX_REE_PERGCSM_RUN_PH1_TMR_j Register (Offset = 8238h + formula) [reset = 009D009Dh]

[RX_REE_PERGCSM_RUN_PH2_TMR_RX_REE_PERGCSM_RUN_PH1_TMR_j](#) is shown in [Figure 12-241](#) and described in [Table 12-724](#).

Return to [Summary Table](#).

REE periodic general control state machine run phase 1 timer value register

Offset = 8238h + (j * 400h); where j = 0h to 3h

Table 12-723.
RX_REE_PERGCSM_RUN_PH2_TMR_RX_REE_PERGCSM_RUN_PH1_TMR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8238h + formula

Figure 12-241. RX_REE_PERGCSM_RUN_PH2_TMR_RX_REE_PERGCSM_RUN_PH1_TMR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_REE_PERGCSM_RUN_PH2_TMR_15_0															
R/W-9Dh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_REE_PERGCSM_RUN_PH1_TMR_15_0															
R/W-9Dh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-724. RX_REE_PERGCSM_RUN_PH2_TMR_RX_REE_PERGCSM_RUN_PH1_TMR_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_PERGCSM_RUN_PH2_TMR_15_0	R/W	9Dh	Run phase 2 timer value : This specifies the number of clock cycles the state machine will wait in the Run Equalization Phase 2 state. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.
15-0	RX_REE_PERGCSM_RUN_PH1_TMR_15_0	R/W	9Dh	Run phase 1 timer value : This specifies the number of clock cycles the state machine will wait in the Run Equalization Phase 1 state. If this register is set to all 1s, the run in the Run Equalization Phase 1 state indefinitely. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.

Table 12-725. Register Call Summary for
RX_REE_PERGCSM_RUN_PH2_TMR_RX_REE_PERGCSM_RUN_PH1_TMR_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_PERGCSM_RUN_PH2_TMR_RX_REE_PERGCSM_RUN_PH1_TMR_j Register \(Offset = 8238h + formula\) \[reset = 009D009Dh\]: \[0\]](#)

12.242 RX_REE_U3GCSM_EQENM_PH1_RX_REE_U3GCSM_CTRL_j Register (Offset = 8240h + formula) [reset = 03C70009h]

RX_REE_U3GCSM_EQENM_PH1_RX_REE_U3GCSM_CTRL_j is shown in Figure 12-242 and described in Table 12-727.

Return to [Summary Table](#).

REE USB 3 general control state machine control register

Offset = 8240h + (j * 400h); where j = 0h to 3h

Table 12-726. RX_REE_U3GCSM_EQENM_PH1_RX_REE_U3GCSM_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8240h + formula

Figure 12-242. RX_REE_U3GCSM_EQENM_PH1_RX_REE_U3GCSM_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_U3GCSM_EQENM_PH1_15	RX_REE_U3GCSM_EQENM_PH1_14	RX_REE_U3GCSM_EQENM_PH1_13	RX_REE_U3GCSM_EQENM_PH1_12	RX_REE_U3GCSM_EQENM_PH1_11	RX_REE_U3GCSM_EQENM_PH1_10	RX_REE_U3GCSM_EQENM_PH1_9	RX_REE_U3GCSM_EQENM_PH1_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h
23	22	21	20	19	18	17	16
RX_REE_U3GCSM_EQENM_PH1_7	RX_REE_U3GCSM_EQENM_PH1_6	RX_REE_U3GCSM_EQENM_PH1_5	RX_REE_U3GCSM_EQENM_PH1_4	RX_REE_U3GCSM_EQENM_PH1_3	RX_REE_U3GCSM_EQENM_PH1_2	RX_REE_U3GCSM_EQENM_PH1_1	RX_REE_U3GCSM_EQENM_PH1_0
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
RX_REE_U3GCSM_CTRL_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_U3GCSM_CTRL_15_4				RX_REE_U3GCSM_CTRL_3	RX_REE_U3GCSM_CTRL_2	RX_REE_U3GCSM_CTRL_1	RX_REE_U3GCSM_CTRL_0
R-0h				R/W-1h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-727. RX_REE_U3GCSM_EQENM_PH1_RX_REE_U3GCSM_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_U3GCSM_EQENM_PH1_15	R/W	0h	Reserved - spare
30	RX_REE_U3GCSM_EQENM_PH1_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
29	RX_REE_U3GCSM_EQENM_PH1_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
28	RX_REE_U3GCSM_EQENM_PH1_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
27	RX_REE_U3GCSM_EQENM_PH1_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.

Table 12-727. RX_REE_U3GCSM_EQENM_PH1__RX_REE_U3GCSM_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	RX_REE_U3GCSM_EQE NM_PH1_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
25	RX_REE_U3GCSM_EQE NM_PH1_9	R/W	1h	RX attenuation : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
24	RX_REE_U3GCSM_EQE NM_PH1_8	R/W	1h	RX VGA gain : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
23	RX_REE_U3GCSM_EQE NM_PH1_7	R/W	1h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
22	RX_REE_U3GCSM_EQE NM_PH1_6	R/W	1h	RX peaking amp gain : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
21	RX_REE_U3GCSM_EQE NM_PH1_5	R/W	0h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
20	RX_REE_U3GCSM_EQE NM_PH1_4	R/W	0h	Reserved - spare
19	RX_REE_U3GCSM_EQE NM_PH1_3	R/W	0h	Reserved - spare
18	RX_REE_U3GCSM_EQE NM_PH1_2	R/W	1h	RX tap 3 : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
17	RX_REE_U3GCSM_EQE NM_PH1_1	R/W	1h	RX tap 2 : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
16	RX_REE_U3GCSM_EQE NM_PH1_0	R/W	1h	RX tap 1 : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
15-4	RX_REE_U3GCSM_CTR L_15_4	R	0h	Reserved
3	RX_REE_U3GCSM_CTR L_3	R/W	1h	Equalization function reset enable: Enables the reset of the functions controlled by this state machine, using the rx_ree_fcn_reset_n pin, when the equalization mode changes. 1'b 1 : Enabled 1'b 0 : Disabled
2	RX_REE_U3GCSM_CTR L_2	R/W	0h	Loop enable: Controls when the equalization functions in this state machine are run one time or loop continuously.
1	RX_REE_U3GCSM_CTR L_1	R/W	0h	Force run equalization: Setting this bit to a 1'b1, will force the general control state machine to run, independent of the macro functions that normally run the equalization.
0	RX_REE_U3GCSM_CTR L_0	R/W	1h	Enable: This bit enables the general control state machine function. 1'b 1 : Enabled 1'b 0 : Disabled

Table 12-728. Register Call Summary for RX_REE_U3GCSM_EQENM_PH1__RX_REE_U3GCSM_CTRL_j

10-G SerDes Registers

- [RX_REE_U3GCSM_EQENM_PH1__RX_REE_U3GCSM_CTRL_j Register \(Offset = 8240h + formula\) \[reset = 03C70009h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.243 RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j Register (Offset = 8244h + formula) [reset = 012501C7h]

RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j is shown in Figure 12-243 and described in Table 12-730.

Return to [Summary Table](#).

REE USB 3 general control state machine phase 2 equalization enable mask register

Offset = 8244h + (j * 400h); where j = 0h to 3h

Table 12-729.
RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8244h + formula

Figure 12-243. RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j Register

31	30	29	28	27	26	25	24
RX_REE_U3GCSM_START_TMR_15_0							
R/W-125h							
23	22	21	20	19	18	17	16
RX_REE_U3GCSM_START_TMR_15_0							
R/W-125h							
15	14	13	12	11	10	9	8
RX_REE_U3GCSM_EQENM_PH2_15	RX_REE_U3GCSM_EQENM_PH2_14	RX_REE_U3GCSM_EQENM_PH2_13	RX_REE_U3GCSM_EQENM_PH2_12	RX_REE_U3GCSM_EQENM_PH2_11	RX_REE_U3GCSM_EQENM_PH2_10	RX_REE_U3GCSM_EQENM_PH2_9	RX_REE_U3GCSM_EQENM_PH2_8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RX_REE_U3GCSM_EQENM_PH2_7	RX_REE_U3GCSM_EQENM_PH2_6	RX_REE_U3GCSM_EQENM_PH2_5	RX_REE_U3GCSM_EQENM_PH2_4	RX_REE_U3GCSM_EQENM_PH2_3	RX_REE_U3GCSM_EQENM_PH2_2	RX_REE_U3GCSM_EQENM_PH2_1	RX_REE_U3GCSM_EQENM_PH2_0
R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-730. RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_U3GCSM_START_TMR_15_0	R/W	125h	Start timer value : The number of clock cycles the state machine will wait in the Start Delay state. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.
15	RX_REE_U3GCSM_EQENM_PH2_15	R/W	0h	Reserved - spare
14	RX_REE_U3GCSM_EQENM_PH2_14	R/W	0h	Ignore 1010 controller : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
13	RX_REE_U3GCSM_EQENM_PH2_13	R/W	0h	TX equalization evaluator : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.

Table 12-730. RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_U3GCSM_EQE NM_PH2_12	R/W	0h	TX post cursor control : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
11	RX_REE_U3GCSM_EQE NM_PH2_11	R/W	0h	TX pre cursor control : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
10	RX_REE_U3GCSM_EQE NM_PH2_10	R/W	0h	Short channel correction : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
9	RX_REE_U3GCSM_EQE NM_PH2_9	R/W	0h	RX attenuation : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
8	RX_REE_U3GCSM_EQE NM_PH2_8	R/W	1h	RX VGA gain : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
7	RX_REE_U3GCSM_EQE NM_PH2_7	R/W	1h	RX offset correction coefficient : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
6	RX_REE_U3GCSM_EQE NM_PH2_6	R/W	1h	RX peaking amp gain : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
5	RX_REE_U3GCSM_EQE NM_PH2_5	R/W	0h	RX low frequency equalizer adaptive control : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
4	RX_REE_U3GCSM_EQE NM_PH2_4	R/W	0h	Reserved - spare
3	RX_REE_U3GCSM_EQE NM_PH2_3	R/W	0h	Reserved - spare
2	RX_REE_U3GCSM_EQE NM_PH2_2	R/W	1h	RX tap 3 : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
1	RX_REE_U3GCSM_EQE NM_PH2_1	R/W	1h	RX tap 2 : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.
0	RX_REE_U3GCSM_EQE NM_PH2_0	R/W	1h	RX tap 1 : When set to 1'b1, this function is enabled when the USB 3.0 general control state machine is controlling the REE.

**Table 12-731. Register Call Summary for
RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j**

10-G SerDes Registers

- [RX_REE_U3GCSM_START_TMR_RX_REE_U3GCSM_EQENM_PH2_j Register \(Offset = 8244h + formula\) \[reset = 012501C7h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.244 RX_REE_U3GCSM_RUN_PH2_TMR_RX_REE_U3GCSM_RUN_PH1_TMR_j Register (Offset = 8248h + formula) [reset = 009D07A2h]

[RX_REE_U3GCSM_RUN_PH2_TMR_RX_REE_U3GCSM_RUN_PH1_TMR_j](#) is shown in [Figure 12-244](#) and described in [Table 12-733](#).

Return to [Summary Table](#).

REE USB 3 general control state machine run phase 1 timer value register

Offset = 8248h + (j * 400h); where j = 0h to 3h

Table 12-732.
RX_REE_U3GCSM_RUN_PH2_TMR_RX_REE_U3GCSM_RUN_PH1_TMR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8248h + formula

Figure 12-244. RX_REE_U3GCSM_RUN_PH2_TMR_RX_REE_U3GCSM_RUN_PH1_TMR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_REE_U3GCSM_RUN_PH2_TMR_15_0															
R/W-9Dh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_REE_U3GCSM_RUN_PH1_TMR_15_0															
R/W-7A2h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-733. RX_REE_U3GCSM_RUN_PH2_TMR_RX_REE_U3GCSM_RUN_PH1_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_REE_U3GCSM_RUN_PH2_TMR_15_0	R/W	9Dh	Run phase 2 timer value : This specifies the number of clock cycles the state machine will wait in the Run Equalization Phase 2 state. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.
15-0	RX_REE_U3GCSM_RUN_PH1_TMR_15_0	R/W	7A2h	Run phase 1 timer value : This specifies the number of clock cycles the state machine will wait in the Run Equalization Phase 1 state. If this register is set to all 1s, the run in the Run Equalization Phase 1 state indefinitely. Note that this value is shifted left 8 bits when loading the timer, the actual time is 256X this value.

Table 12-734. Register Call Summary for
RX_REE_U3GCSM_RUN_PH2_TMR_RX_REE_U3GCSM_RUN_PH1_TMR_j

10-G SerDes Registers

- [10-G SerDes Registers](#): [0]
- [RX_REE_U3GCSM_RUN_PH2_TMR_RX_REE_U3GCSM_RUN_PH1_TMR_j Register \(Offset = 8248h + formula\) \[reset = 009D07A2h\]](#): [0]

12.245 RX_REE_ANAENSM_DEL_TMR_j Register (Offset = 8250h + formula) [reset = X]

[RX_REE_ANAENSM_DEL_TMR_j](#) is shown in [Figure 12-245](#) and described in [Table 12-736](#).

Return to [Summary Table](#).

REE analog enable control state machine delay timer value register

Offset = 8250h + (j * 400h); where j = 0h to 3h

**Table 12-735. RX_REE_ANAENSM_DEL_TMR_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 8250h + formula

Figure 12-245. RX_REE_ANAENSM_DEL_TMR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_REE_ANAENSM_DEL_TMR_15_0															
R/W-64h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-736. RX_REE_ANAENSM_DEL_TMR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RX_REE_ANAENSM_DE L_TMR_15_0	R/W	64h	Analog enable delay timer value : The number of clock cycles the state machine will wait in the Analog Enable Delay state. The time specified here is the number of clock cycles to wait between when the analog enable signal (ana_en) is initially driven active, until the ana_en_ack signal is driven active. The intention of this timer is to provide for the necessary amount of time between when the analog enable is driven active until when data controlled by the analog enable is considered valid.

Table 12-737. Register Call Summary for RX_REE_ANAENSM_DEL_TMR_j

10-G SerDes Registers

- [RX_REE_ANAENSM_DEL_TMR_j Register \(Offset = 8250h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.246 RX_REE_TXPOST_CODE_CTRL__RX_REE_TXPOST_CTRL_j Register (Offset = 8260h + formula) [reset = 800h]

RX_REE_TXPOST_CODE_CTRL__RX_REE_TXPOST_CTRL_j is shown in Figure 12-246 and described in Table 12-739.

Return to [Summary Table](#).

REE TX post cursor control register

Offset = 8260h + (j * 400h); where j = 0h to 3h

Table 12-738. RX_REE_TXPOST_CODE_CTRL__RX_REE_TXPOST_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8260h + formula

Figure 12-246. RX_REE_TXPOST_CODE_CTRL__RX_REE_TXPOST_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_TXPOST_CODE_CTRL_15_14		RX_REE_TXPOST_CODE_CTRL_13_8					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
RX_REE_TXPOST_CODE_CTRL_7_6		RX_REE_TXPOST_CODE_CTRL_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_TXPOST_CTRL_15_12				RX_REE_TXPOST_CTRL_11	RX_REE_TXPOST_CTRL_10_8		
R-0h				R/W-1h	R/W-0h		
7	6	5	4	3	2	1	0
RX_REE_TXPOST_CTRL_7	RX_REE_TXPOST_CTRL_6_4			RX_REE_TXPOST_CTRL_3_0			
R-0h	R/W-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-739. RX_REE_TXPOST_CODE_CTRL__RX_REE_TXPOST_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_REE_TXPOST_CODE_CTRL_15_14	R	0h	Reserved
29-24	RX_REE_TXPOST_CODE_CTRL_13_8	R/W	0h	Peaking amp code maximum value: This is the maximum value that the peaking amp code will be allowed to increase to. Note: This function is unused in the TX post-cursor control.
23-22	RX_REE_TXPOST_CODE_CTRL_7_6	R	0h	Reserved
21-16	RX_REE_TXPOST_CODE_CTRL_5_0	R/W	0h	Peaking amp initial code: Initial value the peaking amp code is set to when training starts. Note: This function is unused in the TX post-cursor control.
15-12	RX_REE_TXPOST_CTRL_15_12	R	0h	Reserved
11	RX_REE_TXPOST_CTRL_11	R/W	1h	Peaking amp feedback path enable: Enables the peaking amp feedback path.

**Table 12-739. RX_REE_TXPOST_CODE_CTRL_RX_REE_TXPOST_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
10-8	RX_REE_TXPOST_CTRL_10_8	R/W	0h	Peaking amp feedback scaler value: Specifies the amount to scale the peaking amp feedback by. The following are the valid settings for this signal: 3'b 110 : /4 3'b 111 : /2 3'b 000 : x1 3'b 001 : x2 3'b 010 : x4
7	RX_REE_TXPOST_CTRL_7	R	0h	Reserved
6-4	RX_REE_TXPOST_CTRL_6_4	R/W	0h	Peaking amp integrator accumulator scaler value: Specifies the amount to scale the input to the peaking amp integrator accumulator by. The following are the valid settings for this field: 3'b 000: x1 3'b 001: x2 3'b 010: x4 3'b 011: x8 3'b 100: x16 3'b 101 - 3'b 111: Reserved Note: This function is unused in the TX post-cursor control.
3-0	RX_REE_TXPOST_CTRL_3_0	R/W	0h	Peaking amp sigma delta accumulator scaler value: Specifies the amount to scale the input to the peaking amp sigma delta accumulator by. The following are the valid settings for this field: 4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768

Table 12-740. Register Call Summary for RX_REE_TXPOST_CODE_CTRL_RX_REE_TXPOST_CTRL_j

10-G SerDes Registers

- [RX_REE_TXPOST_CODE_CTRL_RX_REE_TXPOST_CTRL_j Register \(Offset = 8260h + formula\) \[reset = 800h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.247 RX_REE_TXPOST_LTHR__RX_REE_TXPOST_UTHR_j Register (Offset = 8264h + formula) [reset = 00060008h]

RX_REE_TXPOST_LTHR__RX_REE_TXPOST_UTHR_j is shown in Figure 12-247 and described in Table 12-742.

Return to [Summary Table](#).

REE TX post cursor upper threshold register

Offset = 8264h + (j * 400h); where j = 0h to 3h

Table 12-741. RX_REE_TXPOST_LTHR__RX_REE_TXPOST_UTHR_j Instances

Instance	Physical Address
SERDES_10G0	0505 8264h + formula

Figure 12-247. RX_REE_TXPOST_LTHR__RX_REE_TXPOST_UTHR_j Register

31	30	29	28	27	26	25	24
RX_REE_TXPOST_LTHR_15_9							RX_REE_TXP OST_LTHR_8_ 0
R-0h							R/W-6h
23	22	21	20	19	18	17	16
RX_REE_TXPOST_LTHR_8_0							
R/W-6h							
15	14	13	12	11	10	9	8
RX_REE_TXPOST_UTHR_15_9							RX_REE_TXP OST_UTHR_8_ 0
R-0h							R/W-8h
7	6	5	4	3	2	1	0
RX_REE_TXPOST_UTHR_8_0							
R/W-8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-742. RX_REE_TXPOST_LTHR__RX_REE_TXPOST_UTHR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RX_REE_TXPOST_LTHR_15_9	R	0h	Reserved
24-16	RX_REE_TXPOST_LTHR_8_0	R/W	6h	Peaking amp algorithm lower threshold: This is the lower threshold value used in the peaking amp algorithm.
15-9	RX_REE_TXPOST_UTHR_15_9	R	0h	Reserved
8-0	RX_REE_TXPOST_UTHR_8_0	R/W	8h	Peaking amp algorithm upper threshold: This is the upper threshold value used in the peaking amp algorithm.

Table 12-743. Register Call Summary for RX_REE_TXPOST_LTHR__RX_REE_TXPOST_UTHR_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_TXPOST_LTHR__RX_REE_TXPOST_UTHR_j Register \(Offset = 8264h + formula\) \[reset = 00060008h\]: \[0\]](#)

12.248 RX_REE_TXPOST_COVRD0__RX_REE_TXPOST_IOVRD_j Register (Offset = 8268h + formula) [reset = 0h]

RX_REE_TXPOST_COVRD0__RX_REE_TXPOST_IOVRD_j is shown in Figure 12-248 and described in Table 12-745.

Return to [Summary Table](#).

REE TX post cursor input override register

Offset = 8268h + (j * 400h); where j = 0h to 3h

**Table 12-744. RX_REE_TXPOST_COVRD0__RX_REE_TXPOST_IOVRD_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 8268h + formula

Figure 12-248. RX_REE_TXPOST_COVRD0__RX_REE_TXPOST_IOVRD_j Register

31	30	29	28	27	26	25	24
RX_REE_TXPOST_COVRD0_15_14		RX_REE_TXPOST_COVRD0_13_8					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
RX_REE_TXPOST_COVRD0_7_6		RX_REE_TXPOST_COVRD0_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_TXPOST_IOVRD_15_5		RX_REE_TXPOST_IOVRD_14_8					
R/W-0h		R-0h					
7	6	5	4	3	2	1	0
RX_REE_TXPOST_IOVRD_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-745. RX_REE_TXPOST_COVRD0__RX_REE_TXPOST_IOVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_REE_TXPOST_COVRD0_15_14	R	0h	Reserved
29-24	RX_REE_TXPOST_COVRD0_13_8	R/W	0h	Peaking amp code override value mode 1: Value that will override the peaking amp code when in standard mode 1 when the peaking amp code override enable bit in the REE TX post cursor diagnostics register on page 259 is active.
23-22	RX_REE_TXPOST_COVRD0_7_6	R	0h	Reserved
21-16	RX_REE_TXPOST_COVRD0_5_0	R/W	0h	Peaking amp code override value mode 0: Value that will override the peaking amp code when in standard mode 0 when the peaking amp code override enable bit in the REE TX post cursor diagnostics register on page 259 is active.
15	RX_REE_TXPOST_IOVRD_15	R/W	0h	Peaking amp tap accumulator input override enable: Setting this bit to a 1'b1 will allow the tap accumulator input in the peaking amp gain algorithm to be overridden by the peaking amp tap accumulator input override field in this register. Note: This function is unused in the TX post-cursor control.

Table 12-745. RX_REE_TXPOST_COVRD0__RX_REE_TXPOST_IOVRD_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-8	RX_REE_TXPOST_IOVRD_14_8	R	0h	Reserved
7-0	RX_REE_TXPOST_IOVRD_7_0	R/W	0h	Peaking amp tap accumulator input override : Value that will override the tap accumulator input in the peaking amp gain algorithm, when the Peaking amp tap accumulator input override enable bit is active. Note: This function is unused in the TX post-cursor control.

Table 12-746. Register Call Summary for RX_REE_TXPOST_COVRD0__RX_REE_TXPOST_IOVRD_j

10-G SerDes Registers

- [RX_REE_TXPOST_COVRD0__RX_REE_TXPOST_IOVRD_j Register \(Offset = 8268h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.249 RX_REE_TXPOST_DIAG__RX_REE_TXPOST_COVRD1_j Register (Offset = 826Ch + formula) [reset = 0h]

RX_REE_TXPOST_DIAG__RX_REE_TXPOST_COVRD1_j is shown in Figure 12-249 and described in Table 12-748.

Return to [Summary Table](#).

REE TX post cursor code override 1 register

Offset = 826Ch + (j * 400h); where j = 0h to 3h

**Table 12-747. RX_REE_TXPOST_DIAG__RX_REE_TXPOST_COVRD1_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 826Ch + formula

Figure 12-249. RX_REE_TXPOST_DIAG__RX_REE_TXPOST_COVRD1_j Register

31	30	29	28	27	26	25	24
RX_REE_TXP OST_DIAG_15	RX_REE_TXP OST_DIAG_14	RX_REE_TXP OST_DIAG_13	RX_REE_TXP OST_DIAG_12	RX_REE_TXPOST_DIAG_11_8			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
RX_REE_TXPOST_DIAG_7_6		RX_REE_TXPOST_DIAG_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RX_REE_TXPOST_COVRD1_15_14		RX_REE_TXPOST_COVRD1_13_8					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
RX_REE_TXPOST_COVRD1_7_6		RX_REE_TXPOST_COVRD1_5_0					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-748. RX_REE_TXPOST_DIAG__RX_REE_TXPOST_COVRD1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_TXPOST_DIAG_15	R/W	0h	Peaking amp code override enable: Setting this bit to a 1'b1 will allow the peaking amp code to be overridden by the peaking amp code override value fields in the REE TX post cursor code override 0 register on page 258 and REE TX post cursor code override 1 register on page 259.
30	RX_REE_TXPOST_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the peaking amp voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

**Table 12-748. RX_REE_TXPOST_DIAG__RX_REE_TXPOST_COVRD1_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
29	RX_REE_TXPOST_DIAG_13	R/W	0h	Voter override pos : Writing a 1'b1 in this register bit will force the peaking amp voter function to activate the voter pos signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.
28	RX_REE_TXPOST_DIAG_12	R/W	0h	Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter in the peaking amp. Note : This function is intended to be for diagnostic and verification purposes only. Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.
27-24	RX_REE_TXPOST_DIAG_11_8	R	0h	Reserved
23-22	RX_REE_TXPOST_DIAG_7_6	R	0h	Reserved
21-16	RX_REE_TXPOST_DIAG_5_0	R	0h	Current peaking amp integrator accumulator: Current value of the tap integrator accumulator, without the unused sign bit.
15-14	RX_REE_TXPOST_COVRD1_15_14	R	0h	Reserved
13-8	RX_REE_TXPOST_COVRD1_13_8	R/W	0h	Peaking amp code override value mode 3: Value that will override the peaking amp code when in standard mode 3 when the peaking amp code override enable bit in the REE TX post cursor diagnostics register on page 259 is active.
7-6	RX_REE_TXPOST_COVRD1_7_6	R	0h	Reserved
5-0	RX_REE_TXPOST_COVRD1_5_0	R/W	0h	Peaking amp code override value mode 2: Value that will override the peaking amp code when in standard mode 2 when the peaking amp code override enable bit in the REE TX post cursor diagnostics register on page 259 is active.

Table 12-749. Register Call Summary for RX_REE_TXPOST_DIAG__RX_REE_TXPOST_COVRD1_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_TXPOST_DIAG__RX_REE_TXPOST_COVRD1_j Register \(Offset = 826Ch + formula\) \[reset = 0h\]: \[0\]](#)

12.250 RX_REE_TXPRE_OVRD_RX_REE_TXPRE_CTRL_j Register (Offset = 8270h + formula) [reset = D00h]

RX_REE_TXPRE_OVRD_RX_REE_TXPRE_CTRL_j is shown in Figure 12-250 and described in Table 12-751.

Return to [Summary Table](#).

REE TX pre cursor control register

Offset = 8270h + (j * 400h); where j = 0h to 3h

Table 12-750. RX_REE_TXPRE_OVRD_RX_REE_TXPRE_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8270h + formula

Figure 12-250. RX_REE_TXPRE_OVRD_RX_REE_TXPRE_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_TXPRE_OVRD_15_8							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_TXPRE_OVRD_7	RX_REE_TXPRE_OVRD_6	RX_REE_TXPRE_OVRD_5_0					
R/W-0h	R-0h	R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_TXPRE_CTRL_15_12				RX_REE_TXPRE_CTRL_11	RX_REE_TXPRE_CTRL_10	RX_REE_TXPRE_CTRL_9	RX_REE_TXPRE_CTRL_8
R-0h				R/W-1h	R/W-1h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RX_REE_TXPRE_CTRL_7	RX_REE_TXPRE_CTRL_6_4			RX_REE_TXPRE_CTRL_3_0			
R-0h	R/W-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-751. RX_REE_TXPRE_OVRD_RX_REE_TXPRE_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_REE_TXPRE_OVRD_15_8	R	0h	Reserved
23	RX_REE_TXPRE_OVRD_7	R/W	0h	Tap override enable: Setting this bit to a 1'b1 will enable the tap override field in this register to override the tap integrator accumulator functions. Note: This function is unused in the TX pre-cursor control.
22	RX_REE_TXPRE_OVRD_6	R	0h	Reserved
21-16	RX_REE_TXPRE_OVRD_5_0	R/W	0h	Tap override value: When the tap override enable bit in this register is active, the value in this field will override the integrator accumulator value, as well as the input to the binary to thermometer encoder. Note: This function is unused in the TX pre-cursor control.
15-12	RX_REE_TXPRE_CTRL_15_12	R	0h	Reserved
11	RX_REE_TXPRE_CTRL_11	R/W	1h	Tap coefficient combinational logic zero crossing enable: 1'b 0: Zero crossing combinational logic input not enabled. 1'b 1: Zero crossing combinational logic input enabled.

Table 12-751. RX_REE_TXPRE_OVRD__RX_REE_TXPRE_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_REE_TXPRE_CTRL_10	R/W	1h	Tap coefficient combinational logic non zero crossing enable: 1'b 0: non zero crossing combinational logic input not enabled. 1'b 1: non zero crossing combinational logic input enabled.
9	RX_REE_TXPRE_CTRL_9	R/W	0h	Tap coefficient combinational logic bit 0 only enable: 1'b 0: All enabled combinational logic input modules will be used. 1'b 1: Only the enabled combinational logic input modules associated with bit 0 will be used.
8	RX_REE_TXPRE_CTRL_8	R/W	1h	Receiver DFE tap coefficient disable: This bit disables the rxda_dfe_tap_coef output signal. 1'b 0 : rxda_dfe_tap_coef output enabled. 1'b 1 : rxda_dfe_tap_coef output disabled (all 0s). Note: This function is unused in the TX pre-cursor control.
7	RX_REE_TXPRE_CTRL_7	R	0h	Reserved
6-4	RX_REE_TXPRE_CTRL_6_4	R/W	0h	Tap integrator accumulator scaler value: Specifies the amount to scale the input to the tap integrator accumulator by. The following are the valid settings for this field: 3'b 000: x1 3'b 001 - 3'b 111: Reserved Note: This function is unused in the TX pre-cursor control.
3-0	RX_REE_TXPRE_CTRL_3_0	R/W	0h	Tap sigma delta accumulator scaler value: Specifies the amount to scale the input to the tap sigma delta accumulator by. The following are the valid settings for this field: 4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768

Table 12-752. Register Call Summary for RX_REE_TXPRE_OVRD__RX_REE_TXPRE_CTRL_j

10-G SerDes Registers

- [RX_REE_TXPRE_OVRD__RX_REE_TXPRE_CTRL_j Register \(Offset = 8270h + formula\) \[reset = D00h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.251 RX_REE_TXPRE_DIAG_j Register (Offset = 8274h + formula) [reset = X]

RX_REE_TXPRE_DIAG_j is shown in [Figure 12-251](#) and described in [Table 12-754](#).

Return to [Summary Table](#).

REE TX pre cursor diagnostics register

Offset = 8274h + (j * 400h); where j = 0h to 3h

Table 12-753. RX_REE_TXPRE_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 8274h + formula

Figure 12-251. RX_REE_TXPRE_DIAG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_REE_TXPRE_DIAG_15	RX_REE_TXPRE_DIAG_14	RX_REE_TXPRE_DIAG_13	RX_REE_TXPRE_DIAG_12	RX_REE_TXPRE_DIAG_11_6			
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
RX_REE_TXPRE_DIAG_11_6		RX_REE_TXPRE_DIAG_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-754. RX_REE_TXPRE_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RX_REE_TXPRE_DIAG_15	R	0h	Reserved
14	RX_REE_TXPRE_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the tap voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.
13	RX_REE_TXPRE_DIAG_13	R/W	0h	Voter override pos : Writing a 1'b1 in this register bit will force the tap voter function to activate the voter pos signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

Table 12-754. RX_REE_TXPRE_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_TXPRE_DIAG_12	R/W	0h	<p>Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter in the tap.</p> <p>Note : This function is intended to be for diagnostic and verification purposes only.</p> <p>Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.</p>
11-6	RX_REE_TXPRE_DIAG_11_6	R	0h	Reserved
5-0	RX_REE_TXPRE_DIAG_5_0	R	0h	Current tap integrator accumulator: Current value of the tap integrator accumulator.

Table 12-755. Register Call Summary for RX_REE_TXPRE_DIAG_j

10-G SerDes Registers

- [RX_REE_TXPRE_DIAG_j Register \(Offset = 8274h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.252 RX_REE_PEAK_CODE_CTRL_RX_REE_PEAK_CTRL_j Register (Offset = 8280h + formula) [reset = 2A200F01h]

RX_REE_PEAK_CODE_CTRL_RX_REE_PEAK_CTRL_j is shown in [Figure 12-252](#) and described in [Table 12-757](#).

Return to [Summary Table](#).

REE peaking amp control register

Offset = 8280h + (j * 400h); where j = 0h to 3h

Table 12-756. RX_REE_PEAK_CODE_CTRL_RX_REE_PEAK_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 8280h + formula

Figure 12-252. RX_REE_PEAK_CODE_CTRL_RX_REE_PEAK_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_PEAK_CODE_CTRL_15_14		RX_REE_PEAK_CODE_CTRL_13_8					
R-0h		R/W-2Ah					
23	22	21	20	19	18	17	16
RX_REE_PEAK_CODE_CTRL_7_6		RX_REE_PEAK_CODE_CTRL_5_0					
R-0h		R/W-20h					
15	14	13	12	11	10	9	8
RX_REE_PEAK_CTRL_15_12				RX_REE_PEAK_CTRL_11	RX_REE_PEAK_CTRL_10_8		
R-0h				R/W-1h	R/W-7h		
7	6	5	4	3	2	1	0
RX_REE_PEAK_CTRL_7	RX_REE_PEAK_CTRL_6_4			RX_REE_PEAK_CTRL_3_0			
R-0h	R/W-0h			R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-757. RX_REE_PEAK_CODE_CTRL_RX_REE_PEAK_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_REE_PEAK_CODE_CTRL_15_14	R	0h	Reserved
29-24	RX_REE_PEAK_CODE_CTRL_13_8	R/W	2Ah	Peaking amp code maximum value: This is the maximum value that the peaking amp code will be allowed to increase to.
23-22	RX_REE_PEAK_CODE_CTRL_7_6	R	0h	Reserved
21-16	RX_REE_PEAK_CODE_CTRL_5_0	R/W	20h	Peaking amp initial code: Initial value the peaking amp code is set to when training starts.
15-12	RX_REE_PEAK_CTRL_15_12	R	0h	Reserved
11	RX_REE_PEAK_CTRL_11	R/W	1h	Peaking amp feedback path enable: Enables the peaking amp feedback path.

**Table 12-757. RX_REE_PEAK_CODE_CTRL__RX_REE_PEAK_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
10-8	RX_REE_PEAK_CTRL_1_0_8	R/W	7h	Peaking amp feedback scaler value: Specifies the amount to scale the peaking amp feedback by. The following are the valid settings for this signal: 3'b 110 : /4 3'b 111 : /2 3'b 000 : x1 3'b 001 : x2 3'b 010 : x4
7	RX_REE_PEAK_CTRL_7	R	0h	Reserved
6-4	RX_REE_PEAK_CTRL_6_4	R/W	0h	Peaking amp integrator accumulator scaler value: Specifies the amount to scale the input to the peaking amp integrator accumulator by. The following are the valid settings for this field: 3'b 000: x1 3'b 001: x2 3'b 010: x4 3'b 011: x8 3'b 100: x16 3'b 101 - 3'b 111: Reserved
3-0	RX_REE_PEAK_CTRL_3_0	R/W	1h	Peaking amp sigma delta accumulator scaler value: Specifies the amount to scale the input to the peaking amp sigma delta accumulator by. The following are the valid settings for this field: 4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768

Table 12-758. Register Call Summary for RX_REE_PEAK_CODE_CTRL__RX_REE_PEAK_CTRL_j

10-G SerDes Registers

- [RX_REE_PEAK_CODE_CTRL__RX_REE_PEAK_CTRL_j Register \(Offset = 8280h + formula\) \[reset = 2A200F01h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.253 RX_REE_PEAK_LTHR_RX_REE_PEAK_UTHR_j Register (Offset = 8284h + formula) [reset = 01FA0004h]

[RX_REE_PEAK_LTHR_RX_REE_PEAK_UTHR_j](#) is shown in [Figure 12-253](#) and described in [Table 12-760](#).

Return to [Summary Table](#).

REE peaking amp upper threshold register

Offset = 8284h + (j * 400h); where j = 0h to 3h

Table 12-759.
RX_REE_PEAK_LTHR_RX_REE_PEAK_UTHR_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8284h + formula

Figure 12-253. RX_REE_PEAK_LTHR_RX_REE_PEAK_UTHR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_REE_PEAK_LTHR_15_9								RX_REE_PEAK_LTHR_8_0							
R-0h								R/W-1FAh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_REE_PEAK_UTHR_15_9								RX_REE_PEAK_UTHR_8_0							
R-0h								R/W-4h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-760. RX_REE_PEAK_LTHR_RX_REE_PEAK_UTHR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RX_REE_PEAK_LTHR_15_9	R	0h	Reserved
24-16	RX_REE_PEAK_LTHR_8_0	R/W	1FAh	Peaking amp algorithm lower threshold: This is the lower threshold value used in the peaking amp algorithm.
15-9	RX_REE_PEAK_UTHR_15_9	R	0h	Reserved
8-0	RX_REE_PEAK_UTHR_8_0	R/W	4h	Peaking amp algorithm upper threshold: This is the upper threshold value used in the peaking amp algorithm.

Table 12-761. Register Call Summary for RX_REE_PEAK_LTHR_RX_REE_PEAK_UTHR_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_PEAK_LTHR_RX_REE_PEAK_UTHR_j Register \(Offset = 8284h + formula\) \[reset = 01FA0004h\]: \[0\]](#)

12.254 RX_REE_PEAK_COVRD0__RX_REE_PEAK_IOVRD_j Register (Offset = 8288h + formula) [reset = 0h]

RX_REE_PEAK_COVRD0__RX_REE_PEAK_IOVRD_j is shown in Figure 12-254 and described in Table 12-763.

Return to [Summary Table](#).

REE peaking amp input override register

Offset = 8288h + (j * 400h); where j = 0h to 3h

Table 12-762. RX_REE_PEAK_COVRD0__RX_REE_PEAK_IOVRD_j Instances

Instance	Physical Address
SERDES_10G0	0505 8288h + formula

Figure 12-254. RX_REE_PEAK_COVRD0__RX_REE_PEAK_IOVRD_j Register

31	30	29	28	27	26	25	24
RX_REE_PEAK_COVRD0_15_14		RX_REE_PEAK_COVRD0_13_8					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
RX_REE_PEAK_COVRD0_7_6		RX_REE_PEAK_COVRD0_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_PEAK_IOVRD_15		RX_REE_PEAK_IOVRD_14_8					
R/W-0h		R-0h					
7	6	5	4	3	2	1	0
RX_REE_PEAK_IOVRD_7_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-763. RX_REE_PEAK_COVRD0__RX_REE_PEAK_IOVRD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_REE_PEAK_COVRD0_15_14	R	0h	Reserved
29-24	RX_REE_PEAK_COVRD0_13_8	R/W	0h	Peaking amp code override value mode 1: Value that will override the peaking amp code when in standard mode 1 when the peaking amp code override enable bit in the REE peaking amp diagnostics register on page 264 is active. The value of this override field will ultimately drive the thermometer encoded value on the rxda_dfe_peaking_amp_gain signal driven to the analog.
23-22	RX_REE_PEAK_COVRD0_7_6	R	0h	Reserved
21-16	RX_REE_PEAK_COVRD0_5_0	R/W	0h	Peaking amp code override value mode 0: Value that will override the peaking amp code when in standard mode 0 when the peaking amp code override enable bit in the REE peaking amp diagnostics register on page 264 is active. The value of this override field will ultimately drive the thermometer encoded value on the rxda_dfe_peaking_amp_gain signal driven to the analog.

**Table 12-763. RX_REE_PEAK_COVRD0__RX_REE_PEAK_IOVRD_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15	RX_REE_PEAK_IOVRD_15	R/W	0h	Peaking amp tap accumulator input override enable: Setting this bit to a 1'b1 will allow the tap accumulator input in the peaking amp gain algorithm to be overridden by the peaking amp tap accumulator input override field in this register.
14-8	RX_REE_PEAK_IOVRD_14_8	R	0h	Reserved
7-0	RX_REE_PEAK_IOVRD_7_0	R/W	0h	Peaking amp tap accumulator input override : Value that will override the tap accumulator input in the peaking amp gain algorithm, when the Peaking amp tap accumulator input override enable bit is active.

Table 12-764. Register Call Summary for RX_REE_PEAK_COVRD0__RX_REE_PEAK_IOVRD_j

10-G SerDes Registers

- [RX_REE_PEAK_COVRD0__RX_REE_PEAK_IOVRD_j Register \(Offset = 8288h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.255 RX_REE_PEAK_DIAG__RX_REE_PEAK_COVRD1_j Register (Offset = 828Ch + formula) [reset = 0h]

RX_REE_PEAK_DIAG__RX_REE_PEAK_COVRD1_j is shown in Figure 12-255 and described in Table 12-766.

Return to [Summary Table](#).

REE peaking amp code override 1 register

Offset = 828Ch + (j * 400h); where j = 0h to 3h

Table 12-765. RX_REE_PEAK_DIAG__RX_REE_PEAK_COVRD1_j Instances

Instance	Physical Address
SERDES_10G0	0505 828Ch + formula

Figure 12-255. RX_REE_PEAK_DIAG__RX_REE_PEAK_COVRD1_j Register

31	30	29	28	27	26	25	24
RX_REE_PEAK_DIAG_15	RX_REE_PEAK_DIAG_14	RX_REE_PEAK_DIAG_13	RX_REE_PEAK_DIAG_12	RX_REE_PEAK_DIAG_11_8			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
RX_REE_PEAK_DIAG_7_6		RX_REE_PEAK_DIAG_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RX_REE_PEAK_COVRD1_15_14		RX_REE_PEAK_COVRD1_13_8					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
RX_REE_PEAK_COVRD1_7_6		RX_REE_PEAK_COVRD1_5_0					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-766. RX_REE_PEAK_DIAG__RX_REE_PEAK_COVRD1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_PEAK_DIAG_15	R/W	0h	Peaking amp code override enable: Setting this bit to a 1'b1 will allow the peaking amp code to be overridden by the peaking amp code override value fields in the REE peaking amp code override 0 register on page 263 and REE peaking amp code override 1 register on page 263.
30	RX_REE_PEAK_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the peaking amp voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.
29	RX_REE_PEAK_DIAG_13	R/W	0h	Voter override pos : Writing a 1'b1 in this register bit will force the peaking amp voter function to activate the voter pos signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

Table 12-766. RX_REE_PEAK_DIAG__RX_REE_PEAK_COVRD1_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	RX_REE_PEAK_DIAG_12	R/W	0h	Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter in the peaking amp. Note : This function is intended to be for diagnostic and verification purposes only. Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.
27-24	RX_REE_PEAK_DIAG_11_8	R	0h	Reserved
23-22	RX_REE_PEAK_DIAG_7_6	R	0h	Reserved Note : n = CODE_WIDTH.
21-16	RX_REE_PEAK_DIAG_5_0	R	0h	Current peaking amp integrator accumulator: Current value of the tap integrator accumulator, without the unused sign bit. Note: The reset value for this field is with the transceiver data path power island switched off. In cases where this power island is switched on, the reset value be 6'b100000
15-14	RX_REE_PEAK_COVRD_1_15_14	R	0h	Reserved
13-8	RX_REE_PEAK_COVRD_1_13_8	R/W	0h	Peaking amp code override value mode 3: Value that will override the peaking amp code when in standard mode 3 when the peaking amp code override enable bit in the REE peaking amp diagnostics register on page 264 is active. The value of this override field will ultimately drive the thermometer encoded value on the rxda_dfe_peaking_amp_gain signal driven to the analog.
7-6	RX_REE_PEAK_COVRD_1_7_6	R	0h	Reserved
5-0	RX_REE_PEAK_COVRD_1_5_0	R/W	0h	Peaking amp code override value mode 2: Value that will override the peaking amp code when in standard mode 2 when the peaking amp code override enable bit in the REE peaking amp diagnostics register on page 264 is active. The value of this override field will ultimately drive the thermometer encoded value on the rxda_dfe_peaking_amp_gain signal driven to the analog.

Table 12-767. Register Call Summary for RX_REE_PEAK_DIAG__RX_REE_PEAK_COVRD1_j

10-G SerDes Registers

- [RX_REE_PEAK_DIAG__RX_REE_PEAK_COVRD1_j Register \(Offset = 828Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.256 RX_REE_ATTEN_THR_RX_REE_ATTEN_CTRL_j Register (Offset = 8290h + formula) [reset = 0C020005h]

RX_REE_ATTEN_THR_RX_REE_ATTEN_CTRL_j is shown in Figure 12-256 and described in Table 12-769.

Return to [Summary Table](#).

REE attenuation control register

Offset = 8290h + (j * 400h); where j = 0h to 3h

Table 12-768.
RX_REE_ATTEN_THR_RX_REE_ATTEN_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8290h + formula

Figure 12-256. RX_REE_ATTEN_THR_RX_REE_ATTEN_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_ATTEN_THR_15_13				RX_REE_ATTEN_THR_12_8			
R-0h				R/W-Ch			
23	22	21	20	19	18	17	16
RX_REE_ATTEN_THR_7_5				RX_REE_ATTEN_THR_4_0			
R-0h				R/W-2h			
15	14	13	12	11	10	9	8
RX_REE_ATTEN_CTRL_15_5							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_ATTEN_CTRL_15_5				RX_REE_ATTEN_CTRL_4_0			
R-0h				R/W-5h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-769. RX_REE_ATTEN_THR_RX_REE_ATTEN_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RX_REE_ATTEN_THR_15_13	R	0h	Reserved
28-24	RX_REE_ATTEN_THR_12_8	R/W	Ch	Attenuation high threshold value: High threshold value to compare against the VGA gain accumulator value. Note that the value on this field is not a twos complement value (There is no sign bit and it is always a positive number).
23-21	RX_REE_ATTEN_THR_7_5	R	0h	Reserved
20-16	RX_REE_ATTEN_THR_4_0	R/W	2h	Attenuation low threshold value: Low threshold value to compare against the VGA gain accumulator value. Note that the value on this field is not a twos complement value (There is no sign bit and it is always a positive number).
15-5	RX_REE_ATTEN_CTRL_15_5	R	0h	Reserved
4-0	RX_REE_ATTEN_CTRL_4_0	R/W	5h	Receiver DFE attenuation maximum value: The maximum value the rxda_dfe_attenuation_bin will increase to. Note that the value on this field is not a twos complement value (There is no sign bit and it is always a positive number).

Table 12-770. Register Call Summary for RX_REE_ATTEN_THR__RX_REE_ATTEN_CTRL_j

10-G SerDes Registers

- [RX_REE_ATTEN_THR__RX_REE_ATTEN_CTRL_j](#) Register (Offset = 8290h + formula) [reset = 0C020005h]: [0]
- 10-G SerDes Registers: [0]

12.257 RX_REE_ATTEN_OVRD__RX_REE_ATTEN_CNT_j Register (Offset = 8294h + formula) [reset = 2100h]

RX_REE_ATTEN_OVRD__RX_REE_ATTEN_CNT_j is shown in Figure 12-257 and described in Table 12-772.

Return to [Summary Table](#).

REE attenuation counter register

Offset = 8294h + (j * 400h); where j = 0h to 3h

Table 12-771.
RX_REE_ATTEN_OVRD__RX_REE_ATTEN_CNT_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8294h + formula

Figure 12-257. RX_REE_ATTEN_OVRD__RX_REE_ATTEN_CNT_j Register

31	30	29	28	27	26	25	24
RX_REE_ATTEN_OVRD_15_9							RX_REE_ATTEN_OVRD_8
R-0h							R/W-0h
23	22	21	20	19	18	17	16
RX_REE_ATTEN_OVRD_7_5			RX_REE_ATTEN_OVRD_4_0				
R-0h			R/W-0h				
15	14	13	12	11	10	9	8
RX_REE_ATTEN_CNT_15_0							
R/W-2100h							
7	6	5	4	3	2	1	0
RX_REE_ATTEN_CNT_15_0							
R/W-2100h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-772. RX_REE_ATTEN_OVRD__RX_REE_ATTEN_CNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RX_REE_ATTEN_OVRD_15_9	R	0h	Reserved
24	RX_REE_ATTEN_OVRD_8	R/W	0h	Attenuation override enable: Setting this bit to a 1'b1 will allow the rxda_dfe_attenuation_bin signal to be overridden by the attenuation override value signal in this register.
23-21	RX_REE_ATTEN_OVRD_7_5	R	0h	Reserved

Table 12-772. RX_REE_ATTEN_OVRD__RX_REE_ATTEN_CNT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	RX_REE_ATTEN_OVRD_4_0	R/W	0h	Attenuation override value: When enabled by the attenuation override enable bit in this register, this value will override the current attenuation value on the rxd_dfe_attenuation_bin output pin, and also force a corresponding change on the rxd_dfe_attenuation_therm pin. The following specifies the values that can be written to this register. 6'b 000000: Min 6'b000001 6'b000011 6'b000111 6'b001111 6'b011111 6'b 111111: Max
15-0	RX_REE_ATTEN_CNT_15_0	R/W	2100h	Attenuation counter max: Value used to specify the maximum number of consecutive words above or below the specified thresholds which will result in triggering an increase or decrease in the rxd_dfe_attenuation_bin signal.

Table 12-773. Register Call Summary for RX_REE_ATTEN_OVRD__RX_REE_ATTEN_CNT_j

10-G SerDes Registers

- [RX_REE_ATTEN_OVRD__RX_REE_ATTEN_CNT_j Register \(Offset = 8294h + formula\) \[reset = 2100h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.258 RX_REE_ATTEN_DIAG_j Register (Offset = 8298h + formula) [reset = X]

RX_REE_ATTEN_DIAG_j is shown in [Figure 12-258](#) and described in [Table 12-775](#).

Return to [Summary Table](#).

REE attenuation diagnostics register

Offset = 8298h + (j * 400h); where j = 0h to 3h

Table 12-774. RX_REE_ATTEN_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 8298h + formula

Figure 12-258. RX_REE_ATTEN_DIAG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RX_REE_ATTEN_DIAG_15_5							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_ATTEN_DIAG_15_5				RX_REE_ATTEN_DIAG_4_0			
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 12-775. RX_REE_ATTEN_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-5	RX_REE_ATTEN_DIAG_15_5	R	0h	Reserved
4-0	RX_REE_ATTEN_DIAG_4_0	R	0h	Current attenuation value: Current value of the attenuation.

Table 12-776. Register Call Summary for RX_REE_ATTEN_DIAG_j

10-G SerDes Registers

- [RX_REE_ATTEN_DIAG_j Register \(Offset = 8298h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.259 RX_REE_TAP1_OVRD__RX_REE_TAP1_CTRL_j Register (Offset = 82A0h + formula) [reset = 400h]

RX_REE_TAP1_OVRD__RX_REE_TAP1_CTRL_j is shown in Figure 12-259 and described in Table 12-778.

Return to [Summary Table](#).

REE tap 1 control register

Offset = 82A0h + (j * 400h); where j = 0h to 3h

Table 12-777.
RX_REE_TAP1_OVRD__RX_REE_TAP1_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 82A0h + formula

Figure 12-259. RX_REE_TAP1_OVRD__RX_REE_TAP1_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_TAP1_OVRD_15_8							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_TAP1_OVRD_7	RX_REE_TAP1_OVRD_6	RX_REE_TAP1_OVRD_5_0					
R/W-0h	R-0h	R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_TAP1_CTRL_15_12				RX_REE_TAP1_CTRL_11	RX_REE_TAP1_CTRL_10	RX_REE_TAP1_CTRL_9	RX_REE_TAP1_CTRL_8
R-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_REE_TAP1_CTRL_7	RX_REE_TAP1_CTRL_6_4			RX_REE_TAP1_CTRL_3_0			
R-0h	R/W-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-778. RX_REE_TAP1_OVRD__RX_REE_TAP1_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_REE_TAP1_OVRD_15_8	R	0h	Reserved
23	RX_REE_TAP1_OVRD_7	R/W	0h	Tap override enable: Setting this bit to a 1'b1 will enable the tap override field in this register to override the tap integrator accumulator functions.
22	RX_REE_TAP1_OVRD_6	R	0h	Reserved
21-16	RX_REE_TAP1_OVRD_5_0	R/W	0h	Tap override value: When the tap override enable bit in this register is active, the value in this field will override the integrator accumulator value, as well as the input to the binary to thermometer encoder.
15-12	RX_REE_TAP1_CTRL_15_12	R	0h	Reserved
11	RX_REE_TAP1_CTRL_11	R/W	0h	Tap coefficient combinational logic zero crossing enable: 1'b 0: Zero crossing combinational logic input not enabled. 1'b 1: Zero crossing combinational logic input enabled.
10	RX_REE_TAP1_CTRL_10	R/W	1h	Tap coefficient combinational logic non zero crossing enable: 1'b 0: non zero crossing combinational logic input not enabled. 1'b 1: non zero crossing combinational logic input enabled.

Table 12-778. RX_REE_TAP1_OVRD__RX_REE_TAP1_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RX_REE_TAP1_CTRL_9	R/W	0h	Tap coefficient combinational logic bit 0 only enable: 1'b 0: All enabled combinational logic input modules will be used. 1'b 1: Only the enabled combinational logic input modules associated with bit 0 will be used.
8	RX_REE_TAP1_CTRL_8	R/W	0h	Receiver DFE tap coefficient disable: This bit disables the rxda_dfe_tap_coef output signal. 1'b 0 : rxda_dfe_tap_coef output enabled. 1'b 1 : rxda_dfe_tap_coef output disabled (all 0s).
7	RX_REE_TAP1_CTRL_7	R	0h	Reserved
6-4	RX_REE_TAP1_CTRL_6_4	R/W	0h	Tap integrator accumulator scaler value: Specifies the amount to scale the input to the tap integrator accumulator by. The following are the valid settings for this field: 3'b 000: x1 3'b 001 - 3'b 111: Reserved
3-0	RX_REE_TAP1_CTRL_3_0	R/W	0h	Tap sigma delta accumulator scaler value: Specifies the amount to scale the input to the tap sigma delta accumulator by. The following are the valid settings for this field: 4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768

Table 12-779. Register Call Summary for RX_REE_TAP1_OVRD__RX_REE_TAP1_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_TAP1_OVRD__RX_REE_TAP1_CTRL_j Register \(Offset = 82A0h + formula\) \[reset = 400h\]: \[0\]](#)

12.260 RX_REE_TAP1_DIAG_j Register (Offset = 82A4h + formula) [reset = X]

RX_REE_TAP1_DIAG_j is shown in Figure 12-260 and described in Table 12-781.

Return to [Summary Table](#).

REE tap 1 diagnostics register

Offset = 82A4h + (j * 400h); where j = 0h to 3h

Table 12-780. RX_REE_TAP1_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 82A4h + formula

Figure 12-260. RX_REE_TAP1_DIAG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_REE_TAP1_DIAG_15	RX_REE_TAP1_DIAG_14	RX_REE_TAP1_DIAG_13	RX_REE_TAP1_DIAG_12	RX_REE_TAP1_DIAG_11_6			
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
RX_REE_TAP1_DIAG_11_6		RX_REE_TAP1_DIAG_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-781. RX_REE_TAP1_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RX_REE_TAP1_DIAG_15	R	0h	Reserved
14	RX_REE_TAP1_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the tap voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.
13	RX_REE_TAP1_DIAG_13	R/W	0h	Voter override pos : Writing a 1'b1 in this register bit will force the tap voter function to activate the voter pos signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

Table 12-781. RX_REE_TAP1_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_TAP1_DIAG_12	R/W	0h	Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter in the tap. Note : This function is intended to be for diagnostic and verification purposes only. Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.
11-6	RX_REE_TAP1_DIAG_11_6	R	0h	Reserved
5-0	RX_REE_TAP1_DIAG_5_0	R	0h	Current tap integrator accumulator: Current value of the tap integrator accumulator.

Table 12-782. Register Call Summary for RX_REE_TAP1_DIAG_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_TAP1_DIAG_j Register \(Offset = 82A4h + formula\) \[reset = X\]: \[0\]](#)

12.261 RX_REE_TAP2_OVRD__RX_REE_TAP2_CTRL_j Register (Offset = 82A8h + formula) [reset = 400h]

RX_REE_TAP2_OVRD__RX_REE_TAP2_CTRL_j is shown in Figure 12-261 and described in Table 12-784.

Return to [Summary Table](#).

REE tap 2 control register

Offset = 82A8h + (j * 400h); where j = 0h to 3h

Table 12-783.
RX_REE_TAP2_OVRD__RX_REE_TAP2_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 82A8h + formula

Figure 12-261. RX_REE_TAP2_OVRD__RX_REE_TAP2_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_TAP2_OVRD_15_8							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_TAP2_OVRD_7	RX_REE_TAP2_OVRD_6	RX_REE_TAP2_OVRD_5_0					
R/W-0h	R-0h	R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_TAP2_CTRL_15_12				RX_REE_TAP2_CTRL_11	RX_REE_TAP2_CTRL_10	RX_REE_TAP2_CTRL_9	RX_REE_TAP2_CTRL_8
R-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_REE_TAP2_CTRL_7	RX_REE_TAP2_CTRL_6_4			RX_REE_TAP2_CTRL_3_0			
R-0h	R/W-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-784. RX_REE_TAP2_OVRD__RX_REE_TAP2_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_REE_TAP2_OVRD_15_8	R	0h	Reserved
23	RX_REE_TAP2_OVRD_7	R/W	0h	Tap override enable: Setting this bit to a 1'b1 will enable the tap override field in this register to override the tap integrator accumulator functions.
22	RX_REE_TAP2_OVRD_6	R	0h	Reserved
21-16	RX_REE_TAP2_OVRD_5_0	R/W	0h	Tap override value: When the tap override enable bit in this register is active, the value in this field will override the integrator accumulator value, as well as the input to the binary to thermometer encoder.
15-12	RX_REE_TAP2_CTRL_15_12	R	0h	Reserved
11	RX_REE_TAP2_CTRL_11	R/W	0h	Tap coefficient combinational logic zero crossing enable: 1'b 0: Zero crossing combinational logic input not enabled. 1'b 1: Zero crossing combinational logic input enabled. (This mode is currently not supported)

Table 12-784. RX_REE_TAP2_OVRD__RX_REE_TAP2_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_REE_TAP2_CTRL_10	R/W	1h	Tap coefficient combinational logic non zero crossing enable: 1'b 0: non zero crossing combinational logic input not enabled. 1'b 1: non zero crossing combinational logic input enabled.
9	RX_REE_TAP2_CTRL_9	R/W	0h	Tap coefficient combinational logic bit 0 only enable: 1'b 0: All enabled combinational logic input modules will be used. 1'b 1: Only the enabled combinational logic input modules associated with bit 0 will be used.
8	RX_REE_TAP2_CTRL_8	R/W	0h	Receiver DFE tap coefficient disable: This bit disables the rxda_dfe_tap_coef output signal. 1'b 0: rxda_dfe_tap_coef output enabled. 1'b 1: rxda_dfe_tap_coef output disabled (all 0s).
7	RX_REE_TAP2_CTRL_7	R	0h	Reserved
6-4	RX_REE_TAP2_CTRL_6_4	R/W	0h	Tap integrator accumulator scaler value: Specifies the amount to scale the input to the tap integrator accumulator by. The following are the valid settings for this field: 3'b 000: x1 3'b 001 - 3'b 111: Reserved
3-0	RX_REE_TAP2_CTRL_3_0	R/W	0h	Tap sigma delta accumulator scaler value: Specifies the amount to scale the input to the tap sigma delta accumulator by. The following are the valid settings for this field: 4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768

Table 12-785. Register Call Summary for RX_REE_TAP2_OVRD__RX_REE_TAP2_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_TAP2_OVRD__RX_REE_TAP2_CTRL_j Register \(Offset = 82A8h + formula\) \[reset = 400h\]: \[0\]](#)

12.262 RX_REE_TAP2_DIAG_j Register (Offset = 82ACh + formula) [reset = X]

RX_REE_TAP2_DIAG_j is shown in Figure 12-262 and described in Table 12-787.

Return to [Summary Table](#).

REE tap 2 diagnostics register

Offset = 82ACh + (j * 400h); where j = 0h to 3h

Table 12-786. RX_REE_TAP2_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 82ACh + formula

Figure 12-262. RX_REE_TAP2_DIAG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_REE_TAP2_DIAG_15	RX_REE_TAP2_DIAG_14	RX_REE_TAP2_DIAG_13	RX_REE_TAP2_DIAG_12	RX_REE_TAP2_DIAG_11_6			
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
RX_REE_TAP2_DIAG_11_6		RX_REE_TAP2_DIAG_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-787. RX_REE_TAP2_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RX_REE_TAP2_DIAG_15	R	0h	Reserved
14	RX_REE_TAP2_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the tap voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.
13	RX_REE_TAP2_DIAG_13	R/W	0h	Voter override pos : Writing a 1'b1 in this register bit will force the tap voter function to activate the voter pos signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

Table 12-787. RX_REE_TAP2_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_TAP2_DIAG_12	R/W	0h	Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter in the tap. Note : This function is intended to be for diagnostic and verification purposes only. Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.
11-6	RX_REE_TAP2_DIAG_11_6	R	0h	Reserved
5-0	RX_REE_TAP2_DIAG_5_0	R	0h	Current tap integrator accumulator: Current value of the tap integrator accumulator.

Table 12-788. Register Call Summary for RX_REE_TAP2_DIAG_j

10-G SerDes Registers

- [RX_REE_TAP2_DIAG_j Register \(Offset = 82ACh + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.263 RX_REE_TAP3_OVRD__RX_REE_TAP3_CTRL_j Register (Offset = 82B0h + formula) [reset = 400h]

RX_REE_TAP3_OVRD__RX_REE_TAP3_CTRL_j is shown in [Figure 12-263](#) and described in [Table 12-790](#).

Return to [Summary Table](#).

REE tap 3 control register

Offset = 82B0h + (j * 400h); where j = 0h to 3h

Table 12-789.
RX_REE_TAP3_OVRD__RX_REE_TAP3_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 82B0h + formula

Figure 12-263. RX_REE_TAP3_OVRD__RX_REE_TAP3_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_TAP3_OVRD_15_8							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_TAP3_OVRD_7	RX_REE_TAP3_OVRD_6	RX_REE_TAP3_OVRD_5_0					
R/W-0h	R-0h	R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_TAP3_CTRL_15_12				RX_REE_TAP3_CTRL_11	RX_REE_TAP3_CTRL_10	RX_REE_TAP3_CTRL_9	RX_REE_TAP3_CTRL_8
R-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_REE_TAP3_CTRL_7	RX_REE_TAP3_CTRL_6_4			RX_REE_TAP3_CTRL_3_0			
R-0h	R/W-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-790. RX_REE_TAP3_OVRD__RX_REE_TAP3_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_REE_TAP3_OVRD_15_8	R	0h	Reserved
23	RX_REE_TAP3_OVRD_7	R/W	0h	Tap override enable: Setting this bit to a 1'b1 will enable the tap override field in this register to override the tap integrator accumulator functions.
22	RX_REE_TAP3_OVRD_6	R	0h	Reserved
21-16	RX_REE_TAP3_OVRD_5_0	R/W	0h	Tap override value: When the tap override enable bit in this register is active, the value in this field will override the integrator accumulator value, as well as the input to the binary to thermometer encoder.
15-12	RX_REE_TAP3_CTRL_15_12	R	0h	Reserved
11	RX_REE_TAP3_CTRL_11	R/W	0h	Tap coefficient combinational logic zero crossing enable: 1'b 0: Zero crossing combinational logic input not enabled. 1'b 1: Zero crossing combinational logic input enabled. (This mode is currently not supported)

Table 12-790. RX_REE_TAP3_OVRD__RX_REE_TAP3_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	RX_REE_TAP3_CTRL_10	R/W	1h	Tap coefficient combinational logic non zero crossing enable: 1'b 0: non zero crossing combinational logic input not enabled. 1'b 1: non zero crossing combinational logic input enabled.
9	RX_REE_TAP3_CTRL_9	R/W	0h	Tap coefficient combinational logic bit 0 only enable: 1'b 0: All enabled combinational logic input modules will be used. 1'b 1: Only the enabled combinational logic input modules associated with bit 0 will be used.
8	RX_REE_TAP3_CTRL_8	R/W	0h	Receiver DFE tap coefficient disable: This bit disables the rxda_dfe_tap_coef output signal. 1'b 0: rxda_dfe_tap_coef output enabled. 1'b 1: rxda_dfe_tap_coef output disabled (all 0s).
7	RX_REE_TAP3_CTRL_7	R	0h	Reserved
6-4	RX_REE_TAP3_CTRL_6_4	R/W	0h	Tap integrator accumulator scaler value: Specifies the amount to scale the input to the tap integrator accumulator by. The following are the valid settings for this field: 3'b 000: x1 3'b 001 - 3'b 111: Reserved
3-0	RX_REE_TAP3_CTRL_3_0	R/W	0h	Tap sigma delta accumulator scaler value: Specifies the amount to scale the input to the tap sigma delta accumulator by. The following are the valid settings for this field: 4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768

Table 12-791. Register Call Summary for RX_REE_TAP3_OVRD__RX_REE_TAP3_CTRL_j

10-G SerDes Registers

- [RX_REE_TAP3_OVRD__RX_REE_TAP3_CTRL_j Register \(Offset = 82B0h + formula\) \[reset = 400h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.264 RX_REE_TAP3_DIAG_j Register (Offset = 82B4h + formula) [reset = X]

RX_REE_TAP3_DIAG_j is shown in Figure 12-264 and described in Table 12-793.

Return to [Summary Table](#).

REE tap 3 diagnostics register

Offset = 82B4h + (j * 400h); where j = 0h to 3h

Table 12-792. RX_REE_TAP3_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 82B4h + formula

Figure 12-264. RX_REE_TAP3_DIAG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_REE_TAP3_DIAG_15	RX_REE_TAP3_DIAG_14	RX_REE_TAP3_DIAG_13	RX_REE_TAP3_DIAG_12	RX_REE_TAP3_DIAG_11_6			
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
RX_REE_TAP3_DIAG_11_6		RX_REE_TAP3_DIAG_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-793. RX_REE_TAP3_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RX_REE_TAP3_DIAG_15	R	0h	Reserved
14	RX_REE_TAP3_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the tap voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.
13	RX_REE_TAP3_DIAG_13	R/W	0h	Voter override pos : Writing a 1'b1 in this register bit will force the tap voter function to activate the voter pos signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

Table 12-793. RX_REE_TAP3_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_TAP3_DIAG_12	R/W	0h	Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter in the tap. Note : This function is intended to be for diagnostic and verification purposes only. Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.
11-6	RX_REE_TAP3_DIAG_11_6	R	0h	Reserved
5-0	RX_REE_TAP3_DIAG_5_0	R	0h	Current tap integrator accumulator: Current value of the tap integrator accumulator.

Table 12-794. Register Call Summary for RX_REE_TAP3_DIAG_j

10-G SerDes Registers

- [RX_REE_TAP3_DIAG_j Register \(Offset = 82B4h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.265 RX_REE_LFEQ_OVRD_RX_REE_LFEQ_CTRL_j Register (Offset = 82B8h + formula) [reset = 0h]

RX_REE_LFEQ_OVRD_RX_REE_LFEQ_CTRL_j is shown in Figure 12-265 and described in Table 12-796.

Return to [Summary Table](#).

REE low frequency equalizer control register

Offset = 82B8h + (j * 400h); where j = 0h to 3h

Table 12-795.
RX_REE_LFEQ_OVRD_RX_REE_LFEQ_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 82B8h + formula

Figure 12-265. RX_REE_LFEQ_OVRD_RX_REE_LFEQ_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_LFEQ_OVRD_15_8							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_LFEQ_OVRD_7	RX_REE_LFEQ_OVRD_6	RX_REE_LFEQ_OVRD_5_0					
R/W-0h	R-0h	R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_LFEQ_CTRL_15_9							RX_REE_LFEQ_CTRL_8
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RX_REE_LFEQ_CTRL_7	RX_REE_LFEQ_CTRL_6_4			RX_REE_LFEQ_CTRL_3_0			
R-0h	R/W-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-796. RX_REE_LFEQ_OVRD_RX_REE_LFEQ_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_REE_LFEQ_OVRD_15_8	R	0h	Reserved
23	RX_REE_LFEQ_OVRD_7	R/W	0h	Override enable: Setting this bit to a 1'b1 will enable the override field in this register to override the integrator accumulator functions.
22	RX_REE_LFEQ_OVRD_6	R	0h	Reserved
21-16	RX_REE_LFEQ_OVRD_5_0	R/W	0h	Override value: When the override enable bit in this register is active, the value in this field will override the integrator accumulator value, as well as the input to the binary to thermometer encoder.
15-9	RX_REE_LFEQ_CTRL_15_9	R	0h	Reserved
8	RX_REE_LFEQ_CTRL_8	R/W	0h	Receiver DFE coefficient disable: This bit disables the rxd_dfe_coef output signal. 1'b 0 : rxd_dfe_coef output enabled. 1'b 1 : rxd_dfe_coef output disabled (all 0s).
7	RX_REE_LFEQ_CTRL_7	R	0h	Reserved

Table 12-796. RX_REE_LFEQ_OVRD__RX_REE_LFEQ_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	RX_REE_LFEQ_CTRL_6_4	R/W	0h	<p>Integrator accumulator scaler value: Specifies the amount to scale the input to the integrator accumulator by.</p> <p>The following are the valid settings for this field:</p> <p>3'b 000: x1 3'b 001: x2 3'b 010: x4 3'b 011: x8 3'b 100: x16 3'b 101 - 3'b 111: Reserved</p>
3-0	RX_REE_LFEQ_CTRL_3_0	R/W	0h	<p>Sigma delta accumulator scaler value: Specifies the amount to scale the input to the sigma delta accumulator by.</p> <p>The following are the valid settings for this field:</p> <p>4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768</p>

Table 12-797. Register Call Summary for RX_REE_LFEQ_OVRD__RX_REE_LFEQ_CTRL_j

10-G SerDes Registers

- [RX_REE_LFEQ_OVRD__RX_REE_LFEQ_CTRL_j Register \(Offset = 82B8h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.266 RX_REE_LFEQ_DIAG_j Register (Offset = 82BCh + formula) [reset = X]

RX_REE_LFEQ_DIAG_j is shown in Figure 12-266 and described in Table 12-799.

Return to [Summary Table](#).

REE low frequency equalizer diagnostics register

Offset = 82BCh + (j * 400h); where j = 0h to 3h

Table 12-798. RX_REE_LFEQ_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 82BCh + formula

Figure 12-266. RX_REE_LFEQ_DIAG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_REE_LFEQ_DIAG_15	RX_REE_LFEQ_DIAG_14	RX_REE_LFEQ_DIAG_13	RX_REE_LFEQ_DIAG_12	RX_REE_LFEQ_DIAG_11_6			
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
RX_REE_LFEQ_DIAG_11_6		RX_REE_LFEQ_DIAG_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-799. RX_REE_LFEQ_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RX_REE_LFEQ_DIAG_15	R	0h	Reserved
14	RX_REE_LFEQ_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.
13	RX_REE_LFEQ_DIAG_13	R/W	0h	Voter override pos : Writing a 1'b1 in this register bit will force the voter function to activate the voter pos signal for a single cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

Table 12-799. RX_REE_LFEQ_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_LFEQ_DIAG_12	R/W	0h	Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter. Note : This function is intended to be for diagnostic and verification purposes only. Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.
11-6	RX_REE_LFEQ_DIAG_11_6	R	0h	Reserved
5-0	RX_REE_LFEQ_DIAG_5_0	R	0h	Current integrator accumulator: Current value of the integrator accumulator.

Table 12-800. Register Call Summary for RX_REE_LFEQ_DIAG_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_LFEQ_DIAG_j Register \(Offset = 82BCh + formula\) \[reset = X\]: \[0\]](#)

12.267 RX_REE_VGA_GAIN_OVRD__RX_REE_VGA_GAIN_CTRL_j Register (Offset = 82C0h + formula) [reset = 1701h]

RX_REE_VGA_GAIN_OVRD__RX_REE_VGA_GAIN_CTRL_j is shown in [Figure 12-267](#) and described in [Table 12-802](#).

Return to [Summary Table](#).

REE VGA gain control register

Offset = 82C0h + (j * 400h); where j = 0h to 3h

Table 12-801. RX_REE_VGA_GAIN_OVRD__RX_REE_VGA_GAIN_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 82C0h + formula

Figure 12-267. RX_REE_VGA_GAIN_OVRD__RX_REE_VGA_GAIN_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_VGA_GAIN_OVRD_15	RX_REE_VGA_GAIN_OVRD_14_13	RX_REE_VGA_GAIN_OVRD_12_8					
R/W-0h	R-0h	R/W-0h					
23	22	21	20	19	18	17	16
RX_REE_VGA_GAIN_OVRD_7	RX_REE_VGA_GAIN_OVRD_6_5	RX_REE_VGA_GAIN_OVRD_4_0					
R/W-0h	R-0h	R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_VGA_GAIN_CTRL_15_13			RX_REE_VGA_GAIN_CTRL_12_8				
R-0h			R/W-17h				
7	6	5	4	3	2	1	0
RX_REE_VGA_GAIN_CTRL_7	RX_REE_VGA_GAIN_CTRL_6_4			RX_REE_VGA_GAIN_CTRL_3_0			
R-0h	R/W-0h			R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-802. RX_REE_VGA_GAIN_OVRD__RX_REE_VGA_GAIN_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_VGA_GAIN_OVRD_15	R/W	0h	VGA gain target adjust override enable: Setting this bit to a 1'b1 will enable the VGA gain target adjust override field in this register to override the VGA gain target adjust accumulator functions.
30-29	RX_REE_VGA_GAIN_OVRD_14_13	R	0h	Reserved
28-24	RX_REE_VGA_GAIN_OVRD_12_8	R/W	0h	VGA gain target adjust override value: When the VGA gain target adjust override enable bit in this register is active, the value in this field will override the accumulator value used to drive the vga_gain_tgt_adj signal.
23	RX_REE_VGA_GAIN_OVRD_7	R/W	0h	VGA gain override enable: Setting this bit to a 1'b1 will enable the VGA gain override field in this register to override the VGA gain integrator accumulator functions.
22-21	RX_REE_VGA_GAIN_OVRD_6_5	R	0h	Reserved

**Table 12-802. RX_REE_VGA_GAIN_OVRD__RX_REE_VGA_GAIN_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
20-16	RX_REE_VGA_GAIN_OVRD_4_0	R/W	0h	VGA gain override value: When the VGA gain override enable bit in this register is active, the value in this field will override the integrator accumulator value, as well as the input to the binary to thermometer encoder.
15-13	RX_REE_VGA_GAIN_CTRL_15_13	R	0h	Reserved
12-8	RX_REE_VGA_GAIN_CTRL_12_8	R/W	17h	VGA gain max: Specifies the maximum value of the VGA gain integrator accumulator, and therefore also the maximum number of bits in the rxd_dfe_vga_gain thermometer code that will be set.
7	RX_REE_VGA_GAIN_CTRL_7	R	0h	Reserved
6-4	RX_REE_VGA_GAIN_CTRL_6_4	R/W	0h	VGA gain integrator accumulator scaler value: Specifies the amount to scale the input to the VGA gain integrator accumulator by. The following are the valid settings for this field: 3'b 000: x1 3'b 001: x2 3'b 010: x4 3'b 011: x8 3'b 100: x16 3'b 101 - 3'b 111: Reserved
3-0	RX_REE_VGA_GAIN_CTRL_3_0	R/W	1h	VGA gain sigma delta accumulator scaler value: Specifies the amount to scale the input to the VGA gain sigma delta accumulator by. The following are the valid settings for this field: 4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768

Table 12-803. Register Call Summary for RX_REE_VGA_GAIN_OVRD__RX_REE_VGA_GAIN_CTRL_j

10-G SerDes Registers

- [RX_REE_VGA_GAIN_OVRD__RX_REE_VGA_GAIN_CTRL_j Register](#) (Offset = 82C0h + formula) [reset = 1701h]: [0]
- [10-G SerDes Registers](#): [0]

12.268 RX_REE_VGA_GAIN_TGT_DIAG_RX_REE_VGA_GAIN_DIAG_j Register (Offset = 82C4h + formula) [reset = 0h]

[RX_REE_VGA_GAIN_TGT_DIAG_RX_REE_VGA_GAIN_DIAG_j](#) is shown in [Figure 12-268](#) and described in [Table 12-805](#).

Return to [Summary Table](#).

REE VGA gain diagnostics register

Offset = 82C4h + (j * 400h); where j = 0h to 3h

Table 12-804. RX_REE_VGA_GAIN_TGT_DIAG_RX_REE_VGA_GAIN_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 82C4h + formula

Figure 12-268. RX_REE_VGA_GAIN_TGT_DIAG_RX_REE_VGA_GAIN_DIAG_j Register

31	30	29	28	27	26	25	24
RX_REE_VGA_GAIN_TGT_DIAG_15_5							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_VGA_GAIN_TGT_DIAG_15_5				RX_REE_VGA_GAIN_TGT_DIAG_4_0			
R-0h				R-0h			
15	14	13	12	11	10	9	8
RX_REE_VGA_GAIN_DIAG_15	RX_REE_VGA_GAIN_DIAG_14	RX_REE_VGA_GAIN_DIAG_13	RX_REE_VGA_GAIN_DIAG_12	RX_REE_VGA_GAIN_DIAG_11_6			
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
RX_REE_VGA_GAIN_DIAG_11_6		RX_REE_VGA_GAIN_DIAG_5_0					
R-0h				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-805. RX_REE_VGA_GAIN_TGT_DIAG_RX_REE_VGA_GAIN_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RX_REE_VGA_GAIN_TGT_DIAG_15_5	R	0h	Reserved
20-16	RX_REE_VGA_GAIN_TGT_DIAG_4_0	R	0h	Current VGA gain integrator accumulator: Current value of the VGA gain integrator accumulator.
15	RX_REE_VGA_GAIN_DIAG_15	R	0h	Reserved
14	RX_REE_VGA_GAIN_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the VGA gain voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

Table 12-805. RX_REE_VGA_GAIN_TGT_DIAG__RX_REE_VGA_GAIN_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	RX_REE_VGA_GAIN_DIAG_13	R/W	0h	<p>Voter override pos : Writing a 1'b1 in this register bit will force the VGA gain voter function to activate the voter pos signal for a single clock cycle.</p> <p>Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit.</p> <p>Note : It is not valid to activate both the voter override neg and voter override pos at the same time.</p>
12	RX_REE_VGA_GAIN_DIAG_12	R/W	0h	<p>Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter in the VGA gain.</p> <p>Note : This function is intended to be for diagnostic and verification purposes only.</p> <p>Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.</p>
11-6	RX_REE_VGA_GAIN_DIAG_11_6	R	0h	Reserved
5-0	RX_REE_VGA_GAIN_DIAG_5_0	R	0h	<p>Current VGA gain integrator accumulator: Current value of the VGA gain integrator accumulator.</p> <p>Note: The reset value for this field is with the transceiver data path power island switched off.</p> <p>In cases where this power island is switched on, the reset value be 6'b001010</p>

Table 12-806. Register Call Summary for RX_REE_VGA_GAIN_TGT_DIAG__RX_REE_VGA_GAIN_DIAG_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_VGA_GAIN_TGT_DIAG__RX_REE_VGA_GAIN_DIAG_j Register \(Offset = 82C4h + formula\) \[reset = 0h\]: \[0\]](#)

12.269 RX_REE_OFF_COR_OVRD__RX_REE_OFF_COR_CTRL_j Register (Offset = 82C8h + formula) [reset = 1h]

RX_REE_OFF_COR_OVRD__RX_REE_OFF_COR_CTRL_j is shown in Figure 12-269 and described in Table 12-808.

Return to [Summary Table](#).

REE offset correction control register

Offset = 82C8h + (j * 400h); where j = 0h to 3h

Table 12-807. RX_REE_OFF_COR_OVRD__RX_REE_OFF_COR_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 82C8h + formula

Figure 12-269. RX_REE_OFF_COR_OVRD__RX_REE_OFF_COR_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_OFF_COR_OVRD_15_8							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_OFF_COR_OVRD_7	RX_REE_OFF_COR_OVRD_6	RX_REE_OFF_COR_OVRD_5_0					
R/W-0h	R-0h	R/W-0h					
15	14	13	12	11	10	9	8
RX_REE_OFF_COR_CTRL_15_7							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_OFF_COR_CTRL_15_7	RX_REE_OFF_COR_CTRL_6_4			RX_REE_OFF_COR_CTRL_3_0			
R-0h	R/W-0h			R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-808. RX_REE_OFF_COR_OVRD__RX_REE_OFF_COR_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_REE_OFF_COR_OVRD_15_8	R	0h	Reserved
23	RX_REE_OFF_COR_OVRD_7	R/W	0h	Offset correction override enable: Setting this bit to a 1'b1 will enable the offset correction override field in this register to override the offset correction integrator accumulator functions.
22	RX_REE_OFF_COR_OVRD_6	R	0h	Reserved
21-16	RX_REE_OFF_COR_OVRD_5_0	R/W	0h	Offset correction override value: When the offset correction override enable bit in this register is active, the value in this field will override the integrator accumulator value, as well as the input to the binary to thermometer encoder.
15-7	RX_REE_OFF_COR_CTRL_15_7	R	0h	Reserved

**Table 12-808. RX_REE_OFF_COR_OVRD__RX_REE_OFF_COR_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
6-4	RX_REE_OFF_COR_CTL_6_4	R/W	0h	Offset correction integrator accumulator scaler value: Specifies the amount to scale the input to the offset correction integrator accumulator by. The following are the valid settings for this field: 3'b 000: x1 3'b 001: x2 3'b 010: x4 3'b 011: x8 3'b 100: x16 3'b 101 - 3'b 111: Reserved
3-0	RX_REE_OFF_COR_CTL_3_0	R/W	1h	Offset correction sigma delta accumulator scaler value: Specifies the amount to scale the input to the offset correction sigma delta accumulator by. The following are the valid settings for this field: 4'b 0000: x1 4'b 0001: x2 4'b 0010: x4 4'b 0011: x8 4'b 0100: x16 4'b 0101: x 32 4'b 0110: x 64 4'b 0111: x128 4'b 1000: x256 4'b 1001: x512 4'b 1010: x1024 4'b 1011: x2048 4'b 1100: x 4096 4'b1101 x 8192 4'b1110 x 16384 4'b1111 x 32768

Table 12-809. Register Call Summary for RX_REE_OFF_COR_OVRD__RX_REE_OFF_COR_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_OFF_COR_OVRD__RX_REE_OFF_COR_CTRL_j Register \(Offset = 82C8h + formula\) \[reset = 1h\]: \[0\]](#)

12.270 RX_REE_OFF_COR_DIAG_j Register (Offset = 82CCh + formula) [reset = X]

RX_REE_OFF_COR_DIAG_j is shown in Figure 12-270 and described in Table 12-811.

Return to [Summary Table](#).

REE offset correction diagnostics register

Offset = 82CCh + (j * 400h); where j = 0h to 3h

Table 12-810. RX_REE_OFF_COR_DIAG_j Instances

Instance	Physical Address
SERDES_10G0	0505 82CCh + formula

Figure 12-270. RX_REE_OFF_COR_DIAG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_REE_OFF_COR_DIAG_15	RX_REE_OFF_COR_DIAG_14	RX_REE_OFF_COR_DIAG_13	RX_REE_OFF_COR_DIAG_12	RX_REE_OFF_COR_DIAG_11_6			
R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
RX_REE_OFF_COR_DIAG_11_6		RX_REE_OFF_COR_DIAG_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-811. RX_REE_OFF_COR_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	RX_REE_OFF_COR_DIAG_15	R	0h	Reserved
14	RX_REE_OFF_COR_DIAG_14	R/W	0h	Voter override neg : Writing a 1'b1 in this register bit will force the offset correction voter function to activate the voter neg signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.
13	RX_REE_OFF_COR_DIAG_13	R/W	0h	Voter override pos : Writing a 1'b1 in this register bit will force the offset correction voter function to activate the voter pos signal for a single clock cycle. Note : This bit must be cleared after each time it is enabled, in order to perform follow on voter override functions with this bit. Note : It is not valid to activate both the voter override neg and voter override pos at the same time.

Table 12-811. RX_REE_OFF_COR_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RX_REE_OFF_COR_DIAG_12	R/W	0h	Voter override enable : Setting this bit to a 1'b1 will allow only the voter override pos and voter override neg bits in this register to control the voter in the offset correction. Note : This function is intended to be for diagnostic and verification purposes only. Note : Both the voter override neg and voter override pos bits in this register must be set to 1'b0 when this bit is initially set to 1'b1 when enabling this function.
11-6	RX_REE_OFF_COR_DIAG_11_6	R	0h	Reserved
5-0	RX_REE_OFF_COR_DIAG_5_0	R	0h	Current offset correction integrator accumulator: Current value of the offset correction integrator accumulator.

Table 12-812. Register Call Summary for RX_REE_OFF_COR_DIAG_j

10-G SerDes Registers

- [RX_REE_OFF_COR_DIAG_j Register \(Offset = 82CCh + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.271 RX_REE_SC_COR_TCNT__RX_REE_SC_COR_WCNT_j Register (Offset = 82D0h + formula) [reset = 0004000Ah]

[RX_REE_SC_COR_TCNT__RX_REE_SC_COR_WCNT_j](#) is shown in [Figure 12-271](#) and described in [Table 12-814](#).

Return to [Summary Table](#).

REE short channel correction valid word counter register

Offset = 82D0h + (j * 400h); where j = 0h to 3h

Table 12-813. RX_REE_SC_COR_TCNT__RX_REE_SC_COR_WCNT_j Instances

Instance	Physical Address
SERDES_10G0	0505 82D0h + formula

Figure 12-271. RX_REE_SC_COR_TCNT__RX_REE_SC_COR_WCNT_j Register

31	30	29	28	27	26	25	24
RX_REE_SC_COR_TCNT_15_6							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_SC_COR_TCNT_15_6				RX_REE_SC_COR_TCNT_5_0			
R-0h				R/W-4h			
15	14	13	12	11	10	9	8
RX_REE_SC_COR_WCNT_15_6							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_SC_COR_WCNT_15_6				RX_REE_SC_COR_WCNT_5_0			
R-0h				R/W-Ah			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-814. RX_REE_SC_COR_TCNT__RX_REE_SC_COR_WCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RX_REE_SC_COR_TCN T_15_6	R	0h	Reserved
21-16	RX_REE_SC_COR_TCN T_5_0	R/W	4h	Threshold counter start value : Value used for the starting value when counting the number of bits that are below the error threshold.
15-6	RX_REE_SC_COR_WCN T_15_6	R	0h	Reserved
5-0	RX_REE_SC_COR_WCN T_5_0	R/W	Ah	Valid word counter start value : Value used for the starting value when counting the number of valid words.

Table 12-815. Register Call Summary for RX_REE_SC_COR_TCNT__RX_REE_SC_COR_WCNT_j

10-G SerDes Registers

- [RX_REE_SC_COR_TCNT__RX_REE_SC_COR_WCNT_j Register \(Offset = 82D0h + formula\) \[reset = 0004000Ah\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.272 RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j Register (Offset = 82E0h + formula) [reset = 05190101h]

RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j is shown in Figure 12-272 and described in Table 12-817.

Return to [Summary Table](#).

REE adder configuration register

Offset = 82E0h + (j * 400h); where j = 0h to 3h

Table 12-816.
RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j
Instances

Instance	Physical Address
SERDES_10G0	0505 82E0h + formula

Figure 12-272. RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j Register

31	30	29	28	27	26	25	24
RX_REE_TAP1_CLIP_15_11					RX_REE_TAP1_CLIP_10_8		
R-0h					R/W-5h		
23	22	21	20	19	18	17	16
RX_REE_TAP1_CLIP_7_5				RX_REE_TAP1_CLIP_4_0			
R-0h				R/W-19h			
15	14	13	12	11	10	9	8
RX_REE_ADDR_CFG_15_11					RX_REE_ADDR_CFG_10	RX_REE_ADDR_CFG_9	RX_REE_ADDR_CFG_8
R-0h					R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RX_REE_ADDR_CFG_7_3					RX_REE_ADDR_CFG_2	RX_REE_ADDR_CFG_1	RX_REE_ADDR_CFG_0
R-0h					R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-817. RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RX_REE_TAP1_CLIP_15_11	R	0h	Reserved
26-24	RX_REE_TAP1_CLIP_10_8	R/W	5h	VGA target gain adjust multiplier: Controls how much to multiply the VGA target gain adjust by, when calculating the tap threshold. The following are valid values, and the corresponding multiplier values. 3'b 000 : x 0.00 3'b 001 : x 0.25 3'b 010 : x 0.50 3'b 011 : x 0.75 3'b 100 : x 1.00 3'b 101 : x 1.25 3'b 110 : x 1.50 3'b 111 : x 1.75 Note : By setting this field to 3'b000, the threshold value of the tap can be directly controlled by the threshold adjust field in this register. Note : The VGA gain adjust signal is always a negative number.
23-21	RX_REE_TAP1_CLIP_7_5	R	0h	Reserved

Table 12-817. RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	RX_REE_TAP1_CLIP_4_0	R/W	19h	Threshold adjust: Controls how much the threshold can be adjusted by, after multiplying the VGA target gain adjust multiplier with the VGA target gain adjust. Note that this field is a positive number (not twos complement). Note : The threshold for the taps is equal to : $\pm((\text{VGA target gain adjust} * \text{VGA target gain adjust multiplier}) + \text{Threshold adjust})$
15-11	RX_REE_ADDR_CFG_15_11	R	0h	Reserved
10	RX_REE_ADDR_CFG_10	R/W	0h	TX post cursor tap 3 adder enable: Setting this bit to 1'b1, enables the results of tap 3 to be added to the TX post cursor controller input.
9	RX_REE_ADDR_CFG_9	R/W	0h	TX post cursor tap 2 adder enable: Setting this bit to 1'b1, enables the results of tap 2 to be added to the TX post cursor controller input.
8	RX_REE_ADDR_CFG_8	R/W	1h	TX post cursor tap 1 adder enable: Setting this bit to 1'b1, enables the results of tap 1 to be added to the TX post cursor controller input.
7-3	RX_REE_ADDR_CFG_7_3	R	0h	Reserved
2	RX_REE_ADDR_CFG_2	R/W	0h	RX peaking tap 3 adder enable: Setting this bit to 1'b1, enables the results of tap 3 to be added to the RX peaking amp gain input.
1	RX_REE_ADDR_CFG_1	R/W	0h	RX peaking tap 2 adder enable: Setting this bit to 1'b1, enables the results of tap 2 to be added to the RX peaking amp gain input.
0	RX_REE_ADDR_CFG_0	R/W	1h	RX peaking tap 1 adder enable: Setting this bit to 1'b1, enables the results of tap 1 to be added to the RX peaking amp gain input.

Table 12-818. Register Call Summary for RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_TAP1_CLIP__RX_REE_ADDR_CFG_j Register \(Offset = 82E0h + formula\) \[reset = 05190101h\]: \[0\]](#)

12.273 RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j Register (Offset = 82E4h + formula) [reset = 4000519h]

RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j is shown in Figure 12-273 and described in Table 12-820.

Return to [Summary Table](#).

REE taps 2 and 3 clip control register

Offset = 82E4h + (j * 400h); where j = 0h to 3h

Table 12-819. RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j Instances

Instance	Physical Address
SERDES_10G0	0505 82E4h + formula

Figure 12-273. RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j Register

31	30	29	28	27	26	25	24
RX_REE_CTRL_DATA_MASK_15	RX_REE_CTRL_DATA_MASK_14	RX_REE_CTRL_DATA_MASK_13	RX_REE_CTRL_DATA_MASK_12	RX_REE_CTRL_DATA_MASK_11	RX_REE_CTRL_DATA_MASK_10	RX_REE_CTRL_DATA_MASK_9	RX_REE_CTRL_DATA_MASK_8
R-0h	R-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RX_REE_CTRL_DATA_MASK_7	RX_REE_CTRL_DATA_MASK_6	RX_REE_CTRL_DATA_MASK_5	RX_REE_CTRL_DATA_MASK_4	RX_REE_CTRL_DATA_MASK_3	RX_REE_CTRL_DATA_MASK_2	RX_REE_CTRL_DATA_MASK_1	RX_REE_CTRL_DATA_MASK_0
R/W-0h	R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_REE_TAP2TON_CLIP_15_11					RX_REE_TAP2TON_CLIP_10_8		
R-0h					R/W-5h		
7	6	5	4	3	2	1	0
RX_REE_TAP2TON_CLIP_7_5			RX_REE_TAP2TON_CLIP_4_0				
R-0h			R/W-19h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-820. RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_REE_CTRL_DATA_MASK_15	R	0h	Reserved
30	RX_REE_CTRL_DATA_MASK_14	R	1h	Ignore 1010 controller - Note that this is read only. This should never be disabled.
29	RX_REE_CTRL_DATA_MASK_13	R/W	0h	TX equalization evaluator: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
28	RX_REE_CTRL_DATA_MASK_12	R/W	0h	TX post cursor control: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
27	RX_REE_CTRL_DATA_MASK_11	R/W	0h	TX pre cursor control: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.

**Table 12-820. RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26	RX_REE_CTRL_DATA_MASK_10	R/W	0h	Short channel correction: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
25	RX_REE_CTRL_DATA_MASK_9	R/W	0h	RX attenuation: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
24	RX_REE_CTRL_DATA_MASK_8	R/W	0h	RX VGA gain: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
23	RX_REE_CTRL_DATA_MASK_7	R/W	0h	RX offset correction coefficient: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
22	RX_REE_CTRL_DATA_MASK_6	R/W	0h	RX peaking amp gain: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
21	RX_REE_CTRL_DATA_MASK_5	R/W	0h	RX low frequency equalizer adaptive control: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
20	RX_REE_CTRL_DATA_MASK_4	R	0h	Reserved
19	RX_REE_CTRL_DATA_MASK_3	R	0h	Reserved
18	RX_REE_CTRL_DATA_MASK_2	R/W	0h	RX tap 3: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
17	RX_REE_CTRL_DATA_MASK_1	R/W	0h	RX tap 2: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
16	RX_REE_CTRL_DATA_MASK_0	R/W	0h	RX tap 1: When set to 1'b0, this REE component will be turned off when control data is being received, when either the rx_eq_training_data_valid signal going inactive, or a 1010 pattern is detected on the data signals by the REE.
15-11	RX_REE_TAP2TON_CLIP_15_11	R	0h	Reserved

**Table 12-820. RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
10-8	RX_REE_TAP2TON_CLIP_10_8	R/W	5h	<p>VGA target gain adjust multiplier: Controls how much to multiply the VGA target gain adjust by, when calculating the tap threshold. The following are valid values, and the corresponding multiplier values.</p> <p>3'b 000 : x 0.00 3'b 001 : x 0.25 3'b 010 : x 0.50 3'b 011 : x 0.75 3'b 100 : x 1.00 3'b 101 : x 1.25 3'b 110 : x 1.50 3'b 111 : x 1.75</p> <p>Note : By setting this field to 3'b000, the threshold value of the tap can be directly controlled by the threshold adjust field in this register.</p>
7-5	RX_REE_TAP2TON_CLIP_7_5	R	0h	Reserved
4-0	RX_REE_TAP2TON_CLIP_4_0	R/W	19h	<p>Threshold adjust: Controls how much the threshold can be adjusted by, after multiplying the VGA target gain adjust multiplier with the VGA target gain adjust.</p> <p>Note that this field is a positive number (not twos complement).</p> <p>Note : The threshold for the taps is equal to : +/- ((VGA target gain adjust * VGA target gain adjust multiplier) + Threshold adjust)</p>

Table 12-821. Register Call Summary for RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j

10-G SerDes Registers

- [RX_REE_CTRL_DATA_MASK__RX_REE_TAP2TON_CLIP_j Register \(Offset = 82E4h + formula\) \[reset = 40000519h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.274 RX_REE_DIAG_CTRL_RX_REE_FIFO_DIAG_j Register (Offset = 82E8h + formula) [reset = 00724000h]

RX_REE_DIAG_CTRL_RX_REE_FIFO_DIAG_j is shown in Figure 12-274 and described in Table 12-823.

Return to [Summary Table](#).

REE coefficient FIFO diagnostic register

Offset = 82E8h + (j * 400h); where j = 0h to 3h

Table 12-822.
RX_REE_DIAG_CTRL_RX_REE_FIFO_DIAG_j
Instances

Instance	Physical Address
SERDES_10G0	0505 82E8h + formula

Figure 12-274. RX_REE_DIAG_CTRL_RX_REE_FIFO_DIAG_j Register

31	30	29	28	27	26	25	24
RX_REE_DIAG_CTRL_15_8							
R-0h							
23	22	21	20	19	18	17	16
RX_REE_DIAG_CTRL_7	RX_REE_DIAG_CTRL_6	RX_REE_DIAG_CTRL_5	RX_REE_DIAG_CTRL_4	RX_REE_DIAG_CTRL_3_2		RX_REE_DIAG_CTRL_1	RX_REE_DIAG_CTRL_0
R/W-0h	R/W-1h	R/W-1h	R/W-1h	R-0h		R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
RX_REE_FIFO_DIAG_15	RX_REE_FIFO_DIAG_14	RX_REE_FIFO_DIAG_13	RX_REE_FIFO_DIAG_12	RX_REE_FIFO_DIAG_11	RX_REE_FIFO_DIAG_10	RX_REE_FIFO_DIAG_9	RX_REE_FIFO_DIAG_8
R-0h	R-1h	R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RX_REE_FIFO_DIAG_7	RX_REE_FIFO_DIAG_6	RX_REE_FIFO_DIAG_5	RX_REE_FIFO_DIAG_4	RX_REE_FIFO_DIAG_3	RX_REE_FIFO_DIAG_2	RX_REE_FIFO_DIAG_1	RX_REE_FIFO_DIAG_0
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-823. RX_REE_DIAG_CTRL_RX_REE_FIFO_DIAG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_REE_DIAG_CTRL_15_8	R	0h	Reserved
23	RX_REE_DIAG_CTRL_7	R/W	0h	Analog tap disable: When this bit is set to 1'b1, the rxda_dfe_tap_1_coef, rxda_dfe_tap_2_coef, and rxda_dfe_tap_3_coef signals being driven to the analog will be forced to all 0s.
22	RX_REE_DIAG_CTRL_6	R/W	1h	Hold periodic equalization while RX idle: When this bit is set to 1'b1, a detection of electrical idle on the receiver (rx_signal_detect is set to 1'b0), will disable the periodic REE general control state machine, and as a result freeze the current state of the parts of the REE that are controlled by it. When a high speed signal is later detected, the REE general control state machine will be enabled again.

Table 12-823. RX_REE_DIAG_CTRL_RX_REE_FIFO_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	RX_REE_DIAG_CTRL_5	R/W	1h	Hold general control state machine 2 equalization while RX idle: When this bit is set to 1'b1, a detection of electrical idle on the receiver (rx_signal_detect is set to 1'b0), will disable the REE general control state machine 2, and as a result freeze the current state of the parts of the REE that are controlled by it. When a high speed signal is later detected, the REE general control state machine will be enabled again.
20	RX_REE_DIAG_CTRL_4	R/W	1h	Hold general control state machine 1 equalization while RX idle: When this bit is set to 1'b1, a detection of electrical idle on the receiver (rx_signal_detect is set to 1'b0), will disable the REE general control state machine 1, and as a result freeze the current state of the parts of the REE that are controlled by it. When a high speed signal is later detected, the REE general control state machine will be enabled again.
19-18	RX_REE_DIAG_CTRL_3_2	R	0h	Reserved
17	RX_REE_DIAG_CTRL_1	R/W	1h	Enable REE control clock on : Enables the REE control clock. 1'b 0: Disabled 1'b 1: Enabled
16	RX_REE_DIAG_CTRL_0	R/W	0h	Force REE function clock on : When active, the REE function clock gate will allow the clock to run. Note that because of how the REE reset functions are implemented, the REE controller clock must be enabled in order for REE function clock to be enabled. Therefore, if all of the REE control state machines are disabled, the Force REE controller lock on bit in this register must also be set, for this bit to take effect.
15	RX_REE_FIFO_DIAG_15	R	0h	FIFO underflow : Indicates when a FIFO underflow condition has occurred.
14	RX_REE_FIFO_DIAG_14	R	1h	FIFO empty :Indicates that the FIFO is empty.
13	RX_REE_FIFO_DIAG_13	R/W	0h	FIFO output dequeue : Writing a 1'b1 to this bit will dequeue the current values from the output of the FIFO. Once this register bit is written to a 1'b1, it must be written to a 1'b0 before it is used again to dequeue data.
12	RX_REE_FIFO_DIAG_12	R/W	0h	FIFO output override enable : Enables the FIFO output override functions. This bit must be set to 1'b1 before enabling the transmitter REE functions. When set, FIFO output dequeues can be performed from this register. When set, the TX equalization evaluator will not be able to dequeue data from the FIFO.
11	RX_REE_FIFO_DIAG_11	R	0h	FIFO output data pre cursor increment : Current value on the pre cursor increment bit on the FIFO output.
10	RX_REE_FIFO_DIAG_10	R	0h	FIFO output data pre cursor decrement : Current value on the pre cursor decrement bit on the FIFO output.
9	RX_REE_FIFO_DIAG_9	R	0h	FIFO output data post cursor increment : Current value on the post cursor increment bit on the FIFO output.
8	RX_REE_FIFO_DIAG_8	R	0h	FIFO output data post cursor decrement : Current value on the post cursor decrement bit on the FIFO output.

Table 12-823. RX_REE_DIAG_CTRL__RX_REE_FIFO_DIAG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RX_REE_FIFO_DIAG_7	R	0h	FIFO overflow :Indicates when a FIFO overflow condition has occurred.
6	RX_REE_FIFO_DIAG_6	R	0h	FIFO full :Indicates that the FIFO is full.
5	RX_REE_FIFO_DIAG_5	R/W	0h	FIFO input enqueue : Writing a 1'b1 to this bit will enqueue the values of the FIFO input data bits in this register to their respective FIFO bits. Once this register bit is written to a 1'b1, it must be written to a 1'b0 before it is used again to dequeue data.
4	RX_REE_FIFO_DIAG_4	R/W	0h	FIFO input override enable : Enables the FIFO input override functions. This bit must be set to 1'b1 before enabling the transmitter REE functions. When set, FIFO input enqueues can be performed from this register. When set, the TX pre cursor control and TX post cursor control will not be able to enqueue data to the FIFO.
3	RX_REE_FIFO_DIAG_3	R/W	0h	FIFO input data pre cursor increment : Pre cursor increment value that will be enqueued to the FIFO by the FIFO input enqueue bit in this register.
2	RX_REE_FIFO_DIAG_2	R/W	0h	FIFO input data pre cursor decrement : Pre cursor decrement value that will be enqueued to the FIFO by the FIFO input enqueue bit in this register.
1	RX_REE_FIFO_DIAG_1	R/W	0h	FIFO input data post cursor increment : Post cursor increment value that will be enqueued to the FIFO by the FIFO input enqueue bit in this register.
0	RX_REE_FIFO_DIAG_0	R/W	0h	FIFO input data post cursor decrement : Post cursor decrement value that will be enqueued to the FIFO by the FIFO input enqueue bit in this register.

Table 12-824. Register Call Summary for RX_REE_DIAG_CTRL__RX_REE_FIFO_DIAG_j

10-G SerDes Registers

- [RX_REE_DIAG_CTRL__RX_REE_FIFO_DIAG_j Register \(Offset = 82E8h + formula\) \[reset = 00724000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.275 RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j Register (Offset = 82ECh + formula) [reset = 06F60000h]

RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j is shown in Figure 12-275 and described in Table 12-826.

Return to [Summary Table](#).

REE TX equalization evaluator control register

Offset = 82ECh + (j * 400h); where j = 0h to 3h

**Table 12-825. RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 82ECh + formula

Figure 12-275. RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j Register

31	30	29	28	27	26	25	24
RX_REE_SMGM_CTRL1_15_12				RX_REE_SMGM_CTRL1_11	RX_REE_SMGM_CTRL1_10	RX_REE_SMGM_CTRL1_9	RX_REE_SMGM_CTRL1_8
R-0h				R/W-0h	R/W-1h	R/W-1h	R/W-0h
23	22	21	20	19	18	17	16
RX_REE_SMGM_CTRL1_7	RX_REE_SMGM_CTRL1_6	RX_REE_SMGM_CTRL1_5	RX_REE_SMGM_CTRL1_4	RX_REE_SMGM_CTRL1_3	RX_REE_SMGM_CTRL1_2	RX_REE_SMGM_CTRL1_1	RX_REE_SMGM_CTRL1_0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
RX_REE_TXEQEVAL_CTRL_15_2							
R-0h							
7	6	5	4	3	2	1	0
RX_REE_TXEQEVAL_CTRL_15_2						RX_REE_TXEQEVAL_CTRL_1	RX_REE_TXEQEVAL_CTRL_0
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-826. RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RX_REE_SMGM_CTRL1_15_12	R	0h	Reserved
27	RX_REE_SMGM_CTRL1_11	R/W	0h	REE Periodic general control state machine enable standard mode 3: This bit will control if the REE periodic general control state machine will run, when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled
26	RX_REE_SMGM_CTRL1_10	R/W	1h	REE Periodic general control state machine enable standard mode 2: This bit will control if the REE periodic general control state machine will run, when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled

**Table 12-826. RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
25	RX_REE_SMGM_CTRL1_9	R/W	1h	REE Periodic general control state machine enable standard mode 1: This bit will control if the REE periodic general control state machine will run, when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
24	RX_REE_SMGM_CTRL1_8	R/W	0h	REE Periodic general control state machine enable standard mode 0: This bit will control if the REE periodic general control state machine will run, when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled
23	RX_REE_SMGM_CTRL1_7	R/W	1h	REE general control state machine 2 enable standard mode 3: This bit will control if the REE general control state machine 2 will run, when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled
22	RX_REE_SMGM_CTRL1_6	R/W	1h	REE general control state machine 2 enable standard mode 2: This bit will control if the REE general control state machine 2 will run, when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled
21	RX_REE_SMGM_CTRL1_5	R/W	1h	REE general control state machine 2 enable standard mode 1: This bit will control if the REE general control state machine 2 will run, when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
20	RX_REE_SMGM_CTRL1_4	R/W	1h	REE general control state machine 2 enable standard mode 0: This bit will control if the REE general control state machine 2 will run, when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled
19	RX_REE_SMGM_CTRL1_3	R/W	0h	REE general control state machine 1 enable standard mode 3: This bit will control if the REE general control state machine 1 will run, when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled
18	RX_REE_SMGM_CTRL1_2	R/W	1h	REE general control state machine 1 enable standard mode 2: This bit will control if the REE general control state machine 1 will run, when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled
17	RX_REE_SMGM_CTRL1_1	R/W	1h	REE general control state machine 1 enable standard mode 1: This bit will control if the REE general control state machine 1 will run, when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
16	RX_REE_SMGM_CTRL1_0	R/W	0h	REE general control state machine 1 enable standard mode 0: This bit will control if the REE general control state machine 1 will run, when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled

Table 12-826. RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
15-2	RX_REE_TXEQEVAL_CTRL_15_2	R	0h	Reserved
1	RX_REE_TXEQEVAL_CTRL_1	R/W	0h	TX equalization evaluation counter reset on gen mode change: Controls if the incremental evaluation counter will be reset to its starting value when changing gen modes. When enabled, the reset will take place on the first equalization evaluation after a gen mode change has taken place. 1'b 0 : Gen mode change reset disabled. 1'b 1 : Gen mode change reset enabled.
0	RX_REE_TXEQEVAL_CTRL_0	R/W	0h	TX main coefficient direction change control: This bit controls the function of the main coefficient direction change. 1'b 0 : The main coefficient will always return a value of no change (2'b00), no matter what the pre and post cursor coefficient direction changes are. 1'b 1 : The main coefficient will generate a return value as a function of the pre and post cursor coefficient direction change. If an increment request exists on the pre or post cursor coefficient direction change, a decrement request will be returned for the main coefficient. Similarly, if a decrement request exists on the pre or post cursor coefficient direction change, an increment request will be returned for the main coefficient.

Table 12-827. Register Call Summary for RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_REE_SMGM_CTRL1__RX_REE_TXEQEVAL_CTRL_j Register \(Offset = 82ECh + formula\) \[reset = 06F60000h\]: \[0\]](#)

12.276 RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j Register (Offset = 82F0h + formula) [reset = 4606h]

[RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j](#) is shown in [Figure 12-276](#) and described in [Table 12-829](#).

Return to [Summary Table](#).

REE control state machine gen mode control register 2

Offset = 82F0h + (j * 400h); where j = 0h to 3h

Table 12-828. RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j Instances

Instance	Physical Address
SERDES_10G0	0505 82F0h + formula

Figure 12-276. RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j Register

31	30	29	28	27	26	25	24
RX_REE_TXEQEVAL_PRE_15_14		RX_REE_TXEQEVAL_PRE_13_8					
R-0h		R-0h					
23	22	21	20	19	18	17	16
RX_REE_TXEQEVAL_PRE_7_6		RX_REE_TXEQEVAL_PRE_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RX_REE_SMGM_CTRL2_15	RX_REE_SMGM_CTRL2_14	RX_REE_SMGM_CTRL2_13	RX_REE_SMGM_CTRL2_12	RX_REE_SMGM_CTRL2_11	RX_REE_SMGM_CTRL2_10	RX_REE_SMGM_CTRL2_9	RX_REE_SMGM_CTRL2_8
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h
7	6	5	4	3	2	1	0
RX_REE_SMGM_CTRL2_7	RX_REE_SMGM_CTRL2_6	RX_REE_SMGM_CTRL2_5	RX_REE_SMGM_CTRL2_4	RX_REE_SMGM_CTRL2_3	RX_REE_SMGM_CTRL2_2	RX_REE_SMGM_CTRL2_1	RX_REE_SMGM_CTRL2_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-829. RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RX_REE_TXEQEVAL_PRE_15_14	R	0h	Reserved
29-24	RX_REE_TXEQEVAL_PRE_13_8	R	0h	TX equalization evaluator pre-emphasis increment count: Contains a count of the total number of pre-emphasis increment responses that have taken place during the TX equalization evaluator process.
23-22	RX_REE_TXEQEVAL_PRE_7_6	R	0h	Reserved
21-16	RX_REE_TXEQEVAL_PRE_5_0	R	0h	TX equalization evaluator pre-emphasis decrement count: Contains a count of the total number of pre-emphasis decrement responses that have taken place during the TX equalization evaluator process.
15	RX_REE_SMGM_CTRL2_15	R/W	0h	REE PCIe Gen 3 TX equalization state machine E path enable standard mode 3: This bit controls if the REE PCIe Gen 3 TX equalization state machine will enable the analog E path when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled

**Table 12-829. RX_REE_TXEQEVAL_PRE_RX_REE_SMGM_CTRL2_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
14	RX_REE_SMGM_CTRL2_14	R/W	1h	REE PCIe Gen 3 TX equalization state machine E path en standard mode 2: This bit controls if the REE PCIe Gen 3 TX equalization state machine will enable the analog E path when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled
13	RX_REE_SMGM_CTRL2_13	R/W	0h	REE PCIe Gen 3 TX equalization state machine E path en standard mode 1: This bit controls if the REE PCIe Gen 3 TX equalization state machine will enable the analog E path when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
12	RX_REE_SMGM_CTRL2_12	R/W	0h	REE PCIe Gen 3 TX equalization state machine E path en standard mode 0: This bit controls if the REE PCIe Gen 3 TX equalization state machine will enable the analog E path when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled
11	RX_REE_SMGM_CTRL2_11	R/W	0h	REE Periodic general control state machine E path en standard mode 3: This bit controls if the REE periodic general control state machine will enable the analog E path when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled
10	RX_REE_SMGM_CTRL2_10	R/W	1h	REE Periodic general control state machine E path en standard mode 2: This bit controls if the REE periodic general control state machine will enable the analog E path when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled
9	RX_REE_SMGM_CTRL2_9	R/W	1h	REE Periodic general control state machine E path en standard mode 1: This bit controls if the REE periodic general control state machine will enable the analog E path when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
8	RX_REE_SMGM_CTRL2_8	R/W	0h	REE Periodic general control state machine E path en standard mode 0: This bit controls if the REE periodic general control state machine will enable the analog E path when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled
7	RX_REE_SMGM_CTRL2_7	R/W	0h	REE general control state machine 2 E path en standard mode 3: This bit controls if the REE general control state machine 2 will enable the analog E path when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled

**Table 12-829. RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
6	RX_REE_SMGM_CTRL2_6	R/W	0h	REE general control state machine 2 E path en standard mode 2: This bit controls if the REE general control state machine 2 will enable the analog E path when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled
5	RX_REE_SMGM_CTRL2_5	R/W	0h	REE general control state machine 2 E path en standard mode 1: This bit controls if the REE general control state machine 2 will enable the analog E path when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
4	RX_REE_SMGM_CTRL2_4	R/W	0h	REE general control state machine 2 E path en standard mode 0: This bit controls if the REE general control state machine 2 will enable the analog E path when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled
3	RX_REE_SMGM_CTRL2_3	R/W	0h	REE general control state machine 1 E path en standard mode 3: This bit controls if the REE general control state machine 1 will enable the analog E path when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled
2	RX_REE_SMGM_CTRL2_2	R/W	1h	REE general control state machine 1 E path en standard mode 2: This bit controls if the REE general control state machine 1 will enable the analog E path when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled
1	RX_REE_SMGM_CTRL2_1	R/W	1h	REE general control state machine 1 E path en standard mode 1: This bit controls if the REE general control state machine 1 will enable the analog E path when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
0	RX_REE_SMGM_CTRL2_0	R/W	0h	REE general control state machine 1 E path en standard mode 0: This bit controls if the REE general control state machine 1 will enable the analog E path when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled

Table 12-830. Register Call Summary for RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j

10-G SerDes Registers

- [RX_REE_TXEQEVAL_PRE__RX_REE_SMGM_CTRL2_j Register \(Offset = 82F0h + formula\) \[reset = 4606h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.277 RX_REE_TXEQEVAL_POST_j Register (Offset = 82F4h + formula) [reset = X]

RX_REE_TXEQEVAL_POST_j is shown in Figure 12-277 and described in Table 12-832.

Return to [Summary Table](#).

REE TX equalization evaluator post-emphasis register

Offset = 82F4h + (j * 400h); where j = 0h to 3h

Table 12-831. RX_REE_TXEQEVAL_POST_j Instances

Instance	Physical Address
SERDES_10G0	0505 82F4h + formula

Figure 12-277. RX_REE_TXEQEVAL_POST_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RX_REE_TXEQEVAL_POST_15_14		RX_REE_TXEQEVAL_POST_13_8					
R-0h		R-0h					
7	6	5	4	3	2	1	0
RX_REE_TXEQEVAL_POST_7_6		RX_REE_TXEQEVAL_POST_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 12-832. RX_REE_TXEQEVAL_POST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-14	RX_REE_TXEQEVAL_POST_15_14	R	0h	Reserved
13-8	RX_REE_TXEQEVAL_POST_13_8	R	0h	TX equalization evaluator post-emphasis increment count: Contains a count of the total number of post-emphasis increment responses that have taken place during the TX equalization evaluator process.
7-6	RX_REE_TXEQEVAL_POST_7_6	R	0h	Reserved
5-0	RX_REE_TXEQEVAL_POST_5_0	R	0h	TX equalization evaluator post-emphasis decrement count: Contains a count of the total number of post-emphasis decrement responses that have taken place during the TX equalization evaluator process.

Table 12-833. Register Call Summary for RX_REE_TXEQEVAL_POST_j

10-G SerDes Registers

- [RX_REE_TXEQEVAL_POST_j Register \(Offset = 82F4h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.278 XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j Register (Offset = 8380h + formula) [reset = 0h]

XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j is shown in Figure 12-278 and described in Table 12-835.

Return to [Summary Table](#).

Clock frequency measurement control register

Offset = 8380h + (j * 400h); where j = 0h to 3h

Table 12-834.
XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 8380h + formula

Figure 12-278. XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j Register

31	30	29	28	27	26	25	24
XCVR_CMSMT_TEST_CLK_SEL_15_3							
R-0h							
23	22	21	20	19	18	17	16
XCVR_CMSMT_TEST_CLK_SEL_15_3				XCVR_CMSMT_TEST_CLK_SEL_2_0			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_15	XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_14	XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_13_0					
R/W-0h	R-0h	R-0h					
7	6	5	4	3	2	1	0
XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_13_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-835. XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j Register
Field Descriptions

Bit	Field	Type	Reset	Description
31-19	XCVR_CMSMT_TEST_CLK_SEL_15_3	R	0h	Reserved
18-16	XCVR_CMSMT_TEST_CLK_SEL_2_0	R/W	0h	Test clock select: This field drives the test_clk_select pin, in order to control an external MUX for selecting between multiple test clocks to measure. The following is the encoding for this field, and the clock each value selects. 3'b 000 : Transmitter data clock 3'b 001 : Serializer clock 3'b 010 : Receiver data clock 3'b 011 : Deserializer clock 3'b 100 : Receiver 2X data clock 3'b 101 : Deserializer 2X clock 3'b 110 : Signal detect clock 3'b 111 : Reserved

Table 12-835. XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	XCVR_CMSMT_CLK_FR EQ_MSMT_CTRL_15	R/W	0h	Run test clock measurement: Activating (1'b1) this bit will run the test clock measurement process. This bit must remain active until the test clock measurement process is complete, as indicated by the test clock measurement done bit in this register. To start another measurement process, this bit must first be driven inactive then driven active again. Note: Both of the clocks used to generate the ref_clk and test_clk clocks must be active prior to setting or clearing this bit. Note: The values in the Test clock selection register and Reference clock timer value register must be set prior to activating this bit.
14	XCVR_CMSMT_CLK_FR EQ_MSMT_CTRL_14	R	0h	Test clock measurement done: This bit will be set to 1'b1 when the test clock measurement process is complete. It will be cleared by the deactivation of the start test clock measurement bit in this register.
13-0	XCVR_CMSMT_CLK_FR EQ_MSMT_CTRL_13_0	R	0h	Reserved

**Table 12-836. Register Call Summary for
XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j**

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [XCVR_CMSMT_TEST_CLK_SEL__XCVR_CMSMT_CLK_FREQ_MSMT_CTRL_j Register \(Offset = 8380h + formula\) \[reset = 0h\]: \[0\]](#)

12.279 XCVR_CMSMT_TEST_CLK_CNT_VALUE__XCVR_CMSMT_REF_CLK_TMR_VALUE_j Register (Offset = 8384h + formula) [reset = 0h]

XCVR_CMSMT_TEST_CLK_CNT_VALUE__XCVR_CMSMT_REF_CLK_TMR_VALUE_j is shown in Figure 12-279 and described in Table 12-838.

Return to [Summary Table](#).

Reference clock timer value register

Offset = 8384h + (j * 400h); where j = 0h to 3h

Table 12-837.
XCVR_CMSMT_TEST_CLK_CNT_VALUE__XCVR_CMSMT_REF_CLK_TMR_VA
LUE_j Instances

Instance	Physical Address
SERDES_10G0	0505 8384h + formula

Figure 12-279. XCVR_CMSMT_TEST_CLK_CNT_VALUE__XCVR_CMSMT_REF_CLK_TMR_VALUE_j Register

31	30	29	28	27	26	25	24
XCVR_CMSMT_TEST_CLK_CNT_VALUE_15_12				XCVR_CMSMT_TEST_CLK_CNT_VALUE_11_0			
R-0h				R-0h			
23	22	21	20	19	18	17	16
XCVR_CMSMT_TEST_CLK_CNT_VALUE_11_0							
R-0h							
15	14	13	12	11	10	9	8
XCVR_CMSMT_REF_CLK_TMR_VALUE_15_12				XCVR_CMSMT_REF_CLK_TMR_VALUE_11_0			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
XCVR_CMSMT_REF_CLK_TMR_VALUE_11_0							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-838. XCVR_CMSMT_TEST_CLK_CNT_VALUE__XCVR_CMSMT_REF_CLK_TMR_VALUE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	XCVR_CMSMT_TEST_CLK_CNT_VALUE_15_12	R	0h	Reserved
27-16	XCVR_CMSMT_TEST_CLK_CNT_VALUE_11_0	R	0h	Test clock counter value: When the test clock measurement process is complete, the value in this field specifies the number of test clock cycles that were counted in the time specified by the reference clock timer value. This field is only valid while the test clock measurement done bit in the Clock frequency measurement control register is active.
15-12	XCVR_CMSMT_REF_CLK_TMR_VALUE_15_12	R	0h	Reserved
11-0	XCVR_CMSMT_REF_CLK_TMR_VALUE_11_0	R/W	0h	Reference clock timer value : This specifies the amount of time, in reference clock cycles, to count test clock cycles. This value minus 1 is loaded into the reference clock timer. A value of 0 for this field is not valid when running this function.

**Table 12-839. Register Call Summary for
XCVR_CMSMT_TEST_CLK_CNT_VALUE__XCVR_CMSMT_REF_CLK_TMR_VALUE_j**

10-G SerDes Registers

- [10-G SerDes Registers](#): [0]
- [XCVR_CMSMT_TEST_CLK_CNT_VALUE__XCVR_CMSMT_REF_CLK_TMR_VALUE_j](#) Register (Offset = 8384h + formula) [reset = 0h]: [0]

12.280 RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j Register (Offset = 83C0h + formula) [reset = 4DDD0004h]

RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j is shown in Figure 12-280 and described in Table 12-841.

Return to [Summary Table](#).

Receiver DFE control register

Offset = 83C0h + (j * 400h); where j = 0h to 3h

Table 12-840. RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 83C0h + formula

Figure 12-280. RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j Register

31	30	29	28	27	26	25	24
RX_DIAG_DFE_AMP_TUNE_1_5	RX_DIAG_DFE_AMP_TUNE_14_12			RX_DIAG_DFE_AMP_TUNE_1_1	RX_DIAG_DFE_AMP_TUNE_10_8		
R-0h		R/W-4h		R/W-1h		R/W-5h	
23	22	21	20	19	18	17	16
RX_DIAG_DFE_AMP_TUNE_7	RX_DIAG_DFE_AMP_TUNE_6_4			RX_DIAG_DFE_AMP_TUNE_3	RX_DIAG_DFE_AMP_TUNE_2_0		
R/W-1h		R/W-5h		R/W-1h		R/W-5h	
15	14	13	12	11	10	9	8
RX_DIAG_DFE_CTRL_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_DIAG_DFE_CTRL_15_4				RX_DIAG_DFE_CTRL_3	RX_DIAG_DFE_CTRL_2	RX_DIAG_DFE_CTRL_1	RX_DIAG_DFE_CTRL_0
R-0h				R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-841. RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_DIAG_DFE_AMP_TUNE_15	R	0h	Reserved
30-28	RX_DIAG_DFE_AMP_TUNE_14_12	R/W	4h	DFE constant gm bias tune: Adjusts the constant gm bias. 3'b000: -34 uA 3'b001 3'b010 3'b011 3'b100: - 50 uA 3'b101 3'b110 3'b111: -62 uA
27	RX_DIAG_DFE_AMP_TUNE_11	R/W	1h	DFE VGA constant gm bias enable: Enables the VGA constant gm bias. This bit drives the rxda_vga_cnst_gm_en signal going to the analog. 1'b 0 : Disabled. 1'b 1 : Enabled.

**Table 12-841. RX_DIAG_DFE_AMP_TUNE_RX_DIAG_DFE_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
26-24	RX_DIAG_DFE_AMP_TUNE_10_8	R/W	5h	DFE VGA amp current adjust: Adjusts the current for the DFE VGA amp, using the rxd_a_vga_current_adj signal, as specified below. Note that the percentages are approximate values. 3'b 000: +30% (maximum) ... 3'b 101: 0% ... 3'b 111: -30% (minimum)
23	RX_DIAG_DFE_AMP_TUNE_7	R/W	1h	DFE peaking constant gm bias enable: Enables the peaking constant gm bias. This bit drives the rxd_a_peak_cnst_gm_en signal going to the analog. 1'b 0 : Disabled. 1'b 1 : Enabled.
22-20	RX_DIAG_DFE_AMP_TUNE_6_4	R/W	5h	DFE peaking amp current adjust: Adjusts the current for the DFE peaking amp, using the rxd_a_peak_current_adj signal, as specified below. Note that the percentages are approximate values. 3'b 000: +30% (maximum) ... 3'b 101: 0% ... 3'b 111: -30% (minimum)
19	RX_DIAG_DFE_AMP_TUNE_3	R/W	1h	DFE summing constant gm bias enable: Enables the summing constant gm bias. This bit drives the rxd_a_sum_cnst_gm_en signal going to the analog. 1'b 0 : Disabled. 1'b 1 : Enabled.
18-16	RX_DIAG_DFE_AMP_TUNE_2_0	R/W	5h	DFE summing amp current adjust: Adjusts the current for the DFE summing amp, using the rxd_a_sum_current_adj signal, as specified below. Note that the percentages are approximate values. 3'b 000: +30% (maximum) ... 3'b 101: 0% ... 3'b 111: -30% (minimum)
15-4	RX_DIAG_DFE_CTRL_15_4	R	0h	Reserved
3	RX_DIAG_DFE_CTRL_3	R/W	0h	Receiver DFE low frequency equalization enable value standard mode 3: This bit controls the rxd_a_dfe_lfq_en signal going to the analog, which is used to enable the receiver DFE low frequency equalization analog circuits, when xcvr_standard_mode is set to 2'b11. 1'b 0 : Disabled 1'b 1 : Enabled

**Table 12-841. RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2	RX_DIAG_DFE_CTRL_2	R/W	1h	Receiver DFE low frequency equalization enable value standard mode 2: This bit controls the rxda_dfe_lfq_en signal going to the analog, which is used to enable the receiver DFE low frequency equalization analog circuits, when xcvr_standard_mode is set to 2'b10. 1'b 0 : Disabled 1'b 1 : Enabled
1	RX_DIAG_DFE_CTRL_1	R/W	0h	Receiver DFE low frequency equalization enable value standard mode 1: This bit controls the rxda_dfe_lfq_en signal going to the analog, which is used to enable the receiver DFE low frequency equalization analog circuits, when xcvr_standard_mode is set to 2'b01. 1'b 0 : Disabled 1'b 1 : Enabled
0	RX_DIAG_DFE_CTRL_0	R/W	0h	Receiver DFE low frequency equalization enable value standard mode 0: This bit controls the rxda_dfe_lfq_en signal going to the analog, which is used to enable the receiver DFE low frequency equalization analog circuits, when xcvr_standard_mode is set to 2'b00. 1'b 0 : Disabled 1'b 1 : Enabled

Table 12-842. Register Call Summary for RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_DIAG_DFE_AMP_TUNE__RX_DIAG_DFE_CTRL_j Register \(Offset = 83C0h + formula\) \[reset = 4DDD0004h\]: \[0\]](#)

12.281 RX_DIAG_DFE_AMP_TUNE_3__RX_DIAG_DFE_AMP_TUNE_2_j Register (Offset = 83C4h + formula) [reset = C01h]

RX_DIAG_DFE_AMP_TUNE_3__RX_DIAG_DFE_AMP_TUNE_2_j is shown in Figure 12-281 and described in Table 12-844.

Return to [Summary Table](#).

DFE amp fine tuning 2 register

Offset = 83C4h + (j * 400h); where j = 0h to 3h

Table 12-843. RX_DIAG_DFE_AMP_TUNE_3__RX_DIAG_DFE_AMP_TUNE_2_j Instances

Instance	Physical Address
SERDES_10G0	0505 83C4h + formula

Figure 12-281. RX_DIAG_DFE_AMP_TUNE_3__RX_DIAG_DFE_AMP_TUNE_2_j Register

31	30	29	28	27	26	25	24
RX_DIAG_DFE_AMP_TUNE_3_15_4							
R-0h							
23	22	21	20	19	18	17	16
RX_DIAG_DFE_AMP_TUNE_3_15_4				RX_DIAG_DFE_AMP_TUNE_3_3	RX_DIAG_DFE_AMP_TUNE_3_2	RX_DIAG_DFE_AMP_TUNE_3_1	RX_DIAG_DFE_AMP_TUNE_3_0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RX_DIAG_DFE_AMP_TUNE_2_15_14		RX_DIAG_DFE_AMP_TUNE_2_13_12		RX_DIAG_DFE_AMP_TUNE_2_11	RX_DIAG_DFE_AMP_TUNE_2_10_8		
R-0h		R/W-0h		R/W-1h	R/W-4h		
7	6	5	4	3	2	1	0
RX_DIAG_DFE_AMP_TUNE_2_7	RX_DIAG_DFE_AMP_TUNE_2_6	RX_DIAG_DFE_AMP_TUNE_2_5	RX_DIAG_DFE_AMP_TUNE_2_4	RX_DIAG_DFE_AMP_TUNE_2_3_2		RX_DIAG_DFE_AMP_TUNE_2_1_0	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-844. RX_DIAG_DFE_AMP_TUNE_3__RX_DIAG_DFE_AMP_TUNE_2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RX_DIAG_DFE_AMP_TUNE_3_15_4	R	0h	Reserved
19	RX_DIAG_DFE_AMP_TUNE_3_3	R/W	0h	DFE VGA stage 1 boost standard mode 3: This bit enables the active inductors boost function in stage 1 of the VGA, for high data rates, when xcvr_standard_mode is set to 2'b11. This bit controls the rxda_vga_st1_actind_en signal going to the analog. 1'b 0 : Disabled 1'b 1 : Enabled

Table 12-844. RX_DIAG_DFE_AMP_TUNE_3_RX_DIAG_DFE_AMP_TUNE_2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	RX_DIAG_DFE_AMP_TUNE_3_2	R/W	0h	DFE VGA stage 1 boost standard mode 2: This bit enables the active inductors boost function in stage 1 of the VGA, for high data rates, when xcvr_standard_mode is set to 2'b10. This bit controls the rxd_vga_st1_actind_en signal going to the analog. 1'b 0 : Disabled 1'b 1 : Enabled
17	RX_DIAG_DFE_AMP_TUNE_3_1	R/W	0h	DFE VGA stage 1 boost standard mode 1: This bit enables the active inductors boost function in stage 1 of the VGA, for high data rates, when xcvr_standard_mode is set to 2'b01. This bit controls the rxd_vga_st1_actind_en signal going to the analog. 1'b 0 : Disabled 1'b 1 : Enabled
16	RX_DIAG_DFE_AMP_TUNE_3_0	R/W	0h	DFE VGA stage 1 boost standard mode 0: This bit enables the active inductors boost function in stage 1 of the VGA, for high data rates, when xcvr_standard_mode is set to 2'b00. This bit controls the rxd_vga_st1_actind_en signal going to the analog. 1'b 0 : Disabled 1'b 1 : Enabled
15-14	RX_DIAG_DFE_AMP_TUNE_2_15_14	R	0h	Reserved
13-12	RX_DIAG_DFE_AMP_TUNE_2_13_12	R/W	0h	Receiver peaking amp common mode adjust: Adjusts the common mode voltage for the receiver peaking amp, by driving the rxd_fe_pkamp_cm_adj signal to the analog. 2'b 00 : Nominal common mode voltage. 2'b 01 : Reduces the common mode voltage by one step. 2'b 10 : Increases the common mode voltage by one step. 2'b 11 : Reserved
11	RX_DIAG_DFE_AMP_TUNE_2_11	R/W	1h	DFE low frequency equalizer constant gm bias enable: Enables the low frequency equalizer constant gm bias. This bit drives the rxd_lfeq_cnst_gm_en signal going to the analog. 1'b 0 : Disabled. 1'b 1 : Enabled.
10-8	RX_DIAG_DFE_AMP_TUNE_2_10_8	R/W	4h	DFE low frequency equalizer current adjust: Adjusts the current for the DFE low frequency equalizer, using the rxd_lfeq_current_adj signal, as specified below. Note that the percentages are approximate values. 3'b 000: +30% (maximum) ... 3'b 101: 0% ... 3'b 111: -30% (minimum)
7	RX_DIAG_DFE_AMP_TUNE_2_7	R/W	0h	DFE peaking amp boost: Enables the active inductors boost function in the peaking amp, for high data rates. This bit controls the rxd_peak_actind_en signal going to the analog. 1'b 0 : Disabled 1'b 1 : Enabled
6	RX_DIAG_DFE_AMP_TUNE_2_6	R/W	0h	Reserved - Spare

Table 12-844. RX_DIAG_DFE_AMP_TUNE_3_RX_DIAG_DFE_AMP_TUNE_2_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RX_DIAG_DFE_AMP_TUNE_2_5	R/W	0h	DFE VGA stage 2 boost: Enables the active inductors boost function in stage 2 of the VGA, for high data rates. This bit controls the rxd_vga_st2_actind_en signal going to the analog. 1'b 0 : Disabled 1'b 1 : Enabled
4	RX_DIAG_DFE_AMP_TUNE_2_4	R/W	0h	DFE RX Tap 1 DAC Range Select: Controls the tap 1 DAC range in the analog DFE. This bit controls the rxd_dfe_tap_1_range signal going to the analog. 1'b 0: Normal operation 1'b 1: The tap 1 DAC range is increased.
3-2	RX_DIAG_DFE_AMP_TUNE_2_3_2	R	0h	Reserved
1-0	RX_DIAG_DFE_AMP_TUNE_2_1_0	R/W	1h	DFE RX amp current adjust: Adjusts the mix of constant-gm and External Current for RX front end amplifiers. This controls the rxd_cnstgm_ext_sel signal going into the analog. The encoding of the rxd_cnstgm_ext_sel signal, as a function of the values in this register is specified below. 2'b 00 =X 3'b 000 : gm_bias = 25u, ext = 25u, total = 50u 2'b 01 =X 3'b 001 : gm_bias = 30u, ext = 20u, total = 50u 2'b 10 =X 3'b 011 : gm_bias = 35u, ext = 15u, total = 50u 2'b 11 =X 3'b 111 : gm_bias = 40u, ext = 10u, total = 50u

Table 12-845. Register Call Summary for RX_DIAG_DFE_AMP_TUNE_3_RX_DIAG_DFE_AMP_TUNE_2_j

10-G SerDes Registers
<ul style="list-style-type: none"> RX_DIAG_DFE_AMP_TUNE_3_RX_DIAG_DFE_AMP_TUNE_2_j Register (Offset = 83C4h + formula) [reset = C01h]: [0] 10-G SerDes Registers: [0]

12.282 RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j Register (Offset = 83C8h + formula) [reset = 0B980004h]

[RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j](#) is shown in [Figure 12-282](#) and described in [Table 12-847](#).

Return to [Summary Table](#).

REE DAC control register

Offset = 83C8h + (j * 400h); where j = 0h to 3h

Table 12-846. RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 83C8h + formula

Figure 12-282. RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j Register

31	30	29	28	27	26	25	24
RX_DIAG_NQST_CTRL_15_12				RX_DIAG_NQST_CTRL_11_8			
R/W-0h				R/W-Bh			
23	22	21	20	19	18	17	16
RX_DIAG_NQST_CTRL_7_4				RX_DIAG_NQST_CTRL_3_0			
R/W-9h				R/W-8h			
15	14	13	12	11	10	9	8
RX_DIAG_REE_DAC_CTRL_15_3							
R-0h							
7	6	5	4	3	2	1	0
RX_DIAG_REE_DAC_CTRL_15_3				RX_DIAG_REE_DAC_CTRL_2		RX_DIAG_REE_DAC_CTRL_1	RX_DIAG_REE_DAC_CTRL_0
R-0h				R/W-1h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-847. RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RX_DIAG_NQST_CTRL_15_12	R/W	0h	RX nyquist select value standard mode 3: This field specifies the receiver DFE nyquist frequency select value on the rxda_dfe_nqst_sel signal driven to the analog, when xcvr_standard_mode is set to 2'b11.
27-24	RX_DIAG_NQST_CTRL_11_8	R/W	Bh	RX nyquist select value standard mode 2: This field specifies the receiver DFE nyquist frequency select value on the rxda_dfe_nqst_sel signal driven to the analog, when xcvr_standard_mode is set to 2'b10.
23-20	RX_DIAG_NQST_CTRL_7_4	R/W	9h	RX nyquist select value standard mode 1: This field specifies the receiver DFE nyquist frequency select value on the rxda_dfe_nqst_sel signal driven to the analog, when xcvr_standard_mode is set to 2'b01.
19-16	RX_DIAG_NQST_CTRL_3_0	R/W	8h	RX nyquist select value standard mode 0: This field specifies the receiver DFE nyquist frequency select value on the rxda_dfe_nqst_sel signal driven to the analog, when xcvr_standard_mode is set to 2'b00.
15-3	RX_DIAG_REE_DAC_CTRL_15_3	R	0h	Reserved

**Table 12-847. RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2	RX_DIAG_REE_DAC_CTL RL_2	R/W	1h	DFE Offset DAC enable: Enables the DFE offset DAC associated with the VGA amp. 1'b 0: Disabled. 1'b 1: Enabled.
1	RX_DIAG_REE_DAC_CTL RL_1	R/W	0h	DFE Offset DAC attenuation: Adds attenuation to the DFE offset DAC associated with the VGA amp. 1'b 0: No attenuation. 1'b 1: DAC gain attenuated by 40%.
0	RX_DIAG_REE_DAC_CTL RL_0	R/W	0h	DFE DAC attenuation: Adds attenuation to the DFE DACs associated with the summing amp. 1'b 0: No attenuation. 1'b 1: DAC gain attenuated by 30%.

Table 12-848. Register Call Summary for RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_DIAG_NQST_CTRL__RX_DIAG_REE_DAC_CTRL_j Register \(Offset = 83C8h + formula\) \[reset = 0B980004h\]: \[0\]](#)

12.283 RX_DIAG_LFEQ_TUNE_j Register (Offset = 83CCh + formula) [reset = X]

RX_DIAG_LFEQ_TUNE_j is shown in [Figure 12-283](#) and described in [Table 12-850](#).

Return to [Summary Table](#).

Low frequency equalizer tuning register

Offset = 83CCh + (j * 400h); where j = 0h to 3h

Table 12-849. RX_DIAG_LFEQ_TUNE_j Instances

Instance	Physical Address
SERDES_10G0	0505 83CCh + formula

Figure 12-283. RX_DIAG_LFEQ_TUNE_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_DIAG_LFEQ_TUNE_15_8							
R-0h							
7	6	5	4	3	2	1	0
RX_DIAG_LFEQ_TUNE_7_6		RX_DIAG_LFEQ_TUNE_5_4		RX_DIAG_LFEQ_TUNE_3_2		RX_DIAG_LFEQ_TUNE_1_0	
R/W-3h		R/W-2h		R/W-1h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-850. RX_DIAG_LFEQ_TUNE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	RX_DIAG_LFEQ_TUNE_15_8	R	0h	Reserved
7-6	RX_DIAG_LFEQ_TUNE_7_6	R/W	3h	RX low frequency equalization zero frequency value standard mode 3: This field specifies the receiver zero frequency setting for the low frequency equalization function, by driving the rxda_dfe_lfeq_zero_freq signal going into the analog, when xcvr_standard_mode is set to 2'b11. 2'b 00 : 150 MHz 2'b 01 : 200 MHz 2'b 10 : 250 MHz 2'b 11 : 300 MHz
5-4	RX_DIAG_LFEQ_TUNE_5_4	R/W	2h	RX low frequency equalization zero frequency value standard mode 2: This field specifies the receiver zero frequency setting for the low frequency equalization function, by driving the rxda_dfe_lfeq_zero_freq signal going into the analog, when xcvr_standard_mode is set to 2'b10. 2'b 00 : 150 MHz 2'b 01 : 200 MHz 2'b 10 : 250 MHz 2'b 11 : 300 MHz

Table 12-850. RX_DIAG_LFEQ_TUNE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	RX_DIAG_LFEQ_TUNE_3_2	R/W	1h	RX low frequency equalization zero frequency value standard mode 1: This field specifies the receiver zero frequency setting for the low frequency equalization function, by driving the rxda_dfe_lfeq_zero_freq signal going into the analog, when xcvr_standard_mode is set to 2'b01. 2'b 00 : 150 MHz 2'b 01 : 200 MHz 2'b 10 : 250 MHz 2'b 11 : 300 MHz
1-0	RX_DIAG_LFEQ_TUNE_1_0	R/W	0h	RX low frequency equalization zero frequency value standard mode 0: This field specifies the receiver zero frequency setting for the low frequency equalization function, by driving the rxda_dfe_lfeq_zero_freq signal going into the analog, when xcvr_standard_mode is set to 2'b00. 2'b 00 : 150 MHz 2'b 01 : 200 MHz 2'b 10 : 250 MHz 2'b 11 : 300 MHz

Table 12-851. Register Call Summary for RX_DIAG_LFEQ_TUNE_j

10-G SerDes Registers

- [RX_DIAG_LFEQ_TUNE_j Register \(Offset = 83CCh + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.284 RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j Register (Offset = 83D0h + formula) [reset = 1002h]

RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j is shown in Figure 12-284 and described in Table 12-853.

Return to [Summary Table](#).

RX signal detect tuning and control register

Offset = 83D0h + (j * 400h); where j = 0h to 3h

Table 12-852. RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j Instances

Instance	Physical Address
SERDES_10G0	0505 83D0h + formula

Figure 12-284. RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j Register

31	30	29	28	27	26	25	24
RX_DIAG_SH_SIGDET_15_13			RX_DIAG_SH_SIGDET_12	RX_DIAG_SH_SIGDET_11_8			
R-0h			R-0h	R-0h			
23	22	21	20	19	18	17	16
RX_DIAG_SH_SIGDET_7_5			RX_DIAG_SH_SIGDET_4	RX_DIAG_SH_SIGDET_3_0			
R-0h			R-0h	R-0h			
15	14	13	12	11	10	9	8
RX_DIAG_SIGDET_TUNE_15	RX_DIAG_SIGDET_TUNE_14	RX_DIAG_SIGDET_TUNE_13_12		RX_DIAG_SIGDET_TUNE_11_8			
R-0h	R/W-0h	R/W-1h		R-0h			
7	6	5	4	3	2	1	0
RX_DIAG_SIGDET_TUNE_7	RX_DIAG_SIGDET_TUNE_6	RX_DIAG_SIGDET_TUNE_5	RX_DIAG_SIGDET_TUNE_4	RX_DIAG_SIGDET_TUNE_3	RX_DIAG_SIGDET_TUNE_2_0		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-853. RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RX_DIAG_SH_SIGDET_15_13	R	0h	Reserved
28	RX_DIAG_SH_SIGDET_12	R	0h	Signal detect 1 up: Signal detect 1 calibration up signal value, as it is currently captured in the sample and hold latches.
27-24	RX_DIAG_SH_SIGDET_11_8	R	0h	Signal detect 1 code: Signal detect 1 calibration code signal value, as it is currently captured in the sample and hold latches.
23-21	RX_DIAG_SH_SIGDET_7_5	R	0h	Reserved
20	RX_DIAG_SH_SIGDET_4	R	0h	Signal detect 0 up: Signal detect 0 calibration up signal value, as it is currently captured in the sample and hold latches.
19-16	RX_DIAG_SH_SIGDET_3_0	R	0h	Signal detect 0 code: Signal detect 0 calibration code signal value, as it is currently captured in the sample and hold latches.
15	RX_DIAG_SIGDET_TUNE_15	R	0h	Reserved

**Table 12-853. RX_DIAG_SIGDET_RX_DIAG_SIGDET_TUNE_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
14	RX_DIAG_SIGDET_TUNE_14	R/W	0h	Signal detect calibration half gain select: Controls the resolution of each step in the signal detect calibration code by adjusting the gain of signal detect offset correction, by driving the rxd_a_sd_cal_halfgain signal going to the analog, as specified below. 1'b 0: 8mV resolution per calibration code step. 1'b 1: 4mV resolution per calibration code step.
13-12	RX_DIAG_SIGDET_TUNE_13_12	R/W	1h	Signal detect filter function select: Selects which of the two RX signal detect filter functions are enabled. 2'b 00 : Reserved 2'b 01 : RX low to high filter disabled, RX high to low filter enabled. 2'b 10 : RX low to high filter enabled, RX high to low filter disabled. 2'b 11 : RX low to high filter enabled, RX high to low filter enabled.
11-8	RX_DIAG_SIGDET_TUNE_11_8	R	0h	Reserved
7	RX_DIAG_SIGDET_TUNE_7	R/W	0h	Receiver signal detect invert samplers: Inverts the behavior of the rxd_a_sd_pulse_high and rxd_a_sd_pulse_low samplers, by driving the rxd_a_sd_invert_samplers signal to the analog. 1'b 0 : Normal mode : The rxd_a_sd_pulse_high sampler outputs a 1'b1 if the output of the comparator has been above the positive threshold at any time during the last clock period. Similar behavior exists for the rxd_a_sd_pulse_low sampler in this mode. 1'b 1 : Inverted mode : The rxd_a_sd_pulse_high sampler outputs a 1'b1 if the output of the comparator has been above the positive threshold for the entire duration of the last clock period. Similar behavior exists for the rxd_a_sd_pulse_low sampler in this mode.
6	RX_DIAG_SIGDET_TUNE_6	R/W	0h	Receiver signal detect squelch pulse none: Enable the squelch function for the rxd_a_sd_pulse_none signal, by driving the rxd_a_sd_squelch_pulse_none signal to the analog. This debug feature could allow the detection of LFPS signals having slow transition times (e.g. 4 nSec) and low frequency differential noise (e.g. 500 MHz). The later can create noise glitches taking place over man than 1/2 cycle when DCD is taken into consideration. 1'b 0 : Disabled 1'b 1 : Enabled
5	RX_DIAG_SIGDET_TUNE_5	R/W	0h	Receiver signal detect one comparator mode: Enables one comparator mode, as a power reduction option, by driving the rxd_a_sd_onecomp_mode_en signal to the analog. 1'b 0 : Both signal detect comparators functioning. 1'b 1 : One signal detect comparator functioning.
4	RX_DIAG_SIGDET_TUNE_4	R/W	0h	Receiver signal detect DC coupled path enable: Enables a DC coupled path to the signal detect for verification and testability purposes, by driving the rxd_a_sd_dcpath_en signal to the analog. 1'b 0 : Disabled 1'b 1 : Enabled
3	RX_DIAG_SIGDET_TUNE_3	R	0h	Reserved

**Table 12-853. RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
2-0	RX_DIAG_SIGDET_TUNE_2_0	R/W	2h	Signal detect level: Sets the reference voltage level at which the comparators will detect a signal by driving the rxda_sd_siglvl_n signal going to the analog. 3'b 000 : 8'b 11111110 : Min 3'b 001 : 8'b 111111101 ... 3'b 110 : 8'b 10111111 3'b 111 : 8'b 01111111 : Max

Table 12-854. Register Call Summary for RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_DIAG_SH_SIGDET__RX_DIAG_SIGDET_TUNE_j Register \(Offset = 83D0h + formula\) \[reset = 1002h\]: \[0\]](#)

12.285 RX_DIAG_SD_TEST_j Register (Offset = 83D4h + formula) [reset = X]

RX_DIAG_SD_TEST_j is shown in [Figure 12-285](#) and described in [Table 12-856](#).

Return to [Summary Table](#).

Signal detect test register

Offset = 83D4h + (j * 400h); where j = 0h to 3h

Table 12-855. RX_DIAG_SD_TEST_j Instances

Instance	Physical Address
SERDES_10G0	0505 83D4h + formula

Figure 12-285. RX_DIAG_SD_TEST_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_DIAG_SD_TEST_15_4							
R-0h							
7	6	5	4	3	2	1	0
RX_DIAG_SD_TEST_15_4				RX_DIAG_SD_TEST_3	RX_DIAG_SD_TEST_2	RX_DIAG_SD_TEST_1	RX_DIAG_SD_TEST_0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-856. RX_DIAG_SD_TEST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-4	RX_DIAG_SD_TEST_15_4	R	0h	Reserved
3	RX_DIAG_SD_TEST_3	R/W	0h	LFPS detected low test bit: This bit can be used to detect if the rx_lfps_detect is driven to a low state. The following procedure can be used to detect this condition. Write this bit to a 1'b1. Read this bit. If the value of the read bit is 1'b0, rx_lfps_detect is driven to a low state between the write and the read. Note that if rx_lfps_detect is already driven to a low state at the time of the write, the bit will not be set to 1'b1.
2	RX_DIAG_SD_TEST_2	R/W	0h	LFPS detected high test bit: This bit can be used to detect if the rx_lfps_detect is driven to a high state. The following procedure can be used to detect this condition. Write this bit to a 1'b1. Read this bit. If the value of the read bit is 1'b0, rx_lfps_detect is driven to a high state between the write and the read. Note that if rx_lfps_detect is already driven to a high state at the time of the write, the bit will not be set to 1'b1.

Table 12-856. RX_DIAG_SD_TEST_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RX_DIAG_SD_TEST_1	R/W	0h	Signal detected low test bit: This bit can be used to detect if the rx_signal_detect is driven to a low state. The following procedure can be used to detect this condition. Write this bit to a 1'b1. Read this bit. If the value of the read bit is 1'b0, rx_signal_detect is driven to a low state between the write and the read. Note that if rx_signal_detect is already driven to a low state at the time of the write, the bit will not be set to 1'b1.
0	RX_DIAG_SD_TEST_0	R/W	0h	Signal detected high test bit: This bit can be used to detect if the rx_signal_detect is driven to a high state. The following procedure can be used to detect this condition. Write this bit to a 1'b1. Read this bit. If the value of the read bit is 1'b0, rx_signal_detect is driven to a high state between the write and the read. Note that if rx_signal_detect is already driven to a high state at the time of the write, the bit will not be set to 1'b1.

Table 12-857. Register Call Summary for RX_DIAG_SD_TEST_j

10-G SerDes Registers

- [RX_DIAG_SD_TEST_j Register \(Offset = 83D4h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.286 RX_DIAG_SH_SLC_IPP_RX_DIAG_SAMP_CTRL_j Register (Offset = 83D8h + formula) [reset = 1h]

[RX_DIAG_SH_SLC_IPP_RX_DIAG_SAMP_CTRL_j](#) is shown in [Figure 12-286](#) and described in [Table 12-859](#).

Return to [Summary Table](#).

RX sampler diagnostic control register

Offset = 83D8h + (j * 400h); where j = 0h to 3h

Table 12-858. RX_DIAG_SH_SLC_IPP_RX_DIAG_SAMP_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 83D8h + formula

Figure 12-286. RX_DIAG_SH_SLC_IPP_RX_DIAG_SAMP_CTRL_j Register

31	30	29	28	27	26	25	24
RX_DIAG_SH_SLC_IPP_15	RX_DIAG_SH_SLC_IPP_14_8						
R-0h				R-0h			
23	22	21	20	19	18	17	16
RX_DIAG_SH_SLC_IPP_7	RX_DIAG_SH_SLC_IPP_6_0						
R-0h				R-0h			
15	14	13	12	11	10	9	8
RX_DIAG_SAMP_CTRL_15_2							
R-0h							
7	6	5	4	3	2	1	0
RX_DIAG_SAMP_CTRL_15_2						RX_DIAG_SAMP_CTRL_1	RX_DIAG_SAMP_CTRL_0
R-0h						R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-859. RX_DIAG_SH_SLC_IPP_RX_DIAG_SAMP_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_DIAG_SH_SLC_IPP_15	R	0h	Reserved
30-24	RX_DIAG_SH_SLC_IPP_14_8	R	0h	RX sampler latch calibration I even positive code: RX sampler latch calibration I even positive code signal value, as it is currently captured in the sample and hold latches.
23	RX_DIAG_SH_SLC_IPP_7	R	0h	Reserved
22-16	RX_DIAG_SH_SLC_IPP_6_0	R	0h	RX sampler latch calibration I odd positive code: RX sampler latch calibration I odd positive code signal value, as it is currently captured in the sample and hold latches.
15-2	RX_DIAG_SAMP_CTRL_15_2	R	0h	Reserved
1	RX_DIAG_SAMP_CTRL_1	R/W	0h	RX sampler latch range extend: Controls the range of the RX sampler calibration, by driving the rxda_sampler_latch_cal_range_ext signal to the analog. 1'b 0 : Normal range 1'b 1 : Extended range (adds approximately 1.4 mV per step or 21 mV total.)

Table 12-859. RX_DIAG_SH_SLC_IPP__RX_DIAG_SAMP_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RX_DIAG_SAMP_CTRL_0	R/W	1h	<p>Analog sampler rxda_dfe_0p5ui_mode_en signal control: Selects which delayed I data is to be used to unroll the Q data in the sampler.</p> <p>1'b 0: The I data that occurs 1.5 UI before the Q data is used to select the proper Q sample.</p> <p>1'b 1: The I data that occurs 0.5 UI before the corresponding Q data is used to select the proper Q sample.</p> <p>Note that the signal controlled by this register is forced to 1'b0 when RX sampler latch calibration is running.</p>

Table 12-860. Register Call Summary for RX_DIAG_SH_SLC_IPP__RX_DIAG_SAMP_CTRL_j

10-G SerDes Registers

- [RX_DIAG_SH_SLC_IPP__RX_DIAG_SAMP_CTRL_j Register \(Offset = 83D8h + formula\) \[reset = 1h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.287 RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j Register (Offset = 83DCh + formula) [reset = 0h]

[RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j](#) is shown in [Figure 12-287](#) and described in [Table 12-862](#).

Return to [Summary Table](#).

Sample and hold RX sampler latch calibration I predictive negative code register

Offset = 83DCh + (j * 400h); where j = 0h to 3h

Table 12-861. RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j Instances

Instance	Physical Address
SERDES_10G0	0505 83DCh + formula

Figure 12-287. RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j Register

31	30	29	28	27	26	25	24
RX_DIAG_SH_SLC_QPP_15	RX_DIAG_SH_SLC_QPP_14_8						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RX_DIAG_SH_SLC_QPP_7	RX_DIAG_SH_SLC_QPP_6_0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
RX_DIAG_SH_SLC_IPM_15	RX_DIAG_SH_SLC_IPM_14_8						
R-0h	R-0h						
7	6	5	4	3	2	1	0
RX_DIAG_SH_SLC_IPM_7	RX_DIAG_SH_SLC_IPM_6_0						
R-0h	R-0h						

LEGEND: R = Read Only; -n = value after reset

Table 12-862. RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_DIAG_SH_SLC_QPP_15	R	0h	Reserved
30-24	RX_DIAG_SH_SLC_QPP_14_8	R	0h	RX sampler latch calibration Q even positive code: RX sampler latch calibration Q even positive code signal value, as it is currently captured in the sample and hold latches.
23	RX_DIAG_SH_SLC_QPP_7	R	0h	Reserved
22-16	RX_DIAG_SH_SLC_QPP_6_0	R	0h	RX sampler latch calibration Q odd positive code: RX sampler latch calibration Q odd positive code signal value, as it is currently captured in the sample and hold latches.
15	RX_DIAG_SH_SLC_IPM_15	R	0h	Reserved
14-8	RX_DIAG_SH_SLC_IPM_14_8	R	0h	RX sampler latch calibration I even negative code: RX sampler latch calibration I even negative code signal value, as it is currently captured in the sample and hold latches.
7	RX_DIAG_SH_SLC_IPM_7	R	0h	Reserved

**Table 12-862. RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
6-0	RX_DIAG_SH_SLC_IPM_6_0	R	0h	RX sampler latch calibration I odd negative code: RX sampler latch calibration I odd negative code signal value, as it is currently captured in the sample and hold latches.

Table 12-863. Register Call Summary for RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j

10-G SerDes Registers

- [RX_DIAG_SH_SLC_QPP__RX_DIAG_SH_SLC_IPM_j Register \(Offset = 83DCh + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.288 RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j Register (Offset = 83E0h + formula) [reset = 0h]

RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j is shown in Figure 12-288 and described in Table 12-865.

Return to [Summary Table](#).

Sample and hold RX sampler latch calibration Q predictive negative code register

Offset = 83E0h + (j * 400h); where j = 0h to 3h

Table 12-864. RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j Instances

Instance	Physical Address
SERDES_10G0	0505 83E0h + formula

Figure 12-288. RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j Register

31	30	29	28	27	26	25	24
RX_DIAG_SH_SLC_EPP_15	RX_DIAG_SH_SLC_EPP_14_8						
R-0h				R-0h			
23	22	21	20	19	18	17	16
RX_DIAG_SH_SLC_EPP_7	RX_DIAG_SH_SLC_EPP_6_0						
R-0h				R-0h			
15	14	13	12	11	10	9	8
RX_DIAG_SH_SLC_QPM_15	RX_DIAG_SH_SLC_QPM_14_8						
R-0h				R-0h			
7	6	5	4	3	2	1	0
RX_DIAG_SH_SLC_QPM_7	RX_DIAG_SH_SLC_QPM_6_0						
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 12-865. RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_DIAG_SH_SLC_EPP_15	R	0h	Reserved
30-24	RX_DIAG_SH_SLC_EPP_14_8	R	0h	RX sampler latch calibration E even positive code: RX sampler latch calibration E even positive code signal value, as it is currently captured in the sample and hold latches.
23	RX_DIAG_SH_SLC_EPP_7	R	0h	Reserved
22-16	RX_DIAG_SH_SLC_EPP_6_0	R	0h	RX sampler latch calibration E odd positive code: RX sampler latch calibration E odd positive code signal value, as it is currently captured in the sample and hold latches.
15	RX_DIAG_SH_SLC_QPM_15	R	0h	Reserved
14-8	RX_DIAG_SH_SLC_QPM_14_8	R	0h	RX sampler latch calibration Q even negative code: RX sampler latch calibration Q even negative code signal value, as it is currently captured in the sample and hold latches.
7	RX_DIAG_SH_SLC_QPM_7	R	0h	Reserved

**Table 12-865. RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
6-0	RX_DIAG_SH_SLC_QPM_6_0	R	0h	RX sampler latch calibration Q odd negative code: RX sampler latch calibration Q odd negative code signal value, as it is currently captured in the sample and hold latches.

Table 12-866. Register Call Summary for RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j

10-G SerDes Registers

- [RX_DIAG_SH_SLC_EPP__RX_DIAG_SH_SLC_QPM_j Register \(Offset = 83E0h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.289 RX_DIAG_SH_SLC_EPM_j Register (Offset = 83E4h + formula) [reset = X]

RX_DIAG_SH_SLC_EPM_j is shown in Figure 12-289 and described in Table 12-868.

Return to [Summary Table](#).

Sample and hold RX sampler latch calibration E predictive negative code register

Offset = 83E4h + (j * 400h); where j = 0h to 3h

Table 12-867. RX_DIAG_SH_SLC_EPM_j Instances

Instance	Physical Address
SERDES_10G0	0505 83E4h + formula

Figure 12-289. RX_DIAG_SH_SLC_EPM_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RX_DIAG_SH_SLC_EPM_15	RX_DIAG_SH_SLC_EPM_14_8						
R-0h				R-0h			
7	6	5	4	3	2	1	0
RX_DIAG_SH_SLC_EPM_7	RX_DIAG_SH_SLC_EPM_6_0						
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 12-868. RX_DIAG_SH_SLC_EPM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15	RX_DIAG_SH_SLC_EPM_15	R	0h	Reserved
14-8	RX_DIAG_SH_SLC_EPM_14_8	R	0h	RX sampler latch calibration E even negative code: RX sampler latch calibration E even negative code signal value, as it is currently captured in the sample and hold latches.
7	RX_DIAG_SH_SLC_EPM_7	R	0h	Reserved
6-0	RX_DIAG_SH_SLC_EPM_6_0	R	0h	RX sampler latch calibration E odd negative code: RX sampler latch calibration E odd negative code signal value, as it is currently captured in the sample and hold latches.

Table 12-869. Register Call Summary for RX_DIAG_SH_SLC_EPM_j

10-G SerDes Registers

- [10-G SerDes Registers](#): [0]
- [RX_DIAG_SH_SLC_EPM_j Register \(Offset = 83E4h + formula\) \[reset = X\]](#): [0]

12.290 RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j Register (Offset = 83E8h + formula) [reset = 311h]

RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j is shown in [Figure 12-290](#) and described in [Table 12-871](#).

Return to [Summary Table](#).

PI rate selection register

Offset = 83E8h + (j * 400h); where j = 0h to 3h

Table 12-870.
RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j Instances

Instance	Physical Address
SERDES_10G0	0505 83E8h + formula

Figure 12-290. RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j Register

31	30	29	28	27	26	25	24
RX_DIAG_PI_C AP_15	RX_DIAG_PI_CAP_14_12			RX_DIAG_PI_C AP_11	RX_DIAG_PI_CAP_10_8		
R-0h	R/W-0h			R-0h	R/W-0h		
23	22	21	20	19	18	17	16
RX_DIAG_PI_C AP_7	RX_DIAG_PI_CAP_6_4			RX_DIAG_PI_C AP_3	RX_DIAG_PI_CAP_2_0		
R-0h	R/W-0h			R-0h	R/W-0h		
15	14	13	12	11	10	9	8
RX_DIAG_PI_R ATE_15	RX_DIAG_PI_RATE_14_12			RX_DIAG_PI_R ATE_11	RX_DIAG_PI_RATE_10_8		
R-0h	R/W-0h			R-0h	R/W-3h		
7	6	5	4	3	2	1	0
RX_DIAG_PI_R ATE_7	RX_DIAG_PI_RATE_6_4			RX_DIAG_PI_R ATE_3	RX_DIAG_PI_RATE_2_0		
R-0h	R/W-1h			R-0h	R/W-1h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-871. RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RX_DIAG_PI_CAP_15	R	0h	Reserved
30-28	RX_DIAG_PI_CAP_14_12	R/W	0h	PI capacitor selection standard mode 3: This field is used to implement waveform shaping inside the PI CML cells, by changing the capacitive loading. As the data rate decreases, this is used to increase cap loading, to maintain semi-sinusoidal wave shapes inside the PI CML input buffers and mixers, by driving the rxda_pi_cap_sel signal going into the analog, when xcvr_standard_mode is set to 2'b11. 3'b 000: Default capacitance required for wave shaping for data rates at 2.5G and higher. 3'b 001: Increased capacitance required for wave shaping for data rates below 2.5G. 3'b 010 - 3'b 111: Reserved
27	RX_DIAG_PI_CAP_11	R	0h	Reserved

Table 12-871. RX_DIAG_PI_CAP_RX_DIAG_PI_RATE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-24	RX_DIAG_PI_CAP_10_8	R/W	0h	<p>PI capacitor selection standard mode 2: This field is used to implement waveform shaping inside the PI CML cells, by changing the capacitive loading.</p> <p>As the data rate decreases, this is used to increase cap loading, to maintain semi-sinusoidal wave shapes inside the PI CML input buffers and mixers, by driving the rxd_a_pi_cap_sel signal going into the analog, when xcvr_standard_mode is set to 2'b10.</p> <p>3'b 000: Default capacitance required for wave shaping for data rates at 2.5G and higher.</p> <p>3'b 001: Increased capacitance required for wave shaping for data rates below 2.5G.</p> <p>3'b 010 - 3'b 111: Reserved</p>
23	RX_DIAG_PI_CAP_7	R	0h	Reserved
22-20	RX_DIAG_PI_CAP_6_4	R/W	0h	<p>PI capacitor selection standard mode 1: This field is used to implement waveform shaping inside the PI CML cells, by changing the capacitive loading.</p> <p>As the data rate decreases, this is used to increase cap loading, to maintain semi-sinusoidal wave shapes inside the PI CML input buffers and mixers, by driving the rxd_a_pi_cap_sel signal going into the analog, when xcvr_standard_mode is set to 2'b01.</p> <p>3'b 000: Default capacitance required for wave shaping for data rates at 2.5G and higher.</p> <p>3'b 001: Increased capacitance required for wave shaping for data rates below 2.5G.</p> <p>3'b 010 - 3'b 111: Reserved</p>
19	RX_DIAG_PI_CAP_3	R	0h	Reserved
18-16	RX_DIAG_PI_CAP_2_0	R/W	0h	<p>PI capacitor selection standard mode 0: This field is used to implement waveform shaping inside the PI CML cells, by changing the capacitive loading.</p> <p>As the data rate decreases, this is used to increase cap loading, to maintain semi-sinusoidal wave shapes inside the PI CML input buffers and mixers, by driving the rxd_a_pi_cap_sel signal going into the analog, when xcvr_standard_mode is set to 2'b00.</p> <p>3'b 000: Default capacitance required for wave shaping for data rates at 2.5G and higher.</p> <p>3'b 001: Increased capacitance required for wave shaping for data rates below 2.5G.</p> <p>3'b 010 - 3'b 111: Reserved</p>
15	RX_DIAG_PI_RATE_15	R	0h	Reserved
14-12	RX_DIAG_PI_RATE_14_12	R/W	0h	<p>PI rate selection standard mode 3: This field is used to scale the power of the CML cells inside the PI to tune it for a given data rate, by driving the rxd_a_pi_rate_sel signal going into the analog, when xcvr_standard_mode is set to 2'b11.</p> <p>3'b 000: 1/2X power scaling for the CML cells. This should be the default setting for 2.5G data rates.</p> <p>3'b 001: 1X power scaling for the CML cells. This should be the default setting for 5G data rates.</p> <p>3'b 010: Reserved</p> <p>3'b 011: 2X power scaling for the CML cells. This should be the default setting for 10G data rates.</p> <p>3'b 100 - 3'b 111: Reserved</p>

Table 12-871. RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RX_DIAG_PI_RATE_11	R	0h	Reserved
10-8	RX_DIAG_PI_RATE_10_8	R/W	3h	PI rate selection standard mode 2: This field is used to scale the power of the CML cells inside the PI to tune it for a given data rate, by driving the rxda_pi_rate_sel signal going into the analog, when xcvr_standard_mode is set to 2'b10. 3'b 000: 1/2X power scaling for the CML cells. This should be the default setting for 2.5G data rates. 3'b 001: 1X power scaling for the CML cells. This should be the default setting for 5G data rates. 3'b 010: Reserved 3'b 011: 2X power scaling for the CML cells. This should be the default setting for 10G data rates. 3'b 100 - 3'b 111: Reserved
7	RX_DIAG_PI_RATE_7	R	0h	Reserved
6-4	RX_DIAG_PI_RATE_6_4	R/W	1h	PI rate selection standard mode 1: This field is used to scale the power of the CML cells inside the PI to tune it for a given data rate, by driving the rxda_pi_rate_sel signal going into the analog, when xcvr_standard_mode is set to 2'b01. 3'b 000: 1/2X power scaling for the CML cells. This should be the default setting for 2.5G data rates. 3'b 001: 1X power scaling for the CML cells. This should be the default setting for 5G data rates. 3'b 010: Reserved 3'b 011: 2X power scaling for the CML cells. This should be the default setting for 10G data rates. 3'b 100 - 3'b 111: Reserved
3	RX_DIAG_PI_RATE_3	R	0h	Reserved
2-0	RX_DIAG_PI_RATE_2_0	R/W	1h	PI rate selection standard mode 0: This field is used to scale the power of the CML cells inside the PI to tune it for a given data rate, by driving the rxda_pi_rate_sel signal going into the analog, when xcvr_standard_mode is set to 2'b00. 3'b 000: 1/2X power scaling for the CML cells. This should be the default setting for 2.5G data rates. 3'b 001: 1X power scaling for the CML cells. This should be the default setting for 5G data rates. 3'b 010: Reserved 3'b 011: 2X power scaling for the CML cells. This should be the default setting for 10G data rates. 3'b 100 - 3'b 111: Reserved

Table 12-872. Register Call Summary for RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j

10-G SerDes Registers

- [RX_DIAG_PI_CAP__RX_DIAG_PI_RATE_j Register \(Offset = 83E8h + formula\) \[reset = 311h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.291 RX_DIAG_PI_TUNE_j Register (Offset = 83ECh + formula) [reset = X]

RX_DIAG_PI_TUNE_j is shown in Figure 12-291 and described in Table 12-874.

Return to [Summary Table](#).

PI tuning register

Offset = 83ECh + (j * 400h); where j = 0h to 3h

Table 12-873. RX_DIAG_PI_TUNE_j Instances

Instance	Physical Address
SERDES_10G0	0505 83ECh + formula

Figure 12-291. RX_DIAG_PI_TUNE_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RX_DIAG_PI_TUNE_15_8							
R-0h							
7	6	5	4	3	2	1	0
RX_DIAG_PI_TUNE_7	RX_DIAG_PI_TUNE_6	RX_DIAG_PI_TUNE_5	RX_DIAG_PI_TUNE_4	RX_DIAG_PI_TUNE_3_1		RX_DIAG_PI_TUNE_0	
R/W-0h	R/W-1h	R/W-1h	R/W-0h	R-0h		R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-874. RX_DIAG_PI_TUNE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	RX_DIAG_PI_TUNE_15_8	R	0h	Reserved
7	RX_DIAG_PI_TUNE_7	R/W	0h	Receiver CML to CMOS rate select value standard mode 3: This bit will drive the rxda_c2c_rate_sel signal going into the analog, when xcvr_standard_mode is set to 2'b11. 1'b 0 : High resistance 1'b 1 : Low resistance
6	RX_DIAG_PI_TUNE_6	R/W	1h	Receiver CML to CMOS rate select value standard mode 2: This bit will drive the rxda_c2c_rate_sel signal going into the analog, when xcvr_standard_mode is set to 2'b10. 1'b 0 : High resistance 1'b 1 : Low resistance
5	RX_DIAG_PI_TUNE_5	R/W	1h	Receiver CML to CMOS rate select value standard mode 1: This bit will drive the rxda_c2c_rate_sel signal going into the analog, when xcvr_standard_mode is set to 2'b01. 1'b 0 : High resistance 1'b 1 : Low resistance

Table 12-874. RX_DIAG_PI_TUNE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RX_DIAG_PI_TUNE_4	R/W	0h	Receiver CML to CMOS rate select value standard mode 0: This bit will drive the rxda_c2c_rate_sel signal going into the analog, when xcvr_standard_mode is set to 2'b00. 1'b 0 : High resistance 1'b 1 : Low resistance
3-1	RX_DIAG_PI_TUNE_3_1	R	0h	Reserved
0	RX_DIAG_PI_TUNE_0	R/W	1h	PI current select: Selects either the external based bias or the poly based bias for the PI, by driving the rxda_pi_cur_sel signal going into the analog. 1'b 0: Poly based bias 1'b 1: External based bias

Table 12-875. Register Call Summary for RX_DIAG_PI_TUNE_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_DIAG_PI_TUNE_j Register \(Offset = 83ECh + formula\) \[reset = X\]: \[0\]](#)

12.292 RX_DIAG_RST_DIAG_RX_DIAG_LPBK_CTRL_j Register (Offset = 83F0h + formula) [reset = 0h]

RX_DIAG_RST_DIAG_RX_DIAG_LPBK_CTRL_j is shown in Figure 12-292 and described in Table 12-877.

Return to [Summary Table](#).

RX loopback controller register

Offset = 83F0h + (j * 400h); where j = 0h to 3h

Table 12-876.
RX_DIAG_RST_DIAG_RX_DIAG_LPBK_CTRL_j
Instances

Instance	Physical Address
SERDES_10G0	0505 83F0h + formula

Figure 12-292. RX_DIAG_RST_DIAG_RX_DIAG_LPBK_CTRL_j Register

31	30	29	28	27	26	25	24
RX_DIAG_RST_DIAG_15_6							
R-0h							
23	22	21	20	19	18	17	16
RX_DIAG_RST_DIAG_15_6	RX_DIAG_RST_DIAG_5	RX_DIAG_RST_DIAG_4	RX_DIAG_RST_DIAG_3	RX_DIAG_RST_DIAG_2	RX_DIAG_RST_DIAG_1	RX_DIAG_RST_DIAG_0	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RX_DIAG_LPBK_CTRL_15_6							
R-0h							
7	6	5	4	3	2	1	0
RX_DIAG_LPBK_CTRL_15_6	RX_DIAG_LPBK_CTRL_5_4	RX_DIAG_LPBK_CTRL_3_0					
R-0h	R/W-0h	R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-877. RX_DIAG_RST_DIAG_RX_DIAG_LPBK_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RX_DIAG_RST_DIAG_15_6	R	0h	Reserved
21	RX_DIAG_RST_DIAG_5	R	0h	Current state of the rxd_clk_reset_n reset.
20	RX_DIAG_RST_DIAG_4	R	0h	Current state of the rx_dig_reset_n reset.
19	RX_DIAG_RST_DIAG_3	R	0h	Current state of the rxd_cdrif_reset_n reset.
18	RX_DIAG_RST_DIAG_2	R	0h	Current state of the rx_ree_fcn_reset_n reset.
17	RX_DIAG_RST_DIAG_1	R	0h	Current state of the rx_ree_ctrl_reset_n reset.
16	RX_DIAG_RST_DIAG_0	R	0h	Current state of the rx_lfps_det_filter_reset_n reset.
15-6	RX_DIAG_LPBK_CTRL_15_6	R	0h	Reserved
5-4	RX_DIAG_LPBK_CTRL_5_4	R/W	0h	Recovered clock loopback select: Selects which recovered clock to use when recovered clock loopback is enabled. 2'b 00: I clock. 2'b 01: Q clock 2'b 10: E clock.

Table 12-877. RX_DIAG_RST_DIAG__RX_DIAG_LPBK_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	RX_DIAG_LPBK_CTRL_3_0	R/W	0h	<p>Attenuation settings: Sets the attenuation for the ISI generation loopback filter, as specified below.</p> <p>4'b 0000 : 6 dB</p> <p>4'b0001</p> <p>...</p> <p>4'b 0101 : 13 dB</p> <p>...</p> <p>4'b 1000 : 16 dB</p> <p>...</p> <p>4'b 1100 : 23 dB</p> <p>...</p> <p>4'b1101</p> <p>4'b 1110 : Highest attenuation</p> <p>4'b 1111 : High impedance</p>

Table 12-878. Register Call Summary for RX_DIAG_RST_DIAG__RX_DIAG_LPBK_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [RX_DIAG_RST_DIAG__RX_DIAG_LPBK_CTRL_j Register \(Offset = 83F0h + formula\) \[reset = 0h\]: \[0\]](#)

12.293 RX_DIAG_ACYA__RX_DIAG_DCYA_j Register (Offset = 83FCh + formula) [reset = 0h]

RX_DIAG_ACYA__RX_DIAG_DCYA_j is shown in Figure 12-293 and described in Table 12-880.

Return to [Summary Table](#).

Receiver digital cover your alternatives register

Offset = 83FCh + (j * 400h); where j = 0h to 3h

**Table 12-879. RX_DIAG_ACYA__RX_DIAG_DCYA_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 83FCh + formula

Figure 12-293. RX_DIAG_ACYA__RX_DIAG_DCYA_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_DIAG_ACYA_15_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_DIAG_DCYA_15_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-880. RX_DIAG_ACYA__RX_DIAG_DCYA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_DIAG_ACYA_15_0	R/W	0h	Reserved - spare
15-0	RX_DIAG_DCYA_15_0	R/W	0h	Reserved - spare

Table 12-881. Register Call Summary for RX_DIAG_ACYA__RX_DIAG_DCYA_j

10-G SerDes Registers

- [RX_DIAG_ACYA__RX_DIAG_DCYA_j Register \(Offset = 83FCh + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.294 RESERVEDBIT13ADDRESSC_y Register (Offset = A000h + formula) [reset = 0h]

RESERVEDBIT13ADDRESSC_y is shown in Figure 12-294 and described in Table 12-883.

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Reserved Address bit 13 area C

Offset = A000h + (y * 4h); where y = 0h to 7FFh

**Table 12-882. RESERVEDBIT13ADDRESSC_y
Instances**

Instance	Physical Address
SERDES_10G0	0505 A000h + formula

Figure 12-294. RESERVEDBIT13ADDRESSC_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES_BIT13_ADR_C																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-883. RESERVEDBIT13ADDRESSC_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RES_BIT13_ADR_C	R/W	0h	Write only test region C

Table 12-884. Register Call Summary for RESERVEDBIT13ADDRESSC_y

10-G SerDes Registers

- [RESERVEDBIT13ADDRESSC_y Register \(Offset = A000h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.295 PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register (Offset = C000h) [reset = BD510400h]

PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 is shown in Figure 12-295 and described in Table 12-886.

Return to [Summary Table](#).

PIPE common control1 register

Table 12-885. PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Instances

Instance	Physical Address
SERDES_10G0	0505 C000h

Figure 12-295. PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register

31	30	29	28	27	26	25	24
PHY_PIPE_CMN_CTRL2_15_12				PHY_PIPE_CMN_CTRL2_11_8			
R/W-Bh				R/W-Dh			
23	22	21	20	19	18	17	16
PHY_PIPE_CMN_CTRL2_7	PHY_PIPE_CMN_CTRL2_6	PHY_PIPE_CMN_CTRL2_5	PHY_PIPE_CMN_CTRL2_4	PHY_PIPE_CMN_CTRL2_3	PHY_PIPE_CMN_CTRL2_2	PHY_PIPE_CMN_CTRL2_1	PHY_PIPE_CMN_CTRL2_0
R-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
PHY_PIPE_CMN_CTRL1_15_13			PHY_PIPE_CMN_CTRL1_12	PHY_PIPE_CMN_CTRL1_11	PHY_PIPE_CMN_CTRL1_10	PHY_PIPE_CMN_CTRL1_9	PHY_PIPE_CMN_CTRL1_8
R-0h			RC-0h	R-0h	R/W-1h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
PHY_PIPE_CMN_CTRL1_7	PHY_PIPE_CMN_CTRL1_6	PHY_PIPE_CMN_CTRL1_5_4		PHY_PIPE_CMN_CTRL1_3_2		PHY_PIPE_CMN_CTRL1_1	PHY_PIPE_CMN_CTRL1_0
R/W-0h	R/W-0h	R/W-0h		R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; RC = Read to Clear; -n = value after reset

Table 12-886. PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PHY_PIPE_CMN_CTRL2_15_12	R/W	Bh	USB SuperSpeed Tx LFPS Stretch : Minimum number of data rate clock cycles in which PMA tx_lfps_en signal is asserted for USB SuperSpeed rate. Number of data rate clock cycles must be X 1 PMA RefClk cycle.
27-24	PHY_PIPE_CMN_CTRL2_11_8	R/W	Dh	USB SuperSpeedPlus Tx LFPS Stretch : Minimum number of data rate clock cycles in which PMA tx_lfps_en signal is asserted for USB SuperSpeedPlus rate. Number of data rate clock cycles must be X 1 PMA RefClk cycle.
23	PHY_PIPE_CMN_CTRL2_7	R	0h	Reserved
22	PHY_PIPE_CMN_CTRL2_6	R/W	1h	PCIe PCS TX electrical idle pre release:When this bit is set, the TX electrical idle release to the PMA is advanced 1 cycle to allow the adjustment of the datapath timing
21	PHY_PIPE_CMN_CTRL2_5	R/W	0h	RX equaliser complete mask: When this bit is cleared, the PHY will return direction change of 0 when PMA indicates evaluation complete. Subsequent evaluation requests would clear the PMA iteration counters. When set high, the PMA equalization complete signal is ignored.

Table 12-886. PHY_PIPE_CMN_CTRL2_PHY_PIPE_CMN_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	PHY_PIPE_CMN_CTRL2_4	R/W	1h	PCIe PCS EIOS cycle error mask: When this bit is enabled and the pipe rx interface is outputting an EIOS symbol, decode errors will be masked out
19	PHY_PIPE_CMN_CTRL2_3	R/W	0h	USB Gen 2 Bit Error Correction Disable: When this bit is high, bit error correction on SKP and SDS symbols is disabled.
18	PHY_PIPE_CMN_CTRL2_2	R/W	0h	USB PIPE3 Compatibility Mode enable : When this bit is set to 1, USB PIPE3 compatibility mode is enabled. In this mode, when operating in nominal empty Elasticity Buffer mode, when the EB buffer goes empty, instead of de-asserting PIPE RxDataValid, a USB SKIP OS is inserted into the data stream. This is the behavior as defined in PIPE version 3. When this bit is low, PIPE RxDataValid is de-asserted when the EB buffer goes empty, as recommended by PIPE version 4.
17	PHY_PIPE_CMN_CTRL2_1	R/W	0h	USB Loopback Slave Error Count disable: When this bit is set to 1, disables the error count for US loopback slave, such that the error count is not inserted into the BCNT OS.
16	PHY_PIPE_CMN_CTRL2_0	R/W	1h	USB Elasticity Buffer Re-align enable: When this bit is set to 1, when Rx for a USB link is initially started, the elasticity buffer is re-aligned to its idle point upon seeing 3 consecutive COMMAs (i.e. from TS1/TS2s) in the same relative bit position. The purpose of this is to re-align the elasticity buffer (i.e. CTC) after receiving the TSEQ data, which contains no SKIP OSs.
15-13	PHY_PIPE_CMN_CTRL1_15_13	R	0h	Reserved
12	PHY_PIPE_CMN_CTRL1_12	RC	0h	PHY APB access timeout: When set, an APB read/write request to PHY registers failed (i.e. timed out). When set, this bit is cleared upon read.
11	PHY_PIPE_CMN_CTRL1_11	R	0h	Reserved
10	PHY_PIPE_CMN_CTRL1_10	R/W	1h	PCIe PCS Comma realign: This field controls the comma alignment state machine to re-align to new bit position without going to loss of sync state. The requirement of the new bit position should meet the number of COMMAs as per Symbol unlock count register definition. When new bit position is identified the comma alignment state machine remains in sync state with the alignment now locked to the new bit position. This field needs to be programmed during the PHY initialization routine before training sequences are received. The effect here is that pipe_rx_valid is not de-asserted upon re-alignment. When this bit is 0, pipe_rx_valid will be de-asserted upon loss of COMMA lock and subsequent re-alignment. Applies for PCIe Gen 1/2 and USB3.1 Gen 1 only.
9	PHY_PIPE_CMN_CTRL1_9	R/W	0h	Block alignment clear on EIOS : When set, upon receiving a PCIe EIOS, 128b/130b block alignment is reset regardless of Rx signal detect from the PMA (applies for PCIe Gen 3 only).
8	PHY_PIPE_CMN_CTRL1_8	R/W	0h	Comma alignment clear on EIOS : When set, upon receiving a PCIe EIOS, Comma Alignment is reset regardless of Rx signal detect from the PMA (applies for PCIe Gen 1/2 only).

Table 12-886. PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	PHY_PIPE_CMN_CTRL1_7	R/W	0h	Block alignment ignore Rx SigDetect : When set, 128b/13xb block alignment will not be reset due to loss of signal detection from the PMA (applies for PCIe Gen 3 and USB3.1 Gen 2 only).
6	PHY_PIPE_CMN_CTRL1_6	R/W	0h	Comma alignment ignore Rx SigDetect : When set, Comma alignment will not be reset due to loss of signal detection from the PMA (applies for PCIe Gen 1/2 and USB3.1 Gen 1 only).
5-4	PHY_PIPE_CMN_CTRL1_5_4	R/W	0h	Rx signal detect delay : Selects the number of clock cycles of delay to add to the PMA signal detect when the bit alignment blocks should be reset after losing signal.
3-2	PHY_PIPE_CMN_CTRL1_3_2	R	0h	Reserved
1	PHY_PIPE_CMN_CTRL1_1	R/W	0h	RefClk disable override: 1 = overrides turning off reference clock receiver by forcing cmn_refclk_disable PMA input low. 0 = normal control of cmn_refclk_disable PMA input by PHY logic.
0	PHY_PIPE_CMN_CTRL1_0	R/W	0h	PHY RefClk enable input ignore : 0 = ignore phy_en_refclk PHY input (forces low internally). 1 = phy_en_refclk_used as specified for controlling enable/disable of cmn_refclk_Xp/mX.

Table 12-887. Register Call Summary for PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1

10-G SerDes Registers

- [PHY_PIPE_CMN_CTRL2__PHY_PIPE_CMN_CTRL1 Register \(Offset = C000h\) \[reset = BD510400h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.296 PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Register (Offset = C004h) [reset = 08204400h]

PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 is shown in Figure 12-296 and described in Table 12-889.

Return to [Summary Table](#).

PIPE comma lock configuration1 register

Table 12-888. PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Instances

Instance	Physical Address
SERDES_10G0	0505 C004h

Figure 12-296. PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Register

31	30	29	28	27	26	25	24
PHY_PIPE_COM_LOCK_CFG2_15_8							
R/W-8h							
23	22	21	20	19	18	17	16
PHY_PIPE_COM_LOCK_CFG2_7_0							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_PIPE_COM_LOCK_CFG1_15_12				PHY_PIPE_COM_LOCK_CFG1_11_0			
R/W-4h				R/W-400h			
7	6	5	4	3	2	1	0
PHY_PIPE_COM_LOCK_CFG1_11_0							
R/W-400h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-889. PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_COM_LOCK_CFG2_15_8	R/W	8h	PCIe PCS Comma lock count fast: The number of COMMA symbols that needs to be seen in the same bit position for the comma state machine to lock. This field is used while the PCS is in P0 state after an EIOS has been seen, ie detecting FTS
23-16	PHY_PIPE_COM_LOCK_CFG2_7_0	R/W	20h	PCIe PCS Comma lock count: The number of COMMA symbols that needs to be seen in the same bit position for the comma state machine to lock. This field is used while the PCS is transitioning back to the P0 power state.
15-12	PHY_PIPE_COM_LOCK_CFG1_15_12	R/W	4h	PCIe PCS Comma unlock count: The number of COMMA symbols that need to be seen in the wrong bit position before the comma alignment state machine will transition to RESYNC or LOS state
11-0	PHY_PIPE_COM_LOCK_CFG1_11_0	R/W	400h	PCIe PCS Comma full lock count: The number of COMMA symbols that need to be seen in the same bit position for the comma alignment state machine to lock. The field is used for initial reset lock.

Table 12-890. Register Call Summary for PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1

<div> 10-G SerDes Registers <ul style="list-style-type: none"> PHY_PIPE_COM_LOCK_CFG2__PHY_PIPE_COM_LOCK_CFG1 Register (Offset = C004h) [reset = 08204400h]: [0] 10-G SerDes Registers: [0] </div>
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12.297 PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register (Offset = C008h) [reset = 137Fh]

PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG is shown in Figure 12-297 and described in Table 12-892.

Return to [Summary Table](#).

PIPE EIEOS lock configuration register

Table 12-891. PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Instances

Instance	Physical Address
SERDES_10G0	0505 C008h

Figure 12-297. PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register

31	30	29	28	27	26	25	24
PHY_PIPE_LANE_DSBL_15_8							
R-0h							
23	22	21	20	19	18	17	16
PHY_PIPE_LANE_DSBL_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_PIPE_EIE_LOCK_CFG_15_12				PHY_PIPE_EIE_LOCK_CFG_11_8			
R/W-1h				R/W-3h			
7	6	5	4	3	2	1	0
PHY_PIPE_EIE_LOCK_CFG_7_0							
R/W-7Fh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-892. PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PIPE_LANE_DSBL_15_8	R	0h	Reserved
23-16	PHY_PIPE_LANE_DSBL_7_0	R/W	0h	PIPE lane disable: Each bit corresponds to a lane (i.e. bit [0] -X lane 0, bit [1] -X lane 1, etc). When set the corresponding PIPE lane is disabled. Lanes that are disabled will transmit electrical idle and will not return any data on PIPE Rx interface. Used to disable unused lanes in a multi-lane PCIe link. (The PMA transceiver corresponding to lane will be placed in suspend.)
15-12	PHY_PIPE_EIE_LOCK_CFG_15_12	R/W	1h	EIE lock count fast: The number of EIEOS blocks that need to be seen in the same bit position for the alignment state machine to lock for Gen3/4. The field is used while the PCS is in P0 state after an EIEOS has been seen
11-8	PHY_PIPE_EIE_LOCK_CFG_11_8	R/W	3h	EIE lock count : The number of EIEOS blocks that need to be seen in the same bit position for the alignment state machine to lock for Gen3/4. The field is used while the PCS is transitioning out of a power state change and not performing a rate change

**Table 12-892. PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
7-0	PHY_PIPE_EIE_LOCK_CFG_7_0	R/W	7Fh	EIE full lock count: The number of EIEOS blocks that need to be seen in the same bit position for the alignment state machine to lock for Gen3/4. The field is used for initial after reset lock or lock after a rate change

Table 12-893. Register Call Summary for PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG

10-G SerDes Registers

- [PHY_PIPE_LANE_DSBL__PHY_PIPE_EIE_LOCK_CFG Register \(Offset = C008h\) \[reset = 137Fh\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.298 PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register (Offset = C00Ch) [reset = 3C963D09h]

PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH is shown in Figure 12-298 and described in Table 12-895.

Return to [Summary Table](#).

PIPE receiver detect inhibit register

Table 12-894. PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Instances

Instance	Physical Address
SERDES_10G0	0505 C00Ch

Figure 12-298. PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register

31	30	29	28	27	26	25	24
PHY_PIPE_RX_ELEC_IDLE_DLY_15_10						PHY_PIPE_RX_ELEC_IDLE_DLY_9_0	
R/W-Fh						R/W-96h	
23	22	21	20	19	18	17	16
PHY_PIPE_RX_ELEC_IDLE_DLY_9_0							
R/W-96h							
15	14	13	12	11	10	9	8
PHY_PIPE_RCV_DET_INH_15_0							
R/W-3D09h							
7	6	5	4	3	2	1	0
PHY_PIPE_RCV_DET_INH_15_0							
R/W-3D09h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-895. PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	PHY_PIPE_RX_ELEC_IDLE_DLY_15_10	R/W	Fh	PCIe PCS L1.x exit Rx electrical idle force fast count : Counter load value to hold PIPE Rx Electrical Idle high upon exit from L1.x. Counter is loaded and starts counting down after phy_l*_rx_elec_idle_det_en is asserted high. Default is 500 nsec. This counter accounts for time to power on just the analog Rx signal detect block. Based on reference clock cycles (25 MHz default). Minimum value = 6'd0.
25-16	PHY_PIPE_RX_ELEC_IDLE_DLY_9_0	R/W	96h	PCIe PCS L1.x exit Rx electrical idle force full count : Counter load value to hold PIPE Rx Electrical Idle high upon exit from L1.x when the PMA common was powered down. Counter is loaded and starts counting down upon de-assertion of PMA cmn_ref_clk_disable (upon de-assertion of phy_l*_ent_l1_x for first link). Default is 6 usec. This counter accounts for time to power on the bias and decap and only takes effect if the PMA was suspended. Based on reference clock cycles (25 MHz default). Minimum value = 10'd1.

Table 12-895. PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
15-0	PHY_PIPE_RCV_DET_INH_15_0	R/W	3D09h	<p>PCS Receiver Detect Inhibit Counter Load Value: Counter load value to delay receiver detection request to PMA until PMA common mode is within the required range.</p> <p>The timer (running on divided reference clock from PMA) starts once the PMA common has completed startup.</p> <p>If receiver detect request is received while timer has not expired, the PCS will wait until the timer expires before signaling the request to the PMA.</p> <p>Load value is specified in multiples of 4x the divider reference clock period (typically 40 nsec for 100 MHz reference clock input frequency) for a 2.5 msec inhibit time.</p>

Table 12-896. Register Call Summary for PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH

10-G SerDes Registers

- [PHY_PIPE_RX_ELEC_IDLE_DLY__PHY_PIPE_RCV_DET_INH Register \(Offset = C00Ch\) \[reset = 3C963D09h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.299 PHY_ISO_CMN_CTRL Register (Offset = C010h) [reset = X]

PHY_ISO_CMN_CTRL is shown in [Figure 12-299](#) and described in [Table 12-898](#).

[Return to Summary Table.](#)

PHY common control signal isolation register

Table 12-897. PHY_ISO_CMN_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 C010h

Figure 12-299. PHY_ISO_CMN_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_ISO_CMN_CTRL_15_13			PHY_ISO_CMN_CTRL_12	PHY_ISO_CMN_CTRL_11_9			PHY_ISO_CMN_CTRL_8
R-0h			R-0h	R-0h			R/W-0h
7	6	5	4	3	2	1	0
PHY_ISO_CMN_CTRL_7_6	PHY_ISO_CMN_CTRL_5	PHY_ISO_CMN_CTRL_4	PHY_ISO_CMN_CTRL_3_1			PHY_ISO_CMN_CTRL_0	
R-0h	R/W-0h	R/W-0h	R-0h			R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-898. PHY_ISO_CMN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	PHY_ISO_CMN_CTRL_15_13	R	0h	Reserved
12	PHY_ISO_CMN_CTRL_12	R	0h	Current value of phy_refclk_reqd PHY output.
11-9	PHY_ISO_CMN_CTRL_11_9	R	0h	Reserved
8	PHY_ISO_CMN_CTRL_8	R/W	0h	Drives phy_refclk_en PHY input when in PHY macro and PMA isolation mode.
7-6	PHY_ISO_CMN_CTRL_7_6	R	0h	Reserved
5	PHY_ISO_CMN_CTRL_5	R/W	0h	Drives phy_pma_suspend_override PHY input when in PHY macro and PMA isolation mode.
4	PHY_ISO_CMN_CTRL_4	R/W	0h	Drives refclk_rcvr_pwrn internal PHY signal when in PHY macro and PMA isolation mode (1 = powers down the reference clock receiver). During normal operation, refclk_rcvr_pwrn is driven from ~abp_preset_n, which powers down the reference clock receiver when the PHY is disabled.
3-1	PHY_ISO_CMN_CTRL_3_1	R	0h	Reserved

Table 12-898. PHY_ISO_CMN_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_ISO_CMN_CTRL_0	R/W	1h	Drives phy_reset_n PHY input when in PHY macro and PMA isolation mode.

Table 12-899. Register Call Summary for PHY_ISO_CMN_CTRL

10-G SerDes Registers

- [PHY_ISO_CMN_CTRL Register \(Offset = C010h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.300 PHY_STATE_CHG_TIMEOUT Register (Offset = C014h) [reset = X]

PHY_STATE_CHG_TIMEOUT is shown in Figure 12-300 and described in Table 12-901.

Return to [Summary Table](#).

PHY state change monitor timeout

**Table 12-900. PHY_STATE_CHG_TIMEOUT
Instances**

Instance	Physical Address
SERDES_10G0	0505 C014h

Figure 12-300. PHY_STATE_CHG_TIMEOUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_STATE_CHG_TIMEOUT_15_0															
R/W-30D4h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-901. PHY_STATE_CHG_TIMEOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PHY_STATE_CHG_TIMEOUT_15_0	R/W	30D4h	<p>State change timeout: Bits [19:4] of the state change timeout (bits [3:0] are zero).</p> <p>The timeout is the maximum number of APB clock cycles (abp_pclk) that are allowed for completion of a PHY power state change for the link.</p> <p>If the timeout expires, phy_interrupt_In_XX for the associated lane is asserted and interrupt status register bit is set.</p> <p>For maximum allowed APB clock frequency, this provides 5.2 msec maximum timeout.</p> <p>Default is set for 1 msec for the maximum APB clock frequency.</p>

Table 12-902. Register Call Summary for PHY_STATE_CHG_TIMEOUT

10-G SerDes Registers

- [PHY_STATE_CHG_TIMEOUT Register \(Offset = C014h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.301 PHY_AUTO_CFG_SPDUP Register (Offset = C01Ch) [reset = 1h]

PHY_AUTO_CFG_SPDUP is shown in Figure 12-301 and described in Table 12-904.

Return to [Summary Table](#).

PHY speedup control register

Table 12-903. PHY_AUTO_CFG_SPDUP Instances

Instance	Physical Address
SERDES_10G0	0505 C01Ch

Figure 12-301. PHY_AUTO_CFG_SPDUP Register

31	30	29	28	27	26	25	24
PHY_AUTO_CFG_SPDUP_15_4							
R-0h							
23	22	21	20	19	18	17	16
PHY_AUTO_CFG_SPDUP_15_4				PHY_AUTO_CFG_SPDUP_3	PHY_AUTO_CFG_SPDUP_2	PHY_AUTO_CFG_SPDUP_1	PHY_AUTO_CFG_SPDUP_0
R-0h				R-0h	R/W-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
PHY_PLL_CFG_15_2							
R-0h							
7	6	5	4	3	2	1	0
PHY_PLL_CFG_15_2						PHY_PLL_CFG_1	PHY_PLL_CFG_0
R-0h						R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-904. PHY_AUTO_CFG_SPDUP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PHY_AUTO_CFG_SPDUP_15_4	R	0h	Reserved
19	PHY_AUTO_CFG_SPDUP_3	R	0h	Speedup configuration complete: 1 = PHY speedup configuration is complete, 0 = not complete.
18	PHY_AUTO_CFG_SPDUP_2	R/W	0h	Speedup configuration stall: 1 = upon completion of PHY speedup configuration, do not release reset to PMA until this bit is cleared, 0 = release reset to PMA upon completion of PHY speedup configuration. Do not set high when [1] = 0.
17	PHY_AUTO_CFG_SPDUP_1	R/W	0h	Speedup configuration enable: If set to 1 upon de-assertion (high) of phy_reset_n, the PHY will be configured for simulation speedup. Only for use in RTL or gate-level simulations. Not for use in silicon.
16	PHY_AUTO_CFG_SPDUP_0	R	0h	Reserved
15-2	PHY_PLL_CFG_15_2	R	0h	Reserved
1	PHY_PLL_CFG_1	R/W	0h	PLL configuration: 0 = PHY configured to only use PLL0 / PLL1 disabled. 1 = PHY configured to use both PLL0 and PLL1.

Table 12-904. PHY_AUTO_CFG_SPDUP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PHY_PLL_CFG_0	R/W	1h	Single link PCIe configuration : 1 = PHY configured such that there is only a single PCIe link (1xN) and all PCIe rates will be driven by PLL0. Any other links are not PCIe and will not use PLL0. 0 = ALL other configurations. This is a static configuration, which can only be changed while phy_reset_n is asserted low.

Table 12-905. Register Call Summary for PHY_AUTO_CFG_SPDUP

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_AUTO_CFG_SPDUP Register \(Offset = C01Ch\) \[reset = 1h\]: \[0\]](#)

12.302 PHY_REFCLK_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_LOW Register (Offset = C020h) [reset = 274201C2h]

PHY_REFCLK_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_LOW is shown in Figure 12-302 and described in Table 12-907.

Return to [Summary Table](#).

PHY external reference clock detect low threshold register

Table 12-906.
PHY_REFCLK_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_LOW
Instances

Instance	Physical Address
SERDES_10G0	0505 C020h

Figure 12-302. PHY_REFCLK_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_LOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_REFCLK_DET_THRES_HIGH_15_0															
R/W-2742h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_REFCLK_DET_THRES_LOW_15_0															
R/W-1C2h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-907. PHY_REFCLK_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_REFCLK_DET_THRES_HIGH_15_0	R/W	2742h	External Reference Clock Active Detect High Threshold: This is the maximum number of external reference clock cycles which must be counted during the measurement interval to indicate a valid clock detected. The default value is based on 100MHz reference clock frequency and 10 MHz apb_pclk frequency.
15-0	PHY_REFCLK_DET_THRES_LOW_15_0	R/W	1C2h	External Reference Clock Active Detect Low Threshold: This is the minimum number of external reference clock cycles which must be counted during the measurement interval to indicate a valid clock detected. The default value is based on 100MHz reference clock external frequency and 200 MHz (max) apb_pclk frequency.

Table 12-908. Register Call Summary for
PHY_REFCLK_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_LOW

10-G SerDes Registers

- [PHY_REFCLK_DET_THRES_HIGH__PHY_REFCLK_DET_THRES_LOW Register \(Offset = C020h\) \[reset = 274201C2h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.303 PHY_REFCLK_DET_OP_DELAY__PHY_REFCLK_DET_INTERVAL Register (Offset = C024h) [reset = 106403E8h]

PHY_REFCLK_DET_OP_DELAY__PHY_REFCLK_DET_INTERVAL is shown in Figure 12-303 and described in Table 12-910.

Return to [Summary Table](#).

PHY external reference clock detect measurement interval register

Table 12-909. PHY_REFCLK_DET_OP_DELAY__PHY_REFCLK_DET_INTERVAL Instances

Instance	Physical Address
SERDES_10G0	0505 C024h

Figure 12-303. PHY_REFCLK_DET_OP_DELAY__PHY_REFCLK_DET_INTERVAL Register

31	30	29	28	27	26	25	24
PHY_REFCLK_DET_OP_DELAY_15_8							
R/W-10h							
23	22	21	20	19	18	17	16
PHY_REFCLK_DET_OP_DELAY_7_0							
R/W-64h							
15	14	13	12	11	10	9	8
PHY_REFCLK_DET_INTERVAL_15_0							
R/W-3E8h							
7	6	5	4	3	2	1	0
PHY_REFCLK_DET_INTERVAL_15_0							
R/W-3E8h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-910. PHY_REFCLK_DET_OP_DELAY__PHY_REFCLK_DET_INTERVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_REFCLK_DET_OP_DELAY_15_8	R/W	10h	External Reference Clock Active Detect End Delay: This is the number of apb_pclk cycles to wait upon completion of measurement interval before capturing the result (accounts for synchronization delays).
23-16	PHY_REFCLK_DET_OP_DELAY_7_0	R/W	64h	External Reference Clock Active Detect Start Delay: This is the number of apb_pclk cycles to wait prior to start of measurement interval (accounts for enable delay of reference clock in PMA).
15-0	PHY_REFCLK_DET_INTERVAL_15_0	R/W	3E8h	External Reference Clock Active Detect Measurement Interval: This is the number of apb_pclk cycles in which to count external reference clock cycles. The default corresponds to 5 us for 200 MHz apb_clk and 100 us for 10 MHz apb_clock.

Table 12-911. Register Call Summary for PHY_REFCLK_DET_OP_DELAY__PHY_REFCLK_DET_INTERVAL

10-G SerDes Registers

- [PHY_REFCLK_DET_OP_DELAY__PHY_REFCLK_DET_INTERVAL Register \(Offset = C024h\) \[reset = 106403E8h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.304 PHY_REFCLK_DET_ISO_CTRL Register (Offset = C028h) [reset = X]

PHY_REFCLK_DET_ISO_CTRL is shown in [Figure 12-304](#) and described in [Table 12-913](#).

Return to [Summary Table](#).

PHY external reference clock detect isolation control register

Table 12-912. PHY_REFCLK_DET_ISO_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 C028h

Figure 12-304. PHY_REFCLK_DET_ISO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_REFCLK_DET_ISO_CTRL_15_13			PHY_REFCLK_DET_ISO_CTRL_12	PHY_REFCLK_DET_ISO_CTRL_11_10		PHY_REFCLK_DET_ISO_CTRL_9	PHY_REFCLK_DET_ISO_CTRL_8
R-0h			R-0h	R-0h		R-0h	R-0h
7	6	5	4	3	2	1	0
PHY_REFCLK_DET_ISO_CTRL_7_1						PHY_REFCLK_DET_ISO_CTRL_0	
R-0h						W-0h	

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 12-913. PHY_REFCLK_DET_ISO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-13	PHY_REFCLK_DET_ISO_CTRL_15_13	R	0h	Reserved
12	PHY_REFCLK_DET_ISO_CTRL_12	R	0h	Captures the current value of the pma_cm_n_ext_refclk_detected_cfg PHY input.
11-10	PHY_REFCLK_DET_ISO_CTRL_11_10	R	0h	Reserved
9	PHY_REFCLK_DET_ISO_CTRL_9	R	0h	Current value of pma_cm_n_ext_refclk_detected PHY output.
8	PHY_REFCLK_DET_ISO_CTRL_8	R	0h	Current value of pma_cm_n_ext_refclk_detected_valid PHY output.
7-1	PHY_REFCLK_DET_ISO_CTRL_7_1	R	0h	Reserved
0	PHY_REFCLK_DET_ISO_CTRL_0	W	0h	External Reference Clock Active Detect Start: Write with 1 to initiate an external reference clock active detect operation. Any previous operation must have completed prior to writing with 1.

Table 12-914. Register Call Summary for PHY_REFCLK_DET_ISO_CTRL

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_REFCLK_DET_ISO_CTRL Register \(Offset = C028h\) \[reset = X\]: \[0\]](#)

12.305 PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register (Offset = D000h + formula) [reset = 0h]

PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j is shown in Figure 12-305 and described in Table 12-916.

Return to [Summary Table](#).

PIPE TX control signal isolation register

Offset = D000h + (j * 200h); where j = 0h to 3h

Table 12-915. PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 D000h + formula

Figure 12-305. PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_TX_LPC_LO_15_14		PHY_PIPE_ISO_TX_LPC_LO_13_8					
R-0h		R-0h					
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_TX_LPC_LO_7_6		PHY_PIPE_ISO_TX_LPC_LO_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_TX_CTRL_15_12				PHY_PIPE_ISO_TX_CTRL_11_9			PHY_PIPE_ISO_TX_CTRL_8
R/W-0h				R-0h			R/W-0h
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_TX_CTRL_7_5			PHY_PIPE_ISO_TX_CTRL_4	PHY_PIPE_ISO_TX_CTRL_3	PHY_PIPE_ISO_TX_CTRL_2	PHY_PIPE_ISO_TX_CTRL_1_0	
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-916. PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PIPE_ISO_TX_LPC_LO_15_14	R	0h	Reserved
29-24	PHY_PIPE_ISO_TX_LPC_LO_13_8	R	0h	Current value of pipe_tx_local_tx_preset_coefficients [11:6] for the associated lane when PHY_PCS_ISO_TX_LPC_HI[15] == 1. Otherwise, 0.
23-22	PHY_PIPE_ISO_TX_LPC_LO_7_6	R	0h	Reserved
21-16	PHY_PIPE_ISO_TX_LPC_LO_5_0	R	0h	Current value of pipe_tx_local_tx_preset_coefficients [5:0] for the associated lane when PHY_PCS_ISO_TX_LPC_HI[15] == 1. Otherwise, 0.
15-12	PHY_PIPE_ISO_TX_CTRL_15_12	R/W	0h	Drives pipe_tx_data_k PHY input for the associated lane when in PHY macro and PMA isolation modes.
11-9	PHY_PIPE_ISO_TX_CTRL_11_9	R	0h	Reserved
8	PHY_PIPE_ISO_TX_CTRL_8	R/W	0h	Drives pipe_tx_ones_zeros input for the associated lane when in PHY macro and PMA isolation modes.

**Table 12-916. PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
7-5	PHY_PIPE_ISO_TX_CTRL_7_5	R	0h	Reserved
4	PHY_PIPE_ISO_TX_CTRL_4	R/W	0h	Drives pipe_tx_elec_idle PHY input for the associated lane when in PHY macro and PMA isolation modes
3	PHY_PIPE_ISO_TX_CTRL_3	R/W	0h	Drives pipe_tx_128b_enc_byp PHY input for the associated lane when in PHY macro and PMA isolation modes.
2	PHY_PIPE_ISO_TX_CTRL_2	R/W	0h	Drives pipe_tx_compliance PHY input for the associated lane when in PHY macro and PMA isolation modes.
1-0	PHY_PIPE_ISO_TX_CTRL_1_0	R/W	0h	Drives pipe_tx_pattern PHY input for the associated lane when in PHY macro and PMA isolation modes.

Table 12-917. Register Call Summary for PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j

10-G SerDes Registers

- [PHY_PIPE_ISO_TX_LPC_LO__PHY_PIPE_ISO_TX_CTRL_j Register \(Offset = D000h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.306 PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register (Offset = D004h + formula) [reset = 0h]

PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j is shown in Figure 12-306 and described in Table 12-919.

Return to [Summary Table](#).

PIPE TX local preset coefficients high isolation register

Offset = D004h + (j * 200h); where j = 0h to 3h

Table 12-918. PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Instances

Instance	Physical Address
SERDES_10G0	0505 D004h + formula

Figure 12-306. PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register

31	30	29	28	27	26	25	24
PHY_PCS_ISO_TX_DMPH_LO_15_14		PHY_PCS_ISO_TX_DMPH_LO_13_8					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
PHY_PCS_ISO_TX_DMPH_LO_7_6		PHY_PCS_ISO_TX_DMPH_LO_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_TX_LPC_HI_15	PHY_PIPE_ISO_TX_LPC_HI_14_13		PHY_PIPE_ISO_TX_LPC_HI_12	PHY_PIPE_ISO_TX_LPC_HI_11_8			
R-0h	R-0h		R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_TX_LPC_HI_7_6		PHY_PIPE_ISO_TX_LPC_HI_5_0					
R-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-919. PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PCS_ISO_TX_DMPH_LO_15_14	R	0h	Reserved
29-24	PHY_PCS_ISO_TX_DMPH_LO_13_8	R/W	0h	Drives pipe_tx_deemph[11:6] PHY input for the associated lane when in PHY macro and PMA isolation mode.
23-22	PHY_PCS_ISO_TX_DMPH_LO_7_6	R	0h	Reserved
21-16	PHY_PCS_ISO_TX_DMPH_LO_5_0	R/W	0h	Drives pipe_tx_deemph[5:0] PHY input for the associated lane when in PHY macro and PMA isolation mode.
15	PHY_PIPE_ISO_TX_LPC_HI_15	R	0h	Set upon assertion of pipe_tx_local_tx_coeff_vld PHY output for the associated lane. Cleared upon writing PHY_PCS_ISO_TX_LPC_HI[12] with a 0.
14-13	PHY_PIPE_ISO_TX_LPC_HI_14_13	R	0h	Reserved
12	PHY_PIPE_ISO_TX_LPC_HI_12	R/W	0h	Drives pipe_tx_get_local_preset_coef PHY output for the associated lane when in PHY macro and PMA isolation modes

**Table 12-919. PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
11-8	PHY_PIPE_ISO_TX_LPC_HI_11_8	R/W	0h	Drives pipe_tx_local_preset_index PHY output for the associated lane when in PHY macro and PMA isolation modes.
7-6	PHY_PIPE_ISO_TX_LPC_HI_7_6	R	0h	Reserved
5-0	PHY_PIPE_ISO_TX_LPC_HI_5_0	R	0h	Current value of pipe_tx_local_tx_preset_coefficients[17:12] for the associated lane when PHY_PCS_ISO_TX_LPC_HI[15] == 1. Otherwise, 0.

Table 12-920. Register Call Summary for PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j

10-G SerDes Registers

- [PHY_PCS_ISO_TX_DMPH_LO__PHY_PIPE_ISO_TX_LPC_HI_j Register \(Offset = D004h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.307 PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Register (Offset = D008h + formula) [reset = 0h]

PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j is shown in Figure 12-307 and described in Table 12-922.

Return to [Summary Table](#).

PIPE TX deemphasis high isolation register

Offset = D008h + (j * 200h); where j = 0h to 3h

Table 12-921. PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Instances

Instance	Physical Address
SERDES_10G0	0505 D008h + formula

Figure 12-307. PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_TX_FSLF_15_14		PHY_PIPE_ISO_TX_FSLF_13_8					
R-0h		R-0h					
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_TX_FSLF_7_6		PHY_PIPE_ISO_TX_FSLF_5_0					
R-0h		R-0h					
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_TX_DMPH_HI_15_6							
R-0h							
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_TX_DMPH_HI_15_6		PHY_PIPE_ISO_TX_DMPH_HI_5_0					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-922. PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PIPE_ISO_TX_FSLF_15_14	R	0h	Reserved
29-24	PHY_PIPE_ISO_TX_FSLF_13_8	R	0h	Current value of pipe_tx_local_fs PHY output for the associated lane. (Not re-synchronized to apb_pclk)
23-22	PHY_PIPE_ISO_TX_FSLF_7_6	R	0h	Reserved
21-16	PHY_PIPE_ISO_TX_FSLF_5_0	R	0h	Current value of pipe_tx_local_if PHY output for the associated lane. (Not re-synchronized to apb_pclk)
15-6	PHY_PIPE_ISO_TX_DMPH_HI_15_6	R	0h	Reserved
5-0	PHY_PIPE_ISO_TX_DMPH_HI_5_0	R/W	0h	Drives pipe_tx_deemph[17:12] PHY input for the associated lane when in PHY macro and PMA isolation modes.

Table 12-923. Register Call Summary for PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_PIPE_ISO_TX_FSLF__PHY_PIPE_ISO_TX_DMPH_HI_j Register \(Offset = D008h + formula\) \[reset = 0h\]: \[0\]](#)

12.308 PHY_PCS_ISO_TX_DATA_HI__PHY_PCS_ISO_TX_DATA_LO_j Register (Offset = D00Ch + formula) [reset = 0h]

PHY_PCS_ISO_TX_DATA_HI__PHY_PCS_ISO_TX_DATA_LO_j is shown in [Figure 12-308](#) and described in [Table 12-925](#).

Return to [Summary Table](#).

PCS TX PIPE data low isolation register

Offset = D00Ch + (j * 200h); where j = 0h to 3h

Table 12-924. PHY_PCS_ISO_TX_DATA_HI__PHY_PCS_ISO_TX_DATA_LO_j Instances

Instance	Physical Address
SERDES_10G0	0505 D00Ch + formula

Figure 12-308. PHY_PCS_ISO_TX_DATA_HI__PHY_PCS_ISO_TX_DATA_LO_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_PCS_ISO_TX_DATA_HI_15_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PCS_ISO_TX_DATA_LO_15_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-925. PHY_PCS_ISO_TX_DATA_HI__PHY_PCS_ISO_TX_DATA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_PCS_ISO_TX_DATA_HI_15_0	R/W	0h	Drives pipe_tx_data[31:16] PHY input for the associated lane when in PHY macro and PMA isolation mode.
15-0	PHY_PCS_ISO_TX_DATA_LO_15_0	R/W	0h	Drives pipe_tx_data[15:0] PHY input for the associated lane when in PHY macro and PMA isolation mode.

Table 12-926. Register Call Summary for PHY_PCS_ISO_TX_DATA_HI__PHY_PCS_ISO_TX_DATA_LO_j

10-G SerDes Registers

- [PHY_PCS_ISO_TX_DATA_HI__PHY_PCS_ISO_TX_DATA_LO_j Register \(Offset = D00Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.309 PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CTRL_j Register (Offset = D010h + formula) [reset = 00400010h]

PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CTRL_j is shown in Figure 12-309 and described in Table 12-928.

Return to [Summary Table](#).

PCS RX control signal isolation register

Offset = D010h + (j * 200h); where j = 0h to 3h

**Table 12-927. PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CTRL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 D010h + formula

Figure 12-309. PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PIPE_ISO_RX_EQ_EVAL_15_13			PHY_PIPE_ISO_RX_EQ_EVAL_12	PHY_PIPE_ISO_RX_EQ_EVAL_11	PHY_PIPE_ISO_RX_EQ_EVAL_10	PHY_PIPE_ISO_RX_EQ_EVAL_9	PHY_PIPE_ISO_RX_EQ_EVAL_8
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PHY_PIPE_ISO_RX_EQ_EVAL_7	PHY_PIPE_ISO_RX_EQ_EVAL_6	PHY_PIPE_ISO_RX_EQ_EVAL_5_0					
R-0h	R-1h	R-0h					
15	14	13	12	11	10	9	8
PHY_PCS_ISO_RX_CTRL_15_12				PHY_PCS_ISO_RX_CTRL_11_10	PHY_PCS_ISO_RX_CTRL_9	PHY_PCS_ISO_RX_CTRL_8	
R-0h				R-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
PHY_PCS_ISO_RX_CTRL_7	PHY_PCS_ISO_RX_CTRL_6	PHY_PCS_ISO_RX_CTRL_5	PHY_PCS_ISO_RX_CTRL_4	PHY_PCS_ISO_RX_CTRL_3	PHY_PCS_ISO_RX_CTRL_2_0		
R/W-0h	R-0h	R-0h	R-1h	R-0h	R-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-928. PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	PHY_PIPE_ISO_RX_EQ_EVAL_15_13	R	0h	Reserved
28	PHY_PIPE_ISO_RX_EQ_EVAL_12	R/W	0h	Drives pipe_invalid_request for the associated lane when in PHY macro and PMA isolation modes.
27	PHY_PIPE_ISO_RX_EQ_EVAL_11	R/W	0h	pipe_link_eval_dir_change[5:4] bit reversal enable. When low, no bit reversal. When high, the bit positions for pipe_link_eval_dir_change[5:4] PHY output for the associated lane are reversed.
26	PHY_PIPE_ISO_RX_EQ_EVAL_10	R/W	0h	pipe_link_eval_dir_change[3:2] bit reversal enable. When low, no bit reversal. When high, the bit positions for pipe_link_eval_dir_change[3:2] PHY output for the associated lane are reversed.

**Table 12-928. PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
25	PHY_PIPE_ISO_RX_EQ_EVAL_9	R/W	0h	pipe_link_eval_dir_change[1:0] bit reversal enable. When low, no bit reversal. When high, the bit positions for pipe_link_eval_dir_change[1:0] PHY output for the associated lane are reversed.
24	PHY_PIPE_ISO_RX_EQ_EVAL_8	R/W	0h	Drives pipe_rx_eval PHY input for the associated lane when in PHY macro and PMA isolation modes.
23	PHY_PIPE_ISO_RX_EQ_EVAL_7	R	0h	Reserved
22	PHY_PIPE_ISO_RX_EQ_EVAL_6	R	1h	Captures pipe_phy_status for Rx equalization evaluation PHY output for the associated lane (does not include power state change signaling). Set when pipe_phy_status is high and pipe_rx_eq_eval to the PCS is high (i.e. after the isolation MUX). Cleared upon read.
21-16	PHY_PIPE_ISO_RX_EQ_EVAL_5_0	R	0h	pipe_link_eval_dir_change PHY output for the associated lane (prior to bit reversal logic) upon completion of Rx equalization evaluation. Captured upon assertion of Rx equalization eval pipe_phy_status when pipe_rx_eq_eval to the PCS (i.e. after the isolation MUX) is high. Cleared upon read. (Not re-synchronized to apb_pclk)
15-12	PHY_PCS_ISO_RX_CTRL_15_12	R	0h	Current value of pipe_rx_data_k PHY output for the associated lane, when PHY_PCS_ISO_RX_CTRL[5] == 1. Otherwise, 0. (Not re-synchronized to apb_pclk)
11-10	PHY_PCS_ISO_RX_CTRL_11_10	R	0h	Reserved
9	PHY_PCS_ISO_RX_CTRL_9	R/W	0h	Drives pipe_rx_eq_training PHY input for the associated lane when in PHY macro and PMA isolation modes.
8	PHY_PCS_ISO_RX_CTRL_8	R/W	0h	Drives pipe_rx_termination PHY input for the associated lane when in PHY macro and PMA isolation modes.
7	PHY_PCS_ISO_RX_CTRL_7	R/W	0h	Drives pipe_rx_polarity PHY input for the associated lane when in PHY macro and PMA isolation modes.
6	PHY_PCS_ISO_RX_CTRL_6	R	0h	Reserved
5	PHY_PCS_ISO_RX_CTRL_5	R	0h	Current value of pipe_rx_valid PHY output for the associated lane.
4	PHY_PCS_ISO_RX_CTRL_4	R	1h	Current value of pipe_rx_elec_idle PHY output for the associated lane.
3	PHY_PCS_ISO_RX_CTRL_3	R	0h	Current value of pipe_align_detect PHY output for the associated lane.
2-0	PHY_PCS_ISO_RX_CTRL_2_0	R	0h	Current value of pipe_rx_status PHY output for the associated lane. Holds the highest priority pipe_rx_status value seen, since the last register read. Cleared upon read.

Table 12-929. Register Call Summary for PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CTRL_j

10-G SerDes Registers
<ul style="list-style-type: none"> 10-G SerDes Registers: [0] PHY_PIPE_ISO_RX_EQ_EVAL__PHY_PCS_ISO_RX_CTRL_j Register (Offset = D010h + formula) [reset = 00400010h]: [0]

12.310 PHY_PCS_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register (Offset = D014h + formula) [reset = 00230000h]

PHY_PCS_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j is shown in Figure 12-310 and described in Table 12-931.

Return to [Summary Table](#).

PHY link configuration isolation register

Offset = D014h + (j * 200h); where j = 0h to 3h

Table 12-930. PHY_PCS_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Instances

Instance	Physical Address
SERDES_10G0	0505 D014h + formula

Figure 12-310. PHY_PCS_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register

31	30	29	28	27	26	25	24
PHY_PCS_ISO_LINK_CTRL_15_14	PHY_PCS_ISO_LINK_CTRL_13	PHY_PCS_ISO_LINK_CTRL_12	PHY_PCS_ISO_LINK_CTRL_11	PHY_PCS_ISO_LINK_CTRL_10	PHY_PCS_ISO_LINK_CTRL_9_8		
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		
23	22	21	20	19	18	17	16
PHY_PCS_ISO_LINK_CTRL_7	PHY_PCS_ISO_LINK_CTRL_6_4			PHY_PCS_ISO_LINK_CTRL_3	PHY_PCS_ISO_LINK_CTRL_2	PHY_PCS_ISO_LINK_CTRL_1	PHY_PCS_ISO_LINK_CTRL_0
R-0h	R/W-2h			R-0h	R/W-0h	R-1h	R/W-1h
15	14	13	12	11	10	9	8
PHY_ISO_LINK_CFG_15	PHY_ISO_LINK_CFG_14_13	PHY_ISO_LINK_CFG_12		PHY_ISO_LINK_CFG_11_10		PHY_ISO_LINK_CFG_9_8	
R/W-0h	R-0h	R/W-0h		R-0h		R/W-0h	
7	6	5	4	3	2	1	0
PHY_ISO_LINK_CFG_7_6	PHY_ISO_LINK_CFG_5	PHY_ISO_LINK_CFG_4		PHY_ISO_LINK_CFG_3_2		PHY_ISO_LINK_CFG_1_0	
R-0h	R/W-0h	R/W-0h		R-0h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-931. PHY_PCS_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PCS_ISO_LINK_CTRL_15_14	R	0h	Reserved
29	PHY_PCS_ISO_LINK_CTRL_13	R	0h	Current value of phy_l*_ack_l1_x PHY output for the associated lane.
28	PHY_PCS_ISO_LINK_CTRL_12	R/W	0h	Drives the phy_l*_ent_l1_x PHY input for the associated lane when in PHY macro and PMA isolation modes. (Link signal - for multi-lane links, master lane used for all lanes in link.)
27	PHY_PCS_ISO_LINK_CTRL_11	R/W	0h	Drives the phy_l*_rx_elec_idle_det_en PHY input for the associated lane when in PHY macro and PMA isolation modes. (Link signal - for multi-lane links, master lane used for all lanes in link.)
26	PHY_PCS_ISO_LINK_CTRL_10	R/W	0h	Drives the phy_l*_tx_cm_n_mode_en PHY input for the associated lane when in PHY macro and PMA isolation modes. (Link signal - for multi-lane links, master lane used for all lanes in link.)

Table 12-931. PHY_PCS_ISO_LINK_CTRL_PHY_ISO_LINK_CFG_j Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
25-24	PHY_PCS_ISO_LINK_CTRL_9_8	R/W	0h	Drives the pipe_l*_rate PHY input for the associated lane when in PHY macro and PMA isolation modes. (Link signal - for multi-lane links, master lane used for all lanes in link.)
23	PHY_PCS_ISO_LINK_CTRL_7	R	0h	Reserved
22-20	PHY_PCS_ISO_LINK_CTRL_6_4	R/W	2h	Drives the pipe_l*_powerdown PHY input for the associated lane when in PHY macro and PMA isolation modes. (Link signal - for multi-lane links, master lane used for all lanes in link.)
19	PHY_PCS_ISO_LINK_CTRL_3	R	0h	Reserved
18	PHY_PCS_ISO_LINK_CTRL_2	R/W	0h	Drives the pipe_l*_tx_det_rx_lpbk PHY input for the associated lane when in PHY macro and PMA isolation modes. (Link signal - for multi-lane links, master lane used for all lanes in link.)
17	PHY_PCS_ISO_LINK_CTRL_1	R	1h	Captures pipe_l*_phy_status (for power state and rate change) PHY output for the associated lane. Set when pipe_phy_status is high and cleared upon read if pipe_phy_status is low.
16	PHY_PCS_ISO_LINK_CTRL_0	R/W	1h	Drives the phy_l*_reset_n PHY input for the associated lane when in PHY macro and PMA isolation modes. (Link signal - for multi-lane links, master lane used for all lanes in link.)
15	PHY_ISO_LINK_CFG_15	R/W	0h	Drives phy_link_cfg_ln_{nnnn} PHY input when in PHY macro and PMA isolation modes.
14-13	PHY_ISO_LINK_CFG_14_13	R	0h	Reserved
12	PHY_ISO_LINK_CFG_12	R/W	0h	Drives pipe_l{nnnn}_32bit_sel PHY input when in PHY macro and PMA isolation modes.
11-10	PHY_ISO_LINK_CFG_11_10	R	0h	Reserved
9-8	PHY_ISO_LINK_CFG_9_8	R/W	0h	Drives pma_fullrt_div_ln_{nnnn} PHY input when in PHY macro and PMA isolation modes.
7-6	PHY_ISO_LINK_CFG_7_6	R	0h	Reserved
5	PHY_ISO_LINK_CFG_5	R/W	0h	Drives pipe_l{nnnn}_pcie_l1_ss_sel PHY input when in PHY macro and PMA isolation mode.
4	PHY_ISO_LINK_CFG_4	R/W	0h	Drives pipe_l{nnnn}_eb_mode PHY input when in PHY macro and PMA isolation modes.
3-2	PHY_ISO_LINK_CFG_3_2	R	0h	Reserved
1-0	PHY_ISO_LINK_CFG_1_0	R/W	0h	Drives phy_l{nnnn}_mode PHY input when in PHY macro and PMA isolation modes.

Table 12-932. Register Call Summary for PHY_PCS_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j

10-G SerDes Registers

- [PHY_PCS_ISO_LINK_CTRL__PHY_ISO_LINK_CFG_j Register \(Offset = D014h + formula\) \[reset = 00230000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.311 PHY_PIPE_ISO_USB_BER_CNT_j Register (Offset = D018h + formula) [reset = X]

PHY_PIPE_ISO_USB_BER_CNT_j is shown in Figure 12-311 and described in Table 12-934.

Return to [Summary Table](#).

PIPE USB Gen 1 loopback slave BER count register

Offset = D018h + (j * 200h); where j = 0h to 3h

**Table 12-933. PHY_PIPE_ISO_USB_BER_CNT_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 D018h + formula

Figure 12-311. PHY_PIPE_ISO_USB_BER_CNT_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
PHY_PIPE_ISO_USB_BER_CNT_15_8							
R-0h							
7	6	5	4	3	2	1	0
PHY_PIPE_ISO_USB_BER_CNT_7_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 12-934. PHY_PIPE_ISO_USB_BER_CNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-8	PHY_PIPE_ISO_USB_BER_CNT_15_8	R	0h	Reserved
7-0	PHY_PIPE_ISO_USB_BER_CNT_7_0	R	0h	Current value of USB 3.1 Gen 1 loopback slave Bit Error Count from the PCS.

Table 12-935. Register Call Summary for PHY_PIPE_ISO_USB_BER_CNT_j

10-G SerDes Registers

- [PHY_PIPE_ISO_USB_BER_CNT_j Register \(Offset = D018h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.312 PHY_PCS_ISO_RX_DATA_HI__PHY_PCS_ISO_RX_DATA_LO_j Register (Offset = D01Ch + formula) [reset = 0h]

PHY_PCS_ISO_RX_DATA_HI__PHY_PCS_ISO_RX_DATA_LO_j is shown in [Figure 12-312](#) and described in [Table 12-937](#).

Return to [Summary Table](#).

PCS RX data low isolation register

Offset = D01Ch + (j * 200h); where j = 0h to 3h

Table 12-936. PHY_PCS_ISO_RX_DATA_HI__PHY_PCS_ISO_RX_DATA_LO_j Instances

Instance	Physical Address
SERDES_10G0	0505 D01Ch + formula

Figure 12-312. PHY_PCS_ISO_RX_DATA_HI__PHY_PCS_ISO_RX_DATA_LO_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_PCS_ISO_RX_DATA_HI_15_0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PCS_ISO_RX_DATA_LO_15_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 12-937. PHY_PCS_ISO_RX_DATA_HI__PHY_PCS_ISO_RX_DATA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_PCS_ISO_RX_DATA_HI_15_0	R	0h	Current value of pipe_rx_data[31:16] PHY output. (Not re-synchronized to apb_pclk)
15-0	PHY_PCS_ISO_RX_DATA_LO_15_0	R	0h	Current value of pipe_rx_data[15:0] PHY output. (Not re-synchronized to apb_pclk)

Table 12-938. Register Call Summary for PHY_PCS_ISO_RX_DATA_HI__PHY_PCS_ISO_RX_DATA_LO_j

10-G SerDes Registers

- [PHY_PCS_ISO_RX_DATA_HI__PHY_PCS_ISO_RX_DATA_LO_j Register \(Offset = D01Ch + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.313 PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register (Offset = D020h + formula) [reset = 00810000h]

PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j is shown in Figure 12-313 and described in Table 12-940.

Return to [Summary Table](#).

Ethernet MAC clock configuration isolation register

Offset = D020h + (j * 200h); where j = 0h to 3h

Table 12-939.
PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Instances

Instance	Physical Address
SERDES_10G0	0505 D020h + formula

Figure 12-313. PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register

31	30	29	28	27	26	25	24
PHY_ETH_ISO_MAC_CLK_DIV_15_7							
R/W-1h							
23	22	21	20	19	18	17	16
PHY_ETH_ISO_MAC_CLK_DIV_15_7	PHY_ETH_ISO_MAC_CLK_DIV_6_0						
R/W-1h	R/W-1h						
15	14	13	12	11	10	9	8
PHY_ETH_ISO_MAC_CLK_CFG_15_2							
R-0h							
7	6	5	4	3	2	1	0
PHY_ETH_ISO_MAC_CLK_CFG_15_2						PHY_ETH_ISO_MAC_CLK_CFG_1_0	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-940. PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	PHY_ETH_ISO_MAC_CLK_DIV_15_7	R/W	1h	Drives mac_div_sel1 PHY input for the associated lane when in PHY macro and PMA isolation mode.
22-16	PHY_ETH_ISO_MAC_CLK_DIV_6_0	R/W	1h	Drives mac_div_sel0 PHY input for the associated lane when in PHY macro and PMA isolation mode.
15-2	PHY_ETH_ISO_MAC_CLK_CFG_15_2	R	0h	Reserved
1-0	PHY_ETH_ISO_MAC_CLK_CFG_1_0	R/W	0h	Drives mac_src_sel PHY input for the associated lane when in PHY macro and PMA isolation mode.

Table 12-941. Register Call Summary for
PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j

10-G SerDes Registers

- [PHY_ETH_ISO_MAC_CLK_DIV__PHY_ETH_ISO_MAC_CLK_CFG_j Register \(Offset = D020h + formula\) \[reset = 00810000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.314 PHY_INTERRUPT_STS_j Register (Offset = D024h + formula) [reset = X]

PHY_INTERRUPT_STS_j is shown in [Figure 12-314](#) and described in [Table 12-943](#).

Return to [Summary Table](#).

PHY interrupt status register

Offset = D024h + (j * 200h); where j = 0h to 3h

Table 12-942. PHY_INTERRUPT_STS_j Instances

Instance	Physical Address
SERDES_10G0	0505 D024h + formula

Figure 12-314. PHY_INTERRUPT_STS_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_INTERRUPT_STS_15	PHY_INTERRUPT_STS_14_11				PHY_INTERRUPT_STS_10_8		
R/W-0h	R-0h				R-0h		
7	6	5	4	3	2	1	0
PHY_INTERRUPT_STS_7	PHY_INTERRUPT_STS_6_4			PHY_INTERRUPT_STS_3_2		PHY_INTERRUPT_STS_1	PHY_INTERRUPT_STS_0
R-0h	R-0h			R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-943. PHY_INTERRUPT_STS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	PHY_INTERRUPT_STS_15	R/W	0h	State change monitor enable - 1 = state change monitor enabled, 0 = state change monitor disabled. Note: Only the master lane's state change monitor for a link is enabled. The state change monitor for a slave lane is disabled regardless of the state of this bit.
14-11	PHY_INTERRUPT_STS_14_11	R	0h	Reserved
10-8	PHY_INTERRUPT_STS_10_8	R	0h	Next power state/data rate - Only valid when one of the interrupt status bits is set. Indicates the requested power state or data rate for the state change failure. For PIPE requests, loaded based on the following: For Raw SerDes power state change requests, loaded based on following:
7	PHY_INTERRUPT_STS_7	R	0h	Reserved

Table 12-943. PHY_INTERRUPT_STS_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	PHY_INTERRUPT_STS_6_4	R	0h	Current power state/data rate - Only valid when one of the interrupt status bits is set. Indicates the starting power state or data rate for the state change failure. For PIPE requests, loaded based on the following: For Raw SerDes power state change requests, loaded based on following:
3-2	PHY_INTERRUPT_STS_3_2	R	0h	Reserved
1	PHY_INTERRUPT_STS_1	R/W	0h	Data rate state change interrupt status - Set to 1 upon data rate change timeout. Cleared upon read. Bit is writeable to allow the interrupt to be set manually for test purposes. Only set high by data rate change timeout if bit[0] == 0.
0	PHY_INTERRUPT_STS_0	R/W	0h	Power state change interrupt status - Set to 1 upon power state change timeout. Cleared upon read. Bit is writeable to allow the interrupt to set manually for test purposes. Only set high by power state change timeout if bit[1] == 0.

Table 12-944. Register Call Summary for PHY_INTERRUPT_STS_j

10-G SerDes Registers

- [PHY_INTERRUPT_STS_j Register \(Offset = D024h + formula\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.315 PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1 Register (Offset = E000h) [reset = 000C0000h]

PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1 is shown in Figure 12-315 and described in Table 12-946.

Return to [Summary Table](#).

PMA common control1 register

Table 12-945.
PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1
Instances

Instance	Physical Address
SERDES_10G0	0505 E000h

Figure 12-315. PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1 Register

31	30	29	28	27	26	25	24
PHY_PMA_CMN_CTRL2_15_8							
R-0h							
23	22	21	20	19	18	17	16
PHY_PMA_CMN_CTRL2_7	PHY_PMA_CMN_CTRL2_6	PHY_PMA_CMN_CTRL2_5	PHY_PMA_CMN_CTRL2_4	PHY_PMA_CMN_CTRL2_3	PHY_PMA_CMN_CTRL2_2	PHY_PMA_CMN_CTRL2_1	PHY_PMA_CMN_CTRL2_0
R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-0h	R-0h
15	14	13	12	11	10	9	8
PHY_PMA_CMN_CTRL1_15_7							
R-0h							
7	6	5	4	3	2	1	0
PHY_PMA_CMN_CTRL1_15_7	PHY_PMA_CMN_CTRL1_6	PHY_PMA_CMN_CTRL1_5	PHY_PMA_CMN_CTRL1_4	PHY_PMA_CMN_CTRL1_3_1			PHY_PMA_CMN_CTRL1_0
R-0h	R/W-0h	R-0h	R-0h	R-0h			R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-946. PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PMA_CMN_CTRL2_15_8	R	0h	Reserved
23	PHY_PMA_CMN_CTRL2_7	R	0h	Current value of cmn_pll1_locked PMA output
22	PHY_PMA_CMN_CTRL2_6	R	0h	Current value of cmn_pll0_locked PMA output
21	PHY_PMA_CMN_CTRL2_5	R	0h	Current value of cmn_pll1_clk_en_ack PMA output
20	PHY_PMA_CMN_CTRL2_4	R	0h	Current value of cmn_pll0_clk_en_ack PMA output
19	PHY_PMA_CMN_CTRL2_3	R	1h	Current value of cmn_pll1_disabled PMA output
18	PHY_PMA_CMN_CTRL2_2	R	1h	Current value of cmn_pll0_disabled PMA output
17	PHY_PMA_CMN_CTRL2_1	R	0h	Current value of cmn_pll1_ready PMA output
16	PHY_PMA_CMN_CTRL2_0	R	0h	Current value of cmn_pll0_ready PMA output
15-7	PHY_PMA_CMN_CTRL1_15_7	R	0h	Reserved
6	PHY_PMA_CMN_CTRL1_6	R/W	0h	Drives cmn_refclk_rcv_out_en PMA input

Table 12-946. PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PHY_PMA_CMN_CTRL1_5	R	0h	Current value of cmn_macro_suspend_ack PMA output
4	PHY_PMA_CMN_CTRL1_4	R	0h	Current value of cmn_refclk_active PMA output
3-1	PHY_PMA_CMN_CTRL1_3_1	R	0h	Reserved
0	PHY_PMA_CMN_CTRL1_0	R	0h	Current value of cmn_ready pin PMA output

Table 12-947. Register Call Summary for PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1

10-G SerDes Registers

- [PHY_PMA_CMN_CTRL2__PHY_PMA_CMN_CTRL1 Register \(Offset = E000h\) \[reset = 000C0000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.316 PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE Register (Offset = E004h) [reset = 00030000h]

PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE is shown in Figure 12-316 and described in Table 12-949.

Return to [Summary Table](#).

PMA SSM current state register

Table 12-948. PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE Instances

Instance	Physical Address
SERDES_10G0	0505 E004h

Figure 12-316. PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE Register

31	30	29	28	27	26	25	24
PHY_PMA_PLL_RAW_CTRL_15_2							
R-0h							
23	22	21	20	19	18	17	16
PHY_PMA_PLL_RAW_CTRL_15_2						PHY_PMA_PLL_RAW_CTRL_1	PHY_PMA_PLL_RAW_CTRL_0
R-0h						R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
PHY_PMA_SSM_STATE_15_9						PHY_PMA_SSM_STATE_8_0	
R-0h						R-0h	
7	6	5	4	3	2	1	0
PHY_PMA_SSM_STATE_8_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-949. PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	PHY_PMA_PLL_RAW_CTRL_15_2	R	0h	Reserved
17	PHY_PMA_PLL_RAW_CTRL_1	R/W	1h	Raw SerDes PLL1 control : When set to 1, cmn_pll1_en PMA input is controlled by PHY logic. When set to 0, cmn_pll1_en PMA input is forced low. When PLL1 is driving lanes configured for Raw SerDes operation, this bit allows manual enable/disable of PLL1 to allow reconfiguration of the PLL for a different data rate. The PHY logic drives cmn_pll1_en high unless the PHY is configured to operation on PLL0 only (PHY_PLL_CFG[1] == 0).
16	PHY_PMA_PLL_RAW_CTRL_0	R/W	1h	Raw SerDes PLL0 control : When set to 1, cmn_pll0_en PMA input is controlled by PHY logic. When set to 0, cmn_pll0_en PMA input is forced low. When PLL0 is driving lanes configured for Raw SerDes operation, this bit allows manual enable/disable of PLL0 to allow reconfiguration of the PLL for a different data rate. The PHY logic drives cmn_pll0_en high except when the PHY is configured for single link PCIe mode and is performing a rate change between PCIe Gen 1/2 and PCIe Gen 3 (PHY_PLL_CFG[0] == 1). However, PCIe is only supported for PIPE mode and not applicable when PLL0 is driving lanes configured for Raw SerDes operation.

**Table 12-949. PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15-9	PHY_PMA_SSM_STATE_15_9	R	0h	Reserved
8-0	PHY_PMA_SSM_STATE_8_0	R	0h	PMA SSM : Current state of the PMA startup state machine. PMA output (Not re-synchronized to apb_pclk)

Table 12-950. Register Call Summary for PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_PMA_PLL_RAW_CTRL__PHY_PMA_SSM_STATE Register \(Offset = E004h\) \[reset = 00030000h\]: \[0\]](#)

12.317 PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CTRL Register (Offset = E008h) [reset = 00030001h]

PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CTRL is shown in Figure 12-317 and described in Table 12-952.

Return to [Summary Table](#).

PMA common control signal isolation register

Table 12-951. PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 E008h

Figure 12-317. PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CTRL Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_PLL_CTRL0_15_8							
R-0h							
23	22	21	20	19	18	17	16
PHY_PMA_ISO_PLL_CTRL0_7	PHY_PMA_ISO_PLL_CTRL0_6	PHY_PMA_ISO_PLL_CTRL0_5	PHY_PMA_ISO_PLL_CTRL0_4	PHY_PMA_ISO_PLL_CTRL0_3	PHY_PMA_ISO_PLL_CTRL0_2	PHY_PMA_ISO_PLL_CTRL0_1	PHY_PMA_ISO_PLL_CTRL0_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h
15	14	13	12	11	10	9	8
PHY_PMA_ISO_CMN_CTRL_1_5	PHY_PMA_ISO_CMN_CTRL_1_4	PHY_PMA_ISO_CMN_CTRL_13_12		PHY_PMA_ISO_CMN_CTRL_11_10		PHY_PMA_ISO_CMN_CTRL_9_8	
R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
PHY_PMA_ISO_CMN_CTRL_7	PHY_PMA_ISO_CMN_CTRL_6	PHY_PMA_ISO_CMN_CTRL_5	PHY_PMA_ISO_CMN_CTRL_4	PHY_PMA_ISO_CMN_CTRL_3	PHY_PMA_ISO_CMN_CTRL_2	PHY_PMA_ISO_CMN_CTRL_1	PHY_PMA_ISO_CMN_CTRL_0
R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-952. PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_PMA_ISO_PLL_CTRL0_15_8	R	0h	Reserved
23	PHY_PMA_ISO_PLL_CTRL0_7	R/W	0h	Drives cmn_pll1_ref_clk_sel PMA input when in PHY macro or PMA isolation mode.
22	PHY_PMA_ISO_PLL_CTRL0_6	R/W	0h	Drives cmn_pll0_ref_clk_sel PMA input when in PHY macro or PMA isolation mode.
21	PHY_PMA_ISO_PLL_CTRL0_5	R/W	0h	Drives cmn_pll1_mode_sel PMA input when in PMA isolation mode.
20	PHY_PMA_ISO_PLL_CTRL0_4	R/W	0h	Drives cmn_pll0_mode_sel PMA input when in PMA isolation mode.
19	PHY_PMA_ISO_PLL_CTRL0_3	R/W	0h	Drives cmn_pll1_clk_en PMA input when in PMA isolation mode
18	PHY_PMA_ISO_PLL_CTRL0_2	R/W	0h	Drives cmn_pll0_clk_en PMA input when in PMA isolation mode
17	PHY_PMA_ISO_PLL_CTRL0_1	R/W	1h	Drives cmn_pll1_en PMA input when in PMA isolation mode
16	PHY_PMA_ISO_PLL_CTRL0_0	R/W	1h	Drives cmn_pll0_en PMA input when in PMA isolation mode

**Table 12-952. PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CTRL Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
15	PHY_PMA_ISO_CMN_CTL_15	R/W	0h	Drives cmn_ref_clk_term_en PMA input when in PHY macro or PMA isolation modes
14	PHY_PMA_ISO_CMN_CTL_14	R/W	0h	Drives cmn_ref_clk_dig_sel PMA input when in PHY macro or PMA isolation modes
13-12	PHY_PMA_ISO_CMN_CTL_13_12	R/W	0h	Drives cmn_ref_clk_dig_div PMA input when in PHY macro or PMA isolation modes
11-10	PHY_PMA_ISO_CMN_CTL_11_10	R/W	0h	Drives cmn_ref_clk_int_mode PMA input when in PHY macro and PMA isolation modes.
9-8	PHY_PMA_ISO_CMN_CTL_9_8	R/W	0h	Drives cmn_ref_clk0_mode PMA input when in PHY macro and PMA isolation modes.
7	PHY_PMA_ISO_CMN_CTL_7	R	0h	Current value of cmn_clock_stop_ack PMA output.
6	PHY_PMA_ISO_CMN_CTL_6	R/W	0h	Drives cmn_clock_stop_req PMA input when in PMA isolation mode
5	PHY_PMA_ISO_CMN_CTL_5	R	0h	Reserved
4	PHY_PMA_ISO_CMN_CTL_4	R/W	0h	Drives cmn_ref_clk0_clk_gate_en PMA input when in PMA isolation mode.
3	PHY_PMA_ISO_CMN_CTL_3	R/W	0h	Drives cmn_refclk_disable PMA input when in PMA isolation mode.
2	PHY_PMA_ISO_CMN_CTL_2	R/W	0h	Drives cmn_macro_suspend_req PMA input when in PMA isolation mode.
1	PHY_PMA_ISO_CMN_CTL_1	R	0h	Reserved
0	PHY_PMA_ISO_CMN_CTL_0	R/W	1h	Drives cmn_reset_n PMA input when in PMA isolation mode.

Table 12-953. Register Call Summary for PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CTRL

10-G SerDes Registers

- [PHY_PMA_ISO_PLL_CTRL0__PHY_PMA_ISO_CMN_CTRL Register \(Offset = E008h\) \[reset = 00030001h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.318 PHY_PMA_ISO_PLL_CTRL1 Register (Offset = E00Ch) [reset = X]

PHY_PMA_ISO_PLL_CTRL1 is shown in Figure 12-318 and described in Table 12-955.

Return to [Summary Table](#).

PMA PLL control1 isolation register

Table 12-954. PHY_PMA_ISO_PLL_CTRL1 Instances

Instance	Physical Address
SERDES_10G0	0505 E00Ch

Figure 12-318. PHY_PMA_ISO_PLL_CTRL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_PMA_ISO_PLL_CTRL1_15_12				PHY_PMA_ISO_PLL_CTRL1_11_8			
R/W-1h				R/W-1h			
7	6	5	4	3	2	1	0
PHY_PMA_ISO_PLL_CTRL1_7_4				PHY_PMA_ISO_PLL_CTRL1_3_0			
R/W-2h				R/W-4h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-955. PHY_PMA_ISO_PLL_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-12	PHY_PMA_ISO_PLL_CTRL1_15_12	R/W	1h	Drives cmn_pll1_clk_datart1_div PMA input when in PMA isolation mode
11-8	PHY_PMA_ISO_PLL_CTRL1_11_8	R/W	1h	Drives cmn_pll1_clk_datart0_div PMA input when in PMA isolation mode
7-4	PHY_PMA_ISO_PLL_CTRL1_7_4	R/W	2h	Drives cmn_pll0_clk_datart1_div PMA input when in PMA isolation mode
3-0	PHY_PMA_ISO_PLL_CTRL1_3_0	R/W	4h	Drives cmn_pll0_clk_datart0_div PMA input when in PMA isolation mode

Table 12-956. Register Call Summary for PHY_PMA_ISO_PLL_CTRL1

10-G SerDes Registers

- [PHY_PMA_ISO_PLL_CTRL1 Register \(Offset = E00Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.319 PHY_PMA_PLL0_SM_STATE Register (Offset = E014h) [reset = X]

PHY_PMA_PLL0_SM_STATE is shown in [Figure 12-319](#) and described in [Table 12-958](#).

Return to [Summary Table](#).

PMA PLL0 State Machine current state register

**Table 12-957. PHY_PMA_PLL0_SM_STATE
Instances**

Instance	Physical Address
SERDES_10G0	0505 E014h

Figure 12-319. PHY_PMA_PLL0_SM_STATE Register

31	30	29	28	27	26	25	24
PHY_PMA_PLL0_SM_STATE_15_12				PHY_PMA_PLL0_SM_STATE_11_0			
R-0h				R-300h			
23	22	21	20	19	18	17	16
PHY_PMA_PLL0_SM_STATE_11_0							
R-300h							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							
R-X							

LEGEND: R = Read Only; -n = value after reset

Table 12-958. PHY_PMA_PLL0_SM_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	PHY_PMA_PLL0_SM_STATE_15_12	R	0h	Reserved
27-16	PHY_PMA_PLL0_SM_STATE_11_0	R	300h	Current value of cmn_pllsm0_state[11:0]. PMA output (Debug only: Not re-synchronized)
15-0	RESERVED	R	X	

Table 12-959. Register Call Summary for PHY_PMA_PLL0_SM_STATE

10-G SerDes Registers

- [PHY_PMA_PLL0_SM_STATE Register \(Offset = E014h\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.320 PHY_PMA_PLL1_SM_STATE Register (Offset = E018h) [reset = X]

PHY_PMA_PLL1_SM_STATE is shown in [Figure 12-320](#) and described in [Table 12-961](#).

Return to [Summary Table](#).

PMA PLL1 State Machine current state register

**Table 12-960. PHY_PMA_PLL1_SM_STATE
Instances**

Instance	Physical Address
SERDES_10G0	0505 E018h

Figure 12-320. PHY_PMA_PLL1_SM_STATE Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
PHY_PMA_PLL1_SM_STATE_15_12				PHY_PMA_PLL1_SM_STATE_11_0			
R-0h				R-300h			
7	6	5	4	3	2	1	0
PHY_PMA_PLL1_SM_STATE_11_0							
R-300h							

LEGEND: R = Read Only; -n = value after reset

Table 12-961. PHY_PMA_PLL1_SM_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-12	PHY_PMA_PLL1_SM_STATE_15_12	R	0h	Reserved
11-0	PHY_PMA_PLL1_SM_STATE_11_0	R	300h	Current value of cmn_pllsm1_state[11:0]. PMA output (Debug only: Not re-synchronized)

Table 12-962. Register Call Summary for PHY_PMA_PLL1_SM_STATE

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_PMA_PLL1_SM_STATE Register \(Offset = E018h\) \[reset = X\]: \[0\]](#)

12.321 PHY_PMA_ISOLATION_CTRL Register (Offset = E01Ch) [reset = X]

PHY_PMA_ISOLATION_CTRL is shown in [Figure 12-321](#) and described in [Table 12-964](#).

Return to [Summary Table](#).

PMA Isolation control register

Table 12-963. PHY_PMA_ISOLATION_CTRL Instances

Instance	Physical Address
SERDES_10G0	0505 E01Ch

Figure 12-321. PHY_PMA_ISOLATION_CTRL Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO LATION_CTRL _15	PHY_PMA_ISO LATION_CTRL _14	PHY_PMA_ISO LATION_CTRL _13	PHY_PMA_ISO LATION_CTRL _12	PHY_PMA_ISOLATION_CTRL_11_8			
R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
PHY_PMA_ISOLATION_CTRL_7_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-964. PHY_PMA_ISOLATION_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PMA_ISOLATION_C TRL_15	R/W	0h	PHY/PMA isolation enable (isolation_en) - When set, enables isolation (PHY or PMA).
30	PHY_PMA_ISOLATION_C TRL_14	R/W	0h	PHY/PMA common isolation enable (cmn_isolation_en) - When in PHY Macro Isolation Mode, the PHY common isolation register(s) are selected. When in PMA Isolation Mode, the PMA common isolation register(s) are selected.
29	PHY_PMA_ISOLATION_C TRL_13	R	0h	Reserved
28	PHY_PMA_ISOLATION_C TRL_12	R/W	0h	PHY/PMA isolation mode select (isolation_mode_sel) - When isolation_en is set, this bit selects between PHY isolation mode and PMA isolation mode. 0 = PHYMacro isolation mode 1 = PMA isolation mode.
27-24	PHY_PMA_ISOLATION_C TRL_11_8	R	0h	Reserved
23-16	PHY_PMA_ISOLATION_C TRL_7_0	R/W	0h	PHY/PMA lane isolation enable (ln_isolation_en) - When in PHY Macro Isolation Mode, the selected PHY lane(s) isolation registers are selected. When in PMA Isolation Mode, the selected PMA lane(s) isolation registers are selected.

Table 12-964. PHY_PMA_ISOLATION_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	RESERVED	R/W	X	

Table 12-965. Register Call Summary for PHY_PMA_ISOLATION_CTRL

10-G SerDes Registers

- [PHY_PMA_ISOLATION_CTRL Register \(Offset = E01Ch\) \[reset = X\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.322 PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j Register (Offset = F000h + formula) [reset = 0h]

PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j is shown in Figure 12-322 and described in Table 12-967.

Return to [Summary Table](#).

PMA transceiver control register

Offset = F000h + (j * 200h); where j = 0h to 3h

Table 12-966. PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 F000h + formula

Figure 12-322. PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PMA_XCVR_LPBK_15_9							PHY_PMA_XCVR_LPBK_8
R-0h							R/W-0h
23	22	21	20	19	18	17	16
PHY_PMA_XCVR_LPBK_7_6	PHY_PMA_XCVR_LPBK_5	PHY_PMA_XCVR_LPBK_4	PHY_PMA_XCVR_LPBK_3	PHY_PMA_XCVR_LPBK_2	PHY_PMA_XCVR_LPBK_1	PHY_PMA_XCVR_LPBK_0	
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
PHY_PMA_XCVR_CTRL_15_9							PHY_PMA_XCVR_CTRL_8
R-0h							R/W-0h
7	6	5	4	3	2	1	0
PHY_PMA_XCVR_CTRL_7_5			PHY_PMA_XCVR_CTRL_4	PHY_PMA_XCVR_CTRL_3	PHY_PMA_XCVR_CTRL_2	PHY_PMA_XCVR_CTRL_1	PHY_PMA_XCVR_CTRL_0
R-0h			R-0h	R-0h	R-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-967. PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	PHY_PMA_XCVR_LPBK_15_9	R	0h	Reserved
24	PHY_PMA_XCVR_LPBK_8	R/W	0h	Drives the tx_bist_hold PMA input for all lanes in the associated link (i.e. the bit associated with the master lane of the link drives all lanes in the link). Synchronized to transmit data rate clock.
23-22	PHY_PMA_XCVR_LPBK_7_6	R	0h	Reserved
21	PHY_PMA_XCVR_LPBK_5	R/W	0h	Drives the xcvr_lpbk_fe_parallel_en PMA input for the associated lane.
20	PHY_PMA_XCVR_LPBK_4	R/W	0h	Drives the xcvr_lpbk_ne_parallel_en PMA input for the associated lane.
19	PHY_PMA_XCVR_LPBK_3	R/W	0h	Drives the xcvr_lpbk_recovered_clk_en PMA input for the associated lane.
18	PHY_PMA_XCVR_LPBK_2	R/W	0h	Drives the xcvr_lpbk_line_en PMA input for the associated lane.

**Table 12-967. PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
17	PHY_PMA_XCVR_LPBK_1	R/W	0h	Drives the xcvr_lpbk_isi_gen_en PMA input for the associated lane.
16	PHY_PMA_XCVR_LPBK_0	R/W	0h	Drives the xcvr_lpbk_serial_en PMA input for the associated lane.
15-9	PHY_PMA_XCVR_CTRL_15_9	R	0h	Reserved
8	PHY_PMA_XCVR_CTRL_8	R/W	0h	Drives the tx_differential_invert PMA input for the associated lane.
7-5	PHY_PMA_XCVR_CTRL_7_5	R	0h	Reserved
4	PHY_PMA_XCVR_CTRL_4	R	0h	Current value of rx_cdrif_fphl_locked PMA output for the associated lane.
3	PHY_PMA_XCVR_CTRL_3	R	0h	Current value of rx_bist_status PMA output for the associated lane.
2	PHY_PMA_XCVR_CTRL_2	R	0h	Current value of rx_bist_err_toggle PMA output for the associated lane.
1	PHY_PMA_XCVR_CTRL_1	R	0h	Current value of rx_bist_sync PMA output for the associated lane.
0	PHY_PMA_XCVR_CTRL_0	R/W	0h	Drives the rx_differential_invert PMA input for the associated lane.

Table 12-968. Register Call Summary for PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_PMA_XCVR_LPBK__PHY_PMA_XCVR_CTRL_j Register \(Offset = F000h + formula\) \[reset = 0h\]: \[0\]](#)

12.323 PHY_PMA_ISO_XCVR_CTRL_j Register (Offset = F004h + formula) [reset = 0h]

PHY_PMA_ISO_XCVR_CTRL_j is shown in Figure 12-323 and described in Table 12-970.

Return to [Summary Table](#).

PMA Transceiver control isolation register

Offset = F004h + (j * 200h); where j = 0h to 3h

**Table 12-969. PHY_PMA_ISO_XCVR_CTRL_j
Instances**

Instance	Physical Address
SERDES_10G0	0505 F004h + formula

Figure 12-323. PHY_PMA_ISO_XCVR_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_XCVR_CTRL_15	PHY_PMA_ISO_XCVR_CTRL_14	PHY_PMA_ISO_XCVR_CTRL_13	PHY_PMA_ISO_XCVR_CTRL_12	PHY_PMA_ISO_XCVR_CTRL_11	PHY_PMA_ISO_XCVR_CTRL_10	PHY_PMA_ISO_XCVR_CTRL_9	PHY_PMA_ISO_XCVR_CTRL_8
R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
PHY_PMA_ISO_XCVR_CTRL_7	PHY_PMA_ISO_XCVR_CTRL_6	PHY_PMA_ISO_XCVR_CTRL_5	PHY_PMA_ISO_XCVR_CTRL_4	PHY_PMA_ISO_XCVR_CTRL_3	PHY_PMA_ISO_XCVR_CTRL_2	PHY_PMA_ISO_XCVR_CTRL_1	PHY_PMA_ISO_XCVR_CTRL_0
R/W-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
PHY_PMA_PI_POS_15_8							
R-0h							
7	6	5	4	3	2	1	0
PHY_PMA_PI_POS_7_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-970. PHY_PMA_ISO_XCVR_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PMA_ISO_XCVR_CTRL_15	R	0h	Current value of xcvr_pll_clk_en_ack PMA output for the associated lane.
30	PHY_PMA_ISO_XCVR_CTRL_14	R	0h	Reserved
29	PHY_PMA_ISO_XCVR_CTRL_13	R/W	0h	Drives tx_lfps_en PMA input for the associated lane when in PMA isolation mode.
28	PHY_PMA_ISO_XCVR_CTRL_12	R/W	0h	Drives tx_elec_idle PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
27	PHY_PMA_ISO_XCVR_CTRL_11	R	0h	Current value of tx_rcv_detected PMA output for the associated lane. (Not re-synchronized to apb_pclk)
26	PHY_PMA_ISO_XCVR_CTRL_10	R	0h	Current value of tx_rcv_detect_done PMA output for the associated lane.
25	PHY_PMA_ISO_XCVR_CTRL_9	R/W	0h	Drives tx_rcv_detect_en PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.

Table 12-970. PHY_PMA_ISO_XCVR_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	PHY_PMA_ISO_XCVR_CTRL_8	R/W	0h	Drives xcvr_link_reset_n PMA input for the associated lane when in PMA isolation mode.
23	PHY_PMA_ISO_XCVR_CTRL_7	R/W	0h	Drives xcvr_pll_clk_en PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
22	PHY_PMA_ISO_XCVR_CTRL_6	R	0h	Reserved
21	PHY_PMA_ISO_XCVR_CTRL_5	R/W	0h	Drives xcvr_lane_suspend PMA input for the associated lane when in PMA isolation mode.
20	PHY_PMA_ISO_XCVR_CTRL_4	R	0h	Current value of rx_lfps_detect PMA output for the associated lane.
19	PHY_PMA_ISO_XCVR_CTRL_3	R	0h	Current value of rx_signal_detect PMA output for the associated lane.
18	PHY_PMA_ISO_XCVR_CTRL_2	R	0h	Reserved
17	PHY_PMA_ISO_XCVR_CTRL_1	R/W	0h	Drives rx_termination PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
16	PHY_PMA_ISO_XCVR_CTRL_0	R	0h	Reserved
15-8	PHY_PMA_PI_POS_15_8	R	0h	Current value of rx_pi_val PMA output for the associated lane.
7-0	PHY_PMA_PI_POS_7_0	R	0h	Current value of rx_eye_plot_pi_val PMA output for the associated lane.

Table 12-971. Register Call Summary for PHY_PMA_ISO_XCVR_CTRL_j

10-G SerDes Registers

- [PHY_PMA_ISO_XCVR_CTRL_j Register \(Offset = F004h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.324 PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j Register (Offset = F008h + formula) [reset = 0h]

PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j is shown in Figure 12-324 and described in Table 12-973.

Return to [Summary Table](#).

PMA transmitter local preset coefficient low isolation register

Offset = F008h + (j * 200h); where j = 0h to 3h

Table 12-972. PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j Instances

Instance	Physical Address
SERDES_10G0	0505 F008h + formula

Figure 12-324. PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_TX_LPC_HI_15	PHY_PMA_ISO_TX_LPC_HI_14_13	PHY_PMA_ISO_TX_LPC_HI_12	PHY_PMA_ISO_TX_LPC_HI_11_8				
R-0h	R-0h	R/W-0h	R/W-0h				
23	22	21	20	19	18	17	16
PHY_PMA_ISO_TX_LPC_HI_7_6	PHY_PMA_ISO_TX_LPC_HI_5_0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
PHY_PMA_ISO_TX_LPC_LO_15_14	PHY_PMA_ISO_TX_LPC_LO_13_8						
R-0h	R-0h						
7	6	5	4	3	2	1	0
PHY_PMA_ISO_TX_LPC_LO_7_6	PHY_PMA_ISO_TX_LPC_LO_5_0						
R-0h	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-973. PHY_PMA_ISO_TX_LPC_HI_PHY_PMA_ISO_TX_LPC_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PMA_ISO_TX_LPC_HI_15	R	0h	Current value of tx_local_preset_coef_valid PMA output for the associated lane.
30-29	PHY_PMA_ISO_TX_LPC_HI_14_13	R	0h	Reserved
28	PHY_PMA_ISO_TX_LPC_HI_12	R/W	0h	Drives tx_get_local_preset_coef PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
27-24	PHY_PMA_ISO_TX_LPC_HI_11_8	R/W	0h	Drives tx_local_preset_index PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
23-22	PHY_PMA_ISO_TX_LPC_HI_7_6	R	0h	Reserved

**Table 12-973. PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX_LPC_LO_j Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
21-16	PHY_PMA_ISO_TX_LPC_HI_5_0	R	0h	Value of tx_local_tx_preset_coef[17:12] PMA output for the associated lane captured upon assertion of tx_local_preset_coef_valid for the associated lane. Cleared upon read.
15-14	PHY_PMA_ISO_TX_LPC_LO_15_14	R	0h	Reserved
13-8	PHY_PMA_ISO_TX_LPC_LO_13_8	R	0h	Value of tx_local_tx_preset_coef[11:6] PMA output for the associated lane captured upon assertion of tx_local_preset_coef_valid for the associated lane. Cleared upon read.
7-6	PHY_PMA_ISO_TX_LPC_LO_7_6	R	0h	Reserved
5-0	PHY_PMA_ISO_TX_LPC_LO_5_0	R	0h	Value of tx_local_tx_preset_coef[5:0] PMA output for the associated lane captured upon assertion of tx_local_preset_coef_valid for the associated lane. Cleared upon read.

Table 12-974. Register Call Summary for PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX_LPC_LO_j

10-G SerDes Registers

- [PHY_PMA_ISO_TX_LPC_HI__PHY_PMA_ISO_TX_LPC_LO_j Register \(Offset = F008h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.325 PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Register (Offset = F00Ch + formula) [reset = 0h]

PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j is shown in Figure 12-325 and described in Table 12-976.

Return to [Summary Table](#).

PMA Tx de-emphasis low isolation register

Offset = F00Ch + (j * 200h); where j = 0h to 3h

Table 12-975. PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Instances

Instance	Physical Address
SERDES_10G0	0505 F00Ch + formula

Figure 12-325. PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_TX_DMPH_HI_15_6							
R-0h							
23	22	21	20	19	18	17	16
PHY_PMA_ISO_TX_DMPH_HI_15_6		PHY_PMA_ISO_TX_DMPH_HI_5_0					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
PHY_PMA_ISO_TX_DMPH_LO_15_14		PHY_PMA_ISO_TX_DMPH_LO_13_8					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
PHY_PMA_ISO_TX_DMPH_LO_7_6		PHY_PMA_ISO_TX_DMPH_LO_5_0					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-976. PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	PHY_PMA_ISO_TX_DMPH_HI_15_6	R	0h	Reserved
21-16	PHY_PMA_ISO_TX_DMPH_HI_5_0	R/W	0h	Drives tx_deemphasis [17:12] PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
15-14	PHY_PMA_ISO_TX_DMPH_LO_15_14	R	0h	Reserved
13-8	PHY_PMA_ISO_TX_DMPH_LO_13_8	R/W	0h	Drives tx_deemphasis [11:6] PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
7-6	PHY_PMA_ISO_TX_DMPH_LO_7_6	R	0h	Reserved
5-0	PHY_PMA_ISO_TX_DMPH_LO_5_0	R/W	0h	Drives tx_deemphasis [5:0] PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.

Table 12-977. Register Call Summary for PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_PMA_ISO_TX_DMPH_HI__PHY_PMA_ISO_TX_DMPH_LO_j Register \(Offset = F00Ch + formula\) \[reset = 0h\]: \[0\]](#)

12.326 PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Register (Offset = F010h + formula) [reset = 2E10h]

PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j is shown in Figure 12-326 and described in Table 12-979.

Return to [Summary Table](#).

PMA Tx FS/LF isolation register

Offset = F010h + (j * 200h); where j = 0h to 3h

Table 12-978. PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Instances

Instance	Physical Address
SERDES_10G0	0505 F010h + formula

Figure 12-326. PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_TX_MGN_15_9							PHY_PMA_ISO_TX_MGN_8
R-0h							R/W-0h
23	22	21	20	19	18	17	16
PHY_PMA_ISO_TX_MGN_7_3					PHY_PMA_ISO_TX_MGN_2_0		
R-0h					R/W-0h		
15	14	13	12	11	10	9	8
PHY_PMA_ISO_TX_FSLF_15_14		PHY_PMA_ISO_TX_FSLF_13_8					
R-0h		R-2Eh					
7	6	5	4	3	2	1	0
PHY_PMA_ISO_TX_FSLF_7_6		PHY_PMA_ISO_TX_FSLF_5_0					
R-0h		R-10h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-979. PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	PHY_PMA_ISO_TX_MGN_15_9	R	0h	Reserved
24	PHY_PMA_ISO_TX_MGN_8	R/W	0h	Drives tx_low_power_swing_en PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
23-19	PHY_PMA_ISO_TX_MGN_7_3	R	0h	Reserved
18-16	PHY_PMA_ISO_TX_MGN_2_0	R/W	0h	Drives tx_vmargin PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
15-14	PHY_PMA_ISO_TX_FSLF_15_14	R	0h	Reserved
13-8	PHY_PMA_ISO_TX_FSLF_13_8	R	2Eh	Current value of tx_local_fs PMA output for the associated lane. (Not re-synchronized to apb_pclk)
7-6	PHY_PMA_ISO_TX_FSLF_7_6	R	0h	Reserved
5-0	PHY_PMA_ISO_TX_FSLF_5_0	R	10h	Current value of tx_local_if PMA output for the associated lane. (Not re-synchronized to apb_pclk)

Table 12-980. Register Call Summary for PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j

10-G SerDes Registers

- [PHY_PMA_ISO_TX_MGN__PHY_PMA_ISO_TX_FSLF_j](#) Register (Offset = F010h + formula) [reset = 2E10h]: [0]
- 10-G SerDes Registers: [0]

12.327 PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register (Offset = F014h + formula) [reset = C000h]

PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j is shown in Figure 12-327 and described in Table 12-982.

Return to [Summary Table](#).

PMA Isolation mode control register

Offset = F014h + (j * 200h); where j = 0h to 3h

Table 12-981. PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Instances

Instance	Physical Address
SERDES_10G0	0505 F014h + formula

Figure 12-327. PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_PWRST_CTRL_15	PHY_PMA_ISO_PWRST_CTRL_14	PHY_PMA_ISO_PWRST_CTRL_13_8					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
PHY_PMA_ISO_PWRST_CTRL_7_6	PHY_PMA_ISO_PWRST_CTRL_5_0						
R-0h	R/W-0h						
15	14	13	12	11	10	9	8
PHY_PMA_ISO_LINK_MODE_15	PHY_PMA_ISO_LINK_MODE_14	PHY_PMA_ISO_LINK_MODE_13_6					
R/W-1h	R/W-1h	R-0h					
7	6	5	4	3	2	1	0
PHY_PMA_ISO_LINK_MODE_1_3_6	PHY_PMA_ISO_LINK_MODE_5_4	PHY_PMA_ISO_LINK_MODE_3	PHY_PMA_ISO_LINK_MODE_2_0				
R-0h	R/W-0h	R-0h	R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-982. PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_PMA_ISO_PWRST_CTRL_15	R/W	0h	rx_sig_det_en_ext_in_{nnnn} PMA input when in PMA isolation mode. (Used for PCIe)
30	PHY_PMA_ISO_PWRST_CTRL_14	R/W	0h	tx_cmn_mode_en_ext_in_{nnnn} PMA input when in PMA isolation mode. (Used for PCIe)
29-24	PHY_PMA_ISO_PWRST_CTRL_13_8	R	0h	Current value of xcvr_power_state_ack_in_{nnnn} PMA output.
23-22	PHY_PMA_ISO_PWRST_CTRL_7_6	R	0h	Reserved
21-16	PHY_PMA_ISO_PWRST_CTRL_5_0	R/W	0h	Drives xcvr_power_state_req_in_{nnnn} PMA input when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode..

Table 12-982. PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	PHY_PMA_ISO_LINK_MODE_15	R/W	1h	tx_reset_n_In_{nnnn} PMA input when in PMA isolation mode.
14	PHY_PMA_ISO_LINK_MODE_14	R/W	1h	rx_reset_n_In_{nnnn} PMA input when in PMA isolation mode.
13-6	PHY_PMA_ISO_LINK_MODE_13_6	R	0h	Reserved
5-4	PHY_PMA_ISO_LINK_MODE_5_4	R/W	0h	Drives xcvr_standard_mode_In_{nnnn} PMA input when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
3	PHY_PMA_ISO_LINK_MODE_3	R	0h	Reserved
2-0	PHY_PMA_ISO_LINK_MODE_2_0	R/W	0h	Drives xcvr_data_width_In_{nnnn} PMA input when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.

Table 12-983. Register Call Summary for PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j

10-G SerDes Registers

- [PHY_PMA_ISO_PWRST_CTRL__PHY_PMA_ISO_LINK_MODE_j Register \(Offset = F014h + formula\) \[reset = C000h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

12.328 PHY_PMA_ISO_RX_EQ_CTRL_j Register (Offset = F018h + formula) [reset = X]

PHY_PMA_ISO_RX_EQ_CTRL_j is shown in Figure 12-328 and described in Table 12-985.

Return to [Summary Table](#).

PMA RX equalization control isolation register

Offset = F018h + (j * 200h); where j = 0h to 3h

Table 12-984. PHY_PMA_ISO_RX_EQ_CTRL_j Instances

Instance	Physical Address
SERDES_10G0	0505 F018h + formula

Figure 12-328. PHY_PMA_ISO_RX_EQ_CTRL_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_RX_EQ_CTRL_15_14		PHY_PMA_ISO_RX_EQ_CTRL_13	PHY_PMA_ISO_RX_EQ_CTRL_12	PHY_PMA_ISO_RX_EQ_CTRL_11_10		PHY_PMA_ISO_RX_EQ_CTRL_9_4	
R-0h		R/W-0h	R/W-0h	R-0h		R-0h	
23	22	21	20	19	18	17	16
		PHY_PMA_ISO_RX_EQ_CTRL_9_4		PHY_PMA_ISO_RX_EQ_CTRL_3	PHY_PMA_ISO_RX_EQ_CTRL_2	PHY_PMA_ISO_RX_EQ_CTRL_1	PHY_PMA_ISO_RX_EQ_CTRL_0
		R-0h		R-0h	R/W-0h	R-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-985. PHY_PMA_ISO_RX_EQ_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	PHY_PMA_ISO_RX_EQ_CTRL_15_14	R	0h	Reserved
29	PHY_PMA_ISO_RX_EQ_CTRL_13	R/W	0h	Drives rx_eq_training_data_valid PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
28	PHY_PMA_ISO_RX_EQ_CTRL_12	R/W	0h	Drives rx_eq_training PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
27-26	PHY_PMA_ISO_RX_EQ_CTRL_11_10	R	0h	Reserved
25-20	PHY_PMA_ISO_RX_EQ_CTRL_9_4	R	0h	The value of rx_link_eval_fb_dir_change PMA output for the associated lane upon assertion of rx_eq_eval_status to PMA. Cleared upon read.
19	PHY_PMA_ISO_RX_EQ_CTRL_3	R	0h	The value of rx_eq_eval_complete PMA output for the associated lane upon assertion of rx_eq_eval_status. Cleared upon read.
18	PHY_PMA_ISO_RX_EQ_CTRL_2	R/W	0h	Drives rx_invalid_request PMA input for the associated lane when in PMA isolation mode.

Table 12-985. PHY_PMA_ISO_RX_EQ_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	PHY_PMA_ISO_RX_EQ_CTRL_1	R	0h	Current value of rx_eq_eval_status PMA output for the associated lane.
16	PHY_PMA_ISO_RX_EQ_CTRL_0	R/W	0h	Drives rx_eq_eval PMA input for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
15-0	RESERVED	R/W	X	

Table 12-986. Register Call Summary for PHY_PMA_ISO_RX_EQ_CTRL_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_PMA_ISO_RX_EQ_CTRL_j Register \(Offset = F018h + formula\) \[reset = X\]: \[0\]](#)

12.329 PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Register (Offset = F01Ch + formula) [reset = 0h]

PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j is shown in Figure 12-329 and described in Table 12-988.

Return to [Summary Table](#).

PMA low data isolation register

Offset = F01Ch + (j * 200h); where j = 0h to 3h

Table 12-987. PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Instances

Instance	Physical Address
SERDES_10G0	0505 F01Ch + formula

Figure 12-329. PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Register

31	30	29	28	27	26	25	24
PHY_PMA_ISO_DATA_HI_15_4							
R-0h							
23	22	21	20	19	18	17	16
PHY_PMA_ISO_DATA_HI_15_4				PHY_PMA_ISO_DATA_HI_3_0			
R-0h				R-0h			
15	14	13	12	11	10	9	8
PHY_PMA_ISO_DATA_LO_15_0							
R-0h							
7	6	5	4	3	2	1	0
PHY_PMA_ISO_DATA_LO_15_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 12-988. PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PHY_PMA_ISO_DATA_HI_15_4	R	0h	Reserved
19-16	PHY_PMA_ISO_DATA_HI_3_0	R	0h	Current value of rx_rd[19:16] PMA output for the current lane. (Not re-synchronized to apb_pclk). This register can be written and the value will drive tx_td[19:16] for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.
15-0	PHY_PMA_ISO_DATA_LO_15_0	R	0h	Current value of rx_rd[15:0] PMA output for the current lane. (Not re-synchronized to apb_pclk). This register can be written and the value will drive tx_td[15:0] for the associated lane when in PMA isolation mode or PHY isolation mode and lane is configured for Raw SerDes mode.

Table 12-989. Register Call Summary for PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j

10-G SerDes Registers

- [10-G SerDes Registers: \[0\]](#)
- [PHY_PMA_ISO_DATA_HI__PHY_PMA_ISO_DATA_LO_j Register \(Offset = F01Ch + formula\) \[reset = 0h\]: \[0\]](#)

12.330 PHY_PMA_PSM_STATE_HI__PHY_PMA_PSM_STATE_LO_j Register (Offset = F020h + formula) [reset = 0h]

PHY_PMA_PSM_STATE_HI__PHY_PMA_PSM_STATE_LO_j is shown in Figure 12-330 and described in Table 12-991.

Return to [Summary Table](#).

PMA PSM current state lower register

Offset = F020h + (j * 200h); where j = 0h to 3h

Table 12-990. PHY_PMA_PSM_STATE_HI__PHY_PMA_PSM_STATE_LO_j Instances

Instance	Physical Address
SERDES_10G0	0505 F020h + formula

Figure 12-330. PHY_PMA_PSM_STATE_HI__PHY_PMA_PSM_STATE_LO_j Register

31	30	29	28	27	26	25	24
PHY_PMA_PSM_STATE_HI_15_13			PHY_PMA_PSM_STATE_HI_12	PHY_PMA_PSM_STATE_HI_11_10		PHY_PMA_PSM_STATE_HI_9_0	
R-0h			R-0h	R-0h		R-0h	
23	22	21	20	19	18	17	16
PHY_PMA_PSM_STATE_HI_9_0							
R-0h							
15	14	13	12	11	10	9	8
PHY_PMA_PSM_STATE_LO_15_0							
R-0h							
7	6	5	4	3	2	1	0
PHY_PMA_PSM_STATE_LO_15_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 12-991. PHY_PMA_PSM_STATE_HI__PHY_PMA_PSM_STATE_LO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	PHY_PMA_PSM_STATE_HI_15_13	R	0h	Reserved
28	PHY_PMA_PSM_STATE_HI_12	R	0h	Current value of xcvr_psm_ready for the associated lane.
27-26	PHY_PMA_PSM_STATE_HI_11_10	R	0h	Reserved
25-16	PHY_PMA_PSM_STATE_HI_9_0	R	0h	Current value of xcvr_psm_state[25:16] for the associated lane - PMA power state machine state. (Not re-synchronized to apb_pclk)
15-0	PHY_PMA_PSM_STATE_LO_15_0	R	0h	Current value of xcvr_psm_state[15:0] for the associated lane - PMA power state machine state. (Not re-synchronized to apb_pclk)

Table 12-992. Register Call Summary for PHY_PMA_PSM_STATE_HI__PHY_PMA_PSM_STATE_LO_j

10-G SerDes Registers

- [PHY_PMA_PSM_STATE_HI__PHY_PMA_PSM_STATE_LO_j Register \(Offset = F020h + formula\) \[reset = 0h\]: \[0\]](#)
- [10-G SerDes Registers: \[0\]](#)

13 FSS Registers

Table 13-2 lists the memory-mapped registers for the FSS (MCU_FSS0). All register offset addresses not listed in Table 13-2 should be considered as reserved locations and the register contents should not be modified.

Table 13-1. FSS Instances

Instance	Base Address
MCU_FSS0_CFG	4700 0000h

Table 13-2. FSS Registers

Offset	Acronym	Register Name	MCU_FSS0_CFG Physical Address
0h	MCU_FSS0_REVISION	Revision Register	4700 0000h
4h	MCU_FSS0_SYSCONFIG	Configuration Register	4700 0004h
10h	MCU_FSS0_EOI	End Of Interrupt (EOI) MISC Register	4700 0010h
14h	MCU_FSS0_STATUS_RAW	Interrupt Source Set Register	4700 0014h
18h	MCU_FSS0_STATUS	Interrupt Source Clear Register	4700 0018h
1Ch	MCU_FSS0_ENABLE_SET	Interrupt Source Enable Register	4700 001Ch
20h	MCU_FSS0_ENABLE_CLR	Interrupt Source Disable Register	4700 0020h
30h + formula	MCU_FSS0_ECC_RGSTRT_j	ECC Region Start Register	4700 0030h to 4700 0054h
34h + formula	MCU_FSS0_ECC_RGSIZ_j	ECC Region Size Register	4700 0034h to 4700 0058h
70h	MCU_FSS0_ECC_BLOCK_ADR	ECC Error Block Address Register	4700 0070h
74h	MCU_FSS0_ECC_TYPE	ECC Error Type Register	4700 0074h
78h	MCU_FSS0_WRT_TYPE	Error Write Type Register	4700 0078h

13.1 MCU_FSS0_REVISION Register (Offset = 0h) [reset = 68506900h]

MCU_FSS0_REVISION is shown in [Figure 13-1](#) and described in [Table 13-4](#).

Return to [Summary Table](#).

Revision Register

Used by software to track features, bugs, and compatibility.

Table 13-3. MCU_FSS0_REVISION Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0000h

Figure 13-1. MCU_FSS0_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-6850h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM				REVMIN			
R-Dh				R-1h				R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 13-4. MCU_FSS0_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6850h	Module ID
15-11	REVRTL	R	Dh	RTL Revision
10-8	REVMAJ	R	1h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	0h	Minor Revision

13.2 MCU_FSS0_SYSCONFIG Register (Offset = 4h) [reset = 0h]

MCU_FSS0_SYSCONFIG is shown in [Figure 13-2](#) and described in [Table 13-6](#).

Return to [Summary Table](#).

Configuration Register

Controls various parameters of the controller state.

Table 13-5. MCU_FSS0_SYSCONFIG Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0004h

Figure 13-2. MCU_FSS0_SYSCONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				ECC_DISABLE_ADR	FSS_AES_EN_IPCFG	HB_OSPI	ECC_EN
R-0h				R/W-0h	R-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 13-6. MCU_FSS0_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	ECC_DISABLE_ADR	R/W	0h	Block Address ECC Calculation 0h = Block address within ECC calculation 1h = Block address not within ECC calculation
2	FSS_AES_EN_IPCFG	R	0h	Security Enable 0h = Disable security 1h = Enable security
1	HB_OSPI	R/W	0h	Path Select 0h = Select OSPI path 1h = Select HyperBus interface path
0	ECC_EN	R/W	0h	ECC Enable 0h = ECC disabled 1h = ECC enabled

13.3 MCU_FSS0_EOI Register (Offset = 10h) [reset = 0h]

MCU_FSS0_EOI is shown in [Figure 13-3](#) and described in [Table 13-8](#).

Return to [Summary Table](#).

End Of Interrupt (EOI) MISC Register

The End Of Interrupt (EOI) MISC Register allows the CPU to acknowledge completion of an interrupt by writing to it for misc interrupt sources. An EOI write signal will be generated and another interrupt will be triggered if interrupt sources remain. This register will be reset one cycle after it has been written to.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 13-7. MCU_FSS0_EOI Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0010h

Figure 13-3. MCU_FSS0_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_VECTOR
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 13-8. MCU_FSS0_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_VECTOR	R/W	0h	EOI Vector Write with bit position of targeted interrupt (example: external FSS ECC is bit 0). Upon write, level interrupt will clear and if un-serviced will issue another pulse interrupt.

13.4 MCU_FSS0_STATUS_RAW Register (Offset = 14h) [reset = 0h]

MCU_FSS0_STATUS_RAW is shown in [Figure 13-4](#) and described in [Table 13-10](#).

Return to [Summary Table](#).

Interrupt Source Set Register

The Interrupt Source Set Register allows the interrupt sources to be manually set when writing 1h to a specific bit.

Write 0h = No action

Write 1h = Set event

Read 0h = No event pending

Read 1h = Event pending

Table 13-9. MCU_FSS0_STATUS_RAW Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0014h

Figure 13-4. MCU_FSS0_STATUS_RAW Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_N ONALIGN	ECC_ERROR_ 2BIT	ECC_ERROR_ 1BIT
R-0h					R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 13-10. MCU_FSS0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1S	0h	ECC Write Non Aligned Write is not aligned to 32-byte boundary or not a multiple of 32-byte.
1	ECC_ERROR_2BIT	R/W1S	0h	ECC Error on 2 Bits Not correctable.
0	ECC_ERROR_1BIT	R/W1S	0h	ECC Error on 1 Bit Correctable.

13.5 MCU_FSS0_STATUS Register (Offset = 18h) [reset = 0h]

MCU_FSS0_STATUS is shown in [Figure 13-5](#) and described in [Table 13-12](#).

Return to [Summary Table](#).

Interrupt Source Clear Register

The Interrupt Source Clear Register allows the interrupt sources to be manually cleared when writing 1h to a specific bit.

Write 0h = No action

Write 1h = Clear event

Read 0h = No event pending

Read 1h = Event pending

Table 13-11. MCU_FSS0_STATUS Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0018h

Figure 13-5. MCU_FSS0_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_N ONALIGN	ECC_ERROR_ 2BIT	ECC_ERROR_ 1BIT
R-0h					R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-12. MCU_FSS0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1C	0h	ECC Write Non Aligned Write is not aligned to 32-byte boundary or not a multiple of 32-byte.
1	ECC_ERROR_2BIT	R/W1C	0h	ECC Error on 2 Bits Not correctable.
0	ECC_ERROR_1BIT	R/W1C	0h	ECC Error on 1 Bit Correctable.

13.6 MCU_FSS0_ENABLE_SET Register (Offset = 1Ch) [reset = 0h]

MCU_FSS0_ENABLE_SET is shown in [Figure 13-6](#) and described in [Table 13-14](#).

Return to [Summary Table](#).

Interrupt Source Enable Register

The Interrupt Source Enable Register allows the interrupt sources to be manually enabled when writing 1h to a specific bit.

Write 0h = No action

Write 1h = Enable event

Read 0h = Event is disabled

Read 1h = Event is enabled

Table 13-13. MCU_FSS0_ENABLE_SET Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 001Ch

Figure 13-6. MCU_FSS0_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_N ONALIGN	ECC_ERROR_ 2BIT	ECC_ERROR_ 1BIT
R-0h					R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 13-14. MCU_FSS0_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1S	0h	ECC Write Non Aligned Write is not aligned to 32-byte boundary or not a multiple of 32-byte.
1	ECC_ERROR_2BIT	R/W1S	0h	ECC Error on 2 Bits Not correctable.
0	ECC_ERROR_1BIT	R/W1S	0h	ECC Error on 1 Bit Correctable.

13.7 MCU_FSS0_ENABLE_CLR Register (Offset = 20h) [reset = 0h]

MCU_FSS0_ENABLE_CLR is shown in [Figure 13-7](#) and described in [Table 13-16](#).

Return to [Summary Table](#).

Interrupt Source Disable Register

The Interrupt Source Disable Register allows the interrupt sources to be manually disabled when writing 1h to a specific bit.

Write 0h = No action

Write 1h = Disable event

Read 0h = Event is disabled

Read 1h = Event is enabled

Table 13-15. MCU_FSS0_ENABLE_CLR Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0020h

Figure 13-7. MCU_FSS0_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_WRITE_NONALIGN	ECC_ERROR_2BIT	ECC_ERROR_1BIT
R-0h					R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-16. MCU_FSS0_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	ECC_WRITE_NONALIGN	R/W1C	0h	ECC Write Non Aligned Write is not aligned to 32-byte boundary or not a multiple of 32-byte.
1	ECC_ERROR_2BIT	R/W1C	0h	ECC Error on 2 Bits Not correctable.
0	ECC_ERROR_1BIT	R/W1C	0h	ECC Error on 1 Bit Correctable.

13.8 MCU_FSS0_ECC_RGSTRT_j Register (Offset = 30h + formula) [reset = 0h]

MCU_FSS0_ECC_RGSTRT_j is shown in [Figure 13-8](#) and described in [Table 13-18](#).

Return to [Summary Table](#).

ECC Region Start Register

The ECC Region Start Register defines the start of the ECC region in 4 KB steps.

Offset = 30h + (j × 8h); where j = 0h to 3h

MCU_FSS0_ECC_RGSTRT_0: 4700 0030h

MCU_FSS0_ECC_RGSTRT_1: 4700 0038h

MCU_FSS0_ECC_RGSTRT_2: 4700 0046h

MCU_FSS0_ECC_RGSTRT_3: 4700 0054h

Table 13-17. MCU_FSS0_ECC_RGSTRT_j Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0030h to 4700 0054h

Figure 13-8. MCU_FSS0_ECC_RGSTRT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												R_START																			
R-0h												R/W-0h																			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 13-18. MCU_FSS0_ECC_RGSTRT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-0	R_START	R/W	0h	<p>ECC Region Start Address</p> <p>This bit field defines the start of the ECC region in 4 KB steps.</p> <p>Address start = {start[19:0], 000h}</p> <p>0h = start is 0000 0000h</p> <p>1h = start is 0000 1000h</p> <p>Ah = start is 0000 A000h</p> <p>Note: the offset + size should be <= 4 GB, wrap around is not supported.</p>

13.9 MCU_FSS0_ECC_RGSIZ_j Register (Offset = 34h + formula) [reset = 0h]

MCU_FSS0_ECC_RGSIZ_j is shown in [Figure 13-9](#) and described in [Table 13-20](#).

Return to [Summary Table](#).

ECC Region Size Register

The ECC Region Size Register defines the size of the ECC region in 4 KB steps.

Offset = 34h + (j × 8h); where j = 0h to 3h

MCU_FSS0_ECC_RGSIZ_0: 4700 0034h

MCU_FSS0_ECC_RGSIZ_1: 4700 0042h

MCU_FSS0_ECC_RGSIZ_2: 4700 0050h

MCU_FSS0_ECC_RGSIZ_3: 4700 0058h

Table 13-19. MCU_FSS0_ECC_RGSIZ_j Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0034h to 4700 0058h

Figure 13-9. MCU_FSS0_ECC_RGSIZ_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												R_SIZE																			
R-0h												R/W-0h																			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 13-20. MCU_FSS0_ECC_RGSIZ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-0	R_SIZE	R/W	0h	<p>ECC Region Size</p> <p>This bit field defines the size of the ECC region in 4 KB steps.</p> <p>0h = size is zero and disabled</p> <p>1h = size is 4 KB</p> <p>Ah = size is 40 KB</p> <p>F FFFFh = size is 4 GB</p> <p>Note: offset + size should be <= 4 GB, wrap around is not supported.</p>

13.10 MCU_FSS0_ECC_BLOCK_ADR Register (Offset = 70h) [reset = 0h]

MCU_FSS0_ECC_BLOCK_ADR is shown in [Figure 13-10](#) and described in [Table 13-22](#).

ECC Error Block Address Register

Return to [Summary Table](#).

The ECC Error Block Address Register holds the current top of stack ECC error block address, this is only valid when the MCU_FSS0_ECC_TYPE[31] ECC_ERR_VALID bit is set.

**Table 13-21. MCU_FSS0_ECC_BLOCK_ADR
Instances**

Instance	Physical Address
MCU_FSS0_CFG	4700 0070h

Figure 13-10. MCU_FSS0_ECC_BLOCK_ADR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ERROR_BLOCK_ADDR																												RESERVED			
R-0h																												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 13-22. MCU_FSS0_ECC_BLOCK_ADR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	ECC_ERROR_BLOCK_A DDR	R	0h	ECC Error Block Address ECC 32-byte aligned block address
4-0	RESERVED	R	0h	Reserved

13.11 MCU_FSS0_ECC_TYPE Register (Offset = 74h) [reset = 0h]

MCU_FSS0_ECC_TYPE is shown in [Figure 13-11](#) and described in [Table 13-24](#).

ECC Error Type Register

Return to [Summary Table](#).

The ECC Error Type Register holds the current top of stack ECC error info, this is only valid when the MCU_FSS0_ECC_TYPE[31] ECC_ERR_VALID bit is set.

Table 13-23. MCU_FSS0_ECC_TYPE Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0074h

Figure 13-11. MCU_FSS0_ECC_TYPE Register

31	30	29	28	27	26	25	24
ECC_ERR_VAL ID	RESERVED						
R/W1C-0h				R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		ECC_ERR_AD R	ECC_ERR_MA C	ECC_ERR_DA 1	ECC_ERR_DA 0	ECC_ERR_DE D	ECC_ERR_SE C
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-24. MCU_FSS0_ECC_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ECC_ERR_VALID	R/W1C	0h	ECC Error Valid When set indicates that there is valid ECC error information available. Writing a 1h to this register will pop the top of the stack.
30-6	RESERVED	R	0h	Reserved
5	ECC_ERR_ADR	R	0h	ECC Error Address When set indicates that there was a single error detected within the address field.
4	ECC_ERR_MAC	R	0h	ECC Error MAC When set indicates that there was a single error detected within the MAC field.
3	ECC_ERR_DA1	R	0h	ECC Error High Data Word When set indicates that there was a single error detected within the High Data word.
2	ECC_ERR_DA0	R	0h	ECC Error Low Data Word When set indicates that there was a single error detected within the Low Data word.
1	ECC_ERR_DED	R	0h	ECC Error (DED) When set indicates that there was a double error detected for the block.

Table 13-24. MCU_FSS0_ECC_TYPE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ECC_ERR_SEC	R	0h	ECC Error (SEC) When set indicates that there was a single error detected for the block.

13.12 MCU_FSS0_WRT_TYPE Register (Offset = 78h) [reset = 0h]

MCU_FSS0_WRT_TYPE is shown in [Figure 13-12](#) and described in [Table 13-26](#).

Return to [Summary Table](#).

Error Write Type Register

The Error Write Type Register holds the current top of stack write error info, this is only valid when the MCU_FSS0_WRT_TYPE[31] WRT_ERR_VALID bit is set.

Table 13-25. MCU_FSS0_WRT_TYPE Instances

Instance	Physical Address
MCU_FSS0_CFG	4700 0078h

Figure 13-12. MCU_FSS0_WRT_TYPE Register

31	30	29	28	27	26	25	24
WRT_ERR_VALID	RESERVED						
R/W1C-0h				R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRT_ERR_BEN	WRT_ERR_ADR	WRT_ERR_ROUTEID			
R-0h		R-0h	R-0h	R-0h			
7	6	5	4	3	2	1	0
WRT_ERR_ROUTEID							
R-0h							

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-26. MCU_FSS0_WRT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRT_ERR_VALID	R/W1C	0h	Write Error Valid When set indicates that there is valid write error information available. Writing a 1h to this register will pop the top of the stack.
30-14	RESERVED	R	0h	Reserved
13	WRT_ERR_BEN	R	0h	Write Error Non-Contiguous Byte Enables When set indicates that there was a write error due to a non-contiguous byte enables.
12	WRT_ERR_ADR	R	0h	Write Error Address When set indicates that there was a write error due to a non-aligned address.
11-0	WRT_ERR_ROUTEID	R	0h	Write Error Route ID Indicates the Route ID for the Master that caused the write error.

14 OSPI Registers

This section describes OSPI Global Control registers, OSPI Configuration registers, and OSPI_ECC_AGGR registers.

14.1 OSPI Global Control Registers

Table 14-2 lists the memory-mapped registers for the OSPI Global Control Registers. All register offset addresses not listed in Table 14-2 should be considered as reserved locations and the register contents should not be modified.

The Global Control Registers region is accessed by setting the Region Select signal to 0 during the access. The address map for this region is as follows:

Table 14-1. OSPI Global Control Instances

Instance	Base Address
MCU_FSS0_OSPI0_SS_CFG	4704 4000h

Table 14-2. OSPI Global Control Registers

Offset	Acronym	Register Name	MCU_FSS0_OSPI0_SS_CFG Physical Address
0h	OSPI_PID	Revision register	4704 4000h
4h	OSPI_CTRL	Control register	4704 4004h
8h	OSPI_STAT	Status register	4704 4008h
20h	OSPI_EOI	End of interrupt	4704 4020h

14.2 OSPI_PID Register (Offset = 0h) [reset = X]

OSPI_PID is shown in [Figure 14-1](#) and described in [Table 14-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 14-3. OSPI_PID Instances

Instance	Physical Address
MCU_FSS0_OSPI0_SS_CFG	4704 4000h

Figure 14-1. OSPI_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-874h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-1h					R-0h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 14-4. OSPI_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	OSPI_PID register scheme
29-28	BU	R	2h	Business Unit: 10 = Processors
27-16	MODULE_ID	R	874h	Module ID
15-11	RTL	R		RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

14.3 OSPI_CTRL Register (Offset = 4h) [reset = 0h]

OSPI_CTRL is shown in [Figure 14-2](#) and described in [Table 14-6](#).

Return to [Summary Table](#).

The Control Register contains general control bits for the OSPI.

Table 14-5. OSPI_CTRL Instances

Instance	Physical Address
FSS0_OSPI0_SS_CFG	4004h

Figure 14-2. OSPI_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PIPELINE_MODE_FLUSH	RESERVED		
R-0h				R/W-0h	R-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-6. OSPI_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PIPELINE_MODE_FLUSH	R/W	0h	1h = Flush Flash Controller FIFO by forcing data interface slave select signal low. 0h = Data interface slave select signal to Controller is 1.
2-0	RESERVED	R	0h	Reserved

14.4 OSPI_STAT Register (Offset = 8h) [reset = 0h]

OSPI_STAT is shown in [Figure 14-3](#) and described in [Table 14-8](#).

Return to [Summary Table](#).

The Status register provide general status bits for the OSPI.

Table 14-7. OSPI_STAT Instances

Instance	Physical Address
FSS0_OSPI0_SS_CFG	4008h

Figure 14-3. OSPI_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						MEM_INIT_DONE	RESERVED
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 14-8. OSPI_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	MEM_INIT_DONE	R	0h	0h = Memory initialization is in progress, 1h = Memory initialization is done.
0	RESERVED	R	0h	Reserved

14.5 OSPI_EOI Register (Offset = 20h) [reset = 0h]

OSPI_EOI is shown in [Figure 14-4](#) and described in [Table 14-10](#).

Return to [Summary Table](#).

End of Interrupt Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Note

Some of the OSPI features described in this section may not be supported on this family of devices. For more information, see *OSPI Not Supported Features*.

Table 14-9. OSPI_EOI Instances

Instance	Physical Address
FSS0_OSPI0_SS_CFG	4020h

Figure 14-4. OSPI_EOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								EOI							
R-0h																								W-0h							

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 14-10. OSPI_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	EOI	W	0h	Write with bit position of targetted interrupt. (that is Ext TS is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt.

14.6 OSPI Module Configuration Registers

Table 14-12 lists the memory-mapped registers for the OSPI Module Configuration registers. All register offset addresses not listed in Table 14-12 should be considered as reserved locations and the register contents should not be modified.

Table 14-11. OSPI Module Configuration Instances

Instance	Base Address
MCU_FSS0_OSPI0_CTRL	4704 0000h

Table 14-12. OSPI Module Configuration Registers

Offset	Acronym	Register Name	MCU_FSS0_OSPI0_CTRL Physical Address
0h	OSPI_CONFIG_REG	OSPI configuration register	4704 0000h
4h	OSPI_DEV_INSTR_RD_CONFIG_REG	Read instruction configuration register	4704 0004h
8h	OSPI_DEV_INSTR_WR_CONFIG_REG	Write instruction configuration register	4704 0008h
Ch	OSPI_DEV_DELAY_REG	OSPI delay register	4704 000Ch
10h	OSPI_RD_DATA_CAPTURE_REG	Read data capture register	4704 0010h
14h	OSPI_DEV_SIZE_CONFIG_REG	Device size configuration register	4704 0014h
18h	OSPI_SRAM_PARTITION_CFG_REG	SRAM partition configuration register	4704 0018h
1Ch	OSPI_IND_AHB_ADDR_TRIGGER_REG	Indirect trigger address register	4704 001Ch
20h	OSPI_DMA_PERIPH_CONFIG_REG	DMA configuration register	4704 0020h
24h	OSPI_REMAP_ADDR_REG	Address remapping register	4704 0024h
28h	OSPI_MODE_BIT_CONFIG_REG	Mode bit configuration register	4704 0028h
2Ch	OSPI_SRAM_FILL_REG	SRAM fill level register	4704 002Ch
30h	OSPI_TX_THRESH_REG	TX threshold register	4704 0030h
34h	OSPI_RX_THRESH_REG	RX threshold register	4704 0034h
38h	OSPI_WRITE_COMPLETION_CTRL_REG	Write completion control register	4704 0038h
3Ch	OSPI_NO_OF_POLLS_BEF_EXP_REG	Polling expiration register	4704 003Ch
40h	OSPI_IRQ_STATUS_REG	Interrupt status register	4704 0040h
44h	OSPI_IRQ_MASK_REG	Interrupt mask register	4704 0044h
50h	OSPI_LOWER_WR_PROT_REG	Lower write protection register	4704 0050h
54h	OSPI_UPPER_WR_PROT_REG	Upper write protection register	4704 0054h
58h	OSPI_WR_PROT_CTRL_REG	Write protection control register	4704 0058h
60h	OSPI_INDIRECT_READ_XFER_CTRL_REG	Indirect read transfer control register	4704 0060h
64h	OSPI_INDIRECT_READ_XFER_WATERMARK_REG	Indirect read transfer watermark register	4704 0064h
68h	OSPI_INDIRECT_READ_XFER_START_REG	Indirect read transfer start address register	4704 0068h
6Ch	OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG	Indirect read transfer number bytes register	4704 006Ch
70h	OSPI_INDIRECT_WRITE_XFER_CTRL_REG	Indirect write transfer control register	4704 0070h
74h	OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG	Indirect write transfer watermark register	4704 0074h
78h	OSPI_INDIRECT_WRITE_XFER_START_REG	Indirect write transfer start address register	4704 0078h
7Ch	OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG	Indirect write transfer number bytes register	4704 007Ch
80h	OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG	Indirect trigger address range register	4704 0080h
8Ch	OSPI_FLASH_COMMAND_CTRL_MEM_REG	Flash command control memory register	4704 008Ch
90h	OSPI_FLASH_CMD_CTRL_REG	Flash command control register	4704 0090h
94h	OSPI_FLASH_CMD_ADDR_REG	Flash command address register	4704 0094h
A0h	OSPI_FLASH_RD_DATA_LOWER_REG	Flash command read data register (lower)	4704 00A0h
A4h	OSPI_FLASH_RD_DATA_UPPER_REG	Flash command read data register (upper)	4704 00A4h
A8h	OSPI_FLASH_WR_DATA_LOWER_REG	Flash command write data register (lower)	4704 00A8h
ACH	OSPI_FLASH_WR_DATA_UPPER_REG	Flash command write data register (upper)	4704 00ACH

Table 14-12. OSPI Module Configuration Registers (continued)

Offset	Acronym	Register Name	MCU_FSS0_OSPI0_CTRL Physical Address
B0h	OSPI_POLLING_FLASH_STATUS_REG	Polling Flash status register	4704 00B0h
B4h	OSPI_PHY_CONFIGURATION_REG	PHY configuration register	4704 00B4h
B8h	OSPI_PHY_MASTER_CONTROL_REG	PHY DLL master control register	4704 00B8h
BCh	OSPI_DLL_OBSERVABLE_LOWER_REG	DLL observable register (lower)	4704 00BCh
C0h	OSPI_DLL_OBSERVABLE_UPPER_REG	DLL observable register (upper)	4704 00C0h
E0h	OSPI_OPCODE_EXT_LOWER_REG	Opcode extension register (lower)	4704 00E0h
E4h	OSPI_OPCODE_EXT_UPPER_REG	Opcode extension register (upper)	4704 00E4h
FCh	OSPI_MODULE_ID_REG	Module ID register	4704 00FCh

14.7 OSPI_CONFIG_REG Register (Offset = 0h) [reset = 80780081h]

OSPI_CONFIG_REG is shown in [Figure 14-5](#) and described in [Table 14-14](#).

Return to [Summary Table](#).

OSPI Configuration Register

This register contains basic configuration fields of the controller.

Table 14-13. OSPI_CONFIG_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0000h

Figure 14-5. OSPI_CONFIG_REG Register

31	30	29	28	27	26	25	24
IDLE_FLD	DUAL_BYTE_OPCODE_ENABLE_FLD	CRC_ENABLE_FLD	CONFIG_RESV2_FLD			PIPELINE_PHY_FLD	ENABLE_DTR_PROTOCOL_FLD
R-1h	R/W-0h	R/W-0h	R-0h			R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ENABLE_AHB_DECODER_FLD	MSTR_BAUD_DIV_FLD			ENTER_XIP_MODE_IMM_FLD	ENTER_XIP_MODE_FLD	ENB_AHB_ADDR_REMAP_FLD	
R/W-0h	R/W-Fh			R/W-0h	R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
ENB_DMA_IF_FLD	WR_PROT_FLASH_FLD	PERIPH_CS_LINES_FLD			PERIPH_SELECT_DEC_FLD	ENB_LEGACY_IP_MODE_FLD	
R/W-0h	R/W-0h	R/W-0h			R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
ENB_DIR_ACCESS_CTLR_FLD	RESET_CFG_FLD	RESET_PIN_FLD	HOLD_PIN_FLD	PHY_MODE_ENABLE_FLD	SEL_CLK_PHASE_FLD	SEL_CLK_POL_FLD	ENB_SPI_FLD
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-14. OSPI_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE_FLD	R	1h	Serial interface and low level SPI pipeline is IDLE. This is a STATUS read-only bit. Note this is a retimed signal, so there will be some inherent delay on the generation of this status signal.
30	DUAL_BYTE_OPCODE_ENABLE_FLD	R/W	0h	Dual-byte Opcode Mode enable bit. This bit is to be set in case the target Flash Device supports dual byte opcode. It is applicable for Octal I/O Mode or Protocol only so should be set back to low if the device is configured to work in another SPI Mode. If enabled, the supplementing bytes are taken from OSPI_OPCODE_EXT_LOWER_REG and from OSPI_OPCODE_EXT_UPPER_REG.
29	CRC_ENABLE_FLD	R/W	0h	CRC enable bit. This bit is to be set in case the target Flash Device supports CRC. It is applicable for Octal DDR Protocol only so should be set back to low if the device is configured to work in another SPI Mode
28-26	CONFIG_RESV2_FLD	R	0h	Reserved

Table 14-14. OSPI_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	PIPELINE_PHY_FLD	R/W	0h	Pipeline PHY Mode enable. This bit is relevant only for configuration with PHY module. It should be asserted to 1 between consecutive PHY pipeline reads transfers and de-asserted to 0 otherwise.
24	ENABLE_DTR_PROTOCOL_FLD	R/W	0h	Enable DTR Protocol. This bit should be set if device is configured to work in DTR protocol.
23	ENABLE_AHB_DECODER_FLD	R/W	0h	Enable AHB Decoder. 0h = Active slave is selected based on the OSPI_CONFIG_REG[13:10] PERIPH_CS_LINES_FLD. 1h = Active slave is selected based on actual data interface address (the partition is calculated with respect to bits OSPI_DEV_SIZE_CONFIG_REG[28:21]).
22-19	MSTR_BAUD_DIV_FLD	R/W	Fh	Master mode baud rate divisor (2 to 32), OSPI baud rate = (master reference clock) / (baud rate divisor) Where baud rate divisor is: 0h = /2 1h = /4 2h = /6 3h = /8 4h = /10 5h = /12 6h = /14 7h = /16 8h = /18 ... Fh = /32 Set this register up before enabling the OSPI controller.
18	ENTER_XIP_MODE_IMM_FLD	R/W	0h	Enter XIP Mode immediately. 0h = If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction Value= 1h = Operate the device in XIP mode immediately. Use this register when the external device wakes up in XIP mode [as per the contents of its non-volatile configuration register]. The controller will assume the next READ instruction will be passed to the device as an XIP instruction, and therefore will not require the READ opcode to be transferred. Note: To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only after the next READ instruction is executed. Software therefore should ensure that at least one READ instruction is requested after resetting this bit in order to be sure that XIP mode is exited.
17	ENTER_XIP_MODE_FLD	R/W	0h	Enter XIP Mode on next READ. 0h = If XIP is enabled, then setting to 0 will cause the controller to exit XIP mode on the next READ instruction. 1h = If XIP is disabled, then setting to 1 will inform the controller that the device is ready to enter XIP on the next READ instruction. The controller will therefore send the appropriate command sequence, including mode bits to cause the device to enter XIP mode. Use this register after the controller has ensured the FLASH device has been configured to be ready to enter XIP mode. Note: To exit XIP mode, this bit should be set to 0. This will take effect in the attached device only AFTER the next READ instruction is executed. Software should therefore ensure that at least one READ instruction is requested after resetting this bit before it can be sure XIP mode in the device is exited
16	ENB_AHB_ADDR_REMAP_FLD	R/W	0h	Enable Data Interface Address Remapping [Direct Access Mode Only] 1h = the incoming data interface address will be adapted and sent to the FLASH device as [address + N], where N is the value stored in the remap address register

Table 14-14. OSPI_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description												
15	ENB_DMA_IF_FLD	R/W	0h	Enable DMA Peripheral Interface. 0h = disable the DMA handshaking logic. 1h = enable the DMA handshaking logic. When enabled the controller will trigger DMA transfer requests via the DMA peripheral interface. CAUTION: This bit should be left at 0 as feature is not supported.												
14	WR_PROT_FLASH_FLD	R/W	0h	Write Protect Flash Pin. Set to drive the Write Protect pin of the FLASH device. This is resynchronized to the generated memory clock as necessary.												
13-10	PERIPH_CS_LINES_FLD	R/W	0h	Peripheral Chip Select Lines. If OSPI_CONFIG_REG[9] PERIPH_SEL_DEC_FLD = 0, ss[3:0] are output thus: <table><tr><td>ss[3:0]</td><td>N_SS_OUT[3:0]</td></tr><tr><td>xxx0</td><td>1110</td></tr><tr><td>xx01</td><td>1101</td></tr><tr><td>x011</td><td>1011</td></tr><tr><td>0111</td><td>0111</td></tr><tr><td>1111</td><td>1111 [no peripheral selected]</td></tr></table> else ss[3:0] directly drives N_SS_OUT[3:0]	ss[3:0]	N_SS_OUT[3:0]	xxx0	1110	xx01	1101	x011	1011	0111	0111	1111	1111 [no peripheral selected]
ss[3:0]	N_SS_OUT[3:0]															
xxx0	1110															
xx01	1101															
x011	1011															
0111	0111															
1111	1111 [no peripheral selected]															
9	PERIPH_SEL_DEC_FLD	R/W	0h	Peripheral select decode. 0h = only 1 of 4 selects N_SS_OUT[3:0] is active, 1h = allow external 4-to-16 decode [N_SS_OUT = ss]												
8	ENB_LEGACY_IP_MODE_FLD	R/W	0h	Legacy IP Mode Enable. 0h = Use Direct Access Controller/Indirect Access Controller 1h = Legacy Mode is enabled. In this mode, any write to the controller via the data interface is serialized and sent to the FLASH device. Any valid data read will pop the internal RX-FIFO, retrieving data that was forwarded by the external FLASH device on the SPI lines, 4, 2 or 1 byte transfers are permitted and controlled.												
7	ENB_DIR_ACC_CTLR_FLD	R/W	1h	Enable Direct Access Controller. 0h = Disable the Direct Access Controller once current transfer of the data word is complete. 1h = Enable the Direct Access Controller. When the Direct Access Controller and Indirect Access Controller are both disabled, all data requests are completed with an error response.												
6	RESET_CFG_FLD	R/W	0h	RESET pin configuration. 0h = RESET feature on DQ3 pin of the device 1h = RESET feature on dedicated pin of the device [controlling of 5th bit influences on reset_out output].												
5	RESET_PIN_FLD	R/W	0h	Set to drive the RESET pin of the FLASH device and reset for de-activation of the RESET pin feature.												
4	HOLD_PIN_FLD	R/W	0h	Set to drive the HOLD pin of the FLASH device and reset for de-activation of the HOLD pin feature.												
3	PHY_MODE_ENABLE_FLD	R/W	0h	PHY mode enable. When enabled, the controller is informed that PHY Module is to be used for handling SPI transfers. This bit is relevant only for configuration with PHY Module.												
2	SEL_CLK_PHASE_FLD	R/W	0h	Select Clock Phase. Selects whether the clock is in an active or inactive phase outside the SPI word 0h = The SPI clock is active outside the word 1h = The SPI clock is inactive outside the word												
1	SEL_CLK_POL_FLD	R/W	0h	Clock polarity outside SPI word. 0h = The SPI clock is quiescent low 1h = The SPI clock is quiescent high												
0	ENB_SPI_FLD	R/W	1h	OSPI Enable. 0h = Disable the OSPI, once current transfer of the data word is complete. 1h = Enable the OSPI, when this bit is set to 0, all output enables are inactive and all pins are set to input mode.												

14.8 OSPI_DEV_INSTR_RD_CONFIG_REG Register (Offset = 4h) [reset = 3h]

OSPI_DEV_INSTR_RD_CONFIG_REG is shown in [Figure 14-6](#) and described in [Table 14-16](#).

Return to [Summary Table](#).

Device Read Instruction Configuration Register.

This register defines the configuration of Multiple-SPI READ instruction. This register should be setup while the controller is idle.

**Table 14-15. OSPI_DEV_INSTR_RD_CONFIG_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	0004h

Figure 14-6. OSPI_DEV_INSTR_RD_CONFIG_REG Register

31	30	29	28	27	26	25	24
RD_INSTR_RESV5_FLD				DUMMY_RD_CLK_CYCLES_FLD			
R-0h				R/W-0h			
23	22	21	20	19	18	17	16
RD_INSTR_RESV4_FLD				MODE_BIT_EN ABLE_FLD	RD_INSTR_RESV3_FLD	DATA_XFER_TYPE_EXT_MODE _FLD	
R-0h				R/W-0h	R-0h	R/W-0h	
15	14	13	12	11	10	9	8
RD_INSTR_RESV2_FLD		ADDR_XFER_TYPE_STD_MOD E_FLD		RD_INSTR_RE SV1_FLD	DDR_EN_FLD	INSTR_TYPE_FLD	
R-0h		R/W-0h		R-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
RD_OPCODE_NON_XIP_FLD							
R/W-3h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-16. OSPI_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RD_INSTR_RESV5_FLD	R	0h	Reserved
28-24	DUMMY_RD_CLK_CYCL ES_FLD	R/W	0h	Dummy Read Clock Cycles. Number of dummy clock cycles required by device for read instruction.
23-21	RD_INSTR_RESV4_FLD	R	0h	Reserved
20	MODE_BIT_ENABLE_FL D	R/W	0h	Mode Bit Enable. Set this field to 1 to ensure that the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes.
19-18	RD_INSTR_RESV3_FLD	R	0h	Reserved
17-16	DATA_XFER_TYPE_EXT _MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes. 0h = SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1h = Used for Dual Input/Output instructions For data transfers, DQ0 and DQ1 are used as both inputs and outputs 2h = Used for Quad Input/Output instructions For data transfers, DQ0, DQ1, DQ2, and DQ3 are used as both inputs and outputs 3h = Used for Octal Input/Output instructions For data transfers, DQ[7:0] are used as both inputs and outputs
15-14	RD_INSTR_RESV2_FLD	R	0h	Reserved

Table 14-16. OSPI_DEV_INSTR_RD_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes. 0h = Addresses can be shifted to the device on DQ0 only 1h = Addresses can be shifted to the device on DQ0 and DQ1 only 2h = Addresses can be shifted to the device on DQ0, DQ1, DQ2, and DQ3 3h = Addresses can be shifted to the device on DQ[7:0]
11	RD_INSTR_RESV1_FLD	R	0h	Reserved
10	DDR_EN_FLD	R/W	0h	DDR Enable. This is to inform that opcode from OSPI_DEV_INSTR_RD_CONFIG_REG[7-0] RD_OPCODE_NON_XIP_FLD is compliant with one of the DDR READ commands.
9-8	INSTR_TYPE_FLD	R/W	0h	Instruction Type. 0h = Use Standard SPI mode [instruction always shifted into the device on DQ0 only] 1h = Use DIO-SPI mode [Instructions, Address and Data always sent on DQ0 and DQ1] 2h = Use QIO-SPI mode [Instructions, Address and Data always sent on DQ0, DQ1, DQ2, and DQ3] 3h = Use Octal-IO-SPI mode [Instructions, Address and Data always sent on DQ[7:0]]
7-0	RD_OPCODE_NON_XIP_FLD	R/W	3h	Read Opcode in non-XIP mode: Read Opcode to use when not in XIP mode

14.9 OSPI_DEV_INSTR_WR_CONFIG_REG Register (Offset = 8h) [reset = 2h]

OSPI_DEV_INSTR_WR_CONFIG_REG is shown in [Figure 14-7](#) and described in [Table 14-18](#).

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Device Write Instruction Configuration Register.

This register defines the configuration of Multiple-SPI WRITE (Program Page) instruction. This register should be setup while the controller is idle.

Table 14-17. OSPI_DEV_INSTR_WR_CONFIG_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0008h

Figure 14-7. OSPI_DEV_INSTR_WR_CONFIG_REG Register

31	30	29	28	27	26	25	24
WR_INSTR_RESV4_FLD				DUMMY_WR_CLK_CYCLES_FLD			
R-0h				R/W-0h			
23	22	21	20	19	18	17	16
WR_INSTR_RESV3_FLD						DATA_XFER_TYPE_EXT_MODE_FLD	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
WR_INSTR_RESV2_FLD		ADDR_XFER_TYPE_STD_MODE_FLD		WR_INSTR_RESV1_FLD			WEL_DIS_FLD
R-0h		R/W-0h		R-0h			R/W-0h
7	6	5	4	3	2	1	0
WR_OPCODE_FLD							
R/W-2h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-18. OSPI_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	WR_INSTR_RESV4_FLD	R	0h	Reserved
28-24	DUMMY_WR_CLK_CYCLES_FLD	R/W	0h	Dummy Write Clock Cycles. Number of dummy clock cycles required by device for write instruction
23-18	WR_INSTR_RESV3_FLD	R	0h	Reserved
17-16	DATA_XFER_TYPE_EXT_MODE_FLD	R/W	0h	Data Transfer Type for Standard SPI modes. 0h = SIO mode data is shifted to the device on DQ0 only and from the device on DQ1 only 1h = Used for Dual Input/Output instructions For data transfers, DQ0 and DQ1 are used as both inputs and outputs 2h = Used for Quad Input/Output instructions For data transfers, DQ0, DQ1, DQ2, and DQ3 are used as both inputs and outputs 3h = Used for Octal Input/Output instructions For data transfers, DQ[7:0] are used as both inputs and outputs
15-14	WR_INSTR_RESV2_FLD	R	0h	Reserved
13-12	ADDR_XFER_TYPE_STD_MODE_FLD	R/W	0h	Address Transfer Type for Standard SPI modes. 0h = Addresses can be shifted to the device on DQ0 only 1h = Addresses can be shifted to the device on DQ0 and DQ1 only 2h = Addresses can be shifted to the device on DQ0, DQ1, DQ2, and DQ3 3h = Addresses can be shifted to the device on DQ[7:0]

Table 14-18. OSPI_DEV_INSTR_WR_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	WR_INSTR_RESV1_FLD	R	0h	Reserved
8	WEL_DIS_FLD	R/W	0h	WEL Disable. This is to turn off automatic issuing of WEL Command before write operation for DAC or INDAC.
7-0	WR_OPCODE_FLD	R/W	2h	Write Opcode

14.10 OSPI_DEV_DELAY_REG Register (Offset = Ch) [reset = 0h]

OSPI_DEV_DELAY_REG is shown in [Figure 14-8](#) and described in [Table 14-20](#).

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OSPI Device Delay Register. This register is used to introduce relative delays into the generation of the master output signals. All timings are defined in cycles of the OSPI REFERENCE CLOCK/ext_clk, defined in this table as SPI master ref clock.

This register should be setup while the controller is idle.

Table 14-19. OSPI_DEV_DELAY_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	000Ch

Figure 14-8. OSPI_DEV_DELAY_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D_NSS_FLD								D_BTWN_FLD							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D_AFTER_FLD								D_INIT_FLD							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-20. OSPI_DEV_DELAY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	D_NSS_FLD	R/W	0h	Clock Delay for Chip Select Deassert. Delay in master reference clocks for the length that the master mode chip select outputs are de-asserted between transactions The minimum delay is always SCLK period to ensure the chip select is never re-asserted within an SCLK period.
23-16	D_BTWN_FLD	R/W	0h	Clock Delay for Chip Select Deactivation. Delay in master reference clocks between one chip select being de-activated and the activation of another This is used to ensure a quiet period between the selection of two different slaves and requires the transmit FIFO to be empty.
15-8	D_AFTER_FLD	R/W	0h	Clock Delay for Last Transaction Bit. Delay in master reference clocks between last bit of current transaction and deasserting the device chip select [n_ss_out] By default, the chip select will be deasserted on the cycle following the completion of the current transaction.
7-0	D_INIT_FLD	R/W	0h	Clock Delay with N_SS_OUT. Delay in master reference clocks between setting n_ss_out low and first bit transfer.

14.11 OSPI_RD_DATA_CAPTURE_REG Register (Offset = 10h) [reset = 1h]

OSPI_RD_DATA_CAPTURE_REG is shown in [Figure 14-9](#) and described in [Table 14-22](#).

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Read Data Capture Register.

This register is used to adjust SPI transfer conditions in order to fetch and capture data reliably. This register should be setup while the controller is idle.

**Table 14-21. OSPI_RD_DATA_CAPTURE_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	0010h

Figure 14-9. OSPI_RD_DATA_CAPTURE_REG Register

31	30	29	28	27	26	25	24
RD_DATA_RESV3_FLD							
R-0h							
23	22	21	20	19	18	17	16
RD_DATA_RESV3_FLD				DDR_READ_DELAY_FLD			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
RD_DATA_RESV2_FLD							DQS_ENABLE_FLD
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RD_DATA_RESV1_FLD		SAMPLE_EDGE_SEL_FLD		DELAY_FLD			BYPASS_FLD
R-0h		R/W-0h		R/W-0h			R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-22. OSPI_RD_DATA_CAPTURE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RD_DATA_RESV3_FLD	R	0h	Reserved
19-16	DDR_READ_DELAY_FLD	R/W	0h	DDR read delay. Delay the transmitted data by the programmed number of RCLK cycles. This field is only relevant when DDR Read Command is executed. Otherwise can be ignored.
15-9	RD_DATA_RESV2_FLD	R	0h	Reserved
8	DQS_ENABLE_FLD	R/W	0h	DQS enable bit. If enabled, signal from DQS input is driven into RX DLL and is used for data capturing in PHY Mode rather than internally generated gated RCLK.
7-6	RD_DATA_RESV1_FLD	R	0h	Reserved
5	SAMPLE_EDGE_SEL_FLD	R/W	0h	Sample edge selection. Choose edge on which data outputs from flash memory will be sampled. 0h = Data outputs from flash memory are sampled on falling edge of the RCLK. 1h = Data outputs from flash memory are sampled on rising edge of the RCLK.

Table 14-22. OSPI_RD_DATA_CAPTURE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-1	DELAY_FLD	R/W	0h	Read Delay. Delay the read data capturing logic by the programmed number of RCLK cycles.
0	BYPASS_FLD	R/W	1h	Bypass. Bypass the adapted loopback clock circuit.

14.12 OSPI_DEV_SIZE_CONFIG_REG Register (Offset = 14h) [reset = 00101002h]

OSPI_DEV_SIZE_CONFIG_REG is shown in [Figure 14-10](#) and described in [Table 14-24](#).

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Device Size Configuration Register.

This register allows to define the memory organization of using Flash Devices. This register should be setup while the controller is idle.

**Table 14-23. OSPI_DEV_SIZE_CONFIG_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	0014h

Figure 14-10. OSPI_DEV_SIZE_CONFIG_REG Register

31	30	29	28	27	26	25	24
DEV_SIZE_RESV_FLD			MEM_SIZE_ON_CS3_FLD		MEM_SIZE_ON_CS2_FLD		MEM_SIZE_ON_CS1_FLD
R-0h			R/W-0h		R/W-0h		R/W-0h
23	22	21	20	19	18	17	16
MEM_SIZE_ON_CS1_FLD	MEM_SIZE_ON_CS0_FLD		BYTES_PER_SUBSECTOR_FLD				
R/W-0h	R/W-0h		R/W-10h				
15	14	13	12	11	10	9	8
BYTES_PER_DEVICE_PAGE_FLD							
R/W-100h							
7	6	5	4	3	2	1	0
BYTES_PER_DEVICE_PAGE_FLD				NUM_ADDR_BYTES_FLD			
R/W-100h				R/W-2h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-24. OSPI_DEV_SIZE_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	DEV_SIZE_RESV_FLD	R	0h	Reserved
28-27	MEM_SIZE_ON_CS3_FLD	R/W	0h	Size of Flash Device connected to CS[3] pin: 0h = size of 512Mb 1h = size of 1Gb 2h = size of 2Gb 3h = size of 4Gb
26-25	MEM_SIZE_ON_CS2_FLD	R/W	0h	Size of Flash Device connected to CS[2] pin: 0h = size of 512Mb 1h = size of 1Gb 2h = size of 2Gb 3h = size of 4Gb
24-23	MEM_SIZE_ON_CS1_FLD	R/W	0h	Size of Flash Device connected to CS[1] pin: 0h = size of 512Mb 1h = size of 1Gb 2h = size of 2Gb 3h = size of 4Gb
22-21	MEM_SIZE_ON_CS0_FLD	R/W	0h	Size of Flash Device connected to CS[0] pin: 0h = size of 512Mb 1h = size of 1Gb 2h = size of 2Gb 3h = size of 4Gb

Table 14-24. OSPI_DEV_SIZE_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-16	BYTES_PER_SUBSECTOR_FLD	R/W	10h	Number of bytes per Block. This is required by the controller for performing the write protection logic. The number of bytes per block must be a power of 2 number. 0 = 1 byte h = 2 bytes 3 = 8 bytes ... 16 = 65535 bytes, etc.
15-4	BYTES_PER_DEVICE_PAGE_FLD	R/W	100h	Number of bytes per device page. This is required by the controller for performing FLASH writes up to and across page boundaries.
3-0	NUM_ADDR_BYTES_FLD	R/W	2h	Number of address bytes. A value of 0 indicates 1 byte.

14.13 OSPI_SRAM_PARTITION_CFG_REG Register (Offset = 18h) [reset = 80h]

OSPI_SRAM_PARTITION_CFG_REG is shown in [Figure 14-11](#) and described in [Table 14-26](#).

Return to [Summary Table](#).

SRAM Partition Configuration Register.

Table 14-25. OSPI_SRAM_PARTITION_CFG_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0018h

Figure 14-11. OSPI_SRAM_PARTITION_CFG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM_PARTITION_RESV_FLD																ADDR_FLD															
R-0h																R/W-80h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-26. OSPI_SRAM_PARTITION_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	SRAM_PARTITION_RESV_FLD	R	0h	Reserved
7-0	ADDR_FLD	R/W	80h	Indirect Read Partition Size. Defines the size of the indirect read partition in the SRAM, in units of SRAM locations. By default, half of the SRAM is reserved for indirect read operation, and half for indirect write. The size of this register will scale with the depth of the SRAM.

14.14 OSPI_IND_AHB_ADDR_TRIGGER_REG Register (Offset = 1Ch) [reset = 0h]

OSPI_IND_AHB_ADDR_TRIGGER_REG is shown in [Figure 14-12](#) and described in [Table 14-28](#).

Return to [Summary Table](#).

Indirect AHB Address Trigger Register.

This register allowsto define the address distinguishing DAC access from triggered INDAC one. This register should be setup while the controller is idle.

**Table 14-27. OSPI_IND_AHB_ADDR_TRIGGER_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	001Ch

Figure 14-12. OSPI_IND_AHB_ADDR_TRIGGER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-28. OSPI_IND_AHB_ADDR_TRIGGER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_FLD	R/W	0h	Indirect Trigger Address. This is the base address used by the data interface. When the incoming data read/write access address matches a range of addresses from this trigger address to the trigger address + [configured range in OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG], then the data request is completed by fetching data from the Indirect Controllers SRAM.

14.15 OSPI_DMA_PERIPH_CONFIG_REG Register (Offset = 20h) [reset = 0h]

OSPI_DMA_PERIPH_CONFIG_REG is shown in [Figure 14-13](#) and described in [Table 14-30](#).

Return to [Summary Table](#).

DMA Peripheral Configuration Register.

This register allows to define the parameters of DMA peripheral controller. This register should be setup while the controller is idle.

Note: Reserved. This feature is not supported.

Table 14-29. OSPI_DMA_PERIPH_CONFIG_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0020h

Figure 14-13. OSPI_DMA_PERIPH_CONFIG_REG Register

31	30	29	28	27	26	25	24
DMA_PERIPH_RESV2_FLD							
R-0h							
23	22	21	20	19	18	17	16
DMA_PERIPH_RESV2_FLD							
R-0h							
15	14	13	12	11	10	9	8
DMA_PERIPH_RESV2_FLD				NUM_BURST_REQ_BYTES_FLD			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
DMA_PERIPH_RESV1_FLD				NUM_SINGLE_REQ_BYTES_FLD			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-30. OSPI_DMA_PERIPH_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	DMA_PERIPH_RESV2_FLD	R	0h	Reserved
11-8	NUM_BURST_REQ_BYTES_FLD	R/W	0h	Number of Burst Bytes. Number of bytes in a burst type request on the DMA peripheral request. A programmed value of 0 represents a single byte. This should be setup before starting the indirect read or write operation. The actual number of bytes used is 2**[value in this register] which will simplify implementation.
7-4	DMA_PERIPH_RESV1_FLD	R	0h	Reserved

Table 14-30. OSPI_DMA_PERIPH_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	NUM_SINGLE_REQ_BYTES_FLD	R/W	0h	<p>Number of Single Bytes.</p> <p>Number of bytes in a single type request on the DMA peripheral request.</p> <p>A programmed value of 0 represents a single byte.</p> <p>This should be setup before starting the indirect read or write operation.</p> <p>The actual number of bytes used is $2^{**}[\text{value in this register}]$ which will simplify implementation.</p>

14.16 OSPI_REMAP_ADDR_REG Register (Offset = 24h) [reset = 0h]

OSPI_REMAP_ADDR_REG is shown in [Figure 14-14](#) and described in [Table 14-32](#).

Return to [Summary Table](#).

Remap Address Register.

This register allows to define the address offset for DAC accesses. This register should be setup while the controller is idle.

Table 14-31. OSPI_REMAP_ADDR_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0024h

Figure 14-14. OSPI_REMAP_ADDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-32. OSPI_REMAP_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE_FLD	R/W	0h	This register is used to remap an incoming data address to a different address used by the FLASH device.

14.17 OSPI_MODE_BIT_CONFIG_REG Register (Offset = 28h) [reset = 200h]

OSPI_MODE_BIT_CONFIG_REG is shown in [Figure 14-15](#) and described in [Table 14-34](#).

Return to [Summary Table](#).

Mode Bit Configuration Register.

This register allows to define the mode bits for corresponding Flash Device. It also provides configuration for CRC aware SPI transfers. This register should be setup while the controller is idle.

**Table 14-33. OSPI_MODE_BIT_CONFIG_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	0028h

Figure 14-15. OSPI_MODE_BIT_CONFIG_REG Register

31	30	29	28	27	26	25	24
RX_CRC_DATA_LOW_FLD							
R-0h							
23	22	21	20	19	18	17	16
RX_CRC_DATA_UP_FLD							
R-0h							
15	14	13	12	11	10	9	8
CRC_OUT_EN ABLE_FLD	MODE_BIT_RESV1_FLD				CHUNK_SIZE_FLD		
R/W-0h	R-0h				R/W-2h		
7	6	5	4	3	2	1	0
MODE_FLD							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-34. OSPI_MODE_BIT_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RX_CRC_DATA_LOW_FLD	R	0h	RX CRC data [lower]. The first CRC byte returned after RX data chunk.
23-16	RX_CRC_DATA_UP_FLD	R	0h	RX CRC data [upper]. The second CRC byte returned after RX data chunk.
15	CRC_OUT_ENABLE_FLD	R/W	0h	CRC# output enable bit. When enabled, the controller expects the Flash Device to toggle CRC data on both SPI clock edges in CRC->CRC# sequence and calculates CRC compliance accordingly.
14-11	MODE_BIT_RESV1_FLD	R	0h	Reserved
10-8	CHUNK_SIZE_FLD	R/W	2h	It defines size of chunk after which CRC data is expected to show up on the SPI interface for write and read data transfers. 0h = 4 bytes 1h = 8 bytes 2h = 16 bytes 3h = 32 bytes 4h = 64 bytes 5h = 128 bytes 6h = 256 bytes 7h = 512 bytes

Table 14-34. OSPI_MODE_BIT_CONFIG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	MODE_FLD	R/W	0h	These are the 8 mode bits that are sent to the device following the address bytes if mode bit transmission has been enabled.

14.18 OSPI_SRAM_FILL_REG Register (Offset = 2Ch) [reset = 0h]

OSPI_SRAM_FILL_REG is shown in [Figure 14-16](#) and described in [Table 14-36](#).

Return to [Summary Table](#).

SRAM Fill Register.

This register keeps the values of current fill levels of both SRAM partitions.

Table 14-35. OSPI_SRAM_FILL_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	002Ch

Figure 14-16. OSPI_SRAM_FILL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRAM_FILL_INDAC_WRITE_FLD															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRAM_FILL_INDAC_READ_FLD															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 14-36. OSPI_SRAM_FILL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SRAM_FILL_INDAC_WRITE_FLD	R	0h	SRAM Fill Level [Indirect Write Partition]. Identifies the current fill level of the SRAM Indirect Write partition.
15-0	SRAM_FILL_INDAC_READ_FLD	R	0h	SRAM Fill Level [Indirect Read Partition]. Identifies the current fill level of the SRAM Indirect Read partition.

14.19 OSPI_TX_THRESH_REG Register (Offset = 30h) [reset = 1h]

OSPI_TX_THRESH_REG is shown in [Figure 14-17](#) and described in [Table 14-38](#).

Return to [Summary Table](#).

TX Threshold Register.

This register allows to define the TX FIFO level arousing the corresponding interrupt. This register should be setup while the controller is idle.

Table 14-37. OSPI_TX_THRESH_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0030h

Figure 14-17. OSPI_TX_THRESH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_THRESH_RESV_FLD															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_THRESH_RESV_FLD											LEVEL_FLD				
R-0h											R/W-1h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-38. OSPI_TX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	TX_THRESH_RESV_FLD	R	0h	Reserved
4-0	LEVEL_FLD	R/W	1h	Defines the level at which the small TX FIFO not full interrupt is generated

14.20 OSPI_RX_THRESH_REG Register (Offset = 34h) [reset = 1h]

OSPI_RX_THRESH_REG is shown in [Figure 14-18](#) and described in [Table 14-40](#).

Return to [Summary Table](#).

RX Threshold Register.

This register allows to define the RX FIFO level arousing the corresponding interrupt. This register should be setup while the controller is idle.

Table 14-39. OSPI_RX_THRESH_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0034h

Figure 14-18. OSPI_RX_THRESH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_THRESH_RESV_FLD															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_THRESH_RESV_FLD											LEVEL_FLD				
R-0h											R/W-1h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-40. OSPI_RX_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RX_THRESH_RESV_FLD	R	0h	Reserved
4-0	LEVEL_FLD	R/W	1h	Defines the level at which the small RX FIFO not empty interrupt is generated.

14.21 OSPI_WRITE_COMPLETION_CTRL_REG Register (Offset = 38h) [reset = 00010005h]

OSPI_WRITE_COMPLETION_CTRL_REG is shown in [Figure 14-19](#) and described in [Table 14-42](#).

Return to [Summary Table](#).

Write Completion Control Register. This register defines how the controller will poll the device following a write transfer.

Table 14-41.
OSPI_WRITE_COMPLETION_CTRL_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0038h

Figure 14-19. OSPI_WRITE_COMPLETION_CTRL_REG Register

31	30	29	28	27	26	25	24
POLL_REP_DELAY_FLD							
R/W-0h							
23	22	21	20	19	18	17	16
POLL_COUNT_FLD							
R/W-1h							
15	14	13	12	11	10	9	8
ENABLE_POLLING_EXP_FLD	DISABLE_POLLING_FLD	POLLING_POLARITY_FLD	WR_COMP_CTRL_RESV1_FLD		POLLING_BIT_INDEX_FLD		
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h		
7	6	5	4	3	2	1	0
OPCODE_FLD							
R/W-5h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-42. OSPI_WRITE_COMPLETION_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	POLL_REP_DELAY_FLD	R/W	0h	Polling repetition delay. Defines additional delay for maintain Chip Select de-asserted during auto-polling phase.
23-16	POLL_COUNT_FLD	R/W	1h	Polling count. Defines the number of times the controller should expect to see a true result from the polling in successive reads of the device register. The poll_count_fld in Write Completion Control register should always be set with values greater or equal to 3 (>=3).
15	ENABLE_POLLING_EXP_FLD	R/W	0h	Enable polling expiration. 1h = enabling auto-polling expiration in OSPI_NO_OF_POLLS_BEF_EXP_REG.
14	DISABLE_POLLING_FLD	R/W	0h	Disable polling. This switches off the automatic polling function.
13	POLLING_POLARITY_FLD	R/W	0h	Polling polarity. Defines the polling polarity. 0h = The write transfer to the device will be complete if the polled bit is equal to 0. 1h = The write transfer to the device will be complete if the polled bit is equal to 1.
12-11	WR_COMP_CTRL_RESV1_FLD	R	0h	Reserved

Table 14-42. OSPI_WRITE_COMPLETION_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-8	POLLING_BIT_INDEX_FLD	R/W	0h	<p>Polling bit index.</p> <p>Defines the bit index that should be polled.</p> <p>0h = bit 0 of the returned data will be polled for.</p> <p>1h = bit 1 of the returned data will be polled for.</p> <p>2h = bit 2 of the returned data will be polled for.</p> <p>...</p> <p>7h = bit 7 of the returned data will be polled for.</p>
7-0	OPCODE_FLD	R/W	5h	<p>Polling opcode.</p> <p>Defines the opcode that should be issued by the controller when it is automatically polling for device program completion. This command is issued followed all device write operations. By default, this will poll the standard device STATUS register using opcode 0x05.</p>

14.22 OSPI_NO_OF_POLLS_BEF_EXP_REG Register (Offset = 3Ch) [reset = FFFFFFFFh]

OSPI_NO_OF_POLLS_BEF_EXP_REG is shown in [Figure 14-20](#) and described in [Table 14-44](#).

Return to [Summary Table](#).

Polling Expiration Register.

This register defines maximum number of poll cycles. If the expected value of the bit being polled is not gotten after number defined in this register, the auto-polling is done on the next phase.

Table 14-43. OSPI_NO_OF_POLLS_BEF_EXP_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	003Ch

Figure 14-20. OSPI_NO_OF_POLLS_BEF_EXP_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NO_OF_POLLS_BEF_EXP_FLD																															
R/W-FFFFFFFh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-44. OSPI_NO_OF_POLLS_BEF_EXP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NO_OF_POLLS_BEF_EXP_FLD	R/W	FFFFFFFh	Defines the numbers of poll cycles after which auto-polling phase terminates and polling expiration interrupt is generated.

14.23 OSPI_IRQ_STATUS_REG Register (Offset = 40h) [reset = 0h]

OSPI_IRQ_STATUS_REG is shown in [Figure 14-21](#) and described in [Table 14-46](#).

Return to [Summary Table](#).

Interrupt Status Register. The status fields in this register are set when the described event occurs and the interrupt is enabled in the mask register. When any of these bit fields are set, the interrupt output is asserted high. The fields are each cleared by writing a 1 to the field. Note that bit fields 6 through 10 are only valid when legacy SPI mode is active.

Table 14-45. OSPI_IRQ_STATUS_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0040h

Figure 14-21. OSPI_IRQ_STATUS_REG Register

31	30	29	28	27	26	25	24
IRQ_STAT_RESV_FLD							
R-0h							
23	22	21	20	19	18	17	16
IRQ_STAT_RESV_FLD				ECC_FAIL_FLD	TX_CRC_CHUNK_BRK_FLD	RX_CRC_DATA_VAL_FLD	RX_CRC_DATA_ERR_FLD
R/W1C-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
IRQ_STAT_RESV1_FLD	STIG_REQ_INT_FLD	POLL_EXP_INT_FLD	INDRD_SRAM_FULL_FLD	RX_FIFO_FULL_FLD	RX_FIFO_NOT_EMPTY_FLD	TX_FIFO_FULL_FLD	TX_FIFO_NOT_FULL_FLD
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
RECV_OVERFLOW_FLD	INDIRECT_XFER_LEVEL_BREAK_FLD	ILLEGAL_ACCESS_DET_FLD	PROT_WR_ATTEMPT_FLD	INDIRECT_READ_REJECT_FLD	INDIRECT_OP_DONE_FLD	UNDERFLOW_DET_FLD	MODE_M_FAIL_FLD
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 14-46. OSPI_IRQ_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	IRQ_STAT_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_FLD	R/W1C	0h	ECC failure. This interrupt informs the system that Flash Device reported ECC error.
18	TX_CRC_CHUNK_BRK_FLD	R/W1C	0h	TX CRC chunk was broken. This interrupt informs the system that program page SPI transfer was discontinued somewhere inside the chunk.
17	RX_CRC_DATA_VAL_FLD	R/W1C	0h	RX CRC data valid. New RX CRC data was captured from Flash Device.
16	RX_CRC_DATA_ERR_FLD	R/W1C	0h	RX CRC data error. CRC data from Flash Device does not correspond to the one dynamically calculated by the controller
15	IRQ_STAT_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_INT_FLD	R/W1C	0h	The controller is ready for getting another STIG request.
13	POLL_EXP_INT_FLD	R/W1C	0h	The maximum number of programmed polls cycles is expired.

Table 14-46. OSPI_IRQ_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	INDRD_SRAM_FULL_FLD	R/W1C	0h	Indirect Read Partition overflow. Indirect Read Partition of SRAM is full and unable to immediately complete indirect operation.
11	RX_FIFO_FULL_FLD	R/W1C	0h	Small RX FIFO full. Current FIFO status can be ignored in non-SPI legacy mode. 0h = FIFO is not full 1h = FIFO is full
10	RX_FIFO_NOT_EMPTY_FLD	R/W1C	0h	Small RX FIFO not empty. Current FIFO status can be ignored in non-SPI legacy mode. 0h = FIFO has less than RX THRESHOLD entries. 1h = FIFO has >= THRESHOLD entries.
9	TX_FIFO_FULL_FLD	R/W1C	0h	Small TX FIFO full. Current FIFO status can be ignored in non-SPI legacy mode 0h = FIFO is not full 1h = FIFO is full
8	TX_FIFO_NOT_FULL_FLD	R/W1C	0h	Small TX FIFO not full. Current FIFO status can be ignored in non-SPI legacy mode 0h = FIFO has >= THRESHOLD entries. 1h = FIFO has less than THRESHOLD entries.
7	RECV_OVERFLOW_FLD	R/W1C	0h	Receive Overflow. This should only occur in Legacy SPI mode. Set if an attempt is made to push the RX FIFO when it is full. This bit is reset only by a system reset and cleared only when this register is read. If a new push to the RX FIFO occurs coincident with a register read this flag will remain set. 0h = no overflow has been detected. 1h = an overflow has occurred.
6	INDIRECT_XFER_LEVEL_BREACH_FLD	R/W1C	0h	Indirect Transfer Watermark Level Breached.
5	ILLEGAL_ACCESS_DET_FLD	R/W1C	0h	Illegal AHB access has been detected AHB wrapping bursts and the use of SPLIT/RETRY accesses will cause this error interrupt to trigger.
4	PROT_WR_ATTEMPT_FLD	R/W1C	0h	Write to protected area was attempted and rejected.
3	INDIRECT_READ_REJECT_FLD	R/W1C	0h	Indirect operation was requested but could not be accepted. Two indirect operations already in storage.
2	INDIRECT_OP_DONE_FLD	R/W1C	0h	Indirect Operation Complete: Controller has completed last triggered indirect operation.
1	UNDERFLOW_DET_FLD	R/W1C	0h	Underflow Detected: 0h = no underflow has been detected 1h = underflow is detected and an attempt to transfer data is made when the small TX FIFO is empty. This may occur when AHB write data is being supplied too slowly to keep up with the requested write operation. This bit is reset only by a system reset and cleared only when the register is read.
0	MODE_M_FAIL_FLD	R/W1C	0h	Mode M Failure. Mode M failure indicates the voltage on pin N_SS_IN is inconsistent with the SPI mode. Set =1 if N_SS_IN is low in master mode [multi-master contention]. These conditions will clear the spi_enable bit and disable the SPI. This bit is reset only by a system reset and cleared only when this register is: Read 0h = no mode fault has been detected. Read 1h = a mode fault has occurred.

14.24 OSPI_IRQ_MASK_REG Register (Offset = 44h) [reset = 0h]

OSPI_IRQ_MASK_REG is shown in [Figure 14-22](#) and described in [Table 14-48](#).

Return to [Summary Table](#).

Interrupt Mask Register.

This register allows the user to mask/unmask particular interrupt sources. This register should be setup while the controller is idle.

0h = the interrupt for the corresponding interrupt status register bit is disabled.

1h = the interrupt for the corresponding interrupt status register bit is enabled.

Table 14-47. OSPI_IRQ_MASK_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0044h

Figure 14-22. OSPI_IRQ_MASK_REG Register

31	30	29	28	27	26	25	24
IRQ_MASK_RESV_FLD							
R-0h							
23	22	21	20	19	18	17	16
IRQ_MASK_RESV_FLD				ECC_FAIL_MA SK_FLD	TX_CRC_CHU NK_BRK_MAS K_FLD	RX_CRC_DATA _VAL_MASK_F LD	RX_CRC_DATA _ERR_MASK_F LD
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
IRQ_MASK_RE SV1_FLD	STIG_REQ_MA SK_FLD	POLL_EXP_IN T_MASK_FLD	INDRD_SRAM FULL_MASK_F LD	RX_FIFO_FULL _MASK_FLD	RX_FIFO_NOT _EMPTY_MAS K_FLD	TX_FIFO_FULL _MASK_FLD	TX_FIFO_NOT _FULL_MASK_ FLD
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RECV_OVERF LOW_MASK_F LD	INDIRECT_XFE R_LEVEL_BRE ACH_MASK_FL D	ILLEGAL_ACC ESS_DET_MA SK_FLD	PROT_WR_AT TEMPT_MASK _FLD	INDIRECT_RE AD_REJECT_M ASK_FLD	INDIRECT_OP _DONE_MASK _FLD	UNDERFLOW_ DET_MASK_FL D	MODE_M_FAIL _MASK_FLD
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-48. OSPI_IRQ_MASK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	IRQ_MASK_RESV_FLD	R	0h	Reserved
19	ECC_FAIL_MASK_FLD	R/W	0h	ECC failure Mask
18	TX_CRC_CHUNK_BRK_MASK_FLD	R/W	0h	TX CRC chunk was broken Mask
17	RX_CRC_DATA_VAL_MASK_FLD	R/W	0h	RX CRC data valid Mask
16	RX_CRC_DATA_ERR_MASK_FLD	R/W	0h	RX CRC data error Mask
15	IRQ_MASK_RESV1_FLD	R	0h	Reserved
14	STIG_REQ_MASK_FLD	R/W	0h	STIG request completion Mask
13	POLL_EXP_INT_MASK_FLD	R/W	0h	Polling expiration detected Mask

Table 14-48. OSPI_IRQ_MASK_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	INDRD_SRAM_FULL_MASK_FLD	R/W	0h	Indirect Read Partition overflow mask
11	RX_FIFO_FULL_MASK_FLD	R/W	0h	Small RX FIFO full Mask
10	RX_FIFO_NOT_EMPTY_MASK_FLD	R/W	0h	Small RX FIFO not empty Mask
9	TX_FIFO_FULL_MASK_FLD	R/W	0h	Small TX FIFO full Mask
8	TX_FIFO_NOT_FULL_MASK_FLD	R/W	0h	Small TX FIFO not full Mask
7	RECV_OVERFLOW_MASK_FLD	R/W	0h	Receive Overflow Mask
6	INDIRECT_XFER_LEVEL_BREACH_MASK_FLD	R/W	0h	Transfer Watermark Breach Mask
5	ILLEGAL_ACCESS_DETECTED_MASK_FLD	R/W	0h	Illegal Access Detected Mask
4	PROT_WR_ATTEMPT_MASK_FLD	R/W	0h	Protected Area Write Attempt Mask
3	INDIRECT_READ_REJECT_MASK_FLD	R/W	0h	Indirect Read Reject Mask
2	INDIRECT_OP_DONE_MASK_FLD	R/W	0h	Indirect Complete Mask
1	UNDERFLOW_DETECTED_MASK_FLD	R/W	0h	Underflow Detected Mask
0	MODE_M_FAIL_MASK_FLD	R/W	0h	Mode M Failure Mask

14.25 OSPI_LOWER_WR_PROT_REG Register (Offset = 50h) [reset = 0h]

OSPI_LOWER_WR_PROT_REG is shown in [Figure 14-23](#) and described in [Table 14-50](#).

Return to [Summary Table](#).

Lower Write Protection Register.

This register allows to define lower boundary of the write protection area. This register should be setup while the controller is idle.

**Table 14-49. OSPI_LOWER_WR_PROT_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	0050h

Figure 14-23. OSPI_LOWER_WR_PROT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSECTOR_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-50. OSPI_LOWER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SUBSECTOR_FLD	R/W	0h	Lower Block Number. The block number that defines the lower block in the range of blocks that is to be locked from writing. The definition of a block in terms of number of bytes is programmable via the OSPI_DEV_SIZE_CONFIG_REG register.

14.26 OSPI_UPPER_WR_PROT_REG Register (Offset = 54h) [reset = 0h]

OSPI_UPPER_WR_PROT_REG is shown in [Figure 14-24](#) and described in [Table 14-52](#).

Return to [Summary Table](#).

Upper Write Protection Register.

This register allows to define upper boundary of the write protection area. This register should be setup while the controller is idle.

Table 14-51. OSPI_UPPER_WR_PROT_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0054h

Figure 14-24. OSPI_UPPER_WR_PROT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUBSECTOR_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-52. OSPI_UPPER_WR_PROT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SUBSECTOR_FLD	R/W	0h	Lower Block Number. The block number that defines the upper block in the range of blocks that is to be locked from writing. The definition of a block in terms of number of bytes is programmable via the OSPI_DEV_SIZE_CONFIG_REG register.

14.27 OSPI_WR_PROT_CTRL_REG Register (Offset = 58h) [reset = 0h]

OSPI_WR_PROT_CTRL_REG is shown in [Figure 14-25](#) and described in [Table 14-54](#).

Return to [Summary Table](#).

Write Protection Control Register.

This register allows to define the configuration of write protection settings. This register should be setup while the controller is idle.

Table 14-53. OSPI_WR_PROT_CTRL_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0058h

Figure 14-25. OSPI_WR_PROT_CTRL_REG Register

31	30	29	28	27	26	25	24
WR_PROT_CTRL_RESV_FLD							
R-0h							
23	22	21	20	19	18	17	16
WR_PROT_CTRL_RESV_FLD							
R-0h							
15	14	13	12	11	10	9	8
WR_PROT_CTRL_RESV_FLD							
R-0h							
7	6	5	4	3	2	1	0
WR_PROT_CTRL_RESV_FLD						ENB_FLD	INV_FLD
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-54. OSPI_WR_PROT_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	WR_PROT_CTRL_RESV_FLD	R	0h	Reserved
1	ENB_FLD	R/W	0h	Write Protection Enable Bit. 0h = the protection region is disabled. 1h = any data write access with an address within the protection region defined in the lower and upper write protection registers is rejected. A data error response is generated and an interrupt source triggered.
0	INV_FLD	R/W	0h	Write Protection Inversion Bit. 0h = the protection region defined in the lower and upper write protection registers is the region that the system is not permitted to write to. 1h = the protection region defined in the lower and upper write protection registers is inverted meaning it is the region that the system is permitted to write to.

14.28 OSPI_INDIRECT_READ_XFER_CTRL_REG Register (Offset = 60h) [reset = 0h]

OSPI_INDIRECT_READ_XFER_CTRL_REG is shown in [Figure 14-26](#) and described in [Table 14-56](#).

Return to [Summary Table](#).

Indirect Read Transfer Control Register.

This register allows control of the Indirect Read Transfer logic.

Table 14-55.
OSPI_INDIRECT_READ_XFER_CTRL_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0060h

Figure 14-26. OSPI_INDIRECT_READ_XFER_CTRL_REG Register

31	30	29	28	27	26	25	24
INDIR_RD_XFER_RESV_FLD							
R-0h							
23	22	21	20	19	18	17	16
INDIR_RD_XFER_RESV_FLD							
R-0h							
15	14	13	12	11	10	9	8
INDIR_RD_XFER_RESV_FLD							
R-0h							
7	6	5	4	3	2	1	0
NUM_IND_OPS_DONE_FLD	IND_OPS_DONE_STATUS_FLD	RD_QUEUED_FLD	SRAM_FULL_FLD	RD_STATUS_FLD	CANCEL_FLD	START_FLD	
R-0h	R/W1C-0h	R-0h	R/W1C-0h	R-0h	W-0h	W-0h	

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; W = Write Only; -n = value after reset

Table 14-56. OSPI_INDIRECT_READ_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	INDIR_RD_XFER_RESV_FLD	R	0h	Reserved
7-6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the OSPI_INDIRECT_READ_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD It is incremented by hardware when an indirect operation has completed. Write a 1 to OSPI_INDIRECT_READ_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1C	0h	Indirect Completion Status. This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it.
4	RD_QUEUED_FLD	R	0h	Queued Indirect Read Operations. Two indirect read operations have been queued.
3	SRAM_FULL_FLD	R/W1C	0h	SRAM Full. SRAM full and unable to immediately complete an indirect operation. Write a 1 to this field to clear it indirect operation [status].

Table 14-56. OSPI_INDIRECT_READ_XFER_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RD_STATUS_FLD	R	0h	Indirect Read Status. Indirect read operation in progress [status].
1	CANCEL_FLD	W	0h	Cancel Indirect Read. Writing a 1 to this bit will cancel all ongoing indirect read operations.
0	START_FLD	W	0h	Start Indirect Read. Writing a 1 to this bit will trigger an indirect read operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect read operation.

14.29 OSPI_INDIRECT_READ_XFER_WATERMARK_REG Register (Offset = 64h) [reset = 0h]

OSPI_INDIRECT_READ_XFER_WATERMARK_REG is shown in [Figure 14-27](#) and described in [Table 14-58](#).

Return to [Summary Table](#).

Indirect Read Transfer Watermark Register.

This register allows to define watermark level for Indirect read transfers. This register should be setup before an indirect read transfer is triggered.

Note

Some of the OSPI features described in this section may not be supported on this family of devices. For more information, see *OSPI Not Supported Features*.

Table 14-57.
OSPI_INDIRECT_READ_XFER_WATERMARK_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0064h

Figure 14-27. OSPI_INDIRECT_READ_XFER_WATERMARK_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVEL_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-58. OSPI_INDIRECT_READ_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LEVEL_FLD	R/W	0h	Watermark Value. This represents the minimum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level passes the watermark, an interrupt is also generated. This field can be disabled by writing a value of all zeroes.

14.30 OSPI_INDIRECT_READ_XFER_START_REG Register (Offset = 68h) [reset = 0h]

OSPI_INDIRECT_READ_XFER_START_REG is shown in [Figure 14-28](#) and described in [Table 14-60](#).

Return to [Summary Table](#).

Indirect Read Transfer Start Address Register.

This register allows to define start address of indirect read transfer which is about to be triggered. This register should be setup before an indirect read transfer is triggered.

Table 14-59.
OSPI_INDIRECT_READ_XFER_START_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0068h

Figure 14-28. OSPI_INDIRECT_READ_XFER_START_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-60. OSPI_INDIRECT_READ_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_FLD	R/W	0h	Start of Indirect Access. This is the start address from which the indirect access will commence its READ operation.

14.31 OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG Register (Offset = 6Ch) [reset = 0h]

OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG is shown in [Figure 14-29](#) and described in [Table 14-62](#).

Return to [Summary Table](#).

Indirect Read Transfer Number Bytes Register.

This register allows to define number of bytes to be read of indirect read transfer which is about to be triggered. This register should be setup before an indirect read transfer is triggered.

Table 14-61.
OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	006Ch

Figure 14-29. OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-62. OSPI_INDIRECT_READ_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE_FLD	R/W	0h	Indirect Number of Bytes. This is the number of bytes that the indirect access will consume This can be bigger than the configured size of SRAM.

14.32 OSPI_INDIRECT_WRITE_XFER_CTRL_REG Register (Offset = 70h) [reset = 0h]

OSPI_INDIRECT_WRITE_XFER_CTRL_REG is shown in [Figure 14-30](#) and described in [Table 14-64](#).

Return to [Summary Table](#).

Indirect Write Transfer Control Register.

This register allows control of the Indirect Write Transfer logic.

Table 14-63.
OSPI_INDIRECT_WRITE_XFER_CTRL_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0070h

Figure 14-30. OSPI_INDIRECT_WRITE_XFER_CTRL_REG Register

31	30	29	28	27	26	25	24
INDIR_WR_XFER_RESV2_FLD							
R-0h							
23	22	21	20	19	18	17	16
INDIR_WR_XFER_RESV2_FLD							
R-0h							
15	14	13	12	11	10	9	8
INDIR_WR_XFER_RESV2_FLD							
R-0h							
7	6	5	4	3	2	1	0
NUM_IND_OPS_DONE_FLD	IND_OPS_DONE_STATUS_FLD	WR_QUEUED_FLD	INDIR_WR_XFER_RESV1_FLD	WR_STATUS_FLD	CANCEL_FLD	START_FLD	
R-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h	W-0h	W-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; W = Write Only; -n = value after reset

Table 14-64. OSPI_INDIRECT_WRITE_XFER_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	INDIR_WR_XFER_RESV2_FLD	R	0h	Reserved
7-6	NUM_IND_OPS_DONE_FLD	R	0h	This field contains the number of indirect operations which have been completed. This is used in conjunction with the OSPI_INDIRECT_WRITE_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD. It is incremented by hardware when an indirect operation has completed. Write a 1 to OSPI_INDIRECT_WRITE_XFER_CTRL_REG[5] IND_OPS_DONE_STATUS_FLD of this register to decrement it.
5	IND_OPS_DONE_STATUS_FLD	R/W1C	0h	Indirect Completion Status. This field is set to 1 when an indirect operation has completed. Write a 1 to this field to clear it
4	WR_QUEUED_FLD	R	0h	Two indirect write operations have been queued.
3	INDIR_WR_XFER_RESV1_FLD	R	0h	Reserved
2	WR_STATUS_FLD	R	0h	Indirect Write Status. Indirect write operation in progress [status].

Table 14-64. OSPI_INDIRECT_WRITE_XFER_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CANCEL_FLD	W	0h	Cancel Indirect Write. Writing a 1 to this bit will cancel all ongoing indirect write operations.
0	START_FLD	W	0h	Start Indirect Write. Writing a 1 to this bit will trigger an indirect write operation. The assumption is that the indirect start address and the indirect number of bytes register is setup before triggering the indirect write operation.

14.33 OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG Register (Offset = 74h) [reset = FFFFFFFFh]

OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG is shown in [Figure 14-31](#) and described in [Table 14-66](#).

Return to [Summary Table](#).

Indirect Write Transfer Watermark Register.

This register allows to define watermark level for Indirect write transfers. This register should be setup before an indirect write transfer is triggered.

Note

Some of the OSPI features described in this section may not be supported on this family of devices. For more information, see *OSPI Not Supported Features*.

Table 14-65.
OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0074h

Figure 14-31. OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVEL_FLD																															
R/W-FFFFFFFh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-66. OSPI_INDIRECT_WRITE_XFER_WATERMARK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LEVEL_FLD	R/W	FFFFFFFh	Watermark Value. This represents the maximum fill level of the SRAM before a DMA peripheral access is permitted. When the SRAM fill level falls below the watermark, an interrupt is also generated. This field can be disabled by writing a value of all ones.

14.34 OSPI_INDIRECT_WRITE_XFER_START_REG Register (Offset = 78h) [reset = 0h]

OSPI_INDIRECT_WRITE_XFER_START_REG is shown in [Figure 14-32](#) and described in [Table 14-68](#).

Return to [Summary Table](#).

Indirect Write Transfer Start Address Register.

This register allows to define start address of indirect write transfer which is about to be triggered. This register should be setup before an indirect write transfer is triggered.

Table 14-67.
OSPI_INDIRECT_WRITE_XFER_START_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0078h

Figure 14-32. OSPI_INDIRECT_WRITE_XFER_START_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-68. OSPI_INDIRECT_WRITE_XFER_START_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_FLD	R/W	0h	Start of Indirect Access. This is the start address from which the indirect access will commence its WRITE operation.

14.35 OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register (Offset = 7Ch) [reset = 0h]

OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG is shown in [Figure 14-33](#) and described in [Table 14-70](#).

Return to [Summary Table](#).

Indirect Write Transfer Number Bytes Register.

This register allows to define number of bytes to be written of indirect read transfer which is about to be triggered. This register should be setup before an indirect read transfer is triggered.

Table 14-69.
OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	007Ch

Figure 14-33. OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-70. OSPI_INDIRECT_WRITE_XFER_NUM_BYTES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE_FLD	R/W	0h	Indirect Number of Bytes. This is the number of bytes that the indirect access will consume. This can be bigger than the configured size of SRAM.

14.36 OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG Register (Offset = 80h) [reset = 4h]

OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG is shown in [Figure 14-34](#) and described in [Table 14-72](#).

Return to [Summary Table](#).

Indirect Trigger Address Range Register.

This register allows the user to define the indirect trigger address range. If the configured range exceeds number of bytes programmed for particular indirect transfer, there is no need to detect indirect trigger address boundaries by software. This register should be setup before an indirect read transfer is triggered.

Table 14-71.
OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	0080h

Figure 14-34. OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG Register

31	30	29	28	27	26	25	24
IND_RANGE_RESV1_FLD							
R-0h							
23	22	21	20	19	18	17	16
IND_RANGE_RESV1_FLD							
R-0h							
15	14	13	12	11	10	9	8
IND_RANGE_RESV1_FLD							
R-0h							
7	6	5	4	3	2	1	0
IND_RANGE_RESV1_FLD				IND_RANGE_WIDTH_FLD			
R-0h				R/W-4h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-72. OSPI_INDIRECT_TRIGGER_ADDR_RANGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IND_RANGE_RESV1_FLD	R	0h	Reserved
3-0	IND_RANGE_WIDTH_FLD	R/W	4h	Indirect Range Width. This is the address offset of the OSPI_IND_AHB_ADDR_TRIGGER_REG. When any valid Indirect Access is triggered and data address fits to the range, the request is forwarded into Indirect Write Controller or Indirect Read Controller depending on which one was requested by valid trigger. The value is given as power of 2. The default one is $2^{**4} = 16$ what allows 16-byte bursts to be performed. This field reflects width of the range so number of locations of valid addresses (single location has 32 bits) ranges from Indirect Trigger Address to Indirect Trigger Address + [Indirect Range Width - 1].

14.37 OSPI_FLASH_COMMAND_CTRL_MEM_REG Register (Offset = 8Ch) [reset = 0h]

OSPI_FLASH_COMMAND_CTRL_MEM_REG is shown in [Figure 14-35](#) and described in [Table 14-74](#).

Return to [Summary Table](#).

Flash Command Control Memory Register.

This register controls the Memory Bank accesses. It also defines the number of bytes intended to get by STIG access configured to use the STIG Memory Bank.

Table 14-73.
OSPI_FLASH_COMMAND_CTRL_MEM_REG
Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	008Ch

Figure 14-35. OSPI_FLASH_COMMAND_CTRL_MEM_REG Register

31	30	29	28	27	26	25	24
FLASH_COMMAND_CTRL_MEM_RESV1_FLD				MEM_BANK_ADDR_FLD			
R-0h				R/W-0h			
23	22	21	20	19	18	17	16
MEM_BANK_ADDR_FLD				FLASH_COMMAND_CTRL_MEM_RESV2_FLD	NB_OF_STIG_READ_BYTES_FLD		
R/W-0h				R-0h	R/W-0h		
15	14	13	12	11	10	9	8
MEM_BANK_READ_DATA_FLD							
R-0h							
7	6	5	4	3	2	1	0
FLASH_COMMAND_CTRL_MEM_RESV3_FLD						MEM_BANK_REQ_IN_PROGRESS_FLD	TRIGGER_MEMORY_BANK_REQ_FLD
R-0h						R-0h	W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 14-74. OSPI_FLASH_COMMAND_CTRL_MEM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	FLASH_COMMAND_CTRL_MEM_RESV1_FLD	R	0h	Reserved
28-20	MEM_BANK_ADDR_FLD	R/W	0h	Memory Bank Address. The address of the Memory Bank which data will be read from. It is equivalent to the index value of the byte read by the last STIG access configured to work with STIG Memory Bank
19	FLASH_COMMAND_CTRL_MEM_RESV2_FLD	R	0h	Reserved

Table 14-74. OSPI_FLASH_COMMAND_CTRL_MEM_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-16	NB_OF_STIG_READ_BY TES_FLD	R/W	0h	Number of STIG Memory Bank Read Bytes. It defines the number of read bytes for the STIG configured to work with STIG Memory Bank as follows: 0h = 16 bytes 1h = 32 bytes 2h = 64 bytes 3h = 128 bytes 4h = 256 bytes 5h = 512 bytes others = unused
15-8	MEM_BANK_READ_DATA_FLD	R	0h	Memory Bank Read Data. Last requested data from the STIG Memory Bank.
7-2	FLASH_COMMAND_CTRL_MEM_RESV3_FLD	R	0h	Reserved
1	MEM_BANK_REQ_IN_PROGRESS_FLD	R	0h	Memory Bank data request in progress.
0	TRIGGER_MEM_BANK_REQ_FLD	W	0h	Trigger the Memory Bank data request.

14.38 OSPI_FLASH_CMD_CTRL_REG Register (Offset = 90h) [reset = 0h]

OSPI_FLASH_CMD_CTRL_REG is shown in [Figure 14-36](#) and described in [Table 14-76](#).

Return to [Summary Table](#).

Flash Command Control Register.

This register controls SPI transactions generated by STIG. It allows to define corresponding SPI frame to particular command, triggering the transfer and polling for its completion.

**Table 14-75. OSPI_FLASH_CMD_CTRL_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	0090h

Figure 14-36. OSPI_FLASH_CMD_CTRL_REG Register

31	30	29	28	27	26	25	24
CMD_OPCODE_FLD							
R/W-0h							
23	22	21	20	19	18	17	16
ENB_READ_D ATA_FLD	NUM_RD_DATA_BYTES_FLD			ENB_COMD_A DDR_FLD	ENB_MODE_BI T_FLD	NUM_ADDR_BYTES_FLD	
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
ENB_WRITE_D ATA_FLD	NUM_WR_DATA_BYTES_FLD			NUM_DUMMY_CYCLES_FLD			
R/W-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
NUM_DUMMY_ CYCLES_FLD	FLASH_CMD_CTRL_RESV1_FLD				STIG_MEM_BA NK_EN_FLD	CMD_EXEC_S TATUS_FLD	CMD_EXEC_F LD
R/W-0h	R-0h				R/W-0h	R-0h	W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 14-76. OSPI_FLASH_CMD_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CMD_OPCODE_FLD	R/W	0h	<p>Command Opcode.</p> <p>The command opcode field should be setup before triggering the command. For example, 20h maps to SubSector Erase. Writing to the execute OSPI_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD register launches the command.</p> <p>NOTE: Using this approach to issue commands to the device will make use of the instruction type of the device instruction configuration register.</p> <p>If this field is set to 0h, then the command opcode, command address, command dummy bytes and command data will all be transferred in a serial fashion.</p> <p>If this field is set to 1h, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0 and DQ1 pins.</p> <p>If this field is set to 2h, then the command opcode, command address, command dummy bytes and command data will all be transferred in parallel using DQ0, DQ1, DQ2 and DQ3 pins.</p>

Table 14-76. OSPI_FLASH_CMD_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ENB_READ_DATA_FLD	R/W	0h	Read Data Enable. Set to 1 if the command specified in the OSPI_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD requires read data bytes to be received from the device.
22-20	NUM_RD_DATA_BYTES_FLD	R/W	0h	Number of Read Data Bytes: Up to 8 data bytes may be read using this command Set to 0 for 1 byte and 7 for 8 bytes
19	ENB_COMD_ADDR_FLD	R/W	0h	Command Address Enable. Set to 1 if the command specified in OSPI_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD requires an address This should be setup before triggering the command via writing a 1 to the execute field.
18	ENB_MODE_BIT_FLD	R/W	0h	Mode Bit Enable: Set to 1 to ensure the mode bits as defined in the Mode Bit Configuration register are sent following the address bytes
17-16	NUM_ADDR_BYTES_FLD	R/W	0h	Number of Address Bytes. Set to the number of address bytes required [the address itself is programmed in the OSPI_FLASH_CMD_ADDR_REG. This should be setup before triggering the command via the OSPI_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD: 0h = 1 address byte 1h = 2 address bytes 2h = 3 address bytes 3h = 4 address bytes
15	ENB_WRITE_DATA_FLD	R/W	0h	Write Data Enable. Set to 1 if the command specified in the command opcode field requires write data bytes to be sent to the device.
14-12	NUM_WR_DATA_BYTES_FLD	R/W	0h	Number of Write Data Bytes. Up to 8 Data bytes may be written using this command. Set to 0 for 1 byte, 7 for 8 bytes.
11-7	NUM_DUMMY_CYCLES_FLD	R/W	0h	Number of Dummy cycles. Set to the number of dummy cycles required. This should be setup before triggering the command via the OSPI_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD.
6-3	FLASH_CMD_CTRL_RESV1_FLD	R	0h	Reserved
2	STIG_MEM_BANK_EN_FLD	R/W	0h	STIG Memory Bank enable bit. This should be setup before triggering the command via the OSPI_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD.
1	CMD_EXEC_STATUS_FLD	R	0h	Command execution in progress.
0	CMD_EXEC_FLD	W	0h	Execute the command.

14.39 OSPI_FLASH_CMD_ADDR_REG Register (Offset = 94h) [reset = 0h]

OSPI_FLASH_CMD_ADDR_REG is shown in [Figure 14-37](#) and described in [Table 14-78](#).

Return to [Summary Table](#).

Flash Command Address Register.

This register allows to define the address of the command using by the STIG controller. This register should be setup while the controller is idle.

**Table 14-77. OSPI_FLASH_CMD_ADDR_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	0094h

Figure 14-37. OSPI_FLASH_CMD_ADDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-78. OSPI_FLASH_CMD_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_FLD	R/W	0h	Command Address. This should be setup before triggering the command with execute field [bit 0] of the Flash Command Control register It is the address used by the command specified in the OSPI_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD bit field.

14.40 OSPI_FLASH_RD_DATA_LOWER_REG Register (Offset = A0h) [reset = 0h]

OSPI_FLASH_RD_DATA_LOWER_REG is shown in [Figure 14-38](#) and described in [Table 14-80](#).

Return to [Summary Table](#).

Flash Command Read Data Register (Lower).

This register keeps the last 4 bytes read by STIG SPI access.

Table 14-79. OSPI_FLASH_RD_DATA_LOWER_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00A0h

Figure 14-38. OSPI_FLASH_RD_DATA_LOWER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_FLD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 14-80. OSPI_FLASH_RD_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_FLD	R	0h	Command Read Data (Lower). This is the data that is returned by the flash device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.41 OSPI_FLASH_RD_DATA_UPPER_REG Register (Offset = A4h) [reset = 0h]

OSPI_FLASH_RD_DATA_UPPER_REG is shown in [Figure 14-39](#) and described in [Table 14-82](#).

Return to [Summary Table](#).

Flash Command Read Data Register (Upper).

This register keeps the last but 4 bytes read by STIG SPI access. This register in conjunction with the OSPI_FLASH_RD_DATA_LOWER_REG register enables the controller to keep 8 last bytes read from the Flash Device using STIG.

**Table 14-81. OSPI_FLASH_RD_DATA_UPPER_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	00A4h

Figure 14-39. OSPI_FLASH_RD_DATA_UPPER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_FLD																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 14-82. OSPI_FLASH_RD_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_FLD	R	0h	Command Read Data (Upper). This is the data that is returned by the FLASH device for any status or configuration read operation carried out by triggering the event in the control register. The register will be valid when the polling bit in the control register is low.

14.42 OSPI_FLASH_WR_DATA_LOWER_REG Register (Offset = A8h) [reset = 0h]

OSPI_FLASH_WR_DATA_LOWER_REG is shown in [Figure 14-40](#) and described in [Table 14-84](#).

Return to [Summary Table](#).

Flash Command Write Data Register (Lower).

This register takes the first 4 bytes to be written by STIG.

Table 14-83. OSPI_FLASH_WR_DATA_LOWER_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00A8h

Figure 14-40. OSPI_FLASH_WR_DATA_LOWER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-84. OSPI_FLASH_WR_DATA_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_FLD	R/W	0h	Command Write Data Lower Byte. This is the command write data lower byte. This should be setup before triggering the command with the OSPI_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD bit. It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the OSPI_FLASH_CMD_CTRL_REG register.

14.43 OSPI_FLASH_WR_DATA_UPPER_REG Register (Offset = ACh) [reset = 0h]

OSPI_FLASH_WR_DATA_UPPER_REG is shown in [Figure 14-41](#) and described in [Table 14-86](#).

Return to [Summary Table](#).

Flash Command Write Data Register (Upper).

This register takes the bytes ranging from 5 to 8 to be written by STIG.

**Table 14-85. OSPI_FLASH_WR_DATA_UPPER_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	00ACh

Figure 14-41. OSPI_FLASH_WR_DATA_UPPER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_FLD																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-86. OSPI_FLASH_WR_DATA_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_FLD	R/W	0h	Command Write Data Upper Byte. This is the command write data upper byte. This should be setup before triggering the command with the OSPI_FLASH_CMD_CTRL_REG[0] CMD_EXEC_FLD bitr It is the data that is to be written to the flash for any status or configuration write operation carried out by triggering the event in the OSPI_FLASH_CMD_CTRL_REG register.

14.44 OSPI_POLLING_FLASH_STATUS_REG Register (Offset = B0h) [reset = 0h]

OSPI_POLLING_FLASH_STATUS_REG is shown in [Figure 14-42](#) and described in [Table 14-88](#).

Return to [Summary Table](#).

Polling Flash Status Register.

This register provides auto-polling data. It acts as the extension for the OSPI_WRITE_COMPLETION_CTRL_REG register where full status is not available and any action can be taken only relying on the indication of single bit being polled for.

Table 14-87. OSPI_POLLING_FLASH_STATUS_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00B0h

Figure 14-42. OSPI_POLLING_FLASH_STATUS_REG Register

31	30	29	28	27	26	25	24
DEVICE_STATUS_RSVD_FLD2							
R-0h							
23	22	21	20	19	18	17	16
DEVICE_STATUS_RSVD_FLD2				DEVICE_STATUS_NB_DUMMY			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
DEVICE_STATUS_RSVD_FLD1							DEVICE_STAT US_VALID_FLD
R-0h							R-0h
7	6	5	4	3	2	1	0
DEVICE_STATUS_FLD							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-88. OSPI_POLLING_FLASH_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	DEVICE_STATUS_RSVD_FLD2	R	0h	Reserved
19-16	DEVICE_STATUS_NB_DUMMY	R/W	0h	Number of dummy cycles for auto-polling.
15-9	DEVICE_STATUS_RSVD_FLD1	R	0h	Reserved
8	DEVICE_STATUS_VALID_FLD	R	0h	Device Status Valid. This should be set when value in bits from 7 to 0 is valid.
7-0	DEVICE_STATUS_FLD	R	0h	Defines actual Status Register of Device.

14.45 OSPI_PHY_CONFIGURATION_REG Register (Offset = B4h) [reset = 40000000h]

OSPI_PHY_CONFIGURATION_REG is shown in [Figure 14-43](#) and described in [Table 14-90](#).

Return to [Summary Table](#).

PHY Configuration Register.

This register defines the configuration of PHY Module and controls the internal DLL. This register should be setup while the controller is idle.

Table 14-89. OSPI_PHY_CONFIGURATION_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00B4h

Figure 14-43. OSPI_PHY_CONFIGURATION_REG Register

31	30	29	28	27	26	25	24
PHY_CONFIG_RESYNC_FLD	PHY_CONFIG_RESET_FLD	PHY_CONFIG_RX_DLL_BYPASS_FLD	PHY_CONFIG_RESV2_FLD				
W-0h	W-1h	R/W-0h	R-0h				
23	22	21	20	19	18	17	16
PHY_CONFIG_RESV2_FLD	PHY_CONFIG_TX_DLL_DELAY_FLD						
R-0h	R/W-0h						
15	14	13	12	11	10	9	8
PHY_CONFIG_RESV1_FLD							
R-0h							
7	6	5	4	3	2	1	0
PHY_CONFIG_RESV1_FLD	PHY_CONFIG_RX_DLL_DELAY_FLD						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 14-90. OSPI_PHY_CONFIGURATION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PHY_CONFIG_RESYNC_FLD	W	0h	Re-synchronisation DLL. This bit is used for re-synchronisation delay lines to update them with values from TX DLL Delay and RX DLL Delay fields.
30	PHY_CONFIG_RESET_FLD	W	1h	DLL Reset. This bit is used for reset of Delay Lines by software.
29	PHY_CONFIG_RX_DLL_BYPASS_FLD	R/W	0h	RX DLL Bypass. This field determines if RX DLL is bypassed.
28-23	PHY_CONFIG_RESV2_FLD	R	0h	Reserved
22-16	PHY_CONFIG_TX_DLL_DELAY_FLD	R/W	0h	TX DLL Delay. This field determines the number of delay elements to insert on data path between RCLK and SCLK.
15-7	PHY_CONFIG_RESV1_FLD	R	0h	Reserved

Table 14-90. OSPI_PHY_CONFIGURATION_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	PHY_CONFIG_RX_DLL_DELAY_FLD	R/W	0h	RX DLL Delay. This field determines the number of delay elements to insert on data path between RCLK and sampling clock.

14.46 OSPI_PHY_MASTER_CONTROL_REG Register (Offset = B8h) [reset = 00800000h]

OSPI_PHY_MASTER_CONTROL_REG is shown in [Figure 14-44](#) and described in [Table 14-92](#).

Return to [Summary Table](#).

PHY DLL Master Control Register.

This register defines the configuration and control logic of DLL intended to work in DLL Master Mode.

**Table 14-91. OSPI_PHY_MASTER_CONTROL_REG
Instances**

Instance	Physical Address
FSS0_OSPI0_CTRL	00B8h

Figure 14-44. OSPI_PHY_MASTER_CONTROL_REG Register

31	30	29	28	27	26	25	24
PHY_MASTER_CONTROL_RESV3_FLD							PHY_MASTER_LOCK_MODE_FLD
R-0h							R/W-0h
23	22	21	20	19	18	17	16
PHY_MASTER_BYPASS_MODE_FLD	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD			PHY_MASTER_CONTROL_R_ESV2_FLD	PHY_MASTER_NB_INDICATIONS_FLD		
R/W-1h	R/W-0h			R-0h	R/W-0h		
15	14	13	12	11	10	9	8
PHY_MASTER_CONTROL_RESV1_FLD							
R-0h							
7	6	5	4	3	2	1	0
PHY_MASTER_CONTROL_R_ESV1_FLD	PHY_MASTER_INITIAL_DELAY_FLD						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-92. OSPI_PHY_MASTER_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	PHY_MASTER_CONTROL_RESV3_FLD	R	0h	Reserved
24	PHY_MASTER_LOCK_MODE_FLD	R/W	0h	Determines if the master delay line locks on a full cycle or half cycle of delay. This bit need not be written by software. If DLL does not lock in full cycle, it will automatically try to lock in half cycle mode. 0h = Full cycle of delay 1h = Half cycle of delay

Table 14-92. OSPI_PHY_MASTER_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	PHY_MASTER_BYPASS_MODE_FLD	R/W	1h	Controls the bypass mode of the master and slave DLLs. Controls the bypass mode of the master and slave DLLs. If this bit is set, the bypass mode is intended to be used only for debug. 0h = Master operational mode DLL works in normal mode of operation where the slave delay line settings are used as fractional delay of the master delay line encoder reading of the number of delays in one cycle. 1h = Bypass mode Master DLL is disabled with only 1 delay element in its delay line. The slave delay lines decode delays in absolute delay elements rather than as fractional delays. Delays are defined in OSPI_PHY_CONFIGURATION_REG[22-16] PHY_CONFIG_TX_DLL_DELAY_FLD and OSPI_PHY_CONFIGURATION_REG[6-0] PHY_CONFIG_RX_DLL_DELAY_FLD bit fields.
22-20	PHY_MASTER_PHASE_DETECT_SELECTOR_FLD	R/W	0h	Selects the number of delay elements to be inserted between the phase detect flip-flops. 0h = One delay element 1h = Two delay element 2h = Three delay element 3h = Four delay element 4h = Five delay element 5h = Six delay element 6h = Seven delay element 7h = Eight delay element
19	PHY_MASTER_CONTROL_RESV2_FLD	R	0h	Reserved
18-16	PHY_MASTER_NB_INDICATIONS_FLD	R/W	0h	Holds the number of consecutive increment or decrement indications.
15-7	PHY_MASTER_CONTROL_RESV1_FLD	R	0h	Reserved
6-0	PHY_MASTER_INITIAL_DELAY_FLD	R/W	0h	This value is the initial delay value for the Master DLL.

14.47 OSPI_DLL_OBSERVABLE_LOWER_REG Register (Offset = BCh) [reset = 0h]

OSPI_DLL_OBSERVABLE_LOWER_REG is shown in [Figure 14-45](#) and described in [Table 14-94](#).

Return to [Summary Table](#).

DLL Observable Register Lower.

This register allows to observe and debug DLL status.

Table 14-93.
OSPI_DLL_OBSERVABLE_LOWER_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00BCh

Figure 14-45. OSPI_DLL_OBSERVABLE_LOWER_REG Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD							
R-0h							
23	22	21	20	19	18	17	16
DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD							
R-0h							
15	14	13	12	11	10	9	8
DLL_OBSERVA BLE_LOWER_L OOPBACK_LO CK_FLD	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD						
R-0h	R-0h						
7	6	5	4	3	2	1	0
DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD					DLL_OBSERVABLE_LOWER_L OCK_MODE_FLD		DLL_OBSERVA BLE_LOWER DLL_LOCK_FL D
R-0h					R-0h		R-0h

LEGEND: R = Read Only; -n = value after reset

Table 14-94. OSPI_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DLL_OBSERVABLE_LOWER_DLL_LOCK_INC_FLD	R	0h	Holds the state of the cumulative lock incremental steps when the OSPI_DLL_OBSERVABLE_LOWER_REG[7-3] DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD of this parameter was triggered to increment or was last saturated at a value of 1Fh.
23-16	DLL_OBSERVABLE_LOWER_DLL_LOCK_DEC_FLD	R	0h	Holds the state of the cumulative lock decremental steps when the OSPI_DLL_OBSERVABLE_LOWER_REG[7-3] DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD of this parameter was triggered to decrement or was last saturated at a value of 1Fh.
15	DLL_OBSERVABLE_LOWER_LOOPBACK_LOCK_FLD	R	0h	This bit indicates that lock of loopback is done.
14-8	DLL_OBSERVABLE_LOWER_LOCK_VALUE_FLD	R	0h	DLL Lock Value. Reports the DLL encoder value from the master DLL to the slave DLLs.

Table 14-94. OSPI_DLL_OBSERVABLE_LOWER_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-3	DLL_OBSERVABLE_LOWER_UNLOCK_COUNTER_FLD	R	0h	DLL Unlock Counter. Reports the number of increments or decrements required for the master DLL to complete the locking process.
2-1	DLL_OBSERVABLE_LOWER_LOCK_MODE_FLD	R	0h	DLL Locked Mode. Defines the mode in which the DLL has achieved the lock: 0h = Full clock mode. The master delay line was long enough to lock on one full clock cycle of delay. 1h = Reserved. 2h = Half clock mode. The master delay line was not long enough to lock one full cycle of delay but could lock on a half- cycle of delay. 3h = Saturation mode. The master delay line was not long enough to lock on a full or a half clock cycle. In this mode, the encoder value is fixed at the maximum delay line setting and the master DLL will be disabled. The slave delay lines continue to use the fractional delays based upon the fixed saturation value of the delay line.
0	DLL_OBSERVABLE_LOWER_DLL_LOCK_FLD	R	0h	DLL Lock. Indicates status of DLL 0h = DLL has not locked 1h = DLL is locked

14.48 OSPI_DLL_OBSERVABLE_UPPER_REG Register (Offset = C0h) [reset = 0h]

OSPI_DLL_OBSERVABLE_UPPER_REG is shown in [Figure 14-46](#) and described in [Table 14-96](#).

Return to [Summary Table](#).

DLL Observable Register Upper.

This register allows to observe and debug DLL status.

Table 14-95.
OSPI_DLL_OBSERVABLE_UPPER_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00C0h

Figure 14-46. OSPI_DLL_OBSERVABLE_UPPER_REG Register

31	30	29	28	27	26	25	24
DLL_OBSERVABLE_UPPER_RESV2_FLD							
R-0h							
23	22	21	20	19	18	17	16
DLL_OBSERVABLE_UPPER_RESV2_FLD	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD						
R-0h	R-0h						
15	14	13	12	11	10	9	8
DLL_OBSERVABLE_UPPER_RESV1_FLD							
R-0h							
7	6	5	4	3	2	1	0
DLL_OBSERVABLE_UPPER_RESV1_FLD	DLL_OBSERVABLE_UPPER_RX_DECODER_OUTPUT_FLD						
R-0h	R-0h						

LEGEND: R = Read Only; -n = value after reset

Table 14-96. OSPI_DLL_OBSERVABLE_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	DLL_OBSERVABLE_UPPER_RESV2_FLD	R	0h	Reserved
22-16	DLL_OBSERVABLE_UPPER_TX_DECODER_OUTPUT_FLD	R	0h	TX DLL decoder output. Holds the encoded value for the TX delay line for this slice.
15-7	DLL_OBSERVABLE_UPPER_RESV1_FLD	R	0h	Reserved
6-0	DLL_OBSERVABLE_UPPER_RX_DECODER_OUTPUT_FLD	R	0h	RX DLL decoder output. Holds the encoded value for the RX delay line for this slice.

14.49 OSPI_OPCODE_EXT_LOWER_REG Register (Offset = E0h) [reset = 13EDFA00h]

OSPI_OPCODE_EXT_LOWER_REG is shown in [Figure 14-47](#) and described in [Table 14-98](#).

Return to [Summary Table](#).

Opcode Extension Register (Lower).

This register provides the supplementing opcodes for Dual Byte Opcode Mode activated by OSPI_CONFIG_REG[30] DUAL_BYTE_OPCODE_EN_FLD bit.

Table 14-97. OSPI_OPCODE_EXT_LOWER_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00E0h

Figure 14-47. OSPI_OPCODE_EXT_LOWER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EXT_READ_OPCODE_FLD								EXT_WRITE_OPCODE_FLD							
R/W-13h								R/W-EDh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXT_POLL_OPCODE_FLD								EXT_STIG_OPCODE_FLD							
R/W-FAh								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-98. OSPI_OPCODE_EXT_LOWER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	EXT_READ_OPCODE_FLD	R/W	13h	Supplement byte of any Read Opcoded defined in the OSPI_DEV_INSTR_RD_CONFIG_REG[7-0] RD_OPCODE_NON_XIP_FLD bit field.
23-16	EXT_WRITE_OPCODE_FLD	R/W	EDh	Supplement byte of any Write Opcode defined in the OSPI_DEV_INSTR_WR_CONFIG_REG[7-0] WR_OPCODE_FLD bit field.
15-8	EXT_POLL_OPCODE_FLD	R/W	FAh	Supplement byte of any Polling Opcode defined in the OSPI_WRITE_COMPLETION_CTRL_REG[7-0] OPCODE_FLD bit field.
7-0	EXT_STIG_OPCODE_FLD	R/W	0h	Supplement byte of any STIG Opcode defined in the OSPI_FLASH_CMD_CTRL_REG[31-24] CMD_OPCODE_FLD bit field.

14.50 OSPI_OPCODE_EXT_UPPER_REG Register (Offset = E4h) [reset = 06F90000h]

OSPI_OPCODE_EXT_UPPER_REG is shown in [Figure 14-48](#) and described in [Table 14-100](#).

Return to [Summary Table](#).

Opcode Extension Register (Upper).

This register provides the supplementing opcodes for Dual Byte Opcode Mode activated by OSPI_CONFIG_REG[30] DUAL_BYTE_OPCODE_EN_FLD bit.

Table 14-99. OSPI_OPCODE_EXT_UPPER_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00E4h

Figure 14-48. OSPI_OPCODE_EXT_UPPER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WEL_OPCODE_FLD								EXT_WEL_OPCODE_FLD							
R/W-6h								R/W-F9h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPCODE_EXT_UPPER_RESV1_FLD															
R-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-100. OSPI_OPCODE_EXT_UPPER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	WEL_OPCODE_FLD	R/W	6h	WEL Opcode byte 1. First byte of any WEL Opcode
23-16	EXT_WEL_OPCODE_FLD	R/W	F9h	WEL Opcode byte 2 (Optional). Supplement byte of any WEL Opcode
15-0	OPCODE_EXT_UPPER_RESV1_FLD	R	0h	Reserved

14.51 OSPI_MODULE_ID_REG Register (Offset = FCh) [reset = 03000300h]

OSPI_MODULE_ID_REG is shown in [Figure 14-49](#) and described in [Table 14-102](#).

Return to [Summary Table](#).

Module ID Register.

This register provides the IP release number and the configuration data.

Table 14-101. OSPI_MODULE_ID_REG Instances

Instance	Physical Address
FSS0_OSPI0_CTRL	00FCh

Figure 14-49. OSPI_MODULE_ID_REG Register

31	30	29	28	27	26	25	24
FIX_PATCH_FLD							
R-3h							
23	22	21	20	19	18	17	16
MODULE_ID_FLD							
R-3h							
15	14	13	12	11	10	9	8
MODULE_ID_FLD							
R-3h							
7	6	5	4	3	2	1	0
MODULE_ID_RESV_FLD						CONF_FLD	
R-0h						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 14-102. OSPI_MODULE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	FIX_PATCH_FLD	R	3h	Fix/path number related to revision described by 3 LSBs of this register
23-8	MODULE_ID_FLD	R	3h	Module/Revision ID number
7-2	MODULE_ID_RESV_FLD	R	0h	Reserved
1-0	CONF_FLD	R	0h	Configuration ID number: 0h = OCTAL + PHY Configuration 1h = OCTAL Configuration 2h = QUAD + PHY Configuration 3h = QUAD Configuration

14.52 OSPI_ECC_AGGR Registers

Table 14-104 lists the memory-mapped registers for the OSPI ECC Aggregator. All register offset addresses not listed in Table 14-104 should be considered as reserved locations and the register contents should not be modified.

Table 14-103. OSPI_ECC_AGGR Instances

Instance	Base Address
MCU_FSS0_OSPI0_ECC_AGGR	4706 8000h

Table 14-104. OSPI_ECC_AGGR Registers

Offset	Acronym	Register Name	MCU_FSS0_OSPI0_ECC_AGGR Physical Address
0h	OSPI_ECC_REV	Aggregator revision register	4706 8000h
8h	OSPI_ECC_VECTOR	ECC vector register	4706 8008h
Ch	OSPI_ECC_STAT	Miscellaneous status register	4706 800Ch
10h + formula	OSPI_RESERVED_SVBUS_Y	Reserved area for serial VBUS registers	4706 8010h + formula
3Ch	OSPI_ECC_SEC_EOI_REG	SEC end of interrupt register	4706 803Ch
40h	OSPI_ECC_SEC_STATUS_REG0	SEC interrupt status register 0	4706 8040h
80h	OSPI_ECC_SEC_ENABLE_SET_REG0	SEC interrupt enable set register 0	4706 8080h
C0h	OSPI_ECC_SEC_ENABLE_CLR_REG0	SEC interrupt enable clear register 0	4706 80C0h
13Ch	OSPI_ECC_DED_EOI_REG	DED end of interrupt register	4706 813Ch
140h	OSPI_ECC_DED_STATUS_REG0	DED interrupt status register 0	4706 8140h
180h	OSPI_ECC_DED_ENABLE_SET_REG0	DED interrupt enable set register 0	4706 8180h
1C0h	OSPI_ECC_DED_ENABLE_CLR_REG0	DED interrupt enable clear register 0	4706 81C0h
200h	OSPI_ECC_AGGR_ENABLE_SET	Aggregator interrupt enable set register	4706 8200h
204h	OSPI_ECC_AGGR_ENABLE_CLR	Aggregator interrupt enable clear register	4706 8204h
208h	OSPI_ECC_AGGR_STATUS_SET	Aggregator interrupt status set register	4706 8208h
20Ch	OSPI_ECC_AGGR_STATUS_CLR	Aggregator interrupt status clear register	4706 820Ch

14.53 OSPI_ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

OSPI_ECC_REV is shown in [Figure 14-50](#) and described in [Table 14-106](#).

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Revision parameters.

Table 14-105. OSPI_ECC_REV Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8000h

Figure 14-50. OSPI_ECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 14-106. OSPI_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

14.54 OSPI_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

OSPI_ECC_VECTOR is shown in [Figure 14-51](#) and described in [Table 14-108](#).

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ECC Vector Register.

Table 14-107. OSPI_ECC_VECTOR Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8008h

Figure 14-51. OSPI_ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 14-108. OSPI_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

14.55 OSPI_ECC_STAT Register (Offset = Ch) [reset = 1h]

OSPI_ECC_STAT is shown in [Figure 14-52](#) and described in [Table 14-110](#).

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Miscellaneous status register.

Table 14-109. OSPI_ECC_STAT Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	800Ch

Figure 14-52. OSPI_ECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RESERVED																					NUM_RAMs															
R-0h																					R-1h															

LEGEND: R = Read Only; -n = value after reset

Table 14-110. OSPI_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMs	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

14.56 OSPI_RESERVED_SVBUS_Y Register (Offset = 10h+formula) [reset = 0h]

OSPI_RESERVED_SVBUS_Y is shown in [Figure 14-53](#) and described in .

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Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

Table 14-111. OSPI_RESERVED_SVBUS_Y Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8010h + formula

Figure 14-53. OSPI_RESERVED_SVBUS_Y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-112. OSPI_RESERVED_SVBUS_Y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

14.57 OSPI_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

OSPI_ECC_SEC_EOI_REG is shown in [Figure 14-54](#) and described in [Table 14-114](#).

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EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-113. OSPI_ECC_SEC_EOI_REG Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	803Ch

Figure 14-54. OSPI_ECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 14-114. OSPI_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	EOI Register

14.58 OSPI_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

OSPI_ECC_SEC_STATUS_REG0 is shown in [Figure 14-55](#) and described in [Table 14-116](#).

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Interrupt Status Register 0.

**Table 14-115. OSPI_ECC_SEC_STATUS_REG0
Instances**

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8040h

Figure 14-55. OSPI_ECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 14-116. OSPI_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SRAM_PEND	R/W1S	0h	Interrupt Pending Status for sram_pend

14.59 OSPI_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

OSPI_ECC_SEC_ENABLE_SET_REG0 is shown in [Figure 14-56](#) and described in [Table 14-118](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0.

Table 14-117. OSPI_ECC_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8080h

Figure 14-56. OSPI_ECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABL E_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 14-118. OSPI_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for sram_pend

14.60 OSPI_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

OSPI_ECC_SEC_ENABLE_CLR_REG0 is shown in [Figure 14-57](#) and described in [Table 14-120](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0.

**Table 14-119. OSPI_ECC_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	80C0h

Figure 14-57. OSPI_ECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABL E_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 14-120. OSPI_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for sram_pend

14.61 OSPI_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

OSPI_ECC_DED_EOI_REG is shown in [Figure 14-58](#) and described in [Table 14-122](#).

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EOI Register.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 14-121. OSPI_ECC_DED_EOI_REG Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	813Ch

Figure 14-58. OSPI_ECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 14-122. OSPI_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	EOI Register

14.62 OSPI_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

OSPI_ECC_DED_STATUS_REG0 is shown in [Figure 14-59](#) and described in [Table 14-124](#).

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Interrupt Status Register 0.

**Table 14-123. OSPI_ECC_DED_STATUS_REG0
Instances**

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8140h

Figure 14-59. OSPI_ECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 14-124. OSPI_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SRAM_PEND	R/W1S	0h	Interrupt Pending Status for sram_pend.

14.63 OSPI_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

OSPI_ECC_DED_ENABLE_SET_REG0 is shown in [Figure 14-60](#) and described in [Table 14-126](#).

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Interrupt Enable Set Register 0.

Table 14-125. OSPI_ECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8180h

Figure 14-60. OSPI_ECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABL E_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 14-126. OSPI_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SRAM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for sram_pend.

14.64 OSPI_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

OSPI_ECC_DED_ENABLE_CLR_REG0 is shown in [Figure 14-61](#) and described in [Table 14-128](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0.

**Table 14-127. OSPI_ECC_DED_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	81C0h

Figure 14-61. OSPI_ECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SRAM_ENABL E_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 14-128. OSPI_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SRAM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for sram_pend.

14.65 OSPI_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

OSPI_ECC_AGGR_ENABLE_SET is shown in [Figure 14-62](#) and described in [Table 14-130](#).

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AGGR interrupt enable set register.

Table 14-129. OSPI_ECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8200h

Figure 14-62. OSPI_ECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 14-130. OSPI_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for svbus timeout errors.
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors.

14.66 OSPI_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

OSPI_ECC_AGGR_ENABLE_CLR is shown in [Figure 14-63](#) and described in [Table 14-132](#).

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AGGR interrupt enable clear register.

**Table 14-131. OSPI_ECC_AGGR_ENABLE_CLR
Instances**

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8204h

Figure 14-63. OSPI_ECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 14-132. OSPI_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for svbus timeout errors.
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors.

14.67 OSPI_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

OSPI_ECC_AGGR_STATUS_SET is shown in [Figure 14-64](#) and described in [Table 14-134](#).

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AGGR interrupt status set register.

Table 14-133. OSPI_ECC_AGGR_STATUS_SET Instances

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	8208h

Figure 14-64. OSPI_ECC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wincr-0h		R/Wincr-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 14-134. OSPI_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for svbus timeout errors.
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors.

14.68 OSPI_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

OSPI_ECC_AGGR_STATUS_CLR is shown in [Figure 14-65](#) and described in [Table 14-136](#).

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AGGR interrupt status clear register.

**Table 14-135. OSPI_ECC_AGGR_STATUS_CLR
Instances**

Instance	Physical Address
FSS0_OSPI0_ECC_AGGR	820Ch

Figure 14-65. OSPI_ECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 14-136. OSPI_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for svbus timeout errors.
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors.

15 HyperBus Registers

MCU_FSS0_HPBO_MC_MTR_y

15.1 HyperBus Subsystem Registers

Table 15-2 lists the memory-mapped registers for the HyperBus interface (MCU_FSS0_HPBO) Subsystem. All register offset addresses not listed in Table 15-2 should be considered as reserved locations and the register contents should not be modified.

Table 15-1. HyperBus Subsystem Instances

Instance	Base Address
MCU_FSS0_HPBO_SS_CFG	4703 0000h

Table 15-2. HyperBus Subsystem Registers

Offset	Acronym	Register Name	MCU_FSS0_HPBO_SS_CFG Physical Address
0h	MCU_FSS0_HPBO_SS_REVISION_REG	Revision Register	4703 0000h
4h	MCU_FSS0_HPBO_SS_DLL_STAT_REG	DLL Status Register	4703 0004h
8h	MCU_FSS0_HPBO_SS_RAM_STAT_REG	RAM Status Register	4703 0008h

15.2 MCU_FSS0_HPBO_SS_REVISION_REG Register (Offset = 0h) [reset = 6860D900h]

MCU_FSS0_HPBO_SS_REVISION_REG is shown in [Figure 15-1](#) and described in [Table 15-4](#).

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Revision Register

The Revision Register contains the major and minor revisions for the module.

Table 15-3. MCU_FSS0_HPBO_SS_REVISION_REG Instances

Instance	Physical Address
MCU_FSS0_HPBO_SS_CFG	4703 0000h

Figure 15-1. MCU_FSS0_HPBO_SS_REVISION_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-6860h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM				REVMIN			
R-1Bh				R-1h				R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 15-4. MCU_FSS0_HPBO_SS_REVISION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	6860h	Module ID
15-11	REVRTL	R	1Bh	RTL Revision
10-8	REVMAJ	R	1h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	0h	Minor Revision

15.3 MCU_FSS0_HPB0_SS_DLL_STAT_REG Register (Offset = 4h) [reset = 0h]

MCU_FSS0_HPB0_SS_DLL_STAT_REG is shown in [Figure 15-2](#) and described in [Table 15-6](#).

Return to [Summary Table](#).

DLL Status Register

**Table 15-5. MCU_FSS0_HPB0_SS_DLL_STAT_REG
Instances**

Instance	Physical Address
MCU_FSS0_HPB_SS_CFG	4703 0004h

Figure 15-2. MCU_FSS0_HPB0_SS_DLL_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					MDLL_CODE		
R-0h					R-0h		
7	6	5	4	3	2	1	0
MDLL_CODE						SDL_LOCK	MDLL_LOCK
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-6. MCU_FSS0_HPB0_SS_DLL_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-2	MDLL_CODE	R	0h	MDLL Code The slave delay line length that is currently enabled is determined by the MDLL Code value.
1	SDL_LOCK	R	0h	MDLL Code Valid
0	MDLL_LOCK	R	0h	MDLL Lock When this bit is set, it indicates that the master delay line in the MDLL is locked.

15.4 MCU_FSS0_HPB0_SS_RAM_STAT_REG Register (Offset = 8h) [reset = 0h]

MCU_FSS0_HPB0_SS_RAM_STAT_REG is shown in [Figure 15-3](#) and described in [Table 15-8](#).

Return to [Summary Table](#).

RAM Status Register

Table 15-7. MCU_FSS0_HPB0_SS_RAM_STAT_REG Instances

Instance	Physical Address
MCU_FSS0_HPB_SS_CFG	4703 0008h

Figure 15-3. MCU_FSS0_HPB0_SS_RAM_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							INIT_DONE
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-8. MCU_FSS0_HPB0_SS_RAM_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	INIT_DONE	R	0h	FIFO RAM Initialization Done When this bit is set, it indicates that all the FIFO RAM auto initialization is complete. Software should check that this bit is set before initiating transactions to the external memory.

15.5 HyperBus Memory Controller Registers

Table 15-10 lists the memory-mapped registers for the HyperBus interface (MCU_FSS0_HPBO) Memory Controller. All register offset addresses not listed in Table 15-10 should be considered as reserved locations and the register contents should not be modified.

Table 15-9. HyperBus Memory Controller Instances

Instance	Base Address
MCU_FSS0_HPBO_CTRL	4703 4000h

Table 15-10. HyperBus Memory Controller Registers

Offset	Acronym	Register Name	MCU_FSS0_HPBO_CTRL Physical Address
0h	MCU_FSS0_HPBO_MC_CSR	Controller Status Register	4703 4000h
4h	MCU_FSS0_HPBO_MC_IER	Interrupt Enable Register	4703 4004h
8h	MCU_FSS0_HPBO_MC_ISR	Interrupt Status Register	4703 4008h
10h + formula	MCU_FSS0_HPBO_MC_MBAR_y	Memory Base Address Register	4703 4010h to 4703 4014h
20h + formula	MCU_FSS0_HPBO_MC_MCR_y	Memory Configuration Register	4703 4020h to 4703 4024h
30h + formula	MCU_FSS0_HPBO_MC_MTR_y	Memory Timing Register	4703 4030h to 4703 4034h
40h	MCU_FSS0_HPBO_MC_GPOR	General Purpose Output Register ⁽¹⁾	4703 4040h
44h	MCU_FSS0_HPBO_MC_WPR	Write Protection Register	4703 4044h
48h	MCU_FSS0_HPBO_MC_LBR	Loop Back Register	4703 4048h

(1) General Purpose Output register (MCU_FSS0_HPBO_MC_GPOR) of the HBMC is not used (see *HyperBus Not Supported Features*).

15.6 MCU_FSS0_HPB0_MC_CSR Register (Offset = 0h) [reset = 0h]

MCU_FSS0_HPB0_MC_CSR is shown in [Figure 15-4](#) and described in [Table 15-12](#).

Return to [Summary Table](#).

Controller Status Register

The Controller Status Register is used to access the internal status of the HBMC.

Table 15-11. MCU_FSS0_HPB0_MC_CSR Instances

Instance	Physical Address
MCU_FSS0_HPB_CTRL	4703 4000h

Figure 15-4. MCU_FSS0_HPB0_MC_CSR Register

31	30	29	28	27	26	25	24
RESERVED					WRSTOERR	WTRSERR	WDECERR
R-0h					R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
RESERVED							WACT
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED				RDSSTALL	RRSTOERR	RTRSERR	RDECERR
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED							RACT
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-12. MCU_FSS0_HPB0_MC_CSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26	WRSTOERR	R	0h	Write RSTO Error This bit indicates whether HyperBus memory is under reset state in the latest write operation. When this bit is set, HBMC responds by AXI SLVERR. 0h = Normal operation 1h = HyperBus memory is under reset
25	WTRSERR	R	0h	Write Transaction Error This bit indicates whether AXI protocol is acceptable by HBMC in the latest write transaction. When this bit is set, HBMC responds by AXI SLVERR. 0h = Normal operation 1h = This protocol is not supported
24	WDECERR	R	0h	Write Decode Error This bit indicates whether access address is acceptable in the latest write transaction. When this bit is set, HBMC responds by AXI DECERR. 0h = Normal operation 1h = Access address is not reachable
23-17	RESERVED	R	0h	Reserved

Table 15-12. MCU_FSS0_HPBO_MC_CSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	WACT	R	0h	Write Active This bit indicates whether write transaction is in progress or not. When receiving write request on write address channel, this bit becomes 1h. When retrieving response signaling on write response channel, this bit becomes 0h. 0h = Write is idle 1h = Write is active
15-12	RESERVED	R	0h	Reserved
11	RDSSTALL	R	0h	RDS Stall This bit indicates whether read data transfer from HyperBus memory is stalled (RDS Stall remains LOW) in the latest read transaction. When this bit is set, HBMC responds by AXI SLVERR. 0h = Normal operation 1h = RDS is stalled
10	RRSTOERR	R	0h	Read RSTO Error This bit indicates whether HyperBus memory is under reset state in the latest read operation. When this bit is set, HBMC responds by AXI SLVERR. 0h = Normal operation 1h = HyperBus memory is under reset
9	RTRSERR	R	0h	Read Transaction Error This bit indicates whether AXI protocol is acceptable by HBMC in the latest read transaction. When this bit is set, HBMC responds by AXI SLVERR. 0h = Normal operation 1h = This protocol is not supported
8	RDECERR	R	0h	Read Decode Error This bit indicates whether access address is acceptable in the latest read transaction. When this bit is set, HBMC responds by AXI DECERR. 0h = Normal operation 1h = Access address is not reachable
7-1	RESERVED	R	0h	Reserved
0	RACT	R	0h	Read Active This bit indicates whether read transaction is in progress or not. When receiving read request on read address channel, this bit becomes 1h. When retrieving all requested data on read data channel, this bit becomes 0h. 0h = Read is idle 1h = Read is active

15.7 MCU_FSS0_HPBO_MC_IER Register (Offset = 4h) [reset = 0h]

MCU_FSS0_HPBO_MC_IER is shown in [Figure 15-5](#) and described in [Table 15-14](#).

Return to [Summary Table](#).

Interrupt Enable Register

The HBMC outputs optional interrupt signal by condition enabled by the Interrupt Enable Register.

Table 15-13. MCU_FSS0_HPBO_MC_IER Instances

Instance	Physical Address
MCU_FSS0_HPBO_CTRL	4703 4004h

Figure 15-5. MCU_FSS0_HPBO_MC_IER Register

31	30	29	28	27	26	25	24
INTP	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RPCINTE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-14. MCU_FSS0_HPBO_MC_IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INTP	R/W	0h	Interrupt Polarity Control This bit is used to choose the polarity of optional interrupt signal (IENOn). 0h = IENOn signal is active low 1h = IENOn signal is active high (Reversed mode)
30-1	RESERVED	R	0h	Reserved
0	RPCINTE	R/W	0h	HyperBus Memory Interrupt Enable 0h = Disable interrupt 1h = Enable interrupt by INT# signal of HyperBus memory

15.8 MCU_FSS0_HPBO_MC_ISR Register (Offset = 8h) [reset = 0h]

MCU_FSS0_HPBO_MC_ISR is shown in [Figure 15-6](#) and described in [Table 15-16](#).

Return to [Summary Table](#).

Interrupt Status Register

The Interrupt Status Register is used to read the status for the interrupts generated.

Table 15-15. MCU_FSS0_HPBO_MC_ISR Instances

Instance	Physical Address
MCU_FSS0_HPBO_CTRL	4703 4008h

Figure 15-6. MCU_FSS0_HPBO_MC_ISR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RPCINTS
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 15-16. MCU_FSS0_HPBO_MC_ISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RPCINTS	R	0h	HyperBus Memory Interrupt 0h = No interrupt 1h = This bit displays interrupt from INT# signal of HyperBus memory

15.9 MCU_FSS0_HPBO_MC_MBAR_y Register (Offset = 10h + formula) [reset = 0h]

MCU_FSS0_HPBO_MC_MBAR_y is shown in [Figure 15-7](#) and described in [Table 15-18](#).

Return to [Summary Table](#).

Memory Base Address Register

for device connected to CS#

The base address of addressable region to Hyperflash memory can be set-up using this register. The controller can't assert two chip selects CS0# and CS1# at a time. Hence this register describes how to select chip select.

Offset = 10h + (y × 4h); where y = 0h to 1h

Table 15-17. MCU_FSS0_HPBO_MC_MBAR_y Instances

Instance	Physical Address
MCU_FSS0_HPBO_CTRL	4703 4010h to 4703 4014h

Figure 15-7. MCU_FSS0_HPBO_MC_MBAR_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A_MSB								A_LSB																							
R/W-0h								R-0h																							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-18. MCU_FSS0_HPBO_MC_MBAR_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	A_MSB	R/W	0h	MSB 8 bit of the base address of addressable region to HyperBus memory
23-0	A_LSB	R	0h	Since register can be set in 16 MB boundary, lower 24 bit is fixed to 0h, if read, this field will always return 0h.

15.10 MCU_FSS0_HPBO_MC_MCR_y Register (Offset = 20h + formula) [reset = 3h]

MCU_FSS0_HPBO_MC_MCR_y is shown in [Figure 15-8](#) and described in [Table 15-20](#).

Return to [Summary Table](#).

Memory Configuration Register

for CS#

Offset = 20h + (y × 4h); where y = 0h to 1h

**Table 15-19. MCU_FSS0_HPBO_MC_MCR_y
Instances**

Instance	Physical Address
MCU_FSS0_HPBO_CTRL	4703 4020h to 4703 4024h

Figure 15-8. MCU_FSS0_HPBO_MC_MCR_y Register

31	30	29	28	27	26	25	24
MAXEN	RESERVED					MAXLEN	
R/W-0h		R-0h				R/W-0h	
23	22	21	20	19	18	17	16
MAXLEN						TCMO	ACS
R/W-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		CRT	DEVTYPE	RESERVED		WRAPSIZE	
R-0h		R/W-0h	R/W-0h	R-0h		R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-20. MCU_FSS0_HPBO_MC_MCR_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MAXEN	R/W	0h	Maximum Length Enable When this bit is set to 1h, CS# low time can be configurable by MAXLEN bit. 0h = No configurable CS# low time 1h = Configurable CS# low time
30-27	RESERVED	R	0h	Reserved
26-18	MAXLEN	R/W	0h	Maximum Length This bit indicates maximum read/write transaction length to memory. This bit is ignored when MAXEN bit is 0h. 0h = 2 Byte (1 HyperBus CK) 1h = 4 Byte (2 HyperBus CK) 2h = 6 Byte (3 HyperBus CK) 1FFh = 1024 Byte (512 HyperBus CK)

Table 15-20. MCU_FSS0_HPBO_MC_MCR_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	TCMO	R/W	0h	True Continuous Merge Option Note that this function can be used with the HyperFlash with specific function. Please confirm whether it is available on the corresponding HyperFlash before enabling this function. When HyperBus memory doesn't accept the 8-bit boundary address, and a wrapping burst access with ARSIZE = 0h and ARADDR0 = 1h is used, this bit must not be set to 1h. 0h = No merging WRAP and INCR 1h = Merging WRAP and INCR
16	ACS	R/W	0h	Asymmetry Cache Support This function should be disabled if the HyperBus memory itself supports the asymmetry cache system. 0h = No asymmetry cache system support 1h = Asymmetry cache system support
15-6	RESERVED	R	0h	Reserved
5	CRT	R/W	0h	Configuration Register Target This bit indicates whether the read or write operation accesses the memory or CR space. This bit is mapped to CA-46 bit in HyperRAM. When using HyperFlash, this bit should be set to 0h. 0h = Memory space 1h = CR space
4	DEVTYPE	R/W	0h	Device Type Device type for control target. 0h = HyperFlash 1h = HyperRAM
3-2	RESERVED	R	0h	Reserved
1-0	WRAPSIZE	R/W	3h	Wrap Size The wrap burst length of HyperBus memory. This bit is ignored when the asymmetry cache support bit is 0h. When the asymmetry cache support is 1h, this bit should be set the same as wrap size of configuration register in HyperBus memory. 0h = Reserved 1h = 64 Bytes 2h = 16 Bytes 3h = 32 Bytes

15.11 MCU_FSS0_HPB0_MC_MTR_y Register (Offset = 30h + formula) [reset = 1h]

MCU_FSS0_HPB0_MC_MTR_y is shown in [Figure 15-9](#) and described in [Table 15-22](#).

Return to [Summary Table](#).

Memory Timing Register

Memory access timings for CS# can be configured using the Memory Timing Register.

Offset = 30h + (y × 4h); where y = 0h to 1h

**Table 15-21. MCU_FSS0_HPB0_MC_MTR_y
Instances**

Instance	Physical Address
MCU_FSS0_HPB_CTRL	4703 4030h to 4703 4034h

Figure 15-9. MCU_FSS0_HPB0_MC_MTR_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RCSHI				WCSHI				RCSS				WCSS			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCSH				WCSH				RESERVED				LTCY			
R/W-0h				R/W-0h				R-0h				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-22. MCU_FSS0_HPB0_MC_MTR_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RCSHI	R/W	0h	Read Chip Select High Between Operations This bit indicates CS# high time for read between operations. 0h = corresponds to 1.5 clock cycle Fh = corresponds to 16.5 clock cycle
27-24	WCSHI	R/W	0h	Write Chip Select High Between Operations This bit indicates CS# high time for write between operations. 0h = corresponds to 1.5 clock cycle Fh = corresponds to 16.5 clock cycle
23-20	RCSS	R/W	0h	Read Chip Select Setup to next CK rising edge This bit indicates CS# setup time for read from CS# assertion. 0h = corresponds to 1 clock cycle Fh = corresponds to 16 clock cycle
19-16	WCSS	R/W	0h	Write Chip Select Setup to next CK rising edge This bit indicates CS# setup time for write from CS# assertion. 0h = corresponds to 1 clock cycle Fh = corresponds to 16 clock cycle
15-12	RCSH	R/W	0h	NOTE: This field should be set to a value of 1h Read Chip Select Hold after CK falling edge This bit indicates CS# hold time for read to CS# de-assertion. 1h = corresponds to 2 clock cycles
11-8	WCSH	R/W	0h	Write Chip Select Hold after CK falling edge This bit indicates CS# hold time for write to CS# de-assertion. 0h = corresponds to 1 clock cycle Fh = corresponding to 16 clock cycle
7-4	RESERVED	R	0h	Reserved

Table 15-22. MCU_FSS0_HPBO_MC_MTR_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	LTCY	R/W	1h	<p>Latency Cycle Only uses in HyperRAM</p> <p>This bit indicates initial latency code for read/write access. This bit is ignored when the MCU_FSS0_HPBO_MC_MCR_y[4] DEVTYPE is 0h (HyperFlash).</p> <p>0h = 5 clock latency 1h = 6 clock latency 2h = Reserved Dh = Reserved Eh = 3 clock latency Fh = 4 clock latency</p>

15.12 MCU_FSS0_HPBO_MC_GPOR Register (Offset = 40h) [reset = 0h]

MCU_FSS0_HPBO_MC_GPOR is shown in [Figure 15-10](#) and described in [Table 15-24](#).

Return to [Summary Table](#).

General Purpose Output Register

Output signal polarity can be configured using the General Purpose Output Register.

Note

General Purpose Output register (MCU_FSS0_HPBO_MC_GPOR) of the HBMC is not used (see *HyperBus Not Supported Features*).

**Table 15-23. MCU_FSS0_HPBO_MC_GPOR
Instances**

Instance	Physical Address
MCU_FSS0_HPBO_CTRL	4703 4040h

Figure 15-10. MCU_FSS0_HPBO_MC_GPOR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														GPO	
R-0h														R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-24. MCU_FSS0_HPBO_MC_GPOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	GPO	R/W	0h	General Purpose Output Interface 0h = Output signal polarity is LOW 1h = Output signal polarity is HIGH

15.13 MCU_FSS0_HPB0_MC_WPR Register (Offset = 44h) [reset = 0h]

MCU_FSS0_HPB0_MC_WPR is shown in [Figure 15-11](#) and described in [Table 15-26](#).

Return to [Summary Table](#).

Write Protection Register

Write protection can be configured using the Write Protection Register.

Note

WPn pin is not used on Cypress flash devices (see).

Table 15-25. MCU_FSS0_HPB0_MC_WPR Instances

Instance	Physical Address
MCU_FSS0_HPB_CTRL	4703 4044h

Figure 15-11. MCU_FSS0_HPB0_MC_WPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															WP
R-0h															R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-26. MCU_FSS0_HPB0_MC_WPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	WP	R/W	0h	Write Protection Control 0h = Not Protected WP# signal is HIGH 1h = Protected WP# signal is LOW

15.14 MCU_FSS0_HPBO_MC_LBR Register (Offset = 48h) [reset = 0h]

MCU_FSS0_HPBO_MC_LBR is shown in [Figure 15-12](#) and described in [Table 15-28](#).

Return to [Summary Table](#).

Loop Back Register

Loopback settings can be configured using the Loop Back Register.

Table 15-27. MCU_FSS0_HPBO_MC_LBR Instances

Instance	Physical Address
MCU_FSS0_HPBO_CTRL	4703 4048h

Figure 15-12. MCU_FSS0_HPBO_MC_LBR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							LOOPBACK
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-28. MCU_FSS0_HPBO_MC_LBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	LOOPBACK	R/W	0h	The write transaction data written on AXI bus is looped back as the read data from RPC bus. The loop-back is performed between WDAT FIFO and RDAT FIFO in AXI interface controller. 0h = Disable loopback 1h = Enable loopback

15.15 HyperBus ECC Aggregator Registers

Table 15-30 lists the memory-mapped registers for the HyperBus interface (MCU_FSS0_HPBO) ECC Aggregator. All register offset addresses not listed in Table 15-30 should be considered as reserved locations and the register contents should not be modified.

Table 15-29. HyperBus ECC Aggregator Instances

Instance	Base Address
MCU_FSS0_HPBO_ECC_AGGR	4706 0000h

Table 15-30. HyperBus ECC Aggregator Registers

Offset	Acronym	Register Name	MCU_FSS0_HPBO_ECC_AGGR Physical Address
0h	MCU_FSS0_HPBO_ECC_REV	Aggregator Revision Register	4706 0000h
8h	MCU_FSS0_HPBO_ECC_VECTOR	ECC Vector Register	4706 0008h
Ch	MCU_FSS0_HPBO_ECC_STAT	Misc Status Register	4706 000Ch
3Ch	MCU_FSS0_HPBO_ECC_SEC_EOI_REG	SEC End Of Interrupt (EOI) Register	4706 003Ch
40h	MCU_FSS0_HPBO_ECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	4706 0040h
80h	MCU_FSS0_HPBO_ECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	4706 0080h
C0h	MCU_FSS0_HPBO_ECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	4706 00C0h
13Ch	MCU_FSS0_HPBO_ECC_DED_EOI_REG	DED End Of Interrupt (EOI) Register	4706 013Ch
140h	MCU_FSS0_HPBO_ECC_DED_STATUS_REG0	DED Interrupt Status Register 0	4706 0140h
180h	MCU_FSS0_HPBO_ECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	4706 0180h
1C0h	MCU_FSS0_HPBO_ECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	4706 01C0h
200h	MCU_FSS0_HPBO_ECC_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	4706 0200h
204h	MCU_FSS0_HPBO_ECC_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	4706 0204h
208h	MCU_FSS0_HPBO_ECC_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	4706 0208h
20Ch	MCU_FSS0_HPBO_ECC_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	4706 020Ch

15.16 MCU_FSS0_HPB0_ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MCU_FSS0_HPB0_ECC_REV is shown in [Figure 15-13](#) and described in [Table 15-32](#).

Return to [Summary Table](#).

Aggregator Revision Register

Revision parameters.

Table 15-31. MCU_FSS0_HPB0_ECC_REV Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0000h

Figure 15-13. MCU_FSS0_HPB0_ECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
R-1Dh				R-2h				R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 15-32. MCU_FSS0_HPB0_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

15.17 MCU_FSS0_HPB0_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

MCU_FSS0_HPB0_ECC_VECTOR is shown in [Figure 15-14](#) and described in [Table 15-34](#).

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ECC Vector Register

Table 15-33. MCU_FSS0_HPB0_ECC_VECTOR Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0008h

Figure 15-14. MCU_FSS0_HPB0_ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-34. MCU_FSS0_HPB0_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

15.18 MCU_FSS0_HPB0_ECC_STAT Register (Offset = Ch) [reset = Fh]

MCU_FSS0_HPB0_ECC_STAT is shown in [Figure 15-15](#) and described in [Table 15-36](#).

Return to [Summary Table](#).

Misc Status Register

**Table 15-35. MCU_FSS0_HPB0_ECC_STAT
Instances**

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 000Ch

Figure 15-15. MCU_FSS0_HPB0_ECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																					NUM_RAMs																
R-0h																					R-Fh																

LEGEND: R = Read Only; -n = value after reset

Table 15-36. MCU_FSS0_HPB0_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMs	R	Fh	Number of RAMs Indicates the number of RAMs serviced by the ECC Aggregator.

15.19 MCU_FSS0_HPBO_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = Fh]

MCU_FSS0_HPBO_ECC_SEC_EOI_REG is shown in [Figure 15-16](#) and described in [Table 15-38](#).

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End Of Interrupt (EOI) Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 15-37. MCU_FSS0_HPBO_ECC_SEC_EOI_REG
Instances**

Instance	Physical Address
MCU_FSS0_HPBO_ECC_AGGR	4706 003Ch

Figure 15-16. MCU_FSS0_HPBO_ECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-38. MCU_FSS0_HPBO_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	EOI

15.20 MCU_FSS0_HPB0_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MCU_FSS0_HPB0_ECC_SEC_STATUS_REG0 is shown in [Figure 15-17](#) and described in [Table 15-40](#).

Return to [Summary Table](#).

SEC Interrupt Status Register 0

Table 15-39.
MCU_FSS0_HPB0_ECC_SEC_STATUS_REG0
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0040h

Figure 15-17. MCU_FSS0_HPB0_ECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIF FO_PEND	MEM_AR_FIF FO_PEND	MEM_AWID1_F IFO_PEND	MEM_WID1_FIF FO_PEND	MEM_AW1_FIF O_PEND	MEM_AWID0_F IFO_PEND	MEM_WID0_FIF FO_PEND
R-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
MEM_AW0_FIF O_PEND	MEM_RX_FIF FO_PEND	MEM_RDAT_FIF FO_PEND	MEM_BDAT1_F IFO_PEND	MEM_BDAT0_F IFO_PEND	MEM_WDAT1_F FIFO_PEND	MEM_WDAT0_F FIFO_PEND	MEM_ADR_FIF O_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-40. MCU_FSS0_HPB0_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MEM_ARID_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_arid_fifo_pend
13	MEM_AR_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_PEN D	R/W1S	0h	Interrupt Pending Status for mem_awid1_fifo_pend
11	MEM_WID1_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_PEN D	R/W1S	0h	Interrupt Pending Status for mem_awid0_fifo_pend
8	MEM_WID0_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_aw0_fifo_pend
6	MEM_RX_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_rx_fifo_pend
5	MEM_RDAT_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_PEN D	R/W1S	0h	Interrupt Pending Status for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_PEN D	R/W1S	0h	Interrupt Pending Status for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_PEN D	R/W1S	0h	Interrupt Pending Status for mem_wdat1_fifo_pend

Table 15-40. MCU_FSS0_HPBO_ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MEM_WDAT0_FIFO_PEN D	R/W1S	0h	Interrupt Pending Status for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_adr_fifo_pend

15.21 MCU_FSS0_HPB0_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MCU_FSS0_HPB0_ECC_SEC_ENABLE_SET_REG0 is shown in [Figure 15-18](#) and described in [Table 15-42](#).

Return to [Summary Table](#).

SEC Interrupt Enable Set Register 0

Table 15-41.
MCU_FSS0_HPB0_ECC_SEC_ENABLE_SET_REG0
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0080h

Figure 15-18. MCU_FSS0_HPB0_ECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIFO_ENABLE_SET	MEM_AR_FIFO_ENABLE_SET	MEM_AWID1_FIFO_ENABLE_SET	MEM_WID1_FIFO_ENABLE_SET	MEM_AW1_FIFO_ENABLE_SET	MEM_AWID0_FIFO_ENABLE_SET	MEM_WID0_FIFO_ENABLE_SET
R-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
MEM_AW0_FIFO_ENABLE_SET	MEM_RX_FIFO_ENABLE_SET	MEM_RDAT_FIFO_ENABLE_SET	MEM_BDAT1_FIFO_ENABLE_SET	MEM_BDAT0_FIFO_ENABLE_SET	MEM_WDAT1_FIFO_ENABLE_SET	MEM_WDAT0_FIFO_ENABLE_SET	MEM_ADR_FIFO_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-42. MCU_FSS0_HPB0_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MEM_ARID_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_arid_fifo_pend
13	MEM_AR_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_avid1_fifo_pend
11	MEM_WID1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_avid0_fifo_pend
8	MEM_WID0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_aw0_fifo_pend
6	MEM_RX_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_rx_fifo_pend

Table 15-42. MCU_FSS0_HPBO_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MEM_RDAT_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_wdat1_fifo_pend
1	MEM_WDAT0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_adr_fifo_pend

15.22 MCU_FSS0_HPB0_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MCU_FSS0_HPB0_ECC_SEC_ENABLE_CLR_REG0 is shown in [Figure 15-19](#) and described in [Table 15-44](#).

Return to [Summary Table](#).

SEC Interrupt Enable Clear Register 0

Table 15-43.
MCU_FSS0_HPB0_ECC_SEC_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 00C0h

Figure 15-19. MCU_FSS0_HPB0_ECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIF O_ENABLE_CLR	MEM_AR_FIFO _ENABLE_CLR	MEM_AWID1_FIF O_ENABLE_CLR	MEM_WID1_FIF O_ENABLE_CLR	MEM_AW1_FIF O_ENABLE_CLR	MEM_AWID0_FIF O_ENABLE_CLR	MEM_WID0_FIF O_ENABLE_CLR
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
MEM_AW0_FIF O_ENABLE_CLR	MEM_RX_FIFO _ENABLE_CLR	MEM_RDAT_FIF O_ENABLE_CLR	MEM_BDAT1_FIF O_ENABLE_CLR	MEM_BDAT0_FIF O_ENABLE_CLR	MEM_WDAT1_FIF O_ENABLE_CLR	MEM_WDAT0_FIF O_ENABLE_CLR	MEM_ADR_FIF O_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-44. MCU_FSS0_HPB0_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MEM_ARID_FIFO_ENAB LE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_arid_fifo_pend
13	MEM_AR_FIFO_ENABLE _CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_avid1_fifo_pend
11	MEM_WID1_FIFO_ENAB LE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_ENABL E_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_avid0_fifo_pend
8	MEM_WID0_FIFO_ENAB LE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_ENABL E_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_aw0_fifo_pend
6	MEM_RX_FIFO_ENABLE _CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_rx_fifo_pend

Table 15-44. MCU_FSS0_HPBO_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MEM_RDAT_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_wdat1_fifo_pend
1	MEM_WDAT0_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_adr_fifo_pend

15.23 MCU_FSS0_HPBO_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MCU_FSS0_HPBO_ECC_DED_EOI_REG is shown in [Figure 15-20](#) and described in [Table 15-46](#).

Return to [Summary Table](#).

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 15-45. MCU_FSS0_HPBO_ECC_DED_EOI_REG
Instances**

Instance	Physical Address
MCU_FSS0_HPBO_ECC_AGGR	4706 013Ch

Figure 15-20. MCU_FSS0_HPBO_ECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-46. MCU_FSS0_HPBO_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	EOI

15.24 MCU_FSS0_HPB0_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MCU_FSS0_HPB0_ECC_DED_STATUS_REG0 is shown in [Figure 15-21](#) and described in [Table 15-48](#).

Return to [Summary Table](#).

DED Interrupt Status Register 0

Table 15-47.
MCU_FSS0_HPB0_ECC_DED_STATUS_REG0
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0140h

Figure 15-21. MCU_FSS0_HPB0_ECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIF FO_PEND	MEM_AR_FIF FO_PEND	MEM_AWID1_F IFO_PEND	MEM_WID1_FIF FO_PEND	MEM_AW1_FIF O_PEND	MEM_AWID0_F IFO_PEND	MEM_WID0_FIF FO_PEND
R-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
MEM_AW0_FIF O_PEND	MEM_RX_FIF FO_PEND	MEM_RDAT_FIF FO_PEND	MEM_BDAT1_F IFO_PEND	MEM_BDAT0_F IFO_PEND	MEM_WDAT1_F FIFO_PEND	MEM_WDAT0_F FIFO_PEND	MEM_ADR_FIF O_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-48. MCU_FSS0_HPB0_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MEM_ARID_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_arid_fifo_pend
13	MEM_AR_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_awid1_fifo_pend
11	MEM_WID1_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_awid0_fifo_pend
8	MEM_WID0_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_aw0_fifo_pend
6	MEM_RX_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_rx_fifo_pend
5	MEM_RDAT_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdat1_fifo_pend

Table 15-48. MCU_FSS0_HPBO_ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	MEM_WDAT0_FIFO_PEN D	R/W1S	0h	Interrupt Pending Status for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_PEND	R/W1S	0h	Interrupt Pending Status for mem_adr_fifo_pend

15.25 MCU_FSS0_HPB0_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MCU_FSS0_HPB0_ECC_DED_ENABLE_SET_REG0 is shown in [Figure 15-22](#) and described in [Table 15-50](#).

Return to [Summary Table](#).

DED Interrupt Enable Set Register 0

Table 15-49.
MCU_FSS0_HPB0_ECC_DED_ENABLE_SET_REG0
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0180h

Figure 15-22. MCU_FSS0_HPB0_ECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIFO_ENABLE_SET	MEM_AR_FIFO_ENABLE_SET	MEM_AWID1_FIFO_ENABLE_SET	MEM_WID1_FIFO_ENABLE_SET	MEM_AW1_FIFO_ENABLE_SET	MEM_AWID0_FIFO_ENABLE_SET	MEM_WID0_FIFO_ENABLE_SET
R-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
MEM_AW0_FIFO_ENABLE_SET	MEM_RX_FIFO_ENABLE_SET	MEM_RDAT_FIFO_ENABLE_SET	MEM_BDAT1_FIFO_ENABLE_SET	MEM_BDAT0_FIFO_ENABLE_SET	MEM_WDAT1_FIFO_ENABLE_SET	MEM_WDAT0_FIFO_ENABLE_SET	MEM_ADR_FIFO_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-50. MCU_FSS0_HPB0_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MEM_ARID_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_arid_fifo_pend
13	MEM_AR_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_avid1_fifo_pend
11	MEM_WID1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_avid0_fifo_pend
8	MEM_WID0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_aw0_fifo_pend
6	MEM_RX_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_rx_fifo_pend

Table 15-50. MCU_FSS0_HPBO_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MEM_RDAT_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_wdat1_fifo_pend
1	MEM_WDAT0_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for mem_adr_fifo_pend

15.26 MCU_FSS0_HPB0_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MCU_FSS0_HPB0_ECC_DED_ENABLE_CLR_REG0 is shown in [Figure 15-23](#) and described in [Table 15-52](#).

Return to [Summary Table](#).

DED Interrupt Enable Clear Register 0

Table 15-51.
MCU_FSS0_HPB0_ECC_DED_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 01C0h

Figure 15-23. MCU_FSS0_HPB0_ECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	MEM_ARID_FIF O_ENABLE_CLR	MEM_AR_FIFO _ENABLE_CLR	MEM_AWID1_FIF O_ENABLE_CLR	MEM_WID1_FIF O_ENABLE_CLR	MEM_AW1_FIF O_ENABLE_CLR	MEM_AWID0_FIF O_ENABLE_CLR	MEM_WID0_FIF O_ENABLE_CLR
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
MEM_AW0_FIF O_ENABLE_CLR	MEM_RX_FIFO _ENABLE_CLR	MEM_RDAT_FIF O_ENABLE_CLR	MEM_BDAT1_FIF O_ENABLE_CLR	MEM_BDAT0_FIF O_ENABLE_CLR	MEM_WDAT1_FIF O_ENABLE_CLR	MEM_WDAT0_FIF O_ENABLE_CLR	MEM_ADR_FIF O_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-52. MCU_FSS0_HPB0_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R	0h	Reserved
14	MEM_ARID_FIFO_ENAB LE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_arid_fifo_pend
13	MEM_AR_FIFO_ENABLE _CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_ar_fifo_pend
12	MEM_AWID1_FIFO_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_avid1_fifo_pend
11	MEM_WID1_FIFO_ENAB LE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_wid1_fifo_pend
10	MEM_AW1_FIFO_ENABL E_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_aw1_fifo_pend
9	MEM_AWID0_FIFO_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_avid0_fifo_pend
8	MEM_WID0_FIFO_ENAB LE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_wid0_fifo_pend
7	MEM_AW0_FIFO_ENABL E_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_aw0_fifo_pend
6	MEM_RX_FIFO_ENABLE _CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_rx_fifo_pend

Table 15-52. MCU_FSS0_HPBO_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MEM_RDAT_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_rdat_fifo_pend
4	MEM_BDAT1_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_bdat1_fifo_pend
3	MEM_BDAT0_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_bdat0_fifo_pend
2	MEM_WDAT1_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_wdat1_fifo_pend
1	MEM_WDAT0_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_wdat0_fifo_pend
0	MEM_ADR_FIFO_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for mem_adr_fifo_pend

15.27 MCU_FSS0_HPB0_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MCU_FSS0_HPB0_ECC_AGGR_ENABLE_SET is shown in [Figure 15-24](#) and described in [Table 15-54](#).

Return to [Summary Table](#).

Aggregator Interrupt Enable Set Register

Table 15-53.
MCU_FSS0_HPB0_ECC_AGGR_ENABLE_SET
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0200h

Figure 15-24. MCU_FSS0_HPB0_ECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-54. MCU_FSS0_HPB0_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

15.28 MCU_FSS0_HPB0_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MCU_FSS0_HPB0_ECC_AGGR_ENABLE_CLR is shown in [Figure 15-25](#) and described in [Table 15-56](#).

Return to [Summary Table](#).

Aggregator Interrupt Enable Clear Register

Table 15-55.
MCU_FSS0_HPB0_ECC_AGGR_ENABLE_CLR
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0204h

Figure 15-25. MCU_FSS0_HPB0_ECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-56. MCU_FSS0_HPB0_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

15.29 MCU_FSS0_HPB0_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MCU_FSS0_HPB0_ECC_AGGR_STATUS_SET is shown in [Figure 15-26](#) and described in [Table 15-58](#).

Return to [Summary Table](#).

Aggregator Interrupt Status Set Register

Table 15-57.
MCU_FSS0_HPB0_ECC_AGGR_STATUS_SET
Instances

Instance	Physical Address
MCU_FSS0_HPB_ECC_AGGR	4706 0208h

Figure 15-26. MCU_FSS0_HPB0_ECC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wincr-0h		R/Wincr-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 15-58. MCU_FSS0_HPB0_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

15.30 MCU_FSS0_HPBO_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MCU_FSS0_HPBO_ECC_AGGR_STATUS_CLR is shown in [Figure 15-27](#) and described in [Table 15-60](#).

Return to [Summary Table](#).

Aggregator Interrupt Status Clear Register

Table 15-59.
MCU_FSS0_HPBO_ECC_AGGR_STATUS_CLR
Instances

Instance	Physical Address
MCU_FSS0_HPBO_ECC_AGGR	4706 020Ch

Figure 15-27. MCU_FSS0_HPBO_ECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 15-60. MCU_FSS0_HPBO_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

16 GPMC Registers

Table 16-2 lists the memory-mapped registers for the GPMC. All register offset addresses not listed in Table 16-2 should be considered as reserved locations and the register contents should not be modified.

Note

All GPMC registers are aligned to 32-bit address boundaries. All register file accesses, except to GPMC_NAND_DATA_i register, are little-endian. If the GPMC_NAND_DATA_i register location is accessed, the endianness is access-dependent.

Table 16-1. GPMC Instances

Instance	Base Address
GPMC0_CFG	0539 0000h

Table 16-2. GPMC Registers

Offset	Acronym	Register Name	GPMC0_CFG Physical Address
0h	GPMC_REVISION	IP revision	0539 0000h
10h	GPMC_SYSCONFIG	Module software reset and local power management register	0539 0010h
14h	GPMC_SYSSTATUS	Module status information register	0539 0014h
18h	GPMC_IRQSTATUS	Interrupt status register	0539 0018h
1Ch	GPMC_IRQENABLE	Interrupt enable register	0539 001Ch
40h	GPMC_TIMEOUT_CONTROL	Control register of timeout counter	0539 0040h
44h	GPMC_ERR_ADDRESS	Error address register	0539 0044h
48h	GPMC_ERR_TYPE	Error type register	0539 0048h
50h	GPMC_CONFIG	Global configuration register	0539 0050h
54h	GPMC_STATUS	Global status register	0539 0054h
60h + formula	GPMC_CONFIG1_i	Configuration register 1	0539 0060h + formula
64h + formula	GPMC_CONFIG2_i	Configuration register 2	0539 0064h + formula
68h + formula	GPMC_CONFIG3_i	Configuration register 3	0539 0068h + formula
6Ch + formula	GPMC_CONFIG4_i	Configuration register 4	0539 006Ch + formula
70h + formula	GPMC_CONFIG5_i	Configuration register 5	0539 0070h + formula
74h + formula	GPMC_CONFIG6_i	Configuration register 6	0539 0074h + formula
78h + formula	GPMC_CONFIG7_i	Configuration register 7	0539 0078h + formula
7Ch + formula	GPMC_NAND_COMMAND_i	GPMC NAND COMMAND_i location register	0539 007Ch + formula
80h + formula	GPMC_NAND_ADDRESS_i	GPMC NAND ADDRESS_i location register	0539 0080h + formula
84h + formula	GPMC_NAND_DATA_i	GPMC NAND DATA_i location register	0539 0084h + formula
1E0h	GPMC_PREFETCH_CONFIG1	Prefetch engine configuration 1	0539 01E0h
1E4h	GPMC_PREFETCH_CONFIG2	Prefetch engine configuration 2	0539 01E4h
1ECh	GPMC_PREFETCH_CONTROL	Prefetch engine control	0539 01ECh
1F0h	GPMC_PREFETCH_STATUS	Prefetch engine status	0539 01F0h
1F4h	GPMC_ECC_CONFIG	ECC configuration	0539 01F4h
1F8h	GPMC_ECC_CONTROL	ECC control	0539 01F8h
1FCh	GPMC_ECC_SIZE_CONFIG	ECC size	0539 01FCh
200h + formula	GPMC_ECCj_RESULT	ECC result register	0539 0200h + formula
240h + formula	GPMC_BCH_RESULT0_i	BCH ECC result (bits 0 to 31)	0539 0240h + formula
244h + formula	GPMC_BCH_RESULT1_i	BCH ECC result (bits 32 to 63)	0539 0244h + formula
248h + formula	GPMC_BCH_RESULT2_i	BCH ECC result (bits 64 to 95)	0539 0248h + formula
24Ch + formula	GPMC_BCH_RESULT3_i	BCH ECC result (bits 96 to 127)	0539 024Ch + formula
2D0h	GPMC_BCH_SWDATA	Data to BCH ECC calculator	0539 02D0h

Table 16-2. GPMC Registers (continued)

Offset	Acronym	Register Name	GPMC0_CFG Physical Address
300h + formula	GPMC_BCH_RESULT4_i	BCH ECC result (bits 128 to 159)	0539 0300h + formula
304h + formula	GPMC_BCH_RESULT5_i	BCH ECC result (bits 160 to 191)	0539 0304h + formula
308h + formula	GPMC_BCH_RESULT6_i	BCH ECC result (bits 192 to 207)	0539 0308h + formula

16.1 GPMC_REVISION Register (Offset = 0h) [reset = 60h]

GPMC_REVISION is shown in [Figure 16-1](#) and described in [Table 16-4](#).

This register contains the IP revision code.

Table 16-3. GPMC_REVISION Instances

Instance	Physical Address
GPMC0_CFG	0539 0000h

Figure 16-1. GPMC_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-60h																															

LEGEND: R = Read Only; -n = value after reset

Table 16-4. GPMC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	60h	TI internal data. Identifies revision of peripheral.

16.2 GPMC_SYSCONFIG Register (Offset = 10h) [reset = 0h]

GPMC_SYSCONFIG is shown in [Figure 16-2](#) and described in [Table 16-6](#).

Register related to module software reset and local power management.

Table 16-5. GPMC_SYSCONFIG Instances

Instance	Physical Address
GPMC0_CFG	0539 0010h

Figure 16-2. GPMC_SYSCONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			IDLEMODE		RESERVED	RESERVED	AUTOIDLE
R-0h			R/W-0h		R-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-6. GPMC_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
4-3	IDLEMODE	R/W	0h	0h = Force-idle. A clock stop request is acknowledged unconditionally. 1h (R/W) = No-idle. A clock stop request is never acknowledged. 2h (R/W) = Smart-idle. Acknowledgment to a clock stop request is given based on the internal activity of the module. 3h (R/W) = Reserved. Do not use.
2	RESERVED	R	0h	Write 0 for future compatibility Read returns 0.
1	RESERVED	R/W	0h	This bit must be kept 0 for normal functioning of the IP. Do not set this bit to 1. 0h = Normal mode 1h = The module is reset
0	AUTOIDLE	R/W	0h	Internal interface clock-gating strategy 0h (R/W) = Interface clock is free-running. 1h (R/W) = Automatic Interface clock gating strategy is applied, based on the interconnect activity.

16.3 GPMC_SYSSTATUS Register (Offset = 14h) [reset = 0000000-h]

GPMC_SYSSTATUS is shown in [Figure 16-3](#) and described in [Table 16-8](#).

This register provides status information about the module, excluding the interrupt status information.

Table 16-7. GPMC_SYSSTATUS Instances

Instance	Physical Address
GPMC0_CFG	0539 0014h

Figure 16-3. GPMC_SYSSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R-0h							R-

LEGEND: R = Read Only; -n = value after reset

Table 16-8. GPMC_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Read returns 0.
7-1	RESERVED	R	0h	Read returns 0 (reserved for interconnect-socket status information).
0	RESETDONE	R	-h	Internal reset monitoring 0h (R) = Internal module reset is ongoing. 1h (R) = Reset is complete.

16.4 GPMC_IRQSTATUS Register (Offset = 18h) [reset = 0h]

GPMC_IRQSTATUS is shown in [Figure 16-4](#) and described in [Table 16-10](#).

This interrupt status register regroups all the status of the module internal events that can generate an interrupt.

Table 16-9. GPMC_IRQSTATUS Instances

Instance	Physical Address
GPMC0_CFG	0539 0018h

Figure 16-4. GPMC_IRQSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						WAIT1EDGEDETECTIONSTATUS	WAIT0EDGEDETECTIONSTATUS
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED						TERMINALCOUNTSTATUS	FIFOEVENTSTATUS
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-10. GPMC_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
9	WAIT1EDGEDETECTIONSTATUS	R/W	0h	Status of the Wait1 Edge Detection interrupt Write: 0h = WAIT1EDGEDETECTIONSTATUS bit is unchanged. 1h = WAIT1EDGEDETECTIONSTATUS bit is reset. Read: 0h = A transition on WAIT1 input pin has not been detected. 1h = A transition on WAIT1 input pin has been detected.
8	WAIT0EDGEDETECTIONSTATUS	R/W	0h	Status of the Wait0 Edge Detection interrupt Write: 0h = WAIT0EDGEDETECTIONSTATUS bit is unchanged. 1h = WAIT0EDGEDETECTIONSTATUS bit is reset. Read: 0h = A transition on WAIT0 input pin has not been detected. 1h = A transition on WAIT0 input pin has been detected.
7-2	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
1	TERMINALCOUNTSTATUS	R/W	0h	Status of the TerminalCountEvent interrupt Write: 0h = TERMINALCOUNTSTATUS bit is unchanged. 1h = TERMINALCOUNTSTATUS bit is reset. Read: 0h = Indicates that CountValue is greater than 0. 1h = Indicates that CountValue is equal to 0.

Table 16-10. GPMC_IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FIFOEVENTSTATUS	R/W	0h	<p>Status of the FIFOEvent interrupt</p> <p>Write:</p> <p>0h = FIFOEVENTSTATUS bit is unchanged.</p> <p>1h = FIFOEVENTSTATUS bit is reset.</p> <p>Read:</p> <p>0h = Indicates that less than GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bytes are available in prefetch mode and less than FIFOTHRESHOLD bytes free places are available in write-posting mode.</p> <p>1h = Indicates that at least GPMC_PREFETCH_STATUS[16] FIFOTHRESHOLDSTATUS bytes are available in prefetch mode and at least FIFOTHRESHOLD bytes free places are available in write-posting mode.</p>

16.5 GPMC_IRQENABLE Register (Offset = 1Ch) [reset = 0h]

GPMC_IRQENABLE is shown in [Figure 16-5](#) and described in [Table 16-12](#).

The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.

Table 16-11. GPMC_IRQENABLE Instances

Instance	Physical Address
GPMC0_CFG	0539 001Ch

Figure 16-5. GPMC_IRQENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						WAIT1EDGEDETECTIONENABLE	WAIT0EDGEDETECTIONENABLE
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED						TERMINALCOUNTEVENTENABLE	FIFOEVENTENABLE
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-12. GPMC_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
9	WAIT1EDGEDETECTIONENABLE	R/W	0h	Enables the Wait1 Edge Detection interrupt 0h (R/W) = Wait1EdgeDetection interrupt is masked. 1h (R/W) = Wait1EdgeDetection event generates an interrupt if occurs.
8	WAIT0EDGEDETECTIONENABLE	R/W	0h	Enables the Wait0 Edge Detection interrupt 0h (R/W) = Wait0EdgeDetection interrupt is masked. 1h (R/W) = Wait0EdgeDetection event generates an interrupt if occurs.
7-2	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
1	TERMINALCOUNTEVENTENABLE	R/W	0h	Enables TerminalCountEvent interrupt issuing in prefetch or write-posting mode 0h (R/W) = TerminalCountEvent interrupt is masked. 1h (R/W) = TerminalCountEvent interrupt is not masked.
0	FIFOEVENTENABLE	R/W	0h	Enables the FIFOEvent interrupt 0h (R/W) = FIFOEvent interrupt is masked. 1h (R/W) = FIFOEvent interrupt is not masked.

16.6 GPMC_TIMEOUT_CONTROL Register (Offset = 40h) [reset = 1FF0h]

GPMC_TIMEOUT_CONTROL is shown in [Figure 16-6](#) and described in [Table 16-14](#).

The GPMC_TIMEOUT_CONTROL register allows the user to set the start value of the timeout counter.

Table 16-13. GPMC_TIMEOUT_CONTROL Instances

Instance	Physical Address
GPMC0_CFG	0539 0040h

Figure 16-6. GPMC_TIMEOUT_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				TIMEOUTSTARTVALUE			
R-0h				R/W-1FFh			
7	6	5	4	3	2	1	0
TIMEOUTSTARTVALUE				RESERVED			TIMEOUTENABLE
R/W-1FFh				R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-14. GPMC_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
12-4	TIMEOUTSTARTVALUE	R/W	1FFh	Start value of the time-out counter 000h = Zero GPMC_FCLK cycle 001h = One GPMC_FCLK cycle ... 1FFh = 511 GPMC_FCLK cycles
3-1	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
0	TIMEOUTENABLE	R/W	0h	Enable bit of the TimeOut feature 0h (R/W) = TimeOut feature is disabled. 1h (R/W) = TimeOut feature is enabled.

16.7 GPMC_ERR_ADDRESS Register (Offset = 44h) [reset = 0h]

GPMC_ERR_ADDRESS is shown in [Figure 16-7](#) and described in [Table 16-16](#).

The GPMC_ERR_ADDRESS register stores the address of the illegal access when an error occurs.

Table 16-15. GPMC_ERR_ADDRESS Instances

Instance	Physical Address
GPMC0_CFG	0539 0044h

Figure 16-7. GPMC_ERR_ADDRESS Register

31	30	29	28	27	26	25	24
RESERVED	ILLEGALADD						
R-0h	R-0h						
23	22	21	20	19	18	17	16
ILLEGALADD							
R-0h							
15	14	13	12	11	10	9	8
ILLEGALADD							
R-0h							
7	6	5	4	3	2	1	0
ILLEGALADD							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 16-16. GPMC_ERR_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
30-0	ILLEGALADD	R	0h	Address of illegal access A30: 0 for memory region, 1 for GPMC register region A29-A0: 1GB maximum

16.8 GPMC_ERR_TYPE Register (Offset = 48h) [reset = 0h]

GPMC_ERR_TYPE is shown in [Figure 16-8](#) and described in [Table 16-18](#).

The GPMC_ERR_TYPE register stores the type of error when an error occurs.

Table 16-17. GPMC_ERR_TYPE Instances

Instance	Physical Address
GPMC0_CFG	0539 0048h

Figure 16-8. GPMC_ERR_TYPE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					ILLEGALMCMD		
R-0h				R-0h			
7	6	5	4	3	2	1	0
RESERVED			ERRORNOTSU PPADD	ERRORNOTSU PPCMD	ERRORTIMEO UT	RESERVED	ERRORVALID
R-0h			R-0h	R-0h	R-0h	R-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 16-18. GPMC_ERR_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
10-8	ILLEGALMCMD	R	0h	System command of the transaction that caused the error
7-5	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
4	ERRORNOTSUPPADD	R	0h	Not supported address error 0h (R) = No error occurs. 1h (R) = The error is due to a nonsupported address.
3	ERRORNOTSUPPMCMD	R	0h	Not supported command error 0h (R) = No error occurs. 1h (R) = The error is due to a nonsupported command
2	ERRORTIMEOUT	R	0h	Time-out error 0h (R) = No error occurs. 1h (R) = The error is due to a timeout.
1	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
0	ERRORVALID	R/W1C	0h	Error validity status - Must be explicitly cleared with a write 1 transaction 0h (R/W) = All error fields no longer valid 1h (R/W) = Error detected and logged in the other error fields

16.9 GPMC_CONFIG Register (Offset = 50h) [reset = 200h]

GPMC_CONFIG is shown in [Figure 16-9](#) and described in [Table 16-20](#).

The configuration register allows global configuration of the GPMC.

Table 16-19. GPMC_CONFIG Instances

Instance	Physical Address
GPMC0_CFG	0539 0050h

Figure 16-9. GPMC_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						WAIT1PINPOLARITY	WAIT0PINPOLARITY
R-0h						R/W-1h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			WRITEPROTECT	RESERVED			NANDFORCEPOSTEDWRITE
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-20. GPMC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
9	WAIT1PINPOLARITY	R/W	1h	Selects the polarity of input pin WAIT1 0h (R/W) = WAIT1 active low 1h (R/W) = WAIT1 active high
8	WAIT0PINPOLARITY	R/W	0h	Selects the polarity of input pin WAIT0 0h (R/W) = WAIT0 active low 1h (R/W) = WAIT0 active high
7-5	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
4	WRITEPROTECT	R/W	0h	Controls the WP output pin level 0h (R/W) = nWP output pin is low 1h (R/W) = nWP output pin is high
3-1	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
0	NANDFORCEPOSTEDWRITE	R/W	0h	Enables the Force Posted Write feature to NAND Cmd/Add/Data location 0h (R/W) = Disables Force Posted Write 1h (R/W) = Enables Force Posted Write

16.10 GPMC_STATUS Register (Offset = 54h) [reset = 00000-01h]

GPMC_STATUS is shown in [Figure 16-10](#) and described in [Table 16-22](#).

The status register provides global status bits of the GPMC.

Table 16-21. GPMC_STATUS Instances

Instance	Physical Address
GPMC0_CFG	0539 0054h

Figure 16-10. GPMC_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						WAIT1STATUS	WAIT0STATUS
R-0h						R-	R-
7	6	5	4	3	2	1	0
RESERVED							EMPTYWRITE BUFFERSTATUS
R-0h							R-1h

LEGEND: R = Read Only; -n = value after reset

Table 16-22. GPMC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
9	WAIT1STATUS	R	-h	Is a copy of input pin WAIT1. (Reset value is WAIT1 input pin sampled at device reset.) 0h (R) = WAIT1 asserted (inactive state) 1h (R) = WAIT1 deasserted
8	WAIT0STATUS	R	-h	Is a copy of input pin WAIT0. (Reset value is WAIT0 input pin sampled at device reset.) 0h (R) = WAIT0 asserted (inactive state) 1h (R) = WAIT0 deasserted
7-1	RESERVED	R	0h	Write 0s for future compatibility. Reads returns 0
0	EMPTYWRITEBUFFERS TATUS	R	1h	Stores the empty status of the write buffer 0h (R) = Write buffer is not empty. 1h (R) = Write buffer is empty.

16.11 GPMC_CONFIG1_i Register (Offset = 60h + formula) [reset = 0h]

GPMC_CONFIG1_i (where i = 0 to 3) is shown in [Figure 16-11](#) and described in [Table 16-24](#).

The configuration register 1 sets signal control parameters per chip-select.

Offset = 60h + (i * 30h), where: i = 0 to 3

Table 16-23. GPMC_CONFIG1_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0060h + formula

Figure 16-11. GPMC_CONFIG1_i Register

31	30	29	28	27	26	25	24
WRAPBURST	READMULTIPLE	READTYPE	WRITEMULTIPLE	WRITETYPE	CLKACTIVATIONTIME	ATTACHEDDE VICEPAGELEN GTH	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ATTACHEDDE VICEPAGELEN GTH	WAITREADMONITORING	WAITWRITEMONITORING	RESERVED	WAITMONITORINGTIME	WAITPINSELECT		
R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED	DEVICESIZE	DEVICETYPE	MUXADDDATA				
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	TIMEPARAGRAPH NULARITY	RESERVED	GPMCFCLKDIVIDER				
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-24. GPMC_CONFIG1_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRAPBURST	R/W	0h	Enables the wrapping burst capability. Must be set if the attached device is configured in wrapping burst 0h (R/W) = Synchronous wrapping burst not supported 1h (R/W) = Synchronous wrapping burst supported
30	READMULTIPLE	R/W	0h	Selects the read single or multiple access 0h (R/W) = Single access 1h (R/W) = Multiple access (burst if synchronous, page if asynchronous)
29	READTYPE	R/W	0h	Selects the read mode operation 0h (R/W) = Read asynchronous 1h (R/W) = Read synchronous
28	WRITEMULTIPLE	R/W	0h	Selects the write single or multiple access 0h (R/W) = Single access 1h (R/W) = Multiple access (burst if synchronous, considered as single if asynchronous)
27	WRITETYPE	R/W	0h	Selects the write mode operation 0h (R/W) = Write asynchronous 1h (R/W) = Write synchronous

Table 16-24. GPMC_CONFIG1_i Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-25	CLKACTIVATIONTIME	R/W	0h	Output GPMC CLK activation time 0h (R/W) = First rising edge of GPMC CLK at start access time 1h (R/W) = First rising edge of GPMC CLK one GPMC_FCLK cycle after start access time 2h (R/W) = First rising edge of GPMC CLK two GPMC_FCLK cycles after start access time 3h (R/W) = Reserved
24-23	ATTACHEDDEVICEPAGE LENGTH	R/W	0h	Specifies the attached device page (burst) length 0h (R/W) = 4 words 1h (R/W) = 8 words 2h (R/W) = 16 words 3h (R/W) = Reserved (1 word = interface size)
22	WAITREADMONITORING	R/W	0h	Selects the Wait monitoring configuration for Read accesses 0h (R/W) = WAIT pin is not monitored for read accesses. 1h (R/W) = WAIT pin is monitored for read accesses.
21	WAITWRITEMONITORING	R/W	0h	Selects the Wait monitoring configuration for Write accesses 0h (R/W) = WAIT pin is not monitored for write accesses. 1h (R/W) = WAIT pin is monitored for write accesses.
20	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
19-18	WAITMONITORINGTIME	R/W	0h	Selects input pin Wait monitoring time 0h (R/W) = WAIT pin is monitored with valid data. 1h (R/W) = WAIT pin is monitored one GPMC CLK cycle before valid data. 2h (R/W) = WAIT pin is monitored two GPMC CLK cycle before valid data. 3h (R/W) = Reserved
17-16	WAITPINSELECT	R/W	0h	Selects the input WAIT pin for this chip-select 0h (R/W) = Wait input pin is WAIT0. 1h (R/W) = Wait input pin is WAIT1. 2h (R/W) = Reserved 3h (R/W) = Reserved
15-14	RESERVED	R	0h	Write 0s for future compatibility. Reads returns 0
13-12	DEVICESTYPE	R/W	0h	Selects the device size attached NOTE: Reset value is 0h for CS0 and 1h for CS1 to CS3 0h (R/W) = 8 bit 1h (R/W) = 16 bit 2h (R/W) = Reserved 3h (R/W) = Reserved
11-10	DEVICETYPE	R/W	0h	Selects the attached device type 0h (R/W) = NOR flash-like, asynchronous and synchronous devices 1h (R/W) = Reserved 2h (R/W) = NAND flash-like devices, stream mode 3h (R/W) = Reserved
9-8	MUXADDDATA	R/W	0h	Enables the address and data multiplexed protocol 0h (R/W) = Nonmultiplexed attached device 1h (R/W) = AAD-multiplexed protocol device 2h (R/W) = Address and data multiplexed attached device 3h (R/W) = Reserved
7-5	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.

Table 16-24. GPMC_CONFIG1_i Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TIMEPARAGRANULARITY	R/W	0h	Signals timing latencies scalar factor (RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS) 0h (R/W) = x1 latencies 1h (R/W) = x2 latencies
3-2	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
1-0	GPMCFCLKDIVIDER	R/W	0h	Divides the GPMC_FCLK clock 0h (R/W) = GPMC CLK frequency = GPMC_FCLK frequency 1h (R/W) = GPMC CLK frequency = GPMC_FCLK frequency / 2 2h (R/W) = GPMC CLK frequency = GPMC_FCLK frequency / 3 3h (R/W) = GPMC CLK frequency = GPMC_FCLK frequency / 4

16.12 GPMC_CONFIG2_i Register (Offset = 64h + formula) [reset = 00101001h]

GPMC_CONFIG2_i (where i = 0 to 3) is shown in [Figure 16-12](#) and described in [Table 16-26](#).

CS signal timing parameter configuration

Offset = 64h + (i * 30h), where: i = 0 to 3

Table 16-25. GPMC_CONFIG2_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0064h + formula

Figure 16-12. GPMC_CONFIG2_i Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				CSWROFFTIME			
R-0h				R/W-10h			
15	14	13	12	11	10	9	8
RESERVED				CSRDOFFTIME			
R-0h				R/W-10h			
7	6	5	4	3	2	1	0
CSEXTRADelay	RESERVED			CSONTIME			
R/W-0h	R-0h			R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-26. GPMC_CONFIG2_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
20-16	CSWROFFTIME	R/W	10h	CS i deassertion time from start cycle time for write accesses 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
15-13	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
12-8	CSRDOFFTIME	R/W	10h	CS i de-assertion time from start cycle time for read accesses 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
7	CSEXTRADelay	R/W	0h	CS i Add extra half-GPMC_FCLK cycle 0h (R/W) = CS i Timing control signal is not delayed 1h (R/W) = CS i Timing control signal is delayed of half GPMC_FCLK clock cycle
6-4	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.

Table 16-26. GPMC_CONFIG2_i Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CSONTIME	R/W	1h	CS i assertion time from start cycle time 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... Fh = 15 GPMC_FCLK cycles

16.13 GPMC_CONFIG3_i Register (Offset = 68h + formula) [reset = 22060514h]

GPMC_CONFIG3_i (where i = 0 to 3) is shown in [Figure 16-13](#) and described in [Table 16-28](#).

nADV signal timing parameter configuration

Offset = 68h + (i * 30h), where: i = 0 to 3

Table 16-27. GPMC_CONFIG3_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0068h + formula

Figure 16-13. GPMC_CONFIG3_i Register

31	30	29	28	27	26	25	24
RESERVED	ADVAADMUXWROFFTIME			RESERVED	ADVAADMUXRDOFFTIME		
R-0h	R/W-2h			R-0h	R/W-2h		
23	22	21	20	19	18	17	16
RESERVED				ADVWROFFTIME			
R-0h				R/W-6h			
15	14	13	12	11	10	9	8
RESERVED				ADVRDOFFTIME			
R-0h				R/W-5h			
7	6	5	4	3	2	1	0
ADVEXTRA LAY	ADVAADMUXONTIME			ADVONTIME			
R/W-0h	R/W-1h			R/W-4h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-28. GPMC_CONFIG3_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
30-28	ADVAADMUXWROFFTIME	R/W	2h	nADV deassertion for first address phase when using the AAD-multiplexed protocol 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... 7h = 7 GPMC_FCLK cycles
27	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
26-24	ADVAADMUXRDOFFTIME	R/W	2h	nADV assertion for first address phase when using the AAD-multiplexed protocol 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... 7h = 7 GPMC_FCLK cycles
23-21	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
20-16	ADVWROFFTIME	R/W	6h	nADV deassertion time from start cycle time for write accesses 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
15-13	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.

Table 16-28. GPMC_CONFIG3_i Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	ADVRDOFFTIME	R/W	5h	nADV deassertion time from start cycle time for read accesses 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
7	ADVEXTRADELAY	R/W	0h	nADV add extra half-GPMC_FCLK cycle 0h (R/W) = nADV timing control signal is not delayed 1h (R/W) = nADV timing control signal is delayed of half GPMC_FCLK clock cycle
6-4	ADVAADMUXONTIME	R/W	1h	nADV assertion for first address phase when using the AAD-multiplexed protocol 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... 7h = 7 GPMC_FCLK cycles
3-0	ADVONTIME	R/W	4h	nADV assertion time from start cycle time 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... Fh = 15 GPMC_FCLK cycles

16.14 GPMC_CONFIG4_i Register (Offset = 6Ch + formula) [reset = 10057016h]

GPMC_CONFIG4_i (where i = 0 to 3) is shown in [Figure 16-14](#) and described in [Table 16-30](#).

nWE and nOE signals timing parameter configuration

Offset = 6Ch + (i * 30h), where: i = 0 to 3

Table 16-29. GPMC_CONFIG4_i Instances

Instance	Physical Address
GPMC0_CFG	0539 006Ch + formula

Figure 16-14. GPMC_CONFIG4_i Register

31	30	29	28	27	26	25	24
RESERVED			WEOFFTIME				
R-0h				R/W-10h			
23	22	21	20	19	18	17	16
WEEXTRADEL AY	RESERVED			WEONTIME			
R/W-0h		R-0h		R/W-5h			
15	14	13	12	11	10	9	8
OEADMUX_OFFTIME			OEOFFTIME				
R/W-3h				R/W-10h			
7	6	5	4	3	2	1	0
OEEXTRADEL AY	OEADMUX_ONTIME			OEONTIME			
R/W-0h		R/W-1h		R/W-6h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-30. GPMC_CONFIG4_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
28-24	WEOFFTIME	R/W	10h	nWE deassertion time from start cycle time 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
23	WEEXTRADELAY	R/W	0h	nWE add extra half-GPMC_FCLK cycle 0h (R/W) = nWE timing control signal is not delayed 1h (R/W) = nWE timing control signal is delayed of half-GPMC_FCLK clock cycle
22-20	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
19-16	WEONTIME	R/W	5h	nWE assertion time from start cycle time 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... Fh = 15 GPMC_FCLK cycles

Table 16-30. GPMC_CONFIG4_i Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-13	OEAADMUX_OFFTIME	R/W	3h	nOE deassertion time for the first address phase in an AAD-multiplexed access 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... 7h = 7 GPMC_FCLK cycles
12-8	OEOFFTIME	R/W	10h	nOE deassertion time from start cycle time 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
7	OEEXTRADELAY	R/W	0h	nOE add extra half-GPMC_FCLK cycle 0h (R/W) = nOE timing control signal is not delayed 1h (R/W) = nOE timing control signal is delayed of half-GPMC_FCLK clock cycle
6-4	OEAADMUX_ONTIME	R/W	1h	nOE assertion time for the first address phase in an AAD-mux access 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... 7h = 7 GPMC_FCLK cycles
3-0	OEONTIME	R/W	6h	nOE assertion time from start cycle time 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... Fh = 15 GPMC_FCLK cycles

16.15 GPMC_CONFIG5_i Register (Offset = 70h + formula) [reset = 010F1111h]

GPMC_CONFIG5_i (where i = 0 to 3) is shown in [Figure 16-15](#) and described in [Table 16-32](#).

RdAccessTime and CycleTime timing parameters configuration

Offset = 70h + (i * 30h), where: i = 0 to 3

Table 16-31. GPMC_CONFIG5_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0070h + formula

Figure 16-15. GPMC_CONFIG5_i Register

31	30	29	28	27	26	25	24
RESERVED				PAGEBURSTACCESSTIME			
R-0h				R/W-1h			
23	22	21	20	19	18	17	16
RESERVED				RDACCESSTIME			
R-0h				R/W-Fh			
15	14	13	12	11	10	9	8
RESERVED				WRCYCLETIME			
R-0h				R/W-11h			
7	6	5	4	3	2	1	0
RESERVED				RDCYCLETIME			
R-0h				R/W-11h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-32. GPMC_CONFIG5_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
27-24	PAGEBURSTACCESSTIME	R/W	1h	Delay between successive words in a multiple access 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... Fh = 15 GPMC_FCLK cycles
23-21	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
20-16	RDACCESSTIME	R/W	Fh	Delay between start cycle time and first data valid 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
15-13	RESERVED	R	0h	Write 0s for future compatibility. Reads returns 0
12-8	WRCYCLETIME	R/W	11h	Total write cycle time 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
7-5	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.

Table 16-32. GPMC_CONFIG5_i Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	RDCYCLETIME	R/W	11h	Total read cycle time 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles

16.16 GPMC_CONFIG6_i Register (Offset = 74h + formula) [reset = 8F070000h]

GPMC_CONFIG6_i (where i = 0 to 3) is shown in [Figure 16-16](#) and described in [Table 16-34](#).

WrAccessTime, WrDataOnADmuxBus, Cycle2Cycle and BusTurnAround parameters configuration

Offset = 74h + (i * 30h), where: i = 0 to 3

Table 16-33. GPMC_CONFIG6_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0074h + formula

Figure 16-16. GPMC_CONFIG6_i Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	WRACCESSTIME					
R/W-1h	R-0h	R/W-Fh					
23	22	21	20	19	18	17	16
RESERVED				WRDATAONADMUXBUS			
R-0h				R/W-7h			
15	14	13	12	11	10	9	8
RESERVED				CYCLE2CYCLEDELAY			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
CYCLE2CYCLE SAMECSEN	CYCLE2CYCLE DIFFCSEN	RESERVED		BUSTURNAROUND			
R/W-0h	R/W-0h	R-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-34. GPMC_CONFIG6_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	1h	TI Internal use - Do not modify.
30-29	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
28-24	WRACCESSTIME	R/W	Fh	Delay from start access time to the GPMC_FCLK rising edge corresponding the GPMC CLK rising edge used by the attached memory for the first data capture 00h = 0 GPMC_FCLK cycle 01h = 1 GPMC_FCLK cycle ... 1Fh = 31 GPMC_FCLK cycles
23-20	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
19-16	WRDATAONADMUXBUS	R/W	7h	Specifies on which GPMC_FCLK rising edge the first data of the write is driven in the add/data mux bus
15-12	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
11-8	CYCLE2CYCLEDELAY	R/W	0h	Chip-select high pulse delay between successive accesses 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... Fh = 15 GPMC_FCLK cycles
7	CYCLE2CYCLESAMECS EN	R/W	0h	Add CYCLE2CYCLEDELAY between successive accesses to the same chip-select (any access type) 0h (R/W) = No delay between the two accesses 1h (R/W) = Add CYCLE2CYCLEDELAY

Table 16-34. GPMC_CONFIG6_i Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CYCLE2CYCLEDIFFCSE N	R/W	0h	Add CYCLE2CYCLEDELAY between successive accesses to a different chip-select (any access type) 0h (R/W) = No delay between the two accesses 1h (R/W) = Add CYCLE2CYCLEDELAY
5-4	RESERVED	R	0h	Write 0s for future compatibility. Reads return 0.
3-0	BUSTURNAROUND	R/W	0h	Bus turnaround latency between successive accesses to the same chip-select (read to write) or to a different chip-select (read to read and read to write) 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... Fh = 15 GPMC_FCLK cycles

16.17 GPMC_CONFIG7_i Register (Offset = 78h + formula) [reset = F40h]

GPMC_CONFIG7_i (where i = 0 to 3) is shown in [Figure 16-17](#) and described in [Table 16-36](#).

CS address mapping configuration

Offset = 78h + (i * 30h), where: i = 0 to 3

Table 16-35. GPMC_CONFIG7_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0078h + formula

Figure 16-17. GPMC_CONFIG7_i Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				MASKADDRESS			
R-0h				R/W-Fh			
7	6	5	4	3	2	1	0
RESERVED	CSVALID	BASEADDRESS					
R-0h	R/W-1h	R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-36. GPMC_CONFIG7_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
11-8	MASKADDRESS	R/W	Fh	CS mask address. 0000h = Chip-select size of 256MB 1000h = Chip-select size of 128MB 1100h = Chip-select size of 64MB 1110h = Chip-select size of 32MB 1111h = Chip-select size of 16MB Other values must be avoided as they create holes in the chip-select address space.
7	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
6	CSVALID	R/W	1h	CS enable NOTE: Reset value is 1h for CS0 and 0h for CS1 to CS3 0h (R/W) = CS disabled 1h (R/W) = CS enabled
5-0	BASEADDRESS	R/W	0h	CSi base address where i = 0 to 3 (16-MB minimum granularity) bits [5-0] corresponds to A29, A28, A27, A26, A25, and A24. See .

16.18 GPMC_NAND_COMMAND_i Register (Offset = 7Ch + formula) [reset = -h]

GPMC_NAND_COMMAND_i (where i = 0 to 3) is shown in [Figure 16-18](#) and described in [Table 16-38](#).

This register is not a true register, only an address location.

Offset = 7Ch + (i * 30h), where: i = 0 to 3

Table 16-37. GPMC_NAND_COMMAND_i Instances

Instance	Physical Address
GPMC0_CFG	0539 007Ch + formula

Figure 16-18. GPMC_NAND_COMMAND_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_COMMAND																															
W-																															

LEGEND: W = Write Only; -n = value after reset

Table 16-38. GPMC_NAND_COMMAND_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPMC_NAND_COMMAND	W	-h	This register is not a true register, only an address location. Writing data at the GPMC_NAND_COMMAND_i location places the data as the NAND command value on the bus, using a regular asynchronous write access.

16.19 GPMC_NAND_ADDRESS_i Register (Offset = 80h + formula) [reset = -h]

GPMC_NAND_ADDRESS_i (where i = 0 to 3) is shown in [Figure 16-19](#) and described in [Table 16-40](#).

This register is not a true register, only an address location.

Offset = 80h + (i * 30h), where: i = 0 to 3

Table 16-39. GPMC_NAND_ADDRESS_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0080h + formula

Figure 16-19. GPMC_NAND_ADDRESS_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_ADDRESS																															
W-																															

LEGEND: W = Write Only; -n = value after reset

Table 16-40. GPMC_NAND_ADDRESS_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPMC_NAND_ADDRESS	W	-h	This register is not a true register, only an address location. Writing data at the GPMC_NAND_ADDRESS_i location places the data as the NAND partial address value on the bus, using a regular asynchronous write access.

16.20 GPMC_NAND_DATA_i Register (Offset = 84h + formula) [reset = -h]

GPMC_NAND_DATA_i (where i = 0 to 3) is shown in [Figure 16-20](#) and described in [Table 16-42](#).

This register is not a true register, only an address location.

Offset = 84h + (i * 30h), where: i = 0 to 3

Table 16-41. GPMC_NAND_DATA_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0084h + formula

Figure 16-20. GPMC_NAND_DATA_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_NAND_DATA																															
R/W-																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-42. GPMC_NAND_DATA_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPMC_NAND_DATA	R/W	-h	This register is not a true register, only an address location. Reading data from the GPMC_NAND_DATA_i location or from any location in the associated chip-select memory region activates an asynchronous read access.

16.21 GPMC_PREFETCH_CONFIG1 Register (Offset = 1E0h) [reset = 4000h]

GPMC_PREFETCH_CONFIG1 is shown in [Figure 16-21](#) and described in [Table 16-44](#).

Prefetch engine configuration 1

Note

Some of the GPMC features described in this section may not be supported on this family of devices. For more information, see *GPMC Not Supported Features*.

Table 16-43. GPMC_PREFETCH_CONFIG1 Instances

Instance	Physical Address
GPMC0_CFG	0539 01E0h

Figure 16-21. GPMC_PREFETCH_CONFIG1 Register

31	30	29	28	27	26	25	24
RESERVED	CYCLEOPTIMIZATION			ENABLEOPTIM IZEDACCESS	ENGINECSSELECTOR		
R-0h	R/W-0h			R/W-0h	R/W-0h		
23	22	21	20	19	18	17	16
PFPWENROUN DROBIN	RESERVED			PFPWWEIGHTEDPRIO			
R/W-0h	R-0h			R/W-0h			
15	14	13	12	11	10	9	8
RESERVED	FIFOTHRESHOLD						
R-0h	R/W-40h						
7	6	5	4	3	2	1	0
ENABLEENGIN E	RESERVED	WAITPINSELECTOR		SYNCHROMO DE	DMAMODE	ENDIANISMTY PE	ACCESSMODE
R/W-0h	R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-44. GPMC_PREFETCH_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
30-28	CYCLEOPTIMIZATION	R/W	0h	Define the number of GPMC_FCLK cycles to be subtracted from RDCYCLETIME, WRCYCLETIME, RDACCESSTIME, CSRDOFFTIME, CSWROFFTIME, ADVRDOFFTIME, ADVWROFFTIME, OEOFFTIME, WEOFFTIME 0h = 0 GPMC_FCLK cycle 1h = 1 GPMC_FCLK cycle ... 7h = 7 GPMC_FCLK cycles
27	ENABLEOPTIMIZEDACC ESS	R/W	0h	Enables access cycle optimization 0h (R/W) = Access cycle optimization is disabled. 1h (R/W) = Access cycle optimization is enabled.
26-24	ENGINECSSELECTOR	R/W	0h	Selects the chip-select where Prefetch Postwrite engine is active 0h = CS0 1h = CS1 2h = CS2 3h = CS3 4h-7h = Reserved

Table 16-44. GPMC_PREFETCH_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	PFPWENROUNDROBIN	R/W	0h	Enables the PFPW RoundRobin arbitration 0h (R/W) = Prefetch Postwrite engine round robin arbitration is disabled. 1h (R/W) = Prefetch Postwrite engine round robin arbitration is enabled.
22-20	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
19-16	PFPWWEIGHTEDPRIO	R/W	0h	When an arbitration occurs between a DMA and a PFPW engine access, the DMA is always serviced. If the PFPWEnRoundRobin is enabled, 0h = The next access is granted to the PFPW engine. 1h = The next two accesses are granted to the PFPW engine. ... Fh = The next 16 accesses are granted to the PFPW engine.
15	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
14-8	FIFOTHRESHOLD	R/W	40h	Selects the maximum number of bytes read from the FIFO or written to the FIFO by the host on a DMA or interrupt request 00h = 0 byte 01h = 1 byte ... 40h = 64 bytes
7	ENABLEENGINE	R/W	0h	Enables the Prefetch Postwrite engine 0h (R/W) = Prefetch Postwrite engine is disabled. 1h (R/W) = Prefetch Postwrite engine is enabled.
6	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
5-4	WAITPINSELECTOR	R/W	0h	Select which wait pin edge detector should start the engine in synchronized mode 0h (R/W) = Selects Wait0 EdgeDetection 1h (R/W) = Selects Wait1 EdgeDetection 2h (R/W) = Reserved 3h (R/W) = Reserved
3	SYNCHROMODE	R/W	0h	Selects when the engine starts the access to chip-select 0h (R/W) = Engine starts the access to chip-select as soon as STARTENGINE is set 1h (R/W) = Engine starts the access to chip-select as soon as STARTENGINE is set AND wait to nonwait edge detection on the selected WAIT pin
2	DMAMODE	R/W	0h	Selects interrupt synchronization or DMA request synchronization 0h (R/W) = Interrupt synchronization is enabled. Only interrupt line is activated on FIFO threshold crossing. 1h (R/W) = DMA request synchronization is enabled. A DMA request protocol is used.
1	ENDIANISMTYPE	R/W	0h	Selects endianism for prefetch data 0h = Little endian 1h = Bit endian
0	ACCESSMODE	R/W	0h	Selects prefetch read or write-posting accesses 0h (R/W) = Prefetch read mode 1h (R/W) = Write-posting mode

16.22 GPMC_PREFETCH_CONFIG2 Register (Offset = 1E4h) [reset = 0h]

GPMC_PREFETCH_CONFIG2 is shown in [Figure 16-22](#) and described in [Table 16-46](#).

Prefetch engine configuration 2

Table 16-45. GPMC_PREFETCH_CONFIG2 Instances

Instance	Physical Address
GPMC0_CFG	0539 01E4h

Figure 16-22. GPMC_PREFETCH_CONFIG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TRANSFERCOUNT													
R-0h																		R/W-0h													

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-46. GPMC_PREFETCH_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
13-0	TRANSFERCOUNT	R/W	0h	Selects the number of bytes to be read or written by the engine to the selected chip-select 0000h = 0 byte 0001h = 1 byte ... 2000h = 8K bytes

16.23 GPMC_PREFETCH_CONTROL Register (Offset = 1ECh) [reset = 0h]

GPMC_PREFETCH_CONTROL is shown in [Figure 16-23](#) and described in [Table 16-48](#).

Prefetch engine control

**Table 16-47. GPMC_PREFETCH_CONTROL
Instances**

Instance	Physical Address
GPMC0_CFG	0539 01ECh

Figure 16-23. GPMC_PREFETCH_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							STARTENGINE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-48. GPMC_PREFETCH_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
0	STARTENGINE	R/W	0h	Resets the FIFO pointer and starts the engine Write: 0h = Stops the engine. 1h = Resets the FIFO pointer to 0h in prefetch mode and 40h in postwrite mode and starts the engine. Read: 0h = Engine is stopped. 1h = Engine is running.

16.24 GPMC_PREFETCH_STATUS Register (Offset = 1F0h) [reset = 0h]

GPMC_PREFETCH_STATUS is shown in [Figure 16-24](#) and described in [Table 16-50](#).

Prefetch engine status

Table 16-49. GPMC_PREFETCH_STATUS Instances

Instance	Physical Address
GPMC0_CFG	0539 01F0h

Figure 16-24. GPMC_PREFETCH_STATUS Register

31	30	29	28	27	26	25	24
RESERVED	FIFOPOINTER						
R-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							FIFOTHRESHOLDSTATUS
R-0h							R-0h
15	14	13	12	11	10	9	8
RESERVED			COUNTVALUE				
R-0h			R-0h				
7	6	5	4	3	2	1	0
COUNTVALUE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 16-50. GPMC_PREFETCH_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0.
30-24	FIFOPOINTER	R	0h	Number of available bytes to be read or number of free empty byte places to be written 00h = 0 byte available to be read or 0 free empty place to be written ... 40h = 64 bytes available to be read or 64 empty places to be written
23-17	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
16	FIFOTHRESHOLDSTATUS	R	0h	Set when FIFOPointer exceeds FIFOThreshold value 0h (R) = FIFOPointer smaller or equal to FIFOThreshold. Writing to this bit has no effect. 1h (R) = FIFOPointer greater than FIFOThreshold. Writing to this bit has no effect.
15-14	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
13-0	COUNTVALUE	R	0h	Number of remaining bytes to be read or to be written by the engine according to the TransferCount value 0000h = 0 byte remaining to be read or to be written 0001h = 1 byte remaining to be read or to be written ... 2000h = 8KB remaining to be read or to be written

16.25 GPMC_ECC_CONFIG Register (Offset = 1F4h) [reset = 1030h]

GPMC_ECC_CONFIG is shown in [Figure 16-25](#) and described in [Table 16-52](#).

ECC configuration

Table 16-51. GPMC_ECC_CONFIG Instances

Instance	Physical Address
GPMC0_CFG	0539 01F4h

Figure 16-25. GPMC_ECC_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							ECCALGORITHM
R-0h							M
							R/W-0h
15	14	13	12	11	10	9	8
RESERVED		ECCBCHTSEL			ECCWRAPMODE		
R-0h		R/W-1h			R/W-0h		
7	6	5	4	3	2	1	0
ECC16B	ECCTOPSECTOR			ECCCS		ECCENABLE	
R/W-0h	R/W-3h			R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-52. GPMC_ECC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
16	ECCALGORITHM	R/W	0h	ECC algorithm used 0h (R/W) = Hamming code 1h (R/W) = BCH code
15-14	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
13-12	ECCBCHTSEL	R/W	1h	Error correction capability used for BCH 0h (R/W) = Up to 4 bits error correction (t = 4) 1h (R/W) = Up to 8 bits error correction (t = 8) 2h (R/W) = Up to 16 bits error correction (t = 16) 3h (R/W) = Reserved
11-8	ECCWRAPMODE	R/W	0h	Spare area organization definition for the BCH algorithm. See the BCH syndrome/parity calculator module functional specification for more details
7	ECC16B	R/W	0h	Selects an ECC calculated on 16 columns 0h (R/W) = ECC calculated on 8 columns 1h (R/W) = ECC calculated on 16 columns
6-4	ECCTOPSECTOR	R/W	3h	Number of sectors to process with the BCH algorithm 0h = 1 sector (512-KB page) 1h = 2 sectors ... 3h = 4 sectors (2-KB page) ... 7h = 8 sectors (4-KB page)

Table 16-52. GPMC_ECC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	ECCCS	R/W	0h	Selects the CS where ECC is computed 0h (R/W) = CS0 1h (R/W) = CS1 2h (R/W) = CS2 3h (R/W) = CS3 Other: Reserved
0	ECCENABLE	R/W	0h	Enables the ECC feature 0h (R/W) = ECC disabled 1h (R/W) = ECC enabled

16.26 GPMC_ECC_CONTROL Register (Offset = 1F8h) [reset = 0h]

GPMC_ECC_CONTROL is shown in [Figure 16-26](#) and described in [Table 16-54](#).

ECC control

Table 16-53. GPMC_ECC_CONTROL Instances

Instance	Physical Address
GPMC0_CFG	0539 01F8h

Figure 16-26. GPMC_ECC_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							ECCCLEAR
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				ECCPOINTER			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-54. GPMC_ECC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
8	ECCCLEAR	R/W	0h	Clear all ECC result registers Reads return 0. Write 1h to this field clears all ECC result registers. Write 0h is ignored.
7-4	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
3-0	ECCPOINTER	R/W	0h	Selects ECC result register (Reads to this field give the dynamic position of the ECC pointer - Writes to this field select the ECC result register where the first ECC computation will be stored.); Writing other values disables the ECC engine (ECCENABLE bit of GPMC_ECC_CONFIG set to 0) 0h (R/W) = Writing 0h disables the ECC engine (ECCENABLE bit of GPMC_ECC_CONFIG set to 0) 1h (R/W) = ECC result register 1 selected 2h (R/W) = ECC result register 2 selected 3h (R/W) = ECC result register 3 selected 4h (R/W) = ECC result register 4 selected 5h (R/W) = ECC result register 5 selected 6h (R/W) = ECC result register 6 selected 7h (R/W) = ECC result register 7 selected 8h (R/W) = ECC result register 8 selected 9h (R/W) = ECC result register 9 selected

16.27 GPMC_ECC_SIZE_CONFIG Register (Offset = 1FCh) [reset = FFFF000h]

GPMC_ECC_SIZE_CONFIG is shown in [Figure 16-27](#) and described in [Table 16-56](#).

ECC size

Table 16-55. GPMC_ECC_SIZE_CONFIG Instances

Instance	Physical Address
GPMC0_CFG	0539 01FCh

Figure 16-27. GPMC_ECC_SIZE_CONFIG Register

31	30	29	28	27	26	25	24
ECCSIZE1							
R/W-3FFh							
23	22	21	20	19	18	17	16
ECCSIZE1		ECCSIZE0					
R/W-3FFh		R/W-3FFh					
15	14	13	12	11	10	9	8
ECCSIZE0				RESERVED			ECC9RESULTS IZE
R/W-3FFh				R-0h			R/W-0h
7	6	5	4	3	2	1	0
ECC8RESULTS IZE	ECC7RESULTS IZE	ECC6RESULTS IZE	ECC5RESULTS IZE	ECC4RESULTS IZE	ECC3RESULTS IZE	ECC2RESULTS IZE	ECC1RESULTS IZE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-56. GPMC_ECC_SIZE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	ECCSIZE1	R/W	3FFh	<p>Defines ECC size 1.</p> <p>For Hamming Code:</p> <p>000h corresponds to 2 Bytes,</p> <p>001h corresponds to 4 Bytes,</p> <p>002h corresponds to 6 Bytes,</p> <p>003h corresponds to 8 Bytes,</p> <p>...</p> <p>0FFh corresponds to 512 Bytes.</p> <p>Max supported value is 0FFh.</p> <p>For BCH:</p> <p>000h corresponds to 0 nibbles,</p> <p>001h corresponds to 1 nibble,</p> <p>002h corresponds to 2 nibbles,</p> <p>003h corresponds to 3 nibbles,</p> <p>...</p> <p>3FFh corresponds to 1023 nibbles.</p>

Table 16-56. GPMC_ECC_SIZE_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-12	ECCSIZE0	R/W	3FFh	Defines ECC size 0. For Hamming Code: 000h corresponds to 2 Bytes, 001h corresponds to 4 Bytes, 002h corresponds to 6 Bytes, 003h corresponds to 8 Bytes, ... 0FFh corresponds to 512 Bytes. Max supported value is 0FFh. For BCH: 000h corresponds to 0 nibbles, 001h corresponds to 1 nibble, 002h corresponds to 2 nibbles, 003h corresponds to 3 nibbles, ... 3FFh corresponds to 1023 nibbles.
11-9	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
8	ECC9RESULTSIZ	R/W	0h	Selects ECC size for ECC 9 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected
7	ECC8RESULTSIZ	R/W	0h	Selects ECC size for ECC 8 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected
6	ECC7RESULTSIZ	R/W	0h	Selects ECC size for ECC 7 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected
5	ECC6RESULTSIZ	R/W	0h	Selects ECC size for ECC 6 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected
4	ECC5RESULTSIZ	R/W	0h	Selects ECC size for ECC 5 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected
3	ECC4RESULTSIZ	R/W	0h	Selects ECC size for ECC 4 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected
2	ECC3RESULTSIZ	R/W	0h	Selects ECC size for ECC 3 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected
1	ECC2RESULTSIZ	R/W	0h	Selects ECC size for ECC 2 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected
0	ECC1RESULTSIZ	R/W	0h	Selects ECC size for ECC 1 result register 0h (R/W) = ECCSIZE0 selected 1h (R/W) = ECCSIZE1 selected

16.28 GPMC_ECCj_RESULT Register (Offset = 200h + formula) [reset = 0h]

GPMC_ECCj_RESULT (where j = 0 to 8) is shown in [Figure 16-28](#) and described in [Table 16-58](#).

ECC result register

Offset = 200h + (j * 4h), where: j = 0 to 8

Table 16-57. GPMC_ECCj_RESULT Instances

Instance	Physical Address
GPMC0_CFG	0539 0200h + formula

Figure 16-28. GPMC_ECCj_RESULT Register

31	30	29	28	27	26	25	24
RESERVED				P2048O	P1024O	P512O	P256O
R-0h				R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
P128O	P64O	P32O	P16O	P8O	P4O	P2O	P1O
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED				P2048E	P1024E	P512E	P256E
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
P128E	P64E	P32E	P16E	P8E	P4E	P2E	P1E
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 16-58. GPMC_ECCj_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
27	P2048O	R	0h	Odd row parity bit 2048, only used for ECC computed on 512 bytes
26	P1024O	R	0h	Odd row parity bit 1024
25	P512O	R	0h	Odd row parity bit 512
24	P256O	R	0h	Odd row parity bit 256
23	P128O	R	0h	Odd row parity bit 128
22	P64O	R	0h	Odd row parity bit 64
21	P32O	R	0h	Odd row parity bit 32
20	P16O	R	0h	Odd row parity bit 16
19	P8O	R	0h	Odd row parity bit 8
18	P4O	R	0h	Odd Column Parity bit 4
17	P2O	R	0h	Odd Column Parity bit 2
16	P1O	R	0h	Odd Column Parity bit 1
15-12	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
11	P2048E	R	0h	Even row parity bit 2048, only used for ECC computed on 512 bytes
10	P1024E	R	0h	Even row parity bit 1024
9	P512E	R	0h	Even row parity bit 512
8	P256E	R	0h	Even row parity bit 256

Table 16-58. GPMC_ECCj_RESULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	P128E	R	0h	Even row parity bit 128
6	P64E	R	0h	Even row parity bit 64
5	P32E	R	0h	Even row parity bit 32
4	P16E	R	0h	Even row parity bit 16
3	P8E	R	0h	Even row parity bit 8
2	P4E	R	0h	Even column parity bit 4
1	P2E	R	0h	Even column parity bit 2
0	P1E	R	0h	Even column parity bit 1

16.29 GPMC_BCH_RESULT0_i Register (Offset = 240h + formula) [reset = 0h]

GPMC_BCH_RESULT0_i (where i = 0 to 3) is shown in [Figure 16-29](#) and described in [Table 16-60](#).

BCH ECC result (bits 0 to 31)

Offset = 240h + (i * 10h), where: i = 0 to 3

Table 16-59. GPMC_BCH_RESULT0_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0240h + formula

Figure 16-29. GPMC_BCH_RESULT0_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 16-60. GPMC_BCH_RESULT0_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCH_RESULT_0	R	0h	BCH ECC result (bits 0 to 31)

16.30 GPMC_BCH_RESULT1_i Register (Offset = 244h + formula) [reset = 0h]

GPMC_BCH_RESULT1_i (where i = 0 to 3) is shown in [Figure 16-30](#) and described in [Table 16-62](#).

BCH ECC result (bits 32 to 63)

Offset = 244h + (i * 10h), where: i = 0 to 3

Table 16-61. GPMC_BCH_RESULT1_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0244h + formula

Figure 16-30. GPMC_BCH_RESULT1_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 16-62. GPMC_BCH_RESULT1_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCH_RESULT_1	R	0h	BCH ECC result (bits 32 to 63)

16.31 GPMC_BCH_RESULT2_i Register (Offset = 248h + formula) [reset = 0h]

GPMC_BCH_RESULT2_i (where i = 0 to 3) is shown in [Figure 16-31](#) and described in [Table 16-64](#).

BCH ECC result (bits 64 to 95)

Offset = 248h + (i * 10h), where: i = 0 to 3

Table 16-63. GPMC_BCH_RESULT2_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0248h + formula

Figure 16-31. GPMC_BCH_RESULT2_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 16-64. GPMC_BCH_RESULT2_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCH_RESULT_2	R	0h	BCH ECC result (bits 64 to 95)

16.32 GPMC_BCH_RESULT3_i Register (Offset = 24Ch + formula) [reset = 0h]

GPMC_BCH_RESULT3_i (where i = 0 to 3) is shown in [Figure 16-32](#) and described in [Table 16-66](#).

BCH ECC result (bits 96 to 127)

Offset = 24Ch + (i * 10h), where: i = 0 to 3

Table 16-65. GPMC_BCH_RESULT3_i Instances

Instance	Physical Address
GPMC0_CFG	0539 024Ch + formula

Figure 16-32. GPMC_BCH_RESULT3_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 16-66. GPMC_BCH_RESULT3_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCH_RESULT_3	R	0h	BCH ECC result (bits 96 to 127)

16.33 GPMC_BCH_SWDATA Register (Offset = 2D0h) [reset = 0h]

GPMC_BCH_SWDATA is shown in [Figure 16-33](#) and described in [Table 16-68](#).

This register is used to directly pass data to the BCH ECC calculator without accessing the actual NAND flash interface.

Table 16-67. GPMC_BCH_SWDATA Instances

Instance	Physical Address
GPMC0_CFG	0539 02D0h

Figure 16-33. GPMC_BCH_SWDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BCH_DATA															
R-0h																W-0h															

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 16-68. GPMC_BCH_SWDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
15-0	BCH_DATA	W	0h	Data to be included in the BCH calculation Only bits 0 to 7 are considered if the calculator is configured to use 8-bit data (GPMC_ECC_CONFIG[7] ECC16B = 0)

16.34 GPMC_BCH_RESULT4_i Register (Offset = 300h + formula) [reset = 0h]

GPMC_BCH_RESULT4_i (where i = 0 to 3) is shown in [Figure 16-34](#) and described in [Table 16-70](#).

BCH ECC result (bits 128 to 159)

Offset = 300h + (i * 10h), where: i = 0 to 3

Table 16-69. GPMC_BCH_RESULT4_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0300h + formula

Figure 16-34. GPMC_BCH_RESULT4_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_4																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 16-70. GPMC_BCH_RESULT4_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCH_RESULT_4	R	0h	BCH ECC result (bits 128 to 159)

16.35 GPMC_BCH_RESULT5_i Register (Offset = 304h + formula) [reset = 0h]

GPMC_BCH_RESULT5_i (where i = 0 to 3) is shown in [Figure 16-35](#) and described in [Table 16-72](#).

BCH ECC result (bits 160 to 191)

Offset = 304h + (i * 10h), where: i = 0 to 3

Table 16-71. GPMC_BCH_RESULT5_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0304h + formula

Figure 16-35. GPMC_BCH_RESULT5_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH_RESULT_5																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 16-72. GPMC_BCH_RESULT5_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCH_RESULT_5	R	0h	BCH ECC result (bits 160 to 191)

16.36 GPMC_BCH_RESULT6_i Register (Offset = 308h + formula) [reset = 0h]

GPMC_BCH_RESULT6_i (where i = 0 to 3) is shown in [Figure 16-36](#) and described in [Table 16-74](#).

BCH ECC result (bits 192 to 207)

Offset = 308h + (i * 10h), where: i = 0 to 3

Table 16-73. GPMC_BCH_RESULT6_i Instances

Instance	Physical Address
GPMC0_CFG	0539 0308h + formula

Figure 16-36. GPMC_BCH_RESULT6_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BCH_RESULT_6															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 16-74. GPMC_BCH_RESULT6_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Write 0s for future compatibility. Read returns 0s.
15-0	BCH_RESULT_6	R	0h	BCH ECC result (bits 192 to 207)

17 ELM Registers

Table 17-2 lists the memory-mapped registers for the ELM. All register offset addresses not listed in Table 17-2 should be considered as reserved locations and the register contents should not be modified.

Table 17-1. ELM Instances

Instance	Base Address
ELM0	0538 0000h

Table 17-2. ELM Registers

Offset	Acronym	Register Name	ELM0 Physical Address
0h	ELM_REVISION	IP revision	0538 0000h
10h	ELM_SYSCONFIG	Module software reset and local power management register	0538 0010h
14h	ELM_SYSSTATUS	Internal reset monitoring	0538 0014h
18h	ELM_IRQSTATUS	Interrupt status register	0538 0018h
1Ch	ELM_IRQENABLE	Interrupt enable register	0538 001Ch
20h	ELM_LOCATION_CONFIG	ECC algorithm parameters	0538 0020h
80h	ELM_PAGE_CTRL	Page definition	0538 0080h
400h + formula	ELM_SYNDROME_FRAGMENT_0_i	Input syndrome polynomial bits 0 to 31	0538 0400h + formula
404h + formula	ELM_SYNDROME_FRAGMENT_1_i	Input syndrome polynomial bits 32 to 63	0538 0404h + formula
408h + formula	ELM_SYNDROME_FRAGMENT_2_i	Input syndrome polynomial bits 64 to 95	0538 0408h + formula
40Ch + formula	ELM_SYNDROME_FRAGMENT_3_i	Input syndrome polynomial bits 96 to 127	0538 040Ch + formula
410h + formula	ELM_SYNDROME_FRAGMENT_4_i	Input syndrome polynomial bits 128 to 159	0538 0410h + formula
414h + formula	ELM_SYNDROME_FRAGMENT_5_i	Input syndrome polynomial bits 160 to 191	0538 0414h + formula
418h + formula	ELM_SYNDROME_FRAGMENT_6_i	Input syndrome polynomial bits 192 to 207	0538 0418h + formula
800h + formula	ELM_LOCATION_STATUS_i	Exit status for the syndrome polynomial processing	0538 0800h + formula
880h + formula	ELM_ERROR_LOCATION_0_i	Error-location register 0	0538 0880h + formula
884h + formula	ELM_ERROR_LOCATION_1_i	Error-location register 1	0538 0884h + formula
888h + formula	ELM_ERROR_LOCATION_2_i	Error-location register 2	0538 0888h + formula
88Ch + formula	ELM_ERROR_LOCATION_3_i	Error-location register 3	0538 088Ch + formula
890h + formula	ELM_ERROR_LOCATION_4_i	Error-location register 4	0538 0890h + formula
894h + formula	ELM_ERROR_LOCATION_5_i	Error-location register 5	0538 0894h + formula
898h + formula	ELM_ERROR_LOCATION_6_i	Error-location register 6	0538 0898h + formula
89Ch + formula	ELM_ERROR_LOCATION_7_i	Error-location register 7	0538 089Ch + formula
8A0h + formula	ELM_ERROR_LOCATION_8_i	Error-location register 8	0538 08A0h + formula
8A4h + formula	ELM_ERROR_LOCATION_9_i	Error-location register 9	0538 08A4h + formula
8A8h + formula	ELM_ERROR_LOCATION_10_i	Error-location register 10	0538 08A8h + formula
8ACh + formula	ELM_ERROR_LOCATION_11_i	Error-location register 11	0538 08ACh + formula
8B0h + formula	ELM_ERROR_LOCATION_12_i	Error-location register 12	0538 08B0h + formula
8B4h + formula	ELM_ERROR_LOCATION_13_i	Error-location register 13	0538 08B4h + formula
8B8h + formula	ELM_ERROR_LOCATION_14_i	Error-location register 14	0538 08B8h + formula
8BCh + formula	ELM_ERROR_LOCATION_15_i	Error-location register 15	0538 08BCh + formula

17.1 ELM_REVISION Register (Offset = 0h) [reset = 20h]

ELM_REVISION is shown in [Figure 17-1](#) and described in [Table 17-4](#).

This register contains the IP revision code.

(A write to or reset of this register has no effect.)

Table 17-3. ELM_REVISION Instances

Instance	Physical Address
ELM0	0538 0000h

Figure 17-1. ELM_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-20h																															

LEGEND: R = Read Only; -n = value after reset

Table 17-4. ELM_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	20h	TI internal data. Identifies revision of peripheral.

17.2 ELM_SYSCONFIG Register (Offset = 10h) [reset = 11h]

ELM_SYSCONFIG is shown in [Figure 17-2](#) and described in [Table 17-6](#).

This register controls ELM local power management and software reset.

Note

Some of the ELM features described in this section may not be supported on this family of devices. For more information, see *ELM Not Supported Features*.

Table 17-5. ELM_SYSCONFIG Instances

Instance	Physical Address
ELM0	0538 0010h

Figure 17-2. ELM_SYSCONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CLOCKACTIVI TYOCP
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED			SIDLEMODE		RESERVED	SOFTRESET	AUTOGATING
R-0h			R/W-2h		R-0h	R/W-0h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-6. ELM_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CLOCKACTIVITYOCP	R/W	0h	ELM_FICLK activity when module is in IDLE mode 0h (R/W) = ELM_FICLK can be switched off. 1h (R/W) = ELM_FICLK is maintained.
7-5	RESERVED	R	0h	Reserved
4-3	SIDLEMODE	R/W	2h	Slave interface power management (clock stop req/ack control) 0h (R/W) = Force-idle. A clock stop request is acknowledged unconditionally and immediately 1h (R/W) = No-idle. A clock stop request is never acknowledged. 2h (R/W) = Smart-idle. The acknowledgment to a clock stop request is given based on the internal activity. 3h (R/W) = Reserved — do not use
2	RESERVED	R	0h	Reserved
1	SOFTRESET	R/W	0h	Module software reset This bit is automatically reset by hardware (during reads, it always returns 0). It has same effect as ELM_RST. 0h (R/W) = Normal mode 1h (R/W) = Start soft reset sequence.

Table 17-6. ELM_SYSCONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AUTOGATING	R/W	1h	<p>Internal ELM_FICLK gating strategy (no module visible effect other than saving power)</p> <p>0h (R/W) = ELM_FICLK is free-running.</p> <p>1h (R/W) = Automatic internal ELM_FICLK gating strategy is applied based on the Interconnect interface activity.</p>

17.3 ELM_SYSSTATUS Register (Offset = 14h) [reset = 0h]

ELM_SYSSTATUS is shown in [Figure 17-3](#) and described in [Table 17-8](#).

Internal reset monitoring

Undefined since:

From hardware perspective, the reset state is 0.

From software user perspective, when the accessible module is 1.

Table 17-7. ELM_SYSSTATUS Instances

Instance	Physical Address
ELM0	0538 0014h

Figure 17-3. ELM_SYSSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RESETDONE
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 17-8. ELM_SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RESETDONE	R	0h	Internal reset monitoring Undefined since: From hardware perspective, the reset state is 0. From software user perspective, when the accessible module is 1. 0h (R) = Reset is ongoing. 1h (R) = Reset is done (completed).

17.4 ELM_IRQSTATUS Register (Offset = 18h) [reset = 0h]

ELM_IRQSTATUS is shown in [Figure 17-4](#) and described in [Table 17-10](#).

Interrupt status. This register doubles as a status register for the error-location processes.

Table 17-9. ELM_IRQSTATUS Instances

Instance	Physical Address
ELM0	0538 0018h

Figure 17-4. ELM_IRQSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							PAGE_VALID
R-0h							R/W1C-0h
7	6	5	4	3	2	1	0
LOC_VALID_7	LOC_VALID_6	LOC_VALID_5	LOC_VALID_4	LOC_VALID_3	LOC_VALID_2	LOC_VALID_1	LOC_VALID_0
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 17-10. ELM_IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	PAGE_VALID	R/W1C	0h	Error-location status for a full page, based on the mask definition Read 0h = Error locations invalid for all polynomials enabled in the ECC_INTERRUPT_MASK register Read 1h = All error locations valid Write 0h = No effect Write 1h = Clear interrupt
7	LOC_VALID_7	R/W1C	0h	Error-location status for syndrome polynomial 7 Read 0h = No syndrome processed or process in progress Read 1h = Error-location process completed Write 0h = No effect Write 1h = Clear interrupt
6	LOC_VALID_6	R/W1C	0h	Error-location status for syndrome polynomial 6
5	LOC_VALID_5	R/W1C	0h	Error-location status for syndrome polynomial 5
4	LOC_VALID_4	R/W1C	0h	Error-location status for syndrome polynomial 4
3	LOC_VALID_3	R/W1C	0h	Error-location status for syndrome polynomial 3
2	LOC_VALID_2	R/W1C	0h	Error-location status for syndrome polynomial 2
1	LOC_VALID_1	R/W1C	0h	Error-location status for syndrome polynomial 1
0	LOC_VALID_0	R/W1C	0h	Error-location status for syndrome polynomial 0

17.5 ELM_IRQENABLE Register (Offset = 1Ch) [reset = 0h]

ELM_IRQENABLE is shown in [Figure 17-5](#) and described in [Table 17-12](#).

Interrupt enable.

Table 17-11. ELM_IRQENABLE Instances

Instance	Physical Address
ELM0	0538 001Ch

Figure 17-5. ELM_IRQENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							PAGE_MASK
R-0h							R/W-0h
7	6	5	4	3	2	1	0
LOCATION_MA SK_7	LOCATION_MA SK_6	LOCATION_MA SK_5	LOCATION_MA SK_4	LOCATION_MA SK_3	LOCATION_MA SK_2	LOCATION_MA SK_1	LOCATION_MA SK_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-12. ELM_IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	PAGE_MASK	R/W	0h	Page interrupt mask bit 0h = Disable interrupt 1h = Enable interrupt
7	LOCATION_MASK_7	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 7
6	LOCATION_MASK_6	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 6
5	LOCATION_MASK_5	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 5
4	LOCATION_MASK_4	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 4
3	LOCATION_MASK_3	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 3
2	LOCATION_MASK_2	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 2
1	LOCATION_MASK_1	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 1
0	LOCATION_MASK_0	R/W	0h	Error-location interrupt mask bit for syndrome polynomial 0 0h = Disable interrupt 1h = Enable interrupt

17.6 ELM_LOCATION_CONFIG Register (Offset = 20h) [reset = 0h]

ELM_LOCATION_CONFIG is shown in [Figure 17-6](#) and described in [Table 17-14](#).

ECC algorithm parameters.

Table 17-13. ELM_LOCATION_CONFIG Instances

Instance	Physical Address
ELM0	0538 0020h

Figure 17-6. ELM_LOCATION_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED					ECC_SIZE		
R-0h					R/W-0h		
23	22	21	20	19	18	17	16
ECC_SIZE							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						ECC_BCH_LEVEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-14. ELM_LOCATION_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	0h	Reserved
26-16	ECC_SIZE	R/W	0h	Maximum size of the buffers for which the error-location engine is used, in number of nibbles (4-bit entities)
15-2	RESERVED	R	0h	Reserved
1-0	ECC_BCH_LEVEL	R/W	0h	Error correction level 0h = 4 bits 1h = 8 bits 2h = 16 bits 3h = Reserved

17.7 ELM_PAGE_CTRL Register (Offset = 80h) [reset = 0h]

ELM_PAGE_CTRL is shown in [Figure 17-7](#) and described in [Table 17-16](#).

Page definition.

Table 17-15. ELM_PAGE_CTRL Instances

Instance	Physical Address
ELM0	0538 0080h

Figure 17-7. ELM_PAGE_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SECTOR_7	SECTOR_6	SECTOR_5	SECTOR_4	SECTOR_3	SECTOR_2	SECTOR_1	SECTOR_0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-16. ELM_PAGE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	SECTOR_7	R/W	0h	Set to 1 if syndrome polynomial 7 is part of the page in page mode. Must be 0 in continuous mode.
6	SECTOR_6	R/W	0h	Set to 1 if syndrome polynomial 6 is part of the page in page mode. Must be 0 in continuous mode.
5	SECTOR_5	R/W	0h	Set to 1 if syndrome polynomial 5 is part of the page in page mode. Must be 0 in continuous mode.
4	SECTOR_4	R/W	0h	Set to 1 if syndrome polynomial 4 is part of the page in page mode. Must be 0 in continuous mode.
3	SECTOR_3	R/W	0h	Set to 1 if syndrome polynomial 3 is part of the page in page mode. Must be 0 in continuous mode.
2	SECTOR_2	R/W	0h	Set to 1 if syndrome polynomial 2 is part of the page in page mode. Must be 0 in continuous mode.
1	SECTOR_1	R/W	0h	Set to 1 if syndrome polynomial 1 is part of the page in page mode. Must be 0 in continuous mode.
0	SECTOR_0	R/W	0h	Set to 1 if syndrome polynomial 0 is part of the page in page mode. Must be 0 in continuous mode.

17.8 ELM_SYNDROME_FRAGMENT_0_i Register (Offset = 400h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_0_i (where i = 0 to 7) is shown in [Figure 17-8](#) and described in [Table 17-18](#).

Input syndrome polynomial bits 0 to 31.

Offset = 400h + (i * 40h), where: i = 0 to 7

**Table 17-17. ELM_SYNDROME_FRAGMENT_0_i
Instances**

Instance	Physical Address
ELM0	0538 0400h + formula

Figure 17-8. ELM_SYNDROME_FRAGMENT_0_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-18. ELM_SYNDROME_FRAGMENT_0_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_0	R/W	0h	Syndrome bits 0 to 31

17.9 ELM_SYNDROME_FRAGMENT_1_i Register (Offset = 404h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_1_i (where i = 0 to 7) is shown in [Figure 17-9](#) and described in [Table 17-20](#).

Input syndrome polynomial bits 32 to 63.

Offset = 404h + (i * 40h), where: i = 0 to 7

Table 17-19. ELM_SYNDROME_FRAGMENT_1_i Instances

Instance	Physical Address
ELM0	0538 0404h + formula

Figure 17-9. ELM_SYNDROME_FRAGMENT_1_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-20. ELM_SYNDROME_FRAGMENT_1_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_1	R/W	0h	Syndrome bits 32 to 63

17.10 ELM_SYNDROME_FRAGMENT_2_i Register (Offset = 408h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_2_i (where i = 0 to 7) is shown in [Figure 17-10](#) and described in [Table 17-22](#).

Input syndrome polynomial bits 64 to 95.

Offset = 408h + (i * 40h), where: i = 0 to 7

**Table 17-21. ELM_SYNDROME_FRAGMENT_2_i
Instances**

Instance	Physical Address
ELM0	0538 0408h + formula

Figure 17-10. ELM_SYNDROME_FRAGMENT_2_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-22. ELM_SYNDROME_FRAGMENT_2_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_2	R/W	0h	Syndrome bits 64 to 95

17.11 ELM_SYNDROME_FRAGMENT_3_i Register (Offset = 40Ch + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_3_i (where i = 0 to 7) is shown in [Figure 17-11](#) and described in [Table 17-24](#).

Input syndrome polynomial bits 96 to 127.

Offset = 40Ch + (i * 40h), where: i = 0 to 7

Table 17-23. ELM_SYNDROME_FRAGMENT_3_i Instances

Instance	Physical Address
ELM0	0538 040Ch + formula

Figure 17-11. ELM_SYNDROME_FRAGMENT_3_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-24. ELM_SYNDROME_FRAGMENT_3_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_3	R/W	0h	Syndrome bits 96 to 127

17.12 ELM_SYNDROME_FRAGMENT_4_i Register (Offset = 410h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_4_i (where i = 0 to 7) is shown in [Figure 17-12](#) and described in [Table 17-26](#).

Input syndrome polynomial bits 128 to 159.

Offset = 410h + (i * 40h), where: i = 0 to 7

**Table 17-25. ELM_SYNDROME_FRAGMENT_4_i
Instances**

Instance	Physical Address
ELM0	0538 0410h + formula

Figure 17-12. ELM_SYNDROME_FRAGMENT_4_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_4																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-26. ELM_SYNDROME_FRAGMENT_4_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_4	R/W	0h	Syndrome bits 128 to 159

17.13 ELM_SYNDROME_FRAGMENT_5_i Register (Offset = 414h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_5_i (where i = 0 to 7) is shown in [Figure 17-13](#) and described in [Table 17-28](#).

Input syndrome polynomial bits 160 to 191.

Offset = 414h + (i * 40h), where: i = 0 to 7

Table 17-27. ELM_SYNDROME_FRAGMENT_5_i Instances

Instance	Physical Address
ELM0	0538 0414h + formula

Figure 17-13. ELM_SYNDROME_FRAGMENT_5_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNDROME_5																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-28. ELM_SYNDROME_FRAGMENT_5_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNDROME_5	R/W	0h	Syndrome bits 160 to 191

17.14 ELM_SYNDROME_FRAGMENT_6_i Register (Offset = 418h + formula) [reset = 0h]

ELM_SYNDROME_FRAGMENT_6_i (where i = 0 to 7) is shown in [Figure 17-14](#) and described in [Table 17-30](#).

Input syndrome polynomial bits 192 to 207.

Offset = 418h + (i * 40h), where: i = 0 to 7

**Table 17-29. ELM_SYNDROME_FRAGMENT_6_i
Instances**

Instance	Physical Address
ELM0	0538 0418h + formula

Figure 17-14. ELM_SYNDROME_FRAGMENT_6_i Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							SYNDROME_V ALID
R-0h							R/W-0h
15	14	13	12	11	10	9	8
SYNDROME_6							
R/W-0h							
7	6	5	4	3	2	1	0
SYNDROME_6							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-30. ELM_SYNDROME_FRAGMENT_6_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	SYNDROME_VALID	R/W	0h	Syndrome valid bit 0h = This syndrome polynomial must not be processed. 1h = This syndrome polynomial must be processed.
15-0	SYNDROME_6	R/W	0h	Syndrome bits 192 to 207

17.15 ELM_LOCATION_STATUS_i Register (Offset = 800h + formula) [reset = 0h]

ELM_LOCATION_STATUS_i (where i = 0 to 7) is shown in [Figure 17-15](#) and described in [Table 17-32](#).

Exit status for the syndrome polynomial processing.

Offset = 800h + (i * 100h), where: i = 0 to 7

Table 17-31. ELM_LOCATION_STATUS_i Instances

Instance	Physical Address
ELM0	0538 0800h + formula

Figure 17-15. ELM_LOCATION_STATUS_i Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							ECC_CORREC TABLE
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED			ECC_NB_ERRORS				
R-0h			R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 17-32. ELM_LOCATION_STATUS_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	ECC_CORRECTABLE	R	0h	Error-location process exit status 0h = ECC error-location process failed. Number of errors and error locations are invalid. 1h = All errors were successfully located. Number of errors and error locations are valid.
7-5	RESERVED	R	0h	Reserved
4-0	ECC_NB_ERRORS	R	0h	Number of errors detected and located

17.16 ELM_ERROR_LOCATION_0_i Register (Offset = 880h + formula) [reset = 0h]

ELM_ERROR_LOCATION_0_i (where i = 0 to 7) is shown in [Figure 17-16](#) and described in [Table 17-34](#).

Error-location register 0.

Offset = 880h + (i * 100h), where: i = 0 to 7

Table 17-33. ELM_ERROR_LOCATION_0_i Instances

Instance	Physical Address
ELM0	0538 0880h + formula

Figure 17-16. ELM_ERROR_LOCATION_0_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-34. ELM_ERROR_LOCATION_0_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.17 ELM_ERROR_LOCATION_1_i Register (Offset = 884h + formula) [reset = 0h]

ELM_ERROR_LOCATION_1_i (where i = 0 to 7) is shown in [Figure 17-17](#) and described in [Table 17-36](#).

Error-location register 1.

Offset = 884h + (i * 100h), where: i = 0 to 7

Table 17-35. ELM_ERROR_LOCATION_1_i Instances

Instance	Physical Address
ELM0	0538 0884h + formula

Figure 17-17. ELM_ERROR_LOCATION_1_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-36. ELM_ERROR_LOCATION_1_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.18 ELM_ERROR_LOCATION_2_i Register (Offset = 888h + formula) [reset = 0h]

ELM_ERROR_LOCATION_2_i (where i = 0 to 7) is shown in [Figure 17-18](#) and described in [Table 17-38](#).

Error-location register 2.

Offset = 888h + (i * 100h), where: i = 0 to 7

Table 17-37. ELM_ERROR_LOCATION_2_i Instances

Instance	Physical Address
ELM0	0538 0888h + formula

Figure 17-18. ELM_ERROR_LOCATION_2_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-38. ELM_ERROR_LOCATION_2_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.19 ELM_ERROR_LOCATION_3_i Register (Offset = 88Ch + formula) [reset = 0h]

ELM_ERROR_LOCATION_3_i (where i = 0 to 7) is shown in [Figure 17-19](#) and described in [Table 17-40](#).

Error-location register 3.

Offset = 88Ch + (i * 100h), where: i = 0 to 7

Table 17-39. ELM_ERROR_LOCATION_3_i Instances

Instance	Physical Address
ELM0	0538 088Ch + formula

Figure 17-19. ELM_ERROR_LOCATION_3_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-40. ELM_ERROR_LOCATION_3_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.20 ELM_ERROR_LOCATION_4_i Register (Offset = 890h + formula) [reset = 0h]

ELM_ERROR_LOCATION_4_i (where i = 0 to 7) is shown in [Figure 17-20](#) and described in [Table 17-42](#).

Error-location register 4.

Offset = 890h + (i * 100h), where: i = 0 to 7

Table 17-41. ELM_ERROR_LOCATION_4_i Instances

Instance	Physical Address
ELM0	0538 0890h + formula

Figure 17-20. ELM_ERROR_LOCATION_4_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-42. ELM_ERROR_LOCATION_4_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.21 ELM_ERROR_LOCATION_5_i Register (Offset = 894h + formula) [reset = 0h]

ELM_ERROR_LOCATION_5_i (where i = 0 to 7) is shown in [Figure 17-21](#) and described in [Table 17-44](#).

Error-location register 5.

Offset = 894h + (i * 100h), where: i = 0 to 7

Table 17-43. ELM_ERROR_LOCATION_5_i Instances

Instance	Physical Address
ELM0	0538 0894h + formula

Figure 17-21. ELM_ERROR_LOCATION_5_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-44. ELM_ERROR_LOCATION_5_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.22 ELM_ERROR_LOCATION_6_i Register (Offset = 898h + formula) [reset = 0h]

ELM_ERROR_LOCATION_6_i (where i = 0 to 7) is shown in [Figure 17-22](#) and described in [Table 17-46](#).

Error-location register 6.

Offset = 898h + (i * 100h), where: i = 0 to 7

Table 17-45. ELM_ERROR_LOCATION_6_i Instances

Instance	Physical Address
ELM0	0538 0898h + formula

Figure 17-22. ELM_ERROR_LOCATION_6_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-46. ELM_ERROR_LOCATION_6_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.23 ELM_ERROR_LOCATION_7_i Register (Offset = 89Ch + formula) [reset = 0h]

ELM_ERROR_LOCATION_7_i (where i = 0 to 7) is shown in [Figure 17-23](#) and described in [Table 17-48](#).

Error-location register 7.

Offset = 89Ch + (i * 100h), where: i = 0 to 7

Table 17-47. ELM_ERROR_LOCATION_7_i Instances

Instance	Physical Address
ELM0	0538 089Ch + formula

Figure 17-23. ELM_ERROR_LOCATION_7_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-48. ELM_ERROR_LOCATION_7_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.24 ELM_ERROR_LOCATION_8_i Register (Offset = 8A0h + formula) [reset = 0h]

ELM_ERROR_LOCATION_8_i (where i = 0 to 7) is shown in [Figure 17-24](#) and described in [Table 17-50](#).

Error-location register 8.

Offset = 8A0h + (i * 100h), where: i = 0 to 7

Table 17-49. ELM_ERROR_LOCATION_8_i Instances

Instance	Physical Address
ELM0	0538 08A0h + formula

Figure 17-24. ELM_ERROR_LOCATION_8_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-50. ELM_ERROR_LOCATION_8_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.25 ELM_ERROR_LOCATION_9_i Register (Offset = 8A4h + formula) [reset = 0h]

ELM_ERROR_LOCATION_9_i (where i = 0 to 7) is shown in [Figure 17-25](#) and described in [Table 17-52](#).

Error-location register 9.

Offset = 8A4h + (i * 100h), where: i = 0 to 7

Table 17-51. ELM_ERROR_LOCATION_9_i Instances

Instance	Physical Address
ELM0	0538 08A4h + formula

Figure 17-25. ELM_ERROR_LOCATION_9_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-52. ELM_ERROR_LOCATION_9_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.26 ELM_ERROR_LOCATION_10_i Register (Offset = 8A8h + formula) [reset = 0h]

ELM_ERROR_LOCATION_10_i (where i = 0 to 7) is shown in [Figure 17-26](#) and described in [Table 17-54](#).

Error-location register 10.

Offset = 8A8h + (i * 100h), where: i = 0 to 7

**Table 17-53. ELM_ERROR_LOCATION_10_i
Instances**

Instance	Physical Address
ELM0	0538 08A8h + formula

Figure 17-26. ELM_ERROR_LOCATION_10_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-54. ELM_ERROR_LOCATION_10_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.27 ELM_ERROR_LOCATION_11_i Register (Offset = 8ACh + formula) [reset = 0h]

ELM_ERROR_LOCATION_11_i (where i = 0 to 7) is shown in [Figure 17-27](#) and described in [Table 17-56](#).

Error-location register 11.

Offset = 8ACh + (i * 100h), where: i = 0 to 7

**Table 17-55. ELM_ERROR_LOCATION_11_i
Instances**

Instance	Physical Address
ELM0	0538 08ACh + formula

Figure 17-27. ELM_ERROR_LOCATION_11_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-56. ELM_ERROR_LOCATION_11_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.28 ELM_ERROR_LOCATION_12_i Register (Offset = 8B0h + formula) [reset = 0h]

ELM_ERROR_LOCATION_12_i (where i = 0 to 7) is shown in [Figure 17-28](#) and described in [Table 17-58](#).

Error-location register 12.

Offset = 8B0h + (i * 100h), where: i = 0 to 7

**Table 17-57. ELM_ERROR_LOCATION_12_i
Instances**

Instance	Physical Address
ELM0	0538 08B0h + formula

Figure 17-28. ELM_ERROR_LOCATION_12_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-58. ELM_ERROR_LOCATION_12_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.29 ELM_ERROR_LOCATION_13_i Register (Offset = 8B4h + formula) [reset = 0h]

ELM_ERROR_LOCATION_13_i (where i = 0 to 7) is shown in [Figure 17-29](#) and described in [Table 17-60](#).

Error-location register 13.

Offset = 8B4h + (i * 100h), where: i = 0 to 7

**Table 17-59. ELM_ERROR_LOCATION_13_i
Instances**

Instance	Physical Address
ELM0	0538 08B4h + formula

Figure 17-29. ELM_ERROR_LOCATION_13_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-60. ELM_ERROR_LOCATION_13_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.30 ELM_ERROR_LOCATION_14_i Register (Offset = 8B8h + formula) [reset = 0h]

ELM_ERROR_LOCATION_14_i (where i = 0 to 7) is shown in [Figure 17-30](#) and described in [Table 17-62](#).

Error-location register 14.

Offset = 8B8h + (i * 100h), where: i = 0 to 7

**Table 17-61. ELM_ERROR_LOCATION_14_i
Instances**

Instance	Physical Address
ELM0	0538 08B8h + formula

Figure 17-30. ELM_ERROR_LOCATION_14_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-62. ELM_ERROR_LOCATION_14_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

17.31 ELM_ERROR_LOCATION_15_i Register (Offset = 8BCh + formula) [reset = 0h]

ELM_ERROR_LOCATION_15_i (where i = 0 to 7) is shown in [Figure 17-31](#) and described in [Table 17-64](#).

Error-location register 15.

Offset = 8BCh + (i * 100h), where: i = 0 to 7

**Table 17-63. ELM_ERROR_LOCATION_15_i
Instances**

Instance	Physical Address
ELM0	0538 08BCh + formula

Figure 17-31. ELM_ERROR_LOCATION_15_i Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ECC_ERROR_LOCATION											
R-0h				R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 17-64. ELM_ERROR_LOCATION_15_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	ECC_ERROR_LOCATION	R	0h	Error-location bit address

18 MMCS0 Registers

18.1 MMCS0 Subsystem Registers

Table 18-2 lists the memory-mapped registers for the MMCS0 Subsystem. All register offset addresses not listed in Table 18-2 should be considered as reserved locations and the register contents should not be modified.

Table 18-1. MMCS0 Subsystem Instances

Instance	Base Address
MMCS0_SS_CFG	04F8 8000h

Table 18-2. MMCS0 Subsystem Registers

Offset	Acronym	Register Name	MMCS0_SS_CFG Physical Address
0h	MMCS0_SS_SS_ID_REV_REG	Subsystem ID and Revision Register	04F8 8000h
10h	MMCS0_SS_CTL_CFG_1_REG	Controller Config 1 Register	04F8 8010h
14h	MMCS0_SS_CTL_CFG_2_REG	Controller Config 2 Register	04F8 8014h
18h	MMCS0_SS_CTL_CFG_3_REG	Controller Config 3 Register	04F8 8018h
1Ch	MMCS0_SS_CTL_CFG_4_REG	Controller Config 4 Register	04F8 801Ch
20h	MMCS0_SS_CTL_CFG_5_REG	Controller Config 5 Register	04F8 8020h
24h	MMCS0_SS_CTL_CFG_6_REG	Controller Config 6 Register	04F8 8024h
28h	MMCS0_SS_CTL_CFG_7_REG	Controller Config 7 Register	04F8 8028h
2Ch	MMCS0_SS_CTL_CFG_8_REG	Controller Config 8 Register	04F8 802Ch
30h	MMCS0_SS_CTL_CFG_9_REG	Controller Config 9 Register	04F8 8030h
34h	MMCS0_SS_CTL_CFG_10_REG	Controller Config 10 Register	04F8 8034h
38h	MMCS0_SS_CTL_CFG_11_REG	Controller Config 11 Register	04F8 8038h
3Ch	MMCS0_SS_CTL_CFG_12_REG	Controller Config 12 Register	04F8 803Ch
40h	MMCS0_SS_CTL_CFG_13_REG	Controller Config 13 Register	04F8 8040h
44h	MMCS0_SS_CTL_CFG_14_REG	Controller Config 14 Register	04F8 8044h
60h	MMCS0_SS_CTL_STAT_1_REG	Controller Status 1 Register	04F8 8060h
64h	MMCS0_SS_CTL_STAT_2_REG	Controller Status 2 Register	04F8 8064h
68h	MMCS0_SS_CTL_STAT_3_REG	Controller Status 3 Register	04F8 8068h
6Ch	MMCS0_SS_CTL_STAT_4_REG	Controller Status 4 Register	04F8 806Ch
70h	MMCS0_SS_CTL_STAT_5_REG	Controller Status 5 Register	04F8 8070h
74h	MMCS0_SS_CTL_STAT_6_REG	Controller Status 6 Register	04F8 8074h
100h	MMCS0_SS_PHY_CTRL_1_REG	PHY Control 1 Register	04F8 8100h
104h	MMCS0_SS_PHY_CTRL_2_REG	PHY Control 2 Register	04F8 8104h
108h	MMCS0_SS_PHY_CTRL_3_REG	PHY Control 3 Register	04F8 8108h
10Ch	MMCS0_SS_PHY_CTRL_4_REG	PHY Control 4 Register	04F8 810Ch
110h	MMCS0_SS_PHY_CTRL_5_REG	PHY Control 5 Register	04F8 8110h
114h	MMCS0_SS_PHY_CTRL_6_REG	PHY Control 6 Register	04F8 8114h
130h	MMCS0_SS_PHY_STAT_1_REG	PHY Status 1 Register	04F8 8130h
134h	MMCS0_SS_PHY_STAT_2_REG	PHY Status 2 Register	04F8 8134h

18.1.1 MMCS0_SS_SS_ID_REV_REG Register (Offset = 0h) [reset = 68414A00h]

MMCS0_SS_SS_ID_REV_REG is shown in Figure 18-1 and described in Table 18-4.

Return to [Summary Table](#).

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem.

Table 18-3. MMCS0_SS_SS_ID_REV_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 8000h

Figure 18-1. MMCS0_SS_SS_ID_REV_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_ID															
R-6841h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER				MAJ_REV				CUSTOM				MIN_REV			
R-9h				R-2h				R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 18-4. MMCS0_SS_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MOD_ID	R	6841h	Module ID
15-11	RTL_VER	R	9h	RTL Version
10-8	MAJ_REV	R	2h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	MIN_REV	R	0h	Minor Revision

Table 18-5. Register Call Summary for MMCS0_SS_SS_ID_REV_REG

MMCS0 Subsystem Registers

- [MMCS0_SS_SS_ID_REV_REG Register \(Offset = 0h\) \[reset = 68414A00h\]: \[0\]](#)
- [MMCS0 Subsystem Registers: \[0\]](#)

18.1.2 MMCSD0_SS_CTL_CFG_1_REG Register (Offset = 10h) [reset = 201030C8h]

MMCSD0_SS_CTL_CFG_1_REG is shown in Figure 18-2 and described in Table 18-7.

Return to [Summary Table](#).

The Controller Config 1 Register contains various fields to control the configuration ports on the Host Controller.

**Table 18-6. MMCSD0_SS_CTL_CFG_1_REG
Instances**

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8010h

Figure 18-2. MMCSD0_SS_CTL_CFG_1_REG Register

31	30	29	28	27	26	25	24
RESERVED				TUNINGCOUNT			
R-0h				R/W-20h			
23	22	21	20	19	18	17	16
RESERVED				ASYNCWKUPE NA	RESERVED		
R-0h				R/W-1h	R-0h		
15	14	13	12	11	10	9	8
CQFMUL				RESERVED		CQFVAL	
R/W-3h				R-0h		R/W-C8h	
7	6	5	4	3	2	1	0
CQFVAL							
R/W-C8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-7. MMCSD0_SS_CTL_CFG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	TUNINGCOUNT	R/W	20h	Configures the number of Taps (Phases) of the RX clock that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the RX clock during the Tuning Procedure.
23-21	RESERVED	R	0h	Reserved
20	ASYNCWKUPENA	R/W	1h	Determines the Wakeup Signal Generation Mode. 0h: Synchronous Wakeup Mode: The FCLK has to be running for this mode. The Card Insertion/Removal/Interrupt events are detected synchronously on the FCLK and the Wakeup event is generated. The Assertion and Deassertion of the Wakeup event signal synchronous to FCLK. 1h: Asynchronous Wakeup Mode: The FCLK and the ICLK can be stopped in this mode and the Wakeup event is asynchronously generated based on the Card Insertion/Removal/Interrupt events. The Assertion and Deassertion of the Wakeup event signal is asynchronous.
19-16	RESERVED	R	0h	Reserved
15-12	CQFMUL	R/W	3h	FMUL for the CQ Internal Timer Clock Frequency
11-10	RESERVED	R	0h	Reserved

Table 18-7. MMCS0_SS_CTL_CFG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	CQFVAL	R/W	C8h	FVAL for the CQ Internal Timer Clock Frequency

Table 18-8. Register Call Summary for MMCS0_SS_CTL_CFG_1_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_CFG_1_REG Register \(Offset = 10h\) \[reset = 201030C8h\]: \[0\]](#)

18.1.3 MMCSD0_SS_CTL_CFG_2_REG Register (Offset = 14h) [reset = 24ECC801h]

MMCSD0_SS_CTL_CFG_2_REG is shown in Figure 18-3 and described in Table 18-10.

Return to [Summary Table](#).

The Controller Config 2 Register contains various fields to control the configuration ports on the Host Controller. This register sets the LSB fields in the [MMCSD0_CAPABILITIES](#) register inside the Host Controller.

**Table 18-9. MMCSD0_SS_CTL_CFG_2_REG
Instances**

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8014h

Figure 18-3. MMCSD0_SS_CTL_CFG_2_REG Register

31	30	29	28	27	26	25	24
SLOTTYPE		ASYNCHINTRSUPPORT	RESERVED		SUPPORT1P8VOLT	SUPPORT3P0VOLT	SUPPORT3P3VOLT
R/W-0h		R/W-1h	R-0h		R/W-1h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
SUSPRESSUPPORT	SDMASUPPORT	HIGHSPEEDSUPPORT	RESERVED	ADMA2SUPPORT	SUPPORT8BIT	MAXBLKLENGTH	
R/W-1h	R/W-1h	R/W-1h	R-0h	R/W-1h	R/W-1h	R/W-0h	
15	14	13	12	11	10	9	8
BASECLKFREQ							
R/W-C8h							
7	6	5	4	3	2	1	0
TIMEOUTCLKUNIT	RESERVED	TIMEOUTCLKFREQ					
R/W-0h	R-0h	R/W-1h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-10. MMCSD0_SS_CTL_CFG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SLOTTYPE	R/W	0h	Slot Type Should be set based on the final product usage. 0h: Removable SCard Slot 1h: Embedded Slot for One Device 2h: Shared Bus Slot 3h: Reserved
29	ASYNCHINTRSUPPORT	R/W	1h	Asynchronous Interrupt Support Suggested Value is 1h (The Core supports monitoring of Asynchronous Interrupt).
28-27	RESERVED	R	0h	Reserved
26	SUPPORT1P8VOLT	R/W	1h	1.8 V Support Suggested Value is 1h (The 1.8 Volt Switching is supported by Core). Optionally can be set to 0h if the application doesn't want 1.8 V switching (SD3.0).
25	SUPPORT3P0VOLT	R/W	0h	3.0 V Support Should be set based on whether 3.0 V is supported on the SD Interface.

Table 18-10. MMCSDB_SS_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	SUPPORT3P3VOLT	R/W	0h	3.3 V Support Suggested Value is 1h as the 3.3 V is the default voltage on the SD Interface.
23	SUSPRESSUPPORT	R/W	1h	Suspend/Resume Support Suggested Value is 1h (The Suspend/Resume is supported by Core). Optionally can be set to 0h if the application doesn't want to support Suspend/Resume Mode.
22	SDMASUPPORT	R/W	1h	SDMA Support Suggested Value is 1h (The SDMA is supported by Core). Optionally can be set to 0h if the application doesn't want to support SDMA Mode.
21	HIGHSPEEDSUPPORT	R/W	1h	High Speed Support Suggested Value is 1h (The High Speed mode is supported by Core).
20	RESERVED	R	0h	Reserved
19	ADMA2SUPPORT	R/W	1h	ADMA2 Support Suggested Value is 1h (The ADMA2 is supported by Core). Optionally can be set to 0h if the application doesn't want to support ADMA2 Mode.
18	SUPPORT8BIT	R/W	1h	8-bit Support for Embedded Device Suggested Value is 1h (The Core supports 8-bit Interface). Optionally can be set to 0h if the application supports only 4-bit SD Interface.
17-16	MAXBLKLENGTH	R/W	0h	Max Block Length Maximum Block Length supported by the Core/Device. 0h: 512 Bytes 1h: 1024 Bytes 2h: 2048 Bytes 3h: Reserved
15-8	BASECLKFREQ	R/W	C8h	Base Clock Frequency for SD Clock This is the frequency of the FCLK.
7	TIMEOUTCLKUNIT	R/W	0h	Timeout Clock Unit Suggested Value is 0h (KHz).
6	RESERVED	R	0h	Reserved
5-0	TIMEOUTCLKFREQ	R/W	1h	Timeout Clock Frequency Suggested Value is 1 KHz. Internally the 1 ms Timer is used for Timeout Detection. The 1 ms Timer is generated from the FCLK.

Table 18-11. Register Call Summary for MMCSDB_SS_CTL_CFG_2_REG

MMCSDB Subsystem Registers

- [MMCSDB Subsystem Registers: \[0\]](#)
- [MMCSDB_SS_CTL_CFG_2_REG Register \(Offset = 14h\) \[reset = 24ECC801h\]: \[0\]](#)

18.1.4 MMCSD0_SS_CTL_CFG_3_REG Register (Offset = 18h) [reset = 98000407h]

MMCSD0_SS_CTL_CFG_3_REG is shown in Figure 18-4 and described in Table 18-13.

Return to [Summary Table](#).

The Controller Config 3 Register contains various fields to control the configuration ports on the Host Controller. This register sets the MSB fields in the [MMCSD0_CAPABILITIES](#) register inside the Host Controller.

Table 18-12. MMCSD0_SS_CTL_CFG_3_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8018h

Figure 18-4. MMCSD0_SS_CTL_CFG_3_REG Register

31	30	29	28	27	26	25	24
HS400SUPP RT	RESERVED		SUPPORT1P8 VDD2	ADMA3SUPP RT	RESERVED		
R/W-1h	R-0h		R/W-1h	R/W-1h	R-0h		
23	22	21	20	19	18	17	16
CLOCKMULTIPLIER							
R/W-0h							
15	14	13	12	11	10	9	8
RETUNINGMODES		TUNINGFORS DR50	RESERVED	RETUNINGTIMERCNT			
R/W-0h		R/W-0h	R-0h	R/W-4h			
7	6	5	4	3	2	1	0
TYPE4SUPP RT	DDRIVERSUPP ORT	CDRIVERSUPP ORT	ADRIVERSUPP ORT	RESERVED	DDR50SUPP RT	SDR104SUPP ORT	SDR50SUPP RT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-13. MMCSD0_SS_CTL_CFG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HS400SUPPORT	R/W	1h	HS400 Support Suggested Value is 1h (The Core supports HS400 Mode). This applies only to eMMC5.0 mode. This should be set to 0h for SD3.0 mode. Optionally can be set to 0h if the application doesn't want to support HS400. Note: HS400 mode is not supported (see , <i>MMCSD Not Supported Features</i>).
30-29	RESERVED	R	0h	Reserved
28	SUPPORT1P8VDD2	R/W	1h	1.8 V VDD2 Support
27	ADMA3SUPPORT	R/W	1h	ADMA3 Support
26-24	RESERVED	R	0h	Reserved

Table 18-13. MMCS0_SS_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	CLOCKMULTIPLIER	R/W	0h	<p>Clock Multiplier</p> <p>This field indicates clock multiplier value of programmable clock generator.</p> <p>Refer to Clock Control register.</p> <p>Setting 0h means that the Host Controller does not support programmable clock generator.</p> <p>0h: Clock Multiplier is Not Supported</p> <p>1h: Clock Multiplier M = 2</p> <p>2h: Clock Multiplier M = 3</p> <p>...</p> <p>FFh: Clock Multiplier M = 256</p>
15-14	RETUNINGMODES	R/W	0h	<p>Re-Tuning Modes</p> <p>Should be set to 2h as the Core supports only the Software Timer based Re-Tuning.</p>
13	TUNINGFORSDR50	R/W	0h	<p>Use Tuning for SDR50</p> <p>This bit should be set if the application wants Tuning be used for SDR50 Modes.</p> <p>The Core operates with or without tuning for SDR50 mode as long as the Clock can be manually tuned using tap delay.</p>
12	RESERVED	R	0h	Reserved
11-8	RETUNINGTIMERCNT	R/W	4h	<p>Timer Count for Re-Tuning</p> <p>This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3.</p> <p>Setting to 4h disables Re-Tuning Timer.</p>
7	TYPE4SUPPORT	R/W	0h	<p>Driver Type 4 Support</p> <p>This bit should be set based on whether Driver Type 4 for 1.8 Signalling is supported or not.</p>
6	DDRIVERSUPPORT	R/W	0h	<p>Driver Type D Support</p> <p>This bit should be set based on whether Driver Type D for 1.8 Signalling is supported or not.</p>
5	CDRIVERSUPPORT	R/W	0h	<p>Driver Type C Support</p> <p>This bit should be set based on whether Driver Type C for 1.8 Signalling is supported or not.</p>
4	ADRIVERSUPPORT	R/W	0h	<p>Driver Type A Support</p> <p>This bit should be set based on whether Driver Type A for 1.8 Signalling is supported or not.</p>
3	RESERVED	R	0h	Reserved
2	DDR50SUPPORT	R/W	1h	<p>DDR50 Support</p> <p>Suggested Value is 1h (The Core supports DDR50 mode of operation).</p> <p>Optionally can be set to 0h if the application doesn't want to support DDR50.</p>
1	SDR104SUPPORT	R/W	1h	<p>SDR104 Support.</p> <p>Suggested Value is 1h (The Core supports SDR104 mode of operation).</p> <p>Optionally can be set to 0h if the application doesn't want to support SDR104.</p>

Table 18-13. MMCSD0_SS_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SDR50SUPPORT	R/W	1h	SDR50 Support. Suggested Value is 1h (The Core supports SDR50 mode of operation). Optionally can be set to 0h if the application doesn't want to support SDR50.

Table 18-14. Register Call Summary for MMCSD0_SS_CTL_CFG_3_REG

MMCSD0 Subsystem Registers

- [MMCSD0 Subsystem Registers: \[0\]](#)
- [MMCSD0_SS_CTL_CFG_3_REG Register \(Offset = 18h\) \[reset = 98000407h\]: \[0\]](#)

18.1.5 MMCS0_SS_CTL_CFG_4_REG Register (Offset = 1Ch) [reset = 0h]

MMCS0_SS_CTL_CFG_4_REG is shown in Figure 18-5 and described in Table 18-16.

Return to [Summary Table](#).

The Controller Config 4 Register contains various fields to control the configuration ports on the Host Controller. This register sets the LSB fields in the MMCS0_MAX_CURRENT_CAP register inside the Host Controller.

Table 18-15. MMCS0_SS_CTL_CFG_4_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 801Ch

Figure 18-5. MMCS0_SS_CTL_CFG_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MAXCURRENT1P8V							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXCURRENT3P0V								MAXCURRENT3P3V							
R/W-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-16. MMCS0_SS_CTL_CFG_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	MAXCURRENT1P8V	R/W	0h	Maximum Current For 1.8 V
15-8	MAXCURRENT3P0V	R/W	0h	Maximum Current For 3.0 V
7-0	MAXCURRENT3P3V	R/W	0h	Maximum Current For 3.3 V

Table 18-17. Register Call Summary for MMCS0_SS_CTL_CFG_4_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_CFG_4_REG Register \(Offset = 1Ch\) \[reset = 0h\]: \[0\]](#)

18.1.6 MMCSD0_SS_CTL_CFG_5_REG Register (Offset = 20h) [reset = 0h]

MMCSD0_SS_CTL_CFG_5_REG is shown in [Figure 18-6](#) and described in [Table 18-19](#).

Return to [Summary Table](#).

The Controller Config 5 Register contains various fields to control the configuration ports on the Host Controller. This register sets the MSB fields in the [MMCSD0_MAX_CURRENT_CAP](#) register inside the Host Controller.

**Table 18-18. MMCSD0_SS_CTL_CFG_5_REG
Instances**

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8020h

Figure 18-6. MMCSD0_SS_CTL_CFG_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAXCURRENTVDD2							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-19. MMCSD0_SS_CTL_CFG_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MAXCURRENTVDD2	R/W	0h	Maximum Current For 1.8 V (VDD2)

Table 18-20. Register Call Summary for MMCSD0_SS_CTL_CFG_5_REG

MMCSD0 Subsystem Registers

- [MMCSD0_SS_CTL_CFG_5_REG Register \(Offset = 20h\) \[reset = 0h\]: \[0\]](#)
- [MMCSD0 Subsystem Registers: \[0\]](#)

18.1.7 MMCS0_SS_CTL_CFG_6_REG Register (Offset = 24h) [reset = 100h]

MMCS0_SS_CTL_CFG_6_REG is shown in [Figure 18-7](#) and described in [Table 18-22](#).

Return to [Summary Table](#).

The Controller Config 6 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCS0_PRESET_VALUE0](#) to [MMCS0_PRESET_VALUE10](#)) for Initialization inside the Host Controller.

Table 18-21. MMCS0_SS_CTL_CFG_6_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 8024h

Figure 18-7. MMCS0_SS_CTL_CFG_6_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																INITPRESETVAL															
R-0h																R/W-100h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-22. MMCS0_SS_CTL_CFG_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	INITPRESETVAL	R/W	100h	Preset Value For Initialization

Table 18-23. Register Call Summary for MMCS0_SS_CTL_CFG_6_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_CFG_6_REG Register \(Offset = 24h\) \[reset = 100h\]: \[0\]](#)

18.1.8 MMCSD0_SS_CTL_CFG_7_REG Register (Offset = 28h) [reset = 4h]

MMCSD0_SS_CTL_CFG_7_REG is shown in [Figure 18-8](#) and described in [Table 18-25](#).

Return to [Summary Table](#).

The Controller Config 7 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCSD0_PRESET_VALUE0](#) to [MMCSD0_PRESET_VALUE10](#)) for Default Speed inside the Host Controller.

Table 18-24. MMCSD0_SS_CTL_CFG_7_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8028h

Figure 18-8. MMCSD0_SS_CTL_CFG_7_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DSPDPRESETVAL															
R-0h																R/W-4h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-25. MMCSD0_SS_CTL_CFG_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	DSPDPRESETVAL	R/W	4h	Preset Value For Default Speed

Table 18-26. Register Call Summary for MMCSD0_SS_CTL_CFG_7_REG

MMCSD0 Subsystem Registers

- [MMCSD0 Subsystem Registers: \[0\]](#)
- [MMCSD0_SS_CTL_CFG_7_REG Register \(Offset = 28h\) \[reset = 4h\]: \[0\]](#)

18.1.9 MMCS0_SS_CTL_CFG_8_REG Register (Offset = 2Ch) [reset = 2h]

MMCS0_SS_CTL_CFG_8_REG is shown in [Figure 18-9](#) and described in [Table 18-28](#).

Return to [Summary Table](#).

The Controller Config 8 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCS0_PRESET_VALUE0](#) to [MMCS0_PRESET_VALUE10](#)) for High Speed inside the Host Controller.

Table 18-27. MMCS0_SS_CTL_CFG_8_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 802Ch

Figure 18-9. MMCS0_SS_CTL_CFG_8_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSPDPRESETVAL															
R-0h																R/W-2h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-28. MMCS0_SS_CTL_CFG_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	HSPDPRESETVAL	R/W	2h	Preset Value For High Speed

Table 18-29. Register Call Summary for MMCS0_SS_CTL_CFG_8_REG

MMCS0 Subsystem Registers

- [MMCS0_SS_CTL_CFG_8_REG Register \(Offset = 2Ch\) \[reset = 2h\]: \[0\]](#)
- [MMCS0 Subsystem Registers: \[0\]](#)

18.1.10 MMCSD0_SS_CTL_CFG_9_REG Register (Offset = 30h) [reset = 4h]

MMCSD0_SS_CTL_CFG_9_REG is shown in [Figure 18-10](#) and described in [Table 18-31](#).

Return to [Summary Table](#).

The Controller Config 9 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCSD0_PRESET_VALUE0](#) to [MMCSD0_PRESET_VALUE10](#)) for SDR12 inside the Host Controller.

Table 18-30. MMCSD0_SS_CTL_CFG_9_REG Instances

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8030h

Figure 18-10. MMCSD0_SS_CTL_CFG_9_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDR12PRESETVAL											
R-0h				R/W-4h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-31. MMCSD0_SS_CTL_CFG_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR12PRESETVAL	R/W	4h	Preset Value For SDR12

Table 18-32. Register Call Summary for MMCSD0_SS_CTL_CFG_9_REG

MMCSD0 Subsystem Registers

- [MMCSD0 Subsystem Registers: \[0\]](#)
- [MMCSD0_SS_CTL_CFG_9_REG Register \(Offset = 30h\) \[reset = 4h\]: \[0\]](#)

18.1.11 MMCS0_SS_CTL_CFG_10_REG Register (Offset = 34h) [reset = 2h]

MMCS0_SS_CTL_CFG_10_REG is shown in Figure 18-11 and described in Table 18-34.

Return to [Summary Table](#).

The Controller Config 10 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCS0_PRESET_VALUE0 to MMCS0_PRESET_VALUE10) for SDR25 inside the Host Controller.

Table 18-33. MMCS0_SS_CTL_CFG_10_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 8034h

Figure 18-11. MMCS0_SS_CTL_CFG_10_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDR25PRESETVAL											
R-0h				R/W-2h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-34. MMCS0_SS_CTL_CFG_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR25PRESETVAL	R/W	2h	Preset Value For SDR25

Table 18-35. Register Call Summary for MMCS0_SS_CTL_CFG_10_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_CFG_10_REG Register \(Offset = 34h\) \[reset = 2h\]: \[0\]](#)

18.1.12 MMCSD0_SS_CTL_CFG_11_REG Register (Offset = 38h) [reset = 1h]

MMCSD0_SS_CTL_CFG_11_REG is shown in [Figure 18-12](#) and described in [Table 18-37](#).

Return to [Summary Table](#).

The Controller Config 11 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCSD0_PRESET_VALUE0](#) to [MMCSD0_PRESET_VALUE10](#)) for SDR50 inside the Host Controller.

**Table 18-36. MMCSD0_SS_CTL_CFG_11_REG
Instances**

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8038h

Figure 18-12. MMCSD0_SS_CTL_CFG_11_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDR50PRESETVAL											
R-0h				R/W-1h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-37. MMCSD0_SS_CTL_CFG_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR50PRESETVAL	R/W	1h	Preset Value For SDR50

Table 18-38. Register Call Summary for MMCSD0_SS_CTL_CFG_11_REG

MMCSD0 Subsystem Registers

- [MMCSD0 Subsystem Registers: \[0\]](#)
- [MMCSD0_SS_CTL_CFG_11_REG Register \(Offset = 38h\) \[reset = 1h\]: \[0\]](#)

18.1.13 MMCS0_SS_CTL_CFG_12_REG Register (Offset = 3Ch) [reset = 0h]

MMCS0_SS_CTL_CFG_12_REG is shown in Figure 18-13 and described in Table 18-40.

Return to [Summary Table](#).

The Controller Config 12 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCS0_PRESET_VALUE0 to MMCS0_PRESET_VALUE10) for SDR104 inside the Host Controller.

Table 18-39. MMCS0_SS_CTL_CFG_12_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 803Ch

Figure 18-13. MMCS0_SS_CTL_CFG_12_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDR104PRESETVAL											
R-0h				R/W-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-40. MMCS0_SS_CTL_CFG_12_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR104PRESETVAL	R/W	0h	Preset Value For SDR104

Table 18-41. Register Call Summary for MMCS0_SS_CTL_CFG_12_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_CFG_12_REG Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)

18.1.14 MMCS0_SS_CTL_CFG_13_REG Register (Offset = 40h) [reset = 2h]

MMCS0_SS_CTL_CFG_13_REG is shown in [Figure 18-14](#) and described in [Table 18-43](#).

Return to [Summary Table](#).

The Controller Config 13 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCS0_PRESET_VALUE0](#) to [MMCS0_PRESET_VALUE10](#)) for DDR50 inside the Host Controller.

**Table 18-42. MMCS0_SS_CTL_CFG_13_REG
Instances**

Instance	Physical Address
MMCS0_SS_CFG	04F8 8040h

Figure 18-14. MMCS0_SS_CTL_CFG_13_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				DDR50PRESETVAL											
R-0h				R/W-2h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-43. MMCS0_SS_CTL_CFG_13_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	DDR50PRESETVAL	R/W	2h	Preset Value For DDR50

Table 18-44. Register Call Summary for MMCS0_SS_CTL_CFG_13_REG

MMCS0 Subsystem Registers

- [MMCS0_SS_CTL_CFG_13_REG Register \(Offset = 40h\) \[reset = 2h\]: \[0\]](#)
- [MMCS0 Subsystem Registers: \[0\]](#)

18.1.15 MMCS0_SS_CTL_CFG_14_REG Register (Offset = 44h) [reset = 1h]

MMCS0_SS_CTL_CFG_14_REG is shown in Figure 18-15 and described in Table 18-46.

Return to [Summary Table](#).

The Controller Config 14 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCS0_PRESET_VALUE0 to MMCS0_PRESET_VALUE10) for HS400 inside the Host Controller.

Table 18-45. MMCS0_SS_CTL_CFG_14_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 8044h

Figure 18-15. MMCS0_SS_CTL_CFG_14_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HS400PRESETVAL											
R-0h				R/W-1h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-46. MMCS0_SS_CTL_CFG_14_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	HS400PRESETVAL	R/W	1h	Preset Value For HS400

Table 18-47. Register Call Summary for MMCS0_SS_CTL_CFG_14_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_CFG_14_REG Register \(Offset = 44h\) \[reset = 1h\]: \[0\]](#)

18.1.16 MMCS0_SS_CTL_STAT_1_REG Register (Offset = 60h) [reset = 80000000h]

MMCS0_SS_CTL_STAT_1_REG is shown in Figure 18-16 and described in Table 18-49.

Return to [Summary Table](#).

The Controller Status 1 Register contains various fields to reflect the status of the debug ports on the Host Controller.

**Table 18-48. MMCS0_SS_CTL_STAT_1_REG
Instances**

Instance	Physical Address
MMCS0_SS_CFG	04F8 8060h

Figure 18-16. MMCS0_SS_CTL_STAT_1_REG Register

31	30	29	28	27	26	25	24
SDHC_CMDIDLE	RESERVED						
R-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DMADEBUGBUS							
R-0h							
7	6	5	4	3	2	1	0
DMADEBUGBUS							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-49. MMCS0_SS_CTL_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDHC_CMDIDLE	R	1h	Idle signal to enable software to gate off the clocks
30-16	RESERVED	R	0h	Reserved
15-0	DMADEBUGBUS	R	0h	DMA_CTRL Debug Bus

Table 18-50. Register Call Summary for MMCS0_SS_CTL_STAT_1_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_STAT_1_REG Register \(Offset = 60h\) \[reset = 80000000h\]: \[0\]](#)

18.1.17 MMCS0_SS_CTL_STAT_2_REG Register (Offset = 64h) [reset = 10h]

MMCS0_SS_CTL_STAT_2_REG is shown in Figure 18-17 and described in Table 18-52.

Return to [Summary Table](#).

The Controller Status 2 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 18-51. MMCS0_SS_CTL_STAT_2_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 8064h

Figure 18-17. MMCS0_SS_CTL_STAT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMDDEBUGBUS															
R-0h																R-10h															

LEGEND: R = Read Only; -n = value after reset

Table 18-52. MMCS0_SS_CTL_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CMDDEBUGBUS	R	10h	CMD_CTRL Debug Bus

Table 18-53. Register Call Summary for MMCS0_SS_CTL_STAT_2_REG

MMCS0 Subsystem Registers

- [MMCS0_SS_CTL_STAT_2_REG Register \(Offset = 64h\) \[reset = 10h\]: \[0\]](#)
- [MMCS0 Subsystem Registers: \[0\]](#)

18.1.18 MMCSDB_SS_CTL_STAT_3_REG Register (Offset = 68h) [reset = 0h]

MMCSDB_SS_CTL_STAT_3_REG is shown in Figure 18-18 and described in Table 18-55.

Return to [Summary Table](#).

The Controller Status 3 Register contains various fields to reflect the status of the debug ports on the Host Controller.

**Table 18-54. MMCSDB_SS_CTL_STAT_3_REG
Instances**

Instance	Physical Address
MMCSDB_SS_CFG	04F8 8068h

Figure 18-18. MMCSDB_SS_CTL_STAT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TXDDEBUGBUS															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 18-55. MMCSDB_SS_CTL_STAT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TXDDEBUGBUS	R	0h	TXD_CTRL Debug Bus

Table 18-56. Register Call Summary for MMCSDB_SS_CTL_STAT_3_REG

MMCSDB Subsystem Registers

- [MMCSDB Subsystem Registers: \[0\]](#)
- [MMCSDB_SS_CTL_STAT_3_REG Register \(Offset = 68h\) \[reset = 0h\]: \[0\]](#)

18.1.19 MMCS0_SS_CTL_STAT_4_REG Register (Offset = 6Ch) [reset = 0h]

MMCS0_SS_CTL_STAT_4_REG is shown in Figure 18-19 and described in Table 18-58.

Return to [Summary Table](#).

The Controller Status 4 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 18-57. MMCS0_SS_CTL_STAT_4_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 806Ch

Figure 18-19. MMCS0_SS_CTL_STAT_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RXDDEBUGBUS0															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 18-58. MMCS0_SS_CTL_STAT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RXDDEBUGBUS0	R	0h	RXD_CTRL Debug Bus (SD CLK)

Table 18-59. Register Call Summary for MMCS0_SS_CTL_STAT_4_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_STAT_4_REG Register \(Offset = 6Ch\) \[reset = 0h\]: \[0\]](#)

18.1.20 MMCSDB_SS_CTL_STAT_5_REG Register (Offset = 70h) [reset = 8h]

MMCSDB_SS_CTL_STAT_5_REG is shown in Figure 18-20 and described in Table 18-61.

Return to [Summary Table](#).

The Controller Status 5 Register contains various fields to reflect the status of the debug ports on the Host Controller.

**Table 18-60. MMCSDB_SS_CTL_STAT_5_REG
Instances**

Instance	Physical Address
MMCSDB_SS_CFG	04F8 8070h

Figure 18-20. MMCSDB_SS_CTL_STAT_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RXDDEBUGBUS1															
R-0h																R-8h															

LEGEND: R = Read Only; -n = value after reset

Table 18-61. MMCSDB_SS_CTL_STAT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RXDDEBUGBUS1	R	8h	RXD_CTRL Debug Bus (RX CLK)

Table 18-62. Register Call Summary for MMCSDB_SS_CTL_STAT_5_REG

MMCSDB Subsystem Registers

- [MMCSDB Subsystem Registers: \[0\]](#)
- [MMCSDB_SS_CTL_STAT_5_REG Register \(Offset = 70h\) \[reset = 8h\]: \[0\]](#)

18.1.21 MMCS0_SS_CTL_STAT_6_REG Register (Offset = 74h) [reset = 0h]

MMCS0_SS_CTL_STAT_6_REG is shown in Figure 18-21 and described in Table 18-64.

Return to [Summary Table](#).

The Controller Status 6 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 18-63. MMCS0_SS_CTL_STAT_6_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 8074h

Figure 18-21. MMCS0_SS_CTL_STAT_6_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TUNDEBUGBUS															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 18-64. MMCS0_SS_CTL_STAT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TUNDEBUGBUS	R	0h	TUN_CTRL Debug Bus

Table 18-65. Register Call Summary for MMCS0_SS_CTL_STAT_6_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_CTL_STAT_6_REG Register \(Offset = 74h\) \[reset = 0h\]: \[0\]](#)

18.1.22 MMCS0_SS_PHY_CTRL_1_REG Register (Offset = 100h) [reset = 80010000h]

MMCS0_SS_PHY_CTRL_1_REG is shown in Figure 18-22 and described in Table 18-67.

Return to [Summary Table](#).

The PHY Control 1 Register contains various fields to control the ports on the Host Controller PHY.

**Table 18-66. MMCS0_SS_PHY_CTRL_1_REG
Instances**

Instance	Physical Address
MMCS0_SS_CFG	04F8 8100h

Figure 18-22. MMCS0_SS_PHY_CTRL_1_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED	DR_TY			RESERVED		RETRIM	EN_RTRIM
R-0h	R/W-0h			R-0h		R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DLL_TRM_ICP				RESERVED		ENDLL	PDB
R/W-0h				R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-67. MMCS0_SS_PHY_CTRL_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-20	DR_TY	R/W	0h	Drive Source/Sink Impedance Programming 0h: 50 Ohms 1h: 33 Ohms 2h: 66 Ohms 3h: 100 Ohms 4h: 40 Ohms
19-18	RESERVED	R	0h	Reserved
17	RETRIM	R/W	0h	Start IO Calibration Cycle A positive edge initiates the IO calibration cycle using CALIO.
16	EN_RTRIM	R/W	1h	Enables CALIO When enabled, CALIO will start IO calibration cycle on the positive edge of PDB.
15-8	RESERVED	R	0h	Reserved
7-4	DLL_TRM_ICP	R/W	0h	Analog DLL's Charge Pump Current Trim Programs the analog DLL loop gain.
3-2	RESERVED	R	0h	Reserved
1	ENDLL	R/W	0h	Enable DLL Enables the analog DLL circuits.

Table 18-67. MMCS0_SS_PHY_CTRL_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PDB	R/W	0h	Active Low Power Down for CALIO Software must write a 1h to power-up CALIO during power-up sequence.

Table 18-68. Register Call Summary for MMCS0_SS_PHY_CTRL_1_REG

MMCS0 Subsystem Registers

- [MMCS0_SS_PHY_CTRL_1_REG Register \(Offset = 100h\) \[reset = 80010000h\]: \[0\]](#)
- [MMCS0 Subsystem Registers: \[0\]](#)

18.1.23 MMCSDB_SS_PHY_CTRL_2_REG Register (Offset = 104h) [reset = 0h]

MMCSDB_SS_PHY_CTRL_2_REG is shown in Figure 18-23 and described in Table 18-70.

Return to [Summary Table](#).

The PHY Control 2 Register contains various fields to control the ports on the Host Controller PHY.

**Table 18-69. MMCSDB_SS_PHY_CTRL_2_REG
Instances**

Instance	Physical Address
MMCSDB_SS_CFG	04F8 8104h

Figure 18-23. MMCSDB_SS_PHY_CTRL_2_REG Register

31	30	29	28	27	26	25	24
RESERVED		OD_RELEASE_STRB	OD_RELEASE_CMD	RESERVED			
R-0h		R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
OD_RELEASE_DAT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		ODEN_STRB	ODEN_CMD	RESERVED			
R-0h		R/W-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
ODEN_DAT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-70. MMCSDB_SS_PHY_CTRL_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	OD_RELEASE_STRB	R/W	0h	Internal Pull Select for STRB Line 0h = pull-down 1h = pull-up
28	OD_RELEASE_CMD	R/W	0h	Internal Pull Select for CMD Line 0h = pull-down 1h = pull-up
27-24	RESERVED	R	0h	Reserved
23-16	OD_RELEASE_DAT	R/W	0h	Internal Pull Select for DAT Lines 0h = pull-down 1h = pull-up
15-14	RESERVED	R	0h	Reserved
13	ODEN_STRB	R/W	0h	Enable Internal Pull-up/Down Resistor on the STRB Line 0h = internal pull disabled 1h = internal pull enabled
12	ODEN_CMD	R/W	0h	Enable Internal Pull-up/Down Resistor on the CMD Line 0h = internal pull disabled 1h = internal pull enabled
11-8	RESERVED	R	0h	Reserved

Table 18-70. MMCS0_SS_PHY_CTRL_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	ODEN_DAT	R/W	0h	Enable Internal Pull-up/Down Resistor on the DAT Lines 0h = internal pull disabled 1h = internal pull enabled

Table 18-71. Register Call Summary for MMCS0_SS_PHY_CTRL_2_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_PHY_CTRL_2_REG Register \(Offset = 104h\) \[reset = 0h\]: \[0\]](#)

18.1.24 MMCSD0_SS_PHY_CTRL_3_REG Register (Offset = 108h) [reset = 10FF10FFh]

MMCSD0_SS_PHY_CTRL_3_REG is shown in Figure 18-24 and described in Table 18-73.

Return to [Summary Table](#).

The PHY Control 3 Register contains various fields to control the ports on the Host Controller PHY.

**Table 18-72. MMCSD0_SS_PHY_CTRL_3_REG
Instances**

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8108h

Figure 18-24. MMCSD0_SS_PHY_CTRL_3_REG Register

31	30	29	28	27	26	25	24
RESERVED		PU_STRB	PU_CMD	RESERVED			
R-0h		R/W-0h	R/W-1h	R-0h			
23	22	21	20	19	18	17	16
PU_DAT							
R/W-FFh							
15	14	13	12	11	10	9	8
RESERVED		REN_STRB	REN_CMD	RESERVED			
R-0h		R/W-0h	R/W-1h	R-0h			
7	6	5	4	3	2	1	0
REN_DAT							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-73. MMCSD0_SS_PHY_CTRL_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	PU_STRB	R/W	0h	Enable Pull Up On STRB Line If ren_strb is high week pull up is enabled on STRB line.
28	PU_CMD	R/W	1h	Enable Pull Up On CMD Line If ren_cmd is high week pull up is enabled on CMD line.
27-24	RESERVED	R	0h	Reserved
23-16	PU_DAT	R/W	FFh	Enable Pull Up On DAT Lines If ren_dat is high week pull up is enabled on DATA lines.
15-14	RESERVED	R	0h	Reserved
13	REN_STRB	R/W	0h	Enable Pull Up/Down On The STRB Line If pu_strb is high a week pull up is enabled on STRB line, if low week pull down is enabled on STRB line.
12	REN_CMD	R/W	1h	Enable Pull Up/Down On The CMD Line If pu_cmd is high a week pull up is enabled on CMD line, if low week pull down is enabled on CMD line.
11-8	RESERVED	R	0h	Reserved
7-0	REN_DAT	R/W	FFh	Enable Pull Up/Down On The DAT Lines If pu_dat is high a week pull up is enabled on DATA lines, if low week pull down is enabled on DATA lines.

Table 18-74. Register Call Summary for MMCSD0_SS_PHY_CTRL_3_REG

MMCSD0 Subsystem Registers

- [MMCSD0 Subsystem Registers: \[0\]](#)
- [MMCSD0_SS_PHY_CTRL_3_REG Register \(Offset = 108h\) \[reset = 10FF10FFh\]: \[0\]](#)

18.1.25 MMCS0_SS_PHY_CTRL_4_REG Register (Offset = 10Ch) [reset = 0h]

MMCS0_SS_PHY_CTRL_4_REG is shown in Figure 18-25 and described in Table 18-76.

Return to [Summary Table](#).

The PHY Control 4 Register contains various fields to control the ports on the Host Controller PHY.

**Table 18-75. MMCS0_SS_PHY_CTRL_4_REG
Instances**

Instance	Physical Address
MMCS0_SS_CFG	04F8 810Ch

Figure 18-25. MMCS0_SS_PHY_CTRL_4_REG Register

31	30	29	28	27	26	25	24
STRBSEL							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED			OTAPDLYENA	RESERVED			
R-0h			R/W-0h	R-0h			
15	14	13	12	11	10	9	8
OTAPDLYSEL				RESERVED		ITAPCHGWIN	ITAPDLYENA
R/W-0h				R-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			ITAPDLYSEL				
R-0h			R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-76. MMCS0_SS_PHY_CTRL_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	STRBSEL	R/W	0h	Select the Four Taps for each of STRB_90 and STRB_180 Outputs. strbsel[3:2] selects one of the four for STRB_180 and strbsel[1:0] selects the four taps for STRB_90.
23-21	RESERVED	R	0h	Reserved
20	OTAPDLYENA	R/W	0h	Output Tap Delay Enable Enables manual control of the TX clock tap delay, for clocking the final stage flops for maintaining Hold requirements on EMMC Interface.
19-16	RESERVED	R	0h	Reserved
15-12	OTAPDLYSEL	R/W	0h	Output Tap Delay Select Manual control of the TX clock tap delay for clocking the final stage flops for maintaining Hold requirements on EMMC Interface.
11-10	RESERVED	R	0h	Reserved
9	ITAPCHGWIN	R/W	0h	Input Tap Change Window It gets asserted by the controller while changing the itapdlysel. Used to gate of the RX clock during switching the clock source while tap is changing to avoid clock glitches.
8	ITAPDLYENA	R/W	0h	Input Tap Delay Enable This is used for the manual control of the RX clock Tap Delay.
7-5	RESERVED	R	0h	Reserved

Table 18-76. MMCS0_SS_PHY_CTRL_4_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	ITAPDLYSEL	R/W	0h	Input Tap Delay Select Manual control of the RX clock Tap Delay.

Table 18-77. Register Call Summary for MMCS0_SS_PHY_CTRL_4_REG

MMCS0 Subsystem Registers

- [MMCS0_SS_PHY_CTRL_4_REG Register \(Offset = 10Ch\) \[reset = 0h\]: \[0\]](#)
- [MMCS0 Subsystem Registers: \[0\]](#)

18.1.26 MMCSO_SS_PHY_CTRL_5_REG Register (Offset = 110h) [reset = 0h]

MMCSO_SS_PHY_CTRL_5_REG is shown in Figure 18-26 and described in Table 18-79.

Return to [Summary Table](#).

The PHY Control 5 Register contains various fields to control the ports on the Host Controller PHY.

**Table 18-78. MMCSO_SS_PHY_CTRL_5_REG
Instances**

Instance	Physical Address
MMCSO_SS_CFG	04F8 8110h

Figure 18-26. MMCSO_SS_PHY_CTRL_5_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						SELDLYTXCLK	SELDLYRXCLK
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED					FRQSEL		
R-0h					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED					CLKBUFSEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-79. MMCSO_SS_PHY_CTRL_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	SELDLYTXCLK	R/W	0h	Select the Delay chain based txclk. Enables the TX clock based delay chain rather than analog DLL based delay chain.
16	SELDLYRXCLK	R/W	0h	Select the Delay chain based rxclk. Enables the RX clock based delay chain rather than analog DLL based delay chain.
15-11	RESERVED	R	0h	Reserved
10-8	FRQSEL	R/W	0h	Select the frequency range of DLL operation: 0h: 200 MHz to 170 MHz, 1h: 170 MHz to 140 MHz, 2h: 140 MHz to 110 MHz, 3h: 110 MHz to 80MHz, 4h: 80 MHz to 50 MHz, 5h: 275 Mhz to 250 MHz, 6h: 250 MHz to 225 MHz, 7h: 225 MHz to 200 MHz.
7-3	RESERVED	R	0h	Reserved
2-0	CLKBUFSEL	R/W	0h	Clock Delay Buffer Select. Selects one of the eight taps in the CLK Delay Buffer based on PVT variation.

Table 18-80. Register Call Summary for MMCSD0_SS_PHY_CTRL_5_REG

MMCSD0 Subsystem Registers

- [MMCSD0 Subsystem Registers: \[0\]](#)
- [MMCSD0_SS_PHY_CTRL_5_REG Register \(Offset = 110h\) \[reset = 0h\]: \[0\]](#)

18.1.27 MMCS0_SS_PHY_CTRL_6_REG Register (Offset = 114h) [reset = 0h]

MMCS0_SS_PHY_CTRL_6_REG is shown in Figure 18-27 and described in Table 18-82.

Return to [Summary Table](#).

The PHY Control 6 Register contains various fields to control the ports on the Host Controller PHY.

**Table 18-81. MMCS0_SS_PHY_CTRL_6_REG
Instances**

Instance	Physical Address
MMCS0_SS_CFG	04F8 8114h

Figure 18-27. MMCS0_SS_PHY_CTRL_6_REG Register

31	30	29	28	27	26	25	24
BISTENABLE	BISTSTART	RESERVED		BISTMODE			
R/W-0h	R/W-0h	R-0h		R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
TESTCTRL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-82. MMCS0_SS_PHY_CTRL_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BISTENABLE	R/W	0h	Internal BIST Operation Enable Enables the embedded BIST.
30	BISTSTART	R/W	0h	Internal BIST Start Starts the embedded BIST operation.
29-28	RESERVED	R	0h	Reserved
27-24	BISTMODE	R/W	0h	Internal BIST Mode Select Select the embedded BIST mode of operation.
23-8	RESERVED	R	0h	Reserved
7-0	TESTCTRL	R/W	0h	PHY Test Control: 10h: Test EMMC IOs sink impedance 11h: Test EMMC IOs source impedance 20h: Test RX clock phases on data lines 30h: Test TX clock phases on data lines 40h: Test STRB clock phases on data lines

Table 18-83. Register Call Summary for MMCS0_SS_PHY_CTRL_6_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_PHY_CTRL_6_REG Register \(Offset = 114h\) \[reset = 0h\]: \[0\]](#)

18.1.28 MMCS0_SS_PHY_STAT_1_REG Register (Offset = 130h) [reset = E0h]

MMCS0_SS_PHY_STAT_1_REG is shown in Figure 18-28 and described in Table 18-85.

Return to [Summary Table](#).

The PHY Status 1 Register contains various fields to reflect the status of the Host Controller PHY ports.

Table 18-84. MMCS0_SS_PHY_STAT_1_REG Instances

Instance	Physical Address
MMCS0_SS_CFG	04F8 8130h

Figure 18-28. MMCS0_SS_PHY_STAT_1_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RTRIM				BISTDONE	EXR_NINST	CALDONE	DLLRDY
R-Eh				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 18-85. MMCS0_SS_PHY_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	RTRIM	R	Eh	CALIO Calibration Result Holds the content of CALIO Impedance Calibration Result.
3	BISTDONE	R	0h	Internal BIST Completed Test Cycle Indicates that the embedded BIST has completed the test cycle.
2	EXR_NINST	R	0h	External Resistor On CALIO Absent Indicates trim cycle started and external resistor is absent.
1	CALDONE	R	0h	STATUS, indicate that CALIO Calibration is completed successfully.
0	DLLRDY	R	0h	DLL Ready Indicates that DLL loop is locked.

Table 18-86. Register Call Summary for MMCS0_SS_PHY_STAT_1_REG

MMCS0 Subsystem Registers

- [MMCS0 Subsystem Registers: \[0\]](#)
- [MMCS0_SS_PHY_STAT_1_REG Register \(Offset = 130h\) \[reset = E0h\]: \[0\]](#)

18.1.29 MMCSD0_SS_PHY_STAT_2_REG Register (Offset = 134h) [reset = 0h]

MMCSD0_SS_PHY_STAT_2_REG is shown in [Figure 18-29](#) and described in [Table 18-88](#).

Return to [Summary Table](#).

The PHY Status 2 Register contains various fields to reflect the status of the Host Controller PHY ports.

**Table 18-87. MMCSD0_SS_PHY_STAT_2_REG
Instances**

Instance	Physical Address
MMCSD0_SS_CFG	04F8 8134h

Figure 18-29. MMCSD0_SS_PHY_STAT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BISTSTATUS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-88. MMCSD0_SS_PHY_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BISTSTATUS	R	0h	Internal BIST Data Compare Results BIST cycle data comparison results.

Table 18-89. Register Call Summary for MMCSD0_SS_PHY_STAT_2_REG

MMCSD0 Subsystem Registers

- [MMCSD0 Subsystem Registers: \[0\]](#)
- [MMCSD0_SS_PHY_STAT_2_REG Register \(Offset = 134h\) \[reset = 0h\]: \[0\]](#)

18.2 MMCS0 Host Controller Registers

Table 18-91 lists the memory-mapped registers for the MMCS0 Host Controller. All register offset addresses not listed in Table 18-91 should be considered as reserved locations and the register contents should not be modified.

Note

UHSII is not supported. For more information, see *Not Supported Features*.

**Table 18-90. MMCS0 HOST CONTROLLER
Instances**

Instance	Base Address
MMCS0_CTL_CFG	04F8 0000h

Table 18-91. MMCS0 Host Controller Registers

Offset	Acronym	Register Name	MMCS0_CTL_CFG Physical Address
Host Controller Interface Register			
0h	MMCS0_SDMA_SYS_ADDR_LO	32-bit Block Count/SDMA System Address Low Register	04F8 0000h
2h	MMCS0_SDMA_SYS_ADDR_HI	32-bit Block Count/SDMA System Address High Register	04F8 0002h
4h	MMCS0_BLOCK_SIZE	16-bit Block Size Register	04F8 0004h
6h	MMCS0_BLOCK_COUNT	16-bit Block Count Register	04F8 0006h
8h	MMCS0_ARGUMENT1_LO	Argument1 Low Register	04F8 0008h
Ah	MMCS0_ARGUMENT1_HI	Argument1 High Register	04F8 000Ah
Ch	MMCS0_TRANSFER_MODE	Transfer Mode Register	04F8 000Ch
Eh	MMCS0_COMMAND	Command Register	04F8 000Eh
10h to 1Eh	MMCS0_RESPONSE_0 to MMCS0_RESPONSE_7	Response Register	04F8 0010h to 04F8 001Eh
20h	MMCS0_DATA_PORT	Buffer Data Port Register	04F8 0020h
24h	MMCS0_PRESENTSTATE	Present State Register	04F8 0024h
28h	MMCS0_HOST_CONTROL1	Host Control 1 Register	04F8 0028h
29h	MMCS0_POWER_CONTROL	Power Control Register	04F8 0029h
2Ah	MMCS0_BLOCK_GAP_CONTROL	Block Gap Control Register	04F8 002Ah
2Bh	MMCS0_WAKEUP_CONTROL	Wakeup Control Register	04F8 002Bh
2Ch	MMCS0_CLOCK_CONTROL	Clock Control Register	04F8 002Ch
2Eh	MMCS0_TIMEOUT_CONTROL	Timeout Control Register	04F8 002Eh
2Fh	MMCS0_SOFTWARE_RESET	Software Reset Register	04F8 002Fh
30h	MMCS0_NORMAL_INTR_STS	Normal Interrupt Status Register	04F8 0030h
32h	MMCS0_ERROR_INTR_STS	Error Interrupt Status Register	04F8 0032h
34h	MMCS0_NORMAL_INTR_STS_ENA	Normal Interrupt Status Enable Register	04F8 0034h
36h	MMCS0_ERROR_INTR_STS_ENA	Error Interrupt Status Enable Register	04F8 0036h
38h	MMCS0_NORMAL_INTR_SIG_ENA	Normal Interrupt Signal Enable Register	04F8 0038h
3Ah	MMCS0_ERROR_INTR_SIG_ENA	Error Interrupt Signal Enable Register	04F8 003Ah
3Ch	MMCS0_AUTOCMD_ERR_STS	Auto CMD Error Status Register	04F8 003Ch
3Eh	MMCS0_HOST_CONTROL2	Host Control 2 Register	04F8 003Eh
40h	MMCS0_CAPABILITIES	Capabilities Register	04F8 0040h
48h	MMCS0_MAX_CURRENT_CAP	Maximum Current Capabilities Register	04F8 0048h
50h	MMCS0_FORCE_EVNT_ACMD_ERR_STS	Force Event Register for Auto CMD Error Status	04F8 0050h
52h	MMCS0_FORCE_EVNT_ERR_INT_STS	Force Event Register for Error Interrupt Status	04F8 0052h
54h	MMCS0_ADMA_ERR_STATUS	ADMA Error Status Register	04F8 0054h

Table 18-91. MMCS0 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCS0_CTL_CFG Physical Address
58h	MMCS0_ADMA_SYS_ADDRESS	ADMA System Address Register	04F8 0058h
60h	MMCS0_PRESET_VALUE0	Preset Values 0 Register	04F8 0060h
62h	MMCS0_PRESET_VALUE1	Preset Values 1 Register	04F8 0062h
64h	MMCS0_PRESET_VALUE2	Preset Values 2 Register	04F8 0064h
66h	MMCS0_PRESET_VALUE3	Preset Values 3 Register	04F8 0066h
68h	MMCS0_PRESET_VALUE4	Preset Values 4 Register	04F8 0068h
6Ah	MMCS0_PRESET_VALUE5	Preset Values 5 Register	04F8 006Ah
6Ch	MMCS0_PRESET_VALUE6	Preset Values 6 Register	04F8 006Ch
6Eh	MMCS0_PRESET_VALUE7	Preset Values 7 Register	04F8 006Eh
72h	MMCS0_PRESET_VALUE8	Preset Values 8 Register	04F8 0072h
74h	MMCS0_PRESET_VALUE10	Preset Values 10 Register	04F8 0074h
78h	MMCS0_ADMA3_DESC_ADDRESS	ADMA3 Integrated Descriptor Address Register	04F8 0078h
UHS-II Registers ⁽¹⁾			
80h	MMCS0_UHS2_BLOCK_SIZE	UHS-II Block Size Register	04F8 0080h
84h	MMCS0_UHS2_BLOCK_COUNT	UHS-II Block Count Register	04F8 0084h
88h to 9Bh	MMCS0_UHS2_COMMAND_PKT_0 to MMCS0_UHS2_COMMAND_PKT_19	UHS-II Command Packet Register	04F8 0088h to 04F8 009Bh
9Ch	MMCS0_UHS2_XFER_MODE	UHS-II Transfer Mode Register	04F8 009Ch
9Eh	MMCS0_UHS2_COMMAND	UHS-II Command Register	04F8 009Eh
A0h to B3h	MMCS0_UHS2_RESPONSE_0 to MMCS0_UHS2_RESPONSE_19	UHS-II Response Register	04F8 00A0h to 04F8 00B3h
B4h	MMCS0_UHS2_MESSAGE_SELECT	UHS-II Message Select Register	04F8 00B4h
B8h	MMCS0_UHS2_MESSAGE	UHS-II Message Register	04F8 00B8h
BCh	MMCS0_UHS2_DEVICE_INTR_STATUS	UHS-II Device Interrupt Status Register	04F8 00BCh
BEh	MMCS0_UHS2_DEVICE_SELECT	UHS-II Device Select Register	04F8 00BEh
BFh	MMCS0_UHS2_DEVICE_INT_CODE	UHS-II Device Interrupt Code Register	04F8 00BFh
C0h	MMCS0_UHS2_SOFTWARE_RESET	UHS-II Software Reset Register	04F8 00C0h
C2h	MMCS0_UHS2_TIMER_CONTROL	UHS-II Timeout Control Register	04F8 00C2h
C4h	MMCS0_UHS2_ERR_INTR_STS	UHS-II Error Interrupt Status Register	04F8 00C4h
C8h	MMCS0_UHS2_ERR_INTR_STS_ENA	UHS-II Error Interrupt Status Enable Register	04F8 00C8h
CCh	MMCS0_UHS2_ERR_INTR_SIG_ENA	UHS-II Error Interrupt Signal Enable Register	04F8 00CCh
E0h	MMCS0_UHS2_SETTINGS_PTR	Pointer for UHS-II Settings Register	04F8 00E0h
E2h	MMCS0_UHS2_CAPABILITIES_PTR	Pointer for UHS-II Host Capabilities Register	04F8 00E2h
E4h	MMCS0_UHS2_TEST_PTR	Pointer for UHS-II Test Register	04F8 00E4h
E6h	MMCS0_SHARED_BUS_CTRL_PTR	Pointer for Embedded Control Register	04F8 00E6h
E8h	MMCS0_VENDOR_SPECIFIC_PTR	Pointer for Vendor Specific Area Register	04F8 00E8h
F4h	MMCS0_BOOT_TIMEOUT_CONTROL	Boot Timeout Control Register	04F8 00F4h
F8h	MMCS0_VENDOR_REGISTER	Vendor Register	04F8 00F8h
FCh	MMCS0_SLOT_INT_STS	Slot Interrupt Status Register	04F8 00FCh
FEh	MMCS0_HOST_CONTROLLER_VER	Host Controller Version Register	04F8 00FEh
100h	MMCS0_UHS2_GEN_SETTINGS	UHS-II General Settings Register	04F8 0100h
104h	MMCS0_UHS2_PHY_SETTINGS	UHS-II PHY Settings Register	04F8 0104h
108h	MMCS0_UHS2_LNK_TRN_SETTINGS	UHS-II LINK/TRAN Settings Register	04F8 0108h
110h	MMCS0_UHS2_GEN_CAP	UHS-II General Capabilities Register	04F8 0110h
114h	MMCS0_UHS2_PHY_CAP	UHS-II PHY Capabilities Register	04F8 0114h
118h	MMCS0_UHS2_LNK_TRN_CAP	UHS-II LINK/TRAN Capabilities Register	04F8 0118h

Table 18-91. MMCS0 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCS0_CTL_CFG Physical Address
120h	MMCS0_FORCE_UHSII_ERR_INT_STS	Force Event for UHS-II Error Interrupt Status Register	04F8 0120h
Command Queue Registers			
200h	MMCS0_CQ_VERSION	Command Queueing Version Register	04F8 0200h
204h	MMCS0_CQ_CAPABILITIES	Command Queueing Capabilities Register	04F8 0204h
208h	MMCS0_CQ_CONFIG	Command Queueing Configuration Register	04F8 0208h
20Ch	MMCS0_CQ_CONTROL	Command Queueing Control Register	04F8 020Ch
210h	MMCS0_CQ_INTR_STS	Command Queueing Interrupt Status Register	04F8 0210h
214h	MMCS0_CQ_INTR_STS_ENA	Command Queueing Interrupt Status Enabled Register	04F8 0214h
218h	MMCS0_CQ_INTR_SIG_ENA	Command Queueing Interrupt Signal Enable Register	04F8 0218h
21Ch	MMCS0_CQ_INTR_COALESCING	Interrupt Coalescing Register	04F8 021Ch
220h	MMCS0_CQ_TDL_BASE_ADDR	Command Queueing Task Descriptor List Base Address Low Register	04F8 0220h
224h	MMCS0_CQ_TDL_BASE_ADDR_UPBITS	Command Queueing Task Descriptor List Base Address High Register	04F8 0224h
228h	MMCS0_CQ_TASK_DOOR_BELL	Command Queueing Task Doorbell Register	04F8 0228h
22Ch	MMCS0_CQ_TASK_COMP_NOTIF	Command Queueing Task Doorbell Notification Register	04F8 022Ch
230h	MMCS0_CQ_DEV_QUEUE_STATUS	Command Queueing Device Queue Status Register	04F8 0230h
234h	MMCS0_CQ_DEV_PENDING_TASKS	Command Queueing Device Pending Tasks Register	04F8 0234h
238h	MMCS0_CQ_TASK_CLEAR	Command Queueing Task Clear Register	04F8 0238h
240h	MMCS0_CQ_SEND_STS_CONFIG1	Send Status Timer Configuration 1 Register	04F8 0240h
244h	MMCS0_CQ_SEND_STS_CONFIG2	Send Status Configuration 2 Register	04F8 0244h
248h	MMCS0_CQ_DCMD_RESPONSE	Command Response Register for Direct Command Task	04F8 0248h
250h	MMCS0_CQ_RESP_ERR_MASK	Response Mode Error Mask Register	04F8 0250h
254h	MMCS0_CQ_TASK_ERR_INFO	Task Error Information Register	04F8 0254h
258h	MMCS0_CQ_CMD_RESP_INDEX	Command Response Index Register	04F8 0258h
25Ch	MMCS0_CQ_CMD_RESP_ARG	Command Response Argument Register	04F8 025Ch
260h	MMCS0_CQ_ERROR_TASK_ID	Command Queueing Error Task ID Register	04F8 0260h

(1) UHSII is not supported. For more information, see *Not Supported Features*.

18.2.1 MMCSD0_SDMA_SYS_ADDR_LO Register (Offset = 0h) [reset = 0h]

MMCSD0_SDMA_SYS_ADDR_LO is shown in [Figure 18-30](#) and described in [Table 18-93](#).

Return to [Summary Table](#).

This register contains the Lower 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

**Table 18-92. MMCSD0_SDMA_SYS_ADDR_LO
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0000h

Figure 18-30. MMCSD0_SDMA_SYS_ADDR_LO Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMA_ADDRESS															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-93. MMCS0_SDMA_SYS_ADDR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDMA_ADDRESS	R/W	0h	<p>32-bit Block Count (SDMA System Address) Low</p> <p>When the MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h, DMA uses this register as system address in only 32-bit addressing mode. Auto CMD23 cannot be used with SDMA.</p> <p>When the MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, SDMA uses the MMCS0_ADMA_SYS_ADDRESS register instead of using this register to support both 32-bit and 64-bit addressing. This register is re-assigned to 32-bit Block Count and then SDMA may use Auto CMD23.</p> <p>(1) SDMA System Address (MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h)</p> <p>This register contains the system memory address for a SDMA transfer in 32-bit addressing mode. When the Host Controller (HC) stops a SDMA transfer, this register shall point to the system address of the next contiguous data position.</p> <p>It can be accessed only if no transaction is executing (after a transaction has stopped). Reading this register during SDMA transfers may return an invalid value. The Host Driver (HD) shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the MMCS0_BLOCK_SIZE[14-12] SDMA_BUF_SIZE bit field. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (Offset = 3h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by setting the MMCS0_BLOCK_GAP_CONTROL[1] CONTINUE bit, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register (MMCS0_SDMA_SYS_ADDR_LO/ MMCS0_SDMA_SYS_ADDR_HI). ADMA does not use this register.</p> <p>(2) 32-bit Block Count (MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h)</p> <p>Host Controller Version 4.10 re-defines this register as 32-bit Block Count . In version 4.00, this register may be used as 32-bit block count only for Auto CMD23 to set the argument of the CMD23 while executing Auto CMD23.</p> <p>The Host Controller would decrement the block count of this register every block transfer and data transfer stops when the count reaches zero.</p> <p>FFFF FFFFh (4G - 1 Block)</p> <p>....</p> <p>0000 0002h (2 Blocks)</p> <p>0000 0001h (1 Block)</p> <p>0000 0000h (Stop Count)</p> <p>Note: This register should be accessed only when no transaction is executing. Reading this register during data transfers may return invalid value.</p>

18.2.2 MMCSD0_SDMA_SYS_ADDR_HI Register (Offset = 2h) [reset = 0h]

MMCSD0_SDMA_SYS_ADDR_HI is shown in [Figure 18-31](#) and described in [Table 18-95](#).

Return to [Summary Table](#).

This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

**Table 18-94. MMCSD0_SDMA_SYS_ADDR_HI
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0002h

Figure 18-31. MMCSD0_SDMA_SYS_ADDR_HI Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMA_ADDRESS															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-95. MMCSD0_SDMA_SYS_ADDR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDMA_ADDRESS	R/W	0h	32-bit Block Count (SDMA System Address) High This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

18.2.3 MMCS0_BLOCK_SIZE Register (Offset = 4h) [reset = 0h]

MMCS0_BLOCK_SIZE is shown in [Figure 18-32](#) and described in [Table 18-97](#).

Return to [Summary Table](#).

This register is used to configure the number of bytes in a data block.

Table 18-96. MMCS0_BLOCK_SIZE Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0004h

Figure 18-32. MMCS0_BLOCK_SIZE Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_SIZE			XFER_BLK_SIZE			
R-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
XFER_BLK_SIZE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-97. MMCS0_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	SDMA_BUF_SIZE	R/W	0h	<p>Host SDMA Buffer Size</p> <p>To perform long DMA transfer, System Address register (MMCS0_SDMA_SYS_ADDR_LO/ MMCS0_SDMA_SYS_ADDR_HI) shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the System Address register (MMCS0_SDMA_SYS_ADDR_LO/ MMCS0_SDMA_SYS_ADDR_HI).</p> <p>These bits shall support when the MMCS0_CAPABILITIES[22] SDMA_SUPPORT bit is set to 1h and this function is active when the MMCS0_TRANSFER_MODE[0] DMA_ENA bit is set to 1h.</p> <p>0h: 4KB (Detects A11 Carry out) 1h: 8KB (Detects A12 Carry out) 2h: 16KB (Detects A13 Carry out) 3h: 32KB (Detects A14 Carry out) 4h: 64KB (Detects A15 Carry out) 5h: 128KB (Detects A16 Carry out) 6h: 256KB (Detects A17 Carry out) 7h: 512KB (Detects A18 Carry out)</p>

Table 18-97. MMCSD0_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	XFER_BLK_SIZE	R/W	0h	<p>Transfer Block Size</p> <p>This field specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. It can be accessed only if no transaction is executing (after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored.</p> <p>0000h: No Data Transfer</p> <p>0001h: 1 Byte</p> <p>0002h: 2 Bytes</p> <p>0003h: 3 Bytes</p> <p>0004h: 4 Bytes</p> <p>....</p> <p>01FFh: 511 Bytes</p> <p>0200h: 512 Bytes</p> <p>....</p> <p>0800h: 2048 Bytes</p>

18.2.4 MMCSDB_BLOCK_COUNT Register (Offset = 6h) [reset = 0h]

MMCSDB_BLOCK_COUNT is shown in [Figure 18-33](#) and described in [Table 18-99](#).

Return to [Summary Table](#).

This register is used to configure the number of data blocks.

Table 18-98. MMCSDB_BLOCK_COUNT Instances

Instance	Physical Address
MMCSDB_CTL_CFG	04F8 0006h

Figure 18-33. MMCSDB_BLOCK_COUNT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XFER_BLK_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-99. MMCSDB_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	XFER_BLK_CNT	R/W	0h	<p>16-bit Block Count</p> <p>Host Controller Version 4.10 extends block count to 32-bit .</p> <p>Selection of either 16-bit Block Count register or 32-bit Block Count register is defined as follows:</p> <p>(1) If the MMCSDB_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h or 16-bit Block Count register is set to non-zero, 16-bit Block Count register is selected.</p> <p>(2) If the MMCSDB_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h and 16-bit Block Count register is set to zero, 32-bit Block Count register is selected.</p> <p>Use of 16-bit/32-bit Block Count register is enabled when the MMCSDB_TRANSFER_MODE[1] BLK_CNT_ENA bit is set to 1h and is valid only for multiple block transfers.</p> <p>The Host Driver shall set this register to a value between 1h and the maximum block count. The Host Controller decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0h results in no data blocks is transferred.</p> <p>This register should be accessed only when no transaction is executing (after transactions are stopped).</p> <p>During data transfer, read operations on this register may return an invalid value and write operations are ignored.</p> <p>0000h: Stop Count</p> <p>0001h: 1 Block</p> <p>0002h: 2 Blocks</p> <p>....</p> <p>FFFFh: 65535 Blocks</p>

18.2.5 MMCSD0_ARGUMENT1_LO Register (Offset = 8h) [reset = 0h]

MMCSD0_ARGUMENT1_LO is shown in [Figure 18-34](#) and described in [Table 18-101](#).

Return to [Summary Table](#).

This register contains Lower bits of SD Command Argument.

Table 18-100. MMCSD0_ARGUMENT1_LO Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0008h

Figure 18-34. MMCSD0_ARGUMENT1_LO Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ARG1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-101. MMCSD0_ARGUMENT1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_ARG1	R/W	0h	Command Argument 1 Low The SD Command Argument is specified as bit 23-8 of Command-Format.

18.2.6 MMCS0_ARGUMENT1_HI Register (Offset = Ah) [reset = 0h]

MMCS0_ARGUMENT1_HI is shown in [Figure 18-35](#) and described in [Table 18-103](#).

Return to [Summary Table](#).

This register contains higher bits of SD Command Argument.

Table 18-102. MMCS0_ARGUMENT1_HI Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 000Ah

Figure 18-35. MMCS0_ARGUMENT1_HI Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ARG1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-103. MMCS0_ARGUMENT1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_ARG1	R/W	0h	Command Argument 1 High The SD Command Argument is specified as bit 39-24 of Command-Format.

18.2.7 MMCSD0_TRANSFER_MODE Register (Offset = Ch) [reset = 0h]

MMCSD0_TRANSFER_MODE is shown in [Figure 18-36](#) and described in [Table 18-105](#).

Return to [Summary Table](#).

**Table 18-104. MMCSD0_TRANSFER_MODE
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 000Ch

Figure 18-36. MMCSD0_TRANSFER_MODE Register

15	14	13	12	11	10	9	8
RESERVED							RESP_INTR_DIS
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESP_ERR_CHK_ENA	RESP_TYPE	MULTI_BLK_SEL	DATA_XFER_DIR	AUTO_CMD_ENA		BLK_CNT_ENA	DMA_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-105. MMCSD0_TRANSFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	<p>Response Interrupt Disable</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0h and waits Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE) and then checks the Response register (MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7).</p> <p>If Host Controller checks response error, sets this bit to 1h and sets the MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA bit to 1h. Command Complete Interrupt (MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE) is disabled by this bit regardless of Command Complete Signal Enable (MMCSD0_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE).</p> <p>0h: Response Interrupt is enabled 1h: Response Interrupt is disabled</p>
7	RESP_ERR_CHK_ENA	R/W	0h	<p>Response Error Check Enable</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.</p> <p>If Host Driver checks response error, this bit is set to 0h and the MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 0h.</p> <p>If Host Controller checks response error, sets this bit to 1h and sets the Response Interrupt Disable bit to 1h (MMCSD0_TRANSFER_MODE[8] RESP_INTR_DIS = 1h).</p> <p>The MMCSD0_TRANSFER_MODE[6] RESP_TYPE bit selects either R1 or R5 response type. If an error is detected, Response Error Interrupt is generated in the MMCSD0_ERROR_INTR_STS register.</p> <p>0h: Response Error Check is disabled 1h: Response Error Check is enabled</p>

Table 18-105. MMCS0_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESP_TYPE	R/W	0h	<p>Response Type R1/R5</p> <p>When response error check is enabled (MMCS0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1h), this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO.</p> <p>Error Statuses Checked in R1:</p> <p>Bit31 OUT_OF_RANGE</p> <p>Bit30 ADDRESS_ERROR</p> <p>Bit29 BLOCK_LEN_ERROR</p> <p>Bit26 WP_VIOLATION</p> <p>Bit25 CARD_IS_LOCKED</p> <p>Bit23 COM_CRC_ERROR</p> <p>Bit21 CARD_ECC_FAILED</p> <p>Bit20 CC_ERROR</p> <p>Bit19 ERROR</p> <p>Response Flags Checked in R5:</p> <p>Bit07 COM_CRC_ERROR</p> <p>Bit03 ERROR</p> <p>Bit01 FUNCTION_NUMBER</p> <p>Bit00 OUT_OF_RANGE</p> <p>0h: R1 (Memory)</p> <p>1h: R5 (SDIO)</p>
5	MULTI_BLK_SEL	R/W	0h	<p>Multi/Single Block Select</p> <p>This bit enables multiple block data transfers.</p> <p>0h: Single Block</p> <p>1h: Multiple Block</p>
4	DATA_XFER_DIR	R/W	0h	<p>Data Transfer Direction Select</p> <p>This bit defines the direction of data transfers.</p> <p>0h: Write (Host to Card)</p> <p>1h: Read (Card to Host)</p>

Table 18-105. MMCS0_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	AUTO_CMD_ENA	R/W	0h	<p>Auto CMD Enable</p> <p>This field determines use of auto command functions. There are three methods to stop Multiple-block read and write operation by CMD23 or CMD12. In the other operations (for example single read/write operation), this field is set to 0h.</p> <p>(1) Auto CMD12 Enable:</p> <p>Multiple-block read and write commands for memory require CMD12 to stop the operation. When this field is set to 1h, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the MMCS0_AUTOCMD_ERR_STS register. The Host Driver shall not set this bit if the command does not require CMD12.</p> <p>When MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h, CMD12 is issued when 16-bit Block Count is expired.</p> <p>When MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h, CMD12 is issued when 16-bit Block Count or 32-bit Block Count is expired.</p> <p>(2) Auto CMD23 Enable:</p> <p>When this bit field is set to 2h, the Host Controller issues a CMD23 automatically before issuing a command specified in the MMCS0_COMMAND register. The Host Controller Version 3.00 and later shall support this function.</p> <p>The following conditions are required to use the Auto CMD23:</p> <p>Auto CMD23 Supported (Host Controller Version is 3.00 or later).</p> <p>A memory card that supports CMD23 (SCR[33] = 1h).</p> <p>If DMA is used, it shall be ADMA.</p> <p>Only when CMD18 or CMD25 is issued. Auto CMD23 can be used with or without ADMA. By writing the MMCS0_COMMAND register, the Host Controller issues a CMD23 first and then issues a command specified by the MMCS0_COMMAND[13:8] CMD_INDEX bit field. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the MMCS0_AUTOCMD_ERR_STS register.</p> <p>32-bit block count value for CMD23 is set to 32-bit Block Count (MMCS0_SDMA_SYS_ADDR_LO/MMCS0_SDMA_SYS_ADDR_HI) register.</p> <p>(3) Auto CMD Auto Select (Version 4.10):</p> <p>As CMD23 is optional for SD memory card except UHS 104 card, if card supports CMD23, Auto CMD 23 should be used instead of Auto CMD12. Host Controller Version 4.10 defines this "Auto CMD Auto Select" mode. Selection of Auto CMD depends on setting of the MMCS0_HOST_CONTROL2[11] CMD23_ENA bit which indicates whether card supports CMD23. If MMCS0_HOST_CONTROL2[11] CMD23_ENA = 1h, Auto CMD23 is used and if MMCS0_HOST_CONTROL2[11] CMD23_ENA = 0h, Auto CMD12 is used. In case of Version 4.10 or later, use of Auto CMD Auto Select is recommended rather than use of Auto CMD12 Enable or Auto CMD23 Enable.</p> <p>0h: Auto Command Disabled</p> <p>1h: Auto CMD12 Enable</p> <p>2h: Auto CMD23 Enable</p> <p>3h: Reserved</p>

Table 18-105. MMCS0_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BLK_CNT_ENA	R/W	0h	Block Count Enable This bit is used to enable the MMCS0_BLOCK_COUNT register, which is only relevant for multiple block transfers. When this bit is 0h, the MMCS0_BLOCK_COUNT register is disabled, which is useful in executing an infinite transfer. 0h: Disable 1h: Enable
0	DMA_ENA	R/W	0h	DMA Enable DMA can be enabled only if the MMCS0_CAPABILITIES[22] SDMA_SUPPORT bit is set. If this bit is set to 1h, a DMA operation shall begin when the HD writes to the upper byte of the MMCS0_COMMAND register. 0h: Disable 1h: Enable

This register is used to control the operations of data transfers.

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data (Refer to MMCS0_COMMAND[5] DATA_PRESENT bit), or before issuing a Resume command. The Host Driver shall save the value of this register when the data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller shall implement write protection for this register during data transactions. Writes to this register shall be ignored when the MMCS0_PRESENTSTATE[1] INHIBIT_DAT bit is 1h.

Table 18-106 shows the determination of transfer type.

Table 18-106. Determination of Transfer Type

Multi/Single Block Select	Block Count Enable	Block Count	Function
0	Don't Care	Don't Care	Single Transfer
1	0	Don't Care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

18.2.8 MMCSD0_COMMAND Register (Offset = Eh) [reset = 0h]

MMCSD0_COMMAND is shown in [Figure 18-37](#) and described in [Table 18-108](#).

Return to [Summary Table](#).

This register is used to program the Command for host controller.

Table 18-107. MMCSD0_COMMAND Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 000Eh

Figure 18-37. MMCSD0_COMMAND Register

15	14	13	12	11	10	9	8
RESERVED		CMD_INDEX					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
CMD_TYPE	DATA_PRESEN T	CMD_INDEX_C HK_ENA	CMD_CRC_CH K_ENA	SUB_CMD	RESP_TYPE_SEL		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-108. MMCSD0_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	CMD_INDEX	R/W	0h	Command Index This bit shall be set to the command number (CMD0-63, ACMD0-63).
7-6	CMD_TYPE	R/W	0h	Command Type There are three types of special commands. Suspend, Resume and Abort. These bits shall be set to 0h for all other commands. Suspend Command: If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state, and the HD shall restart the transfer by setting the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit. Resume Command: The HD re-starts the data transfer by restoring the registers in the range of 04F8 0000h - 04F8 000Dh. The HC shall check for busy before starting write transfers. Abort Command: If this command is set when executing a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a write transfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset. 0h: Normal 1h: Suspend 2h: Resume 3h: Abort

Table 18-108. MMCS0_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DATA_PRESENT	R/W	0h	<p>Data Present Select</p> <p>This bit is set to 1h to indicate that data is present and shall be transferred using the DAT line. If is set to 0h for the following:</p> <ol style="list-style-type: none"> 1. Commands using only CMD line (for example CMD52). 2. Commands with no data transfer but using busy signal on DAT[0]line (R1b or R5b for example CMD38). 3. Resume Command. <p>0h: No Data Present 1h: Data Present</p>
4	CMD_INDEX_CHK_ENA	R/W	0h	<p>Command Index Check Enable</p> <p>If this bit is set to 1h, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0h, the Index field is not checked.</p> <p>0h: Disable 1h: Enable</p>
3	CMD_CRC_CHK_ENA	R/W	0h	<p>Command CRC Check Enable</p> <p>If this bit is set to 1h, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0h, the CRC field is not checked.</p> <p>0h: Disable 1h: Enable</p>
2	SUB_CMD	R/W	0h	<p>Sub Command Flag</p> <p>This bit is added from Version 4.10 to distinguish a main command or sub command. When issuing a main command, this bit is set to 0h and when issuing a sub command, this bit is set to 1h. Setting of this bit is checked by the MMCS0_PRESENTSTATE[28] SUB_COMMAND_STS bit.</p> <p>Host Driver manages whether main or sub command. Host Controller does not refer to this bit to issue a command.</p> <p>0h: Sub Command 1h: Main Command</p>
1-0	RESP_TYPE_SEL	R/W	0h	<p>Response Type Select</p> <p>0h: No Response 1h: Response length 136 2h: Response length 48 3h: Response length 48 check Busy after response</p>

18.2.9 MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7 Register (Offset = 10h to 1Eh) [reset = 0h]

MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7 is shown in [Figure 18-38](#) and described in [Table 18-110](#).

Return to [Summary Table](#).

This registers is used to store responses from SD Cards.

**Table 18-109. MMCSD0_RESPONSE_0 to
MMCSD0_RESPONSE_7 Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0010h to 04F8 001Eh

Figure 18-38. MMCSD0_RESPONSE_0 to MMCSD0_RESPONSE_7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_RESP															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 18-110. Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_RESP	R	0h	Command Response R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.

[Table 18-111](#) defines the relation between the parameter and name of response type.

Table 18-111. Relation between Parameters and the Name of Response Type

Response Type	Index Check Enable	CRC Check Enable	Name of Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R6, R5, R7
11	1	1	R1b, R5b

The following table describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.

[Table 18-112](#) shows response bit definition for each response type.

Table 18-112. Response Bit Definition for each Response Type

Kind of Response	Meaning of Response	Response Field	Response Register
R1, R1b (normal response)	Card Status	R[39:8]	REP[31:0]
R1b (Auto CMD12 response)	Card Status for Auto CMD12	R[39:8]	REP[127:96]
R1 (Auto CMD23 response)	Card Status for Auto CMD23	R[39:8]	REP [127:96]
R2 (CID, CSD Register)	CID or CSD register include	R[127:8]	REP[119:0]
R3 (OCR Register)	OCR Register for memory	R[39:8]	REP[31:0]
R4 (OCR Register)	OCR Register for I/O etc.	R[39:8]	REP[31:0]
R5, R5b	SDIO Response	R[39:8]	REP[31:0]
R6 (Published RCA response)	New published RCA[31:16] etc.	R[39:8]	REP[31:0]

The Response Field indicates bit positions of "Responses" defined in the Physical Layer Specification. The table shows most responses with a length of 48 (R[47:0]) have 32 bits of the response data (R[39:8]) stored

in the Response register at REP[31:0]. Responses of type R1b (Auto CMD12 responses) and R1 (Auto CMD23 response) have response data bits R[39:8] stored in the Response register at REP[127:96]. Responses with length 136 (R[135:0]) have 120 bits of the response data (R[127:8]) stored in the Response register at REP[119:0].

To read the response status efficiently, the Host Controller only stores part of the response data in the Response register. This enables the Host Driver to read 32 bits of response data efficiently in one read cycle on a 32-bit bus system. Parts of the response, the Index field and the CRC, are checked by the Host Controller (as specified by the MMCSD0_COMMAND[4] CMD_INDEX_CHK_ENA and MMCSD0_COMMAND[3] CMD_CRC_CHK_ENA bits) and generate an error interrupt if an error is detected. The bit range for the CRC check depends on the response length. If the response length is 48, the Host Controller shall check R[47:1], and if the response length is 136 the Host Controller shall check R[119:1].

Since the Host Controller may have a multiple block data DAT line transfer executing concurrently with a CMD_wo_DAT command, the Host Controller stores the Auto CMD12 response in the upper bits (REP[127:96]) of the Response register. The CMD_wo_DAT response is stored in REP[31:0]. This allows the Host Controller to avoid overwriting the Auto CMD12 response with the CMD_wo_DAT and vice versa.

While executing Auto CMD23, the response of CMD23 is saved to REP [127:96] and the response of multiple-block read and write command is save to REP [31:0]. The response error of CMD23 is indicated in the MMCSD0_AUTOCMD_ERR_STS register. When the Host Controller modifies part of the Response register, as shown in the table, it shall preserve the unmodified bits.

18.2.10 MMCSD0_DATA_PORT Register (Offset = 20h) [reset = 0h]

MMCSD0_DATA_PORT is shown in [Figure 18-39](#) and described in [Table 18-114](#).

Return to [Summary Table](#).

This register is used to access internal buffer.

Table 18-113. MMCSD0_DATA_PORT Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0020h

Figure 18-39. MMCSD0_DATA_PORT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUF_RD_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-114. MMCSD0_DATA_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUF_RD_DATA	R/W	0h	Buffer Data The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

18.2.11 MMCS0_PRESENTSTATE Register (Offset = 24h) [reset = 1F00000h]

MMCS0_PRESENTSTATE is shown in [Figure 18-40](#) and described in [Table 18-116](#).

Return to [Summary Table](#).

The Host Driver can get status of the Host Controller from this 32-bit read-only register.

Table 18-115. MMCS0_PRESENTSTATE Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0024h

Figure 18-40. MMCS0_PRESENTSTATE Register

31	30	29	28	27	26	25	24
UHS2_IF_DETECTION	UHS2_IF_LANE_SYNC	UHS2_DORMANT	SUB_COMMAND_STS	CMD_NOT_ISSUED_BY_ERR	RESERVED		SDIF_CMDIN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		R-1h
23	22	21	20	19	18	17	16
SDIF_DAT3IN	SDIF_DAT2IN	SDIF_DAT1IN	SDIF_DAT0IN	WRITE_PROTECT	CARD_DETECT	CARD_STATE_STABLE	CARD_INSERTED
R-1h	R-1h	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED				BUF_RD_ENA	BUF_WR_ENA	RD_XFER_ACTIVE	WR_XFER_ACTIVE
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
SDIF_DAT7IN	SDIF_DAT6IN	SDIF_DAT5IN	SDIF_DAT4IN	RETUNING_REQ	DATA_LINE_ACTIVE	INHIBIT_DAT	INHIBIT_CMD
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 18-116. MMCS0_PRESENTSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UHS2_IF_DETECTION	R	0h	<p>UHS-II IF Detection (UHS-II Only)</p> <p>This status indicates whether a card supports UHS-II IF. This status is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCS0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). UHS-II interface initialization is activated by setting the MMCS0_CLOCK_CONTROL[2] SD_CLK_ENA bit. Host Controller drives STB.L on D0 lane from EIDL state and waits for receiving STB.L on D1 lane. This bit is set to 1h if STB.L is detected on D1 lane. Host Controller shall compensate latency from setting SD Clock Enable to output STB.L on D0 lane when reading this status. This bit may be read any time after setting SD Clock Enable for faster UHS-II IF detection but Host Driver shall check this status at least 200μs period from setting SD Clock Enable (MMCS0_CLOCK_CONTROL[2] SD_CLK_ENA) until detecting UHS-II IF.</p> <p>After UHS-II IF is detected, this bit is cleared by when EIDL is detected on D0 lane, UHS-II Interface Enable is set to 0h (MMCS0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or Host full reset is executed.</p> <p>1h: UHS-II IF is detected 0h: UHS-II IF is not detected</p>

Table 18-116. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	UHS2_IF_LANE_SYNC	R	0h	<p>Lane Synchronization (UHS-II Only)</p> <p>This status indicates whether lane is synchronized in UHS-II mode. This status is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). On detecting UHS-II Interface (D31 = 1h), Host Controller provides SYN LSS on D0 lane and waits for receiving SYN LSS on D1 lane. If SYN LSS is detected on D1 lane, Host Controller provides LIDL LSS on D0 lane and waits for receiving LIDL LSS on D1 lane.</p> <p>In case of Version 4.00, this bit indicates completion of Device PHY Initialization by detecting LIDL LSS on D1 lane.</p> <p>From Version 4.10, Host Controller may implement a specific PHY verification method and PHY Initialization Failure can be indicated by keeping this bit to 0h even LIDL LSS is detected on D1 lane. Host Driver detects PHY Initialization Failure by timeout.</p> <p>This bit is cleared by when D0 lane is set to EIDL, UHS-II Interface Enable is set to 0h (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or executes Host full reset.</p> <p>1h: UHS-II PHY is initialized 0h: UHS-II PHY is not initialized</p>
29	UHS2_DORMANT	R	0h	<p>In Dormant State (UHS-II Only)</p> <p>This status indicates whether UHS-II lanes enter Dormant state. This function is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). On issuing GO_DORMAT_STATE command, "Go Dormant Command (7h)" is set to Command type in the UHS-II Command register (MMCSD0_UHS2_COMMAND[7:6] CMD_TYPE). This command type acts as a trigger to enter lanes into dormant state. Host Controller provides STB.H and EIDL on D0 lane and waits for receiving STB.H and EIDL on D1 lane. This bit is set to 1h after the time of T_DMT_ENTRY (750 RCLK cycle) or more from detecting EIDL on D1 lane.</p> <p>RCLK may be stopped in dormant state, by setting SD Clock Enable to 0h in the Clock Control register (MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA = 0h) while In Dormant State bit is set to 1h.</p> <p>On writing Clock Control register with setting SD Clock Enable to 1h (MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA = 1h), Host Controller wakes lanes to exit Dormant State and In Dormant State is set to 0h.</p> <p>In case of the card enters Hibernate Mode (RCLK is stopped), Host Driver may turn off VDD1 by clearing SD Bus Power for VDD1 bit in the MMCSD0_POWER_CONTROL register. Host Controller shall turn off VDD1 after stopping RCLK. This bit is cleared by when Host Controller drives STB.L on D0 lane, UHS-II Interface Enable is set to 0h (MMCSD0_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or executes Host full reset.</p> <p>1h: In DORMANT state 0h: Not in DORMANT state</p>

Table 18-116. MMCSDB0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	SUB_COMMAND_STS	R	0h	<p>Sub Command Status</p> <p>The MMCSDB0_COMMAND register and Response register (MMCSDB0_RESPONSE_0 to MMCSDB0_RESPONSE_7) are commonly used for main command and sub command. This status is used to distinguish which response error statuses, main command or sub command, indicated in the MMCSDB0_ERROR_INTR_STS register or in the MMCSDB0_UHS2_ERR_INTR_STS register. Just before reading of this register, the MMCSDB0_COMMAND[2] SUB_CMD bit or the MMCSDB0_UHS2_COMMAND register is copied to this status. This status is effective not only when Response Error interrupt is generated but also when data error interrupt is generated with Command Not Issued by Error (D27 of this register) or Auto CMD Error interrupt is generated with Command Not Issued by Error by Auto CMD12 in the MMCSDB0_AUTOCMD_ERR_STS register.</p> <p>1h: Sub Command Status 0h: Main Command Status</p>
27	CMD_NOT_ISS_BY_ERR	R	0h	<p>Command Not Issued by Error</p> <p>Setting of this status indicates that a command cannot be issued due to an error except Auto CMD12 error (equivalent error status by Auto CMD12 error is defined as Command Not Issued By Auto CMD12 Error in the MMCSDB0_AUTOCMD_ERR_STS register). This status is set to 1h when Host Controller cannot issue a command after setting MMCSDB0_COMMAND register or MMCSDB0_UHS2_COMMAND register. Sub Command Status (D28) indicates which command is not issued (main or sub).</p> <p>1h: Command cannot be issued 0h: No error for issuing a command</p>
26-25	RESERVED	R	0h	Reserved
24	SDIF_CMDIN	R	1h	<p>CMD Line Signal Level (SD Mode Only)</p> <p>This status is used to check CMD line level to recover from errors, and for debugging.</p>
23	SDIF_DAT3IN	R	1h	<p>DAT[3] Line Signal Level (SD Mode Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[3].</p> <p>D23 - DAT[3]</p>
22	SDIF_DAT2IN	R	1h	<p>DAT[2] Line Signal Level (SD Mode Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[2].</p> <p>D22 - DAT[2]</p>
21	SDIF_DAT1IN	R	1h	<p>DAT[1] Line Signal Level (SD Mode Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[1].</p> <p>D21 - DAT[1]</p>
20	SDIF_DAT0IN	R	1h	<p>DAT[0] Line Signal Level (SD Mode Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0].</p> <p>D20 - DAT[0]</p>

Table 18-116. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	WRITE_PROTECT	R	0h	Write Protect Switch Pin Level The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP pin. 0h: Write protected (SDWP = 1) 1h: Write enabled (SDWP = 0)
18	CARD_DETECT	R	0h	Card Detect Pin Level This bit reflects the inverse value of the SD_CD# pin. 0h: No Card present (SD_CD# = 1) 1h: Card present (SD_CD# = 0)
17	CARD_STATE_STABLE	R	0h	Card State Stable This bit is used for testing. If it is 0h, the Card Detect Pin Level is not stable. If this bit is set to 1h, it means the Card Detect Pin Level is stable. The MMCSD0_SOFTWARE_RESET[0] SWRST_FOR_ALL bit shall not affect this bit. 0h: Reset of Debouncing 1h: No Card or Inserted
16	CARD_INSERTED	R	0h	Card Inserted This bit indicates whether a card has been inserted. Changing from 0h to 1h generates a Card Insertion interrupt in the MMCSD0_NORMAL_INTR_STS register and changing from 1h to 0h generates a Card Removal Interrupt in the MMCSD0_NORMAL_INTR_STS register. The MMCSD0_SOFTWARE_RESET[0] SWRST_FOR_ALL bit shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear the MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit and the MMCSD0_CLOCK_CONTROL[2] SD_CLK_ENA bit. In addition the HD should clear the HC by the MMCSD0_SOFTWARE_RESET[0] SWRST_FOR_ALL bit. The card detect is active regardless of the SD Bus Power. 0h: Reset or Debouncing or No Card 1h: Card Inserted
15-12	RESERVED	R	0h	Reserved
11	BUF_RD_ENA	R	0h	Buffer Read Enable This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1h, readable data exists in the buffer. A change of this bit from 1h to 0h occurs when all the block data is read from the buffer. A change of this bit from 0h to 1h occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0h: Read Disable 1h: Read Enable
10	BUF_WR_ENA	R	0h	Buffer Write Enable This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1h, data can be written to the buffer. A change of this bit from 1h to 0h occurs when all the block data is written to the buffer. A change of this bit from 0h to 1h occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. 0h: Write Disable 1h: Write Enable

Table 18-116. MMCSDB0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RD_XFER_ACTIVE	R	0h	<p>Read Transfer Active (SD Mode Only)</p> <p>This status is used for detecting completion of a read transfer. This bit is set to 1h for either of the following conditions:</p> <p>After the end bit of the read command.</p> <p>When writing a 1h to continue Request in the MMCSDB0_BLOCK_GAP_CONTROL register to restart a read transfer.</p> <p>This bit is cleared to 0h for either of the following conditions:</p> <p>When the last data block as specified by block length is transferred to the system.</p> <p>When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1h (MMCSDB0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h). A transfer complete interrupt is generated when this bit changes to 0h.</p> <p>1h: Transferring data 0h: No valid data</p>
8	WR_XFER_ACTIVE	R	0h	<p>Write Transfer Active (SD Mode Only)</p> <p>This status indicates a write transfer is active. If this bit is 0h, it means no valid write data exists in the HC. This bit is set in either of the following cases:</p> <p>After the end bit of the write command.</p> <p>When writing a 1h to the MMCSDB0_BLOCK_GAP_CONTROL[1] CONTINUE bit to restart a write transfer.</p> <p>This bit is cleared in either of the following cases:</p> <p>After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple).</p> <p>After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0h, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy.</p> <p>1h: Transferring data 0h: No valid data</p>
7	SDIF_DAT7IN	R	0h	<p>DAT[7] Line Signal Level (Embedded Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging.</p> <p>D07 - DAT[7]</p>
6	SDIF_DAT6IN	R	0h	<p>DAT[6] Line Signal Level (Embedded Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging.</p> <p>D06 - DAT[6]</p>
5	SDIF_DAT5IN	R	0h	<p>DAT[5] Line Signal Level (Embedded Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging.</p> <p>D05 - DAT[5]</p>

Table 18-116. MMCSD0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SDIF_DAT4IN	R	0h	DAT[4] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D04 - DAT[4]
3	RETUNING_REQ	R	0h	Re-Tuning Request (UHS-I Only) Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting the MMCSD0_HOST_CONTROL2[6] EXECUTE_TUNING bit. Changing of this bit from 0h to 1h generates Re-Tuning Event. This bit isn't set to 1h if the MMCSD0_HOST_CONTROL2[7] SAMPLING_CLK_SELECT bit is set to 0h (using fixed sampling clock). 1h: Sampling clock needs re-tuning 0h: Fixed or well tuned sampling clock
2	DATA_LINE_ACTIVE	R	0h	DAT Line Active (SD Mode Only) This bit indicates whether one of the DAT line on SD bus is in use. 1h: DAT line active 0h: DAT line inactive
1	INHIBIT_DAT	R	0h	Command Inhibit (DAT) (SD Mode Only) This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1h. If this bit is 0h, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (for example R1b, R5b type). Changing from 1h to 0h generates a Transfer Complete interrupt in the MMCSD0_NORMAL_INTR_STS register. Note: The SD Host Driver can save registers in the range of 04F8 0000h - 04F8 000Dh for a suspend transaction after this bit has changed from 1h to 0h. 1h: Cannot issue command which uses the DAT line 0h: Can issue command which uses the DAT line

Table 18-116. MMCSDB0_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INHIBIT_CMD	R	0h	<p>Command Inhibit (CMD)</p> <p>SD Mode:</p> <p>If this bit is 0h, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the MMCSDB0_COMMAND register is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1h.</p> <p>Commands using only the CMD line can be issued if this bit is 0h. Changing from 1h to 0h generates a Command complete interrupt in the MMCSDB0_NORMAL_INTR_STS register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1h and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by the MMCSDB0_COMMAND register.</p> <p>UHS-II Mode:</p> <p>This bit is 0h means that a command packet can be issued by the Host Controller. While this bit is set to 1h, which means the Host Controller is not ready to issue a next command, Host Driver shall not write the registers from the MMCSDB0_UHS2_BLOCK_SIZE to the MMCSDB0_UHS2_COMMAND. Changing from 1h to 0h generates a Command Complete Interrupt in the MMCSDB0_NORMAL_INTR_STS register.</p> <p>1h: Host Controller is not ready to issue a command 0h: Host Controller is ready to issue a command</p> <p>Version 4.10 adds a new control to prevent error statuses from overwriting by receipt of a next command. This status keeps indicating 1h while any of response error statuses is set to 1h, Command Not Issued by Error in this register is set to 1h or the MMCSDB0_AUTOCMD_ERR_STS[7] CMD_NOT_ISSUED bit is set to 1h. Software Reset For CMD Line is used to clear the error statuses above and this status (MMCSDB0_SOFTWARE_RESET[1] SWRST_FOR_CMD).</p>

Note: DAT line active indicates whether one of the DAT line is on SD bus is in use.

(a) In the case of read transactions

This status indicates whether a read transfer is executing on the SD Bus. Changing this value from 1h to 0h generates a Block Gap Event interrupt in the MMCSDB0_NORMAL_INTR_STS register, as the result of the Stop At Block Gap Request being set.

This bit shall be set in either of the following cases:

- (1) After the end bit of the read command.
- (2) When writing a 1h to the MMCSDB0_BLOCK_GAP_CONTROL[1] CONTINUE bit to restart a read transfer.

This bit shall be cleared in either of the following cases:

(1) When the end bit of the last data block is sent from the SD Bus to the Host Controller. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.

(2) When a read transfer is stopped at the block gap initiated by a Stop At Block Gap Request (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP).

The Host Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Host Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use suspend/resume function.

(b) In the case of write transactions

This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1h to 0h generate a Transfer Complete interrupt in the MMCSD0_NORMAL_INTR_STS register.

This bit shall be set in either of the following cases:

(1) After the end bit of the write command.

(2) When writing to 1h to the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit to continue a write transfer.

This bit shall be cleared in either of the following cases:

(1) When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive "Not Busy". In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.

(2) When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request (MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP).

(c) Command with busy

This status indicates whether a command indicates busy (for example erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command with busy and cleared when busy is de-asserted. Changing this bit from 1h to 0h generate a Transfer Complete interrupt in the MMCSD0_NORMAL_INTR_STS register.

Note

The HD can issue cmd0, cmd12, cmd13 (for memory) and cmd52 (for SDIO) when the DAT lines are busy during data transfer. These commands can be issued when Command Inhibit (CMD) is set to zero (MMCSD0_PRESENTSTATE[0] INHIBIT_CMD = 0h). Other commands shall be issued when Command Inhibit (DAT) is set to zero (MMCSD0_PRESENTSTATE[1] INHIBIT_DAT = 0h).

18.2.12 MMCS0_HOST_CONTROL1 Register (Offset = 28h) [reset = 0h]

MMCS0_HOST_CONTROL1 is shown in [Figure 18-41](#) and described in [Table 18-118](#).

Return to [Summary Table](#).

This register is used to program DMA modes, LED control, data transfer width, High Speed enable, card detect test level and signal selection.

Table 18-117. MMCS0_HOST_CONTROL1 Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0028h

Figure 18-41. MMCS0_HOST_CONTROL1 Register

7	6	5	4	3	2	1	0
CD_SIG_SEL	CD_TEST_LEVEL	EXT_DATA_WIDTH	DMA_SELECT	HIGH_SPEED_ENA	DATA_WIDTH	LED_CONTROL	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-118. MMCS0_HOST_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CD_SIG_SEL	R/W	0h	Card Detect Signal Detection This bit selects source for card detection. 1h: The card detect test level is selected 0h: SDCD# is selected (for normal use)
6	CD_TEST_LEVEL	R/W	0h	Card Detect Test Level This bit is enabled while the Card Detect Signal Selection is set to 1h and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal interrupt status enable bit is set. 1h: Card Inserted 0h: No Card
5	EXT_DATA_WIDTH	R/W	0h	Extended Data Transfer Width (Embedded and SD Mode Only) This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the MMCS0_CAPABILITIES register. If a device supports 8-bit bus mode, this bit may be set to 1h. If this bit is 0h, bus width is controlled by the MMCS0_HOST_CONTROL1[1] DATA_WIDTH bit. This bit is not effective when multiple devices are installed on a bus slot (Slot Type is set to 2h in the MMCS0_CAPABILITIES register). In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register (MMCS0_SHARED_BUS_CTRL_PTR). 1h: 8-bit Bus Width 0h: Bus Width is Selected by Data Transfer Width

Table 18-118. MMCSD0_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	DMA_SELECT	R/W	0h	<p>DMA Select</p> <p>This field is used to select DMA type. The Host Driver shall check support of DMA modes by referring the MMCSD0_CAPABILITIES register. Selected DMA is enabled by the MMCSD0_TRANSFER_MODE[0] DMA_ENA bit in SD mode and the MMCSD0_UHS2_XFER_MODE[0] DMA_ENA bit in UHS-II mode.</p> <p>(1) Up to Version 3.00:</p> <p>When MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h, setting of this field is compatible to Host Controller Version 3.00.</p> <p>SDMA is initiated by writing to the MMCSD0_COMMAND register when this field is set to 0h and the SDMA System Address register (32-bit) is used (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI). SDMA does not support 64-bit addressing.</p> <p>ADMA2 is initiated by writing to the MMCSD0_COMMAND register when this field is set to 2h or 3h. Lower 32-bit of the ADMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) is used when this field is set to 2h and 64-bit of the ADMA System Address register is used when this field is set to 3h. Support of 64-bit System Addressing is indicated by the MMCSD0_CAPABILITIES[28] ADDR_64BIT_SUPPORT_V3 bit. 64-bit ADMA2 uses 96-bit Descriptor.</p> <p>0h: SDMA is selected</p> <p>1h: 32-bit Address ADMA1 is selected</p> <p>2h: 32-bit Address ADMA2 is selected</p> <p>3h: 64-bit Address ADMA2 is selected (Optional)</p> <p>(2) Version 4.00 or later:</p> <p>When the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, setting of this field is changed as follows.</p> <p>SDMA is initiated by Host Driver writes to the MMCSD0_COMMAND register when this field is set to 0h.</p> <p>ADMA2 is initiated by Host Driver writes to the MMCSD0_COMMAND register when this field is set to 2h or 3h and by ADMA3 sets to the ADMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) when this field is set to 3h.</p> <p>ADMA3 is initiated by Host Driver writes to the MMCSD0_ADMA3_DESC_ADDRESS register when this field is set to 3h.</p> <p>0h: SDMA is selected</p> <p>1h: Not Used (New assignment is not allowed)</p> <p>2h: ADMA2 is selected (ADMA3 is not supported or disabled)</p> <p>3h: ADMA2 or ADMA3 is selected</p> <p>Support of 64-bit DMA and 128-bit Descriptor is indicated by the MMCSD0_CAPABILITIES[27] ADDR_64BIT_SUPPORT_V4</p>

Table 18-118. MMCS0_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				bit. If the support bit is set to 1h, all supported DMAs (depends on Support, ADMA2 Support and ADMA3 Support) shall support 64-bit addressing. The MMCS0_HOST_CONTROL2[13] BIT64_ADDRESSING bit selects either 32-bit or 64-bit system addressing of DMAs.
2	HIGH_SPEED_ENA	R/W	0h	<p>High Speed Enable (SD Mode Only)</p> <p>This bit is optional. Before setting this bit, the HD shall check the MMCS0_CAPABILITIES[21] HIGH_SPEED_SUPPORT bit. If this bit is set to 0h (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/20 MHz for MMC). If this bit is set to 1h, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52 MHz for MMC)/208 MHz (for SD3.0).</p> <p>If the MMCS0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1h, Host Driver needs to reset SD Clock Enable (MMCS0_CLOCK_CONTROL[2] SD_CLK_ENA) before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. This bit is not effective in UHS-II mode.</p> <p>1h: High Speed Mode 0h: Normal Speed Mode</p>
1	DATA_WIDTH	R/W	0h	<p>Data Transfer Width (SD Mode Only)</p> <p>This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. This bit is not effective in UHS-II mode.</p> <p>1h: 4 bit mode 0h: 1 bit mode</p>
0	LED_CONTROL	R/W	0h	<p>LED Control</p> <p>This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction.</p> <p>1h: LED on 0h: LED off</p>

18.2.13 MMCSD0_POWER_CONTROL Register (Offset = 29h) [reset = 0h]

MMCSD0_POWER_CONTROL is shown in [Figure 18-42](#) and described in [Table 18-120](#).

Return to [Summary Table](#).

This register is used to program the SD Bus power and voltage level.

**Table 18-119. MMCSD0_POWER_CONTROL
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0029h

Figure 18-42. MMCSD0_POWER_CONTROL Register

7	6	5	4	3	2	1	0
UHS2_VOLTAGE			UHS2_POWER	SD_BUS_VOLTAGE			SD_BUS_POWER
R/W-0h			R/W-0h	R/W-0h			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-120. MMCSD0_POWER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	UHS2_VOLTAGE	R/W	0h	SD Bus Voltage Select for VDD2 (UHS-II Only) This field determines supply voltage range to VDD2. This field can be set to 5h if the MMCSD0_CAPABILITIES[60] VDD2_1P8_SUPPORT bit is set to 1h. 111b: Not used 110b: Not used 101b: 1.8 V 100b: Reserved for 1.2 V 011b – 001b: Reserved 000b: VDD2 Not Supported
4	UHS2_POWER	R/W	0h	SD Bus Power for VDD2 (UHS-II Only) Setting this bit enables providing VDD2. 1h: Power on 0h: Power off
3-1	SD_BUS_VOLTAGE	R/W	0h	SD Bus Voltage Select for VDD1 By setting these bits, the HD selects the voltage level for the SD card. Before setting this register, the HD shall check the voltage support bits in the MMCSD0_CAPABILITIES register. If an unsupported voltage is selected, the Host System shall not supply SD bus voltage. 111b: 3.3 V (Flat-top.) 110b: 3.0 V (Typ.) 101b: 1.8 V (Typ.) for Embedded 100b – 000b: Reserved

Table 18-120. MMCS0_POWER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SD_BUS_POWER	R/W	0h	<p>SD Bus Power for VDD1</p> <p>Before setting this bit, the SD host driver shall set SD Bus Voltage Select (MMCS0_POWER_CONTROL[3-1] SD_BUS_VOLTAGE). If the HC detects the No Card State, this bit shall be cleared.</p> <p>If this bit is cleared, the Host Controller should immediately stop driving CMD and DAT[3:0] (tri-state), and drive SDCLK to low level. If card is connected to Host Controller, Host Controller shall set these lines to low before stopping to supply VDD1.</p> <p>In UHS-II mode, before clearing this bit, Host Driver shall clear the MMCS0_CLOCK_CONTROL[2] SD_CLK_ENA bit and before stopping to supply VDD1, Host Controller shall set DAT[2] to low if DAT[2] is used as out-of band interrupt.</p> <p>1h: Power on 0h: Power off</p>

18.2.14 MMCSD0_BLOCK_GAP_CONTROL Register (Offset = 2Ah) [reset = 80h]

MMCSD0_BLOCK_GAP_CONTROL is shown in [Figure 18-43](#) and described in [Table 18-122](#).

Return to [Summary Table](#).

This register is used to program the block gap request, read wait control and interrupt at block gap.

**Table 18-121. MMCSD0_BLOCK_GAP_CONTROL
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 002Ah

Figure 18-43. MMCSD0_BLOCK_GAP_CONTROL Register

7	6	5	4	3	2	1	0
BOOT_ACK_ENA	ALT_BOOT_MODE	BOOT_ENABLE	RESERVED	INTRPT_AT_BLK_GAP	RDWAIT_CTRL	CONTINUE	STOP_AT_BLK_GAP
R/W-1h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-122. MMCSD0_BLOCK_GAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOT_ACK_ENA	R/W	1h	Boot Acknowledge Check To check for the boot acknowledge in boot operation. 1h: Wait for boot ack from eMMC card 0h: Will not wait for boot ack from eMMC card
6	ALT_BOOT_MODE	R/W	0h	Alternative Boot Mode To start boot code access in alternative mode. 1h: To start alternate boot mode access 0h: To stop alternate boot mode access
5	BOOT_ENABLE	R/W	0h	Boot Enable To start boot code access. 1h: To start boot code access 0h: To stop boot code access
4	RESERVED	R	0h	Reserved
3	INTRPT_AT_BLK_GAP	R/W	0h	Interrupt At Block Gap (SD Mode Only) This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1h enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0h. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card.

Table 18-122. MMCSDB_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RDWAIT_CTRL	R/W	0h	<p>Read Wait Control (SD Mode Only)</p> <p>The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1h otherwise DAT line conflict may occur. If this bit is set to 0h, Suspend/Resume cannot be supported.</p> <p>In UHS-II mode, Read Wait is disabled and DAT[2] line is used for Interrupt Signal from UHS-II Card.</p> <p>1h: Enable Read Wait Control 0h: Disable Read Wait Control</p>
1	CONTINUE	R/W	0h	<p>Continue Request</p> <p>This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0h (MMCSDB_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 0h) and set this bit to restart the transfer.</p> <p>The Host Controller automatically clears this bit when the transaction re-starts.</p> <p>If MMCSDB_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h, any write to this bit is ignored.</p> <p>In SD mode, this bit is cleared in either of the following cases:</p> <ol style="list-style-type: none"> 1) In the case of a read transaction, the DAT Line Active changes from 0h to 1h as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0h to 1h as the write transaction restarts. <p>Therefore it is not necessary for Host driver to set this bit to 0h. If MMCSDB_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h, any write to this bit is ignored.</p> <p>1h: Restart 0h: Ignored</p>

Table 18-122. MMCSD0_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	STOP_AT_BLK_GAP	R/W	0h	<p>Stop At Block Gap Request</p> <p>This bit is used to stop executing a transaction at the next block gap for non-DMA, SDMA and ADMA transfers. Until the transfer complete is set to 1h, indicating a transfer completion the HD shall leave this bit set to 1h.</p> <p>Clearing both the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP and MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bits shall not cause the transaction to restart. The MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit is used to stop the read transaction at the block gap. The HC shall honour Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1h (MMCSD0_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL) = 1h). In case of write transfers in which the HD writes data to the MMCSD0_DATA_PORT register, the HD shall set this bit after all block data is written. If this bit is set to 1h, the HD shall not write data to the MMCSD0_DATA_PORT register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit (DAT) in the MMCSD0_PRESENTSTATE register.</p> <p>In case of UHS-II, a transaction can be stopped at the boundary of DATA Burst (Flow Control basis). Host Controller waits for sending Flow Control MSG until the MMCSD0_BLOCK_GAP_CONTROL[1] CONTINUE bit is set to 1h.</p> <p>1h: Stop 0h: Transfer</p>

There are three cases to restart the transfer after stop at the block gap. Which case is appropriate depends on whether the HC issues a Suspend command or the SD card accepts the Suspend command.

1. If the HD does not issue Suspend command, the Continue Request shall be used to restart the transfer.
2. If the HD issues a Suspend command and the SD card accepts it, a Resume Command shall be used to restart the transfer.
3. If the HD issues a Suspend command and the SD card does not accept it, the Continue Request shall be used to restart the transfer.

Any time Stop At Block Gap Request stops the data transfer, the HD shall wait for Transfer Complete (in the MMCSD0_NORMAL_INTR_STS register) before attempting to restart the transfer. When restarting the data transfer by Continue Request, the HD shall clear Stop At Block Gap Request before or simultaneously.

Host Controller should not generate timeout interrupts while Stop At Block Gap is set. Host Driver should ignore timeout interrupts while Stop At Block Gap is set.

18.2.15 MMCS0_WAKEUP_CONTROL Register (Offset = 2Bh) [reset = 0h]

MMCS0_WAKEUP_CONTROL is shown in [Figure 18-44](#) and described in [Table 18-124](#).

Return to [Summary Table](#).

This register is used to program the wakeup functionality.

The MMCS0_WAKEUP_CONTROL register is mandatory for the HC, but wakeup functionality depends on the HC system hardware and software. The HD shall maintain voltage on the SD Bus, by setting the MMCS0_POWER_CONTROL[0] SD_BUS_POWER bit to 1h, when wakeup event via card interrupt is desired.

Table 18-123. MMCS0_WAKEUP_CONTROL Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 002Bh

Figure 18-44. MMCS0_WAKEUP_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED					CARD_REMOVAL	CARD_INSERTION	CARD_INTERRUPT
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-124. MMCS0_WAKEUP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	CARD_REMOVAL	R/W	0h	Wakeup Event Enable On SD Card Removal This bit enables wakeup event via Card removal assertion in the MMCS0_NORMAL_INTR_STS register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1h: Enable 0h: Disable
1	CARD_INSERTION	R/W	0h	Wakeup Event Enable On SD Card Insertion This bit enables wakeup event via Card Insertion assertion in the MMCS0_NORMAL_INTR_STS register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1h: Enable 0h: Disable
0	CARD_INTERRUPT	R/W	0h	Wakeup Event Enable On Card Interrupt This bit enables wakeup event via Card Interrupt assertion in the MMCS0_NORMAL_INTR_STS register. This bit can be set to 1h if FN_WUS (Wake Up Support) in CIS is set to 1h. 1h: Enable 0h: Disable

18.2.16 MMCSD0_CLOCK_CONTROL Register (Offset = 2Ch) [reset = 0h]

MMCSD0_CLOCK_CONTROL is shown in [Figure 18-45](#) and described in [Table 18-126](#).

Return to [Summary Table](#).

This register is used to program the Clock frequency select, Clock generator select, Clock enable, Internal clock state fields.

At the initialization of the HC, the HD shall set the SDCLK Frequency Select (MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL) according to the MMCSD0_CAPABILITIES register. This register controls SDCLK in SD Mode and RCLK in UHS-II mode.

**Table 18-125. MMCSD0_CLOCK_CONTROL
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 002Ch

Figure 18-45. MMCSD0_CLOCK_CONTROL Register

15	14	13	12	11	10	9	8
SDCLK_FRQSEL							
R/W-0h							
7	6	5	4	3	2	1	0
SDCLK_FRQSEL_UPBITS	CLKGEN_SEL	RESERVED	PLL_ENA	SD_CLK_ENA	INT_CLK_STABLE	INT_CLK_ENA	
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-126. MMCS0_CLOCK_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	SDCLK_FRQSEL	R/W	0h	<p>SDCLK/RCLK Frequency Select</p> <p>This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the Capabilities register (MMCS0_CAPABILITIES[15-8] BASE_CLK_FREQ).</p> <p>Only the following settings are allowed.</p> <p>(1) 8-bit Divided Clock Mode:</p> <p>80h: base clock divided by 256</p> <p>40h: base clock divided by 128</p> <p>20h: base clock divided by 64</p> <p>10h: base clock divided by 32</p> <p>08h: base clock divided by 16</p> <p>04h: base clock divided by 8</p> <p>02h: base clock divided by 4</p> <p>01h: base clock divided by 2</p> <p>00h: base clock (10 MHz - 63 MHz)</p> <p>Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The three default divider values can be calculated by the frequency that is defined by the MMCS0_CAPABILITIES[15-8] BASE_CLK_FREQ bit field.</p> <p>400 KHz divider value</p> <p>25 MHz divider value</p> <p>50 MHz divider value</p> <p>According to the Physical Layer Specification, the maximum SD Clock frequency is 25 MHz in normal speed mode and 50 MHz in high speed mode, and shall never exceed this limit.</p> <p>The frequency of SDCLK is set by the following formula:</p> <p>Clock Frequency = (Base Clock) / divisor</p> <p>Thus, choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency.</p> <p>For example, if the MMCS0_CAPABILITIES[15-8] BASE_CLK_FREQ bit field has the value 33 MHz, and the target frequency is 25 MHz, then choosing the divisor value of 1h will yield 16.5 MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400 KHz, the divisor value of 40h yields the optimal clock value of 258 KHz.</p> <p>(2) 10-bit Divided Clock Mode:</p> <p>Host Controller Version 3.00 or later supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits and all divider values shall be supported.</p> <p>3FFh: 1/2046 Divided Clock</p> <p>N: 1/2N Divided Clock (Duty 50%)</p> <p>002h: 1/4 Divided Clock</p> <p>001h: 1/2 Divided Clock</p> <p>000h: Base Clock (10 MHz - 254 MHz)</p> <p>(3) Programmable Clock Mode:</p>

Table 18-126. MMCSD0_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				<p>Host Controller Version 3.00 or later supports this mode as optional. A non-zero value set to the MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field indicates support of this clock mode. The multiplier enables the Host System to select a finer grain SD clock frequency. It is not necessary to support all frequency generation specified by this field because programmable clock generator is vendor specific and dependent on the implementation. Therefore, this mode is used with Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10). The Host Controller vendor provides possible settings and the Host System vendor sets appropriate values to the Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10).</p> <p>3FFh - Base Clock \times M / 1024</p> <p>.....</p> <p>N-1 - Base Clock \times M / N</p> <p>.....</p> <p>002h - Base Clock \times M / 3</p> <p>001h - Base Clock \times M / 2</p> <p>000h - Base Clock \times M</p> <p>This field depends on setting of the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this field is set by Host Driver. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this field is automatically set to a value specified in one of Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10).</p>
7-6	SDCLK_FRQSEL_UPBITS	R/W	0h	<p>Upper Bits of SDCLK/RCLK Frequency Select</p> <p>This bit field is assigned to the MMCSD0_CLOCK_CONTROL[9-8] SDCLK_FRQSEL bit field of clock divider in SDCLK/RCLK Frequency Select.</p>
5	CLKGEN_SEL	R/W	0h	<p>Clock Generator Select</p> <p>This bit is used to select the clock generator mode in SDCLK/RCLK Frequency Select (MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL).</p> <p>If the Programmable Clock Mode is supported (non-zero value is set to the MMCSD0_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field), this bit attribute is R/W, and if not supported, this bit attribute is RO and zero is read.</p> <p>This bit depends on the setting of the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this bit is set by Host Driver. If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this bit is automatically set to a value specified in one of Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10).</p> <p>1h: Programmable Clock Mode</p> <p>0h: Divided Clock Mode</p>

Table 18-126. MMCS0_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	R	0h	Reserved
3	PLL_ENA	R/W	0h	<p>PLL Enable</p> <p>This bit is added from Version 4.10 for Host Controller using PLL. This feature allows Host Controller to initialize clock generator in two steps: by Internal Clock Enable (MMCS0_CLOCK_CONTROL[0] INT_CLK_ENA) and PLL Enable and to minimize output latency (for example SDCLK/RCLK, D0 lane) from SD Clock Enable (MMCS0_CLOCK_CONTROL[2] SD_CLK_ENA). There are two modes to keep Host Drivers compatibility. In both modes, PLL Locked timing is indicated by Internal Clock Stable (MMCS0_CLOCK_CONTROL[1] INT_CLK_STABLE).</p> <p>(1) When MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h (Host Driver Version 3, which does not support this bit) or this bit is not implemented, the MMCS0_CLOCK_CONTROL[0] INT_CLK_ENA bit (or the MMCS0_CLOCK_CONTROL[2] SD_CLK_ENA bit) may activate PLL (exit low power mode and start locking clock).</p> <p>(2) When MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h (Host Driver Version 4), the MMCS0_CLOCK_CONTROL[0] INT_CLK_ENA bit is set before setting this bit and then setting this bit may activate PLL (exit low power mode and start locking clock).</p> <p>1h: PLL is enabled 0h: PLL is in low power mode</p>
2	SD_CLK_ENA	R/W	0h	<p>SD Clock Enable</p> <p>The HC shall stop SDCLK when writing this bit to 0h. The MMCS0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field can be changed when this bit is 0h. Then, the HC shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK = 0). If the HC detects the No Card state, this bit shall be cleared.</p> <p>1h: Enable providing SDCLK or RCLK 0h: Disable providing SDCLK or RCLK</p>
1	INT_CLK_STABLE	R	0h	<p>Internal Clock Stable</p> <p>This bit is set to 1h when SD clock is stable after writing 1h to MMCS0_CLOCK_CONTROL[0] INT_CLK_ENA bit. The SD Host Driver shall wait to set the MMCS0_CLOCK_CONTROL[2] SD_CLK_ENA bit until this bit is set to 1h.</p> <p>Note: This is useful when using PLL for a clock oscillator that requires setup time.</p> <p>(1) Internal Clock Stable (when MMCS0_CLOCK_CONTROL[3] PLL_ENA = 0h or not supported)</p> <p>This bit is set to 1h when internal clock is stable after writing 1h to MMCS0_CLOCK_CONTROL[0] INT_CLK_ENA bit.</p> <p>(2) PLL Clock Stable (when MMCS0_CLOCK_CONTROL[3] PLL_ENA = 1h)</p> <p>Host Controller which supports PLL Enable sets this status to 0h once when PLL Enable is changed 0h to 1h and then this status is set to 1h when PLL is locked (PLL uses an internal clock in stable as a reference clock which is enabled by the MMCS0_CLOCK_CONTROL[0] INT_CLK_ENA bit). After this bit is set to 1h, Host Driver may set the MMCS0_CLOCK_CONTROL[2] SD_CLK_ENA bit.</p> <p>1h: Ready 0h: Not Ready</p>

Table 18-126. MMCSD0_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT_CLK_ENA	R/W	0h	<p>Internal Clock Enable</p> <p>This bit is set to 0h when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1h. When clock oscillation is stable, the HC shall set the MMCSD0_CLOCK_CONTROL[1] INT_CLK_STABLE bit to 1h. This bit shall not affect card detection.</p> <p>1h: Oscillate 0h: Stop</p>

18.2.17 MMCS0_TIMEOUT_CONTROL Register (Offset = 2Eh) [reset = 0h]

MMCS0_TIMEOUT_CONTROL is shown in [Figure 18-46](#) and described in [Table 18-128](#).

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The register sets the data timeout counter value.

At the initialization of the HC, the HD shall set the Data Timeout Counter Value according to the MMCS0_CAPABILITIES register.

**Table 18-127. MMCS0_TIMEOUT_CONTROL
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 002Eh

Figure 18-46. MMCS0_TIMEOUT_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED				COUNTER_VALUE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-128. MMCS0_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	COUNTER_VALUE	R/W	0h	<p>Data Timeout Counter Value</p> <p>This value determines the interval by which DAT line time-outs are detected. Refer to the MMCS0_ERROR_INTR_STS[4] DATA_TIMEOUT bit for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the SD clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the MMCS0_ERROR_INTR_STS[4] DATA_TIMEOUT bit.</p> <p>1111: Reserved</p> <p>1110: $TMCLK \times 2^{27}$</p> <p>-----</p> <p>-----</p> <p>0001: $TMCLK \times 2^{14}$</p> <p>0000: $TMCLK \times 2^{13}$</p>

18.2.18 MMCSD0_SOFTWARE_RESET Register (Offset = 2Fh) [reset = 0h]

MMCSD0_SOFTWARE_RESET is shown in [Figure 18-47](#) and described in [Table 18-130](#).

Return to [Summary Table](#).

This register is used to program the software reset for data, command and for all.

A reset pulse is generated when writing 1h to each bit of this register. After completing the reset, the HC shall clear each bit. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0h.

**Table 18-129. MMCSD0_SOFTWARE_RESET
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 002Fh

Figure 18-47. MMCSD0_SOFTWARE_RESET Register

7	6	5	4	3	2	1	0
RESERVED					SWRST_FOR_DAT	SWRST_FOR_CMD	SWRST_FOR_ALL
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-130. MMCSD0_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	SWRST_FOR_DAT	R/W	0h	<p>Software Reset for DAT Line (SD Mode Only)</p> <p>Only part of data circuit is reset. The following registers and bits are cleared by this bit:</p> <p>MMCSD0_DATA_PORT register:</p> <p>Buffer is cleared and Initialized.</p> <p>MMCSD0_PRESENTSTATE register:</p> <p>Buffer read Enable</p> <p>Buffer write Enable</p> <p>Read Transfer Active</p> <p>Write Transfer Active</p> <p>DAT Line Active</p> <p>Command Inhibit (DAT)</p> <p>MMCSD0_BLOCK_GAP_CONTROL register:</p> <p>Continue Request</p> <p>Stop At Block Gap Request</p> <p>MMCSD0_NORMAL_INTR_ST register:</p> <p>Buffer Read Ready</p> <p>Buffer Write Ready</p> <p>Block Gap Event</p> <p>Transfer Complete</p> <p>1h: Reset</p> <p>0h: Work</p>

Table 18-130. MMCS0_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SWRST_FOR_CMD	R/W	0h	<p>Software Reset for CMD Line (SD Mode Only)</p> <p>Only part of command circuit is reset to be able to issue a command. From Version 4.10, this bit is also used to initialize UHS-II command circuit. This reset is effective only command issuing circuit (including response error statuses related to Command Inhibit (CMD) control - MMCS0_PRESENTSTATE[0] INHIBIT_CMD bit) and does not affect data transfer circuit. Host Controller can continue data transfer even this reset is executed during handling of sub command response errors.</p> <p>The following registers and bits are cleared by this bit:</p> <p>MMCS0_PRESENTSTATE register:</p> <p>Command Inhibit (CMD)</p> <p>MMCS0_NORMAL_INTR_ST register:</p> <p>Command Complete</p> <p>MMCS0_ERROR_INTR_STS register (Error Interrupt Status from Version 4.10)</p> <p>Response error statuses related to Command Inhibit (CMD) - MMCS0_PRESENTSTATE[0] INHIBIT_CMD bit</p> <p>1h: Reset</p> <p>0h: Work</p>
0	SWRST_FOR_ALL	R/W	0h	<p>Software Reset for All</p> <p>This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0h. During its initialization, the HD shall set this bit to 1h to reset the HC. The HC shall reset this bit to 0h when Capabilities registers are valid and the HD can read them. Additional use of 'Software Reset For All' may not affect the value of the Capabilities registers. If this bit is set to 1h, the SD card shall reset itself and must be re-initialized by the HD.</p> <p>1h: Reset</p> <p>0h: Work</p>

18.2.19 MMCSD0_NORMAL_INTR_STS Register (Offset = 30h) [reset = 0h]

MMCSD0_NORMAL_INTR_STS is shown in [Figure 18-48](#) and described in [Table 18-132](#).

Return to [Summary Table](#).

This register gives the status of all the interrupts.

The Normal Interrupt Signal Enable (see MMCSD0_NORMAL_INTR_SIG_ENA register) affects read of this register, but Normal Interrupt Signal does not affect these reads. An Interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1h. For all bits except Card Interrupt (MMCSD0_NORMAL_INTR_STS[8] CARD_INTR) and Error Interrupt (MMCSD0_NORMAL_INTR_STS[15] ERROR_INTR), writing 1h to a bit clears it. The MMCSD0_NORMAL_INTR_STS[8] CARD_INTR bit is cleared when the card stops asserting the interrupt: that is when the Card Driver services the Interrupt condition.

Table 18-131. MMCSD0_NORMAL_INTR_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0030h

Figure 18-48. MMCSD0_NORMAL_INTR_STS Register

15	14	13	12	11	10	9	8
ERROR_INTR	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTR
R-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CARD_REM	CARD_INS	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-132. MMCSD0_NORMAL_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ERROR_INTR	R	0h	Error Interrupt If any of the bits in the MMCSD0_ERROR_INTR_STS register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. In UHS-II mode is enabled, if any of the bits in the MMCSD0_UHS2_ERR_INTR_STS register are set, this bit is also set. 0h: No Error 1h: Error
14	BOOT_COMPLETE	R/W1C	0h	Boot Terminate Interrupt This status is set if the boot operation gets terminated. 0h: Boot operation is not terminated 1h: Boot operation is terminated
13	RCV_BOOT_ACK	R/W1C	0h	Boot Acknowledge Receive This status is set if the boot acknowledge is received from device. 0h: Boot acknowledge is not received 1h: Boot acknowledge is received

Table 18-132. MMCS0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RETUNING_EVENT	R	0h	<p>Re-Tuning Event (UHS-I Only)</p> <p>This status is set if the MMCS0_PRESENTSTATE[3] RETUNING_REQ bit changes from 0h to 1h.</p> <p>Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning.</p> <p>In UHS-II mode, this bit is not effective.</p> <p>1h: Re-Tuning should be performed</p> <p>0h: Re-Tuning is not required</p>
11	INTC	R	0h	<p>int_c (Embedded)</p> <p>This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_C interrupt factor.</p>
10	INTB	R	0h	<p>int_b (Embedded)</p> <p>This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_B interrupt factor.</p>
9	INTA	R	0h	<p>int_a (Embedded)</p> <p>This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_A interrupt factor.</p>

Table 18-132. MMCSD0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CARD_INTR	R	0h	<p>Card Interrupt</p> <p>When this status has been set and the Host Driver needs to start this interrupt service, the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit may be set to 0h in order to clear the card interrupt status latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (it should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 1h and start sampling the interrupt signal again.</p> <p>Writing this bit to 1h does not clear this bit. It is cleared by resetting the SD card interrupt factor.</p> <p>(1) DAT[1] Interrupt Input in SD Mode</p> <p>In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of UHS-I mode, switching time of Interrupt Period is relaxed for 2 clock cycles. Then Host Controller needs to delay start of interrupt sampling at least 2 clocks and should sample interrupt while Interrupt Period is stable.</p> <p>(2) DAT[2] Interrupt Input in UHS-II Mode</p> <p>When the MMCSD0_PRESENTSTATE[16] CARD_INSERTED and MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bits are set to 1h, Host Controller configures DAT[2] as Interrupt Input and enables pull-up of DAT[2]. DAT[2] interrupt is asynchronous to RCLK, low level sensitive and 3.3 V signal level. DAT[2] interrupt is masked by setting the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 0h. When either the MMCSD0_PRESENTSTATE[16] CARD_INSERTED bit or the MMCSD0_POWER_CONTROL[0] SD_BUS_POWER bit is set to 0h, Host Controller sets DAT[2] to low. Only point to point connection is allowed between Host and Card.</p> <p>(3) INT MSG in UHS-II Mode</p> <p>INT MSG is enabled by setting the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit. DAT[2] and INT MSG interrupt sources are ORed and indicated to Card Interrupt. If any bit in the MMCSD0_UHS2_DEVICE_INTR_STATUS register is set to 1h, INT MSG interrupt is generated. INT MSG interrupt is cleared by writing a correspondent bit to 1h in the MMCSD0_UHS2_DEVICE_INTR_STATUS register. Masking DAT[2] interrupt also disables INT MSG interrupt due to the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit is set to 0h. SDIO Version 4.00 does not support INT MSG.</p> <p>1h: Generate Card Interrupt 0h: No Card Interrupt</p>

Table 18-132. MMCSDB0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CARD_REM	R/W1C	0h	<p>Card Removal</p> <p>This status is set if the MMCSDB0_PRESENTSTATE[16] CARD_INSERTED bit changes from 1h to 0h. When the HD writes this bit to 1h to clear this status the status of the MMCSDB0_PRESENTSTATE[16] CARD_INSERTED bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated.</p> <p>0h: Card State Stable or Debouncing 1h: Card Removed</p>
6	CARD_INS	R/W1C	0h	<p>Card Insertion</p> <p>This status is set if the MMCSDB0_PRESENTSTATE[16] CARD_INSERTED bit changes from 0h to 1h. When the HD writes this bit to 1h to clear this status the status of the MMCSDB0_PRESENTSTATE[16] CARD_INSERTED bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated.</p> <p>0h: Card State Stable or Debouncing 1h: Card Inserted</p>
5	BUF_RD_READY	R/W1C	0h	<p>Buffer Read Ready</p> <p>This status is set if the MMCSDB0_PRESENTSTATE[11] BUF_RD_ENA bit changes from 0h to 1h.</p> <p>The MMCSDB0_PRESENTSTATE[11] BUF_RD_ENA bit is set to 1h for every CMD19 execution in tuning procedure.</p> <p>In UHS-II mode, this bit is set at FC (Flow Control) unit basis.</p> <p>0h: Not Ready to read Buffer 1h: Ready to read Buffer</p>
4	BUF_WR_READY	R/W1C	0h	<p>Buffer Write Ready</p> <p>This status is set if the MMCSDB0_PRESENTSTATE[10] BUF_WR_ENA bit changes from 0h to 1h.</p> <p>In UHS-II mode, this bit is set at FC (Flow Control) unit basis.</p> <p>0h: Not Ready to Write Buffer 1h: Ready to Write Buffer</p>
3	DMA_INTERRUPT	R/W1C	0h	<p>DMA Interrupt</p> <p>This status is set if the HC detects the Host DMA Buffer Boundary in the MMCSDB0_BLOCK_SIZE register.</p> <p>0h: No DMA Interrupt 1h: DMA Interrupt is Generated</p>
2	BLK_GAP_EVENT	R/W1C	0h	<p>Block Gap Event</p> <p>If the MMCSDB0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set, this bit is set.</p> <p>Read Transaction:</p> <p>This bit is set at the falling edge of the DAT Line Active Status (see MMCSDB0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit). When the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function.</p> <p>Write Transaction:</p> <p>This bit is set at the falling edge of Write Transfer Active Status (see MMCSDB0_PRESENTSTATE[8] WR_XFER_ACTIVE bit). After getting CRC status at SD Bus timing. In UHS-II mode, this bit is set at FC (Flow Control) unit basis.</p> <p>0h: No Block Gap Event 1h: Transaction stopped at Block Gap</p>

Table 18-132. MMCSD0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XFER_COMPLETE	R/W1C	0h	<p>Transfer Complete</p> <p>This bit is set when a read/write transaction is completed.</p> <p>SD Mode</p> <p>Read Transaction:</p> <p>This bit is set at the falling edge of Read Transfer Active Status (MMCSD0_PRESENTSTATE[9] RD_XFER_ACTIVE).</p> <p>There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length (after the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit (after valid data has been read to the Host System).</p> <p>Write Transaction:</p> <p>This bit is set at the falling edge of the DAT Line Active Status (see MMCSD0_PRESENTSTATE[2] DATA_LINE_ACTIVE bit). There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and data transfers completed (after valid data is written to the SD card and the busy signal is released).</p> <p>Note: MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit has higher priority than the MMCSD0_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If both bits are set to 1h, the data transfer can be considered complete.</p> <p>Note: While performing tuning procedure (the MMCSD0_HOST_CONTROL2[6] EXECUTE_TUNING bit is set to 1h), the MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is not set to 1h.</p> <p>Command with Busy:</p> <p>This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit (DAT) in the MMCSD0_PRESENTSTATE register.</p> <p>UHS-I mode</p> <p>While performing tuning procedure (the MMCSD0_HOST_CONTROL2[6] EXECUTE_TUNING bit is set to 1h), the MMCSD0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is not set to 1h.</p> <p>0h: No Data Transfer Complete 1h: Data Transfer Complete</p> <p>UHS-II Mode</p> <p>This interrupt is generated in following two cases:</p> <p>(a) EBSY Completion (for EBSY supported commands) When the MMCSD0_UHS2_XFER_MODE[14] EBSY_WAIT bit is set to 1h, this bit is set when EBSY packet has been received, and all valid data have been sent to system memory in case of read operation.</p> <p>(b) Stop and Continue during DCMD Data Transfer When the MMCSD0_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1h and data transfer is stopped at the Flow Control.</p> <p>Following is for both SD mode and UHS-II mode.</p>

Table 18-132. MMCS0_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				<p>The table below shows that the MMCS0_NORMAL_INTR_STS[1] XFER_COMPLETE bit has higher priority than the MMCS0_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If both bits are set to 1h, execution of a command can be considered to be completed.</p> <p>1h: Command execution is completed 0h: Not complete</p>
0	CMD_COMPLETE	R/W1C	0h	<p>Command Complete</p> <p>SD Mode</p> <p>This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23).</p> <p>Note: The MMCS0_ERROR_INTR_STS[0] CMD_TIMEOUT bit has higher priority than the MMCS0_NORMAL_INTR_STS[0] CMD_COMPLETE bit. If both are set to 1h, it can be considered that the response was not received correctly.</p> <p>Version 4.00 defines response check function for R1 and R5. If the MMCS0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1h, generation of this interrupt is prohibited regardless of the MMCS0_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit.</p> <p>UHS-II Mode</p> <p>If the MMCS0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 0h, this interrupt is generated when response packet is received.</p> <p>If the MMCS0_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1h, generation of this interrupt is prohibited regardless of the MMCS0_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit.</p> <p>0h: No Command Complete 1h: Command Complete</p>

Table 18-133 shows the relation between transfer complete and data timeout error.

Table 18-133. Relation between transfer complete and data timeout error

Transfer Complete	Data Timeout Error	Meaning of the Status
0	0	Interrupted by Another Factor
0	1	Timeout occur during transfer
1	Don't Care	Data Transfer Complete

Table 18-134 shows the relation between command complete and command timeout error.

Table 18-134. Relation between command complete and command timeout error

Command Complete	Command Timeout Error	Meaning of the Status
0	0	Interrupted by Another Factor
Don't Care	1	Response not received within 64 SDCLK cycles
1	0	Response Received

18.2.20 MMCSD0_ERROR_INTR_STS Register (Offset = 32h) [reset = 0h]

MMCSD0_ERROR_INTR_STS is shown in [Figure 18-49](#) and described in [Table 18-136](#).

Return to [Summary Table](#).

This register gives the status of the error interrupts.

Status defined in this register can be enabled by the MMCSD0_ERROR_INTR_STS_ENA register, but not by the MMCSD0_ERROR_INTR_SIG_ENA register. The Interrupt is generated when the MMCSD0_ERROR_INTR_SIG_ENA register is enabled and at least one of the statuses is set to 1h. Writing to 1h clears the bit and writing to 0h keeps the bit unchanged. More than one status can be cleared at the one register write.

**Table 18-135. MMCSD0_ERROR_INTR_STS
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0032h

Figure 18-49. MMCSD0_ERROR_INTR_STS Register

15	14	13	12	11	10	9	8
RESERVED			HOST	RESP	RESERVED	ADMA	AUTO_CMD
R-0h			R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-136. MMCSD0_ERROR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	HOST	R/W1C	0h	Target Response Error Occurs when detecting ERROR in m_hresp (DMA transaction) 0h: No error 1h: Error
11	RESP	R/W1C	0h	Response Error (SD Mode Only) Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If the MMCSD0_TRANSFER_MODE[7] RESP_ERR_CHK_ENA bit is set to 1h, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1h. 0h: No error 1h: Error
10	RESERVED	R	0h	Reserved
9	ADMA	R/W1C	0h	ADMA Error This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the MMCSD0_ADMA_ERR_STATUS register. 0h: No error 1h: Error

Table 18-136. MMCS0_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	AUTO_CMD	R/W1C	0h	<p>Auto CMD Error (SD Mode Only)</p> <p>Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that any of the bits D00 to D05 in the MMCS0_AUTOCMD_ERR_STS register has changed from 0h to 1h. D07 is effective in case of Auto CMD12. The MMCS0_AUTOCMD_ERR_STS register is valid while this bit is set to 1h and may be cleared with clearing of this bit (another implementation is also allowed).</p> <p>0h: No error 1h: Error</p>
7	CURR_LIMIT	R/W1C	0h	<p>Current Limit Error</p> <p>By setting the MMCS0_POWER_CONTROL[0] SD_BUS_POWER bit, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1h means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function.</p> <p>0h: No error 1h: Power Fail</p>
6	DATA_ENDBIT	R/W1C	0h	<p>Data End Bit Error (SD Mode Only)</p> <p>Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.</p> <p>0h: No error 1h: Error</p>
5	DATA_CRC	R/W1C	0h	<p>Data CRC Error (SD Mode Only)</p> <p>Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 2h.</p> <p>0h: No error 1h: Error</p>
4	DATA_TIMEOUT	R/W1C	0h	<p>Data Timeout Error (SD Mode Only)</p> <p>Occurs when detecting one of following timeout conditions:</p> <ol style="list-style-type: none"> 1. Busy Timeout for R1b, R5b type 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout <p>0h: No error 1h: Timeout</p>
3	CMD_INDEX	R/W1C	0h	<p>Command Index Error (SD Mode Only)</p> <p>Occurs if a Command Index error occurs in the Command Response (MMCS0_RESPONSE_0 to MMCS0_RESPONSE_7).</p> <p>0h: No error 1h: Error</p>
2	CMD_ENDBIT	R/W1C	0h	<p>Command End Bit Error (SD Mode Only)</p> <p>Occurs when detecting that the end bit of a command response is 0h.</p> <p>0h: No error 1h: End Bit Error Generated</p>

Table 18-136. MMCSD0_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CMD_CRC	R/W1C	0h	<p>Command CRC Error (SD Mode Only)</p> <p>Command CRC Error is generated in two cases.</p> <p>1. If a response is returned and the MMCSD0_ERROR_INTR_STS[0] CMD_TIMEOUT bit is set to 0h, this bit is set to 1h when detecting a CRT error in the command response.</p> <p>2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (Stop driving CMD line) and set this bit to 1h. The MMCSD0_ERROR_INTR_STS[0] CMD_TIMEOUT bit shall also be set to 1h to distinguish CMD line conflict.</p> <p>0h: No error 1h: CRC Error Generated</p>
0	CMD_TIMEOUT	R/W1C	0h	<p>Command Timeout Error (SD Mode Only)</p> <p>Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case the MMCSD0_ERROR_INTR_STS[1] CMD_CRC bit shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC.</p> <p>0h: No error 1h: Timeout</p>

Table 18-137 shows the relation between command CRC error and command time-out error.

Table 18-137. Relation between command CRC error and command time-out error

Command CRC Error	Command Time-out Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD Line Conflict

18.2.21 MMCS0_NORMAL_INTR_STS_ENA Register (Offset = 34h) [reset = 0h]

MMCS0_NORMAL_INTR_STS_ENA is shown in [Figure 18-50](#) and described in [Table 18-139](#).

Return to [Summary Table](#).

This register is used to enable the MMCS0_NORMAL_INTR_STS register fields.

Table 18-138. MMCS0_NORMAL_INTR_STS_ENA Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0034h

Figure 18-50. MMCS0_NORMAL_INTR_STS_ENA Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CARD_REMOVE	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-139. MMCS0_NORMAL_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	Fixed to 0 The HC shall control error Interrupts using the MMCS0_ERROR_INTR_STS_ENA register.
14	BOOT_COMPLETE	R/W	0h	Boot Terminate Interrupt Enable 0h: Masked 1h: Enabled
13	RCV_BOOT_ACK	R/W	0h	Boot Acknowledge Enable 0h: Masked 1h: Enabled
12	RETUNING_EVENT	R/W	0h	Re-Tuning Event Status Enable (UHS-I Only) 0h: Masked 1h: Enabled
11	INTC	R/W	0h	INT_C Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts.
10	INTB	R/W	0h	INT_B Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts.
9	INTA	R/W	0h	INT_A Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts.

Table 18-139. MMCSD0_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CARD_INTERRUPT	R/W	0h	<p>Card Interrupt Status Enable</p> <p>If this bit is set to 0h, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1h. The HD may clear the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts.</p> <p>By setting this bit to 0h, interrupt input should be masked by implementation so that the interrupt Input is not affected by external signal in any state (for example: floating).</p> <p>0h: Masked 1h: Enabled</p>
7	CARD_REMOVAL	R/W	0h	<p>Card Removal Status Enable</p> <p>0h: Masked 1h: Enabled</p>
6	CARD_INSERTION	R/W	0h	<p>Card Insertion Status Enable</p> <p>0h: Masked 1h: Enabled</p>
5	BUF_RD_READY	R/W	0h	<p>Buffer Read Ready Status Enable</p> <p>0h: Masked 1h: Enabled</p>
4	BUF_WR_READY	R/W	0h	<p>Buffer Write Ready Status Enable</p> <p>0h: Masked 1h: Enabled</p>
3	DMA_INTERRUPT	R/W	0h	<p>DMA Interrupt Status Enable</p> <p>0h: Masked 1h: Enabled</p>
2	BLK_GAP_EVENT	R/W	0h	<p>Block Gap Event Status Enable</p> <p>0h: Masked 1h: Enabled</p>
1	XFER_COMPLETE	R/W	0h	<p>Transfer Complete Status Enable</p> <p>0h: Masked 1h: Enabled</p>
0	CMD_COMPLETE	R/W	0h	<p>Command Complete Status Enable</p> <p>0h: Masked 1h: Enabled</p>

Note: The HC may sample the card Interrupt signal during interrupt period and may hold its value in the flip-flop. If the MMCSD0_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit is set to 0h, the HC shall clear all internal signals regarding Card Interrupt (MMCSD0_NORMAL_INTR_STS[8] CARD_INTR).

18.2.22 MMCS0_ERROR_INTR_STS_ENA Register (Offset = 36h) [reset = 0h]

MMCS0_ERROR_INTR_STS_ENA is shown in [Figure 18-51](#) and described in [Table 18-141](#).

Return to [Summary Table](#).

This register is used to enable the MMCS0_ERROR_INTR_STS register fields.

Table 18-140. MMCS0_ERROR_INTR_STS_ENA Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0036h

Figure 18-51. MMCS0_ERROR_INTR_STS_ENA Register

15	14	13	12	11	10	9	8
VENDOR_SPECIFIC				RESP	TUNING	ADMA	AUTO_CMD
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-141. MMCS0_ERROR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Status Enable N/A
11	RESP	R/W	0h	Response Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
10	TUNING	R/W	0h	Tuning Error Status Enable (UHS-I Only) 0h: Masked 1h: Enabled
9	ADMA	R/W	0h	ADMA Error Status Enable 0h: Masked 1h: Enabled
8	AUTO_CMD	R/W	0h	Auto CMD Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
7	CURR_LIMIT	R/W	0h	Current Limit Error Status Enable 0h: Masked 1h: Enabled
6	DATA_ENDBIT	R/W	0h	Data End Bit Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
5	DATA_CRC	R/W	0h	Data CRC Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
4	DATA_TIMEOUT	R/W	0h	Data Timeout Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled

Table 18-141. MMCSD0_ERROR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMD_INDEX	R/W	0h	Command Index Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
2	CMD_ENDBIT	R/W	0h	Command End Bit Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
1	CMD_CRC	R/W	0h	Command CRC Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
0	CMD_TIMEOUT	R/W	0h	Command Timeout Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled

Note: To Detect CMD Line conflict, the HD must set both MMCSD0_ERROR_INTR_STS_ENA[0] CMD_TIMEOUT and MMCSD0_ERROR_INTR_STS_ENA[1] CMD_CRC bits to 1h.

18.2.23 MMCS0_NORMAL_INTR_SIG_ENA Register (Offset = 38h) [reset = 0h]

MMCS0_NORMAL_INTR_SIG_ENA is shown in [Figure 18-52](#) and described in [Table 18-143](#).

Return to [Summary Table](#).

Normal Interrupt Signal Enable Register

This register is used to select which interrupt status is indicated to the Host System as the Interrupt. These status bits all share the sample 1 bit interrupt line. Setting any of these bits to 1h enables Interrupt generation.

Table 18-142. MMCS0_NORMAL_INTR_SIG_ENA Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0038h

Figure 18-52. MMCS0_NORMAL_INTR_SIG_ENA Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CARD_REMOVE	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-143. MMCS0_NORMAL_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	Fixed to 0 The HD shall control error Interrupts using the MMCS0_ERROR_INTR_SIG_ENA register.
14	BOOT_COMPLETE	R/W	0h	Boot Terminate Interrupt Signal Enable 0h: Masked 1h: Enabled
13	RCV_BOOT_ACK	R/W	0h	Boot Acknowledge Receive Signal Enable 0h: Masked 1h: Enabled
12	RETUNING_EVENT	R/W	0h	Re-Tuning Event Signal Enable (UHS-I Only) 0h: Masked 1h: Enabled
11	INTC	R/W	0h	INT_C Signal Enable (Embedded) 0h: Masked 1h: Enabled
10	INTB	R/W	0h	INT_B Signal Enable (Embedded) 0h: Masked 1h: Enabled
9	INTA	R/W	0h	INT_A Signal Enable (Embedded) 0h: Masked 1h: Enabled
8	CARD_INTERRUPT	R/W	0h	Card Interrupt Signal Enable 0h: Masked 1h: Enabled

Table 18-143. MMCSD0_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CARD_REMOVAL	R/W	0h	Card Removal Signal Enable 0h: Masked 1h: Enabled
6	CARD_INSERTION	R/W	0h	Card Insertion Signal Enable 0h: Masked 1h: Enabled
5	BUF_RD_READY	R/W	0h	Buffer Read Ready Signal Enable 0h: Masked 1h: Enabled
4	BUF_WR_READY	R/W	0h	Buffer Write Ready Signal Enable 0h: Masked 1h: Enabled
3	DMA_INTERRUPT	R/W	0h	DMA Interrupt Signal Enable 0h: Masked 1h: Enabled
2	BLK_GAP_EVENT	R/W	0h	Block Gap Event Signal Enable 0h: Masked 1h: Enabled
1	XFER_COMPLETE	R/W	0h	Transfer Complete Signal Enable 0h: Masked 1h: Enabled
0	CMD_COMPLETE	R/W	0h	Command Complete Signal Enable 0h: Masked 1h: Enabled

18.2.24 MMCSDB0_ERROR_INTR_SIG_ENA Register (Offset = 3Ah) [reset = 0h]

MMCSDB0_ERROR_INTR_SIG_ENA is shown in [Figure 18-53](#) and described in [Table 18-145](#).

Return to [Summary Table](#).

Error Interrupt Signal Enable Register

This register is used to select which interrupt status is notified to the Host System as the Interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1h enables Interrupt generation.

Table 18-144. MMCSDB0_ERROR_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSDB0_CTL_CFG	04F8 003Ah

Figure 18-53. MMCSDB0_ERROR_INTR_SIG_ENA Register

15	14	13	12	11	10	9	8
VENDOR_SPECIFIC				RESP	TUNING	ADMA	AUTO_CMD
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-145. MMCSDB0_ERROR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Signal Enable N/A
11	RESP	R/W	0h	Response Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
10	TUNING	R/W	0h	Tuning Error Signal Enable (UHS-I Only) 0h: Masked 1h: Enabled
9	ADMA	R/W	0h	ADMA Error Signal Enable 0h: Masked 1h: Enabled
8	AUTO_CMD	R/W	0h	Auto CMD Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
7	CURR_LIMIT	R/W	0h	Current Limit Error Signal Enable 0h: Masked 1h: Enabled
6	DATA_ENDBIT	R/W	0h	Data End Bit Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
5	DATA_CRC	R/W	0h	Data CRC Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled

Table 18-145. MMCSD0_ERROR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DATA_TIMEOUT	R/W	0h	Data Timeout Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
3	CMD_INDEX	R/W	0h	Command Index Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
2	CMD_ENDBIT	R/W	0h	Command End Bit Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
1	CMD_CRC	R/W	0h	Command CRC Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
0	CMD_TIMEOUT	R/W	0h	Command Timeout Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled

18.2.25 MMCS0_AUTOCMD_ERR_STS Register (Offset = 3Ch) [reset = 0h]

MMCS0_AUTOCMD_ERR_STS is shown in [Figure 18-54](#) and described in [Table 18-147](#).

Return to [Summary Table](#).

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD23.

The Host driver can determine what kind of Auto CMD12/CMD23 errors occur by this register. Auto CMD23 errors are indicated in bit 04-01. This register is valid only when the Auto CMD Error is set.

**Table 18-146. MMCS0_AUTOCMD_ERR_STS
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 003Ch

Figure 18-54. MMCS0_AUTOCMD_ERR_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMD_NOT_ISSUED	RESERVED		INDEX	ENDBIT	CRC	TIMEOUT	ACMD12_NOT_EXEC
R-0h	R-0h		R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 18-147. MMCS0_AUTOCMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMD_NOT_ISSUED	R	0h	Command Not Issued By Auto CMD12 Error Setting this bit to 1h means CMD_wo_DAT is not executed due to an Auto CMD12 error (D04- D01) in this register. This bit is set to 0h when Auto CMD Error is generated by Auto CMD23. 0h: No Error 1h: Not Issued
6-5	RESERVED	R	0h	Reserved
4	INDEX	R	0h	Auto CMD Index Error Occurs if the Command Index error occurs in response to a command. 0h: No Error 1h: Error
3	ENDBIT	R	0h	Auto CMD End Bit Error Occurs when detecting that the end bit of command response is 0h. 0h: No Error 1h: End Bit Error Generated
2	CRC	R	0h	Auto CMD CRC Error Occurs when detecting a CRC error in the command response. 0h: No Error 1h: CRC Error Generated

Table 18-147. MMCSD0_AUTOCMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TIMEOUT	R	0h	Auto CMD Timeout Error Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1h, the other error status bits (D04 - D02) are meaningless. 0h: No Error 1h: Timeout
0	ACMD12_NOT_EXEC	R	0h	Auto CMD12 not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1h means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1h, other error status bits (D04 - D01) are meaningless. This bit is set to 0h when Auto CMD Error is generated by Auto CMD23. 0h: Executed 1h: Not Executed

Table 18-148 shows the relation between Auto CMD12 CRC error and Auto CMD12 timeout error.

Table 18-148. Relation between Auto CMD12 CRC Error and Auto CMD12 Timeout Error

Auto Cmd12 CRC Error	Auto CMD12 Timeout Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD Line Conflict

The timing of changing Auto CMD12 Error Status can be classified in three scenarios:

1. When the HC is going to issue Auto CMD12:

Set D00 to 1h if Auto CMD12 cannot be issued due to an error in the previous command.

Set D00 to 0h if Auto CMD12 is issued.

2. At the end bit of Auto CMD12 response:

Check received responses by checking the error bits D01, D02, D03, D04.

set to 1h if Error is Detected.

set to 0h if Error is Not Detected.

3. Before reading the Auto CMD12 Error Status bit D07:

Set D07 to 1h if there is a command cannot be issued.

Set D07 to 0h if there is no command to issue.

Timing of generating the Auto CMD12 Error and writing to the MMCSD0_COMMAND register are Asynchronous. Then D07 shall be sampled when driver never writing to the MMCSD0_COMMAND register. So just before reading the MMCSD0_AUTOCMD_ERR_STS register is good timing to set the D07 status bit.

18.2.26 MMCS0_HOST_CONTROL2 Register (Offset = 3Eh) [reset = 0h]

MMCS0_HOST_CONTROL2 is shown in [Figure 18-55](#) and described in [Table 18-150](#).

Return to [Summary Table](#).

This register is used to program UHS Mode Select, Driver Strength Select, Execute Tuning, Sampling Clock Select, Asynchronous Interrupt Enable and Preset Value Enable.

**Table 18-149. MMCS0_HOST_CONTROL2
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 003Eh

Figure 18-55. MMCS0_HOST_CONTROL2 Register

15	14	13	12	11	10	9	8
PRESET_VALUE_ENA	ASYNCH_INTR_ENA	BIT64_ADDRESSING	HOST_VER40_ENA	CMD23_ENA	ADMA2_LEN_MODE	DRIVER_STRENGTH2	UHS2_INTF_ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SAMPLING_CLOCK_SELECT	EXECUTE_TUNING	DRIVER_STRENGTH1	V1P8_SIGNAL_ENA	UHS_MODE_SELECT			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-150. MMCS0_HOST_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PRESET_VALUE_ENA	R/W	0h	<p>Preset Value Enable</p> <p>Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When the MMCS0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to automatic. This bit enables the functions defined in the Preset Value registers (MMCS0_PRESET_VALUE0 - MMCS0_PRESET_VALUE10).</p> <p>If this bit is set to 0h, SDCLK Frequency Select, Clock Generator Select in the MMCS0_CLOCK_CONTROL register and Driver Strength Select in the MMCS0_HOST_CONTROL2 register are set by Host Driver.</p> <p>If this bit is set to 1h, SDCLK Frequency Select, Clock Generator Select in the MMCS0_CLOCK_CONTROL register and Driver Strength Select in the MMCS0_HOST_CONTROL2 register are set by Host Controller as specified in the Preset Value registers (MMCS0_PRESET_VALUE0 - MMCS0_PRESET_VALUE10).</p> <p>0h: SDCLK and Driver Strength are controlled by Host Driver</p> <p>1h: Automatic Selection by Preset Value are Enabled</p>

Table 18-150. MMCSD0_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ASYNCH_INTR_ENA	R/W	0h	<p>Asynchronous Interrupt Enable</p> <p>This bit can be set to 1h if a card support asynchronous interrupt and the MMCSD0_CAPABILITIES[29] ASYNCH_INTR_SUPPORT bit is set to 1h. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode . If this bit is set to 1h, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card.</p> <p>0h: Disabled 1h: Enabled</p>
13	BIT64_ADDRESSING	R/W	0h	<p>64-bit Addressing</p> <p>This field is effective when the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h.</p> <p>Host Controller selects either of 32-bit or 64-bit addressing modes to access system memory. Whether 32-bit or 64-bit is determined by OS installed in a host system. Host Driver sets this bit depends on addressing mode of installed OS. Refer to 64-bit System Address Support in the MMCSD0_CAPABILITIES register.</p> <p>0h: 32-bits Addressing 1h: 64-bits Addressing</p>
12	HOST_VER40_ENA	R/W	0h	<p>Host Version 4 Enable</p> <p>This bit selects either Version 3.00 compatible mode or Version 4.00 mode. In Version 4.00, support of 64-bit System Addressing is modified. All DMAs support 64-bit System Addressing. UHS-II supported Host Driver shall enable this bit.</p> <p>In Version 4.10, supported 32-bit Block Count for all operations. Functions of following fields are modified.</p> <p>SDMA Address SDMA uses the MMCSD0_ADMA_SYS_ADDRESS register instead of SDMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI)</p> <p>ADMA2/ADMA3 Selection ADMA3 is selected by MMCSD0_HOST_CONTROL1[4-3] DMA_SELECT bit.</p> <p>64-bit ADMA Descriptor Size 128-bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1h.</p> <p>Selection of 32-bit/64-bit System Addressing Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register instead of MMCSD0_HOST_CONTROL1[4-3] DMA_SELECT bit.</p> <p>32-bit Block Count SDMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI) is modified to 32-bit Block Count register.</p> <p>0h: Version 3.00 Compatible Mode 1h: Version 4.0 Mode</p>

Table 18-150. MMCS0_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CMD23_ENA	R/W	0h	<p>CMD23 Enable</p> <p>In memory card initialization, Host Driver Version 4.10 checks whether card supports CMD23 by checking a bit SCR[33]. If the card supports CMD23 (SCR[33] = 1h), this bit is set to 1h. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 data transfer. Refer to MMCS0_TRANSFER_MODE[3-2] AUTO_CMD_ENA bit.</p>
10	ADMA2_LEN_MODE	R/W	0h	<p>ADMA2 Length Mode</p> <p>This bit selects one of ADMA2 Length Modes either 16-bit or 26-bit.</p> <p>0h: 16-bit Data Length Mode</p> <p>1h: 26-bit Data Length Mode</p>
9	DRIVER_STRENGTH2	R/W	0h	<p>Driver Strength Select</p> <p>This is the programmed Drive Strength output and Bit[2] of the sdhccore_drivestrength value.</p>
8	UHS2_INTF_ENABLE	R/W	0h	<p>UHS-II Interface Enable</p> <p>This bit is used to enable UHS-II Interface. Before trying to start UHS-II initialization, this bit shall be set to 1h. Before trying to start SD mode initialization, this bit shall be set to 0h.</p> <p>This bit is used to enable UHS-II IF Detection, Lane Synchronization and In Dormant State in the MMCS0_PRESENTSTATE register, and to select clock source of either SD mode or UHS-II mode. Host Controller shall not leave unused SD 4-bit Interface lines (CLK, CMD and DAT[3:2]) floating in UHS-II mode by using pull-up or driving to low. When DAT[2] is used as interrupt input in UHS-II mode, DAT[2] of Host Controller is set to input and then DAT[2] of SDIO card is set to output to avoid conflict.</p> <p>0h: 4-bit SD Interface Enabled</p> <p>1h: UHS-II Interface Enabled</p>
7	SAMPLING_CLK_SELECT	R/W	0h	<p>Sampling Clock Select (UHS-I Only)</p> <p>This bit is set by tuning procedure when the MMCS0_HOST_CONTROL2[6] EXECUTE_TUNING bit is cleared. Writing 1h to this bit is meaningless and ignored. Setting 1h means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0h. Change of this bit is not allowed while the Host Controller is receiving response or a read data block.</p> <p>0h: Fixed clock is used to sample data</p> <p>1h: Tuned clock is used to sample data</p>
6	EXECUTE_TUNING	R/W	0h	<p>Execute Tuning (UHS-I Only)</p> <p>This bit is set to 1h to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to the MMCS0_HOST_CONTROL2[7] SAMPLING_CLK_SELECT bit. Tuning procedure is aborted by writing 0h for more detail about tuning procedure.</p> <p>0h: Not Tuned or Tuning Completed</p> <p>1h: Execute Tuning</p>

Table 18-150. MMCSD0_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	DRIVER_STRENGTH1	R/W	0h	<p>Driver Strength Select (UHS-I Only)</p> <p>Host Controller output driver in 1.8 V signaling is selected by this bit. In 3.3 V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the MMCSD0_CAPABILITIES register. This bit depends on setting of the MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit.</p> <p>If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this field is set by Host Driver.</p> <p>If MMCSD0_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this field is automatically set by a value specified in the one of Preset Value registers (MMCSD0_PRESET_VALUE0 - MMCSD0_PRESET_VALUE10).</p> <p>0h: Driver Type B is Selected (Default)</p> <p>1h: Driver Type A is Selected</p> <p>2h: Driver Type C is Selected</p> <p>3h: Driver Type D is Selected</p>
3	V1P8_SIGNAL_ENA	R/W	0h	<p>1.8 V Signaling Enable (UHS-I Only)</p> <p>This bit controls voltage regulator for I/O cell. 3.3 V is supplied to the card regardless of signaling voltage.</p> <p>Setting this bit from 0h to 1h starts changing signal voltage from 3.3 V to 1.8 V.</p> <p>1.8 V regulator output shall be stable within 5 ms. Host Controller clears this bit if switching to 1.8 V signaling fails.</p> <p>Clearing this bit from 1h to 0h starts changing signal voltage from 1.8 V to 3.3 V.</p> <p>3.3 V regulator output shall be stable within 5 ms.</p> <p>Host Driver can set this bit to 1h when Host Controller supports 1.8 V signaling (one of support bits is set to 1h: SDR50, SDR104 or DDR50 in the MMCSD0_CAPABILITIES register) and the card or device supports UHS-I.</p> <p>0h: 3.3 V Signaling</p> <p>1h: 1.8 V Signaling</p>

Table 18-150. MMCSDB_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	UHS_MODE_SELECT	R/W	0h	<p>UHS Mode Select (UHS-I Only)</p> <p>This field is used to select one of UHS-I modes or UHS-II mode. In case of UHS-I mode, this field is effective when the MMCSDB_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit is set to 1h. In case of UHS-II mode, the MMCSDB_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit shall be set to 0h. Setting of this field is used to select one of preset values in UHS-I or UHS-II mode.</p> <p>If the MMCSDB_HOST_CONTROL2[15] PRESET_VALUE_ENA is set to 1h, Host Controller sets SDCLK/RCLK Frequency Select, Clock Generator Select in the MMCSDB_CLOCK_CONTROL register and Driver Strength Select according to Preset Value registers (MMCSDB_PRESET_VALUE0 - MMCSDB_PRESET_VALUE10). In this case, one of preset value registers is selected by this field.</p> <p>Host Driver needs to reset the MMCSDB_CLOCK_CONTROL[2] SD_CLK_ENA bit before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets the MMCSDB_CLOCK_CONTROL[2] SD_CLK_ENA bit again.</p> <p>0h: SDR12 1h: SDR25 2h: SDR50 3h: SDR104 4h: DDR50 5h: HS400 6h: Reserved 7h: UHS-II</p> <p>When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more details.</p>

18.2.27 MMCSO_CAPABILITIES Register (Offset = 40h) [reset = 980004073CECC801h]

MMCSO_CAPABILITIES is shown in [Figure 18-56](#) and described in [Table 18-152](#).

Return to [Summary Table](#).

This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initialization.

Table 18-151. MMCSO_CAPABILITIES Instances

Instance	Physical Address
MMCSO_CTL_CFG	04F8 0040h

Figure 18-56. MMCSO_CAPABILITIES Register

63	62	61	60	59	58	57	56
HS400_SUPPO RT	RESERVED		VDD2_1P8_SU PPORT	ADMA3_SUPP ORT	RESERVED	SPI_BLK_MOD E	SPI_SUPPORT
R-1h	R-0h		R-1h	R-1h	R-0h	R-0h	R-0h
55	54	53	52	51	50	49	48
CLOCK_MULTIPLIER							
R-0h							
47	46	45	44	43	42	41	40
RETUNING_MODES	TUNING_FOR_ SDR50		RESERVED	RETUNING_TIMER_CNT			
R-0h		R-0h	R-0h	R-4h			
39	38	37	36	35	34	33	32
RESERVED	DRIVERD_SUP PORT	DRIVERC_SUP PORT	DRIVERA_SUP PORT	UHS2_SUPPO RT	DDR50_SUPP ORT	SDR104_SUPP ORT	SDR50_SUPP ORT
R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-1h
31	30	29	28	27	26	25	24
SLOT_TYPE		ASYNCH_INTR_ SUPPORT	ADDR_64BIT_ SUPPORT_V3	ADDR_64BIT_ SUPPORT_V4	VOLT_1P8_SU PPORT	VOLT_3P0_SU PPORT	VOLT_3P3_SU PPORT
R-0h		R-1h	R-1h	R-1h	R-1h	R-0h	R-0h
23	22	21	20	19	18	17	16
SUSP_RES_S UPPORT	SDMA_SUPPO RT	HIGH_SPEED_ SUPPORT	RESERVED	ADMA2_SUPP ORT	BUS_8BIT_SU PPORT	MAX_BLK_LENGTH	
R-1h	R-1h	R-1h	R-0h	R-1h	R-1h	R-0h	
15	14	13	12	11	10	9	8
BASE_CLK_FREQ							
R-C8h							
7	6	5	4	3	2	1	0
TIMEOUT_CLK_ UNIT	RESERVED	TIMEOUT_CLK_FREQ					
R-0h	R-0h	R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 18-152. MMCS0_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
63	HS400_SUPPORT	R	1h	HS400 Support 0h: HS400 is Not Supported 1h: HS400 is Supported Note: HS400 mode is not supported (see <i>MMCS0 Not Supported Features</i>).
62-61	RESERVED	R	0h	Reserved
60	VDD2_1P8_SUPPORT	R	1h	1.8 V VDD2 Support This bit indicates that support of VDD2 on Host system. 0h: 1.8 V VDD2 is not supported 1h: 1.8 V VDD2 is supported
59	ADMA3_SUPPORT	R	1h	ADMA3 Support This bit indicates that support of ADMA3 on Host Controller. 0h: ADMA3 is not supported 1h: ADMA3 is supported
58	RESERVED	R	0h	Reserved
57	SPI_BLK_MODE	R	0h	SPI Block Mode This bit indicates whether SPI Block Mode is supported or not. 0h: Not Supported 1h: Supported
56	SPI_SUPPORT	R	0h	SPI Mode This bit indicates whether SPI Mode is supported or not. 0h: Not Supported 1h: Supported
55-48	CLOCK_MULTIPLIER	R	0h	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to the MMCS0_CLOCK_CONTROL register. Setting 00h means that Host Controller does not support programmable clock generator. FFh: Clock Multiplier M = 256 ---- 02h: Clock Multiplier M = 3 01h: Clock Multiplier M = 2 00h: Clock Multiplier is Not Supported
47-46	RETUNING_MODES	R	0h	Re-tuning Modes (UHS-I Only) This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver. 0h: Mode 1 1h: Mode 2 2h: Mode 3 3h: Reserved There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.
45	TUNING_FOR_SDR50	R	0h	Use Tuning for SDR50 (UHS-I Only) If this bit is set to 1h, this Host Controller requires tuning to operate SDR50 (tuning is always required to operate SDR104). 0h: SDR50 does not require tuning 1h: SDR50 requires tuning Note: Tuning is required for SDR50 to compensate temperature variation.

Table 18-152. MMCSD0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
44	RESERVED	R	0h	Reserved
43-40	RETUNING_TIMER_CNT	R	4h	<p>Timer Count for Re-Tuning (UHS-I Only)</p> <p>This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3.</p> <p>0h - Get information via other source</p> <p>1h = 1 seconds</p> <p>2h = 2 seconds</p> <p>3h = 4 seconds</p> <p>4h = 8 seconds</p> <p>----</p> <p>$n = 2_{(n-1)}$ seconds</p> <p>----</p> <p>Bh = 1024 seconds</p> <p>Fh - Ch = Reserved</p>
39	RESERVED	R	0h	Reserved
38	DRIVERD_SUPPORT	R	0h	<p>Driver Type D Support (UHS-I Only)</p> <p>This bit indicates support of Driver Type D for 1.8 Signaling.</p> <p>0h: Driver Type D is Not Supported</p> <p>1h: Driver Type D is Supported</p>
37	DRIVERC_SUPPORT	R	0h	<p>Driver Type C Support (UHS-I Only)</p> <p>This bit indicates support of Driver Type C for 1.8 Signaling.</p> <p>0h: Driver Type C is Not Supported</p> <p>1h: Driver Type C is Supported</p>
36	DRIVERA_SUPPORT	R	0h	<p>Driver Type A Support (UHS-I Only)</p> <p>This bit indicates support of Driver Type A for 1.8 Signaling.</p> <p>0h: Driver Type A is Not Supported</p> <p>1h: Driver Type A is Supported</p>
35	UHS2_SUPPORT	R	0h	<p>UHS-II Support (UHS-II Only)</p> <p>This bit indicates whether Host Controller supports UHS-II.</p> <p>If this bit is set to 1h, the MMCSD0_CAPABILITIES[60] VDD2_1P8_SUPPORT bit shall be set to 1h (Host System shall support VDD2 power supply).</p> <p>0h: UHS-II is Not Supported</p> <p>1h: UHS-II is Supported</p>
34	DDR50_SUPPORT	R	1h	<p>DDR50 Support (UHS-I Only)</p> <p>This bit indicates whether DDR50 is supported or not.</p> <p>0h: DDR50 is Not Supported</p> <p>1h: DDR50 is Supported</p>
33	SDR104_SUPPORT	R	1h	<p>SDR104 Support (UHS-I Only)</p> <p>This bit indicates whether SDR104 is supported or not. SDR104 requires tuning.</p> <p>0h: SDR104 is Not Supported</p> <p>1h: SDR104 is Supported</p>
32	SDR50_SUPPORT	R	1h	<p>SDR50 Support (UHS-I Only)</p> <p>If SDR104 is supported, this bit shall be set to 1h. Bit 40 indicates whether SDR50 requires tuning or not.</p> <p>0h: SDR50 is Not Supported</p> <p>1h: SDR50 is Supported</p>

Table 18-152. MMCS0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31-30	SLOT_TYPE	R	0h	<p>Slot Type</p> <p>This field indicates usage of a slot by a specific Host System (a host controller register set is defined per slot). Embedded slot for one device (1h) means that only one non-removable device is connected to a SD bus slot. Shared Bus Slot (2h) can be set if Host Controller supports Shared Bus Control register.</p> <p>The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus (2h), the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System.</p> <p>0h: Removable Card Slot 1h: Embedded Slot for One Device 2h: Shared Bus Slot (SD Mode) 3h: UHS-II Multiple Embedded Devices</p>
29	ASYNCH_INTR_SUPPORT	R	1h	<p>Asynchronous Interrupt Support (SD Mode Only)</p> <p>Refer to SDIO Specification Version 3.00 about asynchronous interrupt.</p> <p>0h: Asynchronous Interrupt Not Supported 1h: Asynchronous Interrupt Supported</p>
28	ADDR_64BIT_SUPPORT_V3	R	1h	<p>64-bit System Address Support for V3</p> <p>Meaning of this bit is different depends on Versions. Host Controller Version 3.00 and Version 4.10 use this bit as 64-bit System Address support for V3 mode. Host Controller Version 4.00 uses this bit as 64-bit System Address support for both V3 and V4 modes.</p> <p>SDMA cannot be used in 64-bit Addressing in Version 3 mode.</p> <p>If this bit is set to 1h, 64-bit ADMA2 with using 96-bit Descriptor may be enabled as follows:</p> <p>In case of Host Controller Version 3, 64-bit ADMA2 is enabled by MMCS0_HOST_CONTROL1[4-3] DMA_SELECT = 3h. In case of Host Controller Version 4, 64-bit ADMA2 for Version 3 is enabled by setting MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h and MMCS0_HOST_CONTROL1[4-3] DMA_SELECT = 3h.</p> <p>0h: 64-bit System Address for V3 is not Supported 1h: 64-bit System Address for V3 is Supported</p>
27	ADDR_64BIT_SUPPORT_V4	R	1h	<p>64-bit System Address Support for V4</p> <p>This bit is added from Version 4.10. Setting 1h to this bit indicates that the Host Controller supports 64-bit System Addressing of Version 4 mode.</p> <p>When this bit is set to 1h, full or a part of 64-bit address should be used to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to the MMCS0_HOST_CONTROL2[13] BIT64_ADDRESSING bit.</p> <p>If this bit is set to 1h, 64-bit DMA Addressing for Version 4 is enabled by setting MMCS0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h, MMCS0_HOST_CONTROL2[13] BIT64_ADDRESSING = 1h.</p> <p>SDMA can be used and ADMA2 uses 128-bit Descriptor.</p> <p>0h: 64-bit System Address for V4 is not Supported 1h: 64-bit System Address for V4 is Supported</p>

Table 18-152. MMCSD0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	VOLT_1P8_SUPPORT	R	1h	Voltage Support 1.8 V This bit indicates whether the HC supports 1.8 V. 0h: 1.8 V Not Supported 1h: 1.8 V Supported
25	VOLT_3P0_SUPPORT	R	0h	Voltage Support 3.0 V This bit indicates whether the HC supports 3.0 V. 0h: 3.0 V Not Supported 1h: 3.0 V Supported
24	VOLT_3P3_SUPPORT	R	0h	Voltage Support 3.3 V This bit indicates whether the HC supports 3.3 V. 0h: 3.3 V Not Supported 1h: 3.3 V Supported
23	SUSP_RES_SUPPORT	R	1h	Suspend/Resume Support This bit indicates whether the HC supports Suspend/Resume functionality. If this bit is 0h, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend/Resume commands. 0h: Not Supported 1h: Supported
22	SDMA_SUPPORT	R	1h	SDMA Support This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. Version 4.10 Host Controller shall support SDMA if ADMA2 is supported. 0h: SDMA Not Supported 1h: SDMA Supported
21	HIGH_SPEED_SUPPORT	R	1h	High Speed Support This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25 MHz to 50 MHz (for SD)/20 MHz to 52 MHz (for MMC). 0h: High Speed Not Supported 1h: High Speed Supported
20	RESERVED	R	0h	Reserved
19	ADMA2_SUPPORT	R	1h	ADMA2 Support 0h: ADMA2 Not support 1h: ADMA2 support
18	BUS_8BIT_SUPPORT	R	1h	8-bit Support for Embedded Device (Embedded) This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. This bit is not effective when the MMCSD0_CAPABILITIES[31-30] SLOT_TYPE bit field is set to 2h. 0h: 8-bit Bus Width Not Supported 1h: 8-bit Bus Width Supported
17-16	MAX_BLK_LENGTH	R	0h	Max Block Length This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. 0h: 512 byte 1h: 1024 byte 2h: 2048 byte 3h: 4096 byte

Table 18-152. MMCSDB0_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	BASE_CLK_FREQ	R	C8h	Base Clock Frequency for SD Clock (1) 6-bit Base Clock Frequency: This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. 11xx xxxxb: Not Supported 0011 1111b: 63 MHz 0000 0010b: 2 MHz 0000 0001b: 1 MHz 0000 0000b: Get Information via another method (2) 8-bit Base Clock Frequency: This mode is supported by the Host Controller Version 3.00. Unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. FFh: 255 MHz 02h: 2 MHz 01h: 1 MHz 00h: Get Information via another method If the real frequency is 16.5 MHz, the larger value shall be set 0001 0001b (17 MHz) because the Host Driver use this value to calculate the clock divider value (refer to the MMCSDB0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field) and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method.
7	TIMEOUT_CLK_UNIT	R	0h	Timeout Clock Unit This bit shows the unit of base clock frequency used to detect Data Timeout Error (MMCSDB0_ERROR_INTR_STS[4] DATA_TIMEOUT). 0h: KHz 1h: MHz
6	RESERVED	R	0h	Reserved
5-0	TIMEOUT_CLK_FREQ	R	1h	Timeout Clock Frequency This bit shows the base clock frequency used to detect Data Timeout Error (MMCSDB0_ERROR_INTR_STS[4] DATA_TIMEOUT). 0h: Get Information via another method Not 0h: 1 KHz to 63 KHz/1 MHz to 63 MHz

Table 18-153 shows the 64-bit System Address Support depends on Versions.

Table 18-153. 64-bit System Address Support depends on Versions

Host Controller	Version 3.00	Version 4.00	Version 4.10
D28 (from Version 2.00)	for V3	for V3 and V4	for V3
D27 (from Version 4.10)	D27 (from Version 4.10)	Not Defined	for V4
Register Decode	32-bit or 64-bit (up to implementation)	32-bit or 64-bit (up to implementation)	If D27 = 1h, 64-bit
SDMA	Not supported	Supported when MMCSDB0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h	Supported when MMCSDB0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h
ADMA2 (96-bit Descriptor)	DMA Select = 3h	Selected by MMCSDB0_HOST_CONTROL2[12] HOST_VER40_ENA = 0h	MMCSDB0_HOST_CONTROL2

Table 18-153. 64-bit System Address Support depends on Versions (continued)

Host Controller	Version 3.00	Version 4.00	Version 4.10
ADMA2 (128-bit Descriptor)	Not Defined	Selected by MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h	Selected by MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA = 1h

As the specification of 64-bit System Address Support has been changed, capabilities of 64-bit functions are different depends on versions.

Definition of D28 is different depends on Versions. 96-bit Descriptor was defined by Version 2 but notation V3 is used including V2. Version 4.10 divides 64-bit System Address Support into V3 mode (D28) and V4 mode (D27) so that V3 mode can be optional. Migrate to V4 is recommended. From Host Controller Version 4.00, either V3 mode or V4 mode is selected by Host Version 4 Enable in the Host Control 2 register. V3 mode can be used if 64-bit System Address Support for V3 is set to 1h. V4 mode can be used if 64-bit System Address Support for V4 is set to 1h.

Prior to Version 4.10, address length of Host Controller registers decoding is not defined and whether 32-bit or 64-bit address is used to decode Host Controller registers is up to implementation. If Host Controller decodes 32-bit system address in default, the Host Controller Registers shall be placed in 32-bit addressing space.

When D27 = 1h, Host Controller Version 4.10 or later should use full or a part of 64-bit address to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to the MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit. How to decode register also should follow a system bus specification or a mother board specification.

From Version 4.00, 64-bit System Addressing of DMA is enabled by setting to the MMCSD0_HOST_CONTROL2[13] BIT64_ADDRESSING bit. 64-bit SDMA is not supported in V3 mode and is supported in V4 mode. There are two Descriptor types for ADMA2 96-bit (V3) or 128-bit (V4). Support of 96-bit Descriptor is optional for Host Controller Version 4.10. If D28 = 0h, 96-bit Descriptor is not supported.

Note: The Host System shall support at least one of these voltages above. The HD sets the MMCSD0_POWER_CONTROL[3:1] SD_BUS_VOLTAGE bit field according to these support bits. If multiple voltages are supported, select the usable lower voltage by comparing the OCR value from the card.

These registers indicate maximum current capability for each voltage. The value is meaningful if Voltage Support is set in the MMCSD0_CAPABILITIES register.

Table 18-154 describes the re-tuning modes.

Table 18-154. 64-bit System Address Support depends on Versions

Bit47-46	Re-Tuning Mode	Data length	Timer Modes
0h	Mode1	4 MB (Max.)	Always enabled
1h	Mode2	4 MB (Max.)	Stop during data transfer
2h	Reserved	Reserved	Reserved
3h	Reserved	Reserved	Reserved

There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.

Data length per a read/write command is restricted by whether Host Controller generates Re-Tuning Request during data transfer so that re-tuning procedures can be inserted during data transfers.

18.2.28 MMCS0_MAX_CURRENT_CAP Register (Offset = 48h) [reset = 0h]

MMCS0_MAX_CURRENT_CAP is shown in [Figure 18-57](#) and described in [Table 18-156](#).

Return to [Summary Table](#).

This register indicates maximum current capability for each voltage.

Table 18-155. MMCS0_MAX_CURRENT_CAP Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0048h

Figure 18-57. MMCS0_MAX_CURRENT_CAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-0h															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED								VDD2_1P8V							
R-0h								R-0h							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								VDD1_1P8V							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDD1_3P0V								VDD1_3P3V							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-156. MMCS0_MAX_CURRENT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39-32	VDD2_1P8V	R	0h	Maximum Current for 1.8 V VDD2
31-24	RESERVED	R	0h	Reserved
23-16	VDD1_1P8V	R	0h	Maximum Current for 1.8 V VDD1
15-8	VDD1_3P0V	R	0h	Maximum Current for 3.0 V VDD1
7-0	VDD1_3P3V	R	0h	Maximum Current for 3.3 V VDD1

[Table 18-157](#) describes the maximum current value.

Table 18-157. Maximum Current Value Definition

Register Value	Current Value
0	Get Information via another method
1	4 mA
2	8 mA
3	12 mA
-----	-----
255	1020 mA

18.2.29 MMCSD0_FORCE_EVT_ACMD_ERR_STS Register (Offset = 50h) [reset = 0h]

MMCSD0_FORCE_EVT_ACMD_ERR_STS is shown in [Figure 18-58](#) and described in [Table 18-159](#).

Return to [Summary Table](#).

This register is not physically implemented, rather it is an address where the MMCSD0_AUTOCMD_ERR_STS register can be written.

Writing 1h: set each bit of the MMCSD0_AUTOCMD_ERR_STS register

Writing 0h: no effect

By setting a bit in this register, the correspondent bit is set in the MMCSD0_ERROR_INTR_STS register. In order to generate interrupt signal, the correspondent bit shall be set in the MMCSD0_ERROR_INTR_STS_ENA register and MMCSD0_ERROR_INTR_SIG_ENA register.

Table 18-158.
MMCSD0_FORCE_EVT_ACMD_ERR_STS
Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0050h

Figure 18-58. MMCSD0_FORCE_EVT_ACMD_ERR_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMD_NOT_ISS	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACMD_NOT_EXEC
W-0h	R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 18-159. MMCSD0_FORCE_EVT_ACMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMD_NOT_ISS	W	0h	Force Event for Command Not Issued by AUTO CMD12 Error 0h: Not Affected 1h: Command Not Issued By Auto CMD12 Error Status is set
6	RESERVED	R	0h	Reserved
5	RESP	W	0h	Force Event for AUTO CMD Response Error 0h: Not Affected 1h: Auto CMD Response Error Status is set
4	INDEX	W	0h	Force Event for AUTO CMD Index Error 0h: Not Affected 1h: Auto CMD Index Error Status is set
3	ENDBIT	W	0h	Force Event for AUTO CMD End Bit Error 0h: Not Affected 1h: Auto CMD End bit Error Status is set
2	CRC	W	0h	Force Event for AUTO CMD Timeout Error 0h: Not Affected 1h: Auto CMD CRC Error Status is set
1	TIMEOUT	W	0h	Force Event for AUTO CMD Timeout Error 0h: Not Affected 1h: Auto CMD Timeout Error Status is set

Table 18-159. MMCSDB_FORCE_EVT_ACMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ACMD_NOT_EXEC	W	0h	Force Event for AUTO CMD12 Not Executed 0h: Not Affected 1h: Auto CMD12 Not Executed Status is set

18.2.30 MMCSD0_FORCE_EVT_ERR_INT_STS Register (Offset = 52h) [reset = 0h]

MMCSD0_FORCE_EVT_ERR_INT_STS is shown in [Figure 18-59](#) and described in [Table 18-161](#).

Return to [Summary Table](#).

This register is not physically implemented, rather it is an address where the MMCSD0_ERROR_INTR_STS register can be written.

The MMCSD0_FORCE_EVT_ERR_INT_STS register is not a physically implemented register. Rather, it is an address at which the MMCSD0_ERROR_INTR_STS register can be written. The effect of a write to this address will be reflected in the MMCSD0_ERROR_INTR_STS register if the corresponding bit of the MMCSD0_ERROR_INTR_STS_ENA register is set.

Writing 1h: set each bit of the MMCSD0_ERROR_INTR_STS register

Writing 0h: no effect

Table 18-160.
MMCSD0_FORCE_EVT_ERR_INT_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0052h

Figure 18-59. MMCSD0_FORCE_EVT_ERR_INT_STS Register

15	14	13	12	11	10	9	8
VEND_SPEC				RESP	TUNING	ADMA	AUTO_CMD
W-0h				W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CURR_LIM	DAT_ENDBIT	DAT_CRC	DAT_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 18-161. MMCSD0_FORCE_EVT_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VEND_SPEC	W	0h	N/A
11	RESP	W	0h	Force Event for Response Error 0h: Not Affected 1h: Response Error Status is set
10	TUNING	W	0h	Force Event for Tuning Error 0h: Not Affected 1h: Tuning Error Status is set
9	ADMA	W	0h	Force Event for ADMA Error 0h: Not Affected 1h: ADMA Error Status is set
8	AUTO_CMD	W	0h	Force Event for Auto CMD Error 0h: Not Affected 1h: Auto CMD Error Status is set
7	CURR_LIM	W	0h	Force Event for Current Limit Error 0h: Not Affected 1h: Current Limit Error Status is set
6	DAT_ENDBIT	W	0h	Force Event for Data End Bit Error 0h: Not Affected 1h: Data End Bit Error Status is set

Table 18-161. MMCS0_FORCE_EVT_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DAT_CRC	W	0h	Force Event for Data CRC Error 0h: Not Affected 1h: CRC Error Status is set
4	DAT_TIMEOUT	W	0h	Force Event for Data Timeout Error 0h: Not Affected 1h: Timeout Error Status is set
3	CMD_INDEX	W	0h	Force Event for Command Index Error 0h: Not Affected 1h: Command Index Error Status is set
2	CMD_ENDBIT	W	0h	Force Event for Command End Bit Error 0h: Not Affected 1h: Command End Bit Error Status is set
1	CMD_CRC	W	0h	Force Event for Command CRC Error 0h: Not Affected 1h: Command CRC Error Status is set
0	CMD_TIMEOUT	W	0h	Force Event for CMD Timeout Error 0h: Not Affected 1h: Command Timeout Error Status is set

18.2.31 MMCSDB0_ADMA_ERR_STATUS Register (Offset = 54h) [reset = 0h]

MMCSDB0_ADMA_ERR_STATUS is shown in [Figure 18-60](#) and described in [Table 18-163](#).

Return to [Summary Table](#).

When the ADMA Error interrupt occur, this register holds the ADMA State (MMCSDB0_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE) and the MMCSDB0_ADMA_SYS_ADDRESS register holds address around the error descriptor.

**Table 18-162. MMCSDB0_ADMA_ERR_STATUS
Instances**

Instance	Physical Address
MMCSDB0_CTL_CFG	04F8 0054h

Figure 18-60. MMCSDB0_ADMA_ERR_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					ADMA_LENGTH_ERR	ADMA_ERR_STATE	
R-0h					R-0h	R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 18-163. MMCSDB0_ADMA_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	ADMA_LENGTH_ERR	R	0h	ADMA Length Mismatch Error This error occurs in the following 2 cases. While the MMCSDB0_TRANSFER_MODE[1] BLK_CNT_ENA bit being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 0h: No Error 1h: Error
1-0	ADMA_ERR_STATE	R	0h	ADMA Error State This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "2h" because ADMA never stops in this state. D01 - D00: ADMA Error State when error occurred Contents of SYS_SDR register 0h: ST_STOP (Stop DMA) Points to next of the error descriptor 1h: ST_FDS (Fetch Descriptor) Points to the error descriptor 2h: Never set this state (Not used) 3h: ST_TFR (Transfer Data) Points to the next of the error descriptor

18.2.32 MMCS0_ADMA_SYS_ADDRESS Register (Offset = 58h) [reset = Xh]

MMCS0_ADMA_SYS_ADDRESS is shown in [Figure 18-61](#) and described in [Table 18-165](#).

Return to [Summary Table](#).

This register contains the physical address used for ADMA data transfer.

Table 18-164. MMCS0_ADMA_SYS_ADDRESS Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0058h

Figure 18-61. MMCS0_ADMA_SYS_ADDRESS Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADMA_ADDR																															
R/W-Xh																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADMA_ADDR																															
R/W-Xh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-165. MMCSD0_ADMA_SYS_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ADMA_ADDR	R/W	Xh	<p>ADMA System Address</p> <p>The 32-bit addressing Host Driver uses lower 32-bit of this register (upper 32-bit should be set to 0h) and shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. DMA2/3 ignores lower 2-bit of this register and assumes it to be 0h. DMA in 64-bit addressing. The 64-bit addressing Host Driver uses all bits of this register and shall program Descriptor Table on 64-bit boundary and set 64-bit boundary address to this register. DMA2/3 ignores lower 3-bit of this register and assumes it to be 0h.</p> <p>SDMA</p> <p>If the MMCSD0_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, SDMA use this register to indicate System Address of data location instead of using SDMA System Address register (MMCSD0_SDMA_SYS_ADDR_LO/ MMCSD0_SDMA_SYS_ADDR_HI). SDMA can be used in 32-bit and 64-bit addressing in Version 4.00.</p> <p>ADMA2</p> <p>This register holds byte address of executing command of the Descriptor table. At the start of ADMA2, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state.</p> <p>ADMA3</p> <p>This register is set by ADMA3. Host Driver is not necessary to set this register. The ADMA3 increments address of this register, which points to next line, when every time fetching a Descriptor line. When Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state.</p> <p>Register Value - 00000000_xxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxh Addressing Mode - 64-bit System Address</p>

18.2.33 MMCS0_PRESET_VALUE0 Register (Offset = 60h) [reset = 100h]

MMCS0_PRESET_VALUE0 is shown in [Figure 18-62](#) and described in [Table 18-168](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

When the MMCS0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1h, SDCLK/RCLK Frequency Select and Clock Generator Select in the MMCS0_CLOCK_CONTROL register, and Driver Strength Select in the MMCS0_HOST_CONTROL2 register are automatically set based on the Selected Bus Speed Mode (see [Table 18-166](#)). This means the Host Driver needs not set these fields when preset is enabled.

Before starting the initialization sequence, the Host Driver needs to set a clock preset value to SDCLK/RCLK Frequency Select in the MMCS0_CLOCK_CONTROL register. The MMCS0_HOST_CONTROL2[15] PRESET_VALUE_ENA bit can be set after initialization completed.

[Table 18-166](#) shows the conditions to select one of preset value registers.

Table 18-166. Preset Value Register Select Condition

Selected Bus Speed Mode	1.8 V Signaling Enable (Host Control 2)	High Speed Enable (Host Control 1)	UHS-1 Mode Selection (Host Control 2)
Default Speed	0	0	don't care
High Speed	0	1	don't care
SDR12	1	don't care	0h
SDR25	1	don't care	1h
SDR50	1	don't care	2h
SDR104	1	don't care	3h
DDR50	1	don't care	4h
HS400	1	don't care	5h
Reserved	Not determined	don't care	6h
UHS-II	0	don't care	7h

Table 18-167. MMCS0_PRESET_VALUE0 Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0060h

Figure 18-62. MMCS0_PRESET_VALUE0 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-100h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-100h							

LEGEND: R = Read Only; -n = value after reset

Table 18-168. MMCSD0_PRESET_VALUE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SELECT	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	100h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.34 MMCS0_PRESET_VALUE1 Register (Offset = 62h) [reset = 4h]

MMCS0_PRESET_VALUE1 is shown in [Figure 18-63](#) and described in [Table 18-170](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-169. MMCS0_PRESET_VALUE1 Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0062h

Figure 18-63. MMCS0_PRESET_VALUE1 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-4h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-4h							

LEGEND: R = Read Only; -n = value after reset

Table 18-170. MMCS0_PRESET_VALUE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	4h	SDCLK Frequency Select Value 10-bit preset value to set the MMCS0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.35 MMCSD0_PRESET_VALUE2 Register (Offset = 64h) [reset = 2h]

MMCSD0_PRESET_VALUE2 is shown in [Figure 18-64](#) and described in [Table 18-172](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-171. MMCSD0_PRESET_VALUE2 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0064h

Figure 18-64. MMCSD0_PRESET_VALUE2 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-2h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -n = value after reset

Table 18-172. MMCSD0_PRESET_VALUE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.36 MMCS0_PRESET_VALUE3 Register (Offset = 66h) [reset = 4h]

MMCS0_PRESET_VALUE3 is shown in [Figure 18-65](#) and described in [Table 18-174](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-173. MMCS0_PRESET_VALUE3 Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0066h

Figure 18-65. MMCS0_PRESET_VALUE3 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-4h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-4h							

LEGEND: R = Read Only; -n = value after reset

Table 18-174. MMCS0_PRESET_VALUE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	4h	SDCLK Frequency Select Value 10-bit preset value to set the MMCS0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.37 MMCSD0_PRESET_VALUE4 Register (Offset = 68h) [reset = 2h]

MMCSD0_PRESET_VALUE4 is shown in [Figure 18-66](#) and described in [Table 18-176](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-175. MMCSD0_PRESET_VALUE4 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0068h

Figure 18-66. MMCSD0_PRESET_VALUE4 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-2h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -n = value after reset

Table 18-176. MMCSD0_PRESET_VALUE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.38 MMCS0_PRESET_VALUE5 Register (Offset = 6Ah) [reset = 1h]

MMCS0_PRESET_VALUE5 is shown in [Figure 18-67](#) and described in [Table 18-178](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-177. MMCS0_PRESET_VALUE5 Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 006Ah

Figure 18-67. MMCS0_PRESET_VALUE5 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-1h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-1h							

LEGEND: R = Read Only; -n = value after reset

Table 18-178. MMCS0_PRESET_VALUE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	1h	SDCLK Frequency Select Value 10-bit preset value to set the MMCS0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.39 MMCSD0_PRESET_VALUE6 Register (Offset = 6Ch) [reset = 0h]

MMCSD0_PRESET_VALUE6 is shown in [Figure 18-68](#) and described in [Table 18-180](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-179. MMCSD0_PRESET_VALUE6 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 006Ch

Figure 18-68. MMCSD0_PRESET_VALUE6 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-0h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-180. MMCSD0_PRESET_VALUE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.40 MMCS0_PRESET_VALUE7 Register (Offset = 6Eh) [reset = 2h]

MMCS0_PRESET_VALUE7 is shown in [Figure 18-69](#) and described in [Table 18-182](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-181. MMCS0_PRESET_VALUE7 Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 006Eh

Figure 18-69. MMCS0_PRESET_VALUE7 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-2h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -n = value after reset

Table 18-182. MMCS0_PRESET_VALUE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCS0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.41 MMCSD0_PRESET_VALUE8 Register (Offset = 72h) [reset = 1h]

MMCSD0_PRESET_VALUE8 is shown in [Figure 18-70](#) and described in [Table 18-184](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-183. MMCSD0_PRESET_VALUE8 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0072h

Figure 18-70. MMCSD0_PRESET_VALUE8 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-1h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-1h							

LEGEND: R = Read Only; -n = value after reset

Table 18-184. MMCSD0_PRESET_VALUE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	1h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.42 MMCS0_PRESET_VALUE10 Register (Offset = 74h) [reset = 0h]

MMCS0_PRESET_VALUE10 is shown in [Figure 18-71](#) and described in [Table 18-186](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-185. MMCS0_PRESET_VALUE10
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0074h

Figure 18-71. MMCS0_PRESET_VALUE10 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-0h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-186. MMCS0_PRESET_VALUE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCS0_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.2.43 MMCSDB0_ADMA3_DESC_ADDRESS Register (Offset = 78h) [reset = Xh]

MMCSDB0_ADMA3_DESC_ADDRESS is shown in [Figure 18-72](#) and described in [Table 18-188](#).

Return to [Summary Table](#).

The start address of Integrated DMA Descriptor is set to this register.

**Table 18-187. MMCSDB0_ADMA3_DESC_ADDRESS
Instances**

Instance	Physical Address
MMCSDB0_CTL_CFG	04F8 0078h

Figure 18-72. MMCSDB0_ADMA3_DESC_ADDRESS Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
INTG_DESC_ADDR																															
R/W-Xh																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTG_DESC_ADDR																															
R/W-Xh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-188. MMCSDB0_ADMA3_DESC_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	INTG_DESC_ADDR	R/W	Xh	<p>ADMA3 Integrated Descriptor Address</p> <p>The start address of Integrated DMA Descriptor is set to this register. Writing to a specific address starts ADMA3 depends on 32-bit/64-bit address-ing. The ADMA3 fetches one Descriptor Address and increments this field to indicate the next Descriptor address.</p> <p>The 32-bit addressing Host Driver uses lower 32-bit of this register and shall program Descriptor Table on 32-bit boundary. ADMA3 ignores lower 2-bit of this register and assumes it to be 0h. Writing to 07Bh starts ADMA3 data transfer.</p> <p>The 64-bit addressing Host Driver uses all 64-bit of this register and shall program Descriptor Table on 64-bit boundary. ADMA3 ignores lower 3-bit of this register and assumes it to be 0h. Writing to 07Fh starts ADMA3 data transfer.</p> <p>Register Value - 00000000_xxxxxxxh Addressing Mode - 32-bit System Address</p> <p>Register Value - xxxxxxxx_xxxxxxxh Addressing Mode - 64-bit System Address</p>

18.2.44 MMCS0_UHS2_BLOCK_SIZE Register (Offset = 80h) [reset = 0h]

MMCS0_UHS2_BLOCK_SIZE is shown in [Figure 18-73](#) and described in [Table 18-190](#).

Return to [Summary Table](#).

This register is used to configure the number of bytes in a data block.

Table 18-189. MMCS0_UHS2_BLOCK_SIZE Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0080h

Figure 18-73. MMCS0_UHS2_BLOCK_SIZE Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_BOUNDARY				XFER_BLK_SIZE		
R-0h	R/W-0h				R/W-0h		
7	6	5	4	3	2	1	0
XFER_BLK_SIZE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-190. MMCS0_UHS2_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	SDMA_BUF_BOUNDARY	R/W	0h	<p>UHS-II SDMA Buffer Boundary (SDMA only)</p> <p>When system memory is managed by paging, SDMA data transfer is performed in unit of paging. A page size of system memory management is set to this field.</p> <p>Host Controller generates the DMA Interrupt at the page boundary and requests the Host Driver to update the MMCS0_ADMA_SYS_ADDRESS register. SDMA waits until the MMCS0_ADMA_SYS_ADDRESS register is written.</p> <p>At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued (see MMCS0_NORMAL_INTR_STS[1] XFER_COMPLETE).</p> <p>These bits shall be supported when the MMCS0_CAPABILITIES[22] SDMA_SUPPORT bit is set to 1h and this function is active when the MMCS0_UHS2_XFER_MODE[0] DMA_ENA bit register is set to 1h. ADMA does not use this field.</p> <p>0h: 4K bytes (Detects A11 carry out) 1h: 8K bytes (Detects A12 carry out) 2h: 16K Bytes (Detects A13 carry out) 3h: 32K Bytes (Detects A14 carry out) 4h: 64K bytes (Detects A15 carry out) 5h: 128K Bytes (Detects A16 carry out) 6h: 256K Bytes (Detects A17 carry out) 7h: 512K Bytes (Detects A18 carry out)</p>

Table 18-190. MMCSD0_UHS2_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	XFER_BLK_SIZE	R/W	0h	<p>UHS-II Block Size</p> <p>This bit field specifies the block size of data packet. SD Memory Card uses a fixed block size of 512 bytes.</p> <p>Variable block size may be used for SDIO. The maximum value is 2048 Bytes because CRC16 covers up to 2048 bytes. This bit field is effective when the MMCSD0_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h.</p> <p>0000h - No data transfer</p> <p>0001h - 1 Byte</p> <p>0002h - 2 Bytes</p> <p>0003h - 3 Bytes</p> <p>... ..</p> <p>01FFh - 511 Bytes</p> <p>0200h - 512 Bytes</p> <p>... ..</p> <p>0800h - 2048 Bytes</p>

18.2.45 MMCS0_UHS2_BLOCK_COUNT Register (Offset = 84h) [reset = 0h]

MMCS0_UHS2_BLOCK_COUNT is shown in [Figure 18-74](#) and described in [Table 18-192](#).

Return to [Summary Table](#).

This register is used to configure the number of data blocks.

Table 18-191. MMCS0_UHS2_BLOCK_COUNT Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0084h

Figure 18-74. MMCS0_UHS2_BLOCK_COUNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XFER_BLK_COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-192. MMCS0_UHS2_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XFER_BLK_COUNT	R/W	0h	<p>UHS-II Block Count</p> <p>This register is effective when the MMCS0_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h and is enabled when the MMCS0_UHS2_XFER_MODE[1] BLK_CNT_ENA bit is set to 1h and the MMCS0_UHS2_XFER_MODE[5] BYTE_MODE bit is set to 0h. Data transfer stops when the count reaches zero. Setting the block count to 0h results in no data blocks is transferred.</p> <p>This register should be accessed only when no transaction is executing (after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored.</p> <p>00000000h: Stop Count</p> <p>00000001h: 1 block</p> <p>00000002h: 2 blocks</p> <p>... ..</p> <p>FFFFFFFFh: 4G blocks - 1</p>

18.2.46 MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 Register (Offset = 88h to 9Bh) [reset = 0h]

MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 is shown in [Figure 18-75](#) and described in [Table 18-195](#).

Return to [Summary Table](#).

UHS-II Command Packet image is set to this register. The maximum length is 20 bytes (see [Table 18-193](#)). The command length varies depends on a Command Packet type. The length is specified by the MMCSD0_UHS2_COMMAND register.

Table 18-193. UHS-II Command Packet Register

Offset	Preset Value Registers
088h	Command Packet Byte 0
089h	Command Packet Byte 1
08Ah	Command Packet Byte 2
....
09Bh	Command Packet Byte 19

Table 18-194. MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0088h to 04F8 009Bh

Figure 18-75. MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 Register

7	6	5	4	3	2	1	0
CMD_PKT_BYTE							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-195. MMCSD0_UHS2_COMMAND_PKT_0 to MMCSD0_UHS2_COMMAND_PKT_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CMD_PKT_BYTE	R/W	0h	Command Packet Byte UHS-II Command Packet image is set to this register. The command length varies depends on a Command Packet type.

18.2.47 MMCS0_UHS2_XFER_MODE Register (Offset = 9Ch) [reset = 0h]

MMCS0_UHS2_XFER_MODE is shown in [Figure 18-76](#) and described in [Table 18-197](#).

Return to [Summary Table](#).

This register is used to control the operations of data transfers.

On issuing a Command Packet, a Command Packet image is set to UHS-II Command Packet register (see MMCS0_UHS2_COMMAND_PKT_0 - MMCS0_UHS2_COMMAND_PKT_19) but Host Controller does not analyze the setting of UHS-II Command Packet register. Instead, Host Controller refers setting of this register to issue a Command Packet to make the control easy. Setting of these registers shall be correspondent.

**Table 18-196. MMCS0_UHS2_XFER_MODE
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 009Ch

Figure 18-76. MMCS0_UHS2_XFER_MODE Register

15	14	13	12	11	10	9	8
DUPLEX_SELECT	EBSY_WAIT	RESERVED					RESP_INTR_DIS
R/W-0h	R/W-0h	R-0h					R/W-0h
7	6	5	4	3	2	1	0
RESP_ERR_CHK_ENA	RESP_TYPE	BYTE_MODE	DATA_XFER_DIR	RESERVED		BLK_CNT_ENA	DMA_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-197. MMCS0_UHS2_XFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DUPLEX_SELECT	R/W	0h	Half/Full Select Use of 2 lane half duplex mode is determined by Host Driver. 0h: Full Duplex Mode 1h: 2 Lane Half Duplex Mode
14	EBSY_WAIT	R/W	0h	EBSY Wait This bit is set when issuing a command which is accompanied by EBSY packet to indicate end of command execution. Busy is expected for CCMD with R1b/R5b type and DCMD with data transfer. If this bit is set to 1h, Host Controller waits receiving of EBSY packet and on receiving EBSY packet, the MMCS0_NORMAL_INTR_STS[1] XFER_COMPLETE bit is set to 1h to indicate end of busy. If an error is indicated in EBSY packet (for example: Memory Error), the MMCS0_UHS2_ERR_INTR_STS[8] EBSY bit is set to 1h. Setting of the MMCS0_UHS2_ERR_INTR_STS[8] EBSY bit also sets the MMCS0_NORMAL_INTR_STS[15] ERROR_INTR bit to 1h. The MMCS0_NORMAL_INTR_STS[15] ERROR_INTR and MMCS0_NORMAL_INTR_STS[1] XFER_COMPLETE bits shall be set together. 0h: Issue a command without busy 1h: Wait EBSY
13-9	RESERVED	R	0h	Reserved

Table 18-197. MMCSD0_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RESP_INTR_DIS	R/W	0h	<p>Response Interrupt Disable</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.</p> <p>If Host Driver checks response error, sets this bit to 0h and waits the MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit and then check the response register (MMCSD0_RESPONSE_0 - MMCSD0_RESPONSE_7). If Host Controller checks response error, sets this bit to 1h and sets the MMCSD0_UHS2_XFER_MODE[7] RESP_ERR_CHK_ENA bit to 1h. The MMCSD0_NORMAL_INTR_STS[0] CMD_COMPLETE bit is disabled by this bit regardless of MMCSD0_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit.</p> <p>0h: Response Interrupt is enabled 1h: Response Interrupt is disabled</p>
7	RESP_ERR_CHK_ENA	R/W	0h	<p>Response Error Check Enable</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.</p> <p>If Host Driver checks response error, this bit is set to 0h and the MMCSD0_UHS2_XFER_MODE[8] RESP_INTR_DIS bit is set to 0h. If Host Controller checks response error, sets this bit to 1h and sets the MMCSD0_UHS2_XFER_MODE[8] RESP_INTR_DIS bit to 1h. Response Type R1/R5 selects either R1 or R5 response type. If an error is detected, RES Packet Error Interrupt is generated in the MMCSD0_UHS2_ERR_INTR_STS register.</p> <p>0h: Response Error Check is disabled 1h: Response Error Check is enabled</p>

Table 18-197. MMCSDB_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESP_TYPE	R/W	0h	<p>Response Type R1/R5</p> <p>When response error check is enabled, this bit selects either R1 or R5 response types.</p> <p>Two types of response checks are supported: R1 for memory and R5 for SDIO.</p> <p>Error Statuses Checked in R1:</p> <p>Bit31 OUT_OF_RANGE</p> <p>Bit30 ADDRESS_ERROR</p> <p>Bit29 BLOCK_LEN_ERROR</p> <p>Bit26 WP_VIOLATION</p> <p>Bit25 CARD_IS_LOCKED</p> <p>Bit23 COM_CRC_ERROR</p> <p>Bit21 CARD_ECC_FAILED</p> <p>Bit20 CC_ERROR</p> <p>Bit19 ERROR</p> <p>Response Flags Checked in R5:</p> <p>Bit07 COM_CRC_ERROR</p> <p>Bit03 ERROR</p> <p>Bit01 FUNCTION_NUMBER</p> <p>Bit00 OUT_OF_RANGE</p> <p>0h: R1 (Memory)</p> <p>1h: R5 (SDIO)</p>
5	BYTE_MODE	R/W	0h	<p>Block/Byte Mode</p> <p>This bit specifies whether data transfer is in byte mode or block mode when the MMCSDB_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. This bit is effective to a command with data transfer.</p> <p>0h: Block Mode</p> <p>1h: Byte Mode</p>
4	DATA_XFER_DIR	R/W	0h	<p>Data Transfer Direction</p> <p>This bit specifies direction of data transfer when the MMCSDB_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. This bit is effective to a command with data transfer.</p> <p>0h: Read (Card to Host)</p> <p>1h: Write (Host to Card)</p>
3-2	RESERVED	R	0h	Reserved
1	BLK_CNT_ENA	R/W	0h	<p>Block Count Enable</p> <p>This bit specifies whether data transfer uses the MMCSDB_UHS2_BLOCK_COUNT register. If this bit is set to 1h, data transfer is terminated by Block Count. Setting to the MMCSDB_UHS2_BLOCK_COUNT register shall be equivalent to TLEN in UHS-II Command Packet register (MMCSDB_UHS2_COMMAND_PKT_0 - MMCSDB_UHS2_COMMAND_PKT_19).</p> <p>0h: Block Count Disabled</p> <p>1h: Block Count Enabled</p>

Table 18-197. MMCSD0_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMA_ENA	R/W	0h	<p>DMA Enable</p> <p>This bit selects whether DMA is used or not and is effective to a command with data transfer. One of DMA types is selected by the MMCSD0_HOST_CONTROL1[4-3] DMA_SELECT bit field.</p> <p>0h: DMA is disabled</p> <p>1h: DMA is enabled</p>

18.2.48 MMCS0_UHS2_COMMAND Register (Offset = 9Eh) [reset = 0h]

MMCS0_UHS2_COMMAND is shown in [Figure 18-77](#) and described in [Table 18-199](#).

Return to [Summary Table](#).

This register is used to program the Command for host controller.

Table 18-198. MMCS0_UHS2_COMMAND Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 009Eh

Figure 18-77. MMCS0_UHS2_COMMAND Register

15	14	13	12	11	10	9	8
RESERVED			PKT_LENGTH				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
CMD_TYPE	DATA_PRESENT	RESERVED		SUB_COMMAND	RESERVED		
R/W-0h	R/W-0h	R-0h		R/W-0h	R-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-199. MMCS0_UHS2_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	PKT_LENGTH	R/W	0h	UHS-II Command Packet Length A command packet length, which is set in the UHS-II Command Packet register (MMCS0_UHS2_COMMAND_PKT_0 - MMCS0_UHS2_COMMAND_PKT_19), is set to this bit field. 00011b – 00000b: 3-0 Bytes (Not used) 00100b: 4 Bytes 10100b: 20 Bytes 11111b – 10101b
7-6	CMD_TYPE	R/W	0h	Command Type This field is used to distinguish a specific command like abort command. If this field is set to 0h, the UHS-II RES Packet is stored in UHS-II Response register (MMCS0_UHS2_RESPONSE_0 - MMCS0_UHS2_RESPONSE_19). To avoid overwriting the UHS-II Response register, when this field is set to 1h, the RES Packet (4 bytes length) of TRANS_ABORT CCMD is stored in the Response register (04F8 0010h - 04F8 0013h) and when this field is set to 2h, the RES Packet (8 bytes length) of memory or SDIO abort command (CMD12 or SDIO Abort command) is stored in the Response register (04F8 0018h - 04F8 001Fh). When this field is set to 3h, Host Controller controls lane to go into dormant state. 0h: Normal Command 1h: TRANS_ABORT CCMD 3h: CMD12 or SDIO Abort command 4h: Go Dormant Command
5	DATA_PRESENT	R/W	0h	Data Present This bit specifies whether the command is accompanied by data packet. 0h: No Data Present 1h: Data Present

Table 18-199. MMCSD0_UHS2_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	RESERVED	R	0h	Reserved
2	SUB_COMMAND	R/W	0h	<p>Sub Command Flag</p> <p>This bit is added from Version 4.10 to distinguish a main command or sub command.</p> <p>When issuing a main command, this bit is set to 0h and when issuing a sub command, this bit is set to 1h. Setting of this bit is checked by the MMCSD0_PRESENTSTATE[28] SUB_COMMAND_STS bit.</p> <p>0h: Sub Command</p> <p>1h: Main Command</p>
1-0	RESERVED	R	0h	Reserved

18.2.49 MMCS0_UHS2_RESPONSE_0 to MMCS0_UHS2_RESPONSE_19 Register (Offset = A0h to B3h) [reset = 0h]

MMCS0_UHS2_RESPONSE_0 to MMCS0_UHS2_RESPONSE_19 is shown in [Figure 18-78](#) and described in [Table 18-201](#).

Return to [Summary Table](#).

This register is used to store received UHS-II RES Packet image.

Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command, which is specified by setting 1h or 2h to the MMCS0_UHS2_COMMAND[7-6] CMD_TYPE bit field. The maximum response length is 20 bytes.

Table 18-200. MMCS0_UHS2_RESPONSE_0 to UHS2_RESPONSE_19 Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00A0h to 04F8 00B3h

Figure 18-78. MMCS0_UHS2_RESPONSE_0 to MMCS0_UHS2_RESPONSE_19 Register

7	6	5	4	3	2	1	0
RESP_PKT_BYTE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-201. MMCS0_UHS2_RESPONSE_0 to UHS2_RESPONSE_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESP_PKT_BYTE	R	0h	Response Packet Byte Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command.

[Table 18-202](#) shows UHS-II Response Register offsets.

Table 18-202. UHS-II Response Register

Offset	Preset Value Registers
04F8 0A0h	Response Packet Byte 0
04F8 0A1h	Response Packet Byte 1
04F8 0A2h	Response Packet Byte 2
....
04F8 0B3h	Response Packet Byte 19

18.2.50 MMCSD0_UHS2_MESSAGE_SELECT Register (Offset = B4h) [reset = 0h]

MMCSD0_UHS2_MESSAGE_SELECT is shown in [Figure 18-79](#) and described in [Table 18-204](#).

Return to [Summary Table](#).

This register is used to access internal buffer.

**Table 18-203. MMCSD0_UHS2_MESSAGE_SELECT
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 00B4h

Figure 18-79. MMCSD0_UHS2_MESSAGE_SELECT Register

7	6	5	4	3	2	1	0
RESERVED						MSG_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-204. MMCSD0_UHS2_MESSAGE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	MSG_SEL	R/W	0h	UHS-II MSG Select Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs can be read from the MMCSD0_UHS2_MESSAGE register (04F8 00BBh - 04F8 00B8h) by setting this register (assumed for debug usage). 0h: The latest MSG 1h: One MSG before 2h: Two MSGs before 3h: Three MSGs before

18.2.51 MMCS0_UHS2_MESSAGE Register (Offset = B8h) [reset = 0h]

MMCS0_UHS2_MESSAGE is shown in [Figure 18-80](#) and described in [Table 18-206](#).

Return to [Summary Table](#).

This register is used to access internal buffer.

Table 18-205. MMCS0_UHS2_MESSAGE Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00B8h

Figure 18-80. MMCS0_UHS2_MESSAGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSG_BYTE3								MSG_BYTE2							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSG_BYTE1								MSG_BYTE0							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-206. MMCS0_UHS2_MESSAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MSG_BYTE3	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCS0_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCS0_UHS2_MESSAGE Register.
23-16	MSG_BYTE2	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCS0_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCS0_UHS2_MESSAGE Register.
15-8	MSG_BYTE1	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCS0_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCS0_UHS2_MESSAGE Register.
7-0	MSG_BYTE0	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCS0_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCS0_UHS2_MESSAGE Register.

18.2.52 MMCSD0_UHS2_DEVICE_INTR_STATUS Register (Offset = BCh) [reset = 0h]

MMCSD0_UHS2_DEVICE_INTR_STATUS is shown in [Figure 18-81](#) and described in [Table 18-208](#).

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This register shows receipt of INT MSG from which device.

Table 18-207.
MMCSD0_UHS2_DEVICE_INTR_STATUS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 00BCh

Figure 18-81. MMCSD0_UHS2_DEVICE_INTR_STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_INT_STS															
R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-208. MMCSD0_UHS2_DEVICE_INTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEV_INT_STS	R/W1C	0h	<p>UHS-II Device Interrupt Status</p> <p>This register shows receipt of INT MSG from which device and is effective when the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. On receiving INT MSG from a device, Host Controller saves the INT MSG to MMCSD0_UHS2_DEVICE_INT_CODE register. A bit of this register, which is correspondent to Device ID, is set to 1h and generate Card Interrupt in Normal Interrupt Status register (see MMCSD0_NORMAL_INTR_STS[8] CARD_INTR).</p> <p>Writing a bit to 1h clears the status bit (interrupt is treated) and writing a bit to 0h keeps the status value (interrupt is untreated).</p> <p>If the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 0h, this register is cleared to 0h and Host Controller ignores receipt of INT MSG.</p> <p>Effective bit range of this register is determined by the MMCSD0_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. If N devices are supported, bits 1 to N are effective. Then Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. A bit of unsupported Device ID in this register shall be indicated to 0h.</p> <p>D00 - Not used (Reserved)</p> <p>D01 - Setting 1h means INT MSG is received from Device ID 1</p> <p>D02 - Setting 1h means INT MSG is received from Device ID 2</p> <p>.....</p> <p>D15 - Setting 1h means INT MSG is received from Device ID 15</p>

18.2.53 MMCS0_UHS2_DEVICE_SELECT Register (Offset = BEh) [reset = 0h]

MMCS0_UHS2_DEVICE_SELECT is shown in [Figure 18-82](#) and described in [Table 18-210](#).

Return to [Summary Table](#).

UHS-II Device Select Register.

Table 18-209. MMCS0_UHS2_DEVICE_SELECT Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00BEh

Figure 18-82. MMCS0_UHS2_DEVICE_SELECT Register

7	6	5	4	3	2	1	0
INT_MSG_ENA	RESERVED			DEV_SEL			
R/W-0h	R-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-210. MMCS0_UHS2_DEVICE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MSG_ENA	R/W	0h	<p>INT MSG Enable (Optional)</p> <p>This bit enables receipt of INT MSG. If this bit is set to 1h, receipt of INT MSG is informed by the MMCS0_NORMAL_INTR_STS[8] CARD_INTR bit. If this bit is set to 0h, Host Controller ignores receipt of INT MSG and may not set the MMCS0_UHS2_DEVICE_INT_CODE register.</p> <p>Support of INT MSG Interrupt is optional. If trying to set this bit to 1h but still this bit is read 0, INT MSG Interrupt is not supported by the Host Controller. In this case, the MMCS0_UHS2_DEVICE_INTR_STATUS register always shall be read 0 and the MMCS0_UHS2_DEVICE_INT_CODE register may not be implemented.</p> <p>0h: Disabled 1h: Enabled</p>
6-4	RESERVED	R	0h	Reserved
3-0	DEV_SEL	R/W	0h	<p>UHS-II Device Select</p> <p>Host Controller holds an INT MSG packet per device. One of INT MSGs (up to 15) can be selected by this field and read from the MMCS0_UHS2_DEVICE_INT_CODE. This field is effective when the MMCS0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h.</p> <p>The number of devices implemented in the Host Controller is indicated by the MMCS0_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field.</p> <p>0h: Unselected (Default) 1h: INT MSG of Device ID 1 is selected 2h: INT MSG of Device ID 2 is selected Fh: INT MSG of Device ID 15 is selected</p>

18.2.54 MMCSD0_UHS2_DEVICE_INT_CODE Register (Offset = BFh) [reset = 0h]

MMCSD0_UHS2_DEVICE_INT_CODE is shown in [Figure 18-83](#) and described in [Table 18-212](#).

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This register is effective when the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h.

**Table 18-211. MMCSD0_UHS2_DEVICE_INT_CODE
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 00BFh

Figure 18-83. MMCSD0_UHS2_DEVICE_INT_CODE Register

7	6	5	4	3	2	1	0
DEV_INTR							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-212. MMCSD0_UHS2_DEVICE_INT_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEV_INTR	R	0h	UHS II Device Interrupt This register is effective when the MMCSD0_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. Host Controller holds an INT MSG packet per device. One of INT MSGs (Code length is 1 byte) up to 15 can be read from this register by selecting UHS-II Device Select (MMCSD0_UHS2_DEVICE_SELECT[3-0] DEV_SEL). The number of the registers to hold INT MSGs is determined by the MMCSD0_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization.

18.2.55 MMCS0_UHS2_SOFTWARE_RESET Register (Offset = C0h) [reset = 0h]

MMCS0_UHS2_SOFTWARE_RESET is shown in [Figure 18-84](#) and described in [Table 18-214](#).

Return to [Summary Table](#).

UHS-II Software Reset Register.

Table 18-213. MMCS0_UHS2_SOFTWARE_RESET Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00C0h

Figure 18-84. MMCS0_UHS2_SOFTWARE_RESET Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						HOST_SDTRAN_RESET	HOST_FULL_RESET
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-214. MMCS0_UHS2_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	HOST_SDTRAN_RESET	R/W	0h	<p>Host SD-TRAN Reset</p> <p>Host Driver set this bit to 1h to reset SD-TRAN layer when CMD0 is issued to Device or data transfer error occurs. This bit is cleared automatically at completion of SD-TRAN reset. If CMD0 is issued, SD-TRAN Initialization sequence from CMD8 is required to use UHS-II mode. Assuming that bus power is maintained and CM-TRAN Initialization is not required.</p> <p>Host Controller requires to do followings:</p> <ol style="list-style-type: none"> (1) SD Clock Enable is maintained (continue to provide RCLK). (2) All setting register is maintained. (3) Internal sequencers are reset to just after power on be able to issue a command. (4) All Interrupt Status, Status Enable and Signal Enable are cleared. (5) Data transfer is terminated and data in buffer is discarded. <p>0h: Not Affected 1h: Reset SD-TRAN</p>

Table 18-214. MMCSD0_UHS2_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HOST_FULL_RESET	R/W	0h	<p>Host Full Reset</p> <p>On issuing FULL_RESET CCMD, Host Driver set this bit to 1h to reset Host Controller. This bit is cleared automatically at completion of Host Controller reset. Initialization sequence from PHY Initialization is required to use UHS-II mode. Assuming that bus power is maintained.</p> <p>Host Controller requires to do followings:</p> <ul style="list-style-type: none"> (1) SD Clock Enable is cleared (internal Clock is still synchronized). (2) All setting register is cleared. (3) Internal sequencers are reset to just after power on. (4) All Interrupt Status, Status Enable and Signal Enable are cleared. <p>0h: Not Affected 1h: Reset Host Controller</p>

18.2.56 MMCS0_UHS2_TIMER_CONTROL Register (Offset = C2h) [reset = 0h]

MMCS0_UHS2_TIMER_CONTROL is shown in [Figure 18-85](#) and described in [Table 18-216](#).

Return to [Summary Table](#).

UHS-II Timeout Control Register.

Table 18-215. MMCS0_UHS2_TIMER_CONTROL Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00C2h

Figure 18-85. MMCS0_UHS2_TIMER_CONTROL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DEADLOCK_TIMEOUT_CTR				CMDRESP_TIMEOUT_CTR			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-216. MMCS0_UHS2_TIMER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-4	DEADLOCK_TIMEOUT_CTR	R/W	0h	Timeout Counter Value for Deadlock This value determines the deadlock period while host expecting to receive a packet (1 second). Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for Deadlock (in the MMCS0_UHS2_ERR_INTR_STS_ENA register). Fh: Reserved Eh: TMCLK x 2 ²⁷ 1h: TMCLK x 2 ¹⁴ 0h: TMCLK x 2 ¹³
3-0	CMDRESP_TIMEOUT_CTR	R/W	0h	Timeout Counter Value for CMD_RES This value determines the interval between command packet and response packet (5 ms). Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for CMD_RES (in the MMCS0_UHS2_ERR_INTR_STS_ENA register). Fh: Reserved Eh: TMCLK x 2 ²⁷ 1h: TMCLK x 2 ¹⁴ 0h: TMCLK x 2 ¹³

18.2.57 MMCS0_UHS2_ERR_INTR_STS Register (Offset = C4h) [reset = 0h]

MMCS0_UHS2_ERR_INTR_STS is shown in [Figure 18-86](#) and described in [Table 18-218](#).

Return to [Summary Table](#).

This register gives the status of all UHS-II interrupts.

Table 18-217. MMCS0_UHS2_ERR_INTR_STS Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00C4h

Figure 18-86. MMCS0_UHS2_ERR_INTR_STS Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC_ERR					RESERVED		
R/W1C-0h					R-0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W1C-0h	R-0h						R/W1C-0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-218. MMCS0_UHS2_ERR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC_ERR	R/W1C	0h	Vendor Specific Error Vendor may use this field for vendor specific error status. 0h: Interrupt is not generated 1h: Vendor Specific Error
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W1C	0h	Timeout for Deadlock Setting of this bit means that deadlock timeout occurs. Host expects to receive a packet but not received in a specified timeout (1 second). Timeout value is determined by the setting of the MMCS0_UHS2_TIMER_CONTROL[7-4] DEADLOCK_TIMEOUT_CTR bit field. 0h: Interrupt is not generated 1h: Deadlock Error

Table 18-218. MMCS0_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W1C	0h	Timeout for CMD_RES Setting of this bit means that RES Packet timeout occurs. Host expects to receive RES packet but not received in a specified timeout (5 ms). Timeout value is determined by the setting of the MMCS0_UHS2_TIMER_CONTROL[3-0] CMDRESP_TIMEOUT_CTR bit field. 0h: Interrupt is not generated 1h: RES Packet Timeout Error
15	ADMA2_ADMA3	R/W1C	0h	ADMA2/3 Error Setting of this bit means that ADMA2/3 Error occurs in UHS-II mode. ADMA2/3 Error Status is indicated to the MMCS0_ADMA_ERR_STATUS register, which is defined in the Host spec 3.00. 0h: Interrupt is not generated 1h: ADMA2/3 Error
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W1C	0h	EBSY Error On receiving EBSY packet, if the packet indicates an error, this bit is set to 1h. Setting of this bit also sets Error Interrupt and Transfer Completer together in the MMCS0_NORMAL_INTR_STS register. This error check is effective for a command with setting the MMCS0_UHS2_XFER_MODE[14] EBSY_WAIT bit. 0h: Interrupt is not generated 1h: EBSY Error (Backend Error)
7	UNRECOVERABLE	R/W1C	0h	Unrecoverable Error Setting of this bit means that Unrecoverable Error is set in a packet from a device. 0h: Interrupt is not generated 1h: Device Unrecoverable Error
6	RESERVED	R	0h	Reserved
5	TID	R/W1C	0h	TID Error Setting of this bit means that TID Error occurs. 0h: Interrupt is not generated 1h: TID Error
4	FRAMING	R/W1C	0h	Framing Error Setting of this bit means that Framing Error occurs during a packet receiving. 0h: Interrupt is not generated 1h: Framing Error
3	CRC	R/W1C	0h	CRC Error Setting of this bit means that CRC Error occurs during a packet receiving. 0h: Interrupt is not generated 1h: CRC Error
2	RETRY_EXPIRED	R/W1C	0h	Retry Expired Setting of this bit means that Retry Counter Expired Error occurs during data transfer. If this bit is set, either Framing Error or CRC Error in this register shall be set. 0h: Interrupt is not generated 1h: Retry Expired Error

Table 18-218. MMCSD0_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESP_PKT	R/W1C	0h	<p>RES Packet Error</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If the MMCSD0_UHS2_XFER_MODE[7] RESP_ERR_CHK_ENA bit is set to 1h, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1h.</p> <p>0h: Interrupt is not generated 1h: RES Packet Error</p>
0	HEADER	R/W1C	0h	<p>Header Error</p> <p>Setting of this bit means that Header Error occurs in a received packet.</p> <p>0h: Interrupt is not generated 1h: Header Error</p>

18.2.58 MMCSDB0_UHS2_ERR_INTR_STS_ENA Register (Offset = C8h) [reset = 0h]

MMCSDB0_UHS2_ERR_INTR_STS_ENA is shown in [Figure 18-87](#) and described in [Table 18-220](#).

Return to [Summary Table](#).

This register is used to enable the MMCSDB0_UHS2_ERR_INTR_STS register fields.

Table 18-219. MMCSDB0_UHS2_ERR_INTR_STS_ENA Instances

Instance	Physical Address
MMCSDB0_CTL_CFG	04F8 00C8h

Figure 18-87. MMCSDB0_UHS2_ERR_INTR_STS_ENA Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC					RESERVED		
R/W-0h					R-0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TI MEOUT	CMD_RESP_TI MEOUT
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ADMA2_ADMA 3	RESERVED						EBSY
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
UNRECOVERA BLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIR ED	RESP_PKT	HEADER
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-220. MMCSDB0_UHS2_ERR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Setting this bit to 1h enables setting of Vendor Specific Error bit in the MMCSDB0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Timeout for Deadlock Setting this bit to 1h enables setting of Timeout for Dead lock bit in the MMCSDB0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
16	CMD_RESP_TIMEOUT	R/W	0h	Timeout for CMD_RES Setting this bit to 1h enables setting of Timeout for CMD_RES bit in the MMCSDB0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

Table 18-220. MMCSD0_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W	0h	ADMA2/3 Error Setting this bit to 1h enables setting of ADMA2/3 Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W	0h	EBSY Error Setting this bit to 1h enables setting of EBSY Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
7	UNRECOVERABLE	R/W	0h	Unrecoverable Error Setting this bit to 1h enables setting of Unrecoverable Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
6	RESERVED	R	0h	Reserved
5	TID	R/W	0h	TID Error Setting this bit to 1h enables setting of TID Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
4	FRAMING	R/W	0h	Framing Error Setting this bit to 1h enables setting of Framing Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
3	CRC	R/W	0h	CRC Error Setting this bit to 1h enables setting of CRC Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
2	RETRY_EXPIRED	R/W	0h	Retry Expired Setting this bit to 1h enables setting of Retry Expired bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
1	RESP_PKT	R/W	0h	RES Packet Error Setting this bit to 1h enables setting of RES Packet Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
0	HEADER	R/W	0h	Header Error Setting this bit to 1h enables setting of Header Error bit in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

18.2.59 MMCSDB0_UHS2_ERR_INTR_SIG_ENA Register (Offset = CCh) [reset = 0h]

MMCSDB0_UHS2_ERR_INTR_SIG_ENA is shown in Figure 18-88 and described in Table 18-222.

Return to [Summary Table](#).

This register is used to generate UHS-II Interrupt signals.

Table 18-221. MMCSDB0_UHS2_ERR_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSDB0_CTL_CFG	04F8 00CCh

Figure 18-88. MMCSDB0_UHS2_ERR_INTR_SIG_ENA Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC						RESERVED	
R/W-0h						R-0h	
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED_SIG_ENA	RESP_PKT	HEADER
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-222. MMCSDB0_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Setting of a bit to 1h in this field enables generating interrupt signal when correspondent bit of Vendor Specific Error is set in the MMCSDB0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Timeout for Deadlock Setting this bit to 1h enables generating interrupt signal when Timeout for Dead lock bit is set in the MMCSDB0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
16	CMD_RESP_TIMEOUT	R/W	0h	Timeout for CMD_RES Setting this bit to 1h enables generating interrupt signal when Timeout for CMD_RES bit is set in the MMCSDB0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

Table 18-222. MMCSD0_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W	0h	ADMA2/3 Error Setting this bit to 1h enables generating interrupt signal when ADMA2/3 Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W	0h	EBSY Error Setting this bit to 1h enables generating interrupt signal when EBSY Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
7	UNRECOVERABLE	R/W	0h	Unrecoverable Error Setting this bit to 1h enables generating interrupt signal when Unrecoverable Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
6	RESERVED	R	0h	Reserved
5	TID	R/W	0h	TID Error Setting this bit to 1h enables generating interrupt signal when TID Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
4	FRAMING	R/W	0h	Framing Error Setting this bit to 1h enables generating interrupt signal when Framing Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
3	CRC	R/W	0h	CRC Error Setting this bit to 1h enables generating interrupt signal when CRC Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
2	RETRY_EXPIRED_SIG_ENA	R/W	0h	Retry Expired Setting this bit to 1h enables generating interrupt signal when Retry Expired bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
1	RESP_PKT	R/W	0h	RES Packet Error Setting this bit to 1h enables generating interrupt signal when RES Packet Error bit is set in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

Table 18-222. MMCSDB_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HEADER	R/W	0h	Header Error Setting this bit to 1h enables generating interrupt signal when Header Error bit is set in the MMCSDB_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

18.2.60 MMCSD0_UHS2_SETTINGS_PTR Register (Offset = E0h) [reset = 100h]

MMCSD0_UHS2_SETTINGS_PTR is shown in [Figure 18-89](#) and described in [Table 18-224](#).

Return to [Summary Table](#).

This register is pointer for UHS-II settings.

Table 18-223. MMCSD0_UHS2_SETTINGS_PTR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 00E0h

Figure 18-89. MMCSD0_UHS2_SETTINGS_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_SETTINGS_PTR															
R-100h															

LEGEND: R = Read Only; -n = value after reset

Table 18-224. MMCSD0_UHS2_SETTINGS_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_SETTINGS_PTR	R	100h	Pointer for UHS-II Settings Register

18.2.61 MMCS0_UHS2_CAPABILITIES_PTR Register (Offset = E2h) [reset = 110h]

MMCS0_UHS2_CAPABILITIES_PTR is shown in [Figure 18-90](#) and described in [Table 18-226](#).

Return to [Summary Table](#).

This register is pointer for UHS-II Capabilities Register.

Table 18-225. MMCS0_UHS2_CAPABILITIES_PTR Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00E2h

Figure 18-90. MMCS0_UHS2_CAPABILITIES_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_CAPABILITIES_PTR															
R-110h															

LEGEND: R = Read Only; -n = value after reset

Table 18-226. MMCS0_UHS2_CAPABILITIES_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_CAPABILITIES_PTR	R	110h	Pointer for UHS-II Capabilities Register

18.2.62 MMCSD0_UHS2_TEST_PTR Register (Offset = E4h) [reset = 120h]

MMCSD0_UHS2_TEST_PTR is shown in [Figure 18-91](#) and described in [Table 18-228](#).

Return to [Summary Table](#).

This register is pointer for UHS-II Test Register.

Table 18-227. MMCSD0_UHS2_TEST_PTR Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 00E4h

Figure 18-91. MMCSD0_UHS2_TEST_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_TEST_PTR															
R-120h															

LEGEND: R = Read Only; -n = value after reset

Table 18-228. MMCSD0_UHS2_TEST_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_TEST_PTR	R	120h	Pointer for UHS-II Test Register

18.2.63 MMCS0_SHARED_BUS_CTRL_PTR Register (Offset = E6h) [reset = 130h]

MMCS0_SHARED_BUS_CTRL_PTR is shown in [Figure 18-92](#) and described in [Table 18-230](#).

Return to [Summary Table](#).

This register is pointer for UHS-II Shared Bus Control Register.

Table 18-229. MMCS0_SHARED_BUS_CTRL_PTR Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00E6h

Figure 18-92. MMCS0_SHARED_BUS_CTRL_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHARED_BUS_CTRL_PTR															
R-130h															

LEGEND: R = Read Only; -n = value after reset

Table 18-230. MMCS0_SHARED_BUS_CTRL_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SHARED_BUS_CTRL_PTR	R	130h	Pointer for Shared Bus Control Register

18.2.64 MMCSD0_VENDOR_SPECIFIC_PTR Register (Offset = E8h) [reset = 140h]

MMCSD0_VENDOR_SPECIFIC_PTR is shown in [Figure 18-93](#) and described in [Table 18-232](#).

Return to [Summary Table](#).

This register is pointer for UHS-II Vendor Specific Register.

**Table 18-231. MMCSD0_VENDOR_SPECIFIC_PTR
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 00E8h

Figure 18-93. MMCSD0_VENDOR_SPECIFIC_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR_SPECIFIC_PTR															
R-140h															

LEGEND: R = Read Only; -n = value after reset

Table 18-232. MMCSD0_VENDOR_SPECIFIC_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_SPECIFIC_PTR	R	140h	Pointer for Vendor Specific Area

18.2.65 MMCS0_BOOT_TIMEOUT_CONTROL Register (Offset = F4h) [reset = 0h]

MMCS0_BOOT_TIMEOUT_CONTROL is shown in [Figure 18-94](#) and described in [Table 18-234](#).

Return to [Summary Table](#).

This is used to program the boot timeout value counter.

Table 18-233. MMCS0_BOOT_TIMEOUT_CONTROL Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00F4h

Figure 18-94. MMCS0_BOOT_TIMEOUT_CONTROL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_TIMEOUT_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-234. MMCS0_BOOT_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_TIMEOUT_CNT	R/W	0h	Boot Data Timeout Counter Value This value determines the interval by which DAT line timeouts are detected during boot operation for eMMC4.4 card. The value is in number of SD clock.

18.2.66 MMCS0_VENDOR_REGISTER Register (Offset = F8h) [reset = 4E20h]

MMCS0_VENDOR_REGISTER is shown in [Figure 18-95](#) and described in [Table 18-236](#).

Return to [Summary Table](#).

Vendor register added for Auto Gate SD CLK, CMD11 Power Down Timer, Enhanced Strobe and eMMC Hardware Reset.

**Table 18-235. MMCS0_VENDOR_REGISTER
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00F8h

Figure 18-95. MMCS0_VENDOR_REGISTER Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							AUTOGATE_S DCLK
R-0h							R/W-0h
15	14	13	12	11	10	9	8
CMD11_PD_TIMER							
R/W-1388h							
7	6	5	4	3	2	1	0
CMD11_PD_TIMER						EMMC_HW_RE SET	ENHANCED_S STROBE
R/W-1388h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-236. MMCS0_VENDOR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	AUTOGATE_SDCLK	R/W	0h	Auto Gate SD CLK If this bit is set, SD CLK will be gated automatically when there is no transfer. This is applicable only for Embedded Device. 0h: Disable 1h: Enable
15-2	CMD11_PD_TIMER	R/W	1388h	CMD11 Power Down Timer Value
1	EMMC_HW_RESET	R/W	0h	eMMC Hardware Reset Hardware reset signal is generated for eMMC card when this bit is set. 0h: De-assert hardware reset pin 1h: Drives the hardware reset pin as ZERO (Active LOW to eMMC card)
0	ENHANCED_STROBE	R/W	0h	Enhanced Strobe This bit enables the enhanced strobe logic of the Host Controller.

18.2.67 MMCS0_SLOT_INT_STS Register (Offset = FCh) [reset = 0h]

MMCS0_SLOT_INT_STS is shown in [Figure 18-96](#) and described in [Table 18-238](#).

Return to [Summary Table](#).

This register is used to read the interrupt signal for each slot.

Table 18-237. MMCS0_SLOT_INT_STS Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00FCh

Figure 18-96. MMCS0_SLOT_INT_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INTR_SIG							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-238. MMCS0_SLOT_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	INTR_SIG	R	0h	Interrupt Signal for Slot#0 These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

18.2.68 MMCS0_HOST_CONTROLLER_VER Register (Offset = FEh) [reset = 1004h]

MMCS0_HOST_CONTROLLER_VER is shown in [Figure 18-97](#) and described in [Table 18-240](#).

Return to [Summary Table](#).

This register is used to read the vendor version number and specification version number.

**Table 18-239. MMCS0_HOST_CONTROLLER_VER
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 00FEh

Figure 18-97. MMCS0_HOST_CONTROLLER_VER Register

15	14	13	12	11	10	9	8
VEN_VER_NUM							
R-10h							
7	6	5	4	3	2	1	0
SPEC_VER_NUM							
R-4h							

LEGEND: R = Read Only; -n = value after reset

Table 18-240. MMCS0_HOST_CONTROLLER_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	VEN_VER_NUM	R	10h	Vendor Version Number The Vendor Version Number is set to 10h (1.0)
7-0	SPEC_VER_NUM	R	4h	Specification Version Number This status indicates the Host Controller Specification Version. The upper and lower 4-bits indicate the version. 0h: SD Host Controller Specification Version 1.00 1h: SD Host Controller Specification Version 2.00 Including the feature of the ADMA and Test Register 2h: SD Host Controller Specification Version 3.00 3h: SD Host Controller Specification Version 4.00 4h: SD Host Controller Specification Version 4.10 Others: Reserved

18.2.69 MMCS0_UHS2_GEN_SETTINGS Register (Offset = 100h) [reset = 0h]

MMCS0_UHS2_GEN_SETTINGS is shown in [Figure 18-98](#) and described in [Table 18-242](#).

Return to [Summary Table](#).

Start Address of General settings is pointed by the MMCS0_UHS2_SETTINGS_PTR Register.

Table 18-241. MMCS0_UHS2_GEN_SETTINGS Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0100h

Figure 18-98. MMCS0_UHS2_GEN_SETTINGS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		NUMLANES					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED							POWER_MODE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-242. MMCS0_UHS2_GEN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	NUMLANES	R/W	0h	Number of Lanes and Functionalities The lane configuration of a Host System is set to this field depends on the capability among Host Controller and connected devices. 2 Lanes FD mode is mandatory and the others modes are optional. 0h: 2 Lanes FD or 2L-HD 1h: Not Used 2h: 3 Lanes 2D1U-FD (Embedded) 3h: 3 Lanes 1D2U-FD (Embedded) 4h: 4 Lanes 2D2U-FD (Embedded) Others: Reserved
7-1	RESERVED	R	0h	Reserved
0	POWER_MODE	R/W	0h	Power Mode This field determines either Fast mode or Low Power mode. Host and all devices connected to the host shall be set to the same mode. 0h: Fast Mode 1h: Low Power Mode

18.2.70 MMCSD0_UHS2_PHY_SETTINGS Register (Offset = 104h) [reset = 0h]

MMCSD0_UHS2_PHY_SETTINGS is shown in [Figure 18-99](#) and described in [Table 18-244](#).

Return to [Summary Table](#).

Start Address of PHY settings is pointed by the MMCSD0_UHS2_SETTINGS_PTR Register.

**Table 18-243. MMCSD0_UHS2_PHY_SETTINGS
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0104h

Figure 18-99. MMCSD0_UHS2_PHY_SETTINGS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
N_LSS_DIR				N_LSS_SYN			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
HIBERNATE_E NA	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
SPEED_RANGE		RESERVED					
R/W-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-244. MMCSD0_UHS2_PHY_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	N_LSS_DIR	R/W	0h	Host N_LSS_DIR The largest value of N_LSS_DIR capabilities among the Host Controller and Connected Devices is set to this field. 0h: 8 x 16 LSS 1h: 8 x 1 LSS 2h: 8 x 2 LSS 3h: 8 x 3 LSS Fh: 8 x 15 LSS
19-16	N_LSS_SYN	R/W	0h	Host N_LSS_SYN The largest value of N_LSS_SYN capabilities among the Host Controller and Connected Devices is set to this field. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h - 4 x 3 LSS Fh: 4 x 15 LSS

Table 18-244. MMCSDB_UHS2_PHY_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	HIBERNATE_ENA	R/W	0h	<p>Hibernate Enable</p> <p>After checking card capability of Hibernate mode, if all devices support Hibernate mode, this bit may be set. This bit determines whether Host remains in Dormant state or goes to Hibernate state. In Hibernate mode, VDD1 Power may be off.</p> <p>0h: Hibernate Disabled 1h: Hibernate Enabled</p>
14-8	RESERVED	R	0h	Reserved
7-6	SPEED_RANGE	R/W	0h	<p>Speed Range</p> <p>PLL multiplier is selected by this field. Change of PLL Multiplier is not effective immediately and is applied from exiting Dormant State.</p> <p>0h: Range A (Default) 1h: Range B 2h: Reserved 3h: Reserved</p>
5-0	RESERVED	R	0h	Reserved

18.2.71 MMCSD0_UHS2_LNK_TRN_SETTINGS Register (Offset = 108h) [reset = 0h]

MMCSD0_UHS2_LNK_TRN_SETTINGS is shown in [Figure 18-100](#) and described in [Table 18-246](#).

Return to [Summary Table](#).

Start Address of LINK/TRAN settings is pointed by the MMCSD0_UHS2_SETTINGS_PTR Register.

Table 18-245. MMCSD0_UHS2_LNK_TRN_SETTINGS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0108h

Figure 18-100. MMCSD0_UHS2_LNK_TRN_SETTINGS Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
N_DATA_GAP							
R/W-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						RETRY_COUNT	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
HOST_NFCU							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-246. MMCSD0_UHS2_LNK_TRN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved

Table 18-246. MMCS0_UHS2_LNK_TRN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39-32	N_DATA_GAP	R/W	0h	Host N_DATA_GAP The largest value of N_DATA_GAP capabilities among the Host Controller and Connected Devices is set to this field. 00h: No Gap 01h: 1 LSS 02h: 2 LSS 03h: 3 LSS FFh: 255 LSS
31-18	RESERVED	R	0h	Reserved
17-16	RETRY_COUNT	R/W	0h	Retry Count Data Burst retry count is set to this field. 00h: Retry Disabled 01h: 1 time 02h: 2 times 03h: 3 times
15-8	HOST_NFCU	R/W	0h	Host N_FCU Host Driver sets the number of blocks in Data Burst (Flow Control) to this field. The value shall be smaller than or equal to N_FCU capabilities among the Host Controller and connected card and devices. Setting 1 to 4 blocks is recommended considering buffer size. 00h: 256 Blocks 01h: 1 Block 02h: 2 Blocks 03h: 3 Blocks FFh: 255 Blocks
7-0	RESERVED	R	0h	Reserved

18.2.72 MMCS0_UHS2_GEN_CAP Register (Offset = 110h) [reset = 44F11h]

MMCS0_UHS2_GEN_CAP is shown in [Figure 18-101](#) and described in [Table 18-248](#).

Return to [Summary Table](#).

Start Address of General Capabilities is pointed by the MMCS0_UHS2_GEN_CAP Register.

Table 18-247. MMCS0_UHS2_GEN_CAP Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0110h

Figure 18-101. MMCS0_UHS2_GEN_CAP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
CORECFG_UHS2_BUS_TOPOLOGY		CORECFG_UHS2_MAX_DEVICES				DEVICE_TYPE	
R-0h		R-1h				R-0h	
15	14	13	12	11	10	9	8
RESERVED	CFG_64BIT_ADDRESSING	NUM_LANES					
R-0h		R-1h		R-Fh			
7	6	5	4	3	2	1	0
GAP				DAP			
R-1h				R-1h			

LEGEND: R = Read Only; -n = value after reset

Table 18-248. MMCS0_UHS2_GEN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-22	CORECFG_UHS2_BUS_TOPOLOGY	R	0h	Bus Topology This field indicates one of bus topologies configured by a Host system. 0h: P2P Connection 1h: Ring Connection 2h: HUB Connection 3h: HUB is Connected in Ring
21-18	CORECFG_UHS2_MAX_DEVICES	R	1h	Number of Devices Supported This field indicates the maximum number of devices supported by the Host Controller. 0h: Not used 1h: 1 Devices 2h: 2 Devices Fh: 15 Devices
17-16	DEVICE_TYPE	R	0h	Removable/Embedded This field indicates device type configured by a Host system. 0h: Removable Card (P2P) 1h: Embedded Devices 2h: Embedded Devices + Removable Card 3h: Reserved

Table 18-248. MMCS0_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14	CFG_64BIT_ADDRESSING	R	1h	64-bit Addressing This field indicates support of 64-bit addressing by the Host Controller. 0h: 32-bit Addressing is supported 1h: 32-bit and 64-bit Addressing is supported
13-8	NUM_LANES	R	Fh	Number of Lanes and Functionalities This field indicates support of lanes by the Host Controller. 0 mean not supported and 1 means supported. D08: 2L-HD D09: 2D1U-FD D10: 1D2U-FD D11: 2D2U-FD D12: Reserved D13: Reserved
7-4	GAP	R	1h	GAP (Group Allocation Power) This field indicates the maximum capability of host power supply for a group configured by a Host system. This field is used to set the argument of DEVICE_INIT CCM. 0h: Not used 1h: 360 mW 2h: 720 mW Fh: 360 x 15 mW
3-0	DAP	R	1h	DAP (Device Allocation Power) This field indicates the maximum capability of host power supply for a device configured by a Host system. This field is used to set the argument of DEVICE_INIT CCMD. 0h: 360 mW (Default) 1h: 360 mW 2h: 720 mW Fh: 360 x 15 mW

18.2.73 MMCS0_UHS2_PHY_CAP Register (Offset = 114h) [reset = 110000h]

MMCS0_UHS2_PHY_CAP is shown in [Figure 18-102](#) and described in [Table 18-250](#).

Return to [Summary Table](#).

Start Address of PHY Capabilities is pointed by the MMCS0_UHS2_CAPABILITIES_PTR Register.

Table 18-249. MMCS0_UHS2_PHY_CAP Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0114h

Figure 18-102. MMCS0_UHS2_PHY_CAP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
N_LSS_DIR				N_LSS_SYN			
R-1h				R-1h			
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SPEED_RANGE		RESERVED					
R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-250. MMCS0_UHS2_PHY_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	N_LSS_DIR	R	1h	Host N_LSS_DIR This field indicates the minimum N_LSS_DIR required by the Host Controller. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h: 4 x 3 LSS Fh: 4 x 15 LSS
19-16	N_LSS_SYN	R	1h	Host N_LSS_SYN This field indicates the minimum N_LSS_SYN required by the Host Controller. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h: 4 x 3 LSS Fh: 4 x 15 LSS
15-8	RESERVED	R	0h	Reserved

Table 18-250. MMCS0_UHS2_PHY_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	SPEED_RANGE	R	0h	Speed Range This field indicates supported Speed Range by the Host Controller. 0h: Range A (Default) 1h: Range A and Range B 2h: Reserved 3h: Reserved
5-0	RESERVED	R	0h	Reserved

18.2.74 MMCS0_UHS2_LNK_TRN_CAP Register (Offset = 118h) [reset = 8120000100h]

MMCS0_UHS2_LNK_TRN_CAP is shown in [Figure 18-103](#) and described in [Table 18-252](#).

Return to [Summary Table](#).

Start Address of LINK/TRAN settings is pointed by the MMCS0_UHS2_CAPABILITIES_PTR Register.

Table 18-251. MMCS0_UHS2_LNK_TRN_CAP Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0118h

Figure 18-103. MMCS0_UHS2_LNK_TRN_CAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-0h															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED								N_DATA_GAP							
R-0h								R-81h							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_BLK_LENGTH												RESERVED			
R-200h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N_FCU								RESERVED							
R-1h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-252. MMCS0_UHS2_LNK_TRN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39-32	N_DATA_GAP	R	81h	Host N_DATA_GAP This field indicates the minimum number of data gap (DIDL) supported by the Host Controller. 00h: No Gap 01h: 1 LSS 02h: 2 LSS 03h: 3 LSS FFh: 255 LSS
31-20	MAX_BLK_LENGTH	R	200h	Host Maximum Block Length This field indicates maximum block length by the Host Controller. 000h: Not Used 001h: 1 byte 002h: 2 bytes 200h: 512 bytes 800h: 2048 bytes 801h - FFFh: Not Used
19-16	RESERVED	R	0h	Reserved

Table 18-252. MMCS0_UHS2_LNK_TRN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	N_FCU	R	1h	Host N_FCU This field indicates maximum the number of blocks in a Flow Control unit by the Host Controller. This value is determined by supported buffer size. 00h: 256 Blocks 01h: 1 Block 02h: 2 Block 03h: 3 Block FFh: 255 Blocks
7-0	RESERVED	R	0h	Reserved

18.2.75 MMCSD0_FORCE_UHSII_ERR_INT_STS Register (Offset = 120h) [reset = 0h]

MMCSD0_FORCE_UHSII_ERR_INT_STS is shown in [Figure 18-104](#) and described in [Table 18-254](#).

Return to [Summary Table](#).

This register is not physically implemented, rather it is an address where the MMCSD0_UHS2_ERR_INTR_STS register can be written.

Table 18-253.
MMCSD0_FORCE_UHSII_ERR_INT_STS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0120h

Figure 18-104. MMCSD0_FORCE_UHSII_ERR_INT_STS Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC						RESERVED	
W-0h						R-0h	
23	22	21	20	19	18	17	16
RESERVED						TIMEOUT_DEADLOCK	TIMEOUT_CMD_RES
R-0h						W-0h	W-0h
15	14	13	12	11	10	9	8
ADMA	RESERVED						EBSY
W-0h	R-0h						W-0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RES_PKT	HEADER
W-0h	R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 18-254. MMCSD0_FORCE_UHSII_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC	W	0h	Force Event for Vendor Specific Error 0h: Not Affected 1h: Vendor Specific Error Status is set
26-18	RESERVED	R	0h	Reserved
17	TIMEOUT_DEADLOCK	W	0h	Force Event for Timeout for Deadlock Setting this bit forces the Host Controller to set Timeout for Deadlock in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Timeout for Deadlock Error status is set
16	TIMEOUT_CMD_RES	W	0h	Force Event for Timeout for CMD_RES Setting this bit forces the Host Controller to set Timeout for CMD_RES in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Timeout for CMD_RES Status is set
15	ADMA	W	0h	Force Event for ADMA Error Setting this bit forces the Host Controller to set ADMA Error in the MMCSD0_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: ADMA Error Status is set

Table 18-254. MMCS0_FORCE_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-9	RESERVED	R	0h	Reserved
8	EBSY	W	0h	Force Event for EBSY Error Setting this bit forces the Host Controller to set EBSY Error in the MMCS0_FORCE_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: EBSY Error Status is set
7	UNRECOVERABLE	W	0h	Force Event for Unrecoverable Error Setting this bit forces the Host Controller to set Unrecoverable Error in the MMCS0_FORCE_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Unrecoverable Error Status is set
6	RESERVED	R	0h	Reserved
5	TID	W	0h	Force Event for TID Error Setting this bit forces the Host Controller to set TID Error in the MMCS0_FORCE_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: TID Error Status is set
4	FRAMING	W	0h	Force Event for Framing Error Setting this bit forces the Host Controller to set Framing Error in the MMCS0_FORCE_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Framing Error Status is set
3	CRC	W	0h	Force Event for CRC Error Setting this bit forces the Host Controller to set CRC Error in the MMCS0_FORCE_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: CRC Error Status is set
2	RETRY_EXPIRED	W	0h	Force Event for Retry Expired Setting this bit forces the Host Controller to set Retry Expired in the MMCS0_FORCE_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Retry expired error status is set
1	RES_PKT	W	0h	Force Event for RES Packet Error Setting this bit forces the Host Controller to set RES Packet Error in the MMCS0_FORCE_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: RES packet error status is set
0	HEADER	W	0h	Force Event for Header Error Setting this bit forces the Host Controller to set Header Error in the MMCS0_FORCE_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Header error status is set

18.2.76 MMCSD0_CQ_VERSION Register (Offset = 200h) [reset = 510h]

MMCSD0_CQ_VERSION is shown in [Figure 18-105](#) and described in [Table 18-256](#).

Return to [Summary Table](#).

This register provides information about the version of the eMMC CQ (Command Queueing) standard which is 285 implemented by the CQE, in BCD format. The current version is rev 5.1.

The following table describes the CQBASE+00h: Command Queueing Version.

Table 18-255. MMCSD0_CQ_VERSION Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0200h

Figure 18-105. MMCSD0_CQ_VERSION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				EMMC_MAJOR_VER_NUM			
R-0h				R-5h			
7	6	5	4	3	2	1	0
EMMC_MINOR_VER_NUM				EMMC_VERSION_SUFFIX			
R-1h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 18-256. MMCSD0_CQ_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	EMMC_MAJOR_VER_NUM	R	5h	eMMC Major Version Number (digit left of decimal point), in BCD format
7-4	EMMC_MINOR_VER_NUM	R	1h	eMMC Minor Version Number (digit right of decimal point), in BCD format
3-0	EMMC_VERSION_SUFFIX	R	0h	eMMC Version Suffix (2nd digit right of decimal point), in BCD format

18.2.77 MMCS0_CQ_CAPABILITIES Register (Offset = 204h) [reset = 30C8h]

MMCS0_CQ_CAPABILITIES is shown in [Figure 18-106](#) and described in [Table 18-258](#).

Return to [Summary Table](#).

This register is reserved for capability indication.

**Table 18-257. MMCS0_CQ_CAPABILITIES
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0204h

Figure 18-106. MMCS0_CQ_CAPABILITIES Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CF_MUL				RESERVED		CF_VAL	
R-3h				R-0h		R-C8h	
7	6	5	4	3	2	1	0
CF_VAL							
R-C8h							

LEGEND: R = Read Only; -n = value after reset

Table 18-258. MMCS0_CQ_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	CF_MUL	R	3h	Internal Timer Clock Frequency Multiplier (ITCFMUL) ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details (MMCS0_CQ_CAPABILITIES[9-0] CF_VAL). Field Value Description: 0h: 0.001 MHz 1h: 0.01 MHz 2h: 0.1 MHz 3h: 1 MHz 4h: 10 MHz Other values are reserved
11-10	RESERVED	R	0h	Reserved
9-0	CF_VAL	R	C8h	Internal Timer Clock Frequency Value (ITCFVAL) ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the polling period when using periodic SEND_QUEUE_STATUS (CMD13) polling. The clock frequency is calculated as ITCFVAL × ITCFMUL. For example, to encode 19.2 MHz ITCFVAL shall be C0h (= 192 decimal) and ITCFMUL shall be 2h (0.1 MHz). 192 × 0.1 MHz = 19.2 MHz

18.2.78 MMCSD0_CQ_CONFIG Register (Offset = 208h) [reset = 0h]

MMCSD0_CQ_CONFIG is shown in [Figure 18-107](#) and described in [Table 18-260](#).

Return to [Summary Table](#).

This register controls CQE behavior affecting the general operation of command queueing 290 module or operation of multiple tasks in the same time.

Table 18-259. MMCSD0_CQ_CONFIG Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0208h

Figure 18-107. MMCSD0_CQ_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			DCMD_ENA	RESERVED			TASK_DESC_SIZE
R-0h			R/W-0h	R-0h			R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CQ_ENABLE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-260. MMCSD0_CQ_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	DCMD_ENA	R/W	0h	Direct Command (DCMD) Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 0h: Task descriptor in slot #31 is a Data Transfer Task Descriptor 1h: Task descriptor in slot #31 is a DCMD Task Descriptor
11-9	RESERVED	R	0h	Reserved
8	TASK_DESC_SIZE	R/W	0h	Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits . This bit can only be configured when the MMCSD0_CQ_CONFIG[0] CQ_ENABLE bit is 0hh (command queueing is disabled). Bit Value Description 0h: Task descriptor size is 64 bits 1h: Task descriptor size is 128 bits
7-1	RESERVED	R	0h	Reserved

Table 18-260. MMCS0_CQ_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CQ_ENABLE	R/W	0h	<p>Command Queueing Enable</p> <p>Software shall write 1h to this bit when in order to enable command queueing mode (enable CQE).</p> <p>When this bit is 0h, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller.</p> <p>Before software writes 1h to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing.</p> <p>When software wants to exit command queueing mode, it shall clear all previous tasks if such exist before setting this bit to 0h.</p>

18.2.79 MMCS0_CQ_CONTROL Register (Offset = 20Ch) [reset = 0h]

MMCS0_CQ_CONTROL is shown in [Figure 18-108](#) and described in [Table 18-262](#).

Return to [Summary Table](#).

This register controls CQE behavior affecting the general operation of command queueing 293 module or operation of multiple tasks in the same time.

Table 18-261. MMCS0_CQ_CONTROL Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 020Ch

Figure 18-108. MMCS0_CQ_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CLEAR_ALL_TASKS
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							HALT_BIT
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-262. MMCS0_CQ_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CLEAR_ALL_TASKS	R/W	0h	<p>Clear All Tasks</p> <p>Software shall write 1h to this bit when it wants to clear all the tasks sent to the device.</p> <p>This bit can only be written when CQE is in halt state (Halt bit is 1h). When software writes 1h, the value of the register is updated to 1h, and CQE shall reset the MMCS0_CQ_TASK_DOOR_BELL register and all other context information for all unfinished tasks. Then CQE will clear this bit.</p> <p>Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit.</p> <p>CQE does not communicate to the device that the tasks were cleared. It is softwares responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0h to this register shall have no effect.</p>
7-1	RESERVED	R	0h	Reserved

Table 18-262. MMCS0_CQ_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_BIT	R/W	0h	<p>Halt</p> <p>Host software shall write 1h to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus.</p> <p>For example, issuing a Discard Task command (CMDQ_TASK_MGMT).</p> <p>When software writes 1h, CQE shall complete the ongoing task if such a task is in progress.</p> <p>Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1h.</p> <p>Software may poll on this bit until it is set to 1h, and may only then send commands on the eMMC bus.</p> <p>In order to exit halt state (resume CQE activity), software shall clear this bit (write 0h). Writing 0h when the value is already 0h shall have no effect.</p>

18.2.80 MMCS0_CQ_INTR_STS Register (Offset = 210h) [reset = 0h]

MMCS0_CQ_INTR_STS is shown in [Figure 18-109](#) and described in [Table 18-264](#).

Return to [Summary Table](#).

This register indicates pending interrupts that require service. Each bit in this registers is asserted 296 in response a specific event, only if the respective bit is set in the MMCS0_CQ_INTR_STS_ENA register.

Table 18-263. MMCS0_CQ_INTR_STS Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0210h

Figure 18-109. MMCS0_CQ_INTR_STS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARE D	RESP_ERR_D ET	TASK_COMPL ETE	HALT_COMPL ETE
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-264. MMCS0_CQ_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W1C	0h	Task Error Interrupt (TERR) This bit is asserted when task error is detected due to invalid task descriptor.
3	TASK_CLEARED	R/W1C	0h	Task Cleared (TCL) This status bit is asserted (if MMCS0_CQ_INTR_STS_ENA[3] TASK_CLEARED = 1h) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (MMCS0_CQ_TASK_CLEAR) or clearing of all tasks (MMCS0_CQ_CONTROL).
2	RESP_ERR_DET	R/W1C	0h	Response Error Detected Interrupt (RED) This status bit is asserted (if MMCS0_CQ_INTR_STS_ENA[2] RESP_ERR_DET = 1h) when a response is received with an error bit set in the device status field. Software uses the MMCS0_CQ_RESP_ERR_MASK register to configure which device status bit fields may trigger an interrupt, and which are masked.

Table 18-264. MMCS0_CQ_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TASK_COMPLETE	R/W1C	0h	Task Complete Interrupt (TCC) This status bit is asserted (if MMCS0_CQ_INTR_STS_ENA[1] TASK_COMPLETE = 1h) when at least one of the following two conditions are met: (1) A task is completed and the INT bit is set in its Task Descriptor (2) Interrupt caused by Interrupt Coalescing logic
0	HALT_COMPLETE	R/W1C	0h	Halt Complete Interrupt (HAC) This status bit is asserted (if MMCS0_CQ_INTR_STS_ENA[0] HALT_COMPLETE = 1h) when the MMCS0_CQ_CONTROL[0] HALT_BIT bit transitions from 0h to 1h indicating that host controller has completed its current ongoing task and has entered halt state.

18.2.81 MMCS0_CQ_INTR_STS_ENA Register (Offset = 214h) [reset = 0h]

MMCS0_CQ_INTR_STS_ENA is shown in [Figure 18-110](#) and described in [Table 18-266](#).

Return to [Summary Table](#).

This register enables and disables the reporting of the corresponding interrupt to host software in 299 MMCS0_CQ_INTR_STS register. When a bit is set (1h) and the corresponding interrupt condition is active, then the 300 bit in the MMCS0_CQ_INTR_STS register is asserted. Interrupt sources that are disabled (0h) are not indicated in the MMCS0_CQ_INTR_STS 301 register. This register is bit-index matched to the MMCS0_CQ_INTR_STS register.

Table 18-265. MMCS0_CQ_INTR_STS_ENA Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0214h

Figure 18-110. MMCS0_CQ_INTR_STS_ENA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-266. MMCS0_CQ_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Status Enable (TERR) 1h: MMCS0_CQ_INTR_STS[4] TASK_ERROR bit will be set when its interrupt condition is active 0h: MMCS0_CQ_INTR_STS[4] TASK_ERROR bit is disabled
3	TASK_CLEARED	R/W	0h	Task Cleared Status Enable (TCL) 1h: MMCS0_CQ_INTR_STS[3] TASK_CLEARED bit will be set when its interrupt condition is active 0h: MMCS0_CQ_INTR_STS[3] TASK_CLEARED bit is disabled
2	RESP_ERR_DET	R/W	0h	Response Error Detected Status Enable (RED) 1h: MMCS0_CQ_INTR_STS[2] RESP_ERR_DET bit will be set when its interrupt condition is active 0h: MMCS0_CQ_INTR_STS[2] RESP_ERR_DET bit is disabled
1	TASK_COMPLETE	R/W	0h	Task Complete Status Enable (TCC) 1h: MMCS0_CQ_INTR_STS[1] TASK_COMPLETE bit will be set when its interrupt condition is active 0h: MMCS0_CQ_INTR_STS[1] TASK_COMPLETE bit is disabled

Table 18-266. MMCS0_CQ_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_COMPLETE	R/W	0h	Halt Complete Status Enable (HAC) 1h: MMCS0_CQ_INTR_STS[0] HALT_COMPLETE bit will be set when its interrupt condition is active 0h: MMCS0_CQ_INTR_STS[0] HALT_COMPLETE bit is disabled

18.2.82 MMCS0_CQ_INTR_SIG_ENA Register (Offset = 218h) [reset = 0h]

MMCS0_CQ_INTR_SIG_ENA is shown in [Figure 18-111](#) and described in [Table 18-268](#).

Return to [Summary Table](#).

This register enables and disables the generation of interrupts to host software. When a bit is set 304 (1h) and the corresponding bit in the MMCS0_CQ_INTR_STS register is set, then an interrupt is generated. Interrupt sources 305 that are disabled (0h) are still indicated in the MMCS0_CQ_INTR_STS register. This register is bit-index matched 306 to the MMCS0_CQ_INTR_STS register.

Table 18-267. MMCS0_CQ_INTR_SIG_ENA Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0218h

Figure 18-111. MMCS0_CQ_INTR_SIG_ENA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-268. MMCS0_CQ_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Signal Enable (TERR) When set and the MMCS0_CQ_INTR_STS[4] TASK_ERROR bit is asserted, the CQE shall generate an interrupt.
3	TASK_CLEARED	R/W	0h	Task Cleared Signal Enable (TCL) When set and the MMCS0_CQ_INTR_STS[3] TASK_CLEARED bit is asserted, the CQE shall generate an interrupt.
2	RESP_ERR_DET	R/W	0h	Response Error Detected Signal Enable (RED) When set and the MMCS0_CQ_INTR_STS[2] RESP_ERR_DET bit is asserted, the CQE shall generate an interrupt.
1	TASK_COMPLETE	R/W	0h	Task Complete Signal Enable (TCC) When set and the MMCS0_CQ_INTR_STS[1] TASK_COMPLETE bit is asserted, the CQE shall generate an interrupt.
0	HALT_COMPLETE	R/W	0h	Halt Complete Signal Enable (HAC) When set and the MMCS0_CQ_INTR_STS[0] HALT_COMPLETE bit is asserted, the CQE shall generate an interrupt.

18.2.83 MMCS0_CQ_INTR_COALESCING Register (Offset = 21Ch) [reset = 0h]

MMCS0_CQ_INTR_COALESCING is shown in [Figure 18-112](#) and described in [Table 18-270](#).

Return to [Summary Table](#).

This register controls the interrupt coalescing feature.

Table 18-269. MMCS0_CQ_INTR_COALESCING Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 021Ch

Figure 18-112. MMCS0_CQ_INTR_COALESCING Register

31	30	29	28	27	26	25	24
CQINTCOALESC_ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED			IC_STATUS	RESERVED			
R-0h			R-0h	R-0h			
15	14	13	12	11	10	9	8
RESERVED			CTR_THRESHOLD				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED	TIMEOUT_VAL						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-270. MMCS0_CQ_INTR_COALESCING Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CQINTCOALESC_ENABLE	R/W	0h	Interrupt Coalescing Enable/Disable: When set to 0h by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT = 1 in the Task Descriptor. When set to 1h, the interrupt coalescing mechanism is enabled and coalesced interrupts are generated.
30-21	RESERVED	R	0h	Reserved
20	IC_STATUS	R	0h	Interrupt Coalescing Status Bit (ICSB): This bit indicates to software whether any tasks (with INT = 0) have completed and counted towards interrupt coalescing (ICSB is set if and only if IC counter > 0). Bit Value Description 0h: No task completions have occurred since last counter reset (IC counter = 0) 1h: At least one task completion has been counted (IC counter > 0)
19-13	RESERVED	R	0h	Reserved

Table 18-270. MMCS0_CQ_INTR_COALESCING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	CTR_THRESHOLD	R/W	0h	<p>Interrupt Coalescing Counter Threshold (ICCTH): Software uses this field to configure the number of task completions (only tasks with INT = 0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT = 0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31. Note: When ICCTH is 0h, task completions are not counted, and counting-based interrupts are not generated.</p>
7	RESERVED	R	0h	Reserved
6-0	TIMEOUT_VAL	R/W	0h	<p>Interrupt Coalescing Timeout Value (ICTOVAL): Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT = 0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timers unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field in the MMCS0_CQ_CAPABILITIES register. The minimum value is 1h (1024 clock periods) and the maximum value is 7Fh (127 × 1024 clock periods). For example, a MMCS0_CQ_CAPABILITIES field value of 0h indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is 16 × 1024 × 52.08 ns = 853.33 μs Note: When ICTOVAL is 0h, the timer is not running, and timer-based interrupts are not generated.</p>

18.2.84 MMCS0_CQ_TDL_BASE_ADDR Register (Offset = 220h) [reset = 0h]

MMCS0_CQ_TDL_BASE_ADDR is shown in [Figure 18-113](#) and described in [Table 18-272](#).

Return to [Summary Table](#).

This register is used for configuring the lower 32 bits of the byte address of the head of the Task 312 Descriptor List in the host memory.

Table 18-271. MMCS0_CQ_TDL_BASE_ADDR Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0220h

Figure 18-113. MMCS0_CQ_TDL_BASE_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQ_TDLBA_LO																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-272. MMCS0_CQ_TDL_BASE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQ_TDLBA_LO	R/W	0h	Task Descriptor List Base Address (TDLBA) This register stores the LSB bits (bits 31-0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is $32 \times (\text{Task Descriptor size} + \text{Transfer Descriptor size})$ as configured by Host driver. This address shall be set on Byte1 KByte boundary. The lower 10 bits of this register shall be set to 0h by software and shall be ignored by CQE.

18.2.85 MMCSO_CQ_TDL_BASE_ADDR_UPBITS Register (Offset = 224h) [reset = 0h]

MMCSO_CQ_TDL_BASE_ADDR_UPBITS is shown in [Figure 18-114](#) and described in [Table 18-274](#).

Return to [Summary Table](#).

This register is used for configuring the upper 32 bits of the byte address of the head of the Task 316 Descriptor List in the host memory.

Table 18-273.
MMCSO_CQ_TDL_BASE_ADDR_UPBITS Instances

Instance	Physical Address
MMCSO_CTL_CFG	04F8 0224h

Figure 18-114. MMCSO_CQ_TDL_BASE_ADDR_UPBITS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQ_TDLBA_HI																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-274. MMCSO_CQ_TDL_BASE_ADDR_UPBITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQ_TDLBA_HI	R/W	0h	Task Descriptor List Base Address (TDLBA) This register stores the MSB bits (bits 63-32) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is $32 \times (\text{Task Descriptor size} + \text{Transfer Descriptor size})$ as configured by Host driver. This register is reserved when using 32-bit addressing mode.

18.2.86 MMCS0_CQ_TASK_DOOR_BELL Register (Offset = 228h) [reset = 0h]

MMCS0_CQ_TASK_DOOR_BELL is shown in [Figure 18-115](#) and described in [Table 18-276](#).

Return to [Summary Table](#).

Using this register, software triggers CQE to process a new task.

Table 18-275. MMCS0_CQ_TASK_DOOR_BELL Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0228h

Figure 18-115. MMCS0_CQ_TASK_DOOR_BELL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTDB_VAL																															
W1S-0h																															

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 18-276. MMCS0_CQ_TASK_DOOR_BELL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTDB_VAL	W1S	0h	<p>Command Queueing Task Doorbell</p> <p>Software shall configure the MMCS0_CQ_TDL_BASE_ADDR[31-0] CQTDLBA_LO and MMCS0_CQ_TDL_BASE_ADDR_UPBITS[31-0] CQTDLBA_HI bit fields, and enable CQE in the MMCS0_CQ_CONFIG register before using this register.</p> <p>Writing 1h to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL.</p> <p>CQE always processes tasks in-order according to the order submitted to the list by the MMCS0_CQ_TASK_DOOR_BELL register write transactions.</p> <p>CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device.</p> <p>CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument.</p> <p>The corresponding bit is cleared to 0h by CQE in one of the following events:</p> <ul style="list-style-type: none"> (a) When a task execution is completed (with success or error) (b) The task is cleared using MMCS0_CQ_TASK_CLEAR register (c) All tasks are cleared using MMCS0_CQ_CONTROL register (d) CQE is disabled using MMCS0_CQ_CONFIG register <p>Software may initiate multiple tasks at the same time (batch submission) by writing 1h to multiple bits of this register in the same transaction.</p> <p>In the case of batch submission:</p> <p>CQE shall process the tasks in order of the task index, starting with the lowest index.</p> <p>If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order.</p> <p>Writing 0h by software shall have no impact on the hardware, and will not change the value of the register bit.</p>

18.2.87 MMCS0_CQ_TASK_COMP_NOTIF Register (Offset = 22Ch) [reset = 0h]

MMCS0_CQ_TASK_COMP_NOTIF is shown in [Figure 18-116](#) and described in [Table 18-278](#).

Return to [Summary Table](#).

This register is used by CQE to notify software about completed tasks.

**Table 18-277. MMCS0_CQ_TASK_COMP_NOTIF
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 022Ch

Figure 18-116. MMCS0_CQ_TASK_COMP_NOTIF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTCN_VAL																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-278. MMCS0_CQ_TASK_COMP_NOTIF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTCN_VAL	R/W1C	0h	<p>Task Complete Notification</p> <p>CQE shall set bit n of this register (at the same time it clears bit n of the MMCS0_CQ_TASK_DOOR_BELL register) when a task execution is completed (with success or error).</p> <p>When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1h to the corresponding bits.</p>

18.2.88 MMCS0_CQ_DEV_QUEUE_STATUS Register (Offset = 230h) [reset = 0h]

MMCS0_CQ_DEV_QUEUE_STATUS is shown in [Figure 18-117](#) and described in [Table 18-280](#).

Return to [Summary Table](#).

This register stores the most recent value of the device's queue status.

Table 18-279. MMCS0_CQ_DEV_QUEUE_STATUS Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0230h

Figure 18-117. MMCS0_CQ_DEV_QUEUE_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQDQ_STS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-280. MMCS0_CQ_DEV_QUEUE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQDQ_STS	R	0h	Device Queue Status Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command (the device's queue status).

18.2.89 MMCSD0_CQ_DEV_PENDING_TASKS Register (Offset = 234h) [reset = 0h]

MMCSD0_CQ_DEV_PENDING_TASKS is shown in [Figure 18-118](#) and described in [Table 18-282](#).

Return to [Summary Table](#).

This register indicates to software which tasks are queued in the device, awaiting execution.

Table 18-281. MMCSD0_CQ_DEV_PENDING_TASKS Instances

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0234h

Figure 18-118. MMCSD0_CQ_DEV_PENDING_TASKS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQDP_TSKS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-282. MMCSD0_CQ_DEV_PENDING_TASKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQDP_TSKS	R	0h	<p>Device Pending Tasks</p> <p>Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasnt been executed yet.</p> <p>CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution.</p> <p>Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE.</p> <p>Only then the software orders CQE to resume its operation using MMCSD0_CQ_CONTROL register.</p>

18.2.90 MMCS0_CQ_TASK_CLEAR Register (Offset = 238h) [reset = 0h]

MMCS0_CQ_TASK_CLEAR is shown in [Figure 18-119](#) and described in [Table 18-284](#).

Return to [Summary Table](#).

This register is used for removing an outstanding task in the CQE 327. The register should be used only when CQE is in Halt state.

Table 18-283. MMCS0_CQ_TASK_CLEAR Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0238h

Figure 18-119. MMCS0_CQ_TASK_CLEAR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTCLR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-284. MMCS0_CQ_TASK_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTCLR	R/W	0h	<p>Command Queueing Task Clear</p> <p>Writing 1h to bit n of this register orders CQE to clear a task which software has previously issued.</p> <p>This bit can only be written when CQE is in Halt state as indicated in the MMCS0_CQ_CONFIG register Halt bit.</p> <p>When software writes 1h to a bit in this register, CQE updates the value to 1h, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0h) in the MMCS0_CQ_TASK_CLEAR and in MMCS0_CQ_TASK_DOOR_BELL registers once clear operation is complete.</p> <p>Software should poll on the MMCS0_CQ_TASK_CLEAR register until it is cleared to verify clear operation was complete.</p> <p>Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK_MGMT while CQE is still in Halt state.</p> <p>Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using MMCS0_CQ_CONTROL register.</p> <p>Writing 0h to a register bit shall have no impact.</p>

18.2.91 MMCS0_CQ_SEND_STS_CONFIG1 Register (Offset = 240h) [reset = 11000h]

MMCS0_CQ_SEND_STS_CONFIG1 is shown in [Figure 18-120](#) and described in [Table 18-286](#).

Return to [Summary Table](#).

The register controls when the SEND_QUEUE_STATUS commands are sent.

**Table 18-285. MMCS0_CQ_SEND_STS_CONFIG1
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0240h

Figure 18-120. MMCS0_CQ_SEND_STS_CONFIG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												CMD_BLK_CNTR			
R-0h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_IDLE_TIMER															
R/W-1000h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-286. MMCS0_CQ_SEND_STS_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	CMD_BLK_CNTR	R/W	1h	Send Status Command Block Counter This field indicates to CQE when to send SEND_QUEUE_STATUS (CMD13) command to inquire the status of the devices task queue. A value of n means CQE shall send status command on the CMD line, during the transfer of data block BLOCK_CNT-n , on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. A value of 0h means that SEND_QUEUE_STATUS (CMD13) command shall not be sent during the transaction. Instead it will be sent only when the data lines are idle. A value of 1 means that STATUS command is to be sent during the last block of the transaction.
15-0	CMD_IDLE_TIMER	R/W	1000h	Send Status Command Idle Timer This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field in the MMCS0_CQ_CAPABILITIES register. The minimum value is 1h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is: 4096 clock periods. For example, a MMCS0_CQ_CAPABILITIES field value of 0h indicates a 19.2 MHz clock frequency (period = 52.08 ns).

18.2.92 MMCS0_CQ_SEND_STS_CONFIG2 Register (Offset = 244h) [reset = 0h]

MMCS0_CQ_SEND_STS_CONFIG2 is shown in [Figure 18-121](#) and described in [Table 18-288](#).

Return to [Summary Table](#).

This register is used for 333 configuring RCA field in SEND_QUEUE_STATUS command argument.

**Table 18-287. MMCS0_CQ_SEND_STS_CONFIG2
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0244h

Figure 18-121. MMCS0_CQ_SEND_STS_CONFIG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																QUEUE_RCA															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-288. MMCS0_CQ_SEND_STS_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	QUEUE_RCA	R/W	0h	Send Queue RCA This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE shall copy this field to bits 31-16 of the argument when transmitting SEND_QUEUE_STATUS (CMD13) command.

18.2.93 MMCSO_CQ_DCMD_RESPONSE Register (Offset = 248h) [reset = 0h]

MMCSO_CQ_DCMD_RESPONSE is shown in [Figure 18-122](#) and described in [Table 18-290](#).

Return to [Summary Table](#).

This register is used for passing the response of a DCMD task to software.

**Table 18-289. MMCSO_CQ_DCMD_RESPONSE
Instances**

Instance	Physical Address
MMCSO_CTL_CFG	04F8 0248h

Figure 18-122. MMCSO_CQ_DCMD_RESPONSE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAST_RESP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-290. MMCSO_CQ_DCMD_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LAST_RESP	R	0h	Direct Command Last Response This register contains the response of the command generated by the last direct command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of the MMCSO_CQ_TASK_DOOR_BELL register is cleared by CQE.

18.2.94 MMCS0_CQ_RESP_ERR_MASK Register (Offset = 250h) [reset = FDF9A080h]

MMCS0_CQ_RESP_ERR_MASK is shown in [Figure 18-123](#) and described in [Table 18-292](#).

Return to [Summary Table](#).

This register controls the generation of Response Error Detection (RED) interrupt.

Table 18-291. MMCS0_CQ_RESP_ERR_MASK Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0250h

Figure 18-123. MMCS0_CQ_RESP_ERR_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQRMEM																															
R-FDF9A080h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-292. MMCS0_CQ_RESP_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQRMEM	R	FDF9A080h	<p>Response Mode Error Mask</p> <p>This bit is used as in interrupt mask on the device status field which is received in R1/R1b responses.</p> <p>Bit Value Description (for any bit i):</p> <p>1h: When a R1/R1b response is received, with bit i in the device status set, a RED interrupt is generated</p> <p>0h: When a R1/R1b response is received, bit i in the device status is ignored</p> <p>The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status.</p> <p>Note: Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.</p>

18.2.95 MMCSD0_CQ_TASK_ERR_INFO Register (Offset = 254h) [reset = 0h]

MMCSD0_CQ_TASK_ERR_INFO is shown in [Figure 18-124](#) and described in [Table 18-294](#).

Return to [Summary Table](#).

This register is updated by CQE when an error occurs on data or command related to a task activity. When such error is detected by CQE or indicated by the eMMC controller CQE stores in the MMCSD0_CQ_TASK_ERR_INFO register the task IDs and the command indices of the commands which were executed on the 343 command line and data lines when the error occurred.

Software is expected to use this information in the error recovery procedure.

**Table 18-293. MMCSD0_CQ_TASK_ERR_INFO
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0254h

Figure 18-124. MMCSD0_CQ_TASK_ERR_INFO Register

31	30	29	28	27	26	25	24
DATERR_VALID	RESERVED			DATERR_TASK_ID			
R-0h	R-0h			R-0h			
23	22	21	20	19	18	17	16
RESERVED		DATERR_CMD_INDEX					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RESP_MODE_VALID	RESERVED			RESP_MODE_TASK_ID			
R-0h	R-0h			R-0h			
7	6	5	4	3	2	1	0
RESERVED		RESP_MODE_CMD_INDEX					
R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-294. MMCSD0_CQ_TASK_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DATERR_VALID	R	0h	Data Transfer Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1h. If a no data transfer is in progress when the error is detected/indicated, the bit is cleared to 0h.
30-29	RESERVED	R	0h	Reserved
28-24	DATERR_TASK_ID	R	0h	Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23-22	RESERVED	R	0h	Reserved

Table 18-294. MMCS0_CQ_TASK_ERR_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	DATERR_CMD_INDEX	R	0h	Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	RESP_MODE_VALID	R	0h	Response Mode Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1h. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0h.
14-13	RESERVED	R	0h	Reserved
12-8	RESP_MODE_TASK_ID	R	0h	Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7-6	RESERVED	R	0h	Reserved
5-0	RESP_MODE_CMD_INDEX	R	0h	Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

18.2.96 MMCSD0_CQ_CMD_RESP_INDEX Register (Offset = 258h) [reset = 0h]

MMCSD0_CQ_CMD_RESP_INDEX is shown in [Figure 18-125](#) and described in [Table 18-296](#).

Return to [Summary Table](#).

This register stores the index of the last received command response.

**Table 18-295. MMCSD0_CQ_CMD_RESP_INDEX
Instances**

Instance	Physical Address
MMCSD0_CTL_CFG	04F8 0258h

Figure 18-125. MMCSD0_CQ_CMD_RESP_INDEX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										LAST_CRI					
R-0h										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-296. MMCSD0_CQ_CMD_RESP_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	LAST_CRI	R	0h	Last Command Response Index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

18.2.97 MMCS0_CQ_CMD_RESP_ARG Register (Offset = 25Ch) [reset = 0h]

MMCS0_CQ_CMD_RESP_ARG is shown in [Figure 18-126](#) and described in [Table 18-298](#).

Return to [Summary Table](#).

This register stores the index of the last received command response.

Table 18-297. MMCS0_CQ_CMD_RESP_ARG Instances

Instance	Physical Address
MMCS0_CTL_CFG	04F8 025Ch

Figure 18-126. MMCS0_CQ_CMD_RESP_ARG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAST_CRA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-298. MMCS0_CQ_CMD_RESP_ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LAST_CRA	R	0h	Last Command Response Argument This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

18.2.98 MMCS0_CQ_ERROR_TASK_ID Register (Offset = 260h) [reset = 0h]

MMCS0_CQ_ERROR_TASK_ID is shown in [Figure 18-127](#) and described in [Table 18-300](#).

Return to [Summary Table](#).

CQ Error Task ID Register

**Table 18-299. MMCS0_CQ_ERROR_TASK_ID
Instances**

Instance	Physical Address
MMCS0_CTL_CFG	04F8 0260h

Figure 18-127. MMCS0_CQ_ERROR_TASK_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TERR_ID			
R-0h												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 18-300. MMCS0_CQ_ERROR_TASK_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	TERR_ID	R	0h	Task Error ID

18.3 MMCS0 RX RAM ECC Aggregator Registers

Table 18-302 lists the memory-mapped registers for the MMCS0 RX RAM ECC Aggregator. All register offset addresses not listed in Table 18-302 should be considered as reserved locations and the register contents should not be modified.

**Table 18-301. MMCS0 RX RAM ECC Aggregator
Instances**

Instance	Base Address
MMCS0_ECC_AGGR_RXMEM	02A2 4000h

Table 18-302. MMCS0 RX RAM ECC Aggregator Registers

Offset	Acronym	Register Name	MMCS0_ECC_AGGR_RXMEM Physical Address
0h	MMCS0_RXECC_REV	Aggregator Revision Register	02A2 4000h
8h	MMCS0_RXECC_VECTOR	ECC Vector Register	02A2 4008h
Ch	MMCS0_RXECC_STAT	Misc Status Register	02A2 400Ch
3Ch	MMCS0_RXECC_SEC_EOI_REG	SEC EOI Register	02A2 403Ch
40h	MMCS0_RXECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	02A2 4040h
80h	MMCS0_RXECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	02A2 4080h
C0h	MMCS0_RXECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	02A2 40C0h
13Ch	MMCS0_RXECC_DED_EOI_REG	DED EOI Register	02A2 413Ch
140h	MMCS0_RXECC_DED_STATUS_REG0	DED Interrupt Status Register 0	02A2 4140h
180h	MMCS0_RXECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	02A2 4180h
1C0h	MMCS0_RXECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	02A2 41C0h
200h	MMCS0_RXECC_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	02A2 4200h
204h	MMCS0_RXECC_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	02A2 4204h
208h	MMCS0_RXECC_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	02A2 4208h
20Ch	MMCS0_RXECC_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	02A2 420Ch

18.3.1 MMCS0_RXECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MMCS0_RXECC_REV is shown in Figure 18-128 and described in Table 18-304.

Return to [Summary Table](#).

Aggregator Revision Register

Revision parameters.

Table 18-303. MMCS0_RXECC_REV Instances

Instance	Physical Address
MMCS0_ECC_AGGR_RXMEM	02A2 4000h

Figure 18-128. MMCS0_RXECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-304. MMCS0_RXECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

Table 18-305. Register Call Summary for MMCS0_RXECC_REV

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]: \[0\]](#)

18.3.2 MMCS0_RXECC_VECTOR Register (Offset = 8h) [reset = 0h]

MMCS0_RXECC_VECTOR is shown in Figure 18-129 and described in Table 18-307.

Return to [Summary Table](#).

ECC Vector Register

Table 18-306. MMCS0_RXECC_VECTOR Instances

Instance	Physical Address
MMCS0_ECC_AGGG_RXMEM	02A2 4008h

Figure 18-129. MMCS0_RXECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-307. MMCS0_RXECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

Table 18-308. Register Call Summary for MMCS0_RXECC_VECTOR

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_VECTOR Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)

18.3.3 MMCSD0_RXECC_STAT Register (Offset = Ch) [reset = 1h]

MMCSD0_RXECC_STAT is shown in Figure 18-130 and described in Table 18-310.

Return to [Summary Table](#).

Misc Status Register

Table 18-309. MMCSD0_RXECC_STAT Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	02A2 400Ch

Figure 18-130. MMCSD0_RXECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RESERVED																					NUM_RAMs															
R-0h																					R-1h															

LEGEND: R = Read Only; -n = value after reset

Table 18-310. MMCSD0_RXECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMs	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

Table 18-311. Register Call Summary for MMCSD0_RXECC_STAT

MMCSD0 RX RAM ECC Aggregator Registers

- [MMCSD0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSD0_RXECC_STAT Register \(Offset = Ch\) \[reset = 1h\]: \[0\]](#)

18.3.4 MMCS0_RXECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MMCS0_RXECC_SEC_EOI_REG is shown in Figure 18-131 and described in Table 18-313.

Return to [Summary Table](#).

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 18-312. MMCS0_RXECC_SEC_EOI_REG Instances

Instance	Physical Address
MMCS0_ECC_AGG_RXMEM	02A2 403Ch

Figure 18-131. MMCS0_RXECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-313. MMCS0_RXECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	SEC EOI

Table 18-314. Register Call Summary for MMCS0_RXECC_SEC_EOI_REG

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)

18.3.5 MMCS0_RXECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MMCS0_RXECC_SEC_STATUS_REG0 is shown in [Figure 18-132](#) and described in [Table 18-316](#).

Return to [Summary Table](#).

SEC Interrupt Status Register 0

Table 18-315.
MMCS0_RXECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
MMCS0_ECC_AGGREGATOR_RXMEM	02A2 4040h

Figure 18-132. MMCS0_RXECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-316. MMCS0_RXECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_PEND	R/W1S	0h	Interrupt Pending Status for rxmem_pend

Table 18-317. Register Call Summary for MMCS0_RXECC_SEC_STATUS_REG0

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = 0h\]: \[0\]](#)

18.3.6 MMCS0_RXECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MMCS0_RXECC_SEC_ENABLE_SET_REG0 is shown in Figure 18-133 and described in Table 18-319.

Return to [Summary Table](#).

SEC Interrupt Enable Set Register 0

Table 18-318.
MMCS0_RXECC_SEC_ENABLE_SET_REG0
Instances

Instance	Physical Address
MMCS0_ECC_AGGR_RXMEM	02A2 4080h

Figure 18-133. MMCS0_RXECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-319. MMCS0_RXECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for rxmem_pend

Table 18-320. Register Call Summary for MMCS0_RXECC_SEC_ENABLE_SET_REG0

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = 0h\]: \[0\]](#)

18.3.7 MMCS0_RXECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MMCS0_RXECC_SEC_ENABLE_CLR_REG0 is shown in Figure 18-134 and described in Table 18-322.

Return to [Summary Table](#).

SEC Interrupt Enable Clear Register 0

Table 18-321.
MMCS0_RXECC_SEC_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MMCS0_ECC_AGGG_RXMEM	02A2 40C0h

Figure 18-134. MMCS0_RXECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENAB LE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-322. MMCS0_RXECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for rxmem_pend

Table 18-323. Register Call Summary for MMCS0_RXECC_SEC_ENABLE_CLR_REG0

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = 0h\]: \[0\]](#)

18.3.8 MMCS0_RXECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MMCS0_RXECC_DED_EOI_REG is shown in Figure 18-135 and described in Table 18-325.

Return to [Summary Table](#).

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 18-324. MMCS0_RXECC_DED_EOI_REG Instances

Instance	Physical Address
MMCS0_ECC_AGG_RXMEM	02A2 413Ch

Figure 18-135. MMCS0_RXECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-325. MMCS0_RXECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	DED EOI

Table 18-326. Register Call Summary for MMCS0_RXECC_DED_EOI_REG

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = 0h\]: \[0\]](#)

18.3.9 MMCS0_RXECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MMCS0_RXECC_DED_STATUS_REG0 is shown in [Figure 18-136](#) and described in [Table 18-328](#).

Return to [Summary Table](#).

DED Interrupt Status Register 0

Table 18-327.
MMCS0_RXECC_DED_STATUS_REG0 Instances

Instance	Physical Address
MMCS0_ECC_AGGG_RXMEM	02A2 4140h

Figure 18-136. MMCS0_RXECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-328. MMCS0_RXECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_PEND	R/W1S	0h	Interrupt Pending Status for rxmem_pend

Table 18-329. Register Call Summary for MMCS0_RXECC_DED_STATUS_REG0

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_DED_STATUS_REG0 Register \(Offset = 140h\) \[reset = 0h\]: \[0\]](#)

18.3.10 MMCS0_RXECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MMCS0_RXECC_DED_ENABLE_SET_REG0 is shown in Figure 18-137 and described in Table 18-331.

Return to [Summary Table](#).

DED Interrupt Enable Set Register 0

Table 18-330.
MMCS0_RXECC_DED_ENABLE_SET_REG0
Instances

Instance	Physical Address
MMCS0_ECC_AGGR_RXMEM	02A2 4180h

Figure 18-137. MMCS0_RXECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-331. MMCS0_RXECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for rxmem_pend

Table 18-332. Register Call Summary for MMCS0_RXECC_DED_ENABLE_SET_REG0

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_DED_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = 0h\]: \[0\]](#)

18.3.11 MMCS0_RXECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MMCS0_RXECC_DED_ENABLE_CLR_REG0 is shown in Figure 18-138 and described in Table 18-334.

Return to [Summary Table](#).

DED Interrupt Enable Clear Register 0

Table 18-333.
MMCS0_RXECC_DED_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MMCS0_ECC_AGGR_RXMEM	02A2 41C0h

Figure 18-138. MMCS0_RXECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENAB LE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-334. MMCS0_RXECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for rxmem_pend

Table 18-335. Register Call Summary for MMCS0_RXECC_DED_ENABLE_CLR_REG0

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = 0h\]: \[0\]](#)

18.3.12 MMCS0_RXECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MMCS0_RXECC_AGGR_ENABLE_SET is shown in Figure 18-139 and described in Table 18-337.

Return to [Summary Table](#).

Aggregator Interrupt Enable Set Register

Table 18-336.
MMCS0_RXECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
MMCS0_ECC_AGGR_RXMEM	02A2 4200h

Figure 18-139. MMCS0_RXECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-337. MMCS0_RXECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

Table 18-338. Register Call Summary for MMCS0_RXECC_AGGR_ENABLE_SET

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_AGGR_ENABLE_SET Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)

18.3.13 MMCSD0_RXECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MMCSD0_RXECC_AGGR_ENABLE_CLR is shown in Figure 18-140 and described in Table 18-340.

Return to [Summary Table](#).

Aggregator Interrupt Enable Clear Register

Table 18-339.
MMCSD0_RXECC_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_RXMEM	02A2 4204h

Figure 18-140. MMCSD0_RXECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-340. MMCSD0_RXECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

Table 18-341. Register Call Summary for MMCSD0_RXECC_AGGR_ENABLE_CLR

MMCSD0 RX RAM ECC Aggregator Registers

- [MMCSD0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSD0_RXECC_AGGR_ENABLE_CLR Register \(Offset = 204h\) \[reset = 0h\]: \[0\]](#)

18.3.14 MMCS0_RXECC_AGG_STATUS_SET Register (Offset = 208h) [reset = 0h]

MMCS0_RXECC_AGG_STATUS_SET is shown in Figure 18-141 and described in Table 18-343.

Return to [Summary Table](#).

Aggregator Interrupt Status Set Register

Table 18-342.
MMCS0_RXECC_AGG_STATUS_SET Instances

Instance	Physical Address
MMCS0_ECC_AGG_RXMEM	02A2 4208h

Figure 18-141. MMCS0_RXECC_AGG_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 18-343. MMCS0_RXECC_AGG_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

Table 18-344. Register Call Summary for MMCS0_RXECC_AGG_STATUS_SET

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_AGG_STATUS_SET Register \(Offset = 208h\) \[reset = 0h\]: \[0\]](#)

18.3.15 MMCS0_RXECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MMCS0_RXECC_AGGR_STATUS_CLR is shown in [Figure 18-142](#) and described in [Table 18-346](#).

Return to [Summary Table](#).

Aggregator Interrupt Status Clear Register

Table 18-345.
MMCS0_RXECC_AGGR_STATUS_CLR Instances

Instance	Physical Address
MMCS0_ECC_AGGR_RXMEM	02A2 420Ch

Figure 18-142. MMCS0_RXECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 18-346. MMCS0_RXECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

Table 18-347. Register Call Summary for MMCS0_RXECC_AGGR_STATUS_CLR

MMCS0 RX RAM ECC Aggregator Registers

- [MMCS0 RX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_RXECC_AGGR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = 0h\]: \[0\]](#)

18.4 MMCS0 TX RAM ECC Aggregator Registers

Table 18-349 lists the memory-mapped registers for the MMCS0 TX RAM ECC Aggregator. All register offset addresses not listed in Table 18-349 should be considered as reserved locations and the register contents should not be modified.

Table 18-348. MMCS0 TX RAM ECC Aggregator Instances

Instance	Base Address
MMCS0_ECC_AGGR_TXMEM	02A2 5000h

Table 18-349. MMCS0 TX RAM ECC Aggregator Registers

Offset	Acronym	Register Name	MMCS0_ECC_AGGR_TXMEM Physical Address
0h	MMCS0_TXECC_REV	Aggregator Revision Register	02A2 5000h
8h	MMCS0_TXECC_VECTOR	ECC Vector Register	02A2 5008h
Ch	MMCS0_TXECC_STAT	Misc Status Register	02A2 500Ch
3Ch	MMCS0_TXECC_SEC_EOI_REG	SEC EOI Register	02A2 503Ch
40h	MMCS0_TXECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	02A2 5040h
80h	MMCS0_TXECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	02A2 5080h
C0h	MMCS0_TXECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	02A2 50C0h
13Ch	MMCS0_TXECC_DED_EOI_REG	DED EOI Register	02A2 513Ch
140h	MMCS0_TXECC_DED_STATUS_REG0	DED Interrupt Status Register 0	02A2 5140h
180h	MMCS0_TXECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	02A2 5180h
1C0h	MMCS0_TXECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	02A2 51C0h
200h	MMCS0_TXECC_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	02A2 5200h
204h	MMCS0_TXECC_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	02A2 5204h
208h	MMCS0_TXECC_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	02A2 5208h
20Ch	MMCS0_TXECC_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	02A2 520Ch

18.4.1 MMCSD0_TXECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MMCSD0_TXECC_REV is shown in [Figure 18-143](#) and described in [Table 18-351](#).

[Return to Summary Table.](#)

Aggregator Revision Register

Revision parameters.

Table 18-350. MMCSD0_TXECC_REV Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	02A2 5000h

Figure 18-143. MMCSD0_TXECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-351. MMCSD0_TXECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

Table 18-352. Register Call Summary for MMCSD0_TXECC_REV

MMCSD0 TX RAM ECC Aggregator Registers

- [MMCSD0 TX RAM ECC Aggregator Registers](#): [0]
- [MMCSD0_TXECC_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]](#): [0]

18.4.2 MMCS0_TXECC_VECTOR Register (Offset = 8h) [reset = 0h]

MMCS0_TXECC_VECTOR is shown in Figure 18-144 and described in Table 18-354.

Return to [Summary Table](#).

ECC Vector Register

Table 18-353. MMCS0_TXECC_VECTOR Instances

Instance	Physical Address
MMCS0_ECC_AGGR_TXMEM	02A2 5008h

Figure 18-144. MMCS0_TXECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-354. MMCS0_TXECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

Table 18-355. Register Call Summary for MMCS0_TXECC_VECTOR

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_VECTOR Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)

18.4.3 MMCSD0_TXECC_STAT Register (Offset = Ch) [reset = 1h]

MMCSD0_TXECC_STAT is shown in Figure 18-145 and described in Table 18-357.

Return to [Summary Table](#).

Misc Status Register

Table 18-356. MMCSD0_TXECC_STAT Instances

Instance	Physical Address
MMCSD0_ECC_AGGR_TXMEM	02A2 500Ch

Figure 18-145. MMCSD0_TXECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												NUM_RAMs																			
R-0h												R-1h																			

LEGEND: R = Read Only; -n = value after reset

Table 18-357. MMCSD0_TXECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMs	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

Table 18-358. Register Call Summary for MMCSD0_TXECC_STAT

MMCSD0 TX RAM ECC Aggregator Registers

- [MMCSD0_TXECC_STAT Register \(Offset = Ch\) \[reset = 1h\]: \[0\]](#)
- [MMCSD0 TX RAM ECC Aggregator Registers: \[0\]](#)

18.4.4 MMCS0_TXECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MMCS0_TXECC_SEC_EOI_REG is shown in Figure 18-146 and described in Table 18-360.

Return to [Summary Table](#).

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 18-359. MMCS0_TXECC_SEC_EOI_REG Instances

Instance	Physical Address
MMCS0_ECC_AGGR_TXMEM	02A2 503Ch

Figure 18-146. MMCS0_TXECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-360. MMCS0_TXECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	SEC EOI

Table 18-361. Register Call Summary for MMCS0_TXECC_SEC_EOI_REG

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)

18.4.5 MMCS0_TXECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MMCS0_TXECC_SEC_STATUS_REG0 is shown in Figure 18-147 and described in Table 18-363.

Return to [Summary Table](#).

SEC Interrupt Status Register 0

Table 18-362.
MMCS0_TXECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
MMCS0_ECC_AGGREGATOR_TXMEM	02A2 5040h

Figure 18-147. MMCS0_TXECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-363. MMCS0_TXECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_PEND	R/W1S	0h	Interrupt Pending Status for txmem_pend

Table 18-364. Register Call Summary for MMCS0_TXECC_SEC_STATUS_REG0

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0_TXECC_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = 0h\]: \[0\]](#)
- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)

18.4.6 MMCS0_TXECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MMCS0_TXECC_SEC_ENABLE_SET_REG0 is shown in Figure 18-148 and described in Table 18-366.

Return to [Summary Table](#).

SEC Interrupt Enable Set Register 0

Table 18-365.
MMCS0_TXECC_SEC_ENABLE_SET_REG0
Instances

Instance	Physical Address
MMCS0_ECC_AGGREGATOR_TXMEM	02A2 5080h

Figure 18-148. MMCS0_TXECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-366. MMCS0_TXECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for txmem_pend

Table 18-367. Register Call Summary for MMCS0_TXECC_SEC_ENABLE_SET_REG0

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = 0h\]: \[0\]](#)

18.4.7 MMCS0_TXECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MMCS0_TXECC_SEC_ENABLE_CLR_REG0 is shown in Figure 18-149 and described in Table 18-369.

Return to [Summary Table](#).

SEC Interrupt Enable Clear Register 0

Table 18-368.
MMCS0_TXECC_SEC_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MMCS0_ECC_AGGREGATOR_TXMEM	02A2 50C0h

Figure 18-149. MMCS0_TXECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-369. MMCS0_TXECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for txmem_pend

Table 18-370. Register Call Summary for MMCS0_TXECC_SEC_ENABLE_CLR_REG0

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = 0h\]: \[0\]](#)

18.4.8 MMCS0_TXECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MMCS0_TXECC_DED_EOI_REG is shown in Figure 18-150 and described in Table 18-372.

Return to [Summary Table](#).

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 18-371. MMCS0_TXECC_DED_EOI_REG Instances

Instance	Physical Address
MMCS0_ECC_AGGR_TXMEM	02A2 513Ch

Figure 18-150. MMCS0_TXECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-372. MMCS0_TXECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	DED EOI

Table 18-373. Register Call Summary for MMCS0_TXECC_DED_EOI_REG

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = 0h\]: \[0\]](#)

18.4.9 MMCS0_TXECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MMCS0_TXECC_DED_STATUS_REG0 is shown in Figure 18-151 and described in Table 18-375.

Return to [Summary Table](#).

DED Interrupt Status Register 0

Table 18-374.
MMCS0_TXECC_DED_STATUS_REG0 Instances

Instance	Physical Address
MMCS0_ECC_AGGREGATOR_TXMEM	02A2 5140h

Figure 18-151. MMCS0_TXECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-375. MMCS0_TXECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_PEND	R/W1S	0h	Interrupt Pending Status for txmem_pend

Table 18-376. Register Call Summary for MMCS0_TXECC_DED_STATUS_REG0

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0_TXECC_DED_STATUS_REG0 Register \(Offset = 140h\) \[reset = 0h\]: \[0\]](#)
- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)

18.4.10 MMCS0_TXECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MMCS0_TXECC_DED_ENABLE_SET_REG0 is shown in Figure 18-152 and described in Table 18-378.

Return to [Summary Table](#).

DED Interrupt Enable Set Register 0

Table 18-377.
MMCS0_TXECC_DED_ENABLE_SET_REG0
Instances

Instance	Physical Address
MMCS0_ECC_AGGREGATOR_TXMEM	02A2 5180h

Figure 18-152. MMCS0_TXECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-378. MMCS0_TXECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for txmem_pend

Table 18-379. Register Call Summary for MMCS0_TXECC_DED_ENABLE_SET_REG0

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_DED_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = 0h\]: \[0\]](#)

18.4.11 MMCS0_TXECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MMCS0_TXECC_DED_ENABLE_CLR_REG0 is shown in Figure 18-153 and described in Table 18-381.

Return to [Summary Table](#).

DED Interrupt Enable Clear Register 0

Table 18-380.
MMCS0_TXECC_DED_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MMCS0_ECC_AGGREGATOR_TXMEM	02A2 51C0h

Figure 18-153. MMCS0_TXECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-381. MMCS0_TXECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for txmem_pend

Table 18-382. Register Call Summary for MMCS0_TXECC_DED_ENABLE_CLR_REG0

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = 0h\]: \[0\]](#)

18.4.12 MMCS0_TXECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MMCS0_TXECC_AGGR_ENABLE_SET is shown in Figure 18-154 and described in Table 18-384.

Return to [Summary Table](#).

Aggregator Interrupt Enable Set Register

Table 18-383.
MMCS0_TXECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
MMCS0_ECC_AGGR_TXMEM	02A2 5200h

Figure 18-154. MMCS0_TXECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-384. MMCS0_TXECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

Table 18-385. Register Call Summary for MMCS0_TXECC_AGGR_ENABLE_SET

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_AGGR_ENABLE_SET Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)

18.4.13 MMCS0_TXECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MMCS0_TXECC_AGGR_ENABLE_CLR is shown in Figure 18-155 and described in Table 18-387.

Return to [Summary Table](#).

Aggregator Interrupt Enable Clear Register

Table 18-386.
MMCS0_TXECC_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MMCS0_ECC_AGGR_TXMEM	02A2 5204h

Figure 18-155. MMCS0_TXECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-387. MMCS0_TXECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

Table 18-388. Register Call Summary for MMCS0_TXECC_AGGR_ENABLE_CLR

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS0_TXECC_AGGR_ENABLE_CLR Register \(Offset = 204h\) \[reset = 0h\]: \[0\]](#)

18.4.14 MMCS0_TXECC_AGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MMCS0_TXECC_AGR_STATUS_SET is shown in Figure 18-156 and described in Table 18-390.

Return to [Summary Table](#).

Aggregator Interrupt Status Set Register

Table 18-389.
MMCS0_TXECC_AGR_STATUS_SET Instances

Instance	Physical Address
MMCS0_ECC_AGR_TXMEM	02A2 5208h

Figure 18-156. MMCS0_TXECC_AGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 18-390. MMCS0_TXECC_AGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

Table 18-391. Register Call Summary for MMCS0_TXECC_AGR_STATUS_SET

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0_TXECC_AGR_STATUS_SET Register \(Offset = 208h\) \[reset = 0h\]: \[0\]](#)
- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)

18.4.15 MMCS0_TXECC_AGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MMCS0_TXECC_AGR_STATUS_CLR is shown in [Figure 18-157](#) and described in [Table 18-393](#).

Return to [Summary Table](#).

Aggregator Interrupt Status Clear Register

Table 18-392.
MMCS0_TXECC_AGR_STATUS_CLR Instances

Instance	Physical Address
MMCS0_ECC_AGR_TXMEM	02A2 520Ch

Figure 18-157. MMCS0_TXECC_AGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 18-393. MMCS0_TXECC_AGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

Table 18-394. Register Call Summary for MMCS0_TXECC_AGR_STATUS_CLR

MMCS0 TX RAM ECC Aggregator Registers

- [MMCS0_TXECC_AGR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = 0h\]: \[0\]](#)
- [MMCS0 TX RAM ECC Aggregator Registers: \[0\]](#)

18.5 MMCSDB1 / MMCSDB2 Subsystem Registers

Table 18-396 lists the memory-mapped registers for the MMCSDB1 / MMCSDB2 Subsystem. All register offset addresses not listed in Table 18-396 should be considered as reserved locations and the register contents should not be modified.

**Table 18-395. MMCSDB1 / MMCSDB2 Subsystem
Instances**

Instance	Base Address
MMCSDB1_SS_CFG	04FB 8000h
MMCSDB2_SS_CFG	04F9 0000h

Table 18-396. MMCSDB1 / MMCSDB2 Subsystem Registers

Offset	Acronym	Register Name	MMCSDB1_SS_CFG Physical Address	MMCSDB2_SS_CFG Physical Address
0h	MMCSDB12_SS_SS_ID_REV_REG	Subsystem ID and Revision Register	04FB 8000h	04F9 0000h
10h	MMCSDB12_SS_CTL_CFG_1_REG	Controller Config 1 Register	04FB 8010h	04F9 0010h
14h	MMCSDB12_SS_CTL_CFG_2_REG	Controller Config 2 Register	04FB 8014h	04F9 0014h
18h	MMCSDB12_SS_CTL_CFG_3_REG	Controller Config 3 Register	04FB 8018h	04F9 0018h
1Ch	MMCSDB12_SS_CTL_CFG_4_REG	Controller Config 4 Register	04FB 801Ch	04F9 001Ch
20h	MMCSDB12_SS_CTL_CFG_5_REG	Controller Config 5 Register	04FB 8020h	04F9 0020h
24h	MMCSDB12_SS_CTL_CFG_6_REG	Controller Config 6 Register	04FB 8024h	04F9 0024h
28h	MMCSDB12_SS_CTL_CFG_7_REG	Controller Config 7 Register	04FB 8028h	04F9 0028h
2Ch	MMCSDB12_SS_CTL_CFG_8_REG	Controller Config 8 Register	04FB 802Ch	04F9 002Ch
30h	MMCSDB12_SS_CTL_CFG_9_REG	Controller Config 9 Register	04FB 8030h	04F9 0030h
34h	MMCSDB12_SS_CTL_CFG_10_REG	Controller Config 10 Register	04FB 8034h	04F9 0034h
38h	MMCSDB12_SS_CTL_CFG_11_REG	Controller Config 11 Register	04FB 8038h	04F9 0038h
3Ch	MMCSDB12_SS_CTL_CFG_12_REG	Controller Config 12 Register	04FB 803Ch	04F9 003Ch
40h	MMCSDB12_SS_CTL_CFG_13_REG	Controller Config 13 Register	04FB 8040h	04F9 0040h
60h	MMCSDB12_SS_CTL_STAT_1_REG	Controller Status 1 Register	04FB 8060h	04F9 0060h
64h	MMCSDB12_SS_CTL_STAT_2_REG	Controller Status 2 Register	04FB 8064h	04F9 0064h
68h	MMCSDB12_SS_CTL_STAT_3_REG	Controller Status 3 Register	04FB 8068h	04F9 0068h
6Ch	MMCSDB12_SS_CTL_STAT_4_REG	Controller Status 4 Register	04FB 806Ch	04F9 006Ch
70h	MMCSDB12_SS_CTL_STAT_5_REG	Controller Status 5 Register	04FB 8070h	04F9 0070h
74h	MMCSDB12_SS_CTL_STAT_6_REG	Controller Status 6 Register	04FB 8074h	04F9 0074h
100h	MMCSDB12_SS_PHY_CTRL_1_REG	PHY Control 1 Register	04FB 8100h	04F9 0100h
10Ch	MMCSDB12_SS_PHY_CTRL_4_REG	PHY Control 4 Register	04FB 810Ch	04F9 010Ch
110h	MMCSDB12_SS_PHY_CTRL_5_REG	PHY Control 5 Register	04FB 8110h	04F9 0110h

18.5.1 MMCSD12_SS_SS_ID_REV_REG Register (Offset = 0h) [reset = 68403200h]

MMCSD12_SS_SS_ID_REV_REG is shown in Figure 18-158 and described in Table 18-398.

Return to [Summary Table](#).

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem.

**Table 18-397. MMCSD12_SS_SS_ID_REV_REG
Instances**

Instance	Physical Address
MMCSD1_SS_CFG	04FB 8000h
MMCSD2_SS_CFG	04F9 0000h

Figure 18-158. MMCSD12_SS_SS_ID_REV_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_ID															
R-6840h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER				MAJ_REV				CUSTOM				MIN_REV			
R-6h				R-2h				R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 18-398. MMCSD12_SS_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MOD_ID	R	6840h	Module ID
15-11	RTL_VER	R	6h	RTL Version
10-8	MAJ_REV	R	2h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	MIN_REV	R	0h	Minor Revision

Table 18-399. Register Call Summary for MMCSD12_SS_SS_ID_REV_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)
- [MMCSD12_SS_SS_ID_REV_REG Register \(Offset = 0h\) \[reset = 68403200h\]: \[0\]](#)

18.5.2 MMCSDB12_SS_CTL_CFG_1_REG Register (Offset = 10h) [reset = 201030C8h]

MMCSDB12_SS_CTL_CFG_1_REG is shown in Figure 18-159 and described in Table 18-401.

Return to [Summary Table](#).

The Controller Config 1 Register contains various fields to control the configuration ports on the Host Controller.

Table 18-400. MMCSDB12_SS_CTL_CFG_1_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 8010h
MMCSDB2_SS_CFG	04F9 0010h

Figure 18-159. MMCSDB12_SS_CTL_CFG_1_REG Register

31	30	29	28	27	26	25	24
RESERVED				TUNINGCOUNT			
R-0h				R/W-20h			
23	22	21	20	19	18	17	16
RESERVED				ASYNCKWKUPENA	RESERVED		
R-0h				R/W-1h	R-0h		
15	14	13	12	11	10	9	8
CQFMUL				RESERVED		CQFVAL	
R/W-3h				R-0h		R/W-C8h	
7	6	5	4	3	2	1	0
CQFVAL							
R/W-C8h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-401. MMCSDB12_SS_CTL_CFG_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-24	TUNINGCOUNT	R/W	20h	Configures the number of Taps (Phases) of the RX clock that is supported. The Tuning State machine uses this information to select one of the Taps (Phases) of the RX clock during the Tuning Procedure.
23-21	RESERVED	R	0h	Reserved
20	ASYNCKWKUPENA	R/W	1h	Determines the Wakeup Signal Generation Mode. 0h: Synchronous Wakeup Mode: The FCLK has to be running for this mode. The Card Insertion/Removal/Interrupt events are detected synchronously on the FCLK and the Wakeup event is generated. The Assertion and Deassertion of the Wakeup event signal synchronous to FCLK. 1h: Asynchronous Wakeup Mode: The FCLK and the ICLK can be stopped in this mode and the Wakeup event is asynchronously generated based on the Card Insertion/Removal/Interrupt events. The Assertion and Deassertion of the Wakeup event signal is asynchronous.
19-16	RESERVED	R	0h	Reserved
15-12	CQFMUL	R/W	3h	FMUL for the CQ Internal Timer Clock Frequency

Table 18-401. MMCSD12_SS_CTL_CFG_1_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	RESERVED	R	0h	Reserved
9-0	CQFVAL	R/W	C8h	FVAL for the CQ Internal Timer Clock Frequency

Table 18-402. Register Call Summary for MMCSD12_SS_CTL_CFG_1_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)
- [MMCSD12_SS_CTL_CFG_1_REG Register \(Offset = 10h\) \[reset = 201030C8h\]: \[0\]](#)

18.5.3 MMCSDB12_SS_CTL_CFG_2_REG Register (Offset = 14h) [reset = 27E8C801h]

MMCSDB12_SS_CTL_CFG_2_REG is shown in Figure 18-160 and described in Table 18-404.

Return to [Summary Table](#).

The Controller Config 2 Register contains various fields to control the configuration ports on the Host Controller. This register sets the LSB fields in the [MMCSDB12_CAPABILITIES](#) register inside the Host Controller.

Table 18-403. MMCSDB12_SS_CTL_CFG_2_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 8014h
MMCSDB2_SS_CFG	04F9 0014h

Figure 18-160. MMCSDB12_SS_CTL_CFG_2_REG Register

31	30	29	28	27	26	25	24
SLOTTYPE	ASYNCHINTRSUPPORT	RESERVED	SUPPORT1P8VOLT	SUPPORT3P0VOLT	SUPPORT3P3VOLT		
R/W-0h	R/W-1h	R-0h	R/W-1h	R/W-1h	R/W-1h		
23	22	21	20	19	18	17	16
SUSPRESSUPPORT	SDMASUPPORT	HIGHSPEEDSUPPORT	RESERVED	ADMA2SUPPORT	SUPPORT8BIT	MAXBLKLENGTH	
R/W-1h	R/W-1h	R/W-1h	R-0h	R/W-1h	R/W-0h	R/W-0h	
15	14	13	12	11	10	9	8
BASECLKFREQ							
R/W-C8h							
7	6	5	4	3	2	1	0
TIMEOUTCLKUNIT	RESERVED	TIMEOUTCLKFREQ					
R/W-0h	R-0h	R/W-1h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-404. MMCSDB12_SS_CTL_CFG_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SLOTTYPE	R/W	0h	Slot Type Should be set based on the final product usage. 0h: Removable SCard Slot 1h: Embedded Slot for One Device 2h: Shared Bus Slot 3h: Reserved
29	ASYNCHINTRSUPPORT	R/W	1h	Asynchronous Interrupt Support Suggested Value is 1h (The Core supports monitoring of Asynchronous Interrupt).
28-27	RESERVED	R	0h	Reserved
26	SUPPORT1P8VOLT	R/W	1h	1.8 V Support Suggested Value is 1h (The 1.8 Volt Switching is supported by Core). Optionally can be set to 0h if the application doesn't want 1.8 V switching (SD3.0).
25	SUPPORT3P0VOLT	R/W	1h	3.0 V Support Should be set based on whether 3.0 V is supported on the SD Interface.

Table 18-404. MMCSDB12_SS_CTL_CFG_2_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	SUPPORT3P3VOLT	R/W	1h	3.3 V Support Suggested Value is 1h as the 3.3 V is the default voltage on the SD Interface.
23	SUSPRESSUPPORT	R/W	1h	Suspend/Resume Support Suggested Value is 1h (The Suspend/Resume is supported by Core). Optionally can be set to 0h if the application doesn't want to support Suspend/Resume Mode.
22	SDMASUPPORT	R/W	1h	SDMA Support Suggested Value is 1h (The SDMA is supported by Core). Optionally can be set to 0h if the application doesn't want to support SDMA Mode.
21	HIGHSPEEDSUPPORT	R/W	1h	High Speed Support Suggested Value is 1h (The High Speed mode is supported by Core).
20	RESERVED	R	0h	Reserved
19	ADMA2SUPPORT	R/W	1h	ADMA2 Support Suggested Value is 1h (The ADMA2 is supported by Core). Optionally can be set to 0h if the application doesn't want to support ADMA2 Mode.
18	SUPPORT8BIT	R/W	0h	8-bit Support for Embedded Device Suggested Value is 1h (The Core supports 8-bit Interface). Optionally can be set to 0h if the application supports only 4-bit SD Interface.
17-16	MAXBLKLENGTH	R/W	0h	Max Block Length Maximum Block Length supported by the Core/Device. 0h: 512 Bytes 1h: 1024 Bytes 2h: 2048 Bytes 3h: Reserved
15-8	BASECLKFREQ	R/W	C8h	Base Clock Frequency for SD Clock This is the frequency of the FCLK.
7	TIMEOUTCLKUNIT	R/W	0h	Timeout Clock Unit Suggested Value is 0h (KHz).
6	RESERVED	R	0h	Reserved
5-0	TIMEOUTCLKFREQ	R/W	1h	Timeout Clock Frequency Suggested Value is 1 KHz. Internally the 1 ms Timer is used for Timeout Detection. The 1 ms Timer is generated from the FCLK.

Table 18-405. Register Call Summary for MMCSDB12_SS_CTL_CFG_2_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB12_SS_CTL_CFG_2_REG Register \(Offset = 14h\) \[reset = 27E8C801h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 Subsystem Registers: \[0\]](#)

18.5.4 MMCSDB12_SS_CTL_CFG_3_REG Register (Offset = 18h) [reset = 18000407h]

MMCSDB12_SS_CTL_CFG_3_REG is shown in Figure 18-161 and described in Table 18-407.

Return to [Summary Table](#).

The Controller Config 3 Register contains various fields to control the configuration ports on the Host Controller. This register sets the MSB fields in the [MMCSDB12_CAPABILITIES](#) register inside the Host Controller.

Table 18-406. MMCSDB12_SS_CTL_CFG_3_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 8018h
MMCSDB2_SS_CFG	04F9 0018h

Figure 18-161. MMCSDB12_SS_CTL_CFG_3_REG Register

31	30	29	28	27	26	25	24
RESERVED			SUPPORT1P8 VDD2	ADMA3SUPPO RT	RESERVED		
R-0h			R/W-1h	R/W-1h	R-0h		
23	22	21	20	19	18	17	16
CLOCKMULTIPLIER							
R/W-0h							
15	14	13	12	11	10	9	8
RETUNINGMODES		TUNINGFORS DR50	RESERVED	RETUNINGTIMERCNT			
R/W-0h		R/W-0h	R-0h	R/W-4h			
7	6	5	4	3	2	1	0
TYPE4SUPPO RT	DDRIVERSUPP ORT	CDRIVERSUPP ORT	ADRIVERSUPP ORT	RESERVED	DDR50SUPPO RT	SDR104SUPP ORT	SDR50SUPPO RT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-407. MMCSDB12_SS_CTL_CFG_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	SUPPORT1P8VDD2	R/W	1h	1.8 V VDD2 Support
27	ADMA3SUPPORT	R/W	1h	ADMA3 Support
26-24	RESERVED	R	0h	Reserved
23-16	CLOCKMULTIPLIER	R/W	0h	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 0h means that the Host Controller does not support programmable clock generator. 0h: Clock Multiplier is Not Supported 1h: Clock Multiplier M = 2 2h: Clock Multiplier M = 3 ... FFh: Clock Multiplier M = 256
15-14	RETUNINGMODES	R/W	0h	Re-Tuning Modes Should be set to 2h as the Core supports only the Software Timer based Re-Tuning.

Table 18-407. MMCSDB12_SS_CTL_CFG_3_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	TUNINGFORSDR50	R/W	0h	Use Tuning for SDR50 This bit should be set if the application wants Tuning be used for SDR50 Modes. The Core operates with or without tuning for SDR50 mode as long as the Clock can be manually tuned using tap delay.
12	RESERVED	R	0h	Reserved
11-8	RETUNINGTIMERCNT	R/W	4h	Timer Count for Re-Tuning This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 4h disables Re-Tuning Timer.
7	TYPE4SUPPORT	R/W	0h	Driver Type 4 Support This bit should be set based on whether Driver Type 4 for 1.8 Signalling is supported or not.
6	DDRIVERSUPPORT	R/W	0h	Driver Type D Support This bit should be set based on whether Driver Type D for 1.8 Signalling is supported or not.
5	CDRIVERSUPPORT	R/W	0h	Driver Type C Support This bit should be set based on whether Driver Type C for 1.8 Signalling is supported or not.
4	ADRIVERSUPPORT	R/W	0h	Driver Type A Support This bit should be set based on whether Driver Type A for 1.8 Signalling is supported or not.
3	RESERVED	R	0h	Reserved
2	DDR50SUPPORT	R/W	1h	DDR50 Support Suggested Value is 1h (The Core supports DDR50 mode of operation). Optionally can be set to 0h if the application doesn't want to support DDR50.
1	SDR104SUPPORT	R/W	1h	SDR104 Support. Suggested Value is 1h (The Core supports SDR104 mode of operation). Optionally can be set to 0h if the application doesn't want to support SDR104. Note: SDR104 mode is not supported (see , <i>MMCSDB Not Supported Features</i>).
0	SDR50SUPPORT	R/W	1h	SDR50 Support. Suggested Value is 1h (The Core supports SDR50 mode of operation). Optionally can be set to 0h if the application doesn't want to support SDR50.

Table 18-408. Register Call Summary for MMCSDB12_SS_CTL_CFG_3_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers: \[0\]](#)
- [MMCSDB12_SS_CTL_CFG_3_REG Register \(Offset = 18h\) \[reset = 18000407h\]: \[0\]](#)

18.5.5 MMCSDB12_SS_CTL_CFG_4_REG Register (Offset = 1Ch) [reset = 0h]

MMCSDB12_SS_CTL_CFG_4_REG is shown in Figure 18-162 and described in Table 18-410.

Return to [Summary Table](#).

The Controller Config 4 Register contains various fields to control the configuration ports on the Host Controller. This register sets the LSB fields in the MMCSDB12_MAX_CURRENT_CAP register inside the Host Controller.

Table 18-409. MMCSDB12_SS_CTL_CFG_4_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 801Ch
MMCSDB2_SS_CFG	04F9 001Ch

Figure 18-162. MMCSDB12_SS_CTL_CFG_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MAXCURRENT1P8V							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXCURRENT3P0V								MAXCURRENT3P3V							
R/W-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-410. MMCSDB12_SS_CTL_CFG_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	MAXCURRENT1P8V	R/W	0h	Maximum Current For 1.8 V
15-8	MAXCURRENT3P0V	R/W	0h	Maximum Current For 3.0 V
7-0	MAXCURRENT3P3V	R/W	0h	Maximum Current For 3.3 V

Table 18-411. Register Call Summary for MMCSDB12_SS_CTL_CFG_4_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers: \[0\]](#)
- [MMCSDB12_SS_CTL_CFG_4_REG Register \(Offset = 1Ch\) \[reset = 0h\]: \[0\]](#)

18.5.6 MMCSD12_SS_CTL_CFG_5_REG Register (Offset = 20h) [reset = 0h]

MMCSD12_SS_CTL_CFG_5_REG is shown in [Figure 18-163](#) and described in [Table 18-413](#).

Return to [Summary Table](#).

The Controller Config 5 Register contains various fields to control the configuration ports on the Host Controller. This register sets the MSB fields in the [MMCSD12_MAX_CURRENT_CAP](#) register inside the Host Controller.

**Table 18-412. MMCSD12_SS_CTL_CFG_5_REG
Instances**

Instance	Physical Address
MMCSD1_SS_CFG	04FB 8020h
MMCSD2_SS_CFG	04F9 0020h

Figure 18-163. MMCSD12_SS_CTL_CFG_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MAXCURRENTVDD2							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-413. MMCSD12_SS_CTL_CFG_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	MAXCURRENTVDD2	R/W	0h	Maximum Current For 1.8 V (VDD2)

Table 18-414. Register Call Summary for MMCSD12_SS_CTL_CFG_5_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)
- [MMCSD12_SS_CTL_CFG_5_REG Register \(Offset = 20h\) \[reset = 0h\]: \[0\]](#)

18.5.7 MMCSDB12_SS_CTL_CFG_6_REG Register (Offset = 24h) [reset = 100h]

MMCSDB12_SS_CTL_CFG_6_REG is shown in Figure 18-164 and described in Table 18-416.

Return to [Summary Table](#).

The Controller Config 6 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSDB0_PRESET_VALUE1 to MMCSDB12_PRESET_VALUE10) for Initialization inside the Host Controller.

Table 18-415. MMCSDB12_SS_CTL_CFG_6_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 8024h
MMCSDB2_SS_CFG	04F9 0024h

Figure 18-164. MMCSDB12_SS_CTL_CFG_6_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																INITPRESETVAL															
R-0h																R/W-100h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-416. MMCSDB12_SS_CTL_CFG_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	INITPRESETVAL	R/W	100h	Preset Value For Initialization

Table 18-417. Register Call Summary for MMCSDB12_SS_CTL_CFG_6_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers](#): [0]
- [MMCSDB12_SS_CTL_CFG_6_REG Register \(Offset = 24h\) \[reset = 100h\]](#): [0]

18.5.8 MMCSD12_SS_CTL_CFG_7_REG Register (Offset = 28h) [reset = 4h]

MMCSD12_SS_CTL_CFG_7_REG is shown in [Figure 18-165](#) and described in [Table 18-419](#).

Return to [Summary Table](#).

The Controller Config 7 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCSD0_PRESET_VALUE1](#) to [MMCSD12_PRESET_VALUE10](#)) for Default Speed inside the Host Controller.

Table 18-418. MMCSD12_SS_CTL_CFG_7_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	04FB 8028h
MMCSD2_SS_CFG	04F9 0028h

Figure 18-165. MMCSD12_SS_CTL_CFG_7_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DSPDPRESETVAL															
R-0h																R/W-4h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-419. MMCSD12_SS_CTL_CFG_7_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	DSPDPRESETVAL	R/W	4h	Preset Value For Default Speed

Table 18-420. Register Call Summary for MMCSD12_SS_CTL_CFG_7_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers](#): [0]
- [MMCSD12_SS_CTL_CFG_7_REG Register \(Offset = 28h\) \[reset = 4h\]](#): [0]

18.5.9 MMCSDB12_SS_CTL_CFG_8_REG Register (Offset = 2Ch) [reset = 2h]

MMCSDB12_SS_CTL_CFG_8_REG is shown in Figure 18-166 and described in Table 18-422.

Return to [Summary Table](#).

The Controller Config 8 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSDB0_PRESET_VALUE1 to MMCSDB12_PRESET_VALUE10) for High Speed inside the Host Controller.

Table 18-421. MMCSDB12_SS_CTL_CFG_8_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 802Ch
MMCSDB2_SS_CFG	04F9 002Ch

Figure 18-166. MMCSDB12_SS_CTL_CFG_8_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HSPDPRESETVAL															
R-0h																R/W-2h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-422. MMCSDB12_SS_CTL_CFG_8_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	HSPDPRESETVAL	R/W	2h	Preset Value For High Speed

Table 18-423. Register Call Summary for MMCSDB12_SS_CTL_CFG_8_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers](#): [0]
- [MMCSDB12_SS_CTL_CFG_8_REG Register \(Offset = 2Ch\) \[reset = 2h\]](#): [0]

18.5.10 MMCSD12_SS_CTL_CFG_9_REG Register (Offset = 30h) [reset = 4h]

MMCSD12_SS_CTL_CFG_9_REG is shown in [Figure 18-167](#) and described in [Table 18-425](#).

Return to [Summary Table](#).

The Controller Config 9 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD12_PRESET_VALUE10) for SDR12 inside the Host Controller.

**Table 18-424. MMCSD12_SS_CTL_CFG_9_REG
Instances**

Instance	Physical Address
MMCSD1_SS_CFG	04FB 8030h
MMCSD2_SS_CFG	04F9 0030h

Figure 18-167. MMCSD12_SS_CTL_CFG_9_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDR12PRESETVAL											
R-0h				R/W-4h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-425. MMCSD12_SS_CTL_CFG_9_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR12PRESETVAL	R/W	4h	Preset Value For SDR12

Table 18-426. Register Call Summary for MMCSD12_SS_CTL_CFG_9_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)
- [MMCSD12_SS_CTL_CFG_9_REG Register \(Offset = 30h\) \[reset = 4h\]: \[0\]](#)

18.5.11 MMCSd12_SS_CTL_CFG_10_REG Register (Offset = 34h) [reset = 2h]

MMCSd12_SS_CTL_CFG_10_REG is shown in [Figure 18-168](#) and described in [Table 18-428](#).

Return to [Summary Table](#).

The Controller Config 10 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCSd0_PRESET_VALUE1](#) to [MMCSd12_PRESET_VALUE10](#)) for SDR25 inside the Host Controller.

Table 18-427. MMCSd12_SS_CTL_CFG_10_REG Instances

Instance	Physical Address
MMCSd1_SS_CFG	04FB 8034h
MMCSd2_SS_CFG	04F9 0034h

Figure 18-168. MMCSd12_SS_CTL_CFG_10_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDR25PRESETVAL											
R-0h				R/W-2h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-428. MMCSd12_SS_CTL_CFG_10_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR25PRESETVAL	R/W	2h	Preset Value For SDR25

Table 18-429. Register Call Summary for MMCSd12_SS_CTL_CFG_10_REG

MMCSd1 / MMCSd2 Subsystem Registers

- [MMCSd1 / MMCSd2 Subsystem Registers: \[0\]](#)
- [MMCSd12_SS_CTL_CFG_10_REG Register \(Offset = 34h\) \[reset = 2h\]: \[0\]](#)

18.5.12 MMCSD12_SS_CTL_CFG_11_REG Register (Offset = 38h) [reset = 1h]

MMCSD12_SS_CTL_CFG_11_REG is shown in [Figure 18-169](#) and described in [Table 18-431](#).

Return to [Summary Table](#).

The Controller Config 11 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSD0_PRESET_VALUE1 to MMCSD12_PRESET_VALUE10) for SDR50 inside the Host Controller.

Table 18-430. MMCSD12_SS_CTL_CFG_11_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	04FB 8038h
MMCSD2_SS_CFG	04F9 0038h

Figure 18-169. MMCSD12_SS_CTL_CFG_11_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDR50PRESETVAL											
R-0h				R/W-1h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-431. MMCSD12_SS_CTL_CFG_11_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR50PRESETVAL	R/W	1h	Preset Value For SDR50

Table 18-432. Register Call Summary for MMCSD12_SS_CTL_CFG_11_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)
- [MMCSD12_SS_CTL_CFG_11_REG Register \(Offset = 38h\) \[reset = 1h\]: \[0\]](#)

18.5.13 MMCSDB12_SS_CTL_CFG_12_REG Register (Offset = 3Ch) [reset = 0h]

MMCSDB12_SS_CTL_CFG_12_REG is shown in Figure 18-170 and described in Table 18-434.

Return to [Summary Table](#).

The Controller Config 12 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers (MMCSDB0_PRESET_VALUE1 to MMCSDB12_PRESET_VALUE10) for SDR104 inside the Host Controller.

Table 18-433. MMCSDB12_SS_CTL_CFG_12_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 803Ch
MMCSDB2_SS_CFG	04F9 003Ch

Figure 18-170. MMCSDB12_SS_CTL_CFG_12_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDR104PRESETVAL											
R-0h				R/W-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-434. MMCSDB12_SS_CTL_CFG_12_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	SDR104PRESETVAL	R/W	0h	Preset Value For SDR104

Table 18-435. Register Call Summary for MMCSDB12_SS_CTL_CFG_12_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers: \[0\]](#)
- [MMCSDB12_SS_CTL_CFG_12_REG Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)

18.5.14 MMCSD12_SS_CTL_CFG_13_REG Register (Offset = 40h) [reset = 2h]

MMCSD12_SS_CTL_CFG_13_REG is shown in [Figure 18-171](#) and described in [Table 18-437](#).

Return to [Summary Table](#).

The Controller Config 13 Register contains various fields to control the configuration ports on the Host Controller. This register sets the fields in the Preset Values registers ([MMCSD0_PRESET_VALUE1](#) to [MMCSD12_PRESET_VALUE10](#)) for DDR50 inside the Host Controller.

Table 18-436. MMCSD12_SS_CTL_CFG_13_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	04FB 8040h
MMCSD2_SS_CFG	04F9 0040h

Figure 18-171. MMCSD12_SS_CTL_CFG_13_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				DDR50PRESETVAL											
R-0h				R/W-2h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-437. MMCSD12_SS_CTL_CFG_13_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-0	DDR50PRESETVAL	R/W	2h	Preset Value For DDR50

Table 18-438. Register Call Summary for MMCSD12_SS_CTL_CFG_13_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)
- [MMCSD12_SS_CTL_CFG_13_REG Register \(Offset = 40h\) \[reset = 2h\]: \[0\]](#)

18.5.15 MMCSDB12_SS_CTL_STAT_1_REG Register (Offset = 60h) [reset = 80000000h]

MMCSDB12_SS_CTL_STAT_1_REG is shown in Figure 18-172 and described in Table 18-440.

Return to [Summary Table](#).

The Controller Status 1 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 18-439. MMCSDB12_SS_CTL_STAT_1_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 8060h
MMCSDB2_SS_CFG	04F9 0060h

Figure 18-172. MMCSDB12_SS_CTL_STAT_1_REG Register

31	30	29	28	27	26	25	24
SDHC_CMDIDLE	RESERVED						
R-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DMADEBUGBUS							
R-0h							
7	6	5	4	3	2	1	0
DMADEBUGBUS							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-440. MMCSDB12_SS_CTL_STAT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SDHC_CMDIDLE	R	1h	Idle signal to enable software to gate off the clocks
30-16	RESERVED	R	0h	Reserved
15-0	DMADEBUGBUS	R	0h	DMA_CTRL Debug Bus

Table 18-441. Register Call Summary for MMCSDB12_SS_CTL_STAT_1_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers: \[0\]](#)
- [MMCSDB12_SS_CTL_STAT_1_REG Register \(Offset = 60h\) \[reset = 80000000h\]: \[0\]](#)

18.5.16 MMCSD12_SS_CTL_STAT_2_REG Register (Offset = 64h) [reset = 10h]

MMCSD12_SS_CTL_STAT_2_REG is shown in Figure 18-173 and described in Table 18-443.

Return to [Summary Table](#).

The Controller Status 2 Register contains various fields to reflect the status of the debug ports on the Host Controller.

**Table 18-442. MMCSD12_SS_CTL_STAT_2_REG
Instances**

Instance	Physical Address
MMCSD1_SS_CFG	04FB 8064h
MMCSD2_SS_CFG	04F9 0064h

Figure 18-173. MMCSD12_SS_CTL_STAT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMDDEBUGBUS															
R-0h																R-10h															

LEGEND: R = Read Only; -n = value after reset

Table 18-443. MMCSD12_SS_CTL_STAT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CMDDEBUGBUS	R	10h	CMD_CTRL Debug Bus

Table 18-444. Register Call Summary for MMCSD12_SS_CTL_STAT_2_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)
- [MMCSD12_SS_CTL_STAT_2_REG Register \(Offset = 64h\) \[reset = 10h\]: \[0\]](#)

18.5.17 MMCSDB12_SS_CTL_STAT_3_REG Register (Offset = 68h) [reset = 0h]

MMCSDB12_SS_CTL_STAT_3_REG is shown in Figure 18-174 and described in Table 18-446.

Return to [Summary Table](#).

The Controller Status 3 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 18-445. MMCSDB12_SS_CTL_STAT_3_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 8068h
MMCSDB2_SS_CFG	04F9 0068h

Figure 18-174. MMCSDB12_SS_CTL_STAT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TXDDEBUGBUS															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 18-446. MMCSDB12_SS_CTL_STAT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TXDDEBUGBUS	R	0h	TXD_CTRL Debug Bus

Table 18-447. Register Call Summary for MMCSDB12_SS_CTL_STAT_3_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers](#): [0]
- [MMCSDB12_SS_CTL_STAT_3_REG Register \(Offset = 68h\) \[reset = 0h\]](#): [0]

18.5.18 MMCSD12_SS_CTL_STAT_4_REG Register (Offset = 6Ch) [reset = 0h]

MMCSD12_SS_CTL_STAT_4_REG is shown in Figure 18-175 and described in Table 18-449.

Return to [Summary Table](#).

The Controller Status 4 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 18-448. MMCSD12_SS_CTL_STAT_4_REG Instances

Instance	Physical Address
MMCSD1_SS_CFG	04FB 806Ch
MMCSD2_SS_CFG	04F9 006Ch

Figure 18-175. MMCSD12_SS_CTL_STAT_4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RXDDEBUGBUS0															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 18-449. MMCSD12_SS_CTL_STAT_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RXDDEBUGBUS0	R	0h	RXD_CTRL Debug Bus (SD CLK)

Table 18-450. Register Call Summary for MMCSD12_SS_CTL_STAT_4_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers](#): [0]
- [MMCSD12_SS_CTL_STAT_4_REG Register \(Offset = 6Ch\) \[reset = 0h\]](#): [0]

18.5.19 MMCSDB12_SS_CTL_STAT_5_REG Register (Offset = 70h) [reset = 8h]

MMCSDB12_SS_CTL_STAT_5_REG is shown in Figure 18-176 and described in Table 18-452.

Return to [Summary Table](#).

The Controller Status 5 Register contains various fields to reflect the status of the debug ports on the Host Controller.

Table 18-451. MMCSDB12_SS_CTL_STAT_5_REG Instances

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 8070h
MMCSDB2_SS_CFG	04F9 0070h

Figure 18-176. MMCSDB12_SS_CTL_STAT_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RXDDEBUGBUS1															
R-0h																R-8h															

LEGEND: R = Read Only; -n = value after reset

Table 18-452. MMCSDB12_SS_CTL_STAT_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	RXDDEBUGBUS1	R	8h	RXD_CTRL Debug Bus (RX CLK)

Table 18-453. Register Call Summary for MMCSDB12_SS_CTL_STAT_5_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers](#): [0]
- [MMCSDB12_SS_CTL_STAT_5_REG Register \(Offset = 70h\) \[reset = 8h\]](#): [0]

18.5.20 MMCSDB12_SS_CTL_STAT_6_REG Register (Offset = 74h) [reset = 0h]

MMCSDB12_SS_CTL_STAT_6_REG is shown in Figure 18-177 and described in Table 18-455.

Return to [Summary Table](#).

The Controller Status 6 Register contains various fields to reflect the status of the debug ports on the Host Controller.

**Table 18-454. MMCSDB12_SS_CTL_STAT_6_REG
Instances**

Instance	Physical Address
MMCSDB1_SS_CFG	04FB 8074h
MMCSDB2_SS_CFG	04F9 0074h

Figure 18-177. MMCSDB12_SS_CTL_STAT_6_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TUNDEBUBBUS															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 18-455. MMCSDB12_SS_CTL_STAT_6_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	TUNDEBUBBUS	R	0h	TUN_CTRL Debug Bus

Table 18-456. Register Call Summary for MMCSDB12_SS_CTL_STAT_6_REG

MMCSDB1 / MMCSDB2 Subsystem Registers

- [MMCSDB1 / MMCSDB2 Subsystem Registers](#): [0]
- [MMCSDB12_SS_CTL_STAT_6_REG Register \(Offset = 74h\) \[reset = 0h\]](#): [0]

18.5.21 MMCS D12_SS_PHY_CTRL_1_REG Register (Offset = 100h) [reset = 80010000h]

MMCS D12_SS_PHY_CTRL_1_REG is shown in Figure 18-178 and described in Table 18-458.

Return to [Summary Table](#).

The PHY Control 1 Register contains various fields to control the ports on the Host Controller PHY.

Table 18-457. MMCS D12_SS_PHY_CTRL_1_REG Instances

Instance	Physical Address
MMCS D1_SS_CFG	04FB 8100h
MMCS D2_SS_CFG	04F9 0100h

Figure 18-178. MMCS D12_SS_PHY_CTRL_1_REG Register

31	30	29	28	27	26	25	24
IOMUX_ENABLE	RESERVED						
R/W-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-458. MMCS D12_SS_PHY_CTRL_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IOMUX_ENABLE	R/W	1h	IO Mux Enable Set 1h for GPIO. Set 0h for MMCS D.
30-0	RESERVED	R	0h	Reserved

Table 18-459. Register Call Summary for MMCS D12_SS_PHY_CTRL_1_REG

MMCS D1 / MMCS D2 Subsystem Registers

- [MMCS D1 / MMCS D2 Subsystem Registers: \[0\]](#)
- [MMCS D12_SS_PHY_CTRL_1_REG Register \(Offset = 100h\) \[reset = 80010000h\]: \[0\]](#)

18.5.22 MMCS D12_SS_PHY_CTRL_4_REG Register (Offset = 10Ch) [reset = 0h]

MMCS D12_SS_PHY_CTRL_4_REG is shown in Figure 18-179 and described in Table 18-461.

Return to [Summary Table](#).

The PHY Control 4 Register contains various fields to control the ports on the Host Controller PHY.

**Table 18-460. MMCS D12_SS_PHY_CTRL_4_REG
Instances**

Instance	Physical Address
MMCS D1_SS_CFG	04FB 810Ch
MMCS D2_SS_CFG	04F9 010Ch

Figure 18-179. MMCS D12_SS_PHY_CTRL_4_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED			OTAPDLYENA	RESERVED			
R-0h			R/W-0h	R-0h			
15	14	13	12	11	10	9	8
OTAPDLYSEL				RESERVED		ITAPCHGWIN	ITAPDLYENA
R/W-0h				R-0h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			ITAPDLYSEL				
R-0h			R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-461. MMCS D12_SS_PHY_CTRL_4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20	OTAPDLYENA	R/W	0h	Output Tap Delay Enable Enables manual control of the TX clock tap delay, for clocking the final stage flops for maintaining Hold requirements on EMMC Interface.
19-16	RESERVED	R	0h	Reserved
15-12	OTAPDLYSEL	R/W	0h	Output Tap Delay Select Manual control of the TX clock tap delay for clocking the final stage flops for maintaining Hold requirements on EMMC Interface.
11-10	RESERVED	R	0h	Reserved
9	ITAPCHGWIN	R/W	0h	Input Tap Change Window It gets asserted by the controller while changing the itapdlysel. Used to gate of the RX clock during switching the clock source while tap is changing to avoid clock glitches.
8	ITAPDLYENA	R/W	0h	Input Tap Delay Enable This is used for the manual control of the RX clock Tap Delay.
7-5	RESERVED	R	0h	Reserved
4-0	ITAPDLYSEL	R/W	0h	Input Tap Delay Select Manual control of the RX clock Tap Delay.

Table 18-462. Register Call Summary for MMCSD12_SS_PHY_CTRL_4_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD12_SS_PHY_CTRL_4_REG Register \(Offset = 10Ch\) \[reset = 0h\]: \[0\]](#)
- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)

18.5.23 MMCSD12_SS_PHY_CTRL_5_REG Register (Offset = 110h) [reset = 0h]

MMCSD12_SS_PHY_CTRL_5_REG is shown in [Figure 18-180](#) and described in [Table 18-464](#).

Return to [Summary Table](#).

The PHY Control 5 Register contains various fields to control the ports on the Host Controller PHY.

**Table 18-463. MMCSD12_SS_PHY_CTRL_5_REG
Instances**

Instance	Physical Address
MMCSD1_SS_CFG	04FB 8110h
MMCSD2_SS_CFG	04F9 0110h

Figure 18-180. MMCSD12_SS_PHY_CTRL_5_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CLKBUFSEL		
R-0h													R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-464. MMCSD12_SS_PHY_CTRL_5_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLKBUFSEL	R/W	0h	Clock Delay Buffer Select. Selects one of the eight taps in the CLK Delay Buffer based on PVT variation.

Table 18-465. Register Call Summary for MMCSD12_SS_PHY_CTRL_5_REG

MMCSD1 / MMCSD2 Subsystem Registers

- [MMCSD1 / MMCSD2 Subsystem Registers: \[0\]](#)
- [MMCSD12_SS_PHY_CTRL_5_REG Register \(Offset = 110h\) \[reset = 0h\]: \[0\]](#)

18.6 MMCSDB1 / MMCSDB2 Host Controller Registers

lists the memory-mapped registers for the MMCSDB1 / MMCSDB2 Host Controller. All register offset addresses not listed in should be considered as reserved locations and the register contents should not be modified.

Note

UHSII is not supported. For more information, see *Not Supported Features*.

Table 18-466. MMCSDB1 / MMCSDB2 HOST CONTROLLER Instances

Instance	Base Address
MMCSDB1_CTL_CFG	04FB 0000h
MMCSDB2_CTL_CFG	04F9 8000h

Table 18-467. MMCSDB1 / MMCSDB2 Host Controller Registers

Offset	Acronym	Register Name	MMCSDB1_CTL_CFG Physical Address	MMCSDB2_CTL_CFG Physical Address
Host Controller Interface Register				
0h	MMCSDB12_SDMA_SYS_ADDR_LO	32-bit Block Count/SDMA System Address Low Register	04FB 0000h	04F9 8000h
2h	MMCSDB12_SDMA_SYS_ADDR_HI	32-bit Block Count/SDMA System Address High Register	04FB 0002h	04F9 8002h
4h	MMCSDB12_BLOCK_SIZE	16-bit Block Size Register	04FB 0004h	04F9 8004h
6h	MMCSDB12_BLOCK_COUNT	16-bit Block Count Register	04FB 0006h	04F9 8006h
8h	MMCSDB12_ARGUMENT1_LO	Argument1 Low Register	04FB 0008h	04F9 8008h
Ah	MMCSDB12_ARGUMENT1_HI	Argument1 High Register	04FB 000Ah	04F9 800Ah
Ch	MMCSDB12_TRANSFER_MODE	Transfer Mode Register	04FB 000Ch	04F9 800Ch
Eh	MMCSDB12_COMMAND	Command Register	04FB 000Eh	04F9 800Eh
10h to 1Eh	MMCSDB12_RESPONSE_0 to MMCSDB12_RESPONSE_7	Response Register	04FB 0010h to 04FB 001Eh	04F9 8010h to 04F9 801Eh
20h	MMCSDB12_DATA_PORT	Buffer Data Port Register	04FB 0020h	04F9 8020h
24h	MMCSDB12_PRESENTSTATE	Present State Register	04FB 0024h	04F9 8024h
28h	MMCSDB12_HOST_CONTROL1	Host Control 1 Register	04FB 0028h	04F9 8028h
29h	MMCSDB12_POWER_CONTROL	Power Control Register	04FB 0029h	04F9 8029h
2Ah	MMCSDB12_BLOCK_GAP_CONTROL	Block Gap Control Register	04FB 002Ah	04F9 802Ah
2Bh	MMCSDB12_WAKEUP_CONTROL	Wakeup Control Register	04FB 002Bh	04F9 802Bh
2Ch	MMCSDB12_CLOCK_CONTROL	Clock Control Register	04FB 002Ch	04F9 802Ch
2Eh	MMCSDB12_TIMEOUT_CONTROL	Timeout Control Register	04FB 002Eh	04F9 802Eh
2Fh	MMCSDB12_SOFTWARE_RESET	Software Reset Register	04FB 002Fh	04F9 802Fh
30h	MMCSDB12_NORMAL_INTR_STS	Normal Interrupt Status Register	04FB 0030h	04F9 8030h
32h	MMCSDB12_ERROR_INTR_STS	Error Interrupt Status Register	04FB 0032h	04F9 8032h
34h	MMCSDB12_NORMAL_INTR_STS_ENA	Normal Interrupt Status Enable Register	04FB 0034h	04F9 8034h
36h	MMCSDB12_ERROR_INTR_STS_ENA	Error Interrupt Status Enable Register	04FB 0036h	04F9 8036h
38h	MMCSDB12_NORMAL_INTR_SIG_ENA	Normal Interrupt Signal Enable Register	04FB 0038h	04F9 8038h
3Ah	MMCSDB12_ERROR_INTR_SIG_ENA	Error Interrupt Signal Enable Register	04FB 003Ah	04F9 803Ah

Table 18-467. MMCSD1 / MMCSD2 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCSD1_CTL_CFG Physical Address	MMCSD2_CTL_CFG Physical Address
3Ch	MMCSD12_AUTOCMD_ERR_STS	Auto CMD Error Status Register	04FB 003Ch	04F9 803Ch
3Eh	MMCSD12_HOST_CONTROL2	Host Control 2 Register	04FB 003Eh	04F9 803Eh
40h	MMCSD12_CAPABILITIES	Capabilities Register	04FB 0040h	04F9 8040h
48h	MMCSD12_MAX_CURRENT_CAP	Maximum Current Capabilities Register	04FB 0048h	04F9 8048h
50h	MMCSD12_FORCE_EVNT_ACMD_ERR_STS	Force Event Register for Auto CMD Error Status	04FB 0050h	04F9 8050h
52h	MMCSD12_FORCE_EVNT_ERR_INT_STS	Force Event Register for Error Interrupt Status	04FB 0052h	04F9 8052h
54h	MMCSD12_ADMA_ERR_STATUS	ADMA Error Status Register	04FB 0054h	04F9 8054h
58h	MMCSD12_ADMA_SYS_ADDRESS	ADMA System Address Register	04FB 0058h	04F9 8058h
60h	MMCSD12_PRESET_VALUE0	Preset Values 0 Register	04FB 0060h	04F9 8060h
62h	MMCSD12_PRESET_VALUE1	Preset Values 1 Register	04FB 0062h	04F9 8062h
64h	MMCSD12_PRESET_VALUE2	Preset Values 2 Register	04FB 0064h	04F9 8064h
66h	MMCSD12_PRESET_VALUE3	Preset Values 3 Register	04FB 0066h	04F9 8066h
68h	MMCSD12_PRESET_VALUE4	Preset Values 4 Register	04FB 0068h	04F9 8068h
6Ah	MMCSD12_PRESET_VALUE5	Preset Values 5 Register	04FB 006Ah	04F9 806Ah
6Ch	MMCSD12_PRESET_VALUE6	Preset Values 6 Register	04FB 006Ch	04F9 806Ch
6Eh	MMCSD12_PRESET_VALUE7	Preset Values 7 Register	04FB 006Eh	04F9 806Eh
72h	MMCSD12_PRESET_VALUE8	Preset Values 8 Register	04FB 0072h	04F9 8072h
74h	MMCSD12_PRESET_VALUE10	Preset Values 10 Register	04FB 0074h	04F9 8074h
78h	MMCSD12_ADMA3_DESC_ADDRESS	ADMA3 Integrated Descriptor Address Register	04FB 0078h	04F9 8078h
UHS-II Registers				
80h	MMCSD12_UHS2_BLOCK_SIZE	UHS-II Block Size Register	04FB 0080h	04F9 8080h
84h	MMCSD12_UHS2_BLOCK_COUNT	UHS-II Block Count Register	04FB 0084h	04F9 8084h
88h to 9Bh	MMCSD12_UHS2_COMMAND_PKT_0 to MMCSD12_UHS2_COMMAND_PKT_19	UHS-II Command Packet Register	04FB 0088h to 04FB 009Bh	04F9 8088h to 04F9 809Bh
9Ch	MMCSD12_UHS2_XFER_MODE	UHS-II Transfer Mode Register	04FB 009Ch	04F9 809Ch
9Eh	MMCSD12_UHS2_COMMAND	UHS-II Command Register	04FB 009Eh	04F9 809Eh
A0h to B3h	MMCSD12_UHS2_RESPONSE_0 to MMCSD12_UHS2_RESPONSE_19	UHS-II Response Register	04FB 00A0h to 04FB 00B3h	04F9 80A0h to 04F9 80B3h
B4h	MMCSD12_UHS2_MESSAGE_SELECT	UHS-II Message Select Register	04FB 00B4h	04F9 80B4h
B8h	MMCSD12_UHS2_MESSAGE	UHS-II Message Register	04FB 00B8h	04F9 80B8h
BCh	MMCSD12_UHS2_DEVICE_INTR_STATUS	UHS-II Device Interrupt Status Register	04FB 00BCh	04F9 80BCh
BEh	MMCSD12_UHS2_DEVICE_SELECT	UHS-II Device Select Register	04FB 00BEh	04F9 80BEh
BFh	MMCSD12_UHS2_DEVICE_INT_CODE	UHS-II Device Interrupt Code Register	04FB 00BFh	04F9 80BFh
C0h	MMCSD12_UHS2_SOFTWARE_RESET	UHS-II Software Reset Register	04FB 00C0h	04F9 80C0h
C2h	MMCSD12_UHS2_TIMER_CONTROL	UHS-II Timeout Control Register	04FB 00C2h	04F9 80C2h

Table 18-467. MMCSd1 / MMCSd2 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCSd1_CTL_CFG Physical Address	MMCSd2_CTL_CFG Physical Address
C4h	MMCSd12_UHS2_ERR_INTR_STS	UHS-II Error Interrupt Status Register	04FB 00C4h	04F9 80C4h
C8h	MMCSd12_UHS2_ERR_INTR_STS_ENA	UHS-II Error Interrupt Status Enable Register	04FB 00C8h	04F9 80C8h
CCh	MMCSd12_UHS2_ERR_INTR_SIG_ENA	UHS-II Error Interrupt Signal Enable Register	04FB 00CCh	04F9 80CCh
E0h	MMCSd12_UHS2_SETTINGS_PTR	Pointer for UHS-II Settings Register	04FB 00E0h	04F9 80E0h
E2h	MMCSd12_UHS2_CAPABILITIES_PTR	Pointer for UHS-II Host Capabilities Register	04FB 00E2h	04F9 80E2h
E4h	MMCSd12_UHS2_TEST_PTR	Pointer for UHS-II Test Register	04FB 00E4h	04F9 80E4h
E6h	MMCSd12_SHARED_BUS_CTRL_PTR	Pointer for Embedded Control Register	04FB 00E6h	04F9 80E6h
E8h	MMCSd12_VENDOR_SPECIFIC_PTR	Pointer for Vendor Specific Area Register	04FB 00E8h	04F9 80E8h
F4h	MMCSd12_BOOT_TIMEOUT_CONTROL	Boot Timeout Control Register	04FB 00F4h	04F9 80F4h
F8h	MMCSd12_VENDOR_REGISTER	Vendor Register	04FB 00F8h	04F9 80F8h
FCh	MMCSd12_SLOT_INT_STS	Slot Interrupt Status Register	04FB 00FCh	04F9 80FCh
FEh	MMCSd12_HOST_CONTROLLER_VER	Host Controller Version Register	04FB 00FEh	04F9 80FEh
100h	MMCSd12_UHS2_GEN_SETTINGS	UHS-II General Settings Register	04FB 0100h	04F9 8100h
104h	MMCSd12_UHS2_PHY_SETTINGS	UHS-II PHY Settings Register	04FB 0104h	04F9 8104h
108h	MMCSd12_UHS2_LNK_TRN_SETTINGS	UHS-II LINK/TRAN Settings Register	04FB 0108h	04F9 8108h
110h	MMCSd12_UHS2_GEN_CAP	UHS-II General Capabilities Register	04FB 0110h	04F9 8110h
114h	MMCSd12_UHS2_PHY_CAP	UHS-II PHY Capabilities Register	04FB 0114h	04F9 8114h
118h	MMCSd12_UHS2_LNK_TRN_CAP	UHS-II LINK/TRAN Capabilities Register	04FB 0118h	04F9 8118h
120h	MMCSd12_FORCE_UHSII_ERR_INT_STS	Force Event for UHS-II Error Interrupt Status Register	04FB 0120h	04F9 8120h
Command Queue Registers				
200h	MMCSd12_CQ_VERSION	Command Queueing Version Register	04FB 0200h	04F9 8200h
204h	MMCSd12_CQ_CAPABILITIES	Command Queueing Capabilities Register	04FB 0204h	04F9 8204h
208h	MMCSd12_CQ_CONFIG	Command Queueing Configuration Register	04FB 0208h	04F9 8208h
20Ch	MMCSd12_CQ_CONTROL	Command Queueing Control Register	04FB 020Ch	04F9 820Ch
210h	MMCSd12_CQ_INTR_STS	Command Queueing Interrupt Status Register	04FB 0210h	04F9 8210h
214h	MMCSd12_CQ_INTR_STS_ENA	Command Queueing Interrupt Status Enabled Register	04FB 0214h	04F9 8214h
218h	MMCSd12_CQ_INTR_SIG_ENA	Command Queueing Interrupt Signal Enable Register	04FB 0218h	04F9 8218h

Table 18-467. MMCSD1 / MMCSD2 Host Controller Registers (continued)

Offset	Acronym	Register Name	MMCSD1_CTL_CFG Physical Address	MMCSD2_CTL_CFG Physical Address
21Ch	MMCSD12_CQ_INTR_COALESCING	Interrupt Coalescing Register	04FB 021Ch	04F9 821Ch
220h	MMCSD12_CQ_TDL_BASE_ADDR	Command Queueing Task Descriptor List Base Address Low Register	04FB 0220h	04F9 8220h
224h	MMCSD12_CQ_TDL_BASE_ADDR_UPBITS	Command Queueing Task Descriptor List Base Address High Register	04FB 0224h	04F9 8224h
228h	MMCSD12_CQ_TASK_DOOR_BELL	Command Queueing Task Doorbell Register	04FB 0228h	04F9 8228h
22Ch	MMCSD12_CQ_TASK_COMP_NOTIF	Command Queueing Task Doorbell Notification Register	04FB 022Ch	04F9 822Ch
230h	MMCSD12_CQ_DEV_QUEUE_STATUS	Command Queueing Device Queue Status Register	04FB 0230h	04F9 8230h
234h	MMCSD12_CQ_DEV_PENDING_TASKS	Command Queueing Device Pending Tasks Register	04FB 0234h	04F9 8234h
238h	MMCSD12_CQ_TASK_CLEAR	Command Queueing Task Clear Register	04FB 0238h	04F9 8238h
240h	MMCSD12_CQ_SEND_STS_CONFIG1	Send Status Timer Configuration 1 Register	04FB 0240h	04F9 8240h
244h	MMCSD12_CQ_SEND_STS_CONFIG2	Send Status Configuration 2 Register	04FB 0244h	04F9 8244h
248h	MMCSD12_CQ_DCMD_RESPONSE	Command Response Register for Direct Command Task	04FB 0248h	04F9 8248h
250h	MMCSD12_CQ_RESP_ERR_MASK	Response Mode Error Mask Register	04FB 0250h	04F9 8250h
254h	MMCSD12_CQ_TASK_ERR_INFO	Task Error Information Register	04FB 0254h	04F9 8254h
258h	MMCSD12_CQ_CMD_RESP_INDEX	Command Response Index Register	04FB 0258h	04F9 8258h
25Ch	MMCSD12_CQ_CMD_RESP_ARG	Command Response Argument Register	04FB 025Ch	04F9 825Ch
260h	MMCSD12_CQ_ERROR_TASK_ID	Command Queueing Error Task ID Register	04FB 0260h	04F9 8260h

(1) UHSII is not supported. For more information, see *Not Supported Features*.

18.6.1 MMCSDB12_SDMA_SYS_ADDR_LO Register (Offset = 0h) [reset = 0h]

MMCSDB12_SDMA_SYS_ADDR_LO is shown in [Figure 18-181](#) and described in [Table 18-469](#).

Return to [Summary Table](#).

This register contains the Lower 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

**Table 18-468. MMCSDB12_SDMA_SYS_ADDR_LO
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0000h
MMCSDB2_CTL_CFG	04F9 8000h

Figure 18-181. MMCSDB12_SDMA_SYS_ADDR_LO Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMA_ADDRESS															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-469. MMCS12_SDMA_SYS_ADDR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDMA_ADDRESS	R/W	0h	<p>32-bit Block Count (SDMA System Address) Low</p> <p>When the MMCS12_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h, DMA uses this register as system address in only 32-bit addressing mode. Auto CMD23 cannot be used with SDMA. When the MMCS12_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, SDMA uses the MMCS12_ADMA_SYS_ADDRESS register instead of using this register to support both 32-bit and 64-bit addressing. This register is re-assigned to 32-bit Block Count and then SDMA may use Auto CMD23.</p> <p>(1) SDMA System Address (MMCS12_HOST_CONTROL2[12] HOST_VER40_ENA = 0h)</p> <p>This register contains the system memory address for a SDMA transfer in 32-bit addressing mode. When the Host Controller (HC) stops a SDMA transfer, this register shall point to the system address of the next contiguous data position.</p> <p>It can be accessed only if no transaction is executing (after a transaction has stopped). Reading this register during SDMA transfers may return an invalid value. The Host Driver (HD) shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the MMCS12_BLOCK_SIZE[14-12] SDMA_BUF_SIZE bit field. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (Offset = 3h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by setting the MMCS12_BLOCK_GAP_CONTROL[1] CONTINUE bit, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register (MMCS12_SDMA_SYS_ADDR_LO/MMCS12_SDMA_SYS_ADDR_HI). ADMA does not use this register.</p> <p>(2) 32-bit Block Count (MMCS12_HOST_CONTROL2[12] HOST_VER40_ENA = 1h)</p> <p>Host Controller Version 4.10 re-defines this register as 32-bit Block Count. In version 4.00, this register may be used as 32-bit block count only for Auto CMD23 to set the argument of the CMD23 while executing Auto CMD23.</p> <p>The Host Controller would decrement the block count of this register every block transfer and data transfer stops when the count reaches zero.</p> <p>FFFF FFFFh (4G - 1 Block)</p> <p>....</p> <p>0000 0002h (2 Blocks)</p> <p>0000 0001h (1 Block)</p> <p>0000 0000h (Stop Count)</p> <p>Note: This register should be accessed only when no transaction is executing. Reading this register during data transfers may return invalid value.</p>

18.6.2 MMCSDB12_SDMA_SYS_ADDR_HI Register (Offset = 2h) [reset = 0h]

MMCSDB12_SDMA_SYS_ADDR_HI is shown in [Figure 18-182](#) and described in [Table 18-471](#).

Return to [Summary Table](#).

This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

**Table 18-470. MMCSDB12_SDMA_SYS_ADDR_HI
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0002h
MMCSDB2_CTL_CFG	04F9 8002h

Figure 18-182. MMCSDB12_SDMA_SYS_ADDR_HI Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMA_ADDRESS															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-471. MMCSDB12_SDMA_SYS_ADDR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SDMA_ADDRESS	R/W	0h	32-bit Block Count (SDMA System Address) High This register contains the Upper 16-bit of physical system memory address used for DMA transfers or the second argument for the Auto CMD23 in Host version 3.0 and as 32-bit Block Count in Version 4.10.

18.6.3 MMCSD12_BLOCK_SIZE Register (Offset = 4h) [reset = 0h]

MMCSD12_BLOCK_SIZE is shown in [Figure 18-183](#) and described in [Table 18-473](#).

Return to [Summary Table](#).

This register is used to configure the number of bytes in a data block.

Table 18-472. MMCSD12_BLOCK_SIZE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0004h
MMCSD2_CTL_CFG	04F9 8004h

Figure 18-183. MMCSD12_BLOCK_SIZE Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_SIZE			XFER_BLK_SIZE			
R-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
XFER_BLK_SIZE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-473. MMCSD12_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	SDMA_BUF_SIZE	R/W	0h	<p>Host SDMA Buffer Size</p> <p>To perform long DMA transfer, System Address register (MMCSD12_SDMA_SYS_ADDR_LO/ MMCSD12_SDMA_SYS_ADDR_HI) shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the Host Controller generates the DMA Interrupt to request the Host Driver to update the System Address register (MMCSD12_SDMA_SYS_ADDR_LO/ MMCSD12_SDMA_SYS_ADDR_HI).</p> <p>These bits shall support when the MMCSD12_CAPABILITIES[22] SDMA_SUPPORT bit is set to 1h and this function is active when the MMCSD12_TRANSFER_MODE[0] DMA_ENA bit is set to 1h.</p> <p>0h: 4KB (Detects A11 Carry out) 1h: 8KB (Detects A12 Carry out) 2h: 16KB (Detects A13 Carry out) 3h: 32KB (Detects A14 Carry out) 4h: 64KB (Detects A15 Carry out) 5h: 128KB (Detects A16 Carry out) 6h: 256KB (Detects A17 Carry out) 7h: 512KB (Detects A18 Carry out)</p>

Table 18-473. MMCSDB12_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	XFER_BLK_SIZE	R/W	0h	<p>Transfer Block Size</p> <p>This field specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. It can be accessed only if no transaction is executing (after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored.</p> <p>0000h: No Data Transfer</p> <p>0001h: 1 Byte</p> <p>0002h: 2 Bytes</p> <p>0003h: 3 Bytes</p> <p>0004h: 4 Bytes</p> <p>....</p> <p>01FFh: 511 Bytes</p> <p>0200h: 512 Bytes</p> <p>....</p> <p>0800h: 2048 Bytes</p>

18.6.4 MMCSD12_BLOCK_COUNT Register (Offset = 6h) [reset = 0h]

MMCSD12_BLOCK_COUNT is shown in [Figure 18-184](#) and described in [Table 18-475](#).

Return to [Summary Table](#).

This register is used to configure the number of data blocks.

Table 18-474. MMCSD12_BLOCK_COUNT Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0006h
MMCSD2_CTL_CFG	04F9 8006h

Figure 18-184. MMCSD12_BLOCK_COUNT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XFER_BLK_CNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-475. MMCSD12_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	XFER_BLK_CNT	R/W	0h	<p>16-bit Block Count</p> <p>Host Controller Version 4.10 extends block count to 32-bit. Selection of either 16-bit Block Count register or 32-bit Block Count register is defined as follows:</p> <p>(1) If the MMCSD12_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h or 16-bit Block Count register is set to non-zero, 16-bit Block Count register is selected.</p> <p>(2) If the MMCSD12_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h and 16-bit Block Count register is set to zero, 32-bit Block Count register is selected.</p> <p>Use of 16-bit/32-bit Block Count register is enabled when the MMCSD12_TRANSFER_MODE[1] BLK_CNT_ENA bit is set to 1h and is valid only for multiple block transfers.</p> <p>The Host Driver shall set this register to a value between 1h and the maximum block count. The Host Controller decrements the block count after each block transfer and stops when the count reaches zero. Setting the block count to 0h results in no data blocks is transferred.</p> <p>This register should be accessed only when no transaction is executing (after transactions are stopped).</p> <p>During data transfer, read operations on this register may return an invalid value and write operations are ignored.</p> <p>0000h: Stop Count 0001h: 1 Block 0002h: 2 Blocks FFFFh: 65535 Blocks</p>

18.6.5 MMCSDB12_ARGUMENT1_LO Register (Offset = 8h) [reset = 0h]

MMCSDB12_ARGUMENT1_LO is shown in [Figure 18-185](#) and described in [Table 18-477](#).

Return to [Summary Table](#).

This register contains Lower bits of SD Command Argument.

Table 18-476. MMCSDB12_ARGUMENT1_LO Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0008h
MMCSDB2_CTL_CFG	04F9 8008h

Figure 18-185. MMCSDB12_ARGUMENT1_LO Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ARG1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-477. MMCSDB12_ARGUMENT1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_ARG1	R/W	0h	Command Argument 1 Low The SD Command Argument is specified as bit 23-8 of Command-Format.

18.6.6 MMCSD12_ARGUMENT1_HI Register (Offset = Ah) [reset = 0h]

MMCSD12_ARGUMENT1_HI is shown in [Figure 18-186](#) and described in [Table 18-479](#).

Return to [Summary Table](#).

This register contains higher bits of SD Command Argument.

Table 18-478. MMCSD12_ARGUMENT1_HI Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 000Ah
MMCSD2_CTL_CFG	04F9 800Ah

Figure 18-186. MMCSD12_ARGUMENT1_HI Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ARG1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-479. MMCSD12_ARGUMENT1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_ARG1	R/W	0h	Command Argument 1 High The SD Command Argument is specified as bit 39-24 of Command-Format.

18.6.7 MMCS12_TRANSFER_MODE Register (Offset = Ch) [reset = 0h]

MMCS12_TRANSFER_MODE is shown in [Figure 18-187](#) and described in [Table 18-481](#).

Return to [Summary Table](#).

Table 18-480. MMCS12_TRANSFER_MODE Instances

Instance	Physical Address
MMCS1_CTL_CFG	04FB 000Ch
MMCS2_CTL_CFG	04F9 800Ch

Figure 18-187. MMCS12_TRANSFER_MODE Register

15	14	13	12	11	10	9	8
RESERVED							RESP_INTR_DIS
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESP_ERR_CHK_ENA	RESP_TYPE	MULTI_BLK_SEL	DATA_XFER_DIR	AUTO_CMD_ENA		BLK_CNT_ENA	DMA_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-481. MMCS12_TRANSFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0h	Reserved
8	RESP_INTR_DIS	R/W	0h	<p>Response Interrupt Disable</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked. If Host Driver checks response error, sets this bit to 0h and waits Command Complete Interrupt (MMCS12_NORMAL_INTR_STS[0] CMD_COMPLETE) and then checks the Response register (MMCS12_RESPONSE_0 to MMCS12_RESPONSE_7).</p> <p>If Host Controller checks response error, sets this bit to 1h and sets the MMCS12_TRANSFER_MODE[7] RESP_ERR_CHK_ENA bit to 1h. Command Complete Interrupt (MMCS12_NORMAL_INTR_STS[0] CMD_COMPLETE) is disabled by this bit regardless of Command Complete Signal Enable (MMCS12_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE).</p> <p>0h: Response Interrupt is enabled</p> <p>1h: Response Interrupt is disabled</p>

Table 18-481. MMCSD12_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESP_ERR_CHK_ENA	R/W	0h	<p>Response Error Check Enable</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.</p> <p>If Host Driver checks response error, this bit is set to 0h and the MMCSD12_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 0h. If Host Controller checks response error, sets this bit to 1h and sets the Response Interrupt Disable bit to 1h (MMCSD12_TRANSFER_MODE[8] RESP_INTR_DIS = 1h). The MMCSD12_TRANSFER_MODE[6] RESP_TYPE bit selects either R1 or R5 response type. If an error is detected, Response Error Interrupt is generated in the MMCSD12_ERROR_INTR_STS register.</p> <p>0h: Response Error Check is disabled 1h: Response Error Check is enabled</p>
6	RESP_TYPE	R/W	0h	<p>Response Type R1/R5</p> <p>When response error check is enabled (MMCSD12_TRANSFER_MODE[7] RESP_ERR_CHK_ENA = 1h), this bit selects either R1 or R5 response types. Two types of response checks are supported: R1 for memory and R5 for SDIO. Error Statuses Checked in R1:</p> <p>Bit31 OUT_OF_RANGE Bit30 ADDRESS_ERROR Bit29 BLOCK_LEN_ERROR Bit26 WP_VIOLATION Bit25 CARD_IS_LOCKED Bit23 COM_CRC_ERROR Bit21 CARD_ECC_FAILED Bit20 CC_ERROR Bit19 ERROR</p> <p>Response Flags Checked in R5:</p> <p>Bit07 COM_CRC_ERROR Bit03 ERROR Bit01 FUNCTION_NUMBER Bit00 OUT_OF_RANGE</p> <p>0h: R1 (Memory) 1h: R5 (SDIO)</p>
5	MULTI_BLK_SEL	R/W	0h	<p>Multi/Single Block Select</p> <p>This bit enables multiple block data transfers.</p> <p>0h: Single Block 1h: Multiple Block</p>
4	DATA_XFER_DIR	R/W	0h	<p>Data Transfer Direction Select</p> <p>This bit defines the direction of data transfers.</p> <p>0h: Write (Host to Card) 1h: Read (Card to Host)</p>

Table 18-481. MMCSDB12_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	AUTO_CMD_ENA	R/W	0h	<p>Auto CMD Enable</p> <p>This field determines use of auto command functions. There are three methods to stop Multiple-block read and write operation by CMD23 or CMD12. In the other operations (for example single read/write operation), this field is set to 0h.</p> <p>(1) Auto CMD12 Enable:</p> <p>Multiple-block read and write commands for memory require CMD12 to stop the operation. When this field is set to 1h, the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the MMCSDB12_AUTOCMD_ERR_STS register. The Host Driver shall not set this bit if the command does not require CMD12. When MMCSDB12_HOST_CONTROL2[12] HOST_VER40_ENA = 0h, CMD12 is issued when 16-bit Block Count is expired. When MMCSDB12_HOST_CONTROL2[12] HOST_VER40_ENA = 1h, CMD12 is issued when 16-bit Block Count or 32-bit Block Count is expired.</p> <p>(2) Auto CMD23 Enable:</p> <p>When this bit field is set to 2h, the Host Controller issues a CMD23 automatically before issuing a command specified in the MMCSDB12_COMMAND register. The Host Controller Version 3.00 and later shall support this function.</p> <p>The following conditions are required to use the Auto CMD23: Auto CMD23 Supported (Host Controller Version is 3.00 or later). A memory card that supports CMD23 (SCR[33] = 1h). If DMA is used, it shall be ADMA.</p> <p>Only when CMD18 or CMD25 is issued. Auto CMD23 can be used with or without ADMA. By writing the MMCSDB12_COMMAND register, the Host Controller issues a CMD23 first and then issues a command specified by the MMCSDB12_COMMAND[13:8] CMD_INDEX bit field. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the MMCSDB12_AUTOCMD_ERR_STS register.</p> <p>32-bit block count value for CMD23 is set to 32-bit Block Count (MMCSDB12_SDMA_SYS_ADDR_LO/MMCSDB12_SDMA_SYS_ADDR_HI) register.</p> <p>(3) Auto CMD Auto Select (Version 4.10):</p> <p>As CMD23 is optional for SD memory card except UHS 104 card, if card supports CMD23, Auto CMD 23 should be used instead of Auto CMD12. Host Controller Version 4.10 defines this "Auto CMD Auto Select" mode. Selection of Auto CMD depends on setting of the MMCSDB12_HOST_CONTROL2[11] CMD23_ENA bit which indicates whether card supports CMD23. If MMCSDB12_HOST_CONTROL2[11] CMD23_ENA = 1h, Auto CMD23 is used and if MMCSDB12_HOST_CONTROL2[11] CMD23_ENA = 0h, Auto CMD12 is used. In case of Version 4.10 or later, use of Auto CMD Auto Select is recommended rather than use of Auto CMD12 Enable or Auto CMD23 Enable.</p> <p>0h: Auto Command Disabled 1h: Auto CMD12 Enable 2h: Auto CMD23 Enable 3h: Reserved</p>

Table 18-481. MMCSD12_TRANSFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BLK_CNT_ENA	R/W	0h	Block Count Enable This bit is used to enable the MMCSD12_BLOCK_COUNT register, which is only relevant for multiple block transfers. When this bit is 0h, the MMCSD12_BLOCK_COUNT register is disabled, which is useful in executing an infinite transfer. 0h: Disable 1h: Enable
0	DMA_ENA	R/W	0h	DMA Enable DMA can be enabled only if the MMCSD12_CAPABILITIES[22] SDMA_SUPPORT bit is set. If this bit is set to 1h, a DMA operation shall begin when the HD writes to the upper byte of the MMCSD12_COMMAND register. 0h: Disable 1h: Enable

This register is used to control the operations of data transfers.

This register is used to control the operation of data transfers. The Host Driver shall set this register before issuing a command which transfers data (Refer to MMCSD12_COMMAND[5] DATA_PRESENT bit), or before issuing a Resume command. The Host Driver shall save the value of this register when the data transfer is suspended (as a result of a Suspend command) and restore it before issuing a Resume command. To prevent data loss, the Host Controller shall implement write protection for this register during data transactions. Writes to this register shall be ignored when the MMCSD12_PRESENTSTATE[1] INHIBIT_DAT bit is 1h.

Table 18-482 shows the determination of transfer type.

Table 18-482. Determination of Transfer Type

Multi/Single Block Select	Block Count Enable	Block Count	Function
0	Don't Care	Don't Care	Single Transfer
1	0	Don't Care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

18.6.8 MMCSDB12_COMMAND Register (Offset = Eh) [reset = 0h]

MMCSDB12_COMMAND is shown in [Figure 18-188](#) and described in [Table 18-484](#).

Return to [Summary Table](#).

This register is used to program the Command for host controller.

Table 18-483. MMCSDB12_COMMAND Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 000Eh
MMCSDB2_CTL_CFG	04F9 800Eh

Figure 18-188. MMCSDB12_COMMAND Register

15	14	13	12	11	10	9	8
RESERVED		CMD_INDEX					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
CMD_TYPE		DATA_PRESENT	CMD_INDEX_CHK_ENA	CMD_CRC_CHK_ENA	SUB_CMD	RESP_TYPE_SEL	
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-484. MMCSDB12_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	CMD_INDEX	R/W	0h	Command Index This bit shall be set to the command number (CMD0-63, ACMD0-63).

Table 18-484. MMCSD12_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	CMD_TYPE	R/W	0h	<p>Command Type</p> <p>There are three types of special commands. Suspend, Resume and Abort. These bits shall be set to 0h for all other commands.</p> <p>Suspend Command:</p> <p>If the Suspend command succeeds, the HC shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The HC shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the HC shall maintain its current state. and the HD shall restart the transfer by setting the MMCSD12_BLOCK_GAP_CONTROL[1] CONTINUE bit.</p> <p>Resume Command:</p> <p>The HD re-starts the data transfer by restoring the registers in the range of 04FB 0000h - 04FB 000Dh (04F9 8000h - 04F9 800Dh). The HC shall check for busy before starting write transfers.</p> <p>Abort Command:</p> <p>If this command is set when executing a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a write transfer, the HC shall stop driving the DAT line. After issuing the Abort command, the HD should issue a software reset.</p> <p>0h: Normal 1h: Suspend 2h: Resume 3h: Abort</p>
5	DATA_PRESENT	R/W	0h	<p>Data Present Select</p> <p>This bit is set to 1h to indicate that data is present and shall be transferred using the DAT line. If is set to 0h for the following:</p> <ol style="list-style-type: none"> 1. Commands using only CMD line (for example CMD52). 2. Commands with no data transferbut using busy signal on DAT[0]line (R1b or R5b for example CMD38). 3. Resume Command. <p>0h: No Data Present 1h: Data Present</p>
4	CMD_INDEX_CHK_ENA	R/W	0h	<p>Command Index Check Enable</p> <p>If this bit is set to 1h, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0h, the Index field is not checked.</p> <p>0h: Disable 1h: Enable</p>
3	CMD_CRC_CHK_ENA	R/W	0h	<p>Command CRC Check Enable</p> <p>If this bit is set to 1h, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0h, the CRC field is not checked.</p> <p>0h: Disable 1h: Enable</p>

Table 18-484. MMCSDB12_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SUB_CMD	R/W	0h	<p>Sub Command Flag</p> <p>This bit is added from Version 4.10 to distinguish a main command or sub command. When issuing a main command, this bit is set to 0h and when issuing a sub command, this bit is set to 1h. Setting of this bit is checked by the MMCSDB12_PRESENTSTATE[28] SUB_COMMAND_STS bit.</p> <p>Host Driver manages whether main or sub command. Host Controller does not refer to this bit to issue a command.</p> <p>0h: Sub Command 1h: Main Command</p>
1-0	RESP_TYPE_SEL	R/W	0h	<p>Response Type Select</p> <p>0h: No Response 1h: Response length 136 2h: Response length 48 3h: Response length 48 check Busy after response</p>

18.6.9 MMCSD12_RESPONSE_0 to MMCSD12_RESPONSE_7 Register (Offset = 10h to 1Eh) [reset = 0h]

MMCSD12_RESPONSE_0 to MMCSD12_RESPONSE_7 is shown in [Figure 18-189](#) and described in [Table 18-486](#).

Return to [Summary Table](#).

This registers is used to store responses from SD Cards.

Table 18-485. MMCSD12_RESPONSE_0 to MMCSD12_RESPONSE_7 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0010h to 04FB 001Eh
MMCSD2_CTL_CFG	04F9 8010h to 04F9 801Eh

Figure 18-189. MMCSD12_RESPONSE_0 to MMCSD12_RESPONSE_7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_RESP															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 18-486. Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CMD_RESP	R	0h	Command Response R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.

[Table 18-487](#) defines the relation between the parameter and name of response type.

Table 18-487. Relation between Parameters and the Name of Response Type

Response Type	Index Check Enable	CRC Check Enable	Name of Response Type
00	0	0	No Response
01	0	1	R2
10	0	0	R3, R4
10	1	1	R1, R6, R5, R7
11	1	1	R1b, R5b

The following table describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.

[Table 18-488](#) shows response bit definition for each response type.

Table 18-488. Response Bit Definition for each Response Type

Kind of Response	Meaning of Response	Response Field	Response Register
R1, R1b (normal response)	Card Status	R[39:8]	REP[31:0]
R1b (Auto CMD12 response)	Card Status for Auto CMD12	R[39:8]	REP[127:96]
R1 (Auto CMD23 response)	Card Status for Auto CMD23	R[39:8]	REP [127:96]
R2 (CID, CSD Register)	CID or CSD register include	R[127:8]	REP[119:0]
R3 (OCR Register)	OCR Register for memory	R[39:8]	REP[31:0]
R4 (OCR Register)	OCR Register for I/O etc.	R[39:8]	REP[31:0]
R5, R5b	SDIO Response	R[39:8]	REP[31:0]
R6 (Published RCA response)	New published RCA[31:16] etc.	R[39:8]	REP[31:0]

The Response Field indicates bit positions of "Responses" defined in the Physical Layer Specification. The table shows most responses with a length of 48 (R[47:0]) have 32 bits of the response data (R[39:8]) stored in the Response register at REP[31:0]. Responses of type R1b (Auto CMD12 responses) and R1 (Auto CMD23 response) have response data bits R[39:8] stored in the Response register at REP[127:96]. Responses with length 136 (R[135:0]) have 120 bits of the response data (R[127:8]) stored in the Response register at REP[119:0].

To read the response status efficiently, the Host Controller only stores part of the response data in the Response register. This enables the Host Driver to read 32 bits of response data efficiently in one read cycle on a 32-bit bus system. Parts of the response, the Index field and the CRC, are checked by the Host Controller (as specified by the MMCSD12_COMMAND[4] CMD_INDEX_CHK_ENA and MMCSD12_COMMAND[3] CMD_CRC_CHK_ENA bits) and generate an error interrupt if an error is detected. The bit range for the CRC check depends on the response length. If the response length is 48, the Host Controller shall check R[47:1], and if the response length is 136 the Host Controller shall check R[119:1].

Since the Host Controller may have a multiple block data DAT line transfer executing concurrently with a CMD_wo_DAT command, the Host Controller stores the Auto CMD12 response in the upper bits (REP[127:96]) of the Response register. The CMD_wo_DAT response is stored in REP[31:0]. This allows the Host Controller to avoid overwriting the Auto CMD12 response with the CMD_wo_DAT and vice versa.

While executing Auto CMD23, the response of CMD23 is saved to REP [127:96] and the response of multiple-block read and write command is save to REP [31:0]. The response error of CMD23 is indicated in the MMCSD12_AUTOCMD_ERR_STS register. When the Host Controller modifies part of the Response register, as shown in the table, it shall preserve the unmodified bits.

18.6.10 MMCSD12_DATA_PORT Register (Offset = 20h) [reset = 0h]

MMCSD12_DATA_PORT is shown in [Figure 18-190](#) and described in [Table 18-490](#).

Return to [Summary Table](#).

This register is used to access internal buffer.

Table 18-489. MMCSD12_DATA_PORT Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0020h
MMCSD2_CTL_CFG	04F9 8020h

Figure 18-190. MMCSD12_DATA_PORT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUF_RD_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-490. MMCSD12_DATA_PORT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUF_RD_DATA	R/W	0h	Buffer Data The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

18.6.11 MMCSDB12_PRESENTSTATE Register (Offset = 24h) [reset = 1F00000h]

MMCSDB12_PRESENTSTATE is shown in [Figure 18-191](#) and described in [Table 18-492](#).

Return to [Summary Table](#).

The Host Driver can get status of the Host Controller from this 32-bit read-only register.

Table 18-491. MMCSDB12_PRESENTSTATE Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0024h
MMCSDB2_CTL_CFG	04F9 8024h

Figure 18-191. MMCSDB12_PRESENTSTATE Register

31	30	29	28	27	26	25	24
UHS2_IF_DETECTION	UHS2_IF_LANE_SYNC	UHS2_DORMANT	SUB_COMMAND_STS	CMD_NOT_ISSUED_BY_ERR	RESERVED		SDIF_CMDIN
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		R-1h
23	22	21	20	19	18	17	16
SDIF_DAT3IN	SDIF_DAT2IN	SDIF_DAT1IN	SDIF_DAT0IN	WRITE_PROTECT	CARD_DETECTED	CARD_STATE_STABLE	CARD_INSERTED
R-1h	R-1h	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED				BUF_RD_ENA	BUF_WR_ENA	RD_XFER_ACTIVE	WR_XFER_ACTIVE
R-0h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
SDIF_DAT7IN	SDIF_DAT6IN	SDIF_DAT5IN	SDIF_DAT4IN	RETUNING_REQ	DATA_LINE_ACTIVE	INHIBIT_DAT	INHIBIT_CMD
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 18-492. MMCSDB12_PRESENTSTATE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UHS2_IF_DETECTION	R	0h	<p>UHS-II IF Detection (UHS-II Only)</p> <p>This status indicates whether a card supports UHS-II IF. This status is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSDB12_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). UHS-II interface initialization is activated by setting the MMCSDB12_CLOCK_CONTROL[2] SD_CLK_ENA bit. Host Controller drives STB.L on D0 lane from EIDL state and waits for receiving STB.L on D1 lane. This bit is set to 1h if STB.L is detected on D1 lane. Host Controller shall compensate latency from setting SD Clock Enable to output STB.L on D0 lane when reading this status. This bit may be read any time after setting SD Clock Enable for faster UHS-II IF detection but Host Driver shall check this status at least 200µs period from setting SD Clock Enable (MMCSDB12_CLOCK_CONTROL[2] SD_CLK_ENA) until detecting UHS-II IF.</p> <p>After UHS-II IF is detected, this bit is cleared by when EIDL is detected on D0 lane, UHS-II Interface Enable is set to 0h (MMCSDB12_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or Host full reset is executed.</p> <p>1h: UHS-II IF is detected 0h: UHS-II IF is not detected</p>

Table 18-492. MMCSD12_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	UHS2_IF_LANE_SYNC	R	0h	<p>Lane Synchronization (UHS-II Only)</p> <p>This status indicates whether lane is synchronized in UHS-II mode. This status is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD12_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). On detecting UHS-II Interface (D31 = 1h), Host Controller provides SYN LSS on D0 lane and waits for receiving SYN LSS on D1 lane. If SYN LSS is detected on D1 lane, Host Controller provides LIDL LSS on D0 lane and waits for receiving LIDL LSS on D1 lane.</p> <p>In case of Version 4.00, this bit indicates completion of Device PHY Initialization by detecting LIDL LSS on D1 lane.</p> <p>From Version 4.10, Host Controller may implement a specific PHY verification method and PHY Initialization Failure can be indicated by keeping this bit to 0h even LIDL LSS is detected on D1 lane. Host Driver detects PHY Initialization Failure by timeout.</p> <p>This bit is cleared by when D0 lane is set to EIDL, UHS-II Interface Enable is set to 0h (MMCSD12_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or executes Host full reset.</p> <p>1h: UHS-II PHY is initialized 0h: UHS-II PHY is not initialized</p>
29	UHS2_DORMANT	R	0h	<p>In Dormant State (UHS-II Only)</p> <p>This status indicates whether UHS-II lanes enter Dormant state. This function is enabled by setting UHS-II Interface Enable to 1h in the Host Control 2 register (MMCSD12_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 1h). On issuing GO_DORMANT_STATE command, "Go Dormant Command (7h)" is set to Command type in the UHS-II Command register (MMCSD12_UHS2_COMMAND[7:6] CMD_TYPE). This command type acts as a trigger to enter lanes into dormant state. Host Controller provides STB.H and EIDL on D0 lane and waits for receiving STB.H and EIDL on D1 lane. This bit is set to 1h after the time of T_DMT_ENTRY (750 RCLK cycle) or more from detecting EIDL on D1 lane.</p> <p>RCLK may be stopped in dormant state, by setting SD Clock Enable to 0h in the Clock Control register (MMCSD12_CLOCK_CONTROL[2] SD_CLK_ENA = 0h) while In Dormant State bit is set to 1h. On writing Clock Control register with setting SD Clock Enable to 1h (MMCSD12_CLOCK_CONTROL[2] SD_CLK_ENA = 1h), Host Controller wakes lanes to exit Dormant State and In Dormant State is set to 0h.</p> <p>In case of the card enters Hibernate Mode (RCLK is stopped), Host Driver may turn off VDD1 by clearing SD Bus Power for VDD1 bit in the MMCSD12_POWER_CONTROL register. Host Controller shall turn off VDD1 after stopping RCLK. This bit is cleared by when Host Controller drives STB.L on D0 lane, UHS-II Interface Enable is set to 0h (MMCSD12_HOST_CONTROL2[8] UHS2_INTF_ENABLE = 0h) or executes Host full reset.</p> <p>1h: In DORMANT state 0h: Not in DORMANT state</p>

Table 18-492. MMCSDB12_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	SUB_COMMAND_STS	R	0h	<p>Sub Command Status</p> <p>The MMCSDB12_COMMAND register and Response register (MMCSDB12_RESPONSE_0 to MMCSDB12_RESPONSE_7) are commonly used for main command and sub command. This status is used to distinguish which response error statuses, main command or sub command, indicated in the MMCSDB12_ERROR_INTR_STS register or in the MMCSDB12_UHS2_ERR_INTR_STS register. Just before reading of this register, the MMCSDB12_COMMAND[2] SUB_CMD bit or the MMCSDB12_UHS2_COMMAND register is copied to this status. This status is effective not only when Response Error interrupt is generated but also when data error interrupt is generated with Command Not Issued by Error (D27 of this register) or Auto CMD Error interrupt is generated with Command Not Issued by Error by Auto CMD12 in the MMCSDB12_AUTOCMD_ERR_STS register.</p> <p>1h: Sub Command Status 0h: Main Command Status</p>
27	CMD_NOT_ISS_BY_ERR	R	0h	<p>Command Not Issued by Error</p> <p>Setting of this status indicates that a command cannot be issued due to an error except Auto CMD12 error (equivalent error status by Auto CMD12 error is defined as Command Not Issued By Auto CMD12 Error in the MMCSDB12_AUTOCMD_ERR_STS register). This status is set to 1h when Host Controller cannot issue a command after setting MMCSDB12_COMMAND register or MMCSDB12_UHS2_COMMAND register. Sub Command Status (D28) indicates which command is not issued (main or sub).</p> <p>1h: Command cannot be issued 0h: No error for issuing a command</p>
26-25	RESERVED	R	0h	Reserved
24	SDIF_CMDIN	R	1h	<p>CMD Line Signal Level (SD Mode Only)</p> <p>This status is used to check CMD line level to recover from errors, and for debugging.</p>
23	SDIF_DAT3IN	R	1h	<p>DAT[3] Line Signal Level (SD Mode Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[3].</p> <p>D23 - DAT[3]</p>
22	SDIF_DAT2IN	R	1h	<p>DAT[2] Line Signal Level (SD Mode Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[2].</p> <p>D22 - DAT[2]</p>
21	SDIF_DAT1IN	R	1h	<p>DAT[1] Line Signal Level (SD Mode Only)</p> <p>This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[1].</p> <p>D21 - DAT[1]</p>

Table 18-492. MMCSD12_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	SDIF_DAT0IN	R	1h	DAT[0] Line Signal Level (SD Mode Only) This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0]. D20 - DAT[0]
19	WRITE_PROTECT	R	0h	Write Protect Switch Pin Level The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP pin. 0h: Write protected (SDWP = 1) 1h: Write enabled (SDWP = 0)
18	CARD_DETECT	R	0h	Card Detect Pin Level This bit reflects the inverse value of the SDCD# pin. 0h: No Card present (SDCD# = 1) 1h: Card present (SDCD# = 0)
17	CARD_STATE_STABLE	R	0h	Card State Stable This bit is used for testing. If it is 0h, the Card Detect Pin Level is not stable. If this bit is set to 1h, it means the Card Detect Pin Level is stable. The MMCSD12_SOFTWARE_RESET[0] SWRST_FOR_ALL bit shall not affect this bit. 0h: Reset of Debouncing 1h: No Card or Inserted
16	CARD_INSERTED	R	0h	Card Inserted This bit indicates whether a card has been inserted. Changing from 0h to 1h generates a Card Insertion interrupt in the MMCSD12_NORMAL_INTR_STS register and changing from 1h to 0h generates a Card Removal Interrupt in the MMCSD12_NORMAL_INTR_STS register. The MMCSD12_SOFTWARE_RESET[0] SWRST_FOR_ALL bit shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear the MMCSD12_POWER_CONTROL[0] SD_BUS_POWER bit and the MMCSD12_CLOCK_CONTROL[2] SD_CLK_ENA bit. In addition the HD should clear the HC by the MMCSD12_SOFTWARE_RESET[0] SWRST_FOR_ALL bit. The card detect is active regardless of the SD Bus Power. 0h: Reset or Debouncing or No Card 1h: Card Inserted
15-12	RESERVED	R	0h	Reserved
11	BUF_RD_ENA	R	0h	Buffer Read Enable This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1h, readable data exists in the buffer. A change of this bit from 1h to 0h occurs when all the block data is read from the buffer. A change of this bit from 0h to 1h occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0h: Read Disable 1h: Read Enable

Table 18-492. MMCSDB12_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	BUF_WR_ENA	R	0h	<p>Buffer Write Enable</p> <p>This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1h, data can be written to the buffer. A change of this bit from 1h to 0h occurs when all the block data is written to the buffer. A change of this bit from 0h to 1h occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt.</p> <p>0h: Write Disable 1h: Write Enable</p>
9	RD_XFER_ACTIVE	R	0h	<p>Read Transfer Active (SD Mode Only)</p> <p>This status is used for detecting completion of a read transfer. This bit is set to 1h for either of the following conditions:</p> <p>After the end bit of the read command.</p> <p>When writing a 1h to continue Request in the MMCSDB12_BLOCK_GAP_CONTROL register to restart a read transfer.</p> <p>This bit is cleared to 0h for either of the following conditions:</p> <p>When the last data block as specified by block length is transferred to the system.</p> <p>When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1h (MMCSDB12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h). A transfer complete interrupt is generated when this bit changes to 0h.</p> <p>1h: Transferring data 0h: No valid data</p>
8	WR_XFER_ACTIVE	R	0h	<p>Write Transfer Active (SD Mode Only)</p> <p>This status indicates a write transfer is active. If this bit is 0h, it means no valid write data exists in the HC. This bit is set in either of the following cases:</p> <p>After the end bit of the write command.</p> <p>When writing a 1h to the MMCSDB12_BLOCK_GAP_CONTROL[1] CONTINUE bit to restart a write transfer.</p> <p>This bit is cleared in either of the following cases:</p> <p>After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple).</p> <p>After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0h, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy.</p> <p>1h: Transferring data 0h: No valid data</p>

Table 18-492. MMCSD12_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SDIF_DAT7IN	R	0h	DAT[7] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D07 - DAT[7]
6	SDIF_DAT6IN	R	0h	DAT[6] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D06 - DAT[6]
5	SDIF_DAT5IN	R	0h	DAT[5] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D05 - DAT[5]
4	SDIF_DAT4IN	R	0h	DAT[4] Line Signal Level (Embedded Only) This status is used to check DAT line level to recover from errors, and for debugging. D04 - DAT[4]
3	RETUNING_REQ	R	0h	Re-Tuning Request (UHS-I Only) Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting the MMCSD12_HOST_CONTROL2[6] EXECUTE_TUNING bit. Changing of this bit from 0h to 1h generates Re-Tuning Event. This bit isn't set to 1h if the MMCSD12_HOST_CONTROL2[7] SAMPLING_CLK_SELECT bit is set to 0h (using fixed sampling clock). 1h: Sampling clock needs re-tuning 0h: Fixed or well tuned sampling clock
2	DATA_LINE_ACTIVE	R	0h	DAT Line Active (SD Mode Only) This bit indicates whether one of the DAT line on SD bus is in use. 1h: DAT line active 0h: DAT line inactive
1	INHIBIT_DAT	R	0h	Command Inhibit (DAT) (SD Mode Only) This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1h. If this bit is 0h, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (for example R1b, R5b type). Changing from 1h to 0h generates a Transfer Complete interrupt in the MMCSD12_NORMAL_INTR_STS register. Note: The SD Host Driver can save registers in the range of 04FB 0000h - 04FB 000Dh (04F9 8000h - 04F9 800Dh) for a suspend transaction after this bit has changed from 1h to 0h. 1h: Cannot issue command which uses the DAT line 0h: Can issue command which uses the DAT line

Table 18-492. MMCSDB12_PRESENTSTATE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INHIBIT_CMD	R	0h	<p>Command Inhibit (CMD)</p> <p>SD Mode:</p> <p>If this bit is 0h, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the MMCSDB12_COMMAND register is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1h.</p> <p>Commands using only the CMD line can be issued if this bit is 0h. Changing from 1h to 0h generates a Command complete interrupt in the MMCSDB12_NORMAL_INTR_STS register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1h and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by the MMCSDB12_COMMAND register.</p> <p>UHS-II Mode:</p> <p>This bit is 0h means that a command packet can be issued by the Host Controller. While this bit is set to 1h, which means the Host Controller is not ready to issue a next command, Host Driver shall not write the registers from the MMCSDB12_UHS2_BLOCK_SIZE to the MMCSDB12_UHS2_COMMAND. Changing from 1h to 0h generates a Command Complete Interrupt in the MMCSDB12_NORMAL_INTR_STS register.</p> <p>1h: Host Controller is not ready to issue a command 0h: Host Controller is ready to issue a command</p> <p>Version 4.10 adds a new control to prevent error statuses from overwriting by receipt of a next command. This status keeps indicating 1h while any of response error statuses is set to 1h, Command Not Issued by Error in this register is set to 1h or the MMCSDB12_AUTOCMD_ERR_STS[7] CMD_NOT_ISSUED bit is set to 1h. Software Reset For CMD Line is used to clear the error statuses above and this status (MMCSDB12_SOFTWARE_RESET[1] SWRST_FOR_CMD).</p>

Note: DAT line active indicates whether one of the DAT line is on SD bus is in use.

(a) In the case of read transactions

This status indicates whether a read transfer is executing on the SD Bus. Changing this value from 1h to 0h generates a Block Gap Event interrupt in the MMCSDB12_NORMAL_INTR_STS register, as the result of the Stop At Block Gap Request being set.

This bit shall be set in either of the following cases:

- (1) After the end bit of the read command.
- (2) When writing a 1h to the MMCSDB12_BLOCK_GAP_CONTROL[1] CONTINUE bit to restart a read transfer.

This bit shall be cleared in either of the following cases:

(1) When the end bit of the last data block is sent from the SD Bus to the Host Controller. In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.

(2) When a read transfer is stopped at the block gap initiated by a Stop At Block Gap Request (MMCSD12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP).

The Host Controller shall stop read operation at the start of the interrupt cycle of the next block gap by driving Read Wait or stopping SD clock. If the Read Wait signal is already driven (due to data buffer cannot receive data), the Host Controller can continue to stop read operation by driving the Read Wait signal. It is necessary to support Read Wait in order to use suspend/resume function.

(b) In the case of write transactions

This status indicates that a write transfer is executing on the SD Bus. Changing this value from 1h to 0h generate a Transfer Complete interrupt in the MMCSD12_NORMAL_INTR_STS register.

This bit shall be set in either of the following cases:

(1) After the end bit of the write command.

(2) When writing to 1h to the MMCSD12_BLOCK_GAP_CONTROL[1] CONTINUE bit to continue a write transfer.

This bit shall be cleared in either of the following cases:

(1) When the SD card releases write busy of the last data block. If SD card does not drive busy signal for 8 SD Clocks, the Host Controller shall consider the card drive "Not Busy". In case of ADMA2, the last block is designated by the last transfer of Descriptor Table.

(2) When the SD card releases write busy prior to waiting for write transfer as a result of a Stop At Block Gap Request (MMCSD12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP).

(c) Command with busy

This status indicates whether a command indicates busy (for example erase command for memory) is executing on the SD Bus. This bit is set after the end bit of the command with busy and cleared when busy is de-asserted. Changing this bit from 1h to 0h generate a Transfer Complete interrupt in the MMCSD12_NORMAL_INTR_STS register.

Note

The HD can issue cmd0, cmd12, cmd13 (for memory) and cmd52 (for SDIO) when the DAT lines are busy during data transfer. These commands can be issued when Command Inhibit (CMD) is set to zero (MMCSD12_PRESENTSTATE[0] INHIBIT_CMD = 0h). Other commands shall be issued when Command Inhibit (DAT) is set to zero (MMCSD12_PRESENTSTATE[1] INHIBIT_DAT = 0h).

18.6.12 MMCSDB12_HOST_CONTROL1 Register (Offset = 28h) [reset = 0h]

MMCSDB12_HOST_CONTROL1 is shown in [Figure 18-192](#) and described in [Table 18-494](#).

Return to [Summary Table](#).

This register is used to program DMA modes, LED control, data transfer width, High Speed enable, card detect test level and signal selection.

Table 18-493. MMCSDB12_HOST_CONTROL1 Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0028h
MMCSDB2_CTL_CFG	04F9 8028h

Figure 18-192. MMCSDB12_HOST_CONTROL1 Register

7	6	5	4	3	2	1	0
CD_SIG_SEL	CD_TEST_LEVEL	EXT_DATA_WIDTH	DMA_SELECT	HIGH_SPEED_ENA	DATA_WIDTH	LED_CONTROL	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-494. MMCSDB12_HOST_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CD_SIG_SEL	R/W	0h	Card Detect Signal Detection This bit selects source for card detection. 1h: The card detect test level is selected 0h: SDCD# is selected (for normal use)
6	CD_TEST_LEVEL	R/W	0h	Card Detect Test Level This bit is enabled while the Card Detect Signal Selection is set to 1h and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal interrupt status enable bit is set. 1h: Card Inserted 0h: No Card
5	EXT_DATA_WIDTH	R/W	0h	Extended Data Transfer Width (Embedded and SD Mode Only) This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the MMCSDB12_CAPABILITIES register. If a device supports 8-bit bus mode, this bit may be set to 1h. If this bit is 0h, bus width is controlled by the MMCSDB12_HOST_CONTROL1[1] DATA_WIDTH bit. This bit is not effective when multiple devices are installed on a bus slot (Slot Type is set to 2h in the MMCSDB12_CAPABILITIES register). In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register (MMCSDB12_SHARED_BUS_CTRL_PTR). 1h: 8-bit Bus Width 0h: Bus Width is Selected by Data Transfer Width

Table 18-494. MMCSD12_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	DMA_SELECT	R/W	0h	<p>DMA Select</p> <p>This field is used to select DMA type. The Host Driver shall check support of DMA modes by referring the MMCSD12_CAPABILITIES register. Selected DMA is enabled by the MMCSD12_TRANSFER_MODE[0] DMA_ENA bit in SD mode and the MMCSD12_UHS2_XFER_MODE[0] DMA_ENA bit in UHS-II mode.</p> <p>(1) Up to Version 3.00:</p> <p>When MMCSD12_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 0h, setting of this field is compatible to Host Controller Version 3.00.</p> <p>SDMA is initiated by writing to the MMCSD12_COMMAND register when this field is set to 0h and the SDMA System Address register (32-bit) is used (MMCSD12_SDMA_SYS_ADDR_LO/ MMCSD12_SDMA_SYS_ADDR_HI). SDMA does not support 64-bit addressing.</p> <p>ADMA2 is initiated by writing to the MMCSD12_COMMAND register when this field is set to 2h or 3h. Lower 32-bit of the ADMA System Address register (MMCSD12_SDMA_SYS_ADDR_LO/ MMCSD12_SDMA_SYS_ADDR_HI) is used when this field is set to 2h and 64-bit of the ADMA System Address register is used when this field is set to 3h. Support of 64-bit System Addressing is indicated by the MMCSD12_CAPABILITIES[28] ADDR_64BIT_SUPPORT_V3 bit. 64-bit ADMA2 uses 96-bit Descriptor.</p> <p>0h: SDMA is selected</p> <p>1h: 32-bit Address ADMA1 is selected</p> <p>2h: 32-bit Address ADMA2 is selected</p> <p>3h: 64-bit Address ADMA2 is selected (Optional)</p> <p>(2) Version 4.00 or later:</p> <p>When the MMCSD12_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, setting of this field is changed as follows.</p> <p>SDMA is initiated by Host Driver writes to the MMCSD12_COMMAND register when this field is set to 0h.</p> <p>ADMA2 is initiated by Host Driver writes to the MMCSD12_COMMAND register when this field is set to 2h or 3h and by ADMA3 sets to the ADMA System Address register (MMCSD12_SDMA_SYS_ADDR_LO/ MMCSD12_SDMA_SYS_ADDR_HI) when this field is set to 3h.</p> <p>ADMA3 is initiated by Host Driver writes to the MMCSD12_ADMA3_DESC_ADDRESS register when this field is set to 3h.</p> <p>0h: SDMA is selected</p> <p>1h: Not Used (New assignment is not allowed)</p> <p>2h: ADMA2 is selected (ADMA3 is not supported or disabled)</p> <p>3h: ADMA2 or ADMA3 is selected</p>

Table 18-494. MMCSDB12_HOST_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				Support of 64-bit DMA and 128-bit Descriptor is indicated by the MMCSDB12_CAPABILITIES[27] ADDR_64BIT_SUPPORT_V4 bit. If the support bit is set to 1h, all supported DMAs (depends on Support, ADMA2 Support and ADMA3 Support) shall support 64-bit addressing. The MMCSDB12_HOST_CONTROL2[13] BIT64_ADDRESSING bit selects either 32-bit or 64-bit system addressing of DMAs.
2	HIGH_SPEED_ENA	R/W	0h	<p>High Speed Enable (SD Mode Only)</p> <p>This bit is optional. Before setting this bit, the HD shall check the MMCSDB12_CAPABILITIES[21] HIGH_SPEED_SUPPORT bit. If this bit is set to 0h (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/20 MHz for MMC). If this bit is set to 1h, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52 MHz for MMC)/208 MHz (for SD3.0).</p> <p>If the MMCSDB12_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1h, Host Driver needs to reset SD Clock Enable (MMCSDB12_CLOCK_CONTROL[2] SD_CLK_ENA) before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again. This bit is not effective in UHS-II mode.</p> <p>1h: High Speed Mode 0h: Normal Speed Mode</p>
1	DATA_WIDTH	R/W	0h	<p>Data Transfer Width (SD Mode Only)</p> <p>This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. This bit is not effective in UHS-II mode.</p> <p>1h: 4 bit mode 0h: 1 bit mode</p>
0	LED_CONTROL	R/W	0h	<p>LED Control</p> <p>This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction.</p> <p>1h: LED on 0h: LED off</p>

18.6.13 MMCSD12_POWER_CONTROL Register (Offset = 29h) [reset = 0h]

MMCSD12_POWER_CONTROL is shown in [Figure 18-193](#) and described in [Table 18-496](#).

Return to [Summary Table](#).

This register is used to program the SD Bus power and voltage level.

Table 18-495. MMCSD12_POWER_CONTROL Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0029h
MMCSD2_CTL_CFG	04F9 8029h

Figure 18-193. MMCSD12_POWER_CONTROL Register

7	6	5	4	3	2	1	0
UHS2_VOLTAGE			UHS2_POWER	SD_BUS_VOLTAGE			SD_BUS_POWER
R/W-0h			R/W-0h	R/W-0h			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-496. MMCSD12_POWER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	UHS2_VOLTAGE	R/W	0h	SD Bus Voltage Select for VDD2 (UHS-II Only) This field determines supply voltage range to VDD2. This field can be set to 5h if the MMCSD12_CAPABILITIES[60] VDD2_1P8_SUPPORT bit is set to 1h. 111b: Not used 110b: Not used 101b: 1.8 V 100b: Reserved for 1.2 V 011b – 001b: Reserved 000b: VDD2 Not Supported
4	UHS2_POWER	R/W	0h	SD Bus Power for VDD2 (UHS-II Only) Setting this bit enables providing VDD2. 1h: Power on 0h: Power off
3-1	SD_BUS_VOLTAGE	R/W	0h	SD Bus Voltage Select for VDD1 By setting these bits, the HD selects the voltage level for the SD card. Before setting this register, the HD shall check the voltage support bits in the MMCSD12_CAPABILITIES register. If an unsupported voltage is selected, the Host System shall not supply SD bus voltage. 111b: 3.3 V (Flattop.) 110b: 3.0 V (Typ.) 101b: 1.8 V (Typ.) for Embedded 100b – 000b: Reserved

Table 18-496. MMCSDB12_POWER_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SD_BUS_POWER	R/W	0h	<p>SD Bus Power for VDD1</p> <p>Before setting this bit, the SD host driver shall set SD Bus Voltage Select (MMCSDB12_POWER_CONTROL[3-1] SD_BUS_VOLTAGE). If the HC detects the No Card State, this bit shall be cleared. If this bit is cleared, the Host Controller should immediately stop driving CMD and DAT[3:0] (tri-state), and drive SDCLK to low level. If card is connected to Host Controller, Host Controller shall set these lines to low before stopping to supply VDD1.</p> <p>In UHS-II mode, before clearing this bit, Host Driver shall clear the MMCSDB12_CLOCK_CONTROL[2] SD_CLK_ENA bit and before stopping to supply VDD1, Host Controller shall set DAT[2] to low if DAT[2] is used as out-of band interrupt.</p> <p>1h: Power on 0h: Power off</p>

18.6.14 MMCSD12_BLOCK_GAP_CONTROL Register (Offset = 2Ah) [reset = 80h]

MMCSD12_BLOCK_GAP_CONTROL is shown in [Figure 18-194](#) and described in [Table 18-498](#).

Return to [Summary Table](#).

This register is used to program the block gap request, read wait control and interrupt at block gap.

**Table 18-497. MMCSD12_BLOCK_GAP_CONTROL
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 002Ah
MMCSD2_CTL_CFG	04F9 802Ah

Figure 18-194. MMCSD12_BLOCK_GAP_CONTROL Register

7	6	5	4	3	2	1	0
BOOT_ACK_ENA	ALT_BOOT_MODE	BOOT_ENABLE	RESERVED	INTRPT_AT_BLK_GAP	RDWAIT_CTRL	CONTINUE	STOP_AT_BLK_GAP
R/W-1h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-498. MMCSD12_BLOCK_GAP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOT_ACK_ENA	R/W	1h	Boot Acknowledge Check To check for the boot acknowledge in boot operation. 1h: Wait for boot ack from eMMC card 0h: Will not wait for boot ack from eMMC card
6	ALT_BOOT_MODE	R/W	0h	Alternative Boot Mode To start boot code access in alternative mode. 1h: To start alternate boot mode access 0h: To stop alternate boot mode access
5	BOOT_ENABLE	R/W	0h	Boot Enable To start boot code access. 1h: To start boot code access 0h: To stop boot code access
4	RESERVED	R	0h	Reserved
3	INTRPT_AT_BLK_GAP	R/W	0h	Interrupt At Block Gap (SD Mode Only) This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1h enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0h. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card.

Table 18-498. MMCSDB12_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RDWAIT_CTRL	R/W	0h	<p>Read Wait Control (SD Mode Only)</p> <p>The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1h otherwise DAT line conflict may occur. If this bit is set to 0h, Suspend/Resume cannot be supported.</p> <p>In UHS-II mode, Read Wait is disabled and DAT[2] line is used for Interrupt Signal from UHS-II Card.</p> <p>1h: Enable Read Wait Control 0h: Disable Read Wait Control</p>
1	CONTINUE	R/W	0h	<p>Continue Request</p> <p>This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0h (MMCSDB12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 0h) and set this bit to restart the transfer.</p> <p>The Host Controller automatically clears this bit when the transaction re-starts.</p> <p>If MMCSDB12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h, any write to this bit is ignored.</p> <p>In SD mode, this bit is cleared in either of the following cases:</p> <ol style="list-style-type: none"> 1) In the case of a read transaction, the DAT Line Active changes from 0h to 1h as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0h to 1h as the write transaction restarts. <p>Therefore it is not necessary for Host driver to set this bit to 0h. If MMCSDB12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP = 1h, any write to this bit is ignored.</p> <p>1h: Restart 0h: Ignored</p>

Table 18-498. MMCSD12_BLOCK_GAP_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	STOP_AT_BLK_GAP	R/W	0h	<p>Stop At Block Gap Request</p> <p>This bit is used to stop executing a transaction at the next block gap for non-DMA, SDMA and ADMA transfers. Until the transfer complete is set to 1h, indicating a transfer completion the HD shall leave this bit set to 1h.</p> <p>Clearing both the MMCSD12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP and MMCSD12_BLOCK_GAP_CONTROL[1] CONTINUE bits shall not cause the transaction to restart. The MMCSD12_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL bit is used to stop the read transaction at the block gap. The HC shall honour Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1h (MMCSD12_BLOCK_GAP_CONTROL[2] RDWAIT_CTRL) = 1h). In case of write transfers in which the HD writes data to the MMCSD12_DATA_PORT register, the HD shall set this bit after all block data is written. If this bit is set to 1h, the HD shall not write data to the MMCSD12_DATA_PORT register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit (DAT) in the MMCSD12_PRESENTSTATE register.</p> <p>In case of UHS-II, a transaction can be stopped at the boundary of DATA Burst (Flow Control basis). Host Controller waits for sending Flow Control MSG until the MMCSD12_BLOCK_GAP_CONTROL[1] CONTINUE bit is set to 1h.</p> <p>1h: Stop 0h: Transfer</p>

There are three cases to restart the transfer after stop at the block gap. Which case is appropriate depends on whether the HC issues a Suspend command or the SD card accepts the Suspend command.

1. If the HD does not issue Suspend command, the Continue Request shall be used to restart the transfer.
2. If the HD issues a Suspend command and the SD card accepts it, a Resume Command shall be used to restart the transfer.
3. If the HD issues a Suspend command and the SD card does not accept it, the Continue Request shall be used to restart the transfer.

Any time Stop At Block Gap Request stops the data transfer, the HD shall wait for Transfer Complete (in the MMCSD12_NORMAL_INTR_STS register) before attempting to restart the transfer. When restarting the data transfer by Continue Request, the HD shall clear Stop At Block Gap Request before or simultaneously.

Host Controller should not generate timeout interrupts while Stop At Block Gap is set. Host Driver should ignore timeout interrupts while Stop At Block Gap is set.

18.6.15 MMCSDB12_WAKEUP_CONTROL Register (Offset = 2Bh) [reset = 0h]

MMCSDB12_WAKEUP_CONTROL is shown in [Figure 18-195](#) and described in [Table 18-500](#).

Return to [Summary Table](#).

This register is used to program the wakeup functionality.

The MMCSDB12_WAKEUP_CONTROL register is mandatory for the HC, but wakeup functionality depends on the HC system hardware and software. The HD shall maintain voltage on the SD Bus, by setting the MMCSDB12_POWER_CONTROL[0] SD_BUS_POWER bit to 1h, when wakeup event via card interrupt is desired.

Table 18-499. MMCSDB12_WAKEUP_CONTROL Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 002Bh
MMCSDB2_CTL_CFG	04F9 802Bh

Figure 18-195. MMCSDB12_WAKEUP_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED					CARD_REMOVAL	CARD_INSERTION	CARD_INTERRUPT
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-500. MMCSDB12_WAKEUP_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	CARD_REMOVAL	R/W	0h	Wakeup Event Enable On SD Card Removal This bit enables wakeup event via Card removal assertion in the MMCSDB12_NORMAL_INTR_STS register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1h: Enable 0h: Disable
1	CARD_INSERTION	R/W	0h	Wakeup Event Enable On SD Card Insertion This bit enables wakeup event via Card Insertion assertion in the MMCSDB12_NORMAL_INTR_STS register. FN_WUS (Wake up Support) in CIS does not affect this bit. 1h: Enable 0h: Disable
0	CARD_INTERRUPT	R/W	0h	Wakeup Event Enable On Card Interrupt This bit enables wakeup event via Card Interrupt assertion in the MMCSDB12_NORMAL_INTR_STS register. This bit can be set to 1h if FN_WUS (Wake Up Support) in CIS is set to 1h. 1h: Enable 0h: Disable

18.6.16 MMCSD12_CLOCK_CONTROL Register (Offset = 2Ch) [reset = 0h]

MMCSD12_CLOCK_CONTROL is shown in [Figure 18-196](#) and described in [Table 18-502](#).

Return to [Summary Table](#).

This register is used to program the Clock frequency select, Clock generator select, Clock enable, Internal clock state fields.

At the initialization of the HC, the HD shall set the SDCLK Frequency Select (MMCSD12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL) according to the MMCSD12_CAPABILITIES register. This register controls SDCLK in SD Mode and RCLK in UHS-II mode.

**Table 18-501. MMCSD12_CLOCK_CONTROL
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 002Ch
MMCSD2_CTL_CFG	04F9 802Ch

Figure 18-196. MMCSD12_CLOCK_CONTROL Register

15	14	13	12	11	10	9	8
SDCLK_FRQSEL							
R/W-0h							
7	6	5	4	3	2	1	0
SDCLK_FRQSEL_UPBITS	CLKGEN_SEL	RESERVED	PLL_ENA	SD_CLK_ENA	INT_CLK_STABLE	INT_CLK_ENA	
R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-502. MMCS12_CLOCK_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	SDCLK_FRQSEL	R/W	0h	<p>SDCLK/RCLK Frequency Select</p> <p>This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the Capabilities register (MMCS12_CAPABILITIES[15-8] BASE_CLK_FREQ).</p> <p>Only the following settings are allowed.</p> <p>(1) 8-bit Divided Clock Mode:</p> <p>80h: base clock divided by 256</p> <p>40h: base clock divided by 128</p> <p>20h: base clock divided by 64</p> <p>10h: base clock divided by 32</p> <p>08h: base clock divided by 16</p> <p>04h: base clock divided by 8</p> <p>02h: base clock divided by 4</p> <p>01h: base clock divided by 2</p> <p>00h: base clock (10 MHz - 63 MHz)</p> <p>Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The three default divider values can be calculated by the frequency that is defined by the MMCS12_CAPABILITIES[15-8] BASE_CLK_FREQ bit field.</p> <p>400 KHz divider value</p> <p>25 MHz divider value</p> <p>50 MHz divider value</p> <p>According to the Physical Layer Specification, the maximum SD Clock frequency is 25 MHz in normal speed mode and 50 MHz in high speed mode, and shall never exceed this limit.</p> <p>The frequency of SDCLK is set by the following formula:</p> <p>Clock Frequency = (Base Clock) / divisor</p> <p>Thus, choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency.</p> <p>For example, if the MMCS12_CAPABILITIES[15-8] BASE_CLK_FREQ bit field has the value 33 MHz, and the target frequency is 25 MHz, then choosing the divisor value of 1h will yield 16.5 MHz, which is the nearest frequency less than or equal to the target. Similarly, to approach a clock value of 400 KHz, the divisor value of 40h yields the optimal clock value of 258 KHz.</p> <p>(2) 10-bit Divided Clock Mode:</p> <p>Host Controller Version 3.00 or later supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits and all divider values shall be supported.</p> <p>3FFh: 1/2046 Divided Clock</p> <p>N: 1/2N Divided Clock (Duty 50%)</p> <p>002h: 1/4 Divided Clock</p> <p>001h: 1/2 Divided Clock</p> <p>000h: Base Clock (10 MHz - 254 MHz)</p> <p>(3) Programmable Clock Mode:</p>

Table 18-502. MMCSD12_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				<p>Host Controller Version 3.00 or later supports this mode as optional. A non-zero value set to the MMCSD12_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field indicates support of this clock mode. The multiplier enables the Host System to select a finer grain SD clock frequency. It is not necessary to support all frequency generation specified by this field because programmable clock generator is vendor specific and dependent on the implementation. Therefore, this mode is used with Preset Value registers (MMCSD12_PRESET_VALUE0 - MMCSD12_PRESET_VALUE10). The Host Controller vendor provides possible settings and the Host System vendor sets appropriate values to the Preset Value registers (MMCSD12_PRESET_VALUE0 - MMCSD12_PRESET_VALUE10).</p> <p>3FFh - Base Clock \times M / 1024</p> <p>.....</p> <p>N-1 - Base Clock \times M / N</p> <p>.....</p> <p>002h - Base Clock \times M / 3</p> <p>001h - Base Clock \times M / 2</p> <p>000h - Base Clock \times M</p> <p>This field depends on setting of the MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this field is set by Host Driver. If MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this field is automatically set to a value specified in one of Preset Value registers (MMCSD12_PRESET_VALUE0 - MMCSD12_PRESET_VALUE10).</p>
7-6	SDCLK_FRQSEL_UPBITS	R/W	0h	<p>Upper Bits of SDCLK/RCLK Frequency Select</p> <p>This bit field is assigned to the MMCSD12_CLOCK_CONTROL[9-8] SDCLK_FRQSEL bit field of clock divider in SDCLK/RCLK Frequency Select.</p>
5	CLKGEN_SEL	R/W	0h	<p>Clock Generator Select</p> <p>This bit is used to select the clock generator mode in SDCLK/RCLK Frequency Select (MMCSD12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL).</p> <p>If the Programmable Clock Mode is supported (non-zero value is set to the MMCSD12_CAPABILITIES[55-48] CLOCK_MULTIPLIER bit field), this bit attribute is R/W, and if not supported, this bit attribute is RO and zero is read.</p> <p>This bit depends on the setting of the MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this bit is set by Host Driver. If MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this bit is automatically set to a value specified in one of Preset Value registers (MMCSD12_PRESET_VALUE0 - MMCSD12_PRESET_VALUE10).</p> <p>1h: Programmable Clock Mode</p> <p>0h: Divided Clock Mode</p>

Table 18-502. MMCS12_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	R	0h	Reserved
3	PLL_ENA	R/W	0h	<p>PLL Enable</p> <p>This bit is added from Version 4.10 for Host Controller using PLL. This feature allows Host Controller to initialize clock generator in two steps: by Internal Clock Enable (MMCS12_CLOCK_CONTROL[0] INT_CLK_ENA) and PLL Enable and to minimize output latency (for example SDCLK/RCLK, D0 lane) from SD Clock Enable (MMCS12_CLOCK_CONTROL[2] SD_CLK_ENA). There are two modes to keep Host Drivers compatibility. In both modes, PLL Locked timing is indicated by Internal Clock Stable (MMCS12_CLOCK_CONTROL[1] INT_CLK_STABLE).</p> <p>(1) When MMCS12_HOST_CONTROL2[12] HOST_VER40_ENA = 0h (Host Driver Version 3, which does not support this bit) or this bit is not implemented, the MMCS12_CLOCK_CONTROL[0] INT_CLK_ENA bit (or the MMCS12_CLOCK_CONTROL[2] SD_CLK_ENA bit) may activate PLL (exit low power mode and start locking clock).</p> <p>(2) When MMCS12_HOST_CONTROL2[12] HOST_VER40_ENA = 1h (Host Driver Version 4), the MMCS12_CLOCK_CONTROL[0] INT_CLK_ENA bit is set before setting this bit and then setting this bit may activate PLL (exit low power mode and start locking clock).</p> <p>1h: PLL is enabled 0h: PLL is in low power mode</p>
2	SD_CLK_ENA	R/W	0h	<p>SD Clock Enable</p> <p>The HC shall stop SDCLK when writing this bit to 0h. The MMCS12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field can be changed when this bit is 0h. Then, the HC shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK = 0). If the HC detects the No Card state, this bit shall be cleared.</p> <p>1h: Enable providing SDCLK or RCLK 0h: Disable providing SDCLK or RCLK</p>
1	INT_CLK_STABLE	R	0h	<p>Internal Clock Stable</p> <p>This bit is set to 1h when SD clock is stable after writing 1h to MMCS12_CLOCK_CONTROL[0] INT_CLK_ENA bit. The SD Host Driver shall wait to set the MMCS12_CLOCK_CONTROL[2] SD_CLK_ENA bit until this bit is set to 1h.</p> <p>Note: This is useful when using PLL for a clock oscillator that requires setup time.</p> <p>(1) Internal Clock Stable (when MMCS12_CLOCK_CONTROL[3] PLL_ENA = 0h or not supported)</p> <p>This bit is set to 1h when internal clock is stable after writing 1h to MMCS12_CLOCK_CONTROL[0] INT_CLK_ENA bit.</p> <p>(2) PLL Clock Stable (when MMCS12_CLOCK_CONTROL[3] PLL_ENA = 1h)</p> <p>Host Controller which supports PLL Enable sets this status to 0h once when PLL Enable is changed 0h to 1h and then this status is set to 1h when PLL is locked (PLL uses an internal clock in stable as a reference clock which is enabled by the MMCS12_CLOCK_CONTROL[0] INT_CLK_ENA bit). After this bit is set to 1h, Host Driver may set the MMCS12_CLOCK_CONTROL[2] SD_CLK_ENA bit.</p> <p>1h: Ready 0h: Not Ready</p>

Table 18-502. MMCSD12_CLOCK_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT_CLK_ENA	R/W	0h	<p>Internal Clock Enable</p> <p>This bit is set to 0h when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1h. When clock oscillation is stable, the HC shall set the MMCSD12_CLOCK_CONTROL[1] INT_CLK_STABLE bit to 1h. This bit shall not affect card detection.</p> <p>1h: Oscillate 0h: Stop</p>

18.6.17 MMCS12_TIMEOUT_CONTROL Register (Offset = 2Eh) [reset = 0h]

MMCS12_TIMEOUT_CONTROL is shown in [Figure 18-197](#) and described in [Table 18-504](#).

Return to [Summary Table](#).

The register sets the data timeout counter value.

At the initialization of the HC, the HD shall set the Data Timeout Counter Value according to the MMCS12_CAPABILITIES register.

Table 18-503. MMCS12_TIMEOUT_CONTROL Instances

Instance	Physical Address
MMCS1_CTL_CFG	04FB 002Eh
MMCS2_CTL_CFG	04F9 802Eh

Figure 18-197. MMCS12_TIMEOUT_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED				COUNTER_VALUE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-504. MMCS12_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	COUNTER_VALUE	R/W	0h	<p>Data Timeout Counter Value</p> <p>This value determines the interval by which DAT line time-outs are detected. Refer to the MMCS12_ERROR_INTR_STS[4] DATA_TIMEOUT bit for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the SD clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the MMCS12_ERROR_INTR_STS[4] DATA_TIMEOUT bit.</p> <p>1111: Reserved</p> <p>1110: $TMCLK \times 2^{27}$</p> <p>-----</p> <p>-----</p> <p>0001: $TMCLK \times 2^{14}$</p> <p>0000: $TMCLK \times 2^{13}$</p>

18.6.18 MMCSD12_SOFTWARE_RESET Register (Offset = 2Fh) [reset = 0h]

MMCSD12_SOFTWARE_RESET is shown in [Figure 18-198](#) and described in [Table 18-506](#).

Return to [Summary Table](#).

This register is used to program the software reset for data, command and for all.

A reset pulse is generated when writing 1h to each bit of this register. After completing the reset, the HC shall clear each bit. Because it takes some time to complete software reset, the SD Host Driver shall confirm that these bits are 0h.

**Table 18-505. MMCSD12_SOFTWARE_RESET
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 002Fh
MMCSD2_CTL_CFG	04F9 802Fh

Figure 18-198. MMCSD12_SOFTWARE_RESET Register

7	6	5	4	3	2	1	0
RESERVED					SWRST_FOR_DAT	SWRST_FOR_CMD	SWRST_FOR_ALL
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-506. MMCSD12_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	SWRST_FOR_DAT	R/W	0h	<p>Software Reset for DAT Line (SD Mode Only)</p> <p>Only part of data circuit is reset. The following registers and bits are cleared by this bit:</p> <p>MMCSD12_DATA_PORT register:</p> <p>Buffer is cleared and Initialized.</p> <p>MMCSD12_PRESENTSTATE register:</p> <p>Buffer read Enable</p> <p>Buffer write Enable</p> <p>Read Transfer Active</p> <p>Write Transfer Active</p> <p>DAT Line Active</p> <p>Command Inhibit (DAT)</p> <p>MMCSD12_BLOCK_GAP_CONTROL register:</p> <p>Continue Request</p> <p>Stop At Block Gap Request</p> <p>MMCSD12_NORMAL_INTR_STS register:</p> <p>Buffer Read Ready</p> <p>Buffer Write Ready</p> <p>Block Gap Event</p> <p>Transfer Complete</p> <p>1h: Reset</p> <p>0h: Work</p>

Table 18-506. MMCSDB12_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SWRST_FOR_CMD	R/W	0h	<p>Software Reset for CMD Line (SD Mode Only)</p> <p>Only part of command circuit is reset to be able to issue a command. From Version 4.10, this bit is also used to initialize UHS-II command circuit. This reset is effective only command issuing circuit (including response error statuses related to Command Inhibit (CMD) control - MMCSDB12_PRESENTSTATE[0] INHIBIT_CMD bit) and does not affect data transfer circuit. Host Controller can continue data transfer even this reset is executed during handling of sub command response errors.</p> <p>The following registers and bits are cleared by this bit:</p> <p>MMCSDB12_PRESENTSTATE register:</p> <p>Command Inhibit (CMD)</p> <p>MMCSDB12_NORMAL_INTR_STS register:</p> <p>Command Complete</p> <p>MMCSDB12_ERROR_INTR_STS register (Error Interrupt Status from Version 4.10)</p> <p>Response error statuses related to Command Inhibit (CMD) - MMCSDB12_PRESENTSTATE[0] INHIBIT_CMD bit</p> <p>1h: Reset</p> <p>0h: Work</p>
0	SWRST_FOR_ALL	R/W	0h	<p>Software Reset for All</p> <p>This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0h. During its initialization, the HD shall set this bit to 1h to reset the HC. The HC shall reset this bit to 0h when Capabilities registers are valid and the HD can read them. Additional use of 'Software Reset For All' may not affect the value of the Capabilities registers. If this bit is set to 1h, the SD card shall reset itself and must be re-initialized by the HD.</p> <p>1h: Reset</p> <p>0h: Work</p>

18.6.19 MMCSDB12_NORMAL_INTR_STS Register (Offset = 30h) [reset = 0h]

MMCSDB12_NORMAL_INTR_STS is shown in [Figure 18-199](#) and described in [Table 18-508](#).

Return to [Summary Table](#).

This register gives the status of all the interrupts.

The Normal Interrupt Signal Enable (see MMCSDB12_NORMAL_INTR_SIG_ENA register) affects read of this register, but Normal Interrupt Signal does not affect these reads. An Interrupt is generated when the Normal Interrupt Signal Enable is enabled and at least one of the status bits is set to 1h. For all bits except Card Interrupt (MMCSDB12_NORMAL_INTR_STS[8] CARD_INTR) and Error Interrupt (MMCSDB12_NORMAL_INTR_STS[15] ERROR_INTR), writing 1h to a bit clears it. The MMCSDB12_NORMAL_INTR_STS[8] CARD_INTR bit is cleared when the card stops asserting the interrupt: that is when the Card Driver services the Interrupt condition.

**Table 18-507. MMCSDB12_NORMAL_INTR_STS
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0030h
MMCSDB2_CTL_CFG	04F9 8030h

Figure 18-199. MMCSDB12_NORMAL_INTR_STS Register

15	14	13	12	11	10	9	8
ERROR_INTR	BOOT_COMPL ETE	RCV_BOOT_A CK	RETUNING_EV ENT	INTC	INTB	INTA	CARD_INTR
R-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CARD_REM	CARD_INS	BUF_RD_REA DY	BUF_WR_REA DY	DMA_INTERRU PT	BLK_GAP_EVE NT	XFER_COMPL ETE	CMD_COMPLE TE
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-508. MMCSDB12_NORMAL_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ERROR_INTR	R	0h	Error Interrupt If any of the bits in the MMCSDB12_ERROR_INTR_STS register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. In UHS-II mode is enabled, if any of the bits in the MMCSDB12_UHS2_ERR_INTR_STS register are set, this bit is also set. 0h: No Error 1h: Error
14	BOOT_COMPLETE	R/W1C	0h	Boot Terminate Interrupt This status is set if the boot operation gets terminated. 0h: Boot operation is not terminated 1h: Boot operation is terminated
13	RCV_BOOT_ACK	R/W1C	0h	Boot Acknowledge Receive This status is set if the boot acknowledge is received from device. 0h: Boot acknowledge is not received 1h: Boot acknowledge is received

Table 18-508. MMCS D12_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	RETUNING_EVENT	R	0h	Re-Tuning Event (UHS-I Only) This status is set if the MMCS D12_PRESENTSTATE[3] RETUNING_REQ bit changes from 0h to 1h. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. In UHS-II mode, this bit is not effective. 1h: Re-Tuning should be performed 0h: Re-Tuning is not required
11	INTC	R	0h	int_c (Embedded) This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_C interrupt factor.
10	INTB	R	0h	int_b (Embedded) This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_B interrupt factor.
9	INTA	R	0h	int_a (Embedded) This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1h does not clear this bit. It is cleared by resetting the INT_A interrupt factor.

Table 18-508. MMCSD12_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CARD_INTR	R	0h	<p>Card Interrupt</p> <p>When this status has been set and the Host Driver needs to start this interrupt service, the MMCSD12_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit may be set to 0h in order to clear the card interrupt status latched in the Host Controller and to stop driving the interrupt signal to the Host System. After completion of the card interrupt service (it should reset interrupt factors in the SD card and the interrupt signal may not be asserted), set the MMCSD12_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 1h and start sampling the interrupt signal again. Writing this bit to 1h does not clear this bit. It is cleared by resetting the SD card interrupt factor.</p> <p>(1) DAT[1] Interrupt Input in SD Mode</p> <p>In 1-bit mode, the Host Controller shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the SD card and the interrupt to the Host System. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of UHS-I mode, switching time of Interrupt Period is relaxed for 2 clock cycles. Then Host Controller needs to delay start of interrupt sampling at least 2 clocks and should sample interrupt while Interrupt Period is stable.</p> <p>(2) DAT[2] Interrupt Input in UHS-II Mode</p> <p>When the MMCSD12_PRESENTSTATE[16] CARD_INSERTED and MMCSD12_POWER_CONTROL[0] SD_BUS_POWER bits are set to 1h, Host Controller configures DAT[2] as Interrupt Input and enables pull-up of DAT[2]. DAT[2] interrupt is asynchronous to RCLK, low level sensitive and 3.3 V signal level. DAT[2] interrupt is masked by setting the MMCSD12_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit to 0h. When either the MMCSD12_PRESENTSTATE[16] CARD_INSERTED bit or the MMCSD12_POWER_CONTROL[0] SD_BUS_POWER bit is set to 0h, Host Controller sets DAT[2] to low. Only point to point connection is allowed between Host and Card.</p> <p>(3) INT MSG in UHS-II Mode</p> <p>INT MSG is enabled by setting the MMCSD12_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit. DAT[2] and INT MSG interrupt sources are ORed and indicated to Card Interrupt. If any bit in the MMCSD12_UHS2_DEVICE_INTR_STATUS register is set to 1h, INT MSG interrupt is generated. INT MSG interrupt is cleared by writing a correspondent bit to 1h in the MMCSD12_UHS2_DEVICE_INTR_STATUS register. Masking DAT[2] interrupt also disables INT MSG interrupt due to the MMCSD12_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit is set to 0h. SDIO Version 4.00 does not support INT MSG.</p> <p>1h: Generate Card Interrupt 0h: No Card Interrupt</p>

Table 18-508. MMCSDB12_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CARD_REM	R/W1C	0h	<p>Card Removal</p> <p>This status is set if the MMCSDB12_PRESENTSTATE[16] CARD_INSERTED bit changes from 1h to 0h. When the HD writes this bit to 1h to clear this status the status of the MMCSDB12_PRESENTSTATE[16] CARD_INSERTED bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated.</p> <p>0h: Card State Stable or Debouncing 1h: Card Removed</p>
6	CARD_INS	R/W1C	0h	<p>Card Insertion</p> <p>This status is set if the MMCSDB12_PRESENTSTATE[16] CARD_INSERTED bit changes from 0h to 1h. When the HD writes this bit to 1h to clear this status the status of the MMCSDB12_PRESENTSTATE[16] CARD_INSERTED bit should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated.</p> <p>0h: Card State Stable or Debouncing 1h: Card Inserted</p>
5	BUF_RD_READY	R/W1C	0h	<p>Buffer Read Ready</p> <p>This status is set if the MMCSDB12_PRESENTSTATE[11] BUF_RD_ENA bit changes from 0h to 1h.</p> <p>The MMCSDB12_PRESENTSTATE[11] BUF_RD_ENA bit is set to 1h for every CMD19 execution in tuning procedure.</p> <p>In UHS-II mode, this bit is set at FC (Flow Control) unit basis.</p> <p>0h: Not Ready to read Buffer 1h: Ready to read Buffer</p>
4	BUF_WR_READY	R/W1C	0h	<p>Buffer Write Ready</p> <p>This status is set if the MMCSDB12_PRESENTSTATE[10] BUF_WR_ENA bit changes from 0h to 1h.</p> <p>In UHS-II mode, this bit is set at FC (Flow Control) unit basis.</p> <p>0h: Not Ready to Write Buffer 1h: Ready to Write Buffer</p>
3	DMA_INTERRUPT	R/W1C	0h	<p>DMA Interrupt</p> <p>This status is set if the HC detects the Host DMA Buffer Boundary in the MMCSDB12_BLOCK_SIZE register.</p> <p>0h: No DMA Interrupt 1h: DMA Interrupt is Generated</p>
2	BLK_GAP_EVENT	R/W1C	0h	<p>Block Gap Event</p> <p>If the MMCSDB12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set, this bit is set.</p> <p>Read Transaction:</p> <p>This bit is set at the falling edge of the DAT Line Active Status (see MMCSDB12_PRESENTSTATE[2] DATA_LINE_ACTIVE bit). When the transaction is stopped at SD Bus timing. The Read Wait must be supported in order to use this function.</p> <p>Write Transaction:</p> <p>This bit is set at the falling edge of Write Transfer Active Status (see MMCSDB12_PRESENTSTATE[8] WR_XFER_ACTIVE bit). After getting CRC status at SD Bus timing. In UHS-II mode, this bit is set at FC (Flow Control) unit basis.</p> <p>0h: No Block Gap Event 1h: Transaction stopped at Block Gap</p>

Table 18-508. MMCSD12_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	XFER_COMPLETE	R/W1C	0h	<p>Transfer Complete</p> <p>This bit is set when a read/write transaction is completed.</p> <p>SD Mode</p> <p>Read Transaction:</p> <p>This bit is set at the falling edge of Read Transfer Active Status (MMCSD12_PRESENTSTATE[9] RD_XFER_ACTIVE).</p> <p>There are two cases in which the Interrupt is generated. The first is when a data transfer is completed as specified by data length (after the last data has been read to the Host System). The second is when data has stopped at the block gap and completed the data transfer by setting the MMCSD12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit (after valid data has been read to the Host System).</p> <p>Write Transaction:</p> <p>This bit is set at the falling edge of the DAT Line Active Status (see MMCSD12_PRESENTSTATE[2] DATA_LINE_ACTIVE bit). There are two cases in which the Interrupt is generated. The first is when the last data is written to the card as specified by data length and Busy signal is released. The second is when data transfers are stopped at the block gap by setting the MMCSD12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit and data transfers completed (after valid data is written to the SD card and the busy signal is released).</p> <p>Note: MMCSD12_NORMAL_INTR_STS[1] XFER_COMPLETE bit has higher priority than the MMCSD12_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If both bits are set to 1h, the data transfer can be considered complete.</p> <p>Note: While performing tuning procedure (the MMCSD12_HOST_CONTROL2[6] EXECUTE_TUNING bit is set to 1h), the MMCSD12_NORMAL_INTR_STS[1] XFER_COMPLETE bit is not set to 1h.</p> <p>Command with Busy:</p> <p>This bit is set when busy is de-asserted. Refer to DAT Line Active and Command Inhibit (DAT) in the MMCSD12_PRESENTSTATE register.</p> <p>UHS-I mode</p> <p>While performing tuning procedure (the MMCSD12_HOST_CONTROL2[6] EXECUTE_TUNING bit is set to 1h), the MMCSD12_NORMAL_INTR_STS[1] XFER_COMPLETE bit is not set to 1h.</p> <p>0h: No Data Transfer Complete 1h: Data Transfer Complete</p> <p>UHS-II Mode</p> <p>This interrupt is generated in following two cases:</p> <p>(a) EBSY Completion (for EBSY supported commands) When the MMCSD12_UHS2_XFER_MODE[14] EBSY_WAIT bit is set to 1h, this bit is set when EBSY packet has been received, and all valid data have been sent to system memory in case of read operation.</p> <p>(b) Stop and Continue during DCMD Data Transfer When the MMCSD12_BLOCK_GAP_CONTROL[0] STOP_AT_BLK_GAP bit is set to 1h and data transfer is stopped at the Flow Control.</p> <p>Following is for both SD mode and UHS-II mode.</p>

Table 18-508. MMCSDB12_NORMAL_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				<p>The table below shows that the MMCSDB12_NORMAL_INTR_STS[1] XFER_COMPLETE bit has higher priority than the MMCSDB12_ERROR_INTR_STS[4] DATA_TIMEOUT bit. If both bits are set to 1h, execution of a command can be considered to be completed.</p> <p>1h: Command execution is completed 0h: Not complete</p>
0	CMD_COMPLETE	R/W1C	0h	<p>Command Complete</p> <p>SD Mode</p> <p>This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23).</p> <p>Note: The MMCSDB12_ERROR_INTR_STS[0] CMD_TIMEOUT bit has higher priority than the MMCSDB12_NORMAL_INTR_STS[0] CMD_COMPLETE bit. If both are set to 1h, it can be considered that the response was not received correctly.</p> <p>Version 4.00 defines response check function for R1 and R5. If the MMCSDB12_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1h, generation of this interrupt is prohibited regardless of the MMCSDB12_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit.</p> <p>UHS-II Mode</p> <p>If the MMCSDB12_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 0h, this interrupt is generated when response packet is received.</p> <p>If the MMCSDB12_TRANSFER_MODE[8] RESP_INTR_DIS bit is set to 1h, generation of this interrupt is prohibited regardless of the MMCSDB12_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit.</p> <p>0h: No Command Complete 1h: Command Complete</p>

Table 18-509 shows the relation between transfer complete and data timeout error.

Table 18-509. Relation between transfer complete and data timeout error

Transfer Complete	Data Timeout Error	Meaning of the Status
0	0	Interrupted by Another Factor
0	1	Timeout occur during transfer
1	Don't Care	Data Transfer Complete

Table 18-510 shows the relation between command complete and command timeout error.

Table 18-510. Relation between command complete and command timeout error

Command Complete	Command Timeout Error	Meaning of the Status
0	0	Interrupted by Another Factor
Don't Care	1	Response not received within 64 SDCLK cycles
1	0	Response Received

18.6.20 MMCSD12_ERROR_INTR_STS Register (Offset = 32h) [reset = 0h]

MMCSD12_ERROR_INTR_STS is shown in [Figure 18-200](#) and described in [Table 18-512](#).

Return to [Summary Table](#).

This register gives the status of the error interrupts.

Status defined in this register can be enabled by the MMCSD12_ERROR_INTR_STS_ENA register, but not by the MMCSD12_ERROR_INTR_SIG_ENA register. The Interrupt is generated when the MMCSD12_ERROR_INTR_SIG_ENA register is enabled and at least one of the statuses is set to 1h. Writing to 1h clears the bit and writing to 0h keeps the bit unchanged. More than one status can be cleared at the one register write.

**Table 18-511. MMCSD12_ERROR_INTR_STS
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0032h
MMCSD2_CTL_CFG	04F9 8032h

Figure 18-200. MMCSD12_ERROR_INTR_STS Register

15	14	13	12	11	10	9	8
RESERVED			HOST	RESP	RESERVED	ADMA	AUTO_CMD
R-0h			R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-512. MMCSD12_ERROR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	HOST	R/W1C	0h	Target Response Error Occurs when detecting ERROR in m_hresp (DMA transaction) 0h: No error 1h: Error
11	RESP	R/W1C	0h	Response Error (SD Mode Only) Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If the MMCSD12_TRANSFER_MODE[7] RESP_ERR_CHK_ENA bit is set to 1h, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1h. 0h: No error 1h: Error
10	RESERVED	R	0h	Reserved
9	ADMA	R/W1C	0h	ADMA Error This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the MMCSD12_ADMA_ERR_STATUS register. 0h: No error 1h: Error

Table 18-512. MMCSDB12_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	AUTO_CMD	R/W1C	0h	<p>Auto CMD Error (SD Mode Only)</p> <p>Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that any of the bits D00 to D05 in the MMCSDB12_AUTOCMD_ERR_STS register has changed from 0h to 1h. D07 is effective in case of Auto CMD12. The MMCSDB12_AUTOCMD_ERR_STS register is valid while this bit is set to 1h and may be cleared with clearing of this bit (another implementation is also allowed).</p> <p>0h: No error 1h: Error</p>
7	CURR_LIMIT	R/W1C	0h	<p>Current Limit Error</p> <p>By setting the MMCSDB12_POWER_CONTROL[0] SD_BUS_POWER bit, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1h means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function.</p> <p>0h: No error 1h: Power Fail</p>
6	DATA_ENDBIT	R/W1C	0h	<p>Data End Bit Error (SD Mode Only)</p> <p>Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status.</p> <p>0h: No error 1h: Error</p>
5	DATA_CRC	R/W1C	0h	<p>Data CRC Error (SD Mode Only)</p> <p>Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 2h.</p> <p>0h: No error 1h: Error</p>
4	DATA_TIMEOUT	R/W1C	0h	<p>Data Timeout Error (SD Mode Only)</p> <p>Occurs when detecting one of following timeout conditions:</p> <ol style="list-style-type: none"> 1. Busy Timeout for R1b, R5b type 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout <p>0h: No error 1h: Timeout</p>
3	CMD_INDEX	R/W1C	0h	<p>Command Index Error (SD Mode Only)</p> <p>Occurs if a Command Index error occurs in the Command Response (MMCSDB12_RESPONSE_0 to MMCSDB12_RESPONSE_7).</p> <p>0h: No error 1h: Error</p>

Table 18-512. MMCSD12_ERROR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CMD_ENDBIT	R/W1C	0h	Command End Bit Error (SD Mode Only) Occurs when detecting that the end bit of a command response is 0h. 0h: No error 1h: End Bit Error Generated
1	CMD_CRC	R/W1C	0h	Command CRC Error (SD Mode Only) Command CRC Error is generated in two cases. 1. If a response is returned and the MMCSD12_ERROR_INTR_STS[0] CMD_TIMEOUT bit is set to 0h, this bit is set to 1h when detecting a CRT error in the command response. 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (Stop driving CMD line) and set this bit to 1h. The MMCSD12_ERROR_INTR_STS[0] CMD_TIMEOUT bit shall also be set to 1h to distinguish CMD line conflict. 0h: No error 1h: CRC Error Generated
0	CMD_TIMEOUT	R/W1C	0h	Command Timeout Error (SD Mode Only) Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case the MMCSD12_ERROR_INTR_STS[1] CMD_CRC bit shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. 0h: No error 1h: Timeout

Table 18-513 shows the relation between command CRC error and command time-out error.

Table 18-513. Relation between command CRC error and command time-out error

Command CRC Error	Command Time-out Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD Line Conflict

18.6.21 MMCSDB12_NORMAL_INTR_STS_ENA Register (Offset = 34h) [reset = 0h]

MMCSDB12_NORMAL_INTR_STS_ENA is shown in [Figure 18-201](#) and described in [Table 18-515](#).

Return to [Summary Table](#).

This register is used to enable the MMCSDB12_NORMAL_INTR_STS register fields.

Table 18-514. MMCSDB12_NORMAL_INTR_STS_ENA Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0034h
MMCSDB2_CTL_CFG	04F9 8034h

Figure 18-201. MMCSDB12_NORMAL_INTR_STS_ENA Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPL ETE	RCV_BOOT_A CK	RETUNING_EV ENT	INTC	INTB	INTA	CARD_INTERRUPT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CARD_REMOV AL	CARD_INSERT ION	BUF_RD_REA DY	BUF_WR_REA DY	DMA_INTERRUPT	BLK_GAP_EVE NT	XFER_COMPL ETE	CMD_COMPLE TE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-515. MMCSDB12_NORMAL_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	Fixed to 0 The HC shall control error Interrupts using the MMCSDB12_ERROR_INTR_STS_ENA register.
14	BOOT_COMPLETE	R/W	0h	Boot Terminate Interrupt Enable 0h: Masked 1h: Enabled
13	RCV_BOOT_ACK	R/W	0h	Boot Acknowledge Enable 0h: Masked 1h: Enabled
12	RETUNING_EVENT	R/W	0h	Re-Tuning Event Status Enable (UHS-I Only) 0h: Masked 1h: Enabled
11	INTC	R/W	0h	INT_C Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts.
10	INTB	R/W	0h	INT_B Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts.
9	INTA	R/W	0h	INT_A Status Enable (Embedded) If this bit is set to 0h, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts.

Table 18-515. MMCSD12_NORMAL_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CARD_INTERRUPT	R/W	0h	<p>Card Interrupt Status Enable</p> <p>If this bit is set to 0h, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1h. The HD may clear the MMCSD12_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts.</p> <p>By setting this bit to 0h, interrupt input should be masked by implementation so that the interrupt Input is not affected by external signal in any state (for example: floating).</p> <p>0h: Masked 1h: Enabled</p>
7	CARD_REMOVAL	R/W	0h	<p>Card Removal Status Enable</p> <p>0h: Masked 1h: Enabled</p>
6	CARD_INSERTION	R/W	0h	<p>Card Insertion Status Enable</p> <p>0h: Masked 1h: Enabled</p>
5	BUF_RD_READY	R/W	0h	<p>Buffer Read Ready Status Enable</p> <p>0h: Masked 1h: Enabled</p>
4	BUF_WR_READY	R/W	0h	<p>Buffer Write Ready Status Enable</p> <p>0h: Masked 1h: Enabled</p>
3	DMA_INTERRUPT	R/W	0h	<p>DMA Interrupt Status Enable</p> <p>0h: Masked 1h: Enabled</p>
2	BLK_GAP_EVENT	R/W	0h	<p>Block Gap Event Status Enable</p> <p>0h: Masked 1h: Enabled</p>
1	XFER_COMPLETE	R/W	0h	<p>Transfer Complete Status Enable</p> <p>0h: Masked 1h: Enabled</p>
0	CMD_COMPLETE	R/W	0h	<p>Command Complete Status Enable</p> <p>0h: Masked 1h: Enabled</p>

Note: The HC may sample the card Interrupt signal during interrupt period and may hold its value in the flip-flop. If the MMCSD12_NORMAL_INTR_STS_ENA[8] CARD_INTERRUPT bit is set to 0h, the HC shall clear all internal signals regarding Card Interrupt (MMCSD12_NORMAL_INTR_STS[8] CARD_INTR).

18.6.22 MMCSDB12_ERROR_INTR_STS_ENA Register (Offset = 36h) [reset = 0h]

MMCSDB12_ERROR_INTR_STS_ENA is shown in [Figure 18-202](#) and described in [Table 18-517](#).

Return to [Summary Table](#).

This register is used to enable the MMCSDB12_ERROR_INTR_STS register fields.

Table 18-516. MMCSDB12_ERROR_INTR_STS_ENA Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0036h
MMCSDB2_CTL_CFG	04F9 8034h

Figure 18-202. MMCSDB12_ERROR_INTR_STS_ENA Register

15	14	13	12	11	10	9	8
VENDOR_SPECIFIC				RESP	TUNING	ADMA	AUTO_CMD
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-517. MMCSDB12_ERROR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Status Enable N/A
11	RESP	R/W	0h	Response Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
10	TUNING	R/W	0h	Tuning Error Status Enable (UHS-I Only) 0h: Masked 1h: Enabled
9	ADMA	R/W	0h	ADMA Error Status Enable 0h: Masked 1h: Enabled
8	AUTO_CMD	R/W	0h	Auto CMD Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
7	CURR_LIMIT	R/W	0h	Current Limit Error Status Enable 0h: Masked 1h: Enabled
6	DATA_ENDBIT	R/W	0h	Data End Bit Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
5	DATA_CRC	R/W	0h	Data CRC Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
4	DATA_TIMEOUT	R/W	0h	Data Timeout Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled

Table 18-517. MMCSD12_ERROR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMD_INDEX	R/W	0h	Command Index Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
2	CMD_ENDBIT	R/W	0h	Command End Bit Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
1	CMD_CRC	R/W	0h	Command CRC Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled
0	CMD_TIMEOUT	R/W	0h	Command Timeout Error Status Enable (SD Mode Only) 0h: Masked 1h: Enabled

Note: To Detect CMD Line conflict, the HD must set both MMCSD12_ERROR_INTR_STS_ENA[0] CMD_TIMEOUT and MMCSD12_ERROR_INTR_STS_ENA[1] CMD_CRC bits to 1h.

18.6.23 MMCSDB12_NORMAL_INTR_SIG_ENA Register (Offset = 38h) [reset = 0h]

MMCSDB12_NORMAL_INTR_SIG_ENA is shown in [Figure 18-203](#) and described in [Table 18-519](#).

Return to [Summary Table](#).

Normal Interrupt Signal Enable Register

This register is used to select which interrupt status is indicated to the Host System as the Interrupt. These status bits all share the sample 1 bit interrupt line. Setting any of these bits to 1h enables Interrupt generation.

Table 18-518. MMCSDB12_NORMAL_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0038h
MMCSDB2_CTL_CFG	04F9 8038h

Figure 18-203. MMCSDB12_NORMAL_INTR_SIG_ENA Register

15	14	13	12	11	10	9	8
BIT15_FIXED0	BOOT_COMPLETE	RCV_BOOT_ACK	RETUNING_EVENT	INTC	INTB	INTA	CARD_INTERRUPT
R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CARD_REMOVE	CARD_INSERTION	BUF_RD_READY	BUF_WR_READY	DMA_INTERRUPT	BLK_GAP_EVENT	XFER_COMPLETE	CMD_COMPLETE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-519. MMCSDB12_NORMAL_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15_FIXED0	R	0h	Fixed to 0 The HD shall control error Interrupts using the MMCSDB12_ERROR_INTR_SIG_ENA register.
14	BOOT_COMPLETE	R/W	0h	Boot Terminate Interrupt Signal Enable 0h: Masked 1h: Enabled
13	RCV_BOOT_ACK	R/W	0h	Boot Acknowledge Receive Signal Enable 0h: Masked 1h: Enabled
12	RETUNING_EVENT	R/W	0h	Re-Tuning Event Signal Enable (UHS-I Only) 0h: Masked 1h: Enabled
11	INTC	R/W	0h	INT_C Signal Enable (Embedded) 0h: Masked 1h: Enabled
10	INTB	R/W	0h	INT_B Signal Enable (Embedded) 0h: Masked 1h: Enabled
9	INTA	R/W	0h	INT_A Signal Enable (Embedded) 0h: Masked 1h: Enabled
8	CARD_INTERRUPT	R/W	0h	Card Interrupt Signal Enable 0h: Masked 1h: Enabled

Table 18-519. MMCSD12_NORMAL_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CARD_REMOVAL	R/W	0h	Card Removal Signal Enable 0h: Masked 1h: Enabled
6	CARD_INSERTION	R/W	0h	Card Insertion Signal Enable 0h: Masked 1h: Enabled
5	BUF_RD_READY	R/W	0h	Buffer Read Ready Signal Enable 0h: Masked 1h: Enabled
4	BUF_WR_READY	R/W	0h	Buffer Write Ready Signal Enable 0h: Masked 1h: Enabled
3	DMA_INTERRUPT	R/W	0h	DMA Interrupt Signal Enable 0h: Masked 1h: Enabled
2	BLK_GAP_EVENT	R/W	0h	Block Gap Event Signal Enable 0h: Masked 1h: Enabled
1	XFER_COMPLETE	R/W	0h	Transfer Complete Signal Enable 0h: Masked 1h: Enabled
0	CMD_COMPLETE	R/W	0h	Command Complete Signal Enable 0h: Masked 1h: Enabled

18.6.24 MMCSDB12_ERROR_INTR_SIG_ENA Register (Offset = 3Ah) [reset = 0h]

MMCSDB12_ERROR_INTR_SIG_ENA is shown in [Figure 18-204](#) and described in [Table 18-521](#).

Return to [Summary Table](#).

Error Interrupt Signal Enable Register

This register is used to select which interrupt status is notified to the Host System as the Interrupt. These status bits all share the same 1 bit interrupt line. Setting any of these bits to 1h enables Interrupt generation.

Table 18-520. MMCSDB12_ERROR_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 003Ah
MMCSDB2_CTL_CFG	04F9 803Ah

Figure 18-204. MMCSDB12_ERROR_INTR_SIG_ENA Register

15	14	13	12	11	10	9	8
VENDOR_SPECIFIC				RESP	TUNING	ADMA	AUTO_CMD
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CURR_LIMIT	DATA_ENDBIT	DATA_CRC	DATA_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-521. MMCSDB12_ERROR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Signal Enable N/A
11	RESP	R/W	0h	Response Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
10	TUNING	R/W	0h	Tuning Error Signal Enable (UHS-I Only) 0h: Masked 1h: Enabled
9	ADMA	R/W	0h	ADMA Error Signal Enable 0h: Masked 1h: Enabled
8	AUTO_CMD	R/W	0h	Auto CMD Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
7	CURR_LIMIT	R/W	0h	Current Limit Error Signal Enable 0h: Masked 1h: Enabled
6	DATA_ENDBIT	R/W	0h	Data End Bit Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
5	DATA_CRC	R/W	0h	Data CRC Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled

Table 18-521. MMCSD12_ERROR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DATA_TIMEOUT	R/W	0h	Data Timeout Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
3	CMD_INDEX	R/W	0h	Command Index Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
2	CMD_ENDBIT	R/W	0h	Command End Bit Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
1	CMD_CRC	R/W	0h	Command CRC Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled
0	CMD_TIMEOUT	R/W	0h	Command Timeout Error Signal Enable (SD Mode Only) 0h: Masked 1h: Enabled

18.6.25 MMCSDB12_AUTOCMD_ERR_STS Register (Offset = 3Ch) [reset = 0h]

MMCSDB12_AUTOCMD_ERR_STS is shown in [Figure 18-205](#) and described in [Table 18-523](#).

Return to [Summary Table](#).

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD23.

The Host driver can determine what kind of Auto CMD12/CMD23 errors occur by this register. Auto CMD23 errors are indicated in bit 04-01. This register is valid only when the Auto CMD Error is set.

Table 18-522. MMCSDB12_AUTOCMD_ERR_STS Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 003Ch
MMCSDB2_CTL_CFG	04F9 803Ch

Figure 18-205. MMCSDB12_AUTOCMD_ERR_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMD_NOT_ISSUED	RESERVED		INDEX	ENDBIT	CRC	TIMEOUT	ACMD12_NOT_EXEC
R-0h	R-0h		R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 18-523. MMCSDB12_AUTOCMD_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMD_NOT_ISSUED	R	0h	Command Not Issued By Auto CMD12 Error Setting this bit to 1h means CMD_wo_DAT is not executed due to an Auto CMD12 error (D04- D01) in this register. This bit is set to 0h when Auto CMD Error is generated by Auto CMD23. 0h: No Error 1h: Not Issued
6-5	RESERVED	R	0h	Reserved
4	INDEX	R	0h	Auto CMD Index Error Occurs if the Command Index error occurs in response to a command. 0h: No Error 1h: Error
3	ENDBIT	R	0h	Auto CMD End Bit Error Occurs when detecting that the end bit of command response is 0h. 0h: No Error 1h: End Bit Error Generated
2	CRC	R	0h	Auto CMD CRC Error Occurs when detecting a CRC error in the command response. 0h: No Error 1h: CRC Error Generated

Table 18-523. MMCSD12_AUTOCMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TIMEOUT	R	0h	Auto CMD Timeout Error Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1h, the other error status bits (D04 - D02) are meaningless. 0h: No Error 1h: Timeout
0	ACMD12_NOT_EXEC	R	0h	Auto CMD12 not Executed If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1h means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1h, other error status bits (D04 - D01) are meaningless. This bit is set to 0h when Auto CMD Error is generated by Auto CMD23. 0h: Executed 1h: Not Executed

Table 18-524 shows the relation between Auto CMD12 CRC error and Auto CMD12 timeout error.

Table 18-524. Relation between Auto CMD12 CRC Error and Auto CMD12 Timeout Error

Auto Cmd12 CRC Error	Auto CMD12 Timeout Error	Kinds of Error
0	0	No Error
0	1	Response Timeout Error
1	0	Response CRC Error
1	1	CMD Line Conflict

The timing of changing Auto CMD12 Error Status can be classified in three scenarios:

1. When the HC is going to issue Auto CMD12:

Set D00 to 1h if Auto CMD12 cannot be issued due to an error in the previous command.

Set D00 to 0h if Auto CMD12 is issued.

2. At the end bit of Auto CMD12 response:

Check received responses by checking the error bits D01, D02, D03, D04.

set to 1h if Error is Detected.

set to 0h if Error is Not Detected.

3. Before reading the Auto CMD12 Error Status bit D07:

Set D07 to 1h if there is a command cannot be issued.

Set D07 to 0h if there is no command to issue.

Timing of generating the Auto CMD12 Error and writing to the MMCSD12_COMMAND register are Asynchronous. Then D07 shall be sampled when driver never writing to the MMCSD12_COMMAND register. So just before reading the MMCSD12_AUTOCMD_ERR_STS register is good timing to set the D07 status bit.

18.6.26 MMCSDB12_HOST_CONTROL2 Register (Offset = 3Eh) [reset = 0h]

MMCSDB12_HOST_CONTROL2 is shown in [Figure 18-206](#) and described in [Table 18-526](#).

Return to [Summary Table](#).

This register is used to program UHS Mode Select, Driver Strength Select, Execute Tuning, Sampling Clock Select, Asynchronous Interrupt Enable and Preset Value Enable.

**Table 18-525. MMCSDB12_HOST_CONTROL2
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 003Eh
MMCSDB2_CTL_CFG	04F9 803Eh

Figure 18-206. MMCSDB12_HOST_CONTROL2 Register

15	14	13	12	11	10	9	8
PRESET_VALU E_ENA	ASYNCH_INTR _ENA	BIT64_ADDRE SSING	HOST_VER40_ ENA	CMD23_ENA	ADMA2_LEN_ MODE	DRIVER_STRE NGTH2	UHS2_INTF_E NABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SAMPLING_CL K_SELECT	EXECUTE_TU NING	DRIVER_STRENGTH1	V1P8_SIGNAL_ ENA	UHS_MODE_SELECT			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-526. MMCSDB12_HOST_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PRESET_VALUE_ENA	R/W	0h	<p>Preset Value Enable</p> <p>Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When the MMCSDB12_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to automatic. This bit enables the functions defined in the Preset Value registers (MMCSDB12_PRESET_VALUE0 - MMCSDB12_PRESET_VALUE10).</p> <p>If this bit is set to 0h, SDCLK Frequency Select, Clock Generator Select in the MMCSDB12_CLOCK_CONTROL register and Driver Strength Select in the MMCSDB12_HOST_CONTROL2 register are set by Host Driver.</p> <p>If this bit is set to 1h, SDCLK Frequency Select, Clock Generator Select in the MMCSDB12_CLOCK_CONTROL register and Driver Strength Select in the MMCSDB12_HOST_CONTROL2 register are set by Host Controller as specified in the Preset Value registers (MMCSDB12_PRESET_VALUE0 - MMCSDB12_PRESET_VALUE10).</p> <p>0h: SDCLK and Driver Strength are controlled by Host Driver</p> <p>1h: Automatic Selection by Preset Value are Enabled</p>

Table 18-526. MMCSD12_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	ASYNCH_INTR_ENA	R/W	0h	<p>Asynchronous Interrupt Enable</p> <p>This bit can be set to 1h if a card support asynchronous interrupt and the MMCSD12_CAPABILITIES[29] ASYNCH_INTR_SUPPORT bit is set to 1h. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode . If this bit is set to 1h, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card.</p> <p>0h: Disabled 1h: Enabled</p>
13	BIT64_ADDRESSING	R/W	0h	<p>64-bit Addressing</p> <p>This field is effective when the MMCSD12_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h.</p> <p>Host Controller selects either of 32-bit or 64-bit addressing modes to access system memory. Whether 32-bit or 64-bit is determined by OS installed in a host system. Host Driver sets this bit depends on addressing mode of installed OS. Refer to 64-bit System Address Support in the MMCSD12_CAPABILITIES register.</p> <p>0h: 32-bits Addressing 1h: 64-bits Addressing</p>
12	HOST_VER40_ENA	R/W	0h	<p>Host Version 4 Enable</p> <p>This bit selects either Version 3.00 compatible mode or Version 4.00 mode. In Version 4.00, support of 64-bit System Addressing is modified. All DMAs support 64-bit System Addressing. UHS-II supported Host Driver shall enable this bit.</p> <p>In Version 4.10, supported 32-bit Block Count for all operations. Functions of following fields are modified.</p> <p>SDMA Address SDMA uses the MMCSD12_ADMA_SYS_ADDRESS register instead of SDMA System Address register (MMCSD12_SDMA_SYS_ADDR_LO/MMCSD12_SDMA_SYS_ADDR_HI)</p> <p>ADMA2/ADMA3 Selection ADMA3 is selected by MMCSD12_HOST_CONTROL1[4-3] DMA_SELECT bit.</p> <p>64-bit ADMA Descriptor Size 128-bit descriptor is used instead of 96-bit descriptor when 64-bit Addressing is set to 1h.</p> <p>Selection of 32-bit/64-bit System Addressing Either 32-bit or 64-bit system addressing is selected by 64-bit Addressing bit in this register instead of MMCSD12_HOST_CONTROL1[4-3] DMA_SELECT bit.</p> <p>32-bit Block Count SDMA System Address register (MMCSD12_SDMA_SYS_ADDR_LO/MMCSD12_SDMA_SYS_ADDR_HI) is modified to 32-bit Block Count register.</p> <p>0h: Version 3.00 Compatible Mode 1h: Version 4.Mode</p>

Table 18-526. MMCSDB12_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CMD23_ENA	R/W	0h	<p>CMD23 Enable</p> <p>In memory card initialization, Host Driver Version 4.10 checks whether card supports CMD23 by checking a bit SCR[33]. If the card supports CMD23 (SCR[33] = 1h), this bit is set to 1h. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 data transfer. Refer to MMCSDB12_TRANSFER_MODE[3-2] AUTO_CMD_ENA bit.</p>
10	ADMA2_LEN_MODE	R/W	0h	<p>ADMA2 Length Mode</p> <p>This bit selects one of ADMA2 Length Modes either 16-bit or 26-bit.</p> <p>0h: 16-bit Data Length Mode</p> <p>1h: 26-bit Data Length Mode</p>
9	DRIVER_STRENGTH2	R/W	0h	<p>Driver Strength Select</p> <p>This is the programmed Drive Strength output and Bit[2] of the sdhccore_drivestrength value.</p>
8	UHS2_INTF_ENABLE	R/W	0h	<p>UHS-II Interface Enable</p> <p>This bit is used to enable UHS-II Interface. Before trying to start UHS-II initialization, this bit shall be set to 1h. Before trying to start SD mode initialization, this bit shall be set to 0h.</p> <p>This bit is used to enable UHS-II IF Detection, Lane Synchronization and In Dormant State in the MMCSDB12_PRESENTSTATE register, and to select clock source of either SD mode or UHS-II mode. Host Controller shall not leave unused SD 4-bit Interface lines (CLK, CMD and DAT[3:2]) floating in UHS-II mode by using pull-up or driving to low. When DAT[2] is used as interrupt input in UHS-II mode, DAT[2] of Host Controller is set to input and then DAT[2] of SDIO card is set to output to avoid conflict.</p> <p>0h: 4-bit SD Interface Enabled</p> <p>1h: UHS-II Interface Enabled</p>
7	SAMPLING_CLK_SELECT	R/W	0h	<p>Sampling Clock Select (UHS-I Only)</p> <p>This bit is set by tuning procedure when the MMCSDB12_HOST_CONTROL2[6] EXECUTE_TUNING bit is cleared. Writing 1h to this bit is meaningless and ignored. Setting 1h means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0h. Change of this bit is not allowed while the Host Controller is receiving response or a read data block.</p> <p>0h: Fixed clock is used to sample data</p> <p>1h: Tuned clock is used to sample data</p>
6	EXECUTE_TUNING	R/W	0h	<p>Execute Tuning (UHS-I Only)</p> <p>This bit is set to 1h to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to the MMCSDB12_HOST_CONTROL2[7] SAMPLING_CLK_SELECT bit. Tuning procedure is aborted by writing 0h for more detail about tuning procedure.</p> <p>0h: Not Tuned or Tuning Completed</p> <p>1h: Execute Tuning</p>

Table 18-526. MMCSD12_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	DRIVER_STRENGTH1	R/W	0h	<p>Driver Strength Select (UHS-I Only)</p> <p>Host Controller output driver in 1.8 V signaling is selected by this bit. In 3.3 V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the MMCSD12_CAPABILITIES register. This bit depends on setting of the MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA bit. If MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA = 0h, this field is set by Host Driver.</p> <p>If MMCSD12_HOST_CONTROL2[15] PRESET_VALUE_ENA = 1h, this field is automatically set by a value specified in the one of Preset Value registers (MMCSD12_PRESET_VALUE0 - MMCSD12_PRESET_VALUE10).</p> <p>0h: Driver Type B is Selected (Default) 1h: Driver Type A is Selected 2h: Driver Type C is Selected 3h: Driver Type D is Selected</p>
3	V1P8_SIGNAL_ENA	R/W	0h	<p>1.8 V Signaling Enable (UHS-I Only)</p> <p>This bit controls voltage regulator for I/O cell. 3.3 V is supplied to the card regardless of signaling voltage.</p> <p>Setting this bit from 0h to 1h starts changing signal voltage from 3.3 V to 1.8 V.</p> <p>1.8 V regulator output shall be stable within 5 ms. Host Controller clears this bit if switching to 1.8 V signaling fails.</p> <p>Clearing this bit from 1h to 0h starts changing signal voltage from 1.8 V to 3.3 V.</p> <p>3.3 V regulator output shall be stable within 5 ms.</p> <p>Host Driver can set this bit to 1h when Host Controller supports 1.8 V signaling (one of support bits is set to 1h: SDR50, SDR104 or DDR50 in the MMCSD12_CAPABILITIES register) and the card or device supports UHS-I.</p> <p>0h: 3.3 V Signaling 1h: 1.8 V Signaling</p>

Table 18-526. MMCS12_HOST_CONTROL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	UHS_MODE_SELECT	R/W	0h	<p>UHS Mode Select (UHS-I Only)</p> <p>This field is used to select one of UHS-I modes or UHS-II mode. In case of UHS-I mode, this field is effective when the MMCS12_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit is set to 1h. In case of UHS-II mode, the MMCS12_HOST_CONTROL2[3] V1P8_SIGNAL_ENA bit shall be set to 0h. Setting of this field is used to select one of preset values in UHS-I or UHS-II mode.</p> <p>If the MMCS12_HOST_CONTROL2[15] PRESET_VALUE_ENA is set to 1h, Host Controller sets SDCLK/RCLK Frequency Select, Clock Generator Select in the MMCS12_CLOCK_CONTROL register and Driver Strength Select according to Preset Value registers (MMCS12_PRESET_VALUE0 - MMCS12_PRESET_VALUE10). In this case, one of preset value registers is selected by this field.</p> <p>Host Driver needs to reset the MMCS12_CLOCK_CONTROL[2] SD_CLK_ENA bit before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets the MMCS12_CLOCK_CONTROL[2] SD_CLK_ENA bit again.</p> <p>0h: SDR12 1h: SDR25 2h: SDR50 3h: SDR104 4h: DDR50 5h: HS400 6h: Reserved 7h: UHS-II</p> <p>When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more details.</p>

18.6.27 MMCSDB12_CAPABILITIES Register (Offset = 40h) [reset = 180004073FE8C801h]

MMCSDB12_CAPABILITIES is shown in [Figure 18-207](#) and described in [Table 18-528](#).

Return to [Summary Table](#).

This register provides the HD with information specific to the HC implementation. The HC may implement these values as fixed or loaded from flash memory during power on initialization.

Table 18-527. MMCSDB12_CAPABILITIES Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0040h
MMCSDB2_CTL_CFG	04F9 8040h

Figure 18-207. MMCSDB12_CAPABILITIES Register

63	62	61	60	59	58	57	56
HS400_SUPPO RT	RESERVED		VDD2_1P8_SU PPORT	ADMA3_SUPP ORT	RESERVED	SPI_BLK_MOD E	SPI_SUPPORT
R-0h	R-0h		R-1h	R-1h	R-0h	R-0h	R-0h
55	54	53	52	51	50	49	48
CLOCK_MULTIPLIER							
R-0h							
47	46	45	44	43	42	41	40
RETUNING_MODES	TUNING_FOR_ SDR50	RESERVED	RETUNING_TIMER_CNT				
R-0h	R-0h	R-0h	R-4h				
39	38	37	36	35	34	33	32
RESERVED	DRIVERD_SUP PORT	DRIVERC_SUP PORT	DRIVERA_SUP PORT	UHS2_SUPPO RT	DDR50_SUPP ORT	SDR104_SUPP ORT	SDR50_SUPP ORT
R-0h	R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-1h
31	30	29	28	27	26	25	24
SLOT_TYPE	ASYNCH_INTR_ _SUPPORT	ADDR_64BIT_ SUPPORT_V3	ADDR_64BIT_ SUPPORT_V4	VOLT_1P8_SU PPORT	VOLT_3P0_SU PPORT	VOLT_3P3_SU PPORT	
R-0h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h	R-1h
23	22	21	20	19	18	17	16
SUSP_RES_S UPPORT	SDMA_SUPPO RT	HIGH_SPEED_ SUPPORT	RESERVED	ADMA2_SUPP ORT	BUS_8BIT_SU PPORT	MAX_BLK_LENGTH	
R-1h	R-1h	R-1h	R-0h	R-1h	R-0h	R-0h	
15	14	13	12	11	10	9	8
BASE_CLK_FREQ							
R-C8h							
7	6	5	4	3	2	1	0
TIMEOUT_CLK_ _UNIT	RESERVED	TIMEOUT_CLK_FREQ					
R-0h	R-0h	R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 18-528. MMCSDB12_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
63	HS400_SUPPORT	R	0h	HS400 Support 0h: HS400 is Not Supported 1h: HS400 is Supported

Table 18-528. MMCSDB12_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
62-61	RESERVED	R	0h	Reserved
60	VDD2_1P8_SUPPORT	R	1h	1.8 V VDD2 Support This bit indicates that support of VDD2 on Host system. 0h: 1.8 V VDD2 is not supported 1h: 1.8 V VDD2 is supported
59	ADMA3_SUPPORT	R	1h	ADMA3 Support This bit indicates that support of ADMA3 on Host Controller. 0h: ADMA3 is not supported 1h: ADMA3 is supported
58	RESERVED	R	0h	Reserved
57	SPI_BLK_MODE	R	0h	SPI Block Mode This bit indicates whether SPI Block Mode is supported or not. 0h: Not Supported 1h: Supported
56	SPI_SUPPORT	R	0h	SPI Mode This bit indicates whether SPI Mode is supported or not. 0h: Not Supported 1h: Supported
55-48	CLOCK_MULTIPLIER	R	0h	Clock Multiplier This field indicates clock multiplier value of programmable clock generator. Refer to the MMCSDB12_CLOCK_CONTROL register. Setting 00h means that Host Controller does not support programmable clock generator. FFh: Clock Multiplier M = 256 ---- 02h: Clock Multiplier M = 3 01h: Clock Multiplier M = 2 00h: Clock Multiplier is Not Supported
47-46	RETUNING_MODES	R	0h	Re-tuning Modes (UHS-I Only) This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver. 0h: Mode 1 1h: Mode 2 2h: Mode 3 3h: Reserved There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.
45	TUNING_FOR_SDR50	R	0h	Use Tuning for SDR50 (UHS-I Only) If this bit is set to 1h, this Host Controller requires tuning to operate SDR50 (tuning is always required to operate SDR104). 0h: SDR50 does not require tuning 1h: SDR50 requires tuning Note: Tuning is required for SDR50 to compensate temperature variation.
44	RESERVED	R	0h	Reserved

Table 18-528. MMCSD12_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
43-40	RETUNING_TIMER_CNT	R	4h	<p>Timer Count for Re-Tuning (UHS-I Only)</p> <p>This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3.</p> <p>0h - Get information via other source</p> <p>1h = 1 seconds</p> <p>2h = 2 seconds</p> <p>3h = 4 seconds</p> <p>4h = 8 seconds</p> <p>----</p> <p>$n = 2^{(n-1)}$ seconds</p> <p>----</p> <p>Bh = 1024 seconds</p> <p>Fh - Ch = Reserved</p>
39	RESERVED	R	0h	Reserved
38	DRIVERD_SUPPORT	R	0h	<p>Driver Type D Support (UHS-I Only)</p> <p>This bit indicates support of Driver Type D for 1.8 Signaling.</p> <p>0h: Driver Type D is Not Supported</p> <p>1h: Driver Type D is Supported</p>
37	DRIVERC_SUPPORT	R	0h	<p>Driver Type C Support (UHS-I Only)</p> <p>This bit indicates support of Driver Type C for 1.8 Signaling.</p> <p>0h: Driver Type C is Not Supported</p> <p>1h: Driver Type C is Supported</p>
36	DRIVERA_SUPPORT	R	0h	<p>Driver Type A Support (UHS-I Only)</p> <p>This bit indicates support of Driver Type A for 1.8 Signaling.</p> <p>0h: Driver Type A is Not Supported</p> <p>1h: Driver Type A is Supported</p>
35	UHS2_SUPPORT	R	0h	<p>UHS-II Support (UHS-II Only)</p> <p>This bit indicates whether Host Controller supports UHS-II.</p> <p>If this bit is set to 1h, the MMCSD12_CAPABILITIES[60] VDD2_1P8_SUPPORT bit shall be set to 1h (Host System shall support VDD2 power supply).</p> <p>0h: UHS-II is Not Supported</p> <p>1h: UHS-II is Supported</p>
34	DDR50_SUPPORT	R	1h	<p>DDR50 Support (UHS-I Only)</p> <p>This bit indicates whether DDR50 is supported or not.</p> <p>0h: DDR50 is Not Supported</p> <p>1h: DDR50 is Supported</p>
33	SDR104_SUPPORT	R	1h	<p>SDR104 Support (UHS-I Only)</p> <p>This bit indicates whether SDR104 is supported or not. SDR104 requires tuning.</p> <p>0h: SDR104 is Not Supported</p> <p>1h: SDR104 is Supported</p> <p>Note: SDR104 mode is not supported (see <i>MMCSD Not Supported Features</i>).</p>
32	SDR50_SUPPORT	R	1h	<p>SDR50 Support (UHS-I Only)</p> <p>If SDR104 is supported, this bit shall be set to 1h. Bit 40 indicates whether SDR50 requires tuning or not.</p> <p>0h: SDR50 is Not Supported</p> <p>1h: SDR50 is Supported</p>

Table 18-528. MMCSDB12_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31-30	SLOT_TYPE	R	0h	<p>Slot Type</p> <p>This field indicates usage of a slot by a specific Host System (a host controller register set is defined per slot). Embedded slot for one device (1h) means that only one non-removable device is connected to a SD bus slot. Shared Bus Slot (2h) can be set if Host Controller supports Shared Bus Control register.</p> <p>The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus (2h), the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System.</p> <p>0h: Removable Card Slot 1h: Embedded Slot for One Device 2h: Shared Bus Slot (SD Mode) 3h: UHS-II Multiple Embedded Devices</p>
29	ASYNCH_INTR_SUPPORT	R	1h	<p>Asynchronous Interrupt Support (SD Mode Only)</p> <p>Refer to SDIO Specification Version 3.00 about asynchronous interrupt.</p> <p>0h: Asynchronous Interrupt Not Supported 1h: Asynchronous Interrupt Supported</p>
28	ADDR_64BIT_SUPPORT_V3	R	1h	<p>64-bit System Address Support for V3</p> <p>Meaning of this bit is different depends on Versions. Host Controller Version 3.00 and Version 4.10 use this bit as 64-bit System Address support for V3 mode. Host Controller Version 4.00 uses this bit as 64-bit System Address support for both V3 and V4 modes.</p> <p>SDMA cannot be used in 64-bit Addressing in Version 3 mode.</p> <p>If this bit is set to 1h, 64-bit ADMA2 with using 96-bit Descriptor may be enabled as follows:</p> <p>In case of Host Controller Version 3, 64-bit ADMA2 is enabled by MMCSDB12_HOST_CONTROL1[4-3] DMA_SELECT = 3h. In case of Host Controller Version 4, 64-bit ADMA2 for Version 3 is enabled by setting MMCSDB12_HOST_CONTROL2[12] HOST_VER40_ENA = 0h and MMCSDB12_HOST_CONTROL1[4-3] DMA_SELECT = 3h.</p> <p>0h: 64-bit System Address for V3 is not Supported 1h: 64-bit System Address for V3 is Supported</p>
27	ADDR_64BIT_SUPPORT_V4	R	1h	<p>64-bit System Address Support for V4</p> <p>This bit is added from Version 4.10. Setting 1h to this bit indicates that the Host Controller supports 64-bit System Addressing of Version 4 mode.</p> <p>When this bit is set to 1h, full or a part of 64-bit address should be used to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to the MMCSDB12_HOST_CONTROL2[13] BIT64_ADDRESSING bit.</p> <p>If this bit is set to 1h, 64-bit DMA Addressing for Version 4 is enabled by setting MMCSDB12_HOST_CONTROL2[12] HOST_VER40_ENA = 1h, MMCSDB12_HOST_CONTROL2[13] BIT64_ADDRESSING = 1h. SDMA can be used and ADMA2 uses 128-bit Descriptor.</p> <p>0h: 64-bit System Address for V4 is not Supported 1h: 64-bit System Address for V4 is Supported</p>

Table 18-528. MMCSDB12_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	VOLT_1P8_SUPPORT	R	1h	Voltage Support 1.8 V This bit indicates whether the HC supports 1.8 V. 0h: 1.8 V Not Supported 1h: 1.8 V Supported
25	VOLT_3P0_SUPPORT	R	1h	Voltage Support 3.0 V This bit indicates whether the HC supports 3.0 V. 0h: 3.0 V Not Supported 1h: 3.0 V Supported
24	VOLT_3P3_SUPPORT	R	1h	Voltage Support 3.3 V This bit indicates whether the HC supports 3.3 V. 0h: 3.3 V Not Supported 1h: 3.3 V Supported
23	SUSP_RES_SUPPORT	R	1h	Suspend/Resume Support This bit indicates whether the HC supports Suspend/Resume functionality. If this bit is 0h, the Suspend and Resume mechanism are not supported and the HD shall not issue either Suspend/Resume commands. 0h: Not Supported 1h: Supported
22	SDMA_SUPPORT	R	1h	SDMA Support This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. Version 4.10 Host Controller shall support SDMA if ADMA2 is supported. 0h: SDMA Not Supported 1h: SDMA Supported
21	HIGH_SPEED_SUPPORT	R	1h	High Speed Support This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25 MHz to 50 MHz (for SD)/20 MHz to 52 MHz (for MMC). 0h: High Speed Not Supported 1h: High Speed Supported
20	RESERVED	R	0h	Reserved
19	ADMA2_SUPPORT	R	1h	ADMA2 Support 0h: ADMA2 Not support 1h: ADMA2 support
18	BUS_8BIT_SUPPORT	R	0h	8-bit Support for Embedded Device (Embedded) This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. This bit is not effective when the MMCSDB12_CAPABILITIES[31-30] SLOT_TYPE bit field is set to 2h. 0h: 8-bit Bus Width Not Supported 1h: 8-bit Bus Width Supported
17-16	MAX_BLK_LENGTH	R	0h	Max Block Length This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. 0h: 512 byte 1h: 1024 byte 2h: 2048 byte 3h: 4096 byte

Table 18-528. MMCSDB12_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	BASE_CLK_FREQ	R	C8h	<p>Base Clock Frequency for SD Clock</p> <p>(1) 6-bit Base Clock Frequency:</p> <p>This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz.</p> <p>11xx xxxxb: Not Supported</p> <p>0011 1111b: 63 MHz</p> <p>0000 0010b: 2 MHz</p> <p>0000 0001b: 1 MHz</p> <p>0000 0000b: Get Information via another method</p> <p>(2) 8-bit Base Clock Frequency:</p> <p>This mode is supported by the Host Controller Version 3.00. Unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz.</p> <p>FFh: 255 MHz</p> <p>02h: 2 MHz</p> <p>01h: 1 MHz</p> <p>00h: Get Information via another method</p> <p>If the real frequency is 16.5 MHz, the larger value shall be set 0001 0001b (17 MHz) because the Host Driver use this value to calculate the clock divider value (refer to the MMCSDB12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field) and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host System has to get information via another method.</p>
7	TIMEOUT_CLK_UNIT	R	0h	<p>Timeout Clock Unit</p> <p>This bit shows the unit of base clock frequency used to detect Data Timeout Error (MMCSDB12_ERROR_INTR_STS[4] DATA_TIMEOUT).</p> <p>0h: KHz</p> <p>1h: MHz</p>
6	RESERVED	R	0h	Reserved
5-0	TIMEOUT_CLK_FREQ	R	1h	<p>Timeout Clock Frequency</p> <p>This bit shows the base clock frequency used to detect Data Timeout Error (MMCSDB12_ERROR_INTR_STS[4] DATA_TIMEOUT).</p> <p>0h: Get Information via another method</p> <p>Not 0h: 1 KHz to 63 KHz/1 MHz to 63 MHz</p>

Table 18-529 shows the 64-bit System Address Support depends on Versions.

Table 18-529. 64-bit System Address Support depends on Versions

Host Controller	Version 3.00	Version 4.00	Version 4.10
D28 (from Version 2.00)	for V3	for V3 and V4	for V3
D27 (from Version 4.10)	D27 (from Version 4.10)	Not Defined	for V4
Register Decode	32-bit or 64-bit (up to implementation)	32-bit or 64-bit (up to implementation)	If D27 = 1h, 64-bit
SDMA	Not supported	Supported when MMCSDB12_HOST_CONTROL2[12] HOST_VER40_ENA = 1h	Supported when MMCSDB12_HOST_CONTROL2[12] HOST_VER40_ENA = 1h
ADMA2 (96-bit Descriptor)	DMA Select = 3h	Selected by MMCSDB12_HOST_CONTROL2[12] HOST_VER40_ENA = 0h	Selected by MMCSDB12_HOST_CONTROL2[12] HOST_VER40_ENA = 0h

Table 18-529. 64-bit System Address Support depends on Versions (continued)

Host Controller	Version 3.00	Version 4.00	Version 4.10
ADMA2 (128-bit Descriptor)	Not Defined	Selected by MMCSD12_HOST_CONTROL2[12] HOST_VER40_ENA = 1h	Selected by MMCSD12_HOST_CONTROL2[12] HOST_VER40_ENA = 1h

As the specification of 64-bit System Address Support has been changed, capabilities of 64-bit functions are different depends on versions.

Definition of D28 is different depends on Versions. 96-bit Descriptor was defined by Version 2 but notation V3 is used including V2. Version 4.10 divides 64-bit System Address Support into V3 mode (D28) and V4 mode (D27) so that V3 mode can be optional. Migrate to V4 is recommended. From Host Controller Version 4.00, either V3 mode or V4 mode is selected by Host Version 4 Enable in the Host Control 2 register. V3 mode can be used if 64-bit System Address Support for V3 is set to 1h. V4 mode can be used if 64-bit System Address Support for V4 is set to 1h.

Prior to Version 4.10, address length of Host Controller registers decoding is not defined and whether 32-bit or 64-bit address is used to decode Host Controller registers is up to implementation. If Host Controller decodes 32-bit system address in default, the Host Controller Registers shall be placed in 32-bit addressing space.

When D27 = 1h, Host Controller Version 4.10 or later should use full or a part of 64-bit address to decode Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller Registers is effective regardless of setting to the MMCSD12_HOST_CONTROL2[13] BIT64_ADDRESSING bit. How to decode register also should follow a system bus specification or a mother board specification.

From Version 4.00, 64-bit System Addressing of DMA is enabled by setting to the MMCSD12_HOST_CONTROL2[13] BIT64_ADDRESSING bit. 64-bit SDMA is not supported in V3 mode and is supported in V4 mode. There are two Descriptor types for ADMA2 96-bit (V3) or 128-bit (V4). Support of 96-bit Descriptor is optional for Host Controller Version 4.10. If D28 = 0h, 96-bit Descriptor is not supported.

Note: The Host System shall support at least one of these voltages above. The HD sets the MMCSD12_POWER_CONTROL[3:1] SD_BUS_VOLTAGE bit field according to these support bits. If multiple voltages are supported, select the usable lower voltage by comparing the OCR value from the card.

These registers indicate maximum current capability for each voltage. The value is meaningful if Voltage Support is set in the MMCSD12_CAPABILITIES register.

[Table 18-530](#) describes the re-tuning modes.

Table 18-530. 64-bit System Address Support depends on Versions

Bit47-46	Re-Tuning Mode	Data length	Timer Modes
0h	Mode1	4 MB (Max.)	Always enabled
1h	Mode2	4 MB (Max.)	Stop during data transfer
2h	Reserved	Reserved	Reserved
3h	Reserved	Reserved	Reserved

There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue.

Data length per a read/write command is restricted by whether Host Controller generates Re-Tuning Request during data transfer so that re-tuning procedures can be inserted during data transfers.

18.6.28 MMCSDB12_MAX_CURRENT_CAP Register (Offset = 48h) [reset = 0h]

MMCSDB12_MAX_CURRENT_CAP is shown in [Figure 18-208](#) and described in [Table 18-532](#).

Return to [Summary Table](#).

This register indicates maximum current capability for each voltage.

Table 18-531. MMCSDB12_MAX_CURRENT_CAP Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0048h
MMCSDB2_CTL_CFG	04F9 8048h

Figure 18-208. MMCSDB12_MAX_CURRENT_CAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-0h															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED								VDD2_1P8V							
R-0h								R-0h							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								VDD1_1P8V							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDD1_3P0V								VDD1_3P3V							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-532. MMCSDB12_MAX_CURRENT_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39-32	VDD2_1P8V	R	0h	Maximum Current for 1.8 V VDD2
31-24	RESERVED	R	0h	Reserved
23-16	VDD1_1P8V	R	0h	Maximum Current for 1.8 V VDD1
15-8	VDD1_3P0V	R	0h	Maximum Current for 3.0 V VDD1
7-0	VDD1_3P3V	R	0h	Maximum Current for 3.3 V VDD1

[Table 18-533](#) describes the maximum current value.

Table 18-533. Maximum Current Value Definition

Register Value	Current Value
0	Get Information via another method
1	4 mA
2	8 mA
3	12 mA
-----	-----
255	1020 mA

18.6.29 MMCSDB12_FORCE_EVTNT_ACBDB_ERR_STS Register (Offset = 50h) [reset = 0h]

MMCSDB12_FORCE_EVTNT_ACBDB_ERR_STS is shown in [Figure 18-209](#) and described in [Table 18-535](#).

Return to [Summary Table](#).

This register is not physically implemented, rather it is an address where the MMCSDB12_AUTOCBDB_ERR_STS register can be written.

Writing 1h: set each bit of the MMCSDB12_AUTOCBDB_ERR_STS register

Writing 0h: no effect

By setting a bit in this register, the correspondent bit is set in the MMCSDB12_ERROR_INTR_STS register. In order to generate interrupt signal, the correspondent bit shall be set in the MMCSDB12_ERROR_INTR_STS_ENA register and MMCSDB12_ERROR_INTR_SIG_ENA register.

Table 18-534.
MMCSDB12_FORCE_EVTNT_ACBDB_ERR_STS
Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0050h
MMCSDB2_CTL_CFG	04F9 8050h

Figure 18-209. MMCSDB12_FORCE_EVTNT_ACBDB_ERR_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMD_NOT_ISS	RESERVED	RESP	INDEX	ENDBIT	CRC	TIMEOUT	ACBDB_NOT_EXC
W-0h	R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 18-535. MMCSDB12_FORCE_EVTNT_ACBDB_ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMD_NOT_ISS	W	0h	Force Event for Command Not Issued by AUTO CBDB12 Error 0h: Not Affected 1h: Command Not Issued By Auto CBDB12 Error Status is set
6	RESERVED	R	0h	Reserved
5	RESP	W	0h	Force Event for AUTO CBDB Response Error 0h: Not Affected 1h: Auto CBDB Response Error Status is set
4	INDEX	W	0h	Force Event for AUTO CBDB Index Error 0h: Not Affected 1h: Auto CBDB Index Error Status is set
3	ENDBIT	W	0h	Force Event for AUTO CBDB End Bit Error 0h: Not Affected 1h: Auto CBDB End bit Error Status is set
2	CRC	W	0h	Force Event for AUTO CBDB Timeout Error 0h: Not Affected 1h: Auto CBDB CRC Error Status is set

Table 18-535. MMCSDB12_FORCE_EVNT_ACMD_ERR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TIMEOUT	W	0h	Force Event for AUTO CMD Timeout Error 0h: Not Affected 1h: Auto CMD Timeout Error Status is set
0	ACMD_NOT_EXEC	W	0h	Force Event for AUTO CMD12 Not Executed 0h: Not Affected 1h: Auto CMD12 Not Executed Status is set

18.6.30 MMCSDB12_FORCE_EVNT_ERR_INT_STS Register (Offset = 52h) [reset = 0h]

MMCSDB12_FORCE_EVNT_ERR_INT_STS is shown in [Figure 18-210](#) and described in [Table 18-537](#).

Return to [Summary Table](#).

This register is not physically implemented, rather it is an address where the MMCSDB12_ERROR_INTR_STS register can be written.

The MMCSDB12_FORCE_EVNT_ERR_INT_STS register is not a physically implemented register. Rather, it is an address at which the MMCSDB12_ERROR_INTR_STS register can be written. The effect of a write to this address will be reflected in the MMCSDB12_ERROR_INTR_STS register if the corresponding bit of the MMCSDB12_ERROR_INTR_STS_ENA register is set.

Writing 1h: set each bit of the MMCSDB12_ERROR_INTR_STS register

Writing 0h: no effect

Table 18-536.
MMCSDB12_FORCE_EVNT_ERR_INT_STS Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0052h
MMCSDB2_CTL_CFG	04F9 8052h

Figure 18-210. MMCSDB12_FORCE_EVNT_ERR_INT_STS Register

15	14	13	12	11	10	9	8
VEND_SPEC				RESP	TUNING	ADMA	AUTO_CMD
W-0h				W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
CURR_LIM	DAT_ENDBIT	DAT_CRC	DAT_TIMEOUT	CMD_INDEX	CMD_ENDBIT	CMD_CRC	CMD_TIMEOUT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 18-537. MMCSDB12_FORCE_EVNT_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	VEND_SPEC	W	0h	N/A
11	RESP	W	0h	Force Event for Response Error 0h: Not Affected 1h: Response Error Status is set
10	TUNING	W	0h	Force Event for Tuning Error 0h: Not Affected 1h: Tuning Error Status is set
9	ADMA	W	0h	Force Event for ADMA Error 0h: Not Affected 1h: ADMA Error Status is set
8	AUTO_CMD	W	0h	Force Event for Auto CMD Error 0h: Not Affected 1h: Auto CMD Error Status is set
7	CURR_LIM	W	0h	Force Event for Current Limit Error 0h: Not Affected 1h: Current Limit Error Status is set
6	DAT_ENDBIT	W	0h	Force Event for Data End Bit Error 0h: Not Affected 1h: Data End Bit Error Status is set

Table 18-537. MMCSDB12_FORCE_EVNT_ERR_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DAT_CRC	W	0h	Force Event for Data CRC Error 0h: Not Affected 1h: CRC Error Status is set
4	DAT_TIMEOUT	W	0h	Force Event for Data Timeout Error 0h: Not Affected 1h: Timeout Error Status is set
3	CMD_INDEX	W	0h	Force Event for Command Index Error 0h: Not Affected 1h: Command Index Error Status is set
2	CMD_ENDBIT	W	0h	Force Event for Command End Bit Error 0h: Not Affected 1h: Command End Bit Error Status is set
1	CMD_CRC	W	0h	Force Event for Command CRC Error 0h: Not Affected 1h: Command CRC Error Status is set
0	CMD_TIMEOUT	W	0h	Force Event for CMD Timeout Error 0h: Not Affected 1h: Command Timeout Error Status is set

18.6.31 MMCSDB12_ADMA_ERR_STATUS Register (Offset = 54h) [reset = 0h]

MMCSDB12_ADMA_ERR_STATUS is shown in [Figure 18-211](#) and described in [Table 18-539](#).

Return to [Summary Table](#).

When the ADMA Error interrupt occur, this register holds the ADMA State (MMCSDB12_ADMA_ERR_STATUS[1-0] ADMA_ERR_STATE) and the MMCSDB12_ADMA_SYS_ADDRESS register holds address around the error descriptor.

**Table 18-538. MMCSDB12_ADMA_ERR_STATUS
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0054h
MMCSDB2_CTL_CFG	04F9 8054h

Figure 18-211. MMCSDB12_ADMA_ERR_STATUS Register

7	6	5	4	3	2	1	0
RESERVED					ADMA_LENGTH_ERR	ADMA_ERR_STATE	
R-0h					R-0h	R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 18-539. MMCSDB12_ADMA_ERR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	ADMA_LENGTH_ERR	R	0h	ADMA Length Mismatch Error This error occurs in the following 2 cases. While the MMCSDB12_TRANSFER_MODE[1] BLK_CNT_ENA bit being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 0h: No Error 1h: Error
1-0	ADMA_ERR_STATE	R	0h	ADMA Error State This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "2h" because ADMA never stops in this state. D01 - D00: ADMA Error State when error occurred Contents of SYS_SDR register 0h: ST_STOP (Stop DMA) Points to next of the error descriptor 1h: ST_FDS (Fetch Descriptor) Points to the error descriptor 2h: Never set this state (Not used) 3h: ST_TFR (Transfer Data) Points to the next of the error descriptor

18.6.32 MMCSDB12_ADMA_SYS_ADDRESS Register (Offset = 58h) [reset = Xh]

MMCSDB12_ADMA_SYS_ADDRESS is shown in [Figure 18-212](#) and described in [Table 18-541](#).

Return to [Summary Table](#).

This register contains the physical address used for ADMA data transfer.

**Table 18-540. MMCSDB12_ADMA_SYS_ADDRESS
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0058h
MMCSDB2_CTL_CFG	04F9 8058h

Figure 18-212. MMCSDB12_ADMA_SYS_ADDRESS Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ADMA_ADDR																															
R/W-Xh																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADMA_ADDR																															
R/W-Xh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-541. MMCSD12_ADMA_SYS_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ADMA_ADDR	R/W	Xh	<p>ADMA System Address</p> <p>The 32-bit addressing Host Driver uses lower 32-bit of this register (upper 32-bit should be set to 0h) and shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. DMA2/3 ignores lower 2-bit of this register and assumes it to be 0h. DMA in 64-bit addressing. The 64-bit addressing Host Driver uses all bits of this register and shall program Descriptor Table on 64-bit boundary and set 64-bit boundary address to this register. DMA2/3 ignores lower 3-bit of this register and assumes it to be 0h.</p> <p>SDMA</p> <p>If the MMCSD12_HOST_CONTROL2[12] HOST_VER40_ENA bit is set to 1h, SDMA use this register to indicate System Address of data location instead of using SDMA System Address register (MMCSD12_SDMA_SYS_ADDR_LO/ MMCSD12_SDMA_SYS_ADDR_HI). SDMA can be used in 32-bit and 64-bit addressing in Version 4.00.</p> <p>ADMA2</p> <p>This register holds byte address of executing command of the Descriptor table. At the start of ADMA2, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state.</p> <p>ADMA3</p> <p>This register is set by ADMA3. Host Driver is not necessary to set this register. The ADMA3 increments address of this register, which points to next line, when every time fetching a Descriptor line. When Error Interrupt is generated, this register shall hold the Descriptor address depending on the ADMA state.</p> <p>Register Value - 00000000_xxxxxxxh Addressing Mode - 32-bit System Address Register Value - xxxxxxxx_xxxxxxxh Addressing Mode - 64-bit System Address</p>

18.6.33 MMCS12_PRESET_VALUE0 Register (Offset = 60h) [reset = 100h]

MMCS12_PRESET_VALUE0 is shown in [Figure 18-213](#) and described in [Table 18-544](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

When the MMCS12_HOST_CONTROL2[15] PRESET_VALUE_ENA bit is set to 1h, SDCLK/RCLK Frequency Select and Clock Generator Select in the MMCS12_CLOCK_CONTROL register, and Driver Strength Select in the MMCS12_HOST_CONTROL2 register are automatically set based on the Selected Bus Speed Mode (see [Table 18-542](#)). This means the Host Driver needs not set these fields when preset is enabled.

Before starting the initialization sequence, the Host Driver needs to set a clock preset value to SDCLK/RCLK Frequency Select in the MMCS12_CLOCK_CONTROL register. The MMCS12_HOST_CONTROL2[15] PRESET_VALUE_ENA bit can be set after initialization completed.

[Table 18-542](#) shows the conditions to select one of preset value registers.

Table 18-542. Preset Value Register Select Condition

Selected Bus Speed Mode	1.8 V Signaling Enable (Host Control 2)	High Speed Enable (Host Control 1)	UHS-1 Mode Selection (Host Control 2)
Default Speed	0	0	don't care
High Speed	0	1	don't care
SDR12	1	don't care	0h
SDR25	1	don't care	1h
SDR50	1	don't care	2h
SDR104	1	don't care	3h
DDR50	1	don't care	4h
HS400	1	don't care	5h
Reserved	Not determined	don't care	6h
UHS-II	0	don't care	7h

**Table 18-543. MMCS12_PRESET_VALUE0
Instances**

Instance	Physical Address
MMCS1_CTL_CFG	04FB 0060h
MMCS2_CTL_CFG	04F9 8060h

Figure 18-213. MMCS12_PRESET_VALUE0 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENS EL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-100h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-100h							

LEGEND: R = Read Only; -n = value after reset

Table 18-544. MMCSD12_PRESET_VALUE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SELECT	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	100h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.34 MMCSDB12_PRESET_VALUE1 Register (Offset = 62h) [reset = 4h]

MMCSDB12_PRESET_VALUE1 is shown in [Figure 18-214](#) and described in [Table 18-546](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-545. MMCSDB12_PRESET_VALUE1
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0062h
MMCSDB2_CTL_CFG	04F9 8062h

Figure 18-214. MMCSDB12_PRESET_VALUE1 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-4h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-4h							

LEGEND: R = Read Only; -n = value after reset

Table 18-546. MMCSDB12_PRESET_VALUE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	4h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSDB12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.35 MMCSD12_PRESET_VALUE2 Register (Offset = 64h) [reset = 2h]

MMCSD12_PRESET_VALUE2 is shown in [Figure 18-215](#) and described in [Table 18-548](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-547. MMCSD12_PRESET_VALUE2
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0064h
MMCSD2_CTL_CFG	04F9 8064h

Figure 18-215. MMCSD12_PRESET_VALUE2 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-2h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -n = value after reset

Table 18-548. MMCSD12_PRESET_VALUE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.36 MMCSDB12_PRESET_VALUE3 Register (Offset = 66h) [reset = 4h]

MMCSDB12_PRESET_VALUE3 is shown in [Figure 18-216](#) and described in [Table 18-550](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-549. MMCSDB12_PRESET_VALUE3
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0066h
MMCSDB2_CTL_CFG	04F9 8066h

Figure 18-216. MMCSDB12_PRESET_VALUE3 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-4h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-4h							

LEGEND: R = Read Only; -n = value after reset

Table 18-550. MMCSDB12_PRESET_VALUE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	4h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSDB12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.37 MMCSD12_PRESET_VALUE4 Register (Offset = 68h) [reset = 2h]

MMCSD12_PRESET_VALUE4 is shown in [Figure 18-217](#) and described in [Table 18-552](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-551. MMCSD12_PRESET_VALUE4
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0068h
MMCSD2_CTL_CFG	04F9 8068h

Figure 18-217. MMCSD12_PRESET_VALUE4 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-2h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -n = value after reset

Table 18-552. MMCSD12_PRESET_VALUE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.38 MMCSDB12_PRESET_VALUE5 Register (Offset = 6Ah) [reset = 1h]

MMCSDB12_PRESET_VALUE5 is shown in [Figure 18-218](#) and described in [Table 18-554](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-553. MMCSDB12_PRESET_VALUE5
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 006Ah
MMCSDB2_CTL_CFG	04F9 806Ah

Figure 18-218. MMCSDB12_PRESET_VALUE5 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-1h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-1h							

LEGEND: R = Read Only; -n = value after reset

Table 18-554. MMCSDB12_PRESET_VALUE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	1h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSDB12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.39 MMCSD12_PRESET_VALUE6 Register (Offset = 6Ch) [reset = 0h]

MMCSD12_PRESET_VALUE6 is shown in [Figure 18-219](#) and described in [Table 18-556](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-555. MMCSD12_PRESET_VALUE6
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 006Ch
MMCSD2_CTL_CFG	04F9 806Ch

Figure 18-219. MMCSD12_PRESET_VALUE6 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-0h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-556. MMCSD12_PRESET_VALUE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.40 MMCS12_PRESET_VALUE7 Register (Offset = 6Eh) [reset = 2h]

MMCS12_PRESET_VALUE7 is shown in [Figure 18-220](#) and described in [Table 18-558](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-557. MMCS12_PRESET_VALUE7
Instances**

Instance	Physical Address
MMCS1_CTL_CFG	04FB 006Eh
MMCS2_CTL_CFG	04F9 806Eh

Figure 18-220. MMCS12_PRESET_VALUE7 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-2h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-2h							

LEGEND: R = Read Only; -n = value after reset

Table 18-558. MMCS12_PRESET_VALUE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	2h	SDCLK Frequency Select Value 10-bit preset value to set the MMCS12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.41 MMCSD12_PRESET_VALUE8 Register (Offset = 72h) [reset = 0h]

MMCSD12_PRESET_VALUE8 is shown in [Figure 18-221](#) and described in [Table 18-560](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

**Table 18-559. MMCSD12_PRESET_VALUE8
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0072h
MMCSD2_CTL_CFG	04F9 8072h

Figure 18-221. MMCSD12_PRESET_VALUE8 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-0h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-560. MMCSD12_PRESET_VALUE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCSD12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.42 MMCS12_PRESET_VALUE10 Register (Offset = 74h) [reset = 0h]

MMCS12_PRESET_VALUE10 is shown in [Figure 18-222](#) and described in [Table 18-562](#).

Return to [Summary Table](#).

This register is used to read the SDCLK Frequency Select Value, Clock Generator Select Value, Driver Strength Select Value.

Table 18-561. MMCS12_PRESET_VALUE10 Instances

Instance	Physical Address
MMCS1_CTL_CFG	04FB 0074h
MMCS2_CTL_CFG	04F9 8074h

Figure 18-222. MMCS12_PRESET_VALUE10 Register

15	14	13	12	11	10	9	8
DRIVER_STRENGTH_SEL	RESERVED				CLOCK_GENSEL	SDCLK_FRQSEL	
R-0h	R-0h				R-0h	R-0h	
7	6	5	4	3	2	1	0
SDCLK_FRQSEL							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-562. MMCS12_PRESET_VALUE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DRIVER_STRENGTH_SEL	R	0h	Driver Strength Select Value (UHS-I Only) Driver Strength is supported by 1.8 V signaling bus speed modes. This field is meaningless for 3.3 V signaling. 0h: Driver Type D is Selected 1h: Driver Type C is Selected 2h: Driver Type A is Selected 3h: Driver Type B is Selected
13-11	RESERVED	R	0h	Reserved
10	CLOCK_GENSEL	R	0h	Clock Generator Select Value This bit is effective when Host Controller supports programmable clock generator. 0h: Host Controller Version 2.00 Compatible Clock Generator 1h: Programmable Clock Generator
9-0	SDCLK_FRQSEL	R	0h	SDCLK Frequency Select Value 10-bit preset value to set the MMCS12_CLOCK_CONTROL[15-8] SDCLK_FRQSEL bit field is described by a host system.

18.6.43 MMCSDB12_ADMA3_DESC_ADDRESS Register (Offset = 78h) [reset = Xh]

MMCSDB12_ADMA3_DESC_ADDRESS is shown in [Figure 18-223](#) and described in [Table 18-564](#).

Return to [Summary Table](#).

The start address of Integrated DMA Descriptor is set to this register.

**Table 18-563. MMCSDB12_ADMA3_DESC_ADDRESS
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0078h
MMCSDB2_CTL_CFG	04F9 8078h

Figure 18-223. MMCSDB12_ADMA3_DESC_ADDRESS Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
INTG_DESC_ADDR																															
R/W-Xh																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTG_DESC_ADDR																															
R/W-Xh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-564. MMCSDB12_ADMA3_DESC_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	INTG_DESC_ADDR	R/W	Xh	<p>ADMA3 Integrated Descriptor Address</p> <p>The start address of Integrated DMA Descriptor is set to this register. Writing to a specific address starts ADMA3 depends on 32-bit/64-bit address-ing. The ADMA3 fetches one Descriptor Address and increments this field to indicate the next Descriptor address.</p> <p>The 32-bit addressing Host Driver uses lower 32-bit of this register and shall program Descriptor Table on 32-bit boundary. ADMA3 ignores lower 2-bit of this register and assumes it to be 0h. Writing to 07Bh starts ADMA3 data transfer.</p> <p>The 64-bit addressing Host Driver uses all 64-bit of this register and shall program Descriptor Table on 64-bit boundary. ADMA3 ignores lower 3-bit of this register and assumes it to be 0h. Writing to 07Fh starts ADMA3 data transfer.</p> <p>Register Value - 00000000_xxxxxxxh Addressing Mode - 32-bit System Address</p> <p>Register Value - xxxxxxxx_xxxxxxxh Addressing Mode - 64-bit System Address</p>

18.6.44 MMCSDB12_UHS2_BLOCK_SIZE Register (Offset = 80h) [reset = 0h]

MMCSDB12_UHS2_BLOCK_SIZE is shown in [Figure 18-224](#) and described in [Table 18-566](#).

Return to [Summary Table](#).

This register is used to configure the number of bytes in a data block.

**Table 18-565. MMCSDB12_UHS2_BLOCK_SIZE
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0080h
MMCSDB2_CTL_CFG	04F9 8080h

Figure 18-224. MMCSDB12_UHS2_BLOCK_SIZE Register

15	14	13	12	11	10	9	8
RESERVED	SDMA_BUF_BOUNDARY				XFER_BLK_SIZE		
R-0h	R/W-0h				R/W-0h		
7	6	5	4	3	2	1	0
XFER_BLK_SIZE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-566. MMCSDB12_UHS2_BLOCK_SIZE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved
14-12	SDMA_BUF_BOUNDARY	R/W	0h	<p>UHS-II SDMA Buffer Boundary (SDMA only)</p> <p>When system memory is managed by paging, SDMA data transfer is performed in unit of paging. A page size of system memory management is set to this field.</p> <p>Host Controller generates the DMA Interrupt at the page boundary and requests the Host Driver to update the MMCSDB12_ADMA_SYS_ADDRESS register. SDMA waits until the MMCSDB12_ADMA_SYS_ADDRESS register is written.</p> <p>At the end of transfer, the Host Controller may issue or may not issue DMA Interrupt. In particular, DMA Interrupt shall not be issued after Transfer Complete Interrupt is issued (see MMCSDB12_NORMAL_INTR_STS[1] XFER_COMPLETE).</p> <p>These bits shall be supported when the MMCSDB12_CAPABILITIES[22] SDMA_SUPPORT bit is set to 1h and this function is active when the MMCSDB12_UHS2_XFER_MODE[0] DMA_ENA bit register is set to 1h. ADMA does not use this field.</p> <p>0h: 4K bytes (Detects A11 carry out)</p> <p>1h: 8K bytes (Detects A12 carry out)</p> <p>2h: 16K Bytes (Detects A13 carry out)</p> <p>3h: 32K Bytes (Detects A14 carry out)</p> <p>4h: 64K bytes (Detects A15 carry out)</p> <p>5h: 128K Bytes (Detects A16 carry out)</p> <p>6h: 256K Bytes (Detects A17 carry out)</p> <p>7h: 512K Bytes (Detects A18 carry out)</p>

Table 18-566. MMCSD12_UHS2_BLOCK_SIZE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	XFER_BLK_SIZE	R/W	0h	<p>UHS-II Block Size</p> <p>This bit field specifies the block size of data packet. SD Memory Card uses a fixed block size of 512 bytes.</p> <p>Variable block size may be used for SDIO. The maximum value is 2048 Bytes because CRC16 covers up to 2048 bytes. This bit field is effective when the MMCSD12_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h.</p> <p>0000h - No data transfer</p> <p>0001h - 1 Byte</p> <p>0002h - 2 Bytes</p> <p>0003h - 3 Bytes</p> <p>... ..</p> <p>01FFh - 511 Bytes</p> <p>0200h - 512 Bytes</p> <p>... ..</p> <p>0800h - 2048 Bytes</p>

18.6.45 MMCSd12_UHS2_BLOCK_COUNT Register (Offset = 84h) [reset = 0h]

MMCSd12_UHS2_BLOCK_COUNT is shown in [Figure 18-225](#) and described in [Table 18-568](#).

Return to [Summary Table](#).

This register is used to configure the number of data blocks.

Table 18-567. MMCSd12_UHS2_BLOCK_COUNT Instances

Instance	Physical Address
MMCSd1_CTL_CFG	04FB 0084h
MMCSd2_CTL_CFG	04F9 8084h

Figure 18-225. MMCSd12_UHS2_BLOCK_COUNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XFER_BLK_COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-568. MMCSd12_UHS2_BLOCK_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XFER_BLK_COUNT	R/W	0h	<p>UHS-II Block Count</p> <p>This register is effective when the MMCSd12_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h and is enabled when the MMCSd12_UHS2_XFER_MODE[1] BLK_CNT_ENA bit is set to 1h and the MMCSd12_UHS2_XFER_MODE[5] BYTE_MODE bit is set to 0h. Data transfer stops when the count reaches zero. Setting the block count to 0h results in no data blocks is transferred.</p> <p>This register should be accessed only when no transaction is executing (after transactions are stopped). During data transfer, read operations on this register may return an invalid value and write operations are ignored.</p> <p>00000000h: Stop Count</p> <p>00000001h: 1 block</p> <p>00000002h: 2 blocks</p> <p>... ..</p> <p>FFFFFFFFh: 4G blocks - 1</p>

18.6.46 MMCSD12_UHS2_COMMAND_PKT_0 to MMCSD12_UHS2_COMMAND_PKT_19 Register (Offset = 88h to 9Bh) [reset = 0h]

MMCSD12_UHS2_COMMAND_PKT_0 to MMCSD12_UHS2_COMMAND_PKT_19 is shown in [Figure 18-226](#) and described in [Table 18-571](#).

Return to [Summary Table](#).

UHS-II Command Packet image is set to this register. The maximum length is 20 bytes (see [Table 18-569](#)). The command length varies depends on a Command Packet type. The length is specified by the MMCSD12_UHS2_COMMAND register.

Table 18-569. UHS-II Command Packet Register

Offset	Preset Value Registers
088h	Command Packet Byte 0
089h	Command Packet Byte 1
08Ah	Command Packet Byte 2
....
09Bh	Command Packet Byte 19

Table 18-570. MMCSD12_UHS2_COMMAND_PKT_0 to MMCSD12_UHS2_COMMAND_PKT_19 Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0088h to 04FB 009Bh
MMCSD2_CTL_CFG	04F9 8088h to 04F9 809Bh

Figure 18-226. MMCSD12_UHS2_COMMAND_PKT_0 to MMCSD12_UHS2_COMMAND_PKT_19 Register

7	6	5	4	3	2	1	0
CMD_PKT_BYTE							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-571. MMCSD12_UHS2_COMMAND_PKT_0 to MMCSD12_UHS2_COMMAND_PKT_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CMD_PKT_BYTE	R/W	0h	Command Packet Byte UHS-II Command Packet image is set to this register. The command length varies depends on a Command Packet type.

18.6.47 MMCSDB12_UHS2_XFER_MODE Register (Offset = 9Ch) [reset = 0h]

MMCSDB12_UHS2_XFER_MODE is shown in [Figure 18-227](#) and described in [Table 18-573](#).

Return to [Summary Table](#).

This register is used to control the operations of data transfers.

On issuing a Command Packet, a Command Packet image is set to UHS-II Command Packet register (see MMCSDB12_UHS2_COMMAND_PKT_0 - MMCSDB12_UHS2_COMMAND_PKT_19) but Host Controller does not analyze the setting of UHS-II Command Packet register. Instead, Host Controller refers setting of this register to issue a Command Packet to make the control easy. Setting of these registers shall be correspondent.

**Table 18-572. MMCSDB12_UHS2_XFER_MODE
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 009Ch
MMCSDB2_CTL_CFG	04F9 809Ch

Figure 18-227. MMCSDB12_UHS2_XFER_MODE Register

15	14	13	12	11	10	9	8
DUPLEX_SELECT	EBSY_WAIT	RESERVED					RESP_INTR_DIS
R/W-0h	R/W-0h	R-0h					R/W-0h
7	6	5	4	3	2	1	0
RESP_ERR_CHK_ENA	RESP_TYPE	BYTE_MODE	DATA_XFER_DIR	RESERVED		BLK_CNT_ENA	DMA_ENA
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-573. MMCSDB12_UHS2_XFER_MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DUPLEX_SELECT	R/W	0h	Half/Full Select Use of 2 lane half duplex mode is determined by Host Driver. 0h: Full Duplex Mode 1h: 2 Lane Half Duplex Mode
14	EBSY_WAIT	R/W	0h	EBSY Wait This bit is set when issuing a command which is accompanied by EBSY packet to indicate end of command execution. Busy is expected for CCMD with R1b/R5b type and DCMD with data transfer. If this bit is set to 1h, Host Controller waits receiving of EBSY packet and on receiving EBSY packet, the MMCSDB12_NORMAL_INTR_STS[1] XFER_COMPLETE bit is set to 1h to indicate end of busy. If an error is indicated in EBSY packet (for example: Memory Error), the MMCSDB12_UHS2_ERR_INTR_STS[8] EBSY bit is set to 1h. Setting of the MMCSDB12_UHS2_ERR_INTR_STS[8] EBSY bit also sets the MMCSDB12_NORMAL_INTR_STS[15] ERROR_INTR bit to 1h. The MMCSDB12_NORMAL_INTR_STS[15] ERROR_INTR and MMCSDB12_NORMAL_INTR_STS[1] XFER_COMPLETE bits shall be set together. 0h: Issue a command without busy 1h: Wait EBSY
13-9	RESERVED	R	0h	Reserved

Table 18-573. MMCSD12_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RESP_INTR_DIS	R/W	0h	<p>Response Interrupt Disable</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.</p> <p>If Host Driver checks response error, sets this bit to 0h and waits the MMCSD12_NORMAL_INTR_STS[0] CMD_COMPLETE bit and then check the response register (MMCSD12_RESPONSE_0 - MMCSD12_RESPONSE_7). If Host Controller checks response error, sets this bit to 1h and sets the MMCSD12_UHS2_XFER_MODE[7] RESP_ERR_CHK_ENA bit to 1h. The MMCSD12_NORMAL_INTR_STS[0] CMD_COMPLETE bit is disabled by this bit regardless of MMCSD12_NORMAL_INTR_SIG_ENA[0] CMD_COMPLETE bit.</p> <p>0h: Response Interrupt is enabled 1h: Response Interrupt is disabled</p>
7	RESP_ERR_CHK_ENA	R/W	0h	<p>Response Error Check Enable</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver. Only R1 or R5 can be checked.</p> <p>If Host Driver checks response error, this bit is set to 0h and the MMCSD12_UHS2_XFER_MODE[8] RESP_INTR_DIS bit is set to 0h. If Host Controller checks response error, sets this bit to 1h and sets the MMCSD12_UHS2_XFER_MODE[8] RESP_INTR_DIS bit to 1h. Response Type R1/R5 selects either R1 or R5 response type. If an error is detected, RES Packet Error Interrupt is generated in the MMCSD12_UHS2_ERR_INTR_STS register.</p> <p>0h: Response Error Check is disabled 1h: Response Error Check is enabled</p>

Table 18-573. MMCSDB12_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESP_TYPE	R/W	0h	<p>Response Type R1/R5</p> <p>When response error check is enabled, this bit selects either R1 or R5 response types.</p> <p>Two types of response checks are supported: R1 for memory and R5 for SDIO.</p> <p>Error Statuses Checked in R1:</p> <p>Bit31 OUT_OF_RANGE</p> <p>Bit30 ADDRESS_ERROR</p> <p>Bit29 BLOCK_LEN_ERROR</p> <p>Bit26 WP_VIOLATION</p> <p>Bit25 CARD_IS_LOCKED</p> <p>Bit23 COM_CRC_ERROR</p> <p>Bit21 CARD_ECC_FAILED</p> <p>Bit20 CC_ERROR</p> <p>Bit19 ERROR</p> <p>Response Flags Checked in R5:</p> <p>Bit07 COM_CRC_ERROR</p> <p>Bit03 ERROR</p> <p>Bit01 FUNCTION_NUMBER</p> <p>Bit00 OUT_OF_RANGE</p> <p>0h: R1 (Memory)</p> <p>1h: R5 (SDIO)</p>
5	BYTE_MODE	R/W	0h	<p>Block/Byte Mode</p> <p>This bit specifies whether data transfer is in byte mode or block mode when the MMCSDB12_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. This bit is effective to a command with data transfer.</p> <p>0h: Block Mode</p> <p>1h: Byte Mode</p>
4	DATA_XFER_DIR	R/W	0h	<p>Data Transfer Direction</p> <p>This bit specifies direction of data transfer when the MMCSDB12_UHS2_COMMAND[5] DATA_PRESENT bit is set to 1h. This bit is effective to a command with data transfer.</p> <p>0h: Read (Card to Host)</p> <p>1h: Write (Host to Card)</p>
3-2	RESERVED	R	0h	Reserved
1	BLK_CNT_ENA	R/W	0h	<p>Block Count Enable</p> <p>This bit specifies whether data transfer uses the MMCSDB12_UHS2_BLOCK_COUNT register. If this bit is set to 1h, data transfer is terminated by Block Count. Setting to the MMCSDB12_UHS2_BLOCK_COUNT register shall be equivalent to TLEN in UHS-II Command Packet register (MMCSDB12_UHS2_COMMAND_PKT_0 - MMCSDB12_UHS2_COMMAND_PKT_19).</p> <p>0h: Block Count Disabled</p> <p>1h: Block Count Enabled</p>

Table 18-573. MMCSD12_UHS2_XFER_MODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMA_ENA	R/W	0h	<p>DMA Enable</p> <p>This bit selects whether DMA is used or not and is effective to a command with data transfer. One of DMA types is selected by the MMCSD12_HOST_CONTROL1[4-3] DMA_SELECT bit field.</p> <p>0h: DMA is disabled</p> <p>1h: DMA is enabled</p>

18.6.48 MMCSd12_UHS2_COMMAND Register (Offset = 9Eh) [reset = 0h]

MMCSd12_UHS2_COMMAND is shown in [Figure 18-228](#) and described in [Table 18-575](#).

Return to [Summary Table](#).

This register is used to program the Command for host controller.

Table 18-574. MMCSd12_UHS2_COMMAND Instances

Instance	Physical Address
MMCSd1_CTL_CFG	04FB 009Eh
MMCSd2_CTL_CFG	04F9 809Eh

Figure 18-228. MMCSd12_UHS2_COMMAND Register

15	14	13	12	11	10	9	8
RESERVED				PKT_LENGTH			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
CMD_TYPE		DATA_PRESENT	RESERVED		SUB_COMMAND	RESERVED	
R/W-0h		R/W-0h	R-0h		R/W-0h	R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-575. MMCSd12_UHS2_COMMAND Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12-8	PKT_LENGTH	R/W	0h	UHS-II Command Packet Length A command packet length, which is set in the UHS-II Command Packet register (MMCSd12_UHS2_COMMAND_PKT_0 - MMCSd12_UHS2_COMMAND_PKT_19), is set to this bit field. 00011b – 00000b: 3-0 Bytes (Not used) 00100b: 4 Bytes 10100b: 20 Bytes 11111b – 10101b
7-6	CMD_TYPE	R/W	0h	Command Type This field is used to distinguish a specific command like abort command. If this field is set to 0h, the UHS-II RES Packet is stored in UHS-II Response register (MMCSd12_UHS2_RESPONSE_0 - MMCSd12_UHS2_RESPONSE_19). To avoid overwriting the UHS-II Response register, when this field is set to 1h, the RES Packet (4 bytes length) of TRANS_ABORT CCMD is stored in the Response register (04FB 0010h - 04FB 0013h (04F9 8010h - 04F9 8013h)) and when this field is set to 2h, the RES Packet (8 bytes length) of memory or SDIO abort command (CMD12 or SDIO Abort command) is stored in the Response register (04FB 0018h - 04FB 001Fh (04F9 8018h - 04F9 801Fh)). When this field is set to 3h, Host Controller controls lane to go into dormant state. 0h: Normal Command 1h: TRANS_ABORT CCMD 2h: CMD12 or SDIO Abort command 3h: Go Dormant Command

Table 18-575. MMCSD12_UHS2_COMMAND Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	DATA_PRESENT	R/W	0h	Data Present This bit specifies whether the command is accompanied by data packet. 0h: No Data Present 1h: Data Present
4-3	RESERVED	R	0h	Reserved
2	SUB_COMMAND	R/W	0h	Sub Command Flag This bit is added from Version 4.10 to distinguish a main command or sub command. When issuing a main command, this bit is set to 0h and when issuing a sub command, this bit is set to 1h. Setting of this bit is checked by the MMCSD12_PRESENTSTATE[28] SUB_COMMAND_STS bit. 0h: Sub Command 1h: Main Command
1-0	RESERVED	R	0h	Reserved

18.6.49 MMCSDB12_UHS2_RESPONSE_0 to MMCSDB12_UHS2_RESPONSE_19 Register (Offset = A0h to B3h) [reset = 0h]

MMCSDB12_UHS2_RESPONSE_0 to MMCSDB12_UHS2_RESPONSE_19 is shown in [Figure 18-229](#) and described in [Table 18-577](#).

Return to [Summary Table](#).

This register is used to store received UHS-II RES Packet image.

Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command, which is specified by setting 1h or 2h to the MMCSDB12_UHS2_COMMAND[7-6] CMD_TYPE bit field. The maximum response length is 20 bytes.

Table 18-576. MMCSDB12_UHS2_RESPONSE_0 to UHS2_RESPONSE_19 Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00A0h to 04FB 00B3h
MMCSDB2_CTL_CFG	04F9 80A0h to 04F9 80B3h

Figure 18-229. MMCSDB12_UHS2_RESPONSE_0 to MMCSDB12_UHS2_RESPONSE_19 Register

7	6	5	4	3	2	1	0
RESP_PKT_BYTE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-577. MMCSDB12_UHS2_RESPONSE_0 to UHS2_RESPONSE_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESP_PKT_BYTE	R	0h	Response Packet Byte Host Controller saves received UHS-II RES Packet image to this register except the response of an abort command.

[Table 18-578](#) shows UHS-II Response Register offsets.

Table 18-578. UHS-II Response Register

Offset	Preset Value Registers
04FB 0A0h / 04F9 8A0h	Response Packet Byte 0
04FB 0A1h / 04F9 8A1h	Response Packet Byte 1
04FB 0A2h / 04F9 8A2h	Response Packet Byte 2
....
04FB 0B3h / 04F9 8B3h	Response Packet Byte 19

18.6.50 MMCSD12_UHS2_MESSAGE_SELECT Register (Offset = B4h) [reset = 0h]

MMCSD12_UHS2_MESSAGE_SELECT is shown in [Figure 18-230](#) and described in [Table 18-580](#).

Return to [Summary Table](#).

This register is used to access internal buffer.

Table 18-579. MMCSD12_UHS2_MESSAGE_SELECT Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00B4h
MMCSD2_CTL_CFG	04F9 80B4h

Figure 18-230. MMCSD12_UHS2_MESSAGE_SELECT Register

7	6	5	4	3	2	1	0
RESERVED						MSG_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-580. MMCSD12_UHS2_MESSAGE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	MSG_SEL	R/W	0h	UHS-II MSG Select Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs can be read from the MMCSD12_UHS2_MESSAGE register (04FB 00BBh - 04FB 00B8h (04F9 80BBh - 04F9 80B8h) by setting this register (assumed for debug usage). 0h: The latest MSG 1h: One MSG before 2h: Two MSGs before 3h: Three MSGs before

18.6.51 MMCSDB12_UHS2_MESSAGE Register (Offset = B8h) [reset = 0h]

MMCSDB12_UHS2_MESSAGE is shown in [Figure 18-231](#) and described in [Table 18-582](#).

Return to [Summary Table](#).

This register is used to access internal buffer.

Table 18-581. MMCSDB12_UHS2_MESSAGE Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00B8h
MMCSDB2_CTL_CFG	04F9 80B8h

Figure 18-231. MMCSDB12_UHS2_MESSAGE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSG_BYTE3								MSG_BYTE2							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSG_BYTE1								MSG_BYTE0							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-582. MMCSDB12_UHS2_MESSAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MSG_BYTE3	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSDB12_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSDB12_UHS2_MESSAGE Register.
23-16	MSG_BYTE2	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSDB12_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSDB12_UHS2_MESSAGE Register.
15-8	MSG_BYTE1	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSDB12_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSDB12_UHS2_MESSAGE Register.
7-0	MSG_BYTE0	R	0h	UHS II MSG Host Controller holds 4 MSG packets in FIFO buffer. One of 4 MSGs (length is 4 bytes) can be read from this register by setting the MMCSDB12_UHS2_MESSAGE_SELECT register. Usually 2 duplicate MSG packets are sent from/to UHS-II card. One of these 2 MSG packets which Host Controller recognizes as valid one is stored in the MMCSDB12_UHS2_MESSAGE Register.

18.6.52 MMCSD12_UHS2_DEVICE_INTR_STATUS Register (Offset = BCh) [reset = 0h]

MMCSD12_UHS2_DEVICE_INTR_STATUS is shown in [Figure 18-232](#) and described in [Table 18-584](#).

Return to [Summary Table](#).

This register shows receipt of INT MSG from which device.

Table 18-583.
MMCSD12_UHS2_DEVICE_INTR_STATUS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00BCh
MMCSD2_CTL_CFG	04F9 80BCh

Figure 18-232. MMCSD12_UHS2_DEVICE_INTR_STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_INT_STS															
R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-584. MMCSD12_UHS2_DEVICE_INTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEV_INT_STS	R/W1C	0h	<p>UHS-II Device Interrupt Status</p> <p>This register shows receipt of INT MSG from which device and is effective when the MMCSD12_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. On receiving INT MSG from a device, Host Controller saves the INT MSG to MMCSD12_UHS2_DEVICE_INT_CODE register. A bit of this register, which is correspondent to Device ID, is set to 1h and generate Card Interrupt in Normal Interrupt Status register (see MMCSD12_NORMAL_INTR_STS[8] CARD_INTR).</p> <p>Writing a bit to 1h clears the status bit (interrupt is treated) and writing a bit to 0h keeps the status value (interrupt is untreated). If the MMCSD12_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 0h, this register is cleared to 0h and Host Controller ignores receipt of INT MSG.</p> <p>Effective bit range of this register is determined by the MMCSD12_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. If N devices are supported, bits 1 to N are effective. Then Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization. A bit of unsupported Device ID in this register shall be indicated to 0h.</p> <p>D00 - Not used (Reserved)</p> <p>D01 - Setting 1h means INT MSG is received from Device ID 1</p> <p>D02 - Setting 1h means INT MSG is received from Device ID 2</p> <p>.... ..</p> <p>D15 - Setting 1h means INT MSG is received from Device ID 15</p>

18.6.53 MMCS12_UHS2_DEVICE_SELECT Register (Offset = BEh) [reset = 0h]

MMCS12_UHS2_DEVICE_SELECT is shown in [Figure 18-233](#) and described in [Table 18-586](#).

Return to [Summary Table](#).

UHS-II Device Select Register.

Table 18-585. MMCS12_UHS2_DEVICE_SELECT Instances

Instance	Physical Address
MMCS1_CTL_CFG	04FB 00BEh
MMCS2_CTL_CFG	04F9 80BEh

Figure 18-233. MMCS12_UHS2_DEVICE_SELECT Register

7	6	5	4	3	2	1	0
INT_MSG_ENA	RESERVED			DEV_SEL			
R/W-0h	R-0h			R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-586. MMCS12_UHS2_DEVICE_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MSG_ENA	R/W	0h	<p>INT MSG Enable (Optional)</p> <p>This bit enables receipt of INT MSG. If this bit is set to 1h, receipt of INT MSG is informed by the MMCS12_NORMAL_INTR_STS[8] CARD_INTR bit. If this bit is set to 0h, Host Controller ignores receipt of INT MSG and may not set the MMCS12_UHS2_DEVICE_INT_CODE register.</p> <p>Support of INT MSG Interrupt is optional. If trying to set this bit to 1h but still this bit is read 0, INT MSG Interrupt is not supported by the Host Controller. In this case, the MMCS12_UHS2_DEVICE_INTR_STATUS register always shall be read 0 and the MMCS12_UHS2_DEVICE_INT_CODE register may not be implemented.</p> <p>0h: Disabled 1h: Enabled</p>
6-4	RESERVED	R	0h	Reserved
3-0	DEV_SEL	R/W	0h	<p>UHS-II Device Select</p> <p>Host Controller holds an INT MSG packet per device. One of INT MSGs (up to 15) can be selected by this field and read from the MMCS12_UHS2_DEVICE_INT_CODE. This field is effective when the MMCS12_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h.</p> <p>The number of devices implemented in the Host Controller is indicated by the MMCS12_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field.</p> <p>0h: Unselected (Default) 1h: INT MSG of Device ID 1 is selected 2h: INT MSG of Device ID 2 is selected Fh: INT MSG of Device ID 15 is selected</p>

18.6.54 MMCSD12_UHS2_DEVICE_INT_CODE Register (Offset = BFh) [reset = 0h]

MMCSD12_UHS2_DEVICE_INT_CODE is shown in [Figure 18-234](#) and described in [Table 18-588](#).

Return to [Summary Table](#).

This register is effective when the MMCSD12_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h.

Table 18-587. MMCSD12_UHS2_DEVICE_INT_CODE Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00BFh
MMCSD2_CTL_CFG	04F9 80BFh

Figure 18-234. MMCSD12_UHS2_DEVICE_INT_CODE Register

7	6	5	4	3	2	1	0
DEV_INTR							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-588. MMCSD12_UHS2_DEVICE_INT_CODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEV_INTR	R	0h	<p>UHS II Device Interrupt</p> <p>This register is effective when the MMCSD12_UHS2_DEVICE_SELECT[7] INT_MSG_ENA bit is set to 1h. Host Controller holds an INT MSG packet per device. One of INT MSGs (Code length is 1 byte) up to 15 can be read from this register by selecting UHS-II Device Select (MMCSD12_UHS2_DEVICE_SELECT[3-0] DEV_SEL).</p> <p>The number of the registers to hold INT MSGs is determined by the MMCSD12_UHS2_GEN_CAP[21-18] CORECFG_UHS2_MAX_DEVICES bit field. Device ID is supposed to be assigned from 1 sequentially at the UHS-II Initialization.</p>

18.6.55 MMCSDB12_UHS2_SOFTWARE_RESET Register (Offset = C0h) [reset = 0h]

MMCSDB12_UHS2_SOFTWARE_RESET is shown in [Figure 18-235](#) and described in [Table 18-590](#).

Return to [Summary Table](#).

UHS-II Software Reset Register.

Table 18-589. MMCSDB12_UHS2_SOFTWARE_RESET Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00C0h
MMCSDB2_CTL_CFG	04F9 80C0h

Figure 18-235. MMCSDB12_UHS2_SOFTWARE_RESET Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						HOST_SDTRAN_RESET	HOST_FULL_RESET
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-590. MMCSDB12_UHS2_SOFTWARE_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0h	Reserved
1	HOST_SDTRAN_RESET	R/W	0h	<p>Host SD-TRAN Reset</p> <p>Host Driver set this bit to 1h to reset SD-TRAN layer when CMD0 is issued to Device or data transfer error occurs. This bit is cleared automatically at completion of SD-TRAN reset. If CMD0 is issued, SD-TRAN Initialization sequence from CMD8 is required to use UHS-II mode. Assuming that bus power is maintained and CM-TRAN Initialization is not required.</p> <p>Host Controller requires to do followings:</p> <ol style="list-style-type: none"> (1) SD Clock Enable is maintained (continue to provide RCLK). (2) All setting register is maintained. (3) Internal sequencers are reset to just after power on be able to issue a command. (4) All Interrupt Status, Status Enable and Signal Enable are cleared. (5) Data transfer is terminated and data in buffer is discarded. <p>0h: Not Affected 1h: Reset SD-TRAN</p>

Table 18-590. MMCSD12_UHS2_SOFTWARE_RESET Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HOST_FULL_RESET	R/W	0h	<p>Host Full Reset</p> <p>On issuing FULL_RESET CCMD, Host Driver set this bit to 1h to reset Host Controller. This bit is cleared automatically at completion of Host Controller reset. Initialization sequence from PHY Initialization is required to use UHS-II mode. Assuming that bus power is maintained.</p> <p>Host Controller requires to do followings:</p> <ul style="list-style-type: none"> (1) SD Clock Enable is cleared (internal Clock is still synchronized). (2) All setting register is cleared. (3) Internal sequencers are reset to just after power on. (4) All Interrupt Status, Status Enable and Signal Enable are cleared. <p>0h: Not Affected 1h: Reset Host Controller</p>

18.6.56 MMCSDB12_UHS2_TIMER_CONTROL Register (Offset = C2h) [reset = 0h]

MMCSDB12_UHS2_TIMER_CONTROL is shown in [Figure 18-236](#) and described in [Table 18-592](#).

Return to [Summary Table](#).

UHS-II Timeout Control Register.

Table 18-591. MMCSDB12_UHS2_TIMER_CONTROL Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00C2h
MMCSDB2_CTL_CFG	04F9 80C2h

Figure 18-236. MMCSDB12_UHS2_TIMER_CONTROL Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DEADLOCK_TIMEOUT_CTR				CMDRESP_TIMEOUT_CTR			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-592. MMCSDB12_UHS2_TIMER_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-4	DEADLOCK_TIMEOUT_CTR	R/W	0h	Timeout Counter Value for Deadlock This value determines the deadlock period while host expecting to receive a packet (1 second). Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for Deadlock (in the MMCSDB12_UHS2_ERR_INTR_STS_ENA register). Fh: Reserved Eh: TMCLK x 2 ²⁷ 1h: TMCLK x 2 ¹⁴ 0h: TMCLK x 2 ¹³
3-0	CMDRESP_TIMEOUT_CTR	R/W	0h	Timeout Counter Value for CMD_RES This value determines the interval between command packet and response packet (5 ms). Timeout clock frequency will be generated by dividing the base clock TMCLK value by this value. When setting this register, prevent inadvertent timeout events by clearing the Timeout for CMD_RES (in the MMCSDB12_UHS2_ERR_INTR_STS_ENA register). Fh: Reserved Eh: TMCLK x 2 ²⁷ 1h: TMCLK x 2 ¹⁴ 0h: TMCLK x 2 ¹³

18.6.57 MMCSD12_UHS2_ERR_INTR_STS Register (Offset = C4h) [reset = 0h]

MMCSD12_UHS2_ERR_INTR_STS is shown in [Figure 18-237](#) and described in [Table 18-594](#).

Return to [Summary Table](#).

This register gives the status of all UHS-II interrupts.

**Table 18-593. MMCSD12_UHS2_ERR_INTR_STS
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00C4h
MMCSD2_CTL_CFG	04F9 80C4h

Figure 18-237. MMCSD12_UHS2_ERR_INTR_STS Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC_ERR					RESERVED		
R/W1C-0h					R-0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W1C-0h	R-0h						R/W1C-0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED	RESP_PKT	HEADER
R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-594. MMCSD12_UHS2_ERR_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC_ERR	R/W1C	0h	Vendor Specific Error Vendor may use this field for vendor specific error status. 0h: Interrupt is not generated 1h: Vendor Specific Error
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W1C	0h	Timeout for Deadlock Setting of this bit means that deadlock timeout occurs. Host expects to receive a packet but not received in a specified timeout (1 second). Timeout value is determined by the setting of the MMCSD12_UHS2_TIMER_CONTROL[7-4] DEADLOCK_TIMEOUT_CTR bit field. 0h: Interrupt is not generated 1h: Deadlock Error

Table 18-594. MMCSDB12_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	CMD_RESP_TIMEOUT	R/W1C	0h	Timeout for CMD_RES Setting of this bit means that RES Packet timeout occurs. Host expects to receive RES packet but not received in a specified timeout (5 ms). Timeout value is determined by the setting of the MMCSDB12_UHS2_TIMER_CONTROL[3-0] CMDRESP_TIMEOUT_CTR bit field. 0h: Interrupt is not generated 1h: RES Packet Timeout Error
15	ADMA2_ADMA3	R/W1C	0h	ADMA2/3 Error Setting of this bit means that ADMA2/3 Error occurs in UHS-II mode. ADMA2/3 Error Status is indicated to the MMCSDB12_ADMA_ERR_STATUS register, which is defined in the Host spec 3.00. 0h: Interrupt is not generated 1h: ADMA2/3 Error
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W1C	0h	EBSY Error On receiving EBSY packet, if the packet indicates an error, this bit is set to 1h. Setting of this bit also sets Error Interrupt and Transfer Completer together in the MMCSDB12_NORMAL_INTR_STS register. This error check is effective for a command with setting the MMCSDB12_UHS2_XFER_MODE[14] EBSY_WAIT bit. 0h: Interrupt is not generated 1h: EBSY Error (Backend Error)
7	UNRECOVERABLE	R/W1C	0h	Unrecoverable Error Setting of this bit means that Unrecoverable Error is set in a packet from a device. 0h: Interrupt is not generated 1h: Device Unrecoverable Error
6	RESERVED	R	0h	Reserved
5	TID	R/W1C	0h	TID Error Setting of this bit means that TID Error occurs. 0h: Interrupt is not generated 1h: TID Error
4	FRAMING	R/W1C	0h	Framing Error Setting of this bit means that Framing Error occurs during a packet receiving. 0h: Interrupt is not generated 1h: Framing Error
3	CRC	R/W1C	0h	CRC Error Setting of this bit means that CRC Error occurs during a packet receiving. 0h: Interrupt is not generated 1h: CRC Error
2	RETRY_EXPIRED	R/W1C	0h	Retry Expired Setting of this bit means that Retry Counter Expired Error occurs during data transfer. If this bit is set, either Framing Error or CRC Error in this register shall be set. 0h: Interrupt is not generated 1h: Retry Expired Error

Table 18-594. MMCSD12_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESP_PKT	R/W1C	0h	<p>RES Packet Error</p> <p>Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If the MMCSD12_UHS2_XFER_MODE[7] RESP_ERR_CHK_ENA bit is set to 1h, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1h.</p> <p>0h: Interrupt is not generated 1h: RES Packet Error</p>
0	HEADER	R/W1C	0h	<p>Header Error</p> <p>Setting of this bit means that Header Error occurs in a received packet.</p> <p>0h: Interrupt is not generated 1h: Header Error</p>

18.6.58 MMCSDB12_UHS2_ERR_INTR_STS_ENA Register (Offset = C8h) [reset = 0h]

MMCSDB12_UHS2_ERR_INTR_STS_ENA is shown in [Figure 18-238](#) and described in [Table 18-596](#).

Return to [Summary Table](#).

This register is used to enable the MMCSDB12_UHS2_ERR_INTR_STS register fields.

Table 18-595.
MMCSDB12_UHS2_ERR_INTR_STS_ENA Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00C8h
MMCSDB2_CTL_CFG	04F9 80C8h

Figure 18-238. MMCSDB12_UHS2_ERR_INTR_STS_ENA Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC					RESERVED		
R/W-0h					R-0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TI MEOUT	CMD_RESP_TI MEOUT
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ADMA2_ADMA 3	RESERVED						EBSY
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
UNRECOVERA BLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIR ED	RESP_PKT	HEADER
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-596. MMCSDB12_UHS2_ERR_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Setting this bit to 1h enables setting of Vendor Specific Error bit in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Timeout for Deadlock Setting this bit to 1h enables setting of Timeout for Dead lock bit in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
16	CMD_RESP_TIMEOUT	R/W	0h	Timeout for CMD_RES Setting this bit to 1h enables setting of Timeout for CMD_RES bit in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

Table 18-596. MMCSD12_UHS2_ERR_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W	0h	ADMA2/3 Error Setting this bit to 1h enables setting of ADMA2/3 Error bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W	0h	EBSY Error Setting this bit to 1h enables setting of EBSY Error bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
7	UNRECOVERABLE	R/W	0h	Unrecoverable Error Setting this bit to 1h enables setting of Unrecoverable Error bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
6	RESERVED	R	0h	Reserved
5	TID	R/W	0h	TID Error Setting this bit to 1h enables setting of TID Error bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
4	FRAMING	R/W	0h	Framing Error Setting this bit to 1h enables setting of Framing Error bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
3	CRC	R/W	0h	CRC Error Setting this bit to 1h enables setting of CRC Error bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
2	RETRY_EXPIRED	R/W	0h	Retry Expired Setting this bit to 1h enables setting of Retry Expired bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
1	RESP_PKT	R/W	0h	RES Packet Error Setting this bit to 1h enables setting of RES Packet Error bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled
0	HEADER	R/W	0h	Header Error Setting this bit to 1h enables setting of Header Error bit in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Status is Disabled 1h: Status is Enabled

18.6.59 MMCSDB12_UHS2_ERR_INTR_SIG_ENA Register (Offset = CCh) [reset = 0h]

MMCSDB12_UHS2_ERR_INTR_SIG_ENA is shown in [Figure 18-239](#) and described in [Table 18-598](#).

Return to [Summary Table](#).

This register is used to generate UHS-II Interrupt signals.

Table 18-597.
MMCSDB12_UHS2_ERR_INTR_SIG_ENA Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00CCh
MMCSDB2_CTL_CFG	04F9 80CCh

Figure 18-239. MMCSDB12_UHS2_ERR_INTR_SIG_ENA Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC					RESERVED		
R/W-0h					R-0h		
23	22	21	20	19	18	17	16
RESERVED						DEADLOCK_TIMEOUT	CMD_RESP_TIMEOUT
R-0h						R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
ADMA2_ADMA3	RESERVED						EBSY
R/W-0h	R-0h						R/W-0h
7	6	5	4	3	2	1	0
UNRECOVERABLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIRED_SIG_ENA	RESP_PKT	HEADER
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-598. MMCSDB12_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC	R/W	0h	Vendor Specific Error Setting of a bit to 1h in this field enables generating interrupt signal when correspondent bit of Vendor Specific Error is set in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
26-18	RESERVED	R	0h	Reserved
17	DEADLOCK_TIMEOUT	R/W	0h	Timeout for Deadlock Setting this bit to 1h enables generating interrupt signal when Timeout for Dead lock bit is set in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
16	CMD_RESP_TIMEOUT	R/W	0h	Timeout for CMD_RES Setting this bit to 1h enables generating interrupt signal when Timeout for CMD_RES bit is set in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

Table 18-598. MMCSD12_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	ADMA2_ADMA3	R/W	0h	ADMA2/3 Error Setting this bit to 1h enables generating interrupt signal when ADMA2/3 Error bit is set in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
14-9	RESERVED	R	0h	Reserved
8	EBSY	R/W	0h	EBSY Error Setting this bit to 1h enables generating interrupt signal when EBSY Error bit is set in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
7	UNRECOVERABLE	R/W	0h	Unrecoverable Error Setting this bit to 1h enables generating interrupt signal when Unrecoverable Error bit is set in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
6	RESERVED	R	0h	Reserved
5	TID	R/W	0h	TID Error Setting this bit to 1h enables generating interrupt signal when TID Error bit is set in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
4	FRAMING	R/W	0h	Framing Error Setting this bit to 1h enables generating interrupt signal when Framing Error bit is set in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
3	CRC	R/W	0h	CRC Error Setting this bit to 1h enables generating interrupt signal when CRC Error bit is set in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
2	RETRY_EXPIRED_SIG_ENA	R/W	0h	Retry Expired Setting this bit to 1h enables generating interrupt signal when Retry Expired bit is set in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled
1	RESP_PKT	R/W	0h	RES Packet Error Setting this bit to 1h enables generating interrupt signal when RES Packet Error bit is set in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

Table 18-598. MMCSDB12_UHS2_ERR_INTR_SIG_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HEADER	R/W	0h	Header Error Setting this bit to 1h enables generating interrupt signal when Header Error bit is set in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Interrupt Signal is Disabled 1h: Interrupt Signal is Enabled

18.6.60 MMCSD12_UHS2_SETTINGS_PTR Register (Offset = E0h) [reset = 100h]

MMCSD12_UHS2_SETTINGS_PTR is shown in [Figure 18-240](#) and described in [Table 18-600](#).

Return to [Summary Table](#).

This register is pointer for UHS-II settings.

**Table 18-599. MMCSD12_UHS2_SETTINGS_PTR
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00E0h
MMCSD2_CTL_CFG	04F9 80E0h

Figure 18-240. MMCSD12_UHS2_SETTINGS_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_SETTINGS_PTR															
R-100h															

LEGEND: R = Read Only; -n = value after reset

Table 18-600. MMCSD12_UHS2_SETTINGS_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_SETTINGS_PTR	R	100h	Pointer for UHS-II Settings Register

18.6.61 MMCSDB12_UHS2_CAPABILITIES_PTR Register (Offset = E2h) [reset = 110h]

MMCSDB12_UHS2_CAPABILITIES_PTR is shown in [Figure 18-241](#) and described in [Table 18-602](#).

Return to [Summary Table](#).

This register is pointer for UHS-II Capabilities Register.

Table 18-601. MMCSDB12_UHS2_CAPABILITIES_PTR Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00E2h
MMCSDB2_CTL_CFG	04F9 80E2h

Figure 18-241. MMCSDB12_UHS2_CAPABILITIES_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_CAPABILITIES_PTR															
R-110h															

LEGEND: R = Read Only; -n = value after reset

Table 18-602. MMCSDB12_UHS2_CAPABILITIES_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_CAPABILITIES_PTR	R	110h	Pointer for UHS-II Capabilities Register

18.6.62 MMCSD12_UHS2_TEST_PTR Register (Offset = E4h) [reset = 120h]

MMCSD12_UHS2_TEST_PTR is shown in [Figure 18-242](#) and described in [Table 18-604](#).

Return to [Summary Table](#).

This register is pointer for UHS-II Test Register.

**Table 18-603. MMCSD12_UHS2_TEST_PTR
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00E4h
MMCSD2_CTL_CFG	04F9 80E2h

Figure 18-242. MMCSD12_UHS2_TEST_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UHS2_TEST_PTR															
R-120h															

LEGEND: R = Read Only; -n = value after reset

Table 18-604. MMCSD12_UHS2_TEST_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	UHS2_TEST_PTR	R	120h	Pointer for UHS-II Test Register

18.6.63 MMCSDB12_SHARED_BUS_CTRL_PTR Register (Offset = E6h) [reset = 130h]

MMCSDB12_SHARED_BUS_CTRL_PTR is shown in [Figure 18-243](#) and described in [Table 18-606](#).

Return to [Summary Table](#).

This register is pointer for UHS-II Shared Bus Control Register.

Table 18-605. MMCSDB12_SHARED_BUS_CTRL_PTR Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00E6h
MMCSDB2_CTL_CFG	04F9 80E6h

Figure 18-243. MMCSDB12_SHARED_BUS_CTRL_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHARED_BUS_CTRL_PTR															
R-130h															

LEGEND: R = Read Only; -n = value after reset

Table 18-606. MMCSDB12_SHARED_BUS_CTRL_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SHARED_BUS_CTRL_PT R	R	130h	Pointer for Shared Bus Control Register

18.6.64 MMCSDB12_VENDOR_SPECFIC_PTR Register (Offset = E8h) [reset = 140h]

MMCSDB12_VENDOR_SPECFIC_PTR is shown in [Figure 18-244](#) and described in [Table 18-608](#).

Return to [Summary Table](#).

This register is pointer for UHS-II Vendor Specific Register.

**Table 18-607. MMCSDB12_VENDOR_SPECFIC_PTR
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00E8h
MMCSDB2_CTL_CFG	04F9 80E8h

Figure 18-244. MMCSDB12_VENDOR_SPECFIC_PTR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VENDOR_SPECFIC_PTR															
R-140h															

LEGEND: R = Read Only; -n = value after reset

Table 18-608. MMCSDB12_VENDOR_SPECFIC_PTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_SPECFIC_PTR	R	140h	Pointer for Vendor Specific Area

18.6.65 MMCSDB12_BOOT_TIMEOUT_CONTROL Register (Offset = F4h) [reset = 0h]

MMCSDB12_BOOT_TIMEOUT_CONTROL is shown in [Figure 18-245](#) and described in [Table 18-610](#).

Return to [Summary Table](#).

This is used to program the boot timeout value counter.

Table 18-609.
MMCSDB12_BOOT_TIMEOUT_CONTROL Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00F4h
MMCSDB2_CTL_CFG	04F9 80F4h

Figure 18-245. MMCSDB12_BOOT_TIMEOUT_CONTROL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_TIMEOUT_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-610. MMCSDB12_BOOT_TIMEOUT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_TIMEOUT_CNT	R/W	0h	Boot Data Timeout Counter Value This value determines the interval by which DAT line timeouts are detected during boot operation for eMMC4.4 card. The value is in number of SD clock.

18.6.66 MMCSD12_VENDOR_REGISTER Register (Offset = F8h) [reset = 4E20h]

MMCSD12_VENDOR_REGISTER is shown in [Figure 18-246](#) and described in [Table 18-612](#).

Return to [Summary Table](#).

Vendor register added for Auto Gate SD CLK, CMD11 Power Down Timer, Enhanced Strobe and eMMC Hardware Reset.

**Table 18-611. MMCSD12_VENDOR_REGISTER
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00F8h
MMCSD2_CTL_CFG	04F9 80F8h

Figure 18-246. MMCSD12_VENDOR_REGISTER Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							AUTOGATE_S DCLK
R-0h							R/W-0h
15	14	13	12	11	10	9	8
CMD11_PD_TIMER							
R/W-1388h							
7	6	5	4	3	2	1	0
CMD11_PD_TIMER						EMMC_HW_RE SET	ENHANCED_S TROBE
R/W-1388h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-612. MMCSD12_VENDOR_REGISTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	AUTOGATE_SDCLK	R/W	0h	Auto Gate SD CLK If this bit is set, SD CLK will be gated automatically when there is no transfer. This is applicable only for Embedded Device. 0h: Disable 1h: Enable
15-2	CMD11_PD_TIMER	R/W	1388h	CMD11 Power Down Timer Value
1	EMMC_HW_RESET	R/W	0h	eMMC Hardware Reset Hardware reset signal is generated for eMMC card when this bit is set. 0h: De-assert hardware reset pin 1h: Drives the hardware reset pin as ZERO (Active LOW to eMMC card)
0	ENHANCED_STROBE	R/W	0h	Enhanced Strobe This bit enables the enhanced strobe logic of the Host Controller.

18.6.67 MMCSDB12_SLOT_INT_STS Register (Offset = FCh) [reset = 0h]

MMCSDB12_SLOT_INT_STS is shown in [Figure 18-247](#) and described in [Table 18-614](#).

Return to [Summary Table](#).

This register is used to read the interrupt signal for each slot.

Table 18-613. MMCSDB12_SLOT_INT_STS Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 00FCh
MMCSDB2_CTL_CFG	04F9 80FCh

Figure 18-247. MMCSDB12_SLOT_INT_STS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
INTR_SIG							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-614. MMCSDB12_SLOT_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7-0	INTR_SIG	R	0h	Interrupt Signal for Slot#0 These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

18.6.68 MMCSD12_HOST_CONTROLLER_VER Register (Offset = FEh) [reset = 1004h]

MMCSD12_HOST_CONTROLLER_VER is shown in [Figure 18-248](#) and described in [Table 18-616](#).

Return to [Summary Table](#).

This register is used to read the vendor version number and specification version number.

Table 18-615. MMCSD12_HOST_CONTROLLER_VER Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 00FEh
MMCSD2_CTL_CFG	04F9 80FEh

Figure 18-248. MMCSD12_HOST_CONTROLLER_VER Register

15	14	13	12	11	10	9	8
VEN_VER_NUM							
R-10h							
7	6	5	4	3	2	1	0
SPEC_VER_NUM							
R-4h							

LEGEND: R = Read Only; -n = value after reset

Table 18-616. MMCSD12_HOST_CONTROLLER_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	VEN_VER_NUM	R	10h	Vendor Version Number The Vendor Version Number is set to 10h (1.0)
7-0	SPEC_VER_NUM	R	4h	Specification Version Number This status indicates the Host Controller Specification Version. The upper and lower 4-bits indicate the version. 0h: SD Host Controller Specification Version 1.00 1h: SD Host Controller Specification Version 2.00 Including the feature of the ADMA and Test Register 2h: SD Host Controller Specification Version 3.00 3h: SD Host Controller Specification Version 4.00 4h: SD Host Controller Specification Version 4.10 Others: Reserved

18.6.69 MMCSDB12_UHS2_GEN_SETTINGS Register (Offset = 100h) [reset = 0h]

MMCSDB12_UHS2_GEN_SETTINGS is shown in [Figure 18-249](#) and described in [Table 18-618](#).

Return to [Summary Table](#).

Start Address of General settings is pointed by the MMCSDB12_UHS2_SETTINGS_PTR Register.

**Table 18-617. MMCSDB12_UHS2_GEN_SETTINGS
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0100h
MMCSDB2_CTL_CFG	04F9 8100h

Figure 18-249. MMCSDB12_UHS2_GEN_SETTINGS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		NUMLANES					
R-0h		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED							POWER_MODE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-618. MMCSDB12_UHS2_GEN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	NUMLANES	R/W	0h	Number of Lanes and Functionalities The lane configuration of a Host System is set to this field depends on the capability among Host Controller and connected devices. 2 Lanes FD mode is mandatory and the others modes are optional. 0h: 2 Lanes FD or 2L-HD 1h: Not Used 2h: 3 Lanes 2D1U-FD (Embedded) 3h: 3 Lanes 1D2U-FD (Embedded) 4h: 4 Lanes 2D2U-FD (Embedded) Others: Reserved
7-1	RESERVED	R	0h	Reserved
0	POWER_MODE	R/W	0h	Power Mode This field determines either Fast mode or Low Power mode. Host and all devices connected to the host shall be set to the same mode. 0h: Fast Mode 1h: Low Power Mode

18.6.70 MMCSd12_UHS2_PHY_SETTINGS Register (Offset = 104h) [reset = 0h]

MMCSd12_UHS2_PHY_SETTINGS is shown in [Figure 18-250](#) and described in [Table 18-620](#).

Return to [Summary Table](#).

Start Address of PHY settings is pointed by the MMCSd12_UHS2_SETTINGS_PTR Register.

**Table 18-619. MMCSd12_UHS2_PHY_SETTINGS
Instances**

Instance	Physical Address
MMCSd1_CTL_CFG	04FB 0104h
MMCSd2_CTL_CFG	04F9 8104h

Figure 18-250. MMCSd12_UHS2_PHY_SETTINGS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
N_LSS_DIR				N_LSS_SYN			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
HIBERNATE_E NA	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
SPEED_RANGE		RESERVED					
R/W-0h		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-620. MMCSd12_UHS2_PHY_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	N_LSS_DIR	R/W	0h	Host N_LSS_DIR The largest value of N_LSS_DIR capabilities among the Host Controller and Connected Devices is set to this field. 0h: 8 x 16 LSS 1h: 8 x 1 LSS 2h: 8 x 2 LSS 3h: 8 x 3 LSS Fh: 8 x 15 LSS
19-16	N_LSS_SYN	R/W	0h	Host N_LSS_SYN The largest value of N_LSS_SYN capabilities among the Host Controller and Connected Devices is set to this field. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h - 4 x 3 LSS Fh: 4 x 15 LSS

Table 18-620. MMCSDB12_UHS2_PHY_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	HIBERNATE_ENA	R/W	0h	<p>Hibernate Enable</p> <p>After checking card capability of Hibernate mode, if all devices support Hibernate mode, this bit may be set. This bit determines whether Host remains in Dormant state or goes to Hibernate state. In Hibernate mode, VDD1 Power may be off.</p> <p>0h: Hibernate Disabled 1h: Hibernate Enabled</p>
14-8	RESERVED	R	0h	Reserved
7-6	SPEED_RANGE	R/W	0h	<p>Speed Range</p> <p>PLL multiplier is selected by this field. Change of PLL Multiplier is not effective immediately and is applied from exiting Dormant State.</p> <p>0h: Range A (Default) 1h: Range B 2h: Reserved 3h: Reserved</p>
5-0	RESERVED	R	0h	Reserved

18.6.71 MMCSDB12_UHS2_LNK_TRN_SETTINGS Register (Offset = 108h) [reset = 0h]

MMCSDB12_UHS2_LNK_TRN_SETTINGS is shown in [Figure 18-251](#) and described in [Table 18-622](#).

Return to [Summary Table](#).

Start Address of LINK/TRAN settings is pointed by the MMCSDB12_UHS2_SETTINGS_PTR Register.

Table 18-621.
MMCSDB12_UHS2_LNK_TRN_SETTINGS Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0108h
MMCSDB2_CTL_CFG	04F9 8108h

Figure 18-251. MMCSDB12_UHS2_LNK_TRN_SETTINGS Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
N_DATA_GAP							
R/W-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						RETRY_COUNT	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
HOST_NFCU							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-622. MMCSDB12_UHS2_LNK_TRN_SETTINGS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved

Table 18-622. MMCS D12_UHS2_LNK_TRN_SETTINGS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
39-32	N_DATA_GAP	R/W	0h	Host N_DATA_GAP The largest value of N_DATA_GAP capabilities among the Host Controller and Connected Devices is set to this field. 00h: No Gap 01h: 1 LSS 02h: 2 LSS 03h: 3 LSS FFh: 255 LSS
31-18	RESERVED	R	0h	Reserved
17-16	RETRY_COUNT	R/W	0h	Retry Count Data Burst retry count is set to this field. 00h: Retry Disabled 01h: 1 time 02h: 2 times 03h: 3 times
15-8	HOST_NFCU	R/W	0h	Host N_FCU Host Driver sets the number of blocks in Data Burst (Flow Control) to this field. The value shall be smaller than or equal to N_FCU capabilities among the Host Controller and connected card and devices. Setting 1 to 4 blocks is recommended considering buffer size. 00h: 256 Blocks 01h: 1 Block 02h: 2 Blocks 03h: 3 Blocks FFh: 255 Blocks
7-0	RESERVED	R	0h	Reserved

18.6.72 MMCSD12_UHS2_GEN_CAP Register (Offset = 110h) [reset = 44F11h]

MMCSD12_UHS2_GEN_CAP is shown in [Figure 18-252](#) and described in [Table 18-624](#).

Return to [Summary Table](#).

Start Address of General Capabilities is pointed by the MMCSD12_UHS2_GEN_CAP Register.

Table 18-623. MMCSD12_UHS2_GEN_CAP Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0110h
MMCSD2_CTL_CFG	04F9 8110h

Figure 18-252. MMCSD12_UHS2_GEN_CAP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
CORECFG_UHS2_BUS_TOPOLOGY		CORECFG_UHS2_MAX_DEVICES				DEVICE_TYPE	
R-0h		R-1h				R-0h	
15	14	13	12	11	10	9	8
RESERVED	CFG_64BIT_ADDRESSING	NUM_LANES					
R-0h	R-1h	R-Fh					
7	6	5	4	3	2	1	0
GAP				DAP			
R-1h				R-1h			

LEGEND: R = Read Only; -n = value after reset

Table 18-624. MMCSD12_UHS2_GEN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-22	CORECFG_UHS2_BUS_TOPOLOGY	R	0h	Bus Topology This field indicates one of bus topologies configured by a Host system. 0h: P2P Connection 1h: Ring Connection 2h: HUB Connection 3h: HUB is Connected in Ring
21-18	CORECFG_UHS2_MAX_DEVICES	R	1h	Number of Devices Supported This field indicates the maximum number of devices supported by the Host Controller. 0h: Not used 1h: 1 Devices 2h: 2 Devices Fh: 15 Devices

Table 18-624. MMCSDB12_UHS2_GEN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	DEVICE_TYPE	R	0h	Removable/Embedded This field indicates device type configured by a Host system. 0h: Removable Card (P2P) 1h: Embedded Devices 2h: Embedded Devices + Removable Card 3h: Reserved
15	RESERVED	R	0h	Reserved
14	CFG_64BIT_ADDRESSING	R	1h	64-bit Addressing This field indicates support of 64-bit addressing by the Host Controller. 0h: 32-bit Addressing is supported 1h: 32-bit and 64-bit Addressing is supported
13-8	NUM_LANES	R	Fh	Number of Lanes and Functionalities This field indicates support of lanes by the Host Controller. 0 mean not supported and 1 means supported. D08: 2L-HD D09: 2D1U-FD D10: 1D2U-FD D11: 2D2U-FD D12: Reserved D13: Reserved
7-4	GAP	R	1h	GAP (Group Allocation Power) This field indicates the maximum capability of host power supply for a group configured by a Host system. This field is used to set the argument of DEVICE_INIT CCM. 0h: Not used 1h: 360 mW 2h: 720 mW Fh: 360 x 15 mW
3-0	DAP	R	1h	DAP (Device Allocation Power) This field indicates the maximum capability of host power supply for a device configured by a Host system. This field is used to set the argument of DEVICE_INIT CCMD. 0h: 360 mW (Default) 1h: 360 mW 2h: 720 mW Fh: 360 x 15 mW

18.6.73 MMCSD12_UHS2_PHY_CAP Register (Offset = 114h) [reset = 110000h]

MMCSD12_UHS2_PHY_CAP is shown in [Figure 18-253](#) and described in [Table 18-626](#).

Return to [Summary Table](#).

Start Address of PHY Capabilities is pointed by the MMCSD12_UHS2_CAPABILITIES_PTR Register.

Table 18-625. MMCSD12_UHS2_PHY_CAP Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0114h
MMCSD2_CTL_CFG	04F9 8114h

Figure 18-253. MMCSD12_UHS2_PHY_CAP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
N_LSS_DIR				N_LSS_SYN			
R-1h				R-1h			
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SPEED_RANGE		RESERVED					
R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 18-626. MMCSD12_UHS2_PHY_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	N_LSS_DIR	R	1h	Host N_LSS_DIR This field indicates the minimum N_LSS_DIR required by the Host Controller. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h: 4 x 3 LSS Fh: 4 x 15 LSS
19-16	N_LSS_SYN	R	1h	Host N_LSS_SYN This field indicates the minimum N_LSS_SYN required by the Host Controller. 0h: 4 x 16 LSS 1h: 4 x 1 LSS 2h: 4 x 2 LSS 3h: 4 x 3 LSS Fh: 4 x 15 LSS
15-8	RESERVED	R	0h	Reserved

Table 18-626. MMCSDB12_UHS2_PHY_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	SPEED_RANGE	R	0h	Speed Range This field indicates supported Speed Range by the Host Controller. 0h: Range A (Default) 1h: Range A and Range B 2h: Reserved 3h: Reserved
5-0	RESERVED	R	0h	Reserved

18.6.74 MMCSDB12_UHS2_LNK_TRN_CAP Register (Offset = 118h) [reset = 8120000100h]

MMCSDB12_UHS2_LNK_TRN_CAP is shown in [Figure 18-254](#) and described in [Table 18-628](#).

Return to [Summary Table](#).

Start Address of LINK/TRAN settings is pointed by the MMCSDB12_UHS2_CAPABILITIES_PTR Register.

**Table 18-627. MMCSDB12_UHS2_LNK_TRN_CAP
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0118h
MMCSDB2_CTL_CFG	04F9 8118h

Figure 18-254. MMCSDB12_UHS2_LNK_TRN_CAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-0h															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED								N_DATA_GAP							
R-0h								R-81h							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAX_BLK_LENGTH												RESERVED			
R-200h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N_FCU								RESERVED							
R-1h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 18-628. MMCSDB12_UHS2_LNK_TRN_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39-32	N_DATA_GAP	R	81h	Host N_DATA_GAP This field indicates the minimum number of data gap (DIDL) supported by the Host Controller. 00h: No Gap 01h: 1 LSS 02h: 2 LSS 03h: 3 LSS FFh: 255 LSS
31-20	MAX_BLK_LENGTH	R	200h	Host Maximum Block Length This field indicates maximum block length by the Host Controller. 000h: Not Used 001h: 1 byte 002h: 2 bytes 200h: 512 bytes 800h: 2048 bytes 801h - FFFh: Not Used
19-16	RESERVED	R	0h	Reserved

Table 18-628. MMCS D12_UHS2_LNK_TRN_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	N_FCU	R	1h	Host N_FCU This field indicates maximum the number of blocks in a Flow Control unit by the Host Controller. This value is determined by supported buffer size. 00h: 256 Blocks 01h: 1 Block 02h: 2 Block 03h: 3 Block FFh: 255 Blocks
7-0	RESERVED	R	0h	Reserved

18.6.75 MMCSD12_FORCE_UHSII_ERR_INT_STS Register (Offset = 120h) [reset = 0h]

MMCSD12_FORCE_UHSII_ERR_INT_STS is shown in [Figure 18-255](#) and described in [Table 18-630](#).

Return to [Summary Table](#).

This register is not physically implemented, rather it is an address where the MMCSD12_UHS2_ERR_INTR_STS register can be written.

Table 18-629.
MMCSD12_FORCE_UHSII_ERR_INT_STS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0120h
MMCSD2_CTL_CFG	04F9 8120h

Figure 18-255. MMCSD12_FORCE_UHSII_ERR_INT_STS Register

31	30	29	28	27	26	25	24
VENDOR_SPECIFIC					RESERVED		
W-0h					R-0h		
23	22	21	20	19	18	17	16
RESERVED						TIMEOUT_DEA DLOCK	TIMEOUT_CM D_RES
R-0h						W-0h	W-0h
15	14	13	12	11	10	9	8
ADMA	RESERVED						EBSY
W-0h	R-0h						W-0h
7	6	5	4	3	2	1	0
UNRECOVERA BLE	RESERVED	TID	FRAMING	CRC	RETRY_EXPIR ED	RES_PKT	HEADER
W-0h	R-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 18-630. MMCSD12_FORCE_UHSII_ERR_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	VENDOR_SPECIFIC	W	0h	Force Event for Vendor Specific Error 0h: Not Affected 1h: Vendor Specific Error Status is set
26-18	RESERVED	R	0h	Reserved
17	TIMEOUT_DEADLOCK	W	0h	Force Event for Timeout for Deadlock Setting this bit forces the Host Controller to set Timeout for Deadlock in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Timeout for Deadlock Error status is set
16	TIMEOUT_CMD_RES	W	0h	Force Event for Timeout for CMD_RES Setting this bit forces the Host Controller to set Timeout for CMD_RES in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Timeout for CMD_RES Status is set
15	ADMA	W	0h	Force Event for ADMA Error Setting this bit forces the Host Controller to set ADMA Error in the MMCSD12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: ADMA Error Status is set

Table 18-630. MMCSDB12_FORCE_UHS2_ERR_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-9	RESERVED	R	0h	Reserved
8	EBSY	W	0h	Force Event for EBSY Error Setting this bit forces the Host Controller to set EBSY Error in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: EBSY Error Status is set
7	UNRECOVERABLE	W	0h	Force Event for Unrecoverable Error Setting this bit forces the Host Controller to set Unrecoverable Error in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Unrecoverable Error Status is set
6	RESERVED	R	0h	Reserved
5	TID	W	0h	Force Event for TID Error Setting this bit forces the Host Controller to set TID Error in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: TID Error Status is set
4	FRAMING	W	0h	Force Event for Framing Error Setting this bit forces the Host Controller to set Framing Error in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Framing Error Status is set
3	CRC	W	0h	Force Event for CRC Error Setting this bit forces the Host Controller to set CRC Error in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: CRC Error Status is set
2	RETRY_EXPIRED	W	0h	Force Event for Retry Expired Setting this bit forces the Host Controller to set Retry Expired in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Retry expired error status is set
1	RES_PKT	W	0h	Force Event for RES Packet Error Setting this bit forces the Host Controller to set RES Packet Error in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: RES packet error status is set
0	HEADER	W	0h	Force Event for Header Error Setting this bit forces the Host Controller to set Header Error in the MMCSDB12_UHS2_ERR_INTR_STS register. 0h: Not affected 1h: Header error status is set

18.6.76 MMCSD12_CQ_VERSION Register (Offset = 200h) [reset = 510h]

MMCSD12_CQ_VERSION is shown in [Figure 18-256](#) and described in [Table 18-632](#).

Return to [Summary Table](#).

This register provides information about the version of the eMMC CQ (Command Queueing) standard which is 285 implemented by the CQE, in BCD format. The current version is rev 5.1.

The following table describes the CQBASE+00h: Command Queueing Version.

Table 18-631. MMCSD12_CQ_VERSION Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0200h
MMCSD2_CTL_CFG	04F9 8200h

Figure 18-256. MMCSD12_CQ_VERSION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				EMMC_MAJOR_VER_NUM			
R-0h				R-5h			
7	6	5	4	3	2	1	0
EMMC_MINOR_VER_NUM				EMMC_VERSION_SUFFIX			
R-1h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 18-632. MMCSD12_CQ_VERSION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	EMMC_MAJOR_VER_NUM	R	5h	eMMC Major Version Number (digit left of decimal point), in BCD format
7-4	EMMC_MINOR_VER_NUM	R	1h	eMMC Minor Version Number (digit right of decimal point), in BCD format
3-0	EMMC_VERSION_SUFFIX	R	0h	eMMC Version Suffix (2nd digit right of decimal point), in BCD format

18.6.77 MMCS12_CQ_CAPABILITIES Register (Offset = 204h) [reset = 30C8h]

MMCS12_CQ_CAPABILITIES is shown in [Figure 18-257](#) and described in [Table 18-634](#).

Return to [Summary Table](#).

This register is reserved for capability indication.

Table 18-633. MMCS12_CQ_CAPABILITIES Instances

Instance	Physical Address
MMCS1_CTL_CFG	04FB 0204h
MMCS2_CTL_CFG	04F9 8204h

Figure 18-257. MMCS12_CQ_CAPABILITIES Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CF_MUL				RESERVED		CF_VAL	
R-3h				R-0h		R-C8h	
7	6	5	4	3	2	1	0
CF_VAL							
R-C8h							

LEGEND: R = Read Only; -n = value after reset

Table 18-634. MMCS12_CQ_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	CF_MUL	R	3h	Internal Timer Clock Frequency Multiplier (ITCFMUL) ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details (MMCS12_CQ_CAPABILITIES[9-0] CF_VAL). Field Value Description: 0h: 0.001 MHz 1h: 0.01 MHz 2h: 0.1 MHz 3h: 1 MHz 4h: 10 MHz Other values are reserved
11-10	RESERVED	R	0h	Reserved

Table 18-634. MMCSDB12_CQ_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	CF_VAL	R	C8h	Internal Timer Clock Frequency Value (ITCFVAL) ITCFMUL and ITCFVAL indicate the frequency of the clock used for interrupt coalescing timer and for determining the polling period when using periodic SEND_QUEUE_STATUS (CMD13) polling. The clock frequency is calculated as $ITCFVAL \times ITCFMUL$. For example, to encode 19.2 MHz ITCFVAL shall be C0h (= 192 decimal) and ITCFMUL shall be 2h (0.1 MHz). $192 \times 0.1 \text{ MHz} = 19.2 \text{ MHz}$

18.6.78 MMCSDB12_CQ_CONFIG Register (Offset = 208h) [reset = 0h]

MMCSDB12_CQ_CONFIG is shown in [Figure 18-258](#) and described in [Table 18-636](#).

Return to [Summary Table](#).

This register controls CQE behavior affecting the general operation of command queueing 290 module or operation of multiple tasks in the same time.

Table 18-635. MMCSDB12_CQ_CONFIG Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0208h
MMCSDB2_CTL_CFG	04F9 8208h

Figure 18-258. MMCSDB12_CQ_CONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			DCMD_ENA	RESERVED			TASK_DESC_SIZE
R-0h			R/W-0h	R-0h			R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CQ_ENABLE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-636. MMCSDB12_CQ_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	DCMD_ENA	R/W	0h	Direct Command (DCMD) Enable This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Bit Value Description 0h: Task descriptor in slot #31 is a Data Transfer Task Descriptor 1h: Task descriptor in slot #31 is a DCMD Task Descriptor
11-9	RESERVED	R	0h	Reserved
8	TASK_DESC_SIZE	R/W	0h	Task Descriptor Size This bit indicates whether the task descriptor size is 128 bits or 64 bits . This bit can only be configured when the MMCSDB12_CQ_CONFIG[0] CQ_ENABLE bit is 0h (command queueing is disabled). Bit Value Description 0h: Task descriptor size is 64 bits 1h: Task descriptor size is 128 bits
7-1	RESERVED	R	0h	Reserved

Table 18-636. MMCSDB12_CQ_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CQ_ENABLE	R/W	0h	<p>Command Queueing Enable</p> <p>Software shall write 1h to this bit when in order to enable command queueing mode (enable CQE).</p> <p>When this bit is 0h, CQE is disabled and software controls the eMMC bus using the legacy eMMC host controller.</p> <p>Before software writes 1h to this bit, software shall verify that the eMMC host controller is in idle state and there are no commands or data transfers ongoing.</p> <p>When software wants to exit command queueing mode, it shall clear all previous tasks if such exist before setting this bit to 0h.</p>

18.6.79 MMCSd12_CQ_CONTROL Register (Offset = 20Ch) [reset = 0h]

MMCSd12_CQ_CONTROL is shown in [Figure 18-259](#) and described in [Table 18-638](#).

Return to [Summary Table](#).

This register controls CQE behavior affecting the general operation of command queueing 293 module or operation of multiple tasks in the same time.

Table 18-637. MMCSd12_CQ_CONTROL Instances

Instance	Physical Address
MMCSd1_CTL_CFG	04FB 020Ch
MMCSd2_CTL_CFG	04F9 820Ch

Figure 18-259. MMCSd12_CQ_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CLEAR_ALL_T ASKS
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							HALT_BIT
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-638. MMCSd12_CQ_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CLEAR_ALL_TASKS	R/W	0h	Clear All Tasks Software shall write 1h to this bit when it wants to clear all the tasks sent to the device. This bit can only be written when CQE is in halt state (Halt bit is 1h). When software writes 1h, the value of the register is updated to 1h, and CQE shall reset the MMCSd12_CQ_TASK_DOOR_BELL register and all other context information for all unfinished tasks. Then CQE will clear this bit. Software should poll on this bit until it is set to back 0 and may then resume normal operation, by clearing the Halt bit. CQE does not communicate to the device that the tasks were cleared. It is softwares responsibility to order the device to discard the tasks in its queue using CMDQ_TASK_MGMT command. Writing 0h to this register shall have no effect.
7-1	RESERVED	R	0h	Reserved

Table 18-638. MMCSD12_CQ_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HALT_BIT	R/W	0h	<p>Halt</p> <p>Host software shall write 1h to the bit when it wants to acquire software control over the eMMC bus and disable CQE from issuing commands on the bus.</p> <p>For example, issuing a Discard Task command (CMDQ_TASK_MGMT).</p> <p>When software writes 1h, CQE shall complete the ongoing task if such a task is in progress.</p> <p>Once the task is completed and CQE is in idle state, CQE shall not issue new commands and shall indicate so to software by setting this bit to 1h.</p> <p>Software may poll on this bit until it is set to 1h, and may only then send commands on the eMMC bus.</p> <p>In order to exit halt state (resume CQE activity), software shall clear this bit (write 0h). Writing 0h when the value is already 0h shall have no effect.</p>

18.6.80 MMCSDB12_CQ_INTR_STS Register (Offset = 210h) [reset = 0h]

MMCSDB12_CQ_INTR_STS is shown in [Figure 18-260](#) and described in [Table 18-640](#).

Return to [Summary Table](#).

This register indicates pending interrupts that require service. Each bit in this registers is asserted 296 in response a specific event, only if the respective bit is set in the MMCSDB12_CQ_INTR_STS_ENA register.

Table 18-639. MMCSDB12_CQ_INTR_STS Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0210h
MMCSDB2_CTL_CFG	04F9 820Ch

Figure 18-260. MMCSDB12_CQ_INTR_STS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARE D	RESP_ERR_D ET	TASK_COMPL ETE	HALT_COMPL ETE
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-640. MMCSDB12_CQ_INTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W1C	0h	Task Error Interrupt (TERR) This bit is asserted when task error is detected due to invalid task descriptor.
3	TASK_CLEARED	R/W1C	0h	Task Cleared (TCL) This status bit is asserted (if MMCSDB12_CQ_INTR_STS_ENA[3] TASK_CLEARED = 1h) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (MMCSDB12_CQ_TASK_CLEAR) or clearing of all tasks (MMCSDB12_CQ_CONTROL).
2	RESP_ERR_DET	R/W1C	0h	Response Error Detected Interrupt (RED) This status bit is asserted (if MMCSDB12_CQ_INTR_STS_ENA[2] RESP_ERR_DET = 1h) when a response is received with an error bit set in the device status field. Software uses the MMCSDB12_CQ_RESP_ERR_MASK register to configure which device status bit fields may trigger an interrupt, and which are masked.

Table 18-640. MMCSD12_CQ_INTR_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TASK_COMPLETE	R/W1C	0h	Task Complete Interrupt (TCC) This status bit is asserted (if MMCSD12_CQ_INTR_STS_ENA[1] TASK_COMPLETE = 1h) when at least one of the following two conditions are met: (1) A task is completed and the INT bit is set in its Task Descriptor (2) Interrupt caused by Interrupt Coalescing logic
0	HALT_COMPLETE	R/W1C	0h	Halt Complete Interrupt (HAC) This status bit is asserted (if MMCSD12_CQ_INTR_STS_ENA[0] HALT_COMPLETE = 1h) when the MMCSD12_CQ_CONTROL[0] HALT_BIT bit transitions from 0h to 1h indicating that host controller has completed its current ongoing task and has entered halt state.

18.6.81 MMCSDB12_CQ_INTR_STS_ENA Register (Offset = 214h) [reset = 0h]

MMCSDB12_CQ_INTR_STS_ENA is shown in [Figure 18-261](#) and described in [Table 18-642](#).

Return to [Summary Table](#).

This register enables and disables the reporting of the corresponding interrupt to host software in 299 MMCSDB12_CQ_INTR_STS register. When a bit is set (1h) and the corresponding interrupt condition is active, then the 300 bit in the MMCSDB12_CQ_INTR_STS register is asserted. Interrupt sources that are disabled (0h) are not indicated in the MMCSDB12_CQ_INTR_STS 301 register. This register is bit-index matched to the MMCSDB12_CQ_INTR_STS register.

Table 18-641. MMCSDB12_CQ_INTR_STS_ENA Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0214h
MMCSDB2_CTL_CFG	04F9 8214h

Figure 18-261. MMCSDB12_CQ_INTR_STS_ENA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARE D	RESP_ERR_D ET	TASK_COMPL ETE	HALT_COMPL ETE
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-642. MMCSDB12_CQ_INTR_STS_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Status Enable (TERR) 1h: MMCSDB12_CQ_INTR_STS[4] TASK_ERROR bit will be set when its interrupt condition is active 0h: MMCSDB12_CQ_INTR_STS[4] TASK_ERROR bit is disabled
3	TASK_CLEARED	R/W	0h	Task Cleared Status Enable (TCL) 1h: MMCSDB12_CQ_INTR_STS[3] TASK_CLEARED bit will be set when its interrupt condition is active 0h: MMCSDB12_CQ_INTR_STS[3] TASK_CLEARED bit is disabled
2	RESP_ERR_DET	R/W	0h	Response Error Detected Status Enable (RED) 1h: MMCSDB12_CQ_INTR_STS[2] RESP_ERR_DET bit will be set when its interrupt condition is active 0h: MMCSDB12_CQ_INTR_STS[2] RESP_ERR_DET bit is disabled

Table 18-642. MMCSDB12_CQ_INTR_STS_ENA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TASK_COMPLETE	R/W	0h	Task Complete Status Enable (TCC) 1h: MMCSDB12_CQ_INTR_STS[1] TASK_COMPLETE bit will be set when its interrupt condition is active 0h: MMCSDB12_CQ_INTR_STS[1] TASK_COMPLETE bit is disabled
0	HALT_COMPLETE	R/W	0h	Halt Complete Status Enable (HAC) 1h: MMCSDB12_CQ_INTR_STS[0] HALT_COMPLETE bit will be set when its interrupt condition is active 0h: MMCSDB12_CQ_INTR_STS[0] HALT_COMPLETE bit is disabled

18.6.82 MMCS12_CQ_INTR_SIG_ENA Register (Offset = 218h) [reset = 0h]

MMCS12_CQ_INTR_SIG_ENA is shown in [Figure 18-262](#) and described in [Table 18-644](#).

Return to [Summary Table](#).

This register enables and disables the generation of interrupts to host software. When a bit is set 304 (1h) and the corresponding bit in the MMCS12_CQ_INTR_STS register is set, then an interrupt is generated. Interrupt sources 305 that are disabled (0h) are still indicated in the MMCS12_CQ_INTR_STS register. This register is bit-index matched 306 to the MMCS12_CQ_INTR_STS register.

Table 18-643. MMCS12_CQ_INTR_SIG_ENA Instances

Instance	Physical Address
MMCS1_CTL_CFG	04FB 0218h
MMCS2_CTL_CFG	04F9 8218h

Figure 18-262. MMCS12_CQ_INTR_SIG_ENA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			TASK_ERROR	TASK_CLEARED	RESP_ERR_DET	TASK_COMPLETE	HALT_COMPLETE
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-644. MMCS12_CQ_INTR_SIG_ENA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	TASK_ERROR	R/W	0h	Task Error Interrupt Signal Enable (TERR) When set and the MMCS12_CQ_INTR_STS[4] TASK_ERROR bit is asserted, the CQE shall generate an interrupt.
3	TASK_CLEARED	R/W	0h	Task Cleared Signal Enable (TCL) When set and the MMCS12_CQ_INTR_STS[3] TASK_CLEARED bit is asserted, the CQE shall generate an interrupt.
2	RESP_ERR_DET	R/W	0h	Response Error Detected Signal Enable (RED) When set and the MMCS12_CQ_INTR_STS[2] RESP_ERR_DET bit is asserted, the CQE shall generate an interrupt.
1	TASK_COMPLETE	R/W	0h	Task Complete Signal Enable (TCC) When set and the MMCS12_CQ_INTR_STS[1] TASK_COMPLETE bit is asserted, the CQE shall generate an interrupt.
0	HALT_COMPLETE	R/W	0h	Halt Complete Signal Enable (HAC) When set and the MMCS12_CQ_INTR_STS[0] HALT_COMPLETE bit is asserted, the CQE shall generate an interrupt.

18.6.83 MMCSDB12_CQ_INTR_COALESCING Register (Offset = 21Ch) [reset = 0h]

MMCSDB12_CQ_INTR_COALESCING is shown in [Figure 18-263](#) and described in [Table 18-646](#).

Return to [Summary Table](#).

This register controls the interrupt coalescing feature.

Table 18-645. MMCSDB12_CQ_INTR_COALESCING Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 021Ch
MMCSDB2_CTL_CFG	04F9 821Ch

Figure 18-263. MMCSDB12_CQ_INTR_COALESCING Register

31	30	29	28	27	26	25	24
CQINTCOALES C_ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED			IC_STATUS	RESERVED			
R-0h			R-0h	R-0h			
15	14	13	12	11	10	9	8
RESERVED			CTR_THRESHOLD				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED	TIMEOUT_VAL						
R-0h	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-646. MMCSDB12_CQ_INTR_COALESCING Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CQINTCOALESC_ENAB LE	R/W	0h	Interrupt Coalescing Enable/Disable: When set to 0h by software, command responses are neither counted nor timed. Interrupts are still triggered by completion of tasks with INT = 1 in the Task Descriptor. When set to 1h, the interrupt coalescing mechanism is enabled and coalesced interrupts are generated.
30-21	RESERVED	R	0h	Reserved
20	IC_STATUS	R	0h	Interrupt Coalescing Status Bit (ICSB): This bit indicates to software whether any tasks (with INT = 0) have completed and counted towards interrupt coalescing (ICSB is set if and only if IC counter > 0). Bit Value Description 0h: No task completions have occurred since last counter reset (IC counter = 0) 1h: At least one task completion has been counted (IC counter > 0)
19-13	RESERVED	R	0h	Reserved

Table 18-646. MMCS12_CQ_INTR_COALESCING Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	CTR_THRESHOLD	R/W	0h	Interrupt Coalescing Counter Threshold (ICCTH): Software uses this field to configure the number of task completions (only tasks with INT = 0 in the Task Descriptor) which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT = 0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in ICCTH. The maximum allowed value is 31. Note: When ICCTH is 0h, task completions are not counted, and counting-based interrupts are not generated.
7	RESERVED	R	0h	Reserved
6-0	TIMEOUT_VAL	R/W	0h	Interrupt Coalescing Timeout Value (ICTOVAL): Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT = 0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timers unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field in the MMCS12_CQ_CAPABILITIES register. The minimum value is 1h (1024 clock periods) and the maximum value is 7Fh (127 × 1024 clock periods). For example, a MMCS12_CQ_CAPABILITIES field value of 0h indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in ICTOVAL is 10h, the calculated polling period is 16 × 1024 × 52.08 ns = 853.33 μs Note: When ICTOVAL is 0h, the timer is not running, and timer-based interrupts are not generated.

18.6.84 MMCSd12_CQ_TDL_BASE_ADDR Register (Offset = 220h) [reset = 0h]

MMCSd12_CQ_TDL_BASE_ADDR is shown in [Figure 18-264](#) and described in [Table 18-648](#).

Return to [Summary Table](#).

This register is used for configuring the lower 32 bits of the byte address of the head of the Task 312 Descriptor List in the host memory.

**Table 18-647. MMCSd12_CQ_TDL_BASE_ADDR
Instances**

Instance	Physical Address
MMCSd1_CTL_CFG	04FB 0220h
MMCSd2_CTL_CFG	04F9 8220h

Figure 18-264. MMCSd12_CQ_TDL_BASE_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTLBA_LO																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-648. MMCSd12_CQ_TDL_BASE_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTLBA_LO	R/W	0h	Task Descriptor List Base Address (TDLBA) This register stores the LSB bits (bits 31-0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is $32 \times (\text{Task Descriptor size} + \text{Transfer Descriptor size})$ as configured by Host driver. This address shall be set on Byte1 KByte boundary. The lower 10 bits of this register shall be set to 0h by software and shall be ignored by CQE.

18.6.85 MMCSDB12_CQ_TDL_BASE_ADDR_UPBITS Register (Offset = 224h) [reset = 0h]

MMCSDB12_CQ_TDL_BASE_ADDR_UPBITS is shown in [Figure 18-265](#) and described in [Table 18-650](#).

Return to [Summary Table](#).

This register is used for configuring the upper 32 bits of the byte address of the head of the Task 316 Descriptor List in the host memory.

Table 18-649.
MMCSDB12_CQ_TDL_BASE_ADDR_UPBITS
Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0224h
MMCSDB2_CTL_CFG	04F9 8224h

Figure 18-265. MMCSDB12_CQ_TDL_BASE_ADDR_UPBITS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQ_TDLBA_HI																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-650. MMCSDB12_CQ_TDL_BASE_ADDR_UPBITS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQ_TDLBA_HI	R/W	0h	Task Descriptor List Base Address (TDLBA) This register stores the MSB bits (bits 63-32) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is $32 \times (\text{Task Descriptor size} + \text{Transfer Descriptor size})$ as configured by Host driver. This register is reserved when using 32-bit addressing mode.

18.6.86 MMCSDB12_CQ_TASK_DOOR_BELL Register (Offset = 228h) [reset = 0h]

MMCSDB12_CQ_TASK_DOOR_BELL is shown in [Figure 18-266](#) and described in [Table 18-652](#).

Return to [Summary Table](#).

Using this register, software triggers CQE to process a new task.

Table 18-651. MMCSDB12_CQ_TASK_DOOR_BELL Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0228h
MMCSDB2_CTL_CFG	04F9 8228h

Figure 18-266. MMCSDB12_CQ_TASK_DOOR_BELL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTDB_VAL																															
W1S-0h																															

LEGEND: W1S = Write 1 to Set Bit; -n = value after reset

Table 18-652. MMCSDB12_CQ_TASK_DOOR_BELL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTDB_VAL	W1S	0h	<p>Command Queueing Task Doorbell</p> <p>Software shall configure the MMCSDB12_CQ_TDL_BASE_ADDR[31-0] CQTDLBA_LO and MMCSDB12_CQ_TDL_BASE_ADDR_UPBITS[31-0] CQTDLBA_HI bit fields, and enable CQE in the MMCSDB12_CQ_CONFIG register before using this register.</p> <p>Writing 1h to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL.</p> <p>CQE always processes tasks in-order according to the order submitted to the list by the MMCSDB12_CQ_TASK_DOOR_BELL register write transactions.</p> <p>CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device.</p> <p>CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument.</p> <p>The corresponding bit is cleared to 0h by CQE in one of the following events:</p> <ul style="list-style-type: none"> (a) When a task execution is completed (with success or error) (b) The task is cleared using MMCSDB12_CQ_TASK_CLEAR register (c) All tasks are cleared using MMCSDB12_CQ_CONTROL register (d) CQE is disabled using MMCSDB12_CQ_CONFIG register <p>Software may initiate multiple tasks at the same time (batch submission) by writing 1h to multiple bits of this register in the same transaction.</p> <p>In the case of batch submission:</p> <p>CQE shall process the tasks in order of the task index, starting with the lowest index.</p> <p>If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order.</p> <p>Writing 0h by software shall have no impact on the hardware, and will not change the value of the register bit.</p>

18.6.87 MMCSDB12_CQ_TASK_COMP_NOTIF Register (Offset = 22Ch) [reset = 0h]

MMCSDB12_CQ_TASK_COMP_NOTIF is shown in [Figure 18-267](#) and described in [Table 18-654](#).

Return to [Summary Table](#).

This register is used by CQE to notify software about completed tasks.

Table 18-653. MMCSDB12_CQ_TASK_COMP_NOTIF Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 022Ch
MMCSDB2_CTL_CFG	04F9 822Ch

Figure 18-267. MMCSDB12_CQ_TASK_COMP_NOTIF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTCN_VAL																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-654. MMCSDB12_CQ_TASK_COMP_NOTIF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTCN_VAL	R/W1C	0h	Task Complete Notification CQE shall set bit n of this register (at the same time it clears bit n of the MMCSDB12_CQ_TASK_DOOR_BELL register) when a task execution is completed (with success or error). When receiving interrupt for task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1h to the corresponding bits.

18.6.88 MMCSD12_CQ_DEV_QUEUE_STATUS Register (Offset = 230h) [reset = 0h]

MMCSD12_CQ_DEV_QUEUE_STATUS is shown in [Figure 18-268](#) and described in [Table 18-656](#).

Return to [Summary Table](#).

This register stores the most recent value of the device's queue status.

Table 18-655. MMCSD12_CQ_DEV_QUEUE_STATUS Instances

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0230h
MMCSD2_CTL_CFG	04F9 8230h

Figure 18-268. MMCSD12_CQ_DEV_QUEUE_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQDQ_STS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-656. MMCSD12_CQ_DEV_QUEUE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQDQ_STS	R	0h	Device Queue Status Every time the Host controller receives a queue status register (QSR) from the device, it updates this register with the response of status command (the device's queue status).

18.6.89 MMCSDB12_CQ_DEV_PENDING_TASKS Register (Offset = 234h) [reset = 0h]

MMCSDB12_CQ_DEV_PENDING_TASKS is shown in [Figure 18-269](#) and described in [Table 18-658](#).

Return to [Summary Table](#).

This register indicates to software which tasks are queued in the device, awaiting execution.

Table 18-657.
MMCSDB12_CQ_DEV_PENDING_TASKS Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0234h
MMCSDB2_CTL_CFG	04F9 8234h

Figure 18-269. MMCSDB12_CQ_DEV_PENDING_TASKS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQDP_TSXS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-658. MMCSDB12_CQ_DEV_PENDING_TASKS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQDP_TSXS	R	0h	Device Pending Tasks Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task hasnt been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software needs to read this register in the task-discard procedure, when the controller is halted, to determine if the task is queued in the device. If the task is queued, the driver sends a CMDQ_TASK_MGMT (CMD48) to the device ordering it to discard the task. Then software clears the task in the CQE. Only then the software orders CQE to resume its operation using MMCSDB12_CQ_CONTROL register.

18.6.90 MMCSDB12_CQ_TASK_CLEAR Register (Offset = 238h) [reset = 0h]

MMCSDB12_CQ_TASK_CLEAR is shown in [Figure 18-270](#) and described in [Table 18-660](#).

Return to [Summary Table](#).

This register is used for removing an outstanding task in the CQE 327. The register should be used only when CQE is in Halt state.

**Table 18-659. MMCSDB12_CQ_TASK_CLEAR
Instances**

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0238h
MMCSDB2_CTL_CFG	04F9 8238h

Figure 18-270. MMCSDB12_CQ_TASK_CLEAR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQTCLR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-660. MMCSDB12_CQ_TASK_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQTCLR	R/W	0h	<p>Command Queueing Task Clear</p> <p>Writing 1h to bit n of this register orders CQE to clear a task which software has previously issued.</p> <p>This bit can only be written when CQE is in Halt state as indicated in the MMCSDB12_CQ_CONFIG register Halt bit.</p> <p>When software writes 1h to a bit in this register, CQE updates the value to 1h, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0h) in the MMCSDB12_CQ_TASK_CLEAR and in MMCSDB12_CQ_TASK_DOOR_BELL registers once clear operation is complete.</p> <p>Software should poll on the MMCSDB12_CQ_TASK_CLEAR register until it is cleared to verify clear operation was complete.</p> <p>Writing to this register only clears the task in the CQE and does not have impact on the device. In order to discard the task in the device, host software shall send CMDQ_TASK_MGMT while CQE is still in Halt state.</p> <p>Host driver is not allowed to use this register to clear multiple tasks at the same time. Clearing multiple tasks can be done using MMCSDB12_CQ_CONTROL register.</p> <p>Writing 0h to a register bit shall have no impact.</p>

18.6.91 MMCSDB12_CQ_SEND_STS_CONFIG1 Register (Offset = 240h) [reset = 11000h]

MMCSDB12_CQ_SEND_STS_CONFIG1 is shown in [Figure 18-271](#) and described in [Table 18-662](#).

Return to [Summary Table](#).

The register controls when the SEND_QUEUE_STATUS commands are sent.

Table 18-661. MMCSDB12_CQ_SEND_STS_CONFIG1 Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0240h
MMCSDB2_CTL_CFG	04F9 8240h

Figure 18-271. MMCSDB12_CQ_SEND_STS_CONFIG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												CMD_BLK_CNTR			
R-0h												R/W-1h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_IDLE_TIMER															
R/W-1000h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-662. MMCSDB12_CQ_SEND_STS_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	CMD_BLK_CNTR	R/W	1h	Send Status Command Block Counter This field indicates to CQE when to send SEND_QUEUE_STATUS (CMD13) command to inquire the status of the devices task queue. A value of n means CQE shall send status command on the CMD line, during the transfer of data block BLOCK_CNT-n , on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. A value of 0h means that SEND_QUEUE_STATUS (CMD13) command shall not be sent during the transaction. Instead it will be sent only when the data lines are idle. A value of 1 means that STATUS command is to be sent during the last block of the transaction.
15-0	CMD_IDLE_TIMER	R/W	1000h	Send Status Command Idle Timer This field indicates to CQE the polling period to use when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicating that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field in the MMCSDB12_CQ_CAPABILITIES register. The minimum value is 1h (1 clock period) and the maximum value is FFFFh (65535 clock periods). Default interval is: 4096 clock periods. For example, a MMCSDB12_CQ_CAPABILITIES field value of 0h indicates a 19.2 MHz clock frequency (period = 52.08 ns).

18.6.92 MMCSD12_CQ_SEND_STS_CONFIG2 Register (Offset = 244h) [reset = 0h]

MMCSD12_CQ_SEND_STS_CONFIG2 is shown in [Figure 18-272](#) and described in [Table 18-664](#).

Return to [Summary Table](#).

This register is used for 333 configuring RCA field in SEND_QUEUE_STATUS command argument.

**Table 18-663. MMCSD12_CQ_SEND_STS_CONFIG2
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 0244h
MMCSD2_CTL_CFG	04F9 8244h

Figure 18-272. MMCSD12_CQ_SEND_STS_CONFIG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																QUEUE_RCA															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 18-664. MMCSD12_CQ_SEND_STS_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	QUEUE_RCA	R/W	0h	Send Queue RCA This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE shall copy this field to bits 31-16 of the argument when transmitting SEND_QUEUE_STATUS (CMD13) command.

18.6.93 MMCS12_CQ_DCMD_RESPONSE Register (Offset = 248h) [reset = 0h]

MMCS12_CQ_DCMD_RESPONSE is shown in [Figure 18-273](#) and described in [Table 18-666](#).

Return to [Summary Table](#).

This register is used for passing the response of a DCMD task to software.

Table 18-665. MMCS12_CQ_DCMD_RESPONSE Instances

Instance	Physical Address
MMCS1_CTL_CFG	04FB 0248h
MMCS2_CTL_CFG	04F9 8248h

Figure 18-273. MMCS12_CQ_DCMD_RESPONSE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAST_RESP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-666. MMCS12_CQ_DCMD_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LAST_RESP	R	0h	Direct Command Last Response This register contains the response of the command generated by the last direct command (DCMD) task which was sent. CQE shall update this register when it receives the response for a DCMD task. This register is considered valid only after bit 31 of the MMCS12_CQ_TASK_DOOR_BELL register is cleared by CQE.

18.6.94 MMCSDB12_CQ_RESP_ERR_MASK Register (Offset = 250h) [reset = FDF9A080h]

MMCSDB12_CQ_RESP_ERR_MASK is shown in [Figure 18-274](#) and described in [Table 18-668](#).

Return to [Summary Table](#).

This register controls the generation of Response Error Detection (RED) interrupt.

Table 18-667. MMCSDB12_CQ_RESP_ERR_MASK Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0250h
MMCSDB2_CTL_CFG	04F9 8250h

Figure 18-274. MMCSDB12_CQ_RESP_ERR_MASK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CQRMEM																															
R-FDF9A080h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-668. MMCSDB12_CQ_RESP_ERR_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CQRMEM	R	FDF9A080h	<p>Response Mode Error Mask</p> <p>This bit is used as in interrupt mask on the device status field which is received in R1/R1b responses.</p> <p>Bit Value Description (for any bit i):</p> <p>1h: When a R1/R1b response is received, with bit i in the device status set, a RED interrupt is generated</p> <p>0h: When a R1/R1b response is received, bit i in the device status is ignored</p> <p>The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status.</p> <p>Note: Responses to CMD13 (SQS) encode the QSR, so they are ignored by this logic.</p>

18.6.95 MMCSDB12_CQ_TASK_ERR_INFO Register (Offset = 254h) [reset = 0h]

MMCSDB12_CQ_TASK_ERR_INFO is shown in Figure 18-275 and described in Table 18-670.

Return to [Summary Table](#).

This register is updated by CQE when an error occurs on data or command related to a task activity. When such error is detected by CQE or indicated by the eMMC controller CQE stores in the MMCSDB12_CQ_TASK_ERR_INFO register the task IDs and the command indices of the commands which were executed on the 343 command line and data lines when the error occurred.

Software is expected to use this information in the error recovery procedure.

Table 18-669. MMCSDB12_CQ_TASK_ERR_INFO Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0254h
MMCSDB2_CTL_CFG	04F9 8254h

Figure 18-275. MMCSDB12_CQ_TASK_ERR_INFO Register

31	30	29	28	27	26	25	24
DATERR_VALID	RESERVED				DATERR_TASK_ID		
R-0h	R-0h				R-0h		
23	22	21	20	19	18	17	16
RESERVED		DATERR_CMD_INDEX					
R-0h		R-0h					
15	14	13	12	11	10	9	8
RESP_MODE_VALID	RESERVED				RESP_MODE_TASK_ID		
R-0h	R-0h				R-0h		
7	6	5	4	3	2	1	0
RESERVED		RESP_MODE_CMD_INDEX					
R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-670. MMCSDB12_CQ_TASK_ERR_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DATERR_VALID	R	0h	Data Transfer Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a data transfer is in progress when the error is detected/indicated, the bit is set to 1h. If a no data transfer is in progress when the error is detected/indicated, the bit is cleared to 0h.
30-29	RESERVED	R	0h	Reserved
28-24	DATERR_TASK_ID	R	0h	Data Transfer Error Task ID This field indicates the ID of the task which was executed on the data lines when an error occurred. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
23-22	RESERVED	R	0h	Reserved

Table 18-670. MMCSDB12_CQ_TASK_ERR_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	DATERR_CMD_INDEX	R	0h	Data Transfer Error Command Index This field indicates the index of the command which was executed on the data lines when an error occurred. The index shall be set to EXECUTE_READ_TASK (CMD46) or EXECUTE_WRITE_TASK (CMD47) according to the data direction. The field is updated if a data transfer is in progress when an error is detected by CQE, or indicated by eMMC controller.
15	RESP_MODE_VALID	R	0h	Response Mode Error Fields Valid This bit is updated when an error is detected by CQE, or indicated by eMMC controller. If a command transaction is in progress when the error is detected/indicated, the bit is set to 1h. If a no command transaction is in progress when the error is detected/indicated, the bit is cleared to 0h.
14-13	RESERVED	R	0h	Reserved
12-8	RESP_MODE_TASK_ID	R	0h	Response Mode Error Task ID This field indicates the ID of the task which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.
7-6	RESERVED	R	0h	Reserved
5-0	RESP_MODE_CMD_INDEX	R	0h	Response Mode Error Command Index This field indicates the index of the command which was executed on the command line when an error occurred. The field is updated if a command transaction is in progress when an error is detected by CQE, or indicated by eMMC controller.

18.6.96 MMCSd12_CQ_CMD_RESP_INDEX Register (Offset = 258h) [reset = 0h]

MMCSd12_CQ_CMD_RESP_INDEX is shown in [Figure 18-276](#) and described in [Table 18-672](#).

Return to [Summary Table](#).

This register stores the index of the last received command response.

Table 18-671. MMCSd12_CQ_CMD_RESP_INDEX Instances

Instance	Physical Address
MMCSd1_CTL_CFG	04FB 0258h
MMCSd2_CTL_CFG	04F9 8254h

Figure 18-276. MMCSd12_CQ_CMD_RESP_INDEX Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										LAST_CRI					
R-0h										R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-672. MMCSd12_CQ_CMD_RESP_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	LAST_CRI	R	0h	Last Command Response Index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

18.6.97 MMCSD12_CQ_CMD_RESP_ARG Register (Offset = 25Ch) [reset = 0h]

MMCSD12_CQ_CMD_RESP_ARG is shown in [Figure 18-277](#) and described in [Table 18-674](#).

Return to [Summary Table](#).

This register stores the index of the last received command response.

**Table 18-673. MMCSD12_CQ_CMD_RESP_ARG
Instances**

Instance	Physical Address
MMCSD1_CTL_CFG	04FB 025Ch
MMCSD2_CTL_CFG	04F9 825Ch

Figure 18-277. MMCSD12_CQ_CMD_RESP_ARG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LAST_CRA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-674. MMCSD12_CQ_CMD_RESP_ARG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LAST_CRA	R	0h	Last Command Response Argument This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

18.6.98 MMCSDB12_CQ_ERROR_TASK_ID Register (Offset = 260h) [reset = 0h]

MMCSDB12_CQ_ERROR_TASK_ID is shown in [Figure 18-278](#) and described in [Table 18-676](#).

Return to [Summary Table](#).

CQ Error Task ID Register

Table 18-675. MMCSDB12_CQ_ERROR_TASK_ID Instances

Instance	Physical Address
MMCSDB1_CTL_CFG	04FB 0260h
MMCSDB2_CTL_CFG	04F9 8260h

Figure 18-278. MMCSDB12_CQ_ERROR_TASK_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TERR_ID			
R-0h												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 18-676. MMCSDB12_CQ_ERROR_TASK_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	TERR_ID	R	0h	Task Error ID

18.7 MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

Table 18-678 lists the memory-mapped registers for the MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator. All register offset addresses not listed in Table 18-678 should be considered as reserved locations and the register contents should not be modified.

Table 18-677. MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Instances

Instance	Base Address
MMCSDB1_ECC_AGGR_RXMEM	02A2 6000h
MMCSDB2_ECC_AGGR_RXMEM	02A7 1000h

Table 18-678. MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

Offset	Acronym	Register Name	MMCSDB1_ECC_AGGR_RXMEM Physical Address	MMCSDB2_ECC_AGGR_RXMEM Physical Address
0h	MMCSDB12_RXECC_REV	Aggregator Revision Register	02A2 6000h	02A7 1000h
8h	MMCSDB12_RXECC_VECTOR	ECC Vector Register	02A2 6008h	02A7 1008h
Ch	MMCSDB12_RXECC_STAT	Misc Status Register	02A2 600Ch	02A7 100Ch
3Ch	MMCSDB12_RXECC_SEC_EOI_REG	SEC EOI Register	02A2 603Ch	02A7 103Ch
40h	MMCSDB12_RXECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	02A2 6040h	02A7 1040h
80h	MMCSDB12_RXECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	02A2 6080h	02A7 1080h
C0h	MMCSDB12_RXECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	02A2 60C0h	02A7 10C0h
13Ch	MMCSDB12_RXECC_DED_EOI_REG	DED EOI Register	02A2 613Ch	02A7 113Ch
140h	MMCSDB12_RXECC_DED_STATUS_REG0	DED Interrupt Status Register 0	02A2 6140h	02A7 1140h
180h	MMCSDB12_RXECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	02A2 6180h	02A7 1180h
1C0h	MMCSDB12_RXECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	02A2 61C0h	02A7 11C0h
200h	MMCSDB12_RXECC_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	02A2 6200h	02A7 1200h
204h	MMCSDB12_RXECC_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	02A2 6204h	02A7 1204h
208h	MMCSDB12_RXECC_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	02A2 6208h	02A7 1208h
20Ch	MMCSDB12_RXECC_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	02A2 620Ch	02A7 120Ch

18.7.1 MMCSd12_RXECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MMCSd12_RXECC_REV is shown in [Figure 18-279](#) and described in [Table 18-680](#).

Return to [Summary Table](#).

Aggregator Revision Register

Revision parameters.

Table 18-679. MMCSd12_RXECC_REV Instances

Instance	Physical Address
MMCSd1_ECC_AGGR_RXMEM	02A2 6000h
MMCSd2_ECC_AGGR_RXMEM	02A7 1000h

Figure 18-279. MMCSd12_RXECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME			BU		MODULE_ID										
R-1h			R-2h		R-6A0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-680. MMCSd12_RXECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

Table 18-681. Register Call Summary for MMCSd12_RXECC_REV

MMCSd1 / MMCSd2 RX RAM ECC Aggregator Registers

- [MMCSd12_RXECC_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]: \[0\]](#)
- [MMCSd1 / MMCSd2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.2 MMCSD12_RXECC_VECTOR Register (Offset = 8h) [reset = 0h]

MMCSD12_RXECC_VECTOR is shown in [Figure 18-280](#) and described in [Table 18-683](#).

Return to [Summary Table](#).

ECC Vector Register

**Table 18-682. MMCSD12_RXECC_VECTOR
Instances**

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	02A2 6008h
MMCSD2_ECC_AGGR_RXMEM	02A7 1008h

Figure 18-280. MMCSD12_RXECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-683. MMCSD12_RXECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

Table 18-684. Register Call Summary for MMCSD12_RXECC_VECTOR

MMCSD1 / MMCSD2 RX RAM ECC Aggregator Registers

- [MMCSD12_RXECC_VECTOR Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)
- [MMCSD1 / MMCSD2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.3 MMCS12_RXECC_STAT Register (Offset = Ch) [reset = 1h]

MMCS12_RXECC_STAT is shown in Figure 18-281 and described in Table 18-686.

Return to [Summary Table](#).

Misc Status Register

Table 18-685. MMCS12_RXECC_STAT Instances

Instance	Physical Address
MMCS12_ECC_AGGREGATOR_RXMEM	02A2 600Ch
MMCS12_ECC_AGGREGATOR_RXMEM	02A7 100Ch

Figure 18-281. MMCS12_RXECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												NUM_RAM																			
R-0h												R-1h																			

LEGEND: R = Read Only; -n = value after reset

Table 18-686. MMCS12_RXECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAM	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

Table 18-687. Register Call Summary for MMCS12_RXECC_STAT

MMCS12 / MMCS12 RX RAM ECC Aggregator Registers

- [MMCS12_RXECC_STAT Register \(Offset = Ch\) \[reset = 1h\]: \[0\]](#)
- [MMCS12 / MMCS12 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.4 MMCSD12_RXECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MMCSD12_RXECC_SEC_EOI_REG is shown in [Figure 18-282](#) and described in [Table 18-689](#).

Return to [Summary Table](#).

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 18-688. MMCSD12_RXECC_SEC_EOI_REG
Instances**

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	02A2 603Ch
MMCSD2_ECC_AGGR_RXMEM	02A7 103Ch

Figure 18-282. MMCSD12_RXECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-689. MMCSD12_RXECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	SEC EOI

Table 18-690. Register Call Summary for MMCSD12_RXECC_SEC_EOI_REG

MMCSD1 / MMCSD2 RX RAM ECC Aggregator Registers

- [MMCSD12_RXECC_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)
- [MMCSD1 / MMCSD2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.5 MMCSDB12_RXECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MMCSDB12_RXECC_SEC_STATUS_REG0 is shown in Figure 18-283 and described in Table 18-692.

Return to [Summary Table](#).

SEC Interrupt Status Register 0

Table 18-691.
MMCSDB12_RXECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
MMCSDB1_ECC_AGGR_RXMEM	02A2 6040h
MMCSDB2_ECC_AGGR_RXMEM	02A7 1040h

Figure 18-283. MMCSDB12_RXECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-692. MMCSDB12_RXECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_PEND	R/W1S	0h	Interrupt Pending Status for rxmem_pend

Table 18-693. Register Call Summary for MMCSDB12_RXECC_SEC_STATUS_REG0

MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

- [MMCSDB12_RXECC_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.6 MMCSDB12_RXECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MMCSDB12_RXECC_SEC_ENABLE_SET_REG0 is shown in [Figure 18-284](#) and described in [Table 18-695](#).

Return to [Summary Table](#).

SEC Interrupt Enable Set Register 0

Table 18-694.
MMCSDB12_RXECC_SEC_ENABLE_SET_REG0
Instances

Instance	Physical Address
MMCSDB1_ECC_AGR_RXMEM	02A2 6080h
MMCSDB2_ECC_AGR_RXMEM	02A7 1080h

Figure 18-284. MMCSDB12_RXECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENAB LE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-695. MMCSDB12_RXECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for rxmem_pend

Table 18-696. Register Call Summary for MMCSDB12_RXECC_SEC_ENABLE_SET_REG0

MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

- [MMCSDB12_RXECC_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.7 MMCSDB12_RXECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MMCSDB12_RXECC_SEC_ENABLE_CLR_REG0 is shown in Figure 18-285 and described in Table 18-698.

Return to [Summary Table](#).

SEC Interrupt Enable Clear Register 0

Table 18-697.
MMCSDB12_RXECC_SEC_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MMCSDB1_ECC_AGR_RXMEM	02A2 60C0h
MMCSDB2_ECC_AGR_RXMEM	02A7 10C0h

Figure 18-285. MMCSDB12_RXECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENAB LE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-698. MMCSDB12_RXECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for rxmem_pend

Table 18-699. Register Call Summary for MMCSDB12_RXECC_SEC_ENABLE_CLR_REG0

MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

- [MMCSDB12_RXECC_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.8 MMCSD12_RXECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MMCSD12_RXECC_DED_EOI_REG is shown in [Figure 18-286](#) and described in [Table 18-701](#).

Return to [Summary Table](#).

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 18-700. MMCSD12_RXECC_DED_EOI_REG
Instances**

Instance	Physical Address
MMCSD1_ECC_AGGR_RXMEM	02A2 613Ch
MMCSD2_ECC_AGGR_RXMEM	02A7 113Ch

Figure 18-286. MMCSD12_RXECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-701. MMCSD12_RXECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	DED EOI

Table 18-702. Register Call Summary for MMCSD12_RXECC_DED_EOI_REG

MMCSD1 / MMCSD2 RX RAM ECC Aggregator Registers

- [MMCSD12_RXECC_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = 0h\]: \[0\]](#)
- [MMCSD1 / MMCSD2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.9 MMCSDB12_RXECC_DEB_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MMCSDB12_RXECC_DEB_STATUS_REG0 is shown in Figure 18-287 and described in Table 18-704.

Return to [Summary Table](#).

DEB Interrupt Status Register 0

Table 18-703.
MMCSDB12_RXECC_DEB_STATUS_REG0 Instances

Instance	Physical Address
MMCSDB1_ECC_AGGR_RXMEM	02A2 6140h
MMCSDB2_ECC_AGGR_RXMEM	02A7 1140h

Figure 18-287. MMCSDB12_RXECC_DEB_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-704. MMCSDB12_RXECC_DEB_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_PEND	R/W1S	0h	Interrupt Pending Status for rxmem_pend

Table 18-705. Register Call Summary for MMCSDB12_RXECC_DEB_STATUS_REG0

MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

- [MMCSDB12_RXECC_DEB_STATUS_REG0 Register \(Offset = 140h\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.10 MMCS D12_RXECC_DE D_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MMCS D12_RXECC_DE D_ENABLE_SET_REG0 is shown in Figure 18-288 and described in Table 18-707.

Return to [Summary Table](#).

DE D Interrupt Enable Set Register 0

Table 18-706.
MMCS D12_RXECC_DE D_ENABLE_SET_REG0
Instances

Instance	Physical Address
MMCS D1_ECC_A GGR_RXMEM	02A2 6180h
MMCS D2_ECC_A GGR_RXMEM	02A7 1180h

Figure 18-288. MMCS D12_RXECC_DE D_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENAB LE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-707. MMCS D12_RXECC_DE D_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for rxmem_pend

Table 18-708. Register Call Summary for MMCS D12_RXECC_DE D_ENABLE_SET_REG0

MMCS D1 / MMCS D2 RX RAM ECC Aggregator Registers

- [MMCS D12_RXECC_DE D_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = 0h\]: \[0\]](#)
- [MMCS D1 / MMCS D2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.11 MMCSd12_RXECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MMCSd12_RXECC_DED_ENABLE_CLR_REG0 is shown in Figure 18-289 and described in Table 18-710.

Return to [Summary Table](#).

DED Interrupt Enable Clear Register 0

Table 18-709.
MMCSd12_RXECC_DED_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MMCSd1_ECC_Aggr_RxMem	02A2 61C0h
MMCSd2_ECC_Aggr_RxMem	02A7 11C0h

Figure 18-289. MMCSd12_RXECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RXMEM_ENABLE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-710. MMCSd12_RXECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for rxmem_pend

Table 18-711. Register Call Summary for MMCSd12_RXECC_DED_ENABLE_CLR_REG0

MMCSd1 / MMCSd2 RX RAM ECC Aggregator Registers

- [MMCSd12_RXECC_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = 0h\]: \[0\]](#)
- [MMCSd1 / MMCSd2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.12 MMCSd12_RXECC_Aggr_Enable_Set Register (Offset = 200h) [reset = 0h]

MMCSd12_RXECC_Aggr_Enable_Set is shown in [Figure 18-290](#) and described in [Table 18-713](#).

Return to [Summary Table](#).

Aggregator Interrupt Enable Set Register

Table 18-712.
MMCSd12_RXECC_Aggr_Enable_Set Instances

Instance	Physical Address
MMCSd1_ECC_Aggr_RXMEM	02A2 6200h
MMCSd2_ECC_Aggr_RXMEM	02A7 1200h

Figure 18-290. MMCSd12_RXECC_Aggr_Enable_Set Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-713. MMCSd12_RXECC_Aggr_Enable_Set Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

Table 18-714. Register Call Summary for MMCSd12_RXECC_Aggr_Enable_Set

MMCSd1 / MMCSd2 RX RAM ECC Aggregator Registers

- [MMCSd12_RXECC_Aggr_Enable_Set Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)
- [MMCSd1 / MMCSd2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.13 MMCSDB12_RXECC_AGBR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MMCSDB12_RXECC_AGBR_ENABLE_CLR is shown in Figure 18-291 and described in Table 18-716.

Return to [Summary Table](#).

Aggregator Interrupt Enable Clear Register

Table 18-715.
MMCSDB12_RXECC_AGBR_ENABLE_CLR Instances

Instance	Physical Address
MMCSDB1_ECC_AGBR_RXMEM	02A2 6204h
MMCSDB2_ECC_AGBR_RXMEM	02A7 1204h

Figure 18-291. MMCSDB12_RXECC_AGBR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-716. MMCSDB12_RXECC_AGBR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

Table 18-717. Register Call Summary for MMCSDB12_RXECC_AGBR_ENABLE_CLR

MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

- [MMCSDB12_RXECC_AGBR_ENABLE_CLR Register \(Offset = 204h\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.14 MMCSDB12_RXECC_AGBR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MMCSDB12_RXECC_AGBR_STATUS_SET is shown in Figure 18-292 and described in Table 18-719.

Return to [Summary Table](#).

Aggregator Interrupt Status Set Register

Table 18-718.
MMCSDB12_RXECC_AGBR_STATUS_SET Instances

Instance	Physical Address
MMCSDB1_ECC_AGBR_RXMEM	02A2 6208h
MMCSDB2_ECC_AGBR_RXMEM	02A7 1208h

Figure 18-292. MMCSDB12_RXECC_AGBR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 18-719. MMCSDB12_RXECC_AGBR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

Table 18-720. Register Call Summary for MMCSDB12_RXECC_AGBR_STATUS_SET

MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

- [MMCSDB12_RXECC_AGBR_STATUS_SET Register \(Offset = 208h\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.7.15 MMCSDB12_RXECC_AGBR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MMCSDB12_RXECC_AGBR_STATUS_CLR is shown in Figure 18-293 and described in Table 18-722.

Return to [Summary Table](#).

Aggregator Interrupt Status Clear Register

Table 18-721.
MMCSDB12_RXECC_AGBR_STATUS_CLR Instances

Instance	Physical Address
MMCSDB1_ECC_AGBR_RXMEM	02A2 620Ch
MMCSDB2_ECC_AGBR_RXMEM	02A7 120Ch

Figure 18-293. MMCSDB12_RXECC_AGBR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 18-722. MMCSDB12_RXECC_AGBR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

Table 18-723. Register Call Summary for MMCSDB12_RXECC_AGBR_STATUS_CLR

MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers

- [MMCSDB12_RXECC_AGBR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 RX RAM ECC Aggregator Registers: \[0\]](#)

18.8 MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

Table 18-725 lists the memory-mapped registers for the MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator. All register offset addresses not listed in Table 18-725 should be considered as reserved locations and the register contents should not be modified.

Table 18-724. MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Instances

Instance	Base Address
MMCSDB1_ECC_AGR_TXMEM	02A2 7000h
MMCSDB2_ECC_AGR_TXMEM	02A7 0000h

Table 18-725. MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

Offset	Acronym	Register Name	MMCSDB1_ECC_AGR_TXMEM Physical Address	MMCSDB2_ECC_AGR_TXMEM Physical Address
0h	MMCSDB12_TXECC_REV	Aggregator Revision Register	02A2 7000h	02A7 0000h
8h	MMCSDB12_TXECC_VECTOR	ECC Vector Register	02A2 7008h	02A7 0008h
Ch	MMCSDB12_TXECC_STAT	Misc Status Register	02A2 700Ch	02A7 000Ch
3Ch	MMCSDB12_TXECC_SEC_EOI_REG	SEC EOI Register	02A2 703Ch	02A7 003Ch
40h	MMCSDB12_TXECC_SEC_STATUS_REG0	SEC Interrupt Status Register 0	02A2 7040h	02A7 0040h
80h	MMCSDB12_TXECC_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	02A2 7080h	02A7 0080h
C0h	MMCSDB12_TXECC_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	02A2 70C0h	02A7 00C0h
13Ch	MMCSDB12_TXECC_DED_EOI_REG	DED EOI Register	02A2 713Ch	02A7 013Ch
140h	MMCSDB12_TXECC_DED_STATUS_REG0	DED Interrupt Status Register 0	02A2 7140h	02A7 0140h
180h	MMCSDB12_TXECC_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	02A2 7180h	02A7 0180h
1C0h	MMCSDB12_TXECC_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	02A2 71C0h	02A7 01C0h
200h	MMCSDB12_TXECC_AGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	02A2 7200h	02A7 0200h
204h	MMCSDB12_TXECC_AGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	02A2 7204h	02A7 0204h
208h	MMCSDB12_TXECC_AGR_STATUS_SET	Aggregator Interrupt Status Set Register	02A2 7208h	02A7 0208h
20Ch	MMCSDB12_TXECC_AGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	02A2 720Ch	02A7 020Ch

18.8.1 MMCS D12_TXECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MMCS D12_TXECC_REV is shown in [Figure 18-294](#) and described in [Table 18-727](#).

Return to [Summary Table](#).

Aggregator Revision Register

Revision parameters.

Table 18-726. MMCS D12_TXECC_REV Instances

Instance	Physical Address
MMCS D1_ECC_AGGR_TXMEM	02A2 7000h
MMCS D2_ECC_AGGR_TXMEM	02A7 0000h

Figure 18-294. MMCS D12_TXECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME			BU		MODULE_ID										
R-1h			R-2h		R-6A0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 18-727. MMCS D12_TXECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

Table 18-728. Register Call Summary for MMCS D12_TXECC_REV

MMCS D1 / MMCS D2 TX RAM ECC Aggregator Registers

- [MMCS D1 / MMCS D2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS D12_TXECC_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]: \[0\]](#)

18.8.2 MMCSDB12_TXECC_VECTOR Register (Offset = 8h) [reset = 0h]

MMCSDB12_TXECC_VECTOR is shown in Figure 18-295 and described in Table 18-730.

Return to [Summary Table](#).

ECC Vector Register

Table 18-729. MMCSDB12_TXECC_VECTOR Instances

Instance	Physical Address
MMCSDB1_ECC_AGR_TXMEM	02A2 7008h
MMCSDB2_ECC_AGR_TXMEM	02A7 0008h

Figure 18-295. MMCSDB12_TXECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-730. MMCSDB12_TXECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial ECC interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

Table 18-731. Register Call Summary for MMCSDB12_TXECC_VECTOR

MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

- [MMCSDB12_TXECC_VECTOR Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers: \[0\]](#)

18.8.3 MMCSDB12_TXECC_STAT Register (Offset = Ch) [reset = 1h]

MMCSDB12_TXECC_STAT is shown in Figure 18-296 and described in Table 18-733.

Return to [Summary Table](#).

Misc Status Register

Table 18-732. MMCSDB12_TXECC_STAT Instances

Instance	Physical Address
MMCSDB1_ECC_AGGR_TXMEM	02A2 700Ch
MMCSDB2_ECC_AGGR_TXMEM	02A7 000Ch

Figure 18-296. MMCSDB12_TXECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																	NUM_RAMs														
R-0h																	R-1h														

LEGEND: R = Read Only; -n = value after reset

Table 18-733. MMCSDB12_TXECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMs	R	1h	Indicates the number of RAMs serviced by the ECC aggregator.

Table 18-734. Register Call Summary for MMCSDB12_TXECC_STAT

MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

- [MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSDB12_TXECC_STAT Register \(Offset = Ch\) \[reset = 1h\]: \[0\]](#)

18.8.4 MMCSD12_TXECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MMCSD12_TXECC_SEC_EOI_REG is shown in [Figure 18-297](#) and described in [Table 18-736](#).

Return to [Summary Table](#).

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 18-735. MMCSD12_TXECC_SEC_EOI_REG
Instances**

Instance	Physical Address
MMCSD1_ECC_AGGREGATOR_TXMEM	02A2 703Ch
MMCSD2_ECC_AGGREGATOR_TXMEM	02A7 003Ch

Figure 18-297. MMCSD12_TXECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-736. MMCSD12_TXECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	SEC EOI

Table 18-737. Register Call Summary for MMCSD12_TXECC_SEC_EOI_REG

MMCSD1 / MMCSD2 TX RAM ECC Aggregator Registers

- [MMCSD1 / MMCSD2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSD12_TXECC_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)

18.8.5 MMCSDB12_TXECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MMCSDB12_TXECC_SEC_STATUS_REG0 is shown in Figure 18-298 and described in Table 18-739.

Return to [Summary Table](#).

SEC Interrupt Status Register 0

Table 18-738.
MMCSDB12_TXECC_SEC_STATUS_REG0 Instances

Instance	Physical Address
MMCSDB1_ECC_AGGR_TXMEM	02A2 7040h
MMCSDB2_ECC_AGGR_TXMEM	02A7 0040h

Figure 18-298. MMCSDB12_TXECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-739. MMCSDB12_TXECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_PEND	R/W1S	0h	Interrupt Pending Status for txmem_pend

Table 18-740. Register Call Summary for MMCSDB12_TXECC_SEC_STATUS_REG0

MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

- [MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSDB12_TXECC_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = 0h\]: \[0\]](#)

18.8.6 MMCSDB12_TXECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MMCSDB12_TXECC_SEC_ENABLE_SET_REG0 is shown in [Figure 18-299](#) and described in [Table 18-742](#).

Return to [Summary Table](#).

SEC Interrupt Enable Set Register 0

Table 18-741.
MMCSDB12_TXECC_SEC_ENABLE_SET_REG0
Instances

Instance	Physical Address
MMCSDB1_ECC_AGR_TXMEM	02A2 7080h
MMCSDB2_ECC_AGR_TXMEM	02A7 0080h

Figure 18-299. MMCSDB12_TXECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENABLE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-742. MMCSDB12_TXECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for txmem_pend

Table 18-743. Register Call Summary for MMCSDB12_TXECC_SEC_ENABLE_SET_REG0

MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

- [MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSDB12_TXECC_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = 0h\]: \[0\]](#)

18.8.7 MMCSDB12_TXECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MMCSDB12_TXECC_SEC_ENABLE_CLR_REG0 is shown in Figure 18-300 and described in Table 18-745.

Return to [Summary Table](#).

SEC Interrupt Enable Clear Register 0

Table 18-744.
MMCSDB12_TXECC_SEC_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MMCSDB1_ECC_AGR_TXMEM	02A2 70C0h
MMCSDB2_ECC_AGR_TXMEM	02A7 00C0h

Figure 18-300. MMCSDB12_TXECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENAB LE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-745. MMCSDB12_TXECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for txmem_pend

Table 18-746. Register Call Summary for MMCSDB12_TXECC_SEC_ENABLE_CLR_REG0

MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

- [MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSDB12_TXECC_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = 0h\]: \[0\]](#)

18.8.8 MMCSD12_TXECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MMCSD12_TXECC_DED_EOI_REG is shown in [Figure 18-301](#) and described in [Table 18-748](#).

Return to [Summary Table](#).

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 18-747. MMCSD12_TXECC_DED_EOI_REG
Instances**

Instance	Physical Address
MMCSD1_ECC_AGGREGATOR_TXMEM	02A2 713Ch
MMCSD2_ECC_AGGREGATOR_TXMEM	02A7 013Ch

Figure 18-301. MMCSD12_TXECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-748. MMCSD12_TXECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	DED EOI

Table 18-749. Register Call Summary for MMCSD12_TXECC_DED_EOI_REG

MMCSD1 / MMCSD2 TX RAM ECC Aggregator Registers

- [MMCSD1 / MMCSD2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSD12_TXECC_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = 0h\]: \[0\]](#)

18.8.9 MMCSDB12_TXECC_DEB_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MMCSDB12_TXECC_DEB_STATUS_REG0 is shown in Figure 18-302 and described in Table 18-751.

Return to [Summary Table](#).

DEB Interrupt Status Register 0

Table 18-750.
MMCSDB12_TXECC_DEB_STATUS_REG0 Instances

Instance	Physical Address
MMCSDB1_ECC_AGGR_TXMEM	02A2 7140h
MMCSDB2_ECC_AGGR_TXMEM	02A7 0140h

Figure 18-302. MMCSDB12_TXECC_DEB_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_PEND
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-751. MMCSDB12_TXECC_DEB_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_PEND	R/W1S	0h	Interrupt Pending Status for txmem_pend

Table 18-752. Register Call Summary for MMCSDB12_TXECC_DEB_STATUS_REG0

MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

- [MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSDB12_TXECC_DEB_STATUS_REG0 Register \(Offset = 140h\) \[reset = 0h\]: \[0\]](#)

18.8.10 MMCS D12_TXECC_DE D_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MMCS D12_TXECC_DE D_ENABLE_SET_REG0 is shown in Figure 18-303 and described in Table 18-754.

Return to [Summary Table](#).

DE D Interrupt Enable Set Register 0

Table 18-753.
MMCS D12_TXECC_DE D_ENABLE_SET_REG0
Instances

Instance	Physical Address
MMCS D1_ECC_A GGR_TXMEM	02A2 7180h
MMCS D2_ECC_A GGR_TXMEM	02A7 0180h

Figure 18-303. MMCS D12_TXECC_DE D_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENAB LE_SET
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-754. MMCS D12_TXECC_DE D_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for txmem_pend

Table 18-755. Register Call Summary for MMCS D12_TXECC_DE D_ENABLE_SET_REG0

MMCS D1 / MMCS D2 TX RAM ECC Aggregator Registers

- [MMCS D1 / MMCS D2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCS D12_TXECC_DE D_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = 0h\]: \[0\]](#)

18.8.11 MMCSd12_TXECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MMCSd12_TXECC_DED_ENABLE_CLR_REG0 is shown in Figure 18-304 and described in Table 18-757.

Return to [Summary Table](#).

DED Interrupt Enable Clear Register 0

Table 18-756.
MMCSd12_TXECC_DED_ENABLE_CLR_REG0
Instances

Instance	Physical Address
MMCSd1_ECC_Aggr_TXMEM	02A2 71C0h
MMCSd2_ECC_Aggr_TXMEM	02A7 01C0h

Figure 18-304. MMCSd12_TXECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TXMEM_ENAB LE_CLR
R-0h							R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-757. MMCSd12_TXECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TXMEM_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for txmem_pend

Table 18-758. Register Call Summary for MMCSd12_TXECC_DED_ENABLE_CLR_REG0

MMCSd1 / MMCSd2 TX RAM ECC Aggregator Registers

- [MMCSd1 / MMCSd2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSd12_TXECC_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = 0h\]: \[0\]](#)

18.8.12 MMCSDB12_TXECC_AGBR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MMCSDB12_TXECC_AGBR_ENABLE_SET is shown in Figure 18-305 and described in Table 18-760.

Return to [Summary Table](#).

Aggregator Interrupt Enable Set Register

Table 18-759.
MMCSDB12_TXECC_AGBR_ENABLE_SET Instances

Instance	Physical Address
MMCSDB1_ECC_AGBR_TXMEM	02A2 7200h
MMCSDB2_ECC_AGBR_TXMEM	02A7 0200h

Figure 18-305. MMCSDB12_TXECC_AGBR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-760. MMCSDB12_TXECC_AGBR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial ECC interface timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

Table 18-761. Register Call Summary for MMCSDB12_TXECC_AGBR_ENABLE_SET

MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

- [MMCSDB12_TXECC_AGBR_ENABLE_SET Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)
- [MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers: \[0\]](#)

18.8.13 MMCSd12_TXECC_Aggr_Enable_CLR Register (Offset = 204h) [reset = 0h]

MMCSd12_TXECC_Aggr_Enable_CLR is shown in Figure 18-306 and described in Table 18-763.

Return to [Summary Table](#).

Aggregator Interrupt Enable Clear Register

Table 18-762.
MMCSd12_TXECC_Aggr_Enable_CLR Instances

Instance	Physical Address
MMCSd1_ECC_Aggr_TXMEM	02A2 7204h
MMCSd2_ECC_Aggr_TXMEM	02A7 0204h

Figure 18-306. MMCSd12_TXECC_Aggr_Enable_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-763. MMCSd12_TXECC_Aggr_Enable_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial ECC interface timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

Table 18-764. Register Call Summary for MMCSd12_TXECC_Aggr_Enable_CLR

MMCSd1 / MMCSd2 TX RAM ECC Aggregator Registers

- [MMCSd1 / MMCSd2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSd12_TXECC_Aggr_Enable_CLR Register \(Offset = 204h\) \[reset = 0h\]: \[0\]](#)

18.8.14 MMCSDB12_TXECC_AGBR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MMCSDB12_TXECC_AGBR_STATUS_SET is shown in Figure 18-307 and described in Table 18-766.

Return to [Summary Table](#).

Aggregator Interrupt Status Set Register

Table 18-765.
MMCSDB12_TXECC_AGBR_STATUS_SET Instances

Instance	Physical Address
MMCSDB1_ECC_AGBR_TXMEM	02A2 7208h
MMCSDB2_ECC_AGBR_TXMEM	02A7 0208h

Figure 18-307. MMCSDB12_TXECC_AGBR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 18-766. MMCSDB12_TXECC_AGBR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial ECC interface timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

Table 18-767. Register Call Summary for MMCSDB12_TXECC_AGBR_STATUS_SET

MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers

- [MMCSDB1 / MMCSDB2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSDB12_TXECC_AGBR_STATUS_SET Register \(Offset = 208h\) \[reset = 0h\]: \[0\]](#)

18.8.15 MMCSd12_TXECC_Aggr_Status_Clr Register (Offset = 20Ch) [reset = 0h]

MMCSd12_TXECC_Aggr_Status_Clr is shown in Figure 18-308 and described in Table 18-769.

Return to [Summary Table](#).

Aggregator Interrupt Status Clear Register

Table 18-768.
MMCSd12_TXECC_Aggr_Status_Clr Instances

Instance	Physical Address
MMCSd1_ECC_Aggr_TxMem	02A2 720Ch
MMCSd2_ECC_Aggr_TxMem	02A7 020Ch

Figure 18-308. MMCSd12_TXECC_Aggr_Status_Clr Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 18-769. MMCSd12_TXECC_Aggr_Status_Clr Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial ECC interface timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

Table 18-770. Register Call Summary for MMCSd12_TXECC_Aggr_Status_Clr

MMCSd1 / MMCSd2 TX RAM ECC Aggregator Registers

- [MMCSd1 / MMCSd2 TX RAM ECC Aggregator Registers: \[0\]](#)
- [MMCSd12_TXECC_Aggr_Status_Clr Register \(Offset = 20Ch\) \[reset = 0h\]: \[0\]](#)

19 UFS Registers

19.1 UFS0_HCLK_ECC_AGGR_CFG Registers

Table 19-2 lists the memory-mapped registers for the UFS0_HCLK_ECC_AGGR_CFG registers. All register offset addresses not listed in Table 19-2 should be considered as reserved locations and the register contents should not be modified.

**Table 19-1. UFS0_HCLK_ECC_AGGR_CFG
Instances**

Instance	Base Address
UFS0_HCLK_ECC_AGGR_CFG	02A2 8000h

Table 19-2. UFS0_HCLK_ECC_AGGR_CFG Registers

Offset	Acronym	Register Name	UFS0_HCLK_ECC_AGGR_CFG Physical Address
0h	UFS_REV	Aggregator Revision Register	02A2 8000h
8h	UFS_VECTOR	ECC Vector Register	02A2 8008h
Ch	UFS_STAT	Misc Status Register	02A2 800Ch
10h + formula	UFS_RESERVED_SVBUS_y	Reserved Area For Serial VBUS Registers	02A2 8010h + formula
3Ch	UFS_SEC_EOI_REG	SEC End Of Interrupt (EOI) Register	02A2 803Ch
40h	UFS_SEC_STATUS_REG0	SEC Interrupt Status Register 0	02A2 8040h
80h	UFS_SEC_ENABLE_SET_REG0	SEC Interrupt Enable Set Register 0	02A2 8080h
C0h	UFS_SEC_ENABLE_CLR_REG0	SEC Interrupt Enable Clear Register 0	02A2 80C0h
13Ch	UFS_DED_EOI_REG	DED End Of Interrupt (EOI) Register	02A2 813Ch
140h	UFS_DED_STATUS_REG0	DED Interrupt Status Register 0	02A2 8140h
180h	UFS_DED_ENABLE_SET_REG0	DED Interrupt Enable Set Register 0	02A2 8180h
1C0h	UFS_DED_ENABLE_CLR_REG0	DED Interrupt Enable Clear Register 0	02A2 81C0h
200h	UFS_AGGR_ENABLE_SET	Aggregator Interrupt Enable Set Register	02A2 8200h
204h	UFS_AGGR_ENABLE_CLR	Aggregator Interrupt Enable Clear Register	02A2 8204h
208h	UFS_AGGR_STATUS_SET	Aggregator Interrupt Status Set Register	02A2 8208h
20Ch	UFS_AGGR_STATUS_CLR	Aggregator Interrupt Status Clear Register	02A2 820Ch

19.1.1 UFS_REV Register (Offset = 0h) [reset = 66A0EA00h]

UFS_REV is shown in [Figure 19-1](#) and described in [Table 19-4](#).

Return to [Summary Table](#).

Aggregator Revision Register

Revision parameters.

Table 19-3. UFS_REV Instances

Instance	Physical Address
UFS0	02A2 8000h

Figure 19-1. UFS_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 19-4. UFS_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL Version
10-8	REVMAJ	R	2h	Major Version
7-6	CUSTOM	R	0h	Custom Version
5-0	REVMIN	R	0h	Minor Version

Table 19-5. Register Call Summary for UFS_REV

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.2 UFS_VECTOR Register (Offset = 8h) [reset = 0h]

UFS_VECTOR is shown in Figure 19-2 and described in Table 19-7.

Return to [Summary Table](#).

ECC Vector Register

Table 19-6. UFS_VECTOR Instances

Instance	Physical Address
UFS0	02A2 8008h

Figure 19-2. UFS_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-7. UFS_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Read Done Status to indicate if read on the serial VBUS interface is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read Address
15	RD_SVBUS	R/W1S	0h	Read Trigger Write 1h to trigger a read on the serial VBUS interface.
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	ECC RAM ID Value written to select the corresponding ECC RAM for control or status.

Table 19-8. Register Call Summary for UFS_VECTOR

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_VECTOR Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.3 UFS_STAT Register (Offset = Ch) [reset = 14h]

UFS_STAT is shown in [Figure 19-3](#) and described in [Table 19-10](#).

Return to [Summary Table](#).

Misc Status Register

Table 19-9. UFS_STAT Instances

Instance	Physical Address
UFS0	02A2 800Ch

Figure 19-3. UFS_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RESERVED																					NUM_RAMs															
R-0h																					R-14h															

LEGEND: R = Read Only; -n = value after reset

Table 19-10. UFS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMs	R	14h	Number of RAMs Indicates the number of RAMs serviced by the ECC Aggregator.

Table 19-11. Register Call Summary for UFS_STAT

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_STAT Register \(Offset = Ch\) \[reset = 14h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.4 UFS_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

UFS_RESERVED_SVBUS_y is shown in Figure 19-4 and described in Table 19-13.

Return to [Summary Table](#).

Reserved Area For Serial VBUS Registers

Offset = 10h + (y × 4h); where y = 0h to 7h;

Table 19-12. UFS_RESERVED_SVBUS_y Instances

Instance	Physical Address
UFS0	02A2 8010h + formula

Figure 19-4. UFS_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-13. UFS_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS Register Data

Table 19-14. Register Call Summary for UFS_RESERVED_SVBUS_y

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_RESERVED_SVBUS_y Register \(Offset = 10h + formula\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.5 UFS_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

UFS_SEC_EOI_REG is shown in [Figure 19-5](#) and described in [Table 19-16](#).

Return to [Summary Table](#).

SEC End Of Interrupt (EOI) Register

The SEC End Of Interrupt (EOI) register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the SEC End Of Interrupt (EOI) register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the SEC End Of Interrupt (EOI) register is not functional and must not be used.

Table 19-15. UFS_SEC_EOI_REG Instances

Instance	Physical Address
UFS0	02A2 803Ch

Figure 19-5. UFS_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-16. UFS_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	End Of Interrupt (EOI)

Table 19-17. Register Call Summary for UFS_SEC_EOI_REG

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.6 UFS_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

UFS_SEC_STATUS_REG0 is shown in Figure 19-6 and described in Table 19-19.

Return to [Summary Table](#).

SEC Interrupt Status Register 0

Table 19-18. UFS_SEC_STATUS_REG0 Instances

Instance	Physical Address
UFS0	02A2 8040h

Figure 19-6. UFS_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC_PEN D	MEM_CMU1_S VBUS_PEND	MEM_RTT_SV BUS_PEND	MEM_WDC_SV BUS_PEND
R-0h				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
MEM_RDF_SV BUS_PEND	MEM_CMU3_S VBUS_PEND	MEM_TMU_SV BUS_PEND	MEM_WDF_SV BUS_PEND	MEM_CMU5_S VBUS_PEND	MEM_CCI_SVB US_PEND	MEM_CMU4_S VBUS_PEND	MEM_CMU2_S VBUS_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
MEM_ID_SVBUS S_PEND	MEM_CIP_SVB US_PEND	MEM_RDC_SV BUS_PEND	MEM_CMU6_S VBUS_PEND	MEM_WDCM SVBUS_PEND	MEM_CMU7_S VBUS_PEND	MEM_WDCF_S VBUS_PEND	MEM_RX_TC0 _SVBUS_PEN D
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-19. UFS_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for ramecc_pend
18	MEM_CMU1_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu1_svbus_pend
17	MEM_RTT_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_rtt_svbus_pend
16	MEM_WDC_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdc_svbus_pend
15	MEM_RDF_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_rdf_svbus_pend
14	MEM_CMU3_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu3_svbus_pend
13	MEM_TMU_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_tmu_svbus_pend
12	MEM_WDF_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdf_svbus_pend
11	MEM_CMU5_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu5_svbus_pend
10	MEM_CCI_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cci_svbus_pend
9	MEM_CMU4_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu4_svbus_pend

Table 19-19. UFS_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MEM_CMU2_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu2_svbus_pend
7	MEM_ID_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_id_svbus_pend
6	MEM_CIP_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cip_svbus_pend
5	MEM_RDC_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_rdc_svbus_pend
4	MEM_CMU6_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu6_svbus_pend
3	MEM_WDCM_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdcm_svbus_pend
2	MEM_CMU7_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu7_svbus_pend
1	MEM_WDCF_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdcf_svbus_pend
0	MEM_RX_TC0_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_rx_tc0_svbus_pend

Table 19-20. Register Call Summary for UFS_SEC_STATUS_REG0

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.7 UFS_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

UFS_SEC_ENABLE_SET_REG0 is shown in Figure 19-7 and described in Table 19-22.

Return to [Summary Table](#).

SEC Interrupt Enable Set Register 0

Table 19-21. UFS_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
UFS0	02A2 8080h

Figure 19-7. UFS_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC_ENABLE_SET	MEM_CMU1_SVBUS_ENABLE_SET	MEM_RTT_SVBUS_ENABLE_SET	MEM_WDC_SVBUS_ENABLE_SET
R-0h				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
MEM_RDF_SVBUS_ENABLE_SET	MEM_CMU3_SVBUS_ENABLE_SET	MEM_TMU_SVBUS_ENABLE_SET	MEM_WDF_SVBUS_ENABLE_SET	MEM_CMU5_SVBUS_ENABLE_SET	MEM_CCI_SVBUS_ENABLE_SET	MEM_CMU4_SVBUS_ENABLE_SET	MEM_CMU2_SVBUS_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
MEM_ID_SVBUS_ENABLE_SET	MEM_CIP_SVBUS_ENABLE_SET	MEM_RDC_SVBUS_ENABLE_SET	MEM_CMU6_SVBUS_ENABLE_SET	MEM_WDCM_SVBUS_ENABLE_SET	MEM_CMU7_SVBUS_ENABLE_SET	MEM_WDCF_SVBUS_ENABLE_SET	MEM_RX_TC0_SVBUS_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-22. UFS_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for ramecc_pend
18	MEM_CMU1_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu1_svbus_pend
17	MEM_RTT_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_rtt_svbus_pend
16	MEM_WDC_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_wdc_svbus_pend
15	MEM_RDF_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_rdf_svbus_pend
14	MEM_CMU3_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu3_svbus_pend
13	MEM_TMU_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_tmu_svbus_pend
12	MEM_WDF_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_wdf_svbus_pend
11	MEM_CMU5_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu5_svbus_pend

Table 19-22. UFS_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MEM_CCI_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cci_svbus_pend
9	MEM_CMU4_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu4_svbus_pend
8	MEM_CMU2_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu2_svbus_pend
7	MEM_ID_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_id_svbus_pend
6	MEM_CIP_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cip_svbus_pend
5	MEM_RDC_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_rdc_svbus_pend
4	MEM_CMU6_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu6_svbus_pend
3	MEM_WDCM_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_wdcm_svbus_pend
2	MEM_CMU7_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu7_svbus_pend
1	MEM_WDCF_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_wdcf_svbus_pend
0	MEM_RX_TC0_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_rx_tc0_svbus_pend

Table 19-23. Register Call Summary for UFS_SEC_ENABLE_SET_REG0

UFS0_HCLK_ECC_AGGREGATE_CFG Registers

- [UFS_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGREGATE_CFG Registers: \[0\]](#)

19.1.8 UFS_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

UFS_SEC_ENABLE_CLR_REG0 is shown in Figure 19-8 and described in Table 19-25.

Return to [Summary Table](#).

SEC Interrupt Enable Clear Register 0

Table 19-24. UFS_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
UFS0	02A2 80C0h

Figure 19-8. UFS_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC_ENABLE_CLR	MEM_CMU1_SVBUS_ENABLE_CLR	MEM_RTT_SVBUS_ENABLE_CLR	MEM_WDC_SVBUS_ENABLE_CLR
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
MEM_RDF_SVBUS_ENABLE_CLR	MEM_CMU3_SVBUS_ENABLE_CLR	MEM_TMU_SVBUS_ENABLE_CLR	MEM_WDF_SVBUS_ENABLE_CLR	MEM_CMU5_SVBUS_ENABLE_CLR	MEM_CCI_SVBUS_ENABLE_CLR	MEM_CMU4_SVBUS_ENABLE_CLR	MEM_CMU2_SVBUS_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
MEM_ID_SVBUS_ENABLE_CLR	MEM_CIP_SVBUS_ENABLE_CLR	MEM_RDC_SVBUS_ENABLE_CLR	MEM_CMU6_SVBUS_ENABLE_CLR	MEM_WDCM_SVBUS_ENABLE_CLR	MEM_CMU7_SVBUS_ENABLE_CLR	MEM_WDCF_SVBUS_ENABLE_CLR	MEM_RX_TC0_SVBUS_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-25. UFS_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for ramecc_pend
18	MEM_CMU1_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu1_svbus_pend
17	MEM_RTT_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_rtt_svbus_pend
16	MEM_WDC_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_wdc_svbus_pend
15	MEM_RDF_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_rdf_svbus_pend
14	MEM_CMU3_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu3_svbus_pend
13	MEM_TMU_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_tmu_svbus_pend
12	MEM_WDF_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_wdf_svbus_pend
11	MEM_CMU5_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu5_svbus_pend

Table 19-25. UFS_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MEM_CCI_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cci_svbus_pend
9	MEM_CMU4_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu4_svbus_pend
8	MEM_CMU2_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu2_svbus_pend
7	MEM_ID_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_id_svbus_pend
6	MEM_CIP_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cip_svbus_pend
5	MEM_RDC_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_rdc_svbus_pend
4	MEM_CMU6_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu6_svbus_pend
3	MEM_WDCM_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_wdcm_svbus_pend
2	MEM_CMU7_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu7_svbus_pend
1	MEM_WDCF_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_wdcf_svbus_pend
0	MEM_RX_TC0_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_rx_tc0_svbus_pend

Table 19-26. Register Call Summary for UFS_SEC_ENABLE_CLR_REG0

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.9 UFS_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

UFS_DED_EOI_REG is shown in [Figure 19-9](#) and described in [Table 19-28](#).

Return to [Summary Table](#).

DED End Of Interrupt (EOI) Register

The DED End Of Interrupt (EOI) register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the DED End Of Interrupt (EOI) register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the DED End Of Interrupt (EOI) register is not functional and must not be used.

Table 19-27. UFS_DED_EOI_REG Instances

Instance	Physical Address
UFS0	02A2 813Ch

Figure 19-9. UFS_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-28. UFS_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	End Of Interrupt (EOI)

Table 19-29. Register Call Summary for UFS_DED_EOI_REG

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.10 UFS_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

UFS_DED_STATUS_REG0 is shown in Figure 19-10 and described in Table 19-31.

Return to [Summary Table](#).

DED Interrupt Status Register 0

Table 19-30. UFS_DED_STATUS_REG0 Instances

Instance	Physical Address
UFS0	02A2 8140h

Figure 19-10. UFS_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC_PEN D	MEM_CMU1_S VBUS_PEND	MEM_RTT_SV BUS_PEND	MEM_WDC_SV BUS_PEND
R-0h				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
MEM_RDF_SV BUS_PEND	MEM_CMU3_S VBUS_PEND	MEM_TMU_SV BUS_PEND	MEM_WDF_SV BUS_PEND	MEM_CMU5_S VBUS_PEND	MEM_CCI_SVB US_PEND	MEM_CMU4_S VBUS_PEND	MEM_CMU2_S VBUS_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
MEM_ID_SVBUS S_PEND	MEM_CIP_SVB US_PEND	MEM_RDC_SV BUS_PEND	MEM_CMU6_S VBUS_PEND	MEM_WDCM SVBUS_PEND	MEM_CMU7_S VBUS_PEND	MEM_WDCF_S VBUS_PEND	MEM_RX_TC0 _SVBUS_PEN D
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-31. UFS_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for ramecc_pend
18	MEM_CMU1_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu1_svbus_pend
17	MEM_RTT_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_rtt_svbus_pend
16	MEM_WDC_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdc_svbus_pend
15	MEM_RDF_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_rdf_svbus_pend
14	MEM_CMU3_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu3_svbus_pend
13	MEM_TMU_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_tmu_svbus_pend
12	MEM_WDF_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdf_svbus_pend
11	MEM_CMU5_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu5_svbus_pend
10	MEM_CCI_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cci_svbus_pend
9	MEM_CMU4_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu4_svbus_pend

Table 19-31. UFS_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MEM_CMU2_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu2_svbus_pend
7	MEM_ID_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_id_svbus_pend
6	MEM_CIP_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cip_svbus_pend
5	MEM_RDC_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_rdc_svbus_pend
4	MEM_CMU6_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu6_svbus_pend
3	MEM_WDCM_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdcm_svbus_pend
2	MEM_CMU7_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_cmu7_svbus_pend
1	MEM_WDCF_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_wdcf_svbus_pend
0	MEM_RX_TC0_SVBUS_PEND	R/W1S	0h	Interrupt Pending Status for mem_rx_tc0_svbus_pend

Table 19-32. Register Call Summary for UFS_DED_STATUS_REG0

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_DED_STATUS_REG0 Register \(Offset = 140h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.11 UFS_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

UFS_DED_ENABLE_SET_REG0 is shown in Figure 19-11 and described in Table 19-34.

Return to [Summary Table](#).

DED Interrupt Enable Set Register 0

**Table 19-33. UFS_DED_ENABLE_SET_REG0
Instances**

Instance	Physical Address
UFS0	02A2 8180h

Figure 19-11. UFS_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC_ENA BLE_SET	MEM_CMU1_S VBUS_ENABLE _SET	MEM_RTT_SV BUS_ENABLE_ SET	MEM_WDC_SV BUS_ENABLE_ SET
R-0h				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
MEM_RDF_SV BUS_ENABLE_ SET	MEM_CMU3_S VBUS_ENABLE _SET	MEM_TMU_SV BUS_ENABLE_ SET	MEM_WDF_SV BUS_ENABLE_ SET	MEM_CMU5_S VBUS_ENABLE _SET	MEM_CCI_SVB US_ENABLE_ SET	MEM_CMU4_S VBUS_ENABLE _SET	MEM_CMU2_S VBUS_ENABLE _SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
MEM_ID_SVB US_ENABLE_ SET	MEM_CIP_SVB US_ENABLE_ SET	MEM_RDC_SV BUS_ENABLE_ SET	MEM_CMU6_S VBUS_ENABLE _SET	MEM_WDCM SVBUS_ENABL E_SET	MEM_CMU7_S VBUS_ENABLE _SET	MEM_WDCF_S VBUS_ENABLE _SET	MEM_RX_TC0 _SVBUS_ENAB LE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-34. UFS_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for ramecc_pend
18	MEM_CMU1_SVBUS_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu1_svbus_pend
17	MEM_RTT_SVBUS_ENA BLE_SET	R/W1S	0h	Interrupt Enable Set for mem_rtt_svbus_pend
16	MEM_WDC_SVBUS_ENA BLE_SET	R/W1S	0h	Interrupt Enable Set for mem_wdc_svbus_pend
15	MEM_RDF_SVBUS_ENA BLE_SET	R/W1S	0h	Interrupt Enable Set for mem_rdf_svbus_pend
14	MEM_CMU3_SVBUS_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu3_svbus_pend
13	MEM_TMU_SVBUS_ENA BLE_SET	R/W1S	0h	Interrupt Enable Set for mem_tmu_svbus_pend
12	MEM_WDF_SVBUS_ENA BLE_SET	R/W1S	0h	Interrupt Enable Set for mem_wdf_svbus_pend
11	MEM_CMU5_SVBUS_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu5_svbus_pend

Table 19-34. UFS_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MEM_CCI_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cci_svbus_pend
9	MEM_CMU4_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu4_svbus_pend
8	MEM_CMU2_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu2_svbus_pend
7	MEM_ID_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_id_svbus_pend
6	MEM_CIP_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cip_svbus_pend
5	MEM_RDC_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_rdc_svbus_pend
4	MEM_CMU6_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu6_svbus_pend
3	MEM_WDCM_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_wdcm_svbus_pend
2	MEM_CMU7_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_cmu7_svbus_pend
1	MEM_WDCF_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_wdcf_svbus_pend
0	MEM_RX_TC0_SVBUS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set for mem_rx_tc0_svbus_pend

Table 19-35. Register Call Summary for UFS_DED_ENABLE_SET_REG0

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_DED_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.12 UFS_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

UFS_DED_ENABLE_CLR_REG0 is shown in Figure 19-12 and described in Table 19-37.

Return to [Summary Table](#).

DED Interrupt Enable Clear Register 0

**Table 19-36. UFS_DED_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
UFS0	02A2 81C0h

Figure 19-12. UFS_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				RAMECC_ENA BLE_CLR	MEM_CMU1_S VBUS_ENABLE _CLR	MEM_RTT_SV BUS_ENABLE_ CLR	MEM_WDC_SV BUS_ENABLE_ CLR
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
MEM_RDF_SV BUS_ENABLE_ CLR	MEM_CMU3_S VBUS_ENABLE _CLR	MEM_TMU_SV BUS_ENABLE_ CLR	MEM_WDF_SV BUS_ENABLE_ CLR	MEM_CMU5_S VBUS_ENABLE _CLR	MEM_CCI_SVB US_ENABLE_C LR	MEM_CMU4_S VBUS_ENABLE _CLR	MEM_CMU2_S VBUS_ENABLE _CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
MEM_ID_SVB US_ENABLE_C LR	MEM_CIP_SVB US_ENABLE_C LR	MEM_RDC_SV BUS_ENABLE_ CLR	MEM_CMU6_S VBUS_ENABLE _CLR	MEM_WDCM_ SVBUS_ENABL E_CLR	MEM_CMU7_S VBUS_ENABLE _CLR	MEM_WDCF_S VBUS_ENABLE _CLR	MEM_RX_TC0 _SVBUS_ENAB LE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-37. UFS_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for ramecc_pend
18	MEM_CMU1_SVBUS_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu1_svbus_pend
17	MEM_RTT_SVBUS_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_rtt_svbus_pend
16	MEM_WDC_SVBUS_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_wdc_svbus_pend
15	MEM_RDF_SVBUS_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_rdf_svbus_pend
14	MEM_CMU3_SVBUS_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu3_svbus_pend
13	MEM_TMU_SVBUS_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_tmu_svbus_pend
12	MEM_WDF_SVBUS_ENA BLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_wdf_svbus_pend
11	MEM_CMU5_SVBUS_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu5_svbus_pend

Table 19-37. UFS_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MEM_CCI_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cci_svbus_pend
9	MEM_CMU4_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu4_svbus_pend
8	MEM_CMU2_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu2_svbus_pend
7	MEM_ID_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_id_svbus_pend
6	MEM_CIP_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cip_svbus_pend
5	MEM_RDC_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_rdc_svbus_pend
4	MEM_CMU6_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu6_svbus_pend
3	MEM_WDCM_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_wdcm_svbus_pend
2	MEM_CMU7_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_cmu7_svbus_pend
1	MEM_WDCF_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_wdcf_svbus_pend
0	MEM_RX_TC0_SVBUS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear for mem_rx_tc0_svbus_pend

Table 19-38. Register Call Summary for UFS_DED_ENABLE_CLR_REG0

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.13 UFS_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

UFS_AGGR_ENABLE_SET is shown in Figure 19-13 and described in Table 19-40.

Return to [Summary Table](#).

Aggregator Interrupt Enable Set Register

Table 19-39. UFS_AGGR_ENABLE_SET Instances

Instance	Physical Address
UFS0	02A2 8200h

Figure 19-13. UFS_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-40. UFS_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for serial VBUS timeout errors.
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors.

Table 19-41. Register Call Summary for UFS_AGGR_ENABLE_SET

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_AGGR_ENABLE_SET Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.14 UFS_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

UFS_AGGR_ENABLE_CLR is shown in Figure 19-14 and described in Table 19-43.

Return to [Summary Table](#).

Aggregator Interrupt Enable Clear Register

Table 19-42. UFS_AGGR_ENABLE_CLR Instances

Instance	Physical Address
UFS0	02A2 8204h

Figure 19-14. UFS_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-43. UFS_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for serial VBUS timeout errors.
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors.

Table 19-44. Register Call Summary for UFS_AGGR_ENABLE_CLR

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_AGGR_ENABLE_CLR Register \(Offset = 204h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.15 UFS_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

UFS_AGGR_STATUS_SET is shown in Figure 19-15 and described in Table 19-46.

Return to [Summary Table](#).

Aggregator Interrupt Status Set Register

Table 19-45. UFS_AGGR_STATUS_SET Instances

Instance	Physical Address
UFS0	02A2 8208h

Figure 19-15. UFS_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 19-46. UFS_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for serial VBUS timeout errors.
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors.

Table 19-47. Register Call Summary for UFS_AGGR_STATUS_SET

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_AGGR_STATUS_SET Register \(Offset = 208h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.1.16 UFS_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

UFS_AGGR_STATUS_CLR is shown in Figure 19-16 and described in Table 19-49.

Return to [Summary Table](#).

Aggregator Interrupt Status Clear Register

Table 19-48. UFS_AGGR_STATUS_CLR Instances

Instance	Physical Address
UFS0	02A2 820Ch

Figure 19-16. UFS_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 19-49. UFS_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for serial VBUS timeout errors.
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors.

Table 19-50. Register Call Summary for UFS_AGGR_STATUS_CLR

UFS0_HCLK_ECC_AGGR_CFG Registers

- [UFS_AGGR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = 0h\]: \[0\]](#)
- [UFS0_HCLK_ECC_AGGR_CFG Registers: \[0\]](#)

19.2 UFS0_IPS_TCLK_ERR_INJ_CFG Registers

Table 19-52 lists the memory-mapped registers for the UFS0_IPS_TCLK_ERR_INJ_CFG registers. All register offset addresses not listed in Table 19-52 should be considered as reserved locations and the register contents should not be modified.

**Table 19-51. UFS0_IPS_TCLK_ERR_INJ_CFG
Instances**

Instance	Base Address
UFS0_IPS_TCLK_ERR_INJ_CFG	02A2 A000h

Table 19-52. UFS0_IPS_TCLK_ERR_INJ_CFG Registers

Offset	Acronym	Register Name	UFS0_IPS_TCLK_ERR_INJ_CFG Physical Address
0h	UFS_PID	Revision Register	02A2 A000h
4h	UFS_INFO	Info Register	02A2 A004h
8h	UFS_SFT_RST	Global Soft Reset Register	02A2 A008h
10h	UFS_BIT1	Bit 1 Mask Register	02A2 A010h
14h	UFS_BIT2	Bit 2 Mask Register	02A2 A014h
18h	UFS_TRGT	Target Select Register	02A2 A018h
1Ch	UFS_CTRL	Control Register	02A2 A01Ch
20h	UFS_STATUS	Status Register	02A2 A020h

19.2.1 UFS_PID Register (Offset = 0h) [reset = 60000001h]

UFS_PID is shown in [Figure 19-17](#) and described in [Table 19-54](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 19-53. UFS_PID Instances

Instance	Physical Address
UFS0	02A2 A000h

Figure 19-17. UFS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-2h		R-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-0h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 19-54. UFS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business Unit: 2h = Processors
27-16	FUNC	R	0h	Module ID
15-11	RTL	R	0h	RTL Revision
10-8	MAJOR	R	0h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	1h	Minor Revision

Table 19-55. Register Call Summary for UFS_PID

UFS0_IPS_TCLK_ERR_INJ_CFG Registers

- [UFS0_IPS_TCLK_ERR_INJ_CFG Registers: \[0\]](#)

19.2.2 UFS_INFO Register (Offset = 4h) [reset = 1h]

UFS_INFO is shown in [Figure 19-18](#) and described in [Table 19-57](#).

Return to [Summary Table](#).

The Info Register gives the configuration information of the module.

Table 19-56. UFS_INFO Instances

Instance	Physical Address
UFS0	02A2 A004h

Figure 19-18. UFS_INFO Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						ENDPOINTS	
R-0h						R-1h	

LEGEND: R = Read Only; -n = value after reset

Table 19-57. UFS_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	ENDPOINTS	R	1h	Total number of Targets supported by this configuration.

Table 19-58. Register Call Summary for UFS_INFO

UFS0_IPS_TCLK_ERR_INJ_CFG Registers

- [UFS0_IPS_TCLK_ERR_INJ_CFG Registers](#): [0]
- [UFS_INFO Register \(Offset = 4h\) \[reset = 1h\]](#): [0]

19.2.3 UFS_SFT_RST Register (Offset = 8h) [reset = 0h]

UFS_SFT_RST is shown in [Figure 19-19](#) and described in [Table 19-60](#).

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The Global Soft Reset Register clears all programmable registers and returns the injector to idle state.

Table 19-59. UFS_SFT_RST Instances

Instance	Physical Address
UFS0	02A2 A008h

Figure 19-19. UFS_SFT_RST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												KEY			
R-0h																												W-0h			

LEGEND: W = Write Only; -n = value after reset

Table 19-60. UFS_SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	KEY	W	0h	Write Ah to issue a soft reset. All other written values are ignored. Always read as 0h.

Table 19-61. Register Call Summary for UFS_SFT_RST

UFS0_IPS_TCLK_ERR_INJ_CFG Registers

- [UFS0_IPS_TCLK_ERR_INJ_CFG Registers: \[0\]](#)
- [UFS_SFT_RST Register \(Offset = 8h\) \[reset = 0h\]: \[0\]](#)

19.2.4 UFS_BIT1 Register (Offset = 10h) [reset = 0h]

UFS_BIT1 is shown in [Figure 19-20](#) and described in [Table 19-63](#).

Return to [Summary Table](#).

The Bit 1 Mask Register defines the first bit to be flipped when injection is enabled.

Table 19-62. UFS_BIT1 Instances

Instance	Physical Address
UFS0	02A2 A010h

Figure 19-20. UFS_BIT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BIT1															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-63. UFS_BIT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	BIT1	R/W	0h	First bit to be flipped on an error injection.

Table 19-64. Register Call Summary for UFS_BIT1

UFS0_IPS_TCLK_ERR_INJ_CFG Registers

- [UFS_BIT1 Register \(Offset = 10h\) \[reset = 0h\]: \[0\]](#)
- [UFS0_IPS_TCLK_ERR_INJ_CFG Registers: \[0\]](#)

19.2.5 UFS_BIT2 Register (Offset = 14h) [reset = 0h]

UFS_BIT2 is shown in [Figure 19-21](#) and described in [Table 19-66](#).

Return to [Summary Table](#).

The Bit 2 Mask Register defines the second bit to be flipped if 2-bit injection is enabled.

Table 19-65. UFS_BIT2 Instances

Instance	Physical Address
UFS0	02A2 A014h

Figure 19-21. UFS_BIT2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BIT2															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-66. UFS_BIT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	BIT2	R/W	0h	Second bit to be flipped on an error injection if 2-bit injection is chosen.

Table 19-67. Register Call Summary for UFS_BIT2

UFS0_IPS_TCLK_ERR_INJ_CFG Registers

- [UFS0_IPS_TCLK_ERR_INJ_CFG Registers](#): [0]
- [UFS_BIT2 Register \(Offset = 14h\) \[reset = 0h\]](#): [0]

19.2.6 UFS_TRGT Register (Offset = 18h) [reset = 0h]

UFS_TRGT is shown in [Figure 19-22](#) and described in [Table 19-69](#).

Return to [Summary Table](#).

The Target Select Register selects which target to interact with.

Table 19-68. UFS_TRGT Instances

Instance	Physical Address
UFS0	02A2 A018h

Figure 19-22. UFS_TRGT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							TRGT
R-0h							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-69. UFS_TRGT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	TRGT	R/W	0h	Select which target to interact with. Writes of a value higher than the number of targets supported by this configuration will have no effect.

Table 19-70. Register Call Summary for UFS_TRGT

UFS0_IPS_TCLK_ERR_INJ_CFG Registers

- [UFS0_IPS_TCLK_ERR_INJ_CFG Registers](#): [0]
- [UFS_STATUS Register](#) (Offset = 20h) [reset = 0h]: [0]
- [UFS_CTRL Register](#) (Offset = 1Ch) [reset = 0h]: [0] [1] [2] [3]
- [UFS_TRGT Register](#) (Offset = 18h) [reset = 0h]: [0]

19.2.7 UFS_CTRL Register (Offset = 1Ch) [reset = 0h]

UFS_CTRL is shown in Figure 19-23 and described in Table 19-72.

Return to [Summary Table](#).

The Control Register controls the injection.

Table 19-71. UFS_CTRL Instances

Instance	Physical Address
UFS0	02A2 A01Ch

Figure 19-23. UFS_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							TRGT
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED					DONE	TWOBIT	ONEBIT
R-0h					R-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-72. UFS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	TRGT	R	0h	Indicates which target is selected by the UFS_TRGT register.
7-3	RESERVED	R	0h	Reserved
2	DONE	R	0h	Indicates that the target selected by the UFS_TRGT register has completed error injection. The UFS_STATUS register supersedes the armed bit.
1	TWOBIT	R/W	0h	Write 1h to trigger a 2-bit error in target selected by the UFS_TRGT register. Write 0h to finish or cancel 2-bit injection. If both 1 and 2-bit injection are set, 2-bit injection will be performed.
0	ONEBIT	R/W	0h	Write 1h to trigger a 1-bit error in target selected by the UFS_TRGT register. Write 0h to finish or cancel 1-bit injection.

Table 19-73. Register Call Summary for UFS_CTRL

UFS0_IPS_TCLK_ERR_INJ_CFG Registers

- [UFS0_IPS_TCLK_ERR_INJ_CFG](#) Registers: [0]
- [UFS_CTRL](#) Register (Offset = 1Ch) [reset = 0h]: [0]

19.2.8 UFS_STATUS Register (Offset = 20h) [reset = 0h]

UFS_STATUS is shown in Figure 19-24 and described in Table 19-75.

Return to [Summary Table](#).

The Status Register controls the injection.

Table 19-74. UFS_STATUS Instances

Instance	Physical Address
UFS0	02A2 A020h

Figure 19-24. UFS_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ARMED	RESERVED	
R-0h					R-0h	R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 19-75. UFS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	R	Reserved
2	ARMED	R	0h	Indicates that the target selected by the UFS_TRGT register is ARMED for error injection.
1-0	RESERVED	R	R	Reserved

Table 19-76. Register Call Summary for UFS_STATUS

UFS0_IPS_TCLK_ERR_INJ_CFG Registers

- UFS0_IPS_TCLK_ERR_INJ_CFG Registers: [0]
- UFS_STATUS Register (Offset = 20h) [reset = 0h]: [0]
- UFS_CTRL Register (Offset = 1Ch) [reset = 0h]: [0]

19.3 UFS0_P2A_WRAP_CFG_VBP_UFSHCI Registers

Table 19-78 lists the memory-mapped registers for the UFS0_P2A_WRAP_CFG_VBP_UFSHCI registers. All register offset addresses not listed in Table 19-78 should be considered as reserved locations and the register contents should not be modified.

Table 19-77. UFS0_P2A_WRAP_CFG_VBP_UFSHCI Instances

Instance	Base Address
UFS0_P2A_WRAP_CFG_VBP_UFSHCI	04E8 4000h

Table 19-78. UFS0_P2A_WRAP_CFG_VBP_UFSHCI Registers

Offset	Acronym	Register Name	UFS0_P2A_WRAP_CFG_VBP_UFSHCI Physical Address
0h	UFS_CAP	Host Controller Capabilities Register	04E8 4000h
8h	UFS_VER	UFS Version Register	04E8 4008h
10h	UFS_HCPID	Host Controller Identification Descriptor Register (Device ID and Device Class)	04E8 4010h
14h	UFS_HCMID	Host Controller Identification Descriptor Register (Product ID and Manufacturer ID)	04E8 4014h
18h	UFS_AHIT	Auto-Hibernate Idle Timer Register	04E8 4018h
20h	UFS_IS	Interrupt Status Register	04E8 4020h
24h	UFS_IE	Interrupt Enable Register	04E8 4024h
30h	UFS_HCS	Host Controller Status Register	04E8 4030h
34h	UFS_HCE	Host Controller Enable Register	04E8 4034h
38h	UFS_UECPA	Host Controller UIC Error Code PHY Adapter Layer Register	04E8 4038h
3Ch	UFS_UECDL	Host UIC Error Code Data Link Layer Register	04E8 403Ch
40h	UFS_UECN	Host UIC Error Code Network Layer Register	04E8 4040h
44h	UFS_UECT	Host UIC Error Code Transport Layer Register	04E8 4044h
48h	UFS_UECDME	Host UIC Error Code DME Register	04E8 4048h
4Ch	UFS_UTRIACR	UTP Transfer Request Interrupt Aggregation Control Register	04E8 404Ch
50h	UFS_UTRLBA	UTP Transfer Request List Base Address Register	04E8 4050h
54h	UFS_UTRLBAU	UTP Transfer Request List Base Address Upper 32-bits Register	04E8 4054h
58h	UFS_UTRLDBR	UTP Transfer Request List Door Bell Register	04E8 4058h
5Ch	UFS_UTRLCLR	UTP Transfer Request List Clear Register	04E8 405Ch
60h	UFS_UTRLRSR	UTP Transfer Request List Run Stop Register	04E8 4060h
64h	UFS_UTRLCNR	UTP Transfer Request List Completion Notification Register	04E8 4064h
70h	UFS_UTMRLBA	UTP Task Management Request List Base Address Register	04E8 4070h
74h	UFS_UTMRLBAU	UTP Task Management Request List Base Address Upper 32-bits Register	04E8 4074h
78h	UFS_UTMRLDBR	UTP Task Management Request List Door Bell Register	04E8 4078h
7Ch	UFS_UTMRLCLR	UTP Task Management Request List Clear Register	04E8 407Ch
80h	UFS_UTMRLRSR	UTP Task Management Request List Run Stop Register	04E8 4080h
90h	UFS_UICCMD	UIC Command Register	04E8 4090h
94h	UFS_UICCMDARG1	UIC Command Argument 1 Register	04E8 4094h
98h	UFS_UICCMDARG2	UIC Command Argument 2 Register	04E8 4098h

Table 19-78. UFS0_P2A_WRAP_CFG_VBP_UFSHCI Registers (continued)

Offset	Acronym	Register Name	UFS0_P2A_WRAP_CFG_VBP_UFSHCI Physical Address
9Ch	UFS_UICCMDARG3	UIC Command Argument 3 Register	04E8 409Ch
A0h	UFS_SYSTHRTL	SYS Throttling Register	04E8 40A0h
ACh	UFS_HCI_MMIO_TOSH_UNIRESPOL	UniPro Reset Polling Register	04E8 40ACh
C4h	UFS_OSYSR	Outstanding SYS Requests Register	04E8 40C4h
C8h	UFS_XCNF	Extended Configuration Register	04E8 40C8h
CCh	UFS_ADSIT	Auto-Deep-Sleep Idle Timer Register	04E8 40CCh
D0h	UFS_CDACFG	C-Port Direct Access Configuration Register	04E8 40D0h
D4h	UFS_CDATX1	C-Port Direct Access Transmit 1 Register	04E8 40D4h
D8h	UFS_CDATX2	C-Port Direct Access Transmit 2 Register	04E8 40D8h
DCh	UFS_CDARX1	C-Port Direct Access Receive 1 Register	04E8 40DCh
E0h	UFS_CDARX2	C-Port Direct Access Receive 2 Register	04E8 40E0h
E4h	UFS_CDASTA	C-Port Direct Access Status Register	04E8 40E4h
E8h	UFS_XASB	Extended Address Space Base Register	04E8 40E8h
F0h	UFS_LBMCFG	UPIU Loopback Configuration Register	04E8 40F0h
F4h	UFS_LBMSTA	UPIU Loopback Status Register	04E8 40F4h
F8h	UFS_DBG	Debug Register	04E8 40F8h
FCh	UFS_HCLKDIV	HCLK Divider Register	04E8 40FCh
100h	UFS_CCAP	Crypto Capabilities Register	04E8 4100h
104h	UFS_CRYPTOCAP	Crypto Capability X Register	04E8 4104h
500h	UFS_CRYPTOCFG0	Crypto Configuration 0 Register	04E8 4500h
504h	UFS_CRYPTOCFG1	Crypto Configuration 1 Register	04E8 4504h
508h	UFS_CRYPTOCFG2	Crypto Configuration 2 Register	04E8 4508h
50Ch	UFS_CRYPTOCFG3	Crypto Configuration 3 Register	04E8 450Ch
540h	UFS_CRYPTOCFG16	Crypto Configuration 16 Register	04E8 4540h
544h	UFS_CRYPTOCFG17	Crypto Configuration 17 Register	04E8 4544h
580h	UFS_CRYPTOCFG32	Crypto Configuration 0 For Second Crypto Configuration Register	04E8 4580h
584h	UFS_CRYPTOCFG33	Crypto Configuration 1 For Second Crypto Configuration Register	04E8 4584h
588h	UFS_CRYPTOCFG34	Crypto Configuration 2 For Second Crypto Configuration Register	04E8 4588h
58Ch	UFS_CRYPTOCFG35	Crypto Configuration 3 For Second Crypto Configuration Register	04E8 458Ch
5C0h	UFS_CRYPTOCFG48	Crypto Configuration 16 For Second Crypto Configuration Register	04E8 45C0h
5C4h	UFS_CRYPTOCFG49	Crypto Configuration 17 For Second Crypto Configuration Register	04E8 45C4h
1000h	UFS_ASF_INT_STATUS	ASF Interrupt Status Register	04E8 5000h
1004h	UFS_ASF_INT_RAW_STATUS	ASF Interrupt Raw Status Register	04E8 5004h
1008h	UFS_ASF_INT_MASK	ASF Interrupt Mask Register	04E8 5008h
100Ch	UFS_ASF_INT_TEST	ASF Interrupt Test Register	04E8 500Ch
1010h	UFS_ASF_FATAL_NONFATAL_SELECT	Fatal Or Non-Fatal Interrupt Register	04E8 5010h
1020h	UFS_ASF_SRAM_CORR_FAULT_STATUS	Status Register (For SRAM Correctable Fault)	04E8 5020h
1024h	UFS_ASF_SRAM_UNCORR_FAULT_STATUS	Status Register (For SRAM Uncorrectable Fault)	04E8 5024h
1028h	UFS_ASF_SRAM_FAULT_STATS	Statistics Register (For SRAM Faults)	04E8 5028h
1030h	UFS_ASF_TRANS_TO_CTRL	Control Register (To Configure The ASF Transaction Timeout Monitors)	04E8 5030h

Table 19-78. UFS0_P2A_WRAP_CFG_VBP_UFSHCI Registers (continued)

Offset	Acronym	Register Name	UFS0_P2A_WRAP_CFG_VBP_UFSHCI Physical Address
1034h	UFS_ASF_TRANS_TO_FAULT_MASK	Control Register (To Mask Out ASF Transaction Timeout Faults From Triggering Interrupts)	04E8 5034h
1038h	UFS_ASF_TRANS_TO_FAULT_STATUS	Status Register (For Transaction Timeouts Fault)	04E8 5038h
1040h	UFS_ASF_PROTOCOL_FAULT_MASK	Control Register (To Mask Out ASF Protocol Faults From Triggering Interrupts)	04E8 5040h
1044h	UFS_ASF_PROTOCOL_FAULT_STATUS	Status Register (For Protocol Faults)	04E8 5044h
1058h	UFS_ASF_INTEGRITY_ERR_INJ	ASF Integrity Test Register	04E8 5058h
1100h	UFS_MAG_NUM	Magic Number Register	04E8 5100h
1104h	UFS_MPHYSTAT_XCFG01	Output Debug Bits For PHY 1 Register	04E8 5104h
1108h	UFS_MPHYSTAT_XCFG02	Output Debug Bits For PHY 2 Register	04E8 5108h
110Ch	UFS_MPHYSTAT_XCFG03	Output Debug Bits For PHY 3 Register	04E8 510Ch
1110h	UFS_MPHYSTAT_XCFG04	Output Debug Bits For PHY 4 Register	04E8 5110h
1114h	UFS_MPHYSTAT_XCFG05	Output Debug Bits For PHY 5 Register	04E8 5114h
1118h	UFS_MPHYSTAT_XCFG06	Output Debug Bits For PHY 6 Register	04E8 5118h
111Ch	UFS_MPHYSTAT_XCFG07	Output Debug Bits For PHY 7 Register	04E8 511Ch
1120h	UFS_MPHYSTAT_XCFG08	Output Debug Bits For PHY 8 Register	04E8 5120h
1124h	UFS_MPHYSTAT_XCFG09	Output Debug Bits For PHY 9 Register	04E8 5124h
1128h	UFS_MPHY_DEBUG_OUT	M-PHY Debug Out Register	04E8 5128h
112Ch	UFS_MPHY_BIST	BIST Pattern Check Passed For Lane 0 And Lane 1 Register	04E8 512Ch
1130h	UFS_MPHY_SF	Safety Register	04E8 5130h
1134h	UFS_MPHYSTAT	M-PHY Status Register	04E8 5134h
1138h	UFS_MPHY_MMIO_A	M-PHY Configuration - MMIO Access Register	04E8 5138h
113Ch	UFS_MPHYCFG_XCFGD1	M-PHY Configuration For Digital Part 1 Register	04E8 513Ch
1140h	UFS_MPHYCFG_XCFGD2	M-PHY Configuration For Digital Part 2 Register	04E8 5140h
1144h	UFS_MPHYCFG_XCFGD3	M-PHY Configuration For Digital Part 3 Register	04E8 5144h
1148h	UFS_MPHYCFG_XCFGD4	M-PHY Configuration For Digital Part 4 Register	04E8 5148h
114Ch	UFS_MPHYCFG_XCFGD5	M-PHY Configuration For Digital Part 5 Register	04E8 514Ch
1150h	UFS_MPHYCFG_XCFGA1	M-PHY Configuration For Analog Part 1 Register	04E8 5150h
1154h	UFS_MPHYCFG_XCFGA2	M-PHY Configuration For Analog Part 2 Register	04E8 5154h
1158h	UFS_MPHYCFG_XCFGA3	M-PHY Configuration For Analog Part 3 Register	04E8 5158h
115Ch	UFS_MPHYCFG_XCFGA4	M-PHY Configuration For Analog Part 4 Register	04E8 515Ch
1160h	UFS_MPHYCFG_XCFGA5	M-PHY Configuration For Analog Part 5 Register	04E8 5160h
1164h	UFS_MPHYCFG_XCFGA6	M-PHY Configuration For Analog Part 6 Register	04E8 5164h
1168h	UFS_MPHYCFG_XCFGA7	M-PHY Configuration For Analog Part 7 Register	04E8 5168h
116Ch	UFS_MPHYCFG_XCFGA8	M-PHY Configuration For Analog Part 8 Register	04E8 516Ch
1170h	UFS_MPHYCFG_XCFGA9	M-PHY Configuration For Analog Part 9 Register	04E8 5170h
1174h	UFS_MPHYCFG_XCFGA10	M-PHY Configuration For Analog Part 10 Register	04E8 5174h
1178h	UFS_MPHYCFG_XCFGA11	M-PHY Configuration For Analog Part 11 Register	04E8 5178h
117Ch	UFS_MPHYCFG_XCFGA12	M-PHY Configuration For Analog Part 12 Register	04E8 517Ch
1180h	UFS_MPHYCFG_XCFGA13	M-PHY Configuration For Analog Part 13 Register	04E8 5180h
1184h	UFS_MPHYCFG_MISC	M-PHY MISC Configuration Register	04E8 5184h
1188h	UFS_MPHYCFG_VCONTROL	M-PHY VCONTROL Configuration Register	04E8 5188h
118Ch	UFS_MPHY_BIST_CTRLPIN	M-PHY BIST Control Pins Register	04E8 518Ch
1190h	UFS_MPHY_SF_WD	M-PHY Safety Related Watch Dog Register	04E8 5190h

19.3.1 UFS_CAP Register (Offset = 0h) [reset = 1587031Fh]

UFS_CAP is shown in [Figure 19-25](#) and described in [Table 19-80](#).

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Host Controller Capabilities Register

This register describes the basic capabilities of the UFS host controller.

Table 19-79. UFS_CAP Instances

Instance	Physical Address
UFS	04E8 4000h

Figure 19-25. UFS_CAP Register

31	30	29	28	27	26	25	24
RESERVED		MHS	CS	DBMMS	UICDMETMS	OODDS	AS64
R-0h		R-0h	R-1h	R-0h	R-1h	R-0h	R-1h
23	22	21	20	19	18	17	16
AUTOH8	RESERVED				NUTMRS		
R-1h	R-0h				R-7h		
15	14	13	12	11	10	9	8
NORTT							
R-3h							
7	6	5	4	3	2	1	0
RESERVED			NUTRS				
R-0h			R-1Fh				

LEGEND: R = Read Only; -n = value after reset

Table 19-80. UFS_CAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	MHS	R	0h	Multi-Host Support Indicates that the host controller supports multi-host functionality.
28	CS	R	1h	Crypto Support Indicates that the host controller supports cryptographic operations.
27	DBMMS	R	0h	Device Bus Master Mode Supported (Unified Memory (UM) UFSHCI Only) Indicates whether the UFS host controller supports the device bus master mode, which is required to support the Unified Memory feature. The device bus master mode allows sending requests from the UFS device to the UFS host controller. The host controller responds to those requests.
26	UICDMETMS	R	1h	UIC DME_TEST_MODE Command Supported Indicates whether the host controller supports the UniPro DME_TEST_MODE.req SAP primitive.

Table 19-80. UFS_CAP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	OODDS	R	0h	Out of Order Data Delivery Supported Indicates whether the host controller supports out of order data delivery for UTP data transfer. 1h = When set to 1h, the host controller shall support out of order data delivery from the target device. 0h = When set to 0h, the host controller will not support out of order data delivery from the target device.
24	AS64	R	1h	64-bit Addressing Supported Indicates whether the host controller can access 64-bit data structures. 1h = When set to 1h, the host controller shall make the 32-bit upper bits of the UTP Transfer Request List Base Address Upper 32-bit and UTP Task Management Request List Base Address Upper 32-bit, the PRD Base, and each PRD entry read/write. 0h = When cleared to 0h, these are read-only and treated as 0h by the UFS Host Controller.
23	AUTOH8	R	1h	Auto-Hibernation Support Indicates whether the host controller support auto-hibernation: 0h = Host controller does not support auto-hibernation 1h = Host controller does support auto hibernation
22-19	RESERVED	R	0h	Reserved
18-16	NUTMRS	R	7h	Number of UTP Task Management Request Slots Zero-based value indicating the number of slots provided by the UTP Task Management Request List. A minimum of 1 and maximum of 8 slots may be supported.
15-8	NORTT	R	3h	Number of Pending RTTs supported Zero-based value indicating the maximum number of RTTs that can be pending on the host at a particular instance. RTTs will be processed in the same order as they were received (First-come-first-serve).
7-5	RESERVED	R	0h	Reserved
4-0	NUTRS	R	1Fh	Number of UTP Transfer Request Slots Zero-based value indicating the number of slots provided by the UTP Transfer Request List. A minimum of 1 and maximum of 32 slots may be supported.

19.3.2 UFS_VER Register (Offset = 8h) [reset = 210h]

UFS_VER is shown in [Figure 19-26](#) and described in [Table 19-82](#).

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UFS Version Register

This register indicates the major and minor version of the UFSHCI specification that the controller implementation supports. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number.

Table 19-81. UFS_VER Instances

Instance	Physical Address
UFS	04E8 4008h

Figure 19-26. UFS_VER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MJR				MNR				VER							
R-0h																R-2h				R-1h				R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 19-82. UFS_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	MJR	R	2h	Major Version Number Indicates that the major version is 2.
7-4	MNR	R	1h	Minor Version Number Indicates that the minor version is 0.
3-0	VER	R	0h	Version Suffix (VS) Version suffix in BCD format.

19.3.3 UFS_HCPID Register (Offset = 10h) [reset = 0h]

UFS_HCPID is shown in [Figure 19-27](#) and described in [Table 19-84](#).

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Host Controller Identification Descriptor Register (Device ID and Device Class)

This register indicates the product identification information for host controller.

Table 19-83. UFS_HCPID Instances

Instance	Physical Address
UFS	04E8 4010h

Figure 19-27. UFS_HCPID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																PID															
																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 19-84. UFS_HCPID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID	R	0h	Product ID Product ID that host controller manufacturer assigns for the host controller. This is vendor specific.

19.3.4 UFS_HCMID Register (Offset = 14h) [reset = 0h]

UFS_HCMID is shown in [Figure 19-28](#) and described in [Table 19-86](#).

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Host Controller Identification Descriptor Register (Product ID and Manufacturer ID)

This register provides Manufacturer identification information for host controller manufacturer. The Manufacturer ID is defined by JEDEC in Standard Manufacturer's identification code (JEDEC-JEP106). The Manufacturer ID consists of two parts: Manufacturer Identification Code and Bank Index.

Table 19-85. UFS_HCMID Instances

Instance	Physical Address
UFS	04E8 4014h

Figure 19-28. UFS_HCMID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BI				MIC											
R-0h																R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 19-86. UFS_HCMID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	BI	R	0h	Bank Index This field contains an index value of the bank that contains the Manufacturer Identification Code (MIC). The BI value shall be equal to the number of the continuation fields that precede the MIC as specified by (JEDEC-JEP106).
7-0	MIC	R	0h	Manufacturer Identification Code Manufacturer Identification code as defined by JEDEC in Standard Manufacturers identification code (JEDEC-JEP106).

19.3.5 UFS_AHIT Register (Offset = 18h) [reset = 0h]

UFS_AHIT is shown in [Figure 19-29](#) and described in [Table 19-88](#).

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Auto-Hibernate Idle Timer Register

The UFS utilizes UniPro and SCSI standards as its power management framework. To improve power efficiency, the UFS host controller may support a mechanism called auto-hibernation. Auto-hibernation allows the host controller to put the UFS link into HIBERN8 state autonomously. The UFS_CAP[23] AUTOH8 bit provides a method for software to detect support of this feature. The UFS_AHIT[9-0] AH8ITV bit filed together with the UFS_AHIT[12-10] TS bit filed provides a method for software to directly control of this feature.

Note: Additionally to the above conditions, the auto-hibernation counter checks the status of the UniPro protocol layer. The host controller will only enter hibernate state when there is no pending UniPro communication.

Table 19-87. UFS_AHIT Instances

Instance	Physical Address
UFS	04E8 4018h

Figure 19-29. UFS_AHIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			TS		AH8ITV										
R-0h																			R/W-0h				R/W-0h								

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-88. UFS_AHIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-10	TS	R/W	0h	Time Scale 0h = Value times 1 μ s 1h = Value times 10 μ s 2h = Value times 100 μ s 3h = Value times 1 ms 4h = Value times 10 ms 5h = Value times 100 ms 6h-7h = Reserved

Table 19-88. UFS_AHIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	AH8ITV	R/W	0h	<p>Auto-Hibernate Idle Timer Value</p> <p>This is the time that UFS subsystem must be idle before the UFS host controller may put the UFS link into HIBERN8 state autonomously.</p> <p>The idle timer value is multiplied by the indicated timer scale to yield an absolute timer value.</p> <p>The idle timer starts decrement when all of the following conditions are satisfied:</p> <ul style="list-style-type: none"> - UFS_UTRLDBR = 0h - UFS_UTMRLDBR = 0h - No UIC commanding is outstanding <p>The idle timer shall continue decrement until it reaches zero or it is stopped as result of software access to one of host controller interface registers.</p> <p>When idle timer changes a non-zero to zero, the host controller shall put the UFS link into HIBERN8 state.</p> <p>The host controller reloads this value each time the UFS link transitions out of the HIBERN8 state.</p> <p>Software writes 0h to disable Auto-Hibernate Idle Timer.</p> <p>Any non-zero value will enable Auto-Hibernate Idle Timer.</p> <p>Software access to any one of host controller interface registers shall automatically put UFS link out of HIBERN8 state.</p>

19.3.6 UFS_IS Register (Offset = 20h) [reset = 0h]

UFS_IS is shown in [Figure 19-30](#) and described in [Table 19-90](#).

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Interrupt Status Register

This register indicates pending interrupts that require service by the low level driver firmware.

Table 19-89. UFS_IS Instances

Instance	Physical Address
UFS	04E8 4020h

Figure 19-30. UFS_IS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				CEFES		SBFES	HCFES
R-0h				R/W1C-0h		R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
RESERVED			UTPES	DFES	UCCS	UTMRCS	ULSS
R-0h			R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
ULLS	UHES	UHXS	UPMS	UTMS	UE	UDEPRI	UTRCS
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-90. UFS_IS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	CEFES	R/W1C	0h	Crypto Engine Fatal Error Status Indicates that the host controller's encryption/decryption hardware has encountered an error from which it cannot recover. When the error occurs, the host controller is stopped and both the UFS_UTRLRSR and UFS_UTMRLRSR registers will be cleared to 0h by host controller.
17	SBFES	R/W1C	0h	System Bus Fatal Error Status Indicates that the host controller encountered a system bus error that it cannot recover from, such as a bad software pointer. When the error occurs, the host controller is stopped and both the UFS_UTRLRSR and UFS_UTMRLRSR registers will be cleared to 0h by host controller.
16	HCFES	R/W1C	0h	Host Controller Fatal Error Status Indicates that the host controller encountered a fatal error that it cannot recover from. When the error occurs, the host controller is stopped and both the UFS_UTRLRSR and UFS_UTMRLRSR register will be cleared to 0h by host controller. If the error occurs, host software should reset the host controller.
15-13	RESERVED	R	0h	Reserved

Table 19-90. UFS_IS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	UTPES	R/W1C	0h	<p>UTP Error Status</p> <p>Indicates that the host controller encountered an error at UTP layer that it cannot recover from.</p> <p>When the error occurs, the host controller will update the UFS_HCS[15-12] UTPEC bit field.</p> <p>It is up to host software to decide how to handle the error condition.</p>
11	DFES	R/W1C	0h	<p>Device Fatal Error Status</p> <p>Indicates that the host controller encountered a fatal error from device that it cannot recover.</p> <p>When the error occurs, the host controller is stopped and both the UFS_UTRLRSR and UFS_UTMRLRSR registers will be cleared to 0h by host controller.</p> <p>If the error occurs, host software should reset the host controller.</p>
10	UCCS	R/W1C	0h	<p>UIC Command Completion Status</p> <p>This bit is set to 1h by the host controller upon completion of a UIC command.</p>
9	UTMRCS	R/W1C	0h	<p>UTP Task Management Request Completion Status</p> <p>This bit is set to 1h by the host controller upon completion of a task management function.</p>
8	ULSS	R/W1C	0h	<p>UIC Link Startup Status</p> <p>Indication that Link start-up process has been initiated by the remote end of the Link.</p> <p>This bit corresponds to the UniPro DME_LINKSTARTUP.ind SAP primitive.</p>
7	ULLS	R/W1C	0h	<p>UIC Link Lost Status</p> <p>This indicates a condition where remote end is trying to re-establish a link and the link is lost.</p> <p>This bit corresponds to the UniPro DME_LINKLOST.ind SAP primitive.</p>
6	UHES	R/W1C	0h	<p>UIC Hibernate Enter Status</p> <p>Indicate that UniPro hibernate entering process has been completed and the Link state is changed to the Hibernate state if the process was successful.</p> <p>The UFS_HCS[10-8] UPMCRS bit field indicates if exit process was unsuccessful the failure.</p> <p>This bit corresponds to the UniPro DME_HIBERNATE_ENTER.ind SAP primitive.</p>
5	UHXS	R/W1C	0h	<p>UIC Hibernate Exit Status</p> <p>Indicates that the Link has exited UniPro Hibernate state.</p> <p>The UFS_HCS[10-8] UPMCRS bit field indicates if exit process was unsuccessful the failure.</p> <p>This bit corresponds to the UniPro DME_HIBERNATE_EXIT.ind SAP primitive.</p>
4	UPMS	R/W1C	0h	<p>UIC Power Mode Status</p> <p>Indicate that the UniPro/PA/DL part of the power mode change has been completed.</p> <p>The UFS_HCS[10-8] UPMCRS bit field contains the power mode change status.</p> <p>This bit corresponds to the UniPro DME_POWERMODE.ind SAP primitive.</p>

Table 19-90. UFS_IS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	UTMS	R/W1C	0h	<p>UIC Test Mode Status</p> <p>Indicate that the peer UniPro stack has been set to a given UniPro test mode.</p> <p>This bit corresponds to the UniProSM DME_TEST_MODE.ind SAP primitive.</p>
2	UE	R/W1C	0h	<p>UIC Error</p> <p>Indicate that a layer in the UniPro stack has encountered an error condition.</p> <p>The UFS_HCS[15-12] UTPEC bit field contains the error code for the condition.</p> <p>This bit corresponds to the UniPro DME_ERROR.ind SAP primitive.</p> <p>This bit is asserted if at least one of the following bits is asserted:</p> <ul style="list-style-type: none"> - UFS_UECPA[31] ERR - UFS_UECDL[31] ERR - UFS_UECN[31] ERR - UFS_UECT[31] ERR - UFS_UECDME[31] ERR
1	UDEPRI	R/W1C	0h	<p>UIC DME_ENDPOINTRESET Indication</p> <p>Indicate that the attached device has issued an DME_ENDPOINTRESET indication which is not allowed.</p>
0	UTRCS	R/W1C	0h	<p>UTP Transfer Request Completion Status</p> <p>This bit is set to 1h by the host controller upon one of the following:</p> <ul style="list-style-type: none"> - Completion of a UTP transfer request with its UTRD Interrupt bit set to 1h. - Interrupt caused by the UTR interrupt aggregation logic.

19.3.7 UFS_IE Register (Offset = 24h) [reset = 0h]

UFS_IE is shown in [Figure 19-31](#) and described in [Table 19-92](#).

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Interrupt Enable Register

This register enables and disables the reporting of the corresponding interrupt to host software. When a bit is set (1h) and the corresponding interrupt condition is active, then an interrupt is generated. Interrupt sources that are disabled (0h) are still indicated in the UFS_IS register. The register bit assignment matches with the UFS_IS register.

Table 19-91. UFS_IE Instances

Instance	Physical Address
UFS	04E8 4024h

Figure 19-31. UFS_IE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED					CEFEE	SBFEE	HCFEE
R-0h					R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED			UTPEE	DFEE	UCCE	UTMRCE	ULSSE
R-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ULLSE	UHESE	UHXSE	UPMSE	UTMSE	UEE	UDEPRIE	UTRCE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-92. UFS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18	CEFEE	R/W	0h	Crypto Engine Fatal Error Enable When set and the UFS_IS[18] CEFES bit is set, the controller shall generate an interrupt. This bit is functional only, if the crypto engine is implemented.
17	SBFEE	R/W	0h	System Bus Fatal Error Enable When set and the UFS_IS[17] SBFES bit is set, the controller shall generate an interrupt.
16	HCFEE	R/W	0h	Host Controller Fatal Error Enable When set and the UFS_IS[16] HCFES is set, the controller shall generate an interrupt.
15-13	RESERVED	R	0h	Reserved
12	UTPEE	R/W	0h	UTP Error Enable When set and the UFS_IS[12] UTPES bit is set, the controller shall generate an interrupt.
11	DFEE	R/W	0h	Device Fatal Error Enable When set and the UFS_IS[11] DFES bit is set, the host controller shall generate an interrupt.

Table 19-92. UFS_IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	UCCE	R/W	0h	UIC COMMAND Completion Enable When set and the UFS_IS[10] UCCS bit is set, the host controller shall generate an interrupt.
9	UTMRCE	R/W	0h	UTP Task Management Request Completion Enable When set and the UFS_IS[9] UTMRCs bit is set, the host controller shall generate an interrupt.
8	ULSSE	R/W	0h	UIC Link Startup Status Enable When set and the UFS_IS[8] ULSS bit is set, the controller shall generate an interrupt.
7	ULLSE	R/W	0h	UIC Link Lost Status Enable When set and the UFS_IS[7] ULLS bit is set, the controller shall generate an interrupt.
6	UHESE	R/W	0h	UIC Hibernate Enter Status Enable When set and the UFS_IS[6] UHES bit is set, the controller shall generate an interrupt.
5	UHXSE	R/W	0h	UIC Hibernate Exit Status Enable When set and the UFS_IS[5] UHXS bit is set, the controller shall generate an interrupt.
4	UPMSE	R/W	0h	UIC Power Mode Status Enable When set and the UFS_IS[4] UPMS bit is set, the controller shall generate an interrupt.
3	UTMSE	R/W	0h	UIC Test Mode Status Enable When set and the UFS_IS[3] UTMS bit is set, the controller shall generate an interrupt.
2	UEE	R/W	0h	UIC Error Enable When set and the UFS_IS[2] UEE bit is set, the controller shall generate an interrupt.
1	UDEPRIE	R/W	0h	UIC DME_ENDPOINTRESET When set and the UFS_IS[1] UDEPRI bit is set, the controller shall generate an interrupt.
0	UTRCE	R/W	0h	UTP Transfer Request Completion Enable When set and the UFS_IS[0] UTRCS bit is set, the host controller shall generate an interrupt.

19.3.8 UFS_HCS Register (Offset = 30h) [reset = 0h]

UFS_HCS is shown in [Figure 19-32](#) and described in [Table 19-94](#).

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Host Controller Status Register

The software shall check that the UFS_HCS[2] UTMRLRDY bit is set to 1h before issuing a Task Management command.

The software shall check that the UFS_HCS[1] UTRLRDY bit is set to 1h before issuing an UTP command.

The prerequisite to send any DME command is that the UFS_HCS[0] HCE and UFS_HCS[3] UCRDY bits are set to 1h. The hardware does not check nor restrict the usage of any UIC command.

Sending the DME_ENABLE UIC command is not permitted.

Additional UIC command specific prerequisites:

DME cmd = DME_SET, DP = Don't care, UIC state = Don't care

DME cmd = DME_GET, DP = Don't care, UIC state = Don't care

DME cmd = DME_PEER_SET, DP = 1, UIC state = LinkUp

DME cmd = DME_PEER_GET, DP = 1, UIC state = LinkUp

DME cmd = DME_RESET, DP = Don't care, UIC state = Don't care

DME cmd = DME_ENPOINTRESET, DP = 1, UIC state = LinkUp

DME cmd = DME_LINKSTARTUP, DP = 0, UIC state = LinkDown

DME cmd = DME_HIBERNATE_ENTER, DP = Don't care, UIC state = LinkUp, LinkDown

DME cmd = DME_HIBERNATE_EXIT, DP = 0, UIC state = Hibernate

Table 19-93. UFS_HCS Instances

Instance	Physical Address
UFS	04E8 4030h

Figure 19-32. UFS_HCS Register

31	30	29	28	27	26	25	24
TLUNUTPE							
R-0h							
23	22	21	20	19	18	17	16
TTAGUTPE							
R-0h							
15	14	13	12	11	10	9	8
UTPEC				RESERVED	UPMCRS		
R-0h				R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED				UCRDY	UTMRLRDY	UTRLRDY	DP
R-0h				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 19-94. UFS_HCS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TLUNUTPE	R	0h	Target LUN of UTP Error The LUN of the command that a UTP error occurs during execution of the command. This field is valid only when the UFS_IS[12] UTPES bit is set. It is automatically reset by the UFS host controller when the UFS_IS[12] UTPES bit is cleared.

Table 19-94. UFS_HCS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	TTAGUTPE	R	0h	<p>Task Tag of UTP Error</p> <p>The Task Tag of the command that a UTP error occurs during execution of the command.</p> <p>This field is valid only when the UFS_IS[12] UTPES bit is set. It is automatically reset by the UFS host controller when the UFS_IS[12] UTPES is cleared.</p>
15-12	UTPEC	R	0h	<p>UTP Error Code</p> <p>Indicate that the error code of a UTP layer error.</p> <p>This field is valid only when the UFS_IS[12] UTPES bit is set. It is automatically reset by the UFS host controller when the UFS_IS[12] UTPES bit is cleared.</p> <p>0h = Reserved 1h = Invalid Transaction Type 2h-Fh = Reserved</p>
11	RESERVED	R	0h	Reserved
10-8	UPMCRS	R	0h	<p>UIC Power Mode Change Request Status</p> <p>Indicate that the status of a UIC layer request for power mode change.</p> <p>Value Description:</p> <p>0h = PWR_OK. The request was accepted. 1h = PWR_LOCAL. The local request was successfully applied. 2h = PWR_REMOTE. The remote request was successfully applied. Not used since this is associated to an UIC power mode change request from the UFS Device, which is not permitted. 3h = PWR_BUSY. The request was aborted due to concurrent requests. Not used since this is associated to an UIC power mode change request from the UFS Device, which is not permitted. 4h = PWR_ERROR_CAP. The request was rejected because the requested configuration exceeded the Link's capabilities. 5h = PWR_FATAL_ERROR. The request was aborted due to a communication problem. The Link may be inoperable. 6h-7h = Reserved</p>
7-4	RESERVED	R	0h	Reserved
3	UCRDY	R	0h	<p>UIC COMMAND Ready</p> <p>This bit indicates whether the host controller is ready to process UIC COMMAND.</p> <p>Host software shall only set the UFS_UICCMD register if the UFS_HCS[3] UCRDY bit is set to 1h.</p> <p>This bit is set to 1h if all of the following conditions are true:</p> <ul style="list-style-type: none"> - UFS_IS[11] DFES = 0h - UFS_IS[16] HCFES = 0h <p>No UIC command has been issued or the outstanding UIC command has been completed (UFS_IS[10] UCCS = 1h).</p> <p>This bit is cleared to 0h by host controller when one of the following conditions occur:</p> <ul style="list-style-type: none"> UFS_IS[11] DFES = 1h UFS_IS[16] HCFES = 1h <p>A write access to the UFS_UICCMD register.</p>

Table 19-94. UFS_HCS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UTMRLRDY	R	0h	<p>UTP Task Management Request List Ready</p> <p>This bit is set to 1h if all of the following conditions are true:</p> <ul style="list-style-type: none"> - UFS_HCS[0] DP = 1h - UFS_UTMRLDBR less than FFh - UFS_IS[11] DFES = 0h - UFS_IS[16] HCFES = 0h <p>This bit is cleared to 0h by host controller when one of the following conditions occur:</p> <ul style="list-style-type: none"> - UFS_HCS[0] DP = 0h - UFS_UTMRLDBR = FFh - UFS_IS[11] DFES = 1h - UFS_IS[16] HCFES == 1h <p>Host software shall only set the UFS_UTMRLRSR register if the UFS_HCS[2] UTMRLRDY bit is set to 1h.</p>
1	UTRLRDY	R	0h	<p>UTP Transfer Request List Ready</p> <p>This bit is set to 1h if all of the following conditions are true:</p> <ul style="list-style-type: none"> - UFS_HCS[0] DP = 1h - UFS_UTRLDBR less than FFFF FFFFh - UFS_IS[11] DFES = 0h - UFS_IS[16] HCFES = 0h <p>This bit is cleared to 0h by host controller when one of the following conditions occur:</p> <ul style="list-style-type: none"> - UFS_HCS[0] DP = 0h - UFS_UTRLDBR = FFFF FFFFh - UFS_IS[11] DFES = 1h - UFS_IS[16] HCFES = 1h <p>Host software shall only set the UFS_UTRLRSR register to 1h if the UFS_HCS[1] UTRLRDY bit is set to 1h.</p>
0	DP	R	0h	<p>Device Present</p> <p>This bit is set to 1h when an UFS device is attached to the controller. This bit is cleared to 0h when non-volatile memory is not attached to this controller.</p> <p>The UFS_HCS[0] DP bit is set to 1h if the UIC layer is in the LinkUp power state.</p>

19.3.9 UFS_HCE Register (Offset = 34h) [reset = 0h]

UFS_HCE is shown in [Figure 19-33](#) and described in [Table 19-96](#).

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Host Controller Enable Register

Table 19-95. UFS_HCE Instances

Instance	Physical Address
UFS	04E8 4034h

Figure 19-33. UFS_HCE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CGE	HCE	
R-0h													R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-96. UFS_HCE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	CGE	R/W	0h	Crypto General Enable Enable/Disable bit for Crypto Engine. This bit is functional only, if the crypto engine is implemented. 0h = Disable cryptographic operations for all transactions. 1h = Enable cryptographic for transactions where UTRD.CE = 1h.
0	HCE	R/W	0h	Host Controller Enable When set to 1h, host controller will autonomously go through the following initialization sequence: 1) Warm hardware reset of the UFS Host Controller 2) DME_RESET 3) DME_ENABLE The UFS_HCE[0] HCE bit stays 0h during the initialization sequence. In case the DME_ENABLE is not successful, the UFS_HCE stays 0h. If the initialization sequence is successful, the UFS_HCE[0] HCE bit becomes 1h. When the UFS_HCE register is cleared to 0h, the UFS Host Controller is disabled and register values except for the UFS_CAP register are volatile and may lose their content. If the UFS_HCE[0] HCE bit is 1h and a 0h is written to the UFS_HCE register, the UFS_HCE[0] HCE bit stays 1h until all outstanding system bus read requests are completed.

19.3.10 UFS_UECPA Register (Offset = 38h) [reset = 0h]

UFS_UECPA is shown in [Figure 19-34](#) and described in [Table 19-98](#).

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Host Controller UIC Error Code PHY Adapter Layer Register

Note: The register content is automatically cleared after reading.

Table 19-97. UFS_UECPA Instances

Instance	Physical Address
UFS	04E8 4038h

Figure 19-34. UFS_UECPA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERR	RESERVED														
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											EC				
R-0h											R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 19-98. UFS_UECPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERR	R	0h	UIC PHY Adapter Layer Error Indicates whether an error was generated by the PHY Adapter Layer.
30-5	RESERVED	R	0h	Reserved
4-0	EC	R	0h	UIC Adapter Layer Error Error code generated when the UFS_IS[2] UE and UFS_UECPA[31] bits ERR are set to 1h. Bit Description: 0h = PHY error on Lane 0 1h = PHY error on Lane 1 (Fixed to 0 since only Lane 0 is supported) 2h = PHY error on Lane 2 (Fixed to 0 since only Lane 0 is supported) 3h = PHY error on Lane 3 (Fixed to 0 since only Lane 0 is supported) 4h = Generic PHY Adapter error is flagged in case of a line reset that is either initiated by the local or peer device.

19.3.11 UFS_UECDL Register (Offset = 3Ch) [reset = 0h]

UFS_UECDL is shown in [Figure 19-35](#) and described in [Table 19-100](#).

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Host UIC Error Code Data Link Layer Register

Note: The register content is automatically cleared after reading.

Table 19-99. UFS_UECDL Instances

Instance	Physical Address
UFS	04E8 403Ch

Figure 19-35. UFS_UECDL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERR	RESERVED														
R-0h	R-0h														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED	EC														
R-0h	R-0h														

LEGEND: R = Read Only; -n = value after reset

Table 19-100. UFS_UECDL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERR	R	0h	UIC Data Link Layer Error Indicates whether an error was generated by the Data Link Layer.
30-15	RESERVED	R	0h	Reserved
14-0	EC	R	0h	UIC Data Link Layer Error Error code generated when the UFS_IS[2] UE and UFS_UECDL[31] ERR bits are set to 1h. Reader is referred to UniPro Specification (UNIPRO) for the definition of the error codes. Bit Description: 1h = NAC_RECEIVED 2h = TCx_REPLAY_TIMER_EXPIRED 3h = AFCx_REQUEST_TIMER_EXPIRED 4h = FCx_PROTECTION_TIMER_EXPIRED 5h = CRC_ERROR 6h = RX_BUFFER_OVERFLOW 7h = MAX_FRAME_LENGTH_EXCEEDED 8h = WRONG_SEQUENCE_NUMBER 9h = AFC_FRAME_SYNTAX_ERROR 10h = NAC_FRAME_SYNTAX_ERROR 11h = EOF_SYNTAX_ERROR 12h = FRAME_SYNTAX_ERROR 13h = BAD_CTRL_SYMBOL_TYPE 14h = PA_INIT_ERROR 15h = PA_ERROR_IND_RECEIVED

19.3.12 UFS_UECN Register (Offset = 40h) [reset = 0h]

UFS_UECN is shown in [Figure 19-36](#) and described in [Table 19-102](#).

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Host UIC Error Code Network Layer Register

Note: The register content is automatically cleared after reading.

Table 19-101. UFS_UECN Instances

Instance	Physical Address
UFS	04E8 4040h

Figure 19-36. UFS_UECN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERR	RESERVED														
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													EC		
R-0h													R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 19-102. UFS_UECN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERR	R	0h	UIC Network Layer Error Indicates whether an error was generated by the Network Layer.
30-3	RESERVED	R	0h	Reserved
2-0	EC	R	0h	UIC Network Layer Error Code Error code generated when the UFS_IS[2] UE and UFS_UECN[31] ERR bits are set to 1h. Reader is referred to UniPro Specification (UNIPRO) for the definition of the error codes. Bit Description: 0h = UNSUPPORTED_HEADER_TYPE 1h = BAD_DEVICEID_ENC 2h = LHDR_TRAP_PACKET_DROPPING

19.3.13 UFS_UECT Register (Offset = 44h) [reset = 0h]

UFS_UECT is shown in [Figure 19-37](#) and described in [Table 19-104](#).

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Host UIC Error Code Transport Layer Register

Note: The register content is automatically cleared after reading.

Table 19-103. UFS_UECT Instances

Instance	Physical Address
UFS	04E8 4044h

Figure 19-37. UFS_UECT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERR	RESERVED														
R-0h	R-0h														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									EC						
R-0h									R-0h						

LEGEND: R = Read Only; -n = value after reset

Table 19-104. UFS_UECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERR	R	0h	UIC Transport Layer Error Indicates whether an error was generated by the Transport Layer.
30-7	RESERVED	R	0h	Reserved
6-0	EC	R	0h	UIC Transport Layer Error Code Error code generated when the UFS_IS[2] UE and UFS_UECT[31] ERR bits are set to 1h. Reader is referred to UniPro Specification (UNIPRO) for the definition of the error codes. Bit Description: 0h = UNSUPPORTED_HEADER_TYPE 1h = UNKNOWN_CPORTID 2h = NO_CONNECTION_RX 3h = CONTROLLED_SEGMENT_DROPPING 4h = BAD_TC 5h = E2E_CREDIT_OVERFLOW 6h = SAFETY_VALVE_DROPPING

19.3.14 UFS_UECDME Register (Offset = 48h) [reset = 0h]

UFS_UECDME is shown in [Figure 19-38](#) and described in [Table 19-106](#).

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Host UIC Error Code DME Register

The UFS_UECDME register is reserved for future use and is fixed to 0000 0000h.

Note: The register content is automatically cleared after reading.

Table 19-105. UFS_UECDME Instances

Instance	Physical Address
UFS	04E8 4048h

Figure 19-38. UFS_UECDME Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERR	RESERVED														
R-0h	R-0h														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EC
R-0h															R-0h

LEGEND: R = Read Only; -n = value after reset

Table 19-106. UFS_UECDME Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERR	R	0h	UIC DME Error Indicates whether an error was generated by the DME.
30-1	RESERVED	R	0h	Reserved
0	EC	R	0h	UIC DME Error Code Error code generated when the UFS_IS[2] UE and UFS_UECDME[31] ERR bits are set to 1h. Bit Description: 0h = Generic DME error

19.3.15 UFS_UTRIACR Register (Offset = 4Ch) [reset = 0h]

UFS_UTRIACR is shown in [Figure 19-39](#) and described in [Table 19-108](#).

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UTP Transfer Request Interrupt Aggregation Control Register

Table 19-107. UFS_UTRIACR Instances

Instance	Physical Address
UFS	04E8 404Ch

Figure 19-39. UFS_UTRIACR Register

31	30	29	28	27	26	25	24
IAEN	RESERVED						IAPWEN
R/W-0h	R-0h						R/W-0h
23	22	21	20	19	18	17	16
RESERVED			IASB	RESERVED			CTR
R-0h			R-0h	R-0h			W-0h
15	14	13	12	11	10	9	8
RESERVED			IACTH				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
IATOVAL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 19-108. UFS_UTRIACR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IAEN	R/W	0h	Interrupt Aggregation Enable/Disable When set to 0h by host software, command responses are not counted nor timed. Interrupts are still triggered by responses where the interrupt bit is set in the UTRD. When set to 1h, the interrupt aggregation mechanism is enabled and aggregation-based interrupts are generated.
30-25	RESERVED	R	0h	Reserved
24	IAPWEN	R/W	0h	Interrupt Aggregation Parameter Write Enable When host software writes 1h, the values in the UFS_UTRIACR[12-8] IACTH and UFS_UTRIACR[7-0] IATOVAL bit fields are updated with the contents written at the same cycle. When host software writes 0h, the values in the UFS_UTRIACR[12-8] IACTH and UFS_UTRIACR[7-0] IATOVAL bit fields are not updated. Note: Write operations to the UFS_UTRIACR[12-8] IACTH and UFS_UTRIACR[7-0] IATOVAL bit fields are only allowed when no commands are outstanding.
23-21	RESERVED	R	0h	Reserved

Table 19-108. UFS_UTRIACR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	IASB	R	0h	<p>Interrupt Aggregation Status Bit</p> <p>This bit indicates to Host software whether any responses have been received and counted towards interrupt aggregation (the UFS_UTRIACR[20] IASB bit is set if IA (Interrupt Aggregation) counter greater than 0).</p> <p>Bit Value Description:</p> <p>0h = No commands has been received since last counter reset (IA counter == 0h)</p> <p>1h = At least one command has been received and counted (IA counter greater than 0h)</p>
19-17	RESERVED	R	0h	Reserved
16	CTR	W	0h	<p>Counter and Timer Reset</p> <p>When host software writes 1h, the interrupt aggregation timer and counter are reset.</p> <p>It is recommended that host software use this bit to reset the timer and counter every time it services newly received UTP responses.</p>
15-13	RESERVED	R	0h	Reserved
12-8	IACTH	R/W	0h	<p>Interrupt Aggregation Counter Threshold</p> <p>Host software uses this field to configure the number of responses that are required to generate an interrupt.</p> <p>As UTP responses are received by the host controller, they are counted.</p> <p>When the count reaches the value configured in this field, an interrupt is generated (the UFS_IS[0] UTRCS bit is set).</p> <p>The maximum allowed value is 31.</p> <p>Note: When the UFS_UTRIACR[12-8] IACTH bit field is 0h, responses are not counted, and counting-based interrupts are not generated.</p> <p>In order to write to this field, the UFS_UTRIACR[24] IAPWEN bit must be set at the same write operation.</p>
7-0	IATOVAL	R/W	0h	<p>Interrupt Aggregation Timeout Value</p> <p>Host software uses this field to configure the maximum time allowed between a response arrival to the host controller and the generation of an interrupt.</p> <p>Timer Operation: The timer is reset by software during the interrupt service routine.</p> <p>It starts running when the host controller receives the first response to a Regular Command, after the timer was reset.</p> <p>The timer stops when it reaches the value configured in the UFS_UTRIACR[7-0] IATOVAL bit field, and UFS_IS[0] UTRCS bit is set.</p> <p>Note: When the UFS_UTRIACR[7-0] IATOVAL bit field is 0h, the timer is not running, and timer-based interrupts are not generated.</p> <p>The Time units in this field are 40 μs.</p> <p>Therefore, writing 0x01 represents a time-out value of 40 μs, and writing 0xFF represents a time-out value of 10.2 ms</p>

19.3.16 UFS_UTRLBA Register (Offset = 50h) [reset = 0h]

UFS_UTRLBA is shown in [Figure 19-40](#) and described in [Table 19-110](#).

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UTP Transfer Request List Base Address Register

Table 19-109. UFS_UTRLBA Instances

Instance	Physical Address
UFS	04E8 4050h

Figure 19-40. UFS_UTRLBA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UTRLBA										RESERVED																					
R/W-0h										R-0h																					

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-110. UFS_UTRLBA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	UTRLBA	R/W	0h	UTP Transfer Request List Base Address Indicates the 32-bit base physical address for the UTP Transfer Request list. This base is used when fetching commands for execution. The structure pointed to by this address range is 1 KB in length. This address shall be 1 KB aligned as indicated by bits 9-0 being read only.
9-0	RESERVED	R	0h	Reserved

19.3.17 UFS_UTRLBAU Register (Offset = 54h) [reset = 0h]

UFS_UTRLBAU is shown in [Figure 19-41](#) and described in [Table 19-112](#).

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UTP Transfer Request List Base Address Upper 32-bits Register

Note: Since this UFS host controller implementation supports an 32-bit address bus, the upper 32-bit of the base address are ignored.

Table 19-111. UFS_UTRLBAU Instances

Instance	Physical Address
UFS	04E8 4054h

Figure 19-41. UFS_UTRLBAU Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UTRLBAU																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-112. UFS_UTRLBAU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UTRLBAU	R/W	0h	UTP Transfer Request List Base Address Upper Indicates the upper 32-bits for the UTP Transfer Request list base physical address. This base is used when fetching commands for execution.

19.3.18 UFS_UTRLDBR Register (Offset = 58h) [reset = 0h]

UFS_UTRLDBR is shown in [Figure 19-42](#) and described in [Table 19-114](#).

Return to [Summary Table](#).

UTP Transfer Request List Door Bell Register

This register controls the basic actions of the host controller.

Table 19-113. UFS_UTRLDBR Instances

Instance	Physical Address
UFS	04E8 4058h

Figure 19-42. UFS_UTRLDBR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UTRLDBR																															
R/W1S-0h																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-114. UFS_UTRLDBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UTRLDBR	R/W1S	0h	<p>UTP Transfer Request List Door Bell Register</p> <p>This field is bit significant.</p> <p>Each bit corresponds to a slot in the UTP Transfer Request List, where bit 0 corresponds to request slot 0.</p> <p>A bit in this field is set to 1h by host software to indicate to the host controller that a transfer request has been built in system memory for the associated transfer request slot and may be ready for execution. The host software indicates no change to request slots by setting the associated bits in this field to 0h.</p> <p>Bits in this field shall only be set 1h or 0h by host software when the UFS_UTRLRSR register is set to 1h.</p> <p>When a transfer request is completed (with success or error), the corresponding bit is cleared to 0h by the host controller.</p> <p>The host controller always process transfer requests in-order according to the order submitted to the list.</p> <p>In case of multiple commands with single door bell register ringing (batch mode), The dispatch order for these transfer requests by host controller will base on their index in the List.</p> <p>A transfer request with lower index value will be executed before a transfer request with higher index value.</p> <p>This field is also cleared when the UFS_UTRLRSR register is written from a 1h to a 0h by host software.</p>

19.3.19 UFS_UTRLCLR Register (Offset = 5Ch) [reset = 0h]

UFS_UTRLCLR is shown in [Figure 19-43](#) and described in [Table 19-116](#).

Return to [Summary Table](#).

UTP Transfer Request List Clear Register

Table 19-115. UFS_UTRLCLR Instances

Instance	Physical Address
UFS	04E8 405Ch

Figure 19-43. UFS_UTRLCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UTRLCLR																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-116. UFS_UTRLCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UTRLCLR	W	0h	<p>UTP Transfer Request List Clear</p> <p>This field is bit significant.</p> <p>Each bit corresponds to a slot in the UTP Transfer Request List, where bit 0 corresponds to request slot 0.</p> <p>A bit in this field is set to 0h by host software to indicate to the host controller that a transfer request slot is cleared.</p> <p>The host controller shall free up any resources associated to the request slot immediately, and shall set the associated bit in the UFS_UTRLDBR register to 0h.</p> <p>The host software indicates no change to request slots by setting the associated bits in this field to 1h.</p> <p>Bits in this field shall only be set 1h or 0h by host software when the UFS_UTRLRSR register is set to 1h.</p> <p>The host software shall use this field only when a UTP Transfer Request is expected to not be completed, for example: when a Transfer Request was aborted, or in case of a system bus error, such as an invalid UTRD.</p>

19.3.20 UFS_UTRLRSR Register (Offset = 60h) [reset = 0h]

UFS_UTRLRSR is shown in [Figure 19-44](#) and described in [Table 19-118](#).

Return to [Summary Table](#).

UTP Transfer Request List Run Stop Register

This register controls the command processing of the UFS host controller.

Table 19-117. UFS_UTRLRSR Instances

Instance	Physical Address
UFS	04E8 4060h

Figure 19-44. UFS_UTRLRSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							UTRLRSR
R-0h							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-118. UFS_UTRLRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	UTRLRSR	R/W	0h	UTP Transfer Request List Run-Stop When set to 1h, the host controller may process the list. Host controller starts processing the list at entry 0h. The host controller continues process the list as long as this bit is set to a 1h. When cleared to 0h, the host controller shall continue to complete all the outstanding transfer requests in the list and then stop. This bit shall only be set to 1h when the UFS_HCS[1] UTRLRDY bit is set to 1h.

19.3.21 UFS_UTRLCNR Register (Offset = 64h) [reset = 0h]

UFS_UTRLCNR is shown in [Figure 19-45](#) and described in [Table 19-120](#).

Return to [Summary Table](#).

UTP Transfer Request List Completion Notification Register

Table 19-119. UFS_UTRLCNR Instances

Instance	Physical Address
UFS	04E8 4064h

Figure 19-45. UFS_UTRLCNR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UTRLCNR																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-120. UFS_UTRLCNR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UTRLCNR	R/W1C	0h	<p>UTP Transfer Request List Completion Notification Register</p> <p>This field is bit significant.</p> <p>Each bit corresponds to a slot in the UTP Transfer Request List, where bit 0 corresponds to request slot 0.</p> <p>A bit in this field is set to 1h by the host controller when a transfer request from the associated transfer request slot has completed (with success or error).</p> <p>The host controller sets the bit at the same time it clears the bit with the same index in the UFS_UTRLDBR register.</p> <p>Host software is expected to clear the bit, by writing 1h to it, after processing the completed task.</p> <p>Clearing a bit in this register shall have no effect on the hardware, other than changing the value of this register.</p> <p>The host controller shall clear this register when the UFS_UTRLRSR register is written from a 0h to a 1h by host software.</p>

19.3.22 UFS_UTMRLBA Register (Offset = 70h) [reset = 0h]

UFS_UTMRLBA is shown in [Figure 19-46](#) and described in [Table 19-122](#).

Return to [Summary Table](#).

UTP Task Management Request List Base Address

Table 19-121. UFS_UTMRLBA Instances

Instance	Physical Address
UFS	04E8 4070h

Figure 19-46. UFS_UTMRLBA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UTMRLBA																						RESERVED									
R/W-0h																						R-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-122. UFS_UTMRLBA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	UTMRLBA	R/W	0h	UTP Task Management Request List Base Address Indicates the 32-bit base physical address for the list. This base is used when fetching Task Management Functions for execution. The structure pointed to by this address range is 1 KB in length. This address shall be 1 KB aligned as indicated by bits 9-0 being read only.
9-0	RESERVED	R	0h	Reserved

19.3.23 UFS_UTMRLBAU Register (Offset = 74h) [reset = 0h]

UFS_UTMRLBAU is shown in [Figure 19-47](#) and described in [Table 19-124](#).

Return to [Summary Table](#).

UTP Task Management Request List Base Address Upper 32-bits Register

Note: This register is only used when the host is configured to use a 64-bit address bus.

Table 19-123. UFS_UTMRLBAU Instances

Instance	Physical Address
UFS	04E8 4074h

Figure 19-47. UFS_UTMRLBAU Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UTMRLBAU																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-124. UFS_UTMRLBAU Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	UTMRLBAU	R/W	0h	UTP Task Management Request List Base Address Indicates the upper 32-bits for the list base physical address. This base is used when fetching task management functions for execution.

19.3.24 UFS_UTMRLDBR Register (Offset = 78h) [reset = 0h]

UFS_UTMRLDBR is shown in [Figure 19-48](#) and described in [Table 19-126](#).

Return to [Summary Table](#).

UTP Task Management Request List Door Bell Register

Table 19-125. UFS_UTMRLDBR Instances

Instance	Physical Address
UFS	04E8 4078h

Figure 19-48. UFS_UTMRLDBR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								UTMRLDBR							
R-0h																								R/W1S-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-126. UFS_UTMRLDBR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	UTMRLDBR	R/W1S	0h	<p>UTP Task Management Request List Doorbell Register</p> <p>This field is bit significant.</p> <p>Each bit corresponds to a task management request slot in the List, where bit 0 corresponds to T slot 0.</p> <p>This field is set by host software to indicate to the host controller that a task management request has been built in system memory and may be ready for execution.</p> <p>When a task management request is completed (with success or error), the corresponding bit is cleared to 0h by the host controller. Bits in this field shall only be set to 1h by host software when the UFS_UTMRLRSR register is set to 1h.</p> <p>The host controller always process task management request in-order according to the order submitted to the list.</p> <p>In case of multiple requests with single door bell register ringing (batch mode), The dispatch order for these requests by host controller will base on their index in the List.</p> <p>A task management with lower index value will be executed before a task management request with higher index value.</p> <p>This field is also cleared when the UFS_UTMRLRSR register is written from a 1h to a 0h by host software.</p>

19.3.25 UFS_UTMRLCLR Register (Offset = 7Ch) [reset = 0h]

UFS_UTMRLCLR is shown in [Figure 19-49](#) and described in [Table 19-128](#).

Return to [Summary Table](#).

UTP Task Management Request List Clear Register

Table 19-127. UFS_UTMRLCLR Instances

Instance	Physical Address
UFS	04E8 407Ch

Figure 19-49. UFS_UTMRLCLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								UTMRLCLR							
R-0h																								W-0h							

LEGEND: W = Write Only; -n = value after reset

Table 19-128. UFS_UTMRLCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	UTMRLCLR	W	0h	<p>UTP Task Management List Clear Register</p> <p>This field is bit significant.</p> <p>Each bit corresponds to a slot in the task management request List, where bit 0 corresponds to slot 0.</p> <p>A bit in this field is set to 0h by host software to indicate to the host controller that a task management request slot is cleared.</p> <p>The host controller shall free up any resources associated to the task management request slot immediately, and shall set the associated bit in the UFS_UTMRLDBR register to 0h.</p> <p>The host software indicates no change to task management request slots by setting the associated bits in this field to 1h.</p> <p>Bits in this field shall only be set 1h or 0h by host software when the UFS_UTRLRSR register is set to 1h.</p> <p>The host software shall use this field only when a UTP Task Management Request is expected to not be completed, for example: in case of a system bus error, such as an invalid UTMRD.</p>

19.3.26 UFS_UTMRLRSR Register (Offset = 80h) [reset = 0h]

UFS_UTMRLRSR is shown in [Figure 19-50](#) and described in [Table 19-130](#).

Return to [Summary Table](#).

UFS_UTMRLRSR - UTP Task Management Request List Run Stop Register

Table 19-129. UFS_UTMRLRSR Instances

Instance	Physical Address
UFS	04E8 4080h

Figure 19-50. UFS_UTMRLRSR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							UTMRLRSR
R-0h							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-130. UFS_UTMRLRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	UTMRLRSR	R/W	0h	<p>UTP Task Management Request List Run-Stop Register</p> <p>When set to 1h, the host controller may process the list. Host controller starts processing the list at entry 0h. The host controller continues process the list as long as this bit is set to a 1h.</p> <p>When cleared to 0h, the host controller shall continue to complete all the outstanding task management requests in the list and then stop. This bit shall only be set to 1h when the UFS_HCS[2] UTMRLRDY is set to 1h.</p>

19.3.27 UFS_UICC_CMD Register (Offset = 90h) [reset = 0h]

UFS_UICC_CMD is shown in [Figure 19-51](#) and described in [Table 19-132](#).

Return to [Summary Table](#).

UIC Command Register

Sending the DME_ENABLE UIC command is not permitted since this will be done automatically during the UFS host controller initialization.

Table 19-131. UFS_UICC_CMD Instances

Instance	Physical Address
UFS	04E8 4090h

Figure 19-51. UFS_UICC_CMD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								CMDOP							
R-0h																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-132. UFS_UICC_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	CMDOP	R/W	0h	<p>Command Opcode</p> <p>Indicate the Opcode of a UIC Command to be dispatched to local UIC layer.</p> <p>When this register is set, the host controller shall take the values of UICC_CMDARGx as the corresponding parameters (input and output) that are a part of the UIC Command.</p> <p>Opcode UIC Command Configuration:</p> <p>1h: DME_GET</p> <p>2h: DME_SET</p> <p>3h: DME_PEER_GET</p> <p>4h: DME_PEER_SET</p> <p>5h-Fh: Reserved</p> <p>Control:</p> <p>10h-11h: Reserved</p> <p>12h: DME_ENABLE (Not permitted)</p> <p>13h: Reserved</p> <p>14h: DME_RESET</p> <p>15h: DME_ENDPOINTRESET</p> <p>16h: DME_LINKSTARTUP</p> <p>17h: DME_HIBERNATE_ENTER</p> <p>18h: DME_HIBERNATE_EXIT</p> <p>19h-FFh: Reserved</p>

19.3.28 UFS_UICCMDARG1 Register (Offset = 94h) [reset = 0h]

UFS_UICCMDARG1 is shown in [Figure 19-52](#) and described in [Table 19-134](#).

Return to [Summary Table](#).

UIC Command Argument 1 Register

MIBAttribute: Indicates the ID of the attribute of the requested. See MIPI UniPro Specification (UNIPRO) for the details of the MIBAttribute parameter.

GenSelectorIndex: Indicates the targeted M-PHY data lane or CPort or Test Feature when relevant. See MIPI UniPro Specification (UNIPRO) for the details of the GenSelectorIndex parameter.

Layer: L1 - Valid Range: 0 to 2×PA_MaxDataLanes - 1

Layer: L4/Cport - Valid Range: 0 to T_NumCPorts - 1

Layer: L4/Test Feature - Valid Range: 0 to T_NumTestFeatures - 1

ResetLevel: Indicates the reset type. See MIPI UniPro Specification (UNIPRO) for the details of the ResetLevel parameter.

0h - Cold Reset

1h - Warm Reset

2h-FFh - Reserved

Table 19-133. UFS_UICCMDARG1 Instances

Instance	Physical Address
UFS	04E8 4094h

Figure 19-52. UFS_UICCMDARG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																ARG1															
																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-134. UFS_UICCMDARG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ARG1	R/W	0h	<p>UIC Command Argument 1 (MIBAttribute, GenSelectorIndex, ResetLevel)</p> <p>This contains the value for the 1st argument of the UIC command if applicable.</p> <p>The content of this field varies with the UIC Command (UFS_UICCMD).</p> <p>UIC cmd = DME_GET:</p> <p>Bit[31-24] = MIBAttribute</p> <p>Bit[23-16] = MIBAttribute</p> <p>Bit[15-08] = GenSelectorIndex</p> <p>Bit[7-0] = GenSelectorIndex</p> <p>UIC cmd = DME_SET:</p> <p>Bit[31-24] = MIBAttribute</p> <p>Bit[23-16] = MIBAttribute</p> <p>Bit[15-08] = GenSelectorIndex</p> <p>Bit[7-0] = GenSelectorIndex</p> <p>UIC cmd = DME_PEER_GET:</p> <p>Bit[31-24] = MIBAttribute</p> <p>Bit[23-16] = MIBAttribute</p> <p>Bit[15-08] = GenSelectorIndex</p> <p>Bit[7-0] = GenSelectorIndex</p> <p>UIC cmd = DME_PEER_SET:</p> <p>Bit[31-24] = MIBAttribute</p> <p>Bit[23-16] = MIBAttribute</p> <p>Bit[15-08] = GenSelectorIndex</p> <p>Bit[7-0] = GenSelectorIndex</p> <p>UIC cmd = DME_POWERON:</p> <p>Bit[31-0] = Reserved</p> <p>UIC cmd = DME_POWEROFF:</p> <p>Bit[31-0] = Reserved</p> <p>UIC cmd = DME_ENABLE:</p> <p>Bit[31-0] = Reserved</p> <p>UIC cmd = DME_RESET:</p> <p>Bit[31-24] = Reserved</p> <p>Bit[23-16] = Reserved</p> <p>Bit[15-8] = Reserved</p> <p>Bit[07-0] = ResetLevel</p> <p>UIC cmd = DME_ENDPOINTRESET:</p> <p>Bit[31-0] = Reserved</p> <p>UIC cmd = DME_LINKSTARTUP:</p> <p>Bit[31-0] = Reserved</p> <p>UIC cmd = DME_HIBERNATE_ENTER:</p> <p>Bit[31-0] = Reserved</p> <p>UIC cmd = DME_HIBERNATE_EXIT:</p> <p>Bit[31-0] = Reserved</p> <p>UIC cmd = DME_TEST_MODE:</p> <p>Bit[31-0] = Reserved</p>

19.3.29 UFS_UICCMDARG2 Register (Offset = 98h) [reset = 0h]

UFS_UICCMDARG2 is shown in [Figure 19-53](#) and described in [Table 19-136](#).

Return to [Summary Table](#).

UIC Command Argument 2 Register

AttrSetType: Indicates whether the attribute value (AttrSet = NORMAL) or the attribute non-volatile reset value (STATIC) setting is requested. See MIPI UniPro Specification (UNIPRO) for the details of the AttrSetType parameter.

ConfigResultCode: Indicates the result of the UIC configuration command request. It is valid after host controller has set the UFS_IS[10] UCCS bit to 1h. See MIPI UniPro Specification (UNIPRO) for the details of the ConfigResultCode parameter.

0h = SUCCESS

1h = INVALID_MIB_ATTRIBUTE

2h = INVALID_MIB_ATTRIBUTE_VALUE

3h = READ_ONLY_MIB_ATTRIBUTE

4h = WRITE_ONLY_MIB_ATTRIBUTE

5h = BAD_INDEX

6h = LOCKED_MIB_ATTRIBUTE

7h = BAD_TEST_FEATURE_INDEX

8h = PEER_COMMUNICATION_FAILURE

9h = BUSY

Ah = DME_FAILURE

Bh-FFh = Reserved

GenericErrorCode: Indicates the result of the UIC control command request. It is valid after host controller has set the UFS_IS[10] UCCS bit to 1h. See MIPI UniPro Specification (UNIPRO) for the details of the GenericErrorCode parameter.

0h = SUCCESS

1h = FAILURE

2h-FFh = Reserved

Table 19-135. UFS_UICCMDARG2 Instances

Instance	Physical Address
UFS	04E8 4098h

Figure 19-53. UFS_UICCMDARG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																ARG2															
																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-136. UFS_UICCMDARG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ARG2	R/W	0h	<p>UIC Command Argument 2 (AttrSetType, ConfigResultCode, GenericErrorCode)</p> <p>This register contains the value for the 2nd argument of the UIC command if applicable.</p> <p>The content of this field vary with UIC Command.</p> <p>UIC Command = DME_GET: Bit[7-0] = ConfigResultCode</p> <p>UIC Command = DME_SET: Bit[7-0] = ConfigResultCode</p> <p>UIC Command = DME_PEER_GET: Bit[7-0] = ConfigResultCode</p> <p>UIC Command = DME_PEER_SET: Bit[7-0] = ConfigResultCode</p> <p>UIC Command = DME_POWERON: Bit[7-0] = GenericErrorCode</p> <p>UIC Command = DME_POWEROFF: Bit[7-0] = GenericErrorCode</p> <p>UIC Command = DME_ENABLE: Bit[7-0] = GenericErrorCode</p> <p>UIC Command = DME_RESET: Bit[7-0] = Reserved</p> <p>UIC Command = DME_ENDPOINTRESET: Bit[7-0] = GenericErrorCode</p> <p>UIC Command = DME_LINKSTARTUP: Bit[7-0] = GenericErrorCode</p> <p>UIC Command = DME_HIBERNATE_ENTER: Bit[7-0] = GenericErrorCode</p> <p>UIC Command = DME_HIBERNATE_EXIT: Bit[7-0] = GenericErrorCode</p> <p>UIC Command = DME_TEST_MODE: Bit[7-0] = GenericErrorCode</p>

19.3.30 UFS_UICCMDARG3 Register (Offset = 9Ch) [reset = 0h]

UFS_UICCMDARG3 is shown in [Figure 19-54](#) and described in [Table 19-138](#).

Return to [Summary Table](#).

UIC Command Argument 3 Register

MIBvalue_R: Indicates the value of the attribute as returned by the UIC command returned. It is valid after host controller has set the UFS_IS[10] UCCS bit to 1h. See MIPI UniPro Specification (UNIPRO) for the details of the MIBvalue parameter.

MIBvalue_W: Indicates the value of the attribute to be set. See MIPI UniPro Specification (UNIPRO) for details of the MIBvalue parameter.

Table 19-137. UFS_UICCMDARG3 Instances

Instance	Physical Address
UFS	04E8 409Ch

Figure 19-54. UFS_UICCMDARG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARG3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-138. UFS_UICCMDARG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ARG3	R/W	0h	<p>Argument 3</p> <p>This register contains the value for the 3rd argument of the UIC command if applicable.</p> <p>The content of this field vary with UIC Command.</p> <p>UIC Command = DME_GET:</p> <p>Bit[31-0] = MIBvalue_R</p> <p>UIC Command = DME_SET:</p> <p>Bit[31-0] = MIBvalue_W</p> <p>UIC Command = DME_PEER_GET:</p> <p>Bit[31-0] = MIBvalue_R</p> <p>UIC Command = DME_PEER_SET:</p> <p>Bit[31-0] = MIBvalue_W</p> <p>UIC Command = DME_POWERON:</p> <p>Bit[31-0] = Reserved</p> <p>UIC Command = DME_POWEROFF:</p> <p>Bit[31-0] = Reserved</p> <p>UIC Command = DME_ENABLE:</p> <p>Bit[31-0] = Reserved</p> <p>UIC Command = DME_RESET:</p> <p>Bit[31-0] = Reserved</p> <p>UIC Command = DME_ENDPOINTRESET:</p> <p>Bit[31-0] = Reserved</p> <p>UIC Command = DME_LINKSTARTUP:</p> <p>Bit[31-0] = Reserved</p> <p>UIC Command = DME_HIBERNATE_ENTER:</p> <p>Bit[31-0] = Reserved</p> <p>UIC Command = DME_HIBERNATE_EXIT:</p> <p>Bit[31-0] = Reserved</p> <p>UIC Command = DME_TEST_MODE:</p> <p>Bit[31-0] = Reserved</p>

19.3.31 UFS_SYSTHRTL Register (Offset = A0h) [reset = 00181200h]

UFS_SYSTHRTL is shown in [Figure 19-55](#) and described in [Table 19-140](#).

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SYS Throttling Register

In case of heavy data traffic, the UFS host controller might not leave sufficient bandwidth of the OCP/AXI fabric for other peripheral. This register allows throttling the UFS host controller either by limiting the number of outstanding read requests on the OCP/AXI bus or by specifying a minimum delay between two consecutive OCP/AXI accesses.

Limiting the number of outstanding requests may also be required in case the bus fabric can only handle a limited amount of requests.

Table 19-139. UFS_SYSTHRTL Instances

Instance	Physical Address
UFS	04E8 40A0h

Figure 19-55. UFS_SYSTHRTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MAXOSYSRW							
R-0h								R/W-18h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXOSYSRR								SYSDLY							
R/W-12h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-140. UFS_SYSTHRTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24-16	MAXOSYSRW	R/W	18h	Max Outstanding SYS Write Requests (AXI Only) Actual limit of outstanding SYS write requests. This register value shall not be higher than specified by the P_P_RDP_MAX_OUTSTANDING parameter. Writing of illegal values is not checked or prohibited by the hardware. The default value is defined by the P_P_RDP_MAX_OUTSTANDING parameter, so that the Software knows the maximum allowed value by reading this register. 0h = no limitation 0xF = 15 outstanding requests
15-8	MAXOSYSRR	R/W	12h	Max Outstanding SYS Read Requests Actual limit of outstanding SYS read requests. This register value shall not be higher than specified by the P_P_WDP_MAX_OUTSTANDING parameter. Writing of illegal values is not checked or prohibited by the hardware. The default value is defined by the P_P_WDP_MAX_OUTSTANDING parameter, so that the Software knows the maximum allowed value by reading this register. 0h = no limitation 0xF = 15 outstanding requests Note: For the IP module with the OCP bus interface, this register defines the total number of outstanding request read and writes combined.

Table 19-140. UFS_SYSTHRTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SYSDLY	R/W	0h	<p>SYS Delay</p> <p>This register defines the minimum delay in host clock cycles between two system bus accesses.</p> <p>The register defines the delay for both, read and write channel.</p>

19.3.32 UFS_HCI_MMIO_TOSH_UNIRESPOL Register (Offset = ACh) [reset = 0h]

UFS_HCI_MMIO_TOSH_UNIRESPOL is shown in [Figure 19-56](#) and described in [Table 19-142](#).

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UniPro Reset Polling Register

Table 19-141. UFS_HCI_MMIO_TOSH_UNIRESPOL Instances

Instance	Physical Address
UFS	04E8 40ACh

Figure 19-56. UFS_HCI_MMIO_TOSH_UNIRESPOL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							RESPOL
R-0h							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-142. UFS_HCI_MMIO_TOSH_UNIRESPOL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	RESPOL	R/W	0h	<p>UniPro Reset Polling</p> <p>0h = Wait for power on ResetCnf pulse</p> <p>1h = Skip polling of ResetCnf</p> <p>When the UFSHCI come out of reset, the host controller interface will wait for LA_ResetCnf and then the UFSHCI enable request can be forwarded.</p> <p>At this point the Host Controller will wait again for LA_ResetCnf. Having this bit set to 1h will allow to skip the first waiting period.</p> <p>The default value of this register depends from the P_P_RESPOL_1B parameter.</p>

19.3.33 UFS_OSYSR Register (Offset = C4h) [reset = 0h]

UFS_OSYSR is shown in [Figure 19-57](#) and described in [Table 19-144](#).

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Outstanding SYS Requests Register

Table 19-143. UFS_OSYSR Instances

Instance	Physical Address
UFS	04E8 40C4h

Figure 19-57. UFS_OSYSR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				OSYSW						OSYSR					
R-0h																				R-0h						R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 19-144. UFS_OSYSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-6	OSYSW	R	0h	Outstanding SYS Write Requests This register gives the number of outstanding SYS write requests. In case the System Host writes a 0h to the UFS_HCE register, the UFS Host Controller stays enabled (UFS_HCE = 0) until all outstanding SYS write requests are completed, means OSYSW = 0.
5-0	OSYSR	R	0h	Outstanding SYS Read Requests This register gives the number of outstanding SYS read requests. In case the System Host writes a 0 to the UFS_HCE register, the UFS Host Controller stays enabled (UFS_HCE = 0h) until all outstanding SYS read requests are completed, means UFS_OSYSR = 0h. This register can be used to detect system bus problems. In case the system does not correctly return to 0h, the system bus may hang.

19.3.34 UFS_XCNF Register (Offset = C8h) [reset = 4h]

UFS_XCNF is shown in [Figure 19-58](#) and described in [Table 19-146](#).

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Extended Configuration Register

Table 19-145. UFS_XCNF Instances

Instance	Physical Address
UFS	04E8 40C8h

Figure 19-58. UFS_XCNF Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						PCPCONFEX	
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
DSGM		RESERVED	CAPWREN	RESERVED	MHSDIS	RESERVED	
R/W-0h		R-0h	R/W-0h	R-0h	R/W-0h	R-0h	
7	6	5	4	3	2	1	0
MCLKGE					AXIIDS	DSE	XRSE
R/W-0h					R/W-1h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-146. UFS_XCNF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	PCPCONFEX	R/W	0h	Peer C-Port Configuration Extended These bits configure the peer C-Port configuration. 0h = Standard, no action 1h = Standard, no action 2h = Peer C-Port 0 connection state polling 3h = Peer configuration by UFSHCI

Table 19-146. UFS_XCNF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	DSGM	R/W	0h	<p>Deep-Sleep Generation Mode</p> <p>These bits define, how and when the (MK2,MK2) pattern is sent by the UFS host controller.</p> <p>0h = Disabled</p> <p>Regardless of the UFS_XCNF[1] DSE bit setting, no (MK2,MK2) pattern is generated.</p> <p>1h = Use UFS_XCNF[1] DSE bit, static assignment.</p> <p>With this setting, the (MK2,MK2) pattern will be generated every time the TX path at the end of every data traffic, for example: when the data path has no more data to send.</p> <p>Although this setting will generate the required (MK2,MK2) sequence, the (MK2,MK2) pattern is generated too often and unnecessary guard time delays appear in the system.</p> <p>2h = Use UFS_ADSIT register and UFS_XCNF[1] DSE bit</p> <p>With this setting, the (MK2,MK2) pattern will be send after the auto-deep-sleep counter is expired.</p> <p>The method how the (MK2,MK2) pattern is sent, is via 0-byte payload, for example: at the end of the data transfer.</p> <p>This method also works when the device has not send a (MK2,MK2) with the final AFC.</p> <p>3h = Use UFS_ADSIT register and UFS_XCNF[1] DSE bit</p> <p>With this setting the, (MK2,MK2) pattern will be send after the auto-deep-sleep counter is expired.</p> <p>The method how the (MK2,MK2) pattern is send is via assertion of the UniPro burst signal, for example: filler pattern.</p> <p>This method will not work if the device has not sent the (MK2,MK2) pattern yet, as there are AFCs going back as a response to a filler sequence.</p> <p>The deep-sleep mode defines the way, how and when the (MK2,MK2) pattern will be generated.</p> <p>The LA_TxLastMessage setting is taken from the UFS_XCNF[1] DSE bit.</p>
13	RESERVED	R	0h	Reserved
12	CAPWREN	R/W	0h	<p>Capability Register Write Enable</p> <p>Setting this bit, will change the JEDEC capability register to be writable.</p> <p>0h = Default behavior.</p> <p>Capability register is read only.</p> <p>1h = Capability register can be written.</p> <p>This function can be used to verify different driver behavior.</p> <p>This is typically a debug feature and the register is most likely fixed in a production release.</p>
11	RESERVED	R	0h	Reserved
10	MHSDIS	R/W	0h	MHSDIS
9-8	RESERVED	R	0h	Reserved

Table 19-146. UFS_XCNF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-3	MCLKGE	R/W	0h	<p>Module Clock Gating Enable</p> <p>These bits enable or disable the hierarchical clock gating per module.</p> <p>[8] - UM support module clock gating enable/disable.</p> <p>[7] - OCS status word write module clock gating enable/disable.</p> <p>[6] - Read DMA data path module clock gating enable/disable.</p> <p>[5] - Write DMA data path module clock gating enable/disable.</p> <p>[4] - Command processing module clock gating enable/disable.</p> <p>[3] - Command fetching module clock gating enable/disable.</p> <p>All enable/disable bits follow the logic:</p> <p>0h = Hierarchical clock gating enabled.</p> <p>1h = Hierarchical clock gating disabled.</p> <p>The clocks are disabled at the individual module or function hierarchical boundary, based on internal status information, for example:</p> <p>the 'OCS status word write module' will not be clocked whenever there is no status word to be written.</p>
2	AXIIDS	R/W	1h	<p>AXI ID support</p> <p>0h = AXI ID support is disabled.</p> <p>1h = AXI ID support is enabled.</p>
1	DSE	R/W	0h	<p>Deep Sleep Enable</p> <p>This bit enables the extended (MK2,MK2) pattern generation.</p> <p>This extension is a MIPI UniPro features which allows saving power in the MPHY by turning off part of the MPHYs RX/TX logic - assuming that host and device are supporting deep-sleep.</p> <p>This happens transparent from the rest of the UFS system - unlike hibernate enter/exit which requires either host controller or software interaction.</p> <p>Internally, this bit is connected to the LA_TxLastMessage port of the UniPro IP, thus it allows for a static setting of the port.</p> <p>0h = LA_LastMessage is de-asserted.</p> <p>No last message is generated based on the setting in the UFS_XCNF register fields.</p> <p>Sending a (MK2,MK2) pattern is still possible by using the MMTR register.</p> <p>1h = LA_LastMessage is asserted.</p> <p>The (MK2,MK2) pattern is sent in the mode defined in the UFS_XCNF[15-14] DSGM bit field.</p> <p>Setting this bit to 1h and the UFS_XCNF[15-14] DSGM to 1h will always send a (MK2,MK2) pattern after the data transmission is complete.</p> <p>Depending on the traffic pattern, this may introduce additional guard time delay on the link.</p>
0	XRSE	R/W	0h	<p>Extended Register Space Enable</p> <p>This bit enables the extended register space.</p> <p>This register space is located directly on top of the JEDEC defined UFSHCI register addresses.</p> <p>0h = Extended Register Space not enabled.</p> <p>1h = Extended Register Space enabled.</p> <p>Before enabling the pseudo error register space, the UFS_XASB[5-0] XDP bit field has to be configured with the correct base address.</p>

19.3.35 UFS_ADSIT Register (Offset = CCh) [reset = 0h]

UFS_ADSIT is shown in [Figure 19-59](#) and described in [Table 19-148](#).

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Auto-Deep-Sleep Idle Timer Register

UFS utilizes UniPro and SCSI standards as its power management framework. To improve power efficiency, the UFS host controller may support a mechanism called deep-sleep.

Deep-Sleep allows the host controller to put the UFS link into deep-sleep state autonomously. Unlike hibernation, deep-sleep can be entered without input or information from the (UFS) application layer.

Thus, deep-sleep is transparent to the UFS software stack.

In case, both, Auto-Hibernate and Auto-DeepSleep are both enabled, the Auto Hibernate Time shall be set greater than the Auto DeepSleep Time:

UFS_AHIT[12-10] TS bit filed × UFS_AHIT[9-0] AH8ITV bit filed greater than UFS_ADSIT[12-10] TS bit filed × UFS_ADSIT[9-0] ADSTV bit filed

Table 19-147. UFS_ADSIT Instances

Instance	Physical Address
UFS	04E8 40CCh

Figure 19-59. UFS_ADSIT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TS		ADSTV											
R-0h																		R/W-0h						R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-148. UFS_ADSIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12-10	TS	R/W	0h	Time Scale Multiply value to increase count time 0h = Value times 1 μs 1h = Value times 10 μs 2h = Value times 100 μs 3h = Value times 1 ms 4h = Value times 10 ms 5h = Value times 100 ms 6h-7h = Reserved

Table 19-148. UFS_ADSIT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-0	ADSTV	R/W	0h	<p>Auto-Deep-Sleep Idle Timer Value</p> <p>This is the time that UFS subsystem must be idle before the UFS host controller may put the UFS link into deep-sleep state autonomously.</p> <p>The idle timer value is multiplied by the indicated timer scale to yield an absolute timer value.</p> <p>The idle timer starts decrement when all of the following conditions are satisfied:</p> <ul style="list-style-type: none"> - UFS_UTRLDBR = 0h - UFS_UTMRLDBR = 0h - No UIC commanding is outstanding <p>The idle timer shall continue decrement until it reaches zero or it is stopped as result of software access to one of host controller interface registers.</p> <p>When idle timer changes a non-zero to zero, the host controller shall put the UFS link into deep-sleep state.</p> <p>The host controller reloads this value each time the UFS link transitions out of the deep-sleep state.</p> <p>Software writes 0h to disable Auto-Deep-Sleep Idle Timer.</p> <p>Any non-zero value will enable Auto-Deep-Sleep idle timer.</p> <p>The minimum counter value is 1 μs, the maximum counter value is 102.3 s.</p> <p>The Auto-Deep-Sleep idle timer will trigger the generation of the (MK2,MK2) transfer.</p> <p>The method, how the (MK2,MK2) pattern is generated is defined in the UFC_XCFN[15-14] DSGM register:</p> <p>00b - Disabled.</p> <p>Setting this value will suppress any (MK2,MK2) pattern generation.</p> <p>Expiration of the auto-deep-sleep timer will have no effect.</p> <p>1h = Use the UFS_XCNF[1] DSE bit, static assignment.</p> <p>Expiration of the auto-deep-sleep timer will have no effect, for example: there will be no activity.</p> <p>2h = Use the UFS_ADSIT register.</p> <p>With this setting the (MK2,MK2) pattern will be send after the auto-deep-sleep counter has expired.</p> <p>The method how the (MK2,MK2) pattern is send is via 0-byte payload.</p> <p>3h = Use UFS_ADSIT register.</p> <p>With this setting the (MK2,MK2) pattern will be send after the auto-deep-sleep counter has expired.</p> <p>The method how the (MK2,MK2) pattern is send is via assertion of the UniPro burst signal.</p>

19.3.36 UFS_CDACFG Register (Offset = D0h) [reset = 0h]

UFS_CDACFG is shown in [Figure 19-60](#) and described in [Table 19-150](#).

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C-Port Direct Access Configuration Register

This register configures and manages the basic functionality of this feature.

To use this function in a 128-bit system, the IP module provides shadow register for the upper 64 bit data.

A write in the following order is required: UFS_CDATX1, CDATX1S, UFS_CDATX2, CDATX2S.

For receive data, a read in the following order is required: UFS_CDARX1, CDARX1S, UFS_CDARX2, CDARX2S.

Table 19-149. UFS_CDACFG Instances

Instance	Physical Address
UFS	04E8 40D0h

Figure 19-60. UFS_CDACFG Register

31	30	29	28	27	26	25	24
RESERVED			CDAEN	RESERVED			
R-0h			R/W-0h	R-0h			
23	22	21	20	19	18	17	16
RESERVED							CDAEOM
R-0h							R/W-0h
15	14	13	12	11	10	9	8
CDABE							
R/W-0h							
7	6	5	4	3	2	1	0
CDABES							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-150. UFS_CDACFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	CDAEN	R/W	0h	C-Port Direct Access Enable This bit enables the direct access feature.
27-17	RESERVED	R	0h	Reserved
16	CDAEOM	R/W	0h	C-Port Direct Access End of message indicator. Setting this bit forces the Host UniPro adapter to flush the message.

Table 19-150. UFS_CDACFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	CDABE	R/W	0h	<p>C-Port Direct Access Byte Enables</p> <p>Byte enables for the transmit data.</p> <p>Bit 15: CDATX2B0</p> <p>Bit 14: CDATX2B1</p> <p>Bit 13: CDATX2B2</p> <p>Bit 12: CDATX2B3</p> <p>Bit 11: CDATX1B4</p> <p>Bit 10: CDATX1B5</p> <p>Bit 9: CDATX1B6</p> <p>Bit 8: CDATX1B7</p> <p>If not all bytes carry valid payload, valid bytes shall use the lower CDATXx byte fields.</p> <p>Example (Supported):</p> <p>CDABE = FCh</p> <p>Example (Not supported):</p> <p>CDABE = CFh</p>
7-0	CDABES	R	0h	<p>C-Port Direct Access Shadow Byte Enables</p> <p>Reserved for 64-bit data bus setup.</p> <p>In a 128-bit system setup this field specifies the byte enables for the 64-bit shadow register.</p> <p>Byte enables for the transmit data.</p> <p>Bit 15: CDATX2B0 shadow</p> <p>Bit 14: CDATX2B1 shadow</p> <p>Bit 13: CDATX2B2 shadow</p> <p>Bit 12: CDATX2B3 shadow</p> <p>Bit 11: CDATX1B4 shadow</p> <p>Bit 10: CDATX1B5 shadow</p> <p>Bit 9: CDATX1B6 shadow</p> <p>Bit 8: CDATX1B7 shadow</p> <p>If not all bytes carry valid payload, valid bytes shall use the lower CDATXx byte fields.</p>

19.3.37 UFS_CDATX1 Register (Offset = D4h) [reset = 0h]

UFS_CDATX1 is shown in [Figure 19-61](#) and described in [Table 19-152](#).

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C-Port Direct Access Transmit 1 Register

This register takes the lower 32 bit of the 64-bit data word to be transferred.

In a 128-bit implementation, an additional shadow register is available under the same address.

Thus two writes are required to set the lower 64 bit of a received 128-bit word.

Note: Since the UIC layer follows big endian byte order, also the UFS_CDATX1 and UFS_CDATX2 registers follow big endian byte order.

Table 19-151. UFS_CDATX1 Instances

Instance	Physical Address
UFS	04E8 40D4h

Figure 19-61. UFS_CDATX1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDATX1B4								CDATX1B5								CDATX1B6								CDATX1B7							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-152. UFS_CDATX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CDATX1B4	R/W	0h	CDATX1B 4 - Write Data Byte 4
23-16	CDATX1B5	R/W	0h	CDATX1B 5 - Write Data Byte 5
15-8	CDATX1B6	R/W	0h	CDATX1B 6 - Write Data Byte 6
7-0	CDATX1B7	R/W	0h	CDATX1B 7 - Write Data Byte 7

19.3.38 UFS_CDATX2 Register (Offset = D8h) [reset = 0h]

UFS_CDATX2 is shown in [Figure 19-62](#) and described in [Table 19-154](#).

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C-Port Direct Access Transmit 2 Register

This register takes the lower 32 bit of the 64-bit data word to be transferred.

Writing to this address will push the data to the UniPro adapter.

In a 128bit implementation, an additional shadow register is available under the same address.

Thus two writes are required to set the lower 64 bit of a received 128-bit word.

Note: Since the UIC layer follows big endian byte order, also the UFS_CDATX1 and UFS_CDATX2 registers follow big endian byte order.

Table 19-153. UFS_CDATX2 Instances

Instance	Physical Address
UFS	04E8 40D8h

Figure 19-62. UFS_CDATX2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDATX2B0								CDATX2B1								CDATX2B2								CDATX2B3							
R/W-0h								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-154. UFS_CDATX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CDATX2B0	R/W	0h	CDATX2B 0 - Write Data Byte 0
23-16	CDATX2B1	R/W	0h	CDATX2B 1 - Write Data Byte 1
15-8	CDATX2B2	R/W	0h	CDATX2B 2 - Write Data Byte 2
7-0	CDATX2B3	R/W	0h	CDATX2B 3 - Write Data Byte 3

19.3.39 UFS_CDARX1 Register (Offset = DCh) [reset = 0h]

UFS_CDARX1 is shown in [Figure 19-63](#) and described in [Table 19-156](#).

Return to [Summary Table](#).

C-Port Direct Access Receive 1 Register

This register takes the lower 32 bit of the received 64-bit data word in case of a 64-bit system bus configuration. In a 128-bit implementation, an additional shadow register is available under the same address.

Thus two reads are required to get the lower 64 bit of a received 128-bit word.

Note: Since the UIC layer follows big endian byte order, also the UFS_CDARX1 and UFS_CDARX2 registers follow big endian byte order.

Table 19-155. UFS_CDARX1 Instances

Instance	Physical Address
UFS	04E8 40DCh

Figure 19-63. UFS_CDARX1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDARX1B4								CDARX1B5								CDARX1B6								CDARX1B7							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 19-156. UFS_CDARX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CDARX1B4	R	0h	CDARX1B 4 - Read Data Byte 4
23-16	CDARX1B5	R	0h	CDARX1B 5 - Read Data Byte 5
15-8	CDARX1B6	R	0h	CDARX1B 6 - Read Data Byte 6
7-0	CDARX1B7	R	0h	CDARX1B 7 - Read Data Byte 7

19.3.40 UFS_CDARX2 Register (Offset = E0h) [reset = 0h]

UFS_CDARX2 is shown in [Figure 19-64](#) and described in [Table 19-158](#).

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C-Port Direct Access Receive 2 Register

This register takes the upper 32 bit of the received 64-bit data word.

In a 128-bit implementation, an additional shadow register is available under the same address.

Thus two reads are required to get the upper 64 bit of a received 128-bit word.

Note: Since the UIC layer follows big endian byte order, also the UFS_CDARX1 and UFS_CDARX2 registers follow big endian byte order.

Table 19-157. UFS_CDARX2 Instances

Instance	Physical Address
UFS	04E8 40E0h

Figure 19-64. UFS_CDARX2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CDARX2B0								CDARX2B1								CDARX2B2								CDARX2B3							
R-0h								R-0h								R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 19-158. UFS_CDARX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CDARX2B0	R	0h	CDARX2B 0 - Read Data Byte 0
23-16	CDARX2B1	R	0h	CDARX2B 1 - Read Data Byte 1
15-8	CDARX2B2	R	0h	CDARX2B 2 - Read Data Byte 2
7-0	CDARX2B3	R	0h	CDARX2B 3 - Read Data Byte 3

19.3.41 UFS_CDASTA Register (Offset = E4h) [reset = 0h]

UFS_CDASTA is shown in [Figure 19-65](#) and described in [Table 19-160](#).

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C-Port Direct Access Status Register

This register contains status information related to the last transfer.

Table 19-159. UFS_CDASTA Instances

Instance	Physical Address
UFS	04E8 40E4h

Figure 19-65. UFS_CDASTA Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED	CDARES			CDABUSY	CDASTA	CDAEOM	CDASOM
R-0h	R-0h			R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
CDABE							
R-0h							
7	6	5	4	3	2	1	0
CDASBE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 19-160. UFS_CDASTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22-20	CDARES	R	0h	C-Port Direct Access Result Transmit result code. This field stores the result information from the last transmit operation. This field carries the TxResultCode from the UIC layer. It becomes valid one host clock cycle after the transfer has been completed. 0h = Access successful 1h = local CPort is unconnected 2h = reserved, unused for data transmission 3h = local CPort is not available 6h = peer device does not support selected TC 7h = Message of 0 size rejected (EOM false)
19	CDABUSY	R	0h	C-Port Direct Access Busy This bit indicates whether the C-Port is busy. The software shall poll this bit and make sure that the C-Port is available prior to any write access to the UFS_CDATX1 or UFS_CDATX2 registers. During data transmission, this bit is set to 1h until the transfer has been completed. 0h = C-Port available 1h = C-Port busy

Table 19-160. UFS_CDASTA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	CDASTA	R	0h	C-Port Direct Access Status The status bit indicates if there is new data in the buffer.
17	CDAEOM	R	0h	C-Port Direct Access EOM End of message indicator.
16	CDASOM	R	0h	C-Port Direct Access SOM Start of message indicator
15-8	CDABE	R	0h	C-Port Direct Access Byte Enable Byte enable settings for the received data.
7-0	CDASBE	R	0h	C-Port Direct Access Shadow Byte Enable Reserved in a 64 system bus configuration. In a 128 system bus configuration this field contains the byte enable settings for the received data in the shadow register.

19.3.42 UFS_XASB Register (Offset = E8h) [reset = 302h]

UFS_XASB is shown in [Figure 19-66](#) and described in [Table 19-162](#).

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Extended Address Space Base Register

Table 19-161. UFS_XASB Instances

Instance	Physical Address
UFS	04E8 40E8h

Figure 19-66. UFS_XASB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PEP				RESERVED				XDP			
R-0h				R/W-3h				R-0h				R/W-2h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-162. UFS_XASB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-8	PEP	R/W	3h	Pseudo Error Page This address defines the page address for the pseudo error configuration and control register in units of 1Kbytes. Minimum value is 1h to avoid collisions with MMIO page. Available Register: - All pseudo error register The page address is only valid (and will be used for address selection) when the UFS_XCNF[PERSEN] bit is set to 1h.
7-6	RESERVED	R	0h	Reserved
5-0	XDP	R/W	2h	Extended Debug Page This address defines the page address of the extended debugging information. Available registers: - EXTREG1 - - EXTREG8 - UFSDC - UPSTAT - URW - URS - CDC - RTDDC - TPTXF - TPRXF - IUE - MMTR The page address is only valid [and will be used for address selection] when the UFS_XCNF[0] XRSE is set to 1h. All accesses to the Extended Debug Page will not wake up the host controller from auto-hibernate or auto deep-sleep.

19.3.43 UFS_LBMCFG Register (Offset = F0h) [reset = 0h]

UFS_LBMCFG is shown in [Figure 19-67](#) and described in [Table 19-164](#).

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UPIU Loopback Configuration Register

Table 19-163. UFS_LBMCFG Instances

Instance	Physical Address
UFS	04E8 40F0h

Figure 19-67. UFS_LBMCFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				BEP			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
BEPS	TRTLDV			MRTTE	LBME	PDSIZE	
R/W-0h	R/W-1h			R/W-0h	R/W-0h	R/W-0h	
7	6	5	4	3	2	1	0
PDSIZE			USDLY	UDLY			
R/W-0h			R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-164. UFS_LBMCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	BEP	R/W	0h	<p>Byte Enable Pattern</p> <p>This field defines the number of valid byte enables.</p> <p>The byte enables are filled up from MSB to LSB.</p> <p>This is a test mode only.</p> <p>For normal operation this field should be kept at the default value.</p> <p>1 - Byte 7 enabled</p> <p>2 - Byte 7-6 enabled</p> <p>3 - Byte 7-5 enabled</p> <p>4 - Byte 7-4 enabled</p> <p>5 - Byte 7-3 enabled</p> <p>6 - Byte 7-2 enabled</p> <p>7 - Byte 7-1 enabled</p> <p>Others - Byte 7-0 enabled</p> <p>The field width is 4 bit in case the IP module is configured for 64-bit system data bus width and 5-bit for a 128-bit configuration.</p>

Table 19-164. UFS_LBMCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	BEPS	R/W	0h	<p>Byte Enable Pattern Selection</p> <p>This bit selects between a random byte enable pattern and a fixed byte enable pattern in 'read only' mode (LUN 0). In write only and 'loopback mode' this bit is ignored. The fixed byte enable pattern is taken from the UFS_LBMCFG[19-16] BEP bit field. This is a test mode only. For normal operation this field should be kept at the default value.</p> <p>0h = Fixed byte enable pattern taken from BEP field 1h = Random byte enable pattern</p>
14-11	TRTLDV	R/W	1h	<p>Throttle Divide</p> <p>Since the bandwidth on the system bus may be much higher than actually supported by the UniPro link, this value allows to throttle the bandwidth in order to better mimic a real UFS Device. However, by this, some inaccuracy to the performance measurement will be introduced since the time to fill or empty the system bus buffer changes, which in turn has influence on the rate in which system bus requests to the bus fabric can be issued.</p> <p>Value 0h = Reserved Value 1h-15h = Divide the frequency in which data is requested from the system bus RX buffer and/or stored into the system bus TX buffer.</p>
10	MRTTE	R/W	0h	<p>Multi RTT Enable</p> <p>This bit enables the multiple RTT feature. Here multiple RTT may be submitted by the loopback logic. This feature tests the performance of back to back DATAOUT UPIUs. It provides feedback about the capabilities of the host controller RTT management capabilities. If DATAOUT UPIUs exceed a certain size (size depends on the access latency to the system memory), a second outstanding RTT may help reducing the latency between two consecutive DATAOUT UPIUs. This feature requires that a second RTT is send to the host controller ahead of time. This enables the data management to fetch the data for the second RTT, while the data for the first RTT is still being sent over the UniPro link. It should be noted, that data transfer is in-order, and thus sending of data which belongs to the second RTT will not start before the first RTT is completely handled. The maximum number of outstanding RTT is two. Once the DATAOUT UPIUs for both RTTs have been transmitted, the next RTTs (2 or less) will be issued until all data that have been requested by the SCSI command were transferred.</p> <p>0h = Only one RTT 1h = Up to two outstanding RTTs</p>

Table 19-164. UFS_LBMCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	LBME	R/W	0h	<p>Loopback Enable bit</p> <p>Setting this bit decouples the UniPro layer from the host controller logic and switches the input data stream to take packets from the loopback logic.</p> <p>If UFS_LBMCFG[9] LBME = 0h , the UPIU loopback circuit is in reset.</p> <p>If UFS_LBMCFG[9] LBME = 1h , it is assured that no interaction with an attached UFS Device takes place.</p>
8-5	PDSIZE	R/W	0h	<p>Data Size</p> <p>This value is a 4-bit field and defines the amount of the data that will be requested by the RTT.</p> <p>This mimics the ability of the UFS Device to limit the size of a DATAOUT UPIU.</p> <p>In loopback mode, the UFS_LBMCFG[8-5] PDSIZE bit field defines the size of DATAOUT and DATAIN UPIUs.</p> <p>The field should be interpreted as the exponent of the function $\text{pow}[2, \text{UFS_LBMCFG}[8-5] \text{ PDSIZE} + 1]$.</p> <p>UFS_LBMCFG[8-5] PDSIZE bit values from 3h to Eh are supported. This allows sizes from 16 to 32768 bytes.</p>
4	USDLY	R/W	0h	<p>UPIU Source Delay</p> <p>This one-bit field defines whether there is a delay before every RTTs or DATAIN packet or just before the first one.</p>
3-0	UDLY	R/W	0h	<p>UPIU Delay</p> <p>This value is a 4-bit field and defines the delay (in clock cycles) from receiving the command till the response is send back to the host controller.</p> <p>The response could either be an RTT UPIU or a DATAIN UPIU. This allows the host controller to fetch the required PRD entries an immediately continue with processing the RTT or DATAIN UPIU.</p> <p>The field should be interpreted as the exponent of the function $\text{pow}(2, \text{UFS_LBMCFG}[3-0] \text{ UDLY} + 4)$.</p> <p>This allows delays from 16 to 524288 clock cycles which is approx. from 80 ns to 2.6 ms with a 200 MHz clock.</p> <p>Those large numbers mimic the real behaviour of current devices. A value of zero disables this feature, means no delay.</p> <p>Whether or not this delay is used for every return packet or just for the first one is controlled by the USDLY field.</p>

19.3.44 UFS_LBMSTA Register (Offset = F4h) [reset = 0h]

UFS_LBMSTA is shown in [Figure 19-68](#) and described in [Table 19-166](#).

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UPIU Loopback Status Register

Table 19-165. UFS_LBMSTA Instances

Instance	Physical Address
UFS	04E8 40F4h

Figure 19-68. UFS_LBMSTA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															ERR
R-0h															R-0h

LEGEND: R = Read Only; -n = value after reset

Table 19-166. UFS_LBMSTA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ERR	R	0h	<p>Error Indicator</p> <p>Indicates that there is general error.</p> <p>UFS_LBMSTA[0] ERR = 1h indicates that an error condition has been detected.</p> <p>Once an error condition has been detected, the UPIU loopback circuit needs to be disabled and enabled again via the UFS_LBMCFG[9] LBME bit.</p> <p>By this, the UFS_LBMSTA[0] ERR bit is cleared.</p> <p>Detectable error conditions:</p> <p>Command sent to unsupported LUN</p> <p>Unsupported command (Transaction Type)</p>

19.3.45 UFS_DBG Register (Offset = F8h) [reset = 0h]

UFS_DBG is shown in [Figure 19-69](#) and described in [Table 19-168](#).

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Debug Register

Table 19-167. UFS_DBG Instances

Instance	Physical Address
UFS	04E8 40F8h

Figure 19-69. UFS_DBG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														HCIER	
R-0h														R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HCSTATE															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 19-168. UFS_DBG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	HCIER	R	0h	Host Controller Internal Error Register This register displays host controller internal errors which are not covered by the JEDEC official errors reported back via the OCS value. 0h = No error occurred 1h = No valid TAG/LUN combination found. The UPIU with no valid TAG/LUN combination will be silently discarded. 2h = No valid TAG/LUN/IID combination found. The UPIU with no valid TAG/LUN/IID combination will be silently discarded.
15-0	HCSTATE	R	0h	Host Controller State These bits indicate the internal state of the host controller. The value is used for internal use only. 0h = No error occurred value: An error occurred. The meaning of the value is not disclosed.

19.3.46 UFS_HCLKDIV Register (Offset = FCh) [reset = 190h]

UFS_HCLKDIV is shown in [Figure 19-70](#) and described in [Table 19-170](#).

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Host Clock Divider Register

Note: This register configures the Tick1us clock required by UniPro.

This clock is actually a 500 KHz signal, thus there is one clock edge every 1 μ s (rising and falling).

This signal is used for UniPro internal counters. The signal is not used as a clock directly. Rather the UniPro logic is doing an edge detection and the signal sampled inside the core.

As an alternative the UFSHCI also provides an external input ad a select to provide the signal. From a system's point of view, this signal may be created by the M-PHY logic.

Table 19-169. UFS_HCLKDIV Instances

Instance	Physical Address
UFS	04E8 40FCh

Figure 19-70. UFS_HCLKDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																HCLKDIV															
R-0h																R/W-190h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-170. UFS_HCLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	HCLKDIV	R/W	190h	Host Clock Divide Host Clock Frequency [MHz] The default value of the UFS_HCLKDIV register assumes a host clock frequency of 400 MHz. The default value may be adjusted during implementation by changing the P_P_CLKDIV parameter.

19.3.47 UFS_CCAP Register (Offset = 100h) [reset = 05000101h]

UFS_CCAP is shown in [Figure 19-71](#) and described in [Table 19-172](#).

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Crypto Capabilities Register

Table 19-171. UFS_CCAP Instances

Instance	Physical Address
UFS	04E8 4100h

Figure 19-71. UFS_CCAP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFGPTR								RESERVED								CFGC								CC							
R-5h								R-0h								R-1h								R-1h							

LEGEND: R = Read Only; -n = value after reset

Table 19-172. UFS_CCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CFGPTR	R	5h	Configuration Array Pointer An offset pointer to the base of the Configuration Array [X-CRYPTOCFG registers], in 256B units. UFS_CCAP[31-24] CFGPTR bit filed value shall be larger than 4h, so it does not conflict with a maximum size X-UFS_CRYPTOCAP array. The address for entry x of the X-CRYPTOCFG array is calculated as follows: ADDR [X-CRYPTOCFG] = CFGPTR×100h + x×80h, with x in [0..UFS_CCAP[15-8] CFGC] and x derived from UTRD.CCI field.
23-16	RESERVED	R	0h	Reserved
15-8	CFGC	R	1h	Configuration Count The maximum number of configurations supported by the host controller. The actual number of configurations is equal to [CFGC + 1]. The minimum number of configurations supported is 1 [CFGC = 0h]. The maximum number of configurations supported is 256 [CFGC = FFh].
7-0	CC	R	1h	Crypto Capabilities The number of crypto capabilities that the host controller provides. The values allowed are between 1 and 255 (the limit on the number of crypto capabilities).

19.3.48 UFS_CRYPTOCAP Register (Offset = 104h) [reset = 00010802h]

UFS_CRYPTOCAP is shown in [Figure 19-72](#) and described in [Table 19-174](#).

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Crypto Capability X Register

Table 19-173. UFS_CRYPTOCAP Instances

Instance	Physical Address
UFS	04E8 4104h

Figure 19-72. UFS_CRYPTOCAP Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								KS								SDUSB								ALGID							
R-0h								R-1h								R-8h								R-2h							

LEGEND: R = Read Only; -n = value after reset

Table 19-174. UFS_CRYPTOCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	KS	R	1h	Key Size Specifies the Key Size in bits used by this algorithm: 0h = Reserved 1h = 128 bits 2h = 192 bits(not supported) 3h = 256 bits (not supported) 4h = 512 bits (not supported) 5h-FFh = Reserved
15-8	SDUSB	R	8h	Supported Data Unit Size Bitmask Specifies the data unit sizes supported by the capability, in bitmask encoding. When bit j in the field (j=0...7) is set, data unit size of 512×2 ^j bytes is supported. Supported values: 512B (j = 0) through 64 KB (j = 7). One bit or more in this field may be set. For example, if sizes 1 KB, 4 KB, and 16 KB are supported by the capability, then SDUSB = 00101010b (= 2Ah).
7-0	ALGID	R	2h	Algorithm Identification code of the crypto algorithm according to the following table value: 0h = AES-XTS (not supported) 1h = Bitlocker-AES-CBC (not supported) 2h = AES-ECB 3h = ESSIV AES-CBC (not supported) 4h-7Fh = Reserved 80h-FFh = Vendor specific This register can only be accessed when the encryption feature is implemented (UFS_CAP[28] CS = 1h).

19.3.49 UFS_CRYPTOCFG0 Register (Offset = 500h) [reset = 0h]

UFS_CRYPTOCFG0 is shown in [Figure 19-73](#) and described in [Table 19-176](#).

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Crypto Configuration 0 Register

Table 19-175. UFS_CRYPTOCFG0 Instances

Instance	Physical Address
UFS	04E8 4500h

Figure 19-73. UFS_CRYPTOCFG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPTOKEY0																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-176. UFS_CRYPTOCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRYPTOKEY0	W	0h	<p>Crypto Key 0</p> <p>Specifies the key to be used for this configuration.</p> <p>The specific key layout is defined according to the key size and algorithm specified in the Crypto Capability with index value specified in CAPIDX.</p> <p>When configuring CRYPTOKEY field software shall write the entire key sequentially, in one atomic set of operations.</p> <p>To regions of CRYPTOKEY which are unused, according to key size and algorithm selection, software shall write zeros.</p>

19.3.50 UFS_CRYPTOCFG1 Register (Offset = 504h) [reset = 0h]

UFS_CRYPTOCFG1 is shown in [Figure 19-74](#) and described in [Table 19-178](#).

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Crypto Configuration 1 Register

Table 19-177. UFS_CRYPTOCFG1 Instances

Instance	Physical Address
UFS	04E8 4504h

Figure 19-74. UFS_CRYPTOCFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPTOKEY1																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-178. UFS_CRYPTOCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRYPTOKEY1	W	0h	<p>Crypto Key 1</p> <p>Specifies the key to be used for this configuration.</p> <p>The specific key layout is defined according to the key size and algorithm specified in the Crypto Capability with index value specified in CAPIDX.</p> <p>When configuring CRYPTOKEY field software shall write the entire key sequentially, in one atomic set of operations.</p> <p>To regions of CRYPTOKEY which are unused, according to key size and algorithm selection, software shall write zeros.</p>

19.3.51 UFS_CRYPTOCFG2 Register (Offset = 508h) [reset = 0h]

UFS_CRYPTOCFG2 is shown in [Figure 19-75](#) and described in [Table 19-180](#).

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Crypto Configuration 2 Register

Table 19-179. UFS_CRYPTOCFG2 Instances

Instance	Physical Address
UFS	04E8 4508h

Figure 19-75. UFS_CRYPTOCFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPTOKEY2																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-180. UFS_CRYPTOCFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRYPTOKEY2	W	0h	<p>Crypto Key 2</p> <p>Specifies the key to be used for this configuration.</p> <p>The specific key layout is defined according to the key size and algorithm specified in the Crypto Capability with index value specified in CAPIDX.</p> <p>When configuring CRYPTOKEY field software shall write the entire key sequentially, in one atomic set of operations.</p> <p>To regions of CRYPTOKEY which are unused, according to key size and algorithm selection, software shall write zeros.</p>

19.3.52 UFS_CRYPTOCFG3 Register (Offset = 50Ch) [reset = 0h]

UFS_CRYPTOCFG3 is shown in [Figure 19-76](#) and described in [Table 19-182](#).

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Crypto Configuration 3 Register

Table 19-181. UFS_CRYPTOCFG3 Instances

Instance	Physical Address
UFS	04E8 450Ch

Figure 19-76. UFS_CRYPTOCFG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPTOKEY3																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-182. UFS_CRYPTOCFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRYPTOKEY3	W	0h	<p>Crypto Key 3</p> <p>Specifies the key to be used for this configuration.</p> <p>The specific key layout is defined according to the key size and algorithm specified in the Crypto Capability with index value specified in CAPIDX.</p> <p>When configuring CRYPTOKEY field software shall write the entire key sequentially, in one atomic set of operations.</p> <p>To regions of CRYPTOKEY which are unused, according to key size and algorithm selection, software shall write zeros.</p>

19.3.53 UFS_CRYPTOCFG16 Register (Offset = 540h) [reset = 0h]

UFS_CRYPTOCFG16 is shown in [Figure 19-77](#) and described in [Table 19-184](#).

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Crypto Configuration 16 Register

Table 19-183. UFS_CRYPTOCFG16 Instances

Instance	Physical Address
UFS	04E8 4540h

Figure 19-77. UFS_CRYPTOCFG16 Register

31	30	29	28	27	26	25	24
CFGE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CAPIDX							
R/W-0h							
7	6	5	4	3	2	1	0
DUSIZE							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-184. UFS_CRYPTOCFG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFGE	R/W	0h	Configuration Enable This field is used by software to enable/disable a Crypto Configuration usage by software 0h = Configuration Disabled. Transaction using this Crypto Configuration in the UTRD.CCI field shall be terminated with error by host controller (OCS=INVALID_CRYPTOCFG) 1h = Configuration Enabled. Transaction using this Configuration in the UTRD.CCI field can be executed.
30-16	RESERVED	R	0h	Reserved
15-8	CAPIDX	R/W	0h	Crypto Capability Index Specifies the index of the Crypto Capability to be used for this configuration. Values allowed are between 0 and UFS_CCAP[7-0] CC - 1. There is no hardware range check implemented.

Table 19-184. UFS_CRYPTOCFG16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DUSIZE	R/W	0h	<p>Data Unit Size</p> <p>Size of data unit used with this configuration, one-hot encoded, analogous to bitmask used in the UFS_CRYPTOCAP[15-8] SDUSB bit field.</p> <p>When bit j in this field (j=0...7) is set, a data unit size of 512×2^j bytes is selected.</p> <p>Bit j shall only be set if the same bit is also set in the UFS_CRYPTOCAP[15-8] SDUSB bit field of the capability referenced in CAPIDX field.</p> <p>There is no hardware check for consistency between the UFS_CRYPTOCFG16[7-0] DUSIZE and UFS_CRYPTOCAP[15-8] SDUSB bit field.</p>

19.3.54 UFS_CRYPTOCFG17 Register (Offset = 544h) [reset = 0h]

UFS_CRYPTOCFG17 is shown in [Figure 19-78](#) and described in [Table 19-186](#).

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Crypto Configuration 17 Register

Table 19-185. UFS_CRYPTOCFG17 Instances

Instance	Physical Address
UFS	04E8 4544h

Figure 19-78. UFS_CRYPTOCFG17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSB																RESERVED															
R/W-0h																R-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-186. UFS_CRYPTOCFG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VSB	R/W	0h	Vendor-Specific Bits This field is used by software to enable host-features associated with the Crypto Configuration.
15-0	RESERVED	R	0h	Reserved

19.3.55 UFS_CRYPTOCFG32 Register (Offset = 580h) [reset = 0h]

UFS_CRYPTOCFG32 is shown in [Figure 19-79](#) and described in [Table 19-188](#).

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Crypto Configuration 0 for Second Crypto Configuration Register

Table 19-187. UFS_CRYPTOCFG32 Instances

Instance	Physical Address
UFS	04E8 4580h

Figure 19-79. UFS_CRYPTOCFG32 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPTOKEY32																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-188. UFS_CRYPTOCFG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRYPTOKEY32	W	0h	<p>Crypto Key 0 for second crypto configuration</p> <p>Specifies the key to be used for this configuration.</p> <p>The specific key layout is defined according to the key size and algorithm specified in the Crypto Capability with index value specified in CAPIDX.</p> <p>When configuring CRYPTOKEY field software shall write the entire key sequentially, in one atomic set of operations.</p> <p>To regions of CRYPTOKEY which are unused, according to key size and algorithm selection, software shall write zeros.</p>

19.3.56 UFS_CRYPTOCFG33 Register (Offset = 584h) [reset = 0h]

UFS_CRYPTOCFG33 is shown in [Figure 19-80](#) and described in [Table 19-190](#).

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Crypto Configuration 1 for Second Crypto Configuration Register

Table 19-189. UFS_CRYPTOCFG33 Instances

Instance	Physical Address
UFS	04E8 4584h

Figure 19-80. UFS_CRYPTOCFG33 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPTOKEY33																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-190. UFS_CRYPTOCFG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRYPTOKEY33	W	0h	<p>Crypto Key 1 for second crypto configuration</p> <p>Specifies the key to be used for this configuration.</p> <p>The specific key layout is defined according to the key size and algorithm specified in the Crypto Capability with index value specified in CAPIDX.</p> <p>When configuring CRYPTOKEY field software shall write the entire key sequentially, in one atomic set of operations.</p> <p>To regions of CRYPTOKEY which are unused, according to key size and algorithm selection, software shall write zeros.</p>

19.3.57 UFS_CRYPTOCFG34 Register (Offset = 588h) [reset = 0h]

UFS_CRYPTOCFG34 is shown in [Figure 19-81](#) and described in [Table 19-192](#).

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Crypto Configuration 2 for Second Crypto Configuration Register

Table 19-191. UFS_CRYPTOCFG34 Instances

Instance	Physical Address
UFS	04E8 4588h

Figure 19-81. UFS_CRYPTOCFG34 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPTOKEY34																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-192. UFS_CRYPTOCFG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRYPTOKEY34	W	0h	<p>Crypto Key 2 for second crypto configuration</p> <p>Specifies the key to be used for this configuration.</p> <p>The specific key layout is defined according to the key size and algorithm specified in the Crypto Capability with index value specified in CAPIDX.</p> <p>When configuring CRYPTOKEY field software shall write the entire key sequentially, in one atomic set of operations.</p> <p>To regions of CRYPTOKEY which are unused, according to key size and algorithm selection, software shall write zeros.</p>

19.3.58 UFS_CRYPTOCFG35 Register (Offset = 58Ch) [reset = 0h]

UFS_CRYPTOCFG35 is shown in [Figure 19-82](#) and described in [Table 19-194](#).

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Crypto Configuration 3 for Second Crypto Configuration Register

Table 19-193. UFS_CRYPTOCFG35 Instances

Instance	Physical Address
UFS	04E8 458Ch

Figure 19-82. UFS_CRYPTOCFG35 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPTOKEY35																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 19-194. UFS_CRYPTOCFG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CRYPTOKEY35	W	0h	<p>Crypto Key 3 for second crypto configuration</p> <p>Specifies the key to be used for this configuration.</p> <p>The specific key layout is defined according to the key size and algorithm specified in the Crypto Capability with index value specified in CAPIDX.</p> <p>When configuring CRYPTOKEY field software shall write the entire key sequentially, in one atomic set of operations.</p> <p>To regions of CRYPTOKEY which are unused, according to key size and algorithm selection, software shall write zeros.</p>

19.3.59 UFS_CRYPTOCFG48 Register (Offset = 5C0h) [reset = 0h]

UFS_CRYPTOCFG48 is shown in [Figure 19-83](#) and described in [Table 19-196](#).

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Crypto Configuration 16 for Second Crypto Configuration Register

Table 19-195. UFS_CRYPTOCFG48 Instances

Instance	Physical Address
UFS	04E8 45C0h

Figure 19-83. UFS_CRYPTOCFG48 Register

31	30	29	28	27	26	25	24
CFGE1	RESERVED						
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CAPIDX1							
R/W-0h							
7	6	5	4	3	2	1	0
DUSIZE1							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-196. UFS_CRYPTOCFG48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CFGE1	R/W	0h	Configuration Enable for second crypto configuration This field is used by software to enable/disable a Crypto Configuration usage by software. 0h = Configuration Disabled. Transaction using this Crypto Configuration in the UTRD.CCI field shall be terminated with error by host controller (OCS = INVALID_CRYPTOCFG) 1b: Configuration Enabled. Transaction using this Configuration in the UTRD.CCI field can be executed.
30-16	RESERVED	R	0h	Reserved
15-8	CAPIDX1	R/W	0h	Crypto Capability Index for second crypto configuration Specifies the index of the Crypto Capability to be used for this configuration. Values allowed are between 0 and UFS_CCAP[7-0] CC - 1. There is no hardware range check implemented.

Table 19-196. UFS_CRYPTOCFG48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	DUSIZE1	R/W	0h	<p>Data Unit Size for second crypto configuration</p> <p>Size of data unit used with this configuration, one-hot encoded, analogous to bitmask used in the UFS_CRYPTOCAP[15-8] SDUSB bit field.</p> <p>When bit j in this field ($j=0\dots7$) is set, a data unit size of 512×2^j bytes is selected.</p> <p>Bit j shall only be set if the same bit is also set in the SDUSB field of the capability referenced in CAPIDX field.</p> <p>There is no hardware check for consistency between the UFS_CRYPTOCFG48[7-0] DUSIZE1 and UFS_CRYPTOCAP[15-8] SDUSB bit fields.</p>

19.3.60 UFS_CRYPTOCFG49 Register (Offset = 5C4h) [reset = 0h]

UFS_CRYPTOCFG49 is shown in [Figure 19-84](#) and described in [Table 19-198](#).

Return to [Summary Table](#).

Crypto Configuration 17 for Second Crypto Configuration Register

Table 19-197. UFS_CRYPTOCFG49 Instances

Instance	Physical Address
UFS	04E8 45C4h

Figure 19-84. UFS_CRYPTOCFG49 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSB1																RESERVED															
R/W-0h																R-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-198. UFS_CRYPTOCFG49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VSB1	R/W	0h	Vendor-Specific Bits for Second Crypto Configuration This field is used by software to enable host-features associated with the Crypto Configuration.
15-0	RESERVED	R	0h	Reserved

19.3.61 UFS_ASF_INT_STATUS Register (Offset = 1000h) [reset = 0h]

UFS_ASF_INT_STATUS is shown in [Figure 19-85](#) and described in [Table 19-200](#).

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ASF Interrupt Status Register

This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the `asf_int_fatal` or `asf_int_nonfatal` signal will be asserted. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 19-199. UFS_ASF_INT_STATUS Instances

Instance	Physical Address
UFS	04E8 5000h

Figure 19-85. UFS_ASF_INT_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR	ASF_PROTOCOL_ERR	ASF_TRANSACTION_TIMEOUT_ERR	RESERVED	RESERVED	ASF_SRAM_UNCORRECTABLE_ERR	ASF_SRAM_CORRECTABLE_ERR
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-200. UFS_ASF_INT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	ASF_INTEGRITY_ERR	R/W1C	0h	Integrity error interrupt
5	ASF_PROTOCOL_ERR	R/W1C	0h	Protocol error interrupt
4	ASF_TRANSACTION_TIMEOUT_ERR	R/W1C	0h	Transaction timeouts error interrupt
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	ASF_SRAM_UNCORRECTABLE_ERR	R/W1C	0h	SRAM uncorrectable error interrupt
0	ASF_SRAM_CORRECTABLE_ERR	R/W1C	0h	SRAM correctable error interrupt

19.3.62 UFS_ASF_INT_RAW_STATUS Register (Offset = 1004h) [reset = 0h]

UFS_ASF_INT_RAW_STATUS is shown in [Figure 19-86](#) and described in [Table 19-202](#).

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ASF Interrupt Raw Status Register

A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 19-201. UFS_ASF_INT_RAW_STATUS Instances

Instance	Physical Address
UFS	04E8 5004h

Figure 19-86. UFS_ASF_INT_RAW_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR	ASF_PROTOCOL_ERR	ASF_TRANSACTION_TIMEOUT_ERR	RESERVED	RESERVED	ASF_SRAM_UNCORRECTABLE_ERR	ASF_SRAM_CORRECTABLE_ERR
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-202. UFS_ASF_INT_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	ASF_INTEGRITY_ERR	R/W1C	0h	Integrity error interrupt
5	ASF_PROTOCOL_ERR	R/W1C	0h	Protocol error interrupt
4	ASF_TRANSACTION_TIMEOUT_ERR	R/W1C	0h	Transaction timeouts error interrupt
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	ASF_SRAM_UNCORRECTABLE_ERR	R/W1C	0h	SRAM uncorrectable error interrupt
0	ASF_SRAM_CORRECTABLE_ERR	R/W1C	0h	SRAM correctable error interrupt

19.3.63 UFS_ASF_INT_MASK Register (Offset = 1008h) [reset = 73h]

UFS_ASF_INT_MASK is shown in [Figure 19-87](#) and described in [Table 19-204](#).

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ASF Interrupt Mask Register

The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt status register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt.

Table 19-203. UFS_ASF_INT_MASK Instances

Instance	Physical Address
UFS	04E8 5008h

Figure 19-87. UFS_ASF_INT_MASK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR_MASK	ASF_PROTOCOL_ERR_MASK	ASF_TRANSACTION_ERR_MASK	RESERVED	RESERVED	ASF_SRAM_UNCORRECTABLE_ERR_MASK	ASF_SRAM_CORRECTABLE_ERR_MASK
R-0h	R/W-1h	R/W-1h	R/W-1h	R-0h	R-0h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-204. UFS_ASF_INT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	ASF_INTEGRITY_ERR_MASK	R/W	1h	Mask bit for integrity error interrupt
5	ASF_PROTOCOL_ERR_MASK	R/W	1h	Mask bit for protocol error interrupt.
4	ASF_TRANSACTION_ERR_MASK	R/W	1h	Mask bit for transaction timeouts error interrupt.
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	ASF_SRAM_UNCORRECTABLE_ERR_MASK	R/W	1h	Mask bit for SRAM uncorrectable error interrupt.
0	ASF_SRAM_CORRECTABLE_ERR_MASK	R/W	1h	Mask bit for SRAM correctable error interrupt.

19.3.64 UFS_ASF_INT_TEST Register (Offset = 100Ch) [reset = 73h]

UFS_ASF_INT_TEST is shown in [Figure 19-88](#) and described in [Table 19-206](#).

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ASF Interrupt Test Register

The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) status registers according to mask and will generate interrupt accordingly.

Table 19-205. UFS_ASF_INT_TEST Instances

Instance	Physical Address
UFS	04E8 500Ch

Figure 19-88. UFS_ASF_INT_TEST Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR_TEST	ASF_PROTOCOL_ERR_TEST	ASF_TRANSACTION_ERR_TEST	RESERVED	RESERVED	ASF_SRAM_UNCORR_ERR_TEST	ASF_SRAM_CORR_ERR_TEST
R-0h	W-1h	W-1h	W-1h	R-0h	R-0h	W-1h	W-1h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 19-206. UFS_ASF_INT_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	ASF_INTEGRITY_ERR_TEST	W	1h	Test bit for integrity error interrupt
5	ASF_PROTOCOL_ERR_TEST	W	1h	Test bit for protocol error interrupt.
4	ASF_TRANSACTION_ERR_TEST	W	1h	Test bit for transaction timeouts error interrupt.
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	ASF_SRAM_UNCORR_ERR_TEST	W	1h	Test bit for SRAM uncorrectable error interrupt.
0	ASF_SRAM_CORR_ERR_TEST	W	1h	Test bit for SRAM correctable error interrupt.

19.3.65 UFS_ASF_FATAL_NONFATAL_SELECT Register (Offset = 1010h) [reset = 73h]

UFS_ASF_FATAL_NONFATAL_SELECT is shown in [Figure 19-89](#) and described in [Table 19-208](#).

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Fatal or Non-Fatal Interrupt Register

The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered.

Table 19-207.
UFS_ASF_FATAL_NONFATAL_SELECT Instances

Instance	Physical Address
UFS	04E8 5010h

Figure 19-89. UFS_ASF_FATAL_NONFATAL_SELECT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	ASF_INTEGRITY_ERR	ASF_PROTOCOL_ERR	ASF_TRANSACTION_TIMEOUT_ERR	RESERVED	RESERVED	ASF_SRAM_UNCORRECTABLE_ERR	ASF_SRAM_CORRECTABLE_ERR
R-0h	R/W-1h	R/W-1h	R/W-1h	R-0h	R-0h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-208. UFS_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	ASF_INTEGRITY_ERR	R/W	1h	Enable integrity error interrupt as fatal
5	ASF_PROTOCOL_ERR	R/W	1h	Enable protocol error interrupt as fatal.
4	ASF_TRANSACTION_TIMEOUT_ERR	R/W	1h	Enable transaction timeouts error interrupt as fatal.
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	ASF_SRAM_UNCORRECTABLE_ERR	R/W	1h	Enable SRAM uncorrectable error interrupt as fatal.
0	ASF_SRAM_CORRECTABLE_ERR	R/W	1h	Enable SRAM correctable error interrupt as fatal.

19.3.66 UFS_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 1020h) [reset = 0h]

UFS_ASF_SRAM_CORR_FAULT_STATUS is shown in [Figure 19-90](#) and described in [Table 19-210](#).

Return to [Summary Table](#).

Status Register for SRAM Correctable Fault Register

This captures all SRAM ECC Correctable Errors. This records the Instance and the address of the first error seen in the SRAM Correctable error.

Table 19-209.
UFS_ASF_SRAM_CORR_FAULT_STATUS Instances

Instance	Physical Address
UFS	04E8 5020h

Figure 19-90. UFS_ASF_SRAM_CORR_FAULT_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ASF_SRAM_CORR_FAULT_INST								ASF_SRAM_CORR_FAULT_ADDR							
R-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASF_SRAM_CORR_FAULT_ADDR															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 19-210. UFS_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ASF_SRAM_CORR_FAULT_INST	R	0h	<p>This encoding indicates which SRAM Instance has a Correctable Fault.</p> <p>The encoding of the SRAM is as follow:</p> <p>Decimal Encoding - Instance Type - Description - Module Name</p> <p>0 - RDF - Read Data FIFO - RDP</p> <p>1 - RDC - Read Data Path Control Unit - RDC</p> <p>2 - WDF - Write Data FIFO - WDP</p> <p>3 - WDCF - Write Data Path Control FIFO - WDC</p> <p>4 - WDC - Write Data Path Control Unit - WDC</p> <p>5 - RTT - WDC RTT command stack - WDC</p> <p>6 - WDCM - WDC task management command stack - WDC</p> <p>7 - CIP - Command Interface Port - CIP</p> <p>8 - CMU1 - Command Memmory Unit - CMU</p> <p>9 - CMU2 - Command Memmory Unit - CMU</p> <p>10 - CMU3 - Command Memmory Unit - CMU</p> <p>11 - CMU4 - Command Memmory Unit - CMU</p> <p>12 - CMU5 - Command Memmory Unit - CMU</p> <p>13 - CMU6 - Command Memmory Unit - CMU</p> <p>14 - CMU7 - Command Memmory Unit - CMU</p> <p>15 - TMU - Task Management Unit - TMU</p> <p>16 - UniPro L2RX - UniPro - L2TX</p> <p>17* - UniPro L2TX - UniPro - L2RX</p> <p>18* - UniPro L2TX - UniPro - L2RX</p> <p>19 - CCI - Crypto Configuration Index - AES</p> <p>20 - ID - Stores the identifiers for the selected Doorbell Register slot numbers - AES</p> <p>*NOTE: ID17 used for uncorrectable errors ID18 used for correctable errors.</p>

Table 19-210. UFS_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-0	ASF_SRAM_CORR_FAULT_ADDR	R	0h	This indicates the address where the Correctable fault was observed.

19.3.67 UFS_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 1024h) [reset = 0h]

UFS_ASF_SRAM_UNCORR_FAULT_STATUS is shown in [Figure 19-91](#) and described in [Table 19-212](#).

Return to [Summary Table](#).

Status Register (For SRAM Uncorrectable Fault)

This captures all SRAM ECC UnCorrectable Errors. Uncorrectable Errors Include both ECC multi bit errors and parity errors found on data and address for SRAM. This records the Instance and the address of the first error seen in the SRAM UnCorrectable error.

Table 19-211.
UFS_ASF_SRAM_UNCORR_FAULT_STATUS
Instances

Instance	Physical Address
UFS	04E8 5024h

Figure 19-91. UFS_ASF_SRAM_UNCORR_FAULT_STATUS Register

31	30	29	28	27	26	25	24
ASF_SRAM_UNCORR_FAULT_INST							
R-0h							
23	22	21	20	19	18	17	16
ASF_SRAM_UNCORR_FAULT_ADDR							
R-0h							
15	14	13	12	11	10	9	8
ASF_SRAM_UNCORR_FAULT_ADDR							
R-0h							
7	6	5	4	3	2	1	0
ASF_SRAM_UNCORR_FAULT_ADDR							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 19-212. UFS_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ASF_SRAM_UNCORR_FAULT_INST	R	0h	<p>This encoding indicates which SRAM Instance has a UnCorrectable Fault.</p> <p>The encoding of the SRAM is as follow:</p> <p>Decimal Encoding - Instance Type - Description - Module Name</p> <p>0 - RDF - Read Data FIFO - RDP</p> <p>1 - RDC - Read Data Path Control Unit - RDC</p> <p>2 - WDF - Write Data FIFO - WDP</p> <p>3 - WDCF - Write Data Path Control FIFO - WDC</p> <p>4 - WDC - Write Data Path Control Unit - WDC</p> <p>5 - RTT - WDC RTT command stack - WDC</p> <p>6 - WDCM - WDC task management command stack - WDC</p> <p>7 - CIP - Command Interface Port - CIP</p> <p>8 - CMU1 - Command Memmory Unit - CMU</p> <p>9 - CMU2 - Command Memmory Unit - CMU</p> <p>10 - CMU3 - Command Memmory Unit - CMU</p> <p>11 - CMU4 - Command Memmory Unit - CMU</p> <p>12 - CMU5 - Command Memmory Unit - CMU</p> <p>13 - CMU6 - Command Memmory Unit - CMU</p> <p>14 - CMU7 - Command Memmory Unit - CMU</p> <p>15 - TMU - Task Management Unit - TMU</p> <p>16 - UniPro L2RX - UniPro - L2TX</p> <p>17* - UniPro L2TX - UniPro - L2RX</p> <p>18* - UniPro L2TX - UniPro - L2RX</p> <p>19 - CCI - Crypto Configuration Index - AES</p> <p>20 - ID - Stores the identifiers for the selected Doorbell Register slot numbers - AES</p> <p>*NOTE: ID17 used for uncorrectable errors ID18 used for correctable errors.</p>
23-0	ASF_SRAM_UNCORR_FAULT_ADDR	R	0h	<p>This indicates the address where the UnCorrectable fault was observed.</p>

19.3.68 UFS_ASF_SRAM_FAULT_STATS Register (Offset = 1028h) [reset = 0h]

UFS_ASF_SRAM_FAULT_STATS is shown in [Figure 19-92](#) and described in [Table 19-214](#).

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Statistics Register (For SRAM Faults)

Note that this register clears when software writes to any field.

Table 19-213. UFS_ASF_SRAM_FAULT_STATS Instances

Instance	Physical Address
UFS	04E8 5028h

Figure 19-92. UFS_ASF_SRAM_FAULT_STATS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ASF_SRAM_FAULT_UNCORR_STATS															
R/W1C-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASF_SRAM_FAULT_CORR_STATS															
R/W1C-0h															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-214. UFS_ASF_SRAM_FAULT_STATS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ASF_SRAM_FAULT_UNCORR_STATS	R/W1C	0h	Count of number of uncorrectable errors if implemented. Count value will saturate at 0xFFFF.
15-0	ASF_SRAM_FAULT_CORR_STATS	R/W1C	0h	Count of number of correctable errors if implemented. Count value will saturate at 0xFFFF.

19.3.69 UFS_ASF_TRANS_TO_CTRL Register (Offset = 1030h) [reset = 0h]

UFS_ASF_TRANS_TO_CTRL is shown in [Figure 19-93](#) and described in [Table 19-216](#).

Return to [Summary Table](#).

Control Register (To Configure The ASF Transaction Timeout Monitors)

Table 19-215. UFS_ASF_TRANS_TO_CTRL Instances

Instance	Physical Address
UFS	04E8 5030h

Figure 19-93. UFS_ASF_TRANS_TO_CTRL Register

31	30	29	28	27	26	25	24
ASF_TRANS_TO_EN	RESERVED						
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ASF_TRANS_TO_CTRL							
R/W-0h							
7	6	5	4	3	2	1	0
ASF_TRANS_TO_CTRL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-216. UFS_ASF_TRANS_TO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ASF_TRANS_TO_EN	R/W	0h	Enable transaction timeout monitoring.
30-16	RESERVED	R	0h	Reserved
15-0	ASF_TRANS_TO_CTRL	R/W	0h	Reserved

19.3.70 UFS_ASF_TRANS_TO_FAULT_MASK Register (Offset = 1034h) [reset = 7h]

UFS_ASF_TRANS_TO_FAULT_MASK is shown in [Figure 19-94](#) and described in [Table 19-218](#).

Return to [Summary Table](#).

Control Register (To Mask Out ASF Transaction Timeout Faults From Triggering Interrupts)

On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterizable and the bit definitions are implementation specific.

Table 19-217. UFS_ASF_TRANS_TO_FAULT_MASK Instances

Instance	Physical Address
UFS	04E8 5034h

Figure 19-94. UFS_ASF_TRANS_TO_FAULT_MASK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					TCX_REPL_TM R_MASK	AFCX_REQ_T MR_MASK	FCX_PROT_T MR_MASK
R-0h					R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-218. UFS_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	TCX_REPL_TMR_MASK	R/W	1h	TCx_REPLAY_TIMER_EXPIRED mask.
1	AFCX_REQ_TMR_MASK	R/W	1h	AFCx_REQUEST_TIMER_EXPIRED mask.
0	FCX_PROT_TMR_MASK	R/W	1h	FCx_PROTECTION_TIMER_EXPIRED mask.

19.3.71 UFS_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 1038h) [reset = 0h]

UFS_ASF_TRANS_TO_FAULT_STATUS is shown in [Figure 19-95](#) and described in [Table 19-220](#).

Return to [Summary Table](#).

Status Register (For Transaction Timeouts Fault)

Status register for transaction timeouts fault. If a fault occurs the relevant status bit will be set to 1h. Each bit can be cleared by software writing 1h to each bit.

Table 19-219.
UFS_ASF_TRANS_TO_FAULT_STATUS Instances

Instance	Physical Address
UFS	04E8 5038h

Figure 19-95. UFS_ASF_TRANS_TO_FAULT_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					TCX_REPL_TM R_ERR	AFCX_REQ_T MR_ERR	FCX_PROT_T MR_ERR
R-0h					R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-220. UFS_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	TCX_REPL_TMR_ERR	R/W1C	0h	TCx_REPLAY_TIMER_EXPIRED timeout detected. The replay timer (TCx_REPLAY_TIMER, where x = 0 or 1) guards against losing AFC or NAC Frame detection.
1	AFCX_REQ_TMR_ERR	R/W1C	0h	AFCx_REQUEST_TIMER_EXPIRED timeout detected. The Frame acknowledge timer (AFCx_REQUEST_TIMER) shall guarantee that the remote transmitter schedules an AFC Frame before the transmitter TCx_REPLAY_TIMER expires.
0	FCX_PROT_TMR_ERR	R/W1C	0h	FCx_PROTECTION_TIMER_EXPIRED timeout detected. The FCx_PROTECTION_TIMER id used for protecting against loss of credits due to the loss of the AFCx Frame.

19.3.72 UFS_ASF_PROTOCOL_FAULT_MASK Register (Offset = 1040h) [reset = FFFh]

UFS_ASF_PROTOCOL_FAULT_MASK is shown in [Figure 19-96](#) and described in [Table 19-222](#).

Return to [Summary Table](#).

Control Register (To Mask Out ASF Protocol Faults From Triggering Interrupts)

On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterizable and the bit definitions are implementation specific.

Table 19-221. UFS_ASF_PROTOCOL_FAULT_MASK Instances

Instance	Physical Address
UFS	04E8 5040h

Figure 19-96. UFS_ASF_PROTOCOL_FAULT_MASK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				PA_IND_RCV_MASK	PA_INT_MASK	BAD_CTRL_S_MASK	FRM_S_MASK
R-0h				R/W-1h	R/W-1h	R/W-1h	R/W-1h
7	6	5	4	3	2	1	0
EOF_S_MASK	NAC_F_S_MASK	AFC_F_S_MASK	WSQ_NO_MASK	MFL_EX_MASK	RXBUG_OF_MASK	CRC_ERR_MASK	NAC_RCV_MASK
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-222. UFS_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	PA_IND_RCV_MASK	R/W	1h	When set to 1h disables the UniPro PA_ERROR_IND_RECEIVED.
10	PA_INT_MASK	R/W	1h	When set to 1h disables the UniPro PA_INIT_ERROR.
9	BAD_CTRL_S_MASK	R/W	1h	When set to 1h disables the UniPro BAD_CTRL_SYMBOL_TYPE.
8	FRM_S_MASK	R/W	1h	When set to 1h disables the UniPro FRAME_SYNTAX_ERROR.
7	EOF_S_MASK	R/W	1h	When set to 1h disables the UniPro EOF_SYNTAX_ERROR.
6	NAC_F_S_MASK	R/W	1h	When set to 1h disables the UniPro NAC_FRAME_SYNTAX_ERROR.
5	AFC_F_S_MASK	R/W	1h	When set to 1h disables the UniPro AFC_FRAME_SYNTAX_ERROR.
4	WSQ_NO_MASK	R/W	1h	When set to 1h disables the UniPro WRONG_SEQUENCE_NUMBER.
3	MFL_EX_MASK	R/W	1h	When set to 1h disables the UniPro MAX_FRAME_LENGTH_EXCEEDED.
2	RXBUG_OF_MASK	R/W	1h	When set to 1h disables the UniPro RX_BUFFER_OVERFLOW.
1	CRC_ERR_MASK	R/W	1h	When set to 1h disables the UniPro CRC_ERROR.

Table 19-222. UFS_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAC_RCV_MASK	R/W	1h	When set to 1h disables the UniPro NAC_RECEIVED.

19.3.73 UFS_ASF_PROTOCOL_FAULT_STATUS Register (Offset = 1044h) [reset = 0h]

UFS_ASF_PROTOCOL_FAULT_STATUS is shown in [Figure 19-97](#) and described in [Table 19-224](#).

Return to [Summary Table](#).

Status Register (For Protocol Faults)

If a fault occurs the relevant status bit will be set to 1h. Each bit can be cleared by software writing 1h to each bit.

Table 19-223.
UFS_ASF_PROTOCOL_FAULT_STATUS Instances

Instance	Physical Address
UFS	04E8 5044h

Figure 19-97. UFS_ASF_PROTOCOL_FAULT_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				PA_IND_RCV_ERR	PA_INT_ERR	BAD_CTRL_S_ERR	FRM_S_ERR
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
EOF_S_ERR	NAC_F_S_ERR	AFC_F_S_ERR	WSQ_NO_ERR	MFL_EX_ERR	RXBUG_OF_ERR	CRC_ERR_ERR	NAC_RCV_ERR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-224. UFS_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11	PA_IND_RCV_ERR	R/W1C	0h	UniPro PA_ERROR_IND_RECEIVED reported.
10	PA_INT_ERR	R/W1C	0h	UniPro PA_INIT_ERROR reported.
9	BAD_CTRL_S_ERR	R/W1C	0h	UniPro BAD_CTRL_SYMBOL_TYPE reported.
8	FRM_S_ERR	R/W1C	0h	UniPro FRAME_SYNTAX_ERROR reported.
7	EOF_S_ERR	R/W1C	0h	UniPro EOF_SYNTAX_ERROR reported.
6	NAC_F_S_ERR	R/W1C	0h	UniPro NAC_FRAME_SYNTAX_ERROR reported.
5	AFC_F_S_ERR	R/W1C	0h	UniPro AFC_FRAME_SYNTAX_ERROR reported.
4	WSQ_NO_ERR	R/W1C	0h	UniPro WRONG_SEQUENCE_NUMBER reported.
3	MFL_EX_ERR	R/W1C	0h	UniPro MAX_FRAME_LENGTH_EXCEEDED reported.
2	RXBUG_OF_ERR	R/W1C	0h	UniPro RX_BUFFER_OVERFLOW reported.
1	CRC_ERR_ERR	R/W1C	0h	UniPro CRC_ERROR reported.
0	NAC_RCV_ERR	R/W1C	0h	UniPro NAC_RECEIVED reported.

19.3.74 UFS_ASF_INTEGRITY_ERR_INJ Register (Offset = 1058h) [reset = 0h]

UFS_ASF_INTEGRITY_ERR_INJ is shown in [Figure 19-98](#) and described in [Table 19-226](#).

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ASF Integrity Test Register

Write one to the enable register inject error to individual n-bit (trigger asf integrity fail to the IP Fault Logging and Reporting module). Please note that only injection error with number to N will generate a fail (i.e. the higher values do not generate fail) where N is the higher value specified in the asf_integrity_err_inj_num field.

**Table 19-225. UFS_ASF_INTEGRITY_ERR_INJ
Instances**

Instance	Physical Address
UFS	04E8 5058h

Figure 19-98. UFS_ASF_INTEGRITY_ERR_INJ Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ASF_INTEGRITY_ERR_INJ_EN	ASF_INTEGRITY_ERR_INJ_NUM						
R/W-0h	R/W-0h						
7	6	5	4	3	2	1	0
ASF_INTEGRITY_ERR_INJ_NUM							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 19-226. UFS_ASF_INTEGRITY_ERR_INJ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	ASF_INTEGRITY_ERR_INJ_EN	R/W	0h	Enable integrity error injection.
14-0	ASF_INTEGRITY_ERR_INJ_NUM	R/W	0h	<p>Bit number at which error is injected.</p> <p>The n is related to:</p> <p>a. 0-CRU_OUTS_DATA_WIDTH*: inject error to n bit in comparator in the duplication of the cryptographic core from zero to CRU_OUTS_DATA_WIDTH.</p> <p>Writing bigger value than CRU_OUTS_DATA_WIDTH does not generate integrity fail.</p> <p>* $CRU_OUTS_DATA_WIDTH = 1 + 1 + P_T_SDataWdth_6B + P_CP + P_P_ST_3B*16 + 1 + P_P_ST_3B*2 + 1 + [7+1] + 1 + 1 + 1 + P_P_SR_3B*16 + P_P_ST_3B*2 + 1 + 1 + [8+1] + [4+1] + [4+1] + 1 + 1 + [4+1] + [7+1] + [7+1] + 1 + 1 [=238 \text{ in asf used configuration}]$.</p>

19.3.75 UFS_MAG_NUM Register (Offset = 1100h) [reset = 0005040Ah]

UFS_MAG_NUM is shown in [Figure 19-99](#) and described in [Table 19-228](#).

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Magic Number Register

Table 19-227. UFS_MAG_NUM Instances

Instance	Physical Address
UFS	04E8 5100h

Figure 19-99. UFS_MAG_NUM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAG_NUM																															
R-0005040Ah																															

LEGEND: R = Read Only; -n = value after reset

Table 19-228. UFS_MAG_NUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MAG_NUM	R	0005040Ah	Magic Number

19.3.76 UFS_MPHYSTAT_XCFG01 Register (Offset = 1104h) [reset = 0h]

UFS_MPHYSTAT_XCFG01 is shown in [Figure 19-100](#) and described in [Table 19-230](#).

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Output Debug Bits For PHY 1 Register

Table 19-229. UFS_MPHYSTAT_XCFG01 Instances

Instance	Physical Address
UFS	04E8 5104h

Figure 19-100. UFS_MPHYSTAT_XCFG01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG01																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-230. UFS_MPHYSTAT_XCFG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG01	R	0h	Output debug bits for PHY. This field is read only.

19.3.77 UFS_MPHYSTAT_XCFG02 Register (Offset = 1108h) [reset = 0h]

UFS_MPHYSTAT_XCFG02 is shown in [Figure 19-101](#) and described in [Table 19-232](#).

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Output Debug Bits For PHY 2 Register

Table 19-231. UFS_MPHYSTAT_XCFG02 Instances

Instance	Physical Address
UFS	04E8 5108h

Figure 19-101. UFS_MPHYSTAT_XCFG02 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG02																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-232. UFS_MPHYSTAT_XCFG02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG02	R	0h	Output debug bits for PHY. This field is read only.

19.3.78 UFS_MPHYSTAT_XCFG03 Register (Offset = 110Ch) [reset = 0h]

UFS_MPHYSTAT_XCFG03 is shown in [Figure 19-102](#) and described in [Table 19-234](#).

Return to [Summary Table](#).

Output Debug Bits For PHY 3 Register

Table 19-233. UFS_MPHYSTAT_XCFG03 Instances

Instance	Physical Address
UFS	04E8 510Ch

Figure 19-102. UFS_MPHYSTAT_XCFG03 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG03																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-234. UFS_MPHYSTAT_XCFG03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG03	R	0h	Output debug bits for PHY. This field is read only.

19.3.79 UFS_MPHYSTAT_XCFG04 Register (Offset = 1110h) [reset = 0h]

UFS_MPHYSTAT_XCFG04 is shown in [Figure 19-103](#) and described in [Table 19-236](#).

Return to [Summary Table](#).

Output Debug Bits For PHY 4 Register

Table 19-235. UFS_MPHYSTAT_XCFG04 Instances

Instance	Physical Address
UFS	04E8 5110h

Figure 19-103. UFS_MPHYSTAT_XCFG04 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG04																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-236. UFS_MPHYSTAT_XCFG04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG04	R	0h	Output debug bits for PHY. This field is read only.

19.3.80 UFS_MPHYSTAT_XCFG05 Register (Offset = 1114h) [reset = 0h]

UFS_MPHYSTAT_XCFG05 is shown in [Figure 19-104](#) and described in [Table 19-238](#).

Return to [Summary Table](#).

Output Debug Bits For PHY 5 Register

Table 19-237. UFS_MPHYSTAT_XCFG05 Instances

Instance	Physical Address
UFS	04E8 5114h

Figure 19-104. UFS_MPHYSTAT_XCFG05 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG05																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-238. UFS_MPHYSTAT_XCFG05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG05	R	0h	Output debug bits for PHY. This field is read only.

19.3.81 UFS_MPHYSTAT_XCFG06 Register (Offset = 1118h) [reset = 0h]

UFS_MPHYSTAT_XCFG06 is shown in [Figure 19-105](#) and described in [Table 19-240](#).

Return to [Summary Table](#).

Output Debug Bits For PHY 6 Register

Table 19-239. UFS_MPHYSTAT_XCFG06 Instances

Instance	Physical Address
UFS	04E8 5118h

Figure 19-105. UFS_MPHYSTAT_XCFG06 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG06																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-240. UFS_MPHYSTAT_XCFG06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG06	R	0h	Output debug bits for PHY. This field is read only.

19.3.82 UFS_MPHYSTAT_XCFG07 Register (Offset = 111Ch) [reset = 0h]

UFS_MPHYSTAT_XCFG07 is shown in [Figure 19-106](#) and described in [Table 19-242](#).

Return to [Summary Table](#).

Output Debug Bits For PHY 7 Register

Table 19-241. UFS_MPHYSTAT_XCFG07 Instances

Instance	Physical Address
UFS	04E8 511Ch

Figure 19-106. UFS_MPHYSTAT_XCFG07 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG07																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-242. UFS_MPHYSTAT_XCFG07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG07	R	0h	Output debug bits for PHY. This field is read only.

19.3.83 UFS_MPHYSTAT_XCFG08 Register (Offset = 1120h) [reset = 0h]

UFS_MPHYSTAT_XCFG08 is shown in [Figure 19-107](#) and described in [Table 19-244](#).

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Output Debug Bits For PHY 8 Register

Table 19-243. UFS_MPHYSTAT_XCFG08 Instances

Instance	Physical Address
UFS	04E8 5120h

Figure 19-107. UFS_MPHYSTAT_XCFG08 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG08																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-244. UFS_MPHYSTAT_XCFG08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG08	R	0h	Output debug bits for PHY. This field is read only.

19.3.84 UFS_MPHYSTAT_XCFG09 Register (Offset = 1124h) [reset = 0h]

UFS_MPHYSTAT_XCFG09 is shown in [Figure 19-108](#) and described in [Table 19-246](#).

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Output Debug Bits For PHY 9 Register

Table 19-245. UFS_MPHYSTAT_XCFG09 Instances

Instance	Physical Address
UFS	04E8 5124h

Figure 19-108. UFS_MPHYSTAT_XCFG09 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XCFG09																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-246. UFS_MPHYSTAT_XCFG09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	XCFG09	R	0h	Output debug bits for PHY. This field is read only.

19.3.85 UFS_MPHY_DEBUG_OUT Register (Offset = 1128h) [reset = 60h]

UFS_MPHY_DEBUG_OUT is shown in [Figure 19-109](#) and described in [Table 19-248](#).

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M-PHY Debug Out Register

Table 19-247. UFS_MPHY_DEBUG_OUT Instances

Instance	Physical Address
UFS	04E8 5128h

Figure 19-109. UFS_MPHY_DEBUG_OUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEBUG_OUT																															
R-60h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-248. UFS_MPHY_DEBUG_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DEBUG_OUT	R	60h	MPHY debug out Vendor Debug Output. This field is read only.

19.3.86 UFS_MPHY_BIST Register (Offset = 112Ch) [reset = 0h]

UFS_MPHY_BIST is shown in [Figure 19-110](#) and described in [Table 19-250](#).

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BIST pattern check passed for Lane 0 and Lane 1

Table 19-249. UFS_MPHY_BIST Instances

Instance	Physical Address
UFS	04E8 512Ch

Figure 19-110. UFS_MPHY_BIST Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHY_BIST																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-250. UFS_MPHY_BIST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHY_BIST	R	0h	BIST pattern check passed for Lane 0 and Lane 1. This field is read only.

19.3.87 UFS_MPHY_SF Register (Offset = 1130h) [reset = 0h]

UFS_MPHY_SF is shown in [Figure 19-111](#) and described in [Table 19-252](#).

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Safety Register

Table 19-251. UFS_MPHY_SF Instances

Instance	Physical Address
UFS	04E8 5130h

Figure 19-111. UFS_MPHY_SF Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHY_SF																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-252. UFS_MPHY_SF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHY_SF	R	0h	Safety related. This field is read only.

19.3.88 UFS_MPHYSTAT Register (Offset = 1134h) [reset = 0h]

UFS_MPHYSTAT is shown in [Figure 19-112](#) and described in [Table 19-254](#).

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MPHY Status Register

Table 19-253. UFS_MPHYSTAT Instances

Instance	Physical Address
UFS	04E8 5134h

Figure 19-112. UFS_MPHYSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-254. UFS_MPHYSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved This field is reserved and read only. MPHY Status.

19.3.89 UFS_MPHY_MMIO_A Register (Offset = 1138h) [reset = 0h]

UFS_MPHY_MMIO_A is shown in [Figure 19-113](#) and described in [Table 19-256](#).

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M-PHY Configuration - MMIO Access Register

Table 19-255. UFS_MPHY_MMIO_A Instances

Instance	Physical Address
UFS	04E8 5138h

Figure 19-113. UFS_MPHY_MMIO_A Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							MMIO_A
R/W-0h							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-256. UFS_MPHY_MMIO_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved This field is reserved and read-write. MPHY Configuration.
0	MMIO_A	R/W	0h	This bit is read-write. Enable MPHY MMIO access.

19.3.90 UFS_MPHYCFG_XCFGD1 Register (Offset = 113Ch) [reset = 0h]

UFS_MPHYCFG_XCFGD1 is shown in [Figure 19-114](#) and described in [Table 19-258](#).

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M-PHY Configuration For Digital Part 1 Register

Table 19-257. UFS_MPHYCFG_XCFGD1 Instances

Instance	Physical Address
UFS	04E8 513Ch

Figure 19-114. UFS_MPHYCFG_XCFGD1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGD1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-258. UFS_MPHYCFG_XCFGD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGD1	R/W	0h	This field is read-write. MPHY Configuration for digital part.

19.3.91 UFS_MPHYCFG_XCFGD2 Register (Offset = 1140h) [reset = 0h]

UFS_MPHYCFG_XCFGD2 is shown in [Figure 19-115](#) and described in [Table 19-260](#).

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M-PHY Configuration For Digital Part 2 Register

Table 19-259. UFS_MPHYCFG_XCFGD2 Instances

Instance	Physical Address
UFS	04E8 5140h

Figure 19-115. UFS_MPHYCFG_XCFGD2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGD2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-260. UFS_MPHYCFG_XCFGD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGD2	R/W	0h	This field is read-write. MPHY Configuration for digital part.

19.3.92 UFS_MPHYCFG_XCFGD3 Register (Offset = 1144h) [reset = 0h]

UFS_MPHYCFG_XCFGD3 is shown in [Figure 19-116](#) and described in [Table 19-262](#).

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M-PHY Configuration For Digital Part 3 Register

Table 19-261. UFS_MPHYCFG_XCFGD3 Instances

Instance	Physical Address
UFS	04E8 5144h

Figure 19-116. UFS_MPHYCFG_XCFGD3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGD3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-262. UFS_MPHYCFG_XCFGD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGD3	R/W	0h	This field is read-write. MPHY Configuration for digital part.

19.3.93 UFS_MPHYCFG_XCFGD4 Register (Offset = 1148h) [reset = 0h]

UFS_MPHYCFG_XCFGD4 is shown in [Figure 19-117](#) and described in [Table 19-264](#).

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M-PHY Configuration For Digital Part 4 Register

Table 19-263. UFS_MPHYCFG_XCFGD4 Instances

Instance	Physical Address
UFS	04E8 5148h

Figure 19-117. UFS_MPHYCFG_XCFGD4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGD4																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-264. UFS_MPHYCFG_XCFGD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGD4	R/W	0h	This field is read-write. MPHY Configuration for digital part.

19.3.94 UFS_MPHYCFG_XCFGD5 Register (Offset = 114Ch) [reset = 0h]

UFS_MPHYCFG_XCFGD5 is shown in [Figure 19-118](#) and described in [Table 19-266](#).

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M-PHY Configuration For Digital Part 5 Register

Table 19-265. UFS_MPHYCFG_XCFGD5 Instances

Instance	Physical Address
UFS	04E8 514Ch

Figure 19-118. UFS_MPHYCFG_XCFGD5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											MPHYCFG_XCFGD5				
R/W-0h											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-266. UFS_MPHYCFG_XCFGD5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved This field is reserved and read-write. MPHY Configuration.
4-0	MPHYCFG_XCFGD5	R/W	0h	This field is read-write. MPHY Configuration for digital part.

19.3.95 UFS_MPHYCFG_XCFGA1 Register (Offset = 1150h) [reset = 0h]

UFS_MPHYCFG_XCFGA1 is shown in [Figure 19-119](#) and described in [Table 19-268](#).

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M-PHY Configuration For Analog Part 1 Register

Table 19-267. UFS_MPHYCFG_XCFGA1 Instances

Instance	Physical Address
UFS	04E8 5150h

Figure 19-119. UFS_MPHYCFG_XCFGA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-268. UFS_MPHYCFG_XCFGA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA1	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.96 UFS_MPHYCFG_XCFGA2 Register (Offset = 1154h) [reset = 0h]

UFS_MPHYCFG_XCFGA2 is shown in [Figure 19-120](#) and described in [Table 19-270](#).

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M-PHY Configuration For Analog Part 2 Register

Table 19-269. UFS_MPHYCFG_XCFGA2 Instances

Instance	Physical Address
UFS	04E8 5154h

Figure 19-120. UFS_MPHYCFG_XCFGA2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-270. UFS_MPHYCFG_XCFGA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA2	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.97 UFS_MPHYCFG_XCFGA3 Register (Offset = 1158h) [reset = 0h]

UFS_MPHYCFG_XCFGA3 is shown in [Figure 19-121](#) and described in [Table 19-272](#).

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M-PHY Configuration For Analog Part 3 Register

Table 19-271. UFS_MPHYCFG_XCFGA3 Instances

Instance	Physical Address
UFS	04E8 5158h

Figure 19-121. UFS_MPHYCFG_XCFGA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-272. UFS_MPHYCFG_XCFGA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA3	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.98 UFS_MPHYCFG_XCFGA4 Register (Offset = 115Ch) [reset = 0h]

UFS_MPHYCFG_XCFGA4 is shown in [Figure 19-122](#) and described in [Table 19-274](#).

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M-PHY Configuration For Analog Part 4 Register

Table 19-273. UFS_MPHYCFG_XCFGA4 Instances

Instance	Physical Address
UFS	04E8 515Ch

Figure 19-122. UFS_MPHYCFG_XCFGA4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA4																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-274. UFS_MPHYCFG_XCFGA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA4	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.99 UFS_MPHYCFG_XCFGA5 Register (Offset = 1160h) [reset = 0h]

UFS_MPHYCFG_XCFGA5 is shown in [Figure 19-123](#) and described in [Table 19-276](#).

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M-PHY Configuration For Analog Part 5 Register

Table 19-275. UFS_MPHYCFG_XCFGA5 Instances

Instance	Physical Address
UFS	04E8 5160h

Figure 19-123. UFS_MPHYCFG_XCFGA5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA5																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-276. UFS_MPHYCFG_XCFGA5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA5	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.100 UFS_MPHYCFG_XCFGA6 Register (Offset = 1164h) [reset = 0h]

UFS_MPHYCFG_XCFGA6 is shown in [Figure 19-124](#) and described in [Table 19-278](#).

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M-PHY Configuration For Analog Part 6 Register

Table 19-277. UFS_MPHYCFG_XCFGA6 Instances

Instance	Physical Address
UFS	04E8 5164h

Figure 19-124. UFS_MPHYCFG_XCFGA6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA6																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-278. UFS_MPHYCFG_XCFGA6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA6	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.101 UFS_MPHYCFG_XCFGA7 Register (Offset = 1168h) [reset = 0h]

UFS_MPHYCFG_XCFGA7 is shown in [Figure 19-125](#) and described in [Table 19-280](#).

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M-PHY Configuration For Analog Part 7 Register

Table 19-279. UFS_MPHYCFG_XCFGA7 Instances

Instance	Physical Address
UFS	04E8 5168h

Figure 19-125. UFS_MPHYCFG_XCFGA7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA7																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-280. UFS_MPHYCFG_XCFGA7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA7	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.102 UFS_MPHYCFG_XCFGA8 Register (Offset = 116Ch) [reset = 0h]

UFS_MPHYCFG_XCFGA8 is shown in [Figure 19-126](#) and described in [Table 19-282](#).

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M-PHY Configuration For Analog Part 8 Register

Table 19-281. UFS_MPHYCFG_XCFGA8 Instances

Instance	Physical Address
UFS	04E8 516Ch

Figure 19-126. UFS_MPHYCFG_XCFGA8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA8																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-282. UFS_MPHYCFG_XCFGA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA8	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.103 UFS_MPHYCFG_XCFGA9 Register (Offset = 1170h) [reset = 0h]

UFS_MPHYCFG_XCFGA9 is shown in [Figure 19-127](#) and described in [Table 19-284](#).

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M-PHY Configuration For Analog Part 9 Register

Table 19-283. UFS_MPHYCFG_XCFGA9 Instances

Instance	Physical Address
UFS	04E8 5170h

Figure 19-127. UFS_MPHYCFG_XCFGA9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA9																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-284. UFS_MPHYCFG_XCFGA9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA9	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.104 UFS_MPHYCFG_XCFGA10 Register (Offset = 1174h) [reset = 0h]

UFS_MPHYCFG_XCFGA10 is shown in [Figure 19-128](#) and described in [Table 19-286](#).

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M-PHY Configuration For Analog Part 10 Register

Table 19-285. UFS_MPHYCFG_XCFGA10 Instances

Instance	Physical Address
UFS	04E8 5174h

Figure 19-128. UFS_MPHYCFG_XCFGA10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA10																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-286. UFS_MPHYCFG_XCFGA10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA10	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.105 UFS_MPHYCFG_XCFGA11 Register (Offset = 1178h) [reset = 0h]

UFS_MPHYCFG_XCFGA11 is shown in [Figure 19-129](#) and described in [Table 19-288](#).

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M-PHY Configuration For Analog Part 11 Register

Table 19-287. UFS_MPHYCFG_XCFGA11 Instances

Instance	Physical Address
UFS	04E8 5178h

Figure 19-129. UFS_MPHYCFG_XCFGA11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA11																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-288. UFS_MPHYCFG_XCFGA11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA11	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.106 UFS_MPHYCFG_XCFGA12 Register (Offset = 117Ch) [reset = 0h]

UFS_MPHYCFG_XCFGA12 is shown in [Figure 19-130](#) and described in [Table 19-290](#).

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M-PHY Configuration For Analog Part 12 Register

Table 19-289. UFS_MPHYCFG_XCFGA12 Instances

Instance	Physical Address
UFS	04E8 517Ch

Figure 19-130. UFS_MPHYCFG_XCFGA12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA12																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-290. UFS_MPHYCFG_XCFGA12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA12	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.107 UFS_MPHYCFG_XCFGA13 Register (Offset = 1180h) [reset = 0h]

UFS_MPHYCFG_XCFGA13 is shown in [Figure 19-131](#) and described in [Table 19-292](#).

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M-PHY Configuration For Analog Part 13 Register

Table 19-291. UFS_MPHYCFG_XCFGA13 Instances

Instance	Physical Address
UFS	04E8 5180h

Figure 19-131. UFS_MPHYCFG_XCFGA13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHYCFG_XCFGA13																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-292. UFS_MPHYCFG_XCFGA13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHYCFG_XCFGA13	R/W	0h	This field is read-write. MPHY Configuration for analog part.

19.3.108 UFS_MPHYCFG_MISC Register (Offset = 1184h) [reset = 0h]

UFS_MPHYCFG_MISC is shown in [Figure 19-132](#) and described in [Table 19-294](#).

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M-PHY MISC Configuration Register

Table 19-293. UFS_MPHYCFG_MISC Instances

Instance	Physical Address
UFS	04E8 5184h

Figure 19-132. UFS_MPHYCFG_MISC Register

31	30	29	28	27	26	25	24
RESERVED	CMN_MPX_EN_MMIO	CMN_MPX_SEL_MMIO	TX0_TEST_15_MMIO	TX1_TEST_15_MMIO			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	REFCLK_NOGATED	REFCLK_FREQ_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
REFCLK_FREQ_SEL	RESERVED	TX_DEEPSTALL_EN	RX_DEEPSTALL_EN	RESERVED	RESERVED	RESERVED	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DEBUG_SEL	DEBUG_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-294. UFS_MPHYCFG_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved This field is reserved and read-write. MPHY Configuration.
29	CMN_MPX_EN_MMIO	R/W	0h	Special debug mode for PLL/CDR
28-26	CMN_MPX_SEL_MMIO	R/W	0h	Special debug mode for PLL/CDR
25	TX0_TEST_15_MMIO	R/W	0h	Special debug mode for PLL/CDR
24	TX1_TEST_15_MMIO	R/W	0h	Special debug mode for PLL/CDR
23-18	RESERVED	R	0h	Reserved This field is reserved and read-write. MPHY Configuration.
17	REFCLK_NOGATED	R/W	0h	This bit is read-write. M31 imprecise reference clocks are not gated in HIBERNATE power state. 0h = Gated 1h = Not Gated

Table 19-294. UFS_MPHYCFG_MISC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-15	REFCLK_FREQ_SEL	R/W	0h	<p>This field is read-write.</p> <p>Reference clock frequency selection.</p> <p>0h = 19.2 MHz</p> <p>1h = 26 MHz</p> <p>2h = Reserved</p> <p>3h = Reserved</p> <p>There are three conditions to use precise reference clock.</p> <p>a) For PHY normal operation in HOST mode, user should know the frequency of output precise reference clock.</p> <p>b) For LS VCO calibration under VENDOR control mode, user should know the frequency of input precise reference clock from automatic test equipment.</p> <p>The precise reference clock input is from REFCLK_PCS_In port when PHY is in HOST mode, and from REFCLK pin when PHY is in DEVICE mode.</p> <p>c) For PHY normal operation in DEVICE mode, user may NOT know the frequency of input precise reference clock from REFCLK pin. User may set this signal to be 0h.</p> <p>PHY will automatically switch correct clock selection internally while m31_HOST_REFCLK_DETECT equals to 1h.</p>
14-13	RESERVED	R	0h	<p>Reserved</p> <p>This field is reserved and read-write. MPHY Configuration.</p>
12	TX_DEEP_STALL_EN	R/W	0h	<p>This bit is read-write.</p> <p>Change M-TX from STALL power mode into DEEP STALL mode to turn off TX PLL.</p> <p>Protocol Layer should only assert and de-assert this signal when M-TX is in STALL power mode.</p> <p>0h = STALL mode.</p> <p>1h = DEEP STALL mode.</p>
11	RX_DEEP_STALL_EN	R/W	0h	<p>This bit is read-write.</p> <p>Change M-RX from STALL power mode into DEEP STALL mode to turn off RX CDR.</p> <p>Protocol Layer should only assert and de-assert this signal when M-RX is in STALL power mode.</p> <p>0h = STALL mode.</p> <p>1h = DEEP STALL mode.</p>
10-7	RESERVED	R	0h	<p>Reserved</p> <p>This field is reserved and read-write. MPHY Configuration.</p>
6-0	DEBUG_SEL	R/W	0h	<p>This field is read-write. Debug signal group selection.</p>

19.3.109 UFS_MPHYCFG_VCONTROL Register (Offset = 1188h) [reset = 0h]

UFS_MPHYCFG_VCONTROL is shown in [Figure 19-133](#) and described in [Table 19-296](#).

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M-PHY VCONTROL Configuration Register

**Table 19-295. UFS_MPHYCFG_VCONTROL
Instances**

Instance	Physical Address
UFS	04E8 5188h

Figure 19-133. UFS_MPHYCFG_VCONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							VCONTROL_L A_SA_SEL
R/W-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				VCONTROL_DEEMP_SEL		VCONTROL	
R/W-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
VCONTROL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-296. UFS_MPHYCFG_VCONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved This field is reserved and read-write. MPHY Configuration.
16	VCONTROL_LA_SA_SEL	R/W	0h	This bit is read-write. TX amplitude selection in VENDOR control mode.
15-12	RESERVED	R	0h	Reserved This field is reserved and read-write. MPHY Configuration.
11-10	VCONTROL_DEEMP_SE L	R/W	0h	This field is read-write. TX deemphasis selection in VENDOR control mode.
9-0	VCONTROL	R/W	0h	This field is read-write. VCONTROL test mode selection.

19.3.110 UFS_MPHY_BIST_CTRLPIN Register (Offset = 118Ch) [reset = 0h]

UFS_MPHY_BIST_CTRLPIN is shown in [Figure 19-134](#) and described in [Table 19-298](#).

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M-PHY BIST Control Pins Register

Table 19-297. UFS_MPHY_BIST_CTRLPIN Instances

Instance	Physical Address
UFS	04E8 518Ch

Figure 19-134. UFS_MPHY_BIST_CTRLPIN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPHY_BIST_CTRLPIN																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-298. UFS_MPHY_BIST_CTRLPIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MPHY_BIST_CTRLPIN	R/W	0h	This field is read-write. Control pins for VENDOR control mode. This is only for vendor internal use.

19.3.111 UFS_MPHY_SF_WD Register (Offset = 1190h) [reset = 0h]

UFS_MPHY_SF_WD is shown in [Figure 19-135](#) and described in [Table 19-300](#).

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M-PHY Safety Related Watch Dog Register

Table 19-299. UFS_MPHY_SF_WD Instances

Instance	Physical Address
UFS	04E8 5190h

Figure 19-135. UFS_MPHY_SF_WD Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					SF_PLL_WATC HDOG_EN_MM IO	SF_CDR0_WAT CHDOG_EN_M MIO	SF_CDR1_WAT CHDOG_EN_M MIO
R/W-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-300. UFS_MPHY_SF_WD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved This field is reserved and RW - MPHY Configuration.
2	SF_PLL_WATCHDOG_E N_MMIO	R/W	0h	This bit is read-write. Safety related, Enable PLL Watch Dog.
1	SF_CDR0_WATCHDOG_ EN_MMIO	R/W	0h	This bit is read-write Safety related, Enable CDR Watch Dog.
0	SF_CDR1_WATCHDOG_ EN_MMIO	R/W	0h	This bit is read-write Safety related, Enable CDR Watch Dog.

19.4 UFS0_SYSCFG_SS_CFG Registers

[Table 19-302](#) lists the memory-mapped registers for the UFS0_SYSCFG_SS_CFG registers. All register offset addresses not listed in [Table 19-302](#) should be considered as reserved locations and the register contents should not be modified.

Table 19-301. UFS0_SYSCFG_SS_CFG Instances

Instance	Base Address
UFS0_SYSCFG_SS_CFG	04E8 0000h

Table 19-302. UFS0_SYSCFG_SS_CFG Registers

Offset	Acronym	Register Name	UFS0_SYSCFG_SS_CFG Physical Address
0h	UFS_SS_PID	Revision Register	04E8 0000h

Table 19-302. UFS0_SYSCFG_SS_CFG Registers (continued)

Offset	Acronym	Register Name	UFS0_SYSCFG_SS_CFG Physical Address
4h	UFS_SS_CTRL	Control Register	04E8 0004h

19.4.1 UFS_SS_PID Register (Offset = 0h) [reset = 68556100h]

UFS_SS_PID is shown in [Figure 19-136](#) and described in [Table 19-304](#).

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The Revision Register contains the major and minor revisions for the module.

Table 19-303. UFS_SS_PID Instances

Instance	Physical Address
UFS0	04E8 0000h

Figure 19-136. UFS_SS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-855h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-Ch					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 19-304. UFS_SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Register Scheme
29-28	BU	R	2h	Business Unit: 2h = Processors
27-16	MODULE_ID	R	855h	Module ID
15-11	RTL	R	Ch	RTL Revision
10-8	MAJOR	R	1h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor Revision

19.4.2 UFS_SS_CTRL Register (Offset = 4h) [reset = 0h]

UFS_SS_CTRL is shown in [Figure 19-137](#) and described in [Table 19-306](#).

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The Control Register contains general control bits for the module.

Table 19-305. UFS_SS_CTRL Instances

Instance	Physical Address
UFS0	04E8 0004h

Figure 19-137. UFS_SS_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		MPHY_REFCLK_FREQ_SEL		MPHY_VCONTROL_DEEMP_SE L		MPHY_VCONT ROL_LA_SA_S EL	RST_N_PCS
R-0h		R/W-0h		R/W-0h		R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-306. UFS_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-4	MPHY_REFCLK_FREQ_SEL	R/W	0h	Reference Clock Frequency Selection 0h = 19.2 MHz 1h = 26 MHz 2h = Reserved 3h = Reserved
3-2	MPHY_VCONTROL_DEE MP_SEL	R/W	0h	M-PHY De-Emphasis Select 0h = No De-Emphasis 1h = De-Emphasis
1	MPHY_VCONTROL_LA_ SA_SEL	R/W	0h	M-PHY Amplitude Select 0h = Small Amplitude 1h = Large Amplitude
0	RST_N_PCS	R/W	0h	Active Low Reset to UFS Slave Device

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